Frequency Synthesizer and Mixer Design for 5G (26 GHz) Communication Systems

by

Mir Hassan Mahmud

Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfillment of
the requirements for the degree of
Master of Science

Sabancı University

Summer, 2020

Frequency Synthesizer and Mixer Design
for 5G (26 GHz) Communication Systems

APPROVED BY

Prof. Dr. Yaşar GÜRBÜZ .....
(Thesis Supervisor)

Asst. Prof. Dr. Ömer CEYLAN .....

Assoc. Prof. Dr. Serkan TOPALOĞLU .....

DATE OF APPROVAL: 26/08/2020

© Mir Hassan Mahmud 2020

All Rights Reserved

Acknowledgements

This thesis is the culmination of two years of work that I have done under the supervision of Prof. Yaşar Gürbüz at the Sabanci University Microelectronics Research (SUMER) group. Prof. Gürbüz has been instrumental in my development as a researcher, and I would like to express my sincerest gratitude for his invaluable advice and guidance during my master's studies.

I am very grateful towards my thesis jury members, Asst. Prof. Ömer Ceylan and Assoc. Prof. Serkan Topaloğlu for taking the time to serve on my thesis committee. Their valuable comments and feedback improved this thesis considerably.

At SUMER, I had the great pleasure of working with a group of highly motivated, knowledgeable, and supportive researchers. I would like to thank Dr. Melik Yazıcı, Dr. Can Çalışkan, Işık Berke Güngör, Tahsin Alper Özkan, Hamza Kandiş, Cerin Ninan Kunnatharayil, and Umut Barış Göğebakan for their support and friendship. Special thanks to Abdurrahman Burak for his assistance throughout my master's studies and especially during my first tape-out. I would also like to thank SUMER alumni Dr. İlker Kalyoncu, Elif Gül Arsoy, Dr. Atia Shafique, and Dr. Shahbaz Abbasi. My thanks to Mr. Ali Kasal, the laboratory specialist, who was always there to provide any technical assistance.

I would not have reached this stage in my career without the unconditional love and support that I have received from my family. I will always remain indebted to my family for the sacrifices that they have made for me. So, to my mother Shaiara, to my father Zakir, and to my brother Zaheen - thank you for everything.

Frequency Synthesizer and Mixer Design for 5G (26 GHz) Communication Systems

Mir Hassan Mahmud
EE, Master's Thesis, 2020
Thesis Supervisor: Prof. Dr. Yaşar GÜRBÜZ

Keywords:Beamformer, 5G, SiGe BiCMOS, Downconversion Mixer, VCO, PLL, Integrated Circuits.

Abstract

Next generation 5G wireless mobile communications systems aim to address the increased demands for high data rates by utilizing the large bandwidths available at mmWave frequencies such as the 26 GHz band (24.25 – 27.5 GHz). Directive communications using highly directive beams will become proliferated at these frequencies in order to overcome the increased path loss at mmWave frequencies. Beamforming technology is poised to find widespread adoption for directive communications. Beamforming transceivers require frequency translation from high frequencies to baseband and vice-versa. The frequency translation is performed using mixers and frequency synthesizers. In this thesis, the design of high linearity downconversion mixers suitable for 5G (26 GHz) beamforming receivers is investigated. The design of frequency synthesizers that provide the LO signal for mixers and are required for frequency translation in transceivers is also investigated. The building blocks for an integer-N 4th order type-II PLL is designed for 26 GHz 5G frequency synthesis applications. The designs are realized using IHP's 0.13 μm SiGe BiCMOS technology.

The presented high linearity Gilbert-cell active downconversion mixer is fully integrated with power combiners and baluns and hence is suitable for beamforming applications. The mixer achieves an input 1-dB compression level of up to 2.6 dBm while featuring a low conversion loss of 2.5 dB. The mixer consumes 19 mW dc power and occupies an area of 3.18 mm^2. The proposed bias decoupled cross coupled HBT VCO for the PLL is simulated to have a phase noise of -116 dBc/Hz @ 1 MHz offset from a 10.5 GHz carrier while achieving a tuning range of 19% from 9.4 GHz to 11.4 GHz. The PLL has a simulated phase noise of -98 dBc/Hz @ 1MHz offset from a 10.5 GHz carrier and an estimated RMS phase jitter of 301 fs.

5G (26 GHz) İletişim Sistemleri için Frekans Sentezleyici ve Karıştırıcı Tasarımı

Mir Hassan Mahmud
EE, Yüksek Lisans Tezi, 2020
Tez Danışmanı: Prof. Dr. Yaşar GÜRBÜZ

Anahtar Kelimeler: Hüzmeleyici. 5G, SiGe BiCMOS, Aşağı Dönüşüm Karıştırıcı, Voltaj Kontrollü Osilatör, Faz Kilitlemeli Döngü, Entegre Devre

Özet

Yeni nesil 5G kablosuz mobil iletişim sistemleri, 26 GHz bandı (24.25 - 27.5 GHz) gibi milimetre-dalga frekanslarında bulunan geniş bantlarını kullanarak yüksek veri hızları için artan talepleri karşılamayı amaçlamaktadır. Milimetre-dalga frekanslarında artan yol kaybının üstesinden gelmek için yüksek düzeyde yönlendirici ışınlar kullanan yönlendirmeli iletişimler bu frekanslarda çoğalacaktır. Hüzmeleme teknolojisi, yönlendirici iletişimler için yaygın bir şekilde benimsenmeye hazırlanıyor. Hüzmeleyici alıcı-vericiler, yüksek frekanslardan temel banda ve tersi yönde frekans çevrimi gerektirir. Frekans çevirisi, frekans karıştırıcı ve sentezleyiciler kullanılarak gerçekleştirilir. Bu tezde, 5G (26 GHz) hüzmeleyici alıcılar için uygun yüksek doğrusallık aşağı dönüşüm karıştırıcıların tasarımı incelenmiştir. Karıştırıcılar için LO sinyali sağlayan ve alıcı-vericilerde frekans öteleme için gerekli olan frekans sentezleyicilerin tasarımı da incelenmiştir. Bir tam sayı-N 4. derece tip-II Faz Kilitlemeli Döngü için yapı taşları, 26 GHz 5G frekans sentezi uygulamaları için tasarlanmıştır. Tasarımlar, IHP'nin 0,13 μm SiGe BiCMOS teknolojisi kullanılarak gerçekleştirilir.

Sunulan yüksek doğrusallık Gilbert- hücreli aktif aşağı dönüştürme karıştırıcı, güç birleştiriciler ve balunlarla tamamen entegredir ve bu nedenle hüzmeleme uygulamaları için uygundur. Karıştırıcı 2,5 dB'lik düşük bir dönüşüm kaybına sahipken, 2,6 dBm'ye kadar 1 dB'lik giriş sıkıştırma seviyesine ulaşır. Karıştırıcı 19 mW dc güç tüketir ve 3,18 mm^2'lik bir alanı kaplar. Faz Kilitlemeli Döngü için önerilen besleme ayrıştırılmış çapraz bağlı HBT VKO, 9,4 GHz'den 11,4 GHz'e %19'luk bir ayar aralığı elde ederken, 10,5 GHz'lik bir taşıyıcıdan -116 dBc/Hz @ 1 MHz ofset faz gürültüsüne sahip olacak şekilde simüle edilmiştir.

Contents

Acknowledgements **iv**

Abstract **v**

List of Figures **ix**

List of Tables **x**

List of Abbreviations **xii**

1 Introduction **1**
1.1 5G Wireless Communication Systems 1
1.2 Thesis Motivation 6
1.3 Technology Selection 8
1.4 Thesis Organization 9

2 Downconversion Mixers for 5G Applications **10**
2.1 Mixer Fundamentals 10
2.1.1 Mixer Operation in Receivers 10
2.1.2 Mixer Performance Parameters 12
2.1.3 Mixer Architectures 16
2.2 Mixer Design for 5G Phased Array Receiver 19
2.2.1 5G Beamforming Receiver 19
2.2.2 Linearization of Gilbert-Cell based Mixer 23
2.2.3 Emitter Degenerated Gilbert-Cell Mixer Design 30
2.2.4 Balun Loaded Gilbert-Cell Mixer Design 53

3 Frequency Synthesizer for 5G Transceivers **60**
3.1 Approaches to Frequency Synthesis 60
3.2 PLL Fundamentals 61
3.3 PLL for Frequency Synthesis 65
3.3.1 Linear Model of the Type-II PLL 66
3.3.2 PLL design procedure 67
3.4 PLL Sub-block Design 68
3.4.1 VCO Design 69
3.4.2 PFD/CP/LF Design Considerations 82
3.4.3 Frequency Divider Design Considerations 87
3.5 PLL Closed-loop behavioral simulation 89

4 Conclusion & Future Work **91**
4.1 Summary of Work 91
4.2 Future Work 92

APPENDIX A. IHP SG13S 130-nm SiGe BiCMOS Process Overview **94**

APPENDIX B. In-house Flip-chip Bonding Process **95**

APPENDIX C. Mixer Measurement Setup **96**

List of Figures

1 Expected capabilities of 5G communication systems 4
2 Expected use cases of 5G communication systems 4
3 5G Spectrum Allocation 5
4 Directive communication using beamforming 5
5 Propagation loss characteristics of single patch antenna and patch antenna array. 5
6 RF Phase Shifting Receiver 7
7 Insertion Loss and Return Loss of 10 mm long CPW TL on a Rogers RO5870 PCB 7
8 Downconversion mixer in the RX path 11
9 Mixer conversion gain definition 13
10 Illustration of mixer noise figure 13
11 Illustration of mixer linearity metrics 15
12 Mixer port-to-port isolation definition 15
13 Mixer architectures based on port types 16
14 Transistor-level implementations of different mixer architectures . . . 18
15 Beamformer sub-blocks 20
16 4×4 phased array beamforming receiver 20
17 The Gilbert-Cell mixer: transistor level (top) and functional block (bottom) 23
18 Gilbert-cell half circuit 24
19 Switching waveform commutating I_{RF} 24
20 Gilbert-cell CG simulation results 26
21 HBT differential pair with emitter degeneration 27
22 HBT differential pair IP_3 variation with L_E 29
23 Overview of downconversion mixer 30
24 Schematic of the designed emitter-degenerated Gilbert-cell mixer . . . 31
25 Bias dependence of NF_{min} of minimum sized HBT at 26 GHz 33
26 $\mathrm{IP_{1dB}}$, CG, and NF variation with L_E 34
27 Ideal balun block diagram 36
28 Balun used at the mixer RF port 37
29 RF balun simulation results 38
30 Balun used at the mixer IF port - primary coil (top), secondary coil (middle), and overall balun structure (bottom) 39
31 IF balun simulation results 40
32 Wilkinson Power Divider/Combiner 41
33 Four-way WPC simulated S-parameters 43
34 3-D view of low pass filter at IF 44
35 Low pass filter simulation results 45
36 Mixer layout and chip micrograph 46
37 Mixer flip-chip bonded for measurement 47
38 Measured and simulated CG vs. RF frequency 48
39 Measured and simulated CG vs. LO power for 26 GHz RF 48
40 Measured and simulated CG vs. RF input power for 26 GHz RF . . . 49
41 Measured and simulated $\mathrm{IP_{1dB}}$ vs. RF frequency 49
42 Mixer port matching 50

43 Mixer port-to-port isolation . . . 51
44 Two-way Wilkinson Power Combiner measured and simulated results 52
45 Schematic of the designed balun loaded Gilbert-cell mixer . . . 54
46 3-D view of the balun used at the IF output of the balun loaded Gilbert-cell mixer . . . 55
47 Balun loaded Gilbert-cell mixer layout and chip micrograph . . . 56
48 Balun loaded mixer CG vs. RF frequency variation . . . 57
49 Balun loaded mixer IP_{1dB} vs. RF frequency variation . . . 57
50 Balun loaded mixer simulated CG vs. RF input power . . . 58
51 A conceptual PLL (top) and a Type-I PLL (bottom) . . . 61
52 Type-II PLL . . . 63
53 Fractional-N PLL . . . 64
54 Sliding-IF transceiver . . . 65
55 Linear model of Type-II PLL in phase domain . . . 66
56 LC resonator with parasitics . . . 69
57 Bias decoupled HBT VCO . . . 72
58 Layout of bias decoupled HBT VCO for 18 GHz operation . . . 73
59 Phase noise vs. frequency of VCO for 18 GHz operation . . . 73
60 Various inductor structures studied for VCO resonator . . . 74
61 Quality factor of the inductors under investigation . . . 75
62 Quality factor of the varactor under investigation . . . 76
63 VCO for frequency synthesizer . . . 77
64 Varactor tuning characteristic . . . 77
65 Tail current under varying mirror supply across process corners . . . 78
66 VCO tuning curves . . . 79
67 Close-in VCO phase noise . . . 79
68 Far-out VCO phase noise . . . 81
69 Tri-state PFD . . . 82
70 Behavioral transfer function of the PFD . . . 83
71 Source switched charge pump . . . 83
72 Behavioral CP output for different PFD outputs . . . 84
73 Third-order passive loop filter . . . 85
74 Loop filter transfer function . . . 86
75 Bode plot of PLL open-loop transfer function . . . 86
76 Static frequency divider . . . 88
77 Emitter Coupled Logic Latch . . . 88
78 Frequency divide by two output . . . 89
79 Estimated step response of PLL . . . 89
80 Estimated phase noise of PLL . . . 90
81 Future integration of frequency synthesizer with sliding-IF transceiver 92
82 IHP SG13S Process cross-section . . . 93
83 f_T vs. collector current density of HBT . . . 94
84 Cross-section of flip-chip bonded IC . . . 95
85 Mixer measurement setup . . . 97

List of Tables

1 Evolution of Mobile Communication Systems 3
2 IC technology performance metric comparison 8
3 Design specifications for the downconversion mixer to be used in the 5G beamforming receiver 22
4 Comparison of 5G Downconversion Mixers 53
5 Downconversion Mixer Performance Comparison 59
6 VCO Performance Comparison 80
7 PLL loop parameters 85

List of Abbreviations

ATT	Attenuator
BEOL	Back End OF Line
BJT	Bipolar Junction Transistor
CG	Conversion Gain
CL	Conversion Loss
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
CP	Charge Pump
CPW	Co-Planar Waveguide
DSB	Double-Sideband
DSP	Digital Signal Processing
ECL	Emitter Coupled Logic
eMBB	enhanced Mobile BroadBand
FET	Field Effect Transistor
FoM	Figure of Merit
GaN	Gallium Nitride
HBT	Heterojunction Bipolar Transistor
IBFD	In-Band Full-Duplex
IC	Integrated Circuit
IF	Intermediate Frequency
IIP_3	Input Third Order Intercept Point
IL	Insertion Loss
IM	Image Frequency
IM_3	Third Order Intermodulation Products
IMT	International Mobile Telecommunications
IoT	Internet-of-Things
IP_{1dB}	Input 1-dB Compression Point
IRR	Image Rejection Ratio
LDO	Low Dropout Regulator
LF	Loop Filter
LNA	Low Noise Amplifier
LO	Local Oscillator
MIM	Metal-Insulator-Metal
NF	Noise Figure
PCB	Printed Circuit Board
PD	Phase Detector
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PM	Phase Margin
PN	Phase Noise
PS	Phase Shifter
PSG	Programmable Signal Generator
Q	Quality Factor
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency

SA	Spectrum Analyzer
SDM	Sigma-Delta Modulator
SiGe	Silicon-Germanium
SSB	Single-Sideband
TL	Transmission Line
TR	Tuning Range
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
VNA	Vector Network Analyzer
WPC	Wilkinson Power Combiner
YIG	Yttrium Iron Garnet

1 Introduction

1.1 5G Wireless Communication Systems

The age of wireless communications was ushered in the late 19th century thanks to the development of the wireless telegraph by Guglielmo Marconi. Ever since then steady development has been made in the field of wireless communications [1], [2]. In the 21st century, wireless communication systems have become ubiquitous and are integral in a wide range of applications. One of the key drivers of innovation in the wireless communications field has been commercial mobile communications. The constant need to increase the speed of mobile communications in conjunction with the need to serve a greater number of users has lead to significant developments in technology.

The development of mobile communication systems are summarized in Table 1 [3]. Starting with the first generation of mobile communication systems, which were introduced in the mid-1980s, there has been a constant increase in the bandwidth available for the users. This increase in the available bandwidth has enabled new services to be introduced which are particularly focused on multimedia rich applications. The increase in performance of mobile communication systems has been enabled by improvements in the modulations and multiple access techniques that were used. Data rates have been increased by increasing the frequency bandwidth allocated for communications.

There is a continued demand for even higher data rates for various media-rich online HD streaming and cloud services. So, next generation (5G) communication systems aim to address this increased demand through the deployment of enhanced Mobile BroadBand (eMBB) services featuring data rates approaching tens of Gbps [4], [5]. The International Mobile Telecommunications (IMT) specified capabilities of 5G are shown in Fig. 1 [6]. It can be seen that the peak user experienced data rate will improve significantly from 10 Mbits/s in LTE-Advanced to 100 Mbits/s in 5G. This improvement will be made in addition to improvements in capacity, connection density, latency, and spectrum and energy efficiency. These improvements will enable the use cases shown in Fig. 2 [6]. These use cases include HD video streaming in crowded areas, closed-loop industrial control, autonomous/semi-autonomous

driving, and the realization of the much awaited Internet-of-Things (IoT) with devices that actually connect to the internet (rather than connect to WiFi routers for example).

To achieve the high data rates 5G will utilize the wide bandwidths available in the mmWave frequency bands. The proposed spectrum allocation for 5G is shown in Fig. 3 [7]. The European 5G mmWave band at 26 GHz has an allocated bandwidth of 3.1 GHz (24.25 GHz - 27.35 GHz) and is the frequency band that the work in this thesis is targeted for. To overcome the path loss at mmWave frequencies beamforming has been proposed as a solution [8].

Beamforming is a directive communication technique. Directive communications become realistic at higher frequencies where antenna arrays are realizable due to the compact size of antennas [9]. These antenna arrays produce narrow beams, shown in Fig. 4, which are used to form beamforming gains [8]. The propagation loss of a single patch antenna at 3 GHz was compared to that of an array at 30 GHz in [8], as shown in Fig. 5. As it can be seen, by utilizing arrays of antennas for both the transmitter and the receiver the propagation loss of a system operating at 30 GHz can be lower than that of a system operating with a single patch antenna at 3 GHz. This advantage of utilizing arrays of antennas at mmWave frequencies has gained a lot of attention recently [10, 11, 12, 13, 14, 15, 16, 17] and beamforming is poised to become one of the core technologies to be utilized in mmWave 5G communications.

Table 1: Evolution of Mobile Communication Systems

Technology	1G	2G	2.5G	3G	4G
Design began	1970	1980	1985	1990	2000
Implementation	1984	1991	1999	2002	2012-2015
Service	Analog voice	Digital voice	High-capacity packets, MMS	High-capacity broadband data	Higher capacity, completely IP, Multimedia
Multiple access	FDMA	TDMA, CDMA	TDMA, CDMA	CDMA	OFDMA
Standards	AMPS, TACS, NMT	CDMA, GSM, PDC	GPRS, EDGE	WCDMA, CDMA2000	Single Standard
Bandwidth	1.9 kbps	14.4 kbps	384 kbps	2 Mbps	200 Mbps
Core network	PSTN	PSTN	PSTN, Packet network	Packet network	Internet

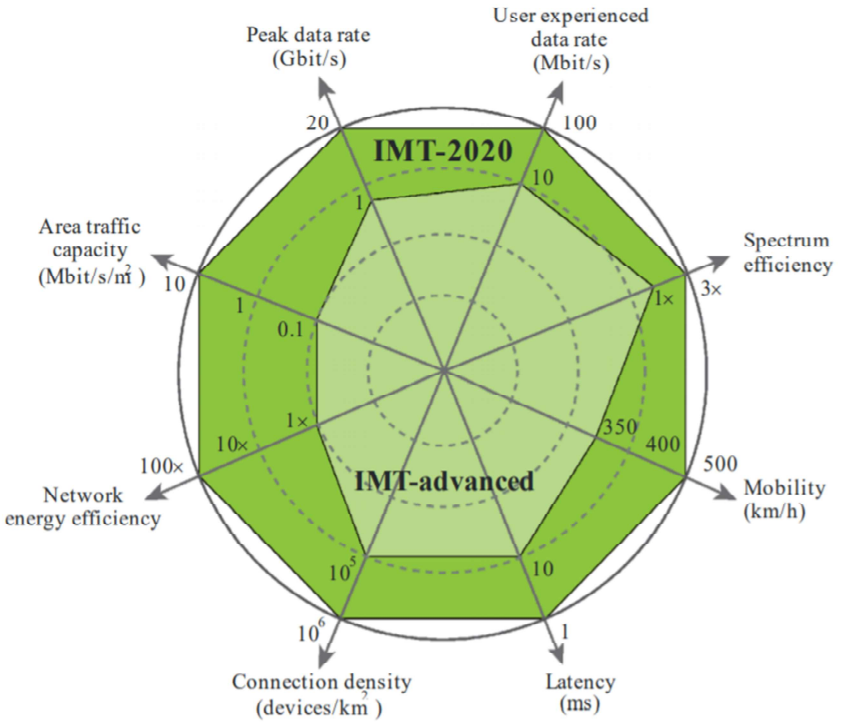


Figure 1: Expected capabilities of 5G communication systems

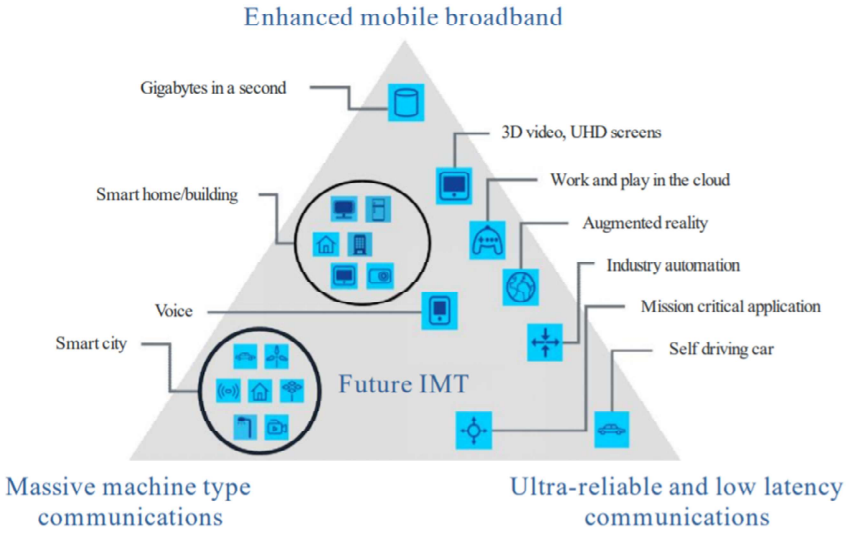


Figure 2: Expected use cases of 5G communication systems

Region	Sub-6 GHz Spectrum							mmWave Spectrum			
	New Band		Existing Band		3GPP Band	Bandwidth (MHz)	Total Bandwidth (MHz)	F_{Low} (GHz)	F_{High} (GHz)	Bandwidth (GHz)	Total Bandwidth (GHz)
	F_{Low} (MHz)	F_{High} (MHz)	F_{Low} (MHz)	F_{High} (MHz)							
Korea	3400	3700				300	300	26.50	29.50	3.00	3.00
European Union	3400	3800	2570 3400	2620 3800	38 42 + 43	50 400	450	24.25 31.80 40.50	27.35 33.40 43.50	3.10 1.60 3.00	7.70
Japan	3600 4400	4200 4900	2496 3400	2690 3600	41 42	194 800 500	1494	27.50	29.50	2.00	2.00
United States	–	–	2496 3550	2690 3700	41 48	194 150	344	27.50 37.00 38.60 64.00	28.35 38.60 40.00 71.00	0.85 1.60 1.40 7.00	10.85
China	3300 4400 4800	3600 4500 4990	2300 2555 3400	2400 2655 3600	40 41B 42	100 100 300 100 190	790	TBD			

Figure 3: 5G Spectrum Allocation

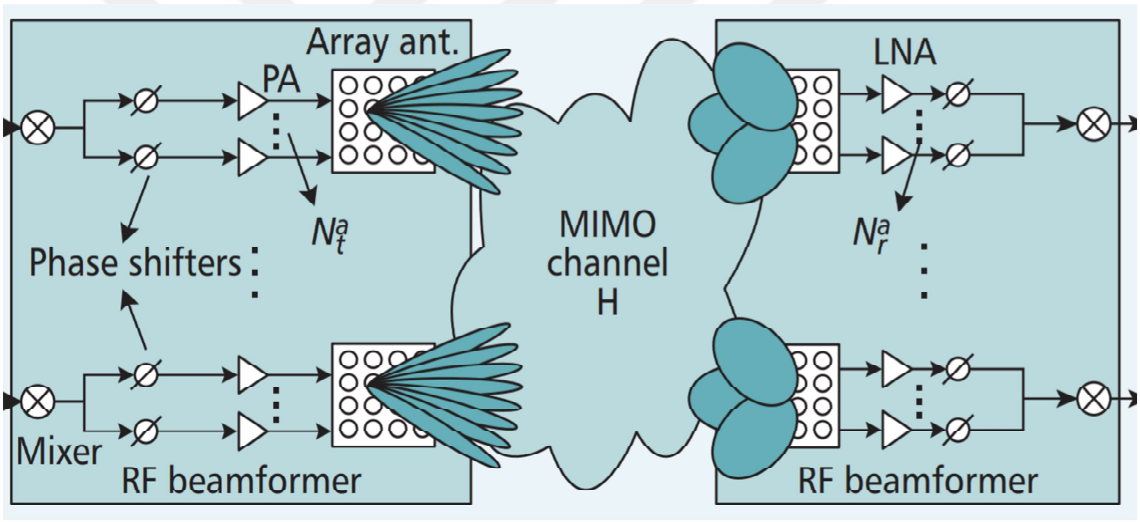


Figure 4: Directive communication using beamforming

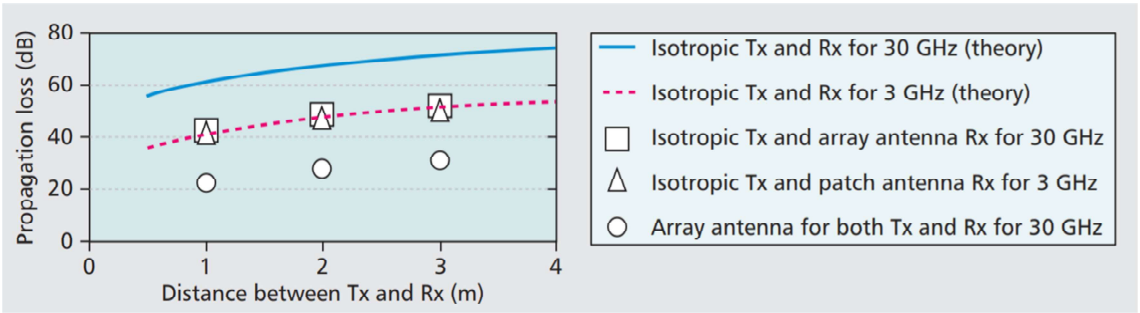


Figure 5: Propagation loss characteristics of single patch antenna and patch antenna array.

1.2 Thesis Motivation

Beamforming systems are composed of transceivers which utilize frequency translation to convert low frequency (baseband) signals to high frequency signals suitable for transmission, and to convert high frequency signals to low frequency signals. Low frequencies are required since the complex digital modulation schemes used in modern communication systems require sophisticated digital signal processing (DSP) schemes which is efficiently performed at these frequencies.

Mixers perform frequency conversion in transceivers. A downconversion mixer is shown in a RF phase shifting receiver in Fig. 6. Each channel of the beamforming receiver is composed of at least a low noise amplifier (LNA) and a phase shifter. Signals from multiple channels are power combined and is then fed to the input of the downconversion mixer. So, the downconversion mixer must exhibit a high linearity to handle the high input power.

The local oscillator (LO) signal that is required by the mixer for downconversion (or upconversion) is generated using a frequency synthesizer. The frequency synthesizer must generate a spectrally pure signal over the required tuning range. This becomes challenging at mmWave frequencies where both active and passive devices typically show degraded performance. In addition to this, the LO signal needs to be routed to many mixers on a large beamforming array. The insertion loss (IL) of a co-planar waveguide (CPW) transmission line (TL) on an printed circuit board (PCB) substrate typically found in RF applications is simulated and the results are shown in Fig. 7. It can be observed that PCB losses become significant at mmWave frequencies and as such high frequency LO routing becomes inefficient.

In this thesis, the design of high linearity downconversion mixers suitable for beamforming receivers are studied. A frequency synthesizer suited for use in a sliding-IF transceiver is also proposed. The proposed frequency synthesis scheme avoids the need for inefficient high frequency LO routing.

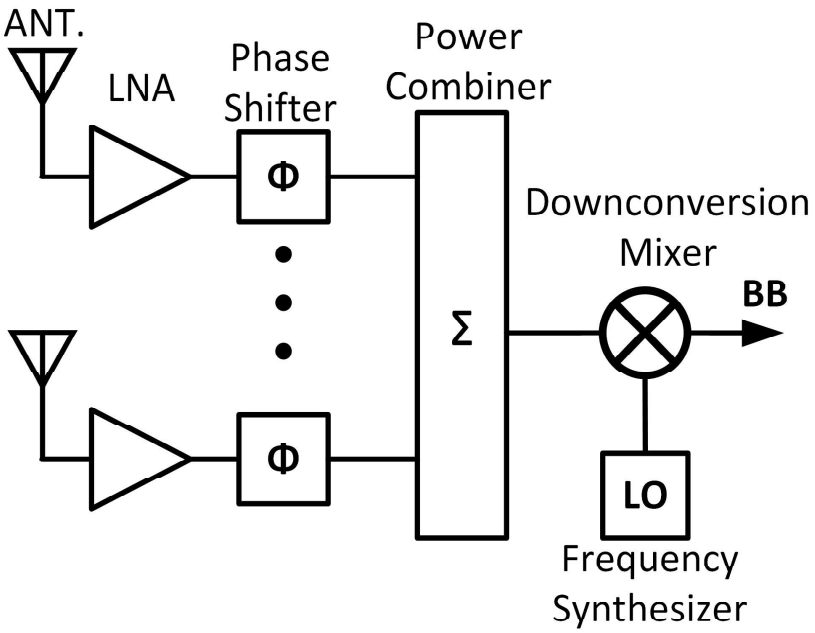


Figure 6: RF Phase Shifting Receiver

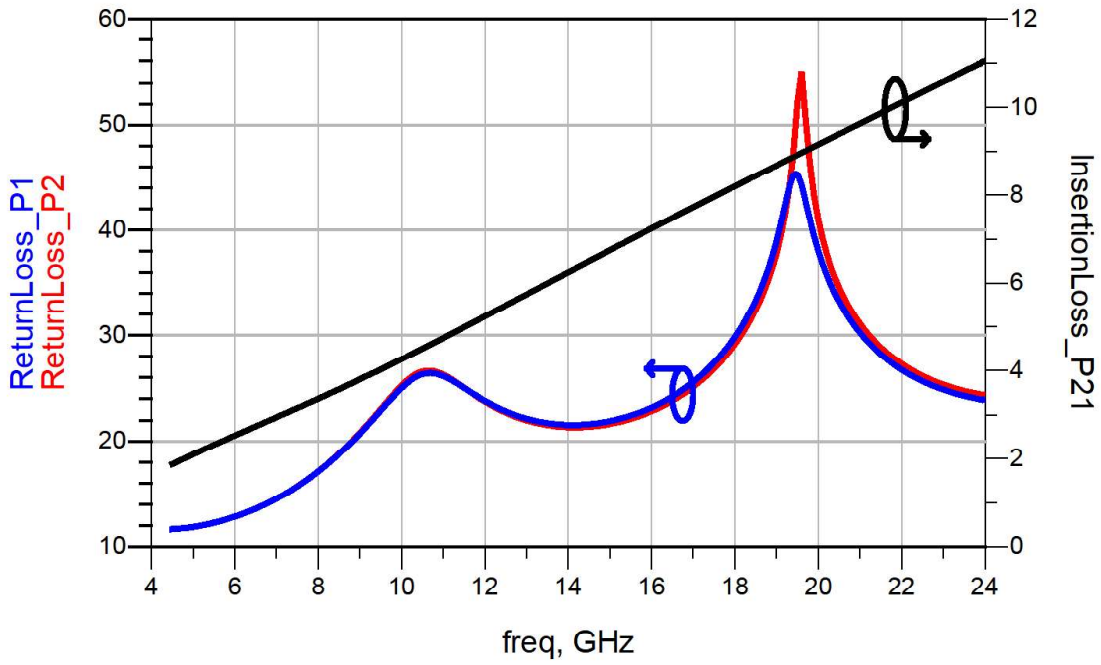


Figure 7: Insertion Loss and Return Loss of 10 mm long CPW TL on a Rogers RO5870 PCB

1.3 Technology Selection

A performance comparison of some common IC technologies is shown in Table 2 [18].

Table 2: IC technology performance metric comparison

Performance Metric	SiGe HBT	Si CMOS	III-V HBT
Frequency Response	Very Good	Good	Excellent
1/f and Phase Noise	Excellent	Fair	Good
Broadband Noise	Very Good	Good	Very Good
Linearity	Very Good	Very Good	Very Good
Output Conductance	Excellent	Fair	Excellent
Transconductance	Excellent	Poor	Excellent
Power Dissipation	Excellent	Fair	Good
CMOS Integration	Excellent	-	Poor
IC Cost	Good	Very Good	Fair

From a purely RF performance point of view both III-V compound semiconductor heterojunction bipolar transistor (HBT) and silicon-germanium (SiGe) HBT offer superior performance when compared to traditional silicon complementary metal oxide semiconductor (CMOS) technologies. This can be seen from the superior frequency response, noise, output conductance, and transconductance of HBTs. Modern III-V technologies such as Gallium Nitride (GaN) also enable very large power handling capabilities. The main disadvantage of III-V technologies is the difficulty in integration with silicon. Silicon CMOS is still the dominant technology for digital applications, and in transceivers where DSP has to be performed, silicon integration remains critical. Additionally, integration with CMOS is also required for digital control of various RF circuit blocks. SiGe HBTs provide an excellent solution for this reason. They offer better RF performance than silicon CMOS and can be fully integrated with silicon CMOS processes. While SiGe does not have the large power handling capabilities of III-V technologies, it more than makes up for it with the CMOS integration advantage. Furthermore, the low 1/f phase noise exhibited by SiGe HBTs make them ideal for the design of low phase noise voltage controlled oscillators (VCO) which is critical for frequency synthesizer's with high spectral purity. The lower voltage swing required for current commutation in SiGe HBTs also make them attractive for designing mixers with low LO drive requirements. So, for

this work a SiGe HBT technology is preferred. IHP's 130-nm SiGe BiCMOS process is selected, since it not only offers high performance HBTs but also CMOS that can be used for digital control circuitry required in the frequency synthesizer design. The details of the IHP SiGe BiCMOS technology can be found in appendix A.

1.4 Thesis Organization

In Chapter 1, an overview of 5G wireless communication systems is provided. The expected requirements and applications of 5G systems are discussed. The motivation behind the studies carried out in this thesis is then stated. Finally. the relevant technology related trade-offs are discussed and the technology selected for this work is justified.

In Chapter 2, the design, simulation, and measurement results of high linearity downconversion mixers for 5G beamforming receivers are discussed. After providing an overview of the fundamentals of mixers, two linearity enhancement techniques are introduced. The inductively degenerated Gilbert-cell mixer and the balun loaded Gilbert-cell mixer are described followed by a comparison with mixers in literature.

In Chapter 3, the design and simulation of the sub-blocks of an integer-N type-II PLL based frequency synthesizer is described. PLL fundamentals are discussed followed by the design considerations for mmWave VCOs. The design of a bias-decoupled HBT VCO with tail current filter and a 4-bit switchable capacitor tank is described. Design of other PLL building blocks are also described. The chapter is concluded with the behavioral level simulation results of the closed-loop PLL.

In Chapter 4, a summary of the work done in this thesis is provided along with the work that is to be carried out in the future.

2 Downconversion Mixers for 5G Applications

This chapter presents the design of high linearity downconversion mixers suitable for 5G phased array beamformers and In-Band Full-Duplex (IBFD) transceivers. The fundamental design aspects of mixers are first discussed. The systems for which the downconversion mixers are intended for are introduced, and then the design of the mixers are described in detail. This is followed by simulation and measurement results. The chapter concludes with a comparison of the presented mixers to comparable works in the existing literature.

2.1 Mixer Fundamentals

2.1.1 Mixer Operation in Receivers

Mixers are required for frequency translation in receivers of communications systems to convert radio frequency (RF) signals to baseband signals. This process of converting high frequency (RF) signals to low frequency signals is known as (frequency) downconversion. This is done to ease the channel selection requirements and to perform signal processing efficiently [19].

Mixers perform the frequency translation using a multiplicative process whereby the RF signal is multiplied by a local oscillator (LO) signal. The generation of the baseband/intermediate frequency (IF) can be shown mathematically as in (1).

$$\begin{aligned} V_{IF}(t) &= \mathrm{LPF}\{V_{RF}(t) \times V_{LO}(t)\} \\ &= \mathrm{LPF}\{A_{RF}\cos(\omega_{RF}t) \times A_{LO}\cos(\omega_{LO}t)\} \\ &= \mathrm{LPF}\{\frac{A_{RF}A_{LO}}{2} \cdot \{\cos[(\omega_{RF}-\omega_{LO})t] + \cos[(\omega_{RF}+\omega_{LO})t]\}\} \\ &= \frac{A_{RF}A_{LO}}{2}\cos[(\omega_{RF}-\omega_{LO})t] \\ \therefore V_{IF}(t) &= A_{IF}\cos(\omega_{IF})t \end{aligned} \tag{1}$$

In (1), LPF is the low-pass filter at the IF output, V_{IF} is the mixer output signal, A_{RF} is the amplitude of the RF signal, A_{LO} is the amplitude of the LO signal, ω_{RF} is the angular frequency of the RF signal, ω_{LO} is the angular frequency of the LO signal, A_{IF} is the amplitude of the output signal at IF, and ω_{IF} is the angular frequency of the output signal at IF.

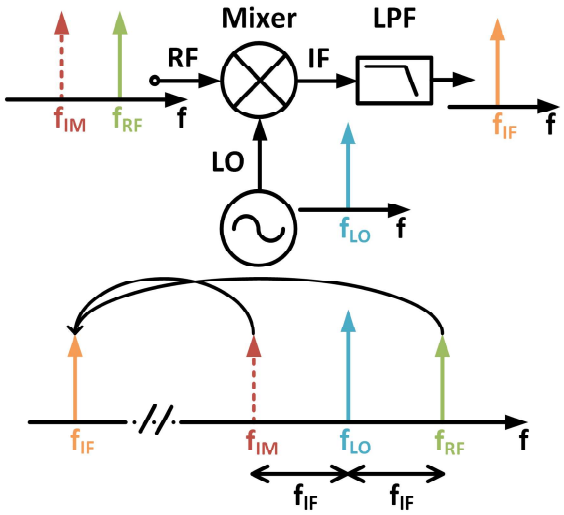


Figure 8: Downconversion mixer in the RX path

The conceptual diagram of a mixer operating within a receiver is shown in Fig. 8. The mixer has three ports, namely the input/RF port, the output/IF port, and the LO port. The low-pass filter, LPF selects the appropriate low frequency component and rejects the high frequency component at the output of the mixer. From Fig. 8 two things can be observed. Firstly, the spacing between the RF and LO signal is IF, i.e. $f_{IF} = f_{RF} - f_{LO}$. Secondly, the downconversion process not only translates the signal at the RF frequency down to IF, but also a frequency that lies IF away from the LO at a lower frequency. This is the image frequency (IM) and needs to be rejected so that the information present in the RF signal can be translated to IF without any corruption. It must be noted that in Fig. 8 it has been assumed that the LO signal is at a lower frequency than the RF signal. This is known as lower-side injection, and is commonly used in mmWave systems where high frequency LO generation is inefficient. Hence lower-side injection downconversion leads to the image frequency to be located at $f_{LO} - f_{IF}$ or equivalently $2f_{LO} - f_{RF}$. If the LO signal is at a higher frequency than the RF signal, then this is known as upper-side injection and leads to an IM frequency to be located at $f_{LO} + f_{IF}$ or equivalently $2f_{LO} - f_{RF}$. The image rejection ratio (IRR) is used to quantify the relative attenuation of the signal at the IM frequency to that at the RF at the mixer input. Image rejection can be performed by placing an image rejection filter at the RF input of the mixer to obtain a certain IRR. A quadrature downconversion architecture may also be utilized for image rejection. The selection of image rejection technique is application dependent,

and will be discussed when the systems, for which the designed mixers are intended for, are described.

2.1.2 Mixer Performance Parameters

Some of the key performance specifications of a mixer are conversion gain (CG), noise figure (NF), linearity, and port-to-port isolation.

The CG of a mixer is a ratio of the power of the desired IF signal at the output to the power of the RF signal at the input as shown in Fig. 9. This is the power conversion gain of the mixer. The voltage conversion gain of the mixer utilizes rms voltage quantities at the output and input of the mixer. If the mixer is matched to identical impedance at both the output and the input, then the two conversion gains are identical. A high CG is desirable in a downconversion mixer since it can then compensate for losses and suppress the noise of the IF chain [20].

There are several mixer noise performance parameters including single-sideband (SSB) NF, double-sideband (DSB) NF, and the IEEE SSB NF. The SSB NF can be explained using Fig. 10a. An ideal mixer which adds no noise during the mixing process will have noise at its output from two different sources - the RF band and the IM band. If the thermal noise contributions of both of these bands to the output are considered to be equal and the CG is equal at both RF and IM frequency bands, then the IF output signal has twice the noise content as the RF input signal. This is defined as the SSB NF, and for a noiseless mixer is 3 dB. SSB NF is typically used for heterodyne receiver architectures where the desired signal lies in only one of the sidebands (RF band). The DSB NF, shown in Fig. 10b, assumes that the signal at the both the upper- and lower- sideband of the LO are the desired signal. In other words, the LO and RF are at the same frequency. In this case there is no extra noise contribution from the IM, and the DSB NF of a noiseless mixer is 0 dB [19]. The DSB NF is typically used in homodyne/direct conversion architectures where the desired signal lies in both the upper- and lower- sidebands.The IEEE SSB NF does not consider the noise at the IM band and hence a noiseless mixer has a NF of 0 dB [21]. The mixer NF definition used in this work is the SSB NF, since heterodyne systems are under consideration. In a receiver chain, the overall noise contributed by the mixer is suppressed by the gain of the blocks preceding the mixer, and in

particular the LNA.

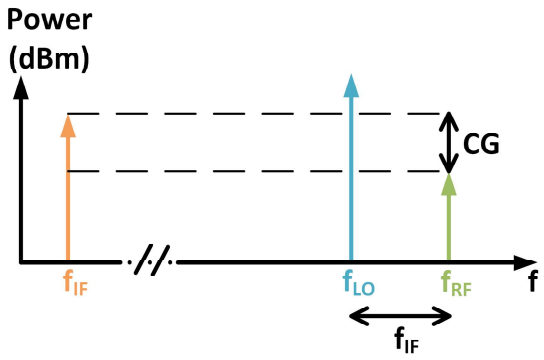
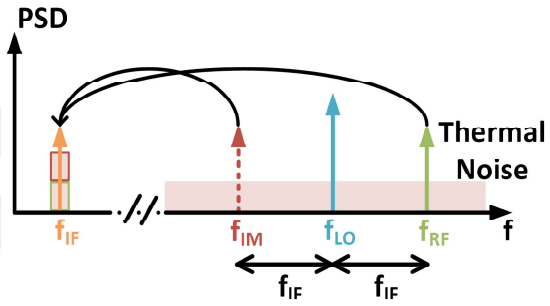
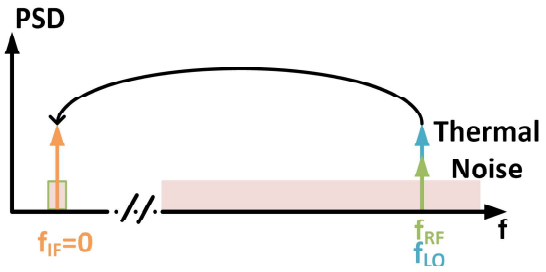


Figure 9: Mixer conversion gain definition



(a) Single-sideband noise figure



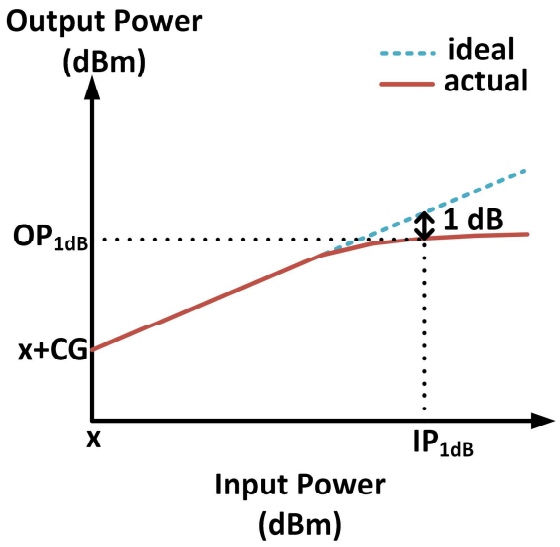
(b) Double-sideband noise figure

Figure 10: Illustration of mixer noise figure

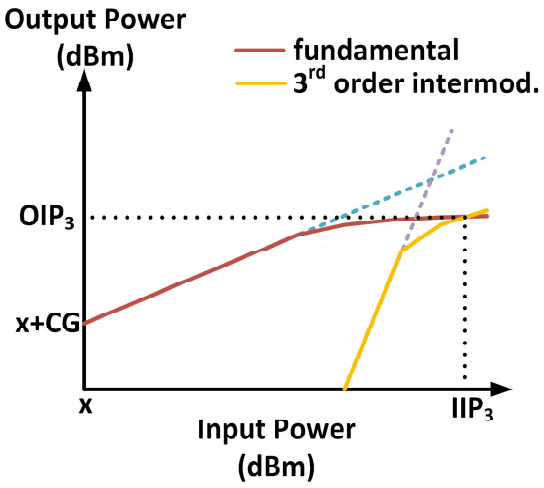
The linearity of a downconversion mixer is measured using two different metrics. The first is the input 1-dB compression point (IP_{1dB}). The IP_{1dB} is the RF input power which leads to a 1 dB drop in the CG of the mixer when compared to the CG under small signal operation, as shown in Fig. 11a. If the input signal is greater than the IP_{1dB} then the output signal has amplitude modulation to phase modulation distortion [20]. This causes errors in modulation schemes such as quadrature amplitude modulation (QAM) where information is carried in the phase as well as in the amplitude. The CG of the mixer may also be compressed in the presence of

a large unwanted signal at a frequency close to the RF frequency [20]. For these reasons a high IP_{1dB} is desirable. The second linearity metric is the input third-order intercept point (IIP_3) shown in Fig. 11b. This is the RF input power at which the power of the third-order intermodulation products have the same power as the fundamental signal. The third-order intermodulation products arise due to device non-linearities when two tones are applied at the input. If the two tones close to the RF band are at f_1 and f_2, then the intermodulation products generated at $2f_1 - f_2$ and $2f_2 - f_1$ will land on the RF band and corrupt the desired signal. The IIP_3 is typically higher than the IP_{1dB}, and if only third-order device non-linearities are considered then the IIP_3 point is 9.6 dB above IP_{1dB}.

The port-to-port isolation of a mixer is a measure of the leakage of signals from one port to another as shown in Fig. 12. The RF-IF isolation is the ratio of the power at the RF frequency present at the IF port to that present at the input RF port. The LO-IF isolation is the ratio of the power at the LO frequency present at the IF port to that present at the LO port. Finally, the LO-RF isolation is the ratio of the power at the LO frequency present at the RF port to that present at the LO port. The aforementioned isolation values are of interest since they are the most significant in integrated mixers and affect the performance of the mixer the most. As shall be seen, the LO signal has the highest power level in a mixer and so any leakage from the LO port to the other ports can corrupt the signals at those ports significantly. So, the LO-RF and LO-IF isolation are of particular importance and high isolation is desired.



(a) 1-dB compression point



(b) Third order intercept point

Figure 11: Illustration of mixer linearity metrics

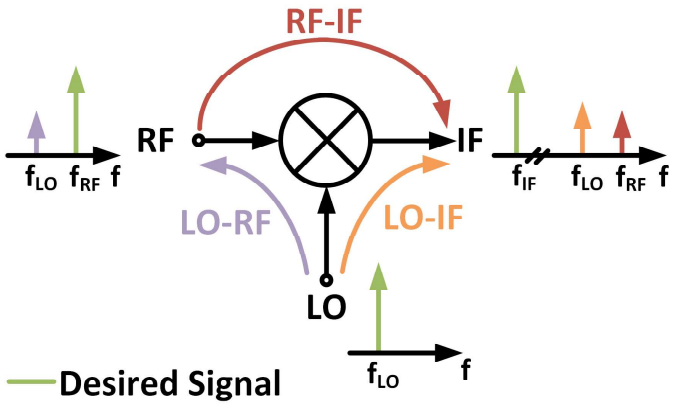
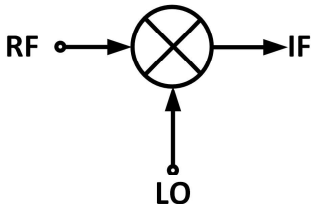
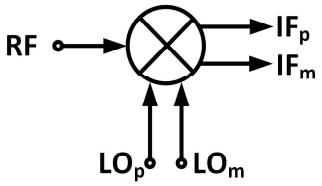


Figure 12: Mixer port-to-port isolation definition

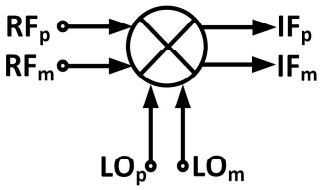
2.1.3 Mixer Architectures



(a) Unbalanced mixer



(b) Single-balanced mixer



(c) Double-balanced mixer

Figure 13: Mixer architectures based on port types

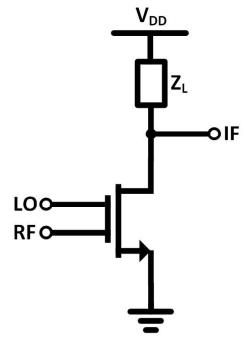
The various mixer architectures present in literature can be categorized as unbalanced, single-balanced or double-balanced, and active or passive.

Mixers are designated as unbalanced, single-balanced, and double-balanced depending on their input and output port types. The unbalanced mixer of Fig. 13a has single-ended RF and LO inputs, and a single-ended IF output. When the LO input is provided differentially, as in Fig 13b, the mixer is termed as single-balanced. In a double-balanced mixer, shown in Fig. 13c, both the RF port and the LO port uses differential/balanced signalling.

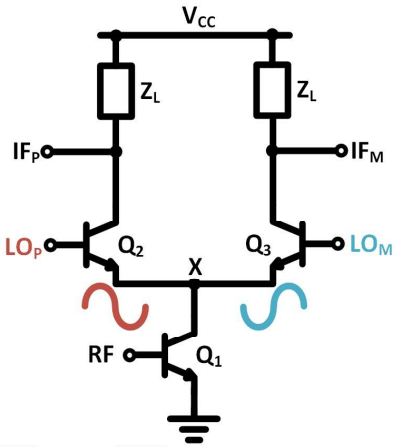
The type of input balance determines the port-to-port isolation of the mixer among other parameters. Example transistor-level implementations of unbalanced, single-balanced, and double-balanced mixers are shown in Fig. 14a, 14b, and 14c respectively. The unbalanced mixer in Fig. 14a uses a dual-gate field effect transistor (FET) for the RF and LO inputs [22]. This can also be performed using a standard FET, bipolar junction transistor (BJT), or heterojunction bipolar transistor and a diplexer. Due to device parasitic capacitances such as the gate-drain capacitance

in FETs or base-collector capacitance in BJTs and HBTs, the LO signal leaks into the IF port. Without a high isolation diplexer, the isolation between the RF and LO ports is also low. So, unbalanced mixers are not suitable for high performance 5G receivers. Fig. 14b shows an implementation of a single-balanced mixer. The differential pair composed of $Q_1 - Q_2$ has a virtual ground at the node labeled X for the LO input. Therefore the LO signal leakage to the RF port is low and hence the LO-RF isolation is high. However, the LO-IF isolation is still low, since the LO signal can leak to the IF port through the base-collector parasitic capacitance. The isolation performance of the single-balanced mixer can be enhanced by adding a second differential pair such that the LO signal also cancels at the IF port. This is the idea behind the double-balanced mixer of Fig. 14c. At each of the IF output nodes, a copy of the LO signal and its complement is present. This cancels out the LO signal at the output and leads to a high LO-IF isolation. The same holds true for the RF leakage to the IF port. So, the RF-IF isolation is also high in addition to the already high LO-RF isolation. From this it can be inferred that double-balanced mixers exhibit the highest port-to-port isolation and unbalanced mixers exhibit the lowest isolation. Single-balanced mixers have an isolation performance in between the two extremes. Additionally, double-balanced mixers can reject the amplitude noise of the LO signal unlike its unbalanced and singled-balanced counterparts [19]. The CG performance of single-balanced and double balanced mixers will be discussed in the following section. The SSB NF of the double-balanced mixer is the highest, since there are a higher number of active devices when compared to a single-balanced mixer [20], and unbalanced mixers have the lowest NF. As shown in [19], the double-balanced mixer exhibits twice the input-referred noise as the single-balanced mixer for a given power budget.

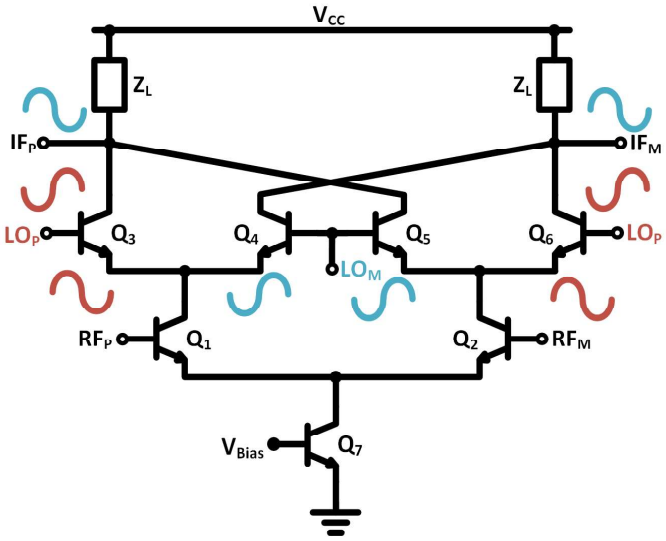
Mixers are designated as passive or active depending on whether or not any amplification occurs using the devices used [19] and in general whether or not a quiescent dc power is consumed when no input signals are present. In passive mixers, the transistors do not provide any amplification and typically do not consume any quiescent dc power. Passive mixers therefore do not provide any CG, but rather a conversion loss (CL). Active mixers on the other hand provide signal amplification using transistors, and consume quiescent dc power. The CG of an active mixer can



(a) Unbalanced mixer



(b) Single-balanced mixer



(c) Double-balanced mixer

Figure 14: Transistor-level implementations of different mixer architectures

be made large at the expense of the linearity of the mixer. Compared to active mixers, the linearity performance of a passive mixer is better. This is because in passive mixers no amplification is provided, and hence a larger input power can be applied before compression occurs. The LO signal swing requirements for passive mixers are typically higher than that required by active mixers. The large LO signal swing is required to ensure proper switching operation of the devices which is fundamental to the mixing process.

2.2 Mixer Design for 5G Phased Array Receiver

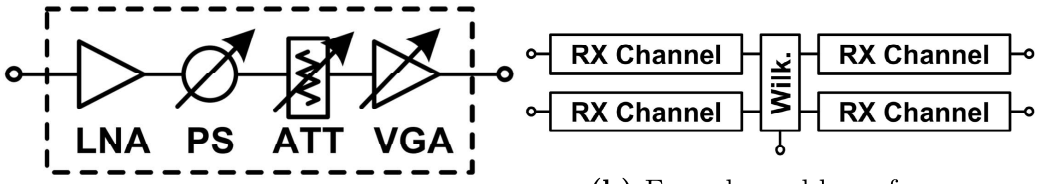
In this section downconversion mixers designed for a 5G phased array beamforming receiver will be presented. The beamformer front-end is described briefly to justify the requirements of the downconversion mixer. The circuit design of three different mixers are then presented along with appropriate simulation and measurement results. The results are then compared with comparable mixers in literature.

2.2.1 5G Beamforming Receiver

Beamforming has been proposed to generate highly directive beams,which can overcome the increased path loss at mmWave frequencies, using antenna arrays [8]. Consequently, there has been a great deal of focus on the design of beamforming transceivers, as demonstrated by [23, 24, 25]. Silicon-based technologies have been selected instead of III-V compound semiconductor technologies for beamformer design due to baseband integration requirements, and Silicon-Germanium (SiGe) in particular offers enhanced gain and noise performance at mmWave frequencies with respect to CMOS technologies [26].

In beamforming receivers, each channel is composed of a gain block - typically a low-noise amplifier (LNA), to suppress the noise of the succeeding blocks as well as to raise the signal power to a level suitable for subsequent processing. The LNA is followed by phase and amplitude control blocks which are used to adjust the beam. Multiple channels are power combined and the RF signal is then input to a mixer for downconversion. A single RX channel and a four-channel beamformer was designed by my colleagues İlker Kalyoncu, Abdurrahman Burak, and Alper Güner at SUMER Lab. These are shown in Fig. 15a and Fig. 15b respectively. The single beamformer

channel is composed of an LNA, a phase shifter (PS), an attenuator (ATT), and a variable gain amplifier (VGA). Four single channels are power combined using a cascaded Wilkinson Power Combiner (WPC) to create a four-channel beamformer. This four-channel beamformer has a simulated gain of 24 dB, noise figure of 3.5 dB, and a input-referred 1-dB compression point of -25 dBm with 200 mW power consumption [27].



(a) Single channel of beamformer

(b) Four-channel beamformer

Figure 15: Beamformer sub-blocks

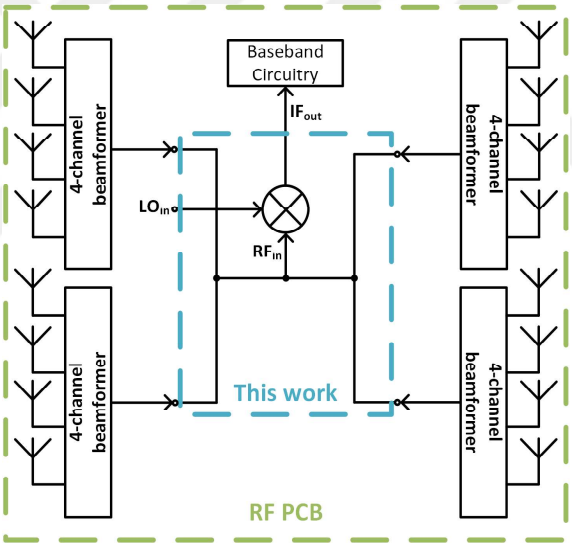


Figure 16: 4×4 phased array beamforming receiver

A 4×4 phased array beamforming receiver was designed using four of the aforementioned four-channel beamformers as shown in Fig. 16. It is envisioned that the four-channel beamformer ICs will be fed by PCB based patch antennas. The beamformer ICs will be flip-chip bonded onto the PCB along with the mixer IC. The outputs of the four beamformers will be routed to the mixer input and then combined at the mixer using a four-way power combiner.The present work will discuss the design of the downconversion mixer with four RF inputs (demarcated in blue in Fig. 16) that is required for such a beamforming receiver.

The primary design target for the mixer is to achieve a high IP_{1dB} since a large RF input power is expected from the 16 combined channels. At the mixer input the combined input power is expected to be around -1 dBm after taking into account the systematic combiner and PCB losses. PCB trace losses of around 2 dB is expected along with 1.5 dB excess loss from each of the power combiners. An IP_{1dB} that is 3 dB greater (2 dBm) is therefore targeted for. Due to the inherent trade-off between CG and linearity, a low CG or even CL is acceptable in this application. Linearity is given a higher priority since the mixer is the final block in the RF chain of the receiver and it affects the overall linearity performance of the receiver. However, the CL of the mixer should not be too high, since the noise contributions from the IF chain will then become significant. The NF of the mixer itself is less critical in this application since the beamformer front end has a large enough gain to greatly suppress the noise added by the mixer. To achieve the high linearity performance a large LO signal will be required to drive the mixer. So, high port-to-port isolations will ensure that both the RF input and IF output signals are not distorted by the LO signal. Finally, a four-way power combiner will be required to combine the inputs from four of the four-channel beamformers.

Since the mixer is targeted for European 5G applications, the RF band is set from 24 GHz to 28 GHz. A high IF of 3 GHz with 500 MHz bandwidth is selected. Lower-side injection is used to ease the generation of the LO signal. With the RF and IF set, the required LO is from 21 GHz to 25 GHz. This sets the IM band to be from 18 GHz to 22 GHz. The high IF relaxes the image rejection requirements due to the inherent narrowband characteristics of the RF front-end and the antennas used in the array [28]. While an integrated image rejection filter could be placed at the input of the mixer after the four-way power combiner, this would occupy a significant area and would introduce additional losses. The narrowband characteristics of the RF front-end is determined to be sufficient for image rejection purposes. Table 3 summarizes the design targets for the downconversion mixer.

Table 3: Design specifications for the downconversion mixer to be used in the 5G beamforming receiver

Specification	Requirement
RF Band	24 GHz - 28 GHz
IF Band	2.75 GHz - 3.25 GHz
LO Band	21 GHz - 25 GHz
CG	> -6 dB
IP1dB	~ 2 dBm
Port-to-port Isolation	> 20 dB

To meet the aforementioned requirements of the downconversion mixer an active double-balanced mixer architecture was selected. An active mixer can be designed to have a low CL while its linearity may be enhanced to meet the specifications. A double-balanced architecture was preferred due to the superior isolation performance as well as the immunity to LO amplitude noise. In this work, active double-balanced mixers are optimized for high linearity performance while maintaining low CL and moderate NF.

2.2.2 Linearization of Gilbert-Cell based Mixer

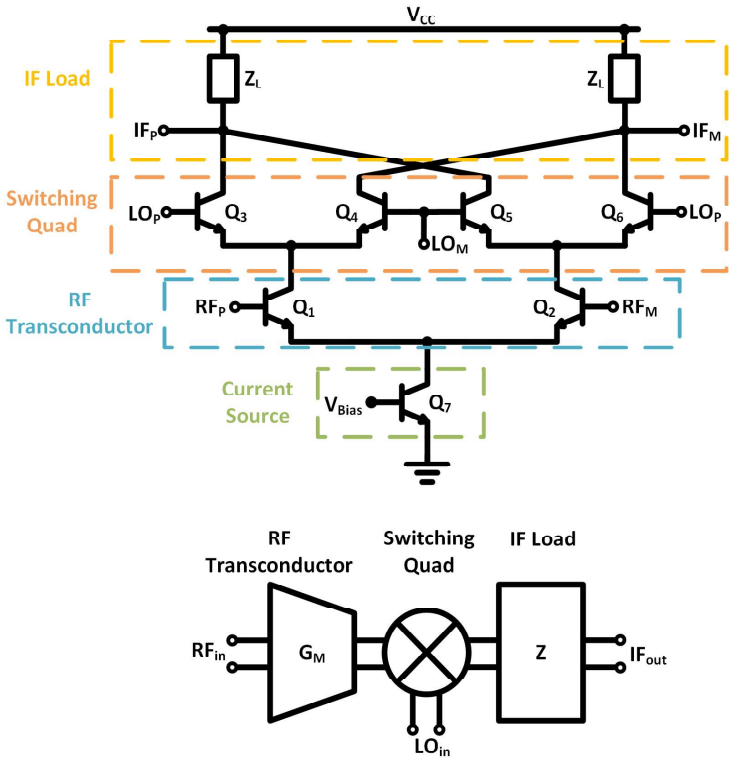


Figure 17: The Gilbert-Cell mixer: transistor level (top) and functional block (bottom)

The Gilbert-cell mixer, shown in Fig. 17, was presented in [29] and then reintroduced in [30]. Conceptually it is composed of three distinct components. The input differential pair composed of the transistors Q_1 and Q_2 along with the tail current source Q_7 act as a transconductance stage. This converts the incoming RF signal voltage into a RF current. The two cross-connected differential pairs composed of transistors $Q_3 - Q_6$ are driven by the LO signal to commutate the RF currents. This has the effect of multiplying the LO signal with the RF signal, and the current generated at the lower beat frequency is converted to an output IF voltage using the load impedance Z_L.

The CG of the Gilbert-cell mixer can be derived by considering the translinear principle in BJT circuits as proposed in [31] or it can be derived conceptually as in [19]. Consider the half circuit of the Gilbert-cell mixer shown in Fig. 18. The differential LO signals commutate the RF current, I_{RF}. This commutation can be represented by the multiplication of the switching waveform shown in Fig. 19 with I_{RF}. Under these conditions the output IF voltage, V_{IF} is given by (2).

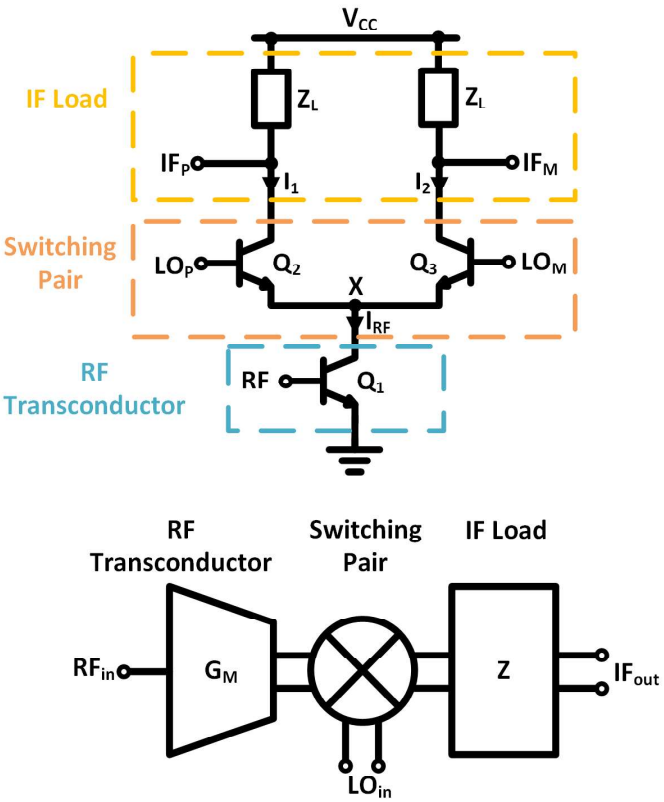


Figure 18: Gilbert-cell half circuit

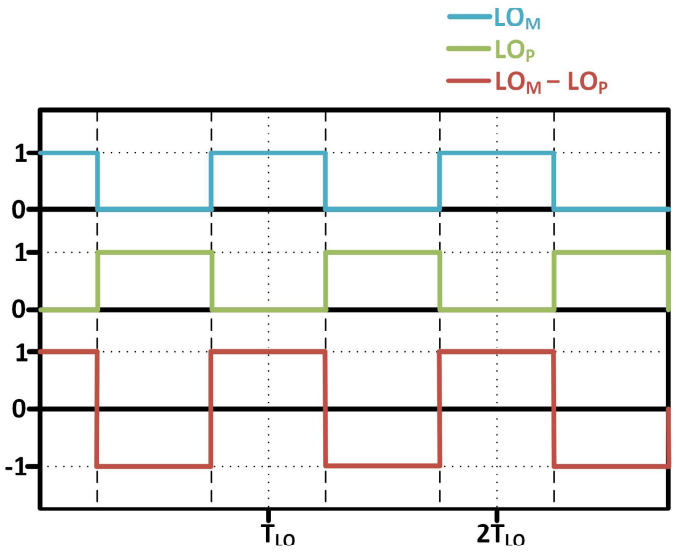


Figure 19: Switching waveform commutating I_{RF}

$$
\begin{aligned}
|V_{IF}| &= |(V_{CC} - I_1 Z_L) - (V_{CC} - I_2 Z_L)| \\
&= |[LO_M - LO_P] I_{RF} Z_L| \\
\therefore |V_{IF}| &= |[LO_M - LO_P] g_{m1} V_{RF} \cos(\omega_{RF} t) Z_L|
\end{aligned} \tag{2}
$$

$$
\mathscr{F}\{LO_M - LO_P\} = \frac{4}{\pi} \sum_{\substack{n=1 \\ \text{n is odd}}}^{\infty} \frac{1}{n} \cos(n\omega_{LO} t)(-1)^{\frac{n+3}{2}} \tag{3}
$$

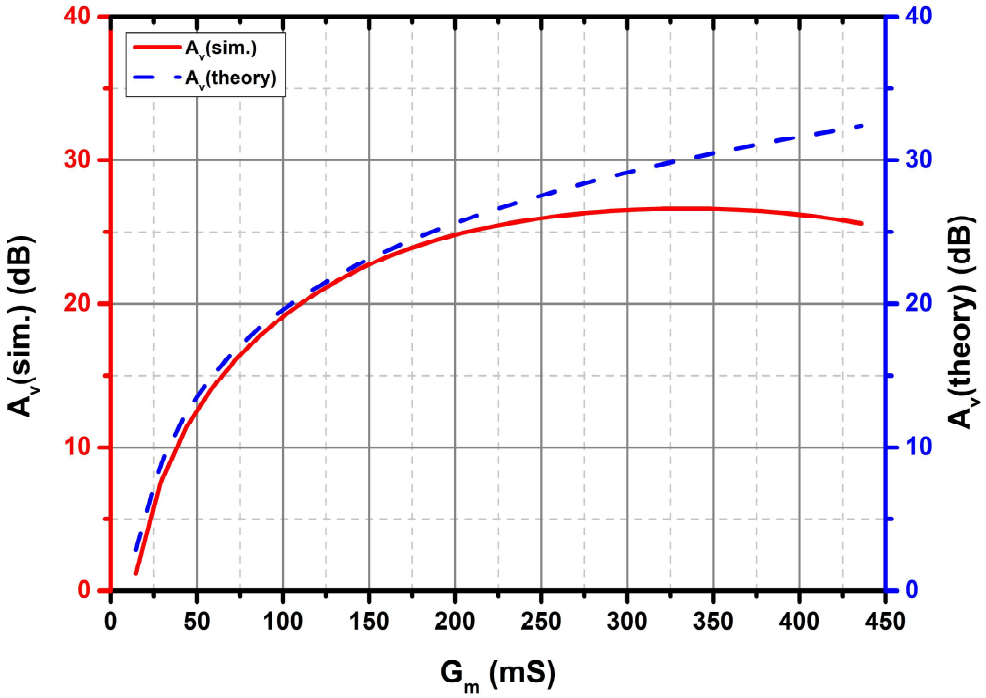
$$
\begin{aligned}
|V_{IF}| &\approx \text{LPF} \left\{ \left| \frac{4}{\pi} \cos(\omega_{LO} t) g_{m1} V_{RF} \cos(\omega_{RF} t) Z_L \right| \right\} \\
&= \left| \frac{4}{\pi} g_{m1} V_{RF} \frac{\cos[(\omega_{RF} - \omega_{RF})t]}{2} Z_L \right| \\
\therefore \left| \frac{V_{IF}}{V_{RF}} \right| &= \left| \frac{2}{\pi} g_{m1} Z_L \right|
\end{aligned} \tag{4}
$$

The Fourier series representation of the difference of the periodic switching waveform is given by (3). The fundamental component of the LO signal (n=1) in (3) mixes with the RF signal to generate the IF signal, as in (4), and the higher order mixing terms are filtered off at the output. From (4) it can be observed that for a Gilbert-cell mixer the CG is dependent on the transconductance $g_{m1,2}$ of the RF input transistors and the load impedance Z_L.

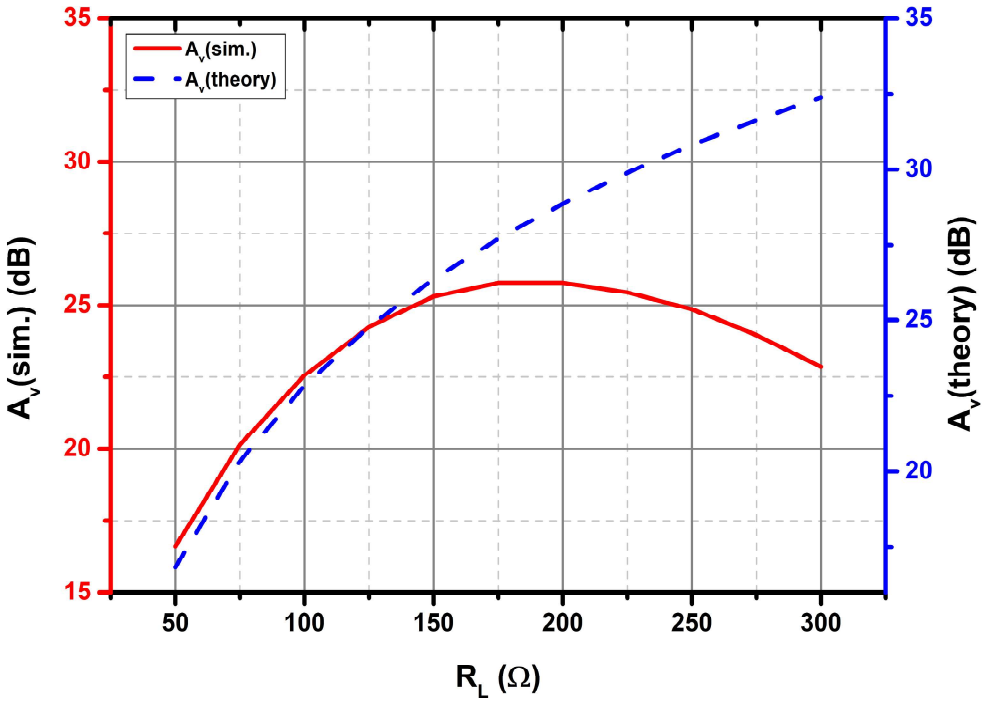
The Gilbert-cell CG dependence on $g_{m1,2}$ and R_L is explored through simulation. In Fig. 20a the CG of the Gilbert-cell is simulated with a constant load resistance while $g_{m1,2}$ is varied by varying the bias current. The theoretical CG in (4) predicts an increasing CG with increasing $g_{m1,2}$, but due to non-linearities and headroom issues the CG compresses. Similarly, in Fig. 20b the CG of the Gilbert-cell is simulated with a constant bias current (hence constant $g_{m1,2}$ while the load resistance is varied. Once again (4) predicts increasing CG with increasing R_L, but the CG compresses once again. In both cases, (4) agrees well with simulation when device non-linearities and headroom issues are absent. Instead of holding one of the parameters constant, it is possible to vary both parameters to explore the CG design space for optimum CG in case the mixer needs to be optimum CG.

At high frequencies the LO signals depart from the ideal square waves and become sinusoidal. A large LO amplitude is then used to obtain the desired switching

conditions shown in Fig. 19.



(a) Gilbert-cell CG dependence on transconductance



(b) Gilbert-cell CG dependence on load resistance

Figure 20: Gilbert-cell CG simulation results

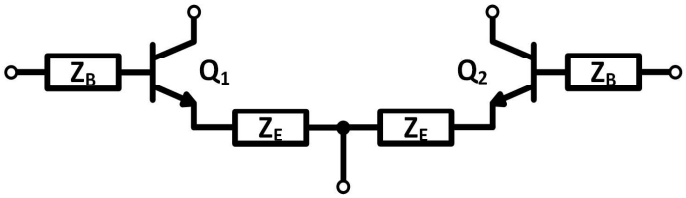


Figure 21: HBT differential pair with emitter degeneration

The linearity of a Gilbert-cell mixer is limited due to the odd-order non-linearities in the transconductance stage and voltage-headroom limitations [20]. Emitter degeneration can be used to increase the linearity of the transconductor at the cost of reduced CG and increased NF. As outlined in [32], the use of inductive degeneration improves the IIP_3 of a differential pair to a greater extent than resistive or capacitive degeneration. In addition to this, inductive degeneration introduces significantly lower noise when compared to resistive degeneration [20]. Volterra series analysis was used in [32] to show that for an emitter degenerated differential pair - shown in Fig. 21, the third order intermodulation products (IM_3) depend on the degeneration impedance, Z_E as shown in (5).

$$|IM_3| \propto |1 + sC_{je}[Z_B(s) + Z_E(s)]| \tag{5}$$

In (5), C_{je} is the base-emitter junction capacitance of the differential pair transistor Q_1/Q_2 and Z_B includes all the impedances at the base of the transistors. Note that the term $sC_{je}Z_E$ in (5) is a negative real number for an inductor with impedance $Z_E = sL_E$. Therefore an inductor can be used in the emitter to decrease the magnitude of the IM_3, and hence improve the linearity of the mixer. Improvement in IIP_3 also leads to improvement in the $\text{IP}_{1\text{dB}}$ due to reduction in odd-order non-linearity.

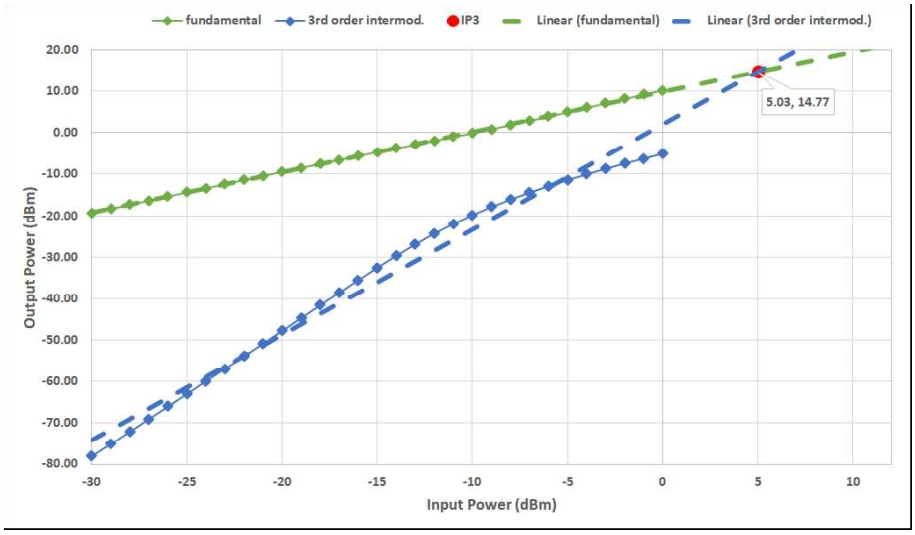
The improvement in transconductor linearity using inductive degeneration is verified using simulation. The emitter-degeneration inductance, L_E of a differential pair is varied under constant DC bias conditions. The IIP_3 of the differential pair is then simulated using two equally powered tones that are situated 100 MHz on either side of a 26 GHz carrier frequency. The input power is increased until the point no compression occurs for the fundamental component, and then the results are linearly extrapolated to obtain the IP_3. From the simulation results in Fig. 22, it can be observed that the IIP_3 of the differential pair improves as L_E increases. This

improvement in the linearity comes at the cost of reduced gain. In Fig. 22a, for no emitter degeneration the IIP_3 is 5.0 dBm with a small-signal gain of approximately 10.7 dB, whereas in Fig. 22c for an L_E of 500 pH the IIP_3 is 24.2 dBm with a small-signal gain of approximately 0 dB.

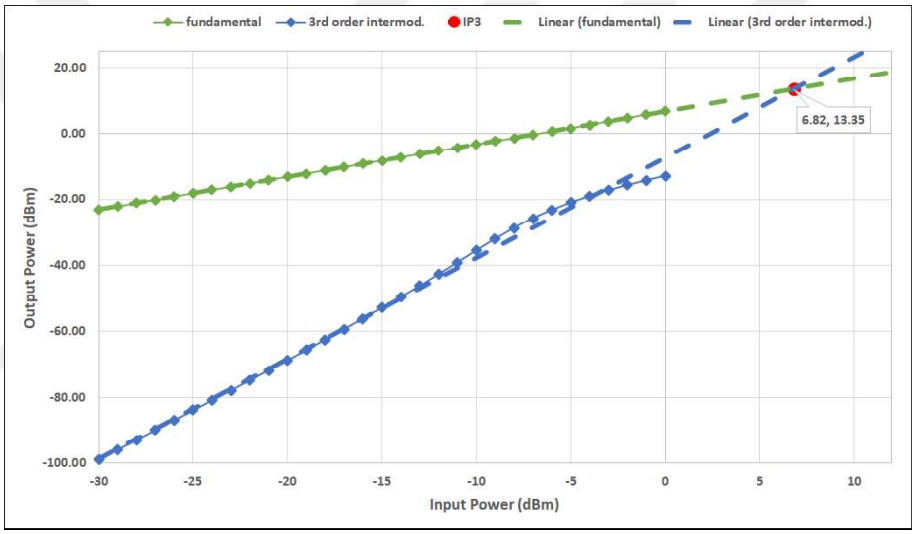
The reduction in gain of the differential pair is due to the reduction of the effective transconductance. The degenerated transconductance shown in (6) enhances the linearity at the expense of gain.

$$g_m \xrightarrow{\text{degenerated}} \frac{g_m}{1 + g_m Z_L} \tag{6}$$

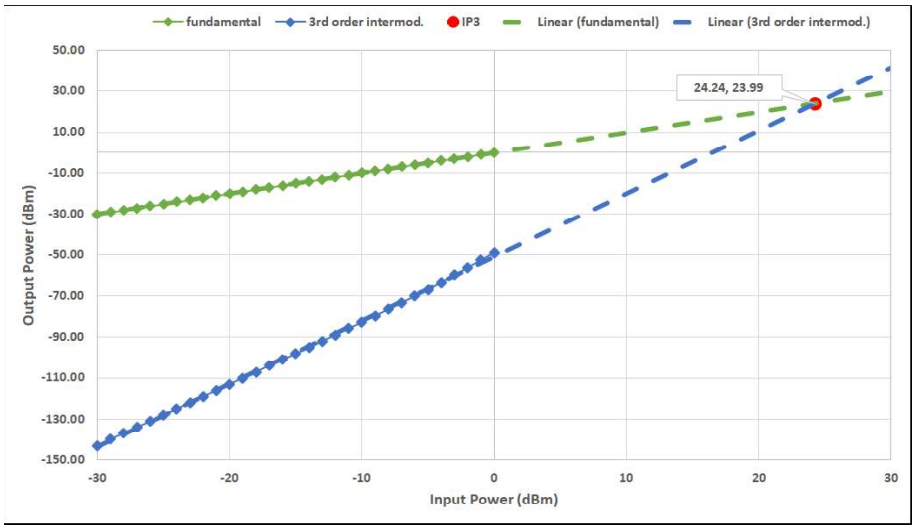
The reduction in linearity of a Gilbert-cell mixer due to limited headroom will be addressed in the design that is presented in the following section.



(a) IP_3 with $L_E = 0$ pH



(b) IP_3 with $L_E = 100$ pH



(c) IP_3 with $L_E = 500$ pH

Figure 22: HBT differential pair IP_3 variation with L_E

2.2.3 Emitter Degenerated Gilbert-Cell Mixer Design

Inductive degeneration was shown to enhance the linearity of a differential pair transconductance stage. In this section a Gilbert-cell based active mixer is optimized for high linearity using inductive degeneration without the requirement for introduction of any extra linearization techniques, thus decreasing the complexity of the design.

The fully-integrated downconversion mixer is composed of a four-way Wilkinson Power Combiner (WPC) to combine the RF signals from four of the beamformers. The incoming RF signal is single-ended and so to obtain the differential RF signal a balun is used. A balun is also utilized at the LO port, since only single-ended LO signal is available. Before the output LPF, a balun is placed at the IF output port since a single-ended output is desired from the mixer. The block-level mixer is shown in Fig. 23.

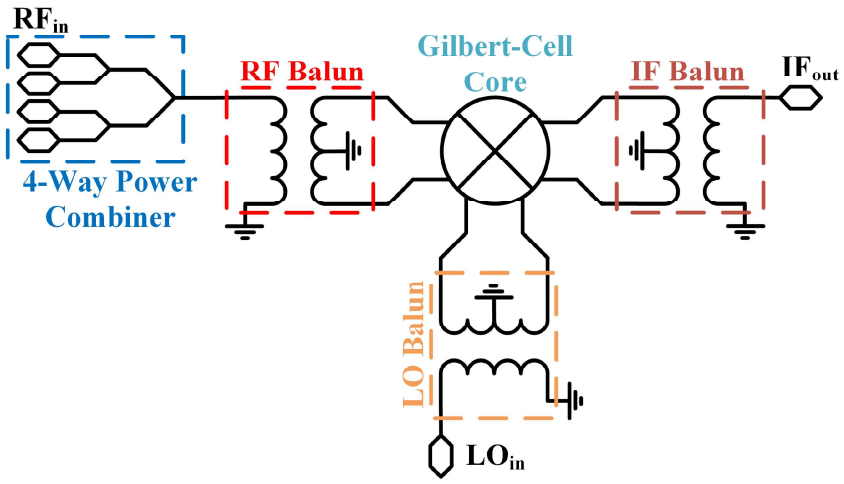
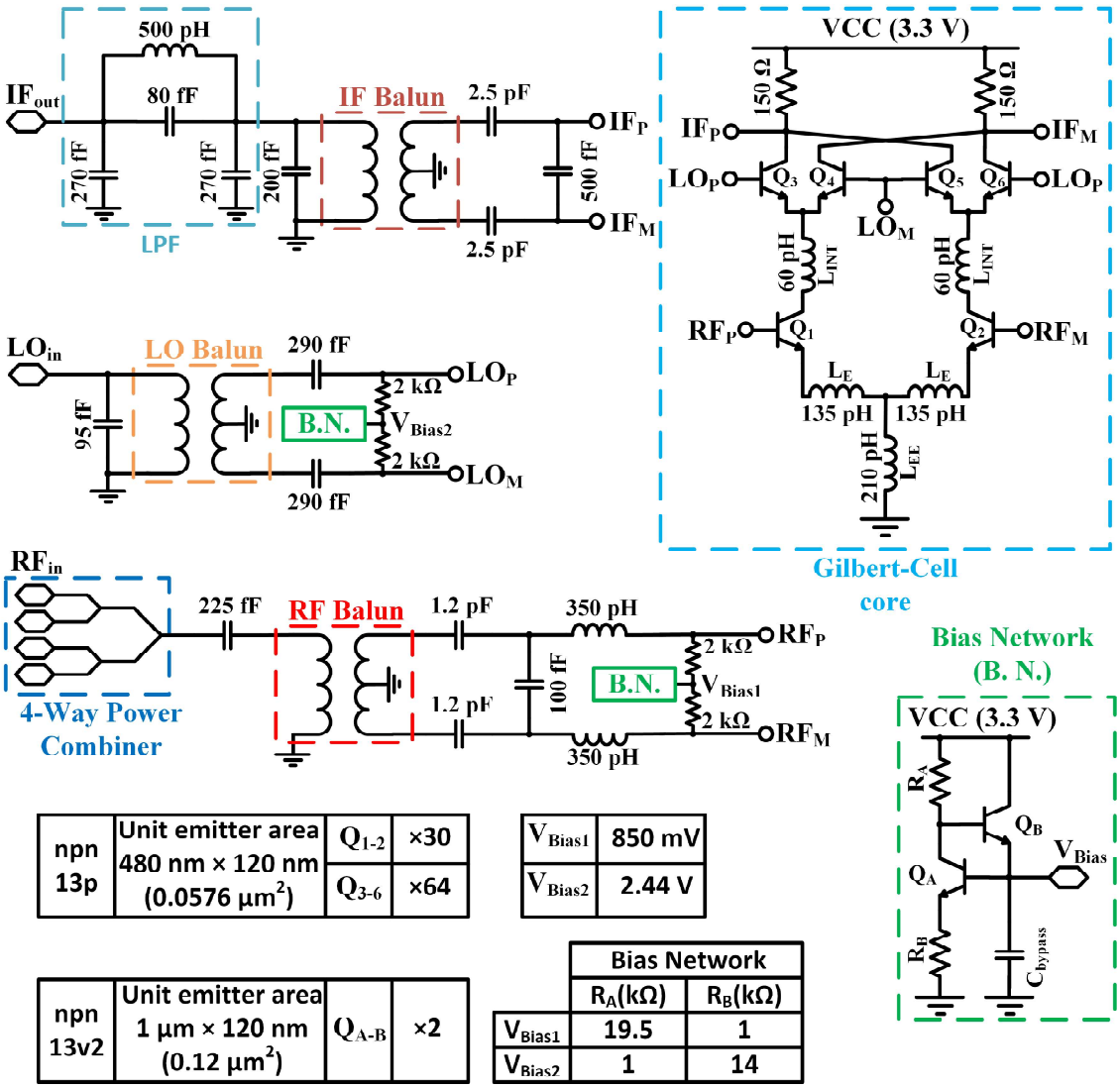


Figure 23: Overview of downconversion mixer



npn 13p	Unit emitter area 480 nm × 120 nm (0.0576 μm²)	$Q_{1\text{-}2}$	×30
		$Q_{3\text{-}6}$	×64

V_{Bias1}	850 mV
V_{Bias2}	2.44 V

npn 13v2	Unit emitter area 1 μm × 120 nm (0.12 μm²)	$Q_{A\text{-}B}$	×2

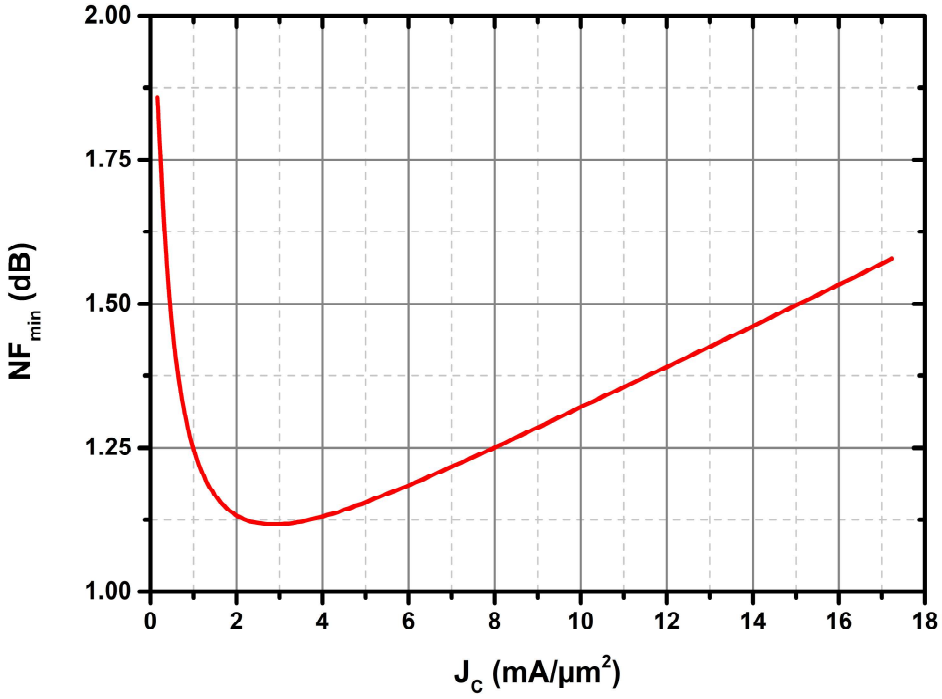
	Bias Network	
	R_A(kΩ)	R_B(kΩ)
V_{Bias1}	19.5	1
V_{Bias2}	1	14

Figure 24: Schematic of the designed emitter-degenerated Gilbert-cell mixer

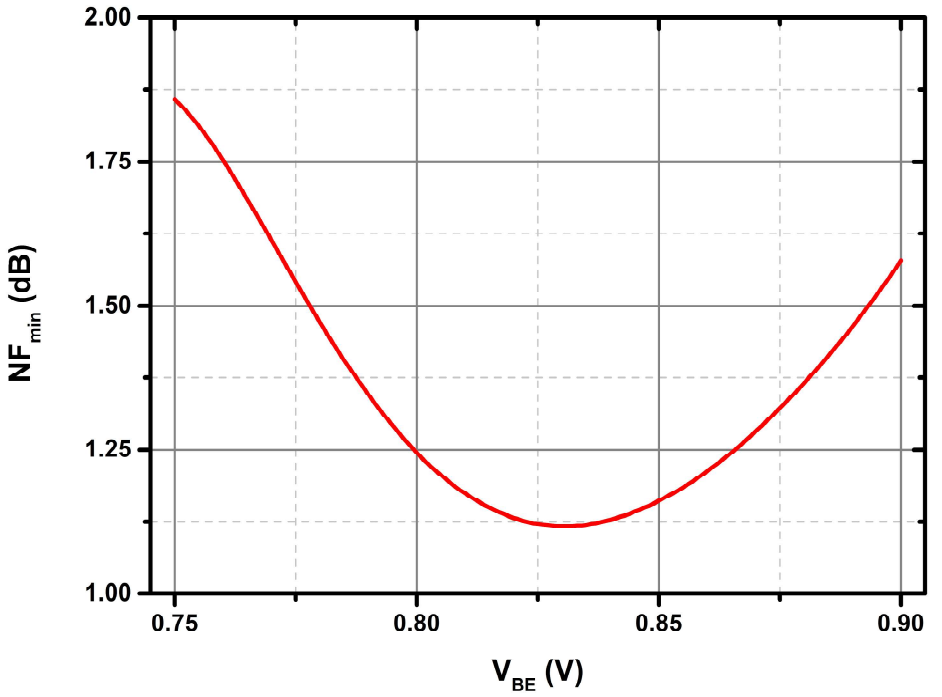
The RF input differential pair consisting of $Q_1 - Q_2$ in Fig. 24 is designed first. High performance NPN HBTs (npn13p) with f_T of 240 GHz is used in this stage for their superior RF performance. The collector-emitter voltage, $V_{CE1,2}$ is set to the maximum value limited by the nominal open base collector-emitter breakdown voltage, BV_{CEO} of 1.65 V. This allows a large signal swing at the input. The transconductance stage is biased for class-A operation. The base bias, V_{Bias1} is set to obtain the optimum current density for minimum NF, J_{OPT} to obtain a transconductor with low NF and large transconductance [33]. The NF_{min} dependence on collector current density, J_C and the base-emitter voltage, V_{BE} at 26 GHz for a minimum sized HBT (0.0576 μm^2 emitter area) is plotted in Fig. 25a and Fig. 25b respectively. From Fig. 25a the NF_{min} remains relatively constant at around 1.1 dB for J_C in the range of 2 mA/μm^2 to 4 mA/μm^2. This translates to a V_{BE} of around 815 mV to 845 mV as can be seen in Fig. 25b. In the designed mixer, V_{Bias1} is set to 850 mV. This is slightly higher than optimum value for V_{Bias1} and it is set due to the resistive parasitics that were introduced at the emitter after layout. The effective V_{BE} is around 833 mV since there is approximately 17 mV voltage drop at the emitter node. This bias voltage leads to a current density of around 3.2 mA/μm^2.

V_{Bias1} is generated using the integrated bias network shown in Fig. 24. The integrated bias networks allow the mixer to operate from a single supply of 3.3 V which reduces the number of voltages that need to be accurately generated for the beamformer and also reduces the PCB routing complexity. Resistors R_A and R_B are used to set the desired bias voltage, and a bypass capacitor of around 2 pF is used to create a short at high frequencies. The high breakdown voltage NPN HBTs (npn13v2) with BV_{CEO} of 3.6 V are used so that they can withstand the large collector-emitter voltage across them.

The number of devices in the RF input differential pair determines the bias current, I_{Bias} and this in turn determines the g_m in (4) and hence the CG. I_{Bias} will also determine the DC bias voltage at the output nodes and will thus determine the maximum allowable voltage swing at the output. To obtain a large voltage swing at the output, the voltage drop across the switching quad (composed of $Q_3 - Q_6$) needs to be set to be approximately equal to the voltage drop across the load resistor



(a) NF_{min} vs. J_C



(b) NF_{min} vs. V_{BE}

Figure 25: Bias dependence of NF_{min} of minimum sized HBT at 26 GHz

R_L [33]. R_L is determined by iteration and is set to 150 Ω in order to balance the trade-off between voltage drop and CG, and just as significantly to provide an output impedance at IF that can be matched using on-chip components. With R_L set, I_{Bias} is determined to be 11.2 mA, which allows a high peak-peak swing of around 1.6 V at the output. To obtain the required I_{Bias}, Q_1 and Q_2 are set to 30 times the unit-sized device.

After the transconductance stage has been designed, the switching quad stage is designed. The bias voltage of the switching quad, V_{Bias2} is set to obtain a high $\text{IP}_{1\text{dB}}$ and a large number of devices (×64) is used to improve the NF [20], and at the same time to provide an output impedance suitable for matching.

The optimum value of L_E is investigated after the DC biasing has been determined. Since there is a trade-off between the CG and linearity, the effect of L_E on CG and $\text{IP}_{1\text{dB}}$ is investigated using ideal lumped components at the schematic level. The simulation results in Fig. 26 show the effect of varying L_E on CG, $\text{IP}_{1\text{dB}}$, and NF. As expected $\text{IP}_{1\text{dB}}$ increases with increasing L_E while CG decreases. The NF increases as well, but the increase is not as drastic as the degradation in CG. To compensate for losses in the passive structures that will be integrated with the mixers, an L_E of 135 pH is selected to provide a positive CG for the mixer core while still achieving a good $\text{IP}_{1\text{dB}}$ performance.

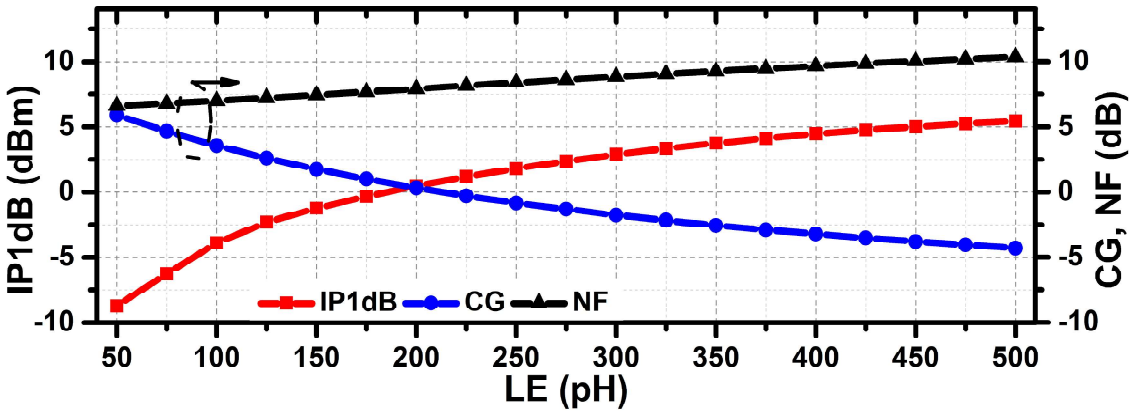


Figure 26: $\text{IP}_{1\text{dB}}$, CG, and NF variation with L_E

The tail current source that is usually present in the Gilbert-cell is replaced by an inductor, L_{EE}. This allows more voltage headroom, since there is no need for a voltage drop across a current source. Inductive broadbanding is used where L_{INT} is placed in series between the transconductor and the switching quad to tune out

the parasitic capacitances and therefore improve the flatness of the CG over a wider bandwidth [34]. The second harmonic of the LO is present at the common emitter junction of the switching quad transistors. This is inherent in a differential pair circuit. L_{EE} in conjunction with L_{INT} suppresses this second harmonic.

Inductive degeneration modifies the differential input impedance of the RF port as in (7), and aids in the input matching [20].

$$Z_{in} = 2\left(r_b + sL_E + \frac{1}{sC_\pi} + \omega_T L_E\right) \tag{7}$$

In (7) r_b is the base resistance of the input transistor, C_π is the base-emitter junction capacitance, and ω_T is the angular transit frequency of the transistor. The reactive part of the input impedance is then neutralized using the series base inductor of 350 pH. Matching networks composed of lumped components are used to match the RF and LO port to a differential impedance of 50 Ω. 1:1 impedance transforming baluns are then used to match the differential RF and LO ports to single-ended 50 Ω inputs. The design of the baluns shall be discussed in the following sub-section.

The IF port is matched using series and shunt capacitors of 2.5 pF and 500 fF respectively, along with the IF balun. The IF balun is used in the matching to avoid using any extra inductors (which need to be large at 3 GHz). The 500 fF shunt capacitor at the output also acts as a low-pass filter which filters out the high frequency mixing spurs that occur at the output.

Balun Design

The function of baluns and their design is briefly described in this section.

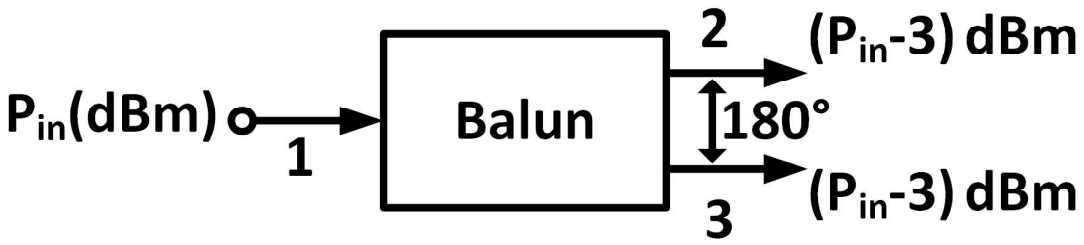


Figure 27: Ideal balun block diagram

An ideal balun performs an equal power split and produces signals that are 180° out of phase for single-ended (unbalanced) to differential (balanced) signal conversion as shown in Fig. 27. For differential to single-ended signal conversion the opposite occurs, and the two out of phase signals are combined to produce a signal with 3-dB more power.The key performance parameters for a balun are its amplitude balance, phase balance, insertion loss, and return loss. For an ideal balun $S_{21} = -S_{31}$. The amplitude and phase imbalance of a balun is a measure of how much the balun deviates from the aforementioned ideal condition. The excess loss (above the systematic 3-dB equal power- splitting loss) introduced by a balun is measured by its insertion loss (IL). The impedance transformation property of baluns make the return loss an important parameter, and the balun must be terminated with appropriate impedances to obtain the desired operation.

The amplitude and phase balance performance of a balun can be represented by the common-mode rejection ratio (CMRR) of the balun which is defined as in (8). A high CMRR translates to low amplitude and phase imbalance and is desirable for common-mode noise reduction [35].

$$CMRR(dB) = 20\log_{10}\left|\frac{S_{21} - S_{31}}{S_{21} + S_{31}}\right| \tag{8}$$

Baluns can have active or passive implementations. Passive baluns are utilized in this work in order to improve the overall linearity of the mixer, and they have an additional advantage of zero DC power consumption. The main penalty of using a

passive balun is the large area that they occupy. At the frequencies of interest, the broadside coupled transformer balun can provide good phase and amplitude balance over a relatively wide bandwidth without occupying a large area when compared to other passive balun structures such as the LC balun or the Marchand balun. Broadside coupled transformer is used in favor of edge-coupled transformer since it has a more compact structure and can provide a high coupling coefficient [36].

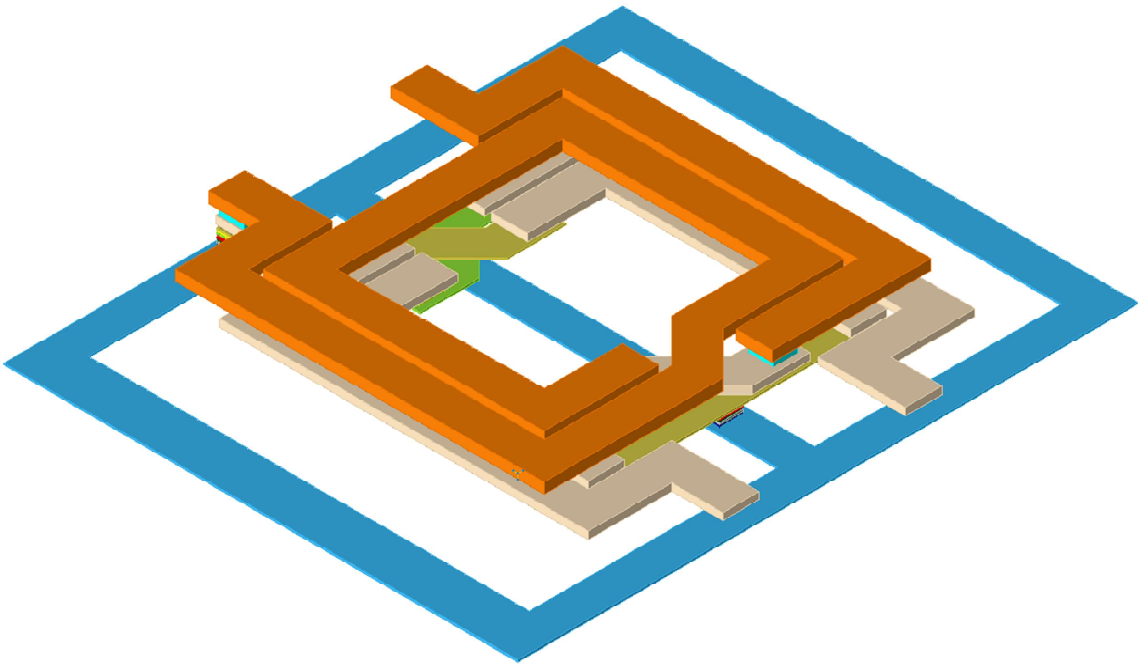
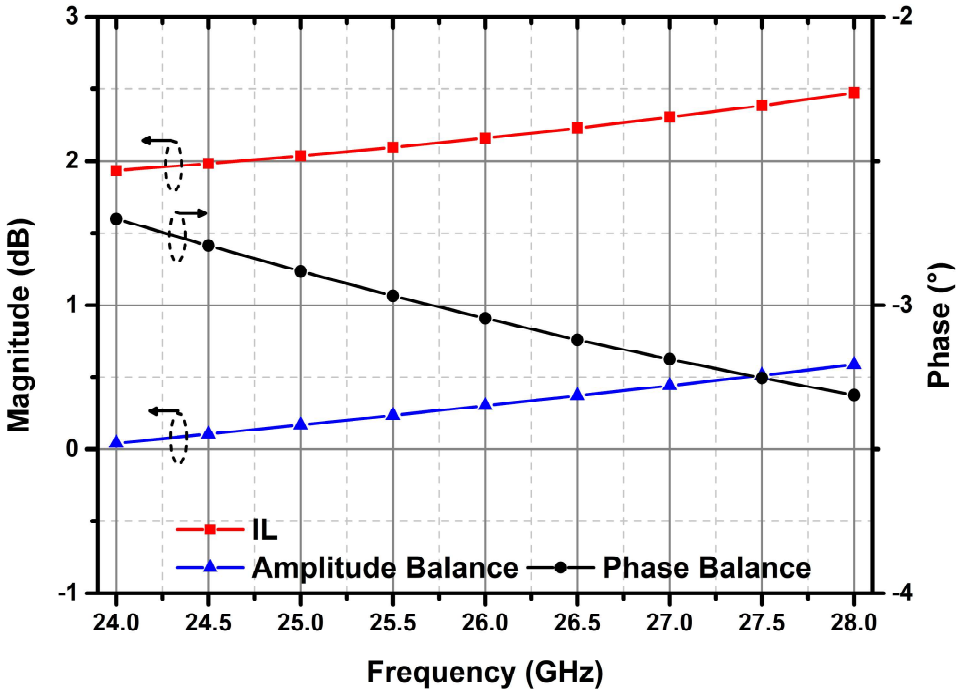
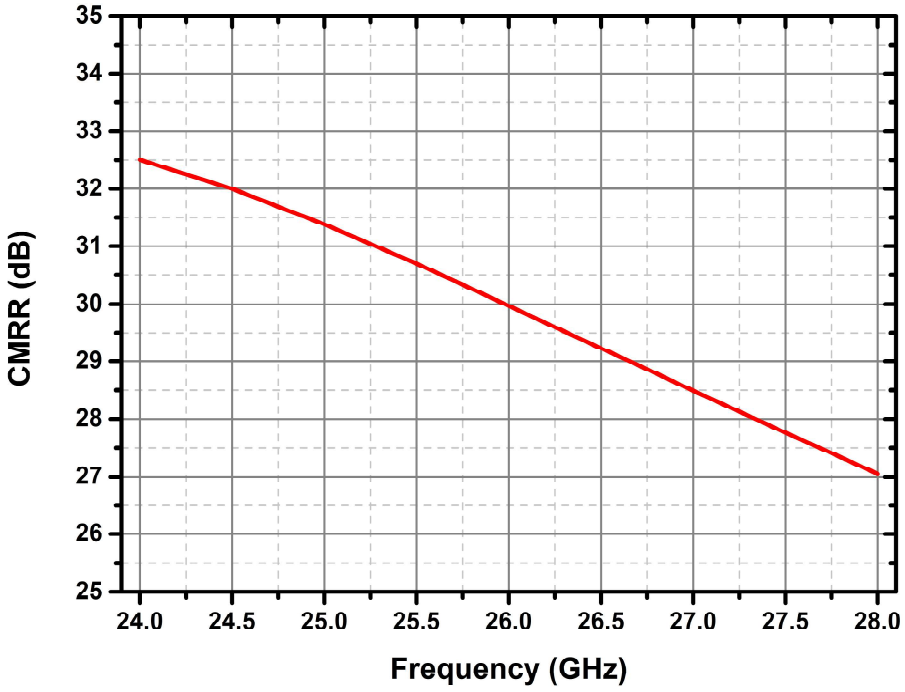


Figure 28: Balun used at the mixer RF port

The 1:1 impedance transforming balun used in the RF port is shown in Fig. 28. The two top-most metal layers in the technology were used in the design of the primary and secondary coils of the transformer in order to minimize the insertion loss. The balun utilizes primary and secondary coils of approximately 450 pH inductance with a quality factor of around 18 for the primary (coil in top-metal 2) and 10 for the secondary (coil in top-metal 1). The addition of a center-tap in the secondary coil and offsetting the coils about their centers provides low amplitude and phase imbalance over the required bandwidth [36]. The simulated amplitude balance, phase balance, and IL performance of the balun is shown in Fig. 29a, and the CMRR is shown in Fig. 29b. The maximum amplitude imbalance is around 0.6 dB and the maximum phase imbalance is around 3.3°, the maximum IL is around 2.5 dB, while the minimum CMRR is 27 dB. A similar balun is used at the LO port.



(a) Amplitude balance, Phase balance, and IL



(b) CMRR

Figure 29: RF balun simulation results

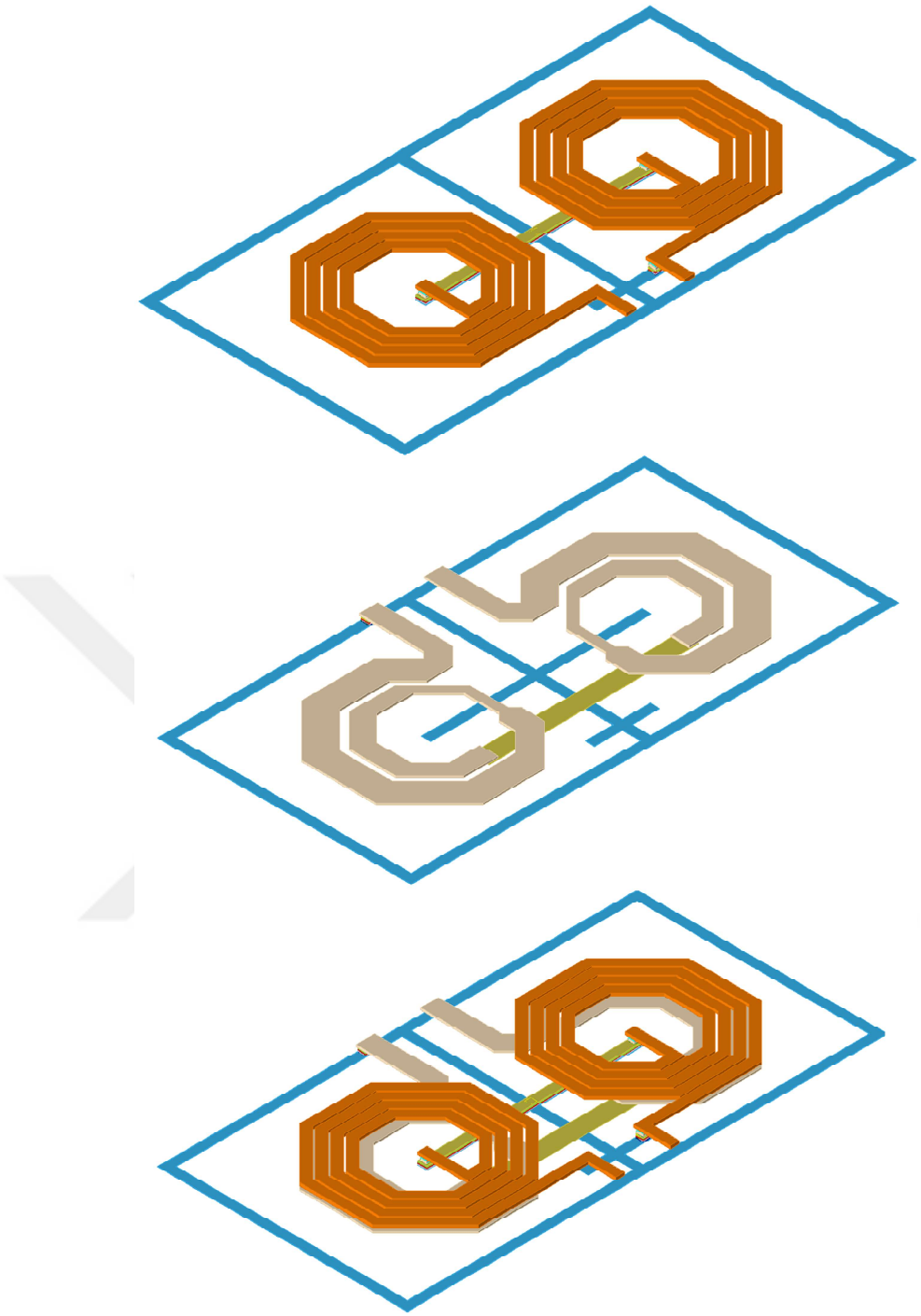
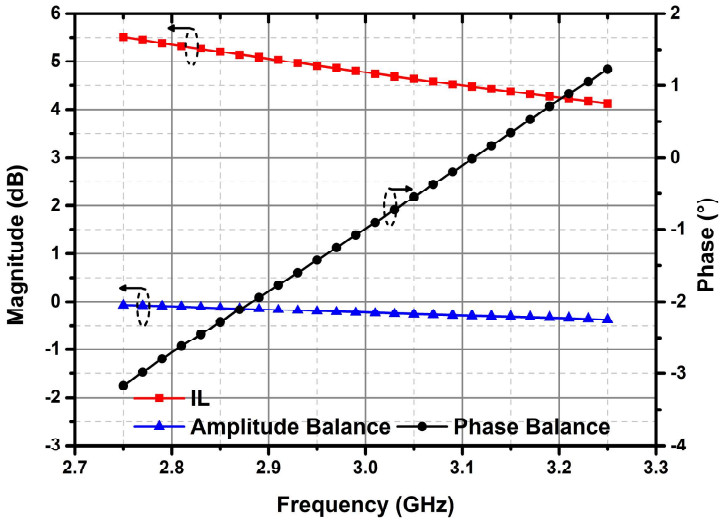


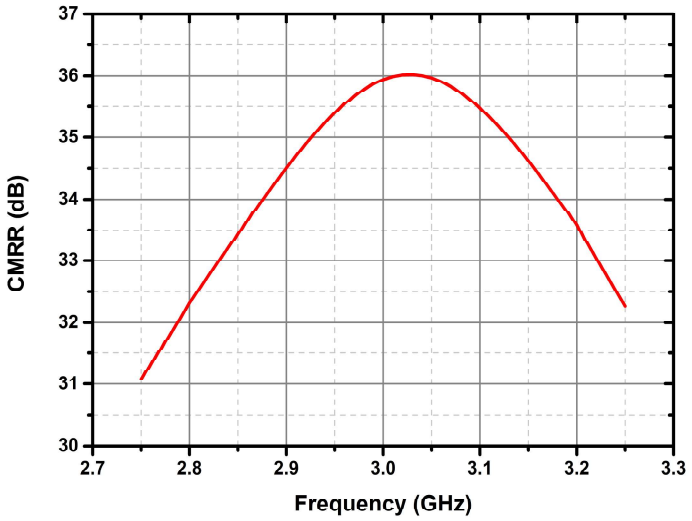
Figure 30: Balun used at the mixer IF port - primary coil (top), secondary coil (middle), and overall balun structure (bottom)

The balun used in the IF port is shown in Fig. 30. The IF balun requires larger inductances due to the lower operating frequency and the need for impedance transformation to 50Ω. The primary coil is 4.8 nH with a quality factor of 8, and the secondary coil is 1.0 nH with a quality factor of 6. The coils were unwrapped in order to optimize the dimensions of the balun with respect to the overall floorplan.

This balun occupies an area of about 0.12 mm^2 while the RF balun occupies an area of about 0.01 mm^2. Even though a large area is required by this balun, it is still the preferred option over active baluns due to linearity and power consumption considerations. The simulation results for the IF balun are shown in Fig. 31. The maximum amplitude imbalance is around 0.4 dB and the maximum phase imbalance is around 3.2°, the maximum IL is around 5.5 dB, while the minimum CMRR is 31 dB. The relatively large IL is due to the low quality factor of the integrated inductors at 3 GHz that are used to implement the balun.



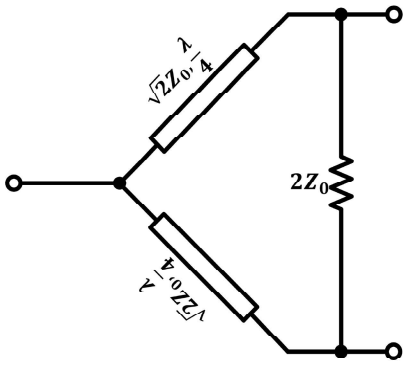
(a) Amplitude balance, Phase balance, and IL



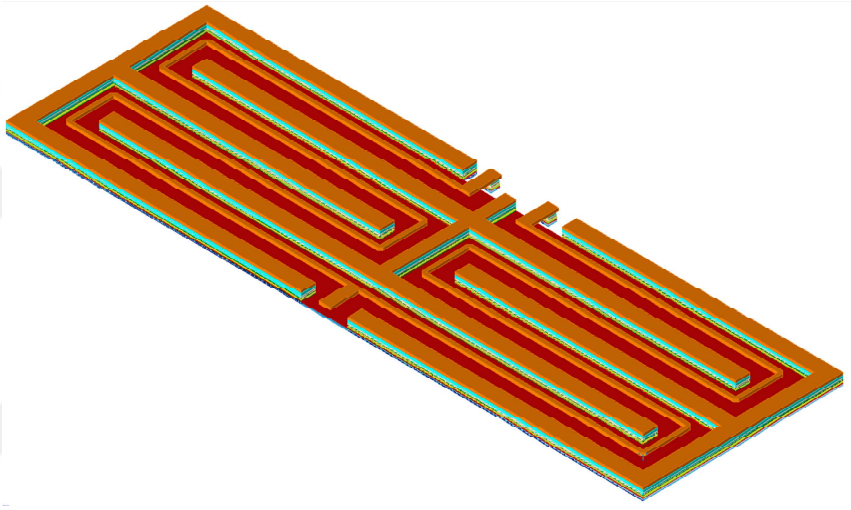
(b) CMRR

Figure 31: IF balun simulation results

Power Combiner Design



(a) WPC Schematic



(b) 3-D view of two-way WPC

Figure 32: Wilkinson Power Divider/Combiner

The input signals from the four channels of the beamforming receiver are combined using a distributed four-way Wilkinson Power Combiner (WPC). The four-way WPC is composed of cascaded two-way WPCs. The schematic of a two-way WPC is shown in Fig. 32a. The quarter-wavelength high impedance sections of the WPC can either be implemented using transmission lines or equivalent lumped element approximations. A distributed implementation of the WPC in general offers wider bandwidth of operation when compared to the lumped element implementation. So, a distributed implementation is utilized in this design. This WPC was designed by Ilker Kalyoncu. Grounded coplanar transmission line structure with multiple bends is used for the quarter-wave sections of the WPC as shown in the 3-D structure of a single two-way WPC in Fig. 32b. The 4 μm wide high impedance quarter-wave sections are realized using the top-most metal layer with the ground planes 16 μm

away from the quarter-wave sections. The 100 Ω isolation resistors are implemented using low temperature coefficient salicided gate polysilicon resistors with sheet resistance of 7 Ω/□. Each two-way WPC measures 712 μm by 224 μm. The two-way WPCs are connected using grounded coplanar transmission lines of width 15 μm and spacing of around 18 μm from the ground plane.

The simulation results for the four-way WPC is shown in Fig. 33. The four-way WPC has a maximum IL of 3.1 dB above the systematic 6 dB. The return loss is better than 15 dB over the bandwidth of interest, and all port-to-port isolations are better than 16 dB. Compared to lumped implementations such as [37], this distributed four-way WPC shows better return loss performance and comparable isolation over the RF bandwidth.

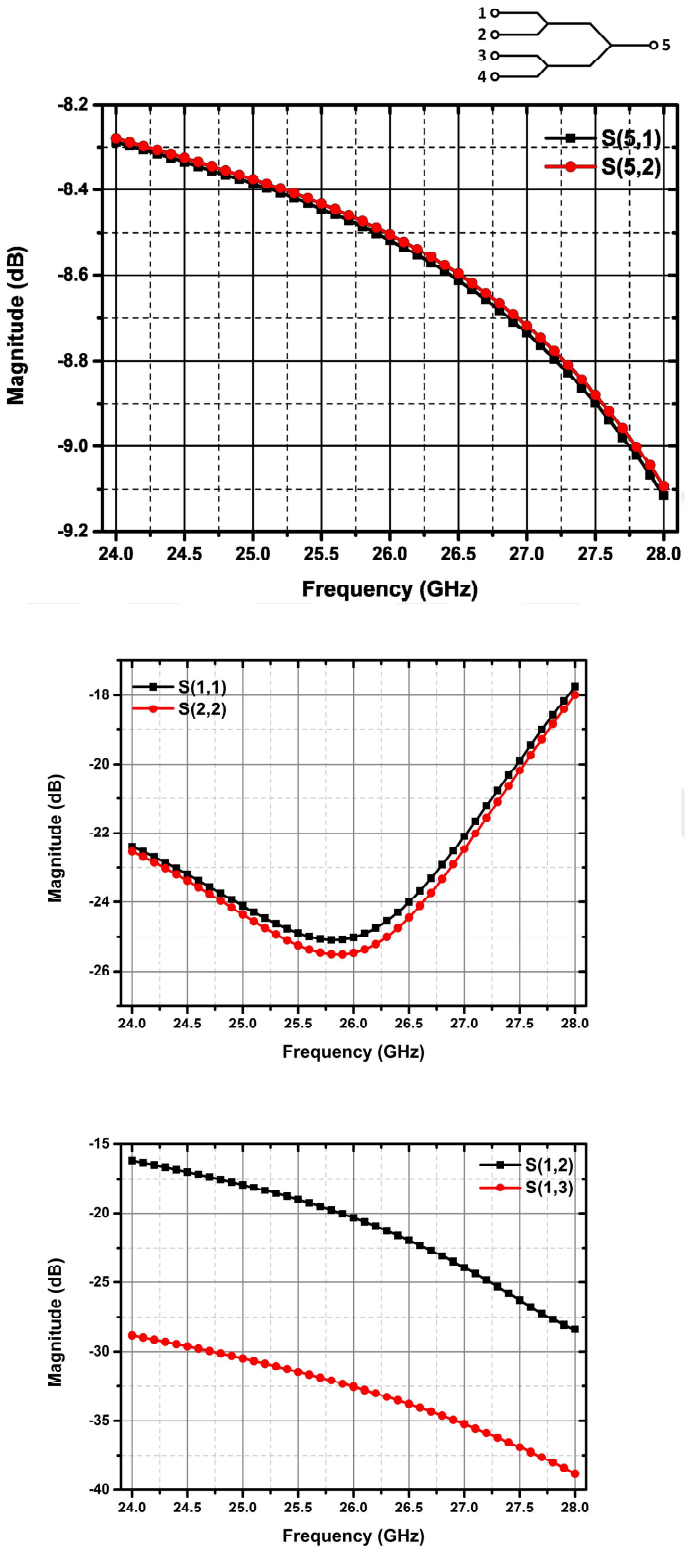


Figure 33: Four-way WPC simulated S-parameters

Low Pass Filter Design

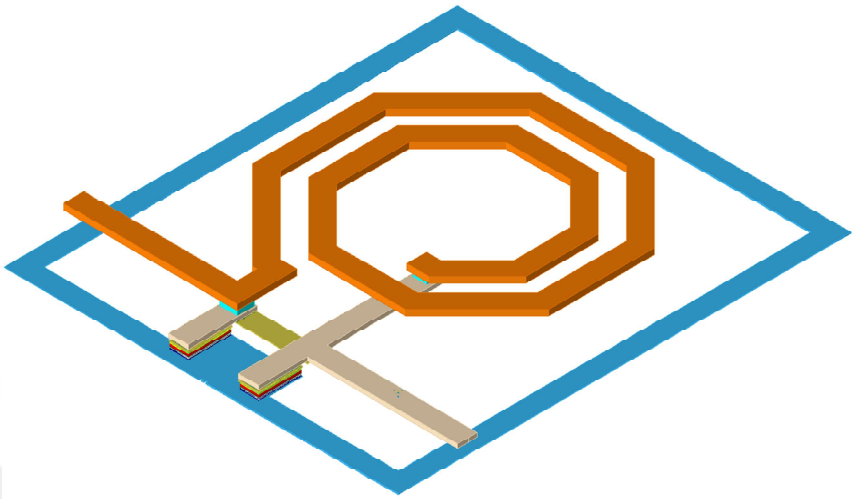


Figure 34: 3-D view of low pass filter at IF

A third order elliptic π-type low pass filter is placed at the IF output of the mixer to attenuate the mixing spurs and the RF and LO leakage signals. An elliptic filter is selected to obtain high attenuation at the stopband without the need for a large number of filter sections. The required passband of the filter is the IF band. The corner frequency of the filter is adjusted such that maximum attenuation/notch is observed at the LO band. This ensures further LO rejection. The filter is matched to 50 Ω at the input and output ports. The filter, as shown in Fig. 34, utilizes a single 500 pH inductor (quality factor of 8 at 3 GHz) in shunt with a 79 fF MIM capacitor, and two 270 fF MIM capacitors shunted to ground. The return loss and insertion loss of the filter are plotted in Fig. 35. The maximum pass band insertion loss is 0.35 dB and the return loss is better than 10 dB. At frequencies greater than 30 GHz, at least 17 dB of attenuation is obtained. This ensures that the mixing spurs and leaked signals are attenuated at the output.

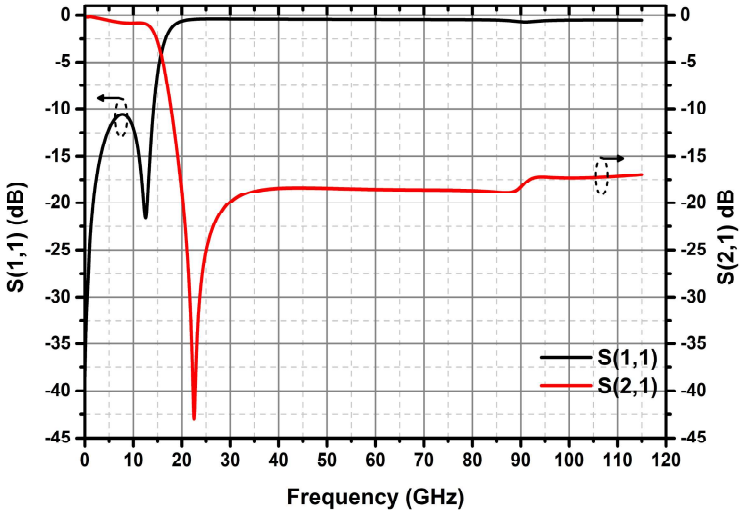
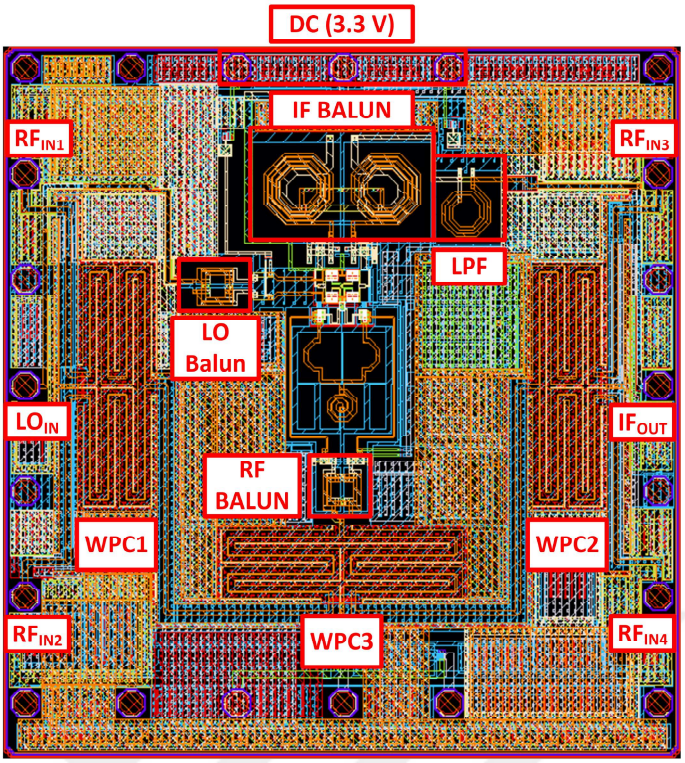


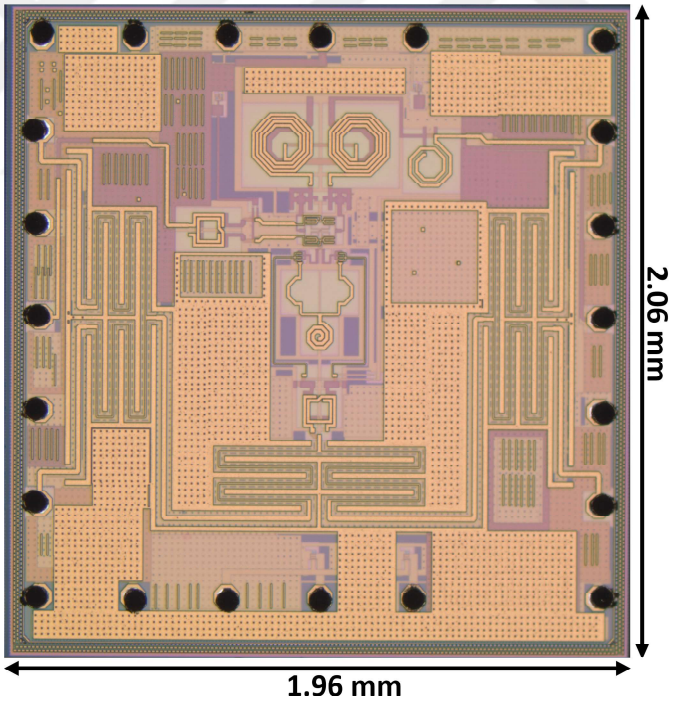
Figure 35: Low pass filter simulation results

Mixer Measurement Results

The annotated layout of the mixer is shown in Fig. 36a and the chip micrograph is shown in Fig. 36b. The mixer occupies an area of 4.03 mm^2 (1.96 mm $\times$ 2.06 mm). The area of the core mixer without power combiners and baluns is around 0.26 mm^2 (410 μm $\times$ 640 μm). The mixer is flip-chip bonded onto a Rogers RO5870 PCB for measurement as shown in Fig. 37 and the measurement setup that is used is described in Appendix C. The measurement results include PCB transmission line losses, and so for proper comparison with the simulation results the effects of these lines are included in simulation.The measured mixer consumes 29.7 mW from a 3.3 V supply.



(a) Mixer layout



(b) Mixer chip micrograph

Figure 36: Mixer layout and chip micrograph

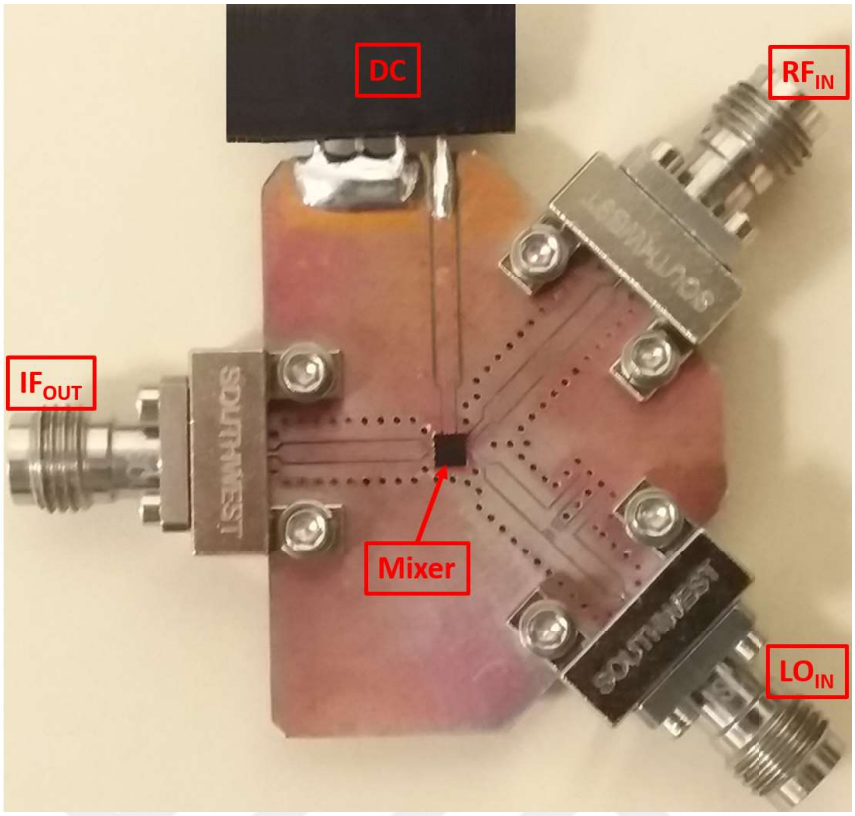


Figure 37: Mixer flip-chip bonded for measurement

The mixer measurement results are presented in Fig. 38 through 43. The CG of the mixer saturates with 6 dBm LO power as in Fig. 39. It should be noted that the LO balun together with the interconnects and PCB traces have an insertion loss of around 4 dB. Hence the LO power at each of the switching quad is around -1 dBm. The required LO power is still significantly large especially for phased array receivers and will be addressed in the subsequent section. Fig. 40 demonstrates that the measured and simulated CG and IP_{1dB} of the mixer at 26 GHz differs by about 0.7 dB. The average CG over the 24 - 28 GHz bandwidth is -12.9 $\pm$ 1 dB from Fig. 38. The NF of the mixer is measured as 23.3 dB (average) over the desired band. It is dominated by the loss of the passive components at the ports of the mixer.

The reflection coefficients at the RF and IF ports are better than -10 dB as in Fig. 42a and Fig. 42c respectively. The LO reflection coefficient shows a shift in the peak from 23 GHz to 26 GHz. Port-to-port isolations are all better than about 30 dB as in Fig. 43a - 43c.

The measured IP_{1dB} is within 1 dB of the simulated values and its minimum value within the band is 5.4 dBm at 24 GHz from Fig. 41 . The average IP_{1dB} is 6.4

dBm over the desired band. Measurements verify that the applied inductive emitter degeneration technique leads to improved linearity.

The measurements of a standalone two-way WPC in Fig. 44a and Fig. 44b are used to de-embed the performance of the core mixer. In Table 4 the simulation results of the core mixer without the four-way WPC and PCB shows that the core mixer exhibits a low CL of 2.05 dB and a high IP_{1dB} of -2.95 dBm. The NF of the core mixer is 11.2 dB, which shows that the overall NF of the mixer is dominated by the WPC.

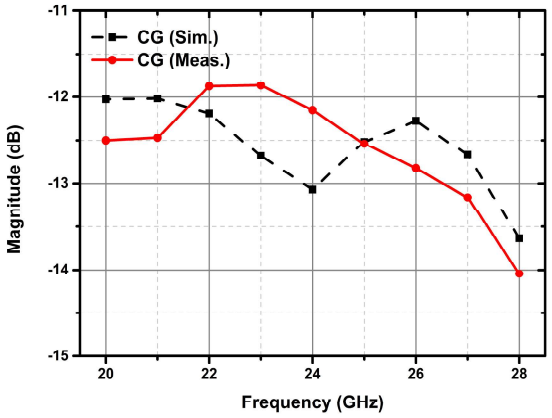


Figure 38: Measured and simulated CG vs. RF frequency

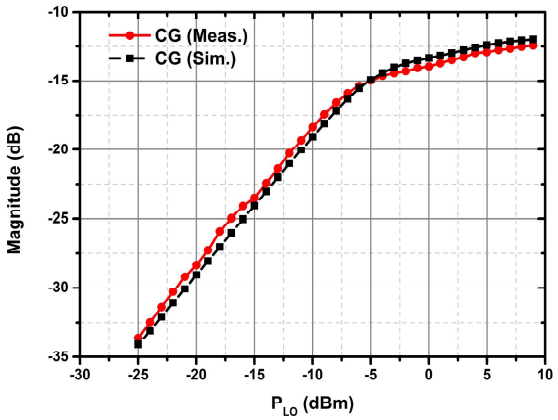


Figure 39: Measured and simulated CG vs. LO power for 26 GHz RF

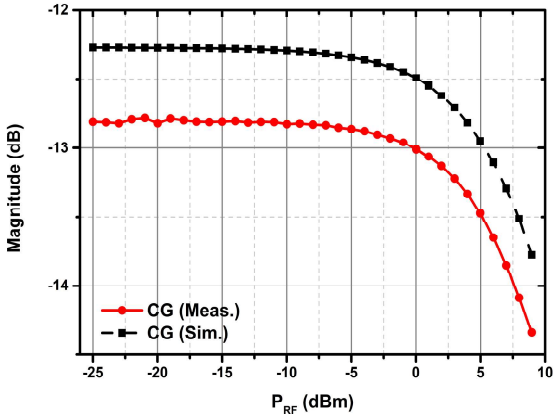


Figure 40: Measured and simulated CG vs. RF input power for 26 GHz RF

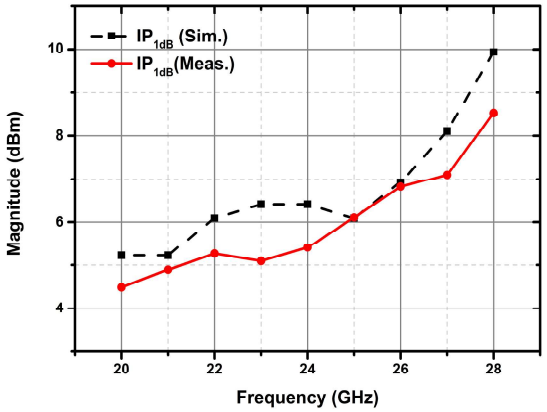
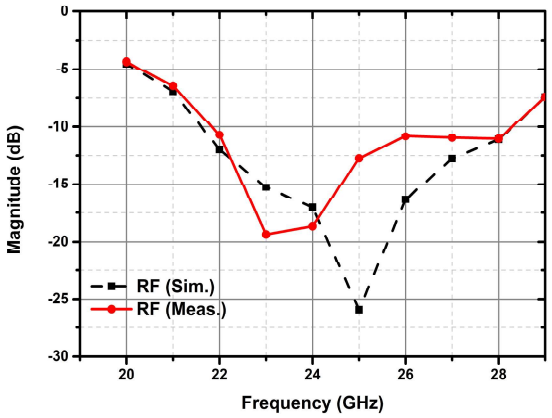
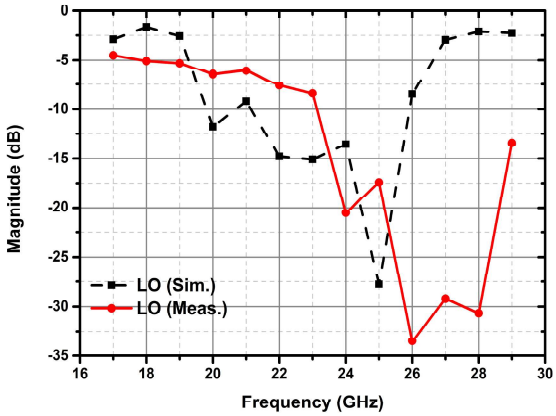


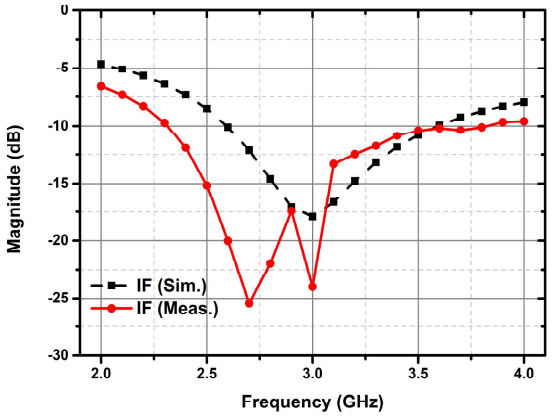
Figure 41: Measured and simulated IP_{1dB} vs. RF frequency



(a) RF port reflection coefficient

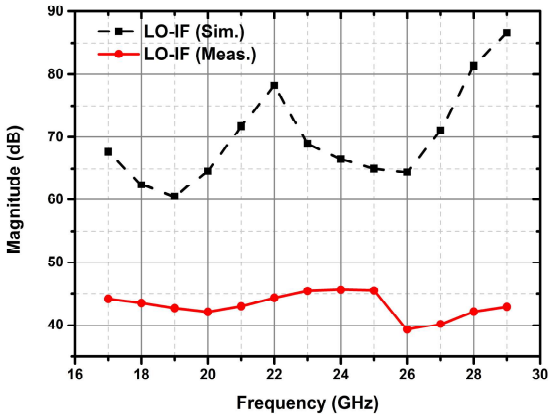


(b) LO port reflection coefficient

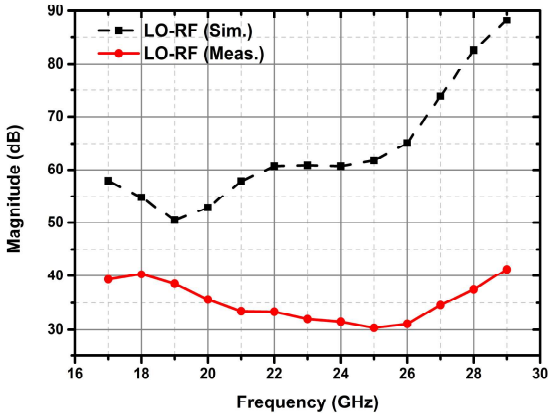


(c) IF port reflection coefficient

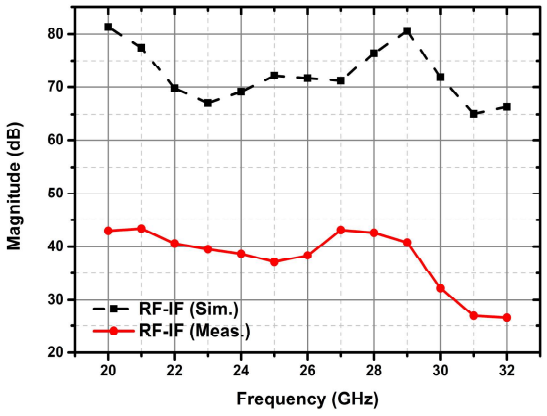
Figure 42: Mixer port matching



(a) LO-IF isolation

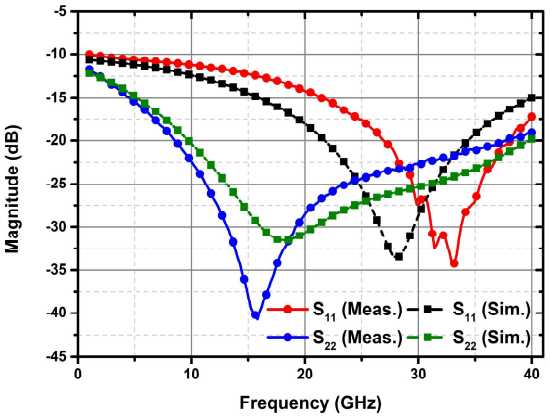


(b) LO-RF isolation

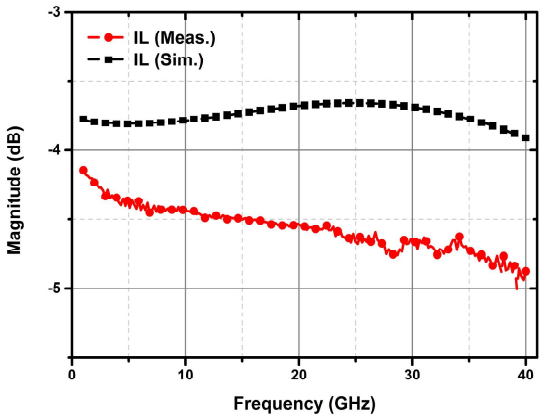


(c) RF-IF isolation

Figure 43: Mixer port-to-port isolation



(a) Reflection coefficients



(b) Insertion Loss

Figure 44: Two-way Wilkinson Power Combiner measured and simulated results

Table 4: Comparison of 5G Downconversion Mixers

	This Work	This Work (sim. w/o WPC)	[38]	[39]	[40]
Tech.	130-nm SiGe	130-nm SiGe	65-nm CMOS	180-nm CMOS	180-nm SiGe
RF (GHz)	24 - 28	24 - 28	26 - 30	27 - 40	20 - 32
CG (dB)	-12.9	-2.05	-8	-15.2	3
IP_{1dB} (dBm)	6.4	-2.95	9.4[1]	-5	-8.05[1]
P_{DC} (mW)	29.7	29.7	0	0	18
P_{LO} (dBm)	6	6	12[2]	6	5
SSB NF (dB)	23.3	11.2	-	-	10.5
Min. Iso. (dB)	30	51	35	60	15

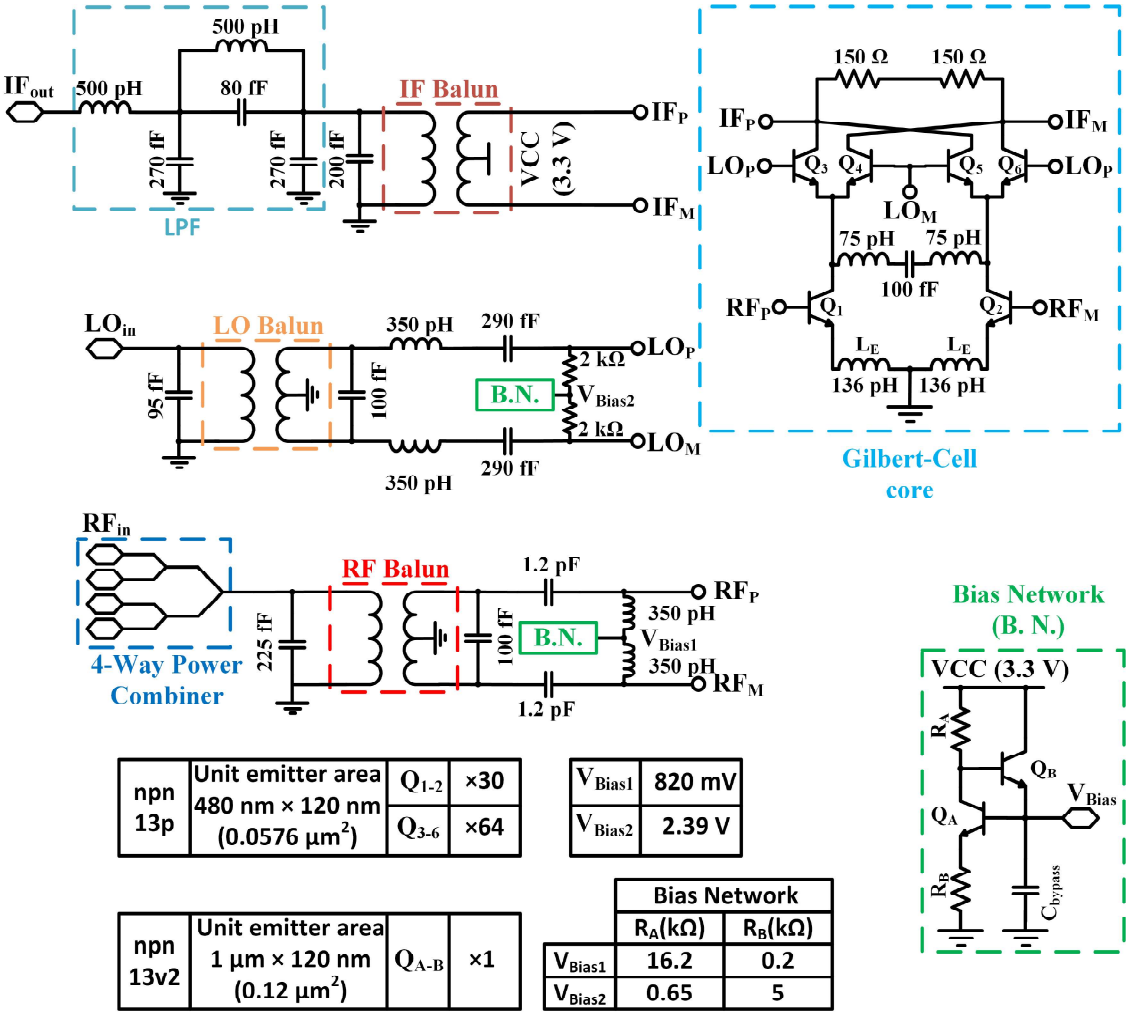
[1]Estimated $IP_{1dB} = IIP_3 - 9.6$ [2]Assumed 10% of power consumption of LO driver.

The core mixer achieves a low loss compared to the passive implementations of [38] and [39] while requiring lower or the same LO power. Compared to the active single-balanced mixer of [40], this work attains better linearity and isolation but consumes more DC power. It must be noted that this is a fully integrated implementation and hence the presented mixer can be used to meet the criteria set for linearity, CG, NF, and LO drive requirements for 5G beamforming applications as a compact solution.

2.2.4 Balun Loaded Gilbert-Cell Mixer Design

From Table 4 it can be deduced that while the designed mixer obtains CL lower than the specifications, the IP_{1dB} is lower than what is stated in the requirements in Table 3. So, to enhance the linearity further a further linearity enhancement technique is investigated as described in this section.

Other than third-order intermodulation products, the voltage-headroom was stated to limit the linearity of the Gilbert-cell mixer in section 2.2.2. To improve the linearity of the Gilbert-cell further, the voltage-headroom is improved by applying the DC supply voltage directly across the output IF balun, instead of across the load resistors. This ensures that there is almost no voltage drop at the collector of the switching quad transistors (a small voltage drop exists in practice due to the ohmic loss of the balun). The schematic of the modified balun loaded Gilbert-cell mixer is shown in Fig. 45.



npn 13p	Unit emitter area 480 nm × 120 nm (0.0576 μm²)	$Q_{1\text{-}2}$	×30
		$Q_{3\text{-}6}$	×64

V_{Bias1}	820 mV
V_{Bias2}	2.39 V

npn 13v2	Unit emitter area 1 μm × 120 nm (0.12 μm²)	$Q_{A\text{-}B}$	×1

	Bias Network	
	R_A(kΩ)	R_B(kΩ)
V_{Bias1}	16.2	0.2
V_{Bias2}	0.65	5

Figure 45: Schematic of the designed balun loaded Gilbert-cell mixer

Apart from applying the DC supply through the center tap of the balun at the IF port, the bias of the transconductor stage is applied across inductors to improve the linearity. The aforementioned bias voltage is also decreased for reduced power consumption. Modifications are made to the matching networks. Instead of series peaking interstage inductors, LC sections are placed shunt at the transconductor output to improve the CG flatness. The required LO power is reduced significantly from 6 dBm to 0 dBm by improving the matching network at the LO port. Finally, the order of the LPF is increased by adding a series inductor to achieve better spurious suppression. To obtain the desired impedance transformation to 50Ω at the IF output, the balun shown in Fig. 46. The coil on the differential side has an inductance of 5.5 nH and Q of 9 at the IF while the other coil has an inductance of 0.6 nH and Q of 8 at the same frequency.

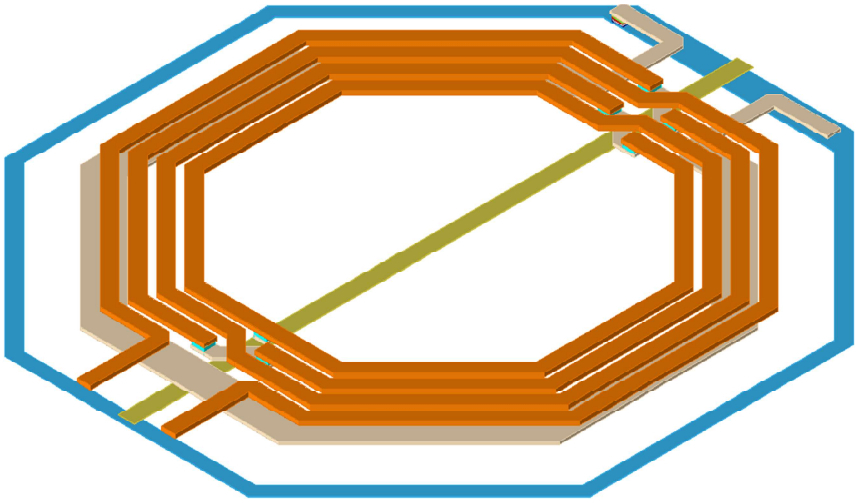
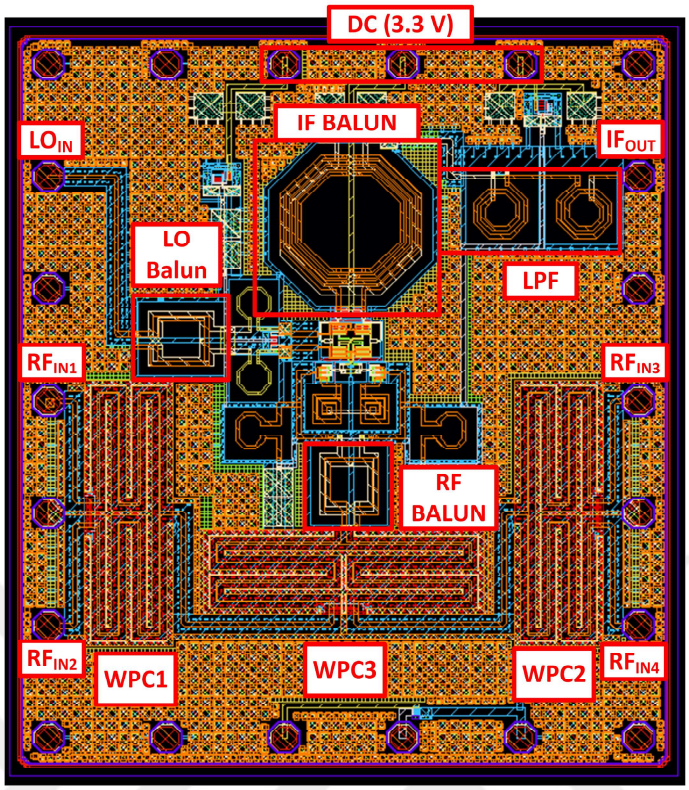
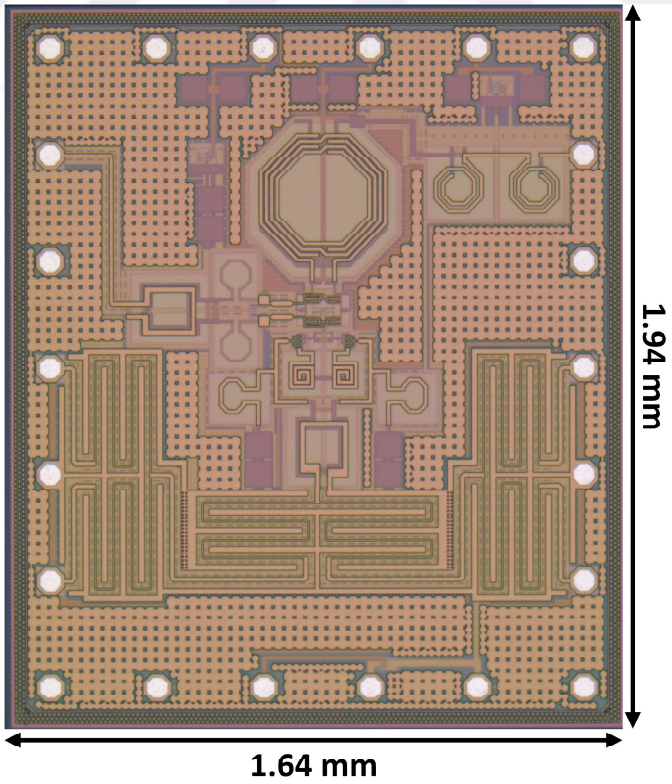


Figure 46: 3-D view of the balun used at the IF output of the balun loaded Gilbert-cell mixer

The balun loaded Gilbert-cell mixer layout and chip micrograph are shown in Fig. 47. The mixer is flip-chip bonded onto a PCB as described in Appendix B and the measured CG and IP_{1dB} are shown in Fig. 48 and Fig. 49 respectively. The mixer is simulated by including the (simulated) effects of the PCB transmission lines. The measurement results agree to within 1.5 dB or so with the simulations. The measured single channel minimum CG is around -17 dB and minimum IP_{1dB} is around 12.5 dBm. To compare the core performance of the mixer, it is simulated without the WPC and the CG vs. RF input power is plotted in Fig. 50. The CG is -2.5 dB with an IP_{1dB} of 2.6 dBm at 26 GHz.



(a) Mixer layout



(b) Mixer chip micrograph

Figure 47: Balun loaded Gilbert-cell mixer layout and chip micrograph

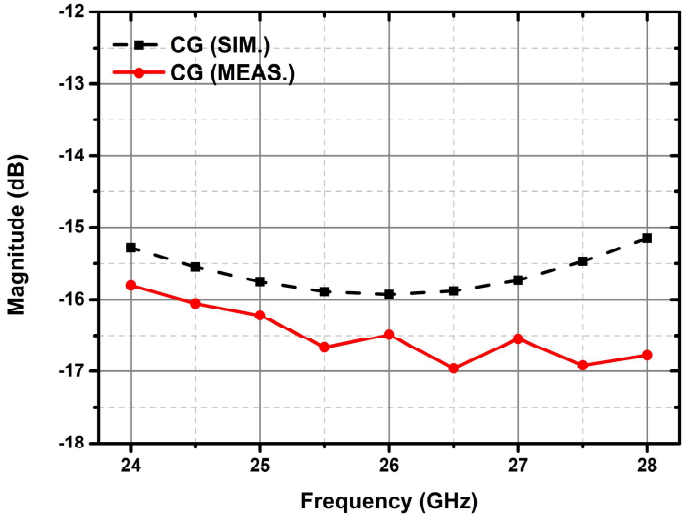


Figure 48: Balun loaded mixer CG vs. RF frequency variation

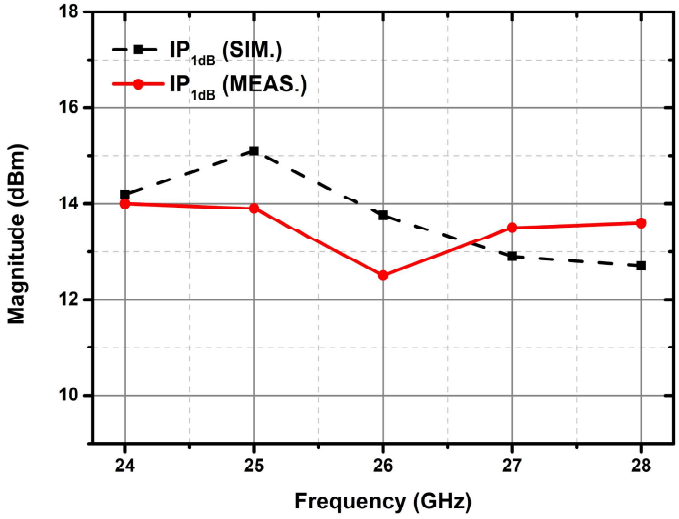


Figure 49: Balun loaded mixer IP_{1dB} vs. RF frequency variation

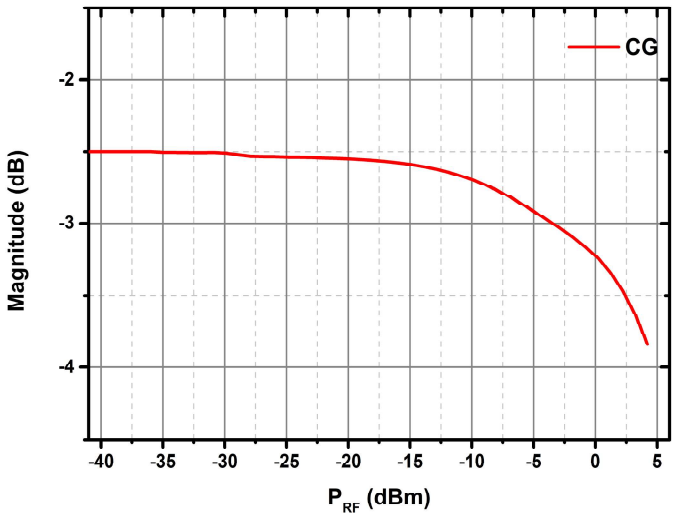


Figure 50: Balun loaded mixer simulated CG vs. RF input power

The performance of various downconversion mixers are compared in Table 5. The balun loaded Gilbert-cell mixer outperforms the other mixers in terms of the defined linearity vs. LO power Figure of Merit (FoM). This mixer also satisfies the requirements defined for the beamforming receiver in Table 3. Therefore, the presented balun loaded Gilbert-cell mixer with fully integrated four-way power combiner and baluns is suitable for use in mmWave 5G beamforming receivers.

Table 5: Downconversion Mixer Performance Comparison

	Balun loaded Gilbert-Cell (sim. w/o WPC)	Emitter Degenerated Gilbert-Cell (sim. w/o WPC)	[38]	[39]	[40]	[41]	[42]
Tech.	130-nm SiGe	130-nm SiGe	65-nm CMOS	180-nm CMOS	180-nm SiGe	180-nm SiGe	130-nm CMOS
RF (GHz)	24 - 28	24 - 28	26 - 30	27 - 40	20 - 32	22 - 39	22 - 29
CG (dB)	-2.5	-2.05	-8	-15.2	3	-8	1
IP_{1dB} (dBm)	2.6	-2.95	9.4^a	-5	-8.05^a	-1.5^a	-11.6^a
P_{DC} (mW)	18.9	29.7	0	0	18	0	6.9
P_{LO} (dBm)	0	6	12^b	6	5	3	-1
SSB NF (dB)	14.5	11.2	-	-	10.5	14	6
Min. Iso. (dB)	68	51	35	60	15	20	36
FoM	0.81	0.06	0.07	0.002	0.08	0.04	0.09

[a] Estimated $IP_{1dB} = IIP_3 - 9.6$ [b] Assumed 10% of power consumption of LO driver.

$$FoM = \frac{OP_{1dB}[mW]}{P_{LO}[mW]}$$

3 Frequency Synthesizer for 5G Transceivers

3.1 Approaches to Frequency Synthesis

5G transceivers system require LO signals at mmWave frequencies with low phase noise/jitter to obtain the SNR desired for high data rates. Various frequency synthesis techniques have been proposed in literature over the years.

Crystal oscillators are commonly used at low frequencies (upto a few hundred MHz) for low phase noise frequency synthesis. Yttrium Iron Garnet (YIG) resonators with very high quality factors can be used to implement frequency synthesizers at mmWave with very low phase noise [43], but they require heterogeneous integration with Si-based technologies.

A phase-locked loop (PLL) can be used as a frequency synthesizer to synthesize a range of frequencies from a given reference frequency. The PLL is a negative-feedback loop that is used to control the output frequency of the voltage-controlled oscillator (VCO). The goal of a PLL is to generate a very accurate frequency output by using an accurate input source (the reference); a low phase noise crystal oscillator is used as the reference to obtain a low phase noise frequency output from a high frequency VCO. Hence, the frequency synthesizer is implemented using a PLL, which locks the phase of the reference with the VCO output. This enables a clean LO signal. Different PLL approaches are reported in the literature, considering the system requirements and the favored frequency conversion approaches. The key performance parameters of a PLL are phase noise, frequency tuning range, stability, and settling time. The period of oscillation of the PLL (and VCO) output signal varies randomly from one cycle to another and this leads to random changes in the zero crossings or the phase of the signal. This is referred to as the phase noise of a source. In the receiver, the phase noise of the synthesizer is responsible for reciprocal mixing (blocker down-conversion) which desensitizes the receiver. In the transmitter, the phase noise leads to emission in undesired frequency bands which violates the spectral mask requirements. In both the transmitter and receiver, the phase noise also corrupts the signal constellation which degrades the SNR of the communication link, which explains why the phase noise is a critical parameter for the frequency synthesizers. The frequency tuning range of a PLL is the range of

frequencies that can be synthesized from the reference frequency. The PLL is a negative feedback control system and it must be ensured that it is stable over its entire tuning range. The PLL must achieve a phase lock at the desired frequency within a certain period of time when its control input is changed. This settling time should be as low as possible to achieve fast switching between different channels in a communication system.

3.2 PLL Fundamentals

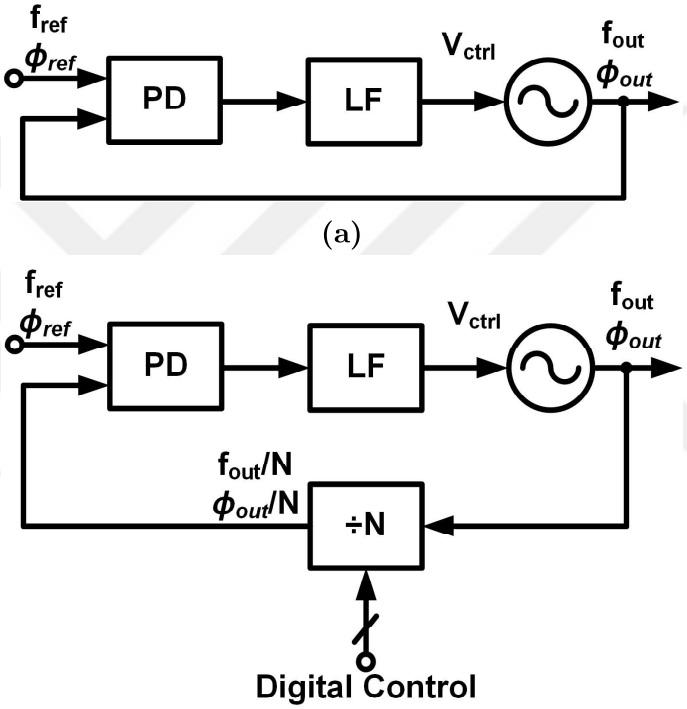


Figure 51: A conceptual PLL (top) and a Type-I PLL (bottom)

A conceptual PLL is shown in Fig. 51a that can adjust the control voltage of the VCO to ensure that the phase of the output of the VCO signal (ϕ_{out}) has a constant difference with the reference signal's phase (ϕ_{ref}). This is achieved by comparing ϕ_{out} and ϕ_{ref} by using a phase detector (PD). The loop filter (LF) then low pass filters the PD output to generate a control voltage, Vctrl for the VCO. This adjusts the ϕ_{out} to ensure that it has a constant difference with ϕ_{ref}. If two signals have a constant phase difference, they have the same frequency. This can be shown as in

(9), where k is a constant with respect to time.

$$\begin{aligned} & \phi_{out} - \phi_{ref} = k \\ \Rightarrow & \frac{d}{dt}\{\phi_{out} - \phi_{ref}\} = 0 \\ \Rightarrow & \omega_{out} = \omega_{ref} \\ \therefore & f_{out} = f_{ref} \end{aligned} \tag{9}$$

The simple PLL in Fig. 51a can only generate the reference frequency. Hence, it cannot be used as a frequency synthesizer. The modified PLL in Fig. 51b can generate multiples of the reference frequency using a frequency divider in the feedback of the control loop. The PLL still maintains a constant phase difference between the reference signal and the signal that is fed back from the VCO as in the aforementioned case. The effect of the frequency (and hence phase) division in the feedback is that the ϕ_{out} that is being compared to the ϕ_{ref}, is N times smaller. So, the loop will try to increase the ϕ_{out} (and hence frequency f_{out}) by N times. If N is incremented in integer steps, then the f_{out} of the PLL can be raised by integer multiples of the f_{ref}. Therefore, (9) becomes (10), where k is a constant with respect to time, and N is the (constant) divisor value. This approach is referred as an integer-N PLL [44].

$$\begin{aligned} & \frac{\phi_{out}}{N} - \phi_{ref} = k \\ \Rightarrow & \frac{d}{dt}\left\{\frac{\phi_{out}}{N} - \phi_{ref}\right\} = 0 \\ \Rightarrow & \frac{\omega_{out}}{N} = \omega_{ref} \\ \therefore & f_{out} = N f_{ref} \end{aligned} \tag{10}$$

In the forward path of the PLL there is one ideal integrator (pole in the origin of the s-plane) in the phase domain due to the VCO, and so this approach is also known as a Type-I PLL. The Type-I PLL includes trade-offs between stability, control voltage ripple, output phase error, and frequency acquisition/capture range. A ripple on Vctrl leads to the modulation on the VCO output, and causes generation of unwanted sidebands. To minimize the ripple, a LF with a lower cut-off frequency must be used. However, this decreases the phase margin and hence the stability of a Type-I PLL. Since a Type-I PLL has one ideal integrator in the forward loop,

which is the VCO, it can be shown that the static (phase) error is not zeroed out by the loop. Hence there exists a constant non-zero phase difference between the ϕ_{ref} and the ϕ_{out}/N. To minimize this static phase error (or offset), the gain of the PD can be increased, which degrades the stability. If the f_{out}/N and f_{ref} are very far apart, then the LF will attenuate the control signal from the PD. Hence, Vctrl will not reach the value required to lock the PLL, which defines a metric called frequency acquisition/capture range; it is the range of frequencies which the PLL can successfully acquire a lock. In a Type-I PLL, the LF bandwidth trades off with the frequency acquisition range. Because as the LF bandwidth increases, the sideband suppression degrades.

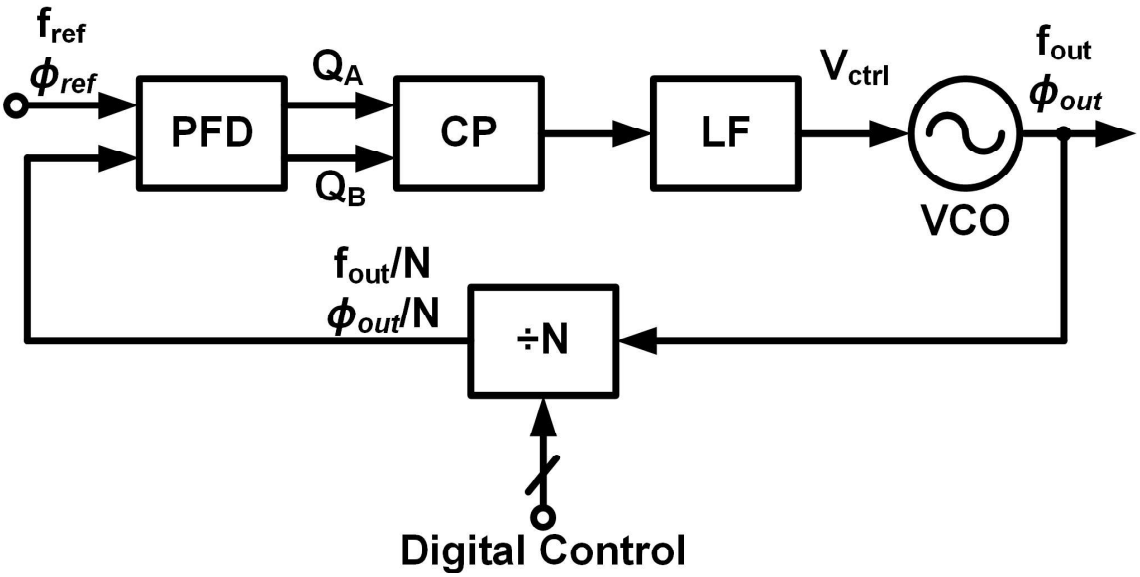


Figure 52: Type-II PLL

To overcome the shortcomings of the Type-I PLL, a Type-II PLL is commonly used. A Type-II PLL consists of two ideal integrators in the forward path. The Type-II PLL in Fig. 52 has a phase-frequency detector (PFD) instead of a PD. The PFD acts as a frequency detector when the divided VCO output frequency is far from the reference frequency, and it operates as phase detector when they are close to each other. The PFD outputs two digital signals which have an average difference that represents the frequency or the phase difference at the PFD input. Vctrl needs to be a dc signal and the digital signals from the PFD cannot be directly used as a control signal. The PFD output could be passed through a LPF as in a Type-I PLL to generate Vctrl, but by introducing the charge pump (CP) a second integrator

is introduced in the loop which allows the static phase error to be cancelled. The Type-II PLL does not suffer from the limited frequency acquisition range of the Type-I PLL, and can be designed to be a stable loop while having a LF that can attenuate the ripples in Vctrl such that the unwanted side-bands at the outputs are minimized.

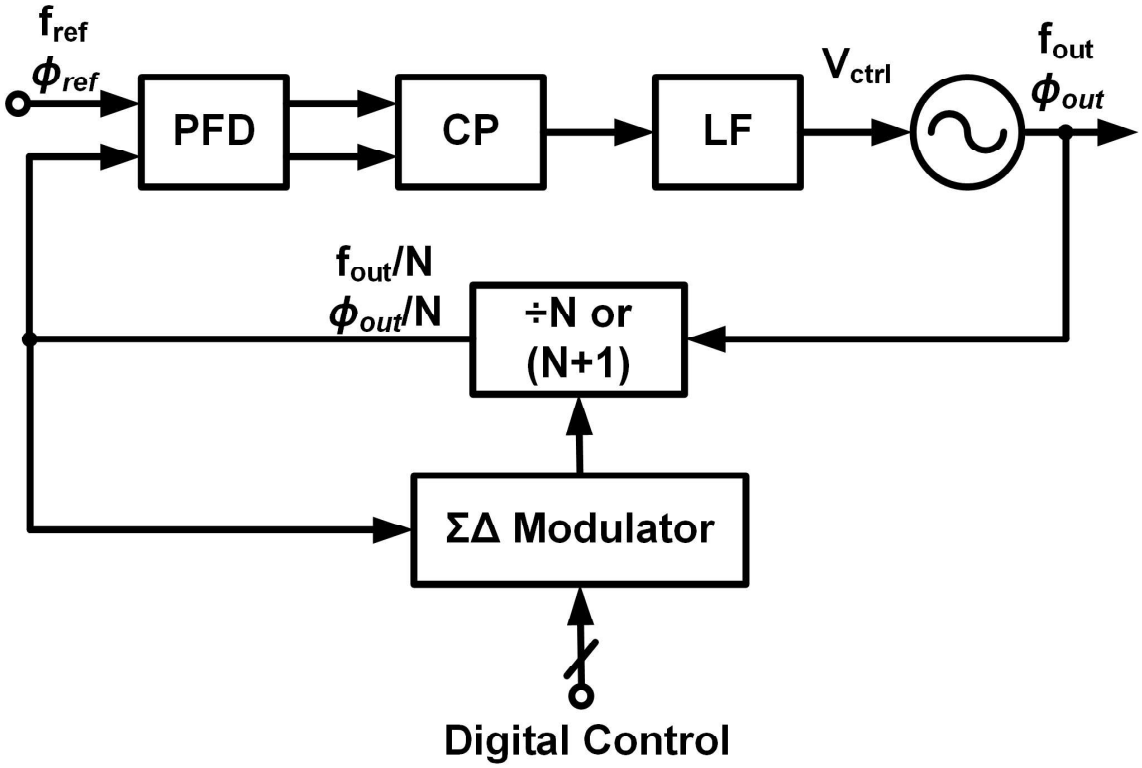


Figure 53: Fractional-N PLL

If non-integer multiples of the reference frequency are required, then the integer-N topology must be modified as in Fig. 53 to include a divider that can switch between two different divisor values for different time periods. By controlling the time for which the divisor is at N and at N+1, the average/effective divisor value can be set to be any fractional value in between N and N+1. The periodic switching of the divisor leads to generation of fractional spurs at the PLL output, and so a sigma-delta modulator (SDM) is required to randomize the divisor switching. The noise introduced by the SDM itself must be minimized by noise shaping and dithering which leads to complex circuitry.

3.3 PLL for Frequency Synthesis

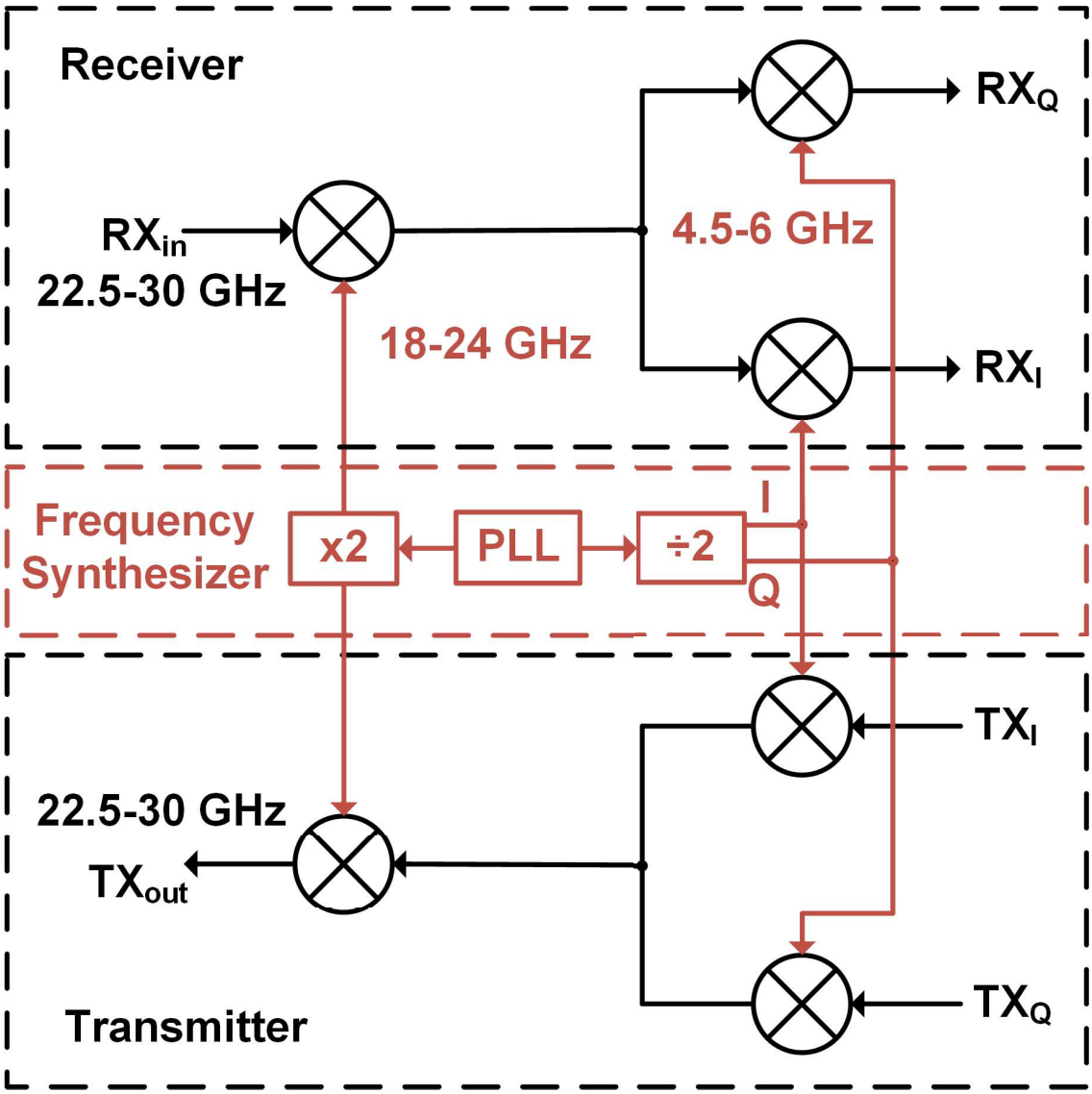


Figure 54: Sliding-IF transceiver

The present work proposes a frequency synthesizer suitable for LO signal generation for the sliding-IF transceiver of Fig. 54. The sliding-IF transceiver has been favored over heterodyne and direct conversion transceivers for 5G applications as demonstrated by its widespread adoption [45, 46, 25]. This is because unlike direction conversion transceivers, sliding-IF transceivers do not require high frequency quadrature signal generation. The sliding-IF transceiver only requires a single frequency source frequency translation purposes unlike the heterodyne transceiver. Overall, this makes sliding-IF transceivers the most promising transceiver architecture for 5G transceiver modules.

3.3.1 Linear Model of the Type-II PLL

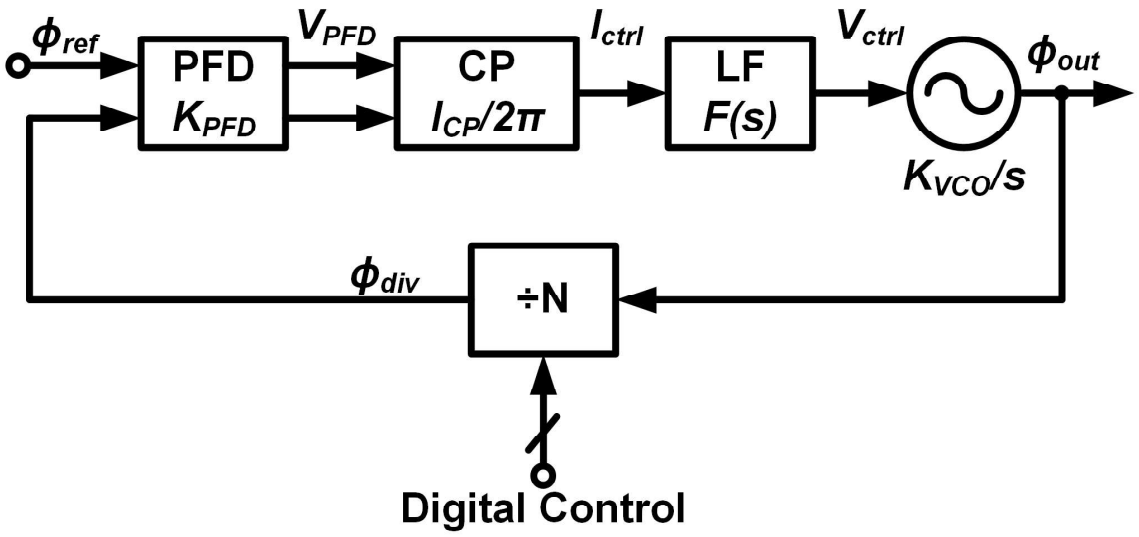


Figure 55: Linear model of Type-II PLL in phase domain

For analysis purposes a linear model of the Type-II PLL can be constructed in the phase domain as in Fig. 55 and control theory can be applied to determine the loop parameters to obtain a stable loop [44]. The phase domain transfer characteristics of the sub-blocks of the PLL are shown in Fig. 55. The open-loop gain is used to determine the phase margin (PM) of the PLL which in turn shows the stability of the PLL.

$$\begin{aligned} H(s) &= \frac{\phi_{out}}{\phi_{in}} = \frac{I_{ctrl}}{\phi_{in}} \times \frac{V_{ctrl}}{I_{ctrl}} \times \frac{\phi_{out}}{V_{ctrl}} \\ \therefore H(s) &= \frac{I_{CP}}{2\pi} \cdot F(s) \cdot \frac{K_{VCO}}{s} \end{aligned} \tag{11}$$

$$\beta = \frac{\phi_{div}}{\phi_{out}} = \frac{1}{N} \tag{12}$$

$$\begin{aligned} \beta H(s) &= \frac{\phi_{out}}{\phi_{in}} \times \frac{\phi_{div}}{\phi_{out}} = \frac{\phi_{div}}{\phi_{in}} \\ \therefore \beta H(s) &= \frac{1}{N} \cdot \frac{I_{CP}}{2\pi} \cdot F(s) \cdot \frac{K_{VCO}}{s} \end{aligned} \tag{13}$$

$$\frac{\phi_{out}}{\phi_{ref}}(s) = \frac{H(s)}{1+\beta H(s)} = \frac{\frac{\phi_{out}}{\phi_{in}}}{1+\frac{\phi_{div}}{\phi_{in}}}$$
$$= \frac{\phi_{out}}{\phi_{in}+\phi_{div}} = \frac{\phi_{out}}{\phi_{ref}} \tag{14}$$
$$\therefore \frac{\phi_{out}}{\phi_{ref}}(s) = \frac{I_{CP}K_{VCO}NF(s)}{2\pi Ns + I_{CP}K_{VCO}F(s)}$$

(11) and (12) are used to derive the open-loop gain of the PLL shown in (13). (13) is then used to determine the closed-loop gain of the PLL in (14). (13) and (14) can be used to analyze the stability, transient, and phase noise performance of the PLL.

3.3.2 PLL design procedure

The design of integer-N PLL begins with the selection of the reference frequency f_{ref}. This frequency is dependent on the channel spacing requirement of the communication system. In an integer-N PLL the frequency step size is determined by f_{ref}. In mmWave 5G communication systems channel bandwidths in the range of 50 MHz to 400 MHz have been allocated [5]. In this work, an f_{ref} of 100 MHz is selected which allows a minimum frequency step size of 100 MHz for the frequency synthesizer.

The reference frequency can be supplied using an external high precision crystal oscillator. One such oscillator is the ABRACON ASGCXA100MHz reference crystal oscillator with a phase noise of -141.5 dBc/Hz @ 1MHz offset from a 100 MHz carrier.

The tuning range required by the communication system along with the choice of f_{ref} fixes the feedback division ratio of the PLL. In this work, a nominal tuning range of 9 GHz - 12 GHz is selected for determining the divider division ratio. A programmable divider that can perform division using ratios from 90 to 120 is therefore required.

From the above mentioned parameters, the loop bandwidth of the PLL can be set. This is done by taking into consideration that the linear model of the PLL that was discussed previously is a continuous time approximation of a discrete system [44]. In order for the continuous time approximations to hold the maximum PLL bandwidth is constrained to be around 10% of f_{ref}. So, a loop bandwidth of at most

10 MHz can be used while utilizing the linear model of the PLL. Once the PLL loop bandwidth is set, the required component values of the individual sub-blocks can be determined.

Some of the considerations that need to be taken in selecting the PLL loop bandwidth are discussed briefly. The PLL loop bandwidth affects the transient response, phase noise, and spurious output performance of the PLL. The phase noise of the VCO in the PLL experiences a high-pass transfer function to the output of the PLL. The PLL suppresses the phase noise of the VCO within the PLL loop bandwidth. So, a wide PLL loop bandwidth suppresses VCO phase noise to a greater extent. But the phase noise contributions due to the rest of the loop components experiences a low-pass transfer function to the output of the PLL. This means that the phase noise contributed by the PLL components (other than VCO) is not suppressed within the PLL loop bandwidth. So, a narrow PLL loop bandwidth suppresses the phase noise contributions due to loop components other than VCO. From a transient response point of view, a wider loop bandwidth improves the time taken for the PLL to lock. At the same time a wider loop bandwidth leads to greater reference spurs at the PLL output. Finally, as discussed earlier, the PLL must have enough PM to ensure that it is stable under all conditions. Therefore, the selection of the PLL loop bandwidth is of critical importance to obtain the optimal performance.

A PLL loop bandwidth of 1 MHz is initially selected to reject the phase noise of the loop components other than the VCO, and to reduce the spurious components at the PLL output. The remaining parameters to be determined are the VCO tuning gain (K_{VCO}), CP current, and LF component values. Since the CP current and LF component values can be modified with relative ease when compared to the K_{VCO}, the VCO is designed first and then the remaining parameters are determined.

3.4 PLL Sub-block Design

In this section the design of mmWave VCOs is described followed by a brief discussion of the design considerations of the other PLL loop components.

3.4.1 VCO Design

Harmonic oscillators based on LC tank resonators will be considered in this work because of their excellent phase noise performance when compared to other oscillators such as ring oscillators. Harmonic oscillators use a frequency selective component - a resonant circuit - to generate a signal at the desired frequency. While series resonant LC circuits have been investigated in literature [47], the parallel LC tank, shown in Fig. 56, is still the most commonly used resonant component in harmonic oscillators. Harmonic oscillators utilize a positive feedback circuit or equivalently a negative resistance circuit to overcome the parasitic resistances which are inherent in the LC tank and thus sustain steady-state oscillation. The method used to generate the negative resistance or to establish the positive feedback gives rise to the various oscillator topologies described in literature.

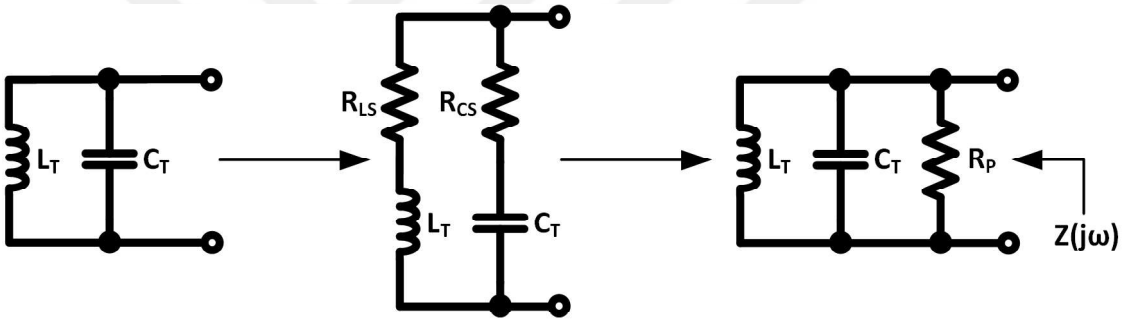


Figure 56: LC resonator with parasitics

VCO Design Considerations

The phase noise (PN), tuning range (TR), and K_{VCO} are the main performance parameters of interest in this work.

Leeson proposed an empirically derived phase noise model for oscillators [48] as shown (15).

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left\{F \cdot \frac{4kTR_p}{A_{pk}^2} \cdot \left[1 + \left(\frac{1}{2Q_T} \cdot \frac{\omega_0}{\Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{\Delta\omega}\right)\right\} \qquad (15)$$

In (15), F is the noise factor of the amplifier/active devices used to sustain the oscillation, k is the Boltzmann constant, T is the absolute temperature in Kelvin,

R_p is the parallel equivalent resistance of the LC tank, A_{pk} is the peak signal swing at the input of the active devices, Q_T is the quality factor (Q) of the resonant tank, ω_0 is the (angular) frequency of oscillation, $\Delta\omega$ is the (angular) offset frequency, and $\Delta\omega_{1/f^3}$ is the upconverted flicker noise corner frequency.

From (15) it can be deduced that there are three distinct regions in the output spectrum of the VCO. The noise contributed by the tank parasitic resistance (R_P) leads drops off at 20 dB/dec, while the upconverted flicker noise leads to a close-in phase noise profile which drops off at 30 dB/dec. The far-out phase noise of the VCO is flat and is dominated by buffers and other circuitry that follow the VCO. From (15), it can be concluded that the phase noise of an oscillator can be minimized by maximizing the resonator quality factor and by increasing the voltage swing at the tank. It must be noted that the negative resistance generating devices must maintain active mode of operation in order not to degrade the tank Q and consequently the phase noise.

The tuning range of the VCO is limited by the tunability of the resonant circuit. While inductor switching has been investigated in literature [49], variable capacitance based designs are more suitable for VCOs operating in a single band with low phase noise requirements. A variable capacitance may be implemented using MOS varactors or by switching fixed capacitors in and out of the resonant tank or by a combination of both techniques. The K_{VCO}, which is dependent on the tunability of the resonant circuit, must be kept low to avoid undesirable spurs at the output of the PLL.

In this work, a cross-coupled topology is used to generate the negative resistance rather than a Colpitts topology. The cross-coupled topology finds widespread application due to its robust performance - particularly its startup performance. The phase noise performance of HBT cross-coupled and Colpitts VCOs were compared in [50]. The simulation results in [50] showed that the cross-coupled oscillator can attain comparable and even better phase noise performance than the Colpitts oscillator. This combined with its robust startup performance makes the cross-coupled oscillator a suitable choice for low phase noise VCOs.

VCO designed for 18 GHz

A cross-coupled HBT based VCO with its base bias decoupled from the tank [51] is shown in Fig. 57. Decoupling the base of the cross-coupled transistors from the tank allows the DC bias of the base to be set independently. This allows a larger voltage swing in the tank before the transistors leave the active mode of operation. The VCO is designed for operation at 18 GHz at a low supply voltage of 1.6 V. The base bias is set to enable maximum swing at the tank, while a tail inductor is used instead of a current source for voltage headroom improvement. The 0.9 fF capacitors are used for decoupling purposes. The resonator is composed of a 130 pH inductor and two varactors of different sizes - one for coarse frequency tuning and one for fine frequency tuning. The capacitors provide around 300 fF of continuous frequency tuning. The overall varactor Q is around 12 and the inductor Q is around 20 at 18 GHz resulting in an overall tank Q of 7.5 using (16).

$$\frac{1}{Q_T} = \frac{1}{Q_C} + \frac{1}{Q_L} \tag{16}$$

The VCO chip is shown in Fig. 58. As shown in Fig. 59 the measured tuning range is from around 15.5 GHz - 18.5 GHz (17.6 %) - there is shift in the center frequency and a decrease in the tuning range when compared to the simulation results. The measured phase noise is around -82 dBc/Hz @ 1MHz offset from a 17 GHz carrier which is around 5 dB higher than expected.

The tuning range and phase noise performance of the designed VCO needed to be improved. The discussion of the improvements made to the design follows.

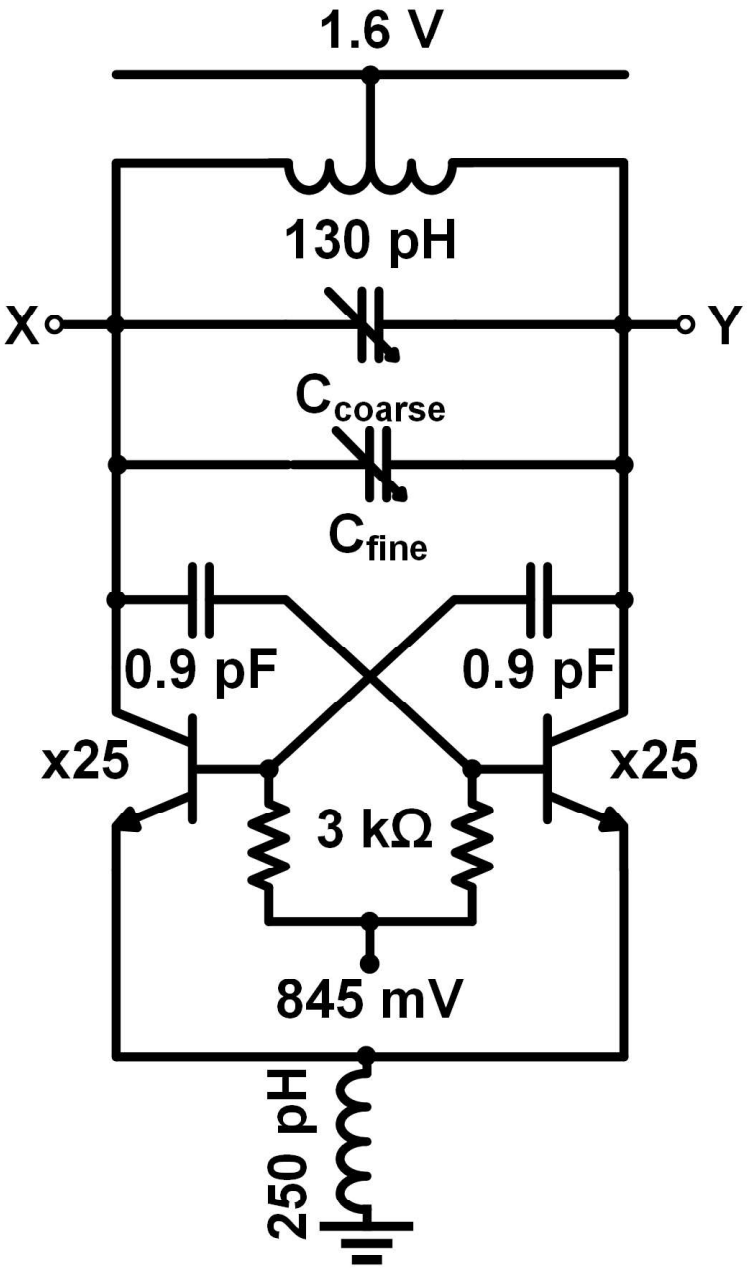


Figure 57: Bias decoupled HBT VCO

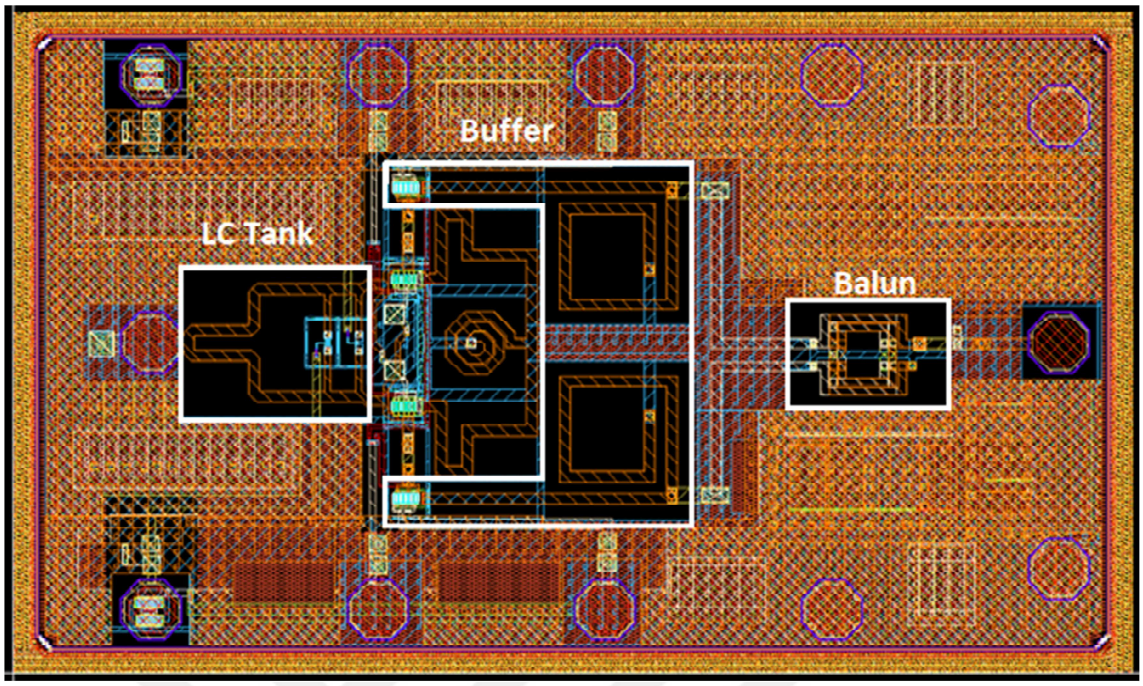


Figure 58: Layout of bias decoupled HBT VCO for 18 GHz operation

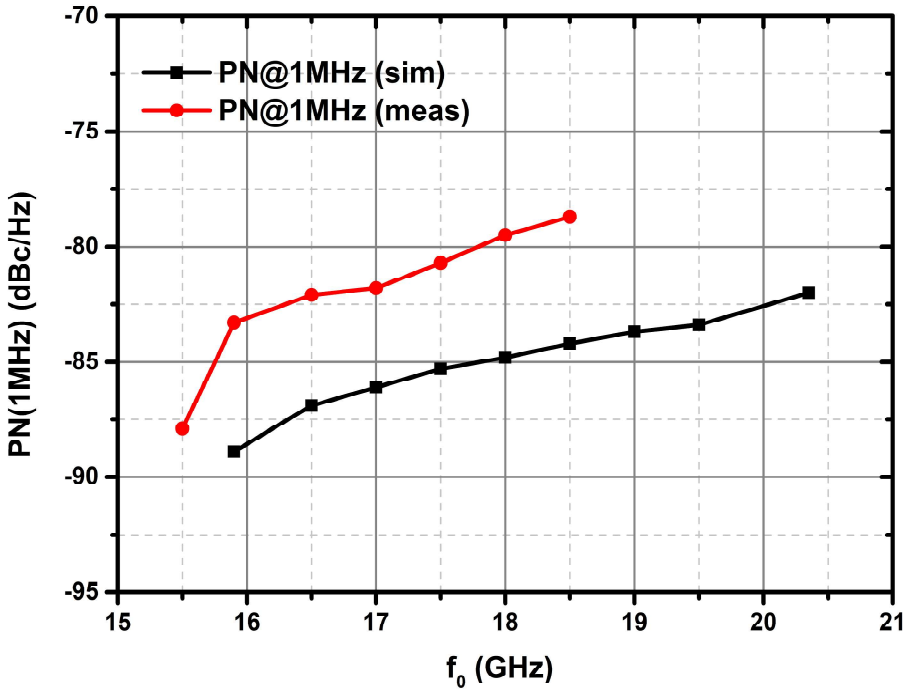
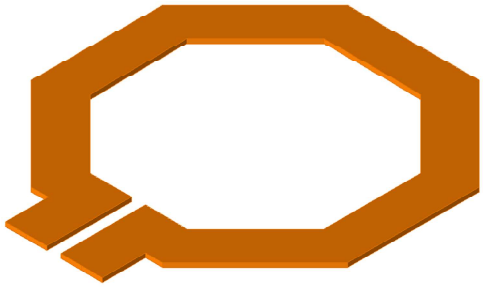


Figure 59: Phase noise vs. frequency of VCO for 18 GHz operation

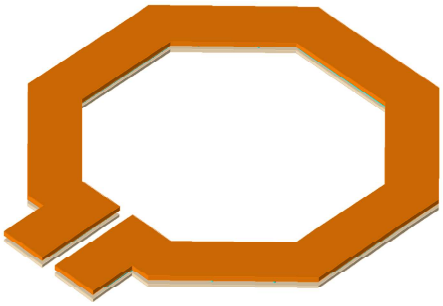
VCO designed for 10 GHz

A number of design modifications were made to enhance the performance of the aforementioned VCO.

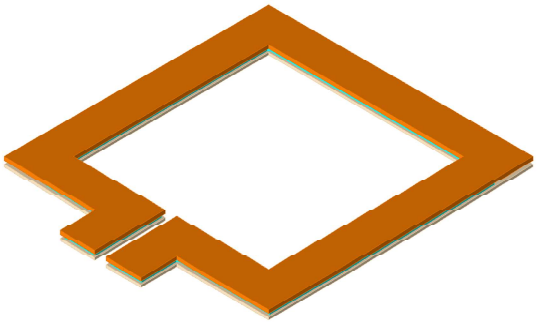
To improve the phase noise performance of the VCO, the Q of the resonator needed to be improved. The improvement of the inductor Q factor is first investigated. The Q of the three different 300 pH inductors is shown in Fig. 60 were simulated and the results are shown in Fig. 61.



IND1: Inductor on TM2



IND2: Octagonal stacked Inductor on TM2+TM1



IND3: Square stacked Inductor on TM2+TM1

Figure 60: Various inductor structures studied for VCO resonator

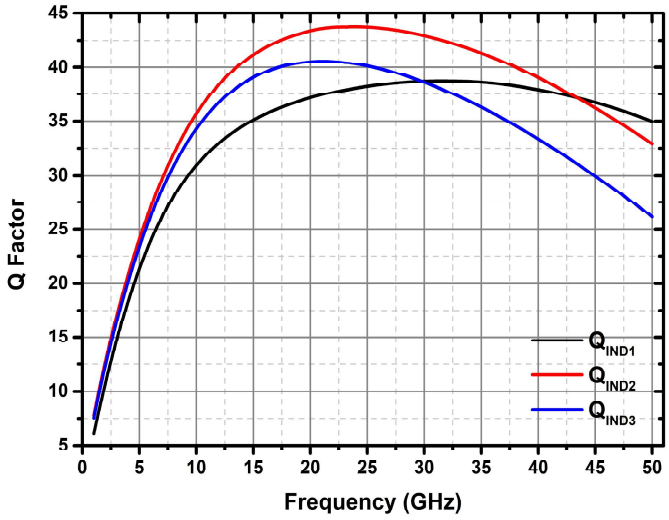


Figure 61: Quality factor of the inductors under investigation

The first inductor is composed of an octagonal coil on TM2, whereas the second structure is composed of two identical coils stacked on top of each other on TM2 and TM2 and connected using vias. The final inductor is a stacked square inductor. It is evident from Fig. 61 that the Q of the indcutor improves when a stacked structure is used. This is due to the reduced parasitic resistance that is present when stacking is used. Also, the octagonal stacked inductor exhibits a better Q than the square stacked inductor. The octagonal stacked inductor has a Q of around 36 at 10 GHz. Therefore, an octagonal stacked inductor structure is adopted for the resonator.

The quality factor of a MOS varactor of size $15 \times 9.74\mu m \times 0.8\mu m$ is simulated as the varactor voltage is varied from 0.65 V to 2.65 V. The results in Fig. 62 show that the Q of the varactor is quite low when compared to the inductor at the frequencies of interest. The varactor has a Q of around 16.75 at 10.5 GHz. At higher frequencies, this quality factor degrades further as can be seen from the Q of the varactor at 11.5 GHz.

To obtain a large tank Q, the VCO is designed at a lower frequency of 10.5 GHz. This ensures that both the inductor and varactor Q are large so as not to degrade the tank Q significantly. This has the added advantage that high frequency LO routing can now be avoided. The schematic of the VCO is shown in Fig. 63.

Bias decoupling is still used to ensure that the voltage swing at the tank can be maximized. Additionally, the supply voltage is increased to 3.3 V, and a tail current

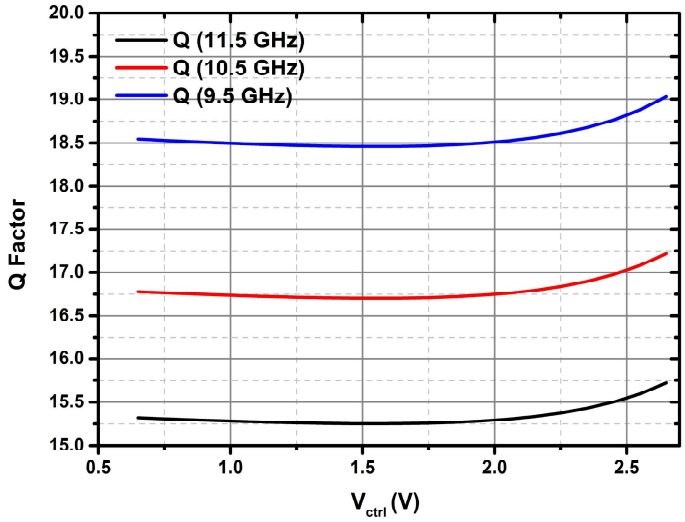


Figure 62: Quality factor of the varactor under investigation

source is introduced along with a tail current filter [52]. The tail current filter is composed of C_{Tail}, L_{Tail}, and the parasitic capacitances present at that emitter of the cross-coupled HBT pair. The tail filter is resonant at twice the oscillating frequency and this creates a high impedance at that frequency at the emitter of the HBT pair. C_{Large} provides a low impedance path to ground for the tail filter and it also filters out the noise from the current source. The device size and bias is optimized for low phase noise operation.

To enhance the tuning range, a discrete capacitor bank is utilized instead of multiple analog varactor control signals. If multiple analog control voltages are used to tune the VCO, then the PLL is required to have a multiloop architecture which complicates the design process. Instead, with digital control, fixed MIM capacitors can be switched into and out of the tank to tune the output frequency of the VCO. To cover the required tuning range a 4-bit binary weighted capcitor bank is designed. The switching of the capacitors in the bank is done using a high voltage NMOS device with an inverter used to set the appropriate bias voltage across its drain and source [53]. Analog control of the VCO is realized using a varactor whose tuning characteristic is shown in Fig. 64.

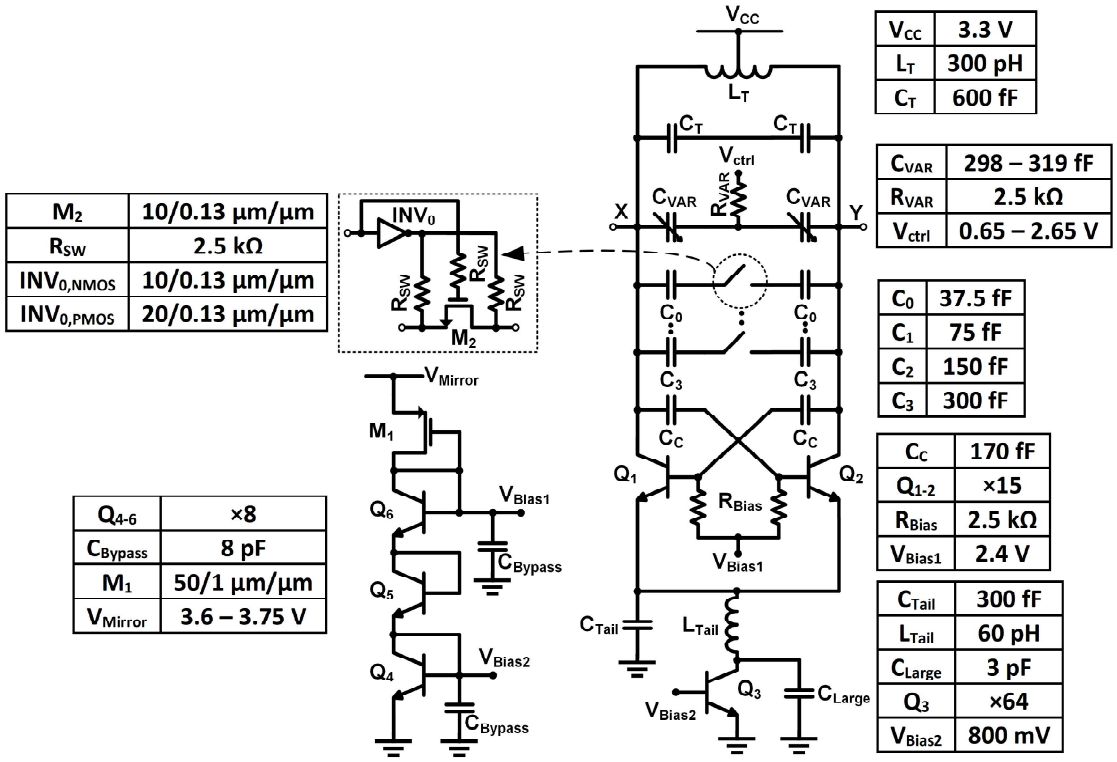


Figure 63: VCO for frequency synthesizer

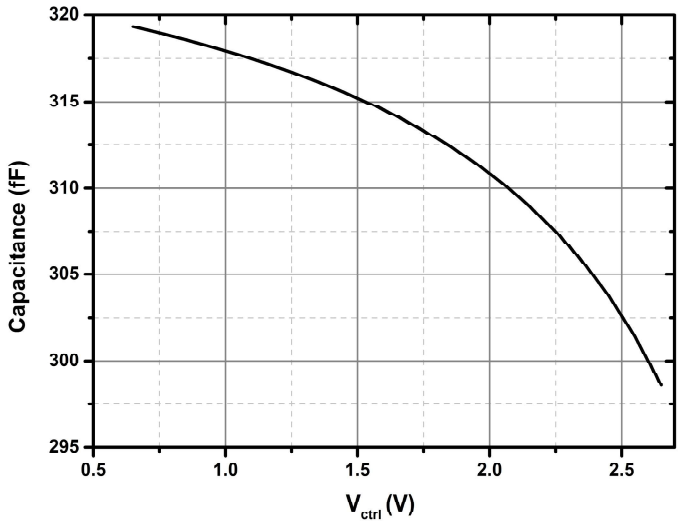


Figure 64: Varactor tuning characteristic

The bias voltages for the cross-coupled HBT pair and the tail current source are provided using a current mirror. The supply voltage of the current mirror will be connected to a low dropout regulator (LDO) such as the Texas Instruments TPS7A88 which has a low noise (3.8 μV_{RMS}) and wide output range (0.8 - 5.0 V). This biasing scheme is adopted to overcome process and temperature variations that may occur. The tail current variation under different process corners is simulated and is shown in Fig. 65. As it can be seen, adjusting the current mirror supply allows the tail current to be varied to obtain the desired value. The VCO draws 3.7 mA from a 3.3 V supply under nominal conditions.

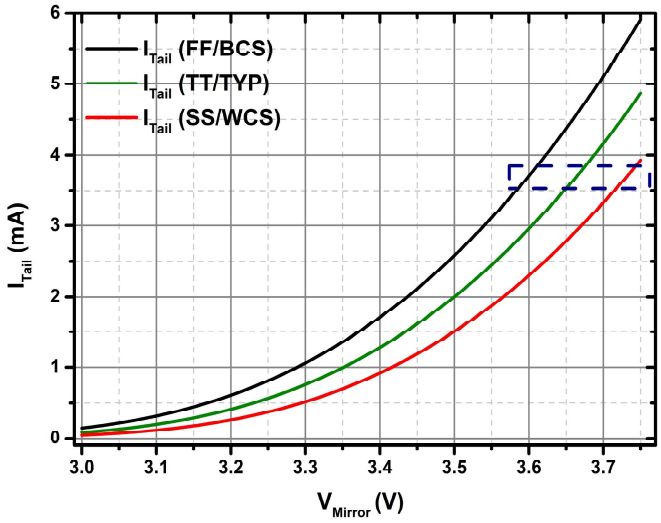


Figure 65: Tail current under varying mirror supply across process corners

The VCO tuning curves are shown in Fig. 66. As the analog control voltage is swept from 0.65 V to 2.65 V and the capacitors in the bank are switched the output frequency of the VCO can be tuned from 9.4 GHz to 11.4 GHz, for a simulated tuning range of 19.2%. It must be noted that there is overlap between the VCO tuning curves which is required for proper functionality in a PLL. The average K_{VCO} is around 75 MHz/V.

The close-in and far-out phase noise of the VCO is simulated at the two extremes of the tuning range, as well as at the center frequency and is shown in Fig. 67 and Fig. 68 respectively. The phase noise varies from around -115 dBc/Hz to -118 dBc/Hz @ 1 MHz offset from carriers at 11.25 GHz and 9.5 GHz. The phase noise is -116 dBc/Hz @ 1 MHz offset from a 10.5 GHz carrier.

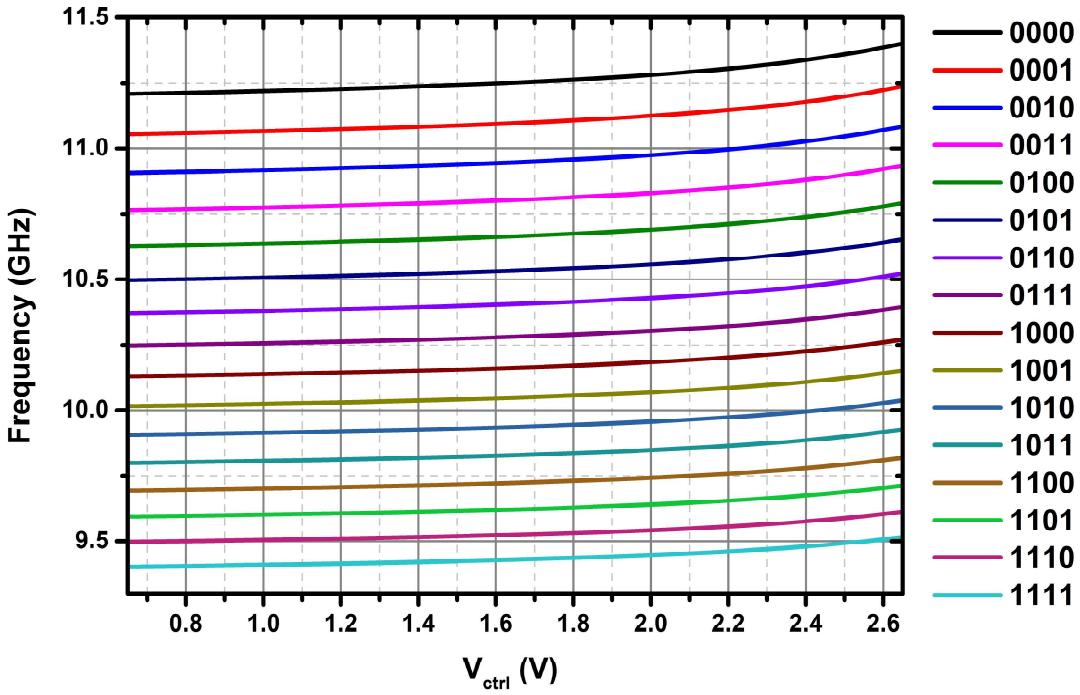


Figure 66: VCO tuning curves

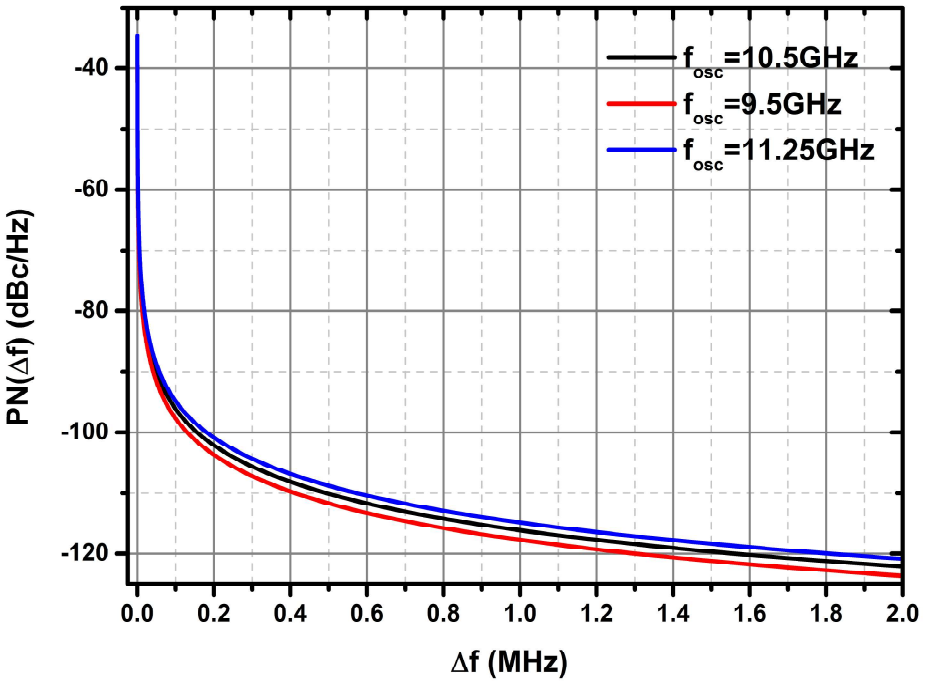


Figure 67: Close-in VCO phase noise

Table 6: VCO Performance Comparison

REF	Tech.	Freq. Range (GHz)	TR (%)	PN (dBc/Hz @ 1 MHz)	P_{DC} (mW)	FoM	FoM_T
This Work (Sim.)	130 nm SiGe	9.4 - 11.4	19.2	-116	12.2	185.48	191.16
[54]	120 nm SiGe	9.9 - 12.45	22.8	-120.5	82	182.33	189.49
[53]	130 nm SiGe	16 - 19	17.1	-110.6	27.5	181.07	185.75
[55]	90 nm CMOS	9.4 - 11.5	20.1	-117	16	185.34	191.40
[56]	65 nm CMOS	6.39 - 14	74.6	-117	10.3	187.04	204.50
[57]	250 nm SiGe	12.43 - 13.08	5.1	-123	93	185.43	179.57

$$FoM = -PN(\Delta f) + 20\log(\frac{f_0}{\Delta f}) - 10\log(\frac{P_{DC}}{1mW})$$

$$FoM_T = FoM + 20\log(\frac{TR[\%]}{10\%})$$

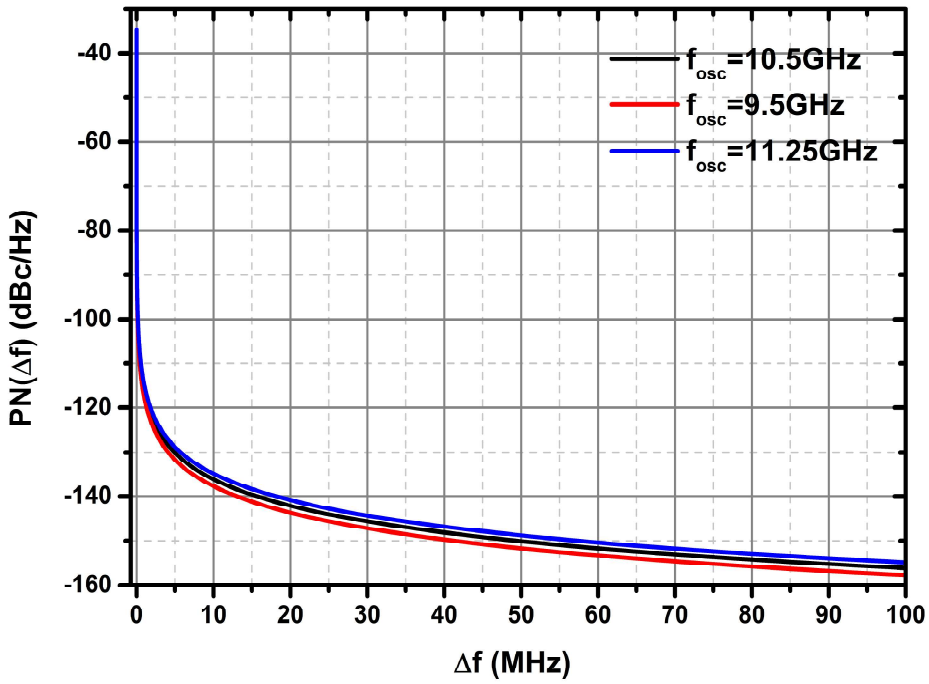


Figure 68: Far-out VCO phase noise

Table 6 shows the performance comparison of the VCO to comparable VCOs in literature. As it can be seen, the core VCO achieves a moderate tuning range and phase noise performance while dissipating low power. From the phase noise and tuning range FoM point of view, it is only behind [56] and either has comparable or better performance than the other VCOs.

3.4.2 PFD/CP/LF Design Considerations

In this section the design considerations for the PFD, CP, and LF will be discussed.

The tri-state PFD shown in Fig. 69 is utilized in this design and the phase noise contributions of the PFD can be minimized by increasing the width of the devices in the NOR gate [58]. The time delay τ, implemented using a buffer, is introduced in the reset path to remove the deadzone - the input region where the PFD does not respond to very small phase differences. The behavioral simulation result of the PFD transfer function is plotted in Fig. 70. The average of the difference of the PFD output linearly increases with the input phase difference.

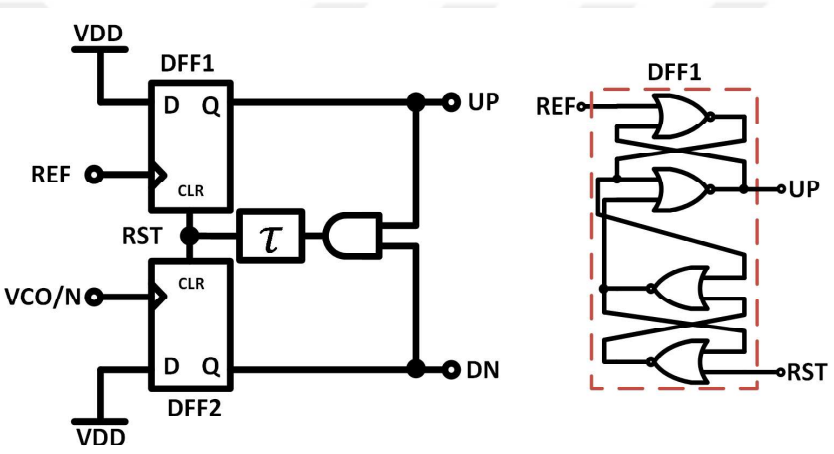


Figure 69: Tri-state PFD

The source switched charge pump topology, shown in Fig. 71, is a relatively simple CP that provides a high output resistance due to the degeneration effect of N_1 and P_2 [44]. A nominal CP current of 1 mA is set by considering the trade-offs between dynamic power consumption and the effect of I_{CP} on loop dynamics. The cascade of PFD and CP is behaviorally simulated and the results are plotted in Fig. 72 and the discrete steps in the CP output voltage can be observed as expected.

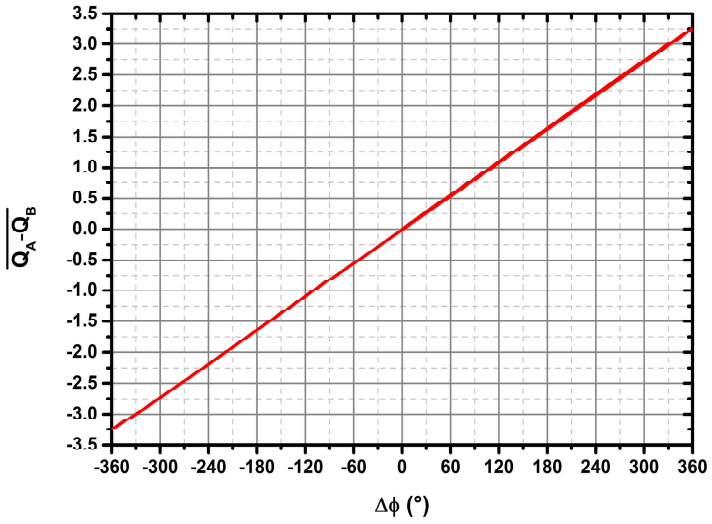


Figure 70: Behavioral transfer function of the PFD

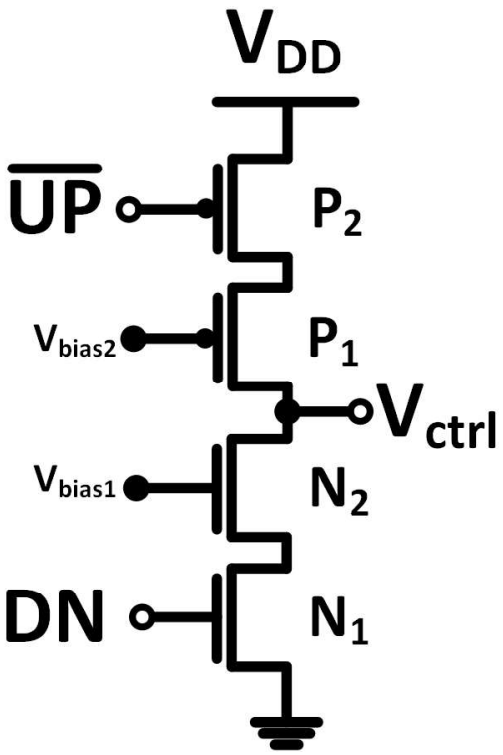
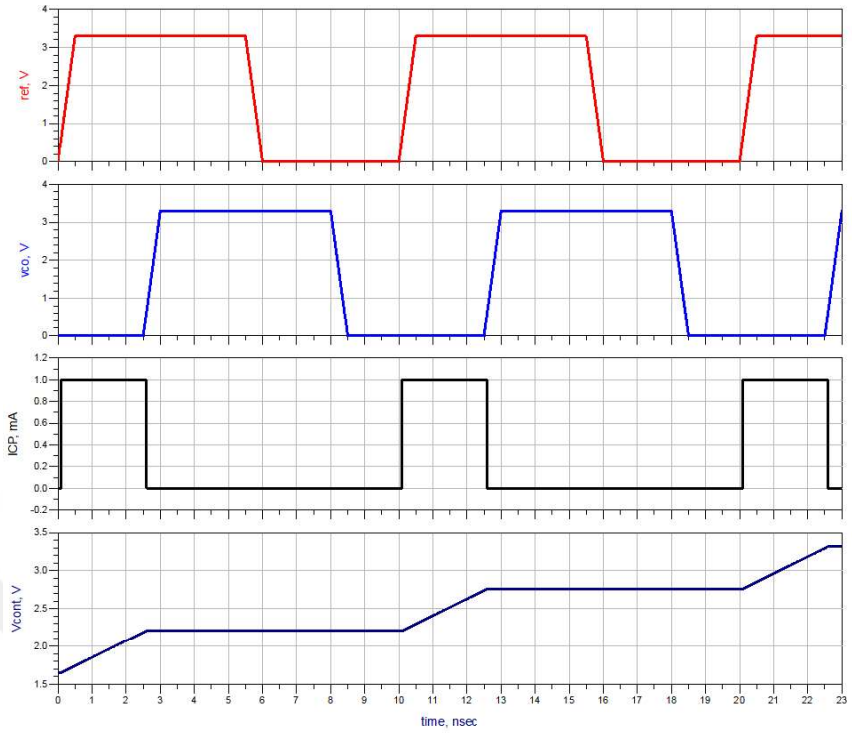
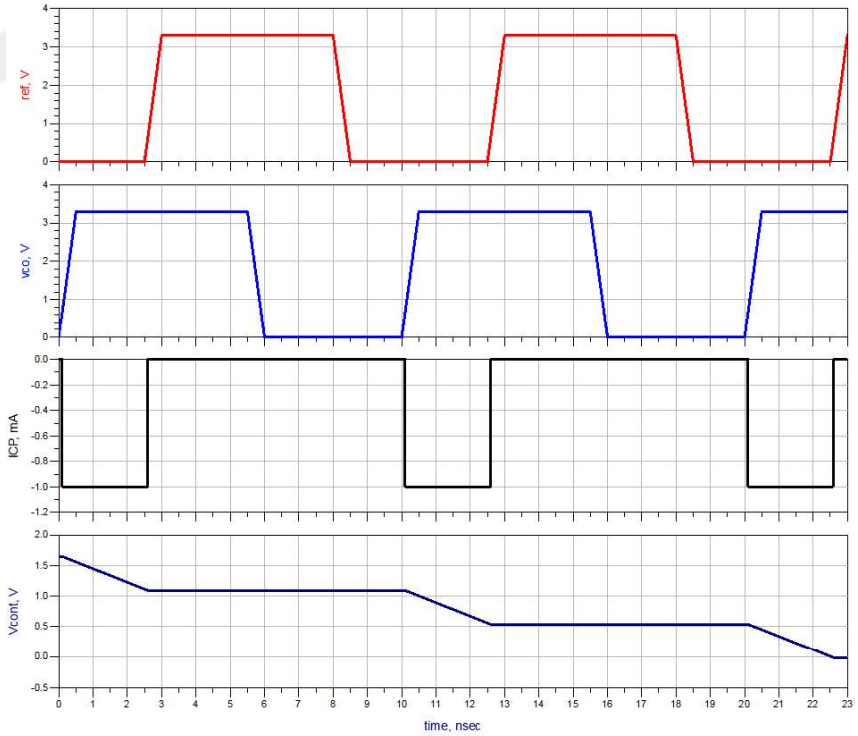


Figure 71: Source switched charge pump



(a) Reference leads feedback signal



(b) Reference lags feedback signal

Figure 72: Behavioral CP output for different PFD outputs

A third-order passive loop filter shown in Fig. 73 is utilized to suppress the spurious response of the PLL and the noise at the output at large frequency offsets [59]. Since there are no closed form solutions to designing the third-order loop [59], Mathworks SIMULINK is used to numerically calculate the required loop filter component values. For a K_{VCO} of 75 MHz/V, a loop bandwidth of 1 MHz, and a phase margin of around 45°, the values of the loop filter components are summarized in Table 7.

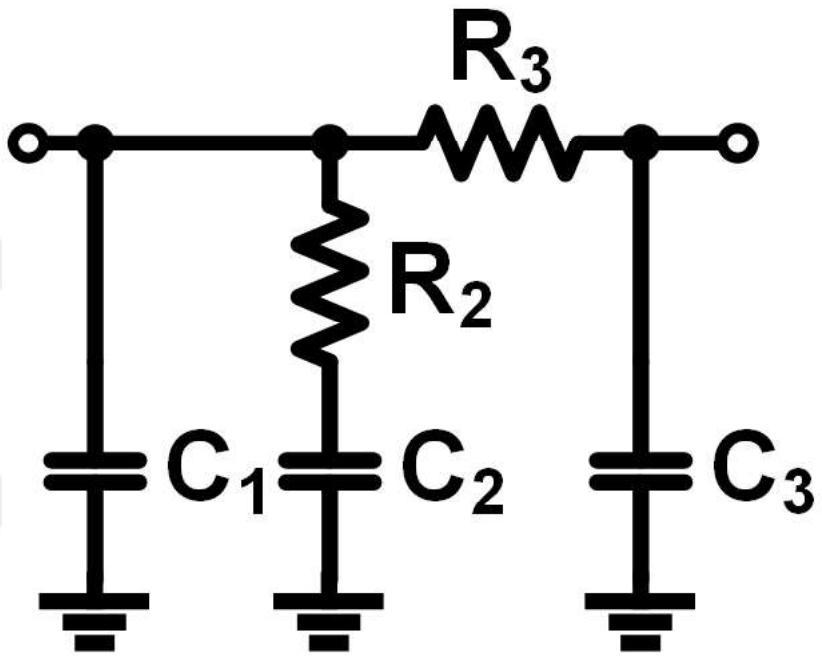


Figure 73: Third-order passive loop filter

Table 7: PLL loop parameters

K_{VCO}	75 MHz/V	C_1	4.37 pF
I_{CP}	1 mA	C_2	48 pF
$min(/N)$	90	C_3	314 fF
Loop BW	1 MHz	R_1	8 kΩ
Target PM	45°	R_2	102 kΩ

The impedance transfer function of the loop filter is plotted in Fig. 74. The impedance of the loop filter falls at higher frequencies, thereby high frequency noise at the CP output modulates the VCO control voltage to a lesser extent thus minimizing the spurs and noise at large offsets.

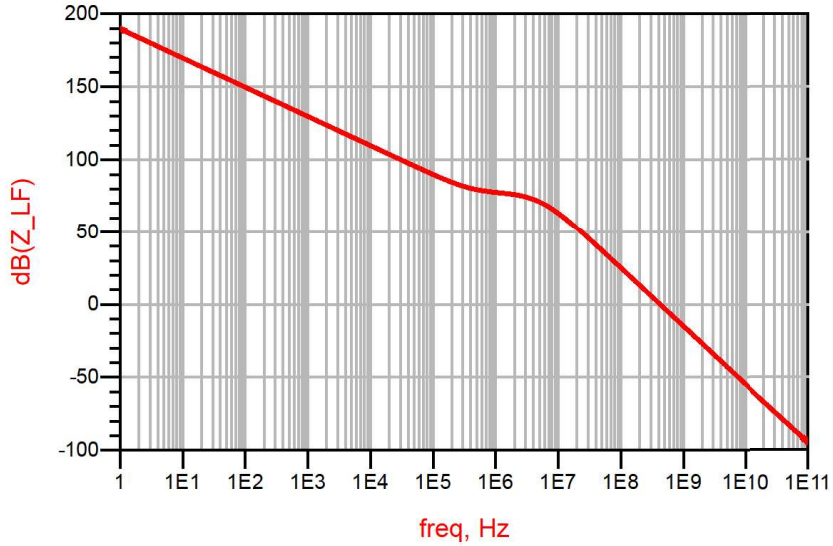


Figure 74: Loop filter transfer function

The open-loop Bode plot of the PLL loop in MATLAB shows a PM of 44° with a unity gain bandwidth of around 1 MHz as shown in Fig. 75. While a PM of greater than 60° is usually the criteria set for stability, in this case a lower PM is justified since this is the lowest feedback divisor value (90), and the PM and hence stability will improve for higher feedback divisor values.

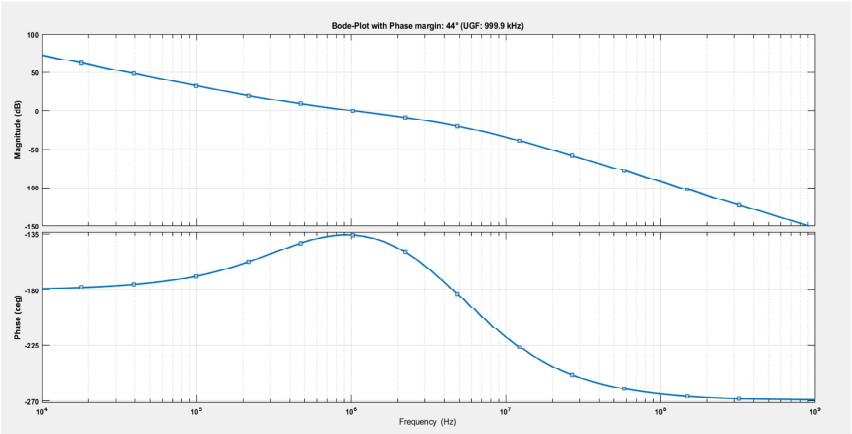


Figure 75: Bode plot of PLL open-loop transfer function

3.4.3 Frequency Divider Design Considerations

Frequency dividers can be broadly categorized into four different types – static, dynamic, Miller, and injection-locked [60]. Static dividers, such as the ones in [60, 61] are the most robust of the four types of dividers and exhibit the widest frequency input range but have a large dc power consumption. Dynamic dividers suffer from limited operating bandwidth and high input voltage swing requirements but can operate at high frequencies. Miller dividers can operate at very high frequencies but are noisy and are not as robust as the other types and may fail to lock under certain conditions. Injection locked frequency dividers too can operate at high frequencies but suffer from a narrow operating bandwidth which requires further modifications [62]. For robustness a static divider is the preferred solution.

A static divider is designed using master-slave flip-flops as shown in Fig. 76. A pair of D-latches are connected in negative feedback to obtain the desired division operation. The operation of the circuit can be qualitatively explained as follows. When the two cascaded latches are clocked using complementary clock signals then the outputs remain at a fixed state when there is no negative feedback. In the presence of negative feedback, from the output of the second latch to the input of the first latch, the latch outputs will toggle at a period that is half the input clock rate and hence achieve the division function [44]. The schematic for one of the Emitter Coupled Logic (ECL) / Current Mode Logic (CML) D-latches is shown in Fig. 77. Inductive peaking is used to widen the operating bandwidth, while the resistance is set to satisfy reliable function towards the lower end of the bandwidth [61].

A static divide by two circuit is designed with master-slave flip-flops which use an inductive load of 500 pH, and a load resistance of 50Ω. The static divider draws approximately 20 mA of current from a 3.3 V supply. An input signal at 10.5 GHz is frequency divided by 2 by the divider as shown in Fig. 78.

The PLL requires a programmable divider that can divide from 90 to 120. The modular divider proposed in [63] is the most appropriate topology. A SiGe BiCMOS implementation of this divider was demonstrated in [64]. A 6-bit divider is required for this PLL, since an n-bit divider can divide from 2^n to $2^{n+1}-1$, and hence a 6-bit divider can divided from 64 to 127. The modular divider utilizes the master-slave

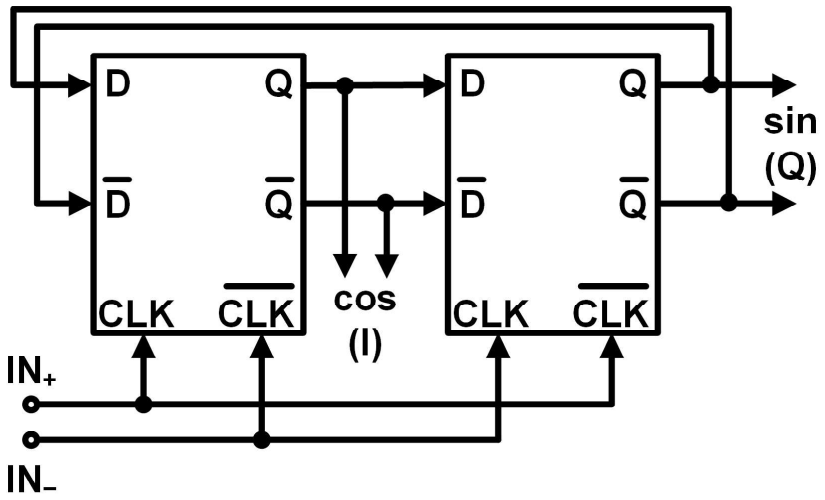


Figure 76: Static frequency divider

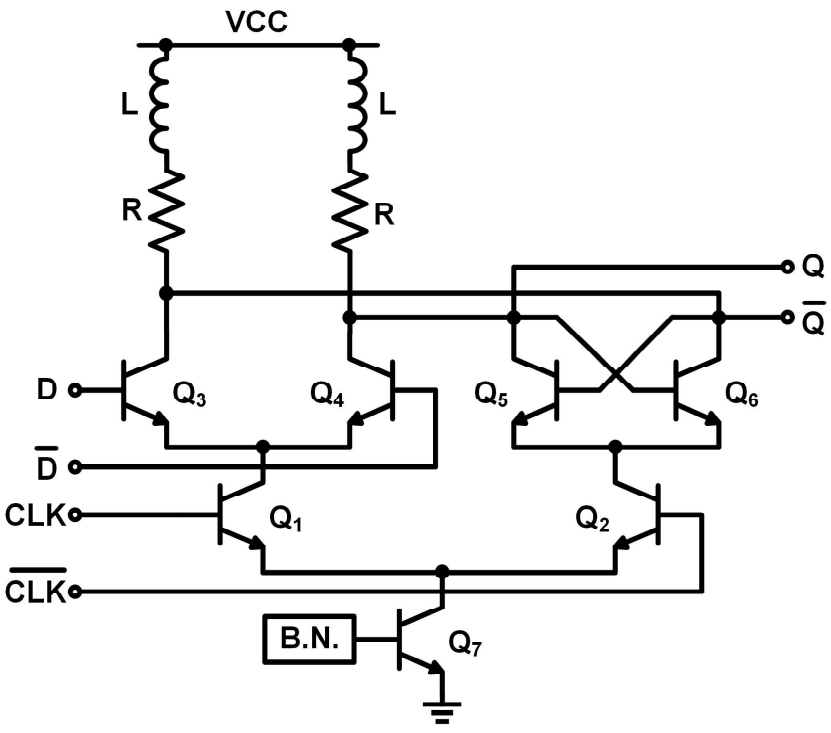


Figure 77: Emitter Coupled Logic Latch

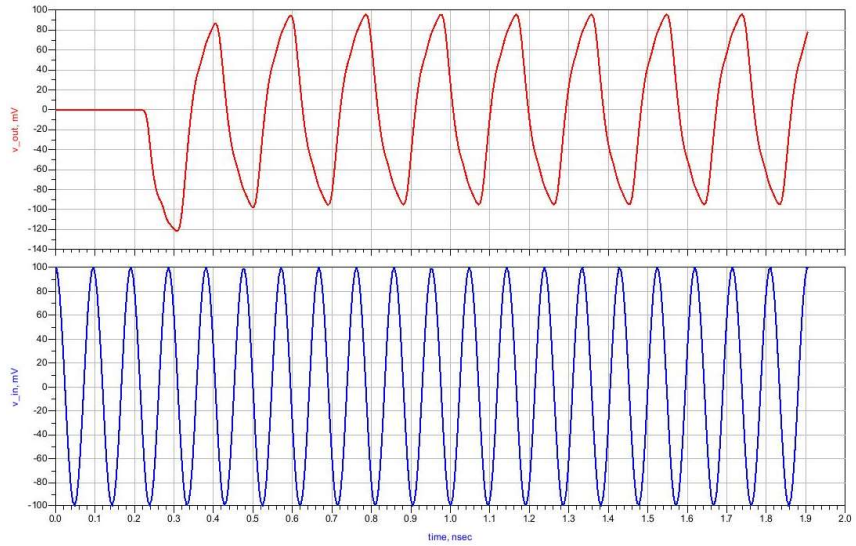


Figure 78: Frequency divide by two output

flip-flop based division technique with additional logic for programmable division.

3.5 PLL Closed-loop behavioral simulation

The closed-loop response of the PLL was simulated using Mathworks SIMULINK. The estimated step response of the PLL is shown in Fig. 79. The settling time is estimated to be 1 μs.

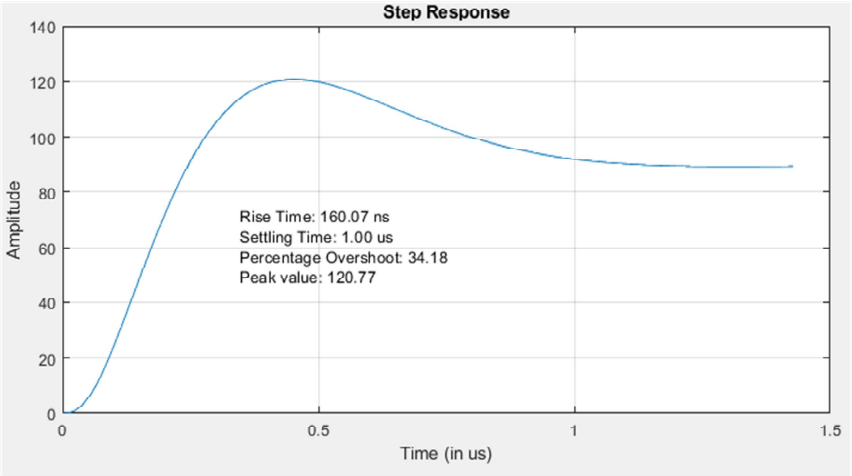


Figure 79: Estimated step response of PLL

The phase noise profile of the designed VCO (at 10 GHz) was used in for behavioral simulation of the PLL phase noise using Keysight ADS. The phase noise profile at the PLL output is estimated as shown in Fig. 80. A phase noise of -98 dBc/Hz @ 1 MHz offset from a 10.5 GHz is estimated with an associated RMS phase jitter of 301 fs. If a narrower loop bandwidth of around 500 kHz is utilized, then the phase noise can be suppressed to a greater extent, but the loop filter capacitor values become large and it becomes unfeasible to integrate the loop filter on-chip.

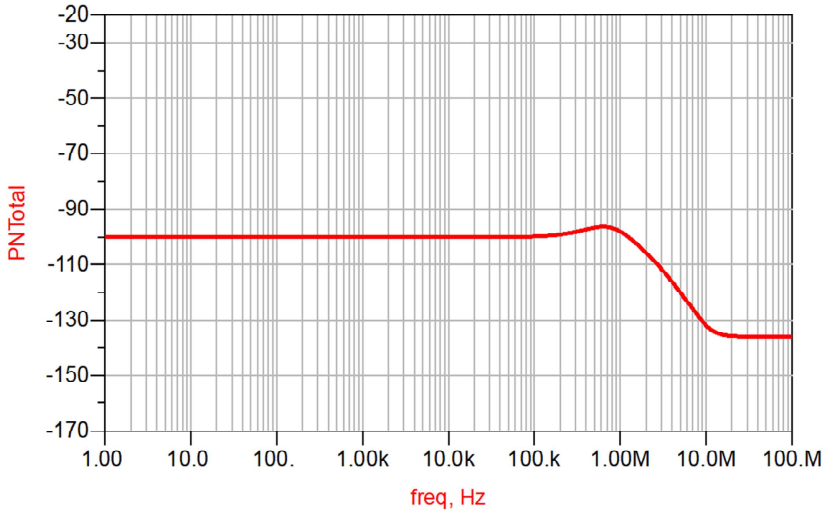


Figure 80: Estimated phase noise of PLL

4 Conclusion & Future Work

4.1 Summary of Work

5G eMBB wireless communications promise a significant improvement in data rates over previous generations of wireless communication systems in order to enable media rich applications. This will be achieved using directive communications techniques such as beamforming at mmWave frequencies (such as the 26 GHz band). The design of frequency generation and conversion blocks required for beamforming transceivers were studied in this thesis.

Beamforming receivers require high-linearity downconversion mixers to handle the large input powers from multiple RF channels. The Gilbert-cell mixer was optimized for high linearity using inductive degeneration to minimize third-order non-linearities. A balun load was used in conjunction to inductive degeneration in order to improve the headroom of the Gilbert-cell mixer. The resulting high-linearity downconversion mixer features an IP_{1dB} of 2.6 dBm while having a low conversion loss of 2.5 dB. The designed mixer is fully integrated with a four-way power combiner and baluns and is therefore suitable for use in beamforming receivers.

Frequency synthesis at mmWaves poses a challenge both due to the inherent low quality factors of integrated passives and due to the issue of high frequency LO routing on lossy PCBs. To address these issues a frequency synthesizer was proposed covering 9.6 GHz - 11.2 GHz which can be used in sliding-IF transceivers for the 26 GHz mmWave 5G band. The sub-blocks of the integer-N type-II 4th order PLL based frequency synthesizer were designed using IHP's 0.13 μm SiGe BiCMOS technology. The VCO for the PLL was optimized for low phase noise by maximizing the resonator quality factor, decoupling the bias of the cross-coupled HBT pair, and by applying tail current filtering. The designed VCO features a 4-bit switchable capacitor bank for increased tuning range. The VCO has a simulated phase noise of -116 dBc/Hz @ 1 MHz offset from a 10.5 GHz carrier and has a 19% tuning range from 9.4 GHz - 11.4 GHz. A behavioral model of the PLL was used for closed-loop PLL simulations. The PLL is estimated to have a phase noise of -98 dBc/Hz @ 1 MHz offset from a 10.5 GHz carrier and an estimated RMS phase jitter of 301 fs.

4.2 Future Work

The high-linearity downconversion mixer performance was verified by measurements. The next step will be to integrate the beamformer front-end with the mixer on an RF PCB, as shown in Fig. 16, and verify the performance of the beamforming receiver.

The frequency synthesizer will require a programmable frequency divider and an automated frequency tuning algorithm. In the long term after the performance of the core PLL has been verified, the PLL can be followed by frequency divide-by-two and frequency doubler for use in a sliding-IF transceiver as shown in Fig. 81.

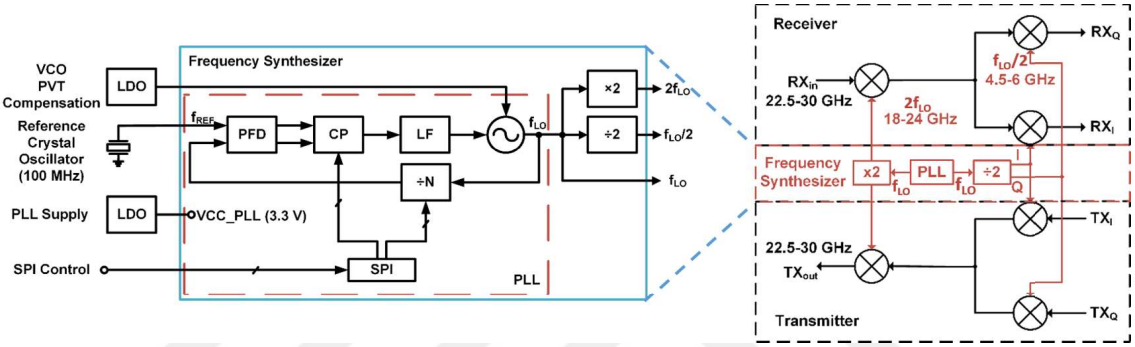


Figure 81: Future integration of frequency synthesizer with sliding-IF transceiver

APPENDIX A. IHP SG13S 130-nm SiGe BiCMOS Process Overview

The IHP Microelectronics Silicon Germanium (SiGe) BiCMOS process, which is the enhanced version of the technology described in [65], provides high performance NPN Heterojunction Bipolar Transistors (HBTs) featuring an f_T/f_{max} of 250/340 GHz. The high performance HBTs have a open-base collector-emitter breakdown voltage, BV_{CEO} of 1.65 V. In addition to the SG13S offers high breakdown voltage NPN HBTs with BV_{CEO} of 3.6 V and f_T/f_{max} of 50/165 GHz. CMOS transistors with a core supply voltage of 1.2 V for logic and 3.3 V for I/O is also provided. The cross-section of the SG13S process is shown in Fig. 82.

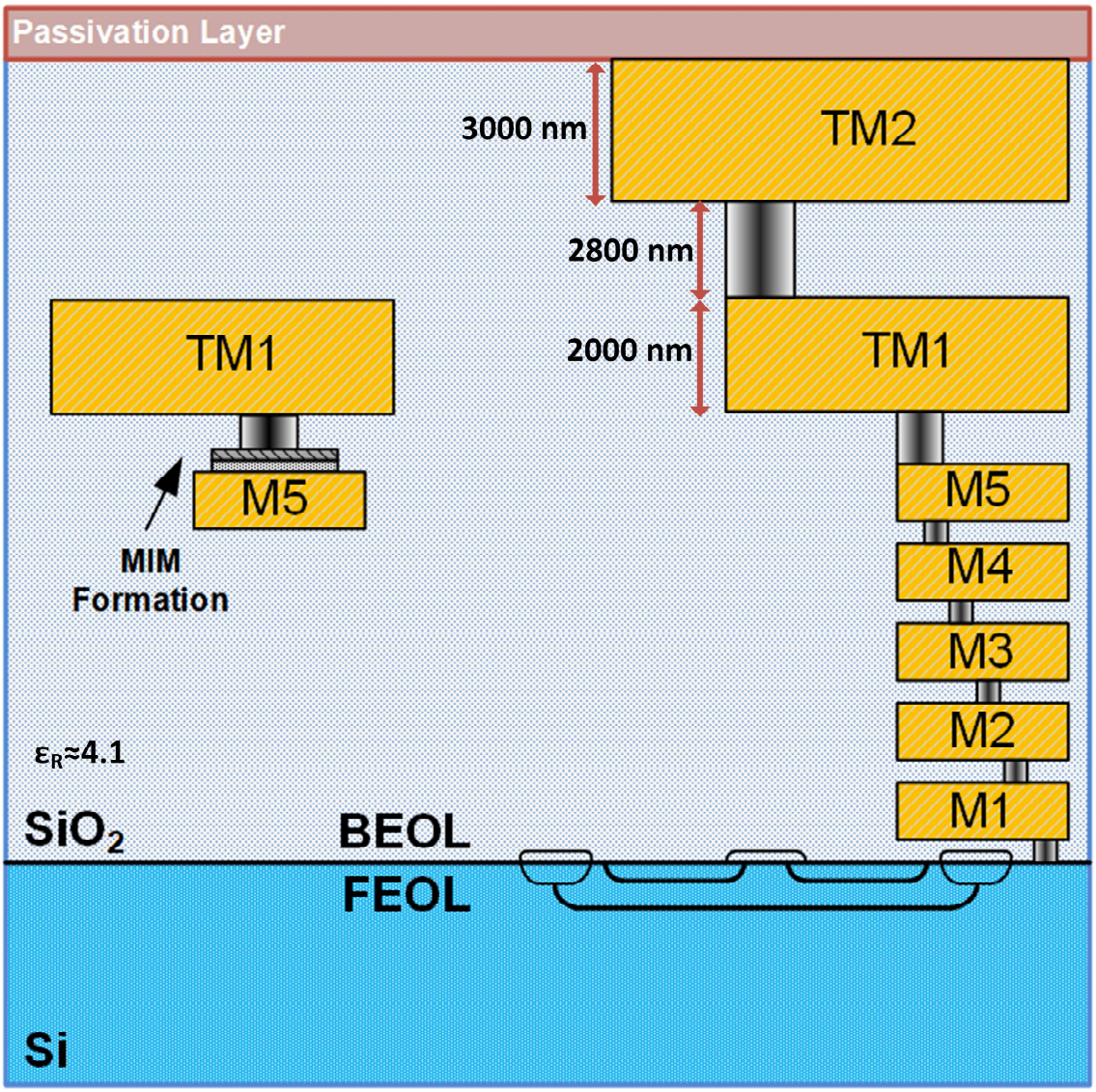


Figure 82: IHP SG13S Process cross-section

SG13S Back End OF Line (BEOL) has 5 thin and 2 thick aluminum metallization layers. The top-most layer (Top Metal 2) is 3 μm thick, and the next layer (Top Metal 1) is 2 μm thick. The isolator layer between Top Metal 2 and Top Metal 1 is 2.8 μm thick.

SG13S provides a wide selection of passives. Three different resistors are offered. This includes salicided n-doped gate polysilicon with sheet resistance of 7 $\Omega/\square$ for precision applications. Metal-Insulator-Metal (MIM) capacitors with capacitance density of 1.5 fF/μm^2 and varactors with C_{max}/C_{min} of 1.7 are also available.

The f_T of a high performance HBT that is 30 times the unit size is plotted versus its collector current density in Fig. 83. The optimum current density is in the range of 20 to 25 mA/μm^2.

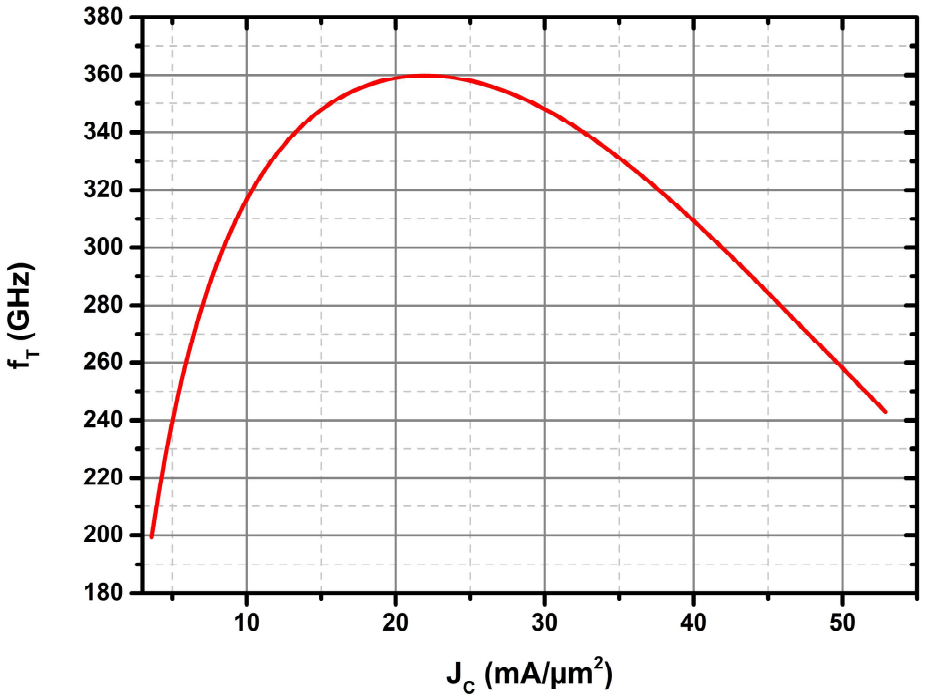


Figure 83: f_T vs. collector current density of HBT

APPENDIX B. In-house Flip-chip Bonding Process

The SUMER in-house flip-chip bonding process described in [66] is used to bond chips that are to be measured onto PCB. The process is briefly described here for reference. The cross-section of an Integrated Circuit (IC) flip-chip bonded onto a Printed Circuit Board (PCB) is shown in Fig. 84.

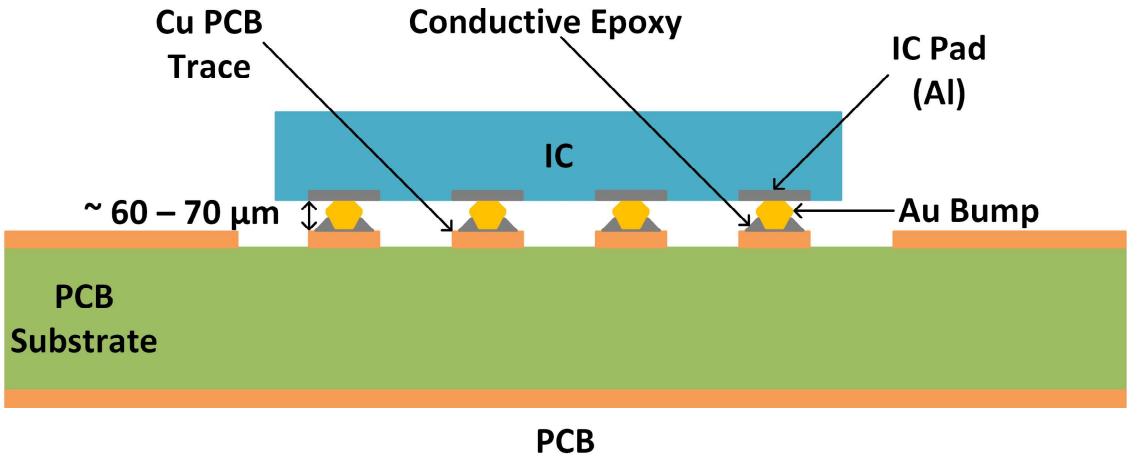


Figure 84: Cross-section of flip-chip bonded IC

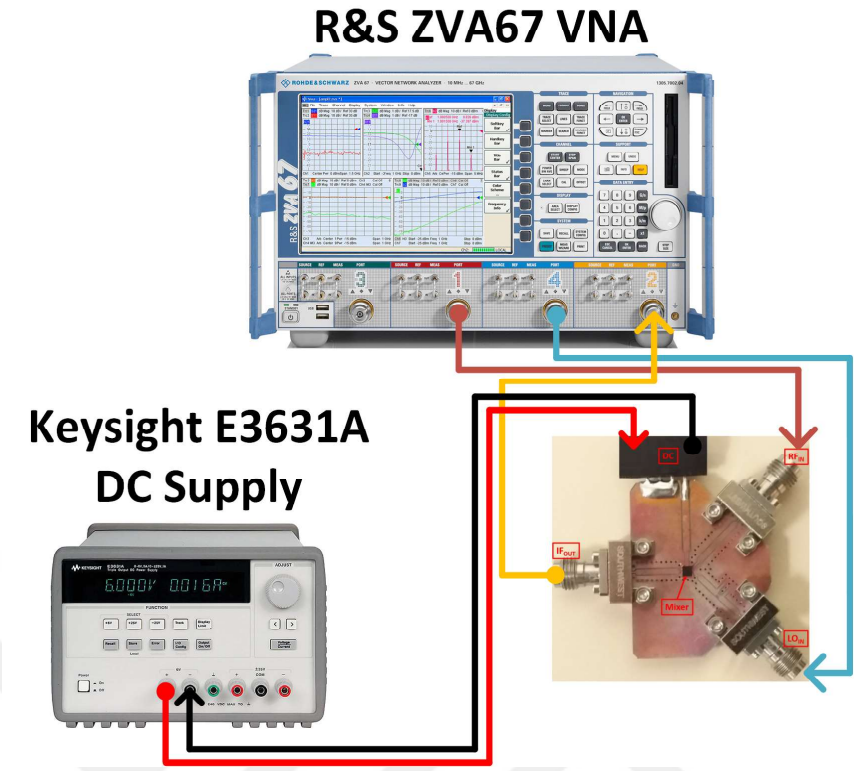
The ICs described in this thesis use 80 μm $\times$ 80 μm pads with a pitch size ranging from 250 μm to 300 μ m. Gold (Au) stud bumps are first bonded on to the aluminum (Al) IC pads using the F&S Bondtec 5310 ball bonding machine. A conductive epoxy is applied onto the PCB traces where the pads are to be bonded, and then the chip is flipped onto the copper (Cu) PCB using the Tresky FC3 flip-chip machine. The bonded chip is then cured under heat to complete the process.

Each of the Au stud bumps have around 1.2 mΩ RMS DC resistance. Electromagnetic simulation is performed on the stud bumps using Keysight EMPro FEM simulator. The simulated loss is around 0.05 dB per stud bump at 26 GHz. This loss is significantly lower than the loss of around 1.0-1.5 dB that is expected when wirebonding is used at these frequencies [67].

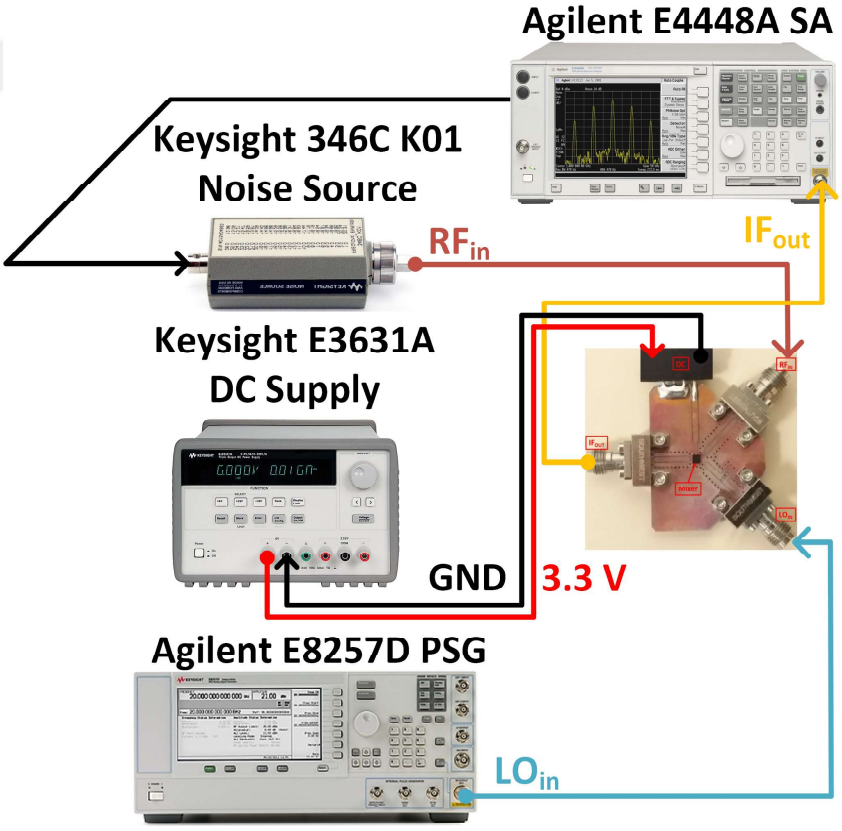
APPENDIX C. Mixer Measurement Setup

The downconversion mixers presented in this thesis are measured as described in the following section. The conversion gain, linearity, LO power dependence of conversion gain, port-to-port isolation, and port return losses are measured using the Rohde & Schwarz ZVA67 Vector Network Analyzer (VNA) as shown in Fig. 85a. The ZVA67 VNA has a preset mixer measurement feature that allows mixers performance parameters to be measured once the appropriate frequencies and power levels have been defined at the RF, IF, and LO ports. For example, the conversion gain is obtained by measuring the ratio of the power of the wave from the output port at the IF frequency and the power of the wave applied to the input port at the RF frequency.

The noise figure of the mixer is measured using the setup shown in Fig. 85b. Single-sideband noise figure measurements are made using this setup. The mixer measurement feature of the Agilent E4448A spectrum analyzer (SA) allows noise figure of frequency translating devices to be measured. This feature is used along with a Keysight 346CK01 noise source to measure the noise figure of the mixer by applying a noise signal at the RF port and measuring the IF signal. The LO signal is provided using an Agilent E8257D programmable signal generator (PSG).



(a) Mixer VNA based measurement setup



(b) Mixer NF measurement setup

Figure 85: Mixer measurement setup

References

[1] J. M. Shea, "History of wireless communication." `http://wireless.ece.ufl.edu/jshea/HistoryOfWirelessCommunication.html`. Accessed: 2020-08-20.

[2] P. Hindle, "History of wireless communications." `https://www.microwavejournal.com/articles/24759-history-of-wireless-communications`. Accessed: 2020-08-20.

[3] G. S. Rao, *Mobile Cellular Communication*. Pearson, 2012.

[4] A. M. Niknejad, S. Thyagarajan, E. Alon, Y. Wang, and C. Hull, "A circuit designer's guide to 5g mm-wave," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–8, 2015.

[5] 3GPP, "Technical Specification Group Services and System Aspects; Release 15 Description; Summary of Rel-15 Work Items (Release 15)," tech. rep., 3rd Generation Partnership Project, Oct. 2018.

[6] ITU, "Recommendation itu-r m.2083-0, imt vision—framework and overall objectives of the future development of imt for 2020 and beyond," Sept. 2015.

[7] S. Ahmadi, *5G NR Architecture, Technology, Implementation, and Operation of 3GPP New Radio Standards*. Oxford:Elsevier, 2019.

[8] W. Roh, J. Seol, J. Park, B. Lee, J. Lee, Y. Kim, J. Cho, K. Cheun, and F. Aryanfar, "Millimeter-wave beamforming as an enabling technology for 5g cellular communications: theoretical feasibility and prototype results," *IEEE Communications Magazine*, vol. 52, no. 2, pp. 106–113, 2014.

[9] F. Khan and Z. Pi, "mmwave mobile broadband (mmb): Unleashing the 3–300ghz spectrum," in *34th IEEE Sarnoff Symposium*, pp. 1–6, 2011.

[10] K. Kolb, J. Potschka, T. Maiwald, K. Aufinger, A. Hagelauer, M. Dietz, and R. Weigel, "A 28 ghz highly accurate phase- and gain-steering transmitter frontend for 5g phased-array applications," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 432–435, 2020.

[11] J. Pang, Z. Li, X. Luo, J. Alvin, R. Saengchan, A. A. Fadila, K. Yanagisawa, Y. Zhang, Z. Chen, Z. Huang, X. Gu, R. Wu, Y. Wang, D. You, B. Liu, Z. Sun, Y. Zhang, H. Huang, N. Oshima, K. Motoi, S. Hori, K. Kunihiro, T. Kaneko, A. Shirane, and K. Okada, "A 28-ghz cmos phased-array beamformer supporting dual-polarized mimo with cross-polarization leakage cancellation," in *2020 IEEE Symposium on VLSI Circuits*, pp. 1–2, 2020.

[12] L. Gao and G. M. Rebeiz, "A 22-44-ghz phased-array receive beamformer in 45-nm cmos soi for 5g applications with 3-3.6-db nf," *IEEE Transactions on Microwave Theory and Techniques*, pp. 1–1, 2020.

[13] A. Nafe, M. Sayginer, K. Kibaroglu, and G. M. Rebeiz, "2 × 64-element dual-polarized dual-beam single-aperture 28-ghz phased array with 2 × 30 gb/s links for 5g polarization mimo," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 9, pp. 3872–3884, 2020.

[14] Y. Yin, S. Zihir, T. Kanar, Q. Ma, H. Chung, L. Gao, and G. M. Rebeiz, "A 37-42-ghz 8x8 phased-array with 48-51-dbm eirp, 64-qam 30-gb/s data rates, and evm analysis versus channel rms errors," *IEEE Transactions on Microwave Theory and Techniques*, pp. 1–1, 2020.

[15] M. Lokhandwala, L. Gao, and G. M. Rebeiz, "A high-power 24-40-ghz transmit-receive front end for phased arrays in 45-nm cmos soi," *IEEE Transactions on Microwave Theory and Techniques*, pp. 1–1, 2020.

[16] J. Pang, Z. Li, R. Kubozoe, X. Luo, R. Wu, Y. Wang, D. You, A. A. Fadila, R. Saengchan, T. Nakamura, J. Alvin, D. Matsumoto, B. Liu, A. T. Narayanan, J. Qiu, H. Liu, Z. Sun, H. Huang, K. K. Tokgoz, K. Motoi, N. Oshima, S. Hori, K. Kunihiro, T. Kaneko, A. Shirane, and K. Okada, "A 28-ghz cmos phased-array beamformer utilizing neutralized bi-directional technique supporting dual-polarized mimo for 5g nr," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2371–2386, 2020.

[17] K. Okada and J. Pang, "Millimeter-wave cmos phased-array transceiver supporting dual-polarized mimo for 5g nr," in *2020 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–8, 2020.

[18] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Artech House, 2003.

[19] B. Razavi, *RF Microelectronics*. Prentice Hall, 2012.

[20] K. L. Fong and R. G. Meyer, "Monolithic RF active mixer design," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 3, pp. 231–239, 1999.

[21] A. Niknejad and O. Shana'a, *Mixer Noise and Design - Advanced Communication Integrated Circuits (EE 242)*. University of California, Berkeley.

[22] A. J. Bergsma and B. A. Syrett, "A comprehensive design method for dual-gate mosfet mixers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 12, pp. 1443–1451, 2000.

[23] S. Shahramian, M. J. Holyoak, A. Singh, and Y. Baeyens, "A fully integrated 384-element, 16-tile, w -band phased array with self-alignment and self-test," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 9, pp. 2419–2434, 2019.

[24] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A low-cost scalable 32-element 28-ghz phased array transceiver for 5g communication links based on a 2×2 beamformer flip-chip unit cell," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, 2018.

[25] B. Sadhu, Y. Tousi, J. Hallin, S. Sahl, S. K. Reynolds, Ö. Renström, K. Sjögren, O. Haapalahti, N. Mazor, B. Bokinge, G. Weibull, H. Bengtsson, A. Carlinger, E. Westesson, J. Thillberg, L. Rexberg, M. Yeck, X. Gu, M. Ferriss, D. Liu, D. Friedman, and A. Valdes-Garcia, "A 28-ghz 32-element trx phased-array ic with concurrent dual-polarized operation and orthogonal phase and gain control for 5g communications," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, 2017.

[26] J. Cressler, *Fabrication of SiGe HBT BiCMOS Technology*. CRC Press, 2008.

[27] I. Kalyoncu, *Four-Element Phased-Array Beamformers and A Self-Interference Canceling Full-Duplex Transceiver in 130-nm SiGe for 5G Applications at 26 GHz*. PhD thesis, Sabanci University, Istanbul, Turkey, 07 2019.

[28] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A 28 ghz transceiver chip for 5g beamforming data links in sige bicmos," in *2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, pp. 74–77, 2017.

[29] H. E. Jones, "Dual output synchronous detector utilizing transistorized differential amplifiers," U.S. patent 3241078A, filed: 18 June 1963 ; issued: 15 March 1966.

[30] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE Journal of Solid-State Circuits*, vol. 3, no. 4, pp. 365–373, 1968.

[31] B. Gilbert, "Translinear circuits: a proposed classification," *Electronics Letters*, vol. 11, no. 1, pp. 14–16, 1975.

[32] Keng Leong Fong and R. G. Meyer, "High-frequency nonlinearity analysis of common-emitter and differential-pair transconductance stages," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 4, pp. 548–555, 1998.

[33] S. Voinigescu, *High-Frequency Integrated Circuits*. Cambridge University Press, 2013.

[34] D. Alldred, B. Cousins, and S. P. Voinigescu, "A 1.2v, 60-ghz radio receiver with on-chip transformers and inductors in 90-nm cmos," in *2006 IEEE Compound Semiconductor Integrated Circuit Symposium*, pp. 51–54, 2006.

[35] W. Eisenstadt, B. Stengel, and B. Thompson, *Differential Circuit Design Using Mixed-Mode S-Parameters*. Artech House, 2006.

[36] J. R. Long, "Monolithic transformers for silicon rf ic design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, 2000.

[37] J. Kim and G. M. Rebeiz, "Miniature four-way and two-way 24 ghz wilkinson power dividers in 0.13 μm cmos," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 9, pp. 658–660, 2007.

[38] H. A. Ameen, K. Abdelmonem, M. A. Elgamal, M. A. Mousa, O. Hamada, Y. Zakaria, and M. A. Y. Abdalla, "A 28 GHz four-channel phased-array transceiver in 65-nm CMOS technology for 5G applications," in *2017 29th International Conference on Microelectronics (ICM)*, pp. 1–4, Dec 2017.

[39] T. Tsai, I. Huang, J. Tsai, A. Alshehri, M. Almalki, A. Saved, and T. Huang, "A Ka-Band Sub-Harmonically Pumped Mixer Using Diode-Connected MOSFET for 5G MM-Wave Transceivers," in *2018 Asia-Pacific Microwave Conference (APMC)*, pp. 488–490, Nov 2018.

[40] M. El-Nozahi, E. Sánchez-Sinencio, and K. Entesari, "A 20–32-GHz Wideband Mixer With 12-GHz IF bandwidth in 0.18-μm SiGe Process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, pp. 2731–2740, Nov 2010.

[41] V. Issakov, H. Knapp, M. Wojnowski, A. Thiede, and W. Simbürger, "A 22–39 ghz passive mixer in sige:c bipolar technology," in *2010 IEEE MTT-S International Microwave Symposium*, pp. 1012–1015, 2010.

[42] A. Verma, Li Gao, K. K. O, and J. Lin, "A k-band down-conversion mixer with 1.4-ghz bandwidth in 0.13-μm cmos technology," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 8, pp. 493–495, 2005.

[43] M. van Delden, N. Pohl, K. Aufinger, C. Baer, and T. Musch, "A low-noise transmission-type yttrium iron garnet tuned oscillator based on a sige mmic and bond-coupling operating up to 48 ghz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 10, pp. 3973–3982, 2019.

[44] B. Razavi, *Design of CMOS Phase-Locked Loops*. Cambridge University Press, 2020.

[45] S. J. Fang, F. Zhang, A. Bellaouar, and S. Embabi, "A 28ghz sliding-if receiver in 22nm fdsoi," in *ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)*, pp. 385–388, 2019.

[46] S. Ek, T. Pahlsson, C. Elgaard, A. Carlsson, A. Axholt, A. Stenman, L. Sundstrom, and H. Sjoland, "A 28-nm fd-soi 115-fs jitter pll-based lo system for 24–30-ghz sliding-if 5g transceivers," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 1988–2000, 2018.

[47] F. Pepe, A. Bevilacqua, and P. Andreani, "On the remarkable performance of the series-resonance cmos oscillator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 2, pp. 531–542, 2018.

[48] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 329–330, 1966.

[49] B. Sadhu, J. Kim, and R. Harjani, "A cmos 3.3-8.4 ghz wide tuning range, low phase noise lc vco," in *2009 IEEE Custom Integrated Circuits Conference*, pp. 559–562, 2009.

[50] A. Fard and P. Andreani, "An analysis of $1/f^2$ phase noise in bipolar colpitts oscillators (with a digression on bipolar differential-pair lc oscillators)," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 374–384, 2007.

[51] C. Samori, A. L. Lacaita, P. Vita, and A. Zanchi, "Design issues of lc tuned oscillators for integrated transceivers," in *Proceedings of the 8th Great Lakes Symposium on VLSI (Cat. No.98TB100222)*, pp. 264–269, 1998.

[52] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower lc oscillator phase noise," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, 2001.

[53] B. Sadhu, T. Anand, and S. K. Reynolds, "A fully decoupled lc tank vco topology for amplitude boosted low phase noise operation," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2488–2499, 2018.

[54] E. Wagner, O. Shana'a, and G. M. Rebeiz, "A very low phase-noise transformer-coupled oscillator and pll for 5g communications in 0.12 μ m sige bicmos," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 4, pp. 1529–1541, 2020.

[55] P. Wang, M. Chou, Y. Chen, Y. Chang, D. Chang, and S. S. H. Hsu, "A ku-band low-phase-noise transformer coupled vco for satellite communications," in *2016 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, pp. 1–3, 2016.

[56] A. Agrawal and A. Natarajan, "A 6.39ghz–14ghz series resonator mode-switching oscillator with 186–188db fom and 197db foma in 65nm cmos," in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 199–202, 2015.

[57] Y. Wang, D. Leenaerts, E. van der Heijden, and R. Mahmoudi, "A low phase noise colpitts vco for ku-band applications," in *2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, pp. 1–4, 2012.

[58] A. Homayoun and B. Razavi, "Analysis of phase noise in phase/frequency detectors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 3, pp. 529–539, 2013.

[59] B. D, *PLL Performance, Simulation, and Design.* Dog Ear Publishing, 2006.

[60] P. Zhou, J. Chen, P. Yan, D. Hou, and W. Hong, "A low power, high sensitivity sige hbt static frequency divider up to 90 ghz for millimeter-wave application," *China Communications*, vol. 16, no. 2, pp. 85–94, 2019.

[61] F. Herzel, J. Borngräber, and A. Ergintav, "A 60 ghz frequency divider with quadrature outputs in 130nm sige bicmos technology for optical ofdm systems," in *2015 10th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 69–72, 2015.

[62] X. Yi, C. C. Boon, J. F. Lin, M. A. Do, K. S. Yeo, and W. M. Lim, "A divide-by-two injection-locked frequency divider with 13-ghz locking range in 0.18-μm cmos technology," in *2011 International Symposium on Integrated Circuits*, pp. 216–219, 2011.

[63] C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-/spl mu/m cmos technology," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, 2000.

[64] M. Kreißig, M. El-Shennawy, and F. Ellinger, "A multi-modulus divider with high sensitivity and extended division range in 0.18 μm bicmos," in *2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 213–216, 2016.

[65] H. Rücker, B. Heinemann, W. Winkler, R. Barth, J. Borngraber, J. Drews, G. G. Fischer, A. Fox, T. Grabolla, U. Haak, D. Knoll, F. Korndörfer, A. Mai, S. Marschmeyer, P. Schley, D. Schmidt, J. Schmidt, M. A. Schubert, K. Schulz,

B. Tillack, D. Wolansky, and Y. Yamamoto, "A 0.13 μm sige bicmos technology featuring f $_T$/f $_{\max}$ of 240/330 ghz and gate delays below 3 ps," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1678–1686, 2010.

[66] C. Çalışkan, M. H. Mahmud, A. Kasal, M.Yazici, and Y. Gurbuz, "Low noise wideband monotonically raising gain active equalizer in sige bicmos for phased arrays," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. accepted and presented, to appear in proceedings., 2020.

[67] D. Jahn, R. Reuter, Y. Yin, and J. Feige, "Characterization and modeling of wire bond interconnects up to 100 ghz," in *2006 IEEE Compound Semiconductor Integrated Circuit Symposium*, pp. 111–114, 2006.