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Burhan Akçil

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Burhan Akçil

Approved by:

Prof. Dr. Serkan Topaloğlu
(Yeditepe University) ……
(Thesis Supervisor)

Prof. Dr. Ahmet Arif Ergin
(Yeditepe University) ……

Assist. Prof. Dr. Ali Akman
(İstanbul Ticaret University) ……

DATE OF APPROVAL: …. / …. / 20….

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ABSTRACT

SMART GAIN SLOPE MANAGEMENT SYSTEM

Cable TV broadcast is an efficient and up-to-date technology that provides television broadcasting and internet communication to end users. This technology, which is used in Turkey as well as all over the world, is one of the main technology providers for internet communication and television broadcasts. With the development of technology, it has developed and continues to develop over time to meet the increasing bandwidth, upload speed, and data rate requirements. With the increasing gain levels, the frequency bands have also expanded and as of today, they have expanded to the 1.8 GHz frequency. Due to the requirements of the technology and the field, the system units that are adjusted by the technicians in the field leave their place to the remotely controlled units. This situation necessitates remotely controlled equalizer structures to compensate for losses at different frequencies in wide bands.

This thesis introduces the design and production of an adaptive module that allows smoothing of the signal gain that can be used in the CATV distribution amplifier by the DOCSIS 4.0 standard. The design includes equalization, inverse equalization, and MCU blocks. The design includes radio frequency (RF) detectors to detect pivot signals close to 258 MHz and 1.8 GHz frequencies which are determined by DOCSIS 4.0 standard. MCU analyzes signal TCP power in pivot signals and measures the slope of the signal. In the automatic mode, the module flattens the S_{21} parameter using equalizer and inverse equalizer signal.

ÖZET

AKILLI KAZANÇ EĞİMİ YÖNETİM SİSTEMİ

Kablo TV yayınları, televizyon yayınlarının ve internet haberleşmesinin son kullanıcılara sağlandığı verimli ve güncel bir teknolojidir.Tüm dünyada olduğu gibi Türkiye'de de kullanılan bu teknoloji, internet iletişimi ve televizyon yayınları için ana teknoloji sağlayıcılarından biridir. Teknolojinin gelişmesi ile birlikte artan bant genişliği, yükleme hızı ve veri hızı gereksinimlerine cevap verebilmek için zamanla gelişim göstermiş ve göstermeye de devam etmektedir. Artan kazanç seviyeleriyle birlikte frekans bantları da genişlemiş ve bugün itibariyle 1.8 GHz frekansına kadar genişlemiştir. Teknolojinin ve sahanın gereksinimleri itibariyle sahada teknikerler tarafından ayarlamaları yapılan sistem birimleri yerini uzaktan kontrollü birimlere bırakmaktadır. Bu durum geniş bantta farklı frekanslardaki kayıpları dengelemek için uzaktan kontrollü dengeleyici yapılarını gereklilik haline getirmiştir.

Bu tez, DOCSIS 4.0 standardına uygun olarak CATV dağıtım yükselticileri bünyesinde de kullanılabilecek sinyal kazancını düzleştirmeyi sağlayan uyarlanabilir bir modülünün tasarımını ve üretimini göstermektedir. Tasarım dengeleyici, ters dengeleyici ve MCU bloğu içerir. Tasarım, DOCSIS 4.0 standardında belirlenen 258 MHz ve 1.8 GHz frekanslarına yakın pivot sinyalleri algılamak için RF dedektörler içerir. MCU, pivot sinyallerdeki toplam bileşik gücü analiz eder ve sinyalin eğimini ölçer. Otomatik modda modül, dengeleyici ve ters dengeleyici sinyali kullanarak S_{21} parametresini düzleştirir.

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LIST OF ABBREVIATIONS

C_L	Capacitance per unit length
η_m	Characteristic impedance of the medium between two conductors
σ_{si}	Conductivity of the inner conductor
σ_{so}	Conductivity of the outer conductor
L_L	Inductance per unit length
f_1	Lower frequency
f_2	Upper frequency
δ_i	Skin depth of the inner conductor
δ_o	Skin depth of the outer conductor
δ_s	Surface depth
ω	Angular frequency
Ω	Electrical resistance
μ	Permeability
ϵ	Permittivity
3D	Three dimensional
ADC	Analog-to-digital converter
AGC	Automatic gain control
BER	Bit error rate
CATV	Community Antenna Television
CM	Cable modem
CMTS	Cable Modem Termination Systems
CSO	Composite second order beat
CTB	Composite triple sequence beat
CW	Continuous wave
dB	Decibel
dBm	Decibel-milliwatts
DF	Dissipation factor

DOCSIS	Data Over Cable Service Interface Specification
DSA	Digital step attenuator
Gbps	Giga bits per second
GHz	Gigahertz
Hz	Hertz
IC	Integrated circuit
ITU	International Telecommunications Union
Mbps	Mega bits per second
MCU	Microcontroller unit
MER	Modulation error rate
MHz	Megahertz
mV	millivolt
USD	United States dollar
QAM	Quadrature amplitude modulation
OPAMP	Operational amplifier
Pf	Picofarad
PCB	Printed circuit board
RF	Radio frequency
SAW	Surface acoustic wave
SCTE	Society of Cable Telecommunications
SGSMS	Smart gain slope management system
SMD	Surface-mounted device
SNR	Signal to noise ratio
SPI	Serial peripheral interface
V	Volt
VNA	Vector network analyzer

1. INTRODUCTION

Cable television, which has been in our lives for a long time since the end of the 1940s, is used today to provide a wide variety of services with the increase in technological developments [12,13]. At the beginning of the 21st century, with the transformation of antenna televisions into the cable communication industry, Community Antenna Television (CATV) which used to be based on broadcasting television programs, today it provides services in many areas such as analog and digital video, digital voice, high-speed data and telephony with developing technologies [12,13].

CATV has become indispensable in social, educational, or economic matters in recent years, and has become an integral part of mass communication and continues to become more important day by day [14]. Today, with the aid of CATV, people can easily socialize, shop, trade, access entertainment content, or research through the high-speed network [12]. As CATV takes up a larger space in our daily lives, it has also become necessary to respond to the need for data capacity. For this reason, this technology also renews itself.

As the use of CATV became widespread and the demand for bandwidth increased, there was a need to standardize this technology. CableLabs created the Data Over Cable Service Interface Specification (DOCSIS) standard in this context. The standard started to be developed by the Society of Cable Telecommunications (SCTE) committee established within CableLabs. This community brought together operators, hardware, and software developers to optimize the standard. CableLabs contributed to these standards by conducting pioneering research on this subject. Thus, the DOCSIS standard was created. This standard was developed from DOCSIS 1.0 and updated to DOCSIS 4.0 level as of 2022. In Table 1.1, the frequency band and data capacity of all DOCSIS versions are given [6,7,8,9,10,11].

Figure 1.1 provides a simplified DOCSIS wired access environment covering all DOCSIS standards. A CATV distribution system consists of a plurality of Cable Modem Termination Systems (CMTS), and each CMTS interfaces with a plurality of cable modems (CMs). A Cable Operator allocates a portion of the radio frequency (RF) spectrum for data usage and assigns a set of channels to CMs. From here, the broadcast reaches the subscriber [1,15].

End-user networks consist of coaxial cables made of a round inner conductor surrounded

Table 1.1. Different DOCSIS versions [6,7,8,9,10,11]

DOCSIS Version	Downstream Frequency (MHz)	Upstream Frequency (MHz)	Downstream Capacity	Upstream Capacity
1.0	5-42	50-860	40 Mbps	10 Mbps
2.0	5-42	50-860	40 Mbps	30 Mbps
3.0	5-42 or 5-85	50-1002	1 Gbps	100 Mbps
3.1	5-204	258-1218	10 Gbps	1-2 Gbps

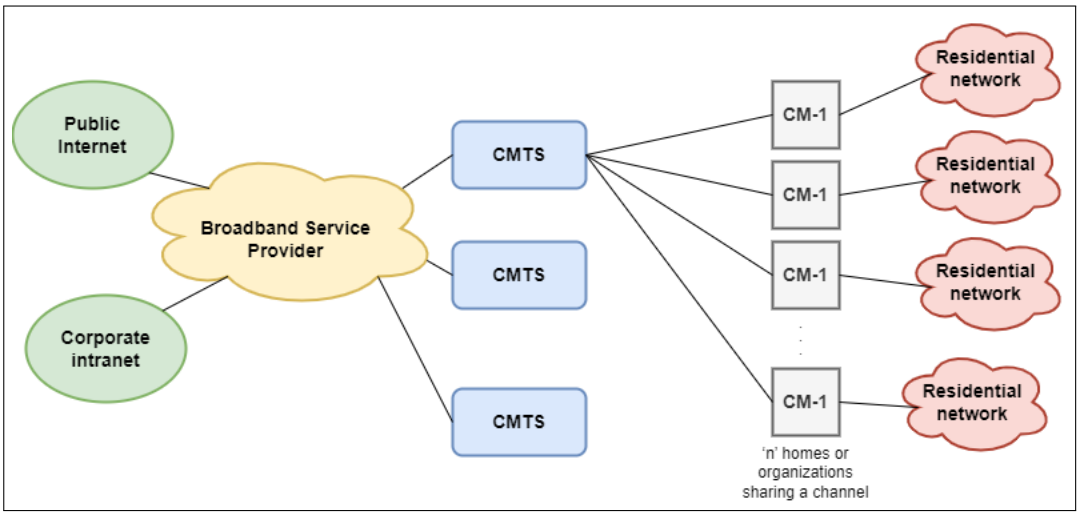

Figure 1.1. DOCSIS cable access environment [1]

by a large diameter, coaxially located cylindrical outer conductor separated by a dielectric material from the inner conductor terminated with Type F connectors. The coaxial cable used here has a characteristic impedance equal to the square root of the ratio of the cable inductance per length to capacitance per length. In other words, the dimensions and structure of the internal and external conductors of the coaxial cable, as well as the conductivity and dielectric properties of the insulating materials used in the coaxial cable, characterize the performance of coaxial lines [2,16,17].

Coaxial cable creates capacitance and inductance and these can be calculated per unit length of coaxial cable. C_L refers to the capacitance per unit length of coaxial cable and L_L refers to the inductance per unit length of coaxial cable. C_L and L_L values can be calculated from the Equations (1.1) and (1.2) [2,17].

$$C_L = \frac{2\pi\epsilon}{ln(\frac{D}{d})} \tag{1.1}$$

$$L_L = \frac{\mu}{2\pi} ln(\frac{D}{d}) \tag{1.2}$$

The characteristic impedance formula of a transmission line and its simplified version are given in Equation (1.3). d is the outer diameter of the inner conductor and D is the inner diameter of the outer conductor. ϵ is the complex permittivity and expression as $\epsilon = \epsilon_0\epsilon_d$. The permeability between d and D is defined by μ [2,17,18].

$$Z_0 = \sqrt{\frac{j\omega L_L + R_c}{j\omega C_0 + G_0}} = \frac{\eta_m}{2\pi} ln(\frac{D}{d}) \tag{1.3}$$

While η_m given in Equation (1.3) gives the characteristic impedance of the medium between two conductors, R_c gives the conductor resistance [2].

$$R_c = \frac{1}{\pi d \delta_{si} \sigma_i} + \frac{1}{\pi D \delta_{so} \sigma_o} \tag{1.4}$$

The formula of R_c is given in Equation (1.4). δ_i gives the skin depth of the inner conductor and δ_o gives the skin depth of the outer conductor. Since inner and outer conductivities are different, skin depths will also be different. It gives the skin depths of the σ_{si} inner and σ_{so}

outer conductor [2,17].

$$a_g = k\sqrt{\epsilon_r}\frac{D_\epsilon}{2} + \frac{R_c}{2Z_0} \tag{1.5}$$

The attenuation expression in Nepers/m, including conductor losses, is given as in Equation (1.5). The k term in Equation (1.5) can be found with Equation (1.6) [2].

$$k_g = k\sqrt{\epsilon_r} \tag{1.6}$$

The attenuation expression defined in Equation (1.5) can be expressed more commonly as in Equation (1.7) [2].

$$A_g = 0.09102\sqrt{\epsilon_r}D_\epsilon f + \frac{2.747}{Z_0}\left(\frac{1}{d\sqrt{\sigma_{si}}} + \frac{1}{D\sqrt{\sigma_{so}}}\right) \tag{1.7}$$

When terminated with a load matched to the cable characteristic impedance, defined by the relative diameters of the conductors and the electrical properties of the dielectric material, the ratio of the voltage between the two conductors to the current passing through the conductors is equal to the characteristic impedance. Bending, stretching, and length of the coaxial cable change the characteristic impedance. This may cause RF signal interference and signal distortion [2,16]. Not only by their physical properties, coaxial cables also depend on the passage of electromagnetic fields through the dielectric medium and the flow of charge in conductors. Therefore, the losses that occur arise not only from the physical dimensions and bending/stretching of the cable but also from the conductors and dielectric properties [2,19].

Penetration of electromagnetic fields into conductors does not occur linearly. Where z is the distance to the conductor and δ_s is the surface depth, the field amplitude decreases exponentially with respect to $\exp(-z/\delta_s)$. The general expression of surface depth is defined in Equation (1.8) [2]:

$$\delta_s = \sqrt{\frac{2}{\omega\mu_0\sigma}} \tag{1.8}$$

where σ is the conductivity and b is the resistance per unit length of the circular wire [2].

$$R_s = \frac{1}{\pi b\delta_s\sigma} = \frac{1}{\pi b}\sqrt{\frac{\omega\mu_0}{2\sigma}} \tag{1.9}$$

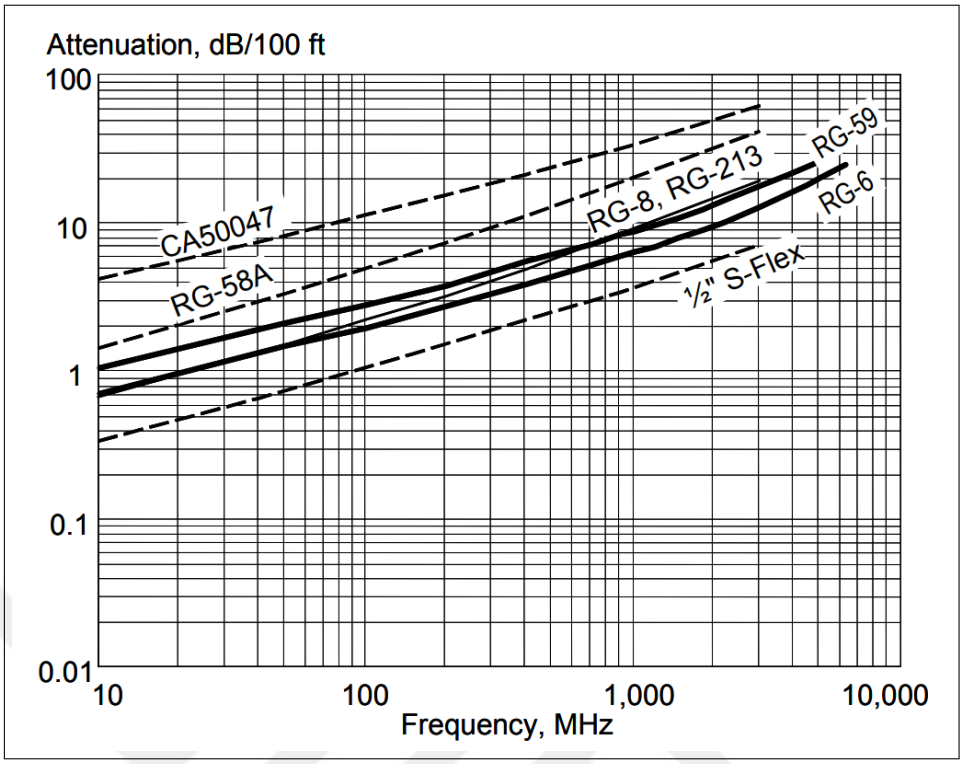

Figure 1.2. Attenuation of various coaxial lines depending on frequency [2]

Considering the Equations (1.1) to (1.9) given above, it is clearly seen that the loss of coaxial cables changes depending on the frequency. In Figure 1.2, the frequency-dependent losses of various 50 Ω and 75 Ω coaxial cables in the range of 10 MHz and 10 GHz are given. Dashed lines give the losses of 50 Ω coaxial cables and solid lines give the losses of 75 Ω coaxial cables. Frequency-dependent attenuation of RG-59 and RG-6, which are 75 Ω coaxial cables commonly used in CATV systems, is important within the scope of this study [2].

Analog TV signal quality is measured and determined with parameters such as composite triple sequence beat (CTB), composite second order beat (CSO), and digital signals which are in the structure of quadrature amplitude modulation (QAM), quality is determined with the parameters modulation error rate (MER) and bit error rate (BER). Gain level variation directly affects the signal quality parameters. In CATV applications, analog and digital channel levels are preferred to be configured for low distortion and high signal-to-noise ratio. while the CATV frequency plan requires digital channels at high frequency and digital channels' signal-to-noise ratio (SNR) is more critical, lowering analog channel levels with equalizers is a common method to increase channel and data capacity. These configurations and channel plans create a requirement to manage the gain slope. Also, like the Figure 1.3,

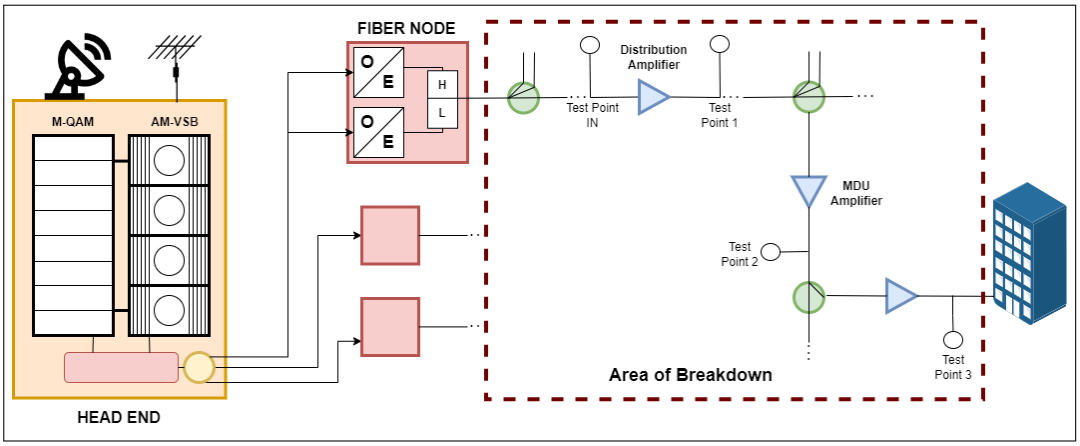

Figure 1.3. Set up of CATV network [3]

cable length should be considered which can be different depending on subsystems and end-user building structures [3,20,21,22].

The conventional CATV solutions solve the gain level and equalization problems with passive, mechanical, and field-upgradable solutions such as onboard attenuators and equalizers, plug-in attenuators, equalizers, and inverse equalizer parts. These solutions need to be applied in the field and for every amplifier one by one with technicians. DOCSIS 4.0 standard brings industry remote-controlled unit requirements and remote measured gain level and signal slope abilities. In this study, a practical design offered a new generation remote controllable, software-supported, digitalized smart method to meet the requirement.

2. THESIS ORGANIZATION

In Chapter 1, brief information about the history of CATV communication is presented and DOCSIS standards are mentioned. Afterward, the losses of CATV distribution systems and the coaxial cables that provide distribution are explained. The research purpose and motivation of this thesis are explained.

In Chapter 2, the steps followed in this study are summarized.

In Chapter 3, studies in the literature that provide gain flats in CATV distribution systems and CATV amplifiers have been examined and presented.

In Chapter 4, the system required for the proposed study is used, and a block diagram of the proposed system is given and explained. The methodology and procedure of the study are presented.

In Chapter 5, for the system proposed, two typologies, first and final, are presented. The theory of the typologies to be used in the design of these two studies is briefly mentioned, the design stages are explained in detail and simulation results are presented. The realized structures were compared with their simulations and the studies were compared.

3. LITERATURE REVIEW

Automatic gain control (AGC) systems are a very important requirement for electronic circuit systems, and there are many about this in the literature [23,24,25,26,27,28,29].

Automatic gain/slope control systems, which are used to maintain signal levels when the signal levels, which are the subject of this study, try to change for any reason, have been used in CATV systems for many years [30]. However, during the literature review, it is seen that there are no active circuits that totally flatten the gain signal level for wide band multi-carrier signal transmission systems although there are many studies on CATV and system gain [31,32]. However, there is no study in the literature regarding remote automatic slope control for CATV systems.

Although active equalizer modules are not designed for CATV systems, they are found in different applications[33,34,35,36].

There is no actual study in the literature for active inverse equalizer circuits that comply with DOCSIS 4.0 standards. However, in the study of Itoh et al. in 2017, there is a study for positive and negative slope equalizers [37]. When this study was examined, it was seen that the frequency band designed an active integrated circuit operating between 100 MHz - 1 GHz, requiring 15 V adjustment voltage, and the slope can be adjusted between -13 dB and 18 dB. Input and output return loss values are between 10 dB and 2 dB. However, when compared to the proposed system, DOCSIS 4.0 standard, which is 258 MHz-1.8 GHz, does not meet the frequency band, the need for 15 V adjustment voltage is high, digital step attenuators can work with 3.3 V, target return loss value better than 10 dB and negative slope. Due to the inadequacy of the operating frequency range, it does not meet the intended requirements of this work.

There is an equalizer design that can make negative and positive slopes, similar to the work of Itoh and Tagaki in 2016 [38]. What sets this work apart from Itoh's previous work is the use of lower voltage and wider operating frequency bands. The equalizer structure worked up to 1 GHz frequency in Itoh's work, although it increased to 1.6 GHz frequency in this study, it remains a low frequency for the proposed structure. In addition, although it can make positive and negative slopes, it provides only one option at the same time. In other

words, it can provide either a negative or positive slope. Tagaki's is not flexible enough for the proposed study.

There is an equalizer study that can make negative and positive slopes, which Bera has done in 2011 [39]. The system operates in the 3-5 GHz frequency band and slope levels are adjusted by changing the pin diode structure and resistance values. Bera's work has many differences from the proposed method because the operating frequency is much higher than the proposed method, the equalization range is narrower, and the configuration structure is adjusted with pin diodes.

It has been seen that the system can attenuate the gain level of the system, unlike the recommended working structure. This is a good example for further studies of the proposed method.

Unlike the studies in the literature, the proposed method, first of all, has an operating frequency of 258 MHz - 1.8 GHz, can be inclined at 1 dB step intervals up to 15 dB in positive and negative slope, has a return loss better than 10 dB, can operate with 3.3 V, and its slope can be adjusted. A circuit structure is proposed that can detect itself and automatically flatten the system gain.

4. METHODOLOGY

CATV systems are tightly controlled to protect the cable network, and systems must be designed according to standards for seamless interactive communication. For this reason, this study will be designed by adopting the DOCSIS standards, which set the standards for CATV systems and are recognized by the International Telecommunications Union (ITU). The device proposed in this study operates to cover the DOCSIS 4.0 extended-spectrum standard announced by the SCTE and was chosen to match the remote-controlled DOCSIS 4.0 announced by SCTE [12,13].

4.1. BLOCK DIAGRAM OF THE PROPOSED SYSTEM

A block diagram of how the transmission from the cable company distribution hub to subscribers is given in Figure 4.1. As explained in the previous sections, cable-relevant losses are experienced from cable company distribution hubs to subscribers, especially at high-frequencies. For this reason, it is vital to improve the gain slope, especially on the main distribution line, which is indicated as the red line in Figure 4.1. On distribution lines designated as green, slope improvement may be mandatory depending on the distance of the subscribers. The block diagram given in Figure 4.1 is important because it gives information about which areas of CATV distribution systems the proposed study can be used [40]. While the gain slope must be corrected in the red area of the block diagram, it may be mandatory in the green areas depending on the location of the subscribers, or gain slope correction may be made, even if it is not mandatory, to improve issues such as speed. It is planned that these gain adjustments can be made much more easily with the proposed method.

In order to better explain the proposed study, a CATV amplifier structure in which the project can be used is also important. Just as there is a general standard for certain frequency bands in CATV systems like 5 to 42/85/204 MHz upstream and 54/102/258 to 1.2 GHz downstream frequencies in DOCSIS 3.1 standards, a similar structure is generally used in system designs. The block diagram of an example CATV system is given in Figure 4.2. Each block of the system has the required frequency, gain, etc. It is specially designed according to the requirements [41].

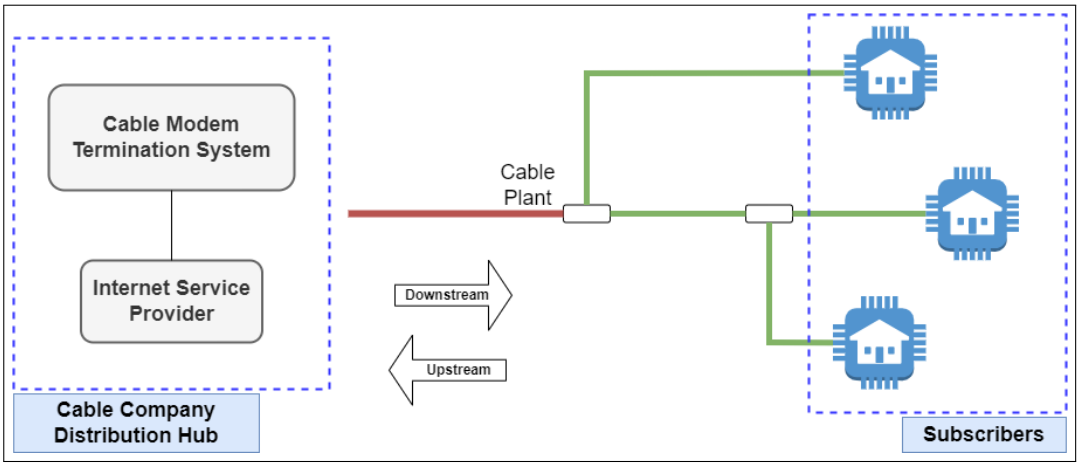

Figure 4.1. Block diagram of a CATV distribution system [4]

A typical CATV Amplifier block diagram is presented in Figure 4.2. CATV amplifiers include an amplifier block, attenuator pad, equalizer, and inverse equalizer. The forward path and the return path are separated by an RF diplexer. The number of gain blocks, attenuator, and equalizer pads are related to operator requirements and subsystem structure.

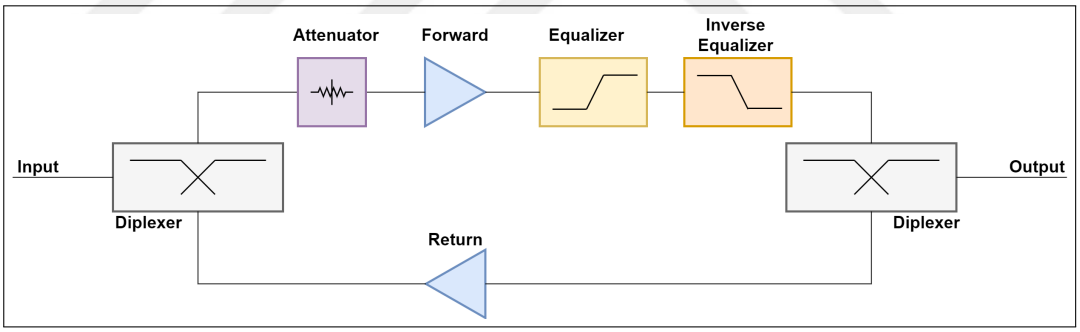

Figure 4.2. Block diagram of a general CATV amplifier [5]

In the proposed system, the inverse equalizer structure will be used before the equalizer structure. The block diagram of the proposed study which is planned to operate in the 258 MHz-1.8 GHz range study is presented in Figure 4.3 and can be located at the entrance, middle, or end of the device in the general CATV systems.

The reason why there is no attenuator in the block diagram of the proposed system, unlike the general CATV block diagram, is that the focus is on the slope of the gain curve, and maintaining the gain level is not important.

In the proposed system, the signal at RF IN primarily enters the Matching circuit/ Fixed

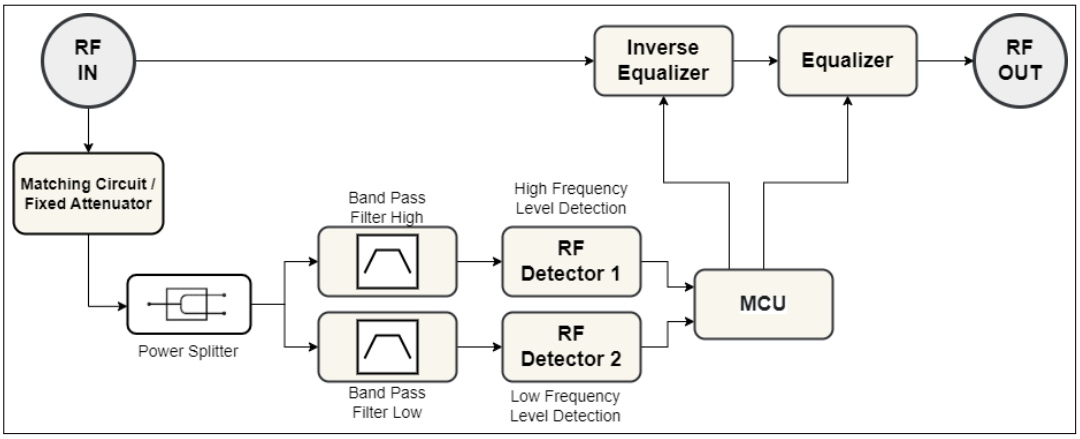

Figure 4.3. Block diagram of the proposed system

attenuator block in order not to enter the RF detector too strongly. Generally, in this type of application, the main signal is reduced by approximately 20 dB and enters the RF detector. In the proposed structure, a fixed attenuator stage was used to reduce the main signal by approximately 20 dB before the power splitter.

After the power splitter, the high-frequency pivot signal and low-frequency pivot signal are extracted by the surface acoustic wave (SAW) filters from the signals that are divided equally and transmitted to the SAW filters. SAW filters were selected at approximately 1575 MHz for high-frequency and 433 MHz for low-frequency. SAW filters provide a cleaner signal transition to the RF detector with a good level of suppression.

The low-frequency transmitted signal passes through the band pass filter low, and the RF detector 2 calculates and detects the level of the low-frequency signal. It outputs this as an analog voltage. Likewise, the high-frequency transmitted signal passes through the band pass filter high, and the signal level is detected by the RF detector 1.

RF detectors are actually hardware-related, not software-related. Detectors do help the software though. Integrated circuits (IC) selected for the proposed system can operate from 100 MHz to 2.7 GHz and have a very high sensitivity. Detectors can measure RF signals at -50 dBm minimum and 0 dBm maximum. The power detected at the input is produced as an analog voltage between 0 V and 1.9 V and transferred to the output. This voltage is increased by the OPAMP between 0 V and 3.3 V, which is the detecting range of the microcontroller unit (MCU). Thus, a wide reading range is produced for the analog-to-digital Converter (ADC)

pins of the MCU.

The microprocessor to be used in the proposed system must have two analog ADC inputs. With the aid of these two ADC inputs, it is possible to detect the level of the high-frequency signal coming from the input of RF detector 1 and the level of the low-frequency signal coming from the input of RF detector 2. This stage is provided with software support. After calculating the difference between the pivot signals, the slope of the gain slope is calculated. In order to correct this slope, the attenuation of which block should be increased and by how much is calculated and applied by the developed software. The amplitude level of the frequencies of 258 MHz, which is the beginning of the band, and 1.8 GHz, which is the end of the band, is considered linear and the entire band is expected to be smoothed with a negligible error.

If the slope calculated with software support is positive, the processor commands the equalizer structure to reduce the gain as necessary. With the aid of the equalizer structure, while the end of the band remains at the same level, the distance between the beginning of the band and the end of the band is reduced by the part where the gain needs to be equalized. If the slope is negative, the processor commands the inverse equalizer structure to reduce the gain as necessary. While the beginning of the band remains at the same level, the end of the band is reduced by the part where the gain needs to be equalized.

Detector values between 3.3 V and 0 V should be divided into 20 equal parts. So this ADC level allows us to read the 100-150 mV range. When choosing a microprocessor, 12-bits or more can be selected and better results can be obtained this way. However, since the prices of detectors over 12-bits are quite high, the 12-bits level is sufficient for the proposed system.

In addition to the reasons stated above, since the equalizer and inverse equalizer structures work with serial peripheral interface (SPI), it was decided to use M031FC1AE-TR from NUVOTON® Manufacturer in microprocessor selection, since the microprocessor is suitable for SPI communication and is advantageous in terms of cost in the proposed system. Low cost is one of the most important criteria for CATV, and the fact that the processor has a 12-bit ADC level makes it a complete price-performance product. The selected microprocessor is not only economical but also easy to obtain.

In summary, in the proposed system, even if the gain slope is positive or negative, the slope is eliminated by determining the signal level at the beginning and end of the band in which the device operates.

4.2. FREQUENCY OF OPERATION

Frequency of operation, one of the most important performance figures, has been determined as the DOCSIS 4.0 standard frequency band to comply with the above-mentioned DOCSIS standards. The system proposed in this study operates between 258 MHz and 1.8 GHz to cover the DOCSIS 4.0 extended-spectrum standard announced by the SCTE and was chosen to match the remote-controlled DOCSIS 4.0 announced by SCTE.

4.3. INSERTION LOSS

some of the signals from the generator are absorbed by a component placed between a generator and a load due to internal resistive losses. When the component is placed, most of the transmitted signals are not transferred to the load as much as when the load is connected directly to the generator. This resulting loss or weakening is called insertion loss. Insertion losses are one of the fundamental parameters of resonant circuits, and are expressed in decibels [16].

In the proposed study, there is a loss of up to 2 dB in resonance frequencies for equalizer and inverse equalizer operation. At maximum slope, the insertion loss can reach -4 dB at the resonance points, which are expected at the beginning and end of the frequency band.

4.4. ADJUSTMENT RANGE

The adjustment range parameter defines the signal level difference between the beginning frequency and the end frequency of the band. There are no active parts for equalizer and inverse equalizer that meet the DOCSIS 4.0 standard in the literature. With this knowledge, the adjustment range of 0 dB to 15 dB is meaningful for conventional CATV systems.

4.5. SYSTEM PORT IMPEDANCE

RF circuits often have system impedance. 75, 300, and 600 Ω are common system impedances, while 50 Ω is an almost universally used system impedance. In RF circuits, all elements of the system are expected to comply with the determined system impedance. In cases where the impedance is not matched, it reflects the signal and causes return loss and many similar problems, especially when power transfer is critical. RF circuits often use transformers or impedance matching networks to achieve impedance matching between source and load [16].

75 Ω is generally preferred in CATV systems as it has a transmission line impedance where the loss depending on the impedance is optimal. CATV system designs and the coaxial cables to be used are designed and selected by this impedance [16].

Coaxial cables used in CATV systems use metal foil as the outer conductor, resulting in a low-loss cable in a wide frequency range. Additionally, F-type connectors are generally used in CATV systems [16].

Since DOCSIS 4.0 standards recommend a 75 Ω impedance for CATV systems, input/output RF port impedances of 75 Ω are preferred in this study.

4.6. COST OF DEVICE

This module is for the CATV industry and cost is a very critical parameter, since there is no similar design to this smart gain slope management system (SGSMS), price is still a key parameter because of the amplifier's price competition. Passive mechanical parts are under 1 USD, and active voltage-controlled equalizers are more than 11 USD per unit price. Digital attenuators are about 3-5 USD per unit price. Also, there should be an MCU and an RF detector, which are common products for remote control. The design is completed with just digital step attenuators (DSA) rather than voltage-controlled equalizers to reduce the cost of the device.

5. SYSTEM DESIGN AND SIMULATION

Two studies were carried out for the system proposed in this thesis. One of them is the structure shown in Figure 4.3 in the Chapter 4 and the other one is the structure given in Figure 5.12.

In the first study, the resonance topology used in the equalizer and inverse equalizer circuits implemented with fixed resistors was used. This design was simulated and realized and measured on the printed circuit board (PCB), the problems seen in the measurement and simulation were explained and determined, then the second study was carried out. In this study the resonance topology was changed, the simulation was made and it was realized and measured on the PCB, in the second design the diplexer used in the first study was removed and instead the band head and end-of-band frequencies were determined with SAW filters, thus the pivot frequencies were fixed, the transfer of power from the input connector to the matching circuit. Impedance matching for the wide band was increased with the power splitter. As a result of these, the final design obtained in the second design was presented as the upgraded one, and it was preferred to present it as an alternative with the idea that it could be continued with the first design.

5.1. SUB-BLOCKS OF THE SYSTEM

The parameters given below include the necessary parameters used in both the first design block diagram and the final design block diagram. Attenuator and resonance circuits are two circuit blocks that form the equalizer and inverse equalizer. For this reason, in this section, resonance circuits and attenuator structures that constitute the equalizer and inverse equalizer structures are given.

5.1.1. Resonance Circuit

In this section, a detailed review of the resonance circuits used in equalizer and inverse equalizer structures and the main parameters affecting the resonance circuits are presented.

Resonant circuits are circuits designed and used to attenuate frequencies outside of a certain pass band. It is often used to pass a certain frequency or frequency group from the source to the load [16]. Electrical resonance occurs in an electric circuit at a particular resonant frequency when the impedances or admittances of circuit elements cancel each other. In some circuits, this happens when the impedance between the input and output of the circuit is almost zero and the transfer function is close to one.

Resonance circuits allow the signal to be transmitted to pass with very low distortion. It provides infinite attenuation above and below the desired frequency band and allows the creation of a perfectly rectangular pass band as shown Figure 5.1. This graph of the frequency response of the practically perfectly designed filter represents frequency-dependent attenuation, while f_1 represents lower frequency and f_2 represents upper frequency. However, due to the physical properties of the components that make up the filter, it is impossible to realize the designed perfect filter exactly [16].

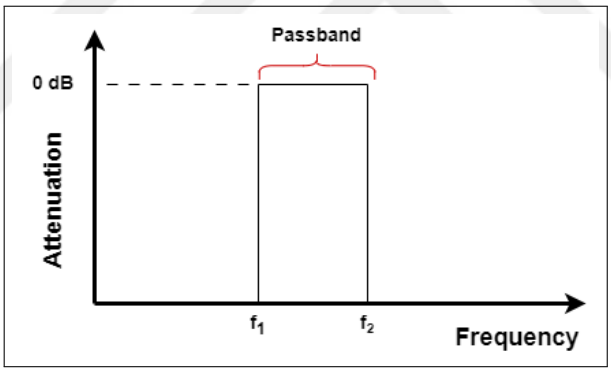

Figure 5.1. Frequency-dependent attenuation graph of practically perfectly designed filter

There are some important parameters in the design of resonant circuits. These are bandwidth, quality factor Q, ripple, attenuation, and insertion loss.

5.1.1.1. Bandwidth

The difference between the lowest (f_1) and the highest (f_2) frequency of the pass band of the amplitude response generated by any resonant circuit is defined as the bandwidth [42].

5.1.1.2. Quality Factor, Q

Since resonant circuits consist of capacitors and inductors, the Q values of each element must be checked when examining the Q factor.

The dissipation factor (DF) is the ratio of resistance to the reactance of a capacitor. Q of a circuit is the opposite of DF. It is defined as the quality factor of a capacitor, and the larger the Q value, the better the capacitor. The Q of an inductor is found as the ratio of its reactance to series resistance, unlike a capacitor. The larger the value of this ratio, which can be used as a measure of the inductor's quality, indicates that the inductor is better [42].

High Q circuits can be obtained using sampling techniques. It is easy to obtain narrow-bandwidth filters at low frequencies, while it is difficult to obtain them at high-frequencies. A high Q filter can be obtained by converting the narrow bandwidth obtained at low frequencies to high frequencies using the sampling process [20].

5.1.1.3. Ripple

The ripple, expressed in decibels, which is a measure of the flatness of the pass band of the resonant circuit, is physically measured in the response characteristics as the difference between the maximum attenuation in the pass band and the minimum attenuation in the pass band [42].

5.1.1.4. Attenuation

A perfect resonance circuit design provides infinite attenuation outside the desired passband, that is, the final attenuation called the final minimum attenuation that the resonant circuit presents outside the specified pass band. However, due to the physical nature of the circuit, it is impossible to achieve infinite attenuation, and if the response of the circuit is responding outside of the desired passband, it means that the resonant circuit is moving away from the attenuation specification [42].

5.1.1.5. Insertion Loss

The insertion loss is one of the important parameters for the resonance circuit as well as for the design in this study. This parameter defines the ratio of output to input RF signal strength and can also be defined as output power [dB] - input power [dB], apart from the expressions in the previous sections. The design goal in insertion loss for this module is -2 dB typical when the signal is flat across the frequency band [42].

5.1.2. Attenuator

An RF attenuator is used to reduce signal levels. There are various types of attenuators. SGSMS does not apply attenuation to the system, and because of that, there is no need for an attenuator in normal operation. In fact, for remote control or automatic operation, passive mechanical equalizers and inverse equalizers are not available for this design, active equalizers can be used but are not cost-effective. Active attenuators will be cost-effective to provide equalization and inverse equalization. Attenuators reduce signal levels in all the bands equally. However, the point of SGSMS is changing the slope of the signal. In this situation, attenuators will be used with resonance frequencies with some additional circuits and these products will be used as an equalizer and inverse equalizer.

Ideal attenuators have very low reflection, namely -40 dB. The most common usage areas of attenuators, which have many uses, can be given as an example to compare two related signals, reduce the effect of incompatibility, and provide isolation [43]. One of the areas where attenuators are frequently used is metrology. With the attenuators, the performance can be measured when necessary by giving a good insulation value and adjusting the parameters of the circuit blocks accordingly [44]. Apart from its widespread use, it is one of the areas where it is critically used in CATV systems [43].

In CATV systems, attenuator modules have a 20-30 dB attenuation range. This attenuation range is critical because this will limit the maximum slope of SGSMS. This range will reduce because the start of the frequency range is far from direct current (DC), when the slope is 20 dB from DC to 1.8 GHz, the actual slope will be 15 dB at 258 MHz because of the due to the slope of the triangle formed.

Although there are many passive and active attenuator circuit topologies, in this study, three passive resistive attenuator types that should be known will be mentioned. Resistive attenuators have three types. T-type, Pi-type, and bridged T-type are commonly known types of attenuators.

5.1.2.1. T-type Resistive Attenuator

T-type resistive attenuator consists of a total of three resistors, two resistors as floating, and a resistor is grounded between these two resistors. The values of the two floating resistors are required to be the same to form a symmetrical structure. Figure 5.2 shows the structure of the T-type resistive attenuator.

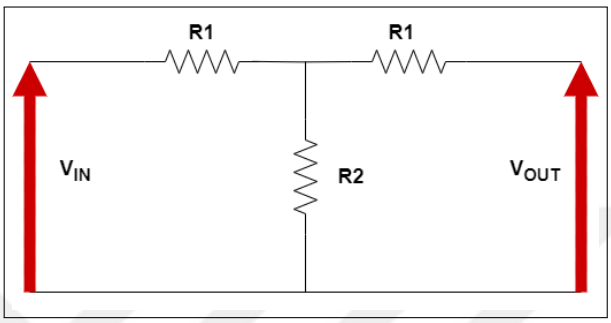

Figure 5.2. T-type resistive attenuator

The impedance matrix of the T-type attenuator is as in Equation (5.1) [45].

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} R1 + R2 & R2 \\ R2 & R1 + R2 \end{bmatrix} \tag{5.1}$$

The scattering matrix is obtained by using Equation (5.1), which is the impedance matrix of the T-type attenuator. The scattering matrix is given in Equation (5.2) [45].

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \frac{1}{(\hat{R_1} + 1)(\hat{R_1} + 2\hat{R_2} + 1)} \begin{bmatrix} \hat{R_1}(\hat{R_1} + 2\hat{R_2}) - 1 & 2\hat{R_2} \\ 2\hat{R_2} & \hat{R_1}(\hat{R_1} + 2\hat{R_2}) \end{bmatrix} \tag{5.2}$$

$\hat{R_1}$ and $\hat{R_2}$ given in Equation (5.2) are R1 and R2 normalized with respect to Z_0 [45].

$$\hat{R_2} = \frac{1 - \hat{R_1}^2}{2\hat{R_1}} \tag{5.3}$$

Assuming that both sides match and therefore S_{11} and S_{22} are equal and equal to zero, so Equation (5.3) can be written [45].

$$\hat{R_1} \leq 1, \hat{R_1} \leq \hat{R_0} \tag{5.4}$$

Both resistors are non-negative. Equation (5.4) can be inferred [45].

$$S_{11} = S_{12} = \frac{1 - \hat{R_1}}{1 + \hat{R_1}} \tag{5.5}$$

This Equation (5.5) can be obtained by using the Equation (5.2) and Equation (5.3) equations. Since S_{12} and S_{21} are also equal, Equation (5.5) can also be used to find S_{21} and S_{12}. Attenuation can be obtained from this Equation (5.5) [45].

$$L = -20log_{10}(S_{21}) \tag{5.6}$$

The attenuation obtained from this Equation (5.6) is a function of R_1 [45].

$$S_{21} = 10^{\frac{-L}{20}} \tag{5.7}$$

$$R_1 = Z_0 \frac{1 - S_{21}}{1 + S_{21}} \tag{5.8}$$

$$R_2 = Z_0 \frac{2S_{21}}{1 - S_{21}^2} \tag{5.9}$$

Thanks to these Equation (5.7),Equation (5.8), and Equation (5.9) R_1, R_2 and S_{11} values can be obtained while attenuation is determined [45].

5.1.2.2. Pi-type Resistive Attenuator

Pi-type resistive attenuator consists of a total of three resistors, one resistor in the transition line, and one resistor from two different ends of this resistor towards the ground. The values of the two resistors going towards the ground from the two separate nodes of the resistor in the series are required to be the same value in order to form a symmetrical structure. Figure 5.3 shows the structure of the Pi-type resistive attenuator.

In a case where the attenuator L value is determined based on the Equations (5.1) to (5.6) given in the T-type attenuator section, R_1 and R_2 formulas can be found from Equations (5.10)

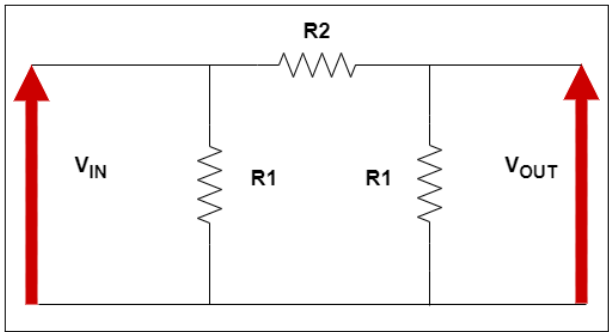

Figure 5.3. Pi-type resistive attenuator

and (5.11) [45].

$$R_1 = Z_0 \frac{1 - S_{21}}{1 + S_{21}} \tag{5.10}$$

$$R_2 = Z_0 \frac{2S_{21}}{1 - S_{21}^2} \tag{5.11}$$

5.1.2.3. Bridge T-type Resistive Attenuator

Bridge T-type resistive attenuator has one resistor in the transition line and one resistor from two different ends of this resistor to the ground and equal to the input impedance of the system, and from a total of four resistors, from the node where the parallel resistors are combined to the ground. occurs. Figure 5.4 shows the structure of the Bridge T-type resistive attenuator.

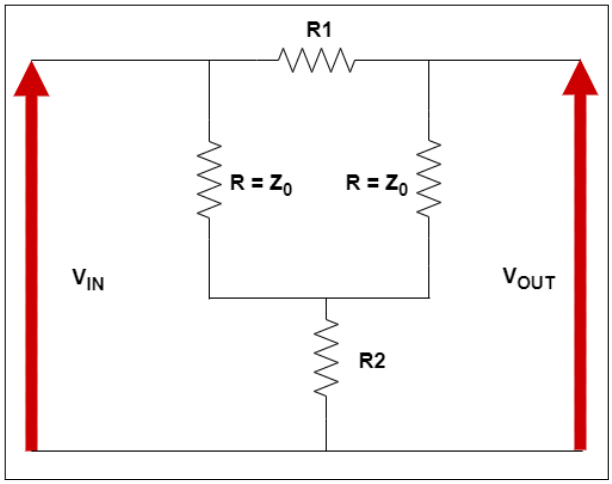

Figure 5.4. Bridge T-type resistive attenuator

5.2. EQUALIZER AND INVERSE EQUALIZER

Frequency-dependent passband ripple and gain slopes cause problems in RF circuits, and the solution to these frequency-relevant problems is to add an RF gain equalizer to the system. Equalizers are passive structures that help smooth out nonlinear curves in the gain response or phase characteristic. With the aid of these structures, a smooth output curve can be obtained. Frequency-dependent attenuation occurs in most broadband amplifiers, passive circuits, and physical transmission lines that are very commonly used in RF circuits, and this attenuation causes even greater attenuation as the operating frequency increases [46].

The main feature that distinguishes the equalizer, which consists of attenuator and resonance circuit structures, from the standard attenuator with a flat frequency response is that it exhibits lower insertion loss as the frequency increases with a certain slope. It is not possible for the equalizer, which ideally works with a minimum loss, to work without loss due to physical factors during rendering [47,48].

There are various types of equalizers for different applications and requirements. Equalizers can generally be divided into two categories active and passive structures. Active gain equalizers are simply structures that equalize the sloped gain of a circuit or flatten its curve. Active gain equalizers are voltage-controlled to change the slope level of the stabilizer with some voltage-controlled resistors and impedances. Passive gain equalizers are designed with passive attenuator topology and passive resonant circuits.

Equalizers are also divided into different types according to the different slope types of the designs. Negative slope equalizers are designed to simulate frequency-varying cable loss or amplifier behavior. When a multi-path communication line is in long range and short range in common, negative slope equalizers are preferred. Inverse equalizers are the most common types of applications. Another type which is the positive slope equalizer, is designed to compensate for the frequency response of long RF cables and amplifiers that cause the signal to fade as the frequency rises. These design types are the most common type of equalizer and are widely used in communication systems to smooth the broadband signal behavior in a system.

Equalizer and inverse equalizer structures are similar structures but with different typologies.

While there is an attenuator structure at the center of the two circuit structures, equalizer, and inverse equalizer structures are formed by connecting two L-C resonance circuits in parallel or shunt to the circuits in parallel or in series.

5.2.1. Equalizer Design

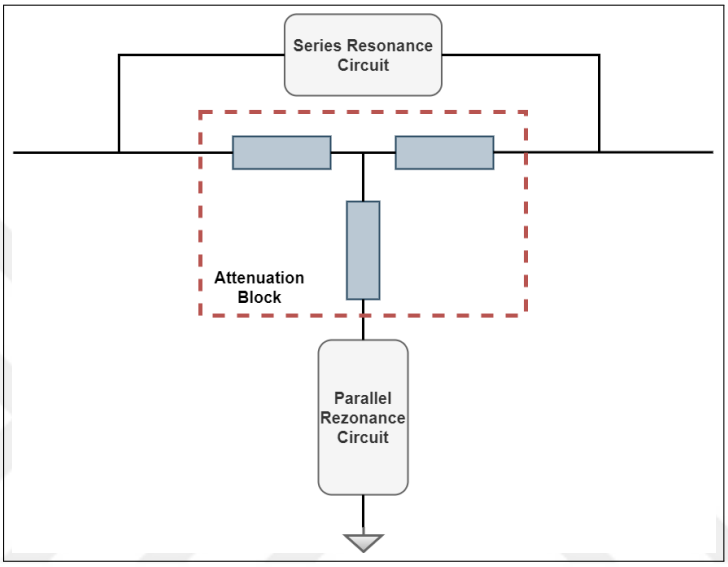

Figure 5.5. Equalizer structure

In order for the Equalizer structure to work, there must be an LC circuit in series with the circuit and an LC resonant circuit in series in parallel with the circuit. In the inverse equalizer, the structure is the opposite. In the inverse equalizer structure, there must be a series LC circuit parallel to the circuit and an LC resonant circuit parallel to the circuit in series. The series resonance circuit brings the impedance to the minimum at the resonance frequency formed by the LC structure. The parallel resonance circuit also maximizes the impedance at the resonance frequency created by the LC circuit. The equalizer structure is shown in Figure 5.5.

5.2.1.1. Fixed Passive Equalizer Design

The proposed circuit in Figure 5.6 shows the equalizer structure. The circuit structure consists of three resistors, one parallel to the circuit but in a series resonance circuit and a series resonance circuit that is parallel within itself but between the ground node and the resistor.

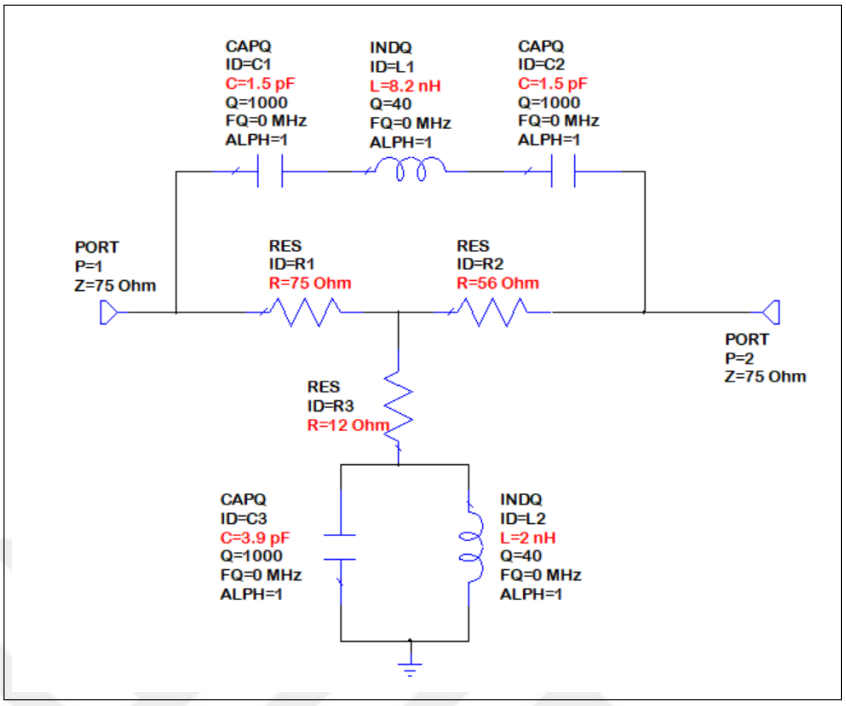

Figure 5.6. The 20 dB equalizer with lumped resistors

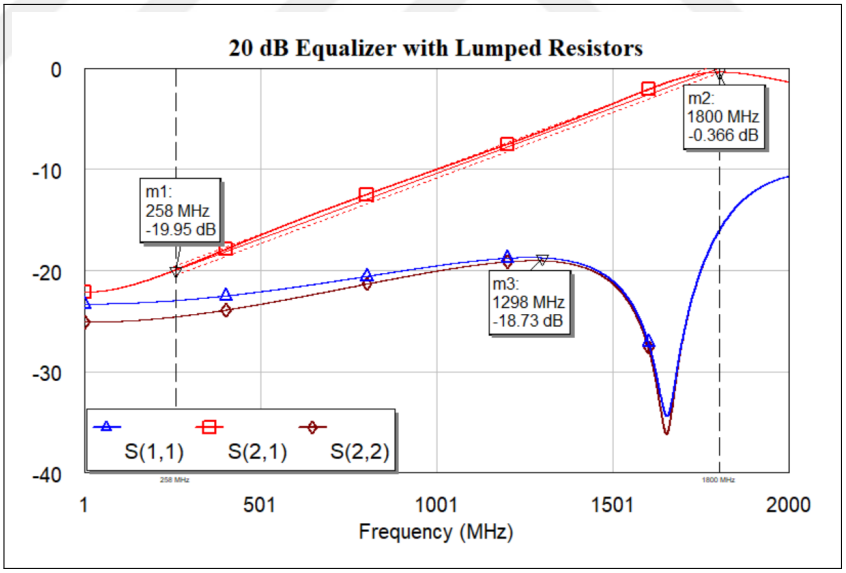

Figure 5.7. Simulation of the 20 dB equalizer with lumped resistors

An equalizer integrated circuit is used in the proposed circuit, but it is first shown that it works with a resistive attenuator. Thus, it has been proven that the equalizer structure in this structure works. The next thing to do is to replace the resistive attenuator with the DSA structure and achieve similar results.

As seen in Figure 5.7, as a result of the simulation of the circuit using AWR® simulation

program, it was observed that it was -19.95 dB at the beginning of the band and approximately -0.37 dB at the end of the band. Reflection results are better than -18 dB across almost the entire band. In the worst case, it provides the -15 dB reflection boundary condition. As a result of this simulation, it has been seen that the equalizer structure works with a resistive attenuator.

Equalizer design with lumped resistors works while 20 dB equalization is selected as seen in Figure 5.8. At the next step, resistors adjust to 0 dB pass but with the same resonance elements.

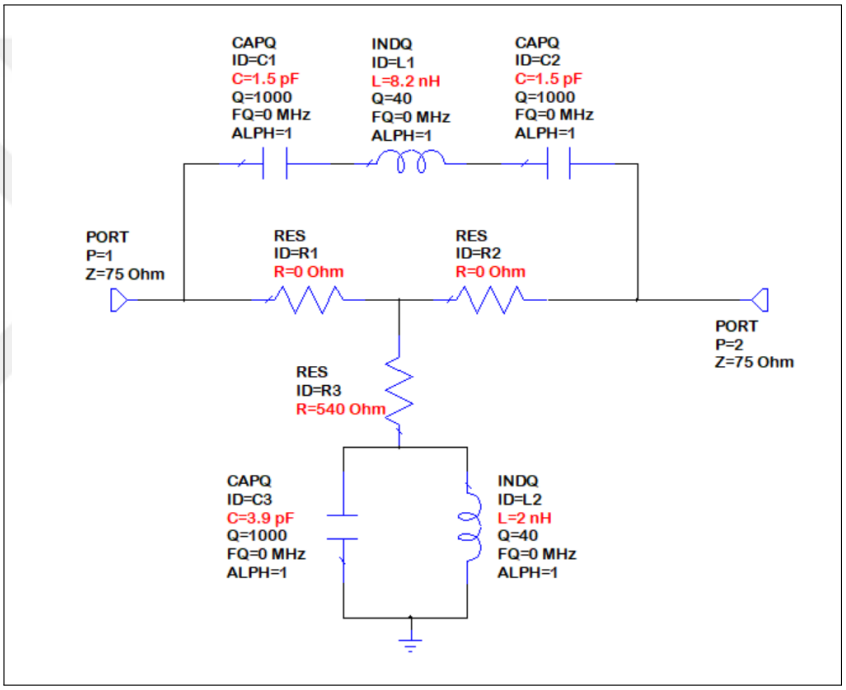

Figure 5.8. The 0 dB equalizer with lumped resistors

Figure 5.8 is basically the same structure as Figure 5.6. However, the resistive attenuator part is set to 0 dB instead of 20 dB. The schematic diagram of the 0 dB equalizer design is given in Figure 5.8.

Figure 5.9 shows the simulation result of 0 dB equalizer. Here, the simulation results are as expected from the theoretical equalizer structure. In this circuit, the resistive attenuator structure was bypassed with 0 Ω resistors, and an almost 0 dB gain loss, that is, a non-inclined structure, was planned and the results were obtained in this way. The beginning of the band has an S_{21} value of approximately -0.59 dB level at 258 MHz and the end of the band has a

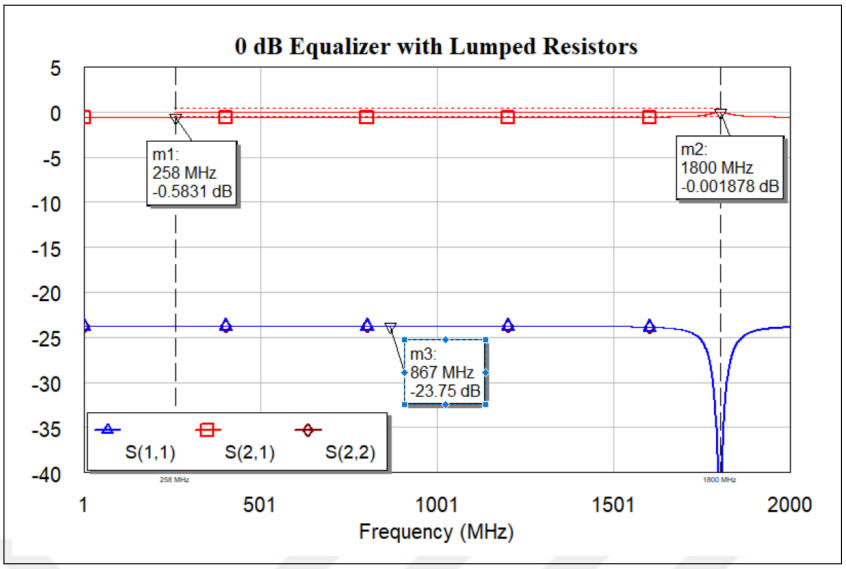

Figure 5.9. Simulation of the 0 dB equalizer with lumped resistors

value of S_{21} of approximately -0,1 dB level at 1.8 GHz. When the input and output reflections are examined, the worst reflection value throughout the band is at the -23.75 dB level at the 867 MHz frequency.

5.2.1.2. Passive Fixed Inverse Equalizer Design

Figure 5.10 has a fixed inverse equalizer structure designed with 75 Ω impedance at 20 dB level. The simulation result of this structure is given in Figure 5.11. Here, as in the Fixed equalizer structure, R1 = 75 Ω, R2 = 56 Ω and R3 = 12 Ω structures form an attenuator structure. However, the structure was transformed into an equalizer structure at a 20 dB level with a series resonance circuit from the attenuator to the ground as peripheral elements and a parallel resonance circuit parallel to the attenuator structure.

When the simulation result of the fixed inverse equalizer structure is examined, it is seen that it has an S_{21} value of -16.56 dB at the end of the band, while it is almost 0 dB at the beginning of the band. When the input and output reflections were examined, it was seen that there was a reflection of -16.54 dB at 636 MHz, which is the worst point.

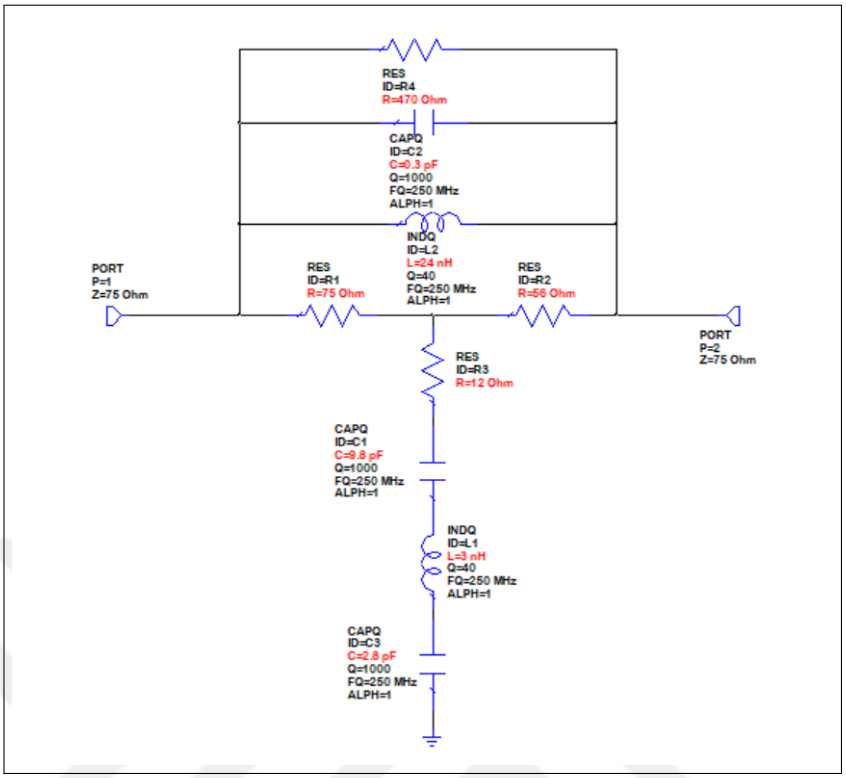

Figure 5.10. The 20 dB fixed inverse equalizer schematic diagram

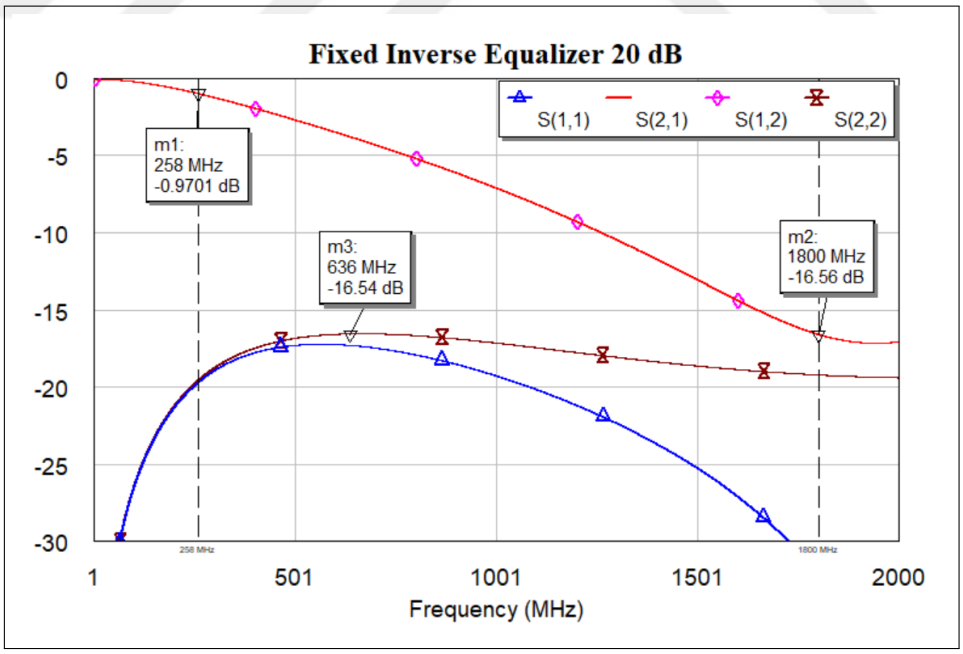

Figure 5.11. Simulation result of the 20 dB fixed inverse equalizer schematic diagram

5.3. SIMULATION RESULTS

5.3.1. First Design

Although the block diagram has essentially the same structure as the block diagram given in the methodology, the lower and upper frequencies are separated by a diplexer structure instead of a SAW filter. The DOCSIS channel plan allows the frequency band to be filled with analog and digital channels. For this reason, even if separated by a diplexer, both the pivot signals and the power of the broadcast channels enter the RF detector together.

In the first design, the diplexer does not pose a problem since only pivot frequencies will be applied to the system. In industrial applications, the correct method would be to use narrow-band bandpass filters operating at pivot frequencies. This is also possible with SAW filters. Although the diplexer application in the first design is sufficient to demonstrate the operability of the system, the SAW filter topology used in the final design is the closest application to reality.

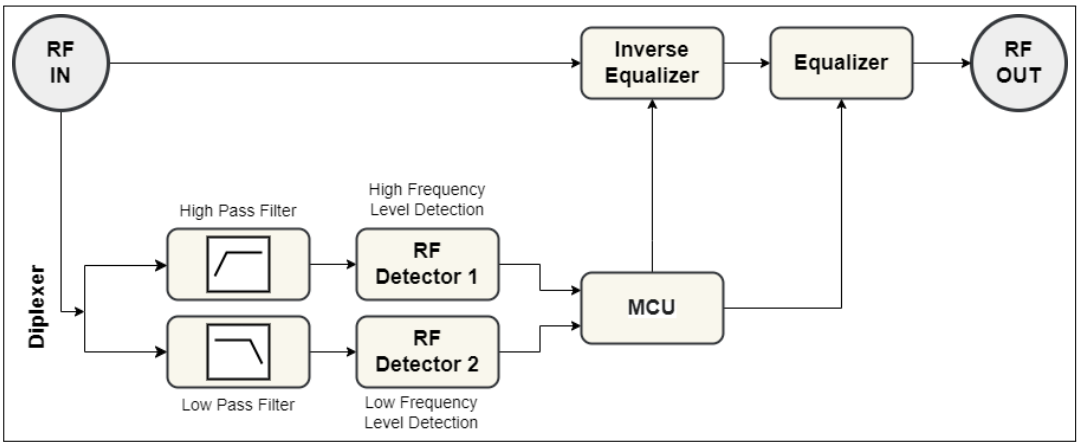

Figure 5.12. Block diagram of the proposed system

The structure created using diplexer is given in Figure 5.12. In this structure, the diplexer filter splits the band below 258 MHz for low-frequency pivot signal and above 700MHz for high-frequency pivot signal. While the system frequency band is 258 MHz to 1.8 GHz, a low-frequency pivot signal can be applied as a 258 MHz analog continuous waveform (CW) signal and a high-frequency pivot signal can be applied as a 1.8 GHz analog CW signal. splitter provides more than 50 dB suppression between pivot signals.

The low-frequency transmitted signal passes through the low-pass filter, and the RF detector calculates and detects the level of the low-frequency signal. The detector generates an analog signal dependent on the RF signal level. Likewise, the high-frequency transmitted signal passes through the high pass filter, and the signal level is detected by the RF detector.

After the RF signal goes in the detector, the final block diagram given in Figure 4.3 and the block diagram structures given in Figure 5.12 have the same structure. However, there are minor differences between the designs.

5.3.1.1. Equalizer Design and Simulation

The equalizer's operating frequency is similar to the design operating frequency of 258 MHz to 1.8 GHz. 0 to 15 dB slope variation is decided for the slope range. Topology is combined with parallel to attenuation circuit and parallel LC, shunt to attenuation circuit, and series LC. Digital step attenuator s2p simulation data provided by the manufacturer also additional impedance matching LC lumped element to adjust return loss and impedance errors when operating in the wide band frequency band. 0 dB and 20 dB DSA simulation data were used to get results for attenuation range behavior.

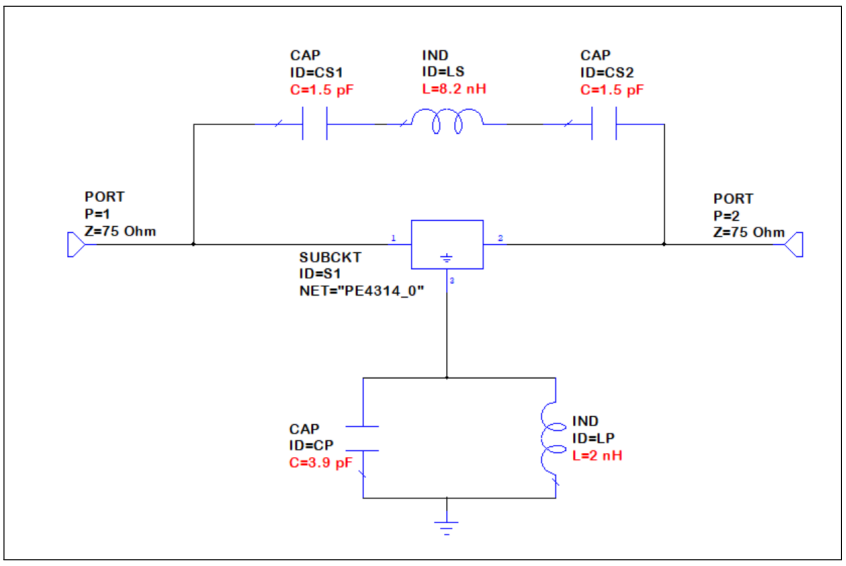

Figure 5.13. The 0 dB equalizer with DSA

The schematic in Figure 5.13 is the same as the 0 dB equalizer structure in Figure 5.8. The circuit structure given in Figure 5.8 and the simulation result in Figure 5.9 are actually to check whether the structure established with the resistive attenuator circuit is the same when

DSA is added to the circuit. In this circuit, instead of using a resistive attenuator structure, it is designed using 0 dB transition DSA.

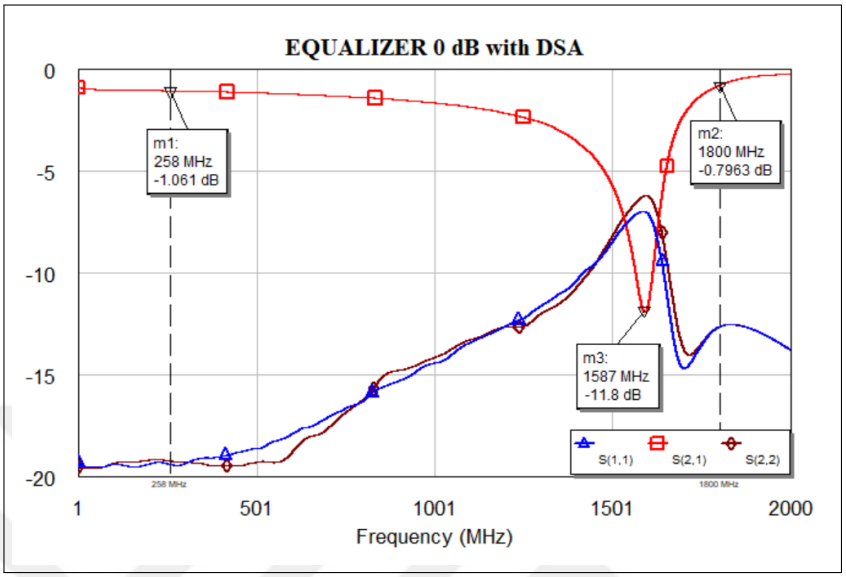

Figure 5.14. Simulation of the 0 dB equalizer with DSA

The simulation result given in Figure 5.14 proves that the equalizer structure can be equated to zero with DSA by giving an unsloped gain graph. This structure has better than 20 dB of return reflection, except at the very beginning of the tape. This value is very good for the proposed project.

However, this simulation result is expected to be the same as Figure 5.18, considering that Figure 5.6 and Figure 5.8 are the same in structure. Figure 5.14 has a loss at the beginning of the band that -1.06 dB and at the end of the band approximately -0.8 dB, however, there is a notch around 1587MHz which has -11.8 dB loss, while Figure 5.9 has a loss across the band between about 0 and 0.5 dB. When the return losses are compared, although Figure 5.14's results are satisfactory, as in the loss ratio, Figure 5.9's results gave better results. Although the results are very similar, the equalizer with DSA is more lossy, as expected, due to the specification of the IC. When the input and output reflections are examined, the worst reflection value throughout the band is at the -17.57 dB level at the 258 MHz frequency. The upgraded problem with the DSA-included simulation result is the notch in the band. This is caused by the DSA's parasitics and it is also analyzed on realized circuit.

In Figure 5.15, there is the manufactured version of the 0 dB pass DSA equalizer structure,

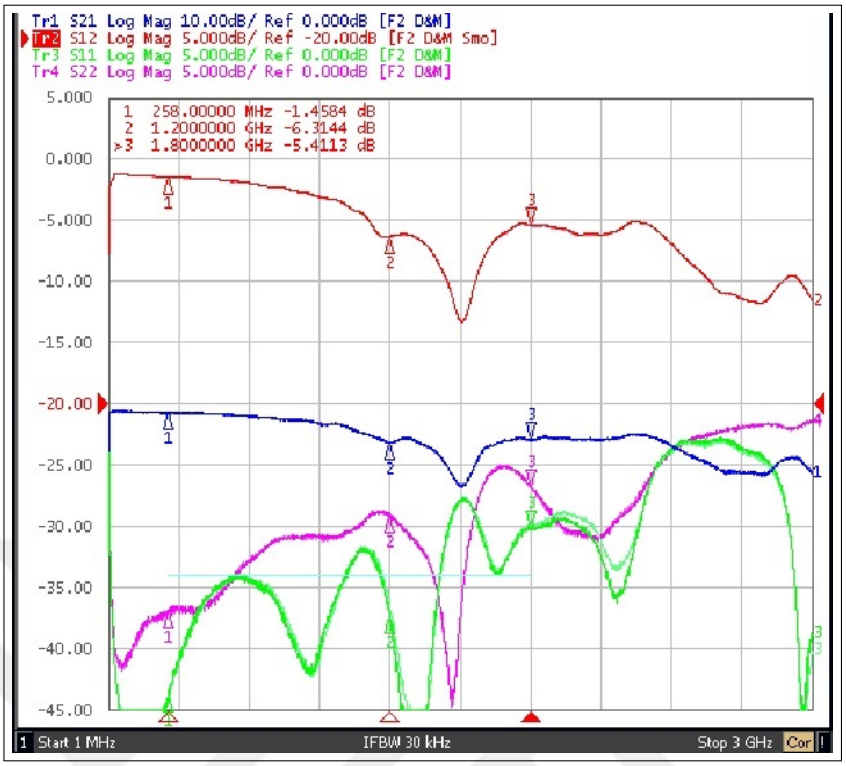

Figure 5.15. Measurement of the 0 dB equalizer with DSA and modified resonance

measured with the Agilent® 5062A Vector Network Analyzer. When the results are examined, there is a loss of about 1.5 dB at the beginning of the band and about 5.5 dB at the end of the band. The equalizer structure, which has a notch around 1.6 GHz, did not give the expected result by obtaining a result far from the simulation of the circuit. When the reflections are examined, it is seen that the output reflection gives good results at the worst 15 dB level at the beginning of the band and the input reflection gives good results at the worst 20 dB levels at the beginning of the band, but the result worsens from the middle of the band and decreases to 5 dB at the end of the band.

In Figure 5.16 is the schematic circuit of the equalizer structure with DSA set to 20 dB level. The structure is the same as the DSA equalizer circuit structure set to 0 dB in Figure 5.13.

In Figure 5.17, the simulation results of the schematic circuit given in Figure 5.16 are given. The result shows that equalizing is not observed as expected. after some optimizations, resonance frequencies are set to lower than 1.8 GHz which occurs in the band notch in the system.

Considering the reflections in the simulation results, it is seen that both the input and output

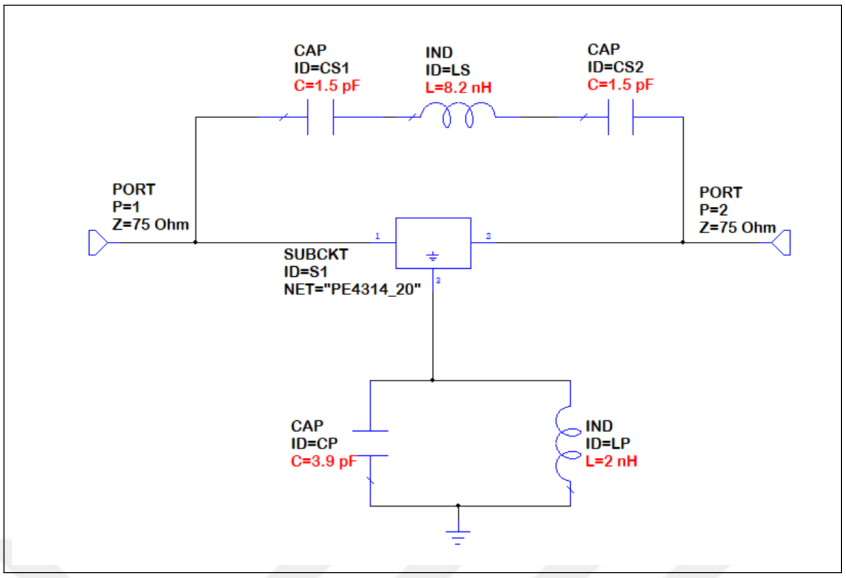

Figure 5.16. The 20 dB equalizer with DSA

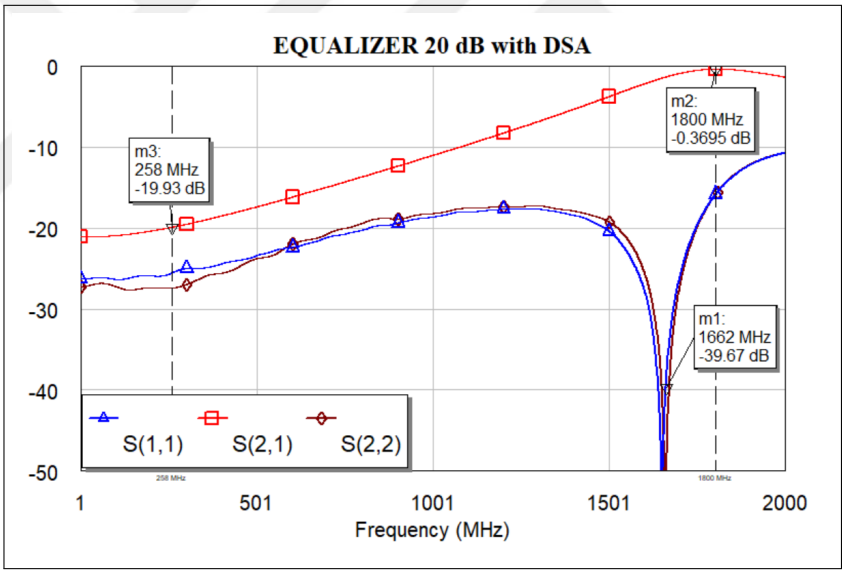

Figure 5.17. Simulation of the 20 dB equalizer with DSA and ideal resonance

reflections are at the level of 30 dB. When the input and output reflections are examined, the worst reflection value throughout the band is at the -15.95 dB level at the 1.8 GHz frequency.

Figure 5.18 shows that the equalizer circuit works up to 20 dB equalization range in the desired band. to provide resonance at the end of the band, resonance element values are selected as bigger than the simulation. thus affects the flat response of the equalizer as an undesired notch in the frequency band.

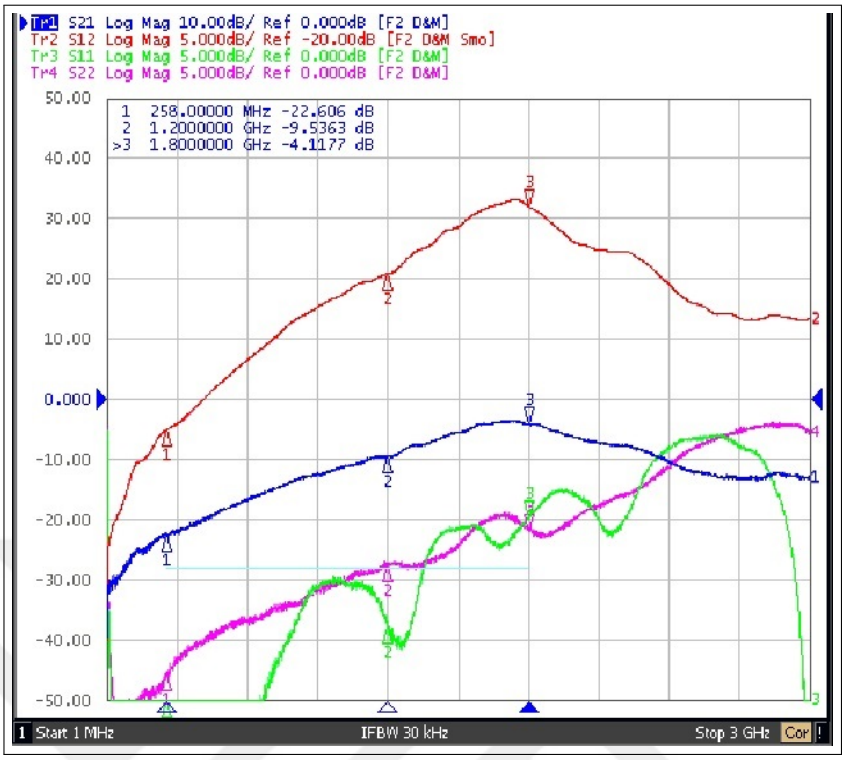

Figure 5.18. Measurement of the 20 dB equalizer with DSA and modified resonance

5.3.1.2. Inverse Equalizer Design and Simulation

The design includes two LC resonances. One resonance topology is generated as a series LCL circuit. This circuit is added to the ground node of the attenuator. The resonance frequency is 1978 MHz. The resonance frequency is higher than 1.8 GHz to reduce the gain decrease near the resonance. Another resonance topology is generated parallel to the attenuator input and output, including parallel LC and an additional resistor to optimize the linearity of the slope. Series resonance's frequency is 1897 MHz. Parallel resistor affects the Q of the circuit and gain decreases at the point of the resonance frequency decreasing also the slope of the gain becomes optimized. DC block series capacitors are selected at 27 pF and 56 pF, these levels provide a neutral high pass filtering while the frequency band of the design starts from 258 MHz. Design is firstly simulated with lumped resistors, after this step, design is simulated with Psemi®'s PE4314's 0 dB attenuation and -20 dB attenuation s2p file which is generated and provided by Psemi®. On the printed circuit, PE4314's pin-to-pin compatible alternative QPC4614 is also tested which is produced by Qorvo®.

AWR Microwave Office Software® simulation tool used to observe the results of the design.

The simulation includes no transmission line simulation and elements are chosen lumped elements with Q parameter definition. Simulation can be upgraded while the circuit layout is designed in PCB design program and transmission lines and dielectric and copper parameters while defined, can be added to the simulation.

Figure 5.19 shows the circuit of the inverse equalizer. There is a parallel LC resonance circuit from the input to the output of the circuit and there is a resistance that makes the curve formed by the LC circuit to be flatter. Adding resistors to the circuit makes the curve taper a little where it notches, thus making the curve more linear. For example, this circuit set to 1.8 GHz, ensures that the gain is at the bottom at 1.8 GHz. The LC resonance circuit, which is placed towards the ground but in series with each other, also helps it. These two resonance circuits are also tuned to 1.8 GHz.

In fact, the parallel LC resonance circuit that is parallel to the circuit and the serial LC resonance circuit between the ground and the ground node of the attenuator do the same job. Inductors, ground capacitances, and bypass capacitances are used to correct the reflection.

The proposed circuit structure starts at almost -1 dB from 258 MHz to 1.8 GHz and goes down almost linearly to 15 dB gain. While this provides a linear curve, it also allows us to see a reflection better than 15 dB inside the band.

The fitting elements used in the circuit, and the resistor also help this. The resonance circuits are also tuned to 1.8 GHz. The resulting curve can be cambered or reverse cambered or pitted. This is determined by the ratio of the capacitance and inductor values used in the resonance circuits, namely the Q-Factor. This slope can be adjusted by changing the ratios by making the ratio of the capacitor value to the inductor value or vice versa too high or too low.

The inverse equalizer circuit schematic with the DSA structure set to 15 dB is given in Figure 5.19.

Figure 5.20, the simulation result of Figure 5.19, provides a better than 18 dB return loss at the beginning of the band and then decreases to 15 dB in the band. This topology‘s results confirm the topology’s expected behavior. The return loss of the systems is better than -15.64 dB and insertion loss is -1.03 dB at the beginning of the band, and -15.08 dB at the end of

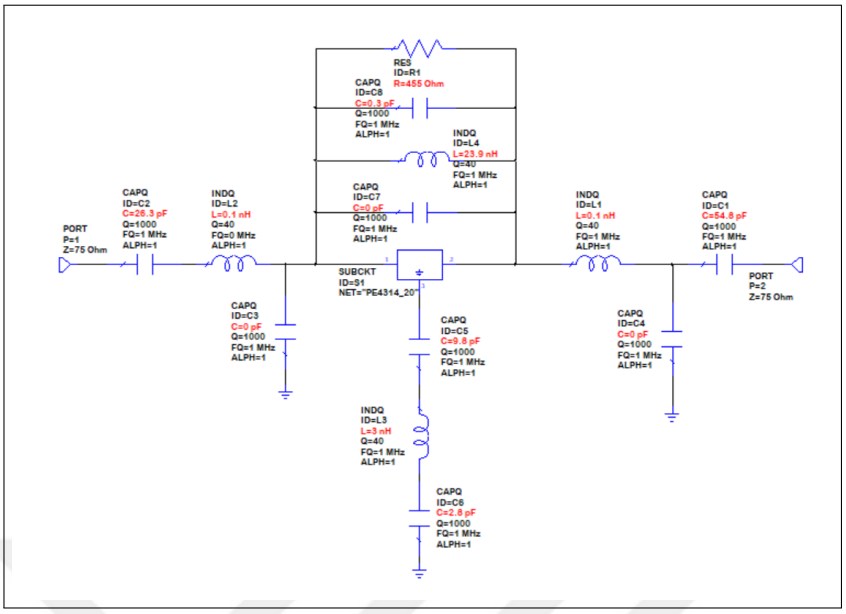

Figure 5.19. The inverse equalizer schematic with 15 dB DSA

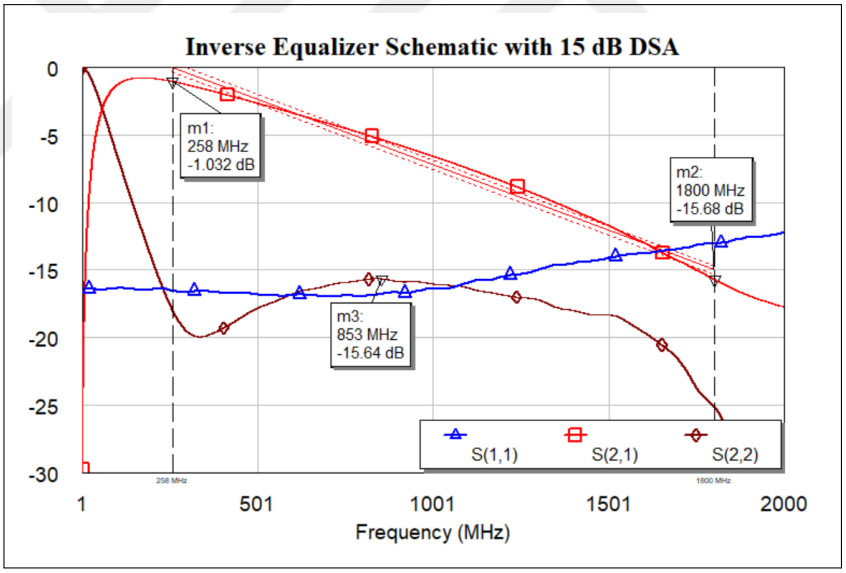

Figure 5.20. Simulation of the inverse equalizer with 15 dB DSA

the frequency band. Additional simulations have been worked to provide better return loss and linear slope.

The schematic of the 0 dB transition of the digital step attenuator used in the inverse equalizer circuit is proposed in Figure 5.21.

0 dB inverse equalizer given in Figure 5.21 in the AWR® simulation program is given in Figure 5.22. It is not possible to dim the digital step attenuator using AWR® simulation tools.

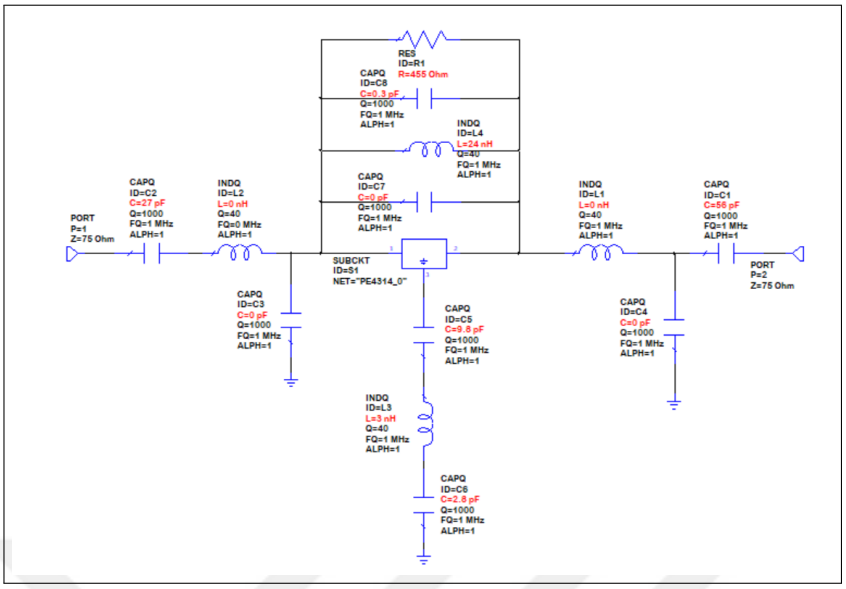

Figure 5.21. The inverse equalizer schematic with 0 dB DSA

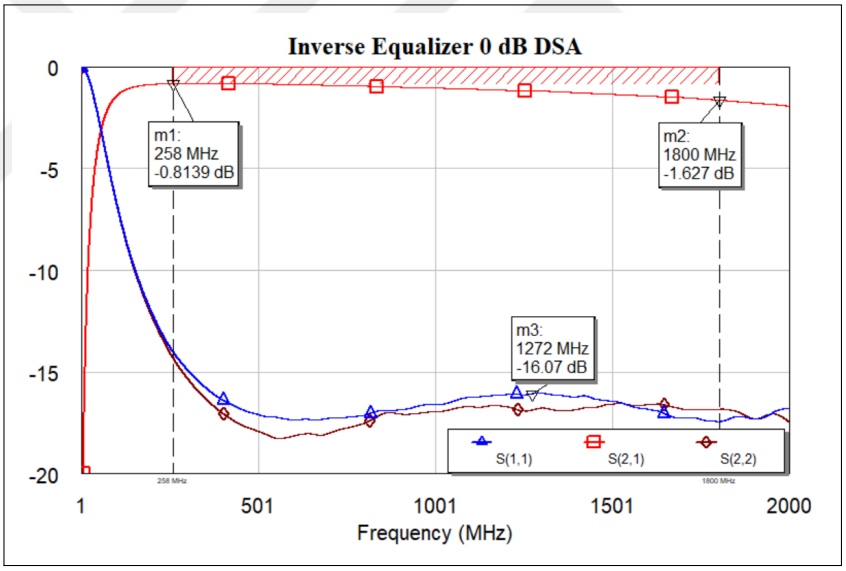

Figure 5.22. Simulation of the inverse equalizer with 0 dB DSA

For this reason, *S*-parameter values are taken for the connection setting of intermediate values between 0 dB, 10 dB, and 15 dB. If the digital step attenuator is set to 0 dB, the circuit gain is expected to be flat. For this setting, the resonance values of the circuit are not changed. The *S*-parameter file of the digital step attenuator is replaced according to the first simulation application, the other elements remain the same. Almost lossless gain is seen from 258 MHz to 1.8 GHz. This loss is already the default loss of the circuit. This loss is due to physical reasons and integrated use. The losses caused by the integration are defined in the datasheet

of the integration.

As a result of the circuit simulation, it is seen that the return losses are almost better than 18 dB. As a result of the simulation, it is clearly seen that the proposed topology operates properly. This result shows that the resonances created by the resonant circuit did not disturb the circuit substantially. So the circuit also works at 0 dB. It also works when the digital step attenuator is used in inverse equalizer mode. It can be seen with the values obtained as a result of these two simulations.

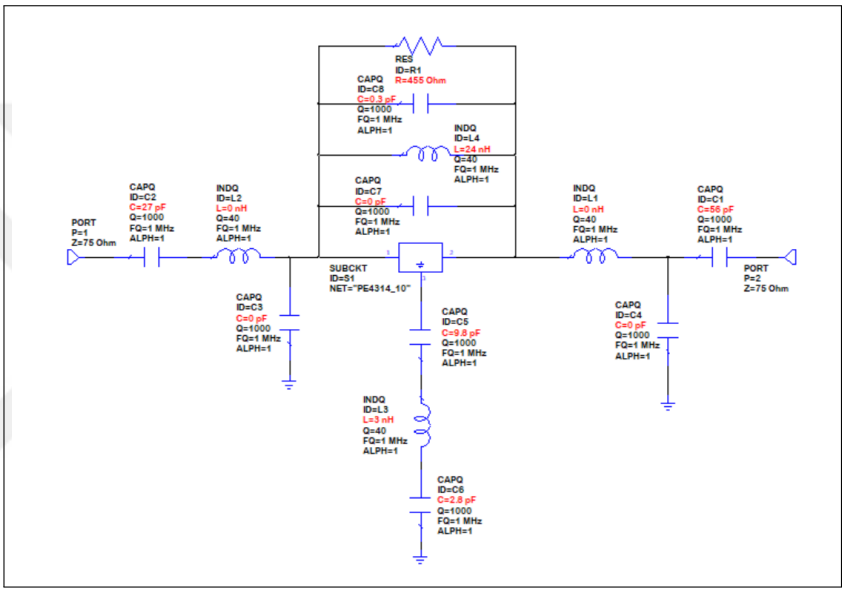

Figure 5.23. The inverse equalizer schematic with 10 dB DSA

In Figure 5.23, the circuit structure of the digital step attenuator, which is created as 10 dB by using another value, is shown. The *S*-parameter of the value used was thrown into the AWR® simulation program and added to the circuit as a sub-circuit.

It can be seen from Figure 5.24 that the circuit created with 10 dB attenuation also works smoothly. This simulation was done to validate the structure. There is a loss of 1.25 dB at the beginning of the band and 9.825 dB at the end of the band. When the reflections are examined, it is seen that the input and output return loss gives good results at the level of 15 dB along the band.

While resonance circuits remain the same, expected equalization results were not observed. Resonance frequencies are higher than the expected band and it occurs unwanted equalization behavior.

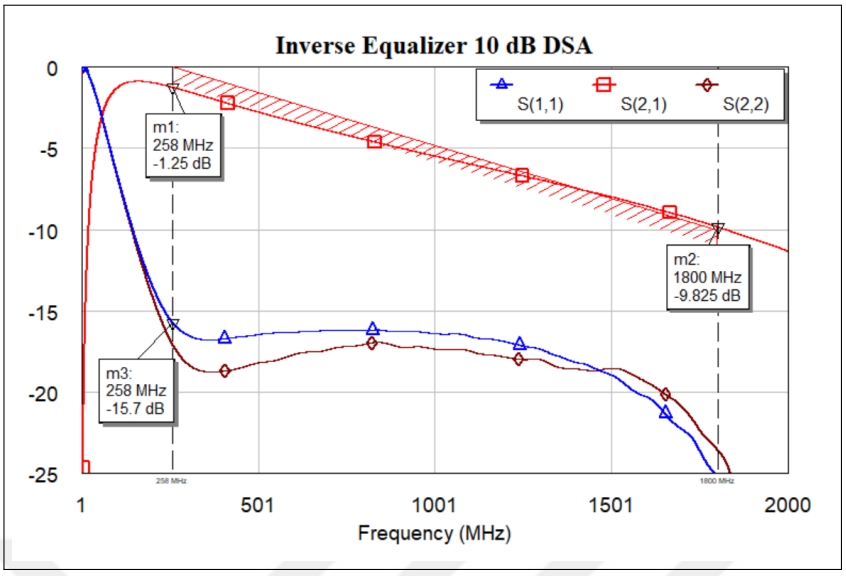

Figure 5.24. Simulation of the inverse equalizer with 10 dB DSA

5.3.1.3. RF Detection

The slope is measured with the signal level of two pivot frequencies. These two frequencies address the beginning and end of the frequency band for the proposed system. These frequencies are selected at the edge of the frequency band, and the gain slope is assumed linear. The AD8314 was chosen as the RF detector IC to measure the total RF power at the outputs of the diplexers.

5.3.1.4. Diplexer

Diplexer is a filter that has three ports combined with a low pass filter and a high pass filter. This filter separates high-frequency and low-frequency with a stop band. This structure is useful for bidirectional systems and frequency division multiplexing applications. For SGSMS, the frequency band is divided as DC to 258 MHz and 700 MHz to 1.8 GHz.

Given in Figure 5.25 is the simple diplexer designed to verify that the equalizer and inverse equalizer constructs designed for the proposed system work.

The result of the AWR® simulation program of the diplexer structure designed for the proposed system in Figure 5.26 is given. Considering the simulation results, it is seen that the designed diplexer structure separates the circuit at 258 MHz, which is determined as the lower frequency, and 700 MHz, which is determined as the upper frequency, very close to the

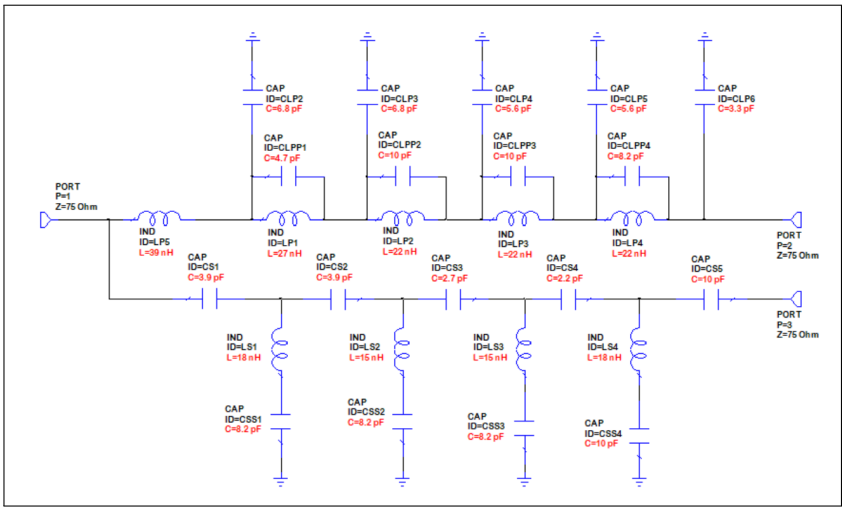

Figure 5.25. The diplexer schematic diagram

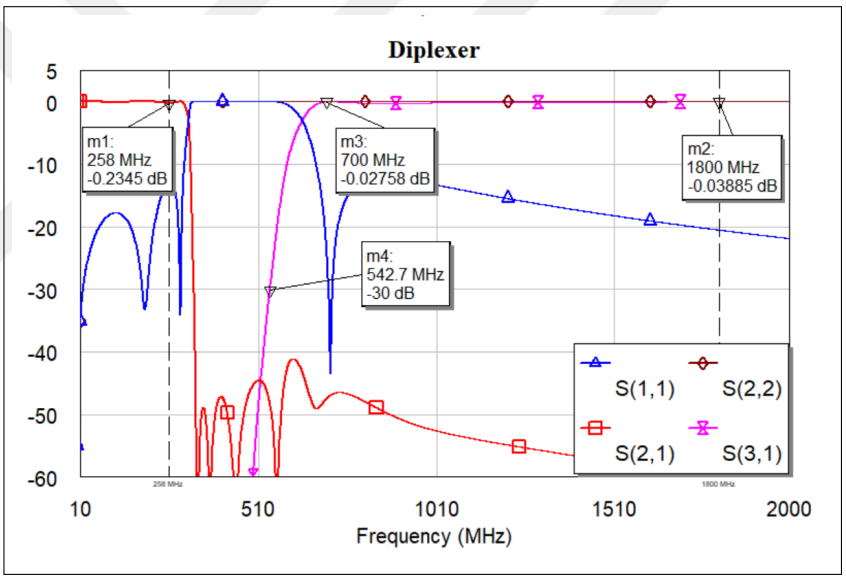

Figure 5.26. Simulation of the diplexer

planned one. It is seen that the diplexer structure suppresses approximately 30 dB after the determined lower frequency band and before the determined frequency point for the upper frequencies. It appears to suppress -30.08 dB at 328.9 MHz and -30.6 dB at 542.8 MHz.

5.3.1.5. The Manufactured Circuit

The PCB Circuit drawn on the PCB design program of the proposed system is given in Figure 5.27. The drawn PCB consists of two layers, the top and bottom layers, and the thickness of these two layers is equal to 1 oz, 35 µm. 1.6 mm thick FR-4 material is used as the dielectric material of the PCB board.

The designed diplexer, equalizer, and inverse structures are collectively arranged on a common board in the circuit. Particular attention has been paid to the fact that the capacitors used on the RF line are C0G dielectric materials.

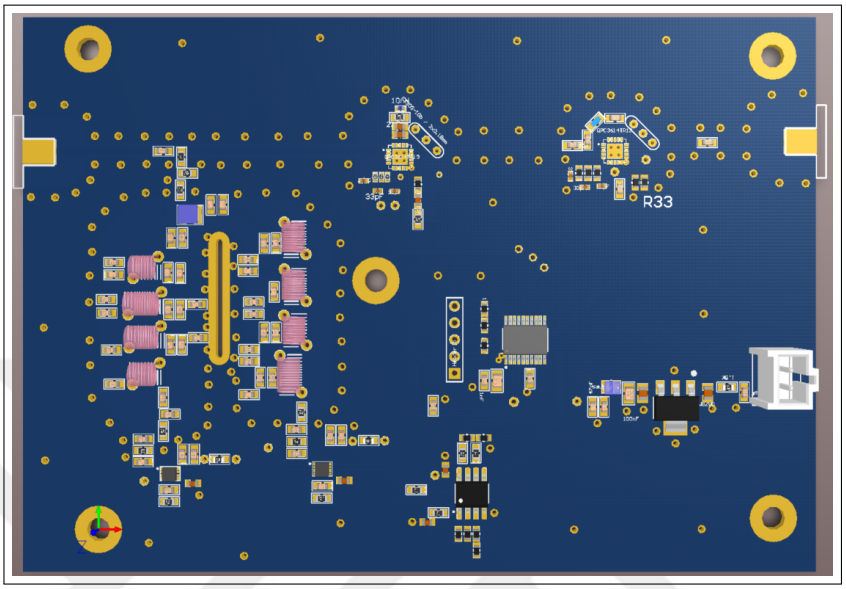

Figure 5.27. The PCB image

The surface mount device (SMD) top string of the designed PCB drawing is given in Figure 5.28. The values of the proposed equalizer, inverse equalizer, and diplexer structures on the PCB can also be found here. Optional elements as X added on the PCB are left for impedance matching of the circuit and places where capacitors should be thrown to the ground.

The produced version of the PCB Circuit drawn on the PCB design program is given in Figure 5.29. The 5 V supply of the card is provided from the DC supply source with a jumper cable, and the ground of the supply source is directly attached to the board.

Since it was decided to use 75 Ω of the circuit as stated in the above sections, an F-type connector was used accordingly. For the input and output ports, two F-type connectors were attached to the right and left sides of the board, and the measurements were taken.

The vector network analyzer (VNA) measurement result of the manufactured version of the PCB designed for the proposed system is given in Figure 5.30. This circuit is measured for the system with the equalizer and inverse equalizer structure turned on. When the measurement results are examined, it is seen that the input and output reflection is measured at the level of

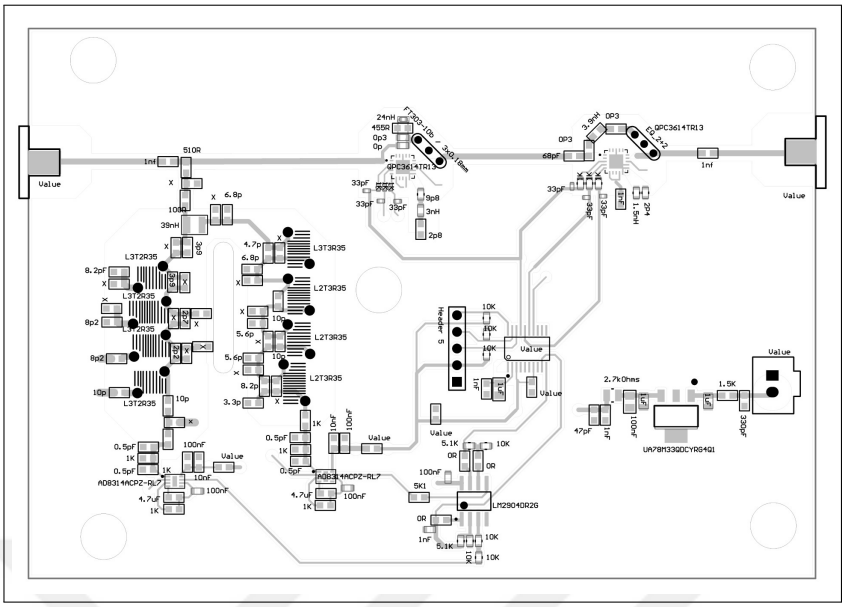

Figure 5.28. The PCB SMD component array and values

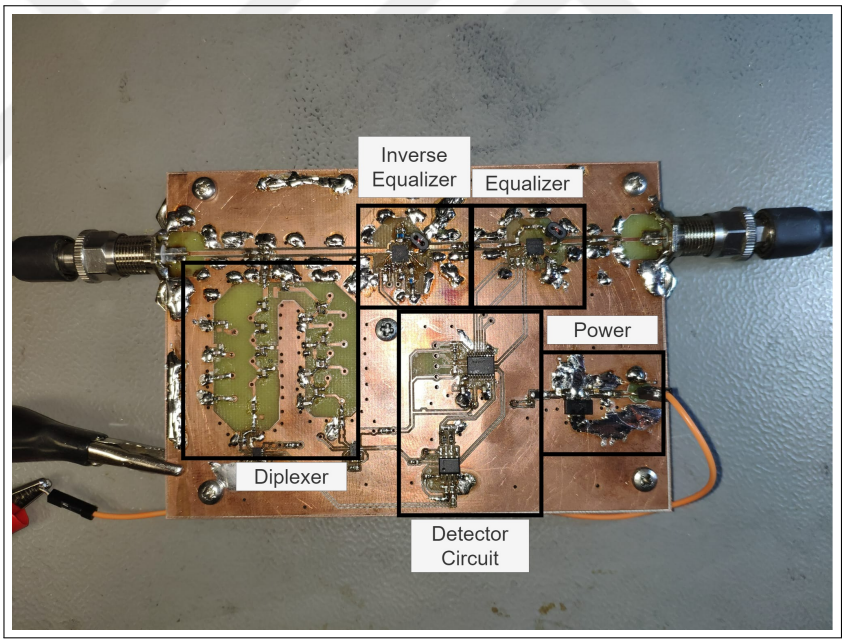

Figure 5.29. The manufactured PCB view

15 dB from the beginning of the band to the frequency of approximately 900 MHz. After this frequency, the output reflection sees the worst 12 dB levels in the continuation of the frequency band, while the input reflection decreases to 8 dB levels in the continuation of the band.

It is seen that the circuit, which has a loss of approximately 24 dB at the beginning and end

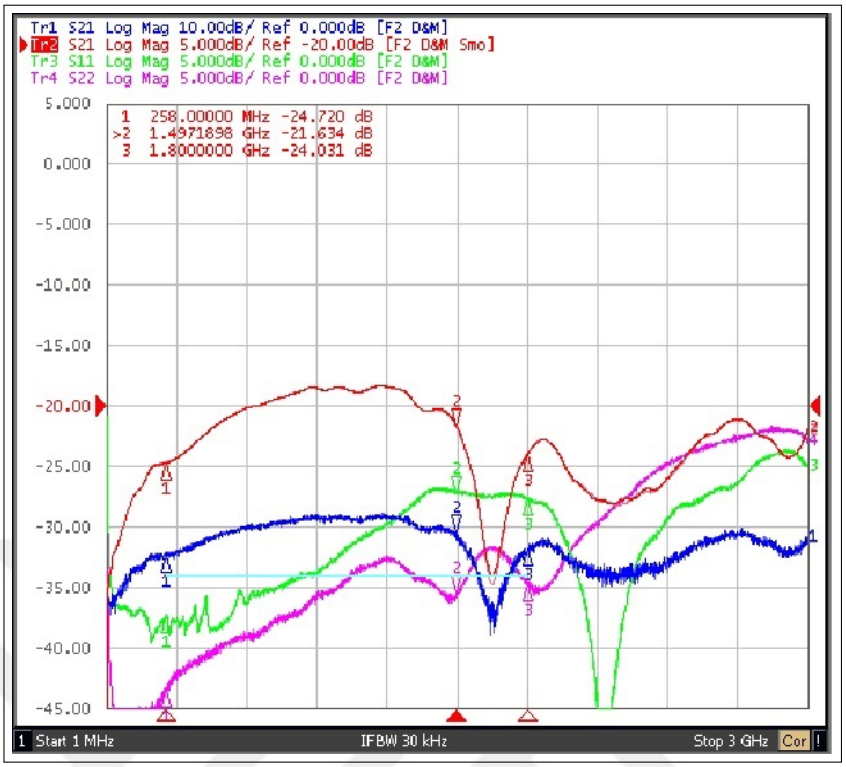

Figure 5.30. The manufactured PCB measurement with equalizer on and inverse equalizer on situation

of the band, does notch. Notch filters are structures that pass all frequencies except those between the lower and upper cut-off frequencies [16]. Here, the notch filter structure is formed due to the equalizer structure of the system.

The VNA measurement result of the manufactured version of the PCB designed for the proposed system is given in Figure 5.31. This circuit is measured for the system where the equalizer structure is on 15 dB equalization and the inverse equalizer structure is on 0 dB pass mode. Looking at the measurement results, it is seen that the output reflection is at the lowest level of 15 dB at the beginning and middle of the band, but at the worst level of 8 dB at the end of the band. Input return loss, on the other hand, sees its lowest level at 10 dB in the middle of the band.

When the equalizer structure is open, it is seen that there is a loss of approximately 11.9 dB at the end of the loss band, which is about 24.5 dB at the beginning of the welded band. It has been observed that there is a 12.6 dB difference at the beginning and end of the band. The reason why the system notchs at approximately 1.6 GHz is that the equalizer structure in

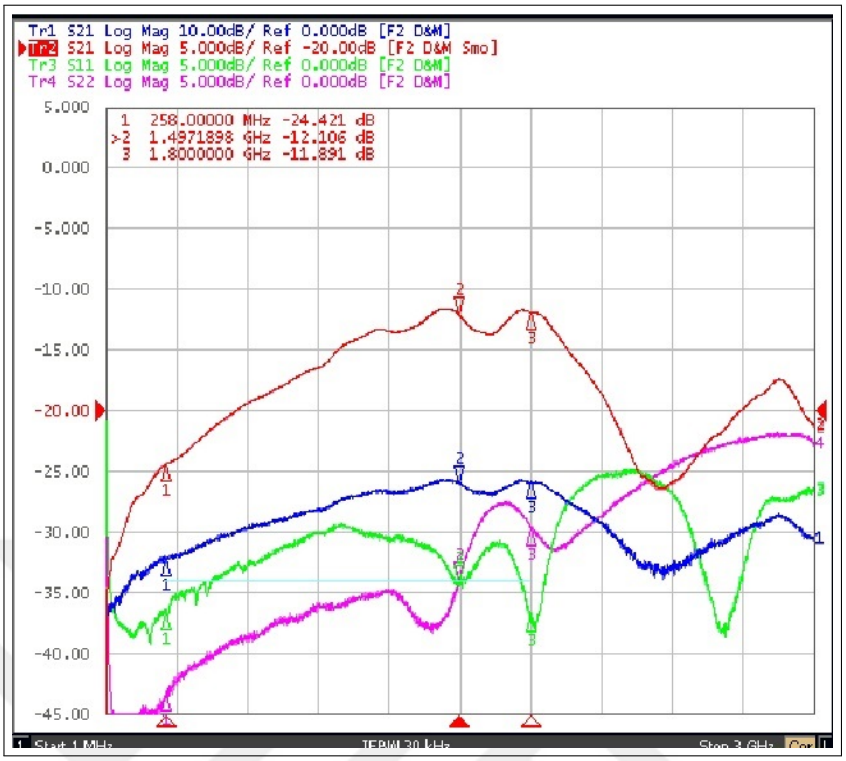

Figure 5.31. The manufactured PCB measurement with equalizer on and inverse equalizer off situation

the system does notch.

The VNA measurement was taken for the 0 dB pass for both structures' state of the produced PCB circuit of the circuit proposed in Figure 5.32. When the return losses are examined, the input and output return loss are at 15 dB levels at the beginning of the band, and 5 dB at the end of the band in the worst case.

The loss of the circuit, which is around 2.9 dB at the beginning of the band, suffers more than expected at the 1.5 GHz frequency. This is due to the notch created by the equalizer structure in the system. Improvement of the notch will be provided in future work.

5.3.2. Final Design

In this section, the final design of the block diagram structure in Figure 4.3, which was designed using the SAW filter structure, is explained. Unlike the first design, the part from the RF IN input to the RF detector has been updated. The diplexer filter structure separates

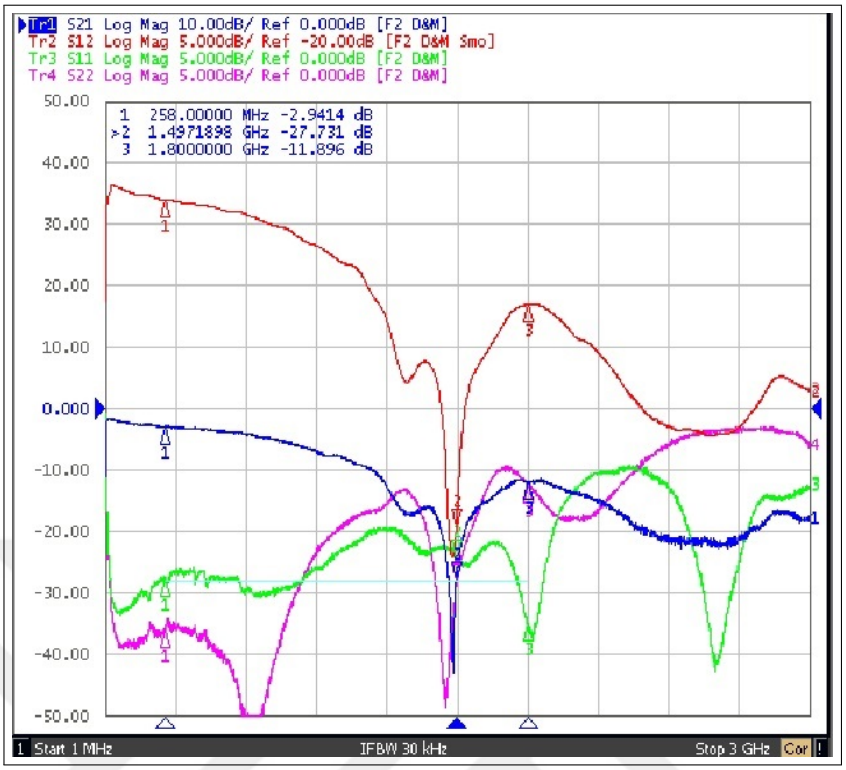

Figure 5.32. The manufactured PCB measurement with full flat situation

low and high-frequencies, but it has a complex filter structure. Instead, the SAW filter structure was used and tested. Diplexer and SAW filter structures will finally be compared.

5.3.2.1. Matching Circuit

The RF detector's maximum total composite input power is 0 dBm. For this reason, it is generally reduced with an attenuator matching circuit in such applications which have higher than 0 dBm composite input power. A fixed attenuator structure of approximately 20 dB levels was placed between the RF IN and the power splitter.

5.3.2.2. SAW Filters

In this study, two SAW filters were used low-frequency and high-frequency filters. For the low-frequency filter, the B3710 SAW filter of the Qualcomm® brand was preferred. It is a filter with a center frequency of 433.92 MHz. For the high-frequency filter, Raltron brand®'s RSF-1575.420-2000-1411-TR RF SAW filter model was preferred. The center frequency of this filter is 1575.420 MHz and has a bandwidth of 2 MHz. Since the operating frequencies of the SAW filters on the market are not suitable for the use of the frequency range of 258

to 1.8 GHz, the most suitable RF SAW filter models in the market were selected for low and high-frequency filter applications.

In addition to the fact that there are no frequency filters in the market that comply with DOCSIS 4.0 standards, a suitable 75 Ω RF SAW filter that can be used for the application cannot be found. For this reason, RF SAW filters with 50 Ω impedance were used for both low and high-frequency SAW filters.

5.3.2.3. Equalizer Design and Simulation

The equalizer structure has been changed in the final structure. In the equalizer circuit in the first structure, there were large notches in the middle of the band shown in Figure 5.15. The notches were undesirably deep, so the notches had to be removed. The equalizer used in the first system had two resonance circuits. These resonance circuits are located between ground and equalizer integrated circuits and between input and output. Resistance is added to these two resonant circuits. These resistors disrupt the Q of the circuit and thus pull the resonance going to the ground a little further inward. While changing the Q value reduces the effect of the notch, the added RC resonance helps to eliminate the targeted notch depth by ensuring that this notch is wide rather than narrow. It causes Notch to reach 1-2 dB levels and spreads. With this structure, it seems like there is only a ripple in gain level, but it is at a tolerable level.

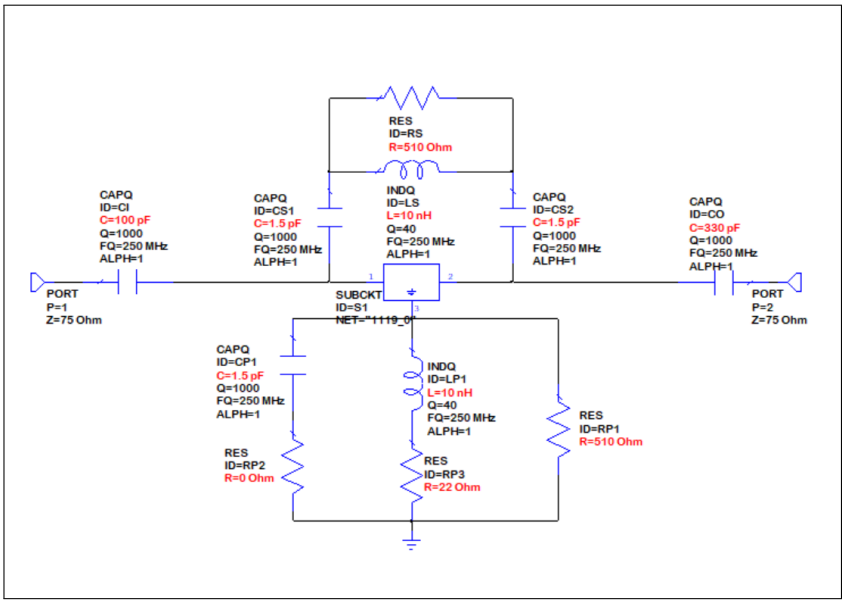

Figure 5.33. The 0 dB equalizer with HMC1119

In Figure 5.33, resistance is added to the resonant circuits, and the HMC1119 integrated circuit is simulated with 0 dB transition parameters.

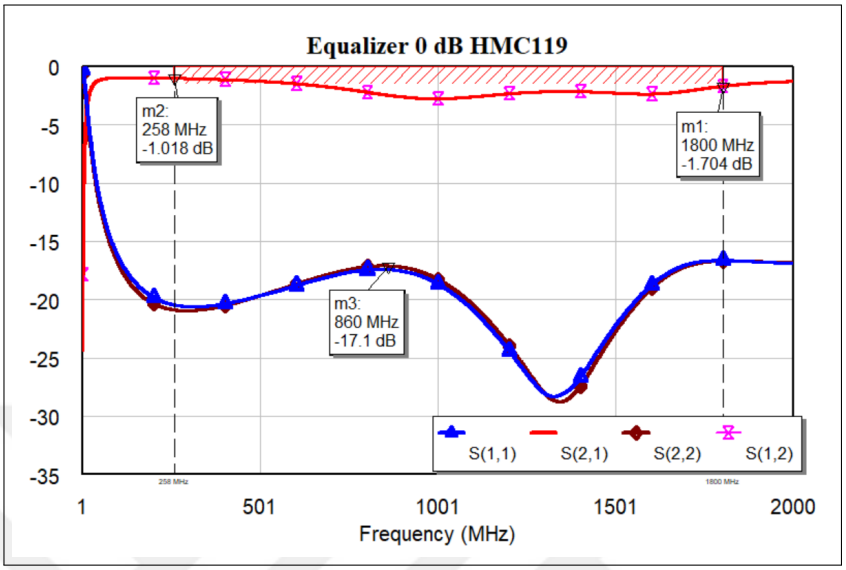

Figure 5.34. Simulation of the 0 dB equalizer with HMC1119

Resistance was added to the resonance circuits given in Figure 5.33, and the simulation result of the equalizer structure of the HMC1119 integrated circuit with 0 dB transition is given in Figure 5.34. Accordingly, the beginning of the band has -1.10 dB at 258 MHz and the end of the band has -1.70 dB S_{21} result at 1.8 GHz.

When examining the input and output reflections, there is approximately a -17.1 dB level of reflection around the 1600 MHz frequency.

For the 15 dB equalizer circuit structure, the circuit was simulated with the 20 dB crossover parameter of the equalizer structure while the environmental elements of the 0 dB crossover circuit given in Figure 5.33 remained the same as shown in Figure 5.35.

The simulation result of the 15 dB equalizer structure, whose schematic circuit is given in Figure 5.35, is given in Figure 5.36. Looking at the results, the beginning of the band has an S_{21} value of -12.16 dB level at 258 MHz and the end of the band has a value of S_{21} of -2.90 dB level at 1.8 GHz.

When the input and output reflections are examined, the worst reflection along the band is at the -12.65 dB level at 1582 MHz.

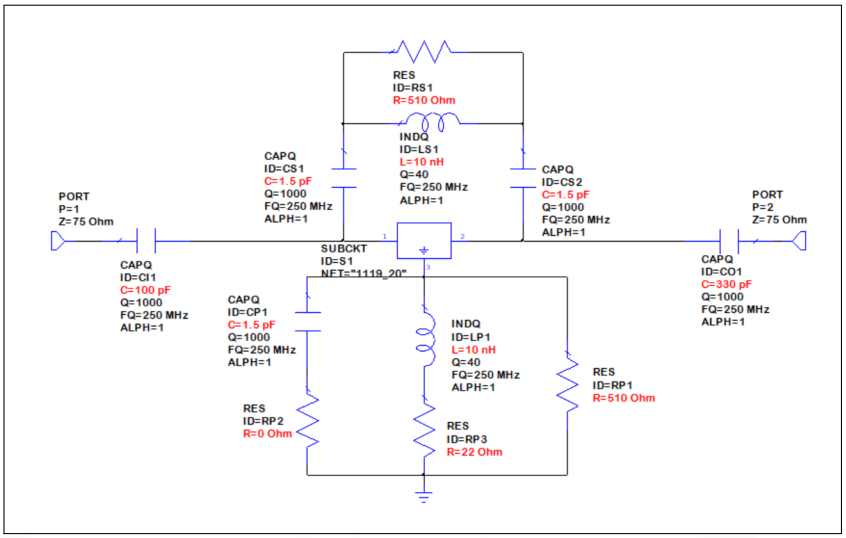

Figure 5.35. The 15 dB equalizer with HMC1119

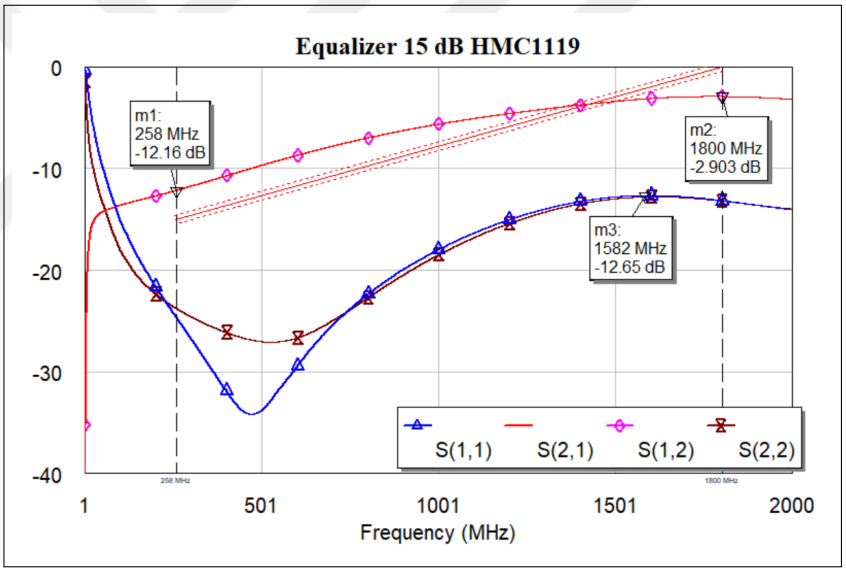

Figure 5.36. Simulation of the 15 dB equalizer with HMC1119

5.3.2.4. Inverse Equalizer Design and Simulation

The inverse equalizer structure to be used in the final structure is generally the same as the inverse equalizer structure used in the first structure. However, it was designed by selecting industrially available SMD elements, so there are very slight differences.

In the equalizer structure given in Figure 5.37, the structure was simulated with the parameters of the HMC1119 integrated circuit with 0 dB transition.

The simulation result of the 0 dB equalizer structure given in Figure 5.37 is given in

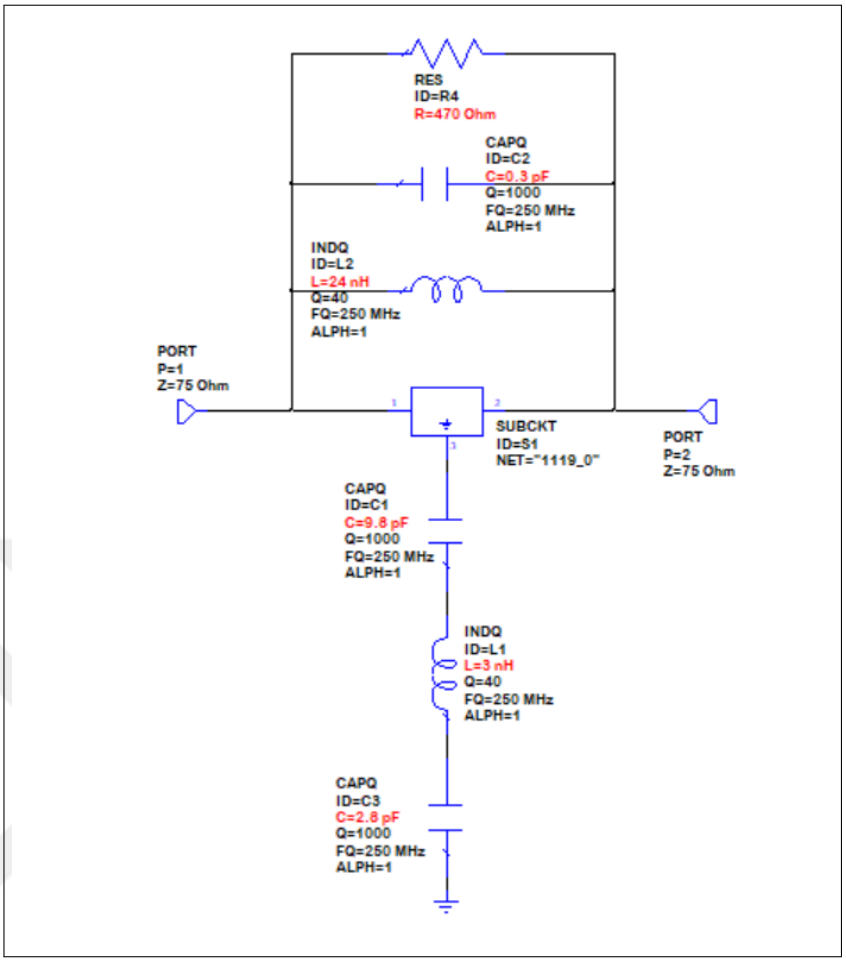

Figure 5.37. The 0 dB inverse equalizer with HMC1119

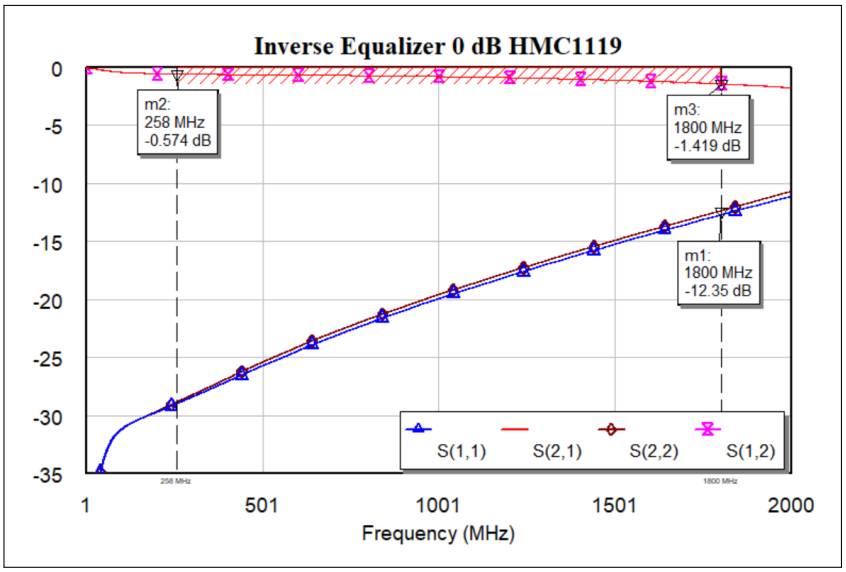

Figure 5.38. Simulation of the 0 dB inverse equalizer with HMC1119

Figure 5.38. When these results are examined, there is an S_{21} value at -0.57 dB at the beginning of the band at 258 MHz and -1.42 dB at the end of the band at 1.8 GHz.

When the input and output reflections are compared, the value with the highest reflection is at 258 MHz per band and at the -12.35 level.

The equalizer and inverse equalizer structures, whose separate designs were explained in the sections above, were simulated together and the results were examined. In this section, structures, where the equalizer and inverse equalizer structures both pass straight to 0 dB, structures where the equalizer structure passes 0 dB while the inverse equalizer passes 20 dB, and structures where the inverse equalizer structure passes 0 dB while the equalizer structure is 20 dB, are examined.

5.3.2.5. The Equalizer 0 dB - The Inverse Equalizer 0 dB

Designed with 75 Ω input and output impedance, the system includes 0 dB transitions of equalizer and inverse equalizer structures. The schematic structure of this system is shown in Figure 5.39. The schematic diagram of the equalizer and inverse equalizer structures used in the system is given in detail in Figure 5.40 and Figure 5.41.

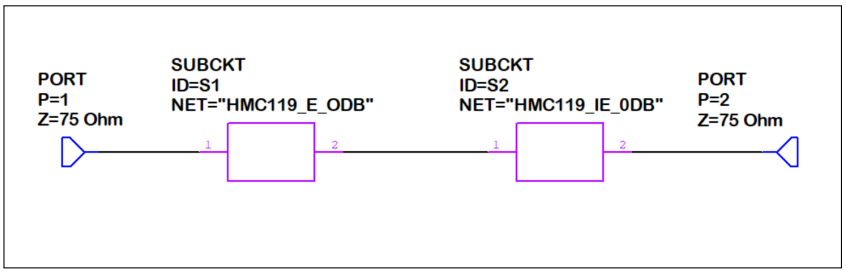

Figure 5.39. The equalizer 0 dB-the inverse equalizer 0 dB system schematic diagram

The schematic diagram of the equalizer structure of the system given in Figure 5.39 is shown in Figure 5.40. The structure, which has 75 Ω input and output impedance like the system, was added to the design using the *S*-Parameters of the HMC1119 integrated circuit with 0 dB transition.

The schematic diagram of the inverse equalizer structure of the system given in Figure 5.39 is shown in Figure 5.41. This structure, which has 75 Ω input and output impedance as in the system and equalizer structure, was added to the design using the *S*-Parameters of the

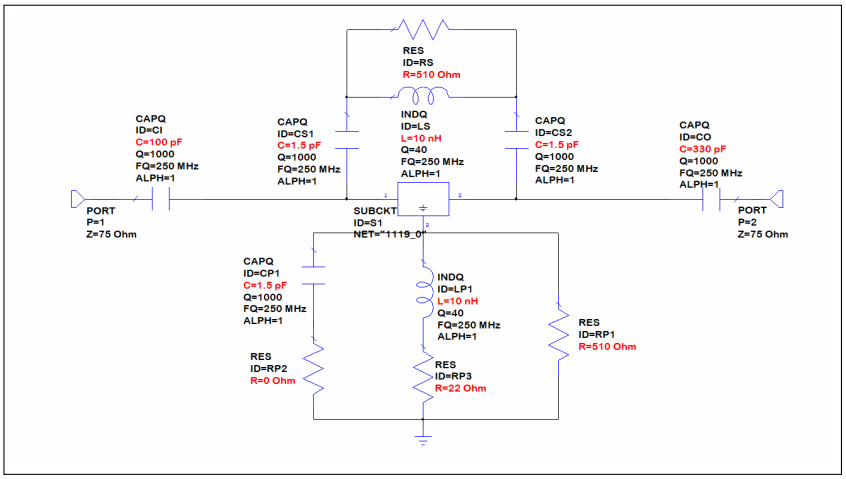

Figure 5.40. The equalizer 0 dB-the inverse equalizer 0 dB system - the equalizer schematic diagram

HMC1119 integrated circuit with 0 dB transition, as in the equalizer structure.

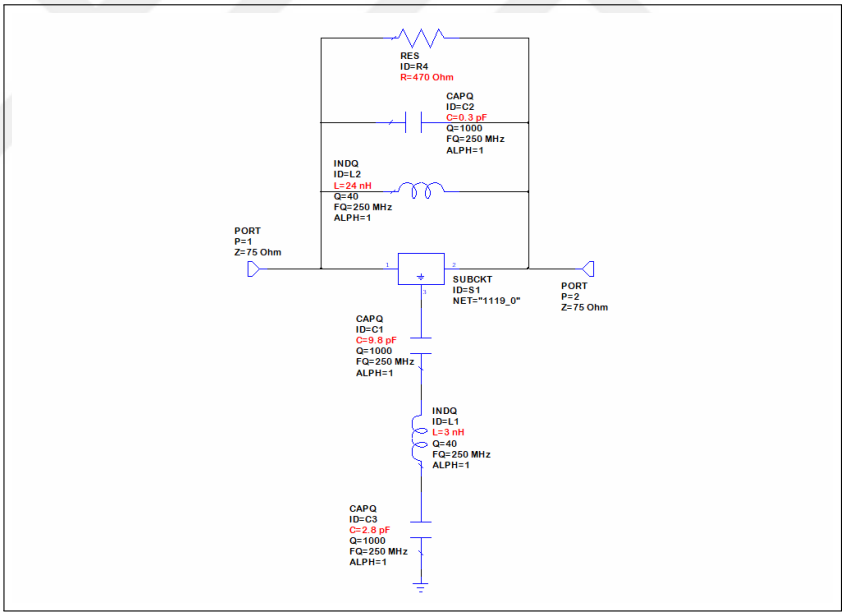

Figure 5.41. The equalizer 0 dB- the inverse equalizer 0 dB system - the inverse equalizer schematic diagram

The simulation result of the system given in Figure 5.39 is given in Figure 5.42. Looking at the results, it has an S_{21} value of -1.83 dB at the beginning of the band at 258 MHz and -3.82 dB at the end of the band at 1.8 GHz.

When looking at the input and output reflections of the simulation result of the system, the worst value is -10.58 dB at approximately 1617 MHz, as seen in the graph.

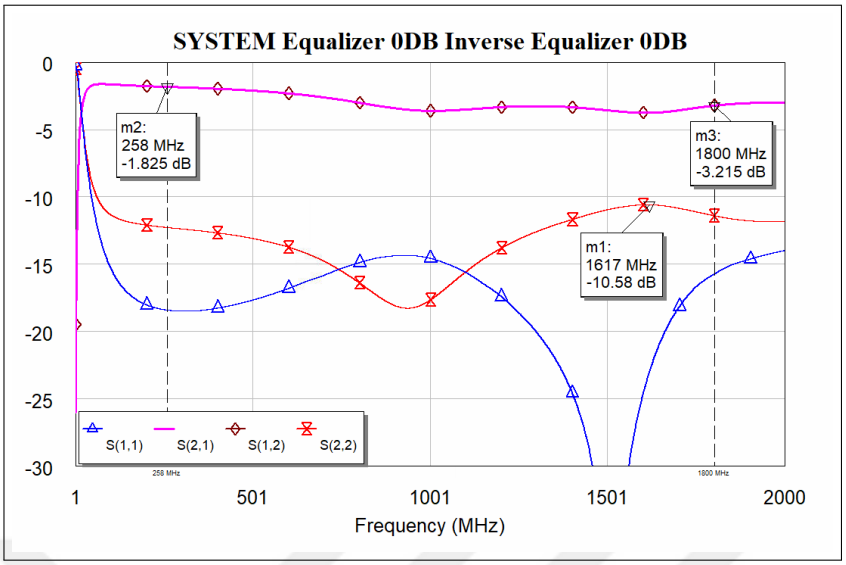

Figure 5.42. Simulation result of the equalizer 0 dB-the inverse equalizer 0 dB system

5.3.2.6. The Equalizer 20 dB - The Inverse Equalizer 0 dB

Designed with 75 Ω input and output impedance, the system includes 20 dB of equalizer and 0 dB of inverse equalizer structures. The schematic structure of this system is shown in Figure 5.43. The schematic diagram of the equalizer and inverse equalizer structures used in the system is given in detail in Figure 5.44 and Figure 5.45.

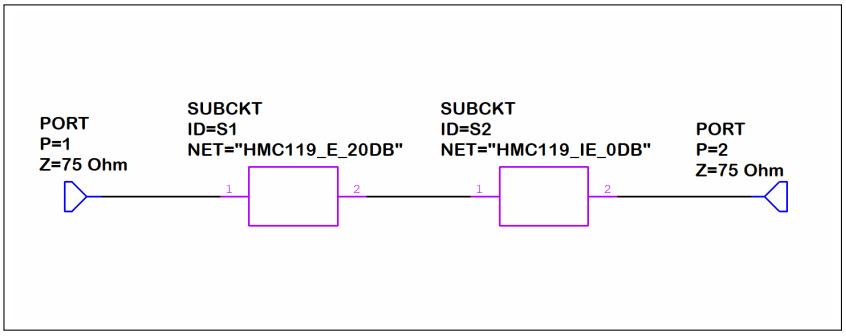

Figure 5.43. The equalizer 20 dB-the inverse equalizer 0 dB system schematic diagram

The schematic diagram of the equalizer structure of the system given in Figure 5.43 is shown in Figure 5.44. The structure, which has 75 Ω input and output impedance like the system, was added to the design using the *S*-Parameters of the HMC1119 integrated circuit with a 20 dB transition.

The schematic diagram of the inverse equalizer structure of the system given in Figure 5.43

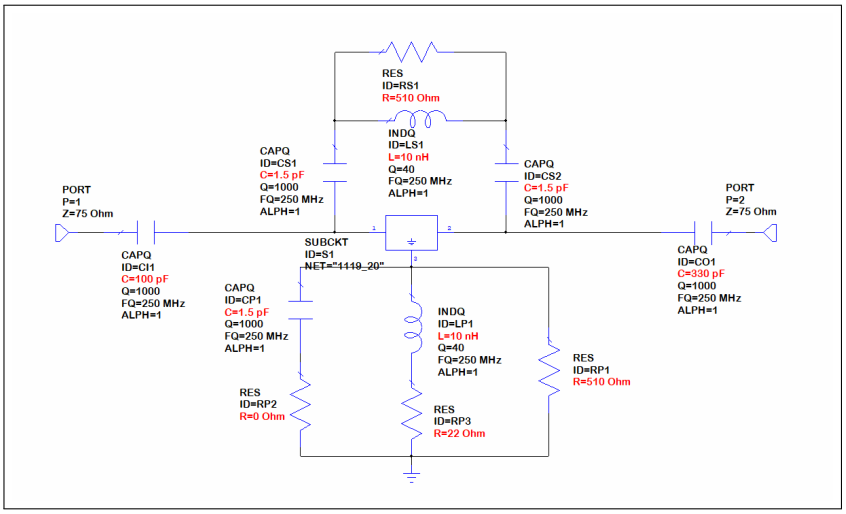

Figure 5.44. The equalizer 20 dB-the inverse equalizer 0 dB system - the equalizer schematic diagram

is shown in Figure 5.45. This structure, which has 75 Ω input and output impedance as in the system and equalizer structure, was added to the design using the *S*-Parameters of the HMC1119 integrated circuit with 0 dB transition, as in the equalizer structure.

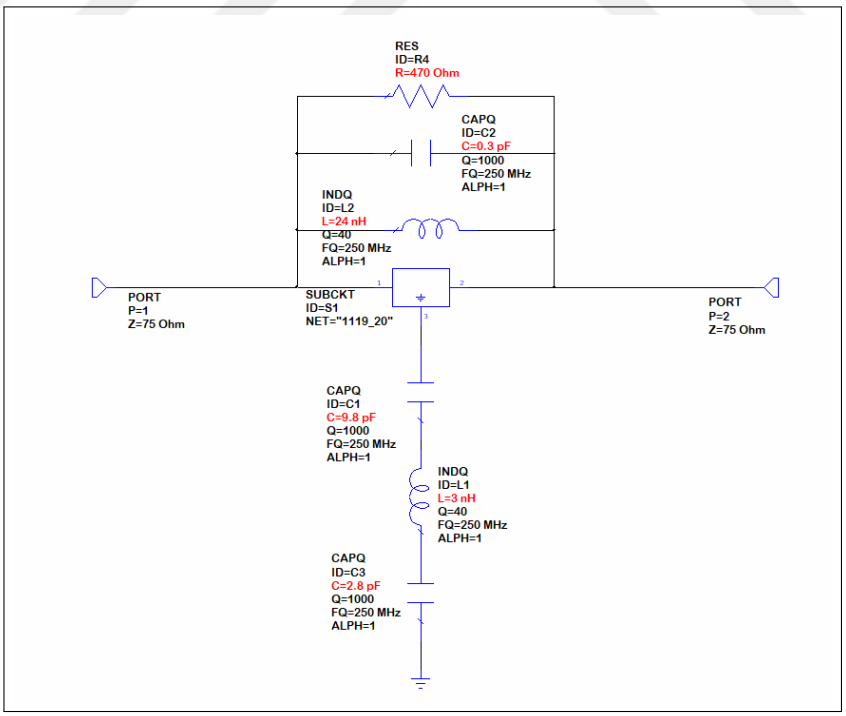

Figure 5.45. The equalizer 20 dB-the inverse equalizer 0 dB system - the inverse equalizer schematic diagram

The simulation result of the system given in Figure 5.43 is given in Figure 5.46. Looking at

the results, it has an S_{21} value of -12.75 dB at the beginning of the band at 258 MHz and -4.63 dB at the end of the band at 1.8 GHz.

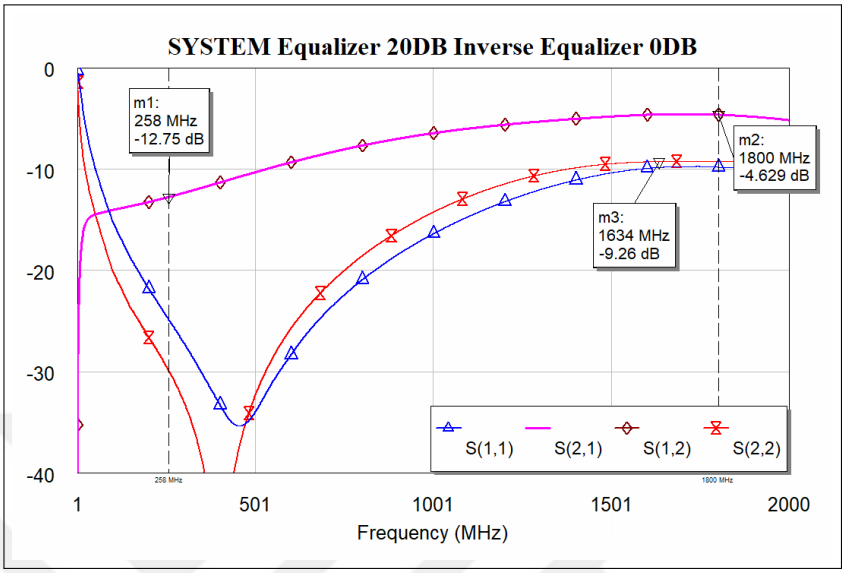

Figure 5.46. Simulation result of the equalizer 20 dB-the inverse equalizer 0 dB system

When examining the input and output reflections of the simulation result of the system, the worst value is -9.26 dB at approximately 1634 MHz, as seen in the graph.

5.3.2.7. The Equalizer 0 dB - The Inverse Equalizer 20 dB

Designed with 75 Ω input and output impedance, the system includes 0 dB of equalizer and 20 dB of inverse equalizer structures. The schematic structure of this system is shown in Figure 5.47. The schematic diagram of the equalizer and inverse equalizer structures used in the system is given in detail in Figure 5.48 and Figure 5.49.

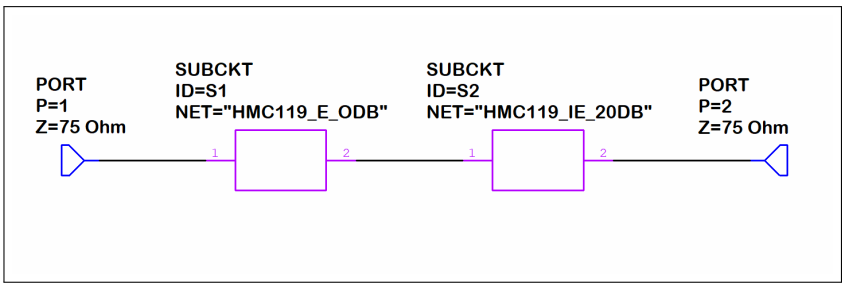

Figure 5.47. The equalizer 0 dB-the inverse equalizer 20 dB system schematic diagram

The schematic diagram of the equalizer structure of the system given in Figure 5.47 is shown in Figure 5.48. The structure, which has 75 Ω input and output impedance like the system,

was added to the design using the *S*-Parameters of the HMC1119 integrated circuit with 0 dB transition.

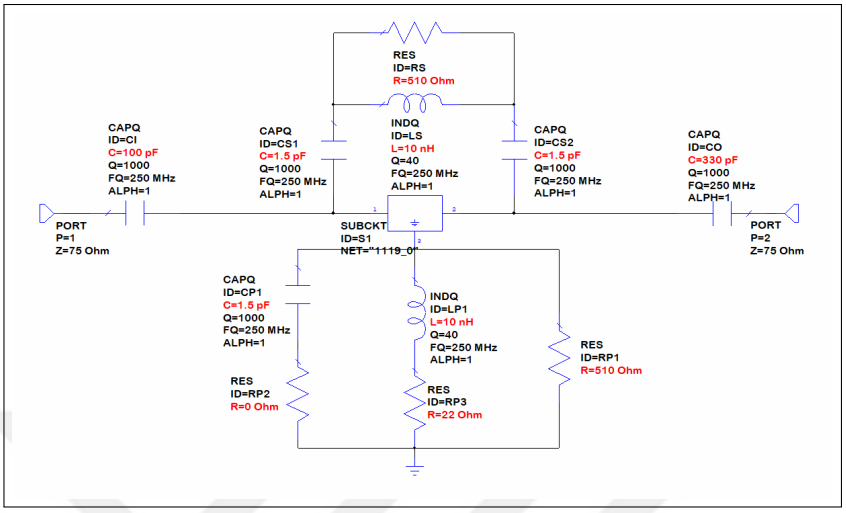

Figure 5.48. The equalizer 0 dB-the inverse equalizer 20 dB system - the equalizer schematic diagram

The schematic diagram of the inverse equalizer structure of the system given in Figure 5.47 is shown in Figure 5.49. This structure, which has 75 Ω input and output impedance as in the system and equalizer structure, was added to the design using the *S*-Parameters of the HMC1119 integrated circuit with a 20 dB transition.

The simulation result of the system given in Figure 5.47 is given in Figure 5.50. Looking at the results, it has an S_{21} value of -2.08 dB at the beginning of the band at 258 MHz and -18.04 dB at the end of the band at 1.8 GHz.

When examining the input and output reflections of the simulation result of the system, the worst value is -12.62 dB at approximately 777.1 MHz, as seen in the Figure 5.50.

5.3.2.8. Measurement Results

Measurements of the inverse equalizer blog have shown Figure 5.51 that when no bias is applied, the circuit exhibits more loss than expected across the entire band, but has a relatively flat gain flatness. The coercion seen at the end of the band is due to resonance circles.

When the slope was applied, a linear slope was observed in Figure 5.52 and this meets the

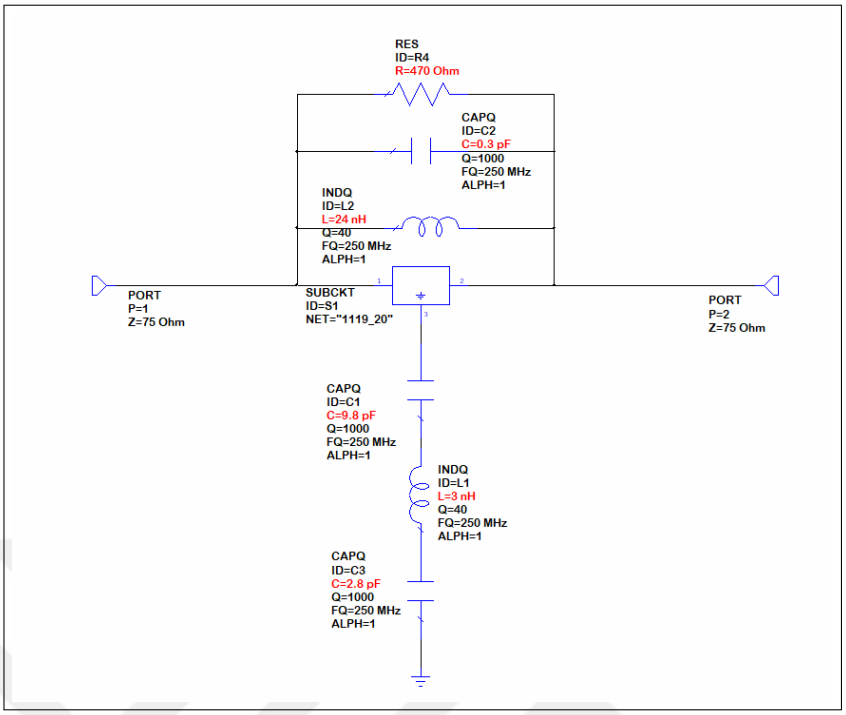

Figure 5.49. The equalizer 0 dB-the inverse equalizer 20 dB system - the inverse equalizer schematic diagram

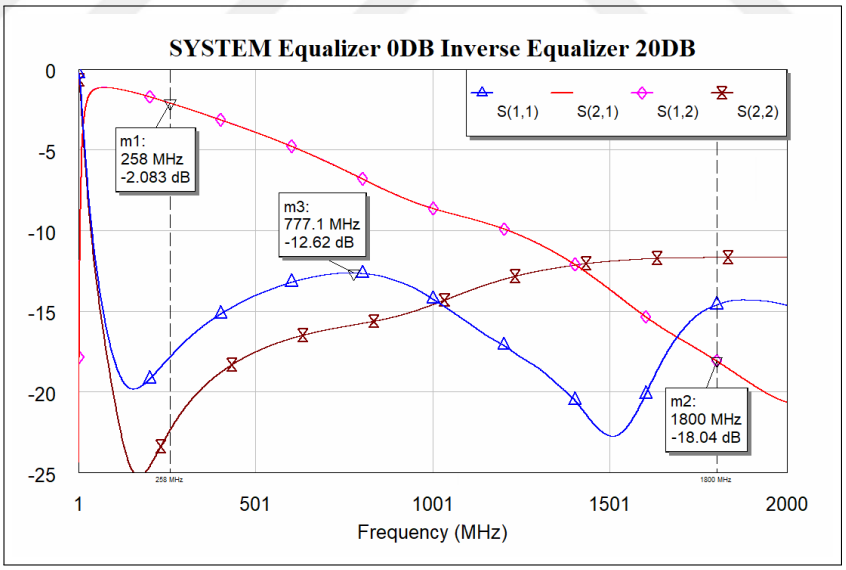

Figure 5.50. Simulation result of the equalizer 0 dB-the inverse equalizer 20 dB system

targeted specifications. Band head loss and lack of gain slope adjustment range are discussed in the discussion section.

In the measurement of the equalizer block after the slope was given in Figure 5.53, the desired level of the gain slope was not observed. linearity is less than expected. The reason for this

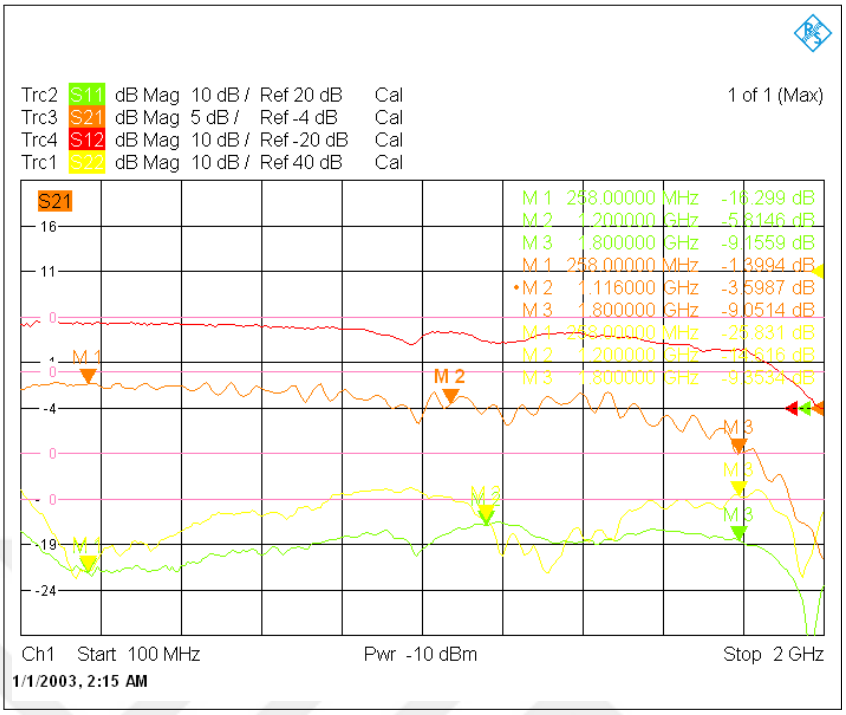

Figure 5.51. Measurement result of the manufactured device

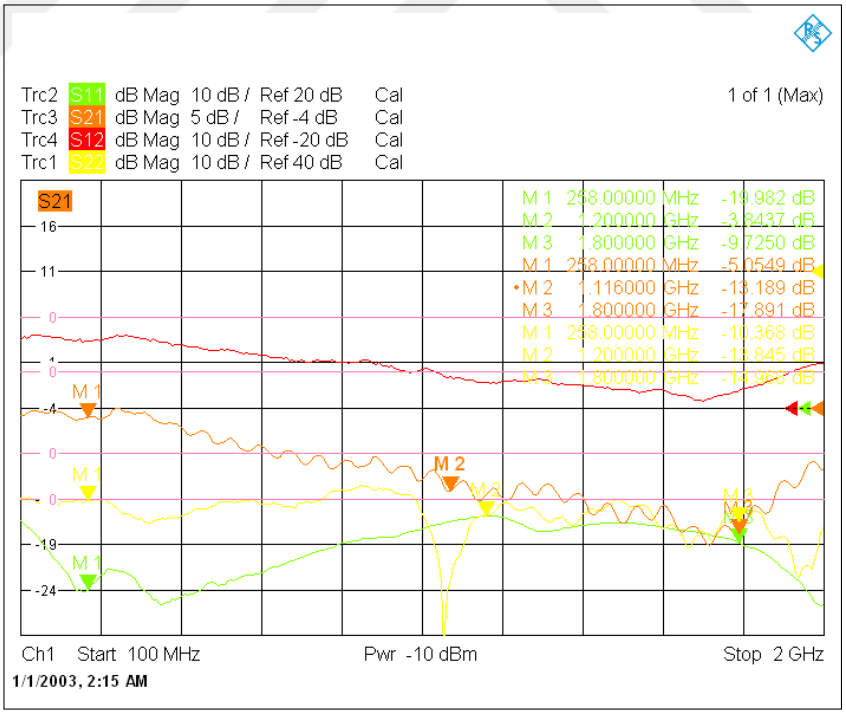

Figure 5.52. Measurement result of the manufactured device

is related to the ratios between LC pairs in resonance circuits. Although the first resonance circuit included in the final design showed a more linear slope, it was formed in the middle of the resonance band. This caused the signal to appear abnormally high up to 1.8 GHz after

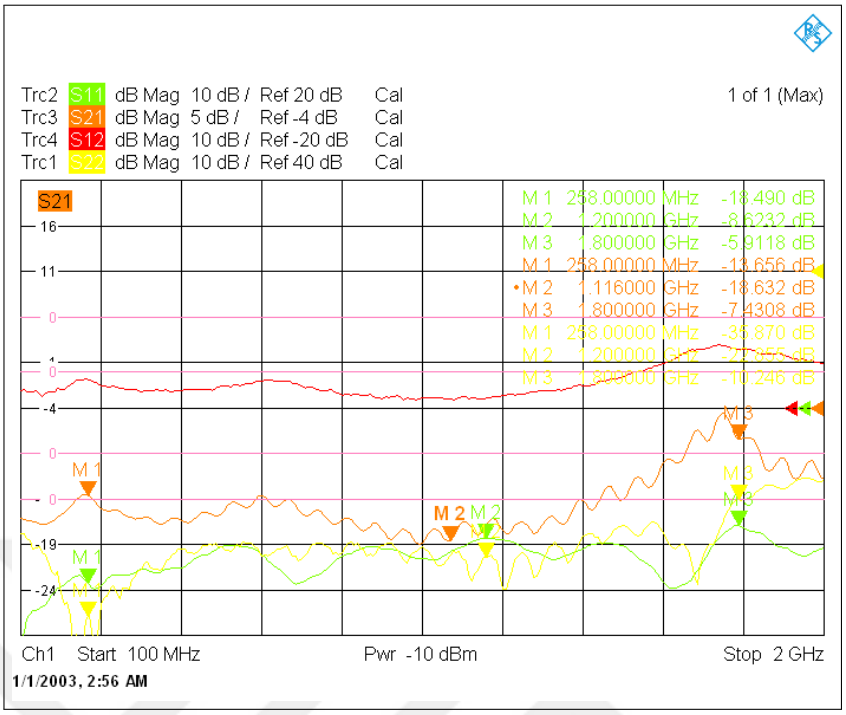

Figure 5.53. Measurement result of the manufactured device

the middle of the band.

Since PCB parasitic values could not be calculated and their effect was seen in the measurements, optimization was made in the resonance circuits after the first measurements. For this reason, the CS1 and CS2 values seen in Figures 5.36 and 5.38 were updated to 0.5 pF, while the LP1 value was updated to 3.3 nH. Thus, the resonance behavior, which was seen to be more effective in the middle of the band in the first measurements, was moved to the end of the band and the gain slope was made smoother. A similar resonance circle optimization was also done for the inverse equalizer and the L2 value was updated to 15 nH, C1 and C3 values to 2.2 pF, and the L1 value to 2.7 nH which can seen in Figure 5.39. It was understood that in order to determine these values in the simulation, a 3D electromagnetic measurement was required, which would include the electromagnetic model and physical structure of the chip used and the drawn layout. Nevertheless, the intended slope behavior was achieved.

Measurements have shown that the behavior of the proposed circuits is the correct concept for gain slope generation, but the performance values are open to improvement and discussion.

5.4. DISCUSSION

As a result of the simulations and measurements, it is observed that gain slope adjustment, which is the main purpose of both equalizer and inverse equalizer circuits, could be achieved.

The equalizer circuit was able to operate in the 258 MHz-1.8 GHz band range that comes with the DOCSIS 4.0 standard. During this study, it was observed that the gain at the end of the band should have remained constant, but it operated with a loss. Again, the notch phenomenon seen in the first design was seen to be reduced in the final design. However, a lower slope adjustment range was obtained compared to the structure used in the fixed attenuator and first design. Again, it was observed that the gain slope flatness value worsened in the final design. The gain slope adjustment value, which was approximately 20 dB in the fixed attenuator structure and approximately 15 dB in the first design, remained in the range of 10-12 dB. Thus, while the final design showed a non-notch performance in the middle of the band, it caused a decrease in the gain slope adjustment value. The targeted benefit of distorting the Q value in resonance circuits was achieved.

The inverse equalizer circuit worked as expected in both the fixed attenuator circuit and the first design circuit. For this reason, the final design was not changed much. On the other hand, due to the integrated change, the layout change also caused a change in DSA parasitics. This change, especially due to layout parasitics and physical parasitics, caused the resonance frequency values in the simulation to appear much more in the middle of the band. For this reason, the values of the L-C resonance elements were changed during the resonance frequency adjustment. Even though the parallel resistor in the parallel resonance circuit was disabled, which caused the gain slope flatness value to be better, its effect on the measurements was seen to be low. Again, while the gain level of the band head was expected to remain constant or decrease by 1-2 dB, the decrease in the gain level per band was seen much more. For this reason, the layout and DSA's own parasitics came to the fore in such a design.

It was observed in the measurement results that the saw filter structure, which was designed differently from the first design in the final design, was necessary and efficient. In CATV systems operating under multiple channels, software balancing can work much more precisely

if the pivot signals can be transmitted to the detectors with good isolation. However, in the measurements made during the final design phase, the insulation was not found sufficient and the second pivot signs could leak into each other's channels. It was evaluated that there was a problem caused by layout and grounding. However, the system worked when the power levels were significantly different. In more sensitive differences, isolation and RF detector sensitivity came to the fore.

High-frequency line and material losses have been one of the weakest points of the design. In the simulations made with only DSA frequency response and ideal materials or Q values close to practice, 1.8 GHz losses were found to be approximately 3-4 dB, while in the realized final design circuit, these losses were over 10 dB. This value can be improved by better grounding via structure, by switching the coplanar waveguide transmission line structure to a more lossless trace with ground gap structure, and by screwing and grounding the entire circuit on a metal base and by screwing frequently. Nevertheless, these high loss values seen at 1.8 GHz will be an important improvement issue for both industrial applications and potential future studies. Here, the naturally occurring gain slope in SGSMS has also created an obstacle in actually detecting and correcting the slope of the actual circuit.

The lack of a gain block of the circuit and the tilt caused by the frequency response of the SGSMS, which occurs especially due to high-frequency line and material losses, as well as the need to correct the gain slope value expected to come from the upgraded circuit, have caused gain equalization to be constantly achieved with loss of gain to the circuit. This situation causes loss of gain, increase in noise figure, power loss, and heating. Although this situation is taken into account in CATV systems, it has also been observed that an earnings blog can be beneficial in terms of gain slope adjustment. This issue has been left for future studies.

The advantages and disadvantages of using DSA structures, which are normally used to change the gain level, as equalizers and inverse equalizers, have been seen in the simulation and measurement results. The main advantages are that DSA structures, which have a cost advantage, can be controlled via SPI and offer ease of supply, allowing gain slope adjustment in 1 dB steps. The main disadvantage is that even though the frequency responses of these structures can be simulated with the help of s2p files, the package structures' pinout

structures, which vary from product to product, require different layouts for each product, which causes uncalculated parasitics to occur. In this case, the main thing to do is to simulate the integrated circuits with their layouts using 3D electromagnetic simulation techniques. Such a study would bring the simulation closer to measurable real results. However, this application provides the opportunity to realize a wide-band design covering the targeted DOCSIS 4.0 frequency band in the desired frequency band, even with general-purpose RF DSA products. The biggest advantage here is that it enables the implementation of inverse equalizer circuits that can operate in the DOCSIS 4.0 band, which cannot be seen in the literature research. For this reason, it can be said that the development of this concept is also obvious.

6. CONCLUSIONS

In the study, inverse equalizer values were obtained both for resistive passive elements and for the design made with active DSA. In the on-circuit analysis, it was seen that the inverse equalizer circuit works for both 0 dB transition and 15 dB end-of-band value. Contrary to the simulation, the default circuit loss at 0 dB transition state is approximately 3 dB higher than expected values. At the 15 dB value, it was observed that the reflectance values deteriorated up to 6 dB instead of the targeted 10 dB value. Return loss values are optimized in the main work and it is kept under 10 dB target value.

Once it was realized that the problem was due to DSA's parasitic capacitance towards the ground, a different path was taken because the resonance frequencies had to be within the band. To break the effect of notches within the band, resistors were added specifically to reduce the Q value of the resonances of the equalizer circuits. thus the effect of the impedance of the resonance was reduced. Thus, only gain ripples were seen, although the resonance was still within the band. The DSA change also helped this. The fact that the HMC1119 can run at 1.8 GHz up to 6 GHz helped us see less interference. In this way, acceptable gain flatness was achieved. The disadvantage of this was that the loss at the end of the band was greater than expected and the slope adjustment range was reduced.

Some of the losses come from the ground insufficiency of the designed circuit, some losses come from DSA losses, and some from an impedance mismatch.

It is designed with low-cost 75 Ω and 50 Ω DSA's as targeted as unit cost. For high-volume productions, the total cost will be less than 10 USD. designing the unit on the FR-4 card and using DSA turned into a cost advantage compared to the alternatives.

Active equalizer and inverse equalizer circuits compatible with DOCSIS 4.0, which have not yet been industrially produced, have also been introduced to the literature at very affordable costs.

In future studies, especially designs with lower insertion loss values in both straight transition and slope modes can be focused on. By making the existing design smaller and more compact, it can be added to the designs as a module in DOCSIS 4.0 devices with connector connection

or PCB on-board mounting possibility and can be used either in automatic slope correction mode or by remote slope value assignment.

By adding attenuator and amplifier structures in addition to the proposed unit, a system that not only corrects the gain curve but also maintains the gain level can be obtained.

The study has shown that the equalizer and inverse equalizer circuits made using DSA cannot be made by removing the attenuator block from the equalizer and inverse equalizer circuits made with a T-type attenuator and replacing it with DSA. The unknown integrated circuit inside the DSA units, other unknown circuit parts going to the ground pins of these units, and the parasitic capacitance and inductance of these circuits do not allow this. For this reason, resonance circuits need to be updated. However, acceptable slope flatness and gain flatness values were obtained by changing the Q values of the resonances within the band. Thus, it has been shown that active inverse equalizer and active equalizer circuits can be designed with readily available, low-cost DSA units with 50 Ω or 75 Ω impedance, which are commercial products. This finding is important for operators and designers who want to switch to DOCSIS 4.0 technology. The frequency band of DOCSIS 4.0 can be met with DSA products that have been on the market for a long time. So far, there are only voltage-controlled products on the market as active equalizers and there is no active inverse equalizer. The design offers a significant advantage in this field with DSAs that allow 1 dB adjustment steps.

If the capacities in the resonance pairs of the inverse equalizer are adjustable or selectable, the system can be made operational for other frequency bands in DOCSIS 4.0 standards.

The fact that MCU was used in the study and a software algorithm was run will enable the design of fully remote-controlled CATV amplifier units, which is one of the targets of DOCSIS 4.0. If external access to the MCU is provided, the user will be able to remotely assign the desired slope value or provide a flat curve as in the study. This makes the current study unique compared to designs found and compared in previous literature research.

With the DOCSIS 4.0 technology, the concept of determining 2 pivot frequencies and determining the gain and slope by reading the power values at these frequencies, which was previously discussed by SCTE, was directly applied in the design, so there is no need to design a detection loop for users using this module.

The weak point of the design is undoubtedly the deterioration of gain flatness and slope flatness values due to the resonances that occur inside the band. These values can be improved in future studies by further studying LC tank circuit structures. The fact that the gain per band does not decrease as much as desired due to the equalizers caused by the resistances added to the optimized resonance circuits, thus remaining at 10-12 dB values while aiming for a slope of 15 dB, is also a subject of future study.

Adding a gain stage to this type of module, thus performing slope management without causing a decrease in the total system gain, is a future study goal as well as an industrial requirement.

Designing and presenting this entire system as an integrated circuit is also valuable for IC manufacturing companies. Especially considering the CATV industry's annual unit production in the millions and considering that this is a necessity due to the DOCSIS 4.0 remote-controlled unit target, it is clear that it is stimulating work for the industry.

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APPENDIX A: SOFTWARE TO CONTROL THE SYSTEM

The software that controls the system is given in Algorithm A.1 and Algorithm A.2.

Algorithm A.1. C Code - 2

```
void TMR0_IRQHandler(void)
{                        ADC_START_CONV(ADC);
                while(!ADC_GET_INT_FLAG(ADC, ADC_ADF_INT));
                ADC_CLR_INT_FLAG(ADC, ADC_ADF_INT);
                rf_detector_1 = ADC_GET_CONVERSION_DATA(ADC, 4);
                rf_detector_2 = ADC_GET_CONVERSION_DATA(ADC, 3);
        if((rf_detector_2 - rf_detector_1)> (300)){
                att_value_1=att_value_1+4;att_value_2=att_value_2-4;
                if(att_value_1>120){att_value_1=120;}
                if(att_value_2>120){att_value_2 = 120;}
                if(att_value_1 < 0){att_value_1 = 0;}
                if(att_value_2 < 0){att_value_2 = 0;}
                spi_transmit_data_1[0] = att_value_1;
                spi_transmit_data_2[0] = att_value_2;
                                PA1 = 0;
                SPI_WRITE_TX(SPI0, spi_transmit_data_1[0]);
                while(SPI_IS_BUSY(SPI0));PA1 = 1;
                SPI_SET_SS_LOW(SPI0);
                SPI_WRITE_TX(SPI0, spi_transmit_data_2[0]);
                while(SPI_IS_BUSY(SPI0));
                SPI_SET_SS_HIGH(SPI0);}
        if((rf_detector_2 < 2850)){
                att_value_1 =att_value_1 - 4;
                if(att_value_1 > 120){att_value_1=120;}
                if(att_value_2 > 120){att_value_2 = 120;}
                if(att_value_1 < 0){att_value_1 = 0;}
                if(att_value_2 < 0){att_value_2 = 0;}
                spi_transmit_data_1[0] = att_value_1;PA1 = 0;
                SPI_WRITE_TX(SPI0, spi_transmit_data_1[0]);
                while(SPI_IS_BUSY(SPI0));PA1 = 1;}
        if((rf_detector_1 - rf_detector_2)> (300)){
                att_value_1 =att_value_1 - 4;
                att_value_2 =att_value_2 + 4;
                if(att_value_1 > 120){att_value_1=120;}
                if(att_value_2 > 120){att_value_2 = 120;}
                if(att_value_1 < 0){att_value_1 = 0;             }
                if(att_value_2 < 0){att_value_2 = 0;}
                spi_transmit_data_1[0] = att_value_1;
                spi_transmit_data_2[0] = att_value_2;PA1 = 0;
                SPI_WRITE_TX(SPI0, spi_transmit_data_1[0]);
```

Algorithm A.2. C Code

```
while(SPI_IS_BUSY(SPI0)); PA1 = 1;
                SPI_SET_SS_LOW(SPI0);
                SPI_WRITE_TX(SPI0, spi_transmit_data_2[0]);
                while(SPI_IS_BUSY(SPI0));
                SPI_SET_SS_HIGH(SPI0);}
        if((rf_detector_1 < 2850)){
                att_value_2 =att_value_2-4;if(att_value_1>120){
            att_value_1 = 120;}
                if(att_value_2 > 120){
                        att_value_2 = 120;}
                if(att_value_1 < 0){att_value_1 = 0;}
                if(att_value_2 < 0){att_value_2 = 0;}
                spi_transmit_data_1[0] = att_value_1;
                spi_transmit_data_2[0] = att_value_2;
                SPI_SET_SS_LOW(SPI0);
                SPI_WRITE_TX(SPI0, spi_transmit_data_2[0]);
                while(SPI_IS_BUSY(SPI0));SPI_SET_SS_HIGH(SPI0);}
                /* clear timer interrupt flag */
                TIMER_ClearIntFlag(TIMER0);}
void ADC_IRQHandler(void)
{    g_u32AdcIntFlag = 1;
    ADC_CLR_INT_FLAG(ADC, ADC_ADF_INT);
int32_t main(void)
{ SYS_Init();
   SPI0_Init(); GPIO_SetMode(PA, BIT1 , GPIO_MODE_OUTPUT);
   GPIO_SetMode(PA, BIT3 , GPIO_MODE_OUTPUT);PA1 = 1;
   PA3 = 1;ADC_POWER_ON(ADC);
   ADC_Open(ADC, ADC_ADCR_DIFFEN_SINGLE_END,
ADC_ADCR_ADMD_CONTINUOUS,BIT3|BIT4);
   ADC_CLR_INT_FLAG(ADC, ADC_ADF_INT);
   IMER_Open(TIMER0, TIMER_PERIODIC_MODE, 100);
   TIMER_EnableInt(TIMER0);NVIC_EnableIRQ(TMR0_IRQn);
   TIMER_Start(TIMER0);
    while(1){}}
```