DESIGN AND DEVELOPMENT OF GaN AMPLIFIERS FOR TRANSCEIVER APPLICATIONS

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By
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We certify that we have read this dissertation and that in our opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

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Dedication

To our venerated Prophet Muhammad (PBUH), whose timeless guidance continues to enlighten humanity,

and

to the devoted members of my beloved family—my parents, wife, brothers, sister, and children.

ABSTRACT

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A transceiver, commonly known as a T/R module, is widely used in phased array radar systems for military, space, and commercial applications. Hybrid microwave integrated circuits and low-temperature co-fired ceramic technologies offer bulky solutions. However, advancements in GaN HEMT-based monolithic microwave integrated circuit (MMIC) technology have led to low-cost, compact, and efficient alternatives over the years.

A microwave transceiver consists of a low noise amplifier (LNA), a high power amplifier (HPA), and a single-pole double-throw switch. The current thesis aims on indigenous design and development of LNA and HPA for an MMIC transceiver at X-band using NANOTAM's in-house 0.15/0.25 µm AlGaN/GaN fabrication process. Robustness, including survivability and reverse recovery time (RRT), and limiting output power are the primary focus of LNAs besides gain and noise figure (NF). The single-stage design based on cascode HEMT and three-stage designs based on source degenerated HEMTs are discussed in the frequency range of 8 to 12 GHz. It is shown that cascode HEMTs-based LNA have high survivability but at the cost of increased NF. In a three-stage design, RRT is studied as a function of the pulse width of the incoming signal. This LNA has the best combination of NF and survivability, surviving 42 dBm input power with sub-1.5 dB NF and having 23.2 dB gain with ±1 dB gain ripple. The output saturated power of the LNA is limited to 20 dBm using a novel un-gated HEMTs approach for easy integration with subsequent circuitry.

Moreover, the design of a three-stage high power amplifier operating in the 8.5 to 11 GHz is discussed in detail. Two design approaches are described, and it is shown that reducing the power dissipation by reducing HEMT peripheries in the first and intermediate stages improves power added efficiency (PAE). The achieved PAE is higher than 43 % with more than 43 dBm output power in a compact size of 2.4 × 3.75 mm^2.

Keywords: noise, power added efficiency, reverse recovery time, survivability.

ÖZET

ALICI-VERİCİ UYGULAMALARI İÇİN GaN YÜKSELTECLERİNİN TASARIMI VE GELİŞTİRİLMESİ

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Genellikle T/R modül olarak bilinen gönderme/alma modulü, askeri, uzay ve ticari uygulamalarda kullanılan faz dizili radar sistemlerinde kritik bir rol oynar. Hibrit mikrodalga entegre devreler ve düşük sıcaklıkta birlikte pişirilen seramik teknolojileri hacimli çözümler sunmaktadır. Ancak, GaN HEMT tabanlı monolitik mikrodalga entegre devre (MMIC) teknolojisindeki gelişmeler, daha düşük maliyetli, kompakt ve yüksek verimli alternatiflerin geliştirilmesini mümkün kılmıştır.

Bir mikrodalga alıcı-verici, düşük gürültülü yükselteç (LNA), yüksek güçlü yükselteç (HPA) ve tek kutuplu çift yönlü anahtardan (SPDT) oluşur. Bu tez, NANOTAM'a ait 0.15/0.25 µm AlGaN/GaN üretim süreci kullanılarak X-band MMIC alıcı-vericisi için LNA ve HPA'nın yerli tasarım ve geliştirilmesini amaçlamaktadır. LNA'larda kazanç ve gürültü katsayısı (NF) dışında sağlamlık, özellikle dayanım kabiliyeti, ters toparlanma süresi (RRT) ve çıkış gücünü sınırlama başlıca odak noktalarıdır. 8-12 GHz frekans aralığında, kaskot HEMT tabanlı tek kademeli tasarım ile kaynak dejenerasyonlu HEMT'lere dayalı üç kademeli tasarımlar ele alınmıştır. Kaskot HEMT tabanlı LNA'ların yüksek dayanıklılığa sahip olduğu ancak bunun NF artışına neden olduğu gösterilmiştir. Üç kademeli tasarımda, gelen sinyalin darbe genişliğine bağlı olarak RRT incelenmiştir. Bu LNA, 42 dBm giriş gücüne dayanabilen, 1.5 dB'in altında NF ve ±1 dB kazanç dalgalanması ile 23.2 dB kazanç sağlayan, en iyi NF ve dayanım kabiliyeti kombinasyonunu sunmaktadır. LNA'nın çıkış doygunluk gücü, sonraki devrelerle kolay entegrasyon sağlamak amacıyla geliştirilen yeni bir kapısız (un-gated) HEMT yaklaşımı kullanılarak 20 dBm ile sınırlandırılmıştır.

Ayrıca, 8.5-11 GHz frekans aralığında çalışan üç kademeli bir yüksek güçlü yükseltecin tasarımı ayrıntılı olarak tartışılmaktadır. İki farklı tasarım yaklaşımı açıklanmaktadır. İlk ve ara kademelerdeki HEMT boyutunun azaltılması ile güç

tüketiminin düşürülmesi, güç eklentili verimliliği (PAE) artırmaktadır. 2.4 × 3.75 mm^2 gibi kompakt bir boyutta %43 üzerinde PAE ve 43 dBm çıkış gücü elde edilmiştir.

Anahtar sözcükler: gürültü, güç eklemeli verimlilik, ters toparlanma süresi, dayanım kabiliyeti.

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Chapter 1

Introduction

A transceiver, commonly known as a T/R module, is a critical component in phased array systems. The phased array systems include radars like active electronically scanned array (AESA), semi-active and passive phased array (PAR) for military (airborne, naval, and ground-based surveillance), space SAR, and commercial (air traffic control) applications. The phase arrays have also become significant for imaging, 5G/6G mobile network technology, and MIMO communication systems. Traditionally, transceivers have been realized using hybrid microwave integrated circuits (HMIC) and low-temperature co-fired ceramic (LTCC) technologies. The HMIC offers thermal management and flexible integration of components onto PCB and housing, but its drawback is its larger size and weight. On the other hand, LTCC provides comparatively low cost and reduced size solution due to vertical stacking of components [1–4], but it is bulky. Advancements in monolithic microwave integrated circuit (MMIC) technology, system-on-chip concept, and miniaturization of the systems have pushed the need for a single-chip integrated MMIC solution for microwave transceivers. This reduces the size further but creates stability, robustness, and thermal management challenges.

The transceiver module consists of both transmit and receive chains. The simplistic feasible architecture for an MMIC transceiver includes a high power

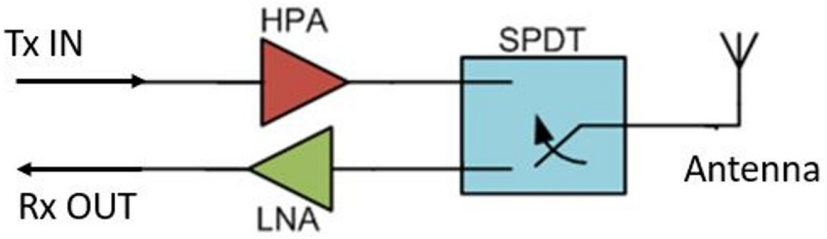


Figure 1.1: Transceiver Block Diagram.

amplifier (HPA), low noise amplifier (LNA), and single-pole double-throw (SPDT) switch, as shown in Fig. 1.1. The transistor technology is vital for the realization of these components. The research on wide band gap semiconductors over past decades has produced devices operating under high voltage, temperature, and frequency conditions. The devices include MESFET, HBTs, HEMT, and pHEMTs built on materials such as Gallium Arsenide (GaAs), Gallium Nitride (GaN), Indium Phosphide (InP), and Silicon Carbide (SiC) [5]. GaN HEMT outperforms other devices in output power, efficiency, breakdown voltage, and high frequency operation due to the formation of a two-dimensional electron gas (2DEG). The 2DEG is naturally formed at the heterojunction between Aluminium Gallium Nitride (AlGaN) and GaN due to piezo-electric and spontaneous polarizations [6]. The unequal band gap at the interface produces a quantum well containing free electrons with high mobility. As the free electrons are spatially separated from the donor items, impurity scattering is less within the 2DEG channel, which results in increased carrier mobility and enhanced drift and saturation velocities [7].

Table 1.1: Material properties of various semiconductors

Property	**Si**	**GaAs**	**SiC**	**GaN**	**InP**	**SiGe**	**Diamond**
E_g (eV)	1.12	1.42	2.9	3.4	1.35	0.84–1.12	5.45
E_c (10^6 V/cm)	0.3	0.4	2.5	3.3	0.5	0.3	5.6
μ_n (cm^2/Vs)	1300	5000	260	2000	5400	1350–4315	1900
v_{sat} (10^7 cm/s)	1.0	1.0	2.4	2.5	1.0	2.0	2.7

Table 1.1 compares GaN with other semiconductor materials [8]. The energy

band gap (E_g), electric field breakdown (E_c), electron mobility (μ_n), and saturation velocity (v_{sat}) of materials are compared. Diamond has excellent properties, but it is costly. GaN is the second-best material and is less costly than diamond. The Si is available in abundant naturally; however, its lower band gap restricts its use for high power applications.

There are various options for the substrate to be used as a carrier for GaN. Table 1.2 shows properties of common substrate materials for GaN HEMTs [9–17]. The bulk GaN cannot be used as carrier due to immaturity of growth process [5]. GaN on diamond has excellent thermal characteristics but higher lattice mismatch and cost. Sapphire, Si, and SiC are good choices. However, GaN on SiC is the best for power applications in electronics because of its good thermal conductivity and better lattice match than others. Otherwise, GaN on Sapphire is used for optical devices.

Table 1.2: Properties of common substrates for GaN-based devices

Substrate	**Lattice Mismatch with GaN (%)**	**Thermal Conductivity (W/m·K)**	**Electrical Conductivity (S/cm)**	**Cost per cm² (USD)**
Sapphire (Al_2O_3)	13.9	25–35	10^{-14}	0.6–2.5
Silicon (Si)	17	150	$1–10^{-3}$	0.03–0.06
SiC (4H/6H)	3.5	370–490	10^{-6}	0.6–1.7
Bulk GaN	0	130–230	10^{-7} to 10^{-5}	12–62
AlN	2.5	285	10^{-14}	6–12
Diamond	15.7	2000	$< 10^{-16}$	500–2000

GaN on SiC HEMT is the promising technology for MMIC development due to high speed, saturation drain current, output power density, and high frequency operation. The GaN technology initially focused on power amplifiers, and much work is reported on the design of broadband drivers and power amplifiers [18–20]. Later, a single-chip transceiver solution pushed the need to work on GaN LNAs and SPDT switches. GaN-based reflective/ absorptive type SPDT switches with high power handling and low insertion loss are reported in the literature [21–23]. Moreover, work on GaN HEMT LNAs operating in a wide range of frequencies has also been published [24–29].

1.1 Motivation and Challenges

MMIC LNAs and HPAs for on-chip microwave transceivers for phased array radars are the focus of the current thesis. The main objective of LNAs in pulsed radar is to provide a high signal-to-noise ratio (SNR) with minimum self-noise. The dynamic range of these systems is limited by the dynamic range of the analog-to-digital converter (ADC) [30]. The system's dynamic range can be extended using larger gain LNA devices at high frequencies right after the antenna. The larger gain involves multi-stage designs for the LNAs while keeping noise figures at an acceptable level to meet SNR requirements.

The recent advancements in GaN HEMT technology have produced LNAs with promising noise figures compared to GaAs technology [31]. The LNAs should be robust enough to operate under highly dense EM environments. They are subjected to high power levels due to the self-leakage of the transceivers, nearby target reflections, and jamming signals from the electronic warfare systems—the high breakdown nature of GaN results in robust LNA solutions.

The robustness of an LNA is defined by two figures of merits (FoMs): survivability and reverse recovery time (RRT). The survivability of an LNA is its ability to limit the forward gate turn-on current to avoid catastrophic failure. Forward gate turn-on current is one of the most prominent possible failure mechanisms in GaN LNAs [32]. In quantitative terms, survivability is the maximum input drive level an LNA can handle without significantly degrading its gain and noise figure.

The LNAs are compressed under the application of higher power signals, and their gain is reduced during the interval of this signal. The RRT of an LNA is defined as the time required for the device gain to return to 100 % of its initial value once the high input stress is released. However, system designers can relax this definition for an affordable drop in gain, for example, upto 0.3 dB as part of the link budget margin of the system, which will redefine the RRT as the time required to reach up to 93% of the initial gain value. The device gate bias is

also shifted due to the forward gate turn-on during the duration of this stress; therefore, RRT is also defined as the time required for the gate bias to return to its original value after the release of the high power pulse. The RRT depends upon two phenomena: RC time constant and trapping. The RC time constant comprises the input capacitance of the HEMT, source resistance, and gate bias resistance of the circuit (if any). The traps are activated and dominate the recovery times as the incoming signal level becomes high enough to forward-bias the metal-semiconductor gate Schottky contact [31].

GaN LNAs have high output power at 1-dB gain compression and high linearity. However, they have high saturated output power (P_{sat}) levels, which pose an integration challenge for system designers. Limiting LNA's P_{sat} is necessary for its safe integration with subsequent subsystems and modules, i.e., mixers, down converters, etc. The P_{sat} level of the device should not exceed a particular level depending on the requirements of the system [33].

For the receive chain of the transceiver module, the prime objective and motivation of the thesis is to investigate RRT for LNAs based on different HEMT configurations and study it as a function of the pulse width of incoming signals. The other goals are to propose an MMIC LNA operating in X-band, having the best combination of high gain, noise figure, and survivability, and easily integrate-able into the system with an acceptable P_{sat}.

On the transmit side, the role of the power amplifier in radars is to extend the range of the system. The advancements in semiconductor technology have gradually replaced vacuum tube devices, magnetrons, traveling wave tubes, etc. GaAs has reliability issues due to its narrower band gap [34]. GaN HEMT is the optimum choice for designing PAs due to its excellent properties, including high voltage operation, improved power added efficiency (PAE), and high output power density. The GaN PAs can handle high reverse power reflected from the antenna (VSWR 10:1) compared to GaAs counterparts, which is very useful for single-chip transceiver solution [35, 36].

The output power, PAE, and gain are fundamental design parameters for any

PA. The higher the output power, the greater the range of the system, but it also involve heat management challenge. The PAE of an amplifier is its ability to convert DC power to useful RF output power. A poor efficiency PA complicates thermal management and challenges its reliability for extended operating hours. Therefore, it is important to design a high efficiency amplifier. The high gain relaxes the input drive requirement from the local oscillators. However, it involves the design of multi-stage amplifiers.

Reducing the on-chip losses and achieving high gain, power, and PAE in a compact area are still challenges for an MMIC PA. Another aim of the thesis is to deal with these challenges simultaneously while working on different design topologies and propose a compact MMIC PA at X-band with promising gain with more than 41% PAE and 43 dBm output power for the on-chip transceiver.

1.2 Organization

This thesis uses NANOTAM's in-house 0.15/0.25 µm AlGaN/GaN fabrication process to realize LNAs and HPAs in the X-band. The fabrication process of an MMIC and device characterizations are described in Chapter 2.

Chapter 3 discusses the design of a single-stage LNA based on cascode HEMT configuration. Its robustness is compared with an LNA based on source degenerated HEMT. The design of three-stage LNA, along with its small signal, noise, linearity, and survivability measurements, are presented in Chapter 4. Moreover, the RRT of LNA as a function of the signal's pulse width is investigated in the same chapter.

Chapter 5 shows a novel approach to limit the output power of LNA using un-gated HEMTs and their effect on LNA's other performance parameters.

Chapter 6 describes HPA's design using two approaches. It explains the complete methodology, including design topology, impedance matching networks,

stability analysis, layout design, and small and large signal measurements.

Finally, the thesis is concluded in Chapter 7, and possible future works are discussed.

Chapter 2

Device Fabrication and Characterization

2.1 GaN MMIC Fabrication Process

The content presented in this Section and Section 2.4 is drawn from the work published in the following sources:

- Imran Nawaz M, Zafar S, Gurdal A, Cankaya Akoglu B, Ozbay E. Robustness of GaN on SiC low-noise amplifiers in common source and cascode configurations for X-band applications. Int J Circ Theor Appl. 2024; 52(8): 4148–4163. doi:10.1002/cta.3937.

- Nawaz MI, Zafar S, Akoglu BC, et al. A highly survivable X-band low noise amplifier based on GaN HEMT technology and impact of pulse width on recovery time. Microw Opt Technol Lett. 2024; 66:e34330. doi:10.1002/mop.34330

NANOTAM's in-house 0.15/0.25 µm GaN-on-SiC X-band technology is used to fabricate active and passive devices. Figure 2.1 shows the cross-sectional view

of the overall structure [37] after all fabrication steps. The ohmic contacts are formed by the regrowth method [38]. The quality of ohmic contacts is analyzed using the four-point probe technique from transmission line measurements (TLM). The contact resistance of 0.5 Ω-mm and sheet resistance of 280 Ω/□ are measured from TLM patterns.

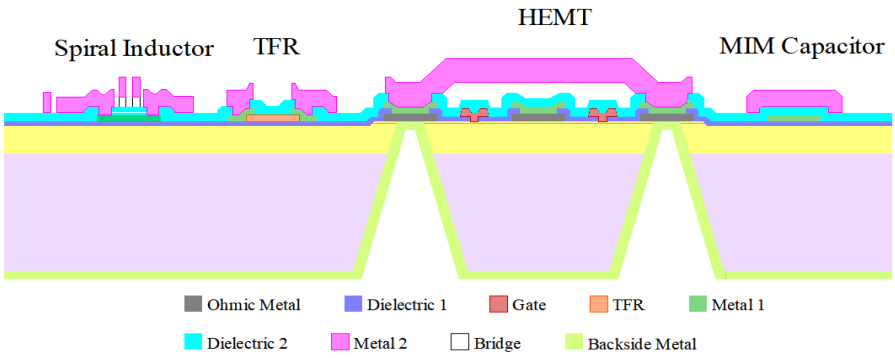


Figure 2.1: Cross-sectional view of MMIC fabrication process.

The first passivation layer, silicon nitride (Si_3N_4), is deposited using a plasma-enhanced chemical vapor deposition (PECVD) system to confine electron entrapment within surface traps and create the gate foot width for the T-gate structures. After that, the Ni/Au metal stack is deposited to the gate foot and head places using an e-beam evaporator system. The gate foot and the head thickness are 50 nm and 600 nm, respectively. The gate foot length is 150 nm, while the gate head is 500 nm long. Second Si_3N_4 passivation layer is deposited with a thickness of 210 nm. This process technology uses two different resistance structures in MMIC designs. One of them is formed with a TaN thin film resistor (thickness of 30 nm), and its value is 30 Ω/□ while the other one is a mesa resistor and its value is 270 Ω/□. As a first metal layer, 1.1 µm Ti/Au metal stack is deposited using the lift-off technique to form the first interconnection metal. After that, a 215 nm thick (Si_3N_4) passivation layer with a dielectric constant of 6.7 is deposited in order to form the metal-insulator-metal (MIM) capacitors. After air-bridge structures are formed to prevent short-circuiting of metal-metal intersections, especially for inductor structures, Au metal structures with a thickness of 4 µm are coated as a thick metal interconnection layer using the electroplating system. The current carrying capacity of the thick metal is

16 mA/µm. For the backside process, the SiC wafer is thinned to 100 µm thickness. Then, back-via holes are opened from the back side of the wafer with a diameter of 85 µm and coated with a 4 µm thick Au metal layer using electroplating.

2.2 DC Performance Tests

MMICs are typically designed based on measurement-based models of the HEMTs. For this purpose, DC characterizations of the desired HEMTs are performed.

A simple transistor model can be derived from DC measurements of HEMTs. These measurements provide maximum saturated drain current (I_{dss}), transconductance (g_m), threshold voltage (V_{th}), and breakdown voltage (V_{br}). These parameters are obtained from I-V measurements using the B1505 Power Device Analyzer from Keysight Technologies. Figure 2.2 shows the on-wafer DC characterization setup.

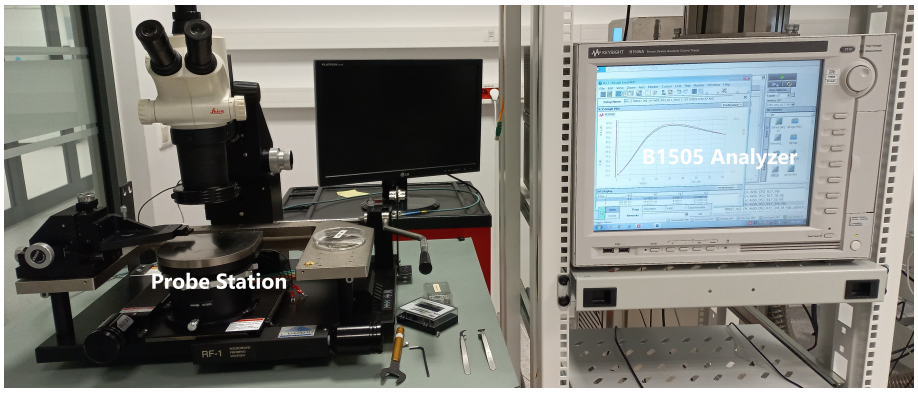


Figure 2.2: DC characterization setup for GaN HEMTs.

The I-V curves of a HEMT predict its small signal and large signal performance. The drain current to drain voltage (I_d - V_{ds}) curve shown in Fig. 2.3 indicates maximum voltage and current swings, which in turn signals the maximum possible RF output power from the device. This curve determines I_{dss} at $V_{gs} = 0$ V. The typical I_{dss} value for GaN HEMTs is 1 A/mm. However, it

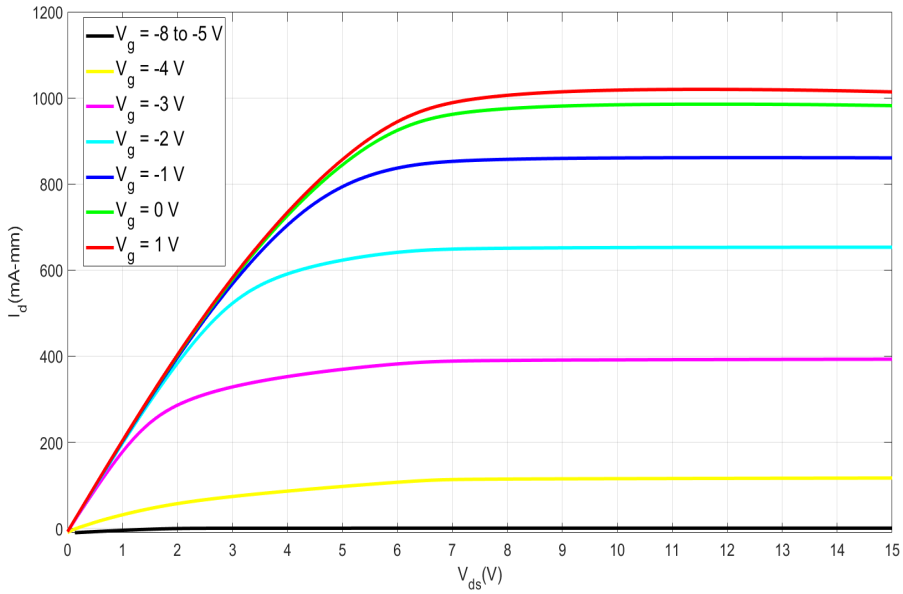
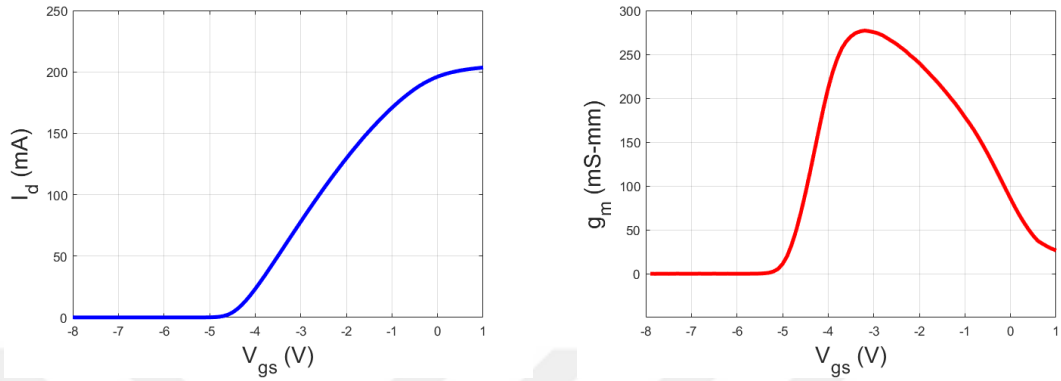


Figure 2.3: I_d - V_{ds} curves of a 4×50 µm cascode HEMT for V_g = -8 V to V_g = 1 V.

may vary depending on the process. This curve also gives knee voltage, V_{knee} (the drain voltage at 0.95*I_{dss}), which reduces the maximum voltage and, therefore, reduces the device's power capacity and power-added efficiency [39].

The drain current to gate voltage (I_d - V_{gs}) curve shown in Fig. 2.4 tells about the threshold voltage where the device starts to conduct.



(a) (b)

Figure 2.4: I_d - V_{gs} and transconductance (g_m) curves of a 4×50 µm cascode HEMT at 10 V V_{ds}.

Moreover, the slope of the curve gives g_m, which predicts a small signal gain of the HEMT at high frequencies without considering parasitic effects.

DC gate and drain current leakages are observed from breakdown measurement as shown in Fig. 2.5.

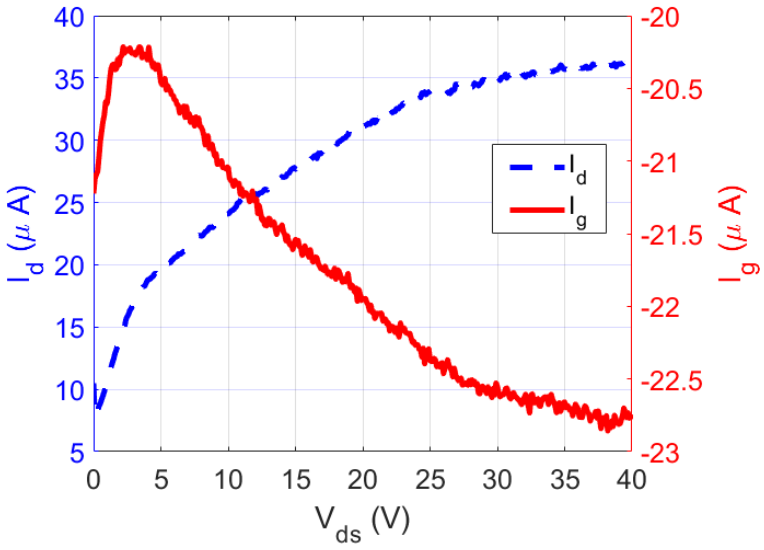


Figure 2.5: Sub-threshold (V_{gs} = -8 V) gate and drain leakage currents of a 4×50 µm cascode HEMT.

In this measurement, the gate is kept below the threshold voltage at -8 V, and the drain voltage is swept up to 40 V. The leakage currents dictate the device's reliability, lower the leakages, better the reliability, and vice versa. The values smaller than 1 mA/mm are acceptable for GaN HEMTs.

2.3 RF Performance Tests

RF performance tests include small signal, large signal, and noise measurements. These tests apply to both HEMTs and MMICs.

2.3.1 Small signal measurements

Small signal measurements give S-parameters of a device that include input reflection coefficient (S_{11}), output reflection coefficient (S_{22}), forward transmission (S_{21}), and reverse transmission (S_{12}) coefficients for a 2-port network. The small signal is the input power, which is low enough to assume that the transistor is operating in the linear region. For linear devices, S-parameters are independent of input power level and output load impedance, simplifying the design of LNAs [40].

Figure 2.6 shows the on-wafer small signal measurement setup. It comprises a performance network analyzer (PNA), probe station, and DC power supplies. HEMTs are biased using DC bias tees at RF ports of PNA. The measurements are performed at different bias points.

The device's stability and maximum available gain (MAG) are determined from S-parameters, which are essential parameters for designing an MMIC. The stability factor (K) indicates the probable oscillations (provided the input or output reflection coefficient is greater than 1) under all possible passive load and source impedances and is given by

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{(|S_{21} * S_{12}|^2)} \tag{2.1}$$

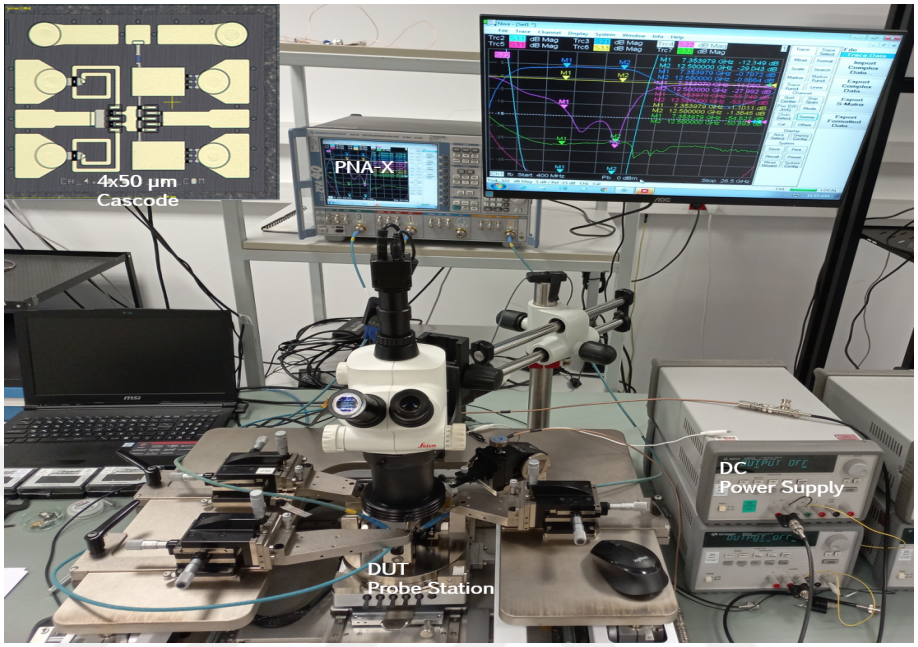


Figure 2.6: Small signal measurement setup.

Where Δ is given by:

$$|\Delta| = |S_{11} * S_{22} - S_{12} * S_{21}| \tag{2.2}$$

As per Rollet's condition, the device will be unconditionally stable if K $>$ 1 and $\Delta < 1$. This is a prime goal while designing an LNA or HPA.

MAG is the maximum gain that can be achieved with a simultaneous conjugate match at the input and output sides of the device. It is dependent upon the stability factor as given by:

$$MAG = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \tag{2.3}$$

In case the device is not unconditionally stable, i.e., K $<$ 1, then the term maximum stable gain (MSG) is used, which is defined as MAG with K = 1 and given as:

$$MSG = \frac{|S_{21}|}{|S_{12}|} \tag{2.4}$$

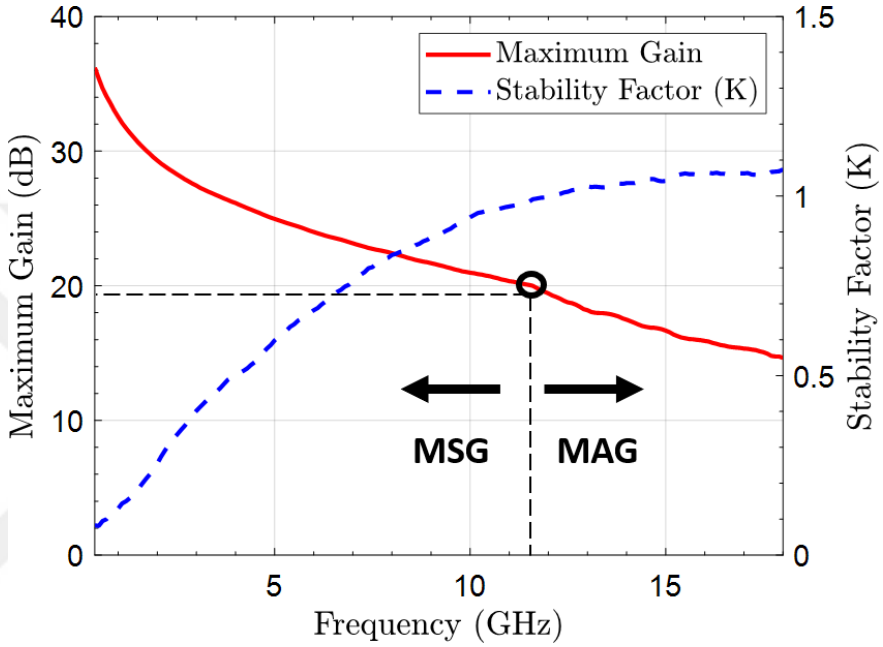


Figure 2.7: MSG/MAG and K-factor of a 4×50 µm cascode HEMT at 12 V, 250 mA/mm.

Figure 2.7 shows maximum gain of a 4×50 µm cascode HEMT. HEMT is unconditionally stable after 11.5 GHz, with maximum gain decreasing with increasing frequency.

2.3.2 Noise measurements

The noise figure (NF) of an LNA depends upon the transistor's inherent noise under a specific bias condition. The thermal noise and shot noise are two fundamental noise sources in GaN HEMTs. The thermal noise comes from the channel resistance and other parasitic resistances, while shot noise is due to leakage current through gate. Noise measurements of the transistor provide noise parameters that relate to its NF as follows:

$$NF \;=\; F_{min} \;+\; 4\, r_n \,\frac{|\Gamma_s - \Gamma_{sopt}|^2}{(1-|\Gamma_s|^2)|1 \;+\; \Gamma_{sopt}|^2} \tag{2.5}$$

F_{min} is the minimum noise figure, r_n is the normalized equivalent noise resistance, Γ_s is the source reflection coefficient, and Γ_{sopt} is the optimum source reflection coefficient corresponding to F_{min}. In an LNA design, Γ_{sopt} is the starting point for the design of an input impedance matching network. These parameters are extracted from a tuner-based automated noise characterization setup shown in Fig. 2.8.

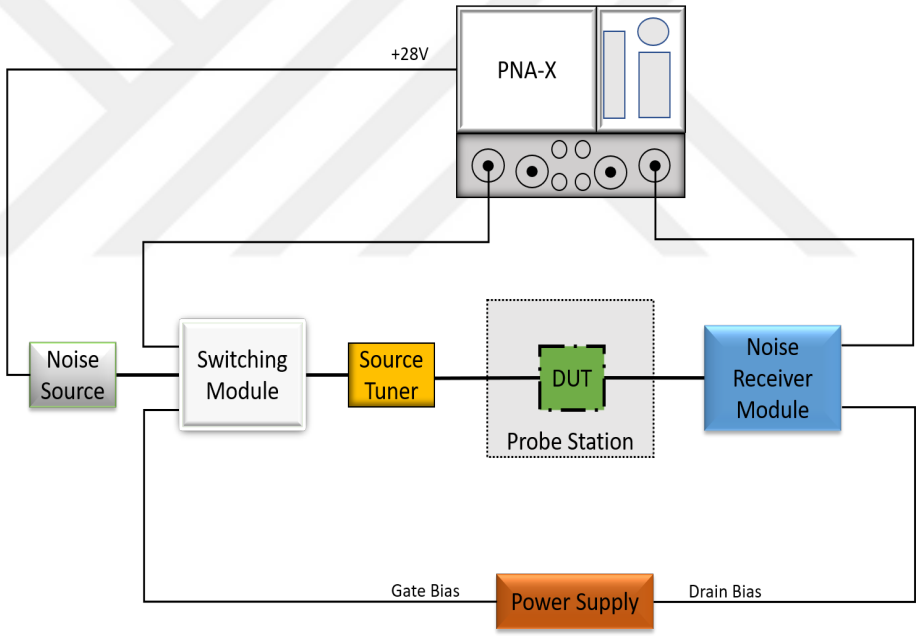


Figure 2.8: Noise parameters measurement setup block diagram.

The noise measurement setup first measures the S-parameters of the device and then noise parameters at twenty-two source impedance points at each frequency. At each impedance point, seven measurements are performed, and then the average value is recorded for each parameter.

2.3.3 Large signal measurements

The large signal refers to the input signal power that is high enough to force the transistor to operate in the non-linear region. In this region, gain starts compressing, but output power (P_{out}) keeps increasing until the saturation point. The load and source impedances corresponding to maximum power differ from small signal impedances for maximum gain. HPAs matching networks are designed for these impedance values at a particular gain compression point.

Large signal measurements are performed using a vector-based load pull characterization system shown in Fig. 2.9. This system comprises a PNA, load and source impedance tuners, low-loss couplers, bias tees, and pulsers or power supplies. The low-loss couplers sample incident and reflected waves at both sides of the device under test (DUT), which are analyzed by AMCAD Engineering's IVCAD software to determine desired parameters at frequency points of interest. For instance, the system constantly measures delivered input power, transducer power gain (G_t), P_{out}, and impedances presented by the tuner.

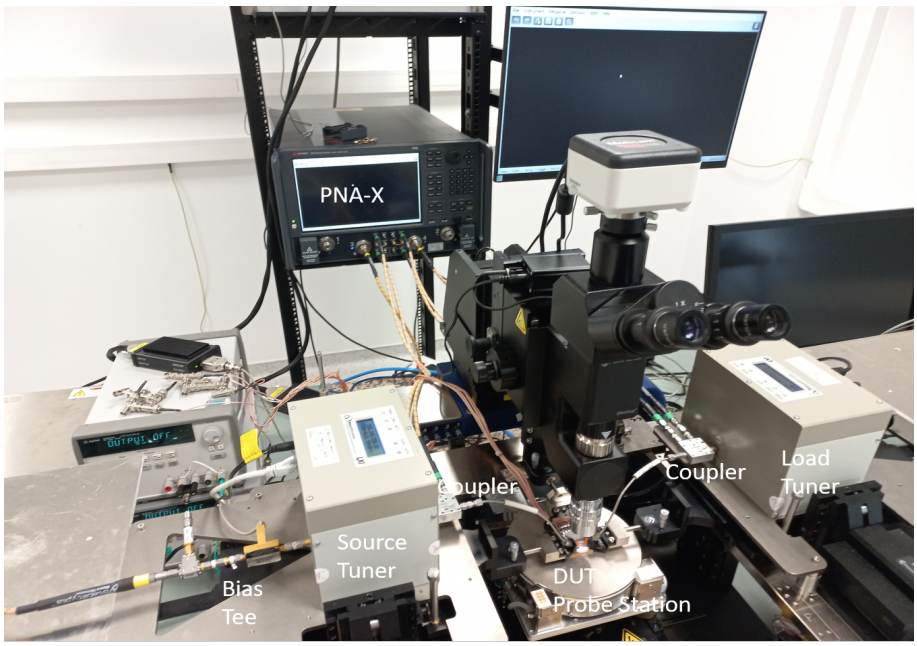
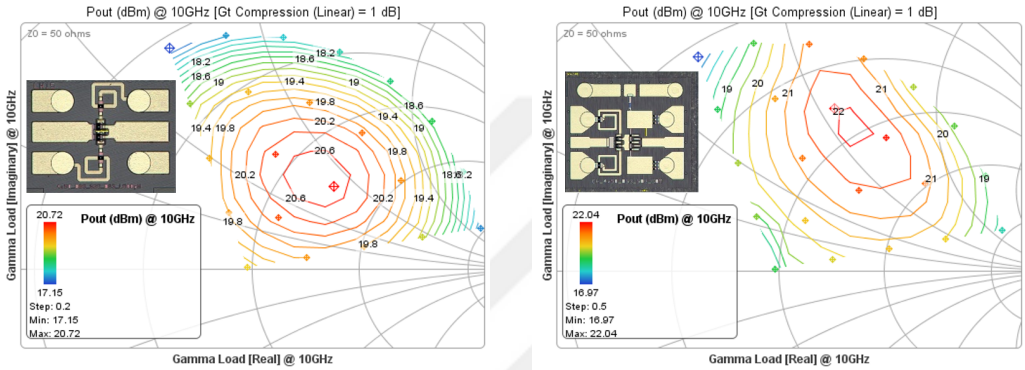


Figure 2.9: Load pull measurement setup.

LNA designers use the load pull measurement data to estimate the P_{1dB} of LNA

based on the load impedances presented to the device from its output matching network. Figure 2.10 shows the P_{out} load pull contours at a 1-dB gain compression point and 10 GHz frequency for 4×50 µm source degenerated (SD) HEMT and 4×50 µm cascode HEMT. Maximum P_{out} for SD HEMT is 20.72 dBm while that of cascode HEMT is 22 dBm.



(a) (b)

Figure 2.10: Load pull contours of : (a) 4×50 µm SD HEMT and (b) 4×50 µm cascode HEMT

2.4 Reverse Recovery Time Test

Reverse recovery time (RRT) test is explicitly used to characterize the robustness of an LNA for pulsed radar applications. Figure 2.11 shows the test setup for the characterization of RRT. The setup consists of two signal generators, a power combiner, a bandpass filter, a high-speed detector, an oscilloscope, and a spectrum analyzer. High power pulsed and low power CW signals are fed simultaneously to LNA's input. The high power signal compresses the MMIC LNA, while the low power signal serves as a reference for RRT measurement. The pulsed signal is filtered out using a narrow-band cavity filter. The low power CW signal is passed through the cavity filter and analyzed simultaneously on a spectrum analyzer via a coupler and an oscilloscope via a detector. The spectrum analyzer provides the signal compression level on the dB scale. The oscilloscope gives information about the recovery time. The critical considerations in the

measurement setup are the pulsed signal generator on/off ratio, detector dynamic range, isolation between two signals, and the sampling rate of the oscilloscope.

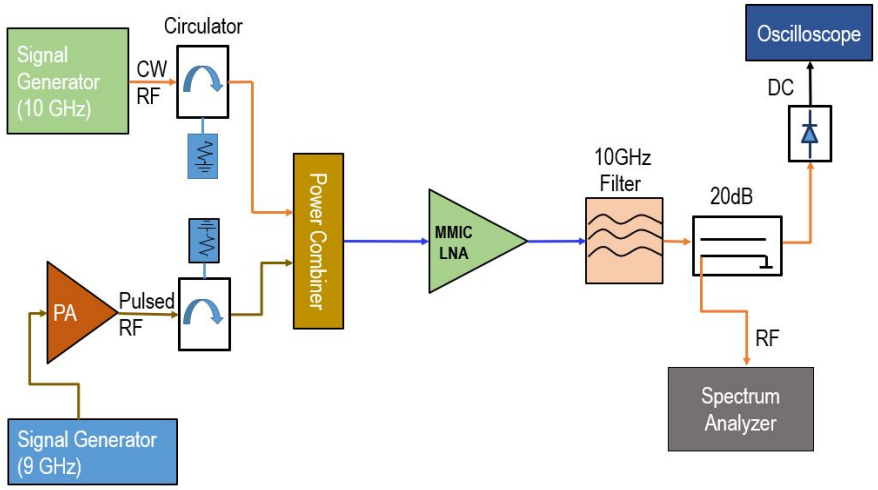


Figure 2.11: Reverse recovery time test setup.

Chapter 3

Robustness of GaN on SiC Low-Noise Amplifiers in Common Source and Cascode Configurations for *X*-band Applications

The content presented in this chapter is drawn from the work published in the following source:

Imran Nawaz M, Zafar S, Gurdal A, Cankaya Akoglu B, Ozbay E. Robustness of GaN on SiC low-noise amplifiers in common source and cascode configurations for X-band applications. Int J Circ Theor Appl. 2024; 52(8): 4148–4163. doi:10.1002/cta.3937.

3.1 Introduction

GaN technology has the advantage of built-in power handling capability to realize robust LNAs. Robustness is defined by two figures of merits (FoMs): survivability and reverse recovery time (RRT). These two FoMs play a critical role in radar applications. Recently highly survivable X-band LNAs have been reported, suitable for radar applications [41–44]. Survivability as high as 42 dBm has been reported owing to the power handling of GaN, combined with an on-chip gate bias resistor acting as a passive limiter [31]. Some designs have used bigger periphery transistors at the first stage, improving survivability at the cost of NF [45]. On the other hand, the trap excitation phenomenon associated with GaN technology has its limitations in terms of RRT [46]. Increasing the input power (P_{in}) levels leads to high gain compressions and thus increases the RRT value. An RRT of 40 ms and 10 ms corresponding to gain compressions of 33 dB and 3 dB has been reported for corresponding P_{in} levels of 36 dBm and 21 dBm, respectively [47]. An RRT of 30 ns is also reported in the literature for a gain compression level of around 8 dB [45]. Zafar et al. have related the recovery times, from nanoseconds to milliseconds, to various P_{in} levels ranging from 15 dBm to 30 dBm [46]. There is no reported work so far discussing RRT of LNAs based upon cascode HEMT configuration in the X-band to the best of authors' knowledge which highlights the novelty of this work. This work compares the robustness of LNAs based on cascode and common source configurations and facilitates the RF designers to choose appropriate HEMT configuration as per their application.

A preliminary work related to this study is reported in [48]. That publication describes the design of a single-stage LNA based on cascode HEMT and highlights the bias-invariant nature of noise figure. The theme of work reported in this submission is to investigate the robustness of cascode HEMTs compared to CS HEMTs. Using the same 4x50 µm HEMTs periphery, it is experimentally shown that cascode HEMTs can survive twice the input drive levels compared to CS HEMTs. Secondly, cascode HEMTs have comparatively better RRT than CS HEMTs shown by measurements for various input drive levels. Moreover, the small and large-signal performances for cascode and common source (CS)

HEMTs-based X-band LNAs are compared. CS HEMTs have limitations of poor isolation (S_{12}) and the Miller effect; however, they have promising noise properties and better input return losses. On the other hand, cascode HEMTs have good isolation, ease of designing the matching networks, and Miller effect suppression at the cost of high power dissipation and noise degradation compared to CS HEMTs.

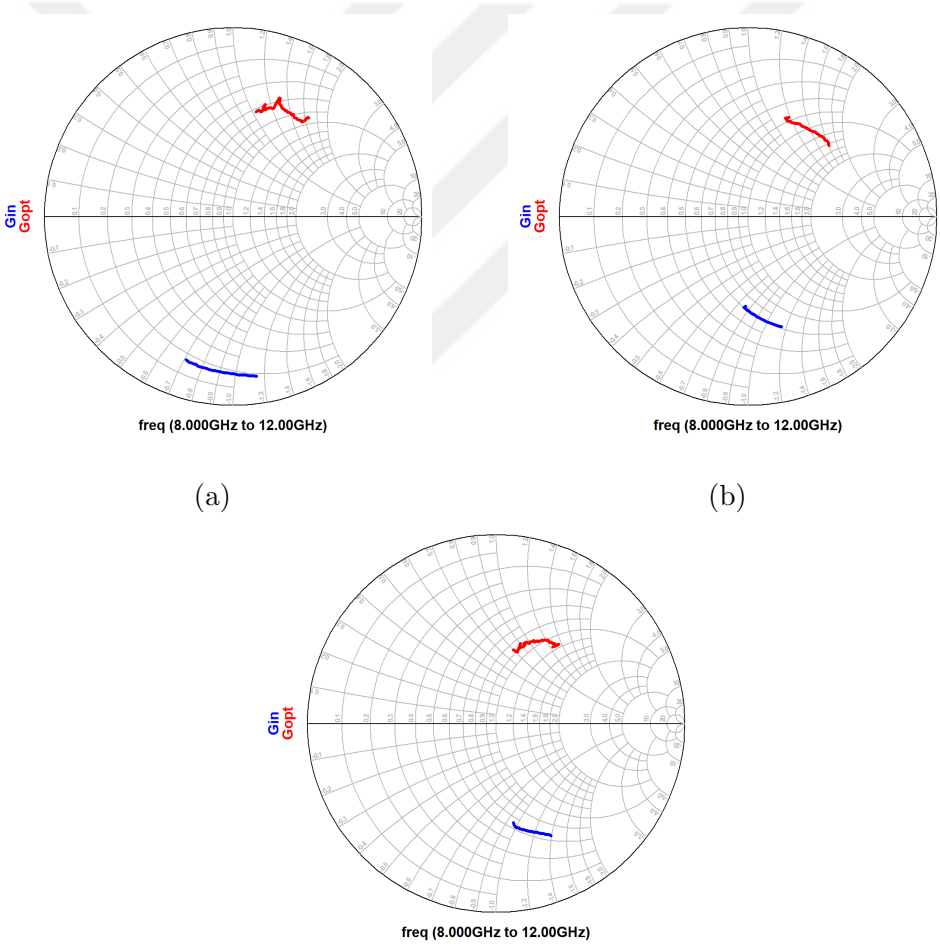
The rest of the chapter is organized as follows: MMIC design and results are discussed in Section 3.2, while robustness is addressed in Section 3.3. Section 3.4 discusses the comparison with the state of the art, while the conclusion is made in Section 3.5.

3.2 MMIC Design

3.2.1 HEMT Choice

HEMT selection is a primary step in designing an LNA because it dictates fundamental performance parameters, namely NF, P_{1dB}, and MAG. MAG comes from small-signal measurements, NF_{min} is obtained from noise measurements, while P_{1dB} and maximum P_{out} are extracted from load-pull measurements of HEMTs. HEMT performance parameters are a function of its configuration as well. Different low noise topologies include CS, cascode, darlington, and distributed amplifier. CS and cascode are renowned for their good NF performance, while darlington and distributed amplifier topologies are limited in terms of NF. In darlington topology, higher noise contribution is due to unity gain transistor, while in distributed amplifier, this contribution comes from input termination resistor. Although darlington and distributed amplifiers have larger gain bandwidth, we have chosen most widely used CS and cascode configurations for LNA applications, focussing on survivability and RRT. CS HEMTs with intentional inductance at the source terminal have Γ_{in} closer to the center of the Smith Chart and conjugate of Γ_{opt}. It facilitates the LNA designer to achieve

conditional stability and simultaneous noise and impedance match with fewer components [49–51] as shown in Fig. 3.1 for both CS and Cascode HEMTs, where Gin means Γ_{in} and Gopt means Γ_{opt}. Cascode configuration; a combination of CS HEMT and common gate HEMT, can provide better MAG and higher bandwidths [52, 53]. It facilitates the designers by providing better bandwidths without utilizing any RC feedback [54]. Higher isolation (S_{12}) values [55] also make the input impedance match less dependent on matching at the output side.



(a) (b)

(c)

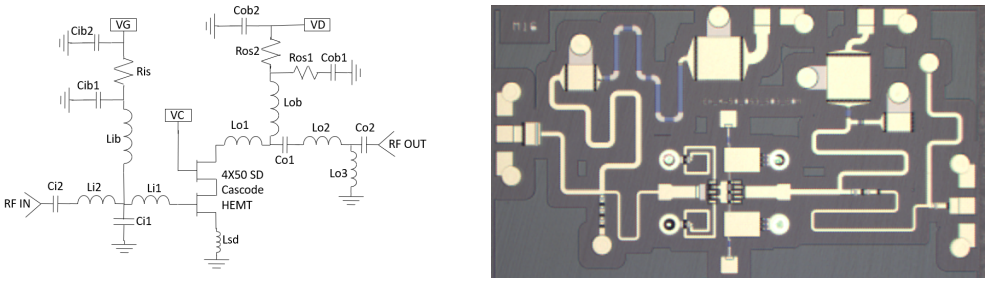
Figure 3.1: Γ_{opt} and Γ_{in} of 4x50 µm CS and cascode HEMTs: (a) CS HEMT (without intentional inductance), (b) CS HEMT (with intentional inductance) and (c) cascode HEMT

DC and small-signal measurements of 4x50 µm cascode and CS HEMTs provide technology figure-of-merits for both configurations. DC measurements of cascode HEMT show maximum drain current (I_{Dmax}) of 1 mA/mm (@Vgs=1 V), maximum transconductance ($g_{m,max}$) of 281 mS/mm and breakdown voltage at Ig=1 mA/mm is more than 100 V for the presented fabrication technology. Small-signal characterization of cascode HEMT gives maximum oscillation frequency (f_{max}) and the cut-off frequency (f_T) as 98 GHz and 35 GHz, respectively. From noise measurements, NF_{min} of cascode HEMTs at 10 GHz is 1.0 dB. On the other hand, DC measurements of CS HEMT show I_{Dmax} of 1.2 mA/mm, $g_{m,max}$ of 285 mS/mm and breakdown voltage at Ig=1 mA/mm is more than 100 V for the presented fabrication technology. The small-signal characterization of CS HEMT gives f_{max} and f_T as 42 GHz and 30 GHz, respectively. From noise measurements, NF_{min} of CS HEMT at 10 GHz is 0.7 dB.

3.2.2 Cascode LNA vs Common Source LNA

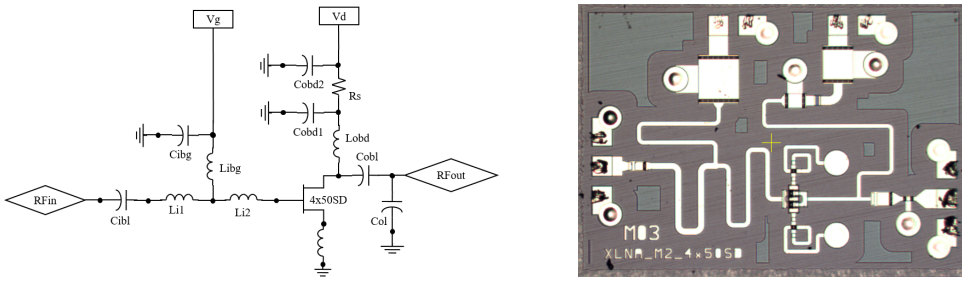
Two single-stage LNAs are designed; one with cascode HEMT (LNA-A) and the other with CS HEMT (LNA-B). We discussed the design of LNA-A in detail [48]. The schematic and layout of LNA-A are reproduced for reference in Fig.3.2a. The design of LNA-B is briefly discussed here.

The schematic and layout diagrams of LNA-B are shown in Fig.3.3. The design process starts with stabilizing HEMT over a broad range of frequencies, i.e., 0.1



(a) (b)

Figure 3.2: Design of LNA-A: (a) LNA-A schematic and (b) fabricated LNA-A



(a) (b)

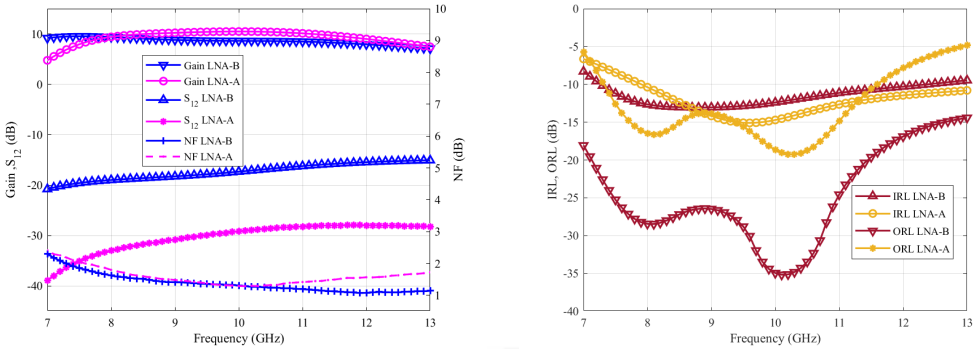
Figure 3.3: Design of LNA-B: (a) LNA-B schematic and (b) fabricated LNA-B

to 18 GHz, with the prime objective of minimum degradation in in-band MAG and NF_{min}. In order to stabilize the transistor, resistive elements are introduced at the drain side, not on the gate side, to have minimal effect on the transistor's NF. Its drawback is a decrease in the output power of the transistor, which is less concern in an LNA design. The second step is designing input matching by matching Γ_{opt} to 50 Ω. Designing an input matching network is a tradeoff between noise and input return loss (IRL). If we match conjugate (Γ_{in}) to 50 Ω, it will give good IRL, but noise will be away from optimum. Due to this reason, we are using source degeneration, which provides simultaneous noise and input impedance match [49]. On the other hand, matching Γ_{opt} to 50 Ω will provide good NF, but compromised IRL.The third step is designing an output matching network for conj(Γ_{out}); L.Boglione et al. elaborated on this step as crucial for simultaneous signal and noise match condition (SSNM) [56, 57]. The output matching can be designed for a different load impedance as well which comes from HEMTs load-pull data, if there is any specific P_{1dB} requirement. In such a case, output return loss (ORL) will be compromised. From Fig.3.3a, the components R_s, L_{obd}, C_{obd1}, and C_{obd2} towards drain side, while L_{i2}, L_{ibg}, and C_{ibg} towards gate side of the HEMT constitute the stability network, additionally providing drain and gate bias and also contributing towards matching. L_{i1} and C_{ib1} are parts of input matching, while C_{ob1} and C_{o1} complete the output match. C_{ib1} and C_{ob1} additionally serve the purpose of input and output blocking capacitors, respectively. C_{ibg}, C_{obd1}, and C_{obd2}, which are parts of the stability network, also act as bypass capacitors.

There are some similarities and differences between the LNA-A and LNA-B. Both utilize resistance at the drain side to achieve unconditional stability. LNA-A utilizes a dual-purpose resistance at the gate: stabilization and survivability. Matching networks of LNA-B comprise fewer components, while LNA-A comprises more components because optimum impedance values for LNA-B are closer to the center of the Smith chart. LNA-A requires an additional DC control voltage to bias the second HEMT in the configuration.

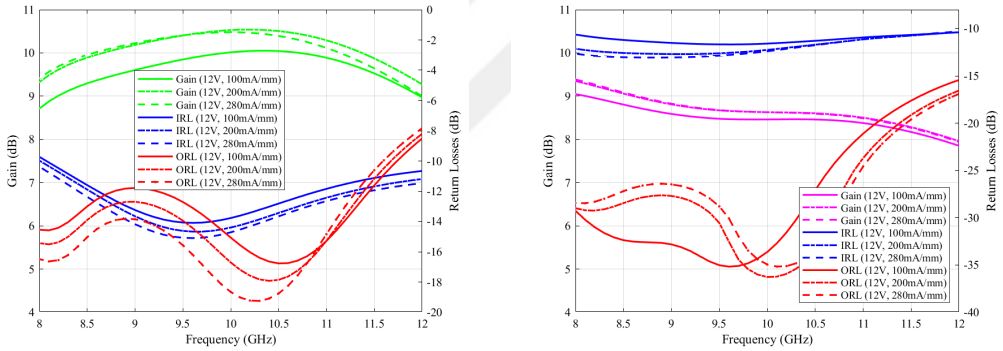
Small-signal, large-signal, and noise measurements of fabricated LNAs are performed under bias conditions of 12 V and 280 mA/mm. The 12 V is the external voltage, and 280 mA/mm is 24 percent with respect to I_{Dmax}. Figure 3.4a compares both amplifiers' small-signal and noise performance. LNA-A's gain is 10.6 dB at the center frequency of 10 GHz, while at edges, it is 9.5 dB and 9.6 dB. On the other hand, LNA-B's gain is 8.6 dB at the center frequency, while at the edges, it is 9.5 dB and 7.9 dB. Therefore, we are getting comparatively higher gain from cascode configuration as expected because cascode HEMT's MAG was about 8 dB higher than CS HEMT [48]. There is another advantage of cascode configuration in terms of impedance matching networks (MNs) design due to reverse transmission (S_{12}). The reverse transmission of LNA-A is 29 dB, and LNA-B's is 17 dB. So, the reverse transmission of LNA-A is 12 dB higher than LNA-B, making it insensitive to the effect of MNs on either side of the gate or drain. The higher reverse transmission is due to the inherent structure of cascode HEMT, where two transistors are stacked on top of each other. NF of LNA-A is 1.7 dB at 10 GHz while corresponding LNA-B has 1.3 dB. Hence, LNA-B has an overall lower NF in the whole frequency band.

Figure 3.4b shows insertion and return losses of both types of LNAs. The IRL follows a similar trend in the gain and noise performance of both amplifiers. IRL of LNA-A is 10.4 dB and 11.5 dB at band edges, while at the center, it is 14.7 dB. LNA-B's IRL is 12.7 dB and 10.3 dB at band edges, while in the center, it is 12.4 dB. Similarly, the maximum ORL value for LNA-A in the band is 7.8 dB, while for LNA-B, it is 17 dB. Hence, it is concluded that designed cascode LNA has comparatively better IRL while designed common source LNA has better ORL. In our case, CS HEMT has lower NF_{min} than cascode HEMT [48].



(a) (b)

Figure 3.4: Measured results of LNA-A and LNA-B: (a) gain, reverse transmittance (S_{12}) and NF, and (b) IRL and ORL.



(a) (b)

Figure 3.5: Measured S-parameters for different bias points: (a) LNA-A, and (b) LNA-B.

Therefore, while matching for optimum noise, we get lower IRL in LNA-B than LNA-A and better NF and vice versa.

We have investigated the S-parameters of both LNAs at different bias points, as shown in Fig.3.5. It is observed from Fig.3.5a that with bias current variation from 100 mA/mm to 280 mA/mm, LNA-A shows an increase in gain of 0.6 dB and improvement in return losses for most of the frequency band. A similar trend is observed in LNA-B except for a little degradation in ORL below 9.5 GHz, as shown in Fig.3.5b. In [48], a detailed investigation is reported on the noise performance of cascode based LNA as a function of supply voltage. There, we have shown that NF increases by only 0.14 dB for a change of drain voltage from

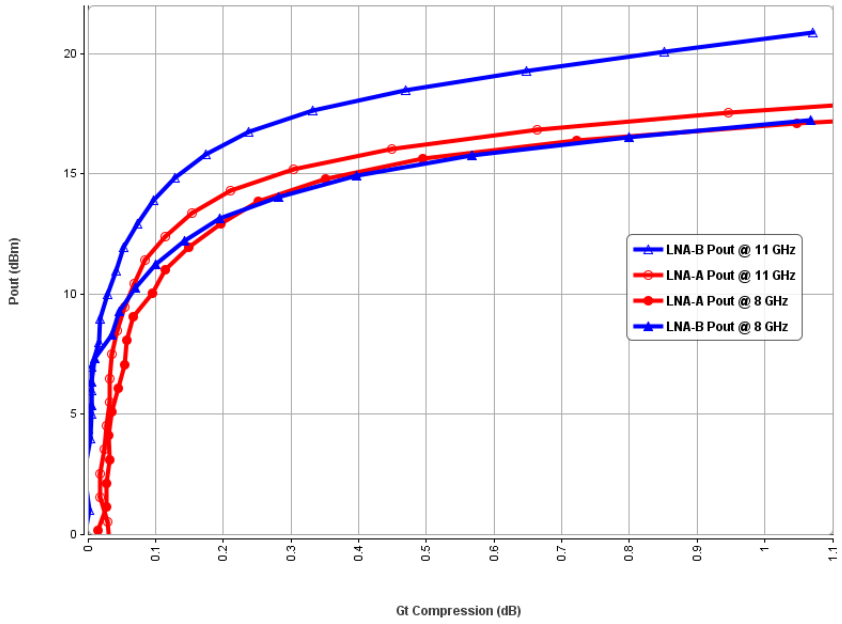


Figure 3.6: P_{1dB} comparison of LNA-A and LNA-B.

9 to 18 V, and there is an insignificant change in NF with current variation from 150 mA/mm to 300 mA/mm.

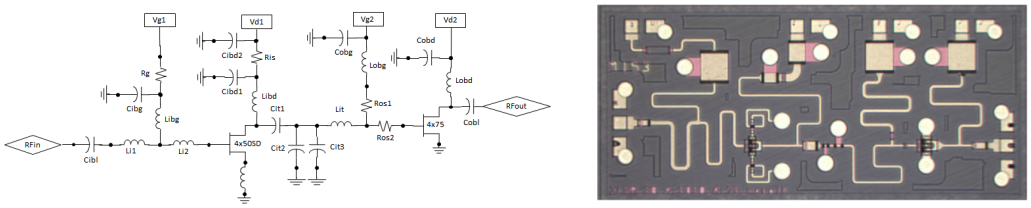
Figure 3.6 compares the large-signal response of both amplifiers. The P_{1dB} is measured at 8 GHz, and 11 GHz frequencies. Both LNAs have the same P_{1dB} at 8 GHz while at 11 GHz, LNA-B has higher P_{1dB} than LNA-A. In the authors' view, this difference in P_{1dB} is not because of different HEMT configurations; rather, it depends on the designer's preference for optimization. LNA-B is better matched for optimum P_{out} at 11 GHz than LNA-A. Two-tone test with carriers at 10 MHz offset is performed to measure the linearity of both LNAs. The minimum value of OIP3 in the band is measured to be 28 dBm for LNA-A and 27 dBm for LNA-B; the same are recorded in Table 3.2.

3.3 Robustness

3.3.1 Survivability

LNAs are an essential component of the receiver front-end for pulsed radars. Their objective is to provide higher SNR with minimum self-noise. They are often subjected to high input drive levels due to close-range target reflections, transmitter leakages, and jamming signals from other electronic warfare systems. The jamming signal can be up to 40 dBm with a duration of 10 µs [58]. Transmitter leakages depend upon transmitter-receiver isolation and are a vital function of transmitted power. Close-range reflection depends upon the target radar cross-section. LNAs should be able to survive such high input drive levels.

The survivability of an LNA is its ability to limit the forward gate turn-on current to avoid catastrophic failure. Forward gate turn-on current is one of the most prominent possible failure mechanisms in GaN LNAs. This risk of failure can be minimized by applying passive [59] and active current limiting circuits [47] at the input of LNA. These treatments enable LNA to survive under exposure to high input power levels. In this study, the survivability of LNA-A with 1 kΩ passive limiting topology is analyzed first. LNA-A survivability comparison cannot be made with LNA-B because LNA-B does not possess a passive limiter at the gate. However, it is compared with a two-stage LNA having a similar 1 kΩ passive limiter and 4x50 µm HEMT at its first stage (named as LNA-C, schematic and layout are shown in Fig.3.7) [31]. Whether a single-stage or two-stage design, 4x50 µm HEMT at the first stage exposed to high input drive decides the survivability; it is irrespective of the second stage because saturated P_{out} of the first stage and inter-stage losses make delivered power to second stage less than what first stage is exposed to as evident from output power stress analysis performed by Zafar et al. [31]. That is why comparing single-stage cascode LNA with 1 kΩ passive limiting resistor and two-stage LNA having 4x50 µm CS HEMT at the first stage with 1 kΩ passive limiting resistor, in terms of robustness is valid in our case.



(a) (b)

Figure 3.7: LNA-C having 4x50 µm HEMT at its first stage: (a) LNA-C schematic and (b) fabricated LNA-C

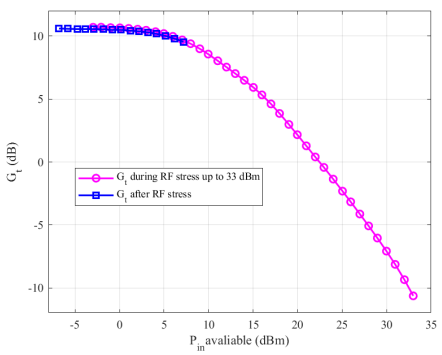


Figure 3.8: Survivability measurements of LNA-A.

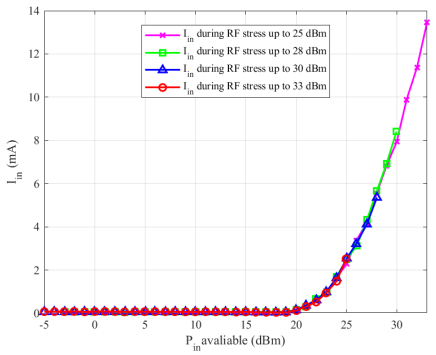


Figure 3.9: Variation in gate current with increasing input stress of LNA-A.

LNA-A with 1 kΩ passive limiter is exposed to large P_{in} levels of 25, 28, 30, and 33 dBm in steps, and small-signal gain is immediately measured after each step to ensure the survivability of the device. Figure 3.8 shows that gain before and after RF stress is almost the same. Increasing the passive limiter resistance value increases survivability, which is thoroughly discussed by Zafar et al. [31] However, there is an upper limit on resistance value as well, which is decided by the peak of negative voltage, which HEMT can withstand before breakdown. Considering 80 V breakdown and 14 mA forward gate current, resistance cannot be bigger than 5.7 kΩ. It is worth mentioning that a bias point shift is observed during survivability measurements; the drain current before and after stress is different. The drain current drop of 4 to 5 mA is observed as the stress is lifted, which is 7 to 9 percent of the nominal bias current.

Figure 3.9 shows the gate current variation as a function of input power level. As P_{in} is increased beyond 20 dBm, the voltage swing on the gate increases and

turns it on in the forward direction. This forward gate turn-on phenomenon is of paramount importance for robustness. The gate feedback resistance reduces the gate voltage swing by the increased voltage drop across it. The gate current increases with the increase in P_{in} and becomes about 14 mA at 33 dBm (2 W) input.

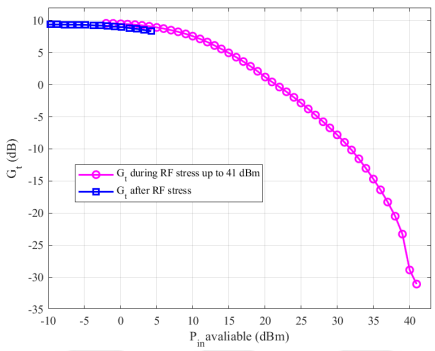


Figure 3.10: Gain before and after input stress level of 41 dBm of LNA-A.

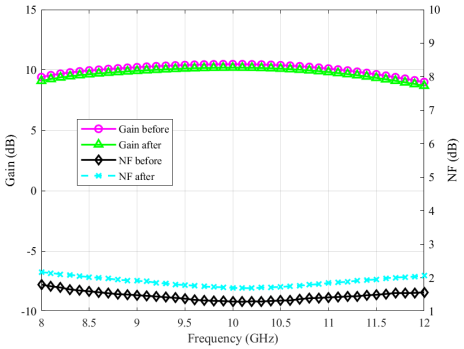


Figure 3.11: Small-signal gain and noise figure before and after input stress level of 33 dBm of LNA-A.

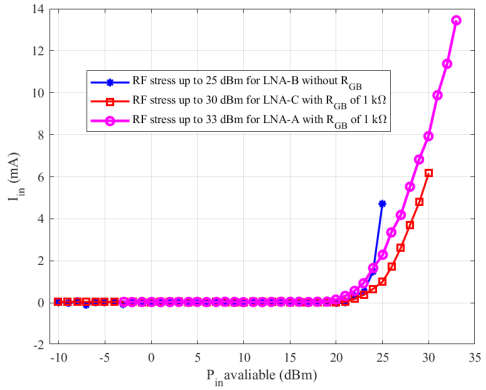


Figure 3.12: Survivability comparison of different types of LNAs, i.e., LNA-A, LNA-B, and LNA-C.

The maximum limit for forward gate current to ensure survivability depends upon recovery of gain and NF after stress. It is observed that LNA-A survives up to 40 dBm, as shown in Fig.3.10, and the corresponding drop in gain is up to 1.1 dB. However, there is a catastrophic failure at 41 dBm for 24 mA forward

gate current, as observed on IVCAD during measurements. These survivability measurements are done with a 100 µs pulse repetition period and 30 µs pulse width at 10 GHz.

Figure 3.11 shows the small-signal gain and NF results of LNA-A measured before and after exposing it to 33 dBm (We have not considered the 40 dBm level for NF after stress because of a significant drop in gain). There is no significant degradation in performance. Gain drops by 0.3 dB while NF increases by 0.4 dB. The overall NF is still below our targeted 2.2 dB value in the operating frequency band.

Figure 3.12 compares the survivability of three different types of LNAs: LNA-B with no passive limiter, 2 stage LNA with 1 kΩ passive limiter (LNA-C) [31] and LNA-A with 1 kΩ passive limiter. All these LNAs use a 4x50 µm device periphery as the only stage or the first one to make them comparable. It is seen that all LNAs get into forward gate turn on around 20 dBm P_{in} due to the same gate technology and Schottky contact. LNA-B survives only up to 25 dBm in terms of noise figure degradation while LNA-C survives up to 30 dBm, [31] results reproduced here for reference only. On the other hand, LNA-A with a similar 1 kΩ limiter survives up to 33 dBm P_{in} without much degradation in gain and noise figures. Therefore, it is concluded that cascode LNAs have comparatively better survivability than CS LNAs. The device periphery is the main reason for this better survivability [60,61] as cascode HEMT has a larger area for the electric field spread under the gate than CS HEMT. This finding is explored and reported for the first time to the best of the authors' knowledge.

3.3.2 Reverse Recovery Time

RRT is another parameter signifying the robustness of an LNA apart from survivability. This parameter is also crucial for radar applications. It is defined as the time required for the gate bias / device gain to return to its nominal value after high input stress is lifted. An LNA should have short recovery times for close-range target pickups for radars. Typical recovery time is 200 ns to

300 ns [62]; however, specific systems may relax this requirement up to 1.5 µs [45]. If we neglect the trapping phenomenon, recovery time is simply RC time constant comprising of HEMT's input capacitance (C_{in}) and gate feedback resistance. The RC time constant for LNAs is typically minimal as their C_{in} is 0.2 to 0.3 pF, which implies around 30 ns recovery time for 1 kΩ gate resistance. Nevertheless, as the input level is increased beyond a certain level (where metal-semiconductor gate Schottky contact becomes forward biased), traps are activated and dominate recovery times [31].

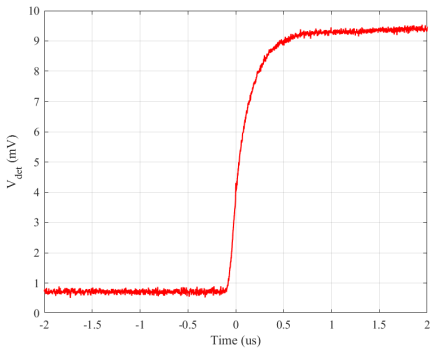


Figure 3.13: RRT with gate turn on at 20 dBm P_{in}.

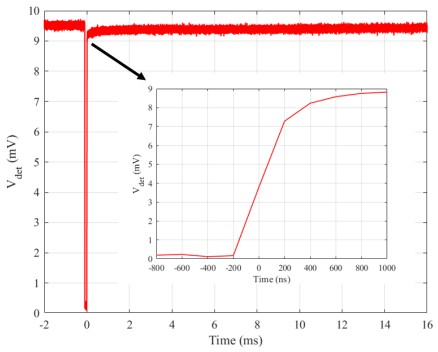


Figure 3.14: RRT with gate turn on at 30 dBm P_{in}.

Figures 3.13 and 3.14 show the RRT measurement results for the cascode LNA with 1 kΩ gate resistance. The 10 GHz CW signal with an 11 dBm level is applied at the input of the DUT (not causing any stress) along with a pulsed signal of 100 µs width, and 200 ms duration generated from a pulsed generator. The pulsed signal level is varied in the large-signal region from 16 dBm to 30 dBm. The CW signal observes compression for 100 µs, and then in a relaxation time of 200 ms, the signal recovery phenomenon occurs. The LNA takes 1.1 µs to recover after being stressed by a high input pulse of 20 dBm, as evident from Fig. 3.13. The recovery time enters the milliseconds' regime as the input power level is raised to 30 dBm. However, 0.3 dB less recovery is 600 ns, as apparent from the inset of Fig. 3.14. Here, a new terminology, "point 3 dB less recovery"(P3DLR), is introduced as an extension to the terminologies 1DLR, and 2DLR defined in [31] related to recovery time. P3DLR is the time that LNA takes to recover its gain to 0.3 dB less than the level before the stress is applied. P3DLR of 600 ns is reasonable and acceptable for some radar applications.

Table 3.1 shows RRT measurements of LNA-A and LNA-C having 4x50 µm HEMT with 1 kΩ gate resistance at the first stage. It can be seen that up till 16 dBm P_{in}, recovery is in nanoseconds but still relatively higher than 30 ns RC time constant value. The reason for being unable to capture 30 ns recovery is the dynamic range of setup; for that, there is a need to make the pulsed input much lower than 16 dBm. However, after 16 dBm P_{in}, recovery time enters microseconds regions and ultimately reaches 13 ms at 30 dBm input. RRT is a non-linear function of input due to trapping. The trapping phenomenon is explained in detail by Zafar et al. [31] . On the other hand, in the considered range of input power, gain compression is accurately approximated by a linear function of input power, as evident from Table 3.1. The LNA-A gain compression is 9 dB at 16 dBm P_{in} and increases 14 dB to 23 dB at 30 dBm, the same increment as in P_{in}.

Table 3.1: Gain compression and RRT for various P_{in}

P_{in} (dBm)	Gain Comp. (dB)	RRT LNA-A (s)	RRT LNA-C [?] (s)
30	23	13 m	-
28	21	529 µ	566 µ
27	19	148 µ	375 µ
26	19	105 µ	193 µ
25	17	7.8 µ	149 µ
20	13	1.1 µ	-
16	9	769 n	-

Table 3.1 also compares LNA-A and LNA-C having 4x50 µm CS HEMT as the first stage with 1 kΩ gate resistance similar to LNA-A. We observe from measurements that the RRT of LNA-A is slightly less than that of LNA-C. For example, at 25 dBm input, LNA-C shows 149 µs recovery while LNA-A shows 7.8 µs. Similarly, the RRT of LNA-C is 566 µs at 28 dBm, while for LNA-A, it is 529 µs. Therefore, it is concluded that cascode LNA exhibits lower RRT than

common source LNA due to its configuration. Traps become activated under a high input drive (sufficient to turn the gate on), and electrons start to flow from the output (drain) to the gate in case of a common source configuration. It takes time for the electron to return once a high pulse is released. However, in the case of cascode configuration, the high pulse is applied to the bottom transistor only, and output is taken from the drain of the second transistor; there is little or no electron flow from the output to the gate of the bottom transistor. The upper transistor helps in reducing the stored charge, which is why the trapping effect is less comparatively, which ultimately results in lower RRT. This finding is being reported for the first time to the best of the author's knowledge.

3.4 Comparison

This work is compared with already reported single-stage cascode and CS HEMT configurations based low noise amplifiers in the X-band in Table 3.2. The bandwidth of the designed amplifiers is 1 – 2 GHz higher than others. Secondly, gain flatness is either comparable or better than reported ones. IRL is comparable, while LNA-B has better ORL than other reported works.

DC power consumption of cascode HEMT-based LNA is less than similar reported work in Table 3.2. For CS topology, power consumption is higher than other CS HEMT-based LNAs because of the higher P_{1dB} target. Although the chip area of LNA-A is slightly higher than Kobayashi et al.'s work [63,64], we are achieving 2 GHz more bandwidth. The chip area of LNA-B is better than others. Due to GaN's inherent capability of handling high powers, higher DC power dissipation in a smaller chip size does not affect the noise and other performance parameters.

There are very few reported works for RRT measurements. Yagbasan et al. [47] have reported RRT of 40 and 10 ms with gain compression of 33 and 3 dB, respectively, for corresponding input drives of 36 and 21 dBm. Liero et

Table 3.2: Small signal performance comparison with reported work in X-band

Ref.	Freq (GHz)	IRL (dB)	ORL (dB)	Gain (dB)	NF (dB)	Gain Flat. (dB)	OIP3 (dBm)	DC Power (mW)	Chip Area (mm^2)	Lg (µm)	HEMT config.
[63]	$9-11$	<11	<4	>13.5	<2.2	≤ 0.5	≥ 29.5	1200	2.7	0.15	Cascode
[64]	$9-11$	<10	-	>13.5	<1.5	≤ 0.75	≥ 28	800	2.6	0.09	Cascode
[65]	$8-11$	<9.8	<12.8	>8	<1.4	≤ 1.4	-	180	3.6	0.15	CS
[66]	$8-11$	<8.5	<9.5	>7	<1.1	≤ 2.7	-	180	3.6	0.15	CS
This work (LNA-A)	$8-12$	<10	<8.4	>9.5	<1.9	≤ 0.5	≥ 28	670	4.2	0.15	Cascode
This work (LNA-B)	$8-12$	<10	<17	>7.9	<1.6	≤ 0.8	≥ 27	670	2.8	0.15	CS

al. [45] reported 30 ns RRT for gain compression levels of around 8 dB with a corresponding input power of 39 dBm. Zafar et al. [31] show the RRT value of 20 ms and 27 ns with 34 dB and 12 dB gain compression, respectively, for corresponding input drives of 30 dBm and 16 dBm. All of these works utilize CS HEMTs in the LNA design. This work shows RRT of 13 ms with 23 dB gain compression at 30 dBm input drive for LNA with cascode HEMT and RRT of 566 µs with 21 dB gain compression for LNA with CS HEMT at 28 dBm drive. On the other hand, a lot of work is reported on survivability, mainly dependent upon the value of the gate feed resistor [67]. In our earlier published work [31], we have reported the best survivability value of 42 dBm in the X-band with 5 kΩ . In this work, we have shown 33 dBm survivability with 1 kΩ gate resistor, which can be increased by increasing the resistor value. However, the chapter's main theme is that LNA design with cascode HEMT configuration can survive twice as much power as LNA design with CS HEMT.

3.5 Conclusions

This study presents robustness analysis of LNAs based on cascode (LNA-A) and common source configurations (LNA-B, LNA-C). The LNAs utilize 4x50 µm gate

widths and 150 nm gate lengths fabricated using an in-house NANOTAM GaN HEMT foundry. LNAs are designed in the frequency range of 8-12 GHz. From a robustness point of view, it is experimentally observed that LNA-A is more survivable as it handles an input power of 33 dBm while LNA-C handles only 30 dBm power, each having a 1 kΩ passive limiting resistor on the gate. These survivability figures correspond to minimal degradation in NF. However, LNA-A survives up to 40 dBm in terms of gain, as at 41 dBm, there is a catastrophic failure. Survivability of LNA-A is higher in terms of gain than survivability in terms of NF. We will further investigate this aspect of survivability in the future. Moreover, the RRT of LNA-A is also comparatively better than LNA-C due to HEMT's stacked topology. The gain of LNA-A is 1.7 dB higher than LNA-B. LNA-A has a better output match, while LNA-B has a better input match. Reverse transmission of LNA-A is 12 dB higher than LNA-B, which makes it less prone to impedance mismatch at the output side. Both LNAs have promising NF values less than 1.9 dB in the whole frequency band. Finally, the outcome of this study is that cascode HEMT configuration is better than the common source for an LNA design in terms of robustness but at the cost of a slightly increased noise figure.

Chapter 4

Highly Survivable X-band Low Noise Amplifier based on GaN HEMT Technology and Impact of Pulse Width on Recovery Time

The content presented in this chapter is drawn from the work published in the following source:

Nawaz MI, Zafar S, Akoglu BC, et al. A highly survivable X-band low noise amplifier based on GaN HEMT technology and impact of pulse width on recovery time. Microw Opt Technol Lett. 2024; 66:e34330. doi:10.1002/mop.34330

4.1 Introduction

GaN HEMT LNAs can operate continuously without protection circuitry up to a certain power level defined by the gate turn-on of the HEMT, which is related to the HEMT periphery itself. LNAs are periodically exposed to high power levels

from the transmitter for phased array radars, and LNAs survivability becomes a critical parameter there. The literature addresses survivability using bigger periphery HEMTs, active limiter, and passive limiting techniques [31, 32, 45, 47, 59]. In [31], the combination of 42 dBm survivability with less than 2 dB NF is reported, while this submission proposes an LNA having NF as low as 1.5 dB and survivability as high as 42 dBm. Improved gain and enhanced bandwidth in a compact area owe to the careful selection of source degenerated (SD) and common source (CS) HEMTs for different stages of proposed LNA.

Reverse recovery time (RRT) of GaN LNAs is an essential parameter for radar applications. RRT is mainly dominated by the traps excitation in GaN HEMTs. RRT as a function of input power level P_{in} and gain compression is reported by [31, 45, 47]. RRT increases as the P_{in} increases, and LNA is driven under high-gain compression stress. In this study, the dependence of RRT on pulse width of incoming signal is investigated. It is experimentally shown that RRT reduces as the pulse width of the input signal is reduced.

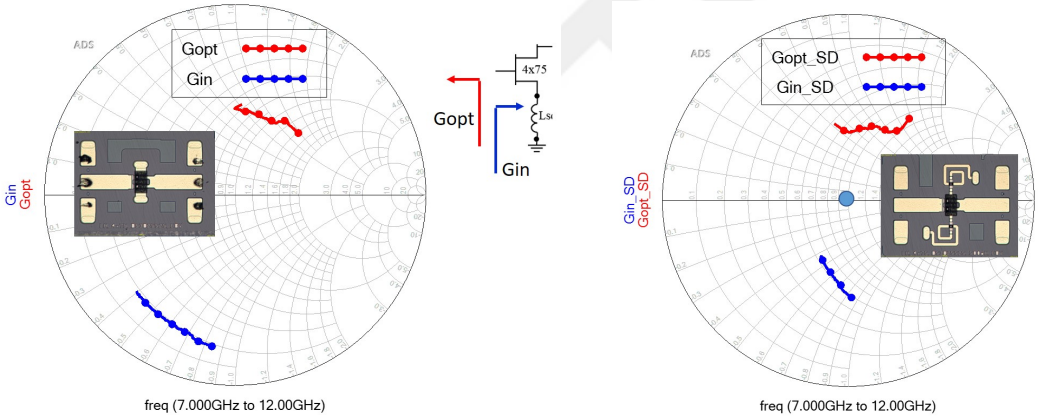
The performance of GaN LNA is associated with HEMT configuration, i.e., source degenerated or common source. SD HEMTs have an intentional small inductance at the source terminal, while the source of CS HEMTs is directly attached to the ground. There are different techniques to achieve simultaneous noise and input impedance match (SNIIM), such as inductive SD [48, 49, 68] and multiple feedback [69]. In our design, we have used inductive SD topology to achieve SNIIM. SD HEMTs are easy to stabilize, while CS HEMTs provide high gain. The advantages of SD and CS HEMTs are exploited to design an LNA with SD configuration at the first two stages and CS configuration at the third stage. This design aspect is discussed in detail in Section 4.2.

The rest of the chapter is organized as follows: LNA design and simulation along with stage-wise analysis for gain and NF is included in Section 4.2; fabrication and measurement results are explained in Section 4.3, and the conclusion is discussed in Section 4.4.

4.2 LNA MMIC Design

4.2.1 Selection of HEMTs

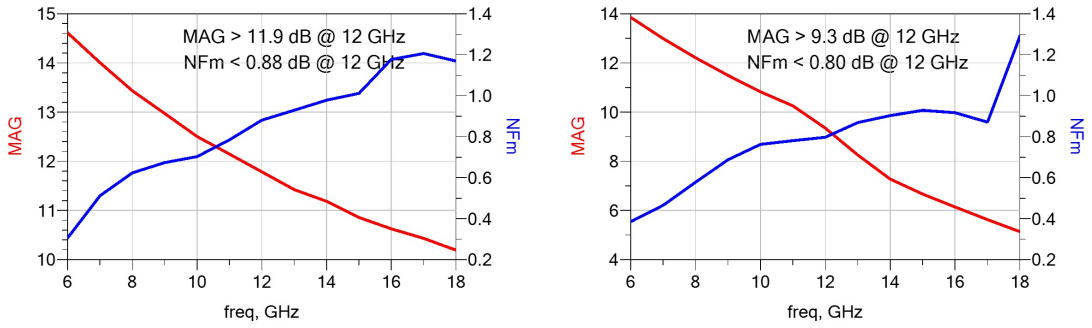
The selection of HEMT is a critical step in designing a monolithic microwave integrated circuit (MMIC) to meet the specifications. SD HEMTs have source reflection coefficient (G_{in}) closer to the center of the Smith chart and conjugate of optimum source reflection coefficient (G_{opt}) for minimum NF (NF_{min}) as shown in Fig. 4.1 for 4x75 µm SD HEMT and 4x75 µm CS HEMT. Therefore, conditional stability and SNIIM are achieved with few components.



(a) (b)

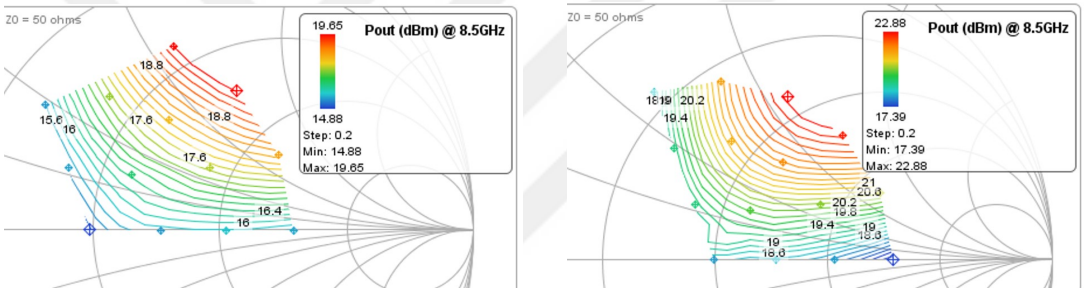
Figure 4.1: G_{in} and G_{opt} of HEMTs: (A) 4x75 µm CS; (B) 4x75 µm SD

Figures 4.2 and 4.3 show noise, maximum available gain (MAG), and large signal performance of the HEMTs from NANOTAM's in-house 0.15 µm AlGaN/GaN on SiC HEMT fabrication process. These performances are measured at 10 V and 110 mA/mm bias points. The 4x75 µm SD HEMT has 0.8 dB NF_{min} and 4x75 µm CS HEMT has 0.88 dB NF_{min} at 12 GHz frequency. On the other hand, the MAG of SD HEMT is low, i.e., 9.3 dB at 12 GHz, while CS HEMT has a higher MAG, i.e., 11.9 dB at 12 GHz. The output power at 1dB compression (P_{1dB}) is 19.7 dBm for the CS version, and that of the SD version is 22.9 dBm. From small signal, noise, and large signal performances, SD HEMTs are promising candidates for the first and second stages due to low noise



(a) (b)

Figure 4.2: NF_{min} and MAG of HEMTs: (A) 4x75 µm CS; (B) 4x75 µm SD



(a) (b)

Figure 4.3: Load pull contours of HEMTs: (A) 4x75 µm CS; (B) 4x75 µm SD

characteristics, while CS HEMT is best for the last stage for increased gain.

4.2.2 Circuit Simulations

The LNA consists of three stages; the advantage of the multi-stage approach is that higher gain levels can be achieved without affecting the NF. Fig. 4.4 shows the schematic of the LNA. The 4x75 µm GaN HEMTs with SD inductor (L_{sd}) are used at the first and second stages. The inductor "L_{sd}" helps stabilization by reducing MAG and provides simultaneous noise and input impedance match. The third stage is also 4x75 µm; however, its source is grounded directly to have better gain comparatively. HEMTs are unconditionally stabilized for even mode stability up to 18 GHz using RC networks at the drain side of the first two stages. Adding lossy networks on the drain side does not impact the device's NF. Biasing inductors also contribute to stabilization. The 3rd stage is stabilized by

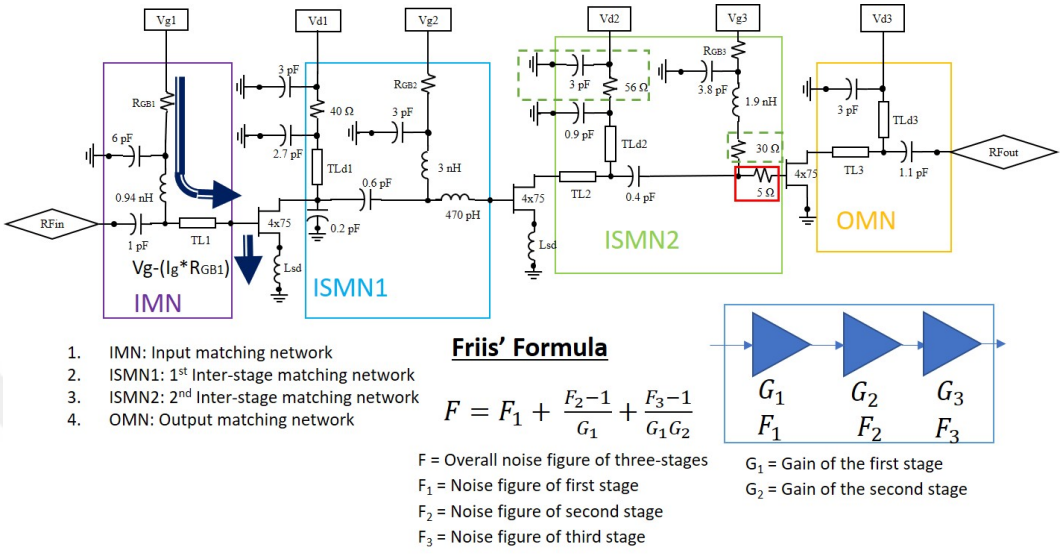


Figure 4.4: Circuit schematic of 3-stage LNA

adding series-shunt (5 Ω - 30 Ω) resistors at the gate, facilitating the matching as well. Although individual NF of the 3rd stage is higher due to a lossy (resistive) network at its gate, its overall contribution is relatively very low per Friis' formula (as shown in Fig. 4.4).

Each LNA stage has a distinct role in overall LNA performance. Stage-1 aims for low NF, stage-2 cares about NF and gain ripple, and stage-3 focuses on better gain and output match. Biasing inductors and series DC blocking capacitors are part of the matching networks to reduce the component count. Spiral inductors are used on the gate side due to their compact nature and to reduce overall chip size. However, these cannot be used on the drain side due to the low current consumption of metal-1 connection, i.e., 2 mA/mm at the junction of metal-1 and metal-2. Meandered transmission lines TL_{d1} – TL_{d3} have larger current carrying capacity, i.e., 16 mA/µm, and therefore, are used as drain bias lines. Matching networks are optimized to obtain promising performance in the operating frequency band regarding NF, gain, return losses, and gain ripple. The gate bias resistors, R_{GB1}, R_{GB2}, and R_{GB3}, are added for survivability purposes (see Section 4.3 for details).

EM simulation results of the designed LNA are shown in Fig. 4.9. Its gain is

in the range of 23.0 – 25.0 dB. NF is below 1.48 dB, while the input reflection coefficient (IRC) and output reflection coefficient (ORC) are below -9.3 dB and -8.7 dB, respectively.

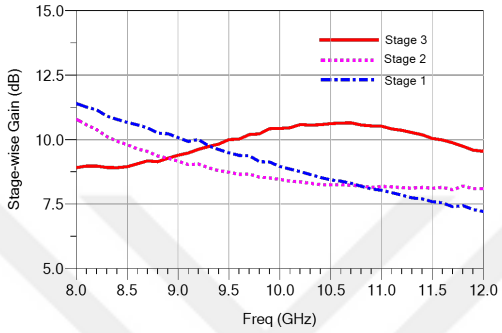


Figure 4.5: Stage-wise gain analysis of LNA MMIC

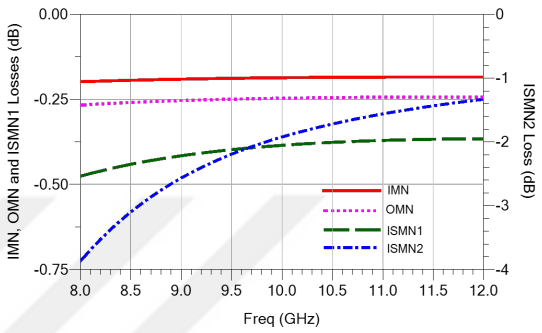


Figure 4.6: Matching networks losses of LNA MMIC

In this study, we have also analyzed the stage-wise gain, network losses, and noise figure of the complete amplifier. Fig. 4.5 and 4.6 show individual gains of each stage and corresponding matching network (MN) losses, respectively. MNs are designed in such a way to have minimum NF, maximum P_{1dB}, and reduced gain ripple. IMN is designed in such a way as to have a loss of less than 0.2 dB. On the other hand, the third stage governs the P_{1dB}, being compressed before the first and second stages. Therefore, to have better linearity, OMN loss is kept below 0.27 dB. Although the contribution in NF from the second stage is less, yet not negligible, ISMN1 loss is kept below 0.48 dB at the design stage. The least contribution from the third stage towards NF gives the designer flexibility to design ISMN2 for controlling the gain ripple by introducing intentional extra losses at the lower half of the frequency band. This effect is evident from Fig. 4.6, where ISMN2 loss varies from 1.3 dB to 3.9 dB. The overall simulated gain ripple of the proposed LNA is $\pm$ 0.7 dB.

Fig. 4.7 shows the stage-wise simulated analysis of the contribution of NF from each stage and is principally a direct translation of Friis' formula. Moving from stage 1 to stage 2, NF value increases from 1.12 dB to 1.42 dB. There is still a minor increase of 0.06 dB in NF from the final stage. The optimum choice of HEMTs explained in Section 2.1, coupled with careful design of MNs, results in achieving an overall NF as low as 1.48 dB.

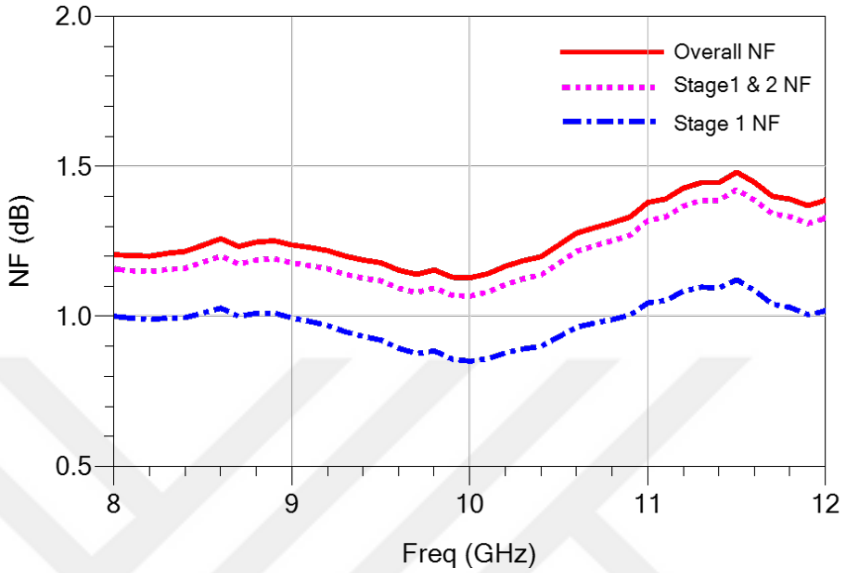


Figure 4.7: Stage-wise noise analysis of LNA MMIC

4.3 Fabrication and Measurements

Fig. 4.8 shows a microphotograph of the fabricated 3-stage LNA MMIC. Grounding is provided by elliptical back-vias. The overall area is minimized by the use of meandered inductive transmission lines. In order to reduce EM coupling in the operating frequency band, minimum spacing of 70 µm is maintained between two adjacent transmission lines. DC and RF pads serve the purpose of measurement and interconnections. The total size of MMIC die is 2.8 mm x 1.39 mm. The fabrication utilizes NANOTAM's GaN HEMT 0.15 µm technology.

4.3.1 Small Signal and Noise

Small signal and noise measurements are performed on the fabricated MMIC using standard test setups under operating bias of 10 V and 110 mA/mm. Fig. 4.9 shows the measured small signal and noise performance of 09 x MMICs placed at different locations on the wafer to see the uniformity across the wafer. The dotted lines show simulation response, while solid lines show measured response. The measured gain is in the range of 22.2 – 24.8 dB. The dB scale's maximum

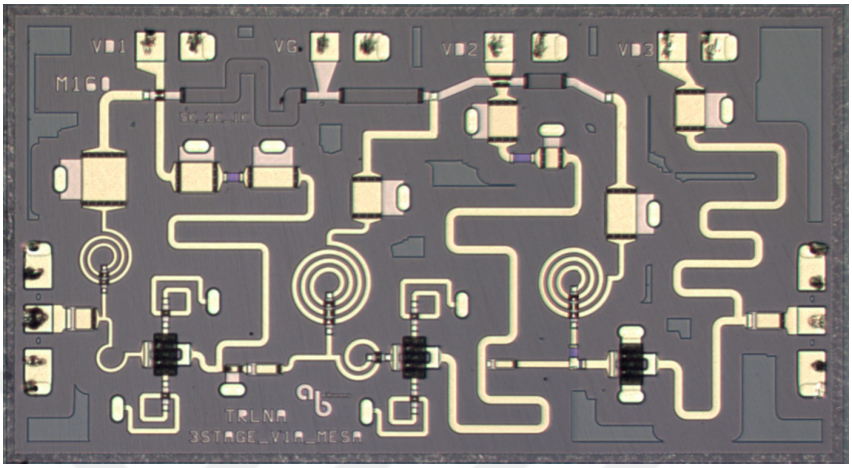


Figure 4.8: Microphotograph of 3-stage LNA MMIC

in-band measured IRC and ORC values are -10 dB and -9.4 dB, respectively. The maximum NF is measured as 1.49 dB from 8.0 GHz to 12.0 GHz. The gain flatness across the operating band is also measured and recorded as ± 1.0 dB. The better gain flatness helps to achieve better inter-symbol-interference levels and optimal range performance for radar applications. Overall, the simulated and measured results are in close-agreement.

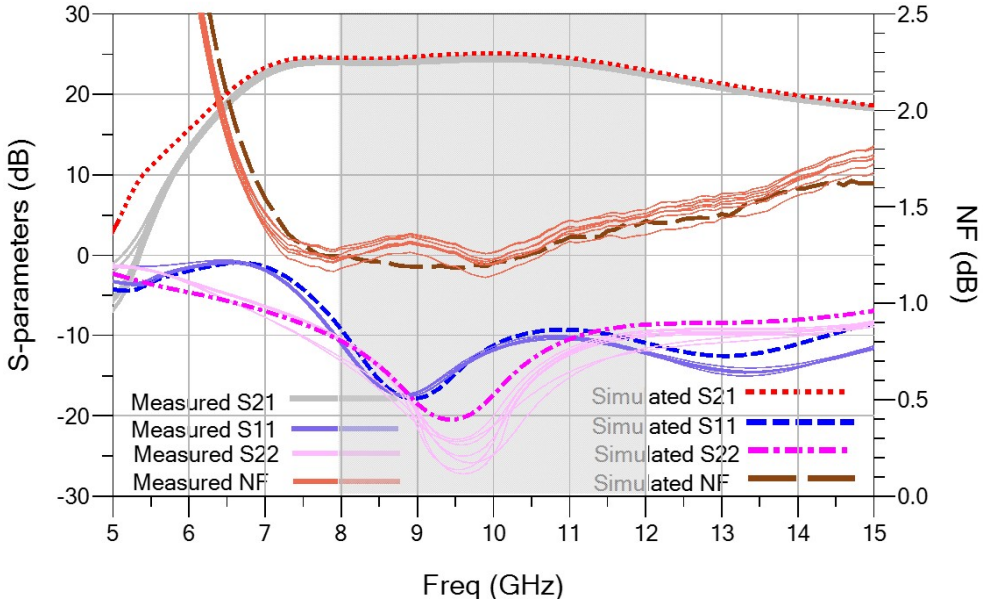
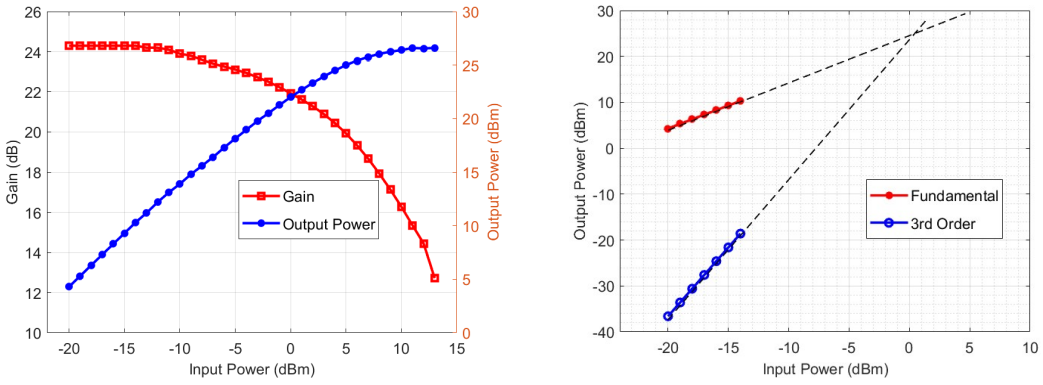


Figure 4.9: Simulated and measured small signal and noise results of 3-stage LNA

It is to be mentioned that each HEMT in the LNA draws 33 mA drain current, and the total current consumption of LNA is 99 mA. There is an RC network on the drain side of the first and second stages, as shown in Fig. 4.4, which reduces the effective voltage at the drain of the HEMT. The 40 Ω resistor at the drain of first stage causes a 1.32 V voltage drop, and the 56 Ω resistor at the drain of second stage causes a 1.85 V drop. Resultantly, the voltage at the drain of the first and second stage reduces to 8.68 V and 8.15 V, respectively, instead of 10 V. The reduction in drain bias does not affect the gain and other parameters, because the voltage drops of 1.32 V and 1.85 V are not significant enough to cause a large mismatch between simulated and measurements results, as evident from Fig. 4.9.

4.3.2 Linearity

Figure 4.10 shows output power at 1-dB gain compression (P_{1dB}), P_{sat}, and output third-order intercept point (OIP3) measurements of the proposed LNA. P_{1dB} is measured at band's center frequency of 10 GHz by sweeping input power from the signal generator and output power is observed on a spectrum analyzer. Gain is also calculated, and the output power value where the gain is compressed by 1 dB is recorded as 16.4 dBm. The corresponding P_{in} is -7 dBm.



(a) (b)

Figure 4.10: Linearity characterization of 3-stage LNA: (A) P_{1dB}; (B) OIP3

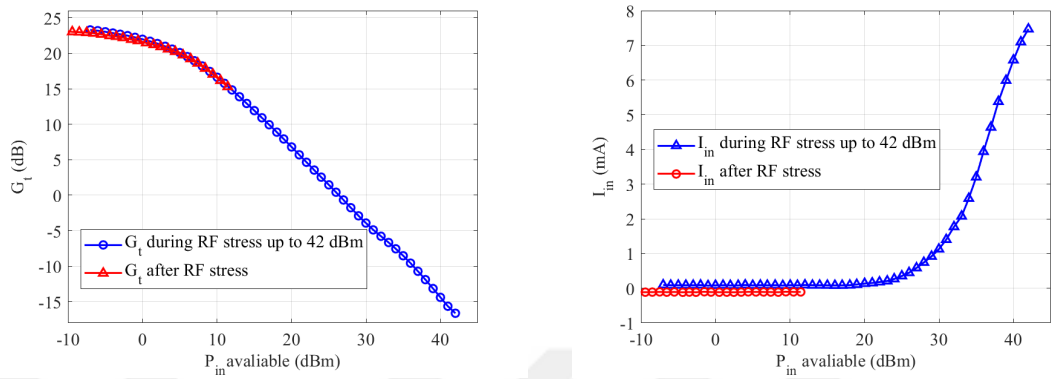
OIP3 is measured by performing the two-tone test with tones at 10 GHz and

10.01 GHz having a 10 MHz offset. The third-order products are expected to be at 9.99 GHz and 10.02 GHz. The power levels of fundamental and third-order products are recorded at low input power levels of -20 dBm to -14 dBm, which are well below -7 dBm (input level for P_{1dB}). The fundamental and third-order product curves are extrapolated linearly to obtain an OIP3 value of 24.7 dBm, as shown in Fig. 4.10b. The corresponding input power at the third-order intercept point (IIP3) value is 0.4 dBm.

4.3.3 Survivability

LNA's survivability is defined as its capability to restrict the forward gate-turn on current (I_g). For multi-stage design, gate feedback resistor (R_{GB}) is used at the first stage by some designers [31, 59], while others use it at all the stages [70, 71]. In this study, R_{GB} at all stages are used, and the values are 5 kΩ (first stage), 2 kΩ (second stage), and 1 kΩ (third stage). The reason for decreasing R_{GB} values stage by stage is the reduction of stress level from one stage to the other. The first stage will be exposed to maximum stress, while for others, stress will be saturated output power of the previous stage minus the matching network loss between the stages. The stress level for the second and third stage is obtained by subtracting the ISMN1 and ISMN2 losses from P_{sat}, respectively. The loss for ISMN1 is 0.37 dB and for ISMN2, it is 1.8 dB at 10 GHz, as evident from Fig. 4.6. This fact shows that the stress level at the input of the third stage HEMT is about 1.4 dB lower than that of the second stage HEMT. Therefore, the value of R_{GB} is chosen smaller than that for the second stage.

The R_{GB} improves the survivability by reducing the I_g of the HEMT [59]. Under a small signal, normal gate current, known as leakage current, flows out of the gate. However, as a high input signal is applied, I_g starts to flow into the gate, and its direction is shown by the arrows in Fig. 4.4. We use normally-ON HEMT, which needs a negative gate voltage for normal operation. Without R_{GB}, larger peaks of the high input signal make the gate Schottky contact forward biased, and I_g starts to flow. With R_{GB}, the negative voltage at the gate becomes



(a) (b)

Figure 4.11: Survivability measurements of 3-stage LNA (A) G_t; (B) I_{in}

more negative by a factor (I_g*R_{GB}), and the effective gate voltage at the gate is V_g – (I_g*R_{GB}), as shown in Fig. 4.4. The RF voltage swing is shifted to lower voltages, and positive peaks of gate voltages cause the forward gate current to be reduced. Resultantly, I_g is reduced, and the device survivability is enhanced.

For survivability analysis, LNA is exposed to step-wise large P_{in} levels of 33, 39, 40, and 42 dBm (setup limit), and transducer power gain (G_t) is immediately measured after each step on IVCAD. The LNA survives up to 42 dBm P_{in} as seen from Fig. 4.11. The gain degradation after stress is within 1 dB, which is in the tolerance limits. Fig. 4.11 also shows the variation in forward gate current with respect to P_{in}. The gate turn-on phenomenon is observed beyond 20 dBm P_{in} level. However, the catastrophic failure condition was not tested due to the limitations of the test setup. These measurements are performed at 10 GHz with 25 µs pulse width and 250 µs pulse period.

4.3.4 Reverse Recovery Time

RRT as defined earlier in Chapter 1 is the time for the device gain / gate bias to return to its initial value after releasing high input stress.The typical C_{in} of small periphery HEMTs used in this design is around 0.3 pF leading to 80 ns recovery for 5 kΩ R_{GB}. However, in the case of a gate feedback resistor at more than one

stage, recovery of the stage under the highest compression state will dominate. Under low input stress, recovery of the last stage will dominate. In contrast, under high input stress, recovery of the first stage will dominate as the following stages will have stress up to P_{sat} level only, as explained in Section 4.3.3. Nevertheless, The traps activation dominates the recovery time after a certain level of P_{in}, where Schottky gate contact is forward-biased.

Table 4.1: Three stage LNA RRT.

	Pulse Width = 200 µs		**Pulse Width = 25 µs**	
Pin (dBm)	**Gain Compression (dB)**	**RRT (msec)**	**Gain Compression (dB)**	**RRT (msec)**
6	7	5	6	2
10	9	7	8	2.3
15	15.5	8.5	15.5	2.4
20	23	10	22	2.6
25	26	70	24.5	4

Table 4.1 shows RRT measurements of the proposed LNA. The pulsed signal is varied from 6 dBm to 25 dBm. The recovery time increases gradually with the increase in P_{in} level. RRT is in a milli-seconds regime, although gain compression is low. In order to see RC time constant recovery, P_{in} needs to be lowered further; however, the same could not be captured due to the dynamic range of setup, mainly the detector. RRT is a non-linear function of P_{in} due to trapping. Buffer traps are activated in Fe-doped GaN HEMTs under exposure to high input signal. The dominance and effect of trap excitation and RC time constant are explained in detail in our earlier publication [31].

In this study, the RRT phenomenon is studied as a function of the pulse width of the high-stress signal. RRT of proposed LNA is measured at pulse widths of 200 µs and 25 µs with 0.25 % duty cycle giving enough time for signal recovery. Table 4.1 shows that recovery time is 2 ms and 7 ms at 6 dBm P_{in} for 25 µs and 200 µs, respectively. Similarly, these values are 4 ms and 70 ms at 25 dBm P_{in}. This shows that RRT is a strong function of the pulse width of the incoming signal; the lower the pulse width, the better the recovery time, and vice versa. The primary reason for better recovery time under low pulse width conditions is that fewer trap sites are ionized than in more extended pulse width conditions. The more significant number of trap sites take longer to de-ionize once the stress is released. Reverse recovery time for different pulse widths in terms of trap excitation is reported for the first time to the best of the authors' knowledge. This fact also emphasizes the need to characterize RRT as per actual pulse conditions of a particular radar system.

4.3.5 Comparison

Table 4.2 compares the proposed X-band LNA with already reported works in the literature. We have reported 42 dBm survivability in our earlier work [31]. However, this LNA is the best combination of survivability and NF in the X-band reported so far in the literature to the best of the author's knowledge. This design also has a broader bandwidth comparatively. The presented work is one of the few X-band GaN LNAs reported using 0.15 µm gate length (L_g). This work proves to be promising for linearity as well as small signal performance in comparison with 0.15 µm and 0.25 µm GaN technology nodes. Moreover, RRT is studied as a function of the pulse width of the high input stress signal. It is shown that RRT is directly related to the pulse width; the shorter the pulse width, the shorter the recovery time, and vice versa.

Table 4.2: Comparison of proposed LNA with the state of the art in the X-band.

Ref.	**Frequency (GHz)**	**NF (dB)**	**IRC (dB)**	**ORC (dB)**	**Gain (dB)**	**Survivability (dBm)**	**OIP3 (dBm)**	**Chip Area (mm^2)**	**Lg (um)**
[41]	$8.4-10.6$	<2.3	<-10	<-12	>25	41	-	7.5	0.25
[42]	$8-11$	<2.3	-	-	>16	41	-	3.5	0.25
[43]	$8-11$	<2.5	<-10	<-8.5	>17	39.5	-	6.3	0.25
[31]	$8-11$	<2.0	<-9	<-11	>19	42	30.5-34.2	3.6	0.15
[72]	$8-11$	<2	<-9	<-5	>22	34	24-29	3.6	0.25
[73]	$8-11$	<2.2	<-8	<-10	>25	37	26	4.3	0.25
[74]	$9.7-12.9$	<2.1	$<-3.0*$	$<-5.0*$	>20	-	-	1.4	0.25
This work	$8-12$	<1.5	<-10	<-9.4	>22	42	24.7	3.9	0.15

* Estimated from figures

4.4 Conclusion

This study presents a highly survivable low-noise amplifier utilizing common source and source degenerated GaN HEMTs. The LNA is fabricated using an in-house NANOTAM 0.15 µm process. The LNA comprises of three stages and operates in the whole X-band. The high gain is achieved in a compact area by carefully utilizing spiral inductors and meandered transmission lines. This LNA achieves a high level 42 dBm survivability along with 1.5 dB NF best reported combination in X-band to the best of author' knowledge. RRT of LNA is measured under low and high pulse width conditions, and it is shown that RRT is 4 ms at 25 µs and 70 ms at 200 µs with the same 25 dBm P_{in} level. RRT dependence upon pulse width, shown experimentally in this study emphasizes the need to characterize the LNAs as per actual pulse conditions of a particular radar system.

Chapter 5

Limiting output power of GaN Low Noise Amplifiers using Un-gated HEMTs

5.1 Introduction

Gallium Nitride (GaN) on Silicon Carbide (SiC) technology has produced low noise amplifiers (LNAs) with high linearity and high output power at 1-dB gain compression point (P_{1dB}). However, they have higher saturated output power (P_{sat}) values, which pose an integration challenge for system designers. For safe integration of an MMIC LNA with subsequent sub-systems and modules, i.e., mixers, down converters, etc., the P_{sat} of the device should not exceed a particular level as per the system requirements.

Several techniques are reported in the literature to reduce the P_{sat}. Kaule et al [75, 76] proposed the idea of using an output attenuator and an adaptive drain supply to keep output power (P_{out}) below 10 dBm. Mayock et al [77] discussed an ad hoc biasing scheme limiting power around 15 dBm. In [33, 78, 79], gated HEMTs are used for limiting the drain current, consisting of a small transistor

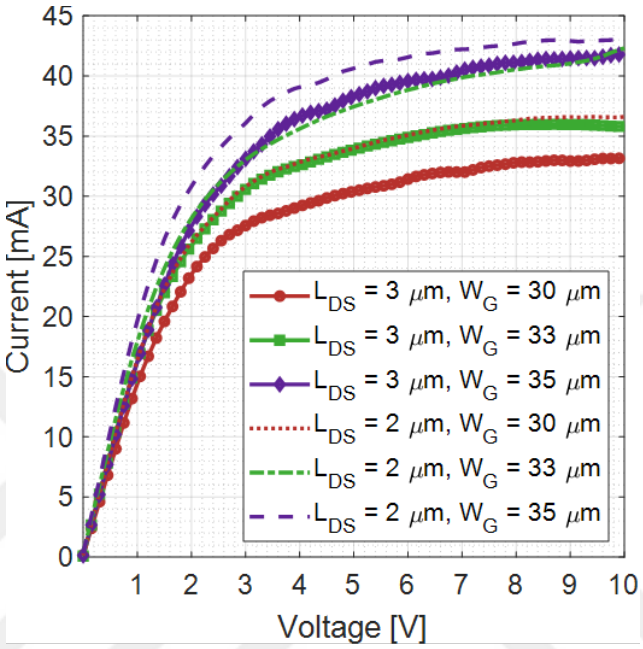
with the gate-source shorted together.

In this study, we propose a novel idea of using un-gated HEMTs, which also restricts the LNA's output current and limits its P_{sat}. This approach is advantageous because the un-gated HEMTs are not susceptible to gate degradation issues and Schottky breakdown phenomenon. The un-gated HEMT acts like a variable resistor, and its resistance varies as a function of the current flowing through it. This study explains the utilization of a 35 µm HEMT on the drain line of three three-stage LNA and its effects on the small signal, noise, linearity, and large signal performance of the LNA in detail, being reported for the first time to the best of the author's knowledge.

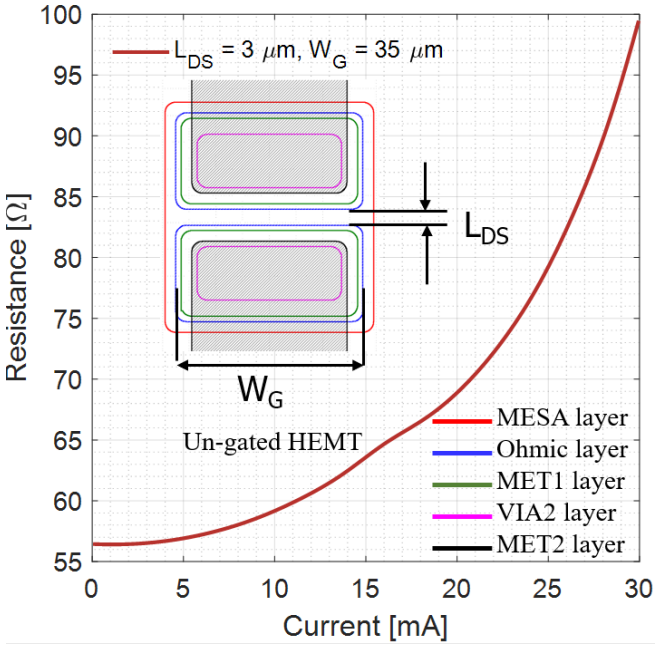
5.2 Un-gated HEMTs

An un-gated HEMT represents a symmetrical placement of two ohmic contacts with a typical separation distance of 2 or 3 µm. In the case of GaN un-gated HEMTs, the current conduction medium is the 2-dimensional electron gas (2DEG), which provides a low sheet resistivity in the range of 300 to 400 $\Omega-$sq. In this configuration, there is no active gating of the current flow. Therefore, current flows freely between the ohmic contacts upon application of a nonzero voltage across the electrodes. However, current flow is passively constrained by the electron velocity saturation [80]. In GaN HEMTs, drift velocity starts to saturate at fields as low as 10 kV/cm, corresponding to a potential difference of just 3 V in the case of 3 µm contact separation. This suggests that un-gated HEMTs can be used as a current limiter of GaN HEMT based LNAs. Of importance is the determination of un-gated HEMT architecture and design parameters. In this study, we studied two parameters: contact separation and contact width. As shown in Fig. 5.1a, saturation, and hence the limiting current, is directly proportional to the contact width. In the same figure, we display the impact of contact separation for two cases at 2 and 3 µm. In effect, reducing the contact separation effectively reduces the on-resistance figure with a slight increase in the saturation current. The drain-to-source resistance also increases with the increase

of current flow as shown in Fig. 5.1b.



(a)

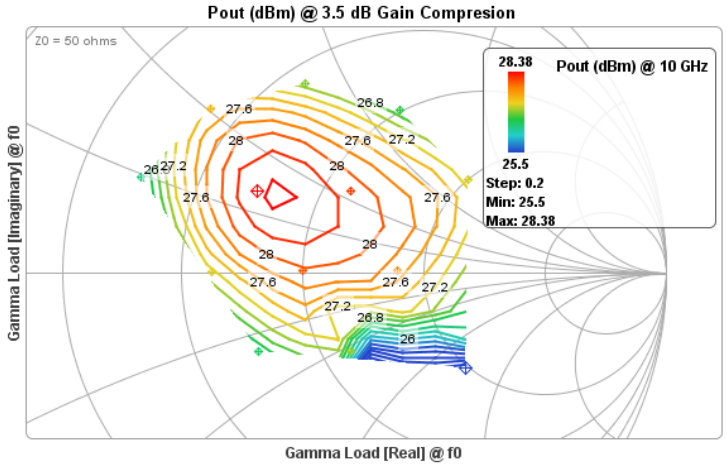


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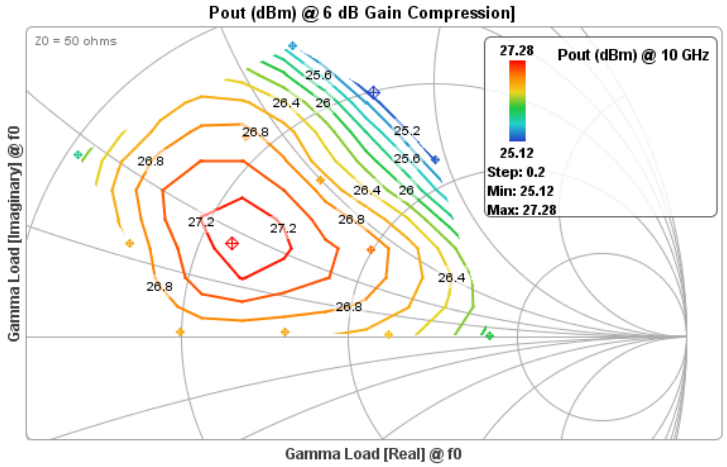
Figure 5.1: DC characteristics of un-gated HEMTs: (a) I_D–V_D for 3 µm and 2 µm drain-to-source separations; (b) r_D–I_D.

5.3 MMIC LNA Design using Un-gated HEMTs

HEMTs are the basic building block of microwave LNA MMIC. The performance of an MMIC is dependent upon the DC, small signal, and large signal parameters of the HEMT. Therefore, a careful selection of HEMTs is needed for the desired minimum noise figure (NF), gain, and (P_{out}) specifications. As output power is the focus of this study, it is pertinent to discuss the large signal performance of the HEMTs.



(a)

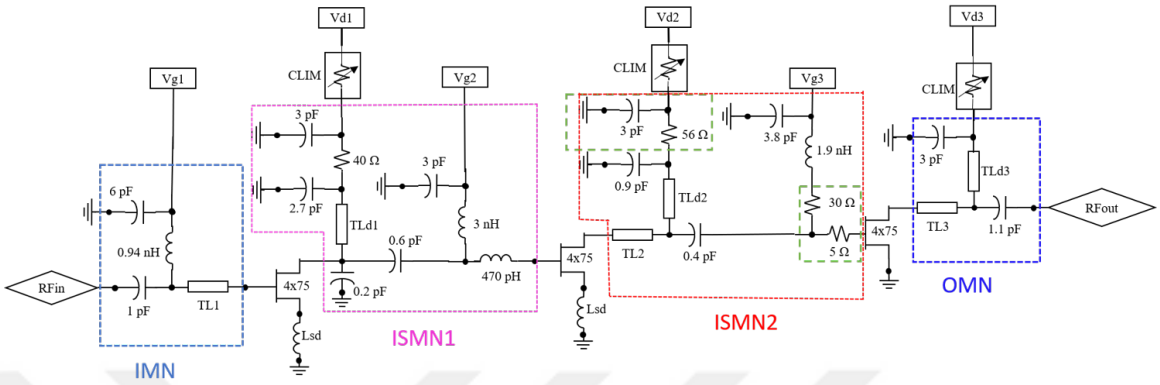


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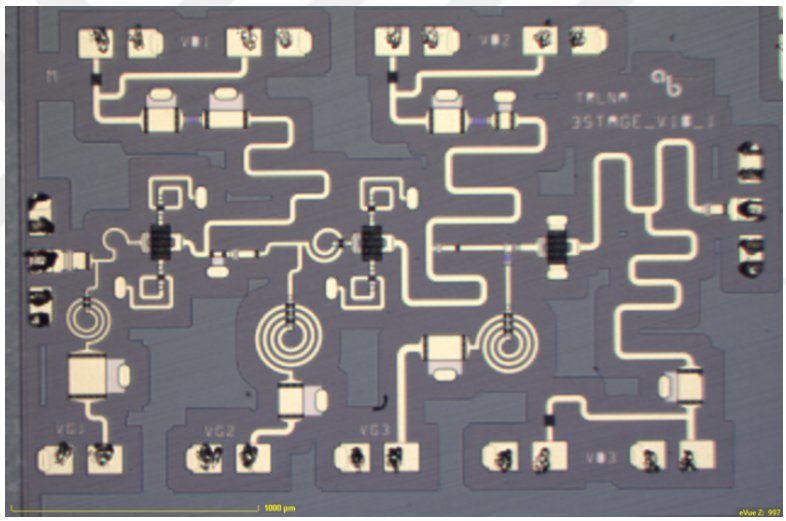
Figure 5.2: Load pull contours of LNA HEMTs; a) 4×75 µm source degenerated, b) 4×75 µm common source.

Figure 5.2 shows load pull contours of the 4×75 µm source degenerated (SD) and common source (CS) HEMTs, which are used in a 3-stage MMIC LNA under discussion. From the load pull contours of the HEMTs, it is evident that the maximum P_{out} of the SD HEMT is approximately 28.4 dBm and that of the CS HEMT is 27.3 dBm. P_{sat} of MMIC can be anticipated by the choice of the HEMT in the last stage.

We are incorporating un-gated HEMTs into our 3-stage LNA. The design of the LNA is discussed in Chapter 4, Section 4.2, which aimed to increase survivability and study the reverse recovery time as a function of the pulse width of the incoming signal. Briefly describing, the design consists of stability networks and four matching networks; input matching network (IMN), output matching network (OMN), and two interstage matching networks (ISMN1 & ISMN2). The IMN governs NF and input return loss (IRL), gain, and gain ripple are controlled by ISMN1/ISMN2, while OMN takes care of the output return loss (ORL) of the LNA. Stabilization of HEMTs is done using resistors and inductors on the drain side for the first two stages and on the gate side for the third stage to have minimum effect on overall NF. This study is focused on limiting the output saturated power of the LNA. For the purpose, the design is modified to include un-gated HEMTs (discussed in Section 5.2) at the drain side of the HEMT. From here onward, we will name un-gated HEMTs as current limiters (CLIMs) since these essentially limit drain currents. The CLIM is symbolized as a variable resistor in the schematic shown in Fig. 5.3. These are made selectable and added at the drain of each stage HEMT. The ohmic contact width for the CLIM is 35 µm. The CLIM at the last stage of LNA limits P_{sat}, while those at preceding stages prevent gate turn on [32, 46, 81] of the following stages.



(a)

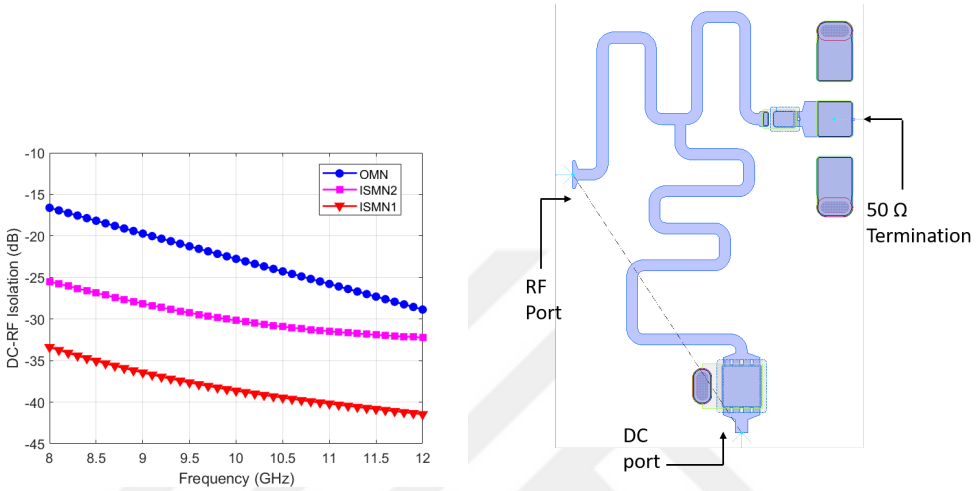


(b)

Figure 5.3: Implementation of un-gated HEMTs within three-stage LNA; a) schematic, b) layout.

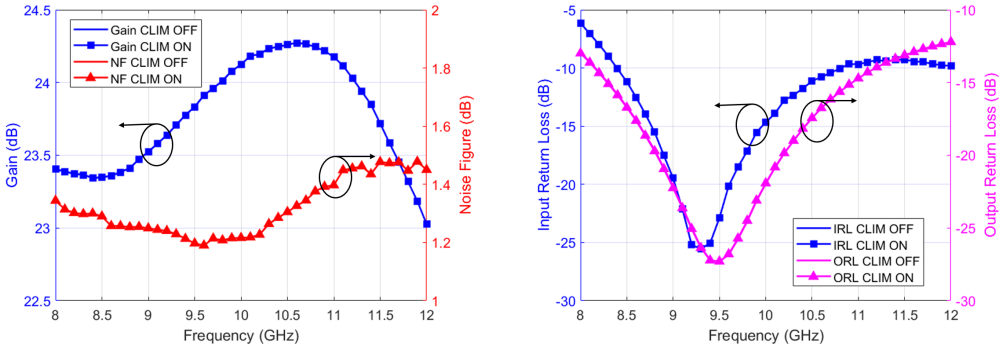
Small signal performance of LNA may degrade due to the addition of extra circuitry in the drain bias network of HEMTs. The DC–RF Isolation test is a good check to anticipate any change in performance. This test is performed by terminating all the ports of the matching network with 50 Ω and measuring forward/reverse transmission coefficient between HEMT's drain port and DC biasing port as shown in Fig. 5.4b for OMN. The same procedure is repeated for ISMN1 and ISMN2 as well. Figure 5.4a shows the DC–RF isolations for each network. OMN provides more than 17 dB isolation in the operating frequency

band. ISMN2 provides more than 25 dB isolation, and ISMN1 has more than 34 dB isolation.



(a) (b)

Figure 5.4: DC to RF Isolation test of LNA; a) isolation between each HEMT drain terminal and corresponding biasing pad for OMN, ISMN2 and ISMN1, b) example test schematic for OMN



(a) (b)

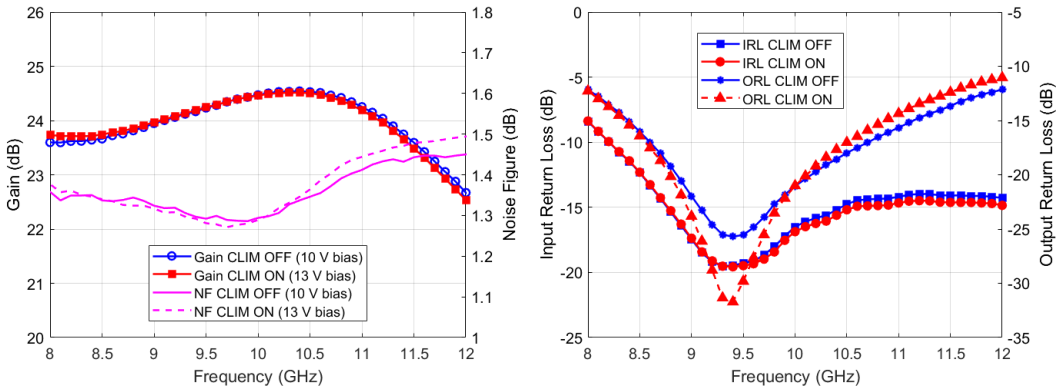
Figure 5.5: Simulated small signal and noise response of LNA with and without un-gated HEMTs; a) gain and NF, b) return losses.

Furthermore, the effect of CLIMs on LNA's small signal and noise response is simulated by adding on-resistances associated with these limiters. For 35 µm

HEMT, value of on-resistance is 100 Ω approx. as seen in Fig. 5.1b. No change is observed in NF and return losses of LNA with and without CLIMs as evident from Fig. 5.5.

5.4 Results and Discussions

The MMIC's overall size is 3 mm×1.8 mm. Small signal characterizations of MMIC are performed using Rohde & Schwarz ZVA-40 vector network analyzer. At first, S-parameter's response is recorded without engagement of CLIMs (as shown in Fig. 5.6) under a nominal operating bias of LNA of 10 V and 100 mA/mm.



(a) (b)

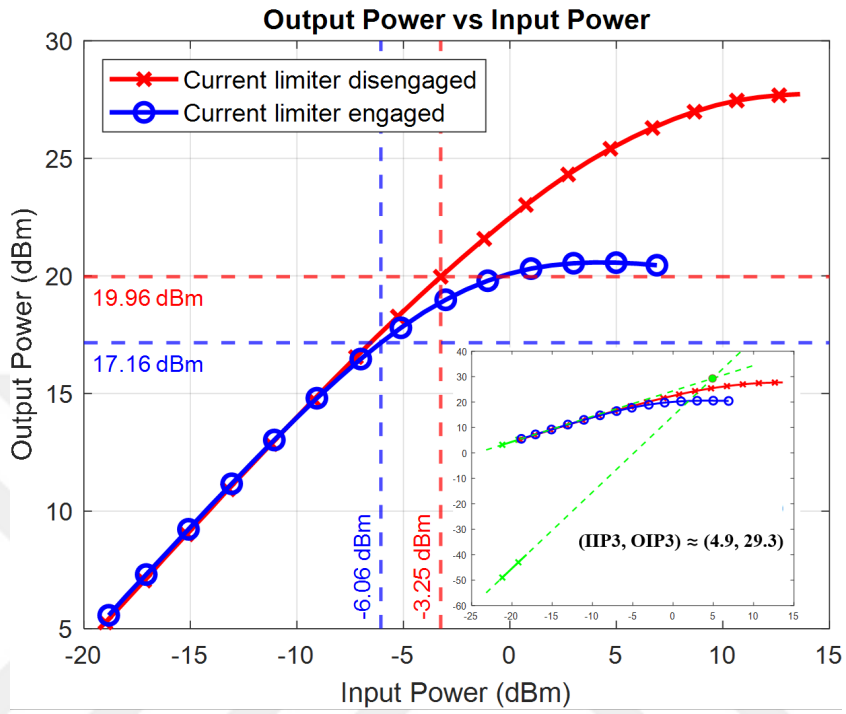
Figure 5.6: Measured small signal and noise response of LNA with and without un-gated HEMTs (at all three stages); a) gain and NF, b) return Losses.

Gain is above 22.5 dB, IRL is below 8 dB, and ORL is below 12 dB from 8 to 12 GHz frequency range. Secondly, CLIM is engaged only at the 3rd stage. The drop in gain and ORL degradation were observed. The performance degradation was due to the drop in bias voltage (below 10V) at the HEMT drain terminal, resulting from additional voltage drop across CLIM acting as a resistor. The drop in drain bias also changes intrinsic capacitances and resistances of the HEMT [82]. Therefore, the change in drain bias is compensated by increasing the voltage

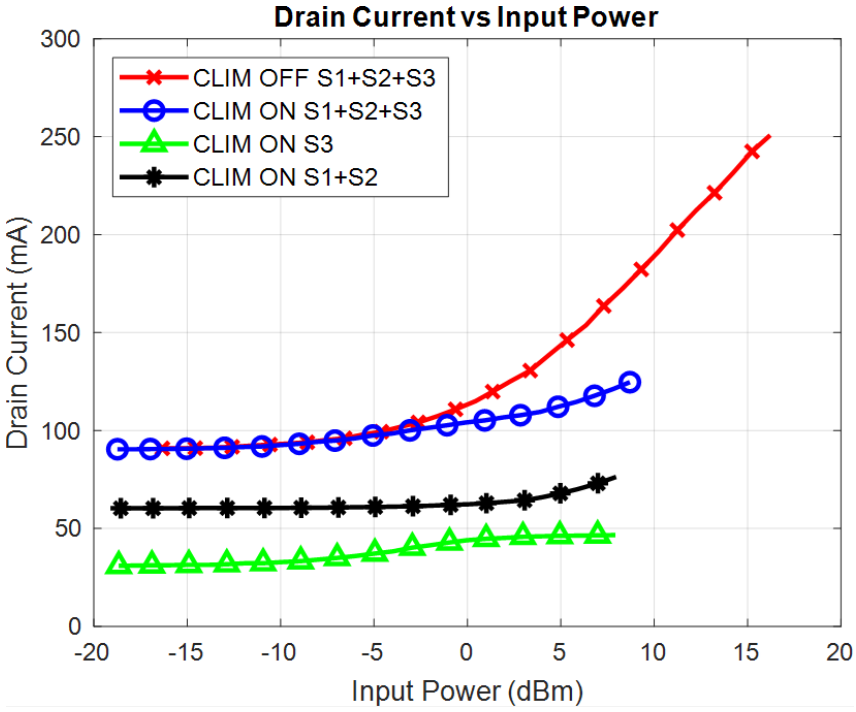
from the power supply. It is observed that a 3 V voltage increase from the supply provided the desired gain. Then, the MMIC response is measured by engaging CLIMs at all three stages. Results are shown in Fig. 5.6 under operating bias of 13 V (compensating voltage drop across limiters) and 100 mA/mm. While comparing the response with the CLIMs OFF case, it is observed that there is no significant change in gain and IRL. However, there is a minor change in ORL response in the mid-band and higher frequency end.

The noise figure of the MMIC LNA is also measured under CLIM ON and OFF conditions using a PNA-X N5244A network analyzer with an integrated noise receiver and a 346A noise source from Keysight Technologies. It is seen from Fig. 5.6a that NF almost remains the same with an insignificant increase at the higher frequency end. This validates our findings from schematic simulations as well.

Main feature of un-gated HEMTs in the drain bias lines of LNA is to limit its P_{sat}, and large signal measurements of the device provide a quantitative measure of this. Large signal measurements are performed simultaneously under CLIMs OFF and ON states in all stages. Results are shown in Fig. 5.7. LNA is saturating around 28 dBm, and the corresponding total drain current is 250 mA when CLIMs are not engaged. As CLIMs are engaged, P_{sat} drops around 20 dBm, and the corresponding total drain current is around 120 mA. The main reason for limiting P_{sat} value is the increase in resistance of CLIM as input power is increased, resulting in less drain voltage at HEMT and, hence less P_{out}. Using IVCAD pulsers from Maury Microwave corporation Inc., drain currents of last stage (S3) alone and drain currents of stage 2 (S2) and 3 (S3) are also recorded. It is found that the drain current of S3 limits around 45 mA, and those of S2 and S3 combined limit around 75 mA. It is to be mentioned that the nominal drain current of each of these stages is 30 mA. We have also measured stage-wise drain currents separately. The S3 limits the current more as it saturates early due to the increased power level at its input.



(a)



(b)

Figure 5.7: Large signal and linearity performance of LNA with and without CLIMs; a) P_{sat} and two-tone test, b) stage-by-stage drain currents.

Using un-gated HEMTs reduces P_{1dB} of the LNA due to a faster gain roll-off and increased drain resistance as a function of input power. The fundamental reason behind this is a drop in drain voltage below 10 V at the HEMT drain due to the increased drain-source resistance of the HEMT. Figure 5.7 shows that P_{1dB} of the LNA without CLIM is 20 dBm, while it reduces to 17 dBm with CLIM engaged. However, linearity of the LNA is not affected at all, and the OIP3 (output power at third-order intercept point) value comes out to be 29.3 dBm (shown as a subfigure in Fig. 5.7a). The primary reason is that the two-tone test is performed at relatively low power levels (-20 dBm) under small signal conditions. The resistance of ungated HEMT is minimal, and the device gain is almost linear. For the linearity check, two signals at 9.995 GHz and 10.005 GHz are combined using a microwave power combiner and provided to the LNA. The outputs, including fundamental tones and third-order products (9.985 GHz and 10.015 GHz), are recorded on the Keysight's spectrum analyzer.

It is to be mentioned that un-gated HEMT periphery plays an important role in limiting the P_{out}. In order to reduce the P_{sat} value below 20 dBm, HEMT periphery can be optimized and reduced further from the current 35 µm. The HEMT on-resistance is a function of the V_{knee} voltage, which depends upon the drain-source distance of the HEMT. This distance can also be reduced from 3 µm to 2 µm to reduce on-resistance of HEMT. The low on-resistance will ultimately result in a lower voltage drop across CLIM, and the operating voltage of the LNA can be reduced further from 13 V. Therefore, choosing an optimum HEMT periphery and layout is essential to obtain the desired P_{sat} as per the application.

5.5 Conclusion

This study proposes a novel un-gated HEMTs-based current limiter to limit the P_{sat} of GaN LNAs. The un-gated HEMTs are used on the drain lines of a 3-stage LNA. It is found with 35 µm HEMT periphery that P_{sat} is reduced to 20 dBm from the normal 28 dBm. There is no effect on the linearity of the LNA. However, its P_{1dB} is reduced by 2 dB. Also, noise figure and small signal parameters are

not degraded. The ungated HEMT size is extremely small and easily integrable without affecting the overall LNA chip size. The P_{sat} value can be further reduced by reducing the HEMT periphery. This study provides an alternative, more robust approach to RF designers for limiting output power and easy integration into systems.

Chapter 6

Design of High Efficiency GaN Power Amplifiers

6.1 Introduction

GaN-on-SiC HEMT technology is known for high power amplifier (HPA) designs due to its wide band gap and excellent thermal management. We have worked on the design of an X-band GaN HPA with particular focus on the power-added efficiency (PAE) along with gain and output power (P_{out}). PAE is the ratio of power delivered to the load minus power available from the source and DC power input to the device. The design process of HPA involves steps similar to those of an LNA design. In an LNA, the input matching network (IMN) is of prime focus and is matched for the source impedance, giving the optimum noise figure. In an HPA design, the focus is on the output matching network (OMN), which is matched for load impedance, providing optimum P_{out} and PAE. The desired specifications of the power amplifier (PA) are described in the Table 6.1. It operates in the frequency range of 8.5 – 11 GHz. The target PAE is 41 % with more than 43 dBm P_{out}.

Table 6.1: Specifications of GaN Power Amplifier

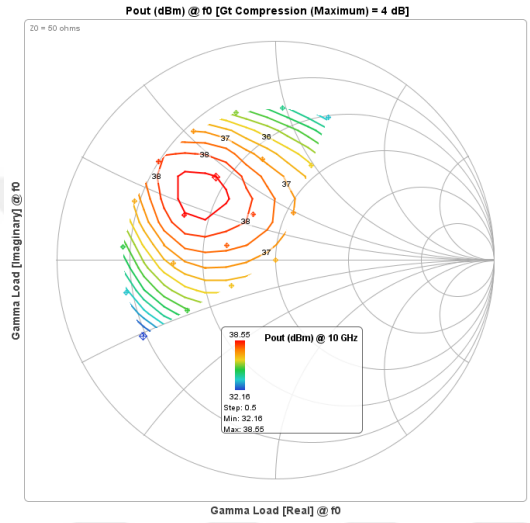
Parameter	**Unit**	**Value**
Frequency Range	GHz	8.5 - 11
Supply Voltage	V	28
$\mathbf{S_{11}}$	dB	< -12
$\mathbf{S_{22}}$	dB	< -8
Small Signal Gain	dB	> 34
Gain Ripple	dB	± 1
$\mathbf{P_{sat}}$	dBm	> 43
PAE	%	> 41

6.2 Design Topology

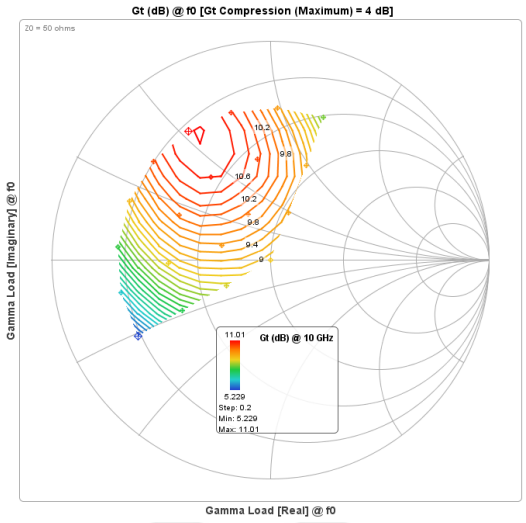
Power amplifier design begins with the selection of design topology. The design topology includes the total number of stages, gate peripheries of each stage, and an overall drive ratio. The periphery of the output stage determines the total P_{out} based on the output power density (P_d) of the foundry process. NANOTAM's 0.25 µm X-band process has 5.6 W/mm P_d [83]. Considering the OMN loss, the gate periphery of the output stage is computed by dividing the desired P_{out} with P_d. For 43 dBm P_{out}, the periphery of the output stage should be between 4.5 – 5 mm. Therefore, four HEMTs having a total of 4800µm periphery should be enough. Based on the gain, the amplifier design is three-stage since a two-stage design will not be enough to reach the desired goal. The amplifier is designed using two approaches; Approach 1 utilizes 10×125 µm HEMTs in the output stage, while approach 2 makes use of 2×6×100 µm HEMTs at the last stage. The topology for approach 1 is 1:1:4 and utilizes one HEMT at the middle and first stages. On the other hand, the topology for approach 2 is 2:2:4, and it utilizes two HEMTs at each subsequent stage. For simplicity, the design for Approach 1 will be described only since the methodology is the same for both approaches.

The design topology highly depends upon the careful selection of the GaN

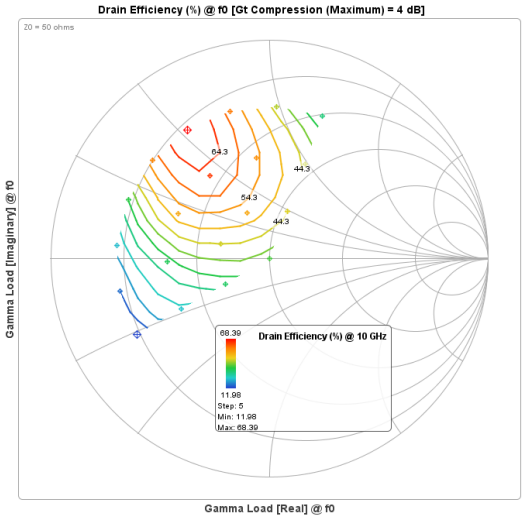
HEMTs. GaN HEMTs are characterized by their large signal and small signal performances. The vector network analyzer (VNA) based load pull setups discussed in chapter 2 provide drain efficiency (DE), transducer power gain (G_t and P_{out} contours. These measurements are typically done on-copper carrier under pulsed conditions to minimize heating effects. Figure 6.1 shows the large signal results of chosen 10×125 µm HEMT for the output stage. The results are measured at 28 V, 100 mA/mm bias, 80°C ambient, and 10 % duty cycle conditions. The HEMT can deliver maximum of 38.5 dBm P_{out}, 11 dB G_t, and 68.4 % DE at 10 GHz and 4-dB gain compression.



(a) contours for output power



(b) contours for gain

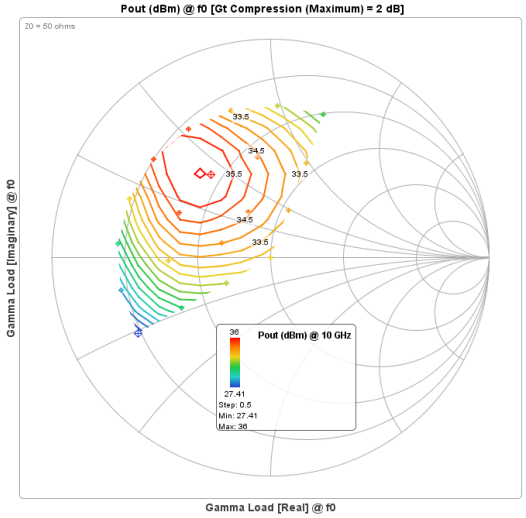


(c) contours for drain efficiency

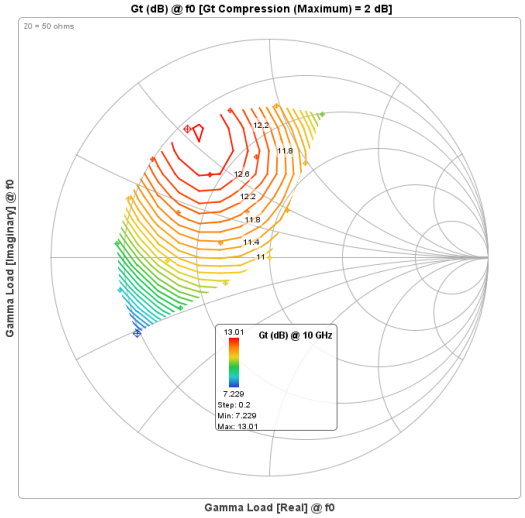
Figure 6.1: Load pull measurements of 10×125 µm HEMT at 10 GHz and 4-dB gain compression.

The load impedance (Z_L) values for maximum P_{out} and DE are 22.3 + 21.5j and 11.5 + 26.4j, respectively at 10 GHz. The difference in load impedances is due to the non-linear characteristics of the HEMTs. We have chosen $Z_L = 19 + 25j$ as optimum impedance point for both P_{out} and DE, and the source impedance point is $Z_S = 10 + 5j$. The impedance points for the start and end of the frequency band are shown in Table 6.2.

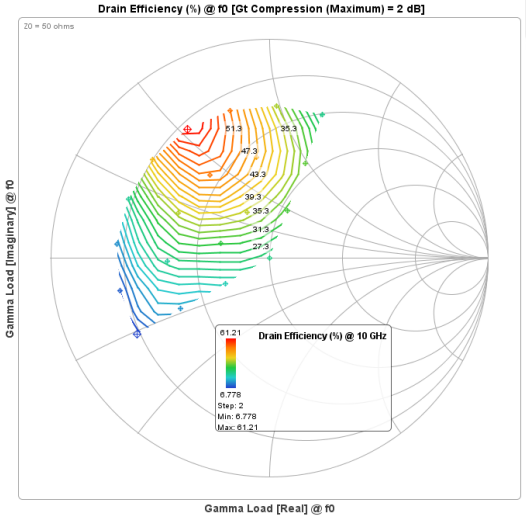
The middle stage has to drive the last stage without compromising P_{out} and PAE. The HEMT should deliver 27.5 dBm power to the following HEMTs at minimum based on G_t. However, stability and power splitting networks at the second inter-stage introduce significant losses. Considering 2.5 dB loss, the chosen HEMT should be able to deliver 36 dBm P_{out}. We have chosen one 10×125 µm HEMT for this stage. It can deliver 36 dBm P_{out}, 13 dB G_t, and 61.2 % DE at 10 GHz and 2-dB gain compression as shown in Fig. 6.2. Since the same HEMT is chosen as for the output stage, optimum load impedance values are also the same.



(a) contours for output power



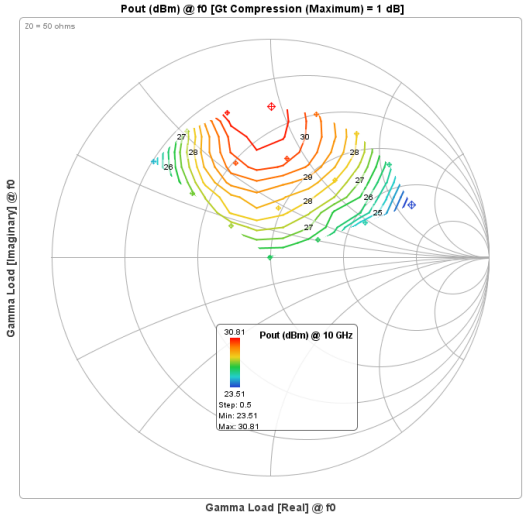
(b) contours for gain



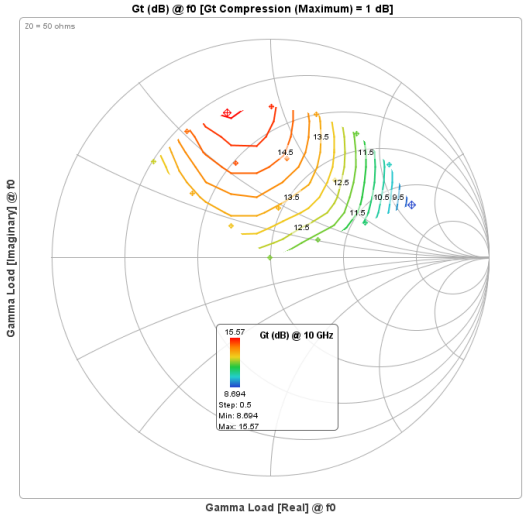
(c) contours for drain efficiency

Figure 6.2: Load pull measurements of 10×125 µm HEMT at 10 GHz and 2-dB gain compression.

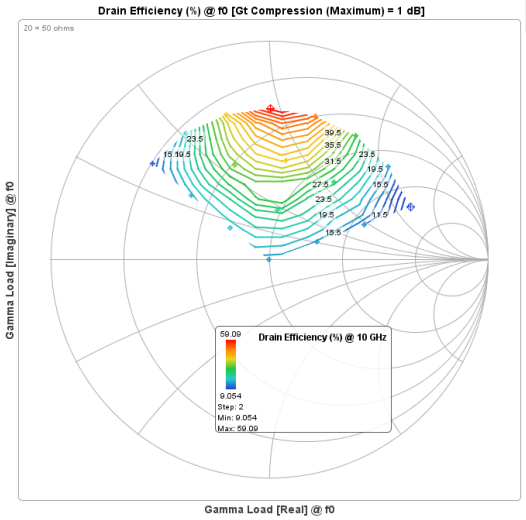
The first stage is a low power stage and has to provide about 26 dBm power to the middle stage, considering 3 dB loss at the first inter-stage network. Therefore, a small 6×75 µm HEMT periphery would be enough. This HEMT can deliver 30.8 dBm P_{out}, 15.5 dB G_t, and 59 % DE at 10 GHz and 1-dB gain compression as shown in Fig. 6.3. We have chosen $Z_L = 18 + 48j$ and $Z_S = 10 + 5j$.



(a) contours for output power



(b) contours for gain



(c) contours for drain efficiency

Figure 6.3: Load pull measurements of 6×75 µm HEMT at 10 GHz and 1-dB gain compression.

The same procedure is repeated for 8.5 and 11 GHz to cover the entire frequency band of interest. Table 6.2 shows all the selected optimum load impedances that will be used to design the matching networks in Section 6.4.

Table 6.2: Optimal Impedances for each HEMT of proposed PA

HEMT	**Frequency**	$Z_{\mathbf{S}}$	$Z_{\mathbf{L}}$
10×125 µm	8.5 GHz	10 + 9j	20 + 29j
	10 GHz	10 + 5j	19 + 25j
	11 GHz	10 + 3j	18 + 21j
6×75 µm	8.5 GHz	10 + 8j	20 + 53j
	10 GHz	10 + 12j	17 + 54j
	11 GHz	10 + 14j	18 + 49j

Figure 6.4 shows the design topology and signal flow diagram for the proposed X-band PA. The periphery of the output stage is 5 mm, where four 10×125 µm HEMTs are combined in parallel. The middle and first stages comprise a single HEMT with 1.25 mm and 0.45 mm peripheries. The overall drive ratio is 1:2.8:11. The assumed matching losses for output, second inter-stage, first inter-stage, and input networks are 0.7 dB, 2.5 dB, 3 dB, and 3.5 dB, respectively. At 10 GHz, the overall expected P_{out} is 43.8 dBm with 14 dBm P_{in} and 7-dB gain compression. The corresponding values for small and large signal gains are 30 dB and 37 dB, respectively.

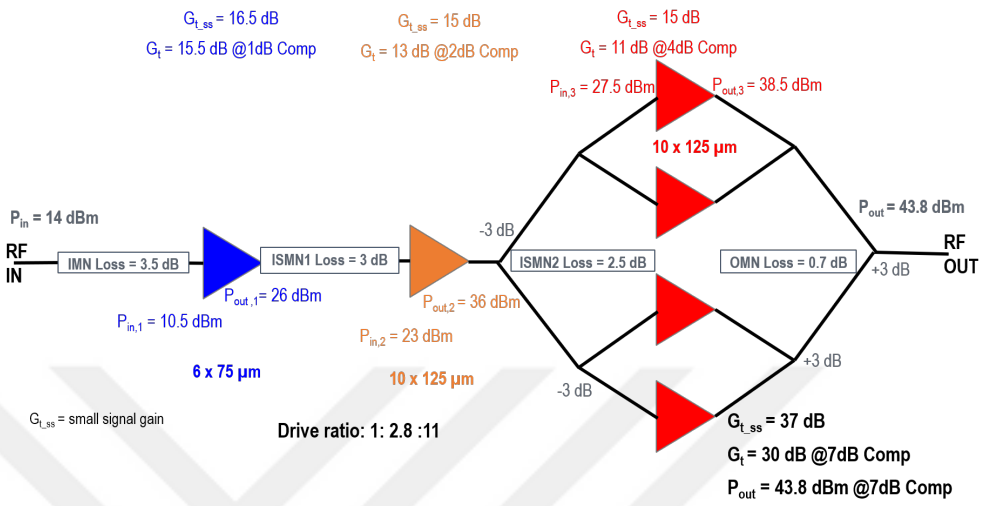


Figure 6.4: Power amplifier design topology and signal flow.

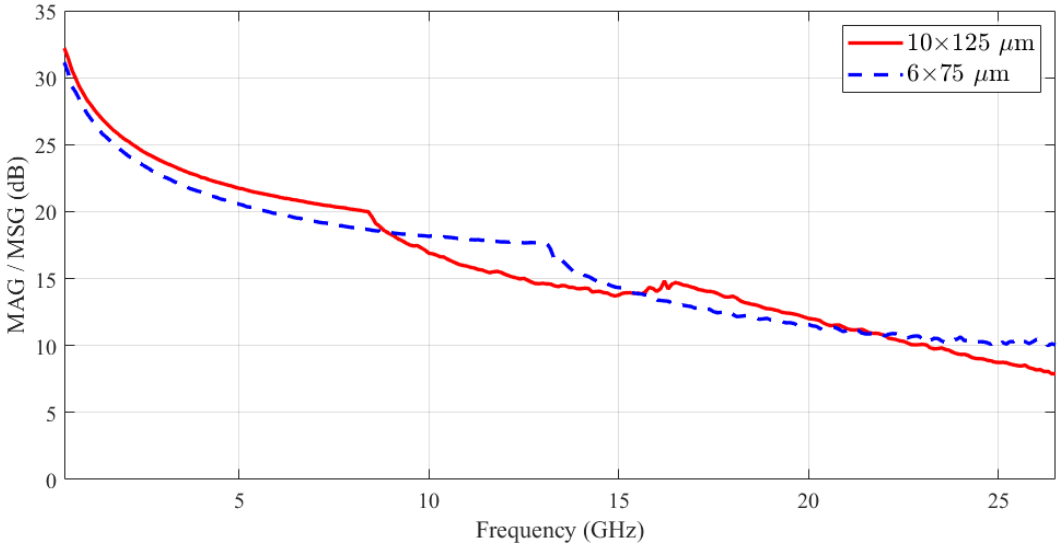


Figure 6.5: Maximum gain of HEMTs for proposed PA.

Small signal performances of GaN HEMTs are measured using the pulsed RF system. Figure 6.5 shows that maximum stable gain (MSG) of 6×75 µm HEMT is 18 dB at 10 GHz. For 10×125 µm HEMT, the maximum available gain (MAG) is 16.9 dB. These measurements are also performed under 10 % duty cycle pulse conditions.

6.3 Stabilization of HEMTs

Stabilization of HEMTs is the second step in a PA design. This is important to prevent unwanted oscillations that could damage the device and measurement equipment. HEMT must be unconditionally stabilized per Rollet's stability criteria discussed in Chapter 2. According to the criteria, stability factor K should be > 1 to achieve stability for any load or source reflection coefficients within the unit circle Smith chart.

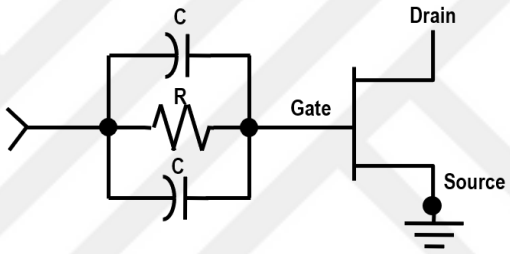
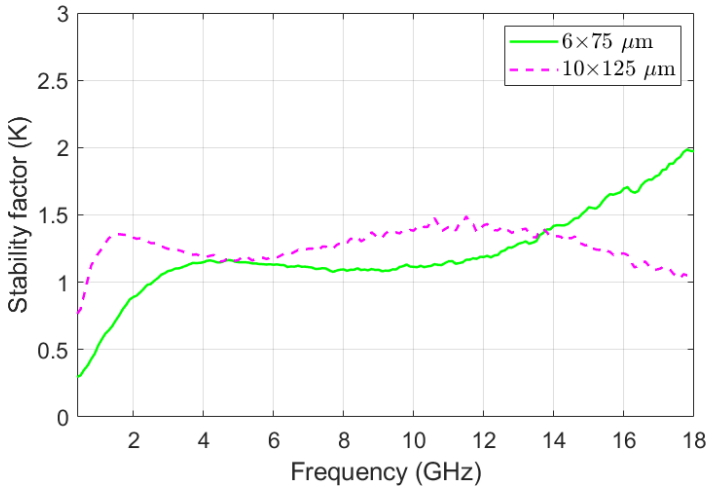


Figure 6.6: Stability network topology for HEMTs.

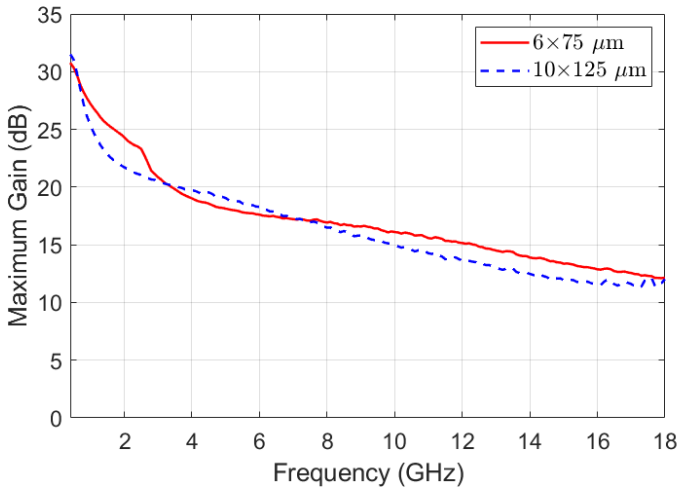
We have used parallel RC networks to stabilize the HEMTs at all stages. The block diagram of the network is shown in Fig. 6.6. The series capacitor is divided into two for symmetric RF signal flow. This network is limited to providing even mode stability. The even mode stability considers that all the parallel HEMTs are excited with the same amplitude and phase. For achieving odd mode stability, odd mode resistors are added between parallel transistors (discussed later in Section 6.5). The stability network is inherently lossy, leading to a reduction in gain at the oscillation frequencies. The series resistor mainly reduces the gain, and series capacitors bypass the resistor within the operating frequency band to cause low in-band loss from the network. In HPAs, the preservation of P_{out} from HEMT is critical. Therefore, stability networks are added on the gate side of the HEMT instead of the drain side to avoid unnecessary power loss. The drop in power on the drain side leads to poor PAE and driving issues in the middle stages.

Figure 6.7 shows the stability factor and maximum gain of HEMTs after the parallel RC stability network. The first stage 6×75 µm HEMT is unconditionally

stabilized from 2.6 GHz to 18 GHz, and it has 16 dB MAG at 10 GHz. The middle and last stage 10×125 µm HEMT is unconditionally stabilized from 0.7 GHz to 18 GHz, and it has 15 dB MAG at 10 GHz after stabilization. There is a 2 dB reduction in MAG after stabilization for both the HEMTs. The stabilization at the low frequencies is obtained from the biasing networks and losses of the matching networks.



(a)



(b)

Figure 6.7: (a) Stability factor, and (b) maximum gain of HEMTs after stability networks

6.4 Design of Impedance Matching Networks

After stabilization, matching networks are designed per the HEMTs' optimum load and source impedances shown in Table 6.2. Since PA is a three-stage design, it has four different impedance matching networks, the design of which is described in this section.

6.4.1 Output Matching Network

The design of an output matching network (OMN) is very crucial because P_{out} and PAE performance of PA is primarily based on this network. The target load impedances are to be matched very closely. Figure 6.8 shows the block diagram for OMN. The network consists of a 4:1 impedance transformer. The conventional reactive matching technique based on transmission lines and metal-insulator-metal (MIM) capacitors is used to translate desired load impedances to 50 Ω.

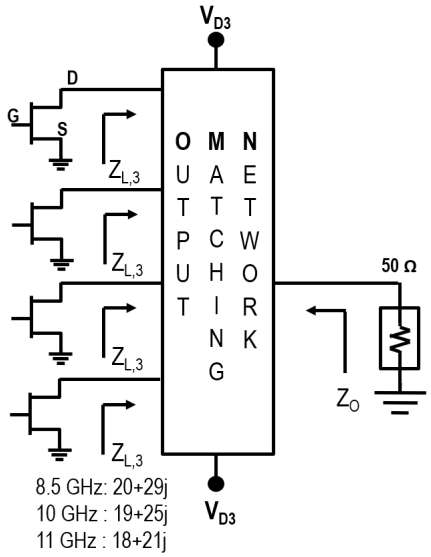
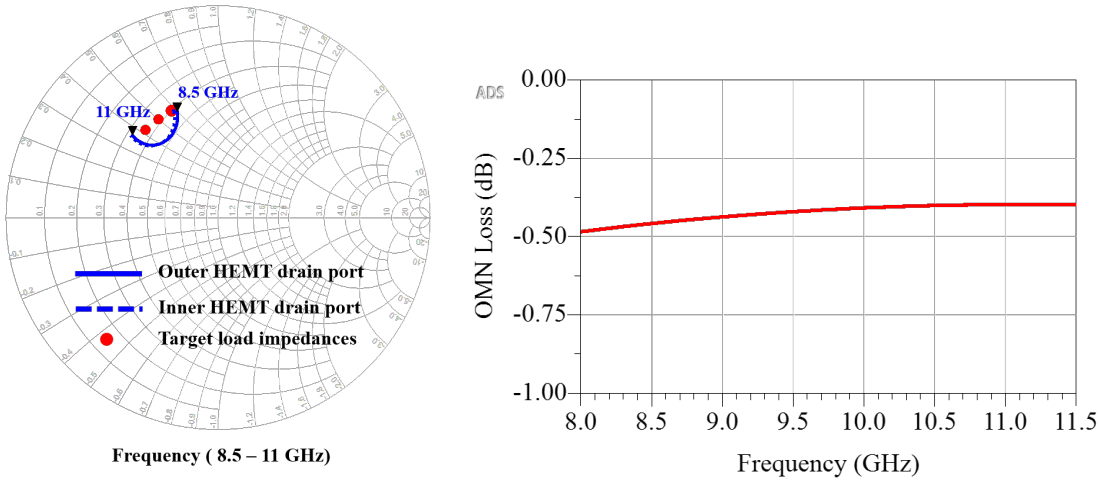


Figure 6.8: Block diagram for output matching network.

A corporate structure power combining methodology [84] is used to combine power from four HEMTs. The combining efficiency of the power combiner

depends on two factors: matching network loss and mismatch of amplitude and phase between combining ports. The electrical symmetry of the network helps to reduce amplitude and phase imbalance. Maintaining physical symmetry along the horizontal line adds to achieving electrical symmetry. In order to observe the symmetry, reflection coefficients are monitored at the outer and inner ports of the combiner. Figure 6.9a shows the impedance looking from the drain of the 10×125 µm HEMT in the final stage. It can be seen that impedance responses from inner and outer ports overlap each other due to the physical symmetry of the network. The achieved load impedances from EM simulations are quite close to the target impedances. The DC biasing network consisting of a narrow transmission line acting as an RF choke, and the MIM bypass capacitor is made part of the matching network for compact design. Figure 6.9b shows the simulated matching network loss. The overall loss is < 0.5 dB in the operating frequency range of 8.5 GHz to 11 GHz, and it is below our 0.7 dB estimate in the preliminary link budget.



(a) (b)

Figure 6.9: (a) Impedance looking from the drain of 10×125 µm HEMT in the final stage, and (b) loss of output matching network

6.4.2 Inter-stage Matching Network 2

The second inter-stage matching network (ISMN2) comes between the gate side of 3rd stage HEMTs and the drain side of 2nd stage HEMT. Therefore, it matches the source and load impedances of both sides. Figure 6.10 shows the block diagram of ISMN2. It is hard to obtain this match simultaneously. A perfect match to load impedance provides optimum power, while a mismatch to source impedance causes a gain reduction.

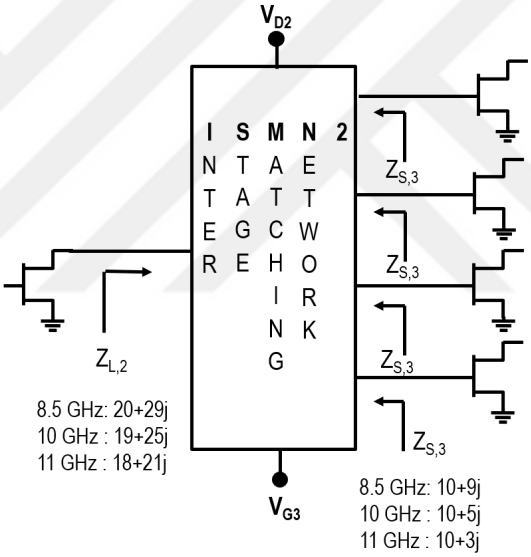
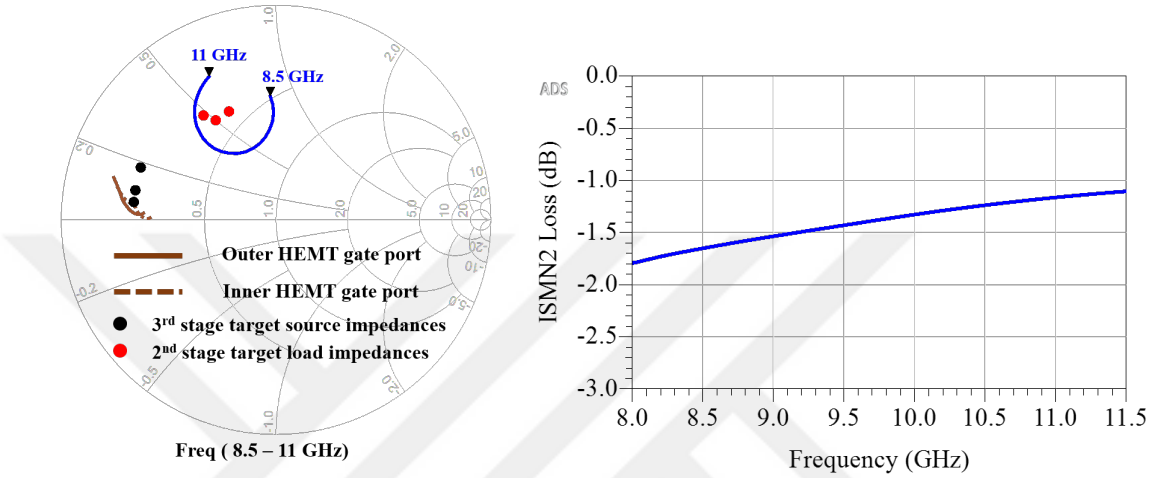


Figure 6.10: Block diagram for second inter-stage matching network.

The ISMN2 consists of a 1:4 impedance transformer. Similar to OMN, physical symmetry along the horizontal line is maintained to have minimal amplitude & phase mismatch to have better electrical symmetry. The reflection coefficients of the outer and inner ports of the divider are observed to check symmetry. Figure 6.11a shows the impedance looking from the gate of the 10×125 µm HEMT in the final stage and drain of the 10×125 µm HEMT in the 2nd stage. It is seen that impedance responses from the inner and outer ports on the gate side overlap each other. The load impedance curve from EM simulations surrounds the target load impedances. The source impedance curve is also close to the target source impedances. Figure 6.11b shows the simulated matching network loss. The overall

loss is < 1.7 dB in the operating frequency range of 8.5 GHz to 11 GHz, which is below our 2.5 dB estimate in the preliminary link budget.



(a) (b)

Figure 6.11: (a) Impedance looking from the gate of 10×125 µm HEMT in the final stage and drain of 10×125 µm HEMT in the 2nd stage, and (b) loss of second inter-stage matching network

6.4.3 Inter-stage Matching Network 1

The first inter-stage matching network (ISMN1) comes between the gate side of 2nd stage HEMT and the drain side of 1st stage HEMT. Therefore, it matches the source and load impedances of both side's HEMTs. Figure 6.12 shows the block diagram of ISMN1. The primary focus of this network is to provide desired power to 2nd stage, while the secondary focus is to control gain ripple. Source impedances are intentionally kept off from target ones to control gain ripple.

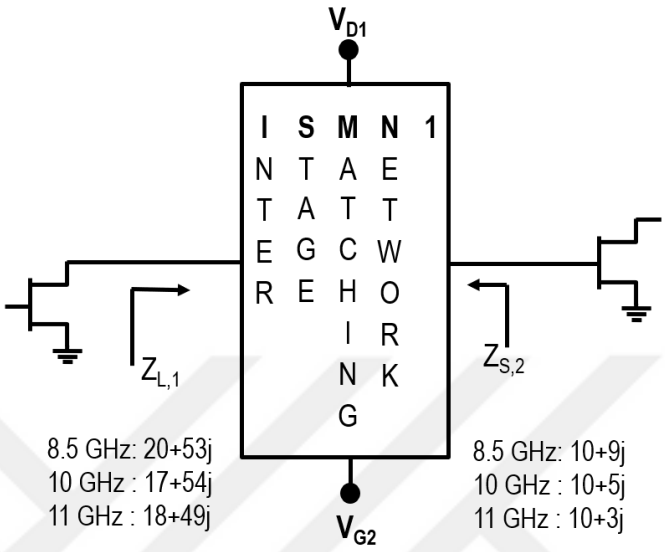
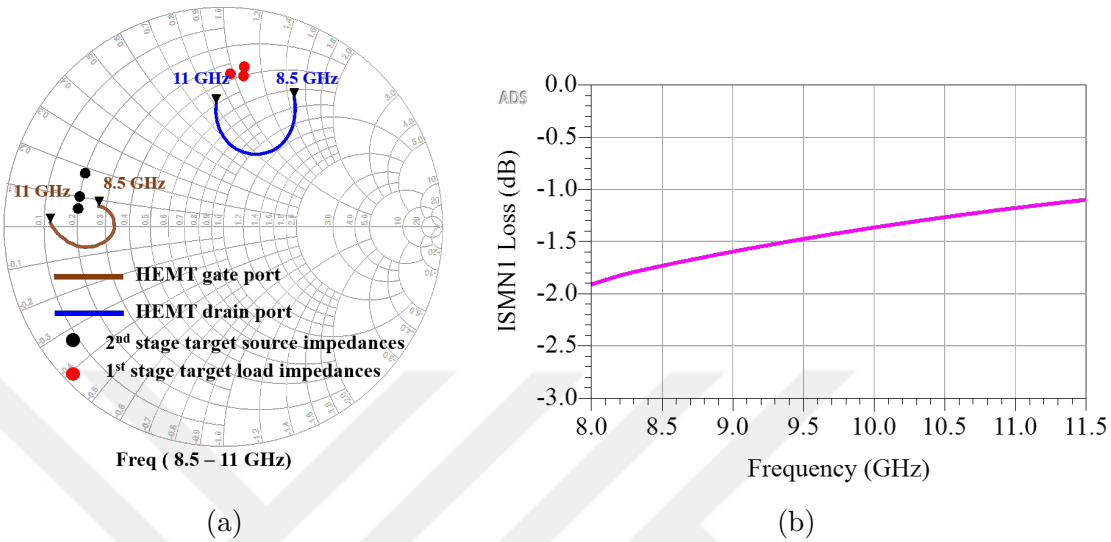


Figure 6.12: Block diagram for first inter-stage matching network.

The ISMN1 consists of a 1:1 impedance transformer since there are single HEMTs on both sides. Figure 6.13a shows the impedance looking from the gate of the 10×125 µm HEMT in the 2nd stage and drain of the 6×75 µm HEMT in the 1st stage. The load impedance curve from EM simulations is a bit away from the target ones. However, HEMT still provides the desired power (verified from measurement data using AMCAD Engineering's IVCAD tool) to the following stage. The source impedance curve is also slightly mismatched from the target source impedances for gain ripple. Figure 6.13b shows the simulated matching network loss. The overall loss is < 1.8 dB in the operating frequency range of 8.5 GHz to 11 GHz, which is below our 3.0 dB estimate in the preliminary link budget.



(a) (b)

Figure 6.13: (a) Impedance looking from the gate of 10×125 µm HEMT in the 2nd and drain of 6×75 µm HEMT in the 1st stage, and (b) loss of first inter-stage matching network

6.4.4 Input Matching Network

The input matching network (IMN), as the name suggests, comes between the gate side of 1st stage HEMT and RF Input. It matches the source impedance of the HEMT to 50 Ω. Figure 6.14 shows the block diagram of IMN. This network provides desired S_{11} and controls the amplifier's gain and gain ripple. For maximum gain and better S_{11}, the source impedance is made conjugate of the input impedance of the HEMT.

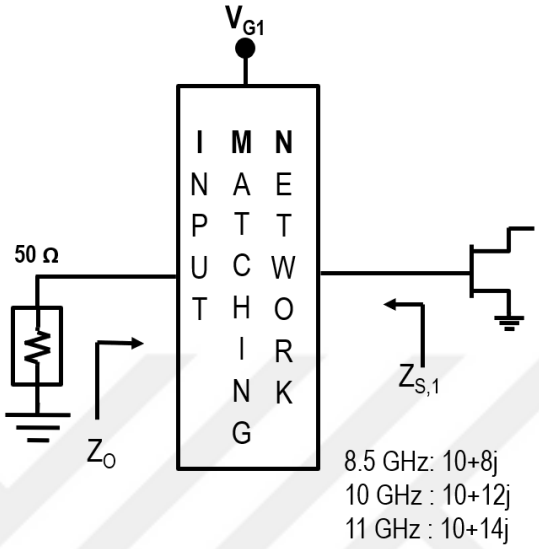
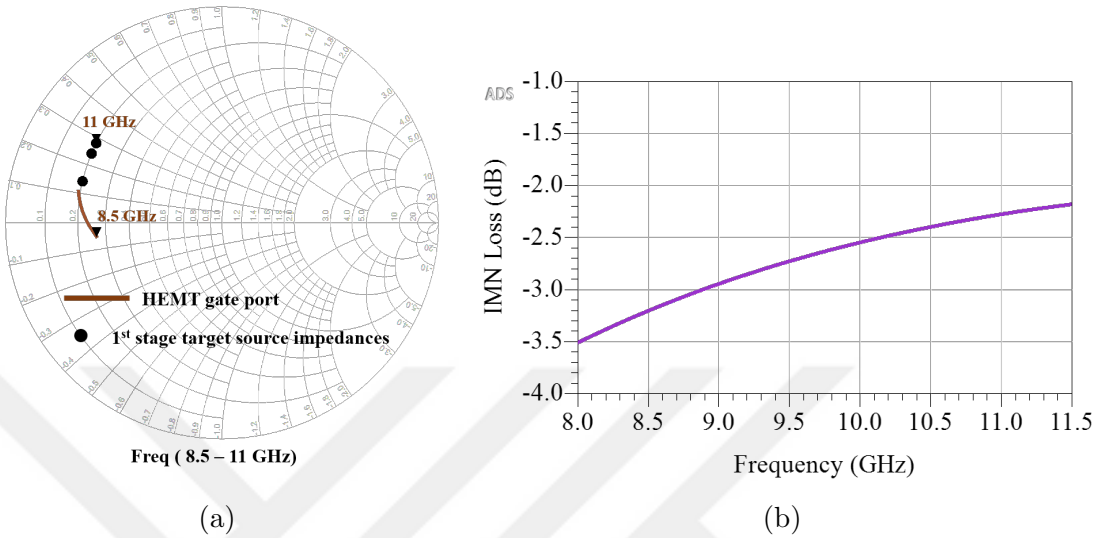


Figure 6.14: Block diagram for input matching network.

Just like ISMN1, IMN also consists of a 1:1 impedance transformer. It contains only gate bias of 1st stage HEMT, so only one DC biasing network. Figure 6.15a shows the impedance looking from the gate of the 6×75 µm HEMT at its gate terminal. The source impedance curve from EM simulations is intentionally kept off for gain ripple control. From the matching network loss as shown in Fig. 6.15b, it is evident that loss decreases with an increase in frequency. The loss at 8.5 GHz is 3.2 dB and 2.2 dB at 11 GHz. The fundamental reason for keeping higher loss at lower frequencies is the higher MAG of HEMT at lower frequencies and reducing the gain ripple. The overall loss in the operating frequency range of 8.5 GHz to 11 GHz is below our 3.5 dB estimate in the preliminary link budget.



(a) (b)

Figure 6.15: (a) Impedance looking from the gate of 6×75 µm HEMT in the 1st stage, and (b) loss of input matching network

6.5 MMIC Schematic and Layout Design

All the individually designed matching networks are combined, and small signal response of the complete amplifier is observed. The source impedances of the matching networks in the first and intermediate stages are adjusted to tune the gain, gain ripple, and S_{11}. Gain and S_{11} are tuned from IMN, while gain ripple is controlled from ISMN1 and ISMN2. The additional resistor on the gate bias line helps in stabilization and tuning the gain ripple. Figure 6.16 shows the schematic of the whole PA MMIC. The component details for each matching network can be seen. The drain bias of the last stage has two ports, one on the top and the other on the bottom, to have uniform current distribution along the drains. Similarly, gate bias for the last stage also has two ports, which allows uniform voltage distribution along the gates. These biasing arrangements affect the thermal distribution and the overall performance of the MMIC. The other stages contain single HEMTs; therefore, they have single ports for gate and drain lines.

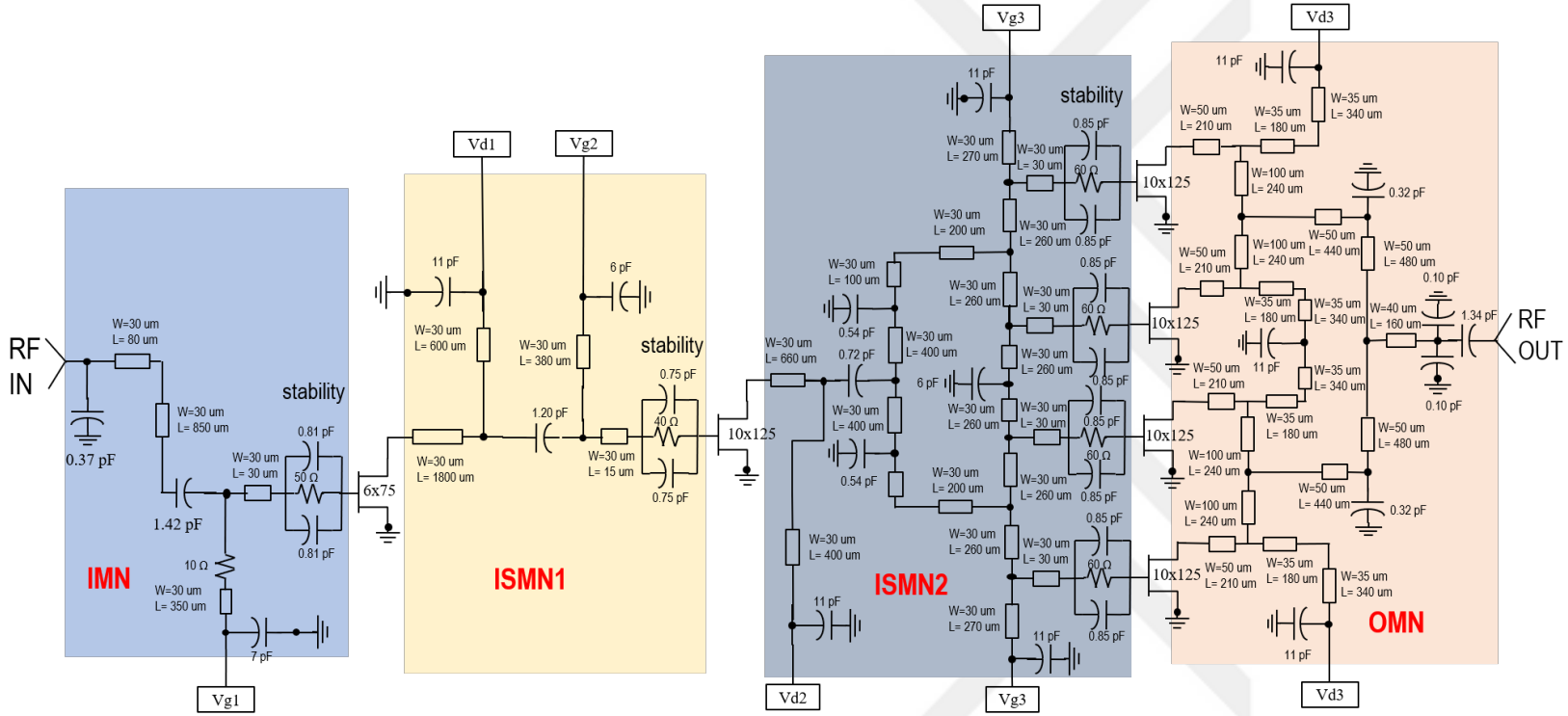


Figure 6.16: PA MMIC Schematic (rotated vertically).

Before finalizing the design, additional checks are performed on the MMIC to ensure proper functionality in the actual operating scenario. These include DC-RF isolation and stability checks. DC probes have specific resistance in the range of 0.1 Ω to 100 Ω. Poor DC-RF isolation may result in increased gain ripple within the frequency band. Therefore, the DC-RF Isolation test is performed on each bias line by terminating it with a lumped resistor. The value of the resistor is varied to see any change in the S-parameter response of the amplifier. In the present case, DC-RF isolation is improved by adding additional 20 - 30 Ω resistors on gate bias lines and 4 - 5 pF capacitances on drain bias lines after the bypass capacitor in the DC biasing network.

The stability checks of the MMIC include even mode and odd mode oscillations tests. The oscillations can distort the signal and cause a loss of output power. The reason for oscillations could be either positive feedback due to external components around HEMTs or coupling between nearby lines. For even mode stability, there is an oscillation condition to satisfy at each node, however, it is sufficient to check the condition near the active devices. This test is important because the HEMTs in the design were not unconditionally stable at the lower frequencies. The oscillation condition is as follows [46, 85]:

1. The real part of the sum of the impedance looking to the left and right of the gate/drain node of the HEMT must be negative:

$$Real(Z_L + Z_R) < 0 \tag{6.1}$$

2. The imaginary part of the sum of impedance looking to the left and right of the gate/drain node of the HEMT must be zero:

$$Imag(Z_L + Z_R) = 0 \tag{6.2}$$

3. The partial derivative of the left side of (6.2) with respect to frequency must be positive:

$$\frac{\partial Imag(Z_L + Z_R)}{\partial f} > 0 \tag{6.3}$$

All these equations should be satisfied simultaneously for oscillations to occur. If (6.1) is true at some frequency, then there must be a zero crossing for (6.2) with a positive slope. This condition takes care of any oscillation due to the series impedance; however, to check for oscillation due to any shunt impedance, Z_L and Z_R can be replaced with admittances Y_L and Y_R looking to left and right of any node of the HEMT in the above equations.

The S-probe tool in ADS is used to check the oscillation conditions. The tool checks the impedance/admittance to its left and right. This tool is placed on the gate and drain sides of each HEMT in the design, as shown in Fig. 6.17.

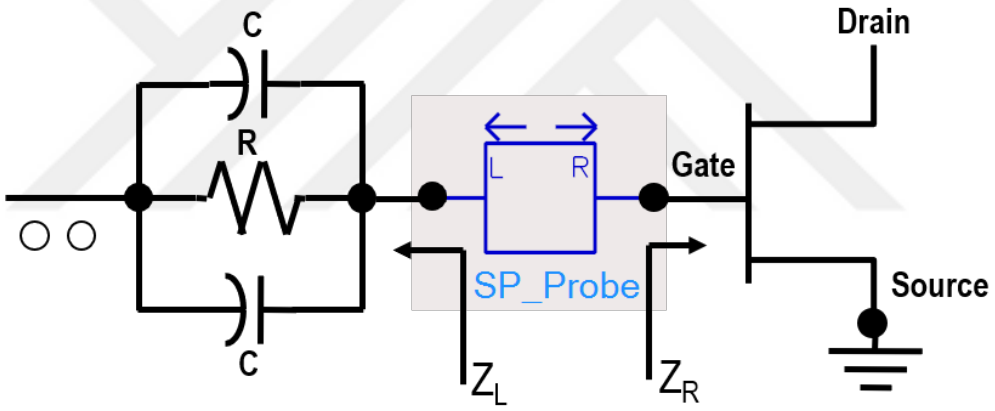
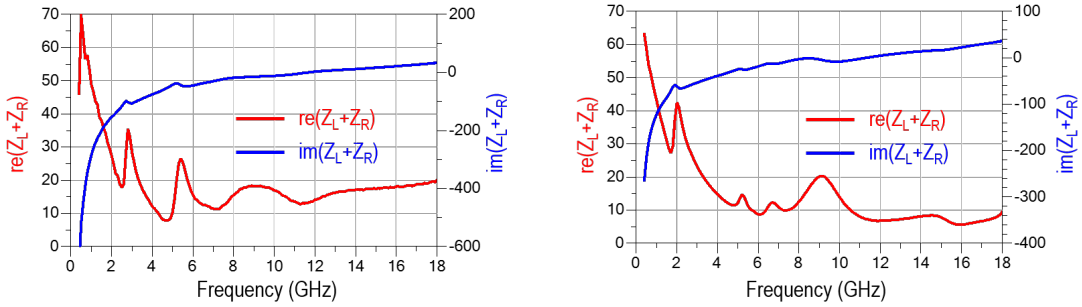


Figure 6.17: Even mode stability test example schematic for one node.

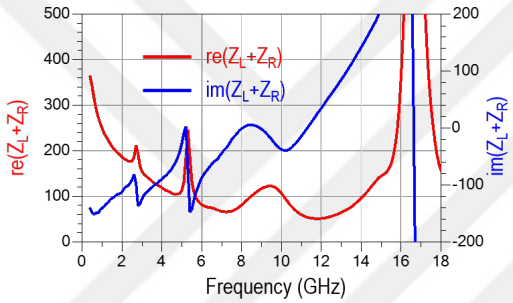
Figure 6.18 shows even mode stability impedance test results performed at all stages' gate and drain nodes of HEMTs. For the last stage, the test is performed for all four parallel HEMTs; however, only outer and inner HEMTs from the top side are shown due to symmetry. The real part of the sum of the impedance looking to the left and right of the gate/drain nodes is positive for all the HEMTs. Therefore, oscillation condition (6.1) is not satisfied. Similarly, an admittance test is also performed (not shown), and no oscillation condition was found to be met.

Moreover, there are four parallel HEMTs in the last stage. Any amplitude and phase mismatch due to fabrication variations or slight electrical asymmetry in power combining and dividing ports may lead to oscillations [86]. The parallel HEMTs create a multi-loop system, and there is a need to reduce these loop gains.

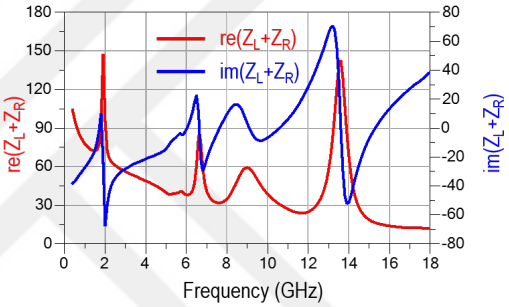


(a) first stage gate

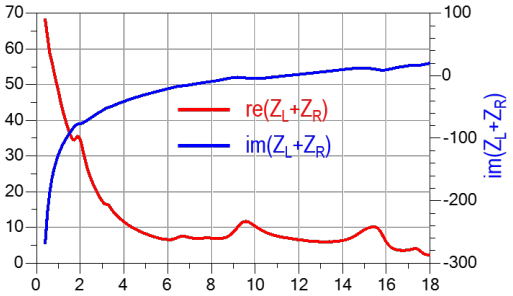
(b) first stage drain



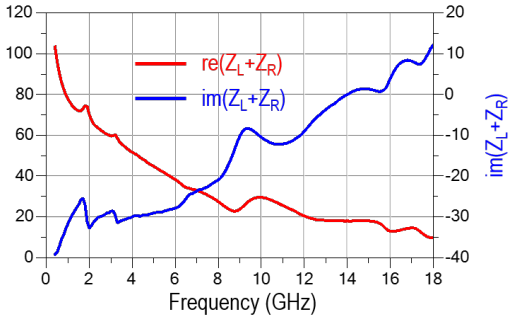
(c) second stage gate



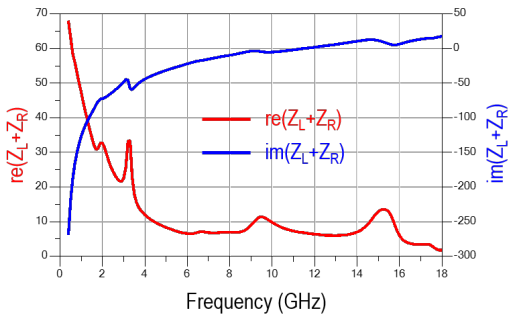
(d) second stage Drain



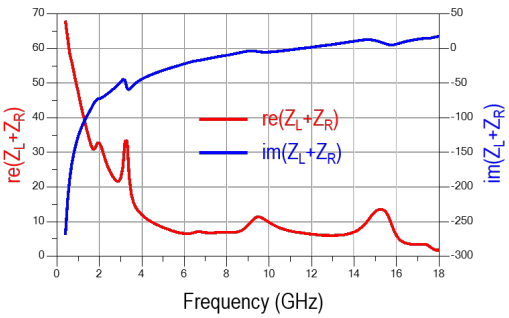
(e) last stage outer HEMT gate



(f) last stage outer HEMT drain



(g) last stage inner HEMT gate



(h) last stage inner HEMT drain

Figure 6.18: Even mode stability test plots for gate and drain nodes of each stage HEMT.

The Freitag method [83, 85] considers these loops and suggests adding odd mode resistors between the parallel HEMTs. The value of these resistors is determined as 50 Ω from the odd mode stability analysis. The MMIC design is proceeded further after these even and odd mode stability checks.

Figure 6.19 shows the layout of the tape-out ready form of the MMIC amplifier. The double metal transmission line structure is utilized in the output matching network for reliable operation and to handle high device currents. MET1 handles 4 mA/µm and MET2 handles 16 mA/µm, therefore a double metal transmission line can allow 20 mA/µm to pass through it. For other networks, the MET2 structure for transmission lines is used. The DC biasing pads are re-arranged to maintain 600 µm pitch. The overall size of the MMIC is 3.75 mm × 2.4 mm.

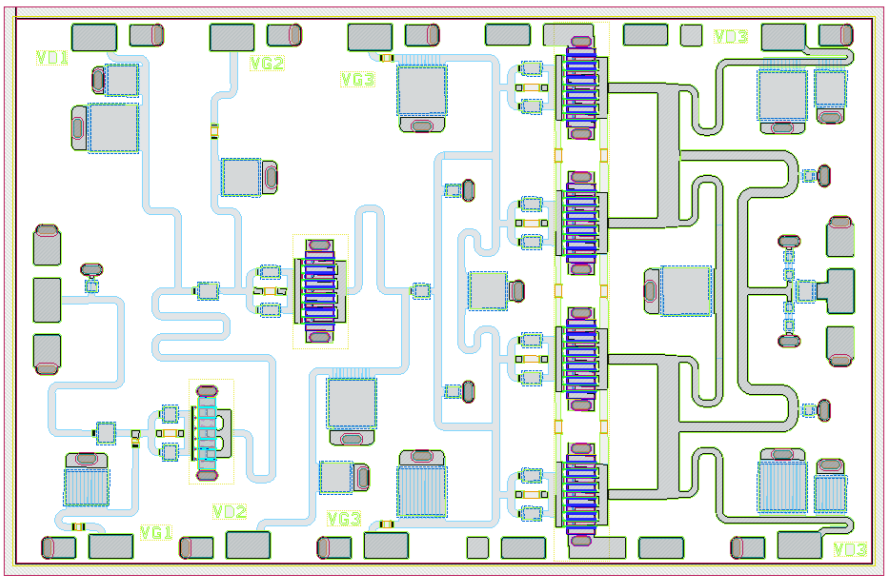


Figure 6.19: MMIC layout for approach 1 PA.

6.5.1 Design Approach 2

The design topology in approach 1 is 1:1:4, having an overall drive ratio of 1:2.8:11. In approach 2, the design topology is changed to 2:2:4, and the overall drive ratio is 1:1.7:4 as shown in Fig. 6.20. In this approach, the output periphery

is 4.8 mm (previous 5.0 mm), where four 2×6×100 µm HEMTs are arranged in parallel. The periphery for second stage is 2 mm (previous 1.25 mm), where two 8×125 µm HEMTs are used. The driver stage periphery is 1.2 mm (previous 0.45 mm), where also 8×75 µm HEMTs are utilized. This approach can provide more power to final stage HEMTs than approach 1 since it has a larger gate periphery between the second inter-stage and final stage.

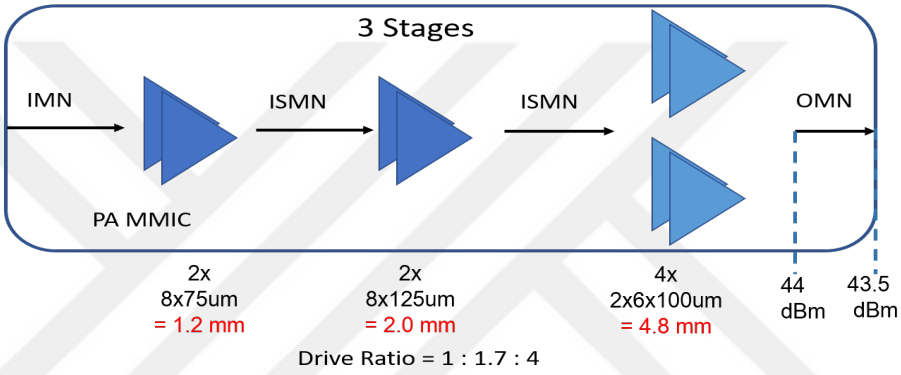


Figure 6.20: Design topology for approach 2 PA.

The same design procedure is adopted as in the design of approach 1 PA MMIC. At first, OMN is designed for target load impedances, and then intermediate stages networks are designed. Finally, IMN is designed. The impedance transformer architecture for ISMN2 is 2:4, 1:1 architecture for ISMN1, and 1:2 architecture for IMN networks. Figure 6.21 shows the layout of the complete amplifier with approach 2. The overall MMIC size is kept the same for both design approaches.

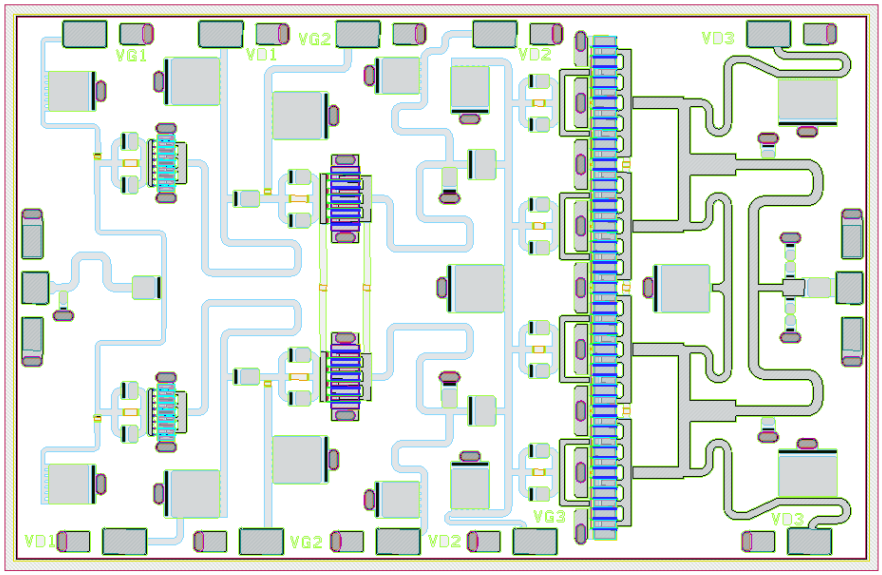
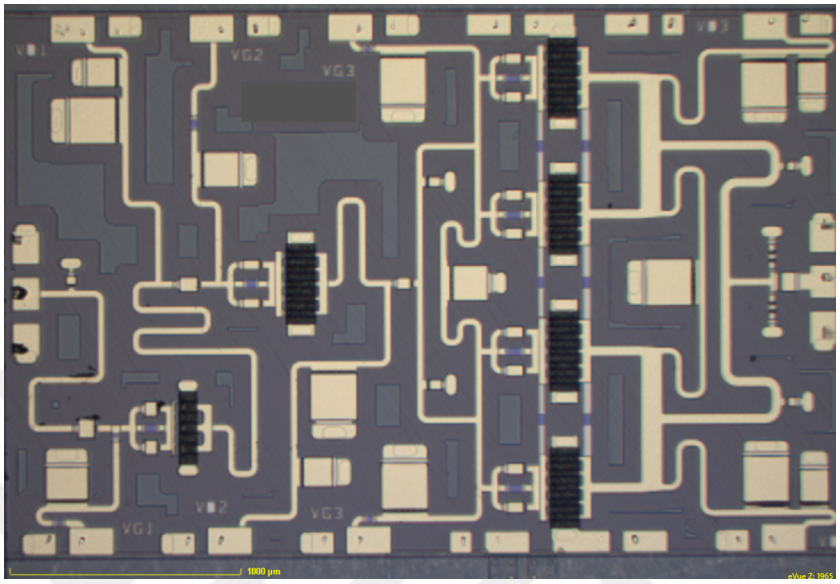


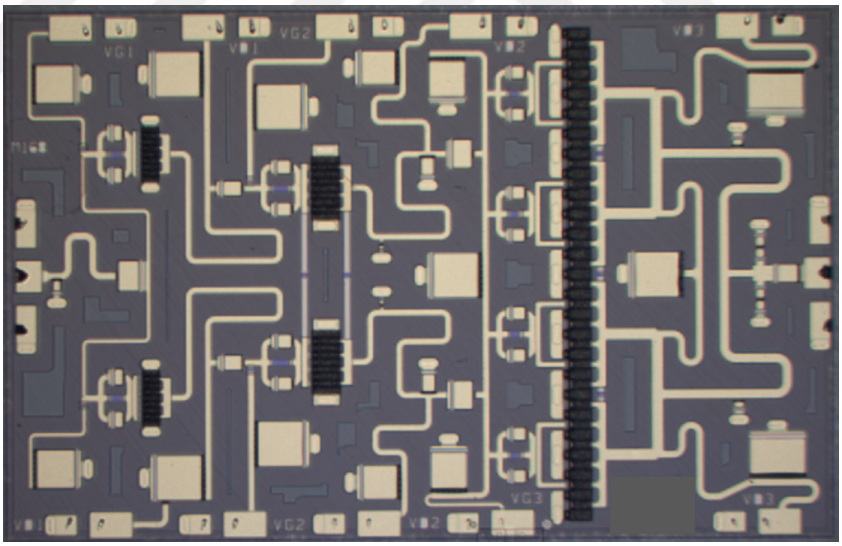
Figure 6.21: PA MMIC layout (design approach 2).

6.6 Simulation and Measurement Results

The amplifiers from the two approaches are fabricated using NAONTAM's in-house 0.25 µm GaN fabrication facility. Figure 6.22 shows micro-photographs of the fabricated MMICs. The measurements of the MMICs are performed on the wafers with 25°C chuck temperature and quiescent bias point of 28 V, 100 mA/mm under pulsed conditions. The pulse duty cycle is kept at 10 % for drain bias, gate bias, and RF input signal.



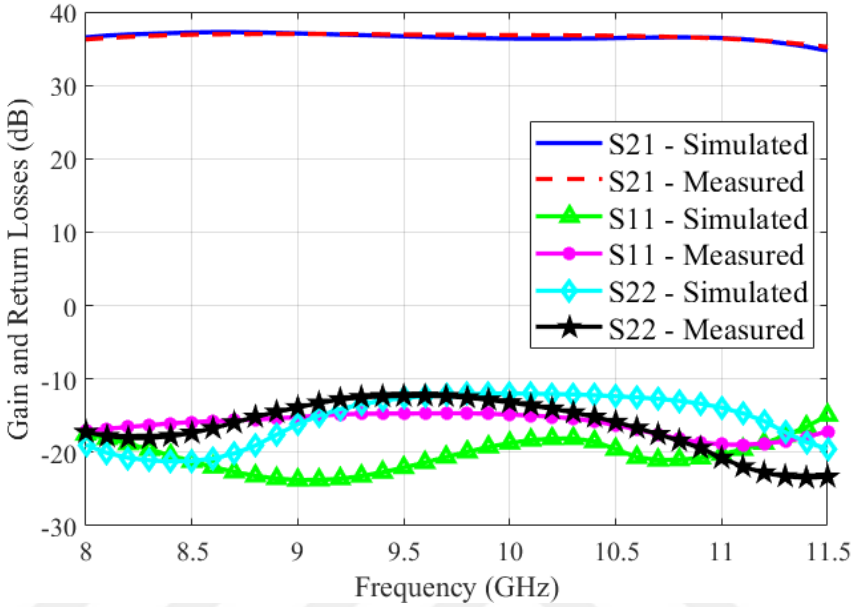
(a) Approach 1



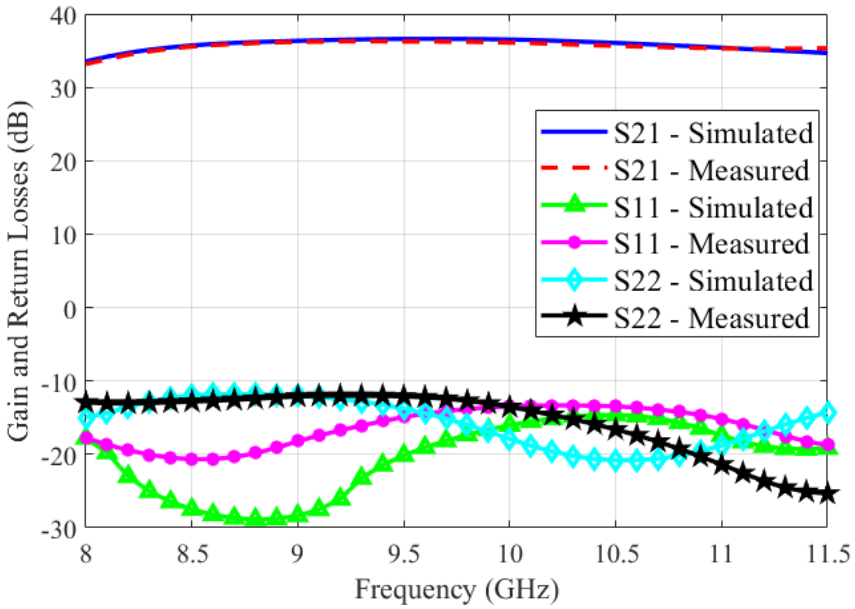
(b) Approach 2

Figure 6.22: Microphotographs of fabricated PA MMICs.

Figure 6.23 shows the simulated and measured small signal performance of the MMIC amplifiers from both design approaches. From Fig. 6.23a, the measured gain of approach 1 amplifier is 36.4 dB to 37 dB in the frequency range of 8.5 - 11 GHz, resulting in ±0.3 dB gain ripple. The corresponding simulated gain of the amplifier is 36.4 dB to 37.2 dB with ±0.4 dB gain ripple. The measured



(a) Approach 1



(b) Approach 2

Figure 6.23: MMIC simulated and on-wafer measured small signal results for two approaches under 10 % duty cycle pulse condition and 28 V, 100 mA/mm at 25°C ambient.

input reflection and output reflection coefficients are lower than -14.7 dB and -13.4 dB, respectively, while the corresponding simulated values are lower than -18 dB and -12 dB.

Similarly, from Fig. 6.23b, the measured gain of approach 2 amplifier is 35.3 dB to 36.3 dB in the frequency range of 8.5 - 11 GHz, resulting in ±0.5 dB gain ripple. The corresponding simulated gain of the amplifier is 35.4 dB to 36.6 dB with ±0.6 dB gain ripple. The measured input reflection and output reflection coefficients are higher than -13.4 dB and -12 dB, respectively, while the corresponding simulated values are higher than -14.6 dB and -11.8 dB.

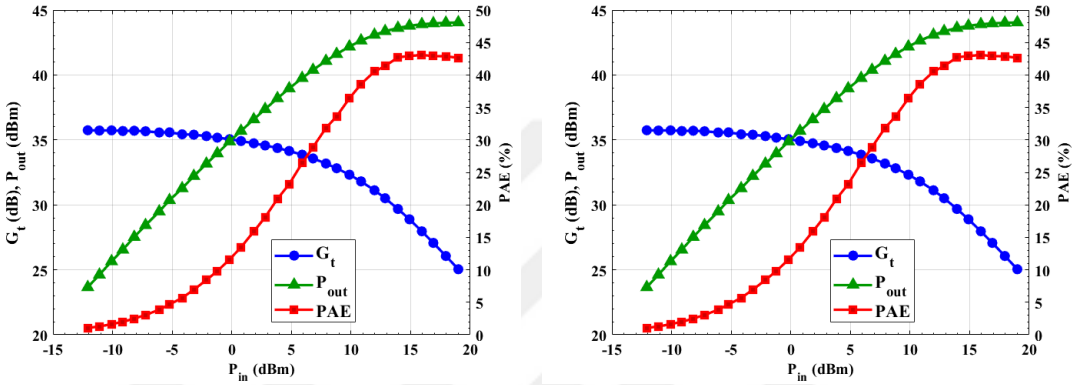
In general, the simulated and measured results of the two amplifier versions agree with each other. Minor insignificant differences in the magnitudes of the parameters can be attributed to the change in passive component values due to fabrication tolerances. The measured results satisfy all small signal requirements, as highlighted in Table 6.3.

Table 6.3: Simulated and on-wafer measured small signal results of the MMIC PA

Parameter	**Unit**	**Specification**	**Design Approach 1**		**Design Approach 2**	
			Simulated	**Measured**	**Simulated**	**Measured**
$\mathbf{S_{11}}$	dB	< -12	< -18.1	< -14.7	< -14.6	< -13.4
$\mathbf{S_{22}}$	dB	< -8	< -12.0	< -12.3	< -11.8	< -12
Small Signal Gain	dB	> 34	> 36.4	> 36.4	> 35.4	> 35.3
Gain Ripple	dB	± 1	± 0.4	± 0.3	± 0.6	± 0.5

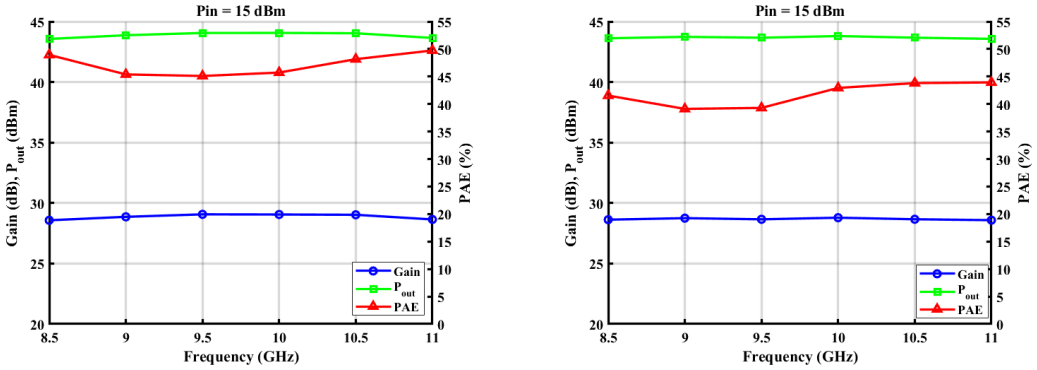
The large signal measurements are performed using load pull setup discussed in Chapter 2 by setting load and source tuners impedance as 50 Ω. MMIC's gain, P_{out}, and PAE parameters are measured as a function of power available from the source at the frequency of interest one at a time. Figure 6.25 shows the performance of the MMIC from two versions at 10 GHz. Both designs provide more than 41 % PAE; however, approach 1 provides comparatively higher peak efficiency than approach 2. The peak PAE achieved from approach 1 is 45.8 %, while from approach 2, it is 43 %. The peak efficiency is observed at 7-dB

and 7.7-dB gain compressions for approach 1 and approach 2, respectively. The saturated output power of approach 1 is 44.2 dBm, which is 0.2 dB higher than that achieved from approach 2. The large signal gains at low input power levels from both designs are close to each other.



(a) Approach 1 load pull (b) Approach 2 load pull

Figure 6.24: Large signal on-wafer measurements for two approaches under 10% duty cycle pulse condition, 28 V, 100 mA/mm quiescent bias, 25°C ambient and 10 GHz frequency.



(a) Approach 1 (b) Approach 2

Figure 6.25: Large signal on-wafer measurements for two approaches under 10% duty cycle pulse condition, 28 V, 100 mA/mm quiescent bias, 25°C ambient, and 15 dBm fixed input power from source.

The large signal measurements are also performed at other in-band frequencies as well. Both designs provide optimum PAE at 15 dBm input power available

from the source. Figure 6.25 shows the performances of both variants of MMIC in the frequency range of 8.5 to 11 GHz. The PAE values recorded from approach 1 are 45.1 % to 49.7 %; the lowest value is in the middle of the band (at 9.5 GHz), while the highest is at the upper end of the band (11 GHz). On the other hand, PAE values recorded from approach 2 are 39.1 % to 43.9 %, and the lowest and highest values are recorded at the middle and upper end of the frequency band as of approach 1. The gain from both approaches is between 28.6 to 29 dB, and output powers are between 43.56 to 44 dBm, with approach 1 having higher power levels overall. These results are shown in tabular form in Table 6.4.

Table 6.4: Large signal on-wafer performance of the MMIC PA at 25°C ambient

Frequency	**Design Approach 1**			**Design Approach 2**		
(GHz)	$\mathbf{G_t}$ **(dB)**	$\mathbf{P_{out}}$ **(dBm)**	**PAE (%)**	$\mathbf{G_t}$ **(dB)**	$\mathbf{P_{out}}$ **(dBm)**	**PAE (%)**
8.5	28.6	43.56	48.9	28.6	43.61	41.5
9.0	28.9	43.87	45.4	28.7	43.74	39.1
9.5	29.0	44.06	45.1	28.7	43.66	39.3
10	29.0	44.06	45.7	28.8	43.80	42.9
10.5	29.0	44.03	48.1	28.6	43.67	43.8
11	28.6	43.64	49.7	28.6	43.57	43.9

Finally, the small and large signal results achieved from the two design approaches are compared with the target specifications of the power amplifier. It is evident from Table 6.5 that PA with approach 2 satisfies all the requirements except PAE. On the other hand, PA with approach 1 meets all the specifications

Table 6.5: Power amplifier approach 1 and approach 2 results comparison with specifications

	Unit	**Value**	**Approach 2**	**Approach 1**
Frequency Range	GHz	8.5 - 11	8.5 - 11	8.5 - 11
Supply Voltage	V	28	28	28
$\mathbf{S_{11}}$	dB	< -12	-13.4	-14.7
$\mathbf{S_{22}}$	dB	< -8	-12	-12.3
Small Signal Gain	dB	> 35	35.3	36.4
Gain Ripple	dB	± 1	± 0.5	± 0.3
$\mathbf{P_{sat}}$	dBm	> 43	43.56	43.61
PAE	%	> 41	39.1	45.1

including PAE. The fundamental difference between the two approaches is the total gate periphery. The gate periphery for approach 1 is 6.7 mm, including all the HEMTs, and for approach 2, it is 8 mm. It is to be mentioned that the gate periphery of the output stage is not compromised; rather, it is 0.2 mm higher than that of approach 1. The total gate periphery is reduced by the number of HEMTs and changing HEMT sizes in the first and middle stages. The dissipated power is directly proportional to the gate periphery; the lower the periphery, the lower the dissipation power. The overall PAE is improved by 6 % by reducing the total gate periphery. Therefore, reducing the gate peripheries helps improve PAE.

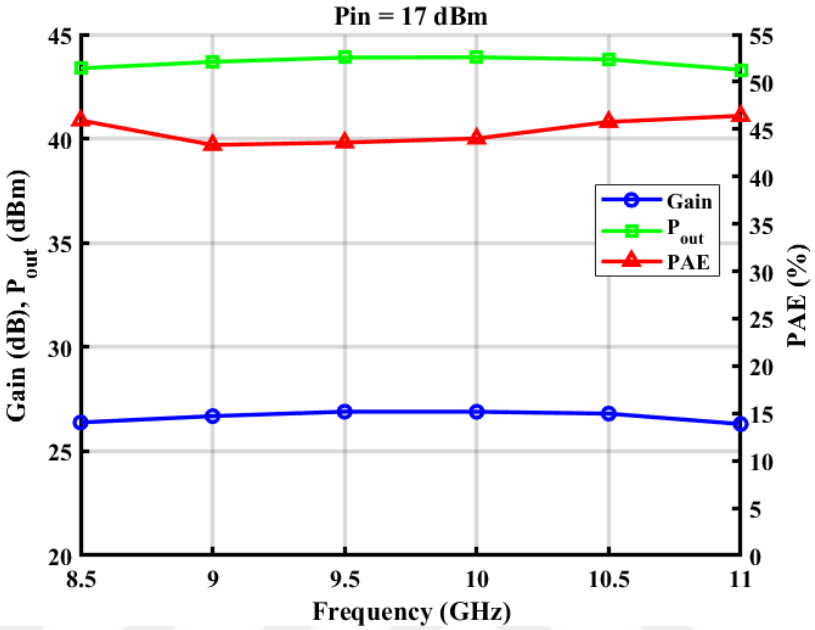


Figure 6.26: Large signal on-wafer measurements for promising design under 10% duty cycle pulse condition, 28 V, 100 mA/mm quiescent bias, 70°C ambient, and 17 dBm fixed input power from source.

Further large signal testing of promising design (approach 1) is performed at high chuck temperatures of 70°C on-wafer. The results are plotted in Fig. 6.26 for the entire operating frequency band. The input power from the source is increased from 15 dBm to 17 dBm to account for the reduction in gain at high temperatures. It is seen that the amplifier provides a large signal gain higher than 26 dB, the P_{out} is greater than 43.3 dBm, and PAE is still better than 43.3 %.

Finally, performance of the promising PA is compared with the state of the art work reported in the X-band as shown in Table 6.6. The proposed PA is compact, and it has the highest PAE. Moreover, its power density is also the best, so power is efficiently combined in a smaller area.

Table 6.6: Comparison with reported MMIC PAs in X-band

Parameter	**Units**	**[83]**	**[87]**	**[88]**	**[89]**	**[90]**	**This Work**
Process	µm	0.25	0.25	0.25	0.25	0.25	0.25
Frequency	GHz	8.5–10.5	8.5–10.5	8.5–11	8.5–11.0	8.5–10.5	8.5–11
S_{21}	dB	40	23	33	15–18	21–25	36.4
P_{out}	W	20	17.8	15	20	21–29	22.7–25
PAE	%	43	37.3	40	36	35–37	45.1–49.7
Area	mm^2	10.26	9.125	12.7	17.02	13.26	9
Power density	W/mm^2	1.95	1.95	1.18	1.18	1.58	2.52

6.7 Conclusions

The design of a high efficiency GaN power amplifier is described using NAONTAM's 0.25 µm facility. The amplifier operates in the frequency range of 8.5 to 11 GHz. It uses two different design topologies: 1:1:4 and 2:2:4. The drive ratios are 1:1.7:4 and 1:2.8:11. The small signal gain of more than 35 dB is achieved from both approaches. The output power is also measured more than 43 dBm from both approaches. There is a difference in PAE of both designs; the design with 1:1:4 topology provides 6 % better efficiency than the other. This enhanced PAE is achieved by reducing the number of HEMTs in the first and middle stages. It reduces the overall gate periphery by 16 %, which in turn reduces power dissipation and results in improved efficiency. The overall PAE achieved is more than 45 percent at room temperature and 43.3 % at a high temperature of 70°C.

Chapter 7

Conclusions and Future Work

Transceivers are fundamental components for all types of phased array radars and mobile communication systems. Miniaturization of electronic modules for such systems has urged MMIC solutions for transceivers. Low noise amplifiers (LNAs) and high power amplifiers (HPAs) are the most challenging components of a transceiver. This thesis focuses on designing and developing these components in the X-band using GaN on SiC HEMT technology. GaN on SiC HEMT technology has outperformed its competitive technologies due to its wider band gap, higher power density, and excellent thermal characteristics.

Designs of LNAs and HPAs in this thesis are based on measurement models of the HEMTs. For that on-wafer DC, small signal, noise, and large signal measurements of the HEMTs are performed using standard probe stations and test equipment.

On the LNA side, the thesis investigates robustness; survivability, and reverse recovery time (RRT) using cascode and source degenerated (SD) HEMT configurations. A single-stage LNA is designed using 4×50 µm cascode HEMT (LNA-A) with 0.15 µm gate length in the frequency range of 8 - 12 GHz. Its performance is compared with a single-stage LNA based on SD configuration (LNA-B). It is experimentally shown that LNA-A has 1.7 dB higher gain and

12 dB higher reverse transmission than LNA-B. The primary reason is the reduced Miller capacitance, making the cascode topology less prone to mismatches at the output side. The noise figures (NFs) for LNA-A and LNA-B are below 1.9 dB. The gate feedback resistor R_{GB} at the gate improves survivability. The LNA-A has 1 kΩ resistor at its gate and its survivability is compared with an equivalent SD version (LNA-C) with same limiting resistor. It is observed that LNA-A survives up to 33 dBm, while LNA-C handles 30 dBm input power (P_{in}), with minimal degradation in NF. The RRT of LNA-A is better than LNA-C. Overall, cascode configuration-based LNA is better than source degenerated-based LNA in terms of robustness, but at the cost of slightly increased NF. This study is useful for choosing the optimum HEMT configuration when designing LNAs for a transceiver system.

Further study on LNA consists of another design having three stages using 4×75 µm SD HEMTs. This LNA presents a stage-wise analysis for gain, NF, and matching network losses at the design stage for achieving promising results. Moreover, high gain in a compact area is achieved using spiral inductors at the gates and meandered transmission line structures on the drain sides. The LNA provides 16.4 dBm output power (P_{out}) at 1-dB gain compression and a third-order intercept point of 24.7 dBm at 10 GHz. For survivability purposes, R_{GB} is used at gates of all the stages, and the values are 5 kΩ (first stage), 2 kΩ (second stage), and 1 kΩ (last stage). The reason for the stage-wise decrease in R_{GB} values is the reduction of stress level from one stage to the next. This LNA survived up to 42 dBm, and its NF is below 1.5 dB, making it the best combination of NF and survivability reported in the literature at X-band to date to the best of the author's knowledge. The RRT of this LNA is measured under the same duty cycle and two different pulse width conditions. It is shown that LNA has better RRT for lower pulse width conditions, i.e., 4 ms at 25 µs and 70 ms at 200 µs with the same 25 dBm P_{in} level. This study is critical to characterize the pulse conditions for installing LNAs in transceiver systems, especially radars, where recovery time becomes a bottleneck for the overall receive chain.

Furthermore, GaN LNAs have high saturated output power (P_{sat}) levels, which causes an integration challenge for the LNA within the system. The subsequent

modules in the system are based on either SiGe or GaAs, and their typical safe operating range for P_{in} is from 15 to 20 dBm. In this thesis, we propose a novel idea of using an un-gated HEMT to reduce P_{sat}. The un-gated HEMT in the drain bias line of the LNA limits the output current of the HEMT. It is experimentally shown by implementing a 35 µm periphery HEMT into a three-stage LNA that P_{sat} is reduced from 28 dBm to 20 dBm. The effect of these HEMTs on other LNA's performances, including noise, small signal, large signal, and linearity, is also studied. The linearity of LNA is not affected. However, P_{1dB} of LNA is reduced by 2 dB. Moreover, NF and small signal parameters are also not degraded. The integration of un-gated HEMT into LNA does not affect the overall size of the chip due to its tiny size. This study provides an alternative approach for limiting the output power of LNA for use in transceivers and its easy integration within the overall receive chain of the system.

Lastly, on the HPA side, the design of a high efficiency GaN power amplifier (PA) is proposed using HEMTs with 0.25 µm gate lengths. The operating frequency band of PA is from 8.5 to 11 GHz. It is designed using two approaches, approach 1 and approach 2, having different design topologies. Approach 1 has a 1:1:4 design topology with a drive ratio of 1:1.7:4, while approach 2 has a 2:2:4 design topology with a 1:2.8:11 drive ratio. The output peripheries for approach 1 and approach 2 are 5 mm and 4.8 mm, respectively. All the measurements are done on-wafer under 10 % duty cycle pulse conditions. Both approaches provide more than 35 dB small signal gain, and P_{out} greater than 43 dBm. The difference lies in the power-added efficiency (PAE) of the two designs. The approach 1 provides 6 % better efficiency than approach 2. This increase in PAE is attributed to the reduction of the number of HEMTs in the middle and first stages, which caused a 16 % (8 mm to 6.7 mm) reduction in the total gate periphery of the amplifier. This reduction in gate periphery lowers dissipated power; hence, PAE is improved for approach 1. The overall PAE achieved is more than 45 percent at 25°C ambient and greater than 43.3 % at 70°C. We have achieved superior performance in terms of size, PAE, and power density compared to what has been reported in the literature so far at the operating frequency band. This study is beneficial for high efficiency PA designs for transceiver systems.

The future work consists of the following studies:

- An LNA design incorporating both feedback resistors for survivability and current limiters to reduce P_{sat}.
- Study RRT of HEMTs only and design a reduced RRT LNA, considering HEMTs peripheries and improvements in epitaxial structure.
- Reliability study of the power amplifier.
- Design an SPDT switch and integrate LNA and PA all together to make a single-chip MMIC transceiver.

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