STRUCTURAL AND ELECTRICAL CHARACTERIZATIONS OF $BiFeO_3$ THIN FILMS AND USAGE IN RADIATION SENSORS

by

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ABSTRACT

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In this thesis, the structural and electrical characterization of $BiFeO_3$ thin films and possible usage of $BiFeO_3$ in MOS based radiation sensors were investigated. $BiFeO_3$ thin films were deposited on (100) p-type silicon wafers with a thickness about 300 nm by magnetron sputtering. The deposited thin films were divided into two groups. First group samples were annealed at 550°C for 30 minutes under atmospheric environment. The second group samples were kept as-deposited. Structural characterizations were studied by using XRD and SEM measurements before and after annealing of samples. The $BiFeO_3$ MOS capacitors were fabricated in both annealed and as-deposited samples by using evaporation technique. High frequency C-V measurements were performed for both type samples, but frequency dependent C-V hysteresis and G/ω-F measurements were carried out for annealed samples exhibited the desired characteristic. To examine

their gamma irradiation response of the annealed ones, the devices were irradiated up to 16 Gray by using the GAMMACELL 220 Co-60 radioactive source at a dose rate of 0.0030 Gy/s. C–V measurements were recorded prior to and after irradiation and the effects of radiation were determined from the mid-gap and flat-band voltage shifts. The results show that $BiFeO_3$ can be used as dielectric layer for future dielectric applications such as radiation sensors.

Keywords: $BiFeO_3$ MOS capacitors, Interface states, Oxide trapped charges, Radiation sensors.

ÖZET

$BiFeO_3$ İNCE FİLMLERİN YAPISAL VE ELEKTRİKSEL ÖZELLİKLERİ VE RADYASYON SENSÖRÜ OLARAK KULLANIMI

Şenol KAYA

Yüksek Lisans, Fizik Bölümü

Tez Danışmanı: Prof. Dr. Ercan YILMAZ

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Bu çalışma kapsamında $BiFeO_3$ ince filmlerinin yapısal ve elektriksel özellikleri incelendi ve üretilen yapıların MOS tabanlı sistemlerde radyasyon sensörü olarak kullanılabilirliği araştırıldı. $BiFeO_3$ ince filmler magnetron saçtırma yöntemiyle (100) p- tipi Si alt taşlar üzerine 300 nm kalınlıklarında büyütüldü. Büyütülen filmler iki gruba ayrıldı. İlk gruptaki filmler 550 ^{0}C derecede 30 dakika süre ile hava ortamında tavlanırken, diğer örnekler üretildikleri şekliyle muhafaza edildi. Filmlerin yapısal karakterizasyonu XRD ve SEM ölçümleri kullanılarak tavlama işlemi öncesi ve sonrasında yapıldı. Tavlama yapılmış ve sadece büyütülmüş $BiFeO_3$ ince filmler buharlaştırma yöntemiyle ön ve arka kontaklar Alüminyum ile kaplanarak MOS kapasitörlerine dönüştürüldü. Üretilen kapasitörlerin yüksek frekans C-V ölçümleri incelendi. Farklı frekanslarda C-V histerezis ve G/ω-F ölçümleri optimum performansa sahip ve tavlama işlemi

yapılmış örnekler için çalışıldı. Tavlanmış örneklerin gamma radyasyonuna duyarlılıklarının çalışılması için kapasitörler 16 Gy'e kadar GAMMACELL 220 Co-60 radyoaktif gamma kaynağı ile 0.0030 Gy/s doz hızında ışınlandı. Her bir ışınlama adımında örneklerin C-V ölçümleri alındı ve cihazların radyasyona duyarlılıkları düzbant (flatbad) ve ortabant (midgap) voltaj kaymaları kullanılarak incelendi. Elde edilen sonuçlar $BiFeO_3$ yapısının radyasyon sensörü gibi sistemlerde dielektrik malzeme olarak kullanıma uygun olduğunu göstermiştir.

Anahtar Kelimeler: $BiFeO_3$ MOS kapasitörleri, Arayüzey tuzakları, Oksitte tuzaklanmış yükler, Radyasyon sensörleri

Dedicated to My Dad, Hasan KAYA, My Mom, Şahinder KAYA and My Sister, Şennur KAYA, whose Love Have Contributed so Much to My Strength and Faith.

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CHAPTER 1

INTRODUCTION

A metal-oxide-semiconductor (MOS) devices are technologically important materials and have enormous technological using area such as transistor structures, some components of computers, radiation sensors etc. In order to use MOS devices as radiation sensors, they have to require high sensitivity and linear performance over the intended energy range, real-time response, low noise and acceptable reliability [1]. Different materials, geometric arrangements and physical detection techniques have been used to detect the radiation. Among these, MOS based radiation sensors have attracted special attention because of their superior sensitivity as well as the excellent compatibility with the existing CMOS technology [2,3]. MOS is a type of capacitor and consists of a semiconductor substrate with a thin oxide layer and at the top of oxide and at the bottom of substrate is coated with a metal structure which stores electric charge according to the level of dielectric property of oxide layer [4]. There exists two important semiconductor structures to classify devices and integrated circuits are silicon (Si) and gallium arsenide (GaAs). Si is more useful because of its economic structure and electrical properties and that is the point that people can get high-quality oxide structure by growing film [4]. Conventional oxide layer is SiO_2 on MOS structure this oxide layer was used to many year because of some important advantages such as easy to grown high quality oxide layer, leakage current and economic, but

nowadays the main research are trying to fabricate new oxide layers because one knows that device performance of MOS device directly depend on gate oxide dielectric and interface states of its with underlying semiconductor [5].

The purpose of this study is to improve of high-k dielectrics to replace silicon dioxide (SiO_2) due to the potential improvement in the operational lifetime and performance of semiconductor devices in high radiation environments. Semiconductor manufacturers are incorporating high-k dielectrics in commercial electronics to reduce leakage current as oxide gates are designed thinner to improve device speed [6]. Many gate oxides have been studied to replace SiO_2. In this study we used Bismuth ferrite ($BiFeO_3$) for oxide layer. It is an inorganic chemical compound with perovskite structure and one of the most promising multiferroic materials. The room-temperature phase of $BiFeO_3$ is classed as rhombohedral belonging to the space group R3c. [7] It is synthesized in bulk and thin film form and both its antiferromagnetic (G type ordering) Néel temperature and ferroelectric Curie temperature are well above room temperature (approximately 653 K and 1100K, respectively) [7,8]. $BiFeO_3$ demonstrates attractive material properties: high dielectric constant, wide band gap, and thermodynamic stability with silicon.

Briefly radiation effect on MOS capacitor is that when radiation pass through to inside the MOS device, electron (e) and hole (h) pairs create in the structure and by strong effect of electric field, the e-h pairs move to different sides and as a result of these e-h motions, a fraction of them trapped on structure and the flatband voltage shift to different values. The electrical characteristics of MOS devices response with performances of MOS device; flat band and flat band shift voltage are given for remarkable information of these characteristics. After the

irradiation of MOS device, some characteristics must be investigated such as electrical response, structural and dielectric characteristics. Electrical characteristics of MOS structures can be determined by interfacial states, series resistances and oxide states [9].

In this work, radiation effects on $BiFeO_3$ MOS capacitor had been investigated by using capacitance- voltage (C-V) characteristic of $BiFeO_3$ MOS capacitor. To do this, firstly structural characterization performed by XRD and SEM measurements for as-deposited and annealed samples. After that the fabricated samples are converted to MOS devices by Al evaporation technique. To investigate fabricated devices performance; firstly high frequency (1MHz) C-V characteristics were measured for both annealed and as-deposited samples. After that frequency dependent capacitance- voltage (C-V) hysteresis and conductance-frequency measurement were performed for annealed samples had desired electrical at room temperature. After that, samples were irradiated with Co-60 gamma sources and interface and oxide state densities were calculated for each given dose steps. Finally, the obtained results were analyzed and discussed.

An outline of this thesis is included in order to gain understanding of what is included in this document beyond the table of contents. On chapter 2 theoric information were given for ideal and non-ideal MOS capacitors. The radiation effects on MOS structure were discussed on chapter 3. Briefly describes at Chapter 4 the details experimental procedure. This includes fabrication of MOS and measurement materials. For last chapters 5 and 6 experimental results were calculated and discussed.

CHAPTER 2

STRUCTURE OF METAL-OXIDE-SEMICONDUCTOR (MOS)

The MOS capacitor consists of an oxide film sandwiched between a P- or N-type silicon substrate and a metal plate called gate as shown in Fig. 2.1. This figure simplest model of MOS structures schematically. The working principle of the behavior of this capacitor under a bias applied condition between substrate and gate is a most useful way to investigate the quality of the oxide layer and the quality of the oxide-silicon interface [10].

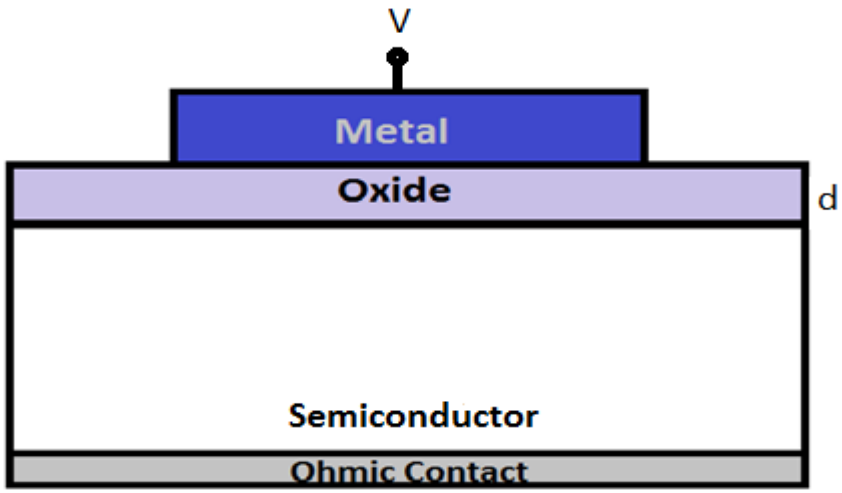

Figure 2. 1: Cross-sectional view of MOS structure.

2.1 Ideal MOS Structure

The metal-oxide-semiconductor (MOS) structure is shown in Fig. 2.1, where d is the thickness of the oxide and V is the applied voltage. V is positive voltage in thesis when the metal plate is positively biased with respect to the semiconductor

body. For both n-type and p-type semiconductors the energy-band diagram of an ideal MOS structure is shown in Fig. 2.2 without bias. According to researches an ideal MOS capacitor is defined as follows: (1) The only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those, with an equal but opposite sign, on the metal surface adjacent to the insulator, i.e., there is no interface trap nor any kind of oxide charge; (2) There is no carrier transport through the insulator under dc biasing conditions or the resistivity of the insulator is infinite [4,10,11].

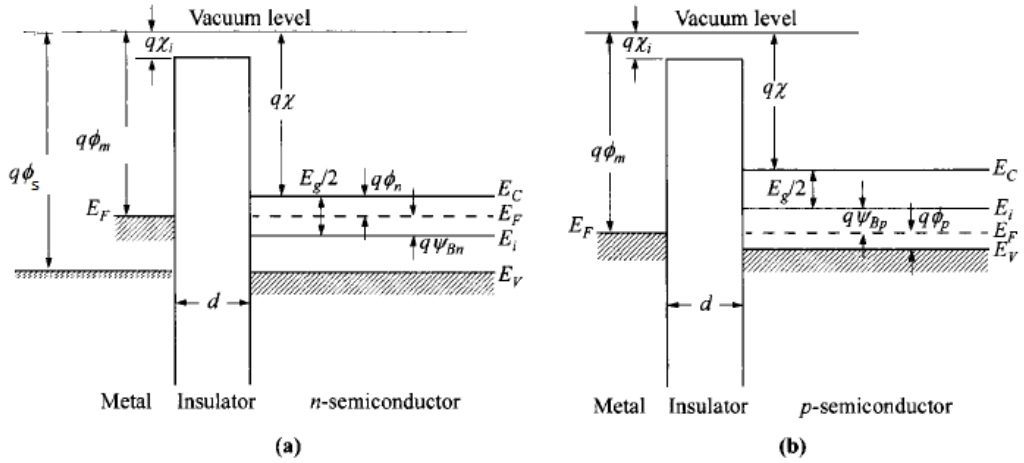

Figure 2. 2: The energy band diagram for ideal MOS structure a-) for n type b- for p type substrate [4].

Furthermore, for simplicity researches assume the metal is chosen such that the difference between the metal work function ϕ_M and the semiconductor work function ϕ_S is zero as following;

$$\phi_{MS} = \phi_M - \phi_S = 0 \tag{2.1}$$

and people can found more details of Eq. (2.1) from Fig 2.2 and Eq. (2.1) became;

$$\phi_{MS} = \phi_M - (\chi - \frac{E_g}{2q} - \Psi_{Bn}) = \phi_M - (\chi + \phi_n) = 0 \qquad \text{for n- type} \qquad (2.2\text{- a})$$

$$\phi_{MS} = \phi_M - (\chi + \frac{E_g}{2q} - \Psi_{Bp}) = \phi_M - (\chi + \frac{E_g}{q} - \phi_p) = 0 \quad \text{for p- type} \qquad (2.2\text{- b})$$

where χ and χ_i are the electron affinities for the semiconductor and oxide respectively, and Ψ_{Bn}, Ψ_{Bp}, ϕ_n, ϕ_p are the Fermi potentials with respect to the midgap and band edges. In other words, the band is flat (flat-band condition) when there is no applied voltage and charge distribution on flatband as shown in Fig. 2.3- (a) [4,12].

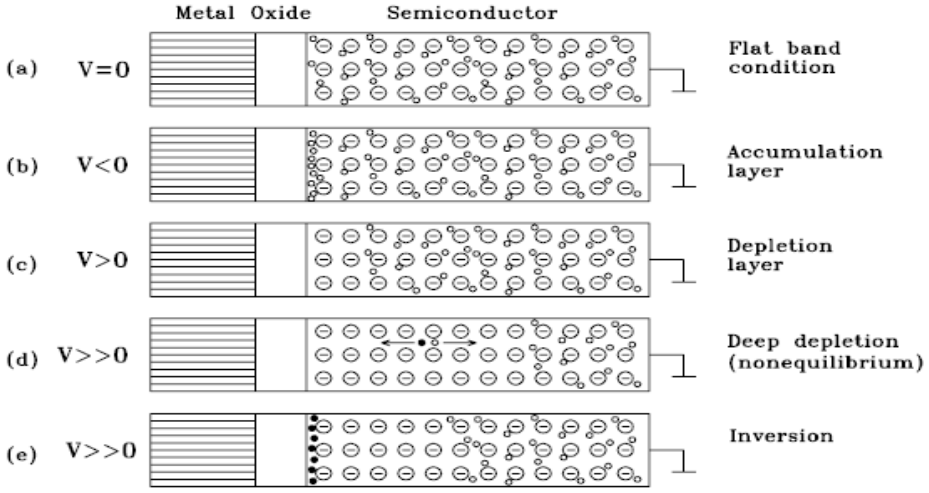

Figure 2. 3: Graph of an ideal p-type MOS structure: a-) thermal equilibrium in flat band condition, b-) accumulation region, c-) surface depletion region, d-) overdepletion region, e-) inversion region [12].

MOS capacitance behavior varies with the applied gate voltage. When an ideal MOS capacitor is biased with positive or negative voltages, basically three cases may exist at the semiconductor surface. The capacitance versus voltage characteristics of MOS capacitors is result of the modulation of the width of the surface space charge layer (SCL) by the gate field have been found to be extremely useful in the evaluation of the electrical properties of oxide-silicon interfaces. The three regions are accumulation, depletion and inversion

respectively in the C–V characteristics of the MOS capacitor as shown in Fig. 2.4. [10].

2.1.1 Accumulation

When an smaller than flat band voltage is applied to the p- type silicon surface in MOS capacitor, the carrier densities change accordingly in its surface region. With large negative bias applied to the gate, holes are attracted by the negative charges to form an accumulation layer (Fig. 2.5-a). The high concentration of these holes will form the second electrode of a parallel plate capacitor with first electrode at the gate. Because of the accumulation layer is an indirect ohmic contact with the P-type substrate, the capacitance of the structure under accumulation conditions must be approximately equal to the capacitance of the oxide [11],

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_{o}}{d_{ox}} \tag{2.3}$$

Here ε_{o} is the permittivity of the free space, ε_{ox} the relative permittivity of oxide, and d_{ox} the oxide thickness. This Eq. (2.3) unit of capacitance is expressed per unit gate area [F cm^{-2}]. The value of it does not depend on gate voltage in accumulation mode (Fig. 2.4).

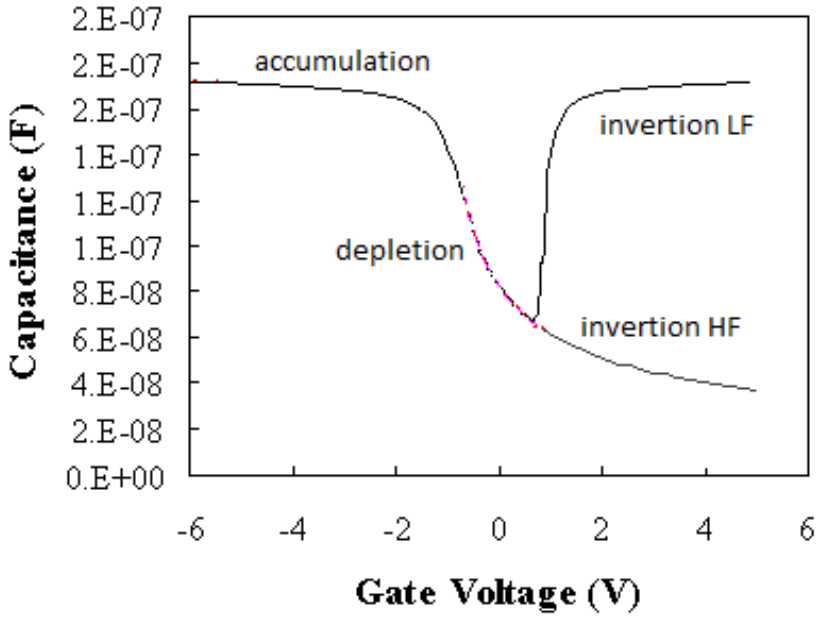

Figure 2. 4 : The three region of MOS capacitance, accumulation, depletion and inversion regions [13].

The capacitance value also does not dependent of the frequency as long as the motion of the majority carriers, which contribute to substrate charge ΔQ_s on ideal MOS structure, can keep pace with the incremental speed of gate charge ΔQ_M . Under this condition, the Fermi level near the Si surface will move to a position closer to the valance band edge as shown in Fig. 2.5- (a) for p- type substrate silicon [10].

2.1.2 Depletion

If the bias applied more positive than flatband voltage from gate than gate is became more positive with respect to flat band, and holes are depleted and a region is formed at the surface which is depleted of carriers [10]. If the voltage is further increased, the depletion width will increase also; however this over depleted situation is not stable [12] as Fig. 2.3- (c) and (d).

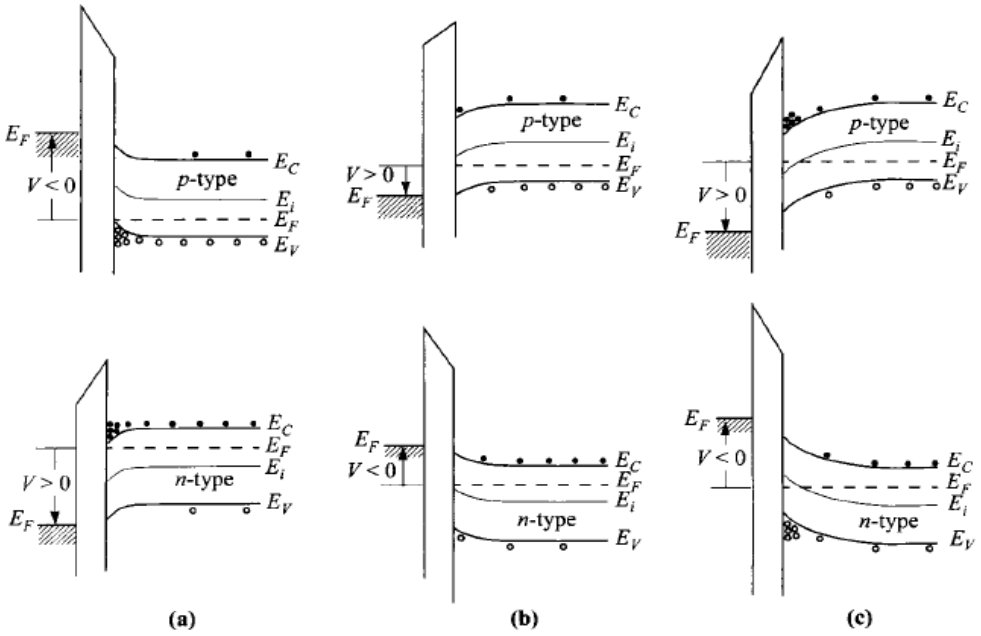

Figure 2. 5: The energy bad diagram of MOS capacitor a-) for accumulation, b-) for depletion, c-) for inversion regions [4].

On this depletion condition Fermi level near the silicon surface will change and it starts to move a position closer to the center of the forbidden region as shown in Fig. 2.5-(b). If one increases the positive voltage V_G, it will tend to increase the width of the surface depletion region X_D, so the capacitance from the gate to the substrate associated with MOS structure will decrease, because the total capacitance value is series combination of surface depletion region and oxide capacitance region. The total capacitance value of system can be calculated as for ideal MOS capacitors

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s(V_g)} \tag{2.4}$$

Here C_s is silicon capacitance and it is defined by

$$C_s(V_g) = \frac{\varepsilon_0 \varepsilon_{si}}{X_d} \tag{2.5}$$

and the X_d can be found

$$X_d = \sqrt{\frac{2\varepsilon_0 \varepsilon_{si} \Psi_s}{qN_a}} \tag{2.6}$$

Where the relation between the applied gate voltage $V_{g\ and}$ the total band banding Ψ_s can be written as

$$V_g = \Psi_s + \sqrt{\frac{2\varepsilon_0 \varepsilon_{si} qN_a \Psi_s}{C_{ox}}} \tag{2.7}$$

The important point here only the majority carriers contribute space charge ΔQ_s [10].

2.1.3 Inversion

When more positive bias applied from gate the bands of semiconductor continue to bend to upward. After some point location of intrinsic Fermi level of semiconductor, $E_{i,}$ pass the Fermi level of semiconductor and the Fermi level near the silicon surface will now lie close to the bottom of conduction band as Fig. 2. 5-(c) for p- type silicon substrate. This inversion layer is very thin and thickness is around 1–10 nm and separated from the bulk of silicon by the depletion layer as seen in Fig. 2. 3- (c). The voltage, which inversion region starts to occur, is called threshold voltage. The threshold condition marks the equality of the concentration of minority carriers to the doping concentration. One important thing about inversion the depletion region length reaches to maximum, Xd_m when inversion region starts to occur. As shown in Fig. 2.4 capacitance value of MOS capacitor depend on the frequency of voltage because sometimes the charge density in the inversion layer may or may not be able to follow the ac variation of the applied gate voltage [10].

2.1.3.1 Low Frequency Capacitance

Measurement frequency low enough less than 100 kHz so that generation or recombination rates in the surface depletion region are equal to or faster than gate voltage frequency, then minority carriers concentration can follow the ac voltage and it lead to charge exchange with inversion layer [4]. The capacitance value, $C_{LF,}$ of MOS structure equal to oxide capacitance in accumulation mode for ideal MOS structure [10].

$$C_{LF} = C_{ox} \tag{2.8}$$

2.1.3.2 High Frequency Capacitance

When measurement frequencies high enough higher than 100 kHz, all incremental charge appears at edge of depletion region. The charge modulation occurs at distance X_{Dm} of the Si–SiO_2 interface. It follows that the high frequency capacitance of the MOS structure, C_{HF}, is given

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_{dm}} \tag{2.9}$$

Where C_{dm} is equal to

$$C_{dm} = \frac{\varepsilon_0 \varepsilon_{si}}{X_{dm}} \tag{2.10}$$

and

$$X_{dm} = \sqrt{\frac{4\varepsilon_0 \varepsilon_{si} kT \ln(N_a / n_i)}{q^2 N_a}} \tag{2.11}$$

2.2 Non-Ideal MOS Structure

Experimental results show us, the real MOS structure is different from ideal MOS structure. There exist some charges in oxide and interface between semiconductor and oxide layer and according to research the reason of differences caused by this charges and early studies of the MOS devices showed that the threshold voltage V_{Th} and the flat band voltage V_{FB} could strongly be affected by these charges [18-20]. The important result of the presence of any charge in the oxide is to induce a charge of opposite polarity in the underlying silicon. The charges in MOS structures are mobile ionic charges, fixed oxide charges, oxide trapped charges, and interface trapped charges as in Fig 2.6.

2.2.1 Mobile Ionic Charges

The mobile charges denoted Q_m at basically exist in the interface between metal and oxide or oxide and semiconductor layer. These charges generally are ionized alkali metal such as sodium or potassium. They are relatively moveable inside of oxide at low temperature under applied voltages. Resulting from drift of these charges, ionic current may occurs in the structure. Therefore it may cause deviation of electrical characteristics of MOS devices. Source of these impurities are cleaning process, used chemical, touching wafer with bare hand in fabrication steps. These mobile ions are specifically Na^+, H^+, H^3O^+, K^+, Li^+ ions [14]. The order of mobile ions are 10^{11} cm^{-2} for real MOS devices [11].

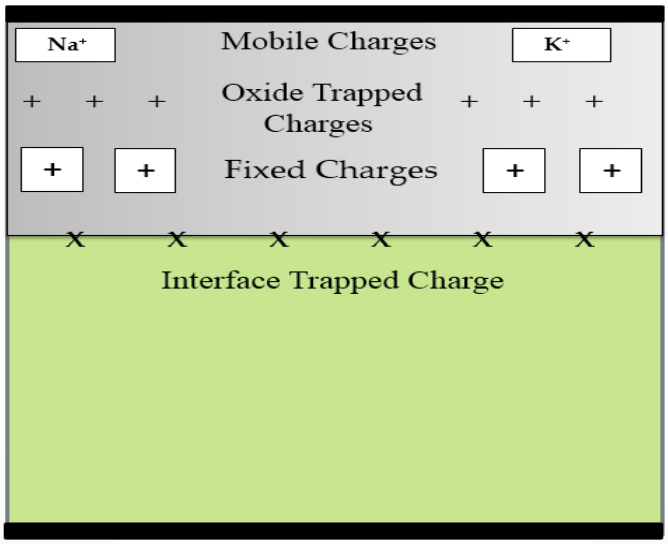

Figure 2. 6 : The impurity charges on the high-frequency MOS devices

2.2.2 Fixed Oxide Charges

These charges located into dielectric layer of MOS devices and cannot move into oxide layer under voltage field. Fixed oxide charges, Q_f. are generally positive and they depend on dielectric deposition standards and orientation of semiconductor wafer. They may deviate device behavior from expected ideal MOS characteristics. The effects of these charges on electrical characteristics of device can be determined in the C-V characteristics. These charges shift the C-V measurements toward more negative voltages than ideal case both for p-type and n-type semiconductor based MOS capacitors.

2.2.3 Interface Trapped Charges

Interface traps are energy levels generated by impurities within the semiconductor crystal [15] allowed for the carriers in the forbidden energy gap of the semiconductor. These energy levels can change their charge state by exchange of carriers with the semiconductor. They are interacting with the conduction band

by capturing or emitting electrons and with the valence band by capturing or emitting holes. The donor like interface states become positively charged, when it emitting electron and the acceptor like interface states become negatively charged, when it capture an electron. There are two types of interface states. They behave like an acceptor or donor. Therefore they may trap both positive and negative charges. Interface trapped charges Q_{it} may shift C-V curves toward positive or negative voltages depending on trapped charges type. Moreover, it has been reported that interface states may show variation with applied voltage frequency during the measurements. Therefore number of trapped charges may show variation depending on measurements standards.

2.2.4 Oxide Trapped Charges

Due to structural defects, oxidation-induced defects, metal impurities, or other defects caused by radiation or similar bond breaking processes of dielectric layer, the oxide traps can be generated. These generated traps may traps mobile charges in the structure known as oxide trapped charges denoted as Q_{ox}. They may be exchange charges between oxide and interface at oxide/semiconductor. Therefore they enhance the number of charge density in the MOS devices. The trapped charges in the oxide layer can be positive of negative but they are generally positive that is holes [5,16,17], and also similar to interface trapped charges with the difference that they exist in the bulk. Owning to increases of positive charges in the structure the C-V curves may shift the negative voltages.

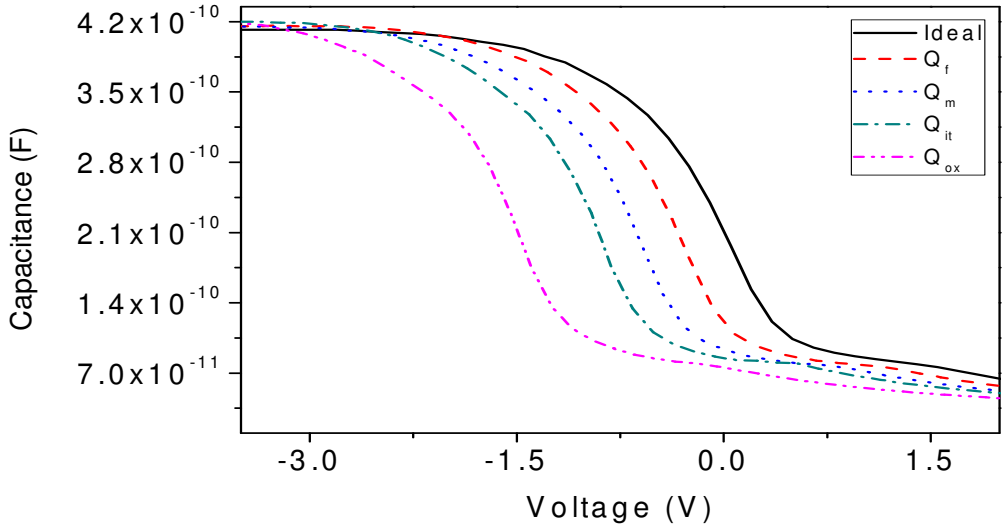

Figure 2. 7: Influence of the impurity charges on the high-frequency MOS C-V curve.

Assume that all impurity charges are positive than the effects of these charges are illustrated in Fig. 2.7. The sum of these oxide charges is also called effective oxide charge Q_{eff} as given in Eq. (2.12).

$$Q_{eff} = Q_m + Q_f + Q_{ox} + Q_{it} \tag{2.12}$$

2.3 Investigation of Interface and Oxide States Density at MOS Devices

In MOS devices, the presence of interface traps and oxide charge affect the characteristics of ideal MOS characteristics. Impurities in the semiconductor lattices and degradation of oxide layer causes the generation of new energy level in the forbidden band energy in the structure. The defects located these new energy levels are called as surface states. The mean density of these energy level is order of 10^{10} cm^{-2} -10^{12} cm^{-2} considering to experimental calculations. There are two types of surface states as slow switching traps and fast switching traps. Slow switching traps located in the interior region of oxide layer. While they are relatively immobile and fixed charges, a fraction of them may immigrate under

high electric fields. These states may be removed by heat treatments. On the contrary the fast switching traps located in the very close to interface between semiconductor and oxide layer, and have nearly same energy with the half of forbidden band energy. Therefore, they may cause band bending of semiconductor by exchanging the charge carriers. For the bare MOS capacitor density of slow switching traps is approximately equal to oxide charges and fast switching trap densities can be called as interface states. The distribution of these two trap densities can be studied by capacitance voltage and at constant voltage, conductance- frequency measurements of the devices.

2.3.1 Capacitance Methods

Due to trapped charges in the structure, the capacitance- voltage characteristics shift toward negative or positive voltages depending on majority of trapped charge density i.e. electrons or holes [16,18,19]. Moreover in the sufficient high frequency, the interface states have less time to follow applied voltage frequency. Therefore C-V characteristics cannot be affected and applied voltage shared with insulator layer and semiconductor layers.

The distributions of trap densities in the structure can be calculated from capacitance methods. Several methods have been derivated to calculate trap densities in the structure. One of the useful methods to calculate interface trap density is low frequency capacitance C_{LF} and high frequency capacitance C_{HF} methods [20]. The interface trap density (N_S) can be calculated by;

$$qAN_s = C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{OX}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{OX}}\right)^{-1} \tag{2.13}$$

Where *A* is the electrode area, q is electric charge, C_{ox} is the oxide capacitance. Also N_S can be calculated using by space charge capacitance (C_{sc}) methods as following;

$$qAN_s = (C_{LF} - C_{sc}) \tag{2.14}$$

It is well known that the presence of frequency dependent charge may deviate the devices characteristics. These effective charge densities Q_{eff} can be calculated by using capacitance measurements as followings;

$$V_{fb} = \varphi_{ms} - \frac{Q_{eff}}{C_{acc}} \tag{2.15}$$

where V_{fb} is flatband voltage measured on C-V characteristics, φ_{ms} is the difference in work function between metal and semiconductor substrate, and C_{acc} is maximum capacitance value in accumulation.

Moreover the changes in the defect densities in the devices may also calculated by using C-V measurements of devices. The changes in the net oxide trap-charge densities (ΔN_{ot}) can be estimated from observed midgap voltage shift (ΔV_{mg}) as given

$$\Delta N_{ot} = -\frac{C_{ox}\Delta V_{mg}}{qA} \tag{2.16}$$

Similarly, ΔN_{it} can be estimated from the midgap-to-flat band stretch-out of the C–V curves by

$$\Delta N_{it} = -\frac{C_{ox}\left(\Delta V_{fb} - \Delta V_{mg}\right)}{qA} \tag{2.17}$$

where C_{ox} is the oxide capacitance, q is electric charge, and A is the capacitor area. In addition, barrier height ϕ_B of the device can be calculated from the following relation

$$\phi_B = V_0 + \frac{kT}{q} + E_F - \Delta\phi_B = V_D + \frac{kT}{q}\ln\left(\frac{N_V}{N_D}\right) - \Delta\phi_B \tag{2.18}$$

where V_0 is the built-in potential and value can be obtained from C^{-2}–V plot by means of extrapolation of straight lines to the voltage axis, where V_D = Vo - kT/q is the diffusion potential, N_D is the doping concentration of p type Si determined from the slope of C^{-2}–V plots, N_V is the effective density of states in valance band and $\Delta\phi_B$ is the image force barrier lowering given by

$$\Delta\phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}} \tag{2.19}$$

where $E_m = \sqrt{2qV_D N_D / \varepsilon_0\varepsilon_s}$ is the maximum electric field and also one of the other important characteristics can be calculated by the following relation

$$\lambda_n = \sqrt{\frac{\varepsilon_s\varepsilon_0 kT}{q^2 N_D}} \tag{2.20}$$

where ε_S is the dielectric constant of semiconductor, ε_0 permittivity of free space, k the Boltzmann constant, q the electrical charge and T the temperature in Kelvin.

2.3.2 Conductance Methods

A very sensitive technique for characterizing insulator-semiconductor interface properties relies on characterizing the interface trap conductance by directly measuring the energy loss during capture and emission of the majority carriers between conduction band and interface trap levels under applied ac signal [11]. The relation between conductance and interface states is given by [21]:

$$\frac{G_p}{\omega} = \frac{AqD_{it}\ln\left(1+\omega^2\tau^2\right)}{2\omega\tau} \tag{2.21}$$

where D_{it} is interface states density, A is the MOS capacitor contact area, q is electrical charge, τ is time constant of interface states, ω is angular frequency. The maximum value in Eq. (2.21) is obtained by setting $d(G_p/\omega)/d(\omega\tau) = 0$, and for the maximum condition, $\omega\tau$ =1.98 is found. Thus, interface state density is expressed as follows:

$$D_{it} = \frac{\left(G_p/\omega\right)_{\max}}{0.402qA} \tag{2.22}$$

In this study the interface charge densities for fabricated devices were calculated using with frequency dependent conductance characteristics due to the it gives more reliable and accurate result [22].

CHAPTER 3

IONIZING RADIATION EFFECTS ON MOS DEVICES

3.1 Radiation-Matter Interaction

The interactions of radiation with materials are broad topics. There are several mechanisms depending on which radiation interacts with solid materials and the type, kinetic energy, mass and charge of the incident particle and the mass, atomic number and density of the target material are also important parameters. The radiation interactions with materials in this study were divided into two groups as charged particles and neutral particles.

3.1.1 Charged Particles

The principle charged particles are the electrons, protons and heavy ions. The charge particles interact mainly through Coulomb attraction or repulsion with the electrons of the irradiated materials.

Protons and non-relativistic nuclei will generate an ionizing density inversely proportional to their energy declining with path length and proportional to square of their charge in semiconductor based detectors. They interact with Coulomb interaction which can induce ionization for proton with energy less than 100 keV. Excitation or displacement can occur while collision with nuclei and nuclear reaction may be also occurs energies higher than 10 MeV.

Electrons, owning to the lower mass of electrons with compared to protons and other nuclei i.e. alpha particles and the lower charge, β ionizes much more feebly than proton radiations. The electrons can interact in two different types. The first one is Coulomb interaction same as proton radiations and the other one is scattering with nuclei if had enough energy to transfer nucleus. When electrons decelerate in the target material, they also loose energy by emitting Bremsstrahlung in form of X-ray.

3.1.2 Neutral Particles

There are basically two types of neutral particles; neutrons and photons. Due to they not have charge, they do not have Coulomb interaction with matter.

Neutrons are uncharged particles that have approximately same mass with protons. Due to they do not have charge, they cannot exhibits electrostatic interactions with materials. Therefore they may more penetrate than other particles that have charged. Neutrons can be divided into two types as slow intermediate had less than 1 eV and fast intermediate had higher than 100 keV. There exist three phenomena of interaction with the atomic nuclei for neutrons. Firstly one is nuclear reaction. The indecent neutrons may be absorbed by nucleus of target materials, after than other particles i.e. protons, gamma rays can be emitted. Second one is elastic collisions. They may collides with nucleus of target materials and continue their path. Having sufficient energy, nucleus of target materials may be displaced as ionization nuclear displacements. Last interaction type is inelastic collision for neutrons. It also collides with nucleus of target materials and continues their path as elastic collision. However only the difference is after excitation of the nucleus, it emits gamma rays. These probabilities of interaction

types depend on the energy of neutrons. Generally slow neutrons interact with target materials as nuclear reactions or elastic collisions, fast neutrons basically to elastic collisions. Also inelastic collisions dominate for extremely energy neutrons.

Photon is a kind of electromagnetic radiation which can be classified depending on their energies. The important photons for nuclear physics are X- rays (energies in the range 100 eV to 100 keV) and gamma rays (few hundred keV to a few MeV). There exist three phenomena of interaction with the atomic nuclei for photons. The first phenomenon is photoelectric effects. The indecent photon ionized the target materials and it loses all of its energies. After photoelectric interaction, the photoelectron is emitted. After that, excited electrons come back to its first level and then low energy photons also emitted in photoelectric interaction. The second phenomenon is Compton scattering. The indecent photon loses its energy and it emits free electron and energetic photons.

The last interaction type is creation of electron-positron pairs for photons. The indecent photons completely lose its energy creating with electron-positron pairs. The interaction type occurs when photons have energies less than 1.024 MeV. The probability of these three effects with the energy and also strongly depends on the atomic number of the target as in Fig. 3.1.

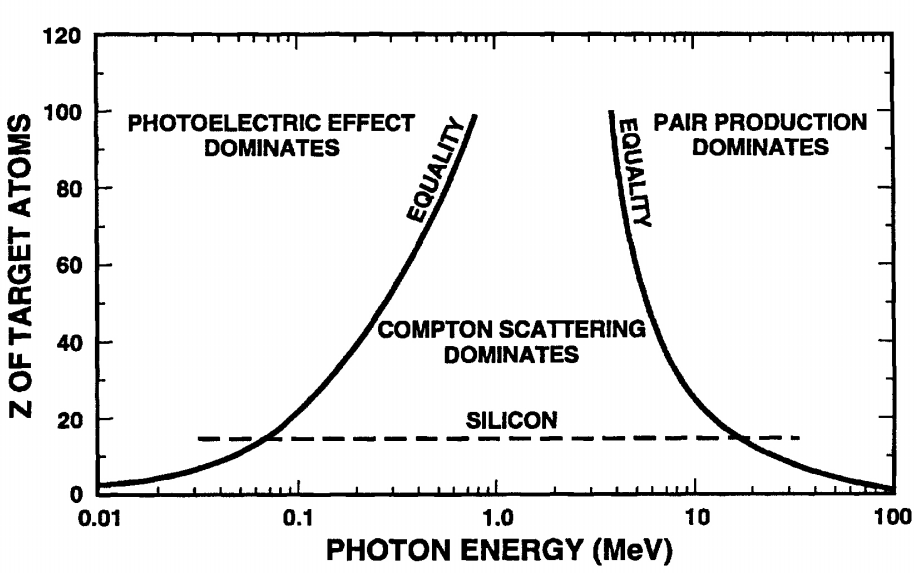

Figure 3. 1: The dominant photon- matter interaction mechanism depending on energy of atomic number of materials.

3.2 Radiation Effect on MOS Structure

The principle effects of irradiation on the MOS device generation of electrons- hole (e-h) pairs and defects sites in the oxide, interface between oxide and semiconductors. The some of these generated e-h pairs are trapped by defects densities in the structure leading to shifts in the flat band, midgap and threshold voltage of characteristics measurements. The detailed mechanism for the irradiation effects on the device structure is depicted in Fig. 3.2.

MOS devices are more sensitive to ionization than to displacement damage. The ionization means generation of e-h pairs in the semiconductor and oxide layers as mentioned above. The atomic displacements give origin to a neighboring interstitial atom and vacancy and have minor effects to radiation response of MOS devices.

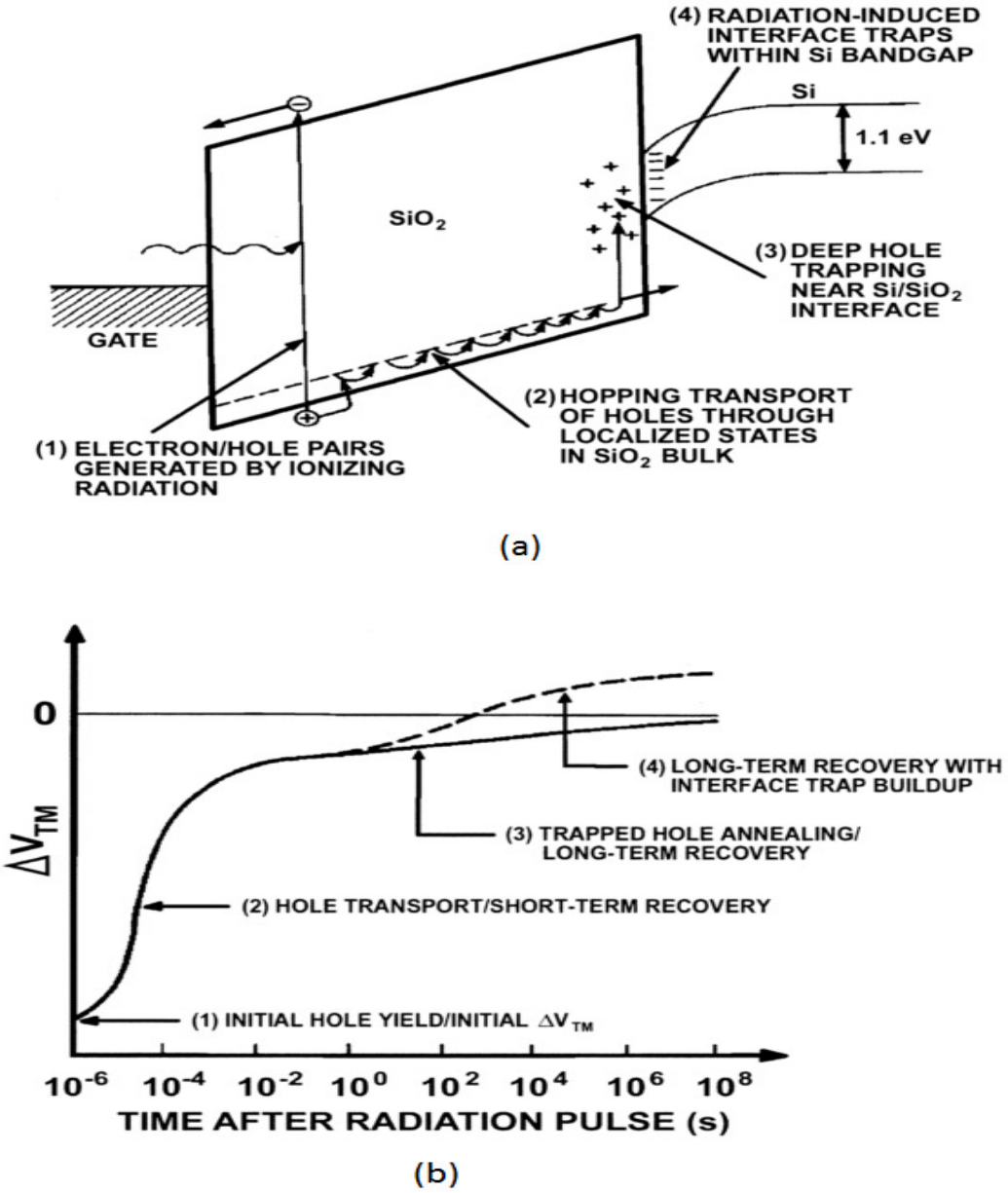

Figure 3. 2: Schematic illustration of a-) the effects induced by ionizing radiation in an MOS device, b-) time dependent threshold voltage change occurring after the irradiation process [23].

This mechanism is dominant for neutron radiations. The part of the MOS structure which is sensitive to ionizing radiation is the oxide layers. Ionizing irradiations creates enormous number of electron-hole pairs (~10^{18} $cm^{-3}Gy^{-1}$ for SiO_2) at devices in few pico-seconds [23]. Due to electrons are much more mobile than holes, they are disappears immediately from metal contacts and also a fraction

of generated these pairs are neutralized by recombination process after few micro seconds. Owning to the high electron and hole yields, the voltage shift is very high in just few micro seconds. These processes can be seen at first steps on Fig. 3.2 (a) and (b). After that, holes start to move towards the oxide- semiconductor interface with a various characteristic transport mechanism. The most excepted mechanism for this holes transport is called as “hopping”. The holes move the oxide layer using by the shallow trap states in the oxide layers and a portion of them recombine with electrons along its path. The hole transportation and influence of recombination on voltage shifts can be seen in second part of Fig. 3.2 (a) and (b). When the holes approach to oxide layer and semiconductor interface, they are trapped by deep traps. These deep traps states had crucial effects on the voltage shifts in the devices, due to they are perennial traps and causes permanent change in the flatband, midgap and threshold voltage. The last important parameter in radiation sensitivity of the devices can be described as an interface traps created by radiation. These traps located in oxide layer / semiconductor interface are energy states in the forbidden energy band gap of the semiconductor and divided into two types as an acceptor states and donors states. These energy states may trap the mobile charges depending on the types of it. Therefore it has contribution the voltage shifts in the structure. The location and effects on the device characteristics of these states can be seen on the last part of the Fig. 3.2 (a) and (b) in addition in Fig. 3. 2 (b) final voltage shifts in the devices is positive, this effects called as “superrecovery effects” here because number of negatively charged interface states exceeds number of trapped holes.

3.3 Theory of Traps Generated by Radiation

The ionizing irradiation interaction with MOS device's gate oxide materials and its interface is quite complex. The some important mechanism signified the below, should be understood to specify radiation response of these devices; (1) accumulation of trapped charges, (2) enhancement in the number of interface states and (3) enhancement in the number of the bulk oxide traps [2,24]. The radiation-trapped charges are directly related to amount of energy deposited by target oxide materials and devices. Some researchers determined that average energy to create e-h pairs is equal to 18 eV for conventional SiO_2 oxide layer [25]. This value can be shown small variations depending on the types of oxide layers. Generated holes are immobile comparing to electrons and may be trapped within the oxide layer by shallow and especially deep traps, leading to build-up net charge density [23,26,27]. Deep traps near to interface but in the still oxide layer arises due to there exist transition region located uncompleted bonds. This zone includes excess semiconductor or oxygen vacancies related to how one looks at it. In addition, mobile charges can be trapped by broken bonds by irradiations. Depending on the bonding types in the oxide, broken bonds may act like a donor sites or acceptor sites. It is well-known that positive or negative mobile charges may be trapped by these acceptor and donor sites. For instance in conventional SiO_2, strained or broken bond on the structure there is one oxygen atom missing from the usual lattice configuration, leaving behind a weak Si–Si bond, where each Si atom may be back-bonded to three oxygen atoms or a positive charge is trapped, the Si–Si bond is broken, and the lattice relaxes as in Fig.3.3 [23].

The defects located at oxide and semiconductor interface also produced by irradiation. It has been reported that whether irradiation arrive in interface or just

totally absorbed in oxide layer, interface states are generated. Therefore one assumes that generated e-h pairs and transport these energetic mobile charges may create interface states. All models in the literatures consistent with the idea that precursors of radiation-induced interface traps is a Si atom bonded to three other Si atoms and a hydrogen atom [28-32] .

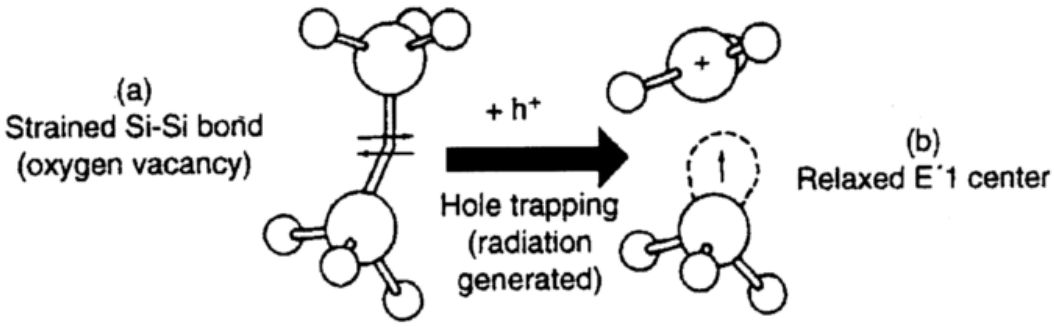

Figure 3. 3: A simple hole trapping mechanism on the SiO_2 layer [23].

When the Si–H bond is broken, the Si is left with an unpassivated dangling bond, as an electrically active defect. The process by which the Si atom is depassivated is where the models differ. Now, it has become clear that the dominant process is a two-stage process involving hopping transport of protons, In the first stage of this process, radiation-induced holes transport through the oxide, and free hydrogen, in the form of protons. In the second stage, the protons undergo hopping transport. When the protons reach the interface, they react, breaking the SiH bonds already there, forming H and a trivalent Si defects [23].

Moreover under applied field in depletion and especially strong inversion regions, the excesses mobile charges accumulate near interface causes a reduction in the surface potential and leading to rise in capacitance value. Surface potential of semiconductor Ψ_r can be derivate by 1D Poisson equation;

$$\frac{d^2\Psi_r}{dx^2} = -\frac{\rho_r(x)}{\varepsilon_s} \tag{3.1}$$

Where ε_s is permittivity of semiconductor and $\rho_r(x)$ is the volume charge density in irradiated condition and given by;

$$\rho_r(x) = q\left(N_D - N_A + p_r - n_t\right) \tag{3.2}$$

For any Ψ_r can be calculated for uniform irradiation steady-state density of electrons and holes as following;

$$n_r = (n_{p0} + \Delta n)\exp(\beta\Psi_r) \tag{3.3-a}$$

$$p_r = (p_{p0} + \Delta n)\exp(-\beta\Psi_r) \tag{3.3-b}$$

Here Δn is excess e-h pairs created per unit volume and formulated by;

$$\Delta n = g_0 \dot{D} \tau_r \tag{3.4}$$

Where g_0 is carrier creation rate in terms of (carrier/ m^3xrad), $\dot{D}$ the indicent dose-rate (rad/s) and τ_r is mean lifetime of carriers in irradiated conditions. Generated carriers in the substrate affect the mean lifetime of carriers. The mean lifetime of carriers in the irradiated condition can be given as

$$\frac{\tau_r}{\tau} = \frac{n_{p0}}{n_{p0} + \Delta n} \tag{3.5}$$

Where τ is average lifetime of minority carriers under unirradiated condition. Using the last two equations ones can obtain;

$$\tau_r = \frac{-n_{p0} + \sqrt{n_{p0}^2 + 4g_0 D\dot{n}_{p0}\tau}}{2g_0 \dot{D}} \tag{3.6}$$

The electric field at the surface in the irradiated condition is given by

$$\Im_{sr} = -\frac{\partial \Psi_r}{\partial x}\Big|_{x=0} = \pm \frac{\sqrt{2}kT}{qL_D} F\left(\beta \Psi_{sr} \frac{n_{p0} + \Delta n}{p_{p0}}\right) \tag{3.7}$$

Where L_D is Debye length, and derivated by

$$L_D = \left[\frac{kT\varepsilon_s}{(p_{p0} + \Delta n)q^2}\right]^{1/2} \tag{3.8}$$

By Gauss's law the space per unit area required to create the field $\Im_{sr}$ can be given

$$Q_{sr} = -\varepsilon_s \Im_{sr} = \pm \frac{\sqrt{2}kT}{qL_D} \varepsilon_s F F\left(\beta \Psi_{sr} \frac{n_{p0} + \Delta n}{p_{p0}}\right) \tag{3.9}$$

The radiation causes an accumulate in the fixed oxide charge and change in the interface charge leading to a change in flatband voltage. The applied voltage (V) is related to surface potential Ψ_{sr} in the irradiated condition as following

$$V = -\frac{Q_{sr}}{C_{ox}} + \Psi_{sr} + \Delta V_{fb} \tag{3.10}$$

The flatband shift can be calculated by ;

$$\Delta V_{fb} = \frac{q}{C_{ox}} (\Delta N_{it} - \Delta N_{ot}) \tag{3.11}$$

Where ΔN_{it} is changes in interface state charges and ΔN_{ot} is changes in oxide trapped charges per unit area created by irradiation and C_{ox} is capacitance per unit area of the oxide layer. It is important to note that radiation- induced excess carrier in radiation- induced changes in interface trapped charge density (ΔN_{it}) can be given;

$$\Delta N_{it} = k_g f_y D t_{ox} f_{it}(N_{it}) \tag{3.12}$$

Where k_g is number of generated e-h pairs per unit dose, f_y the probability density that e-h pairs escapes from recombination, D is incident radiation dose in terms of energy E, $f_{it}(N_{it})$ is interface trapped charges generated per unit irradiation-induced e-h pair. N_{it} is interface charges per unit area which is a function of surface potential given by

$$N_{it} = \int_{E_{VB}+q\Psi_s}^{E_{CB}} D_{it}(E_t) f(E_t) dE_t \tag{3.13}$$

Where $D_{it}(E_t)$ the interface states distributions in energy band gap, ($E_{VB}+q\Psi_s$) and E_{CB} is valance band and conduction band edge at Si surface. The distribution of $f(E_t)$ can be change whether states are donor or acceptor. For donor types;

$$f(E_t) = \frac{1}{1 + g \exp(\frac{E_F - E_t}{kT})} \tag{3.14}$$

whereas for acceptor type interface traps

$$f(E_t) = \frac{1}{1 + g \exp(\frac{-E_F + E_t}{kT})} \tag{3.15}$$

Here E_t is energy of interface traps, E_F is equilibrium Fermi energy level g is degeneracy factor.

The oxide trapped charge density can be formulated by;

$$\Delta N_{ot} = F_H f_T \tag{3.16}$$

Where F_H is total number of holes created in oxide layer given by

$$F_H(\Im_{ox}, E) = t_{ox} \left| k_g(E) f_y(\Im_{ox}, E) D \right| \tag{3.17}$$

Here f_t is fraction of radiation generated holes that are trapped in the oxide layer given by

$$f_T = \sigma_{ht}(\Im_{ox}) \bar{\bar{N}}_{ht} \Delta x \tag{3.18}$$

Where σ_{ht} is local oxide field dependent cross section of hole traps capturing holes, $\overline{\overline{N}}_{ht}$ is average density of hole traps, Δx is width of hole trap regions, t_{ox} is oxide layer thickness, k_g is charge generation coefficient which is function of energy, E_{ox} is electric field in the oxide layer regions.

CHAPTER 4

EXPERIMENTAL PROCEDURE

4.1 Fabrication of MOS

To fabricate MOS capacitors, two main processes were followed. Firstly we clean the all samples considering to standard Radio Corporation of America (RCA) cleaning process. Second process is deposition of $BiFeO_3$ layer onto cleaned wafers and metallization process to make the metal contacts. These two processes explained as followings;

4.1.1 Cleaning Process of Wafers

To fabricate high quality MOS capacitors with a perfect interface, the wafers have to be very clean. Because a well-cleaned semiconductor wafers eliminates many number of surface defects. Impurity free wafers could lead to distorted electrical measurements and sample degradation. Owning to remove organics and heavy metal impurities, the chemical cleaning process were performed in the ultrasonic bath inside the clean room. To fabricate MOS structure, we were used a 4 inch diameter p- type boron doped single crystal (100) Si wafer with a thickness of 500 μm. In this study, the chemical treatment process used to clean the silicon substrate as followings.

In the cleaning process deionized water having a resistance of about 18 Mohm were used. Chemical cleaning procedures were all performed in an

ultrasonic bath. All materials that used in fabrication were sterilized on the boiling water. After that, they were cleaned with hydrogen peroxide, acetone solution and deionized water, respectively. The samples were given a 5 minute ultrasonic bath inside a beaker with acetone followed by methanol, isopropanol, nitric acid and hydrofluoric acid. The ultrasonic bath was performed with deionized water. The beaker with the samples was placed inside the deionized ultrasonic cleaner tube. After the cleaning process, they were blown dry with N_2 so as not to leave residue on samples that could interfere with metallization.

4.1.2 Fabrication of $BiFeO_3$ MOS Capacitors

The $BiFeO_3$ thin films that are used in this study were deposited by after wafer cleaning. The deposited thin films were divided into two groups. First group samples were annealed at 550°C for 30 minutes under atmospheric environment. The second group samples were kept as-deposited and then the ohmic contacts were made of aluminum (Al) deposited by evaporation technique.

RF magnetron sputtering is one of the best techniques to deposit thin films with high quality layer growth, lower contaminations at low temperatures, higher deposition rates with lower voltage operation. Therefore, $BiFeO_3$ films were grown by RF sputtering technique on p-type silicon (100) substrate. The electrons accelerated collide with the outer shell electrons of the neutral sputtering gas atoms in their path. The neutral gas atoms are getting to ionized by accelerated electrons. Due to their positively charged ions (Ar^+), it is accelerated towards to the cathode and strike the target. Now, it is time to eject the electrons for the target. The electrons ejected from the target return to a ground state of the argon gas due to the conservation of energy law, and so the resultant neutral gas atoms

gain energy. However, after a short period the argon releases the energy in the form of a photon, called as the plasma. After these points Ar^+ ions had sufficient energy to eject to targets material to deposit the surface of wafers. This process can be seen in Fig. 4.1 in detailed.

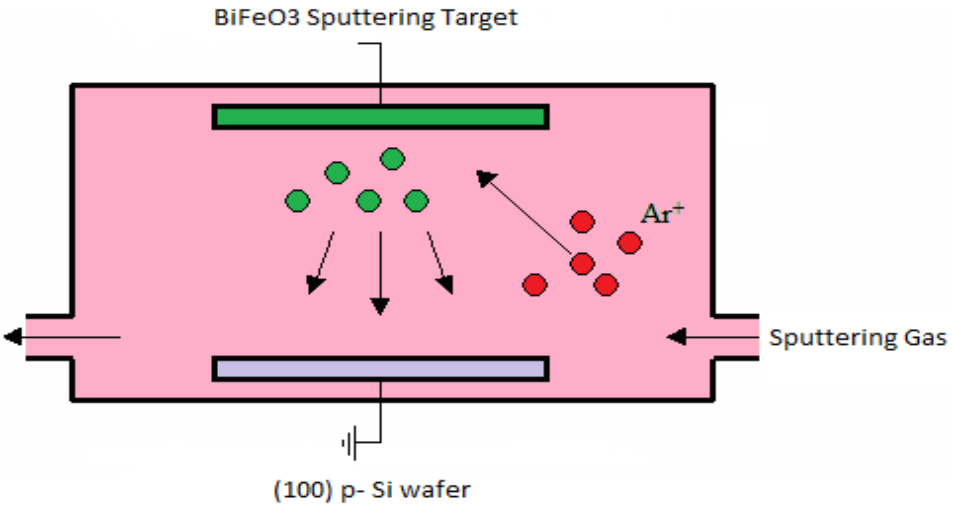

Figure 4. 1: Schematic diagram of the sputtering

$BiFeO_3$ targets with 3'' diameter and a 0.125'' thickness were used as sputtering target. The sputtering systems can be seen from Fig. 4.2. The base pressure before sputtering was $1.1x10^{-5}$ Torr then 150 W powers is applied between the target and plates at 0 ^{0}C in 99.99% pure argon (6 sscm for sputtering gas) atmosphere with 0.17 nm/s growth rate at room temperature. The pressure was measured to be nearly $6.7x10^{-3}$ Torr during film sputtering process. The thickness of films corrected to be 300 nm by ellipsometry. The deposited thin films were divided into two groups. First group samples were annealed at 550 °C for 30 minutes under atmospheric environment. The second group samples were kept as-deposited.

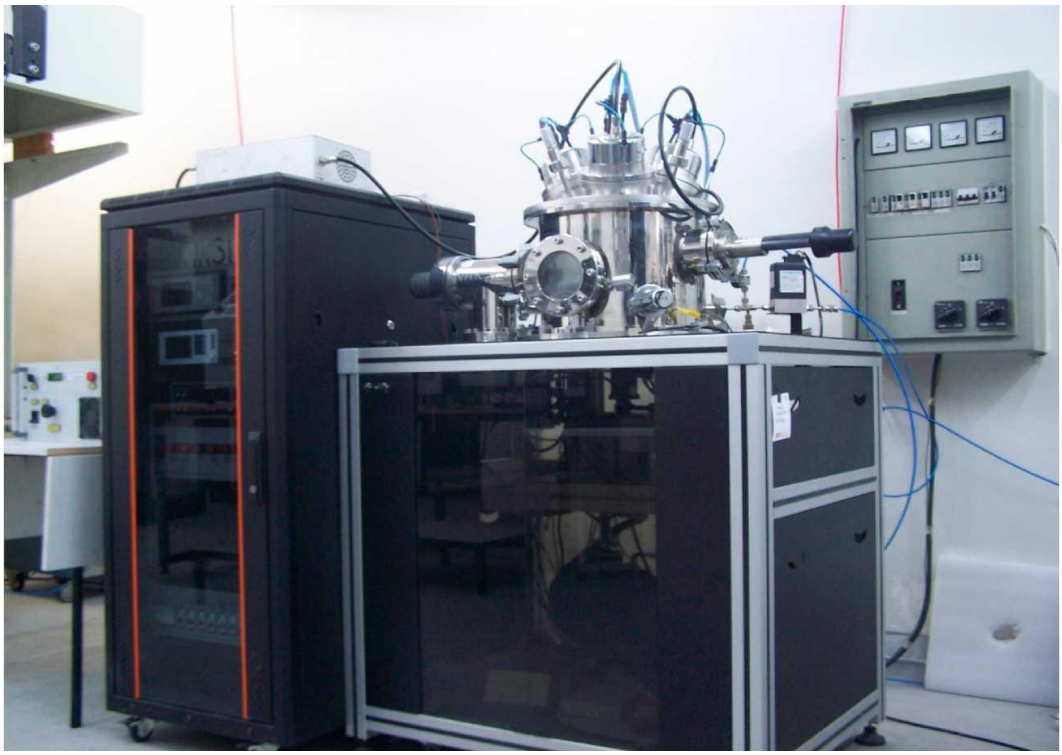

Figure 4. 2: Vaksis three magnetron DC/RF sputtering system in Physics Department in Middle East Technical University.

The XRD and SEM measurements were performed for both as-deposited and annealed samples for structural characterization. X-Ray diffractometer is one of the most important instruments to examine the structure of a material from the scattering pattern. The working mechanism depends on the interaction between high-energy beams of radiation or charged particles and a material. In this work, the phase compositions of the samples are characterized by XRD investigation with the aid of a Rigaku MultiFlex diffractometer (Fig. 4.3) with Cu Kα radiation (=1.5418 Å) in the range 20°–60° at a scan speed of 3°/min and a step increment of 0.02° at room temperature

Figure 4. 3: Rigaku MultiFlex X-Ray Diffractometer

Scanning electron microscope (SEM) pictures the surface of a material with the aid of a high-energy beam of electrons in a raster scan pattern. After the interaction between the incident electrons and atoms in the material, a signal containing the information about the surface topography, texturing and composition of the material appears. In this thesis, crystallinity and grain size the of samples are studied by Scanning Electron Microscopy SEM JEOL 6390-LV in Fig. 4.4. The back ohmic contacts were made of aluminum (Al) deposited by evaporation technique on the back side of wafers. The evaporator is shown in Fig. 4.5. The front Al electrodes were formed in circular dots with 1 mm diameter by Al deposition through a shadow mask at a base pressure of 1.2×10^{-5} Torr.

Figure 4. 4: Scanning Electron Microscope

Gate contact materials must be a good conductor, due to signal propagation speed through the material, and it cannot act as a depletion layer in scaled down technologies. Moreover, it is also very easy to get wire contacts and low-cost materials.

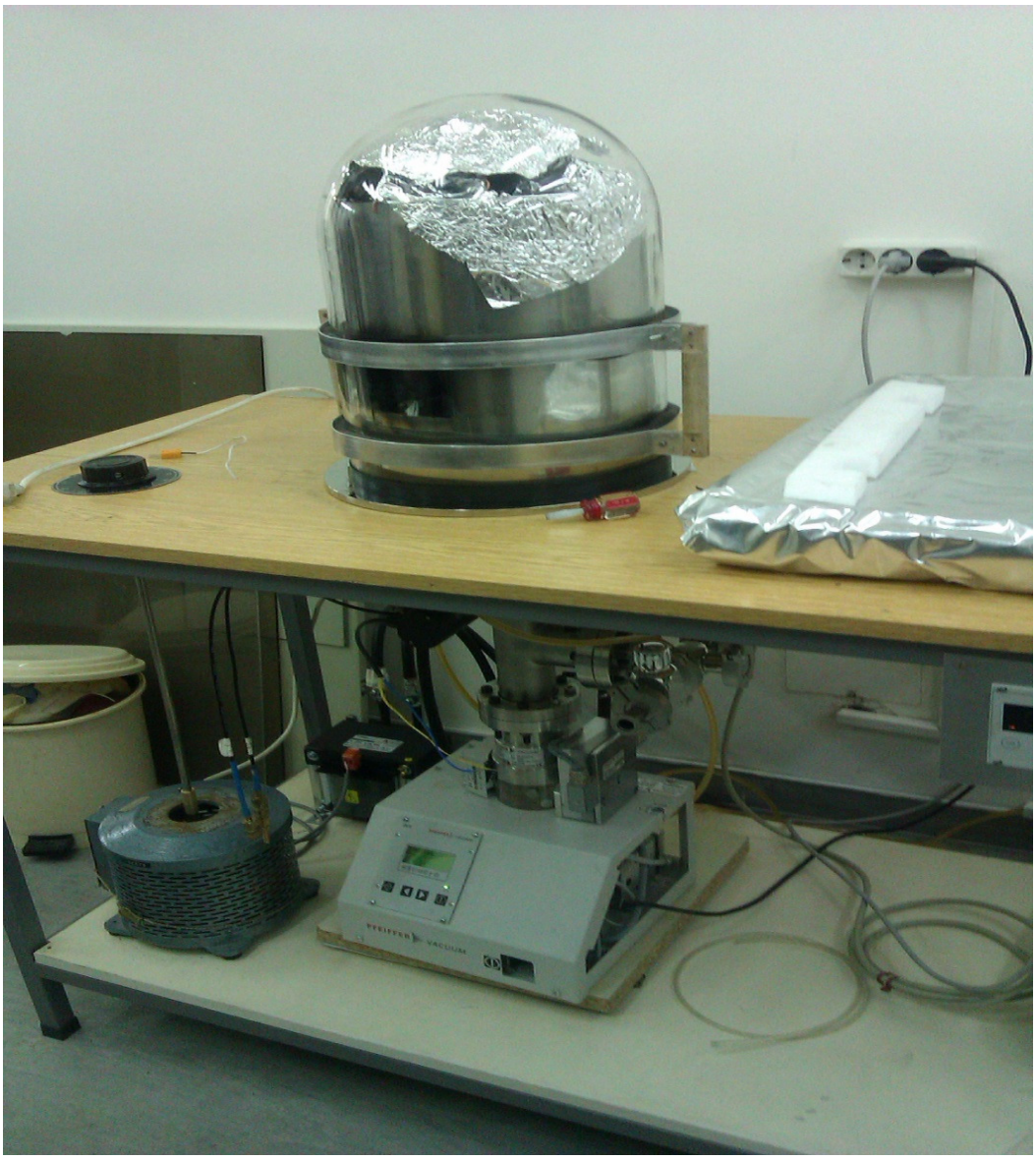

Figure 4. 5: Evaporator system for making ohmic contacts

4.2 Measurement Materials and Irradiation of Fabricated Devices

The all electrical characterizations were performed by Hewlett-Packard 4192A LF impedance analyzer shown in Fig. 4.6 located in the GUNAM-METU laboratory. Capacitance- Voltage (C-V) and Conductance- Frequency (G/ω-F) were measured to different frequencies and voltages, to examine detailed electrical characterization before the irradiation of samples.

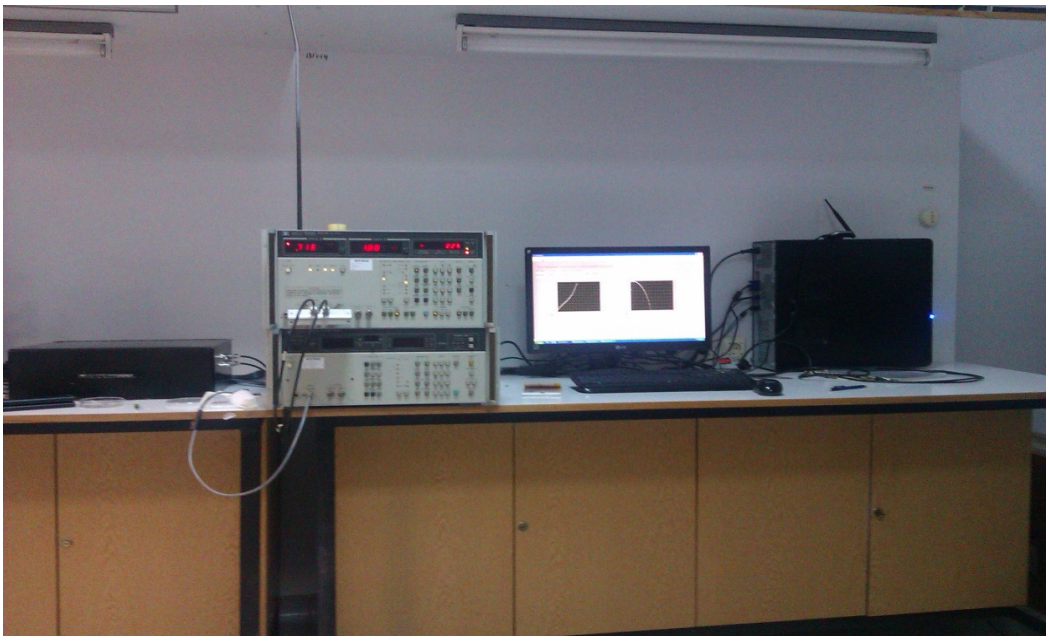

Figure 4. 6: Hewlett-Packard 4192A LF impedance analyzer system

After analysis of the measured data, samples were irradiated using the GAMMACELL 220 Co-60 radioactive source from 0.5 grays to 16 grays at a dose rate of 0.0030 Gy/s. The mean energy of the gamma radiation used in this study is 1.25 MeV. Source is placed into drawers lead protection. The distance between sources and fabricated samples are approximately 30 cm. In order to investigate radiation effects and possible usability of $BiFeO_3$ as a dielectric layer in MOS-based radiation sensors, high frequency (1 MHz) C-V measurements were performed after all given doses by using Hewlett-Packard 4192A LF impedance analyzer.

CHAPTER 5

EXPERIMENTAL RESULTS AND DISCUSSION

5.1 Material Characterizations

The crystal structure and phase identifications of the films were carried out using X-ray diffraction (XRD) for as-deposited and annealed samples. XRD patterns of the $BiFeO_3$ film is shown in Fig. 5.1. As seen in Fig. 5.1, the film was in amorphous form before annealing. After annealing at temperatures of 550°C, the polycrystalline $BiFeO_3$ layer with impurity phases was found in the XRD analysis. This displays that one may possible get $BiFeO_3$ polycrystalline impurity phase films in the annealing process.

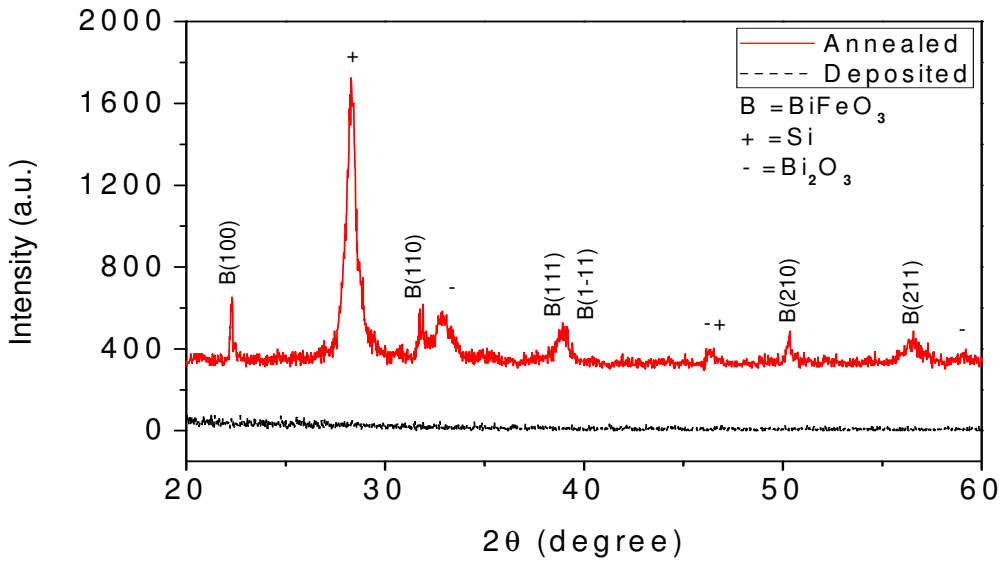

Figure 5. 1: XRD analysis of $BiFeO_3$ films on Si (100) substrate.

The peaks were indexed using the International Center for Diffraction Data (ICDD) with card no-72-2035. By means of (100), (110), and (111) peaks in the XRD pattern, the lattice constants of of the films were calculated to be a = 3.969 Å and c = 4.061 Å. Accordingly, the c/a ratio of the $BiFeO_3$ film was calculated to be 1.023. These results demonstrate that the annealed films have tetragonal structure with space group P4mm [33] which is different from the bulk crystal structure of $BiFeO_3$ known to be a rhombohedrally distorted perovskite structure. This may be attributed to the presence of the compressive strain in the films.

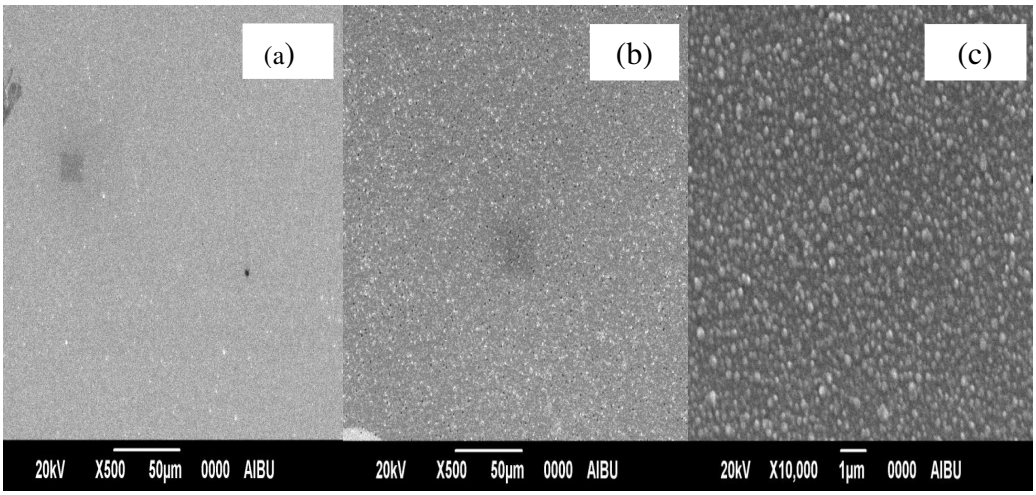

Figure 5. 2: Scanning electron microscopy (SEM) images: a-) as-deposited; b-) annealed; c-) more details of annealed $BiFeO_3$ thin film.

To study the surface morphology of the films, SEM images of as-deposited and annealed $BiFeO_3$ films are shown in Fig. 5.2. As-deposited and annealed $BiFeO_3$ films exhibit different nanostructures. It is evident in Fig. 5.2 that as-deposited films were amorphous. The annealing process transformed the surface morphology and the porosity of the films increased. High temperature treatment provided more crystallization in the films which can be seen more specifically in Fig. 5.2(c).

5.2 Results for Fabricated MOS Capacitors

In order to examine annealing effects to electrical C-V characteristic of fabricated device, C-V measurements were performed in Fig. 5. 3 (a) at 1MHz for as-deposited and annealed samples. As-deposited C-V curve exhibited lower capacitance values compared to annealed devices characteristics, owing to low interface quality and high leakage current at $BiFeO_3$/Si stack [34-36]. High temperature heat treatment provide to getting better interface quality and decrease the density of trap states in device structure [36]. Therefore, it reduce the leakage through the oxide and device exhibits more stable performance. The frequency dependent C-V hysteresis is shown in Fig. 5. 3 (b) for annealed samples. The C-V hysteresis of the device exhibit a MOS-type behavior with accumulation, depletion and inversion regions. The variation of measured capacitance values at different frequencies is mainly due to series resistance and frequency dependent charges [9,37]. At high frequencies, frequency dependent interface states are less influenced less by applied electric fields and thus, the capacitance contribution of interfaces states to the measured capacitance is almost equal to zero [37,38]. Therefore this causes the variations on the measured capacitance. The width of C–V hysteresis loop exhibited variations under frequency dispersion. It decreased with increasing the frequency. Domain wall motion is frequency dependent and can in principle happen in the frequency region below ~1 GHz. However, care was taken that the maximum applied bias between from -6 V to 0 V in measurements which was below the switching threshold of Bismuth Ferrite thin films with a thickness of 300 nm [7,39]. Therefore, main contribution the flat band voltage shifts (ΔV_{fb}) on the C-V hysteresis is results of defects distribution on the structure. The frequency response of traps gives information about their location

into the volume, the distance of traps from the interface with the substrate increasing with decreasing frequency. The highest ΔV_{fb} is obtained at lower frequencies. Therefore, the large clockwise hysteresis loop presented in $BiFeO_3$/Si stacks at different frequencies indicated charge trapping in the oxide. In other words these results demonstrate a low defect density at the interface with the substrate, most of the traps such as oxide trapped charges, fixed charges being located in the oxide volume [36]. The curves did not show any kinks at low frequency side, it is also indicating the good interface between $BiFeO_3$ and p-Si [39].

To investigate the dielectric constant of the $BiFeO_3$ layer, the reverse biased capacitance of the MOS structure was measured at high frequency (1 MHz) in which impurity effects such as interface state contributions are eliminated.

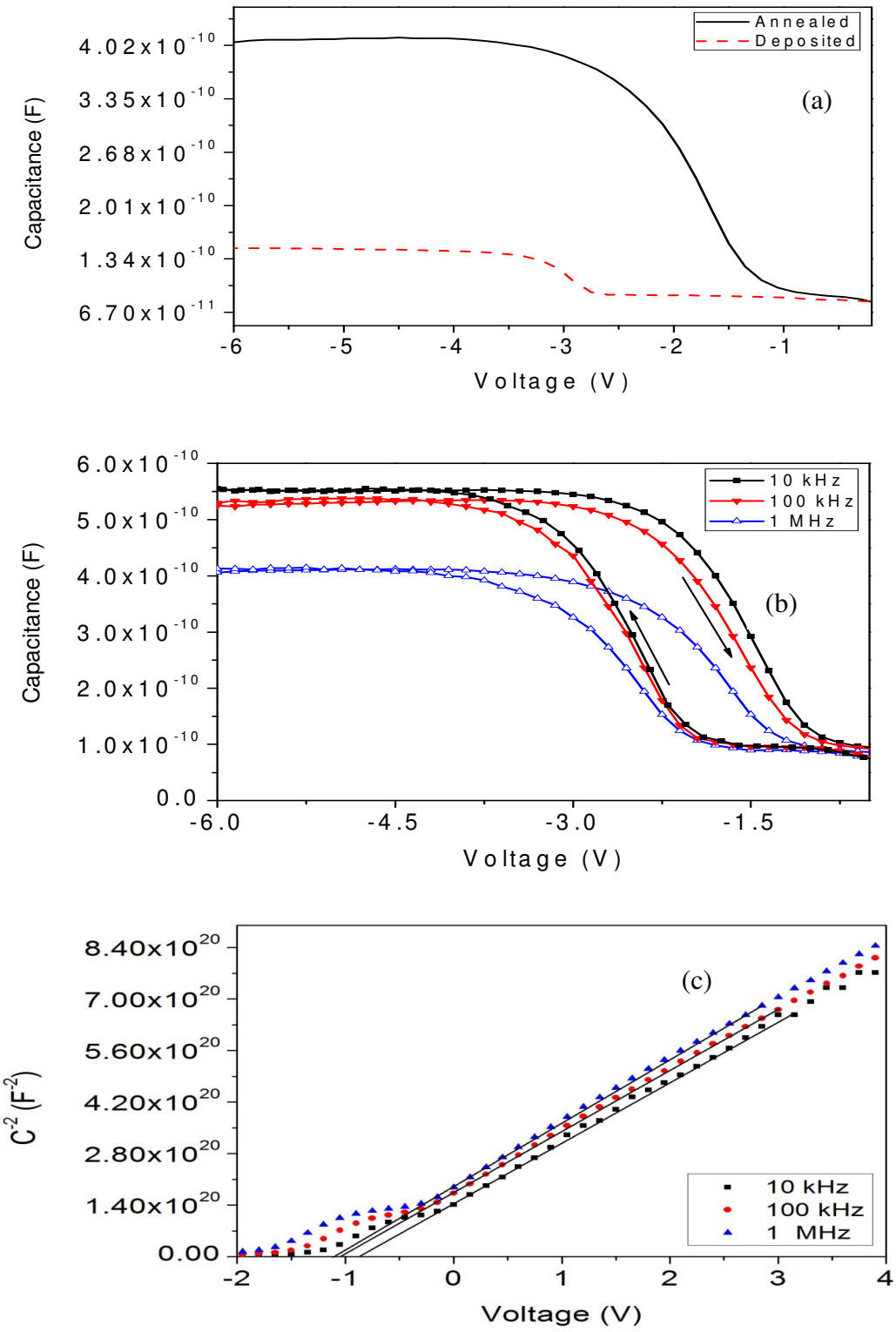

Figure 5. 3: Characteristic (a) C-V for as-deposited and annealed samples at 1 MHz and the variation of (b) C-V hysteresis and (c) reserve bias C^{-2}-V plots of $BiFeO_3$ MOS capacitor at different frequencies.

The measured capacitance value of the $BiFeO_3$ MOS capacitor is $4.1x10^{-10}$ F in the strong accumulation region, and the dielectric constant (k) were calculated and found to be about 18 which is in agreement with reported values for defect containing $BiFeO_3$ [40] and lower than low-defect material where k~40.

Moreover, comparing the experimental value of flat band voltage, V_{fb}, of the device with ideal values, the flat band voltage shifts to more negative voltage values. The lower dielectric constant and a larger flatband voltage shift, suggesting a parasitic phase crystallized $BiFeO_3$ structure and a high oxide charge density [41]. Impurities in the oxide structure may trap the holes and also dangling bonds, particularly localized positive ions such as the Fe^{+3} and Fe^{+2} sites in the $BiFeO_3$ surface [42] act like positive charges. These amounts of positive charge located in the oxide layer are the primary reason for flat band voltage shift of the capacitor [4,26,43,44]. The effective charge densities in the oxide layer were calculated using with Eq. (2.15). The effective charge density Q_{eff} of $BiFeO_3$ MOS capacitors is calculated for different frequencies and obtained Q_{eff} values are given in Table 5. 1. It is seen that Q_{eff} decreases with increasing applied voltage frequency which leads to a shift in flat band voltage. Due to the frequency dependent charges in the MOS devices, the Q_{eff} showed variations with applied voltage frequency. At high frequencies these trapped charges cannot response the applied voltage frequency, hence the effective charge density decrease with increasing the applied voltage frequency.

Moreover, to calculate some basic electrical characteristics of MOS devices, C^{-2}–V characteristics, obtained from reserve bias C-V measurements, were plotted and are displayed for frequencies of 10 kHz, 100 kHz and 1 MHz in Fig. 5. 3 (c). The frequency dependent barrier height, ϕ_B, doping concentration, N_D

and the image force barrier lowering $\Delta\phi_B$ of the device were calculated from the Eq. (2.18) and (2.19). In addition, the Debye length, λ_n is known as an effective shielding distance due to external electric field that penetrates a neutral semiconductor surface without substantially perturbing the semiconductor away from neutrality, and were calculated by Eq. (2.20). These calculated electrical characteristics are given in Table 5.1. The results demonstrate that both ϕ_B and λ_n parameters of the device increase with increasing frequency, and resulting from increases in the slope of the linear part of C^{-2}–V plots, N_D values decrease with increasing frequency. Interface states may affect the C-V characteristics of MOS structures causing a bending of the C^{-2}-V curve as well as affecting the ϕ_B and λ_n parameters [45]. Therefore, the behaviors of ϕ_B and λ_n parameters can be attributed to frequency dependent interface charges.

Table 5. 1: Some basic electrical characteristics of $BiFeO_3$ MOS devices

Frequency	V_D	E_F	N_D	$\Delta\phi_B$	ϕ_B	λ_n	Q_{eff}
kHz	eV	eV	$x10^{15}$ cm^{-3}	meV	eV	nm	$x10^{11}$ Ccm^{-2}
10	0.834	0.2640	1.29	14.1	1.10	102	7.22
100	1.042	0.2643	1.28	16.3	1.32	103	7.18
1000	1.134	0.2644	1.26	17.1	1.41	105	6.31

The interface state density at $BiFeO_3$/Si interfaces is a useful guide to quality of MOS devices. The presences of interface charges affects device response and performance [21]. The conductance technique is one of the mostly used methods to calculate the interface state density in MOS structures. It is based on conductance losses resulting from the exchange of majority carriers between

the interface states and majority carrier band of the semiconductor when a small ac signal is applied to the MOS structures [21,46]. The relation between conductance and interface states can be calculated using Eq. (2.22). The graph of G_p/ω versus frequency of annealed device is shown in Fig. 5.4 for accumulation, depletion and inversion regions voltages.

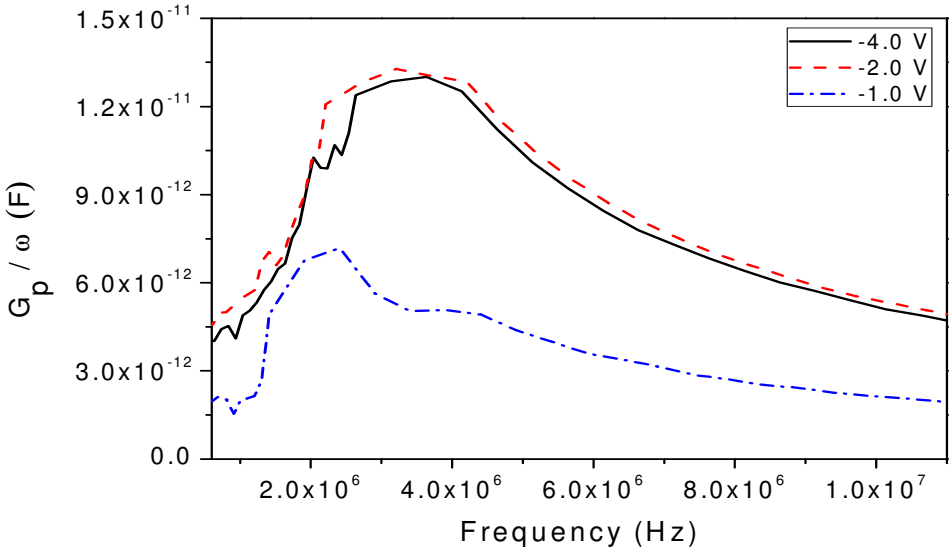

Figure 5. 4: G_p/ω vs. frequency plots of $BiFeO_3$ MOS capacitor at different biases

The G_p/ω-F characteristics give a peak in accumulation and depletion regions voltage due to the presence of high number of majority carriers. Moreover, the frequency dependent conductance characteristics prove the presence of frequency dependent interface states. The highest value of interface state density, $D_{it,,}$ was calculated to be $2.50\text{x}10^{11}$ $eV^{-1}cm^{-2}$. The calculated D_{it} value is not high enough to pin Fermi level of Si substrate corrupting device operation [47,48]. However, it may cause some deviation from expected ideal behavior of MOS devices.

5.3 Results for Irradiated MOS Capacitors

Ionizing radiations such as gamma rays and X-rays generates defects, interface trap- and oxide trap-charges in MOS structure [24]. Hence, ionizing radiation causes a shift in flat band and midgap voltage. One of the useful methods to analyze C-V characteristics of the MOS structures can be used to quantify the density of charge traps in the oxide and at the semiconductor/oxide interface [16]. Radiation induced trapped charges in the oxide determined from the mid-gap voltage shifts due to interface states are expected to be neutral at mid-gap and would not contribute to the mid-gap voltage shift.[49]. In addition, interface state density can also be determined from flat band voltage shifts. The C-V curves of the $BiFeO_3$ MOS capacitor before and after gamma irradiations at high frequency are illustrated in Fig. 5.5. It demonstrates that the measured capacitance remains almost the same after irradiation and basically modifications being a translation towards positive voltage axis. A large number of electron-hole pairs are generated in $BiFeO_3$ layer during irradiation, and the some number of those charges were trapped by defects in the layer, this process has been denoted as ionizing the defects [50].

The type of the trap states responsible for the voltage shift shows that the voltage shift is mostly due to trapped oxide charges rather than the interface states [24]. Thus, it can be concluded that for our study number of negative trapped charges in oxide layer enhance result of irradiation. It is well-known that the electrons are much more mobile than the holes and they are swept out of the oxide, thus positive charges are trapped in oxide layer results of irradiation [5,23,24]. However, in this study Fig. 5.5 indicates that negative charges are trapped.

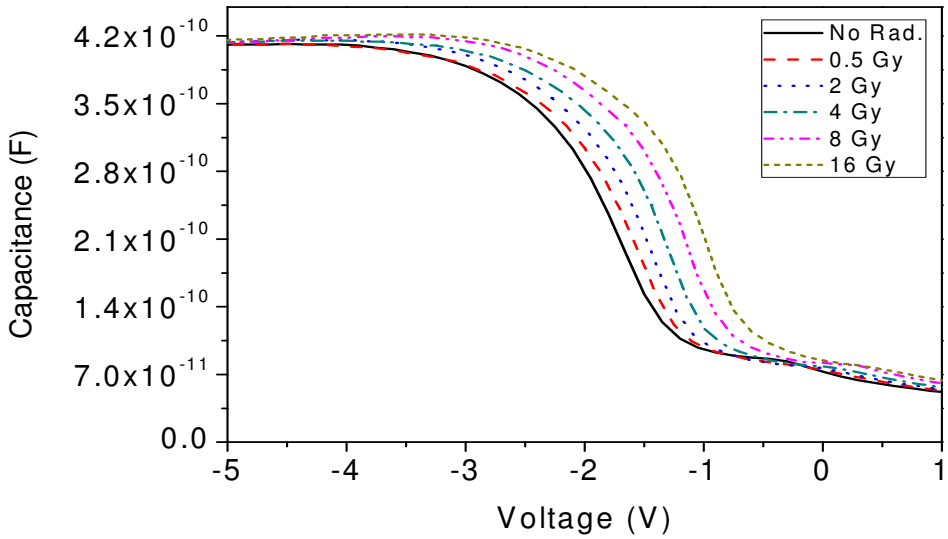

Figure 5. 5: C-V curves of $BiFeO_3$ MOS capacitor before and after gamma irradiation at different doses.

Radiation can ionize the atoms of $BiFeO_3$ and generates lattice defects as oxygen vacancies. The ionized atoms in the structure such as Fe^{+2} and Fe^{+3} exhibit acceptor-like behaviors, hence devices exhibit p-type conductivity. Electrons are then able to easily jump from the valence band into the acceptor bands where they are trapped, the hopping mechanism between Fe^{+3} and Fe^{+2} sites support this behavior. It is worth noting that especially Fe^{+2} ions are the likely trap center in $BiFeO_3$ structure reported by authors [51,52]. Moreover, oxygen vacancies are also important parameter of negative charge traps due to electrons can be trapped from cluster of oxygen vacancies [53]. Therefore, these two trap states are basic reasons of the flat band shifts toward positive voltages. Additionally, several papers demonstrate that most of the defects such as interface states, oxide traps and oxygen vacancies are located at the interface of the domain wall boundaries and at the interface between $BiFeO_3$ and Si layer and these defects can trap mobile charges [53,54]. The variations on the distribution of domain walls such as pinning of domain walls by defects sites generated by radiation in ferroelectric oxide can

lead to changes in electronic characteristics of device [50,55,56]. Therefore, the electrons may be captured at these traps located at the surface of domains and/ or the interface of $BiFeO_3$/Si. Thus, ferroelectric domain walls in $BiFeO_3$ may have also responsible from negative trapped charges lead to shift flatband voltage toward more positive values.

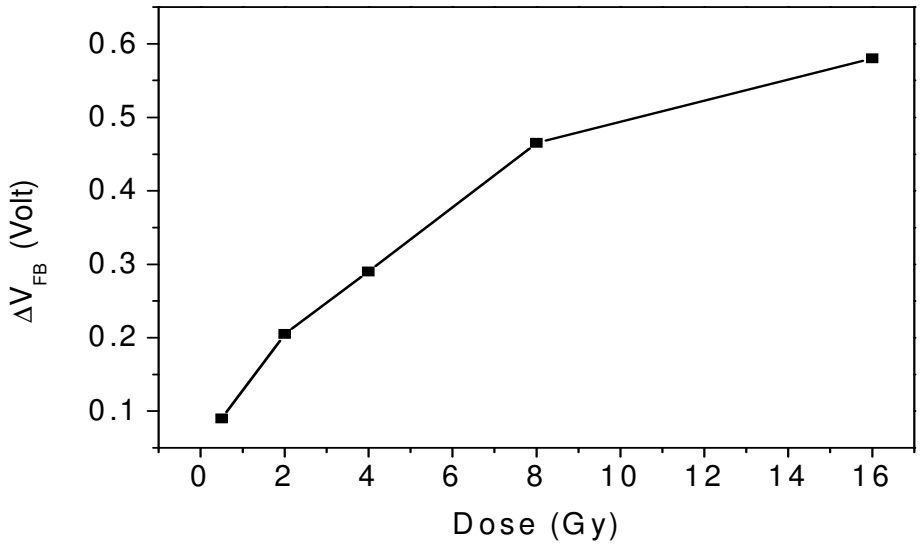

Figure 5. 6: Flatband voltage shift of $BiFeO_3$ MOS capacitor from 0.5 Gray to 16 Grays.

The response of flat band voltage shifts of fabricated MOS capacitor are illustrated in Fig. 5.6. The doses applied to the devices were varied from 0.5 to 16 Grays. The response of the devices is found to be almost linear over given dose range especially from 0.5 Gray to 8 Gray. This characteristic of device is crucial for MOS capacitor usage as radiation sensors [1]. Moreover, the distribution of interface states may be the reason of reduction of linearity of flat band shift between 8 Gray to 16 Gray.

The net oxide trap-charge densities (ΔN_{ot}) can be estimated from observed midgap voltage shift (ΔV_{mg}) as given in Eq. (5.1) [57].

$$\Delta N_{ot} = -\frac{C_{ox}\Delta V_{mg}}{qA} \tag{5.1}$$

where C_{ox} is the oxide capacitance with value of 4.04×10^{-10} F, q = (-1.602×10^{-19} C) is electric charge, and A is the capacitor area. From this equation, ΔN_{ot} was calculated to be ~ 3.21×10^{10} cm^{-2} after 0.5 Gray and ~ 6.37×10^{11} cm^{-2} after 16 Gray for the $BiFeO_3$ MOS device. Interface trap-charge densities (ΔN_{it}) were calculated from flat band voltage shift (ΔV_{FB}). This must take into account both the oxide trapped charge and the charge trapped on interface states between flat band and mid gap [58]. Similarly, ΔN_{it} can be estimated from the midgap-to-flat band stretch-out of the C–V curves by [57]

$$\Delta N_{it} = -\frac{C_{ox}\left(\Delta V_{fb} - \Delta V_{mg}\right)}{qA} \tag{5.2}$$

where C_{ox} is the oxide capacitance, q is electric charge, and A is the capacitor area. Using Eq. (5.2), ΔN_{it} was estimated to be ~ 3.22×10^{9} cm^{-2} after 0.5 Gray and ~ 5.79×10^{10} cm^{-2} after 16 Gray for the $BiFeO_3$ MOS device. The distribution of ΔN_{ot} and ΔN_{it} corresponds to given doses are displayed in Fig. 5.7 and Fig. 5.8, respectively.

The variations in the distribution of ΔN_{it} compared to ΔN_{ot} are observed. The trend in ΔN_{ot} is increase almost linearly from 0.5 Gray to 16 Gray and supports buildup of net oxide trapped charge in the oxide bulk.

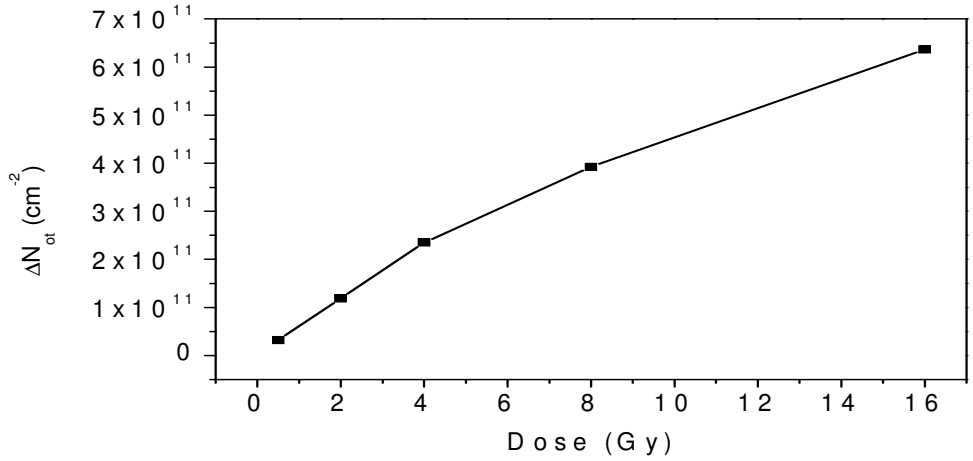

Figure 5. 7: Oxide trap density ΔN_{ot} of $BiFeO_3$ MOS capacitor.

On the other hand, it is seen that the response of ΔN_{it} to radiation is more complicated. The density of interface states enhance almost linearly from 0.5 Gray to 4 Gray. However, it starts to decrease up to 8 Gray. This can be attributed to the passivation of the Si surface due to the deposition layer ($BiFeO_3$) [59]. Interface states are generated dramatically resulting from irradiation between 8 Grays to 16 Grays.

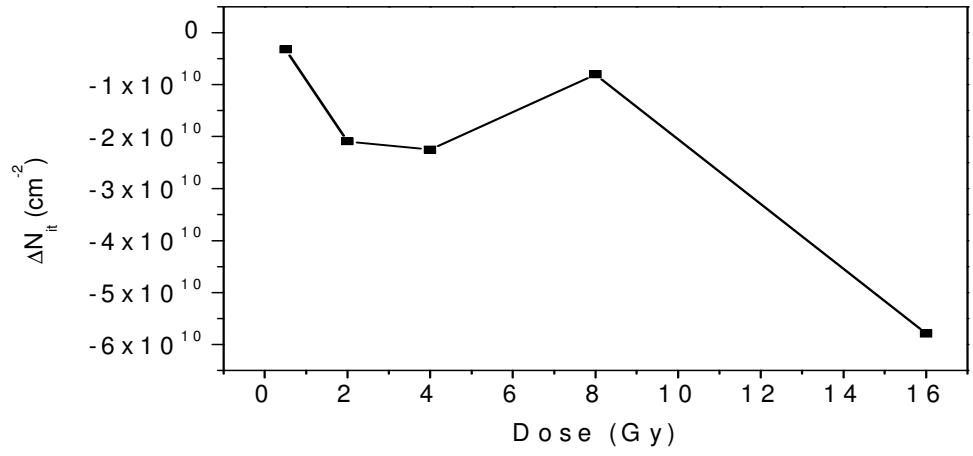

Figure 5. 8: Interface trap density ΔN_{it} of $BiFeO_3$ MOS capacitor.

CHAPTER 6

CONCLUSIONS

The structural, electrical properties and radiation response of $BiFeO_3$ MOS capacitor have been studied for gate dielectric applications. The structure of $BiFeO_3$ thin film has been performed by XRD and SEM measurements. XRD and SEM analysis showed that annealed film structures are in tetragonal polycrystalline form with some impurity phases. The variation of measured capacitance values at different frequencies has been observed. This non-ideality can be ascribed to the frequency dependent charges and series resistance effects at interfacial oxide layer and interface between oxide and semiconductor. In addition, the dielectric constant was calculated to be 18 at high frequency measurements which has an agreement with impurity phase $BiFeO_3$ layers [60]. Moreover, barrier height, effective shielding distance and flat band voltages showed variations with applied voltage frequency for annealed samples. This non-ideality can be ascribed to the frequency dependent charges at interfacial oxide layer and interface between oxide and semiconductor. The frequency dependent conductance characteristics prove the presence of frequency dependent interface states. The highest effective charge density and interface state density were calculated to be 6.31×10^{11} C cm^{-2} and 2.50×10^{11} $eV^{-1}cm^{-2}$, respectively. These obtained electrical parameters are of the same order as reported by some authors for MOS devices [44,61,62]. Therefore it is seen that $BiFeO_3$ dielectric layer in fabricated MOS device shows a stable

insulation property over the entire investigated applied voltage range. Additionally, ignoring effects of frequency dependent charges can lead to significant errors in the analysis electrical characteristics of MOS capacitor.

In order to study response of MOS capacitor to gamma irradiation, MOS devices were irradiated using a Co-60 gamma source from 0.5 to 16 Gray at a dose rate of 0.0030 Gy/s. C–V measurements were performed prior to and after irradiation at high frequency. Results demonstrate that the measured capacitance remains almost the same after irradiation and basically modifications being a translation towards positive voltage axis. The type of the trap states responsible for the voltage shift shows that the voltage shift is mostly due to trapped oxide charges rather than the interface states. Thus, it can be concluded that for our study number of negative trapped charges in oxide layer enhance result of irradiation It is worth to noting that the generated positive ion sites, oxygen vacancies and variations in ferroelectric domain wall boundaries may be reasons of negatively trapped charge in oxide layer. In addition, flat band voltage shift increases linearly due to irradiation. It is also found that the numbers of oxide trap-charges are generated much more than that of interface trap-charges. Thus, oxide trap-charges are more effective comparing to interface trap-charges for the flat band voltage shift in $BiFeO_3$ MOS structure. Consequently, these results suggest that $BiFeO_3$ is a promising material for the future gate dielectric applications particularly from 0.5 to 8 Gray in radiation sensors.

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