ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

DESIGN AND IMPLEMENTATION OF A BROADBAND IMPEDANCE MATCHING NETWORK USING SIMPLIFIED REAL FREQUENCY TECHNIQUE MATCHING 6.25 OHM OUTPUT IMPEDANCE OF A HIGH SPEED DAC TO 50 OHM

M.Sc. THESIS

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Thesis Advisor: Pof. Dr. Serdar ÖZOĞUZ

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

BİR HIZLI DAC' IN ÇIKIŞ KATI İÇİN, SRFT YÖNTEMİ İLE BİR GENİŞ BAND EMPEDANS EŞLEŞTİRİCİ AĞI TASARIMI VE GERÇEKLEŞTİRİLMESİ

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OCAK 2015

Hamid Yadegar Amin, a **M.Sc.** student of ITU **GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY** student ID 504111240, successfully defended the **thesis** entitled "**Design And Implementation of A Broadband Impedance Matching Network Using Simplified Real Frequency Technique Matching 6.25 Ohm Output Impedance of A High Speed DAC to 50 Ohm**", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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January 2015 Hamid YADEGAR AMIN

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SUMMARY

One of the main concerns in RF design is transferring the power between terminals with different terminations. In this regard, impedance matching networks can play a crucial role in surmounting this issue. As the master thesis, this study was therefore conducted for purpose of designing and implementation of an impedance matching network as the output stage of a high speed DAC matching 6.25Ω to 50Ω. The design was accomplished by using SRFT (Simplified Real Frequency Technique) introduced first by Prof. B. S. Yarman and H. J. Carlin in 1982. This thesis consists of six chapters, dealing with the theory of the project, the software coding process in Matlab, simulations and verification, test circuit design and realization and the integrated design in TSMC 0.180 um technology process. In the first chapter, the motivation of the study is investigated. As it is mentioned, in order to design a high-speed data converter satisfying defined design goals, there is a need for a small output load which in this study is a resistive load with value of 6.25 ohm. Since the value of output load is different from the standard common loads such 50 ohm or 75 ohm there is a need for an impedance matching network for avoiding power dissipation. The second chapter deals with fundamentals of the chosen approach for designing desired impedance matching network. The third chapter explains how the technique is implemented in Matlab programs. In the forth chapter, the obtained circuit from the chapter 3 is simulated by ADS Keysight simulator. Also, some realization techniques such as lumped to distributed conversions are applied during the simulations. The next sections are about realization and measurement of the designed network, in this sections the study is focused on measurement techniques. Since all of the measuring devices such as vector network analyzers use ports with characteristic impedance of 50 ohm, for sake of applying a straight forward measuring, two test circuits with two different techniques are designed and implemented during chapter 5. As each of the test circuits includes a transformer before the designed impedance matching network and after the 50 ohm port of the measuring device, such as VNA, converting 50 ohm to 6.25 ohm . Chapter 6 tries out the integrated version of the design. In this regard, the TSMC 180 um technology process is used. During this chapter the design is implemented with component models presented in RF library. Although the design is successful in maintaining the transducer power gain's wave form but it fails to illustrate good results in gain; giving a lossy network.

BİR HIZLI DAC' IN ÇIKIŞ KATI İÇİN, BASİTLEŞTİRİLMİŞ REAL FREKANS TEKNİĞİYLE BİR GENİŞ BAND EMPEDANS EŞLEŞTİRİCİ AĞI TASARIMI VE GERÇEKLEŞTİRİLMESİ

ÖZET

RF tasarımında karşılaşılan başlıca sorunlardan biri, farklı sonlandırıcılar arasındaki güç aktarımındaki kayıplardır. Empedans eşleştirici ağ, bu sorunu giderme konusunda önemli bir katkı sağlar. Bu tez çalışmasında tasarlanan empedans eşleştirme ağı bir yüksek hızlı DAC'ın çıkış katı olarak kullanılmış ve 6.25 ohm'u 50ohm'a eşleştirilmesi amaçlanmıştır. Tasarım, B. S. Yarman ve H. J. Carlin tarafından önerilen SRFT (Simplified Real Frequency Ttechnique) Basitleştirilmiş Real Frekans Tekniği yöntemi kullanılarak gerçekleştirilmiştir. Bu tez, altı bölümden oluşmaktadır. Birinci bölümde çalışmanın esas motivasyonlar ve sorunlardan bahsedilmiştir. İkinci bölümde sorunu gidermek için yaklaşım ve bu yaklaşım için kullanılan yöntemin teorisi anlatılmıştır. Üçüncü bölüm, yötemi matlab kodlarla uygulamaktan bahs ediyor. Bu bölümde Matlab'da kodların nasıl yazıldığıyla ilgili bilgiler veriliyor. Ayrıca bu bölümde tasarım Matlab kodlarından sentezleniyor. Bölüm dörtte benzetim ve doğrulama tekniklerinden bahsediliyor. Bölüm beşte tasarlanan ağ gerçekleniyor. Ayrıca ağın ölçümü için iki test devresi tasarlanıp kırmık üstü imalat sonuçları sunuluyor. Son bölüm olarak tasarlanan ağın integrated versyonu 0.18um CMOS TSMC teknoloji süreci kullanarak tasarlanıyor.

Birinci bölümde, DAC'ın çıkış katıyla ilgili bazı açıklamalar yapılmıştır. Kullanılan DAC, akım çıkış modlu DAC olduğu için çıkış sinyeli akım olarak yüke basar. Bu durumda, yük akım seviyesini direnecek şekilde ayarlanması gerekiyor. Bu yük DAC'ın diğer parçaları gibi çip içinde tasarlanıyor. O yüzden, srecin dökümanları incelenmeli. Bilinen gibi,TSMC teknoloji prosesi altı kat farklı metallerden oluşmaktadır. Böylece, yük için kullanılan metallerin özellikleri çok önemli bir faktör sayılır. Bu çalışmada, metal 6 ile sinyelin yüke doğru gittiği yol sağlanıyor ayrıca, metal5 ,metal4 veya metal3'ten oluşan bir şerit sinyelin toprağa gitmesini sağlıyor. Üç farklı alternatifi inceledikten sonra, çıkış akıma direnecek yükün değeri hesaplanmalıdır. Hesaplamalar ardından, belirlenen çıkış akımı için en uygun direnç 6.25 ohm tespit edildi. Tüm incelemeler, TSMC dökümanlarında verilen değerler üzere hesaplanmıştır. Bahsedildiği gibi, DAC 6.25 ohm'luk bir yükü kullanacaktır. Bu durumda, DAC'ın standart yüklerlre , örneğin 50 ohm veya 75 ohm, bağlanması için bir empedans eşleştirme ağına ihtiyaç duyulur. Bu çalışmada, Basitleştirilmiş Real Frekans Tekniği kullanarak tasarıma yol alındı. Tasarım amacı bir bant geçiren empedans eşleştiricinin tasarlanmasıdır. Bant geçiren ağın orta frekansı 2.4 GHz ve bant genişliği 400 MHz olarak belirlenmiştir. Basitleştirilmiş Real Frekans Tekniğin sağladığı avantajlara göre bu yöntemi kullanarak tasarım başlatıldı. İkinci bölümde, tekniğin temellerinden bahsedildi ve yöntemi Matlab kodlara uygulamak için tasarım prosedürü özetlendi. Bir sonraki bölümde, bölüm3'te tekniğin algoritmaları Matlab kodlarına uygulandı. Matlab programında sayısal iyileştirme paketlerin yanında, daha önce yazılan hazır paketlerde referans verilerek kullanıldı. Matlab kodlarında önce

giriş veriler tanımlandı ve bir sonraki adımda nümerik hatalarla karşılanmamak için normalızasyon yapıldı bu teknikten yararlanarak, tüm değerler bir referans değere bölünerek küçülüyorlar. Böylece hesaplama zamanı ve hata olasılığı düşüyor. Devamında, bir alçak geçiren prototip süzgeç istenen spesifiklere göre tasarlandı ve bir bant geçiren süzgeçe dönüştürüldü. Süzgeçin kazanç karakteristiğini göz önüne alarak, Basitleştirilmiş Real Frekans Tekniğiyle bant geçerin süzgeçe en uyum sağlayan transfer fonksiyon elde edililir ve sentez paketine verilir. Sentez paketi verilen transfer fonksyonu pasif bir ağ olarak lumped elemanlarla sentezler. Bu sürec tasarım için yapıldı ve sentez paketin verdiği ağ elde edildi, sonra ağın eleman değerleri denormalize edildi. Bolüm 4'te ise elde edilen ağın üzerine simülasyonlar yapıldı bu simülasyonlar S-parametreler ve elektromagnet etkiyi inceledi. Devamında simülasyon sonuclarının Matlab sonuçlarıyla örtüştüğü gösterildi. Bir sonraki adımda, devre real komponent modelleriyle incelendi. Bu aşamada kapasitörler için Murata fırmanın modelleri ve indaktörler için Johnson fırmanın modelleri kullanıldı. Pertinaks olarak Modelithics fırmanın benzetim modeli kullanıldı. Önce devre lumped CAD modeller le incelendi sonra, devrenin gerçeklenmesini daha verimli yapmak üzere bir takım uygulamalar ve iyileştirmeler yapıldı. İyileştirme aşamasında, elemanların çoğuna lumped to distributed dönüşümü yapıldı. Böylece tasarım bir mixed-element tasarım olarak hazırlandı.Tüm benzetimler ADS keysight programında yapıldı. Bir sonraki bölüm, bölüm 5'te, ağın ölçümüne odaklanarak, iki ölçüm devresi tasarlanıp ve gerçekleştirildi. Bilindiği gibi, VNA ve PNA gibi ölçüm cihazları, ölçüm için 50 ohm'lu portlar kullanmaktalar. O yüzden, doğrudan ölçmek için, önce ölçüm cihazın ucu 6.25 ohm'a dönüştürülmeli. Bu konuyu gözde bulundurarak, iki trafo, iki farklı yötemler ile tasarlandı. Birinci trafo, çeyrek dalga boyu olarak tasarlandı bu tasarımda önce ideal transmisyon hatlarıyla hazırlandı. Sonra, mikro şerit yollara dönüştürüldü. Dönüşüm esnasında ADS programın Line Calculator imkanı kullanıldı. Böylece pertinaksın ve transmisyon hattın özelliklerini girerek, mikro şerit hattın özellikleri hesaba katmış oluyor. Sonraki adımda, mikro şeritlerle yapılan trafonun layoutı çizildi ve layout üzerine layout sonrası analizler yapıldı. Sonra layout etkilerini kapsayacak şekilde bir sembol olarak hazırlandı ve sonraki analizlerde layout sembolu kullanıldı. Diğer trafo ise lamped elemanlar ile tasarlandı. Bu tasarım tamamen optimize teknikleriyle tasarlandı. Tasarımı elde ettikten sonra lumped to distributed dönüşümü yapıldı ve tüm elemanlar distributed elemanlara çevirildi. Diğer trafo gibi, bu trafonunda layout'ı çizildikten sonra layout sonrası analizler yapıldı ve son olarak sembole çevirildi. Bir sonraki adım olarak semboller empedans eşleştirici ağa bağlanarak tüm devre incelendi ve gereken değişiklikler yapıldı . İyileştirmelerin ardından, tüm devrenin layout'ı çizildi ve üretim için gerber dosyaları çıkarıldı. İmalat ve ölçüm aşamaları İstanbul Üniversitesinde yapıldı ve ölçüm sonuçları simülasyon sonuçlarına göre büyük oranda örtüşme gösterdi. Bahsedilen trafolar empedans eşleştirici ağ ve ölçüm cıhazın arasında yer alarak doğrudan ölçüm sağlıyorlar. Diğer bölümde, tasarlanan empedans eşleştirici ağın çip içi tasarımı yapıldı. Bu tasarımda CMOS TSMC 0.18 um teknoloji süreci kullanıldı. Lumped elemanlı ağ, RF kütüphanesinde bulunan komponent modelleriyle tasarlandı ve devre performansı simülasyonlarla belirlendi. Bu aşamada Cadence Virtuoso programı kullanıldı. Rf kütüphanesinde bulunan İnductörlerin CAD modellerin değerleri doğrudan boyutlarıyla belirleniyor. Bu yüzden devre elemanların değerlerini set etmek için bir test devresi kurulmalı. Bölüm 6 da indaktörler için test devresi kuruldu ve boyutları istenen değerlere göre tespit edildi. Bir sonraki adımda, ağın layout'ı çizildi ve layout sonrası simülasyonlar uygulandı. Bu aşamada, devre için layout sonrası analizler yapıldı ve tüm layout etkileri dahil ederek, ağ bir cell olarak tanımlandı. Çip içi

tasarımın simülasyon sonuçlarına göre, çip içi tasarım kayıplı bir tasarım olarak tespit edildi. Bu sonuç yaklaşık olarak tahmin ediliyordu. Yapılan araştırmalara göre, çip içi indaktörlerin Q-faktörleri düşük olduğu için, fazla kayıba sebep oluyorlar. Buna dayanarak, çip içi tasarımlarda kayıbı azaltmak için iki farklı yöntem öneriliyor. Birinci yöntem, tasarımlarda indaktör sayısını azaltmaya çalışıyor. Ama bu yöntem herzaman yararlı olmayabilir. Örneğin süzgeç tasarımlarında az sayıda indaktör kullanmak süzgeçlerin kazanç grafiklerini daha yayvan yapıyor ve bu dezavantaj keskin filtre tasarımlarında çok baskın bir etki. İkinci yöntem ise, bu sorunu aktif elemanlar kullanmakla gideriyor. Örneğin tranzistörlu aktif süzgeçler. Bu durumda indaktörlerden kaynaklanan kayıp bir aktif yapıyla telafi ediliyor.

1. INTRODUCTION

In this chapter, the main motivation and the objective of the project will be explained in details. First section gives some details about the data converter for which the impedance matching network has been designed. Afterward, a short section presents basic information about microstrip lines. Then the technical obstacles of technology process and how the presented technique surmounts them will be investigated.

1.1 Motivation

Designing broadband impedance matching networks is one of the heated-controversy subjects in the field of electronics and telecommunication. As an instance, one of the major efforts in receiver designs, is maximizing the SNR at the input stage by matching the antenna impedance to the LNA input [1]. Or as another reason which highlights the importance of impedance matching networks is their intermediate role in minimizing power loss when signal is transmitted between different terminations [2]. According to the maximum power transfer theory, the power on the load is maximum, if impedance of the load and source both have a same value. But what if the load is set by a mostly used value as if it is 50Ω or 75 Ω in telecommunication and RF systems [3]. In this regard, for transferring the maximum power to the load, it is inevitable of adjusting source impedance for equalizing its value to the value of load impedance. But the question which raises is, how far we can count on this method. Or in other words, is it always possible to adjust input or output impedance to any arbitrary value?

In some cases due to design conditions or technology restrains, fitting the load impedance to a fixed value (like 50 Ω) is not beneficial or even feasible. As an instance which will be studied in the next chapter, in the design of a high speed DAC, for achieving higher speed, output signal level must not exceed an acceptable upper value However, used process technology may not allow signals to flow with every magnitude on a specific load as same as 50Ω. So the process compels and dictates lower impedances which leads to un-matched systems. More details are given in subsequent sections.

1.2 Objective

One of the most popular design methods of broadband impedance matching network is a numerical method called as Real Frequency Techniques (RFTs). It can be classified into several categories depending on the use of different approaches such as Line Segment Technique (LST), Real Frequency Direct Computational Technique (RFDCT), Parametric Approach (or Bode method), Simplified Real Frequency Technique (SRFT) [4]. In this thesis, the SRFT method is utilized because of its brilliant advantages over the other methods. Here are some to mention:

- As opposed to analytic theory, it neither requires model of load nor the selection of the analytic form of a transfer function of the matching network to be designed. SRFT directly utilizes the measured reflectance data and optimizes the transducer power gain of the matched system as flat and as high as possible which in turn yields the analytic form of the driving point reflectance of the equalizer.[5]
- As opposed to brute force computer design techniques, in SRFT circuit topology is not selected in advance. Rather it is automatically obtained as the result of the synthesis of the input reflection coefficient with desired element values.

At this point, it is important to assess the theoretical gain bandwidth limit of the load. Unfortunately, analytic theory is incapable beyond simple cases in which generator and/or load networks are comprised of several reactive elements only. However, Real Frequency Line Segment Technique of Carlin or SRFT provides an insight to matching problems with an excellent estimate for the upper level of the flat transducer power gain, or equivalently the minimum return loss, over the selected frequency bands. [5]. The design involved in this thesis, is intended to be realized with lumped elements. Whole design process has been developed by Matlab codes. The obtained topology has been optimized by AWR and ADS software. Before implementation, the circuit has passed all layout simulation including EM (electromagnetic) simulation. Implementation has been done by realistic lumped elements of Murata Corporation. The FR4 has been used as substrate

In another try, the integrated version of the network, was designed by Cadence virtuoso program in TSMC 0.18 um technology process. Besides, the layout and post layout analysis was done as well.

1.3 Input Network

As shown in figure 1.1 the designed data converter benefits two current steering DACs, converting 16 bits of digital data to analogue data. According to the design specifics, this data converter is a high speed DAC. The input digital data is separated to two sections, the MSB and LSB. In the MSB part, the codes are converted to thermometric codes which leads to pull a high value of current, almost 1280 u A per bit, this feature, beside other specifics, have made a high total output current, about 80 m A, on the load. Because of the technology obstacles, pushing this amount of current on a standard 50Ω load is not feasible. Therefore by using a load with lower value, which can endure more current, by applying an impedance matching network between load of DAC and 50 ohm antenna, a signal with higher value can be pushed over load with minimum dissipation.

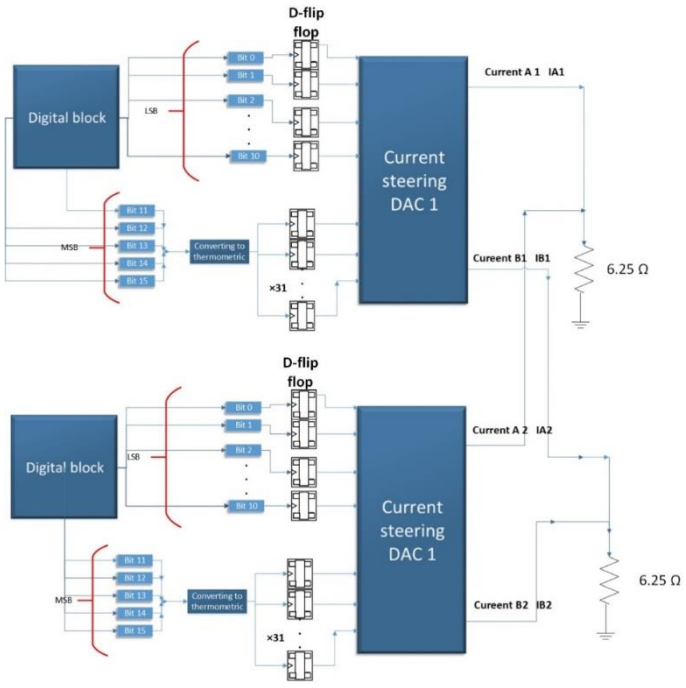

Figure 1.1: Output stage of a high speed data converter.

1.4 Microstrip Lines

Microstrip transmission lines consist of a conductive strip of width "W" and thickness "t" and a wider ground plane, separated by a dielectric layer (substrate) of thickness "H" as shown in the Fig 1.2 [6]

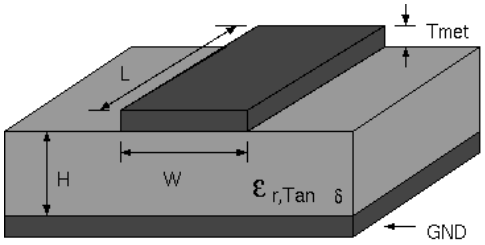

Figure 1.2: A cross-section of a Microstrip transmission line.

The parameters and their descriptions are brought in table 1.1

Table 1.1: Parameters of microstrip line.

Name	Unit	Description
Er	-	Relative dielectric constant Er is the permittivity of the substrate material relative to the permittivity of free space ε0 = 8.85e-12 F/M2
H	{Phys. Units}	Substrate thickness
Tmet	{Phys. Units}	Metal thickness
Rho	-	Rho is the bulk resistivity of conductor metal normalized to gold (that is, to 2.44 x 10 -8Ω*m) So actual metal bulk resistivity = 2.44 x 10 -8Ω*Rho*m.
Tan ∂	-	Loss tangent of the dielectric. This value is only used for loss Calculations.

A closed-form approximate expression for the quasi-static characteristic impedance of a microstrip line developed by Wheeler [7-9] is given by:

$$Z_{mline} = \frac{Z_0}{2\pi\sqrt{2(1+\varepsilon_r)}} \boldsymbol{ln}(1 + \frac{4h}{w_{eff}}(\frac{14+\frac{8}{\varepsilon_r}}{11}\frac{4h}{w_{eff}} + \sqrt{((\frac{14+\frac{8}{\varepsilon_r}}{11}\frac{4h}{w_{eff}})\text{^}2 + \pi\frac{1+\varepsilon_r}{2}}))) \quad \textbf{(1.1)}$$

There are many calculators on the websites or in simulator software like AWR or ADS. Figure 1.3 and Figure 4.1 depict that tool in AWR and ADS programs separately.

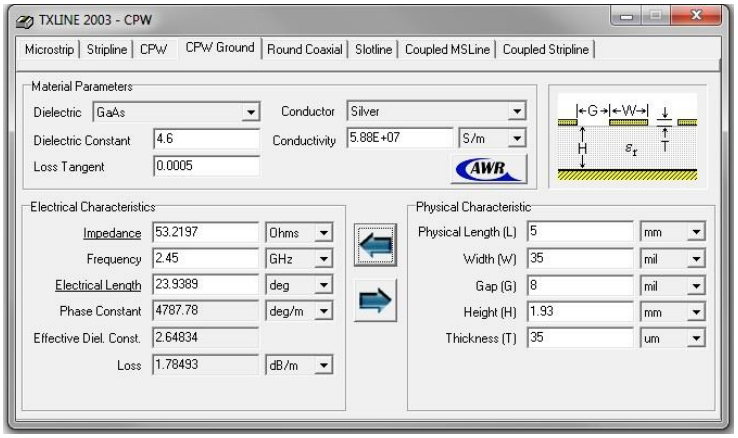

Figure 1.3: Microstrip line impedance calculator of AWR program.

Or as it is seen in figure 1.4 by line calculator tool in ADS

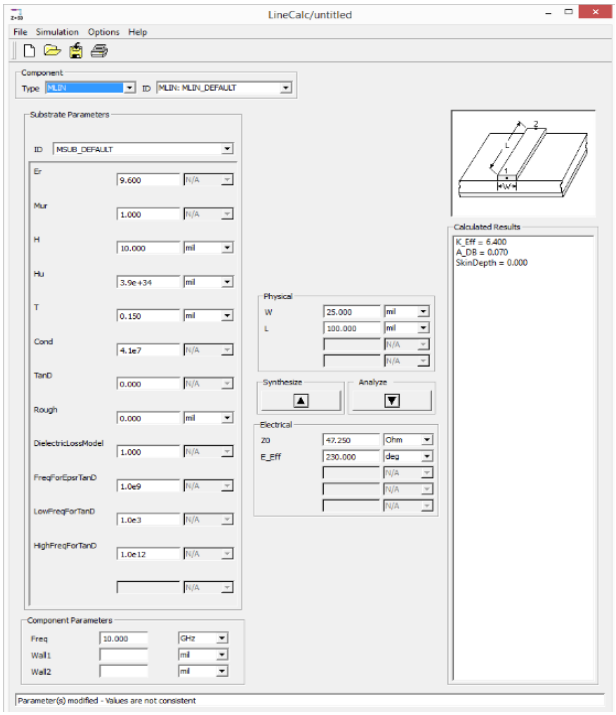

Figure 1.4: Microstrip line impedance calculator of ADS program.

1.5 Design Alternatives and Technology Obstacles

As it is depicted in Fig 1.5, a fabrication technology process like TSMC 180 nm presents some layers of metal and other materials in the same package. In TSMC180 nm technology process, there are six layers of metals, each upon the other, starting from metal 1 in the lowest layer to metal 6 at the top layer. All these layers' behavior is as same as a Microstrip lines. With this in mind, by using physical equations of the Microstrip Lines, the behavior of implementation can be perceived. In designing of the mentioned DAC, metal6 is used as conducting layer and one of Metal5, Metal4 or Metal3 as the ground layer. Since the travelling signal passes through either of conducting layer or ground layer, both layers should flow the signal. By trying all possibilities of choosing ground layer, maximum amplitude of signal can be calculated in terms of current.

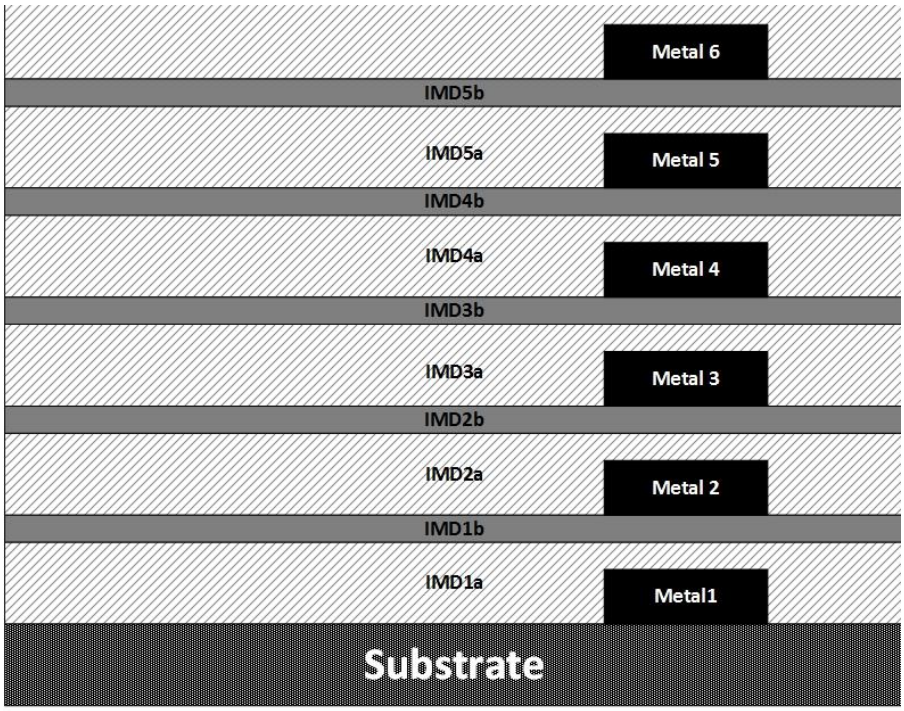

Figure 1.5: Layer sequence in TSMC 180nm technology process.

Case 1: M6- conducting layer, M5-ground:

$$H = \text{IMD5a} + \text{IMD5b} \qquad \textbf{(1.2)}$$

$$\frac{H}{\varepsilon r} \cong \frac{IMD5a}{\varepsilon_5 a} + \frac{IMD5b}{\varepsilon_5 b} \qquad \textbf{(1.3)}$$

Case 2: M6-conducting layer, M4-ground:

$$\mathrm{H} = \mathrm{IMD5a} + \mathrm{IMD5b} + \mathrm{IMD4a} + \mathrm{IMD4b} \quad \textbf{(1.4)}$$

$$\frac{H}{\varepsilon r} \cong \frac{IMD5a}{\varepsilon_5 a} + \frac{IMD5b}{\varepsilon_5 b} + \frac{IMD4a}{\varepsilon_4 a} + \frac{IMD4b}{\varepsilon_4 b} \quad \textbf{(1.5)}$$

Case 3: M6-conducting layer, M3- ground:

$$H = IMD5a + IMD5b + IMD4a + IMD4b + IMD3a + IMD3b \quad \textbf{(1.6)}$$

$$\frac{H}{\varepsilon \mathrm{r}} \cong \frac{IMD5a}{\varepsilon_5 \mathrm{a}} + \frac{IMD5b}{\varepsilon_5 \mathrm{b}} + \frac{IMD4a}{\varepsilon_4 \mathrm{a}} + \frac{IMD4b}{\varepsilon_4 \mathrm{b}} + \frac{IMD3a}{\varepsilon_3 \mathrm{a}} + \frac{IMD3b}{\varepsilon_3 \mathrm{b}}$$

By replacing value of the parameters' value from TSMC documentation, the results of equations (1.1)-(1.6) are obtained as shown in Table 1.2

Table 1.2: Microstrip parameters' value in various alternatives of choosing conducting and ground Layer.

Parameter	Description	M6-M5	M6-M4	M6-M3
H	Substrate thickness(um)	1.53	2.9	4.29
ε_r	Dielectric constant	3.8	3.78	3.77
T	Conductor thickness (um)	2.34	2.34	2.34
Cond	Conductor conductivity (S/meter)	1.2e7	1.2e7	1.2e7

In this step, width of the conducting metal to obtain the intended impedance values is calculated. This step has been accomplished by using the impedance calculator. For three mentioned conditions results are given in Table 1.3

Table 1.3: Metal widths for some impedance values.

Impedances	Width (um) M6-M5	Width (um) M6-M4	Width (um) M6-M3
6.25	42.2505	80.9481	120.322
12.5	19.519	36.8639	55.0491
25	7.6761	15.2523	23.0505
50	2.20075	4.84309	7.63659

Fig 1.6 to Fig 1.8 demonstrate the relation between the width of the conducting metal and its impedance

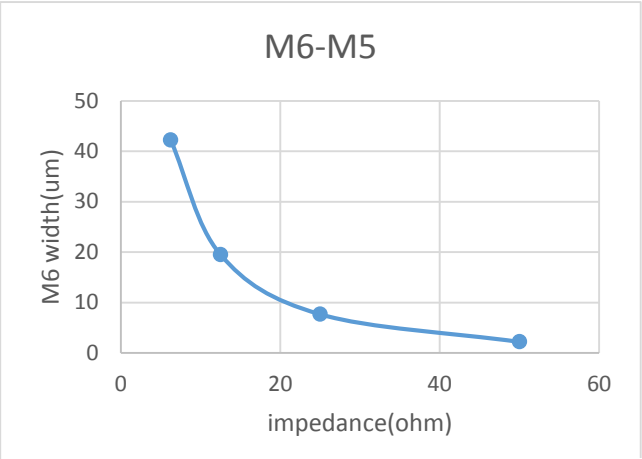

Figure 1.6: M6 conducting metal, M5 ground metal.

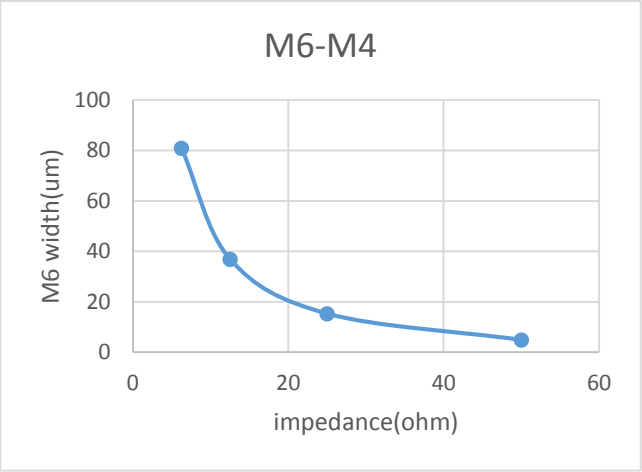

Figure 1.7: M6 conducting metal, M4 ground metal.

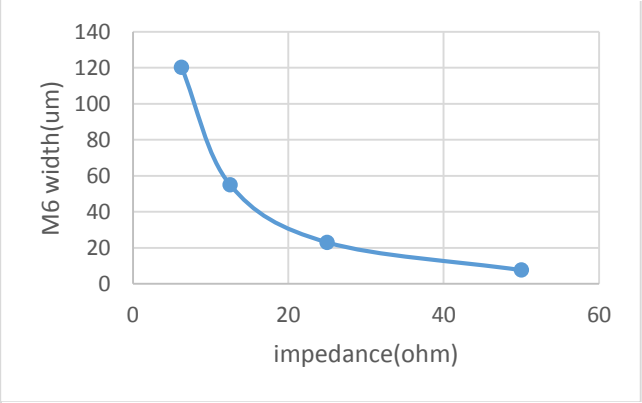

Figure 1.8: M6 conducting metal, M4 ground metal.

Table 1.4 gives the current density of each metal. Thus the maximum allowed current to flow in each metal can be calculated. These values are brought ın Table 1.5

Table 1.4*:* Current density of metals.

Metal	J(mA/um)
M1	1
M2	1
M3	1
M4	1
M5	1.6
M6 (UTM(20KA))	4
M6(UTM(9.2KA))	9.2

Table 1.5: Maximum allowed current.

Impedances	M6-M5 max current (mA)	M6-M4 max current (mA)	M6-M3 max current (mA)
6.25	42.2505	80.9481	120.322
12.5	19.519	36.8639	55.0491
25	7.6761	15.2523	23.0505
50	2.20075	4.84309	7.63659

Since Metal 6 has the largest current density, it has been chosen as the conductive strip. This is the ground layer which determines the amount of the maximum possible current flowing through the ground metal. As it can be seen in the case of using 50 Ω as the output load, amplitude of current, maximally, is as low as 8 mA which is approximately one tenths of intended amount of current.

In conclusion, according to the results, in order to have higher amplitude of output signal, the limitation of process coerces the design to have loads with lower impedance values. In this regard, an impedance matching network can transfer power from a lower value termination to a much higher value termination such as 50 Ohm, with minimum loss.

2. FUNDAMENTAL CONCEPTS OF SIMPLIFIED REAL FREQUENCY TECHNIQUE (SRFT) AND DESIGN PROCEDURE

In this chapter, firstly some basic definitions and rules will be reviewed, afterward by introducing the main idea of the design, the design procedure which benefits the SRFT, will be studied with its mathematical derivations and equations.

2.1 Two Port Networks

A pair of terminals through which a current may enter or leave a network is known as a port. A port is an access to the network and consists of a pair of terminals; the current entering one terminal leaves through the other terminal so that the net current entering to the port equals zero. [10-12] One of the most significant reasons of using two port networks is that, they can be used as a black box [13] describing whole behaviors of the network. This feature brings simplicity in analyzing, processing and above all, designing of the circuits. There are quite a few two port network parameters as: Impedance (Z), admittance (Y) , hybrid parameters (h), inverse hybrid parameters (g), Scattering parameters (S) Scattering transfer parameters (T), to name a few [14].

The fig 2.1 depicts a two port network. The equations (2.1) through (2.4) demonstrate impedance, admittance, hybrid and inverse hybrid parameters respectively

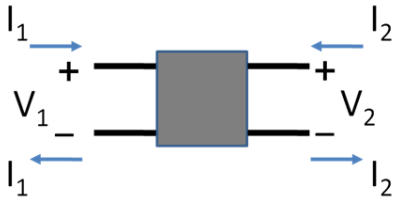

Figure 2.1: A two port network.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$$z_{11} \stackrel{\text{def}}{=} \left.\frac{V_1}{I_1}\right|_{I_2=0} \qquad z_{12} \stackrel{\text{def}}{=} \left.\frac{V_1}{I_2}\right|_{I_1=0}$$

$$z_{21} \stackrel{\text{def}}{=} \left.\frac{V_2}{I_1}\right|_{I_2=0} \qquad z_{22} \stackrel{\text{def}}{=} \left.\frac{V_2}{I_2}\right|_{I_1=0}$$

(2.1)

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$y_{11} \stackrel{\text{def}}{=} \left.\frac{I_1}{V_1}\right|_{V_2=0} \qquad y_{12} \stackrel{\text{def}}{=} \left.\frac{I_1}{V_2}\right|_{V_1=0}$$

$$y_{21} \stackrel{\text{def}}{=} \left.\frac{I_2}{V_1}\right|_{V_2=0} \qquad y_{22} \stackrel{\text{def}}{=} \left.\frac{I_2}{V_2}\right|_{V_1=0}$$

(2.2)

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$h_{11} \stackrel{\text{def}}{=} \left.\frac{V_1}{I_1}\right|_{V_2=0} \qquad h_{12} \stackrel{\text{def}}{=} \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

$$h_{21} \stackrel{\text{def}}{=} \left.\frac{I_2}{I_1}\right|_{V_2=0} \qquad h_{22} \stackrel{\text{def}}{=} \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

(2.3)

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$$

$$g_{11} \stackrel{\text{def}}{=} \left.\frac{I_1}{V_1}\right|_{I_2=0} \qquad g_{12} \stackrel{\text{def}}{=} \left.\frac{I_1}{I_2}\right|_{V_1=0}$$

$$g_{21} \stackrel{\text{def}}{=} \left.\frac{V_2}{V_1}\right|_{I_2=0} \qquad g_{22} \stackrel{\text{def}}{=} \left.\frac{V_2}{I_2}\right|_{V_1=0}$$

(2.4)

2.2 Scattering Parameters

Impedance, admittance, and hybrid parameters which are used mostly in the Verilog designs, are calculated directly by voltage and current signals. However, at microwave frequencies it is difficult to measure both voltage and current signals, this obstacle is because of the difficulty in obtaining perfect opens and shorts in higher frequencies. Moreover Active devices may be unstable under open or short conditions [15]. Therefore, a description in terms of scattering matrix is preferred. The S-parameters can be measured by network analyzer.

Scattering parameters are defined in the terms of incident waves and reflected waves figure 2.2 depicts the reflected and incident waves in a two port network [16].

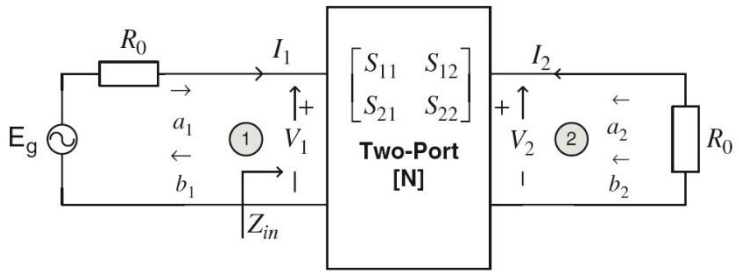

Figure 2.2: Scattering Parameters for Lossless Two-Ports [18].

Where the a_k are the defined as incident waves and the b_k as the reflected waves at port *k*. It is conventional to define a_k and b_k in terms of the square root of power.

Kurokawa defines the incident power wave for each port as [17]:

$$a_1 = \frac{1}{2}\left[\frac{V1}{\sqrt{Real(Z0)}} + Real(Z_0).I1\right] \quad \textbf{(2.5)}$$

$$b_1 = \frac{1}{2}\left[\frac{V1}{\sqrt{Real(Z0)}} - Real(Z_0).I1\right] \quad \textbf{(2.6)}$$

$$a_2 = \frac{1}{2}\left[\frac{V2}{\sqrt{Real(Z0)}} + Real(Z_0).I2\right] \quad \textbf{(2.7)}$$

$$b_2 = \frac{1}{2}\left[\frac{V2}{\sqrt{Real(Z0)}} - Real(Z_0).I2\right] \quad \textbf{(2.8)}$$

And S matrix is defined as [18]:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad \textbf{(2.9)}$$

For reciprocal networks [19]

$$S_{12} = S_{21} \quad \textbf{(2.10)}$$

For symmetrical networks [19]

$$S_{11} = S_{22} \quad \textbf{(2.11)}$$

For lossless reciprocal networks [20]

$$|S_{11}| = |S_{22}| \quad \textbf{(2.12)}$$

And [20]

$$|S_{11}|^2 + |S_{21}|^2 = 1 \quad \textbf{(2.13)}$$

Expanding this matrix into (2.9) gives:

$$\boldsymbol{b_1 = S_{11}.a_1 + S_{12}.a_2} \rightarrow$$

$$\frac{b1}{a1} = \Gamma in = Sin(input\ reflection\ coefficient) = S_{11} + S_{12}.(\frac{a2}{a1}) \quad \textbf{(2.14)}$$

$$\frac{b1}{a2} = S(reverse\ transmission\ coefficient) = S_{rtc} = S_{12} + S_{11}.(\frac{a1}{a2}) \quad \textbf{(2.15)}$$

$$\boldsymbol{b_2 = S_{21}.a_1 + S_{22}.a_2} \rightarrow$$

$$\frac{b2}{a2} = \Gamma out = Sout(output\ reflection\ coefficient) = \boldsymbol{S_{22} + S_{21}.\left(\frac{a1}{a2}\right)} \quad \textbf{(2.16)}$$

$$\frac{b2}{a1} = S(transmision\ coefficient) = S_{tc} = \boldsymbol{S_{21} + S_{22}}.(\frac{a2}{a1}) \quad \textbf{(2.17)}$$

Above calculations suggest that, in the case of resistively terminated two different 1-port networks [S and L as seen in Fig. 2.3) attached at the input and output of the 2-port network, scattering parameters can be rewritten to include the effects of the newly added 1-port networks. This whole structure therefore describes a new "black box" as shown in Fig 2.3.

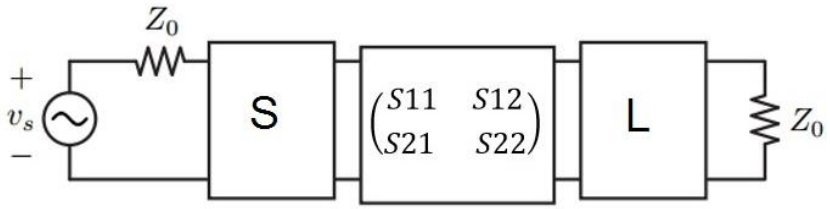

Figure 2.3: Two port network with arbitrary load and generator Termination.

To explain more, let us start with some fundamental definitions of scattering parameters. $\mathbf{S_{11}}$ is the reflected power to generator where both generator and output are loaded by reference load Z_0 [17]. In this case, according to the maximum transfer power theorem, the power transferred from generator to the load of a network is maximum. Therefore there would be no reflected power on load; hence $\mathbf{a_2}$=0.

$$S_{11} = \frac{b1}{a1} \mid (a_2 = 0) \quad \textbf{(2.18)}$$

Nevertheless, Γin or S_{in} is called input reflection coefficient of system which demonstrates the reflected power from output load to the looking point, where the

output is terminated by any arbitrary load. So it can be concluded that Γin or S_{in} is the new S_{11} of the whole system including terminating loads with arbitrary values.

Similarly Γ_{out} or S_{out} is output reflection coefficient of network, regardless of input termination. While S_{22} is the output reflection coefficient where both of generator and output is loaded by Z_0. Again, according to the maximum transfer power $\boldsymbol{a_1}$=0.

$$S_{22} = \frac{b2}{a2} \,|(a_1 = 0) \qquad \textbf{(2.19)}$$

Also, S_{tc} and S_{rtc} are transmision coefficient and reverse transmission coefficient of the network respectively, regardless of input or output terminations, respectively, where S21 and S12 are transmision coefficient reverse transmission coefficient of the network where both of generator and output is loaded by reference load Z_0.

$$S_{21} = \frac{b2}{a1} \,|(a_2 = 0) \qquad \textbf{(2.20)}$$

$$S_{12} = \frac{b1}{a2} \,|(a_1 = 0) \qquad \textbf{(2.21)}$$

Hence, the network of figure 2.3 can be considered as a black box which its new S-parameters describe its behavior as figure 2.4 depicts.

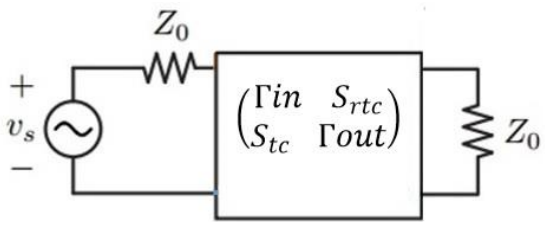

Figure 2.4: S-parameters of total system including unmatched.

As it was mentioned before, this project deals with single matching problem, so let us study the scattering parameters of single matching problem in more details.

2.2.1 Single matched system with matched load

In this case, as shown in the figure 2.5, the load is terminated by matched impedance therefore, reflected coefficients must be calculated. Let's call the network, Equalizer. In this regard, E_{11}, E_{22}, E_{21} and E_{12} stands for S_{11}, S_{22}, S_{21} and S_{12}, respectively

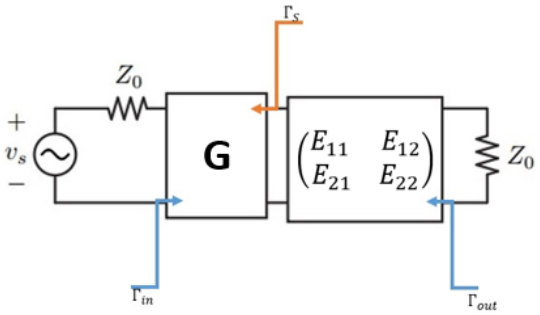

Figure 2.5: The load is terminated with matched impedance and generator is terminated by an arbitrary load.

$$\Gamma out = Sout(\text{output reflection coefficient}) = E_{22} + E_{21}.\left(\frac{a1}{a2}\right) \quad \textbf{(2.22)}$$

Since G_{22} and E_{11} is seen in opposite direction,

$$\frac{b1}{a1} = \frac{aG1}{bG1} = \frac{1}{G_{22}} \quad \textbf{(2.23)}$$

Also from (2.13) we know

$$\frac{b1}{a1} = E_{11} + E_{12}.(\frac{a2}{a1}) \quad \textbf{(2.24)}$$

By replacing (2.22) equation into equation (2.25)

$$\frac{1}{G_{22}} = E_{11} + E_{12}.\left(\frac{a2}{a1}\right) \quad \rightarrow \quad \frac{a1}{a2} = \frac{G_{22}.E_{12}}{1-G_{22}.E_{11}} \quad \textbf{(2.26)}$$

By replacing (2.26) into (2.22)

$$\Gamma out = Sout = G_{22}.\left[\frac{E_{12}.E_{21}}{1-G_{22}.E_{11}}\right] + E_{22} \quad \textbf{(2.27)}$$

$$\Gamma out = sout = \frac{E_{22}-G_{22}(E_{22}.E_{11}-E_{12}.E_{21})}{1-S11.SG11} = \frac{E_{22}-\Gamma_G.\ \Delta E}{1-E_{11}.\Gamma_G} \quad \textbf{(2.28)}$$

And for lossless reciprocal networks, when all mismatched loads are included:

$$|\Gamma out| = |\Gamma in| \quad \textbf{(2.29)}$$

2.2.2 Single matched system – matched generator

In this case, as shown in the figure 2.6, the load is terminated by matched impedance so by a same calculation

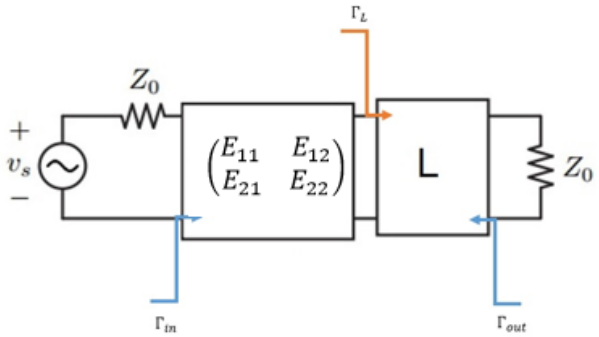

Figure 2.6: Matched generator, unmatched load.

$$sin = \Gamma in = \frac{E_{11} - L_{11}(E_{22}.E_{11} - E_{12}.E_{21})}{1 - E_{22}.L_{11}} = \frac{E_{11} - \Gamma_L.\Delta S}{1 - E_{22}.\Gamma_L} \quad \textbf{(2.30)}$$

And for lossless reciprocal networks, when all mismatched loads are included:

$$|\Gamma out| = |\Gamma in| \quad \textbf{(2.31)}$$

2.3 Verification by T-Parameters

This results can be acquired by using cascade S-parameters calculation. The other group of parameters describing a two port networks are Scattering transfer parameters (T-parameters) [21]. The total T-parameters of some cascade networks is multiplication of their T matrix. Also there is a connection between T-parameters and S-parameters. So after multiplying T-matrices and getting total T matrix, the S-parameters can be obtained through T to S conversion. Figure 2.7 depicts the cascade situation in which the scattering parameters of the whole system is obtainable by its equivalent T-parameters

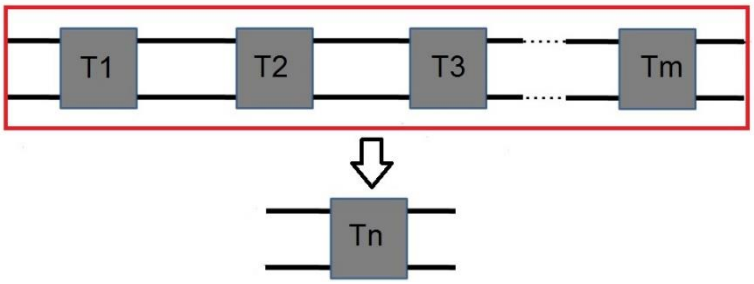

Figure 2.7: Cascade networks.

The total T matrix is calculated as [21]:

$$\mathrm{T}_n = \mathrm{T}_1.\mathrm{T}_2.\mathrm{T}_3 \ldots . \mathrm{T}_m \quad \textbf{(2.32)}$$

where:

$$\mathrm{T}_m = \begin{pmatrix} \mathrm{T}_{m11} & \mathrm{T}_{m12} \\ \mathrm{T}_{m21} & \mathrm{T}_{m22} \end{pmatrix} \quad \textbf{(2.33)}$$

The relation between S-parameters and T-parameters is as below [21]:

S to T conversion:

$$T_{11} = \frac{1}{S_{21}} \quad \textbf{(2.34)}$$

$$T_{12} = -\frac{S_{22}}{S_{21}} \quad \textbf{(2.35)}$$

$$T_{21} = \frac{S_{11}}{S_{21}} \quad \textbf{(2.36)}$$

$$T_{22} = -\frac{\Delta S}{S_{21}} \quad \textbf{(2.37)}$$

T to S conversion:

$$S_{11} = \frac{T_{21}}{T_{11}} \quad \textbf{(2.38)}$$

$$S_{12} = \frac{\Delta T}{T_{11}} \quad \textbf{(2.39)}$$

$$S_{21} = \frac{1}{T_{11}} \quad \textbf{(2.40)}$$

$$S_{22} = -\frac{T_{12}}{T_{11}} \quad \textbf{(2.41)}$$

Let us investigate two situations of single matching problem discussed in previous section.

2.3.1 Single matched system – matched load

Figure 2.8 depicts block schematic of a single matching situation with mached load

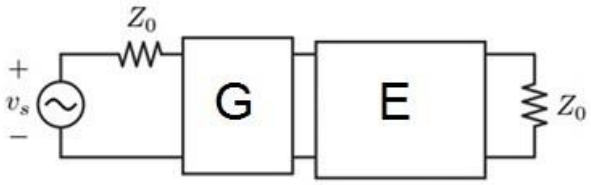

Figure 2.8: Unmatched generator, matched load.

$$G = \begin{pmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{pmatrix} \quad \textbf{(2.42)}$$

$$E = \begin{pmatrix} E_{11} & E_{12} \\ E_{21} & E_{22} \end{pmatrix} \quad \textbf{(2.43)}$$

$$T_G.T_E = \begin{pmatrix} \frac{1}{G_{21}} - \frac{G_{22}.E_{11}}{G_{21}.E_{21}} & -\frac{E_{22}}{G_{21}.E_{21}} + \frac{G_{22}.\Delta E}{G_{21}.E_{21}} \\ \frac{G_{11}}{G_{21}.E_{21}} - \frac{\Delta G.E_{11}}{G_{21}.E_{21}} & -\frac{G_{11}.E_{22}}{G_{21}.E_{21}} + \frac{\Delta G.\Delta E}{G_{21}.E_{21}} \end{pmatrix} \quad \textbf{(2.44)}$$

$$S_t = \begin{pmatrix} \frac{G_{11}-\Delta G.E_{11}}{1+G_{21}.E_{21}} & \frac{\Delta T_G}{T_{11}} \\ \frac{1}{T_{11}} & \frac{E_{22}-G_{22}.\Delta E}{1-G_{22}.E_{11}} \end{pmatrix} \quad \textbf{(2.45)}$$

As it can be seen, the S22 of the whole network, including load of generator, is the same thing we obtained in (2.28)

$$\Gamma_{out} = S_{22} = \frac{E_{22} - \Gamma_G.\ \Delta E}{1 - E_{11}.\Gamma_G}$$

The same thing is true about the other single matching problem

2.3.2 Single matched system – matched generator

As shown in the figure 2.9, the system can be a single matched system with matched generator.

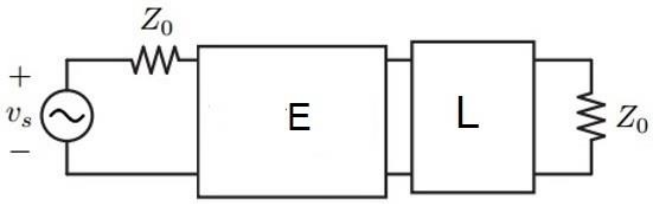

Figure 2.9: Matched generator, unmatched load.

$$L = \begin{pmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{pmatrix} \quad \textbf{(2.46)}$$

$$E = \begin{pmatrix} E_{11} & E_{12} \\ E_{21} & E_{22} \end{pmatrix} \quad \textbf{(2.47)}$$

$$T_G.T_E = \begin{pmatrix} \frac{1}{E_{21}} - \frac{E_{22}.L_{11}}{E_{21}.L_{21}} & -\frac{L_{22}}{E_{21}.L_{21}} + \frac{E_{22}.\Delta L}{E_{21}.L_{21}} \\ \frac{E_{11}}{E_{21}.L_{21}} - \frac{\Delta E.L_{11}}{E_{21}.L_{21}} & -\frac{S_{11}.L_{22}}{S_{21}.L_{21}} + \frac{\Delta S.\Delta L}{S_{21}.L_{21}} \end{pmatrix} \quad \textbf{(2.48)}$$

$$S_t = \begin{pmatrix} \frac{E_{11}-\Delta E.L_{11}}{1+E_{21}.L_{21}} & \frac{\Delta T_G}{T_{11}} \\ \frac{1}{T_{11}} & \frac{L_{22}-E_{22}.\Delta L}{1-E_{22}.L_{11}} \end{pmatrix} \quad \textbf{(2.49)}$$

$$sin = \Gamma in = \frac{E_{11}-L_{11}(E_{22}.E_{11}-E_{12}.E_{21})}{1-E_{22}.L_{11}} = \frac{E_{11}-\Gamma_L.\Delta S}{1-E_{22}.\Gamma_L} \quad \textbf{(2.50)}$$

Later, this feature of scattering parameters will be used for extracting transducer power gain equations.

2.4 Transducer Power Gain (TPG)

The primitive role of an impedance matching network is to transfer the maximum amount of power from source to generator. However, some extra features like behaving as a low-pass or band-pass filter might be intended as well. In this regard we have to adjust transducer power gain to meet the desired specifics.

As shown in the figure 2.10, when both sides of a network is terminated with matched impedances, the TPG is equal to $|S_{21}|^2$ [22]

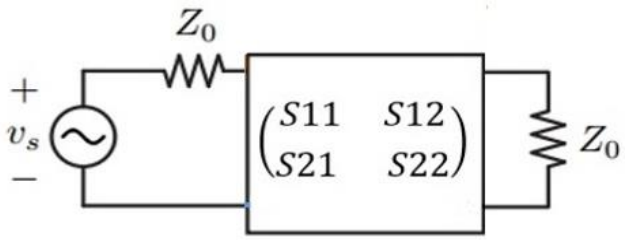

Figure 2.10: Matched generator, matched load.

However when the network is terminated with unmatched loads, the TPG is affected by new conditions. Let's consider the comprehensive and general condition where there are any arbitrary loads on either source or load. As it is shown in Fig 2.11

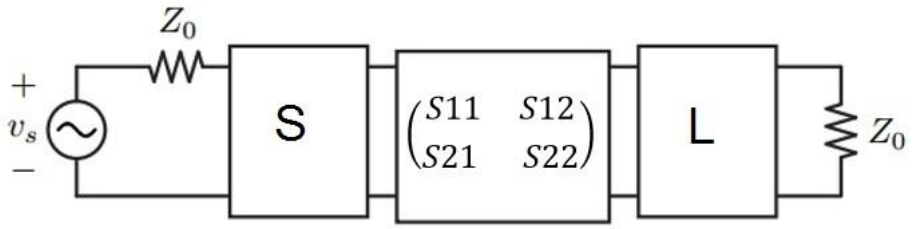

Figure 2.11:Unmatched generator, unmatched load.

In this case the derivation of the transducer power gain can be obtained as below [23]:

$$TPG = \frac{PL}{P_{avs}} = \frac{|S_{21}|^2 .(1-|\Gamma_L|^2).(1-|\Gamma_S|^2)}{|1-\Gamma_{in}\Gamma_S|^2 .|1-S_{22}\Gamma_L|^2} \qquad \textbf{(2.51)}$$

According to the maximum power theorem, if load or generator is terminated by reference impedance, Z_0, the Γ_L or Γ_S respectively becomes zero. Therefore in the cases of single matching problem, the derivation undergoes some changes as shown in the next sections.

2.4.1 TPG of single matched system – matched generator

Case one: the source is terminated by Z_0. As shown in the figure 2.12 the system is single matched system with matched generator.

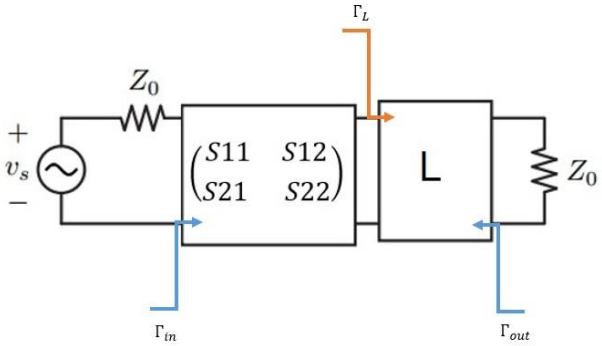

Figure 2.12: Unmatched generator, unmatched load.

Since $Z_S = Z_0$, $\Gamma_S = 0$ the equation (2.51) undergoes some changes as below

$$TPG = \frac{PL}{P_{avs}} = \frac{|S_{21}|^2 .(1-|\Gamma_L|^2)}{|1-S_{22}\Gamma_L|^2} \qquad \textbf{(2.52)}$$

Let's verify (2.52) by another approach. As it was stated in before, scattering parameter can be rewritten to include load effects. So:

$$sin = \Gamma in = \frac{S_{11} - \Gamma_L(S_{22}.S_{11} - S_{12}.S_{21})}{1 - S_{22}.\Gamma_L} = \frac{S_{11} + \Gamma_L.\Delta S}{1 - S_{22}.\Gamma_L}$$

For lossless reciprocal networks $|S_{11}|^2 + |S_{21}|^2 = 1$ **(2.53)**

TPG=1-$|S_{11}|^2$ **(2.54)**

For this case TPG=1-$|\Gamma in|^2$ **(2.55)**

$$\text{TPG} = 1 - |\frac{S_{11} - \Gamma_L.\Delta S}{1 - S_{22}.\Gamma_L}|^2$$

$$\xrightarrow{|\Delta S|=\frac{S21}{|S21^*|}=1} \frac{1 + (S_{22}\Gamma_L)^2 - 2(S_{22}\Gamma_L) - (S_{11})^2 - (\Gamma_L)^2 + 2(S_{11}.\Gamma_L)}{(1 - S_{22}.\Gamma_L)^2}$$

$$\xrightarrow{|S_{11}|=|S_{22}| \; and \; |S_{11}|^2+|S_{21}|^2=1} \frac{|S_{21}|^2.(1-|\Gamma_L|^2)}{|1-S_{22}\Gamma_L|^2}$$

$$TPG = \frac{|S_{21}|^2.(1-|\Gamma_L|^2)}{|1-S_{22}\Gamma_L|^2}$$ **(2.56)**

2.4.2 TPG of Single matched system – matched load

Case two: the load is terminated by Z_0. As shown in the figure 2.12 the system is single matched system with matched load.

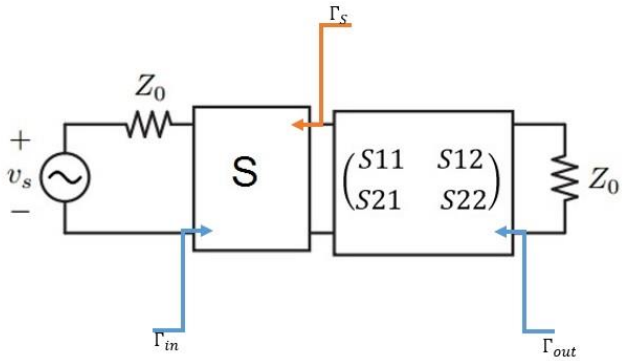

Figure 2.13: Unmatched generator, matched load.

Since $Z_L = Z_0$, $\Gamma_L = 0$ also $\Gamma_{in} = S11$

$$TPG = \frac{PL}{P_{avs}} = \frac{|S_{21}|^2.(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2}$$ **(2.57)**

According to the (2.28)

$$sout = \Gamma out = \frac{S_{22} - \Gamma_S(S_{22}.S_{11} - S_{12}.S_{21})}{1 - S_{11}.\Gamma_S} = \frac{S_{22} - \Gamma_S.\Delta S}{1 - S_{11}.\Gamma_S}$$

For lossless reciprocal networks $|S_{11}| = |S_{22}|$, and $|S_{11}|^2 + |S_{21}|^2 = 1$,

TPG=1-$|S_{11}|^2 = 1 - |S_{22}|^2$

For this case TPG=1-$|\Gamma out|^2$

$$\text{TPG} = 1 - |\frac{S_{22} - \Gamma_S.\Delta S}{1 - S_{11}.\Gamma_S}|^2$$

$$\xrightarrow{|\Delta S|=\frac{S21}{|S21^*|}=1} \frac{1 + (S_{11}\Gamma_S)^2 - 2(S_{11}\Gamma_S) - (S_{22})^2 - (\Gamma_S)^2 + 2(S_{22}.\Gamma_S)}{(1 - S_{11}.\Gamma_S)^2}$$

$$\xrightarrow{|S11|=|S22| \; and \; |S_{22}|^2+|S_{21}|^2=1} \frac{|S_{22}|^2.(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2}$$

$$TPG = \frac{|S_{22}|^2.(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2} \qquad \textbf{(2.58)}$$

2.5 Driving Point Impedance

According to the Darlington theorem any positive real [24] immitance function can be realized as a lossless two port in a resistive termination R [25]. So by designing a desired PR (positive real) impedance or admittance function, the network can be realized by means of lossless elements. In SRFT the process of design starts with defining the driving point reflectance function of the system and ends with calculating its TPG according to the defined impedance network. Then by doing this procedure in an optimization loop the desired TPG is obtained. In the previous section, the TPG equation has been extracted in terms of scattering parameters. In order to have a perspective about the relation between impedance of a network and its TPG, the relation between S-parameters and impedance characteristics are derived. Moreover the TPG is rewritten in terms of impedance characteristics. Merging (2.6), (2.5) and (2.18) gives:

$$S_{11} = \frac{[\frac{V_1}{\sqrt{Real(Z_0)}} - \sqrt{Real(Z_0)}.I_1]}{[\frac{V_1}{\sqrt{Real(Z_0)}} + \sqrt{Real(Z_0)}.I_1]} = \frac{Z_{in} - R_0}{Z_{in} + R_0} \qquad \textbf{(2.59)}$$

Z_{in}, signifies the input impedance of network when both of ports are terminated by Z_0 figure 2.14

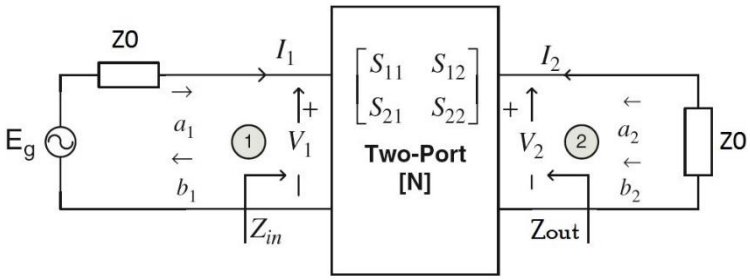

Figure 2.14: Two port network, terminated by matched loads.

Doing the same for (2.8), (2.7) and (2.19)

$$S22 = \frac{[\frac{V2}{\sqrt{Real(Z0)}} - \sqrt{Real(Z0)}.I2]}{[\frac{V2}{\sqrt{Real(Z0)}} + \sqrt{Real(Z0)}.I2]} = \frac{Zout - R0}{Zout + R0} \quad \textbf{(2.60)}$$

Let's call Z_{out} and Z_{in}, back-end (Z_b) and front-end (Z_f) impedances respectively. For extracting the derivation of TPG in terms of impedance, impedance characteristics of S_{in} (Γ_{in}) and S_{out} (Γ_{out}) must be acquired.

2.5.1 Impedance based TPG of single matched system – matched generator

Case one: the source is terminated by Z_0. As shown in the figure 2.15 the system is single matched system with matched generator.

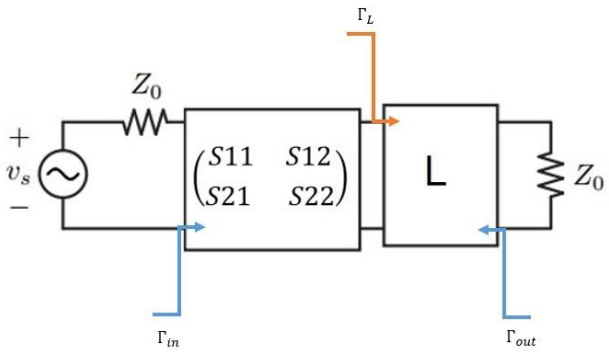

Figure 2.15: Matched generator, unmatched load.

As mentioned before in (2.55)

TPG=1-$|\Gamma in|^2$

$$sin = \Gamma in = \frac{S11 - \Gamma_L(S22.S11 - S12.S21)}{1 - S22.\Gamma_L} = \frac{S11.\Gamma_L.\Delta S}{1 - S22.\Gamma_L}$$

Also Γ_L is input reflection coefficient of the output load. By the same way used in (2.59) we can say:

$$\Gamma_L = \frac{Z_L - 1}{ZL + 1} \quad \textbf{(2.61)}$$

$$S_{in} = \Gamma in = \frac{ZL - ZF}{ZL + ZF} \quad \textbf{(2.62)}$$

By implementing (2.59)-(2.62) into (2.56) and (2.58) TPG derivation of single matching problem is obtained in terms of impedances

$$TPG = \frac{4.RF.RL}{(RF+RL)^2+(XF+XL)^2} \quad \textbf{(2.63)}$$

2.5.2 Impedance based TPG of single matched system – matched load

Case two: the load is terminated by Z_0. As shown in the figure 2.16 the system is single matched system with matched load.

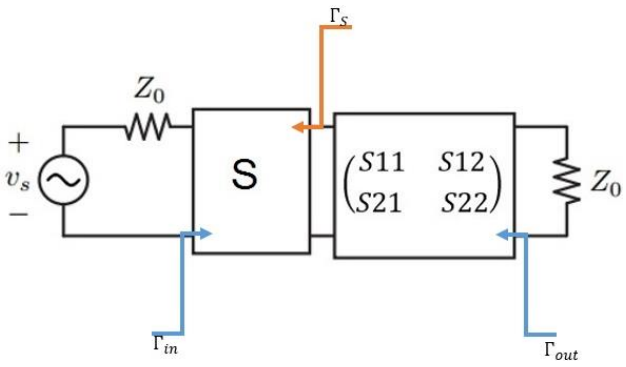

Figure 2.16: Unmatched generator, matched load.

In a same way:

$$\Gamma_G = \frac{Z_G - 1}{ZG + 1} \quad \textbf{(2.64)}$$

TPG=1-$|\Gamma out|^2$ **(2.65)**

$$S_{out} = \Gamma out = \frac{ZG - ZB}{ZG + ZB} \quad \textbf{(2.66)}$$

$$sout = \Gamma out = \frac{S22 - \Gamma_G(S22.S11 - S12.S21)}{1 - S11.\Gamma_G} = \frac{S22 - \Gamma_G.\Delta S}{1 - S11.\Gamma_G}$$

$$TPG = \frac{4.RB.RL}{(RB+RL)^2+(XB+XL)^2} \quad \textbf{(2.67)}$$

2.6 Overview of Simplified Real Frequency Technique

Generation of the TPG function can be accomplished by various techniques. As stated before, this thesis benefits the SRFT. The heart of this technique resides in creation of a driving point reflectance function for the lossless equalizer to be designed by a nonlinear optimization process. This reflectance function is formed as a rational function whose coefficients of the numerator polynomial is determined by the said optimization starting from the unknown values of the coefficients which were chosen in an ad-hoc manner before the optimization begins [26].

As the start point, let us investigate some properties of reflection coefficient (Γout or Γin let's call it Γ for both situations of single matching problem).

If a loss-less one-port consists of passive lumped elements such as inductors, capacitors, resistors and transformers then, the back-end or front-end impedance (as a general situation let us call it Z for both states of single matching problem) is a positive real function (PRF) and rational function in the complex variable p= jω and it is expressed as [27]:

$$z\,(p) = \frac{N(p)}{D(p)} \qquad \textbf{(2.68)}$$

where both numerator N (p) and denominator D (p) polynomials are Hurwitz [27], perhaps with simple roots on the imaginary (or real frequency) axis p = jω of the complex p − plane. Thus, y (p) = 1/z (p) is also a PR-rational function in p. In this case, the corresponding input reflectance $\Gamma = \frac{z-1}{z+1}$ must be a real rational function in p such that [28]

$$\Gamma\,(p) = \frac{h\,(p)}{g\,(p)} \qquad \textbf{(2.69)}$$

$$h\,(p) = N(p) - D(p) \qquad \textbf{(2.70)}$$

$$h\,(p) = h_1\,p^{n-1} + h_2\,p^{n-2} + h_3\,p^{n-3} + \ldots + h_n \qquad \textbf{(2.71)}$$

And

$$g(p) = N(p) + D(p) \quad \textbf{(2.72)}$$

$$= g_1 p^{n-1} + g_2 p^{n-2} + g_3 p^{n-3} + \ldots + g_n \quad \textbf{(2.73)}$$

where degree "*n*" of the polynomials *h* (*p*) and *g* (*p*) refers to total number of reactive elements (i.e. capacitor and inductors) in the one-port under consideration [29].

Subtractions of Hurwitz polynomials results in an arbitrary polynomial with real coefficients [30]. Therefore, the numerator polynomial *h* (*p*) is an ordinary polynomial with real coefficients. On the other hand, addition of two Hurwitz polynomials results in Strictly Hurwitz polynomial which has all its roots in the closed Left Half Plane (LHP) [30]. Thus, the denominator polynomial *g*(*p*) must be strictly Hurwitz which makes the reflection coefficient Γ (*p*) regular on the *jω* axis as well as in the Right Half Plane (RHP) in the complex domain $p = \sigma + j\omega$. In other words, Γ (*p*) is bounded over the entire frequency band as well as in the open RHP.

For lossless one-ports Γ (*p*) = 1 [27]. Thus

$$\Gamma(p) \leq 1; \forall p = \sigma \geq 0. \quad \textbf{(2.74)}$$

The rational form of Γ (*p*) = *h*(*p*)/ *g*(*p*) is called the Bounded-Real (BR) function.

And $|h(j\omega)|^2 \leq |g(j\omega)|^2$ **(2.75)**

Amplitude square functions of $|h(j\omega)|^2$ and $|g(j\omega)|^2$ in real variable *ω*, define non-negative even polynomials $H(\omega^2)$ and $G(\omega^2)$ such that [27]

$$h(j\omega)h(-j\omega) = H(\omega^2) = H_1 \omega^{n-1} + H_2 \omega^{n-2} + H_3 \omega^{n-3} + \ldots + H_n \geq 0 \quad \textbf{(2.76)}$$

$$g(j\omega)g(-j\omega) = G(\omega^2) = G_1 \omega^{n-1} + G_2 \omega^{n-2} + G_3 \omega^{n-3} + \ldots + G_n \geq 0 \quad \textbf{(2.77)}$$

With

$$H(\omega^2) \leq G(\omega^2) \quad \textbf{(2.78)}$$

At this point, we can comfortably state that one can always find a non-negative even polynomial $F(\omega 2) = f(j\omega) f(-j\omega) = F_1 \omega^{n-1} + F_2 \omega^{n-2} + F_3 \omega^{n-3} + \ldots + F_n$

A little bit more complicated form of *f* (*p*) may have only multiple zeros at DC such that $f(p) = p^k$. This form corresponds to a band-pass structure [31]

$$F(p) = f(p).f^*(p) \quad \textbf{(2.79)}$$

$G(\omega^2) = H(\omega^2) + F(\omega^2)$ **(2.80)**

The mirror symmetric roots of

$G(-p^2) = G_1 p^{2n} + G_2 p^{2n-2} + G_3 p^{2n-6} + \ldots + G_n$

Is determined by means of a well-known root finding techniques [32].

$g(p) = \sqrt{G_n} \prod_{r=1}^{n} (p + \sigma r) \pm j\gamma r$ **(2.81)**

Where $pr = -\sigma r \mp j\gamma r$ *is a LHP root of G*

Now, the impedance, reflection coefficient and subsequently the TPG can be obtained:

$$Z = \frac{N(p)}{D(p)} = \frac{g(s) + h(s)}{g(s) - h(s)} \qquad \Gamma = \frac{h(s)}{g(s)} = \frac{N(p) - D(p)}{N(p) + D(p)}$$

TPG=1-$|\Gamma|^2$

2.7 Design Procedure

1. In the first step, h polynomial is defined as it is mentioned

$h(p) = N(p) - D(p) = h(p) = h_1 p^{n-1} + h_2 p^{n-2} + h_3 p^{n-3} + \ldots + h_n$

2. In the second step, the f polynomial is defined as:

$$f = p^k$$

3. Third step is defining the g(p) polynomial

$G(\omega^2) = F(\omega^2) + H(\omega^2)$

$$g(p) = \sqrt{G_n} \prod_{r=1}^{n} (p + \sigma_r) \pm j\gamma_r$$

4. In the fourth step, input reflection coefficient and back-end or front-end impedance are derived as

$$Z = \frac{N(p)}{D(p)} = \frac{g(p) + h(p)}{g(p) - h(p)} \qquad \Gamma = \frac{h(p)}{g(p)} = \frac{N(p) - D(p)}{N(p) + D(p)}$$

Finally, in the fifth step, replacing p^2 by $-\omega^2$, $T(\omega^2)$ is generated as in

$$TPG = 1 - |\Gamma out|^2 = \frac{|S_{22}|^2 . (1 - |\Gamma_S|^2)}{|1 - S_{11}\Gamma_S|^2} = \frac{4.RB.RL}{(RB + RL)^2 + (XB + XL)^2}$$

$$TPG = 1 - |\Gamma in|^2 = \frac{|S_{11}|^2 . (1 - |\Gamma_L|^2)}{|1 - S_{22}\Gamma_S|^2} = \frac{4.RB.RL}{(RB + RL)^2 + (XB + XL)^2}$$

3. EFFECTIVE NUMERICAL IMPLEMENTATION OF SRFT IN MATLAB

In the previous chapters, the theory of design and related techniques were investigate. This chapter deals with applying studied methods into Matlab programming language. During the chapter programing techniques and used packages will be investigated with details and finally the design will be wrapped up by synthesis package. As mentioned before, the objective in this thesis is designing an impedance matching network for output of a high speed DAC, matching an equivalent termination resistance of 6.25 Ohm at its output to a standard 50 Ohm. Since the operating frequency is 2.4 GHz, the matching network is decided to have a Chebyshev band pass form with a center frequency 2.4 GHz and a bandwidth of 400 MHz As long as a discrete circuit design is intended, parasitic effects related to the pin and the package should be taken into account. The Fig 3.1 demonstrates an overall estimation, there is a parasitic inductance between package and pin which is about 2nH also there is a parasitic capacitor between substrate layer and conducting layer, around 0.5 pF.

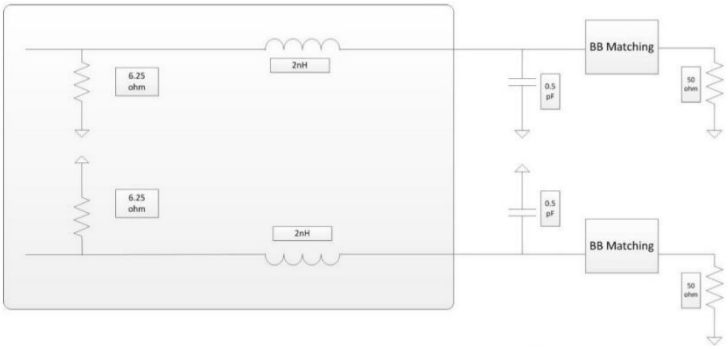

Figure 3.1: Output of the DAC with modeled parasitic effects.

As stated in the previous chapter, the designed equalizer is a two port network. So, the whole system with its parasitic effects can be modeled as shown in fig 3.2.

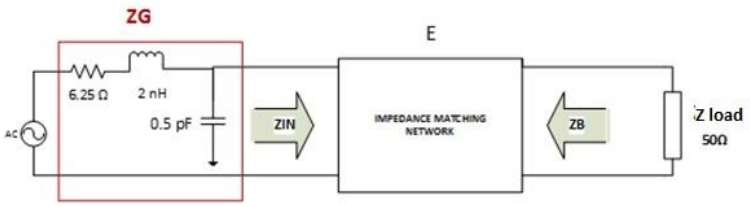

Figure 3.2: Model of the parasitic effects attached to two-port equalizer network.

3.1 Defining Inputs And Specifics

First of all, the specifics of the design like center frequency, upper and lower corner frequencies and bandwidth should be defined. Also, the generator and load side impedances are needed to be defined.

3.2 Impedance And Frequency Normalization

The first and foremost step in a microwave design is to apply a normalization procedure in order to reduce the calculation time and avoid numerical or even convergence errors. Let us explain this advantage through an example.

Suppose, there is a TPG with characteristics as below:

$$TPG = \frac{p^4+p^2+3}{p^3+2p} \quad \textbf{(3.1)}$$

And, let the operating frequency is in the order of GHz. In this regard, if the TPG is evaluated at the frequency of 2.4 GHz, its value will be about 1.5080e+10 now suppose this value repeats during 5000 optimization loop. With no doubt, it will take a lot of time and may lead to numerical errors. Therefore, without any reservation it would be better to normalize huge numbers to small ones. The base frequency for normalizing is chosen as

$$\omega_0 = \sqrt{\omega_h . \omega_l} \quad \textbf{(3.2)}$$

Where:

$$\omega_l = 2.\pi.f_l \quad \textbf{(3.3)}$$

$$\omega_h = 2.\pi.f_h \quad \textbf{(3.4)}$$

$$f_l = f_c - \frac{BW}{2} \quad \textbf{(3.5)}$$

$f_l = f_c - \frac{BW}{2}$ fc = 2.4 BW = 0.4 , **(3.6)**

3.3 Prototype Filter Design

Next step is defining the prototype filter. In this step, the desired band-pass filter is defined so that the optimizer function follow its characteristics.

Firstly a prototype low-pass filter is designed, then that filter is transformed to a band pass filter, by using a low pass to band pass transformation. The band pass filter will have the desired specifics given by the designer such as center frequency fc, bandwidth B, pass band ripple Ap (dB) and stop band attenuation As (dB).

. This package is prepared by Dr. Ramazan Köprü the filter's characteristics is defined such that suit our bandwidth spesific.

3.4 Applying SRFT And Optimization

This section is about defining H, F and consequently the G and g function. As mentioned in chapter 2, the extracted TPG of these functions should suit the desired TPG. Therefore, there should be an optimization loop to iterate the TPG and rebuild until it finds the best solution. This process accomplishes by taking the advantage of fmin search optimization function of Matlab. After getting the best TPG function, the program gets out of optimization loop and hands over the results to the synthesis package.

3.5 Synthesis

In this step, the program synthesizes the back-end impedance network which is obtained according to the best gained TPG function. The synthesis function is performed by the Matlab package which is recently introduced into the literature by Prof. B. S. Yarman [33].

Inside the synthesis package a controller flag is added to check if the impedance network is synthesizable or not. In the case of negative answer the program gets out of the synthesize function and restart it.

figure 3.3 and 3.4 illustrate the designed network's schematic and its TPG characteristics

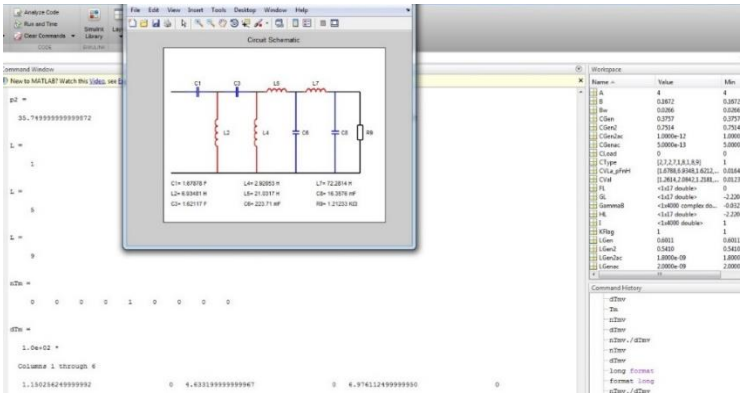

Figure 3.3: Synthesized network

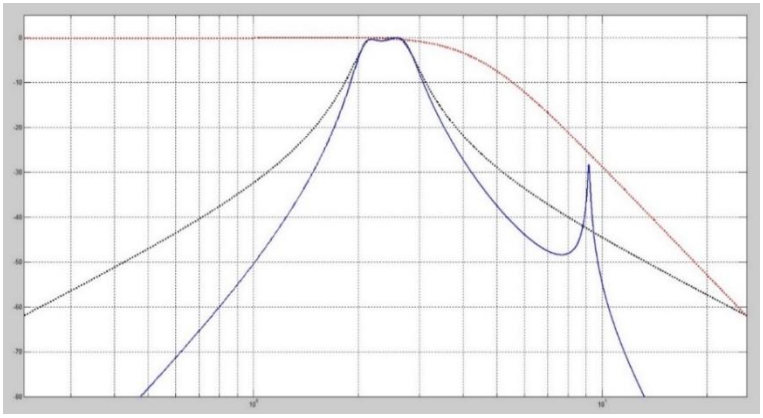

Figure 3.4: TPG of synthesized network

3.6 Denormalization

Since all the given values are in normalized form, the output is given in the normalized form as well. Therefore, in order to obtain the actual values, there should be a denormalization over values[34].

$$L_{act} = \frac{L_n . Z_0}{\omega_n} \quad \textbf{(3.7)}$$

$$C_{act} = \frac{C_n}{\omega_n . Z_0} \quad \textbf{(3.8)}$$

$$R_{act} = Z_0 . R_n \quad \textbf{(3.9)}$$

Where $\omega_n = \omega_0 . 10^9$

4. SIMULATION VERIFICATIONS AND REALIZATION TECHNIQUES

4.1 Software Simulations

After denormalization of the obtained values, the designed network with actual (i.e. denormalized) element values is simulated with ADS software. Figure 4.1 depicts the schematic. As it is shown in figure 4.2, the network gives the same result acquired by Matlab program. The network performances obtained from the simulations are observed to be in a high degree of agreement to those of the Matlab design.

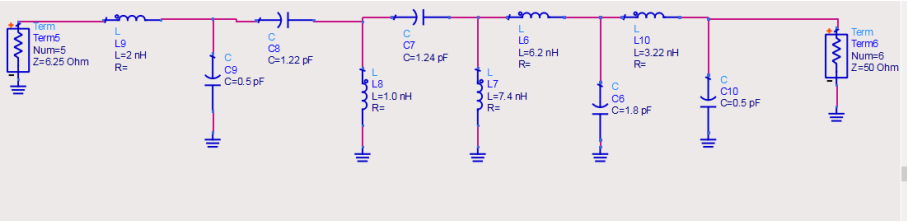

Figure 4.1 Schematic of the design.

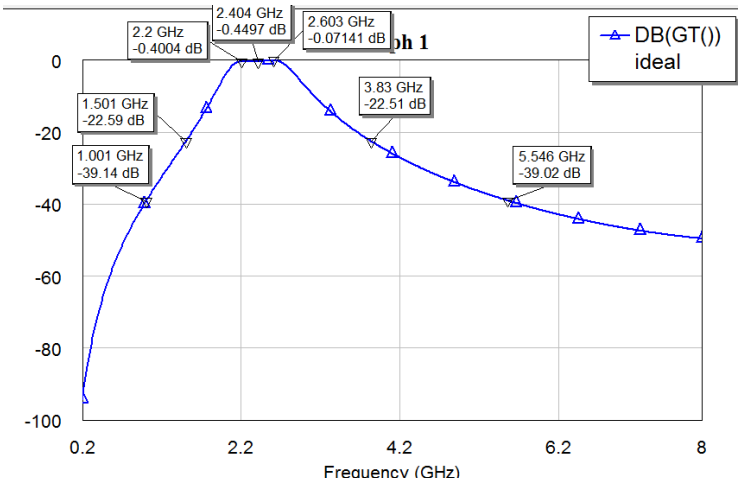

Figure 4.2: The magnitude of the network's TPG.

The magnitude of the network's TPG is given in table 4.1

Table 4.1: The magnitude of the network's TPG.

Frequency (GHz)	Magnitude (dB)
0.5	-62.9023
0.9	-42.9099
1.3	-29.1144
1.7	-15.766
2.1	-1.29003
2.3	-0.450179
2.5	-0.228171
2.7	-0.606192
3.1	-9.53214
3.5	-17.4692

4.2 Sensitivity Analysis

In this step the sensitivity of the network is examined by changing the values of elements by random $+/-4\%$

Since two first elements are the parasitic effects of package, they are not counted as parts of network. Hence, they are excluded from the sensitivity analysis. New elements affect the magnitude of TPG. The results are brought respectively in table 4.2

Table 4.2: TPG results of the sensitivity analysis.

Frequency (GHz)	Ideal (dB)	Sensitivity 1 (dB)	Sensitivity 2 (dB)	Sensitivity 3 (dB)
1.9	-8.01806	-7.60867	-9.63978	-8.19892
2	-4.09862	-3.65114	-5.65003	-4.15349
2.1	-1.29003	-0.956142	-2.1908	
2.2	-0.400404	-0.227062	-0.440591	-0.231181
2.3	-0.450179	-0.327037	-0.21998	-0.324913
2.4	-0.455112	-0.328831	-0.317128	-0.383294
2.5	-0.228171	-0.117645	-0.218149	-0.190787
2.6	-0.0683292	-0.0557949	-0.0235872	-0.0133377
2.7	-0.606192	-0.794411	-0.218626	-0.43625
2.8	-2.23845	-2.62103	-1.35721	-1.90096
2.9	-4.59419	-5.07894	-3.40121	-4.14027

As it is obvious from the gain graph, figure 4.3 and tables, by sweeping the values of the elements the TPG does not change significantly.

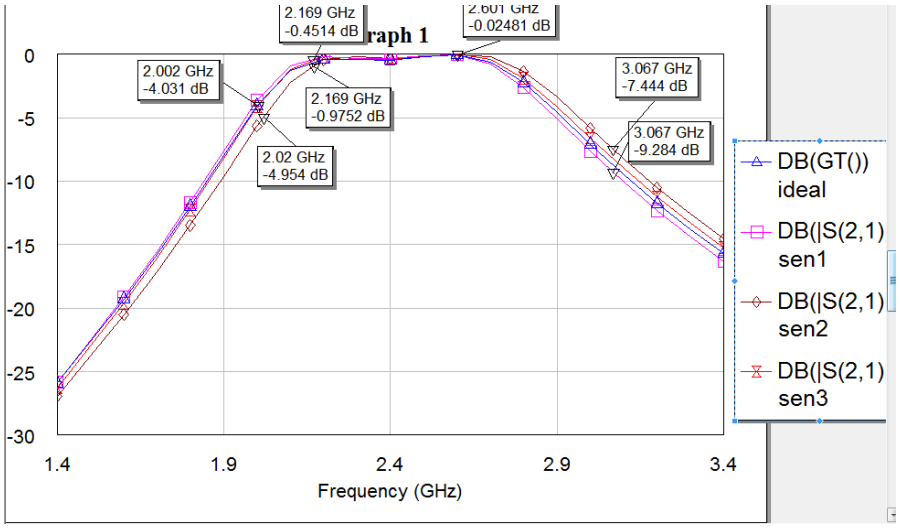

Figure 4.3: TPG results of sensitivity analysis.

4.3 Lumped To Distributed Conversions, Layout And Post Layout Simulations

For designs which include lumped elements, the best way to obtain more realistic results out of simulations is using the practical CAD models of the lumped elements presented by producer or other modeling corporations. However, the features of the technology used for soldering the lumped elements have a great effect on elements' behavior in practical. In another word, various soldering technology may lead to various behavior of elements different from their CAD models. Thus, while the soldering technology is not trustable enough, it had better to avoid using lumped elements by converting them to distributed elements.

Series inductors and shunt capacitors are among the most efficient conversions which the design consists of three series inductor and three shunt to ground capacitors. Thus, the realization of the network can be a mixed elements implementation with four lumped and six distributed elements. Figure 4.4 depicts the lumped elements which are converted to distributed elements

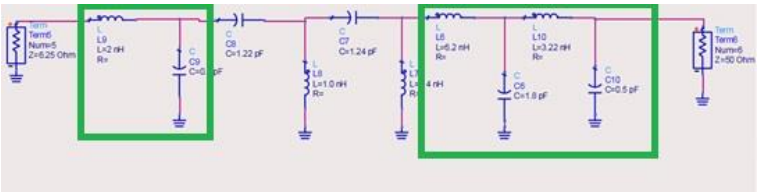

Figure 4.4 Eelements inside the boxes efficiently can be converted to distributed lines.

As it is seen in Fig 4.5 [35], by using the conversion formulas, the distributed equivalent of each element can be obtained

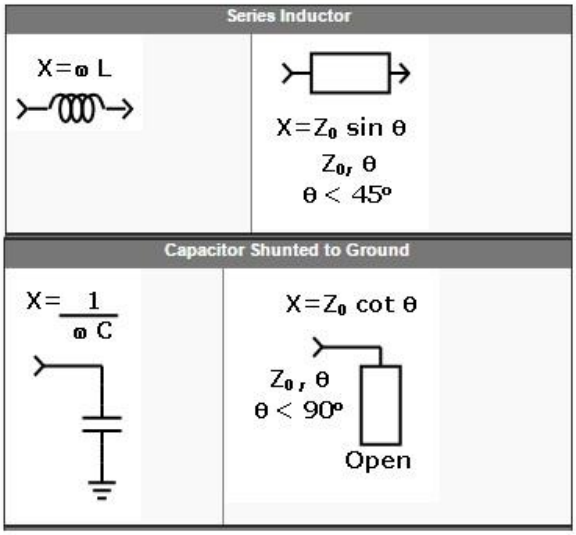

Figure 4.5: Lumped to distributed conversions for series inductor and shunt capacitor.

$$L\omega = Z_0 \sin\theta \qquad \textbf{(4.1)}$$

$$\frac{1}{\omega C} = Z_0 \cot\theta \qquad \textbf{(4.2)}$$

Also In order to have accurate implementation, simulations must be upon real models of materials like connecting ways, substrate and realistic models of the elements to name a few. In order to include effect of connection traces, ideal microstrip line (MLIN) symbol in component palette in ADS is used in the schematic. Figure 4.6 illustrates a substrate modeled used in realization.

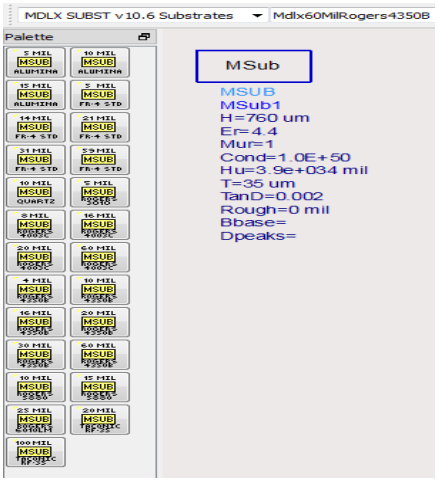

Figure 4.6: Substrate models in ADS.

By using mentioned models, the schematic of the design is prepared as shown in figure 4.7.

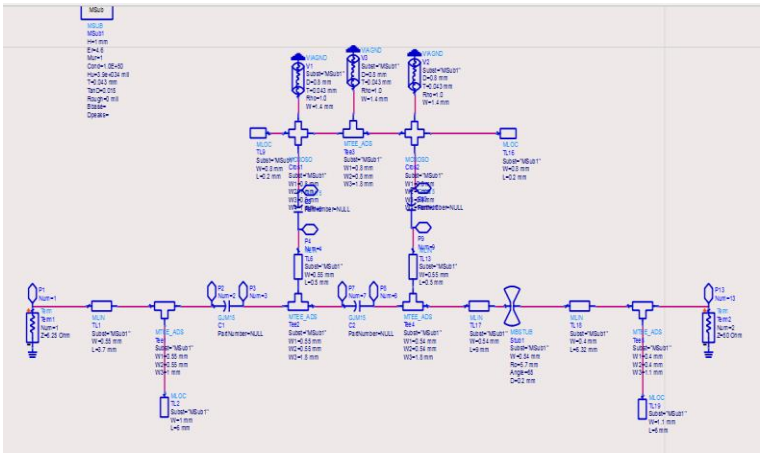

Figure 4.7: Schematic of the network with including parasitic effects.

Moreover, realistic element models of Murata are used for all the passives, i.e. inductors and capacitors.

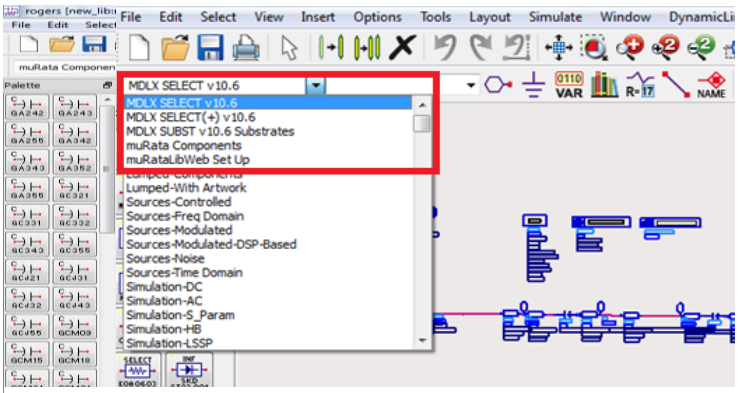

Figure 4.8: Realistic element models of Murata to be used as passives.

As it is seen in figure 4.9, CAD models of Murata are used during simulation

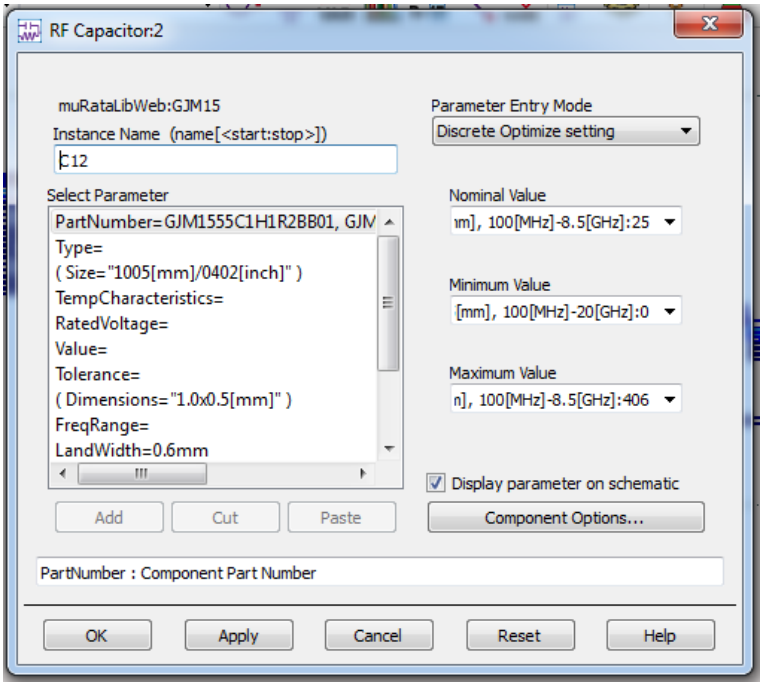

Figure 4.9: Realistic models of parameters.

By auto layout extraction feature of ADS, the layout of the network extracted as below

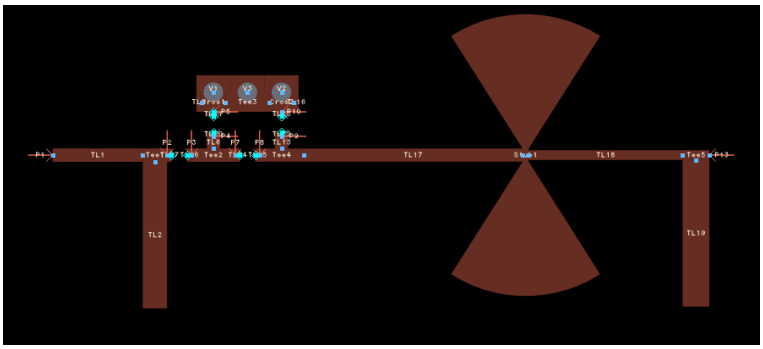

Figure 4.10: Layout extraction of the designed network after applying lumped to distributed conversion.

4.3.1 EM-simulation

Since there are two parallel layers of conducting and ground layers, there might be an effective electromagnetic factor to impair the performance of the network. That is why running EM-simulation is necessary to verify performance of the network. After defining the substrate and ports, ADS can run the EM-simulation based on defined factors and layout. Fig 4.11 demonstrate the circuit schematic to be used in the EM-simulation.

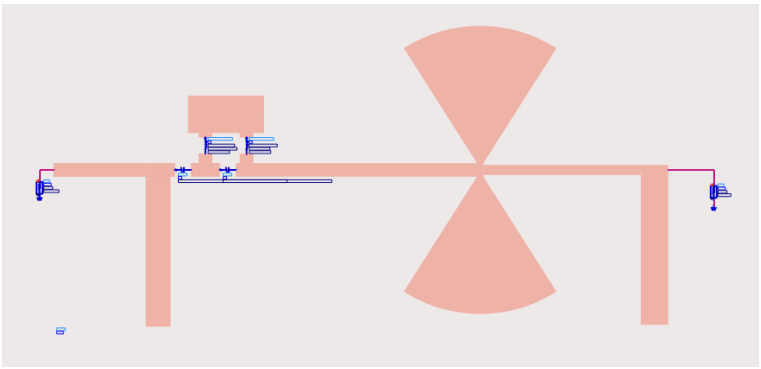

Figure 4.11 Schematic of the network based on EM model.

Finally the optimization yields the best set of components based on optimization goals defined in advance. Figure 4.12 depicts the best TPG graphic found by optimization program.

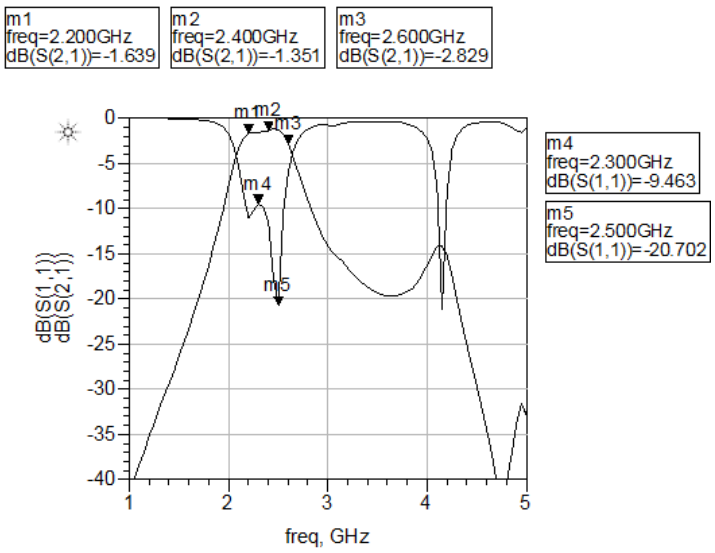

Figure 4.12 Result of the TPG simulation.

5. DESIGN AND IMPLEMENTATION AND MEASUREMENT OF THE TEST CIRCUIT

The impedance matching network is designed to match 6.25 ohm to 50 ohm. Pointing out this fact that the mesuring devices such as Vector Network Analyzor (VNA) use ports with characteristic impedances of 50 ohm, suggests an essential need of an intermediary transformer between 50 ohm port of VNA and the designed network's input, supposed to be 6.25 ohm, for contribution to a straightforward mesurement. Fig 5.1 illustrate the proposed method.

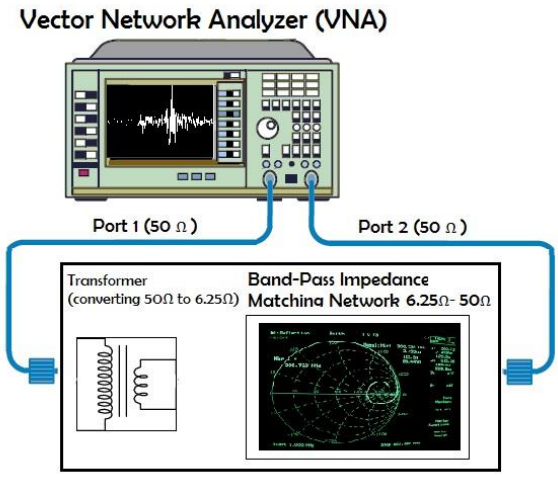

Figure 5.1: The proposed method for measuring the impedance matching network.

In design process of the mentioned transformer, two different approches have been chosen. The first approch is designing a transformer by quarter-wavelength transmission lines and the second one is designing a transformer by lumped elements.

5.1 Designing A Transformer By Quarter Wavelength Transmission Lines

The design process begins with a series of analytical calculations aimed at determining an acceptable set of parameters for the lengths and widths of each quarter-wave section [36].

After determining the wave lengths and characteristic impedances of transmission lines the design accomplished as it is shown in figure 5.2

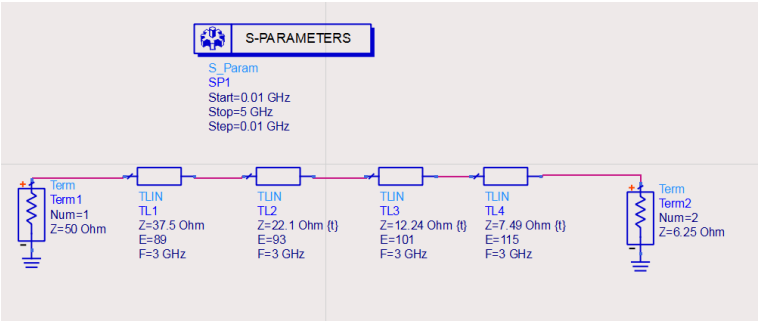

Figure 5.2: The designed transformer by means of quarter wavelength transmission lines.

As it is seen in the schematic brought in figure 5.1, the designed circuit transforms 50 ohm of the input, here is VNA, to a 6.25 ohm port which is the input port of the impedance matching network. The S21 and S11 of the transformer is shown in fig5.3.

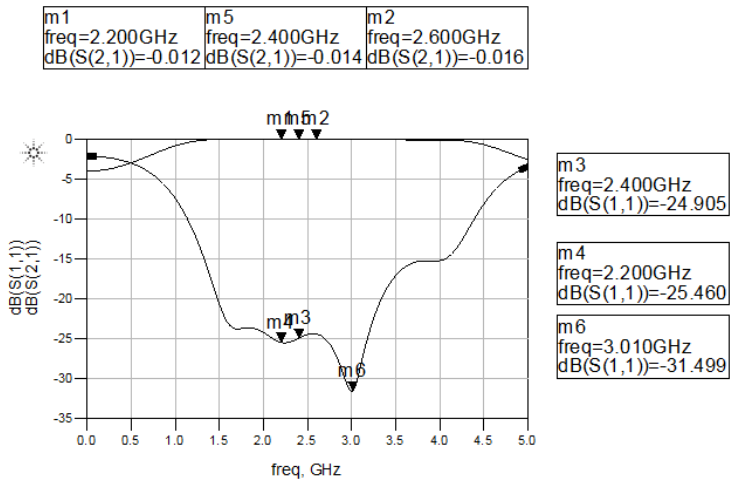

Figure 5.3: The S21 and S11 of the transformer.

As it is seen, the designed transformer performs well in desired bandwidth. Let us attach the transformer to the matching network to investigate the performance of transformer in all whole system. The figure 5.4 depicts the schematic of the whole network

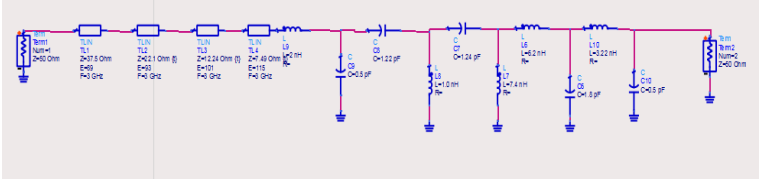

Figure 5.4: The designed transformer attached to impedance matching network.

As it is seen in fig 5.5 the transformer totally satisfies our design goals

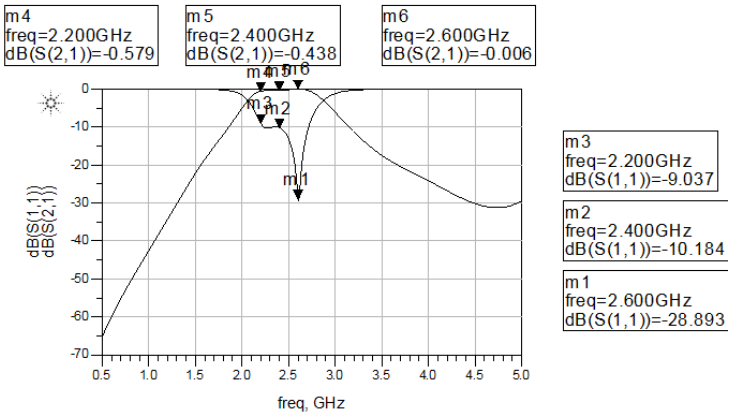

Figure 5.5: S21 and S11 of the schematic in fig 5.3.

5.1.1 Layout and EM simulations

Because of the reasons mentioned in previous chapter, a conversion from ideal transmission lines to microstrip lines should be applied. As shown in figure 5.6, this step benefits the Line Calculator tool in ADS Agilent software.

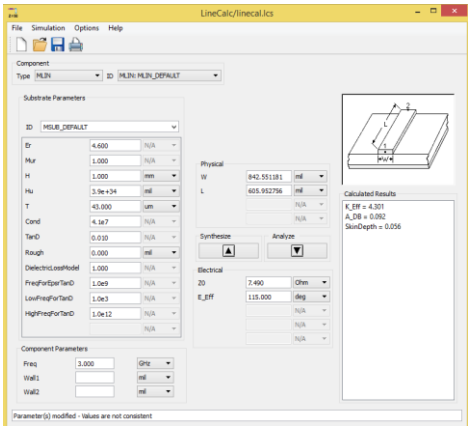

Figure 5.6: ADS line calculator.

The line calculator calculates the width and length of microstrip lines corresponding to ideal transmission lines designed already. Fig 5.7 decpicts the schematic of the transformer set by microstrip lines.

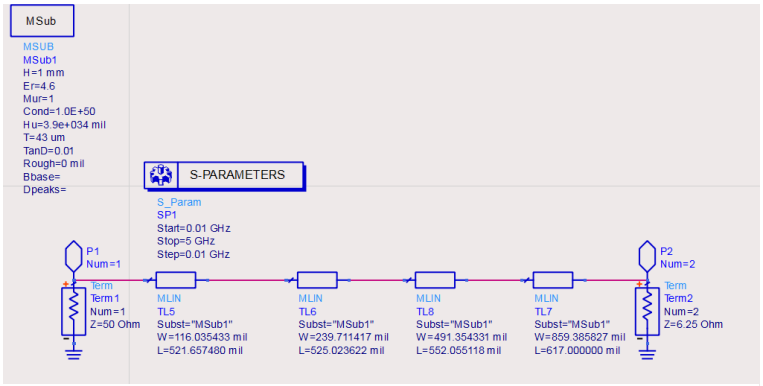

Figure 5.7: The transformer by microstrip lines.

By using Auto-layout extraction feature of the ADS simulator, layout of the transformer is aquired as shown in fig 5.8

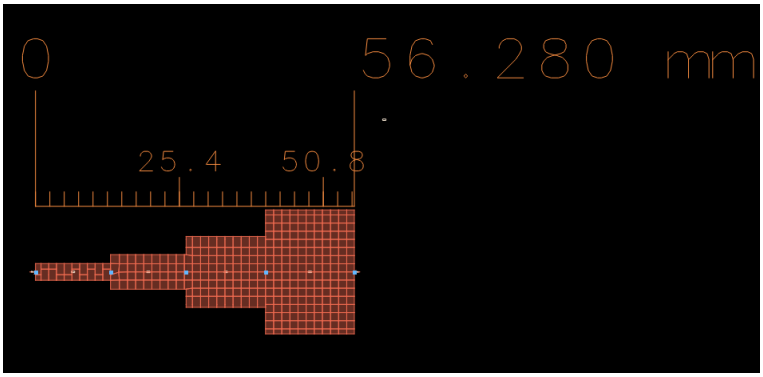

Figure 5.8: Layout of the designed transformer.

As shown in fig 5.9, running a simulation while the EM-extracted model of the transformer is attached to the impedance matching network, gives a perspective about performance of the transformer in test circuit. The simulation results are brought in fig 5.10

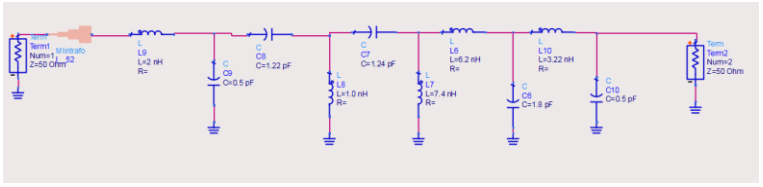

Figure 5.9: The EM-extracted model of the transformer is attached to the impedance matching network.

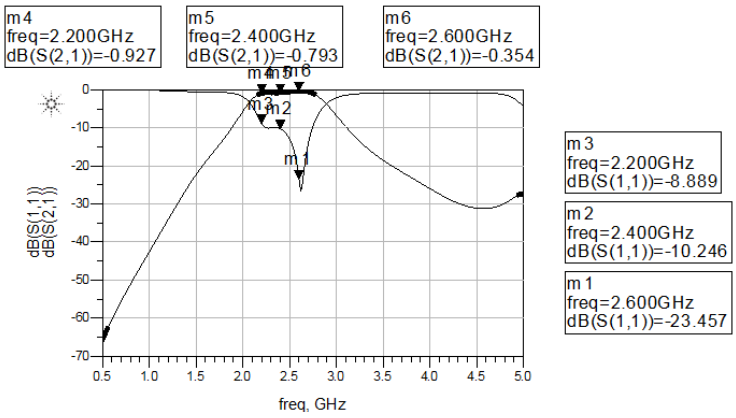

Figure 5.10: S21 and S11 simulation of the schematic in fig 5.9.

5.2 Designing A Transformer By Lumped Elements

Transformers can be realized by means of LC networks as well. Fig 5.11 and Fig 5.12 demonstrate schematic of the designed transformer by means of lumped elements and its corresponding analysis respectively.

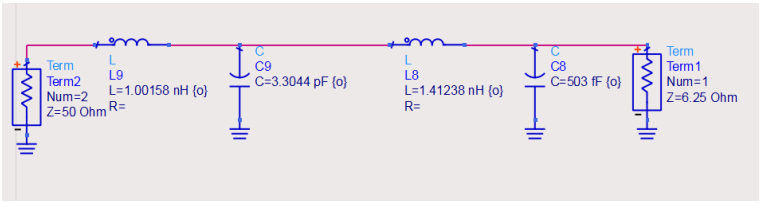

Figure 5.11: Schematic of the transformer designed by means of lumped elements.

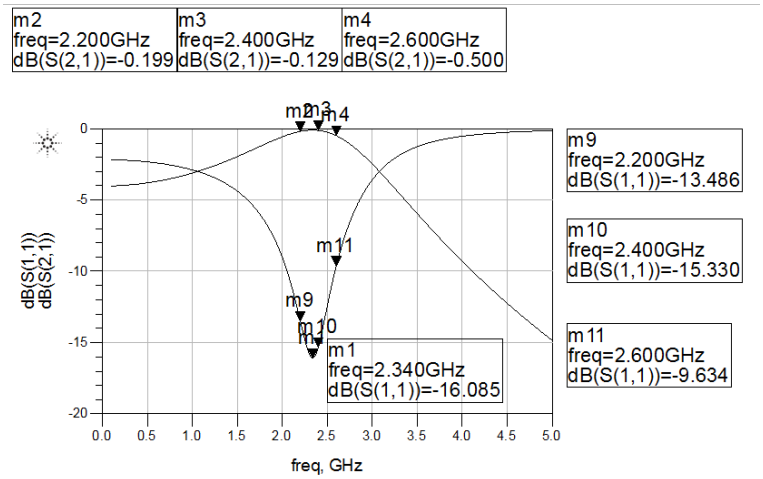

Figure 5.12: S21 and S11 analysis of the schematic in Fig 5.10.

5.2.1 Lumped to distributed conversion

The designd transformer consists of two series inductors and two shunt capacitors. By means of conversion equations (4.1) and (4.2) , the distributed design can be obtained.

After applying conversion equations and running some optimizations the final circuit is to be designed as shown in figure 5.13.

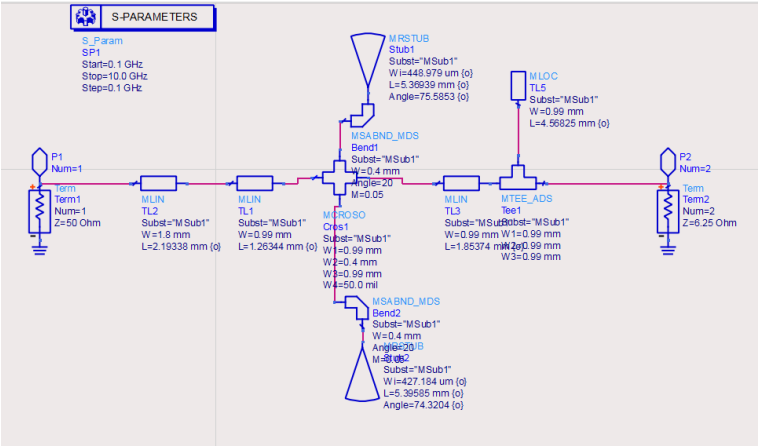

Figure 5.13: The transformer after lumped to distributed conversion.

By using Auto-layout extraction feature of the ADS simulator, layout of the transformer is aquired as shown in fig 5.14

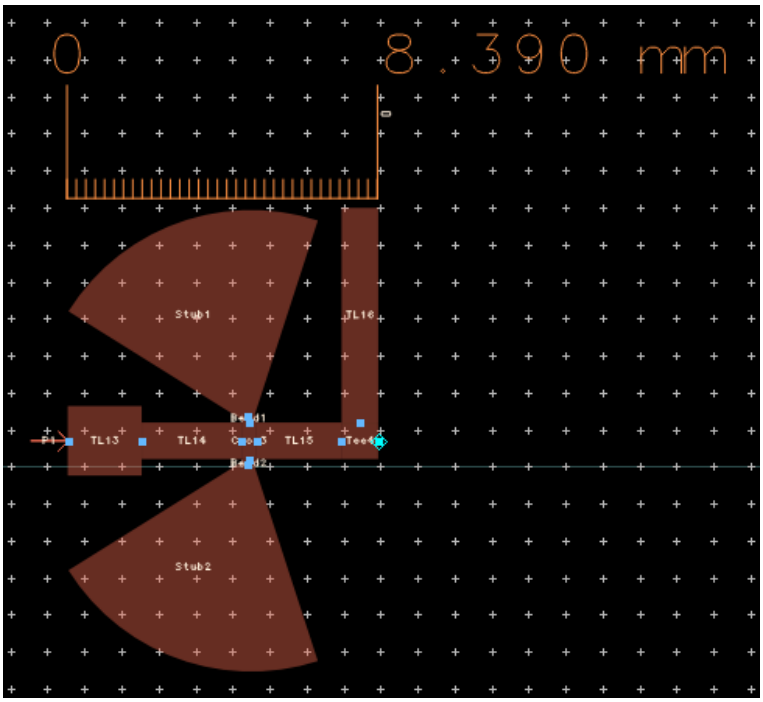

Figure 5.14: Layout of the designed transformer.

The Fig 5.15 demonstrate a good comparison between performance of the transformer with lumped elements and it equivalent distributed design.

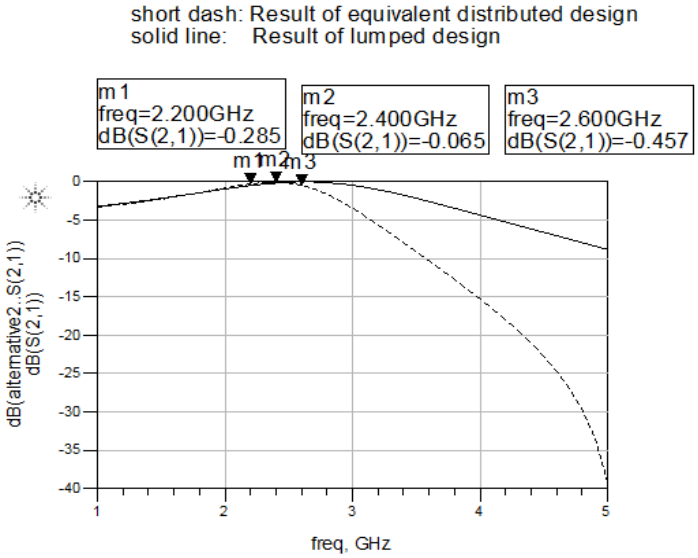

Figure 5.15: A comparison between the design with lumped elements and its equivalent distributed design.

Having run the EM-simulation, the design is attached to the impedance matching network with ideal elements in order to test the transformer's performance in test circuit. The schematic and simulation results are presented in Fig 5.16 and Fig 5.17 respectively.

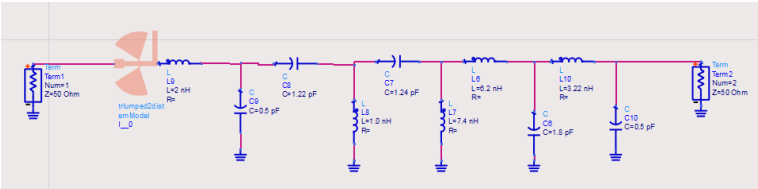

Figure 5.16: Impedance matching network attached to the transformer.

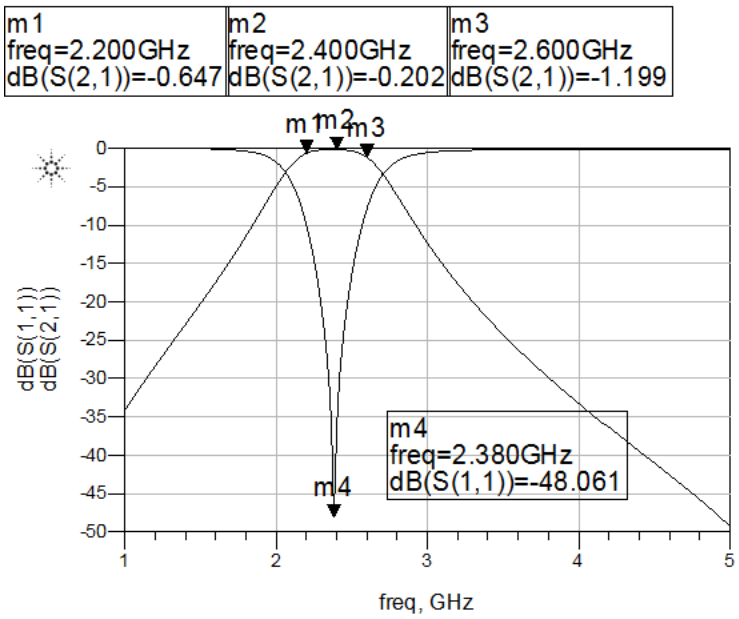

Figure 5.17: S21 and S11 analysis of the schematic in Fig 5.15.

5.3 Implementation Of The Test Circuit

As studied in previous chapter, for sake of accuracy in CAD simulations, some modifications have been applied to the circuit. And the final circuit obtained as circuit in Fig 4.11. By attaching this network to two transformers designed in sections 5.1 and 5.2, the test circuit can be implemented.

5.3.1 Approach 1

The test circuit consists of the impedance matching network and transformer designed in section 5.1

Fig 5.18 -5.20 depict the layout, Schematic and realization of the test circuit respectively

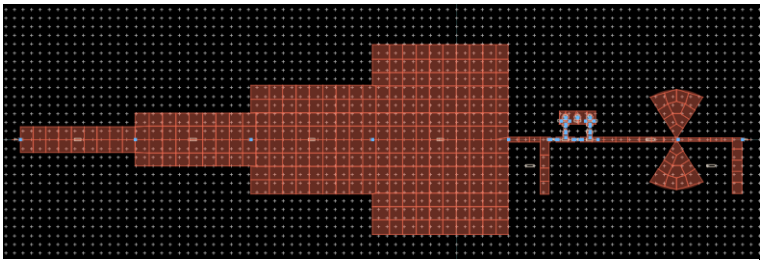

Figure 5.18: Layout of the test circuit by approach 1.

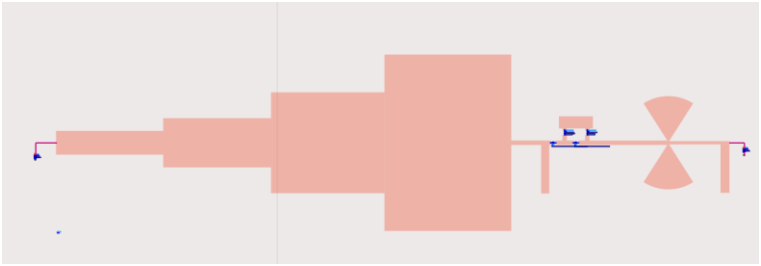

Figure 5.19: Schematic of the test circuit by approach 1 based on the EM-model.

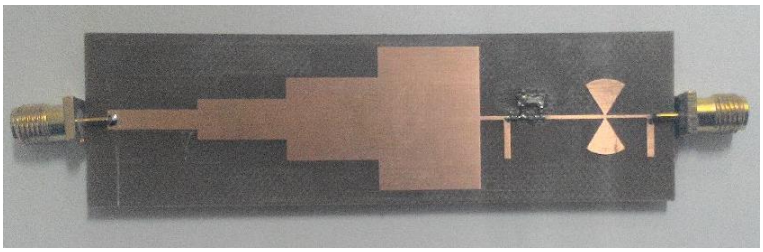

Figure 5.20: Realization of the test circuit by approach 1.

Figure 5.21 compares results of the test circuits in simulation and realization.

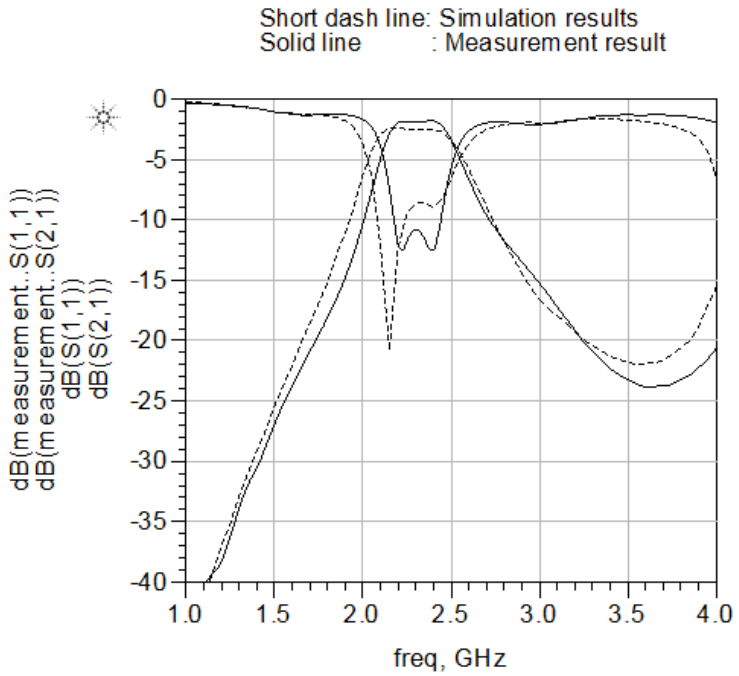

Figure 5.21: Result of the test circuit in simulation and realization.

Data of the plots in Fig 5.21 are presented in Table 5. 1

Table 5.1: Data of the plots in Fig 5.20.

Frequency (GHz)	S21 Simulation (dB)	S21 Measurement (dB)	S11 Simulation (dB)	S11 Measurement (dB)
1.8	-15.194	-18.11	-1.357	-1.257
1.9	-11.088	-14.813	-1.788	-1.293
2	-6.278	-10.31	-3.687	-1.67
2.1	-2.02	-4.97	-12.133	-3.9
2.2	-2.365	-1.964	-12.288	-12.16
2.3	-2.556	-1.933	-8.621	-10.841
2.5	-3.401	-3.39	-6.514	-5.712
2.6	-5.806	-6.646	-3.659	-2.671
2.7	-8.881	-9.603	-2.536	-1.979
2.8	-11.837	-11.714	-2.123	-1.913
2.9	-14.437	-13.491	-1.967	-2.049
3	-16.59	-15.257	-1.986	-2.096

5.3.2 Approach 2

The test circuit consists of the impedance matching network and transformer designed in section 5.1

Fig 5.22 -5.24 depict the layout, Schematic and realization of the test circuit respectively

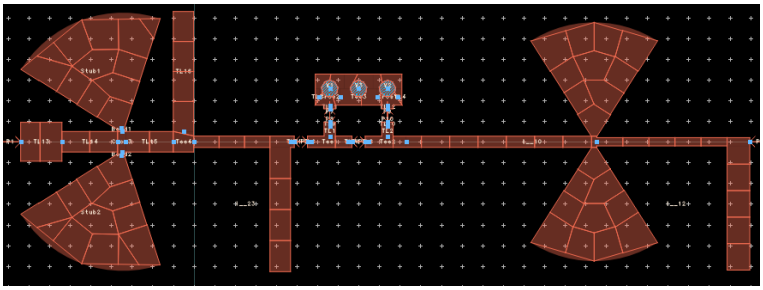

Figure 5.22:Layout of the test circuit by approach 2.

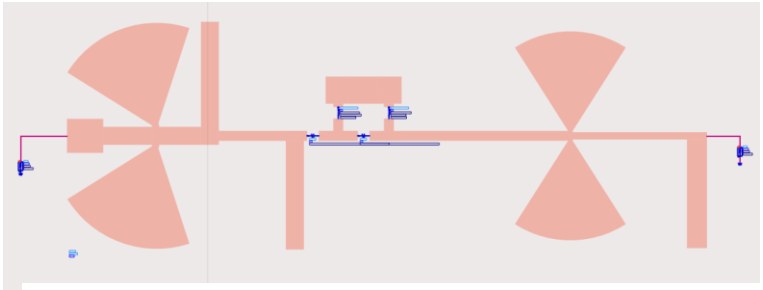

Figure 5.23:Schematic of the test circuit by approach 2 based on the EM-model.

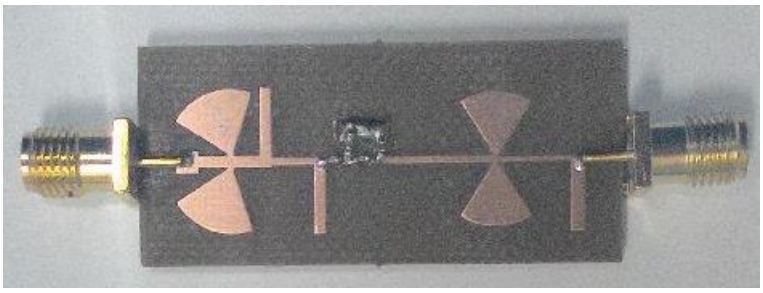

Figure 5.24: Realization of the test circuit by approach 2.

Fig 5.25 compares results of the test circuits in simulation and realization.

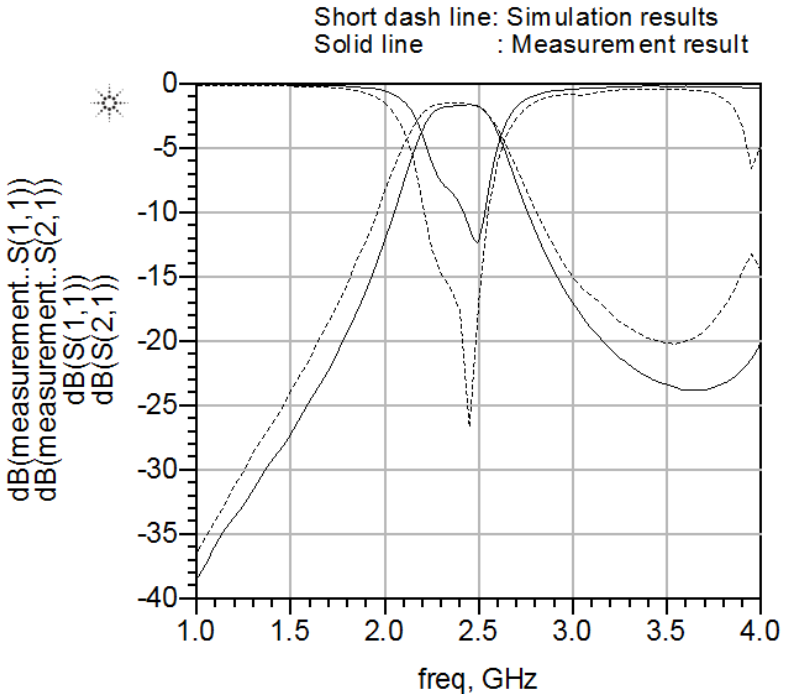

Figure 5.25: Result of the test circuit in simulation and realization.

Data of the plots in Fig 5.25 are presented in Table 5.2

Table 5.2: Data of the plots in Fig 5.25.

Frequency (GHz)	S21 Simulation (dB)	S21 Measurement (dB)	S11 Simulation (dB)	S11 Measurement (dB)
1.8	-15.691	-19.362	-0.44	-0.229
1.9	-12.271	-16.136	-0.748	-0.343
2	-8.324	-12.177	-1.539	-0.591
2.1	-4.795	-7.743	-3.627	-1.39
2.2	-2.274	-3.627	-9.334	-4
2.3	-1.590	-1.906	-14.796	-7.636
2.4	-1.563	-1.719	-17.69	-9.413
2.5	-1.845	-1.797	-16.67	-12.214
2.6	-3.49	-3.855	-6.08	-4.94
2.7	-6.556	-7.743	-2.684	-1.842
2.8	-9.84	-11.453	-1.445	-0.945
2.9	-12.704	-14.593	-0.96	-0.575
3	-15.06	-17.053	-0.883	-0.459

6. INTEGRATED DESIGN

This chapter is about integrated version of impedance matching network, designed by lumped elements in previous chapters. The integrated version is based on the concept that the parasitic effects which modeled as series 2nH inductor and 0.5 pF capacitor still exist. The elements are chosen from TSMC 180nm library also their dimensions get adjusted to desired values then the layout drawing and its verification simulations are presented. Afterwards, its layout is modeled in a cell which is utilized in further simulations. Also some comparing results are brought in order to inquiry the advantages of using network and disadvantages of its making integrated.

6.1 Elements And Dimensions Setting

In this project the technology process of TSMC 180nm is utilized which includes an RF library with prepared layout cells. Inside RF library, "spiral_std_mu_x_20k" and "mimcap_2p0_sin "types are chosen as inductors and capacitors respectively. The Cadence virtuoso can calculate the value of capacitors, while tuning its dimensions as shown in figure 6.1

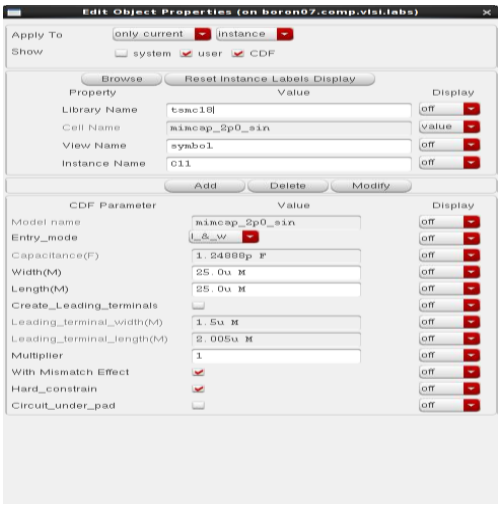

Figure 6.1: There are three effective parameters: length, width and the number of parallel of same capacitor which is named multiplier.

Thus, this feature is not available for inductors. So a value calculator test bench has to be set. As shown in figure this process are done by an AC analysis over two port of inductor. It is well known that the impedance of an inductor is defined as it is in equation 6.1

$$Z = jL\omega \qquad \textbf{(6.1)}$$

So by calculating impedance of the inductor, in an AC analysis, the inductor's value can be obtained. As shown in fig 6.2, the test bench calculates the value of inductor, moreover by running an SP analysis, the test bench extracts scattering parameters of a specific inductor and compares them with those of ideal one with same value.

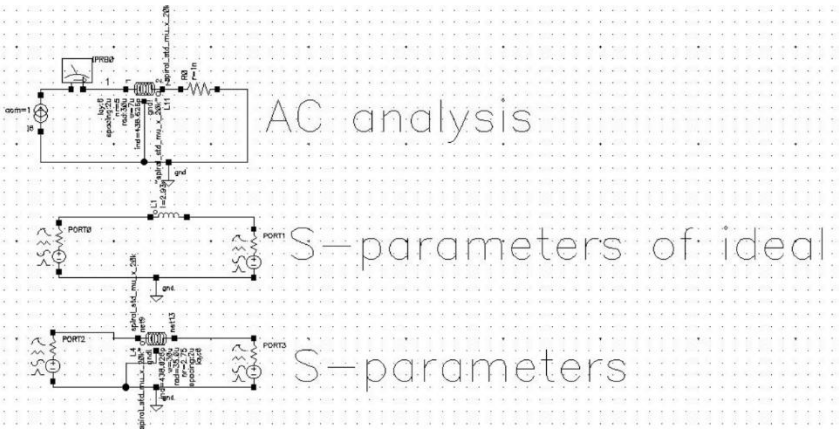

Figure 6.2: The first cell calculates the value of inductor. The second one extracts the scattering parameters of an ideal inductor with the same value as first cell owns. The last cell extracts S-parameters of first cell's .inductor

Stated process have been run through all inductors. As an instance for the inductor 3.2nH- the results are as figure 6.3.

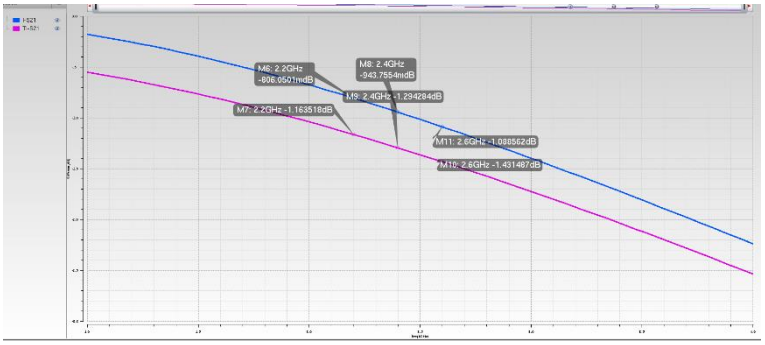

Figure 6.3: S21 (ideal- library model). There is almost a 0.4 dB loss between ideal.

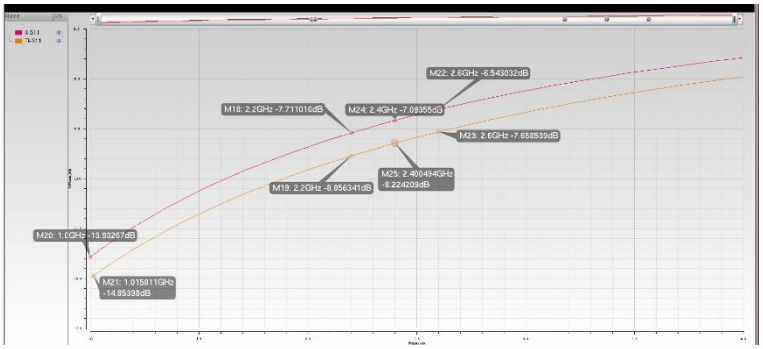

Figure 6.4: S11 (Ideal – library model) There is almost a 0.8 dB loss between ideal inductor and the model inductor by TSMC.

When it comes to comparing transmission and reflected coefficient of model inductor, in comparison to ideal inductor, the reflected coefficient's loss are less than loss of reflected coefficient. The figure 6.5 gives a good perspective about this issue.

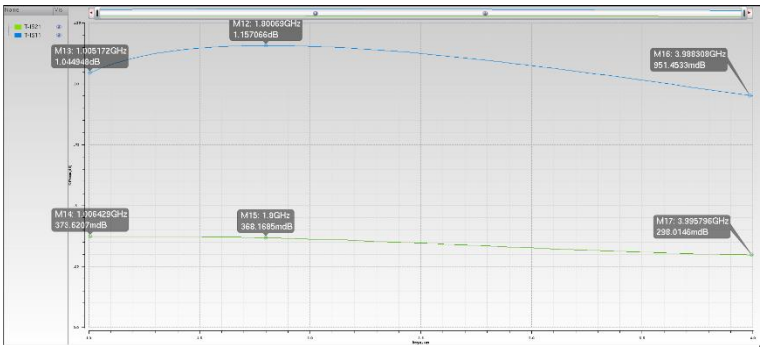

Figure 6.5: Subtraction of scattering parameters of ideal and library model.

After setting dimensions of elements, the schematic is prepared. In order to extract the layout out of schematic and also for using the network in the subsequent simulations, the output and input pins must be set. Fig 6.6 illustrates the schematic.

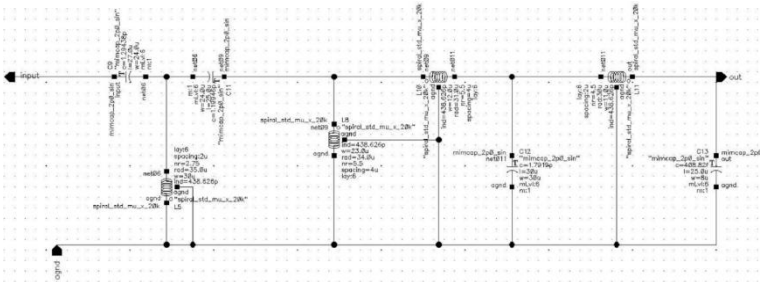

Figure 6.6: Schematic of the network by model elements. The ground, input and output pin is set.

6.2 Layout and Verification

As it is mentioned before, the models have prepared layout cells by extracting and setting connection the layout is ready for post layout analysis. Figure 6.7 illustrates the layout of the design and figure 6.8 depicts the LVS analysis which is a post layout analysis.

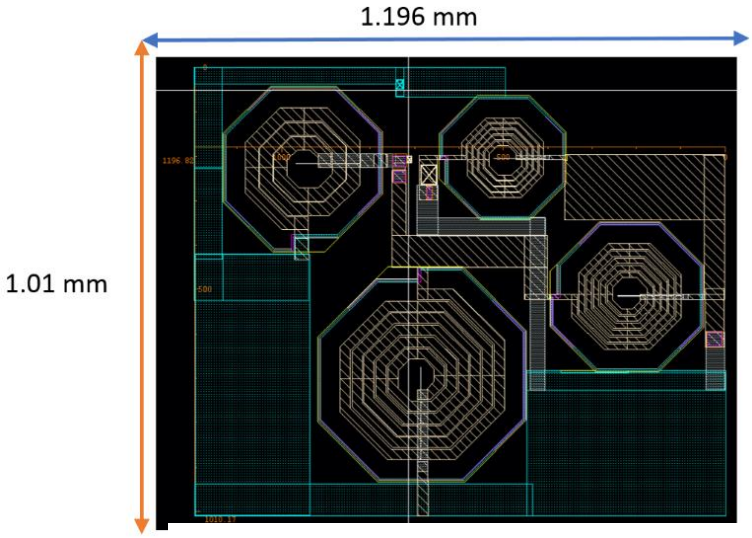

Figure 6.7: The layout of the impedance matching network.

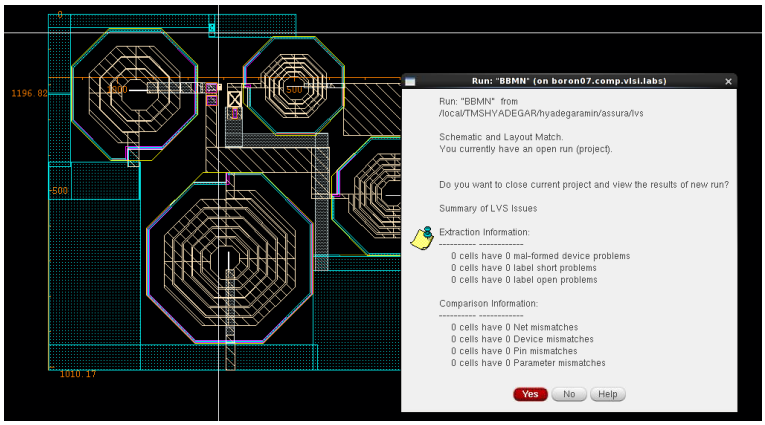

Figure 6.8: LVS analysis of integrated design.

Passing LVS analysis with no error means that the layout totally corresponds the schematic moreover it includes the parasitic effects of layout. Therefore the further simulation is better to be done based on layout cell. In this regard, as it is shown in figure 6.9, by creating a layout cell, all next simulation will be upon layout behavior. By choosing “layout” in cell view window.

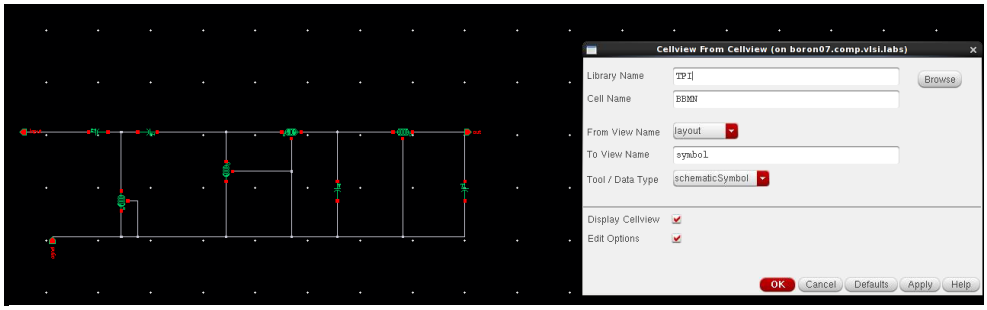

Figure 6.9: Defining the cell based on layout

6.3 Comparing Simulations

In this section three different situations are discussed. First case is where the network is set with all ideal elements. The second design is integrated design with its layout cell and the last one is where there is no impedance matching network applied and 6.25Ω load of data convertor, with its parasitic elements, directly attached to a 50Ω load. The goal of this chapter is examining the effects of model elements besides studying the advantages of using impedance matching network. . The schematic in figure 6.10 includes all explained situations

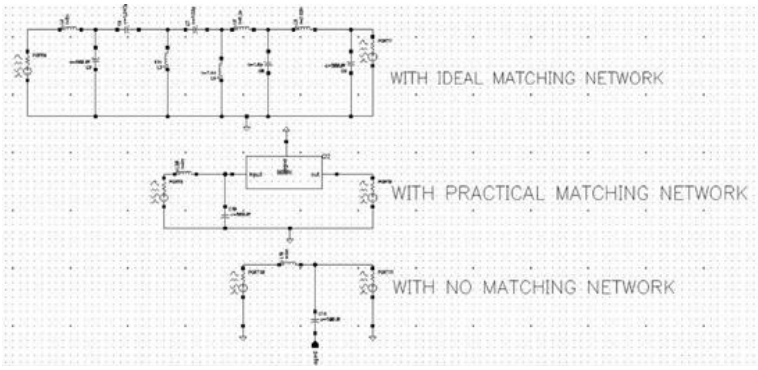

Figure 6.10: The first test bench is the impedance matching network with only ideal elements however the second one includes model elements from TSMC RF library. Finally thelast test bench depicts the condition where there is no matching network.

Fig 6.11 illustrates the compares three designs including the design by ideal elements, a design based on element models of TSMC library and the design with no matching network attached on.

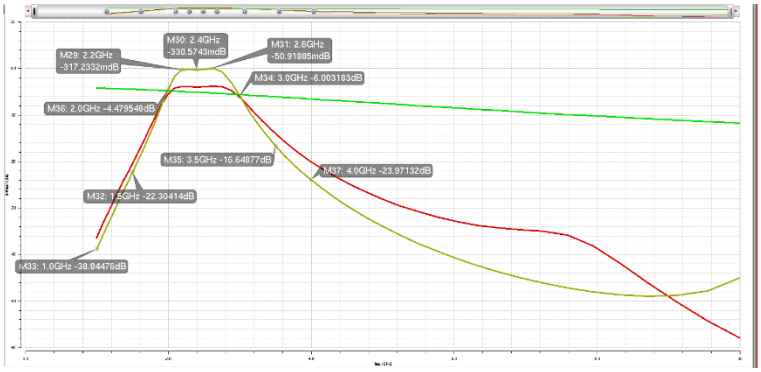

Figure 6.11: S21 graphics of ideal, impedance matched system by TSMC models and totally un-matched system,

As shown in figure 6.11, running the Sp analysis on all situations and plotting S21 of each at the same time, gives good perspective about advantages of the network and disadvantages of lossy integrated inductors

As accurate details the data of graphics are extracted in some frequencies in Table 6.1

Table 6.1: Data of figure 6.11.

Frequency (GHz)/magnitude(dB)	With ideal elements	With TSMC models of components	With no impedance matching network
1	-38.84	-36.30	-4.244
1.5	-22.3	-20.34	-4.95
2	-4.82	-5.55	-5.52
2.2	-0.31	-3.88	-4.97
2.4	-0.327	-4.01	-5.13
2.6	-0.43	-3.83	-5.3
2.8	-1.55	-4.23	-5.47
3	-5.65	-6.23	-5.65
3.5	-16.68	-14.10	-6.1
4	-24	-20.33	-6.58
4.5	-29.5	-24.56	-7

7. CONCLUSIONS AND RECOMMENDTION

The overriding purpose of this thesis is to design and implementation of an impedance matching network for output of a high speed DAC matching 6.25 ohm to 50 ohm in a band width of 400 MHz with center frequency of 2.4 GHz. As studied in chapter two, this goal was accomplished by utilizing Simplfied Real Frequency Technique. Including parasitic effects which modeled by two lumped elements, the designed network is made out of 10 passive elements which could be implemented by lumped elements. However, due to weak realization technology such as soldering technology, it was prefferd to use the equivalent distributed form of lumped elements. After applying conversions, in order to make a straightforward measuring, test circuits was designed. The test circuit consists of a transformer preceding to the impedance matching network and after the measuring device transforming 50 ohm (characteristic impedance of the measuring device) to 6.25 ohm. The transformer was designed in two approches. The first was designed by using quarter wave length transmission lines and the other by lumped elements. Both of the test circuits was realized and measured. As the last chapter, the integrated form of the design was presented. Although the band pass characteristic of the TPG plot of the impedance matching network with integrated elements resembled to its counterpart design with disceret elements, there was a significant loss in TPG due to integrated inductors which suffer from low Q factor. In this regard, in order to decrease the loss, the integrated design should either be designed with lower quantity of inductors which in turn, impairs the band pass characteristics such as sharpness, or be designed with active elements to compensate the loss steming from inductors which in trurn causes much power consumption.

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