DESIGN AND OPTIMIZATION OF A SUB-1dB NOISE FIGURE LOW NOISE AMPLIFIER FOR MAGNETIC RESONANCE APPLICATIONS USING CMOS TECHNOLOGY

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By

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Design and Optimization of a Sub-1dB Noise Figure Low Noise Amplifier for Magnetic Resonance Applications Using CMOS Technology
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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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December 2024

Low Noise Amplifiers (LNAs) are crucial components in magnetic resonance imaging (MRI) receivers, primarily designed to amplify weak signals while minimizing the added noise. They have a special requirement of having an input impedance very close to a short-circuit. This requirement assures that there is no current in the MRI coil when the LNA is connected to the coil with a quarter-wave transmission line. By eliminating the current in the coil, the risk of coupling between coils also known as mutual coupling, within an array is reduced. This thesis explores designs of sub-1dB noise figure CMOS LNAs operating at 437 MHz and 477 MHz for 10.3 T and 10.5 T MRI systems, respectively, using variations of cascode amplifier structures while addressing the challenges and advancements in CMOS RF design. The first LNA designed for a singular 10.3 T MRI coil system demonstrates a power gain of 20.54 dB, a noise figure of 0.97 dB, an input return loss of -11.70 dB, and an IIP3 of -12.26 dBm with its fully modeled design. For a 10.5 T Array MRI system, one single-ended and one differential-ended LNA is designed. The single-ended demonstrates a power gain of 18.42 dB, a noise figure of 0.42 dB, an input return loss of -0.90 dB, an output return loss of -18.03 dB, and an IIP3 of -17.12 dBm, whereas the differential-ended demonstrates a power gain of 14.76 dB, a noise figure of 0.60 dB, an input return loss of -0.94 dB, an output return loss of -18.73 dB, and an IIP3 of -14.36 dBm both with their fully modeled designs. The differential amplifier also displays a significant improvement in PSRR, making it a good choice for array MRI applications.

Keywords: Low Noise Amplifiers (LNAs), CMOS Technology, Magnetic Resonance Imaging, Noise Figure, Cascode Amplifier, Noise Optimization Method.

ÖZET

CMOS TEKNOLOJİSİ KULLANILARAK MANYETIK REZONANS UYGULAMALARI İÇİN 1DB ALTINDA GÜRÜLTÜ RAKAMINA SAHİP DÜŞÜK GÜRÜLTÜLÜ AMPLİFİKATÖR TASARIMI VE OPTİMİZASYONU

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Düşük Gürültülü Yükselteçler (Low Noise Amplifiers, LNAs), manyetik rezonans görüntüleme (MRI) alıcılarında zayıf sinyalleri yükseltirken eklenen gürültüyü en aza indirmek için tasarlanmış kritik bileşenlerdir. MRI sistemlerinde LNAs, giriş empedanslarının kısa devreye çok yakın olmasını gerektirir. Bu özellik, LNA'nın bir çeyrek dalga iletim hattı üzerinden MRI bobinine bağlandığında bobinde akım oluşmamasını sağlar. Bobindeki akımın ortadan kaldırılmasıyla, bir dizi içindeki bobinler arasındaki karşılıklı bağlaşım (mutual coupling) riski önemli ölçüde azaltılır ve bu durum sistemin genel performansını ve görüntü kalitesini iyileştirir. Bu tez, 10.3T ve 10.5T MRI sistemleri için sırasıyla 437 MHz ve 477 MHz'de çalışan, kas kod yükselteç yapılarının farklı varyasyonlarını kullanarak tasarlanmış, 1dB'nin altında gürültü figürüne sahip CMOS LNAs'ların tasarımına odaklanmaktadır. Tek bobinli 10.3T MRI sistemi için tasarlanan ilk LNA, tamamen modellenmiş tasarımıyla 20.54 dB güç kazancı, 0.97 dB gürültü figürü, -11.70 dB giriş yansıma kaybı ve -12.26dBm IIP3 performansı göstermektedir. 10.5T dizi MRI sistemi için bir tek uçlu ve bir diferansiyel uçlu LNA tasarlanmıştır. Tek uçlu LNA, 18.42 dB güç kazancı, 0.42 dB gürültü figürü, -0.90 dB giriş yansıma kaybı, -18.03 dB çıkış yansıma kaybı ve -17.12 dBm IIP3 performansı sergilerken, diferansiyel uçlu LNA 14.76 dB güç kazancı, 0.60 dB gürültü figürü, -0.94 dB giriş yansıma kaybı, -18.73 dB çıkış yansıma kaybı ve -14.36 dBm IIP3 performansı göstermektedir. Ayrıca, diferansiyel yükselteç önemli bir güç kaynağı reddetme oranı (PSRR) iyileştirmesi sunarak, dizi MRI uygulamaları için iyi bir seçenek olduğunu kanıtlamaktadır.

Anahtar sözcükler: Düşük Gürültü Yükselteçleri, CMOS Teknolojisi, Manyetik

Rezonans Görüntüleme, Gürültü Figürü, Cascode Yükselteç, Gürültü Optimizasyon Yöntemi.

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Chapter 1

Introduction

1.1 Low Noise Amplifier (LNA)

A Low Noise Amplifier (LNA) is an essential element in any radio frequency (RF) receiver, primarily amplifying weak signals and enhancing the signal-to-noise ratio. The primary function of an LNA is to amplify the incoming weak signal while adding as minimal noise as possible. In cascaded systems, the noise figure of the first amplification stage is particularly influential, making the LNA's role critical in ensuring overall system performance [1]. Power gain, which can also be defined as a small signal amplification capability, is another crucial parameter of an LNA.

LNAs play a critical role in Magnetic Resonance Imaging (MRI) receiver systems by significantly enhancing the quality of the received signals. MRI works by using the effects of Nuclear Magnetic Resonance (NMR) to create an image of the portion of the body that is scanned. As a result of NRM, weak RF signals emitted by nuclei within the body are captured by the MRI system's coils and must be amplified without adding excessive noise. The LNA, placed at the front end of the MRI receiver, is responsible for amplifying these signals while maintaining a low noise figure to preserve the purity of the signal and total signal-to-noise ratio

(SNR) of the system. By minimizing the noise introduced during amplification, LNAs ensure that the MRI system can produce high-quality images for medical diagnoses [2].

MRI receiver systems can either use a single coil or an array of coils to sense the emitted signal.An array of coils aids in achieving a more sensitive MRI system by capturing signals from multiple regions simultaneously, improving spatial resolution and signal-to-noise ratio (SNR).However, it poses different requirements on the LNA design. In single-coil systems, the LNA input impedance is matched to the coil's impedance of 50 Ω to maximize power transfer and minimize signal reflection, ensuring an input return loss (S_{11}) below 0 dB. On the other hand, in array systems, the LNA's input impedance must resemble a short circuit, achieving an S11 near 0 dB when connected with a quarter-wave transmission line. This short-circuit condition eliminates current in the coil, minimizing mutual coupling and providing decoupling between coils in the array. The differing (S_{11}) requirements highlight the design trade-offs between optimizing for power transfer in single-coil systems and reducing interference in array configurations [3].

In an ideal world, an LNA would be designed to achieve both maximum power gain and minimal additional noise. Still, a trade-off must be made between these two metrics as they cannot be obtained simultaneously due to limitations in electronic components and circuit design [4]. In high-frequency applications such as the ones in this thesis, off-chip components, especially SMD inductors, are often a requirement to achieve precise impedance matching and noise optimization. However, using large inductors with values close to 75 nH at the gate of the input transistor presents significant challenges in terms of noise figures and input return loss. A large inductor is necessary at these frequencies to provide the required reactance for tuning and noise matching. However, integrating such components on-chip is impractical due to size constraints and inherent parasitics. Off-chip inductors, particularly the large SMD types, suffer from substantial parasitic resistance and capacitance, drastically reducing their quality factor (Q). This low Q reduces the inductor's efficiency and amplifies power losses. Furthermore, the parasitic capacitances and inductances introduced by bonding these components to the input pads of the chip can degrade the LNA's overall performance and

stability, making this approach a considerable design challenge.

In the past, GaAs and SiGe technologies were often preferred for high-performance radio frequency (RF) designs due to their superior performance compared to Si in a classic Complementary Metal-Oxide-Semiconductor (CMOS) process. Due to their intrinsic properties, GaAs and SiGe offer excellent noise performance, essential for highly low-noise LNA applications [5]. However, nowadays, the cost-efficiency of CMOS and the flexibility of combining RF, digital, and analog circuits into a single chip has opened the doors for high-frequency design in CMOS technology. Although designing RF circuits in CMOS has numerous advantages for the overall system performance, it brings inherent challenges and limitations to the design and performance of the RF block. The main challenge is noise performance for an LNA.

In this thesis, the RF design world in CMOS is investigated, and a sub-1dB noise figure LNA is designed to operate at 437 MHz and 447 MHz, Larmor frequencies for a 10.3 Tesla (T) and 10.5T magnetic resonance receiver, respectively. The LNA designed for a 10.3T system is purposefully matched to a 50Ω input to satisfy the matching conditions of a singular MRI coil application. The LNAs designed for a 10.5T system are specifically mismatched at the input to provide decoupling between coils in array MRI applications. An inductively generated cascode amplifier structure is used to obtain a power gain of 20.54 dB, a noise figure of 0.97 dB, an input return loss of -11.70 dB, and an IIP3 of -12.26 dBm for the fully RLC extracted LNA model for a 10.3T system with all possible parasitics. For the 10.5 T Array MRI system, a single and differential-ended circuit using a cascode topology with inductive peaking is designed. The single-ended demonstrates a power gain of 18.42 dB, a noise figure of 0.42 dB, an input return loss of -0.90 dB, an output return loss of -18.03 dB, and an IIP3 of -17.12 dBm, whereas the differential-ended demonstrates a significant increase in PSRR, a power gain of 14.76 dB, a noise figure of 0.60 dB, an input return loss of -0.94 dB, an output return loss of -18.73 dB, and an IIP3 of -14.36 dBm both with their fully modeled designs.

1.2 Performance Metrics

An LNA's primary design goal is optimizing its noise figure. After all extractions and parasitics, the noise figure should be under 1 dB to satisfy the sub-1dB goal for all designs. All of the performance metrics set for the final designs can be seen in Table 1.1.

Table 1.1: Performance metrics for the LNA

	min.	max.
S_{21} (dB)	15	
S_{11} (dB)		-1
$\angle S_{11}$	$-15°$	$+15°$
S_{22} (dB)		-10
S_{12} (dB)		-45
NF (dB)		1
IIP_3 (dBm)	-15	
$IP1$ (dBm)	-25	
P (mW)		20
K	1.1	

1.3 Motivation

This thesis aims to design a sub-1dB NF LNA in CMOS technology for various MRI systems and to verify it using lumped models of all parasitic components to get the most realistic results possible. The CMOS technology's noisy nature and high-value parasitics that arise at high operation frequencies make designing an extremely low-noise figure amplifier challenging. Additionally, making the input impedance of the transistor resemble an open circuit at such high frequencies is especially difficult due to the low-quality factor of large SMD inductors and the high input capacitance of the transistor, which together limit the effectiveness of impedance tuning. This thesis will detail the design and walk the reader through the steps of achieving this low-noise performance.

1.4 Thesis Outline

In Chapter 1, a brief introduction to low noise amplifiers and MRI systems, the set performance metrics for the to-be-designed LNA, and the motivation behind the topic of this thesis are given. Chapter 2 introduces the fundamental RF concepts that are crucial to know to understand an LNA's operation and design. The working principles of MRI systems and their implementations in LNAs are also discussed. In Chapter 3, the most common CMOS LNA topologies are discussed and a literature review of the works most relevant to the design in this thesis is performed. In Chapter 4, the design methodologies that can be used to decide on the optimum transistor size and biasing condition for minimum NF are discussed and compared. In Chapter 5, the complete design procedure of the LNA takes place. The chapter starts by choosing the transistors' optimum sizes and biasing points. It then discusses the input matching circuit and highlights the critical steps of the design to ensure the most optimal noise operation. Chapter 6 gives the LNA pre and post-layout simulation results in detail. This chapter clearly shows a detailed model of the LNA design, including bond wire, bonding pad, and external SMD component parasitics. Chapter 7 discusses the LNAs designed for 10.5 T Singular and Array MRI applications and gives the complete simulation results. Lastly, in Chapter 8, a summary of the work done throughout the thesis and possible future work are discussed.

Chapter 2

Basic RF Concepts of LNA Design and MRI Applications

Fundamental RF concepts are a crucial background to have for designing effective LNAs. Knowing the math and logic behind the parameters that need to be optimized and measured is necessary. In this chapter, the fundamental RF concepts required to design an LNA and understand the flow of the thesis are given. All concepts will be based on [1] and [6].

2.1 S-Parameters

S-parameters, also known as scattering parameters, describe the electrical behavior of linear RF networks in the frequency domain. They are instrumental at high frequencies where the performance of circuits is impacted by reflections, impedance mismatches, and other high-frequency effects.

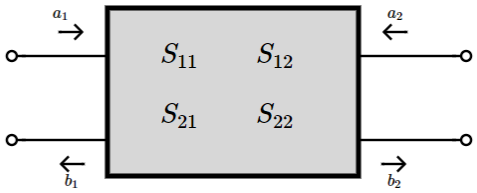


Figure 2.1: General two-port network

2.1.1 Definition of S-parameters

S-parameters relate the incident and reflected waves at the ports of a network. For a two-port network in Fig. 2.1, the S-parameters are defined as:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0}, \quad S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \quad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}, \quad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2.1}$$

where

- a_1, a_2 are the incident waves at port 1 and port 2, respectively.
- b_1, b_2 are the reflected waves at port 1 and port 2, respectively.

Under matched load conditions, the input scattering parameter equals the input reflection coefficient.

$$S_{11} = \Gamma_{in} \tag{2.2}$$

Similarly, the output scattering parameter equals the output reflection coefficient under matched source conditions.

$$S_{22} = \Gamma_{out} \tag{2.3}$$

2.1.2 Input and Output Return Losses

The input return loss is a measure of how much power is reflected back to the source due to impedance mismatch at the input port. It is related to S_{11} and is

expressed in dB as

$$\text{Input Return Loss (dB)} = -20\log|S_{11}| = -20\log|\Gamma_{in}| \tag{2.4}$$

Similarly, the output return loss is related to S_{22} and represents the reflection at the output port. The output return loss can be expressed as

$$\text{Output Return Loss (dB)} = -20\log|S_{22}| = -20\log|\Gamma_{out}| \tag{2.5}$$

2.2 Power Gain

Power gain describes the amplification provided by the LNA. The most commonly used power gain parameters based on certain matching criteria are

- Transducer Power Gain G_T

$$G_T = \frac{P_L}{P_S} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{2.6}$$

  where P_L is the power delivered to the load, and P_S is the power available from the source. It is essentially the power gain considering the effect of both source and load impedance mismatches.

- Available Power Gain G_A

$$G_A = \frac{P_A}{P_S} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{out}|^2} \tag{2.7}$$

  where P_A is the power available from the network, and P_S is the power available from the source. It is the power gain, assuming the load is perfectly matched to the circuit's output impedance. Available gain circles are functions of the source reflection Γ_S. They can be drawn on the Smith chart of Γ_S to find locations of the Γ_S corresponding to a G_A value. In short, the optimum source impedance for the highest operating power gain can be found using the available gain circles.

- Operating Power Gain G_P

$$G_P = \frac{P_L}{P_A} = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{2.8}$$

  where P_L is the power delivered to the load. It is the power gain, assuming the source perfectly matches the circuit's input impedance. Power gain circles (GPC) are functions of the load reflection Γ_L. They can be drawn on the Smith chart of Γ_L to find locations of the Γ_L corresponding to a G_P value. In short, by using the GPC circles, the optimum load impedance for the highest operating power gain can be found.

2.3 Noise Figure

The noise factor (F) is defined as the ratio between the input signal-to-noise (SNR) and the output signal-to-noise ratio. It is defined mathematically as

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{G_A N_{in}}{N_{out}} = 1 + \frac{N_{amp}}{G \cdot N_{in}} \tag{2.9}$$

in which G_A is the gain of the amplifier, N_{amp} is the noise of the amplifier, N_{in} is the input noise and N_{out} is the total output noise. From the noise factor F, noise figure (NF) can be defined as

$$NF = 10\log(F) \tag{2.10}$$

From Friis equations for cascode stages, the first stage mainly determines the overall noise figure. Therefore, the noise performance of the first stage has to be optimized for a low noise design.

2.4 Stability

An LNA must be stable to prevent oscillations. Stability can be determined using the Rollett stability factor K and the Δ parameter:

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|} \tag{2.11}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.12}$$

For unconditional stability, $K > 1$ and $|\Delta| < 1$ conditions must hold.

2.5 Linearity Performance: IIP3 and IP1dB

Nonlinearities in an LNA can generate unwanted harmonics and intermodulation products. Two key metrics used to evaluate linearity are the third-order intercept point (IIP3) and the 1 dB compression point (IP1dB) at the input.

The IIP3 measured in dBm represents the input power level at which the power of the third-order intermodulation products equals the power of the fundamental signal. It is important for the IIP3 to be high in an LNA so that the device can handle large signals without introducing any unwanted signals into the spectrum and making it dirty.

The 1 dB compression point is the input power level at which the gain of the amplifier drops by 1 dB from its small-signal gain value. The IP1dB value reflects how large of a signal an LNA can handle without going into saturation. A general rule of thumb for IIP3 is the following:

$$\text{IIP3 (dBm)} = \text{IP1dB (dBm)} + 10 \tag{2.13}$$

Increasing the supply current or size of the transistors in an LNA is usually an effective way to increase its linearity. However, these also increase the NF of the design. Therefore, linearity a trade-off needs to be made between linearity and NF in an LNA.

2.6 MRI Applications

2.6.1 MRI Working Principle

Magnetic Resonance Imaging (MRI) systems operate on the principle of Nuclear Magnetic Resonance (NMR), where certain atomic nuclei within parts of the body, particularly protons, are excited using electromagnetic energy. This excitation causes spins in the atomic nuclei which when relaxed back to the original lower energy state, release energy. This energy is picked up by MRI's magnetic system and eventually formed into an image.

The spin state of a particle determines whether the particle becomes attracted to or repelled from a magnetic field when moving through it. In a magnetic field, this spin state becomes biased parallel to the field. Although the particle remains stationary, the spin vectors precess around the axis of the field. The rate of this precession is called the $Larmor frequency$, f_0 which can be defined as

$$f_0 = \frac{\gamma}{2\pi} B_o \tag{2.14}$$

in which B_0 is the strength in Tesla (T) of the static magnetic field and

$$\frac{\gamma}{2\pi} = \frac{q}{2m} = 42.577\text{MHz/T} \tag{2.15}$$

for a proton. Therefore, if a proton is placed in a magnetic field of 10.5T, it will precess at a frequency of

$$f_0 = (42.577\text{MHz/T})\text{x}(10.5\text{T}) = 447\text{MHz} \tag{2.16}$$

The same calculation can be done for a magnetic field of 10.3T to obtain an f_0 of 437 MHz. As protons within a particle realign with the magnetic field, they will release energy at these defined f_0 frequencies called the $LarmorFrequency$ [7]. The energy released at these frequencies is detected by MRI coils to create images of the location of the body which was scanned.

2.6.2 LNA Usage in an MRI

The energy released from a particle is picked up by an RF reception coil tuned to the respective Larmor frequency within the MRI receiver system. The signal picked up by the coil is then transferred to an LNA for amplification and then passed on to further systems for digitization. The total required acquisition time of a scan depends on several factors such as the receiver bandwidth and sampling conditions, but it is not directly proportional to f_0. Additionally, the signal-to-noise ratio (SNR) of the image is influenced by various factors like signal strength and system noise, rather than being inversely related to f_0. Therefore, a decrease in scan time does not necessarily lead to a proportional decrease in the SNR of the image. [8].

One of the main advantages of increasing f_0 is that it allows for higher resolution imaging. At higher frequencies, the signal bandwidth increases, enabling better separation between the signal and noise, which can improve the overall image quality. Moreover, higher Larmor frequencies can reduce the susceptibility to low-frequency noise. However, while increasing the Larmor frequency may provide these benefits, it does not directly reduce acquisition time. To minimize scan time effectively, it is essential to optimize the noise performance of the system and the first stage LNA.

Another way to improve the SNR of the image obtained from the system is to employ an array of receiver coils. In some applications, a single coil is used to receive the RF signal, however an array application is more beneficial in terms of SNR. However, having an array of coils comes with extra specifications to the LNA. In single-coil systems, the LNA's input impedance is matched to the coil's impedance to ensure efficient power transfer and optimal noise performance. In contrast, for array systems, the LNA's input impedance must resemble a short circuit when connected via a quarter-wave transmission line to suppress coil currents and minimize mutual coupling between closely spaced coils [9].

In this thesis, LNAs suitable for 10.3 T single coil and 10.5 T array coil systems are designed.

Chapter 3

LNA Design Topologies in CMOS

The performance of an LNA is highly dependent on the chosen process technology. Thanks to the advances in CMOS processes, RF devices, especially LNAs, can now achieve optimal performance with the process's low power and easy fabrication advantages. While most of the examples in literature for LNAs were done in GaAs and GaN technologies using MESFET or HEMT transistors, designers have come up with primary structures for CMOS LNAs, with each having their advantages and drawbacks. Before exploring these structures, it is crucial to introduce and understand the primary noise sources in CMOS that must be minimized to achieve a sub-1dB noise operation.

3.1 Noise Parameters of MOS Transistors

The first primary noise in MOSFETs is thermal noise generated by the random thermal motion of charge carriers in a restive material. Due to the nature of these devices, they essentially act as voltage-controlled resistors and exhibit this characteristic. The thermal noise of a MOSFET operating in the saturation region, which is usually the case in LNA applications, can be modeled as shown in Fig. 3.1 as a current source between the source and drain regions:

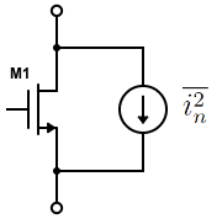


Figure 3.1: Thermal channel noise of a MOSFET

$$\overline{i_n^2} = 4kT\gamma g_{do}\Delta f \tag{3.1}$$

where g_{do} is the triode drain-source conductance and γ is defined as the excess noise coefficient [1]. When it comes to submicron CMOS devices with shorter channel lengths, this phenomenon is believed to pose a threat to low-noise operation due to the heating of carriers as a result of large electric fields [10]. Other sources blame the excess noise in short channel devices on the noise resulting from the substrate resistance and emphasize that excess noise resulting from the substrate will be dominant at frequencies below 1GHz, which falls into the range of the design of this thesis [11].

Resistance coming from the gate connections introduces an additional component to the thermal noise of a MOSFET, which becomes more critical as gate lengths decrease. However, these effects can be minimized by dividing the gate and drain terminals into multiple fingers and adding more contact points during the layout process [6].

Flicker noise, also known as the 1/f noise, is another phenomenon that degrades the noise performance of CMOS designs. Traps at the semiconductor-oxide interface capture and release charge carriers, which cause changes in the current and introduce noise in the channel. This noise shows an inversely proportional relation to frequency, and its model as a current source between the drain and source of a transistor can be modeled as:

$$\overline{i_n^2} = g_m^2 \frac{K}{WLC_{ox}} \frac{1}{f} \tag{3.2}$$

in which K is a constant dependent on the process. Although K is lower for PMOS devices, higher electron mobility, transconductance, and overall lower noise make the NMOS the supreme device in an LNA design. Though flicker noise is negligible at higher frequencies, it is still a concern regarding additional noise for LNA designs operating close to the flicker noise corner frequency, which is the frequency at which thermal noise becomes more dominant [6].

Lastly, due to the capacitive nature of the MOS structure and the excitement of channel charges, the changing channel potential couples into the gate results in another form of noise called gate noise. This effect becomes especially effective at radio frequencies and hence becomes a dominant reason for noise in LNA applications [12].

As a result of these different noise sources that arise from the CMOS technology, LNA designs in CMOS must be optimized to add as little noise as possible since they already start at a higher minimum noise factor when compared to designs in other technologies.

3.2 Common LNA Topologies in CMOS

When designing an LNA, several conflicting goals must be met at once. Providing high gain with good linearity while keeping the noise figure to a minimum and providing a stable 50Ω input and output impedance are the main goals of the design. Four well-known topologies have been introduced and worked on in the literature: common-source with resistive termination, common-gate, common-source with inductive degeneration, and cascode. Each topology will be explained briefly in this section. In literature, the differential forms of these designs can also be found. However, transforming a single-ended signal into a differential signal will require a balun transformer, directly introducing noise to the system [13]. Due to the difficulty of finding a low-loss balun transformer, especially at the UHF range, the single-ended versions are mostly preferred [14].

3.2.1 Common-Source with Resistive Termination LNA

A common-source amplifier is a suitable voltage and transconductance amplifier due to its high voltage gain and high input resistance [15]. This topology shown in Fig. 3.2 was used as an LNA by adding resistor R_1 to the input port to provide a 50Ω input impedance[16]. It is known that due to the additional thermal noise of the resistor itself, the amplifier's noise figure degrades significantly. Therefore, this is not a topology fit for a sub-1dB noise figure design.

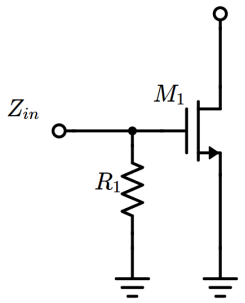


Figure 3.2: Common-source amplifier with resistive termination

3.2.2 Common-Gate LNA

In a common-gate amplifier, the input signal is applied to the source of M_1 while the gate is kept at ground potential. The resistance looking into the source terminal is $\frac{1}{g_m}$; therefore, with a correct selection of device size and bias current, the desired input impedance of 50Ω can be achieved. Due to the presence of the channel in the signal path, which can be considered a noisy resistance, like R_1 in the previous design, this again will face noise figure degradation [1]. An advantage of this design is that it is more suitable for wide-band applications due to its low and stable input impedance, unlike the previous common-source design. However, due to its high noise figure, it is again not a good design for a sub-1dB NF goal [17].

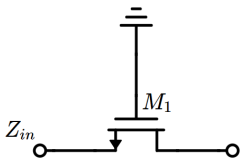


Figure 3.3: Common-gate amplifier

3.2.3 Common-Source with Inductive Degeneration LNA

The common-source with inductive degeneration design shown in Fig. 3.4 uses an inductor L_s connected to the source of transistor M_1 to shift the real term of the input impedance when looking in from the gate of the transistor. With this approach, tuning becomes necessary for impedance matching, hence the design becomes fit for a narrow-band approach [13].

The gate structure of a MOSFET is known to be a parallel plate capacitor, therefore it is difficult to imagine how a real impedance can arise from this structure. The real part of the input impedance arises due to the changing potential of the bottom plate of the gate capacitor. This potential changes along the channel depending on the signal applied at the gate, and due to the finite velocity of

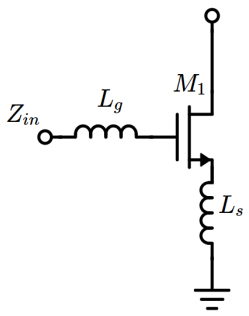


Figure 3.4: Common-source with inductive degeneration amplifier

carriers in the channel the potential of the bottom plate lags behind the current. This lag results in a resistive component in the input impedance [1]. A similar behaviour is also observed in vacuum tubes, where this relationship was first observed [18].

Elongating the transistor to enhance this effect even more can be an option to create a larger input impedance at the gate, however this would degrade the noise performance significantly due to the longer gate length which is not ideal for an LNA. Instead, an inductor which also displays a lag between its current and voltage can be implemented at the source of the transistor. This inductor can be seen as L_s in Fig. 3.4. To shift the input impedance to a purely resistive value in order to achieve input matching and maximum power transfer, another inductor L_g is added to the gate of the transistor [19].

In [20] the input impedance of Fig. 3.2 Z_{in} has been derived as:

$$Z_{in} = \frac{1}{j\omega C_{gs1}} + \frac{g_{m1}}{C_{gs1} + C_{gd1}} L_S + j\omega(L_g + L_s) \tag{3.3}$$

Where:

$$\text{Re}\{Z_{in}\} = \frac{g_{m1}}{C_{gs1} + C_{gd1}} L_S \tag{3.4}$$

and

$$\text{Im}\{Z_{in}\} = \omega(L_g + L_s) - \frac{1}{\omega(C_{gs1} + C_{gd1})} \tag{3.5}$$

In [20], the following relations were also derived:

$$\omega_t = \frac{g_{m1}}{C_{gs1} + C_{gd1}} \tag{3.6}$$

$$f_t = \frac{g_{m1}}{2\pi(C_{gs1} + C_{gd1})} \tag{3.7}$$

From 3.7, it can be said that the cutoff frequency f_t is directly proportional to the transconductance g_{m1}.Therefore, for a design with high transistor transconductance and cutoff frequency, L_s needs to be a small value to satisfy the condition [21]:

$$Z_{in} = w_t L_s = 50\Omega \tag{3.8}$$

The value for L_g can also be derived since at resonance:

$$L_g + L_s = \frac{1}{\omega^2(C_{gs1} + C_{gd1})} \tag{3.9}$$

Unlike the previously discussed topologies, the inductively degenerated CS topology does not place a highly resistive path across the signal path, therefore it offers more promising noise factor results. In [13], a detailed analysis of the MOS noise model for this topology is discussed. An extended model including the effects of gate noise is given in detail and shown in Fig. 3.10.

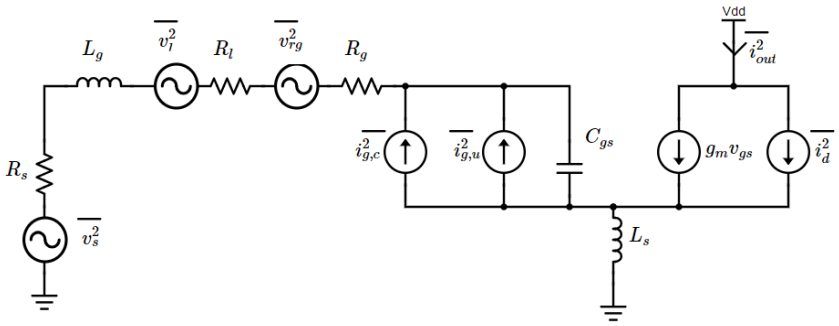


Figure 3.5: Small-signal LNA noise model

In the analysis, total gate noise is divided into two parts: $\overline{i_{gc}^2}$ representing gate noise that is correlated with the drain noise and $\overline{i_{gu}^2}$ representing the the part not correlated with the drain noise. From this model, the noise factor value is derived as:

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}(\frac{\omega_0}{\omega_T}) \tag{3.10}$$

in which γ is a bias-dependent factor and is dependent on channel length. R_g represents the distributed gate resistance and α is the ratio of the transconductance

and zero-bias drain conductance. α is always less than 1 and defined as:

$$\alpha = \frac{g_m}{g_{d0}} \tag{3.11}$$

χ represent constant that are proportional to Q_L and Q_L^2. Q_L is defined as:

$$Q_L = \frac{\omega_o(L_s + L_g)}{R_s} = \frac{1}{w_0 R_s C_{gs}} \tag{3.12}$$

Some important conclusions can be made from these results.

- A minimum F and noise figure exists for a specific Q_L or in other words matching network
- The last term of Eqn. 3.10 represents the gate noise correlated noise, therefore since that establishes a lower bound on the noise performance it should be minimized so the transistor should be kept as small as possible

These considerations should be kept in mind during the design process.

3.2.4 Cascode LNA

A common-source with inductive degeneration LNA cascoded with a common-gate amplifier is referred to as a cascode LNA in literature. This design improves the gain of the common-source amplifier without adding much additional noise to the system. A cascode structure is chosen rather than an additional stage to limit power consumption [5]. The structure can be seen in Fig. 3.6.

The cascode configuration also plays a significant role in improving the reverse isolation of the LNA by minimizing the Miller capacitance C_{gd1} of M_1 by introducing a lower impedance node at the drain of M_1 with the help of M_2 [22]. By reducing the Miller capacitance part of C_{gd1} at the input, degradation of the input impedance is prevented and the overall stability of the circuit is increased [23]. Due to the stacked structure of the design, ideally, an inductive and capacitive load is placed at the drain of M_2 to satisfy the output matching condition

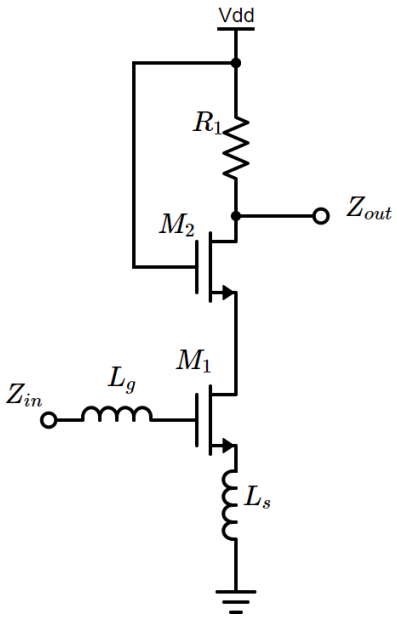


Figure 3.6: Cascode LNA

without consuming a large headroom at the load [24]. However, for low current bias designs a 50Ω resistor can be used instead as the output load.

3.3 Literature Review

Many work has been submitted into the literature about LNA design in the past. They can all be grouped into categories depending on their choice of technology, operating frequencies, and field of use. The amount of published work starts to decrease as we go into the LNAs designed in a classic CMOS technology, and this category specifically tightens once the goal of meeting a sub-1dB NF comes up. Before starting the design of this thesis, a literature review was done on sub-1dB LNAs designed in CMOS and near the operating frequency of 437 MHz, and the following works stood out.

The work published in [23] is an ultralow-power LNA at 404 MHz meant to be used in a cochlear implant device and designed in a $0.18\mu m$ RF/Mixed-Signal CMOS process. Due to its application purpose, it has to be a compact and

low power-consuming design. In the design, the classic cascode amplifier with inductive source degeneration is used as the main topology. The work reports simulation results of a 0.9dB NF, 15.85dB power gain, and an IIP3 of -5.01dBm with a power consumption of 500μ W. This design is very impressive in terms of power consumption and linearity. However, the gain is quite low due to the low drive current being used.

In [25], a few topologies are studied in a 0.13μ m CMOS process for another medical device operating between $402 - 405$ MHz. First, an inductively degenerated cascode structure with a gain of 16.1 dB and a 0.65 dB using 1 mW of power is designed. To reduce power consumption even more, the cascode structure is transformed into a folded cascode, and a current reuse technique is applied. With the help of these two changes, The input amplifier has an increase in power gain due to an increase in transconductance without consuming any extra power. However, the folded structure decreases the IIP3 and the linearity of the system. This design also shows very promising results for an LNA in this frequency band. However, applying it to a more widely available CMOS technology with a minimum channel length of $0.18\mu m$ will most likely deteriorate the results. Therefore, although the designs are good references, they cannot be applied directly to the $0.18\mu m$ CMOS process.

Another work done on an LNA in 435 MHz is shown in [14]. This design shows measured results of a 2.91 dB NF, a 17.5 dB gain, and an IIP3 of -1 dB, all while consuming a total of 12.5 mW from a 2.5 V power supply. The main thing to note about this work is that it is designed on a Silicon On Insulator (SOI) CMOS process. With the help of the oxide, substrate noise is significantly reduced, and the highly resistive SOI substrate suppresses losses from bonding pads, inductors, and other components that can create noise due to their resistance. This design is again based on an inductively degenerated cascode structure. However, it is not applicable to the classic CMOS technology at all.

Lastly, in [26], a 450 MHz LNA is constructed on a $0.13\mu m$ RF/CMOS process. In this design, again an inductively degenerated cascode structure is used and only one inductor is included on-chip. The rest are placed on the external PCB;

however, due to insufficient modeling of the external components, the design has a measured NF of 1.78 dB while the simulated NF is 1.23 dB. Similarly, there is also a huge gap of 8 dB between the measured and simulated power gains. Though this design is still within its performance limits, it highlights the importance of proper modeling of both on and off-chip components by showing how different measurement results can be from the simulated results. Also, since it is designed with a shorter channel length, it is not applicable to the chosen technology within the scope of this thesis.

The works presented above certainly do not reflect all research done on LNAs designed to operate on or near 437 MHz. However, these works are the ones most similar in structure to the work done in this thesis. Therefore, it is important to understand the weaknesses and strengths of each design in order to add to it in the following sections.

Chapter 4

LNA Design Methodologies

In Chapter 3, the available LNA topologies have been introduced. A cascode amplifier is the best choice to meet the design criteria for the LNA to be designed in this thesis. However, more than picking a topology is needed to start a design. The size of the transistor, optimal bias condition, and supply current should also be set. In this section, some methodologies to set these parameters will be discussed before going into the actual design steps.

4.1 Common LNA Design Methodologies in Literature

Various LNA design techniques have been reported in the past [20], all sharing the goal of achieving simultaneous noise and input matching at a given power dissipation. One reported technique, named the classical noise matching (CNM) technique, obtained an NF close to the lowest NF possible for that technology by transforming the input impedance to Z_{opt}, which can be defined as the input impedance of the amplifier for optimum noise performance. However, due to the mismatch between Z_{in}^{*}, which is the desired input impedance for maximum power transfer from the source, and Z_{opt}, the amplifier may experience a gain mismatch.

Its performance may degrade [27].

Another technique, Simultaneous Noise and Impedance Matching (SNIM), was studied in [28]. This technique used the previously described inductive degeneration method to bring Z_{opt} and Z_{in}^{*} to the same point to achieve optimal noise and gain performances. Though this solved the problem, it did not consider any power limitations. The technique worked well for cases of large transistor size, high power consumption, and frequency operation. Still, it caused problems for designs that required lower transistor size and operation frequencies. The problem was the inductance value needed for L_s, the source degeneration inductor, had to be very large, which resulted in the technique being invalid [20].

The Power Constrained Noise Optimization (PCNO) technique is the same as SNIM. However, the power constraint is taken into consideration by using the drain current of the transistors in calculations. In [13], it is shown that with a fixed drain current, the optimum transistor size for minimum NF and input matching is

$$W_{opt} = \frac{1}{3_{ox} R_s Q_{in,opt}} \tag{4.1}$$

where

$$Q_{in,opt} = |c|\sqrt{\frac{5\gamma}{\delta}}[1 + \sqrt{1 + \frac{3}{|c|^2}(1 + \frac{\delta}{5\gamma})}] \tag{4.2}$$

γ and δ are device gate length parameters, and are typically $\frac{2}{3}$ and $\frac{4}{3}$ respectively in long channel devices. Both increase for shorter channels and higher V_{GS} and V_{DS} values. Another parameter used in 4.2 is defined as

$$c = \frac{\overline{i_{ng} \cdot i_{nd}^{*}}}{\sqrt{\overline{i_{ng}^2}} \cdot \sqrt{\overline{i_{nd}^2}}} \tag{4.3}$$

and it is used to show the correlation between the gate-induced noise current and channel noise current. This value can be taken as $j0.395$; due to the capacitive coupling between the noise sources, the value is purely imaginary [1]. It will be helpful to note that these expressions were derived from 3.10, in [13]; therefore, they are all correlated. Although this technique works well for a design with a power constraint, it again requires the amplifier to have large L_s values to reach the minimal noise figure, which is not desired.

The Power Constrained Simultaneous Noise and Input Matching (PCSNIM) technique discussed in [29] resolves these issues by introducing an additional capacitor parallel to C_{gs} of M_1 in 3.6. The study shows that the additional capacitor does not affect the minimum NF or the input impedance of the cascode LNA. It also derives the predicted minimum noise factor value to be

$$F_{min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_t} \sqrt{\gamma\delta(1 - |c|^2)} \tag{4.4}$$

This method relieves the problem of low power-consuming designs and allows flexibility on the value of L_s with the help of the additional capacitor.

4.2 The g_m/I_D Method

As submicron MOSFET technologies evolve, the methods described in the previous section have become less reliable for higher-frequency applications. Additionally, to apply the mentioned techniques for a design, all fabrication parameters should be given to the designer, which is different in most situations. The g_m/I_D method has been used for multiple analog amplifier applications in literature in the past [30]. This method provides a more applicable and quantitative way to obtain the best-performing design for RF applications, especially LNAs. To use this method, the essential characteristics listed below should be derived with a simple DC analysis for the transistor to be used in the amplifier design [31].

- g_m/I_D vs. V_{ov} : Transconductance efficiency versus overdrive voltage
- f_t vs. V_{ov} : Unity current gain frequency versus overdrive voltage
- I_D/ W vs. g_m/I_D : Current density versus transconductance efficiency

With the above characteristics, a designer can select optimum transistor sizing and biasing to achieve the desired minimum NF_{min} value and maximum power gain while staying within the power consumption limit without having to obtain the transistor's fabrication parameters to solve the tedious equations defined in

the previous section. In [13], the general expression for the noise factor of a cascode LNA was defined as

$$F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2 \tag{4.5}$$

where F_{min} is defined as in Eqn. 4.4. Therefore, to obtain the lowest noise figure possible, both parts of Eqn. 4.5 should be minimized. First, the noise coming from the core transistor expressed in 4.4 should be minimized by increasing its cutoff frequency f_t. Second, by making Y_s the source admittance equal to Y_{opt} the optimal source admittance for minimum noise, the noise coming from the rest of the amplifier can be minimized and minimum NF can be achieved [32].

This methodology will be used to start of the design for this thesis.

Chapter 5

LNA Design in CMOS Technology

The main scope of this thesis is to design and optimize a narrow-band LNA operating at 437 MHz and 447 MHz and satisfying a sub-1dB condition using CMOS technology. In this section, the design will be done for a single coil 10.3T system, which means the operation frequency is 437 MHz. The design technology is chosen to be the TSMC 0.18 μm CMOS MS/RF, which is available at the university lab. The process development kit (PDK) offers promising devices optimized for RF designs as well as six metal options with a thicker top metal to be used in inductor designs [33].

5.1 Transistor Sizing and Bias Selection

The methodologies described in Chapter 4 can be used to find the optimal transistor size and bias condition. Within them, the g_m/I_D explained in Section 4.2 will be used because of its accuracy and ease when compared to the others.

To start the design, a 2V RF NMOS device named "rfnmos2v" was chosen

from the TSMC18 library. This is one of the devices optimized by the foundry for RF applications. Compared to their previous versions, this nMOS has a much higher f_t and is coupled to a deep n-well, which aids in noise reduction [33].

To obtain the plots needed for the g_m/I_D method, a DC sweep analysis is done for the transistor as shown in Fig. 5.1. The length of the transistor is set at the lowest possible length of 0.18μm to minimize the noise coming from the channel and optimize speed, and the bulk is connected to ground [34]. The drain voltage is set to 0.9V, which will be the actual voltage once the cascode stage comes, while the gate voltage is swept from 0V to 1.8V.

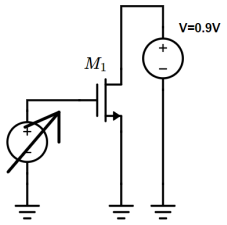


Figure 5.1: DC Sweep Setup

The value of the cutoff frequency was calculated as

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{gb})} \tag{5.1}$$

to derive the following plots [23]. From Fig. 5.2, it is clear that as V_{ov} increases, g_m/I_D decreases but f_t increases. Therefore, when the transistor is in strong inversion, g_m/I_D is low while f_t is high and inversely when the transistor is in weak inversion, the g_m/I_D is high while f_t is low. Since the gain is directly dependent on g_m/I_D, the gain will be high in weak inversion, whereas the NF will worsen since f_t is low in this situation. This is the gain and NF trade-off that must be made. Using the plot in 5.3, the W of the transistor can be found for a specific V_{ov} value.

Table 5.1 summarizes the $\frac{g_m}{i_d}$, f_t, and $\frac{I_d}{W}$ values for three different bias points. With the design requirement of $I_d = 7$ mA, the values of W for the different bias points can be seen in Table 5.2.

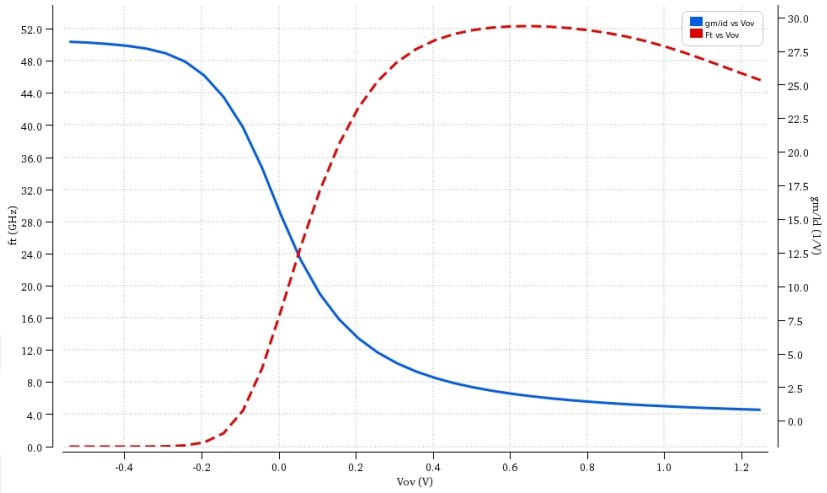


Figure 5.2: f_t and $\frac{g_m}{i_d}$ vs. V_{ov}

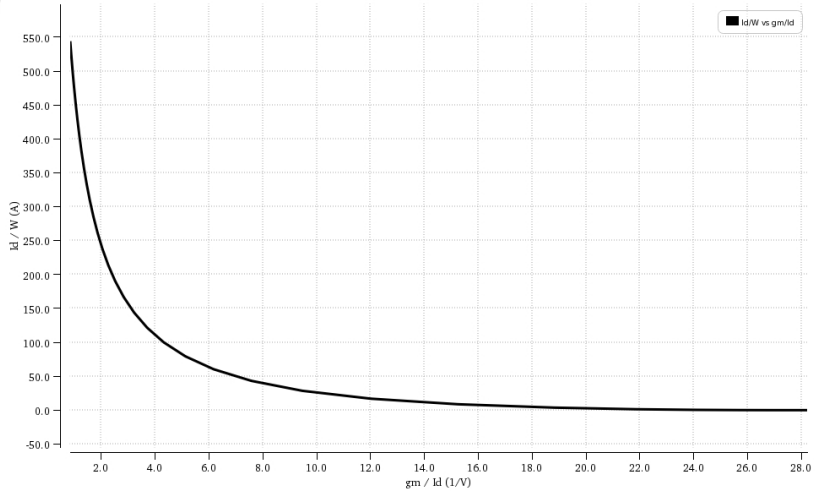


Figure 5.3: $\frac{I_d}{W}$ vs. V_{ov}

Table 5.1: $\frac{g_m}{i_d}$, f_t, $\frac{I_d}{W}$ values for at various V_{gs} and V_{ov} points

$\mathrm{V}_{gs}(V)$	$\mathrm{V}_{ov}(V)$	$\frac{g_m}{i_d}(1/\mathrm{V})$	$f_t(\mathrm{GHz})$	$\frac{I_d}{W}(\mathrm{A})$
0.60	0.056	11.990	24.89	17.00
0.65	0.106	9.452	31.93	28.65
0.70	0.156	7.562	37.73	43.36
0.75	0.206	6.159	42.22	60.64

Table 5.2: W(μm) values for at various V_{gs} and V_{ov} points

$V_{gs}(V)$	$V_{ov}(V)$	Wμm
0.60	0.056	411
0.65	0.106	245
0.70	0.156	160
0.75	0.206	115

From Table 5.2, it is seen that as the overdrive voltage V_{ov} decreases, the W required to support the current increases. As discussed in Section 3.1, large transistors suffer degradation in noise performance due to their large gate resistance and parasitic capacitance [35]. Therefore, it is not ideal to drive the transistor at low V_{ov} values due to the increasing size of the transistor and the decrease in f_t. On the other hand, as V_{ov} increases, the noise performance but the $\frac{g_m}{i_d}$ starts to take a fall. Additionally, from Eqn. 3.8, as the size of the transistor decreases, the L_s value needed for good input matching increases. Having a large inductance value within a chip is not ideal. Therefore, it is important to not bias the transistor at a large V_{ov} as well. Since noise performance is extremely critical for the design within this thesis, biasing the transistor at V_{gs} = 700 mV with a $\frac{W}{L} = \frac{160}{0.18}$ ratio is a good choice. Although a slight gain reduction will be seen, the noise performance will be enhanced to meet the sub-1dB criteria.

5.2 Simultaneous Impedance and Noise Matching

5.2.1 Gate and Source Inductance only Matching Case

Once the device sizes are set, an input and noise matching is designed for the amplifier. Before inserting the inductor matching circuit, the schematic in Fig. 5.4 measures the original input impedance. A voltage bias of 700mV is given to provide the needed threshold drive to the transistor. Both transistors are set to the same width; however, this will be optimized in the future section.

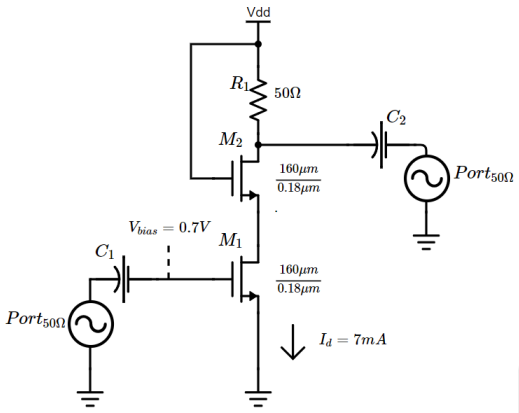


Figure 5.4: LNA schematic without any matching circuit

Without any matching circuit, the input impedance of the LNA looking into the gate of M_1 is measured as $Z_{in} = 23.74 - j1247.1\Omega$. Due to the heavily capacitive nature of the transistor's gate connection, the input impedance reflects a negative imaginary impedance. The real impedance is measured as 23.74Ω, which needs to be matched to the source impedance of 50Ω for good gain and noise performance. The Equations 3.8 and 3.9 are a good place to start to find the approximate L_s and L_g values for the matching circuit.For the chosen design width, $L_s = 300$ pH and $L_g = 460$ nH are found to provide perfect input matching to the circuit. They are placed as shown in Fig. 5.5.

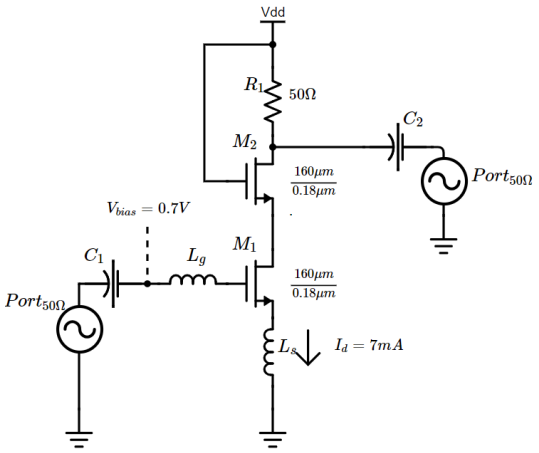


Figure 5.5: LNA schematic with source degeneration and gate inductance

After the addition of L_s to the source of M_1, the input impedance shifts as

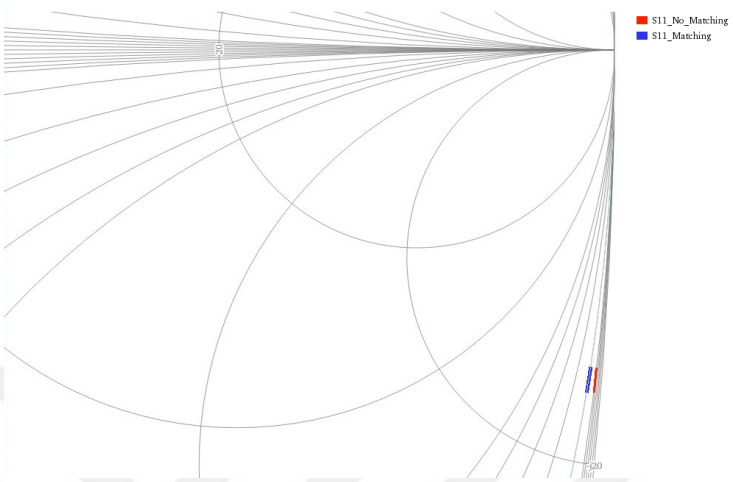


Figure 5.6: Shift in S11 due to L_s

shown in Fig. 5.6. The real part of the impedance moves up to 49.9Ω, much closer to the desired impedance. Since the imaginary input impedance still remains, a series L_g is added to cancel the seen capacitive impedance. The input impedance after the addition of L_g is shown in Fig. 5.7. Due to the frequency-dependent nature of the inductor, the input impedance changes with frequency However, with the chosen L_g value, the impedance at 437 MHz falls directly on the Z_s^* point on the smith chart, which is what is needed for perfect input matching and maximum power transfer. In Figures 5.7, 5.8, and 5.9 the points labeled Z_s and Z_s^* represent the source impedance and its complex conjugate respectively. The source impedance is not exactly 50Ω due to the series bypass capacitor added after it, which is needed for biasing purposes [36].

In Fig. 5.8, the available gain circles of the design are seen. The red circles show the circles that the source impedance should fall on to obtain the desired gain value before any matching is done, and the blue curves show the circles once L_g and L_s are added. The inner solid line circles represent the highest gain of 28 dB for both cases, and the gain value drops as the circles widen into the dashed lines. It can be understood from the figure that before matching, no gain was possible because the source impedance Z_s lied outside all of the red circles. After the matching, however, Z_s lies inside the gain circle representing the highest gain. This shows that the matching was successful in providing maximum power

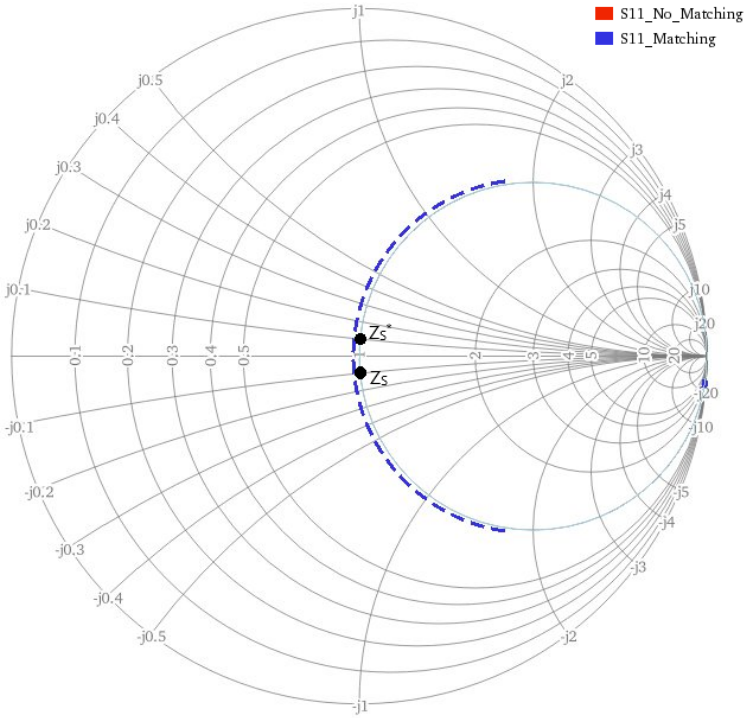


Figure 5.7: Shift in S11 due to L_g

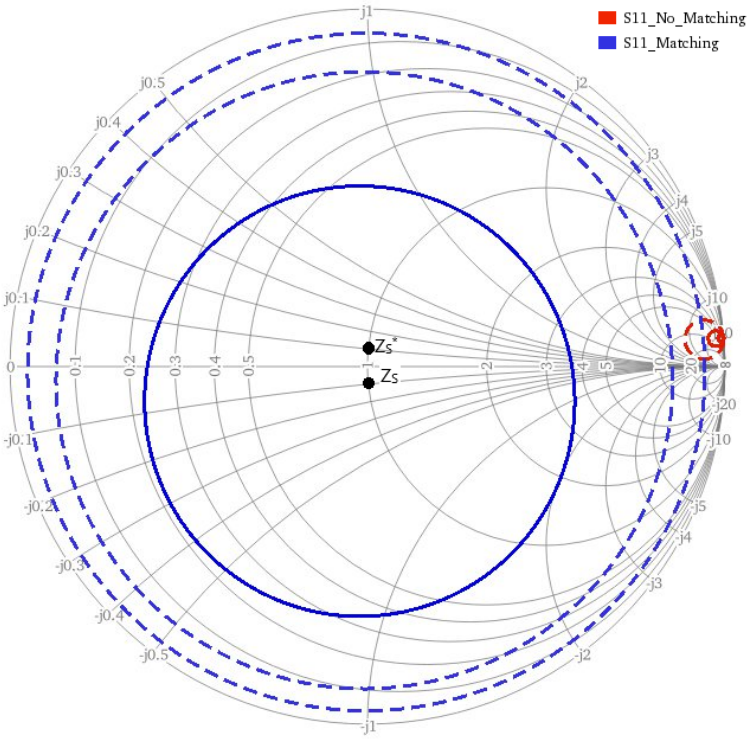


Figure 5.8: Available Gain Circles before and after matching circuit

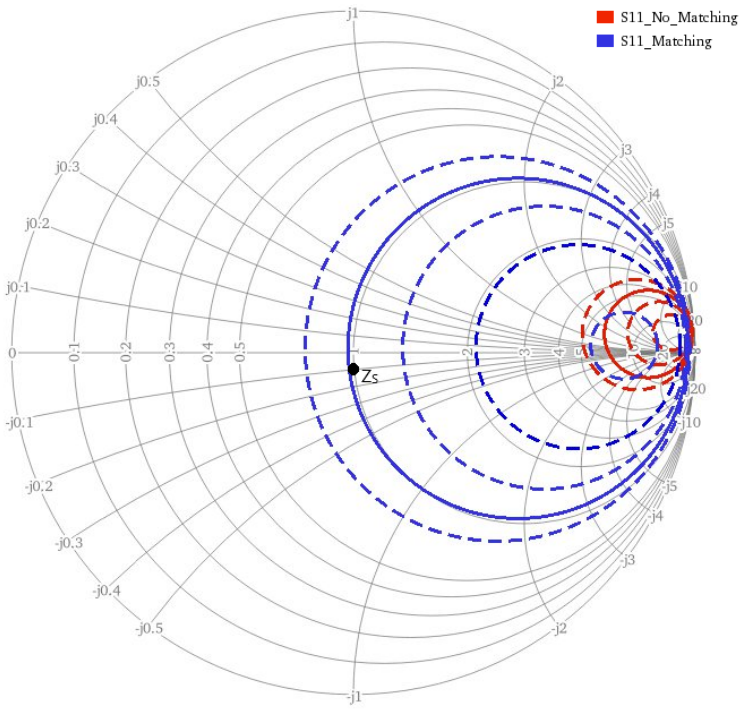


Figure 5.9: Noise Circles before and after matching circuit

transfer in the system.

It is, however, not enough to guarantee maximum power transfer if the NF of the LNA is above the required value. The design requirement for this LNA is the NF to be below 0.5 dB, so this should be satisfied with the input matching circuit as well. Figure 5.9 shows the noise circles of the circuit before and after the matching circuit is implemented. The red circles show the circles that the source impedance should fall on to obtain the desired NF value before any matching is done, and the blue curves show the circles once L_g and L_s are added. The solid lines represent a NF value of 0.8 dB, and the NF value decreases as the circles shrink and move towards the right of the smith chart. Although the matching network did shift the NCs closer to the source impedance, Z_s lies on the NF curve corresponding to 0.8 dB, which is above the goal. For this reason, even though this matching network with just two inductors can function as an LNA, it is not enough to meet the design goals set in this thesis.

To optimize the noise performance of the LNA, a π matching network can be

used at the input. With the additional parallel capacitors, the noise circles for minimum noise levels can be pulled to impedances closer to the source impedance [23]. However, the value for L_s will need to increase in this case, therefore it is important to decide on the possible inductor values beforehand.

5.2.2 TSMC Monolithic Inductors

In integrated circuits, having on-chip inductors come with advantages and disadvantages. Placing the inductor into the chip can aid in lowering the external area consumption and can create a more controlled inductance values which is important if the value of the inductor is critical for the performance of the design. Monolithic inductors are used in chips, however they usually provide lower inductance (L) and lower quality factor (Q) values compared to discrete inductors [37]. TSMC provides silicon-proved inductor designs in its RF/CMOS PDK, which is very helpful for an LNA application since the L and Q values of the inductor are known beforehand [33]. Spiral inductors are offered within the PDK, which are also the most common type of monolithic inductors used in ICs. In this type of inductor the metal is drawn in spirals, therefore mutual coupling aids in increasing the inductance value and performance of the design[37].

Before going into the inductor options, it is important to understand what the Q factor is, and why it is important in an RF design. Even though an inductance is known to have a pure positive imaginary impedance, all inductors have a series resistor within them due to the metal in their designs. The Q factor is used to measure how well an inductor stores magnetic energy compared to how much energy is dissipated due to the internal resistance [6]. The values for Q and R of an inductor with an impedance of Z can be derived as

$$Q = \frac{Im(Z)}{Re(Z)} = \frac{\omega L}{R} \tag{5.2}$$

$$R = Re(Z) = \frac{\omega L}{Q} \tag{5.3}$$

From Eqn. 5.3, it can be seen that an inductor with a high Q value is needed in order to minimize the series resistance and the parasitics coming with it. In the

case of an LNA, it is crucial for the inductor used for source degeneration and at the input to be low in resistance, therefore high in terms of the Q factor.

Using the TSMC's Inductor Finder tool, many different inductors with various L and Q values, sizes, working frquencies, and self-resonant frequencies (SRF) can be found. The SRF is the frequency at which the parasitic capacitances inside the inductor start to resonate and the inductor acts like an open circuit displaying extremely high resistance [6]. It is important to pick an inductor with an SRF greater than the operating frequency to avoid any issues.

Although the frequency of the design for this thesis is considered an RF signal, it is on the lower end of the spectrum. Due to the lower operation frequency, the obtainable Q factors are limited. In order to obtain an inductor with a high Q, the inductor has to be really high in value and therefore large in size [38]. Additionally, increasing the L value does not directly guarantee a better performance since the internal resistance is dependent not just on the Q factor but also the L value itself.

After a series of trials with the TSMC tool, the inductors in Table 5.3 were found to be suitable for the design. L values higher than 1 nH resulted in Q factors less than 2 at 437 MHz, therefore they are not suitable for the design.

Table 5.3: Inductor Designs offered in TSMC PDK

	L(nH)	Q	$R(\Omega)$	Area(μm^2)	f(GHz)
1	0.76	2.67	0.78	245x269	3
2	0.743	2.37	0.86	230x240	3.5
3	1.08	2.63	1.12	238x249	2.5
4	1.04	2.58	1.1	220x230	3

In the following section, the design will continue with the inductor values form Table 5.3.

5.2.3 π-Network Matching Design

In Section 5.2.1, an LNA design at 437 MHz with promising noise and gain results was derived. However, the NF was capped at 0.8 dB. To improve the noise performance, a π-network matching is needed to allow for a more narrow-band design and hence improve the NF [39]. The new circuit design is shown in Figure 5.10.

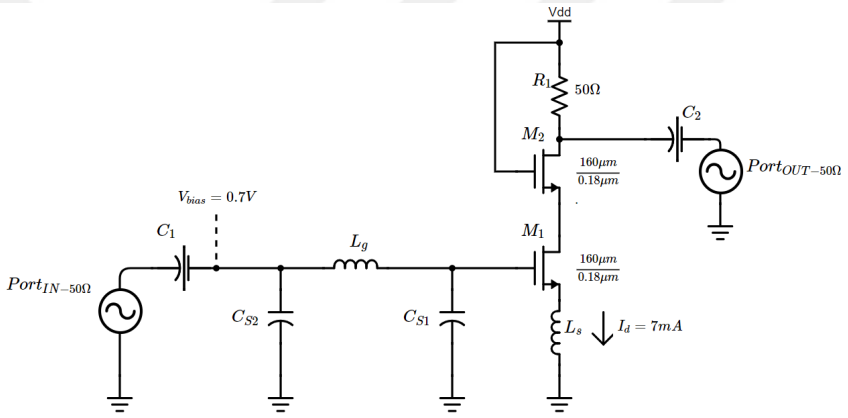


Figure 5.10: LNA schematic with π-network matching

The 3rd inductor from Table 5.3 is chosen as L_s since it has a good Q value and is smaller in size than the 1st option. Values for each parameter can be seen in Table 5.4.

Table 5.4: π-network matching component values

$\frac{W}{L}$	L_s(nH)	C_{s1}(pF)	L_g(nH)	C_{s2}(pF)
$\frac{160}{0.18}$	1	1	108	17

In 5.11, the shift of the input impedance through the π-network can be seen. At the 1st step due to the higher L_s value, the real impedance at the gate of M_1 is shifted to 138Ω. At the 2nd step, due to the parallel capacitor C_{s1}, the real part of the impedance drops to 7Ω and the imaginary part grows. After the series gate inductance L_g at the 3rd step, the real impedance stays constant, but the imaginary part becomes positive. Lastly, after the second parallel capacitor C_{s2}, the real part gets very close to the desired 50Ω impedance. This can be seen at

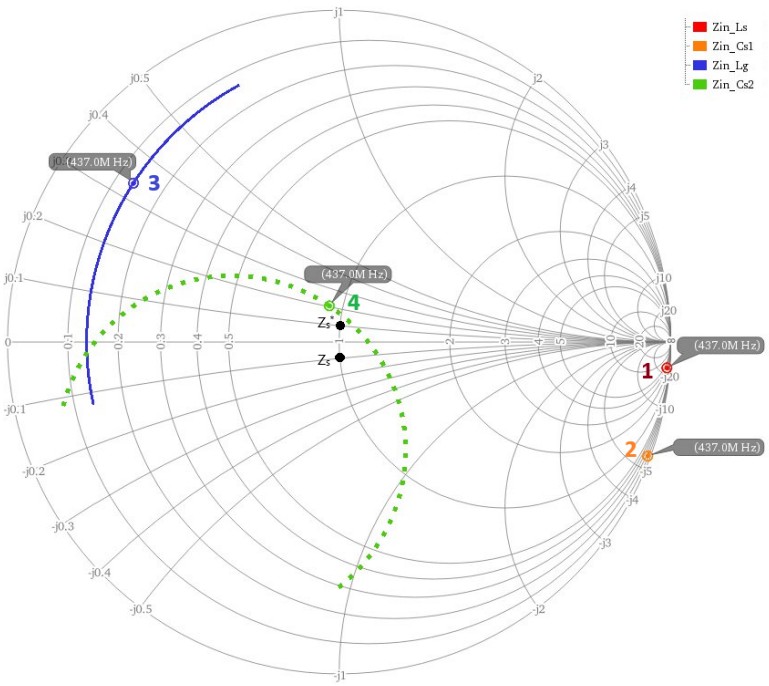


Figure 5.11: Shift in S11 through the π-network

the 4^{th} step. Now, the input impedance is very close to Z_s^*, which guarantees input matching and an almost perfect power transfer.

Like the previous matching design, having a good input match is not a guarantee of having a low NF, so the noise circles need to be reviewed as well. This can be seen in Fig. 5.12. The solid green line closest to our source impedance represents the points that the source impedance Z_s must fall in to obtain a NF=0.35 dB. This is a significant improvement from the previous matching network, and it shows that a carefully designed π-network is indeed more effective for extra low noise and narrow-band designs. The GACs for π-network matching is shown in Fig. 5.13. The solid blue line closes to Z_s represents the points that the source impedance Z_s must fall in to obtain a gain of S_{21}=25 dB. It is important to note that this is lower than the gain of the previous matching network, this is due to the slight mismatch between the input impedance following the π-network and Z_s^*.

In Fig. 5.14, the NF of the circuit and the NF_{min} are plotted. Although the

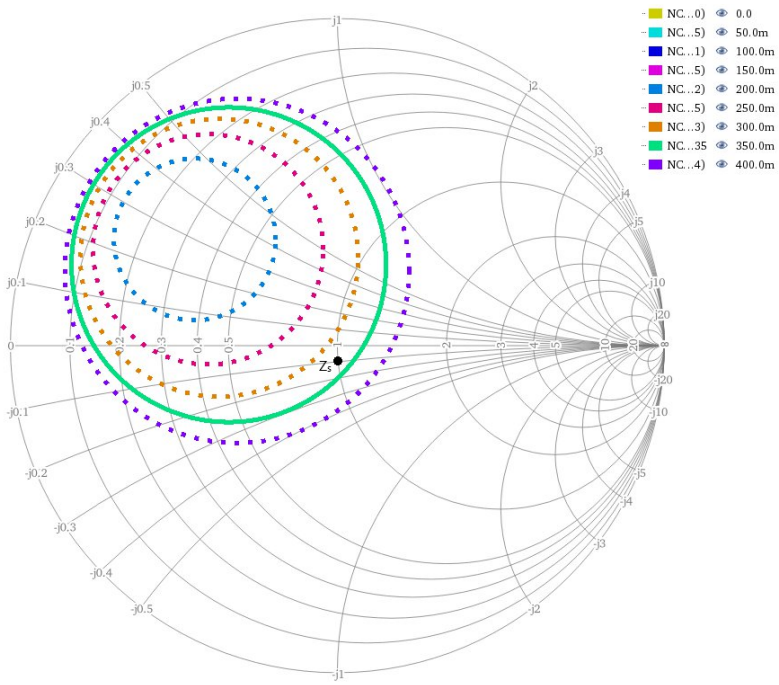


Figure 5.12: Noise Circles with π-network matching

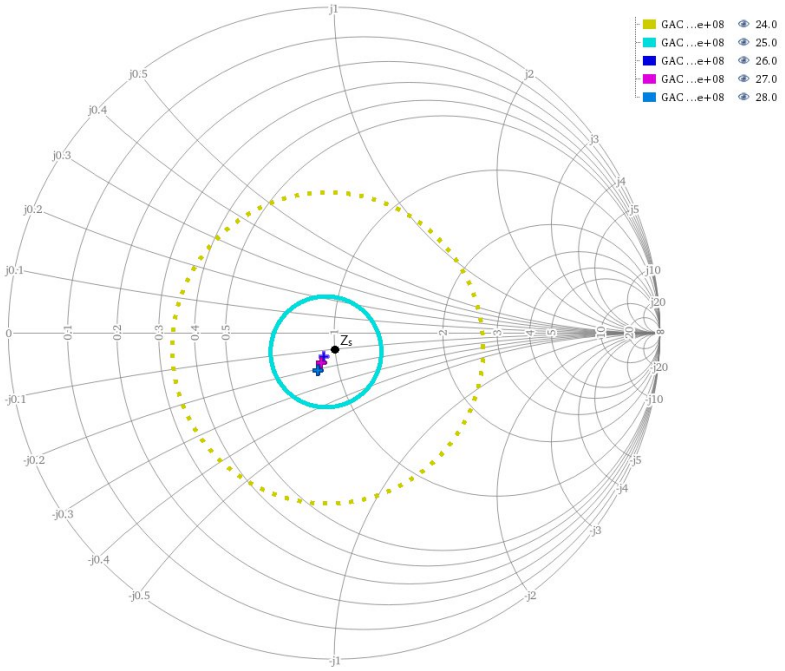


Figure 5.13: Available Circles with π-network matching

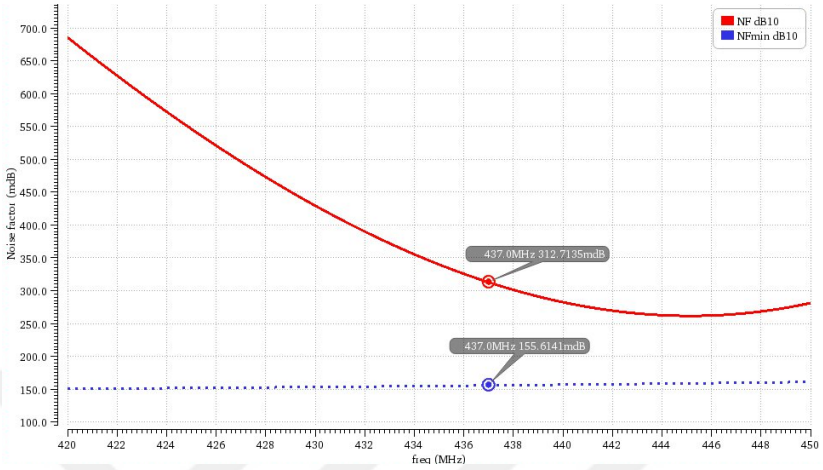


Figure 5.14: NF of LNA with π-network matching

NF is very low, there is still some room for improvement. In order to decrease the NF even more, a lower value of L_s with a better Q factor can be used. Ideally decreasing the value of L_s would require the W of M_1 and hence the power consumtion and area to increase, however, by placing a capacitor parallel to C_{gs1}, this can be avoided [24]. Additionally, it is shown in [40] that the addition of this capacitor also aids in decreasing the NF by decreasing the effect of the gate resistance of M_1 by acting as an autotransformer for the current. To decrease the NF, the degeneration inductor L_s is now the 2$^{\text{nd}}$ inductor in Table 5.3. With a lower inductance and same Q factor, it will bring less parasitic resistance to the source of M_1. The placement of the additional capacitor can be seen in Fig. 5.15.

After these changes, the π-network matching components are tuned to achieve the desired matching. The updates values can be seen in Table 5.5.

Table 5.5: π-network matching component values after additional C_{par}

$\frac{W}{L}$	L_s(nH)	C_{s1}(pF)	L_g(nH)	C_{s2}(pF)	C_{par}(pF)
$\frac{160}{0.18}$	0.743	1	105	16	70

The NF value after the additional capacitor can be seen in Fig. 5.16. It can be seen that this has decreased the NF by 60mdB, making it much closer to the technology limited NF_{min} value.

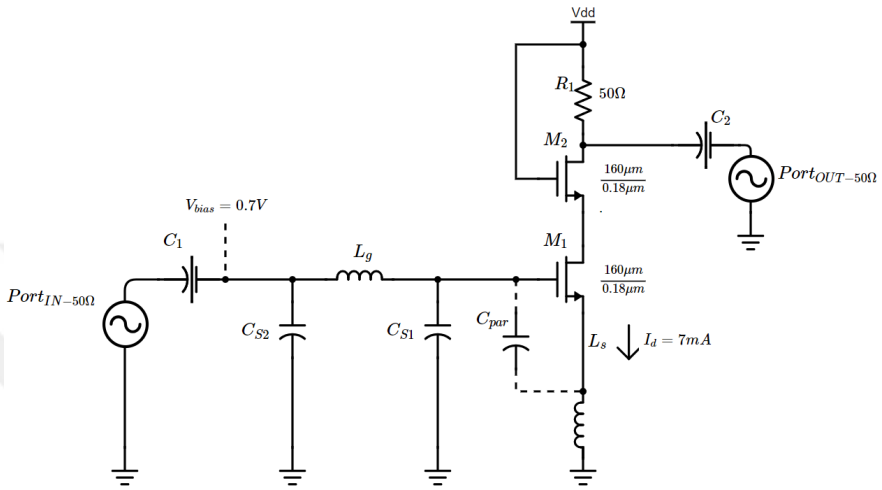


Figure 5.15: LNA schematic with π-network matching and additional capacitor for NF improvement

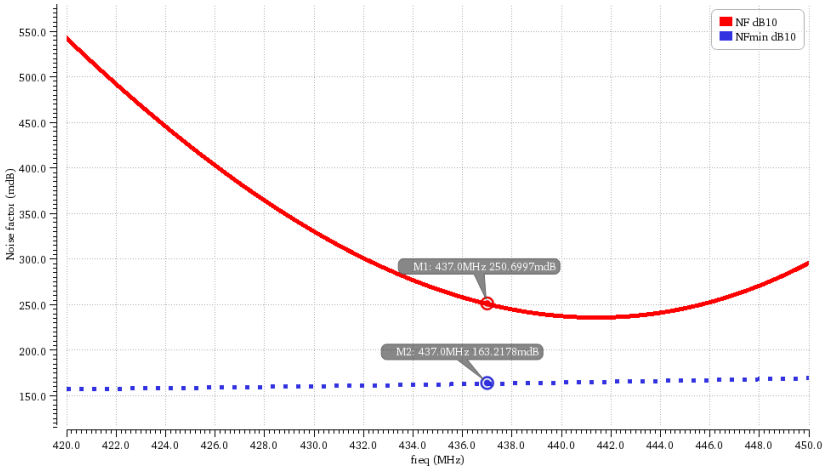


Figure 5.16: NF of LNA with π-network matching and design enhancement

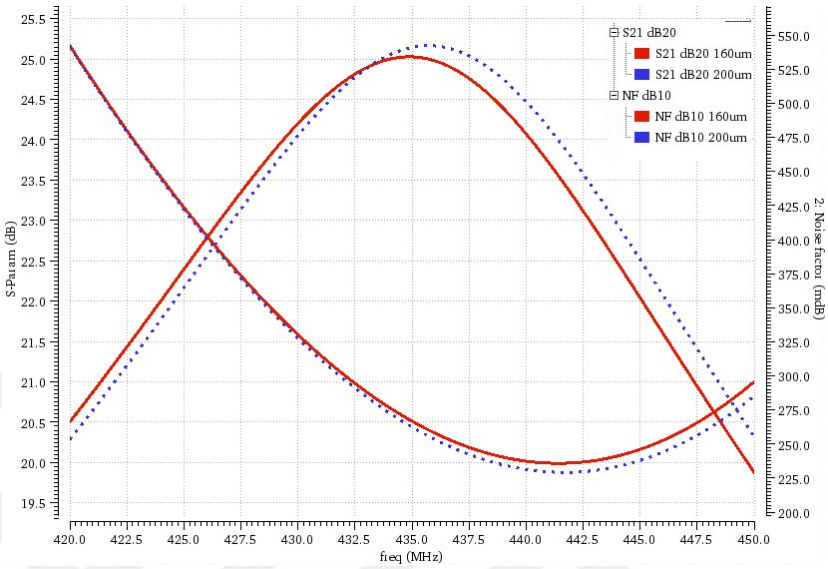


Figure 5.17: S_{21} and NF for two different W_2

5.3 Cascode Common-Gate Stage Design

In Fig. 5.15, the CG cascode stage of M_2 is used mainly to increase the reverse isolation of the circuit and decrease the Miller Capacitor at the input of the circuit due to C_{gs1} [1]. In literature, some studies have kept the sizes of transistors M_1 and M_2 the same by arguing that the cascpde stage will not have an impact on the overall noise figure if the input stage is optimized [14] [25]. However, some studies argue that the small difference between the overall NF and NF_{min} may be due to the cascode stage [34] [23].

In order to get the lowest possible NF value possible, an optimization simulation is performed by sweeping the W of M_2 from 120μm to 220μm. Since the width of the cascode stage does not have a major effect on the input matching, this simulation can be done successfully without having to change the input matching network between each run.

Based on the simulation results in Fig. 5.17, setting $W_2 = 200\mu m$ decreased the NF and increased the gain S_{21} at the operating frequency 437MHz. Based on these results, the new $\frac{W}{L} = \frac{200}{0.18}$ for M_2.

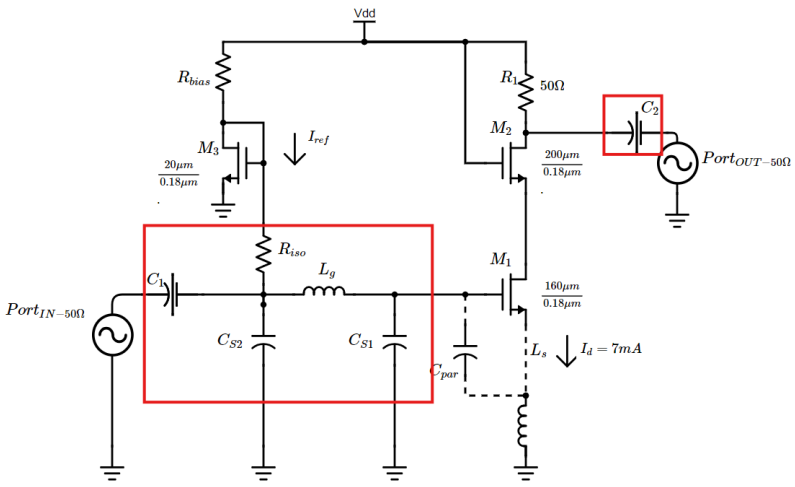


Figure 5.18: Full LNA schematic with biasing

5.4 Bias Structure Design

The LNA is biased with the help of a current mirror. In the full circuit schematic shown in Fig. 5.18, a diode connected NMOS transistor M_1 is biased using R_{bias}. With a size ratio of $\frac{1}{8}$, the bias structure sets the current of the amplifier to eight times its bias current. The constant current biasing will help keep operation stability in case of process variations, which is important for the LNA [23].

The bias network must be isolated from the signal path with a high resistance to prevent the RF signal from coupling to the gate of M_3, R_{iso} is responsible for this [23]. The placement of R_{iso} is very critical for the operation of the LNA. This placement was studied in [41], and it was concluded that placing the isolation resistor before the matching network and closer to the source was less hurtful to the NF of the overall system [41]. With this insight, the R_{iso} is placed directly after the bypass capacitor C_1. The value of the isolation resistance is also very critical for proper operation, and it should be large enough so that its equivalent noise current is small enough to be ignored. For the scope of the design in 5.18, a value greater than $50K\Omega$ is enough to satisfy the values previosly measured in 5.16. However, since it will be placed off-chip, placing a higher value such as $100K\Omega$ will be smarter [1].

With the addition of the bias circuit, the finalized values for all components in Fig. 5.18 are in Tables 5.6 and 5.7.

Table 5.6: All component parameters for final LNA schematic

$\frac{W_1}{L_1}$	$\frac{W_2}{L_2}$	L_s(nH)	C_{s1}(pF)	L_g(nH)	C_{s2}(pF)	C_{par}(pF)	$R_1(\Omega)$
$\frac{160}{0.18}$	$\frac{200}{0.18}$	0.743	1	105	16	70	50

Table 5.7: Biasing component parameters for final LNA schematic

$\frac{W_1}{L_1}$	$R_{bias}(K\Omega)$	$R_{iso}(K\Omega)$
$\frac{20}{0.18}$	1.38	100

5.5 Layout Design

In the proposed LNA, the π-network and isolation resistance R_{iso} are designed to be off-chip. This is beneficial in two ways, firstly chip area is saved by placing big components outside of the chip, and secondly it allows for correction once the chip is fabricated. Since noise and gain matching are heavily dependent on the π-network, having the freedom to play with the network can be used to adopt the design to fabrication and implementation errors. By placing the big components outside, the chip area can be minimized. The majority of the area will be consumed by the on-chip L_s inductor, which was also optimized in Section 5.2.2. Since L_s is a small value, it can be implemented with just a bond wire, however this can create ambiguity since the inductance of a bond wire cannot be known exactly. Placing an on-chip degeneration inductor and then optimizing the design with the bond wire will create a more guarantee design.

In an LNA layout, the first part that should be considered is the optimization of the input transistor so that no additional noise arises from its parasitics. The most critical step in this optimization is to ensure that the transistors which are laid out in a multifinger structure have contacts on both sides of their poly gates. By doing this, the noise asiring from the channel resistance will be minimized [22]. The double contact implementation for this design is shown in Fig. 5.19. Another

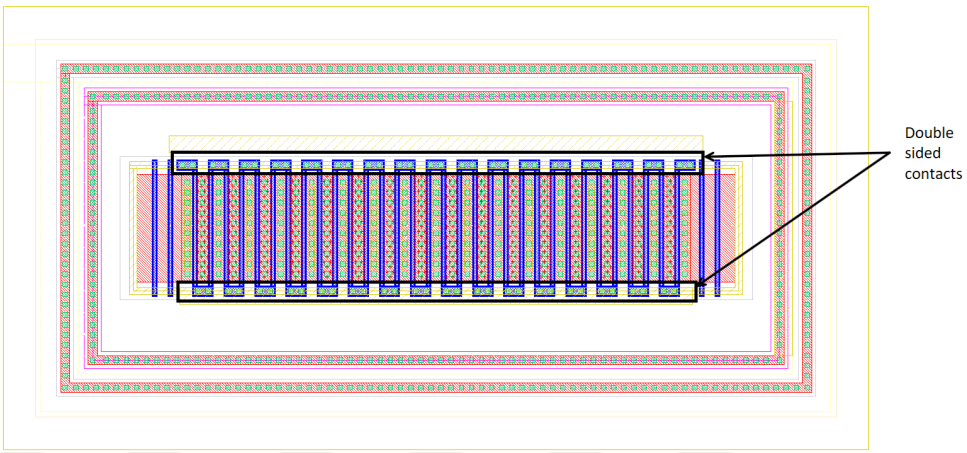


Figure 5.19: NMOS Layout Properties

important optimization to be made is isolation from the substrate. TSMC offers RF devices which come with their own N-wells which isolate the device from the noisy substrate. With these devices, very low NFs become achievable.

In a high frequency layout, the metal connections on the signal path should also be optimized to minimize parasitics as much as possible. At high frequencies, the series inductor and resisotr and parallel capacitor parasitics of a metal transmission line become more dominant, and this can be especially detrimental to the performance of an LNA if the parasitic land on the signal path. To minimize parasitics as much as possible, the input and output signals are drawn with the thickest top metal available $M6$, and the line widths are drawn to meet the width limited by the I/O pads. A ground shield is also constructed with the bottom metal $M1$, to provide shielding for the $M6$ carrying the RF signals to avoid any substrate losses [42]. The fully constructed layout of the LNA can be seen in Fig. 5.20.

To connect to the chip, I/O pads and bond pad connections also need to be added to the layout. First an I/O ring which encompasses individual components used to connect analog I/O, power, and ground signals is created around the core of the chip. Fillers are used within the ring to fill in the gaps between the signal paths. Following the I/O ring, bond pads are added for the I/O RF signals, supply connections which are V_{DD} and V_{bias} in this case, and ground connection.

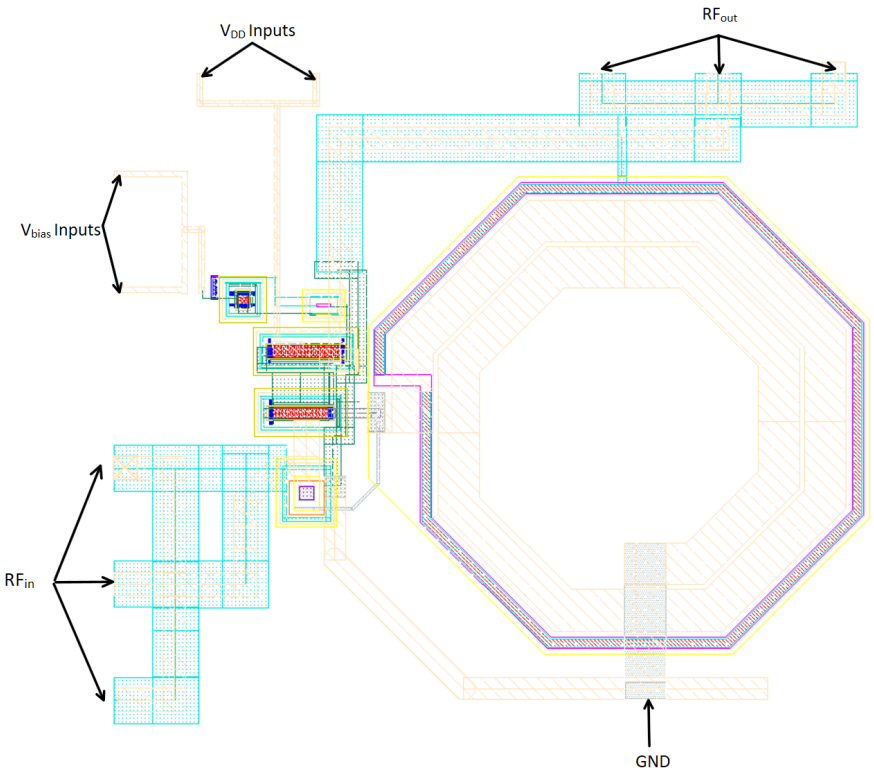


Figure 5.20: Layout of LNA

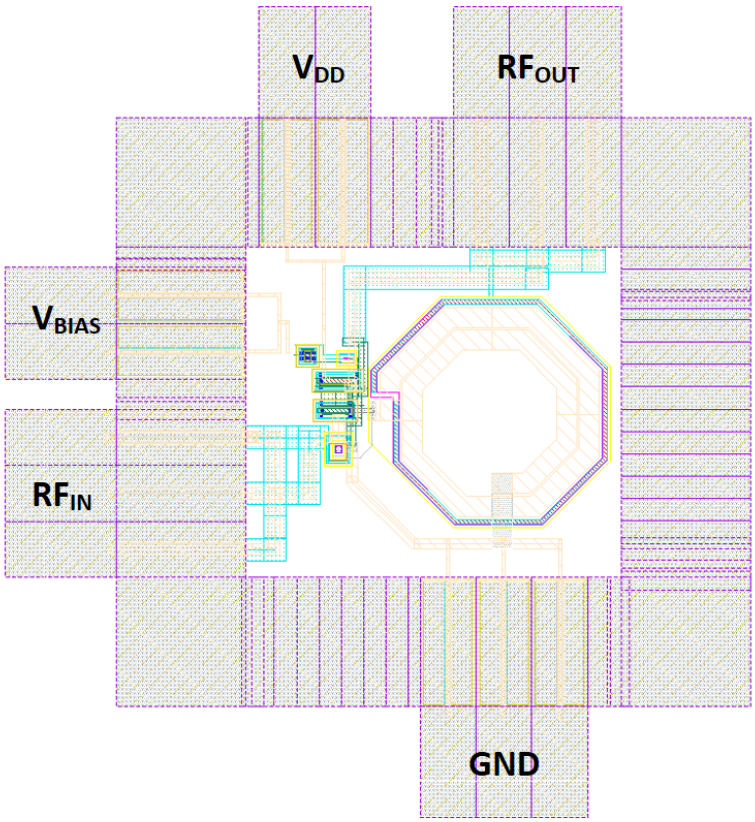


Figure 5.21: Complete LNA layout with pad details

As stated previously, although the voltage to bias the main transistor M_1 is generated inside of the chip, it has to be connected to the input of the matching network which is off-chip. Therefore, the V_{bias} connection is needed. The bond pads come in different sizes capacitance values. To minimize the effects of the bonding pads, the low capacitance pads with a value of 100fF and a size of 50 x 100 μm^2 are used for each signal. To ease bonding and give the user the flexibility of being able to use multiple parallel bonding wires for each signal, two bonding pads were combined for the supply signals and three were combined for the I/O RF signals and the ground connection. The finalized layout is shown in Fig. 5.21. The final area of the chip layout including the bond pads is 655x723 μm^2. The area of the core is 325 x 280 μm^2 ,with the inductor taking up 216.5 x 226 μm^2 of the total area.

Chapter 6

Simulation Results

In RF circuits, simulation, and measurement results can show extreme discrepancies due to parasitics not accounted for in the simulations. Therefore, it is crucial to perform a comprehensive simulation by considering all possible parasitic effects that can arise in the real world. This chapter will discuss the simulation setup and results for the designed LNA.

6.1 Bond Wire Modelling

The designed LNA IC must be mounted onto a PCB, and the I/O pads must be connected to the external signals to use the designed LNA IC in real life. This is obtained by using bonding wires, which are thin pieces of conducting material, usually Gold, used to form an electrical connection between the pads. Due to their conductive nature, they introduce inductance and resistance into the bonding point, which can harm performance if not considered during the design and simulation process. A general rule of thumb when using a bond wire is that for a gold wire with a diameter of 25μm and 1 mm in length, an inductance around 1 nH arises. Placing more than one bond wire on the same pad can decrease this value due to the parallel connection formed between them [43]. Although this is

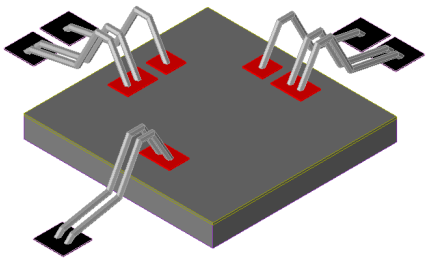


Figure 6.1: 3D bond wire simulation model

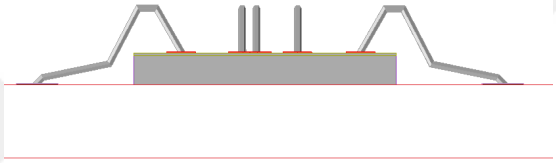


Figure 6.2: 3D bond wire simulation model side view

a good rule to remember, it is still essential to check and ensure this rule holds for the designed IC.

For the design of this thesis, the inductance value used for degeneration is critical for proper performance. If too much additional inductance arises from the bond wires used for the ground connection of the IC, it can throw off the operating point and match completely. To find an estimated value for the inductance that would arise from the bond wires connected to the ground pad, the Advanced Design Systems (ADS) program can be used since it offers a bond wire model that can accurately model its real-life effects.

The 3D view of the simulated model is shown in Fig. 6.1. The top pads in red are the bond pads of the designed LNA, and the black pads are connected to represent pads on the PCB from which the respective signals will be drawn. For this simulation, the thickness of the IC is taken as 120μm, and each bond wire is assigned a length of 0.5mm. The pads that have two bond wires attached are the RF_{IN}, RF_{OUT}, and GND pads. Since parallel bond wires are known to decrease the overall inductance of the connection, the connection points are more sensitive to additional inductance using this technique.

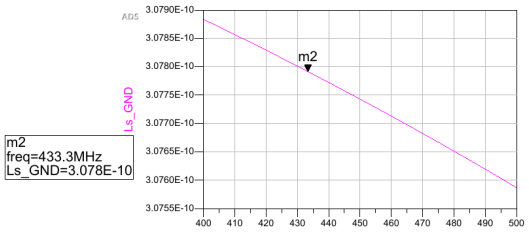


Figure 6.3: Ground pad bond wire inductance

The simulation results for the GND pad is shown in Fig. 6.3. At 430 MHz, the double bond wire connection shows an inductance of 307pH, which is close to the estimated value of 250 pH using the general rule of thumb.

To get more realistic results, this model will now be used in the ground path of the LNA during simulations.

6.2 Post-Layout Simulations

An RLC extraction is performed on the layout shown in 5.21 to see the effects of all the possible parasitics. With the RLC extraction, the parasitic inductors, capacitors, and resistors arising from the metal connections within the chip and pads are accounted for. To get an even more realistic simulation, the schematic shown in Fig. 6.5 is adjusted to include the wire bonding inductances and the parasitic of the external inductor L_g and bond pads. Due to the double bond wire model, the $L_{bw,RF}$ is set at 300 pH while $L_{bw,supply}$ is set at 500 pH assuming a gold bond wire with 25μm diameter and 0.5 mm in length. The external inductor L_g has a more complex model in comparison to the bond wire due to its inductive nature and SMD packaging. The detailed view of the SMD inductor model chosen for the design is shown in Fig. 6.4. The choice for this inductor is highly critical because it is placed directly at the input. Therefore, the parasitic resistance that it carries will have drastic effects on the NF. It is crucial to use an inductor with a high Q factor and low DC resistance to minimize the impact as much as possible. Especially at high inductance values such as 105 nH in this case, a low

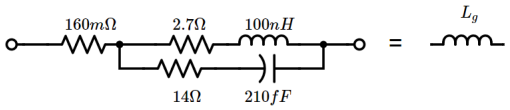


Figure 6.4: 100nH SMD Inductor Model

Q value will directly put a high resistance on the RF signal path, which will lower performance. Therefore, for this design, the 1008HQ Ceramic Inductor with a value of 100nH was chosen due to its extremely high Q value and overall good performance [44].

The S-parameter simulation results of the LNA pre-layout and post-extraction are shown in Figures 6.6a, 6.6b, , 6.7a, and 6.7b. The NF and stability results for the design are shown in Figures 6.8a and 6.8b. The figures display two post-extraction results: the first shows the post-extraction results with just the parasitic models of the bond wires. In contrast, the second one shows the results with all parasitic models, including the external SMD L_s). The results are displayed separately to bring attention to the significant effect of external inductance on the performance of the LNA. All results at the operating frequency of 437 MHz are listed in Tables 7.3 and 7.4. Due to the newly introduced parasitics from both the extraction and other factors, the values of the components in the matching circuit are changed to bring the circuit's resonant frequency back to 437 MHz. The finalized values for the components in the circuit are displayed in Tables 6.1 and 6.2.

Table 6.1: All component parameters for the final LNA post-extraction

$\frac{W_1}{L_1}$	$\frac{W_2}{L_2}$	L_s(nH)	C_{s1}(fF)	L_g(nH)	C_{s2}(pF)	C_{par}(pF)	$R_1(\Omega)$
$\frac{160}{0.18}$	$\frac{200}{0.18}$	0.743	400	100	7	70	50

Table 6.2: Biasing component parameters for the final LNA post-extraction

$\frac{W_1}{L_1}$	$R_{bias}(K\Omega)$	$R_{iso}(K\Omega)$
$\frac{20}{0.18}$	1.38	100

The red curves in all plots represent the performance of the LNA before the layout. The green curves represent the post-extraction results with only the

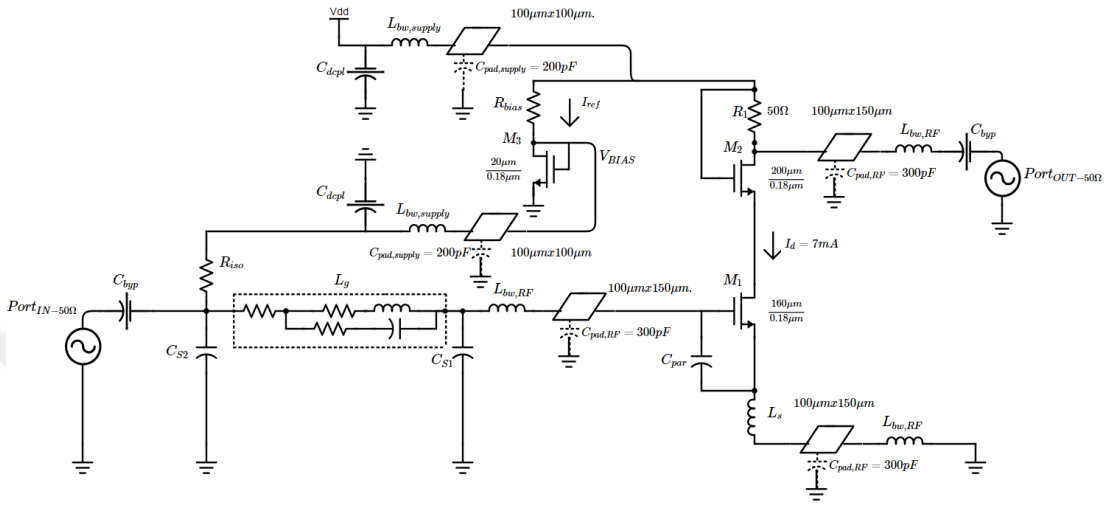
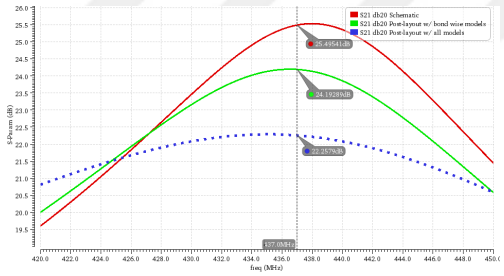
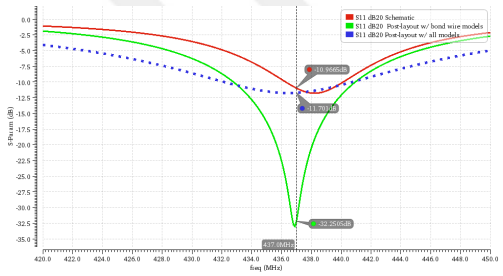


Figure 6.5: Schematic used to simulate the RLC extracted LNA and all parasitics

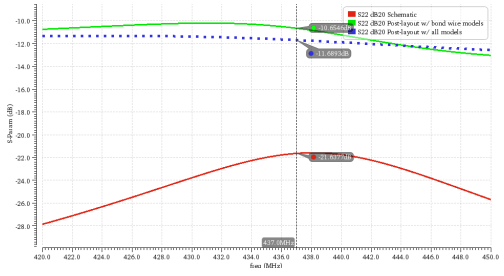


(a) S21 of LNA: schematic and extracted model comparison

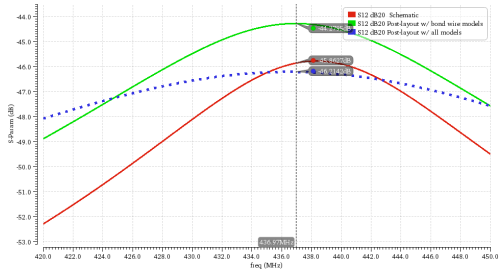


(b) S11 of LNA: schematic and extracted model comparison

Figure 6.6: S21 and S11 of LNA: schematic and extracted model comparison

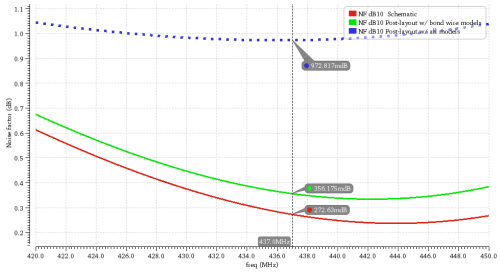


(a) S22 of LNA: schematic and extracted model comparison

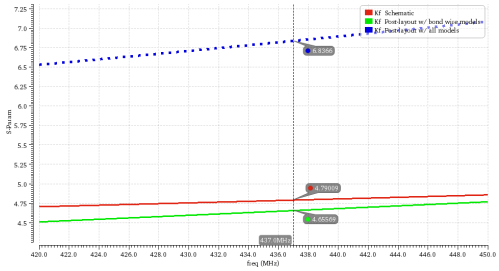


(b) S12 of LNA: schematic and extracted model comparison

Figure 6.7: S22 and S12 of LNA: schematic and extracted model comparison



(a) NF of LNA: schematic and extracted model comparison

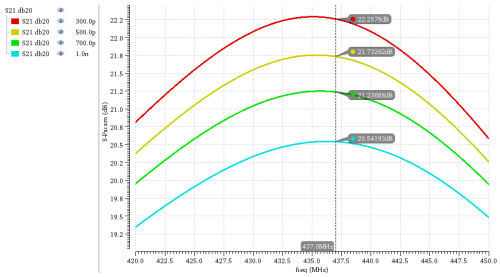


(b) Stability K factor of LNA: schematic and extracted model comparison

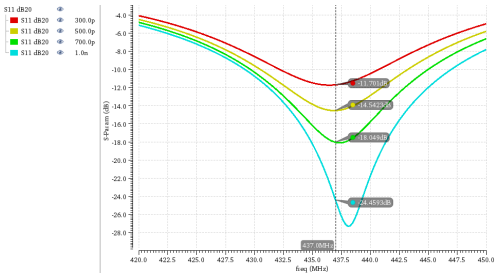
Figure 6.8: Noise Figure and Stability K factor of LNA: schematic and extracted model comparison

bond-wire parasitics, whereas the dotted blue curves include all parasitics including the external SMD inductor. After clear inspection of all simulation results, the degradation in performance due to unwanted parasitics can be seen clearly. To compare fall in performance between the schematic and final post-extraction results, the gain decreased by 2.24 dB, NF increased by 700.18 mdB, and the output return loss S_{22} decreased by 10dB. Not all performance parameters worsened, however. The input return loss increased drastically with the addition of the bond-wire, implying better matching, but it decreased once the SMD inductor was added. Even though the external inductor worsened the matching, it still created an input return loss 200 mdB greater than the pure schematic results. The reverse gain represented by S_{12} and the stability factor K also increased in comparison to the schematic results due to the additional parasitic resistance at the input. The IIP3 also increased, however due to the slight drop in gain, the OIP3 stayed constant.

Although the inductance used for ground connection was found using an accurate 3D solver, it is still important to verify the performance of the LNA at different $L_{bw,RF}$ values ensure that the design will work even if discrepancies arise between the simulated and real world bond wire. The S-parameter simulation results of the LNA with bond wire values of 300 pH, 500 pH, 700 pH, and 1 nH are shown in Figures 6.9a, 6.9b, 6.10a, and 6.10b. The NF and OIP3 results for the design are shown in Figures 6.11a and 6.11b. For comparison, the simulation

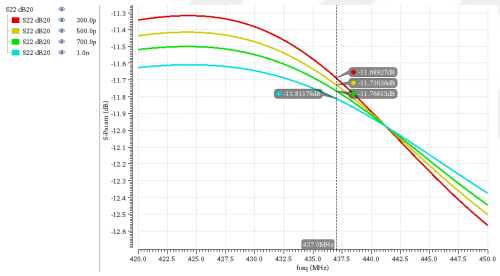


(a) S21 of LNA: results as bond wire is swept from $0pH$ to $1nH$

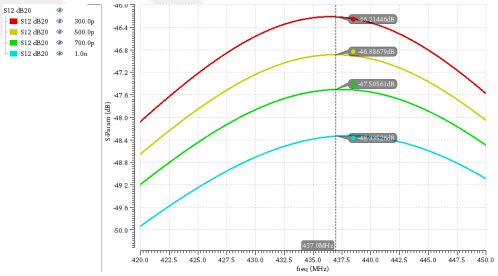


(b) S11 of LNA: results as bond wire is swept from $0pH$ to $1nH$

Figure 6.9: S21 and S11 of LNA: results as bond wire is swept from $0pH$ to $1nH$

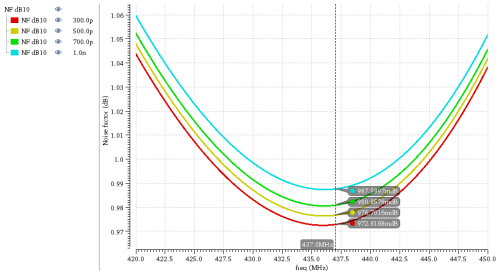


(a) S22 of LNA: results as bond wire is swept from $0pH$ to $1nH$

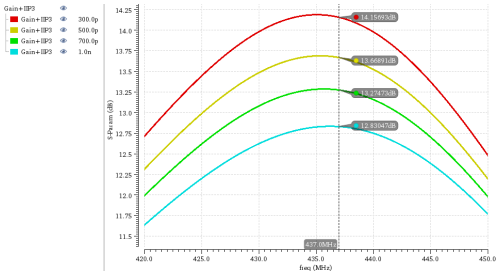


(b) S12 of LNA: results as bond wire is swept from $0pH$ to $1nH$

Figure 6.10: S22 and S12 of LNA: results as bond wire is swept from $0pH$ to $1nH$



(a) NF of LNA: results as bond wire is swept from $0pH$ to $1nH$



(b) Stability K factor of LNA: results as bond wire is swept from $0pH$ to $1nH$

Figure 6.11: Noise Figure and OIP3 of LNA: results as bond wire is swept from $0pH$ to $1nH$

results with a large inductance of 1nH $L_{bw,RF}$ are also listed in Tables 7.3 and 7.4. All parasitics were included in these simulations, therefore the effects of the SMD inductor can be seen in these simulations as well.

Table 6.3: Schematic and post-layout simulation results

	S_{21}(dB)	S_{11}(dB)	S_{22}(dB)	S_{12}(dB)	NF(mdB)	K
Schematic	25.49	-10.96	-21.63	-45.86	272.63	4.65
Post-layout, $L_{bw,RF} = 300pH$	24.19	-32.25	-10.65	-44.28	356.17	4.79
Post-layout w/ all parasitics $L_{bw,RF} = 300pH$	22.25	-11.70	-11.69	-46.21	972.82	6.84
Post-layout w/ all parasitics $L_{bw,RF} = 1nH$	20.54	-24.46	-11.81	-48.33	987.60	11.43

Table 6.4: Schematic and post-layout simulation results cont.

	$IIP3$(dBm)	$IP1dB$(dBm)	P(mW)
Schematic	-15.61	-25.25	12.99
Post-layout, $L_{bw,RF} = 300pH$	-13.71	-23.88	12.57
Post-layout w/ all parasitics $L_{bw,RF} = 300pH$	-12.26	-22.22	12.57
Post-layout w/ all parasitics $L_{bw,RF} = 1nH$	-9.80	-20.20	12.55

In comparison to the 300 pH inductor, a 1 nH ground inductor degraded the performance overall. The NF increases to 987.6 mdB and gain decreased to 20.54 dB. This is expected since placing a higher inductor as the source degeneration causes more parisitic resistance at the source of the transistor. It, however, enhances the input matching significantly which can be beneficial depending on the application. Overall, the performance of the LNA after post-layout RLC extraction and bond wire, bond pad, and external component modeling still satisfies all of the design criteria with the ground pad bond wire inductance ranging from the simulated inductance of 300 pH to 1 nH.

The previous simulations were all done under typical operating conditions, meaning the transistors are in the typical corner, the supply voltage is stable at $1.8V$, and the temperature is room temperature 27(°C). To see the effects of

variation in temperature and supply voltage, a detailed analysis is performed. The results are displayed in Tables 6.5, 6.6, and 6.7. After careful inspection, all results except the NF and power at an operating temperature of 75(°C) meet the initial performance metrics. However, they are in a ±10% margin. This was expected since the circuit is not designed in a temperature and voltage invariant way. This small problem can be resolved in the future by giving the bias voltage of the transistor from a temperature invariant voltage generator.

Table 6.5: Post-layout simulation results of S_{21}, S_{11}, S_{22}, S_{12}, NF with varying temperature and supply voltage

Temp (°C)	Supply Voltage (V)	Performance Metrics				
		S_{21}(dB)	S_{11}(dB)	S_{22}(dB)	S_{12}(dB)	NF(mdB)
-25	1.6	21.93	-11.39	-47.34	-13.00	0.821
	1.8	22.61	-12.51	-47.25	-12.94	0.815
	2.0	23.11	-13.42	-47.02	-12.88	0.810
27	1.6	21.63	-10.79	-46.59	-11.73	0.979
	1.8	22.26	-11.70	-46.21	-11.69	0.972
	2.0	22.72	-12.48	-45.56	-11.65	0.967
75	1.6	21.40	-10.37	-45.69	-10.77	1.12
	1.8	21.97	-11.15	-44.89	-10.75	1.11
	2.0	22.38	-11.86	-43.60	-10.75	1.10

Table 6.6: Post-layout simulation results of IIP3, IP1, and K with varying temperature and supply voltage

Temp (°C)	Supply Voltage (V)	Performance Metrics		
		$IIP3$ (dBm)	$IP1$(dBm)	K
-25	1.6	-13.46	-22.60	8.19
	1.8	-13.00	-22.25	7.63
	2.0	-12.46	-22.14	7.10
27	1.6	-12.79	-22.41	7.53
	1.8	-12.27	-22.23	6.84
	2.0	-11.94	-22.01	6.09
75	1.6	-12.70	-22.60	6.78
	1.8	-12.21	-22.36	5.90
	2.0	-12.36	-22.17	4.92

Another critical simulation is a corner simulation. TSMC has determined the process corners to be TT (Typical-Typical), SS (Slow-Slow), and FF (Fast-Fast).

Table 6.7: Post-layout simulation results of Current (I) and Power (P) with varying temperature and supply voltage

Temp (°C)	Supply Voltage (V)	Current and Power	
		I(mA)	P(mW)
-25	1.6	5.49	8.784
	1.8	6.77	12.186
	2.0	8.07	16.14
27	1.6	5.72	9.152
	1.8	6.98	12.564
	2.0	8.28	16.56
75	1.6	5.88	9.408
	1.8	7.14	12.852
	2.0	8.43	16.86

These corners represent the different manufacturing conditions that could affect the performance of the LNA. TT represents typical conditions, SS represents the worst-case scenario with slower transistors, and FF represents the best-case scenario with faster transistors [33]. In the SS corner, the supply voltage is set to $2V$, and the temperature is -25(°C) to simulate the best case operation scenario whereas in the FF corner, the supply voltage is set to $1.6V$, and the temperature is 75(°C) to simulate the worst case operation scenario. The results of the corner simulation in comparison to the typical operating corner are displayed in Tables 6.8, 6.9, and 6.10. The results of the corner analysis reflect the effects of supply variation again. Therefore, it can be said that the operating corners of the transistor do not affect the performance of the LNA.

Table 6.8: Post-layout simulation results ofS_{21}, S_{11}, S_{22}, S_{12}, NF for TT, FF, and SS corners

Temp	Process Corner	Performance Metrics				
		S_{21}(dB)	S_{11}(dB)	S_{22}(dB)	S_{12}(dB)	NF(mdB)
27°C	TT	22.26	-11.70	-46.21	-11.69	0.972
-25°C	FF	23.36	-13.99	-45.10	-15.63	0.808
75°C	SS	20.85	-9.37	-47.64	-8.69	1.13

Lastly, although the stability factor (K) is given in the result tables, it is important to verify it in a wider frequency rage. The K factor the all process

Table 6.9: Post-layout simulation results of IIP3, IP1, and K for TT, FF, and SS corners

Temp	Process Corner	Performance Metrics		
		$IIP3$ (dBm)	$IP1$(dBm)	K
27°C	TT	-12.27	-22.23	6.84
-25°C	FF	-12.19	-22.22	5.73
75°C	SS	-12.41	-22.26	8.33

Table 6.10: Post-layout simulation results of Current (I), Power (P) for TT, FF, and SS corners

Temp	Process Corner	Current and Power	
		I(mA)	P(mW)
27°C	TT	6.98	12.564
-25°C	FF	9.70	19.400
75°C	SS	4.93	7.888

corners are displayed in Fig. 6.12. It can be seen that the $K > 1$ condition holds for all process corners in a wide frequency range. Therefore, the stability of the LNA is assured under all process conditions.

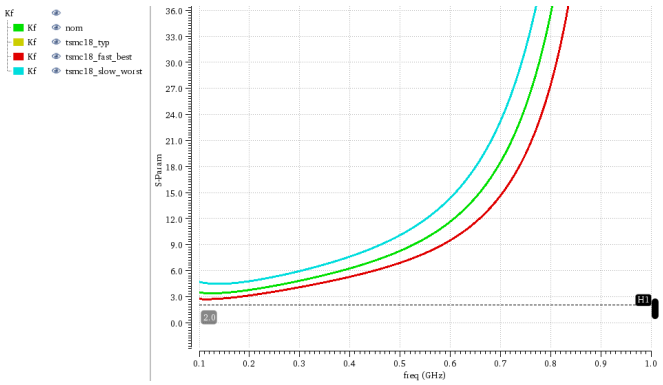


Figure 6.12: Stability Factor (K) of the LNA from $100MHz$ to $1GHz$ for all corners

Chapter 7

LNA Design for Single and Array MRI Applications

The previous design was optimized to work in a single coil 10.3 T MRI system due to its operating frequency of 437 MHz, which is the Lamore frequency of the defined system and its 50Ω input impedance. The advantage of using a $\pi - network$ matching circuit outside of the chip is the flexibility of shifting the network's resonance frequency after production is complete to accommodate various design requests.

In addition to serving as the first amplification stage, an LNA plays a crucial role in decoupling adjacent coils within an array in array MRI applications. It achieves this by terminating each end of the coil in an array with a high impedance set by either the input of the LNA or with a λ conversion of the LNA input. An example system using the λ conversion is shown in Figure 7.1. In this situation, a significant mismatch is seen between the input impedance and source impedance at the LNA inputs; therefore, the measured input return loss S_{11} becomes closer to 0 dB [9]. The high impedance at the coil terminals causes elements in the array to be decoupled. Although this is usually not desired in a typical LNA, it becomes advantageous for array MRI applications [45].

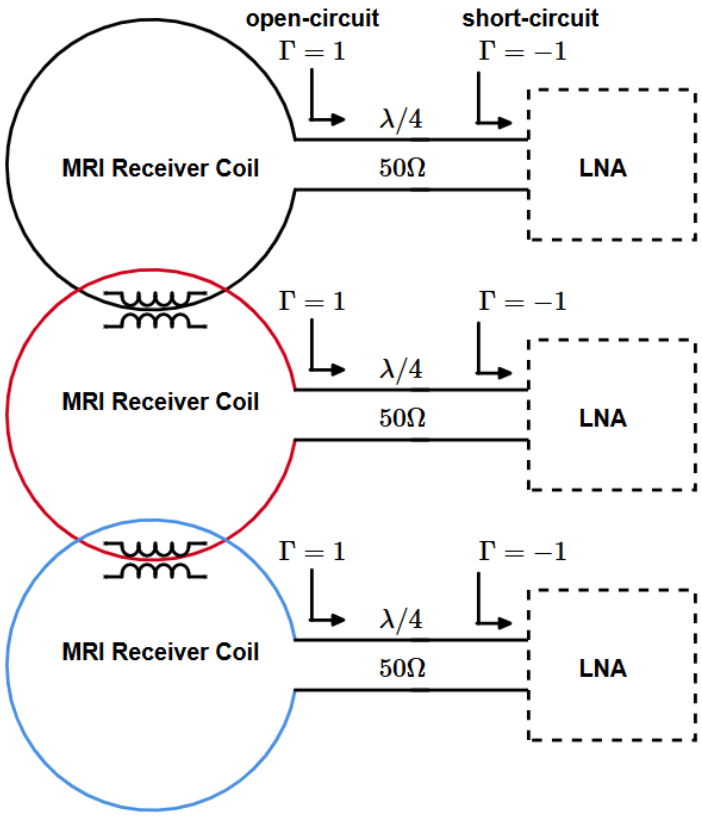


Figure 7.1: MRI Array Decoupling Scheme

In this section, firstly, the π-network of the previously designed LNA will be adjusted to fit the requirements of a 10.5T array MR system by operating at the defined Lamore frequency of 447MHz. Afterward, a single-ended and differential-ended structure will introduce another LNA design better fit for 10.5 T Array MRI applications. In Section 7.1, a design using a 1.8 V supply voltage and initially built for noise and input matching is used as an MRI LNA. Section 7.2 introduces and discusses a new LNA designed specifically for Array MRI applications and built for 3.3 V supply voltages.

7.1 Design Option for a Single 10.5 T 447 MHz MR System LNA

The previous design optimized the π-network for simultaneous input and noise matching. However, for the array application, the input matching can be disregarded. This eases the noise-matching process significantly.

The previous inductively degenerated cascode amplifier was reused for this design with a change in the π-network. As shown in Fig. 6.5, the previous π-network comprises two parallel connected capacitors and a series inductor. The capacitor close to the source C_{S2} shifted the input impedance down close to the source on the admittance Smith Chart. The effect of this component is shown as the shift between the blue and green impedance lines in Fig. 5.11. The desired S_{11} for the array MRI application should lie closer to the left of the Smith Chart, representing a short-circuit input. Therefore, the C_{S2} is removed in the π-network of this application. Another change in this application is the value of the previous design's series gate inductor L_g. To provide input matching, the optimal L_g value was 105 nH. Due to its large value, the SMD inductor brought a huge parasitic resistance to the circuit, as shown in its model in Fig. 6.4. Since input matching is not critical, this value can be scaled down to get a lower parasitic resistance and, therefore, a lower noise figure. For this application, another High-Q SMD Coilcraft inductor with a value of 82 nH is used. The model for this inductor and its parasitic components are shown in Fig. 7.2 [46].

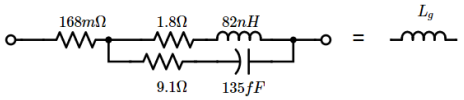


Figure 7.2: 82nH SMD Inductor Model

The reason behind not picking a smaller value inductor might be questioned. To obtain the minimum noise figure and maximum power gain without input matching, the π-network must resonate at the operating frequency. The resonance

frequency of an LC circuit can be defined as

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{7.1}$$

in which L represents L_g and C represents the sum of C_{S1} and the input capacitance of the input transistor M_1. At the resonance frequency, the network impedance is minimal, and energy is transferred between these two components with minimal loss. Therefore, maximum gain and minimum noise figures are attained. This resonance frequency is also equal to the Larmor Frequency of the MRI system, which is 447 MHz in our 10.5 T array design [7]. If the chosen L_g value were to be smaller, the parallel capacitor C_{S1} has to be larger to satisfy the resonance frequency condition. However, like a large inductor value, a large capacitor value also causes an increase in NF. Additionally, a large parallel capacitor causes the impedance to move further down the Smith Chart to lower real impedance circles, and to satisfy the high input impedance condition; a large inductor is required to move it to the left part of the Smith Chart. Therefore, an optimal L_g and C_{S1} exists for each application. For the 10.5 T application, these values are 82 nH and 650 fF. This design's complete list of values is displayed in Tables 7.1 and 7.2. Values other than the π-network components are kept the same.

Table 7.1: All component parameters for the final 10.5T LNA post-extraction

$\frac{W_1}{L_1}$	$\frac{W_2}{L_2}$	L_s(nH)	C_{s1}(fF)	L_g(nH)	C_{par}(pF)	$R_1(\Omega)$
$\frac{160}{0.18}$	$\frac{200}{0.18}$	0.743	650	82	70	50

Table 7.2: Biasing component parameters for the final 10.5T LNA post extraction

$\frac{W_1}{L_1}$	$R_{bias}(K\Omega)$	$R_{iso}(K\Omega)$
$\frac{20}{0.18}$	1.38	100

This optimized input π-network is simulated with the fully modeled and extracted LNA chip from the previous design to obtain the final results of the 10.5 T LNA. The simulation results are shown in Figures 7.3, 7.4, and 7.5.

The NF results shown in Figure 7.5 show the NF values of the LNA with an ideal inductor and SMD inductor model with the dotted and solid red plots

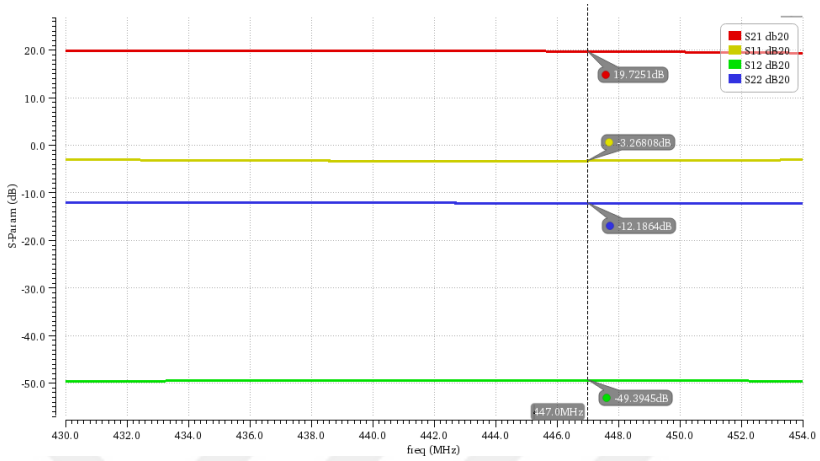


Figure 7.3: S Parameter results of the 10.5T LNA

Table 7.3: Schematic and post-layout simulation results of 10.5T LNA

	S_{21}(dB)	S_{11}(dB)	S_{22}(dB)	S_{12}(dB)	NF(mdB)	K
Post-layout w/ all parasitics $L_{bw,RF} = 300pH$	19.75	-3.27	-12.18	-49.39	507.27	7.49

respectively. The yellow plot shows the minimum NF_{min} value possible with the SMD inductor model. From this plot, the serious jump in NF due to the parasitic resistance of the inductor can be seen. While the NF is below 320 mdB with an ideal inductor, it jumps to 509 mdB once the parasitics of the real inductor come into play within the model. It can also be seen that the LNA has been matched perfectly in terms of noise at exactly 447 MHz and the minimum NF value possible is obtained.

The $S11$ plot in Fig. 7.4 shows the serious mismatch between the source and input impedance. In this design, the input impedance is moved to nearly 10Ω, satisfying the condition needed to terminate the end of each coil successfully to avoid coupling within adjacent coils.

The final values of the performance metrics for this design are displayed in detail in Tables. All simulation results are obtained under the typical operating corner with the simulated bond-wire inductance of 300 pH.

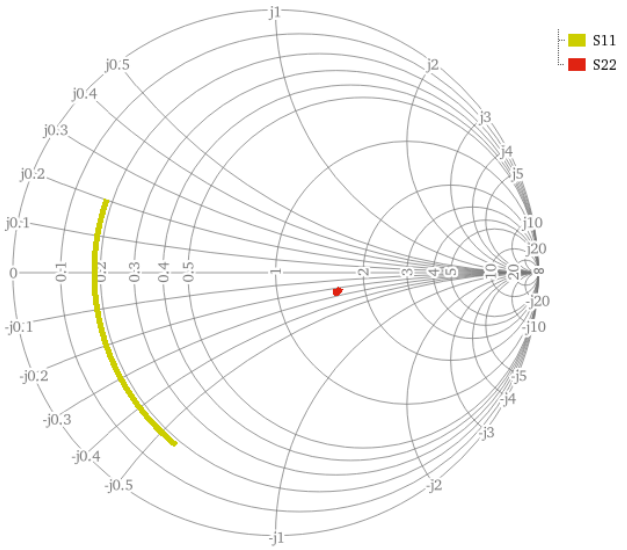


Figure 7.4: S11 and S22 of 10.5T LNA displayed on the Smith Chart

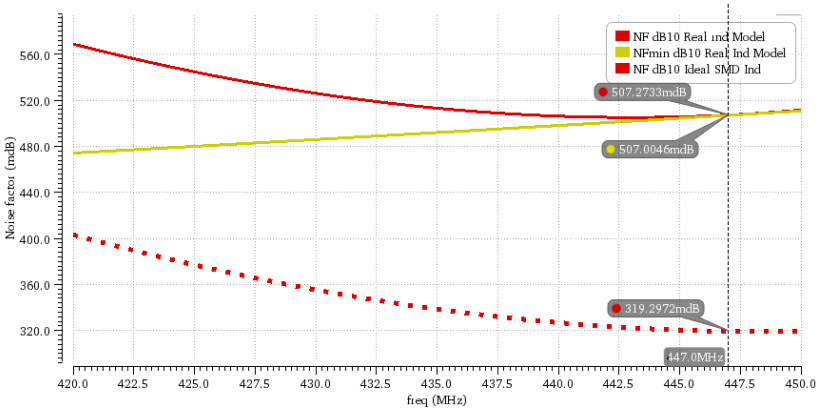


Figure 7.5: NF results of the 10.5T LNA

Table 7.4: Schematic and post-layout simulation results cont. of 10.5T LNA

	$IIP3$(dBm)	$IP1dB$(dBm)	P(mW)
Post-layout w/ all parasitics $L_{bw,RF} = 300pH$	-10.18	-20.16	12.56

7.2 Improved Design Option for a Single 10.5T 447MHz Array MR System LNA

In the previous design, the external matching network was adjusted to accommodate the requirements for an MRI LNA. As stated in previous chapters, although a Common-Source amplifier structure is beneficial in normal LNA designs for input matching, it is actually not as useful for MRI LNA designs. An improved version of the previous Cascode amplifier structure is introduced in this section.

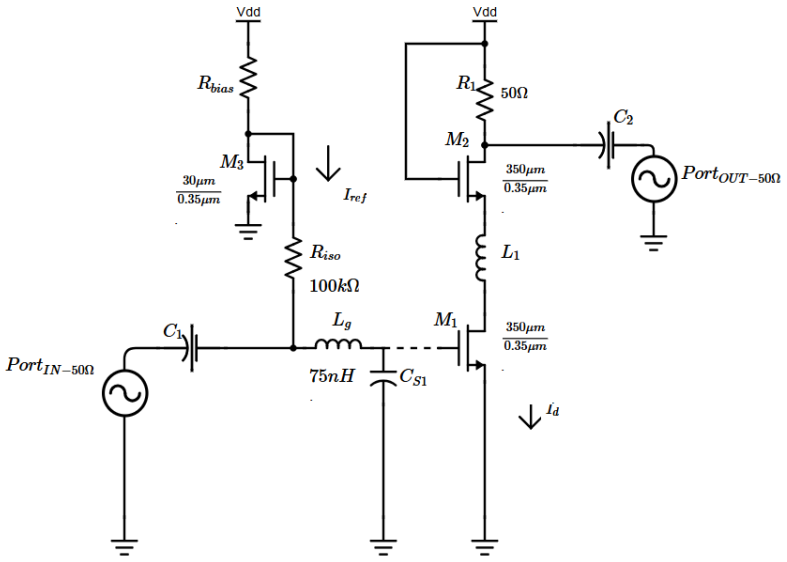


Figure 7.6: Improved Single-Ended MRI LNA Design

The improved amplifier is shown in Fig. 7.6. As it can be seen from the schematic view, the common source degeneration is removed and instead an inductor is placed between the two cascode stages. This technique known as inductive peaking is used as a way to increase gain within a cascode amplifier [6]. In

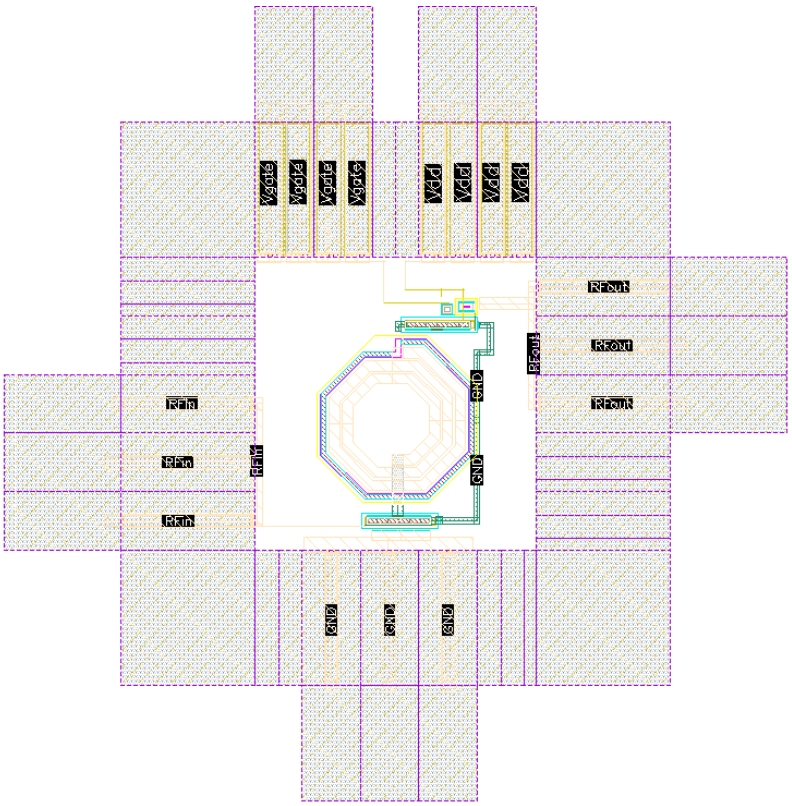


Figure 7.7: MRI LNA Single-Ended Layout

this design, the inductor placed between the common source and common gate stages aids in decreasing the input resistance of the amplifier by interacting with the parasitic capacitances of the input MOSFET devices. With the help of the inductor, the input impedance is pulled down to desired levels while keeping the noise figure constant. A downside of using inductive peaking is loss in stability. By increasing gain within the amplifier and decreasing the input impedance, the amplifier is pushed into a less stable state. However, ensuring stability within the operating region is enough for MRI LNA applications [45]. The layout of the design can be seen in Figure 7.7. Like the previous designs, this layout also includes multiple gate contacts on the transistors and use of thick top metals to decrease parasitics and improve the noise performance. The total size of the layout including the bonding pads is $668\mu m$ x $678\mu m$.

The fully modeled and extracted schematic of the design can be seen in Figure 7.8. The components in the red boxes in Fig. 7.8 represent the external matching

and biasing components. Like the previous design, this version also uses an external SMD inductor with a value of 75 nH to achieve appropriate noise matching. Although this inductor comes with significant parasitic resistance, the inductive peaking technique significantly reduces its effects. The values of the components used in the design can be seen in Tables 7.5 and 7.6.

Table 7.5: All component parameters for the final 10.5T LNA for array applications, post extraction

$\frac{W_1}{L_1}$	$\frac{W_2}{L_2}$	L_1(nH)	C_{s1}(fF)	L_g(nH)	$R_1(\Omega)$
$\frac{300}{0.35}$	$\frac{300}{0.35}$	0.800	600	75	50

Table 7.6: Biasing component parameters for the final 10.5T LNA for array applications post extraction

$\frac{W_3}{L_3}$	$R_{bias}(K\Omega)$	$R_{iso}(K\Omega)$
$\frac{30}{0.350}$	5	100

The schematic and post-layout simulation results for the single-ended designs can be seen in Figures 7.9, 7.10 and 7.11. The schematic results are shown with solid lines, while the post-layout results are shown with dotted lines in all results. In the schematic simulations, all results seem to fall in the initial specifications. With an S_11 of -0.4 dB, NF of 0.3 dB and gain S21 of 18 dB, the designs seems perfect for a single coil MRI application. The decrease in stability can be seen in the lower plot in 7.10 with the schematic having a k factor of 1.8 at the operating frequency. The effects of the layout can be seen in the dotted curves in all results. After extraction, the NF seems to have increased to 0.422 dB, which is still satisfying the requirement of a low noise amplifier. However, the input return loss has increased to 0.9 dB. For the LNA the initial goal was to keep the return loss below 0.5 dB, however this is very hard to achieve with a big external SMD inductor which is unavoidable with these transistors in this operating frequency since it is a must for noise matching. Although the return loss has gone above the initial goal, it is still below the 1 dB limit and as it can be seen in Fig. 7.11, the input impedance is still below 5Ω which is close to being considered a short circuit. Due to additional parasitics and the change in input return loss, the gain slightly increased and the circuit entered a more stable state. The output return

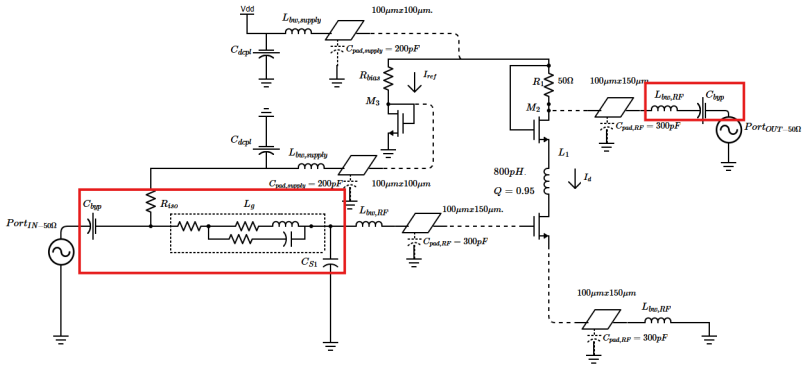


Figure 7.8: Fully Modeled Single-Ended MRI LNA Design

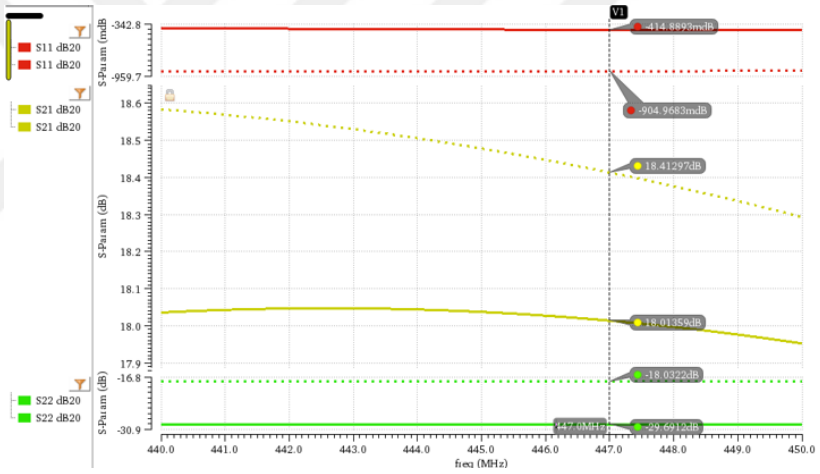


Figure 7.9: Single-Ended MRI LNA Design S-Parameter Results

loss, shown as $S22$ decreased to -18 dB after extraction, which is still under the defined limits. It is important for the output to be perfectly matched to 50Ω to avoid any reflection and loss. The schematic and post-layout simulation results can be seen in Tables 7.7 and 7.8.

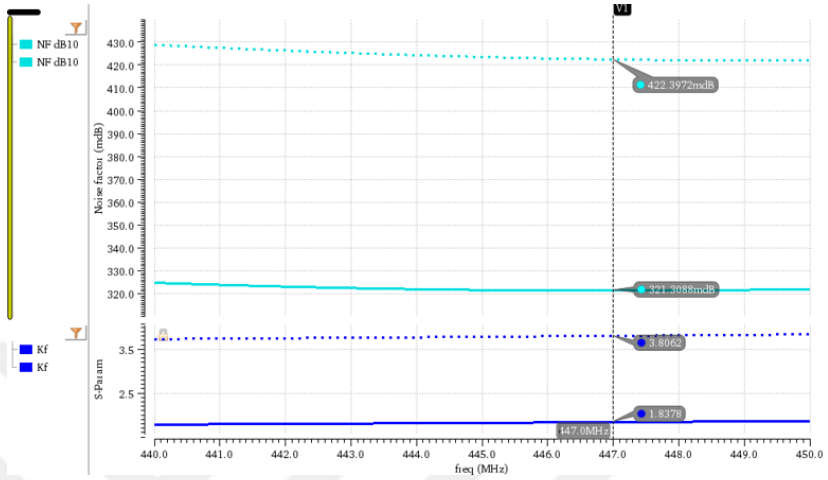


Figure 7.10: Single-Ended MRI LNA Design NF and Stability Results

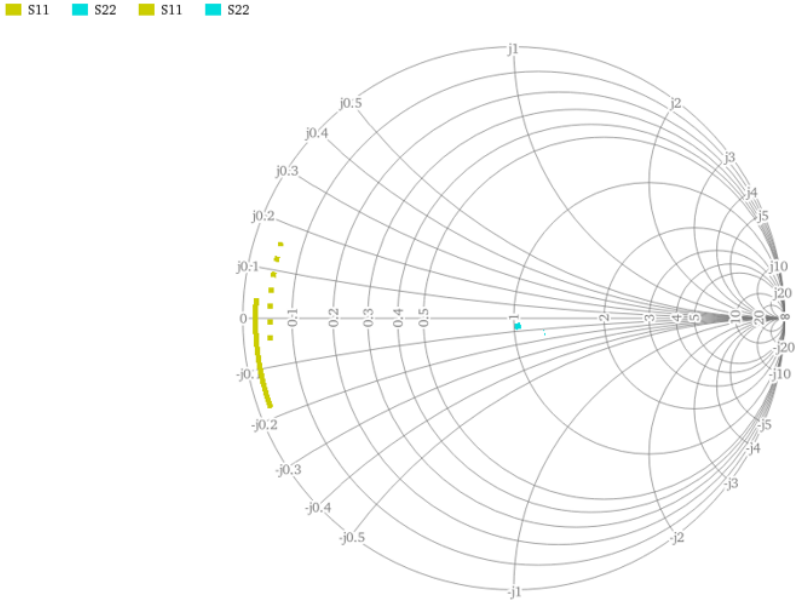


Figure 7.11: Single-Ended MRI LNA Design S11 and S22

Table 7.7: Schematic and post-layout simulation results for single-ended topology

	S_{21}(dB)	S_{11}(dB)	S_{22}(dB)	S_{12}(dB)	NF(mdB)	K
Schematic	18.01	-0.41	-29.69	-42.56	321.00	1.83
Post-layout w/ all parasitics $L_{bw,RF} = 300pH$	18.42	-0.90	-18.03	-39.95	422.39	3.80

Table 7.8: Schematic and post-layout simulation results cont. for single-ended topology

	$IIP3$(dBm)	$IP1dB$(dBm)	P(mW)
Schematic	-19.26	-28.95	17.16
Post-layout w/ all parasitics $L_{bw,RF} = 300pH$	-17.12	-27.38	19.47

7.3 Differential-Ended 10.5T 447MHz Array MR System LNA

The single-ended topology used in the previous section successfully meets the requirements of an MRI LNA, however, thanks to the high integration density coming from CMOS technology, a differential-ended version providing greater amounts of common-mode signal rejection, or a higher *Common Mode Rejection Ratio* (CMRR) can also be implemented [47]. With the help of a differential topology, the amplifier becomes more resilient to distortions like common mode noise and gate voltage variations. The designed amplifier is shown in Figure 7.12 and the complete circuit including all external and parasitic elements is shown in Figure 7.13. The elements shown in red boxes are placed externally and bondwire inductance resulting from external connections are all modeled. The differential-ended topology mirrors the single-ended with the use of inductive peaking between the CG and CS stages, however this topology requires the use of a greater inductor value. For this design, the inductor is chosen to be 1.98 nH with a Q factor of 1.05. The external SMD inductor is again chosen as 75 nH. The main difference between the differential-ended and single-ended designs is the biasing circuit. In the previous designs, a simple current mirror is used to bias the main input transistors at the appropriate operating region for best noise performance. In the differential topology due to the additional tail current source transistor M_B, the amplification transistor M_1 and M_2 experience a significant drop in headroom as a result of the V_{DSat} of the tail source transistor. To provide more headroom to the main transistors and to create a bias for the tail current source, a low headroom current mirror with cascode transistors is designed [6]. These can be seen in the circuit in the left of Fig. 7.13 as transistors M_3 and M_4.

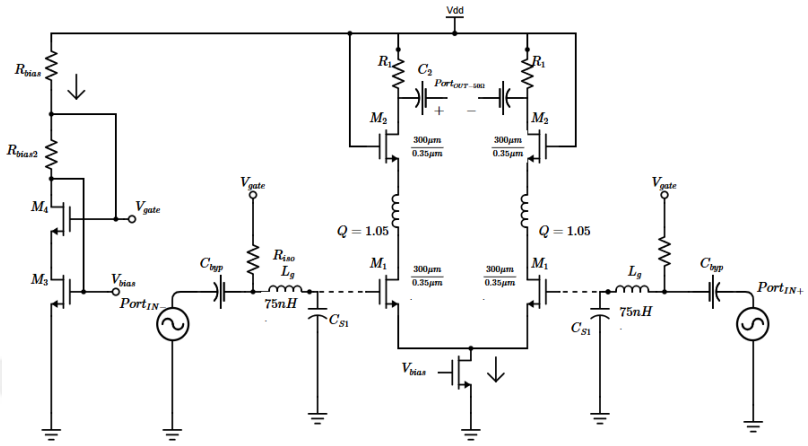


Figure 7.12: Differential-Ended MRI LNA Design

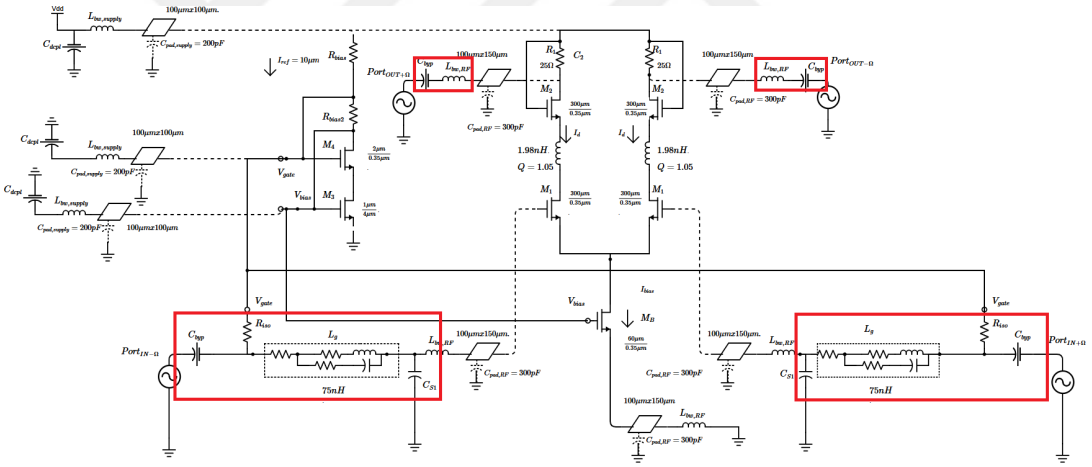


Figure 7.13: Fully Modeled Differential-Ended MRI LNA Design

With the help of this circuit, all transistors including the tail current source are able to stay safely within the saturation operation region.

The layout of the design can be seen in Figure 7.14. The total size of the layout including the bonding pads is 728μm x 778μm.The values of the components used in the design can be seen in Tables 7.9 and 7.10.

The schematic and post-layout simulation results for the differential-ended design can be seen in Figures 7.15, 7.16 and 7.17. The schematic results are shown with solid lines, while the post-layout results are shown with dotted lines

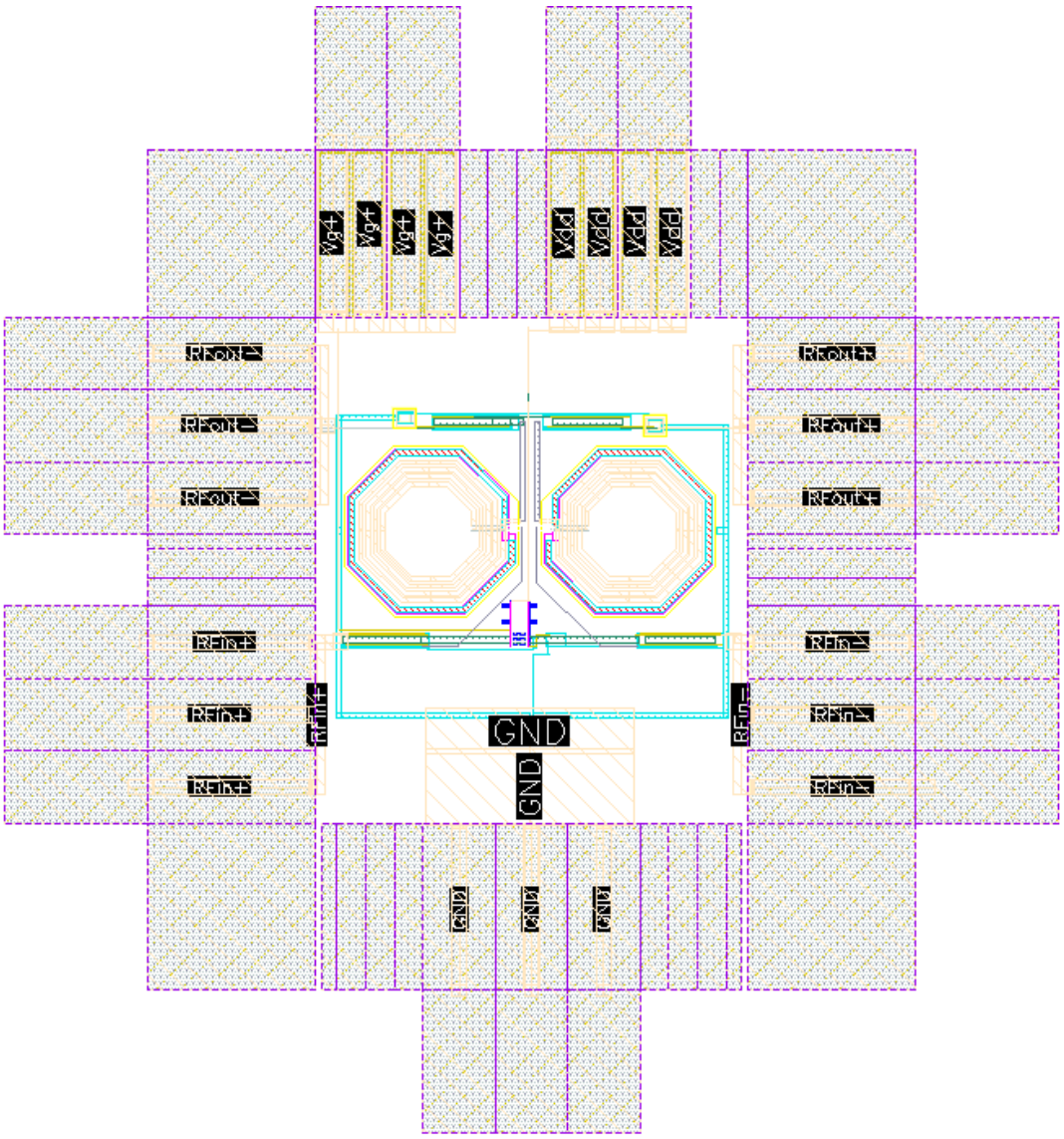


Figure 7.14: Differential-Ended MRI LNA Layout

Table 7.9: All component parameters for the final 10.5T differential-ended LNA for array applications, post extraction

$\frac{W_1}{L_1}$	$\frac{W_2}{L_2}$	$\frac{W_B}{L_B}$	L_1(nH)	C_{s1}(fF)	L_g(nH)	$R_1(\Omega)$
$\frac{300}{0.35}$	$\frac{300}{0.35}$	$\frac{60}{0.35}$	1.98	520	75	25

Table 7.10: Biasing component parameters for the final 10.5T differential-ended LNA for array applications post extraction

$\frac{W_3}{L_3}$	$\frac{W_4}{L_4}$	$R_{bias}(K\Omega)$	$R_{bias2}(K\Omega)$	$R_{iso}(K\Omega)$
$\frac{1}{4}$	$\frac{2}{0.350}$	164	10	100

in all results. In the schematic simulations, all results seem to fall in the initial specifications with an S_11 of -0.379 dB, NF of 0.509 dB and gain S21 of 14.76 dB. Like the single-ended version, the decrease in stability can again be seen in the lower plot in 7.16 with the schematic having a k factor of 3.48 at the operating frequency.

The effects of the layout can be seen in the dotted curves in all results. After extraction, the NF seems to have increased to 0.599 dB, still satisfying the requirement of a low noise amplifier. However, the input return loss has increased to 0.941 dB. Although the return loss has gone above the initial goal, it is still below the 1 dB limit and as it can be seen in Fig. 7.17, the input impedance is still below 5Ω which is close to being considered a short circuit. Due to additional parasitics and the change in input return loss, the gain slightly increased and the circuit entered a more stable state. The output return loss, shown as $S22$ decreased to -18.73 dB after extraction, which is still under the defined limits. It is important for the output to be perfectly matched to 50Ω to avoid any reflection and loss. The schematic and post-layout simulation results can be seen in Tables 7.11 and 7.12. In comparison to the single-ended version, the differential topology came out with a higher current consumption of 6.47 mA, however, the degradation in gain and noise performance is beacuse of the main transistors operating at lower I_{ds} values.

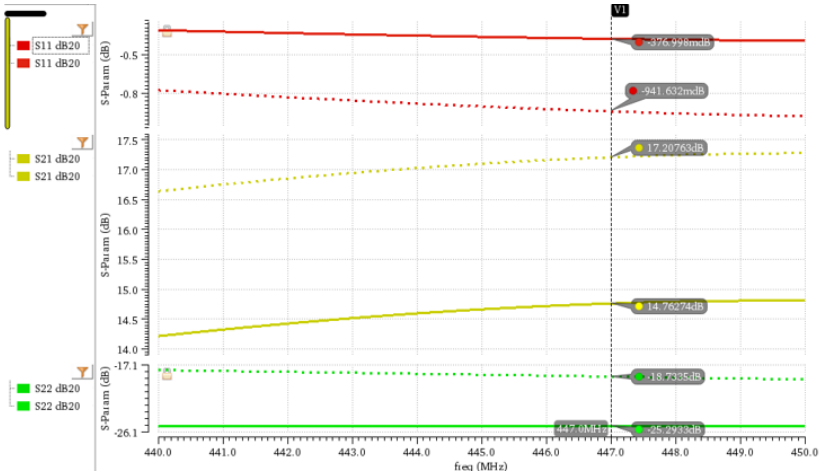


Figure 7.15: Differential-Ended MRI LNA Design S-Parameter Results

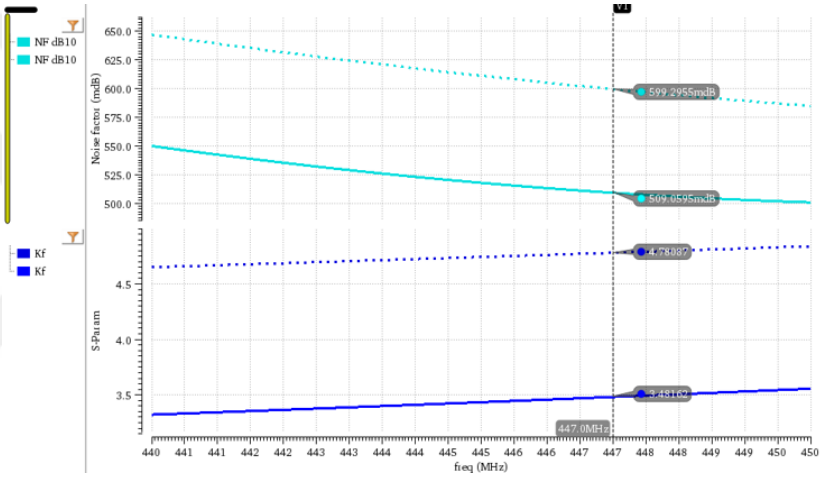


Figure 7.16: Differential-Ended MRI LNA Design NF and Stability Results

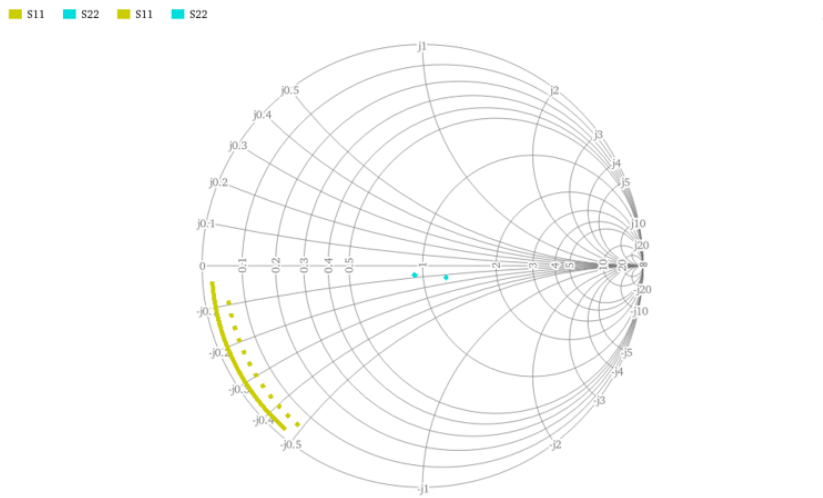


Figure 7.17: Differential-Ended MRI LNA Design S11 and S22

Table 7.11: Schematic and post-layout simulation results for differential-ended topology

	S_{21}(dB)	S_{11}(dB)	S_{22}(dB)	S_{12}(dB)	NF(mdB)	K
Schematic	14.76	-0.38	-25.29	-46.05	509.00	3.48
Post-layout w/ all parasitics $L_{bw,RF} = 300pH$	17.20	-0.94	-18.73	-42.15	599.29	4.78

Table 7.12: Schematic and post-layout simulation results cont. for differential-ended topology

	$IIP3$(dBm)	$IP1dB$(dBm)	P(mW)
Schematic	-18.03	-28.12	19.14
Post-layout w/ all parasitics $L_{bw,RF} = 300pH$	-14.36	-24.42	21.35

As stated in previously, the main advantage in using a differential-ended LNA is the protection it provides to common-mode fluctuations. This can be measured in terms of *Power Supply Rejection Ratio* (PSRR). The PSRR values for both the single-ended and differential-ended Array MRI LNA sturcture is shown in Figure 7.18. The PSRR for the differential-ended structure is clearly significantly better then that of the single-ended structure, hence making it a more reliable topology.

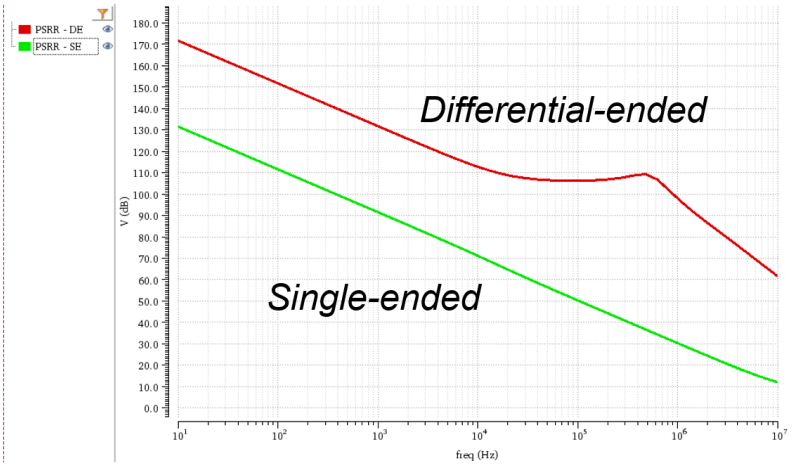


Figure 7.18: PSRR of Designed Circuits

Chapter 8

Conclusion

In today's high-frequency applications, low noise amplifiers (LNAs) play a pivotal role in amplifying weak signals while minimizing noise. They can be found in most receiver systems and are especially critical in MRI implementations used for medical imaging. The literature review highlights that LNAs operating at frequencies around 437MHz and 447MHz can be particularly beneficial for implementation within 10.3T and 10.5T MRI systems. While GaAs and SiGe technologies remain favored for their proven superior RF performance, CMOS technology has gained popularity due to its ability to integrate complete RF systems onto a single silicon chip. However, CMOS technology also presents challenges, such as increased noise from the channel structure and excessive thermal noise due to hot electron effects. In the studied literature, an LNA operating at the desired frequencies of 437MHz and 447MHz and satisfying the sub-1dB noise figure criteria was not found. Although some works were published for 405MHz, 435MHz, and 450MHz, each design has specific limitations.

The goal of this thesis was to design LNAs for both single-coil and array-coil 10.5 T Receiver MRI applications, addressing their distinct requirements and challenges. For single-coil systems, the LNA must achieve precise impedance matching to the coil's typical 50-ohm impedance to ensure maximum power transfer and minimal signal reflection, with an input return loss S_{11} well below 0

dB. In contrast, for array-coil systems, the LNA is required to present an input impedance resembling a short circuit, resulting in an S_{11} near 0 dB when connected via a quarter-wave transmission line. This ensures minimal current in each coil and reduces mutual coupling, a critical requirement for maintaining signal isolation and performance across multiple closely spaced coils. One of the big challenges for these designs is the requirement of off-chip components, especially SMD inductors, to achieve precise impedance matching and noise optimization. The use of large external inductors is necessary at these frequencies to provide the required reactance for tuning and noise matching. However, since the integration of these within a chip is nearly impossible, in addition to the low performance of inductors at VHF bands, the parasitic effects of the external packaging and bonding is detrimental to the performance of the LNA. This issue was specifically tackled in all designs.

A cascode amplifier with source degeneration was chosen as the topology to start the design for a single-coil application. Despite other topologies achieving good input matching with a fixed 50Ω source, the cascode amplifier was preferred for its minimal noise figure operation. The g_m/I_d method was employed to determine the optimal bias point and transistor sizing for both stages of the amplifier. Due to the noisy nature of the CMOS environment, the physical properties and the level of inversion of the transistor significantly influence the achievable noise figure. To ensure a noise figure below 1dB for the complete system, minimizing transistor noise is essential, as parasitics beyond our control contribute additional noise later in the design. When picking this bias point and transistor size, it is crucial to find the points that maximize the gain and minimize the noise figure at once. The g_m/I_d method effectively identifies optimal design points by plotting both the cutoff frequency f_t and the ratio $\frac{g_m}{I_d}$ as functions of the overdrive voltage, allowing the designer the ability to determine the overdrive voltage that yields optimal noise and gain performance.

Following the completion of the biasing optimization, the matching circuit was undertaken. This circuit must resonate precisely with the operating frequency for gain and noise performance. In our LNA design, the matching network was configured in a π configuration and placed off-chip due to the large component values.

This off-chip placement also allows for manual adjustments post-production. This was shown in the following sections, in which the network was adjusted to meet the needs of an array coil MRI system without changing any component within the chip. Once all of the design values were set, the chip layout was drawn. While drawing the layout, noise mitigation techniques were implemented. Within these techniques, double contact implementation at the gate connections of the transistors, shielding of RF paths, and compact layout design to minimize additional noise take place.

For the array-coil application, a new design was implemented using a cascode amplifier topology with inductive peaking to meet the unique challenges posed by this system. Unlike the single-coil application, the array-coil system requires the LNA to present an input impedance resembling a short circuit. This specification ensures that the quarter-wave transmission line connecting the LNA to each coil minimizes the current in the coil, effectively reducing mutual coupling between adjacent coils in the array.The cascode stage with inductive peaking was selected as the topology of the array-coil LNA design. Inductive peaking, achieved by incorporating an inductor in between the two stages, helped reduce the input impedance of the amplifier by interfering with the capacitive parasitics that naturally occur in the VHF frequency range of 437 MHz and 447 MHz, where large parasitics from both the SMD inductors and the transistor itself can otherwise degrade the performance. The challenge in this design arose from the necessity of using large SMD inductors for noise matching because its parasitic series resistance posed a significant challenge while performing the required input matching. The resistance introduced by the inductor reflected as a series impedance at the LNA input, and made it difficult to achieve the required open-circuit condition. The inductive peaking technique helped solve this issue. Like the single-coil design, multiple noise mitigation techniques were implemented while drawing the layout. In this design, extra caution was taken to implement low resistance paths at the input and output of the LNA to satify the impedance requirements.

In an RF design, accounting for resistive and inductive parasitics associated with conductive connections during the simulation stage is crucial to achieve a realistic design. Lumped models were added to realize parasitics from bond

wires and external SMD components in the top-level schematic, with the RLC extraction of the layout to achieve the most realistic simulation results. Following this detailed simulation, the performance metrics set at the beginning of the design were successfully met at typical operating conditions. Overall, the work was successful, and it met the goal of designing a CMOS LNA with sub-1dB noise figure performance fit for 10.3 T single and 10.5 T array coil MRI systems. The differential-ended LNA for the 10.5 T application showed significant improvement tin PSRR and proved to be a highly effective solution for 10.5 T array-coil MRI receiver applications.

In the future, the first thing that should be done is to fabricate these chips to obtain real-life measurement results and compare them with the simulation results. An on-chip inductor designed for a high-Q factor spiral inductor at lower frequencies, such as 500MHz, can also be studied. In these designs, most of the noise resulted from the insufficient Q factors of both on-chip and off-chip inductors. Enhancing the performance of the inductors at lower frequencies will also benefit the LNA design.

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