DOKUZ EYLÜL UNIVERSITY

GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

MITIGATION OF DIODE REVERSE RECOVERY CURRENT PROBLEM IN CLASS-D POWER AMPLIFIERS

by

Cankut BEŞER

February, 2019

İZMİR

MITIGATION OF DIODE REVERSE RECOVERY CURRENT PROBLEM IN CLASS-D POWER AMPLIFIERS

A Thesis Submitted to the
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M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"MITIGATION OF DIODE REVERSE RECOVERY CURRENT PROBLEM IN CLASS-D POWER AMPLIFIERS"** completed by **CANKUT BEŞER** under supervision of **PROF.DR. HALDUN KARACA** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

With the constant increase in demand of high efficiency and power density, linear amplifiers are leaving their grounds to the more sustainable switch mode devices. In switching amplifiers, semiconductor switches are used for applying power at determined instances within an on/off action. These switching topologies are called Class-D amplifiers. Class-D amplifiers consist of half or full bridge switch configuration. The input signal is modulated in a high frequency carrier and fed to the power switches. Continuity of output current is provided via an inductive filter. With this technique, energy consumption can be effectively reduced to a fraction, especially in high voltage applications. However, this introduces many challenges to deal such as switching losses, electromagnetic interference and increased system complexity. If the inductor current path contains a silicon diode, these challenges become severe because of the reverse recovery characteristics. This thesis contains practices of high bandwidth current and voltage measurements, various system simulations covering both power and small signal stages and optimization methods for mitigating reverse recovery current related voltage ringing and current spikes.

Keywords: Class-D, amplifier, diode, reverse recovery, snubber

D SINIFI GÜÇ YÜKSELTİCİLERİNDE DİYOT ZIT TOPARLANMA AKIMI PROBLEMİNİN AZALTILMASI

ÖZ

Yüksek verimlilik ve güç yoğunluğu talebindeki artış sebebi ile lineer yükselteçler yerlerini daha sürdürülebilir olan anahtarlamalı tip yükselteçlere bırakmaktadır. Anahtarlamalı yükselteçler, gücün belirli zamanlarda aktarılması için açık ve kapalı olarak çalışan yarı iletken anahtarlar kullanır. Bu anahtarlamalı topolojilere D Sınıfı yükseltici denmektedir. D sınıfı yükselticiler tam köprü veya yarım köprü konfigürasyonlarını kullanmaktadır. Giriş sinyali yüksek frekanslı bir taşıyıcı ile modüle edilerek çıkış güç anahtarlarını sürmektedir. Çıkışın sürekliliği endüktif bir filtre ile sağlanmaktadır. Bu teknik sayesinde güç tüketimi, özellikle yüksek voltajlı uygulamalarda çok düşük değerlere çekilebilmektedir. Ancak bu anahtarlama kayıpları, elektromanyetik girişim ve devre karmaşıklığı gibi birçok sorunu beraberinde getirmektedir. Endüktör akım yolu bir silikon diyot barındırıyorsa bu sorunlar zıt toparlanma karakteristiği sebebi ile ciddi bir hal almaktadır. Bu tez yüksek bant genişliğinde akım ve voltaj ölçümü pratikleri, güç ve sinyal katlarını kapsayan çeşitli simülasyonlar ve zıt toparlanma akımı kaynaklı voltaj ve akım tepelerinin azaltılmasına yönelik optimizasyon yöntemleri içermektedir.

Anahtar Kelimeler: D-Sınıfı, yükselteç, diyot, zıt toparlanma, bastırıcı

CONTENTS

Page

LIST OF FIGURES

Page

LIST OF TABLES

Page

CHAPTER ONE
CLASS-D AMPLIFIERS

1.1 Introduction

In the early years of electronics, amplification devices were made of vacuum tubes. These devices were extremely versatile however, large size, power dissipation and high cost forced the amplifier technology to evolve into another form; bipolar junction transistor (BJT). BJTs opened a whole new era in the means of compactness and efficiency. Unfortunately, linear transistor-based amplifiers were still dissipating a lot of heat. This is a major concern, especially in battery operated systems. To overcome this issue, transistors are forced to work in such a way that they can only have two distinctive states; cut-off and saturation. In this way, high current flow is limited to the area where the transistors have the least voltage drop. This is the main principle of Class-D amplifiers. The input signal is modulated with a high frequency carrier into a pulse width modulated form (Figure 1.1) and only the required amount of power is delivered to load (Cordell, 2011). In this way, conduction losses are effectively minimized since the transistors only operate in fully blocking or fully conducting regions.

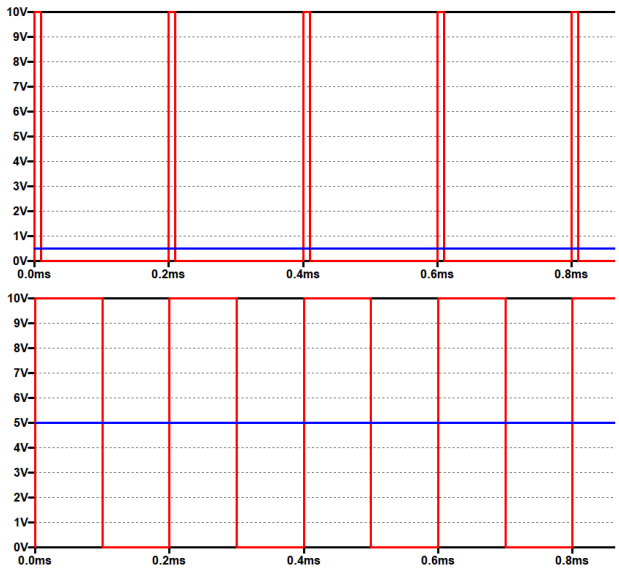


Figure 1.1 Example of PWM waveform (red) and it's averaged value (blue). Top waveform is at %5, bottom waveform is at %50 duty cycle

Successive to the modulation, the output signal is filtered via a filter network, which consists of reactive components. After the filtering, observed output waveform is a clear amplified reconstruction of the input signal.

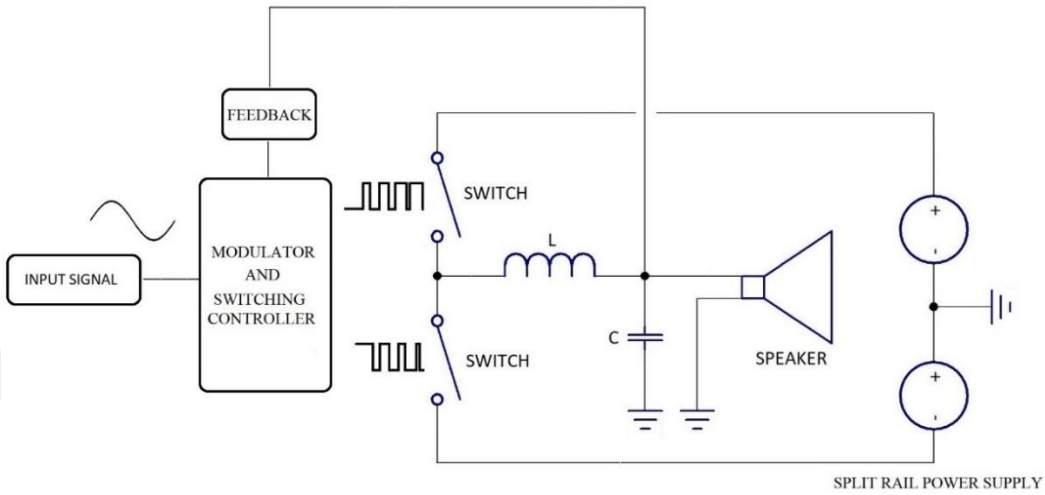


Figure 1.2 Basic block diagram of Class-D amplifier

On principle, everything seems extraordinarily beneficial. Nevertheless, addition of the high frequency carrier and use of magnetic filtering components end up with additional switching losses. Furthermore, fast transitioning signals are greatly contributing electromagnetic compatibility problems, since the high frequency components are now causing the circuit to act as an antenna. The situation becomes more severe for both of the cases when a power diode, which contains reverse recovery charge is introduced to the system. If the diode current is interrupted by forced turn-off, reverse recovery charge causes a narrow, high amplitude current spike. The spike's amplitude may exceed the power switch's maximum current specifications. On the other hand, high $\frac{dI}{dt}$ rate with the combination of circuit parasitic inductances may result in a voltage build up which is greater than the maximum withstanding voltage of the component. Both cases can cause the power switch to eventually fail.

1.2 Class- D Amplifier Basics

Electronic amplifiers can be separated into two subgroups; linear amplifiers and switching amplifiers. In linear amplifiers, power transistors always work in linear region and act as variable resistors, therefore dissipating the excessive energy as heat. Linear designs can be categorized as classes A, B, AB, C and G types (Cordell, 2011). Class-D amplifiers on the other hand, employ a different working principle to overcome excessive heat dissipation. In Class-D operation, power switches are always operated in cut-off or saturation regions. Since the switches are fully blocking or fully conducting, $IxV_{TRANSISTOR\ DROP}$ losses are effectively minimized. To achieve this, the input signal is modulated with a scheme called Pulse Width Modulation (PWM). The modulator stage consists of a comparator and a triangle wave generator. Input signal is compared with a fixed frequency triangle wave. The next, modulated signal is fed to the switching controller, where a complementary signal and desired dead times are introduced. Then, the modulated signal pair is fed to the power switches where the input signal is amplified to the power supply voltage. The final PWM output is then filtered via a low pass LC network, which provides the final sinusoidal waveform. Additionally, a feedback mechanism is also included to avoid signal distortions.

To accommodate continuous demand for energy efficiency and high system density, Class-D amplifiers are becoming the dominant choice of selection for audio market. By using switching topology over the linear type, system efficiency can be dramatically increased. Efficiencies up to %95 can be obtained (Bakker & Duffy, 2017) in properly evaluated system designs. High efficiency results in smaller heat sinking requirements, therefore shrinking the system volume. Designs can be made even more compact by increasing the switching frequency. Higher frequencies require physically smaller filtering components, however, switching losses may become dominant after a certain limit, which defies the primary advantage of the Class-D amplifiers. This concludes to a point that, reducing the switching losses and component stress is a mandatory for high frequency devices in order to keep the efficiency advantage over linear amplifiers.

1.3 Class-D Amplifier Topologies

Class-D amplifier topologies can be separated into two subgroups. These are the half and full bridge architectures.

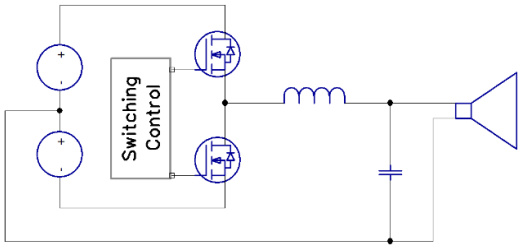


Figure 1.3 Half bridge Class-D amplifier diagram

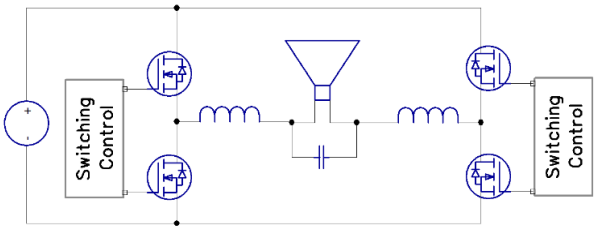


Figure 1.4 Full bridge Class-D amplifier diagram

Both types have their own advantages. In general, full bridge architecture is better for audio applications with better linearity however, system complexity and silicon cost are much higher compared to the half bridge (Cerezo, n.d).

Table 1.1 Half and full bridge topology comparison (Cerezo, n.d)

	Half Bridge	Full Bridge
Power Supply	Split Rail	Single Rail
Current Rating	1	2
Power Switches	2	4
DC Offset	Adjustment needed	Can be cancelled out
PWM Pattern	2 Level	3 Level can be implemented
Current Pumping to Source	Exists	Can be eliminated

CHAPTER TWO
POWER SEMICONDUCTORS

2.1 Power Switch Considerations

The most important component of an amplifier is the switching device. In order to have a robust yet efficient system, power switch selection should be carefully evaluated. There are a variety of power switches available on the market, most common ones are:

- Bipolar junction transistor
- Insulated gate bipolar transistor
- Metal oxide semiconductor field effect transistors

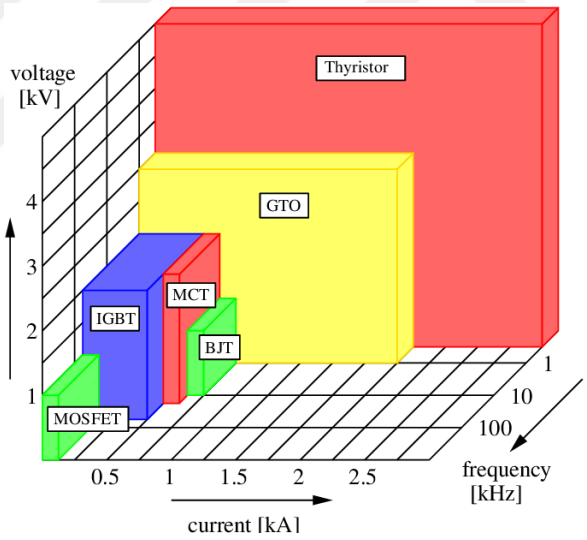


Figure 2.1 Power semiconductor drive capability chart (Sütő & Nagy, 2007)

To provide an efficient solution, there are two key parameters that should be taken in to account:

- Switching transition times
- Saturation voltage / on resistance

In general, MOSFETs are the preferred device for the modern amplifiers, since they are superior in switching speed compared to IGBTs (Figure 2.1), and easier to drive compared to bipolar junction transistors. MOSFETs can be used for switching applications up to 1MHz and manufacturers offer a variety of devices, which have up to 4700V breakdown voltage (IXYS, 2016). This range covers almost all audio applications.

2.2 Power MOSFETs

In most modern amplifier applications, power MOSFETs are the choice of selection over the other power switch types. There are several parameters that make the MOSFETs desirable. These are:

- Integrated body diode, avoids additional component cost
- Majority carrier device, faster operation
- Low $R_{DS\ (on)}$
- Positive temperature coefficient
- Bidirectional current flow

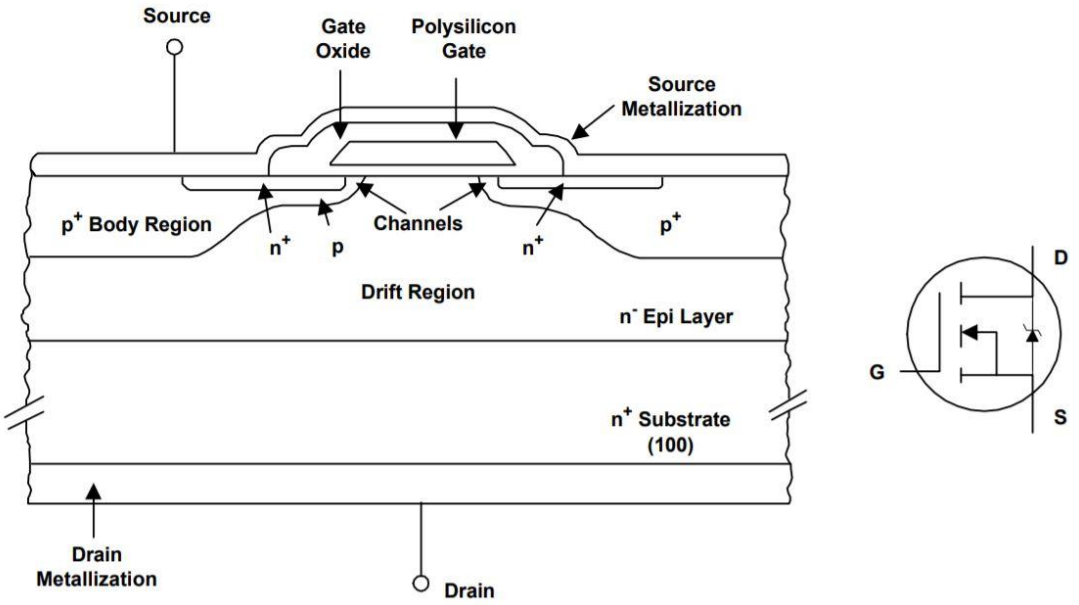


Figure 2.2 Schematic diagram of an N channel power MOSFET **(**Barkhordarian, n.d)

Figure 2.2 shows the basic structure of a power MOSFET. Current begins to flow when the gate potential reaches a threshold level and starts to invert the P doped channel to N channel by attracting the minority carriers. A channel of carriers forms and allow current to flow between source and drain terminals. However, this structure accommodates some parasitically occurring components, shown in Figure 2.3.

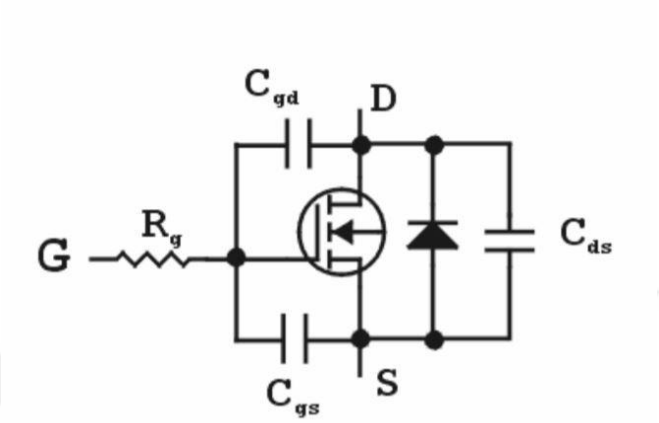


Figure 2.3 Parasitic components of power MOSFET (Sattar, n.d)

Most important one of these parasitic components is the parasitic source drain diode. This diode can be effectively used for conducting the freewheeling current, therefore reducing the component count and overall system cost. Class-D amplifiers are one of these circuits that require freewheeling diodes because of the output filter inductor and inductive speaker forces the current to flow after switch turn off event; resulting in high voltage peaks, breakdown and therefore destruction of power switch if proper re-circulation path is not available.

To provide this path, internal parasitic diodes are used as a common practice. MOSFETs are bi-directional devices that can conduct both forward and reverse current. While switching between high and low side MOSFETs, an additional dead time insertion is required for preventing shoot-through current. First, internal diode automatically catches the freewheeling current immediately after the induced voltage reaches to its forward voltage. Next, dead-time ends and corresponding MOSFET turns on which bypasses the diode current, leading to efficient operation in cases where low $R_{DS\ (on)}$ component are in use. Current circulation cycles of the Class-D amplifier are shown in Figures 2.4, 2.5 and 2.6.

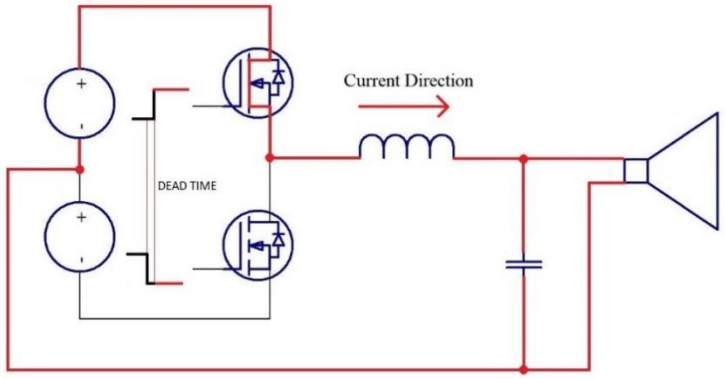


Figure 2.4 Half bridge Class-D amplifier current path; high side MOSFET is on

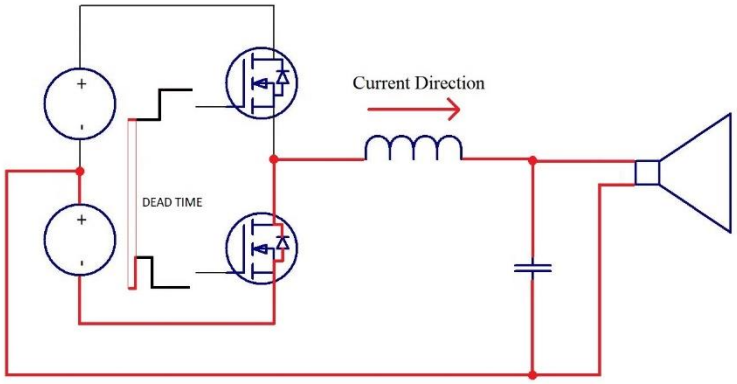


Figure 2.5 Half bridge Class-D amplifier current path; during dead-time insertion

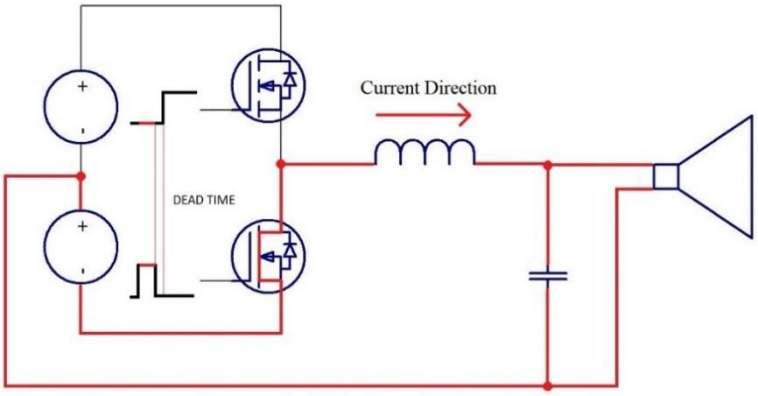


Figure 2.6 Half bridge Class-D amplifier current path, low side MOSFET is on

2.3 P-N Junction Diode Reverse Recovery

Diodes are semiconductor devices that are primarily used for conducting current in one, pre-determined direction. There are many types of diodes with different characteristics. For power amplifier applications, following diode types are commonly used:

- P-N Junction Diodes
- Schottky Diodes
- Silicon Carbide Schottky Diodes

As the most important parameter, component cost is the main selector for many mass production devices. This fact leads the designers to use MOSFET switches and their integrated diodes for system budget reduction. However, P-N junction diodes are notorious for their reverse recovery charge. The reverse recovery current, if estimated improperly, derate the device parameters and leads to the destruction of power semiconductors. Apart from the catastrophic failures, reverse recovery current is also contributing to switching losses and EMC problems (Williams, 2001).

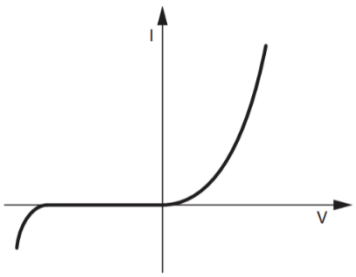


Figure 2.7 Diode V-I characteristics (Vishay, 2011)

Under static operating conditions where the current path contains fully resistive elements, diodes follow their characteristic curve. However, if the diode is used in hard commutating topologies where the existing diode current is interrupted by the forced turn-off, reverse recovery charge causes a short-circuit like behavior until the minority carriers are completely discharged.

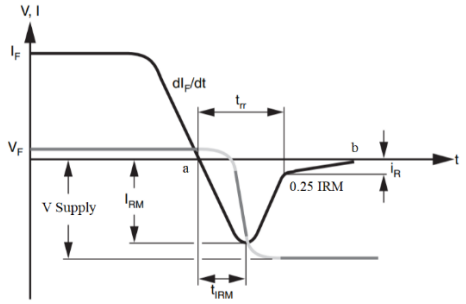


Figure 2.8 V-I waveforms during diode turn- off phase (Vishay, 2011)

Reverse recovery time can be defined as the time-lapse until the reverse recovery current reaches to the 0.25 of the initial IRM peak as shown in Figure 2.8. Q_{rr} can be defined as:

$$Q_{rr} = \int_a^b I_F\,(t).\,dt \tag{2.1}$$

Reverse recovery charge Q_{rr} is related with the die geometry. High voltage diodes that incorporate wide drift regions (Power Integrations, 2011) contain more minority carriers in forward bias mode. Apart from that, die area is also directly proportional to the rated current. Therefore, high power rated diodes have the most reverse recovery charge, which means larger current spikes.

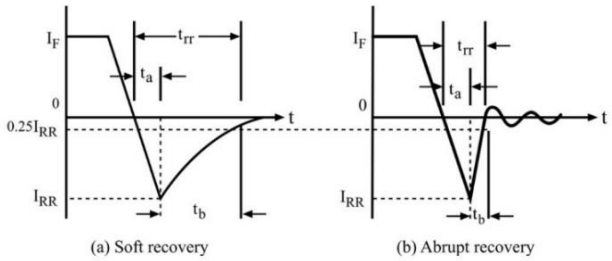


Figure 2.9 Reverse recovery types, (a) soft recovery, (b) abrupt recovery (Allaboutcircuits, n.d)

The reverse recovery action can actualize in two distinctive patterns as shown in Figure 2.9. These are called the soft recovery and abrupt recovery. Softness Factor is defined as RSF = $\frac{tb}{ta}$ (AN-301, n.d). If RSF > 1 the diode can be classified as soft recovery. Abrupt recovery type diodes should be avoided, since they cause oscillations and EMC problems (Williams, 2001).

2.4 Simulations

To reveal the problems associated with reverse recovery charge, the circuit was simulated by using LTspice. The simulation circuit is a clamped inductive load that consists of two N type MOSFETs, where the top MOSFET was operated as freewheeling diode by shorting the gate pin to its source pin. Load is a 100μH inductor. Gate of the bottom MOSFET was excited by using a double pulse sequence in order to observe the reverse recovery current peak.

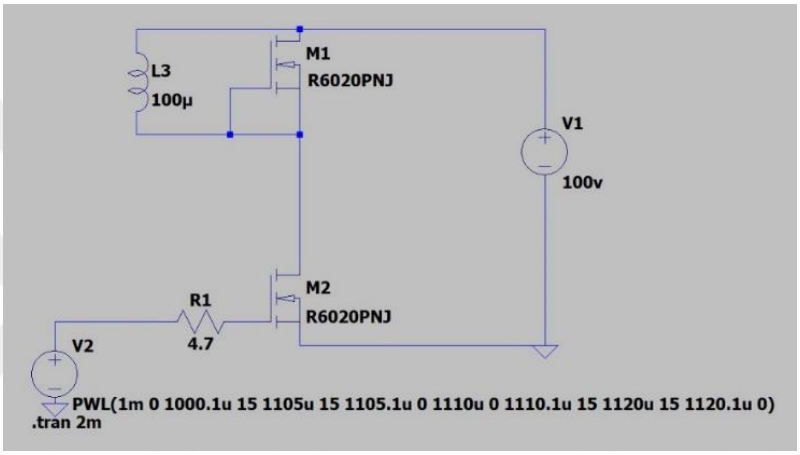


Figure 2.10 Simulation circuit for clamped inductive load test

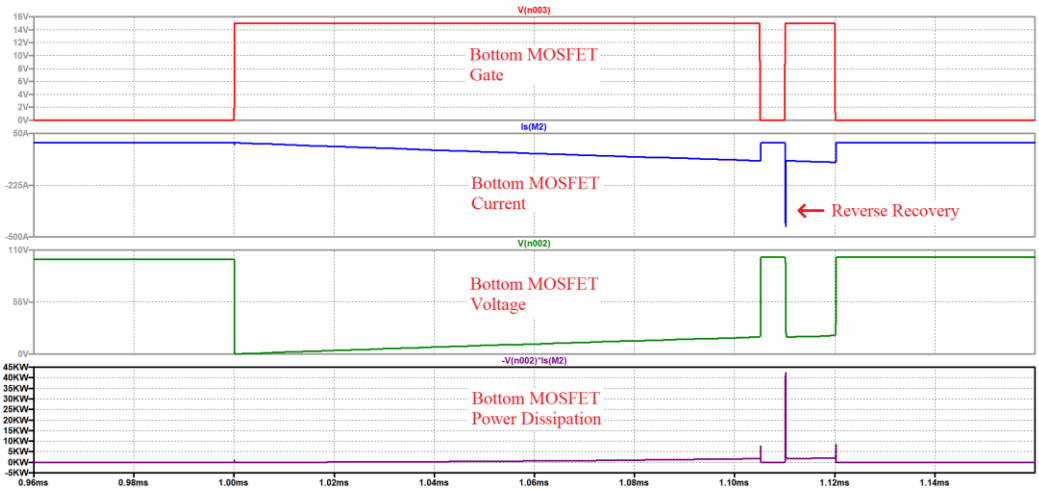


Figure 2.11 Simulated waveforms of gate signal (purple), low side MOSFET drain- source voltage (red), low side MOSFET current (blue) and low side MOSFET power dissipation

The first pulse applied to the low side MOSFET turns the transistor on, causing the inductor to charge for the given period. Next, low side MOSFET turns off, top side MOSFET's parasitic diode becomes forward biased and automatically provides a path for inductor current. When the second pulse is applied, low side MOSFET turns on, forcing the top side MOSFET's diode to turn off. This event starts to discharge the minority carriers present in drift region, causing a sharp current spike, which is called the reverse recovery current. Generally, this current is much higher compared to the MOSFET's nominal operating current. In addition, the current overlaps with the MOSFET's drain- source voltage, which causes a very high-power dissipation, in the orders of Kilo Watts for a short period of time. This may cause device failures, especially in physically small packages.

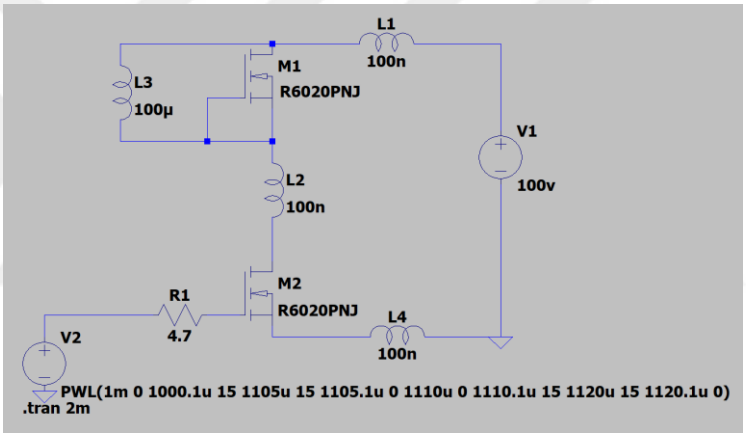


Figure 2.12 Simulation model of clamped inductive load test circuit, including parasitic inductors

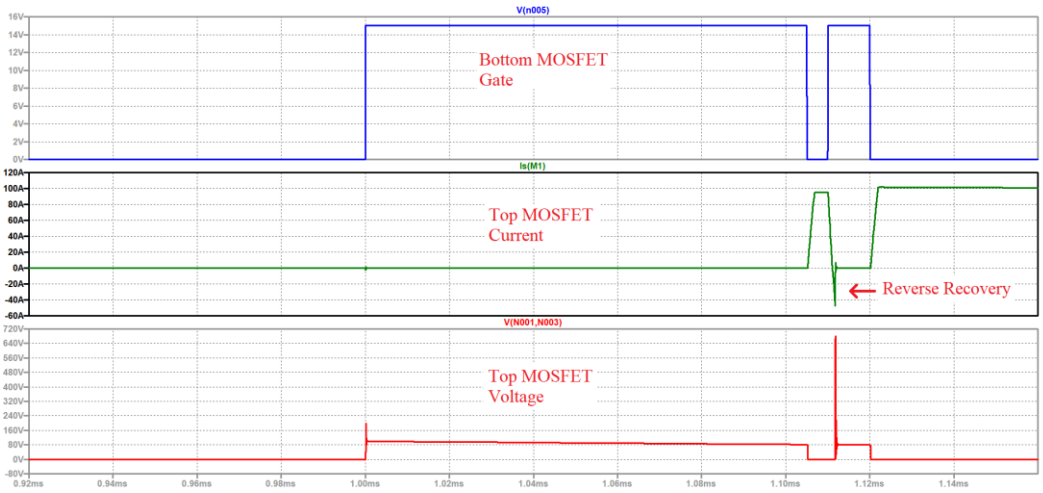


Figure 2.13 Simulated waveforms of bottom MOSFET gate (blue), top MOSFET current (green), top MOSFET drain- source voltage (red)

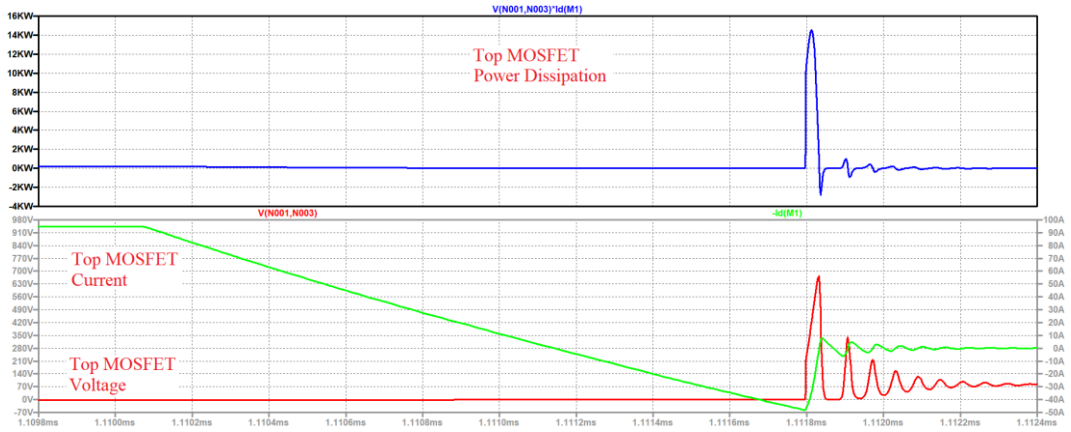


Figure 2.14 Simulated waveforms of reverse recovery zone. Top MOSFET current (green), top MOSFET drain- source voltage (red), top MOSFET power dissipation (blue)

If parasitic inductors are added to the simulation, it reveals a far worse issue. The amplitude of the reverse recovery current is limited by the parasitic components however, it excites the resonant circuit consisting of MOSFET's C_{OSS}, $L_{PARASITIC}$ and MOSFET's $R_{DS\ (on)}$, resulting in high voltage peaks on C_{OSS} that may violate the limiting device parameters and causes breakdown. This can be mitigated by increasing the damping ratio (Cree, 2013).

Natural frequency of the resonant circuit:

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{2.2}$$

Damping ratio for the formed RLC Circuit:

$$\zeta = \frac{\mathrm{R}}{2}\sqrt{\frac{C}{L}} \tag{2.3}$$

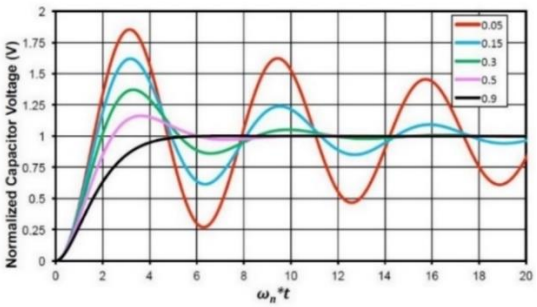


Figure 2.15 Normalized capacitor voltage vs ω_n* t for various ζ (Cree, 2013)

2.5 Class-D Amplifier, Power MOSFET Losses

Since the system is a switching topology, there are two types of losses that should be considered. These are the conduction and switching losses. Conduction loss is also called I^2R loss, as it is directly proportional to MOSFET's $R_{DS\ (on)}$. Modern transistors incorporate significantly lower values of $R_{DS\ (on)}$, starting from several milliohms to as low as 0.001Ω range, depending on the specified voltage. Switching losses are one of the major concerns that should be considered. This type of loss is related with many factors including transition times, switching frequency, switch voltage, switch current and the reverse recovery charge (Cerezo, n.d).

$$\text{Total Switching Power} = P_{Sw} + P_{Gate} \tag{2.4}$$

$$P_{Gate} = 2 * Q_G * V_{Driver} * F_{Sw} \tag{2.5}$$

$$P_{Sw} = E_{SW} * F_{SW} \tag{2.6}$$

$$E_{SW} = \int_0^t V_{DS}(t) * I_D(t)\, dt \tag{2.7}$$

Q_G: MOSFET gate charge

V_{Driver}: Gate drive voltage

F_{Sw}: Switching frequency

V_{DS}: MOSFET drain source voltage

I_D: MOSFET drain current

E_{Sw}: Switching Energy

P_{Sw}: Total switching power loss

P_{Gate}: Gate power loss

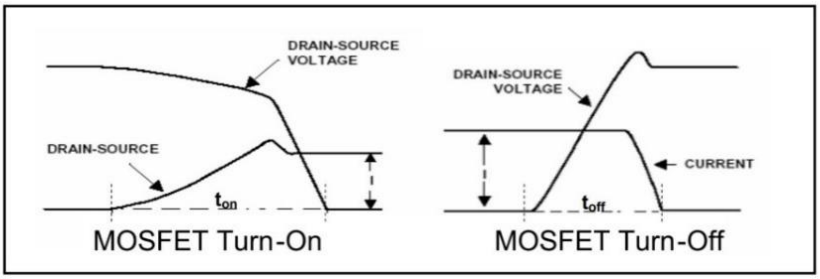


Figure 2.16 MOSFET transition characteristics (Cerezo, n.d)

Total switching power loss can be defined for a Class-D amplifier MOSFET as (Cerezo, n.d):

$$P_{Sw} = \left[0.5 \times I_D \times V_{Bus} \times \left(t_r + t_f\right) \times F_{Sw}\right] + \left[0.5 \times C_{oss} \times {V_{bus}}^2 \times F_{SW}\right] + [K \times 0.5 \times Q_{rr} \times V_{bus} \times F_{SW}] \quad (2.8)$$

$$K = \frac{Qrr(T_{JUNCTION})}{Qrr(125℃)} \quad (2.9)$$

I_D: Drain Current

V_{bus}: Supply Voltage

F_{Sw}: Switching Frequency

t_r: Rise Time

t_f: Fall Time

Qrr: Reverse Recovery Charge

C_{oss}: MOSFET output capacitance

K: Constant, specific to device parameters (STMicroelectronics, 2017)

CHAPTER THREE
EXPERIMENTAL STUDIES

3.1 Double Pulse Testing

Diode characteristics can be measured by clamped inductive switch testing (Jahdi, 2016). In order to measure the reverse recovery behavior of the diodes, test setup should operate under heavy current loading to reach the specified Q_{rr}. With proper thermal design, this seems like an easy task, however, large heatsink area disturbs the optimal layout rules, which ends up creating large current loops. This act results in increased parasitic inductance and makes the measurement results unreliable. To overcome this issue, a method called “Double Pulse Testing” was considered; which can be used to replicate the diode behavior at peak pulsed power levels (Schimel, 2016) and a special signal generator board was designed and realised by using Diptrace software. This method uses standard clamped inductive switch testing setup. Two successive pulses are applied to the gate of the low side MOSFET. First pulse charges the inductor to the specified current rating. Then the low side MOSFET turns off to allow high side MOSFET’s body diode to handle the freewheeling current. Next, another pulse is applied, turning the low side MOSFET on and causing the reverse recovery current to flow in a shoot through manner. The proposed action is controlled as a one-time event, which greatly removes the thermal stress of the switching components and reduces heatsinking requirements.

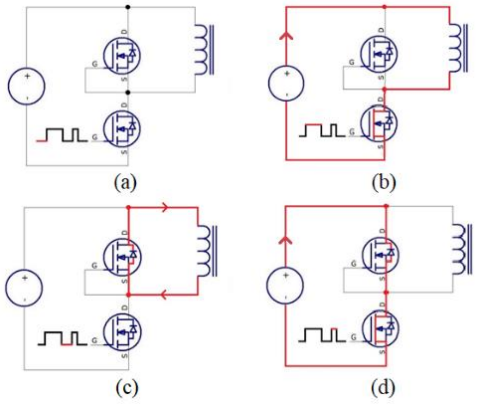


Figure 3.1 Current circulation paths of double pulse test setup, (a) initial state, (b) charging the inductor, (c) freewheeling over the body diode, (d) reverse recovery

3.1.1 Implemented Double Pulse Test Circuit Schematics

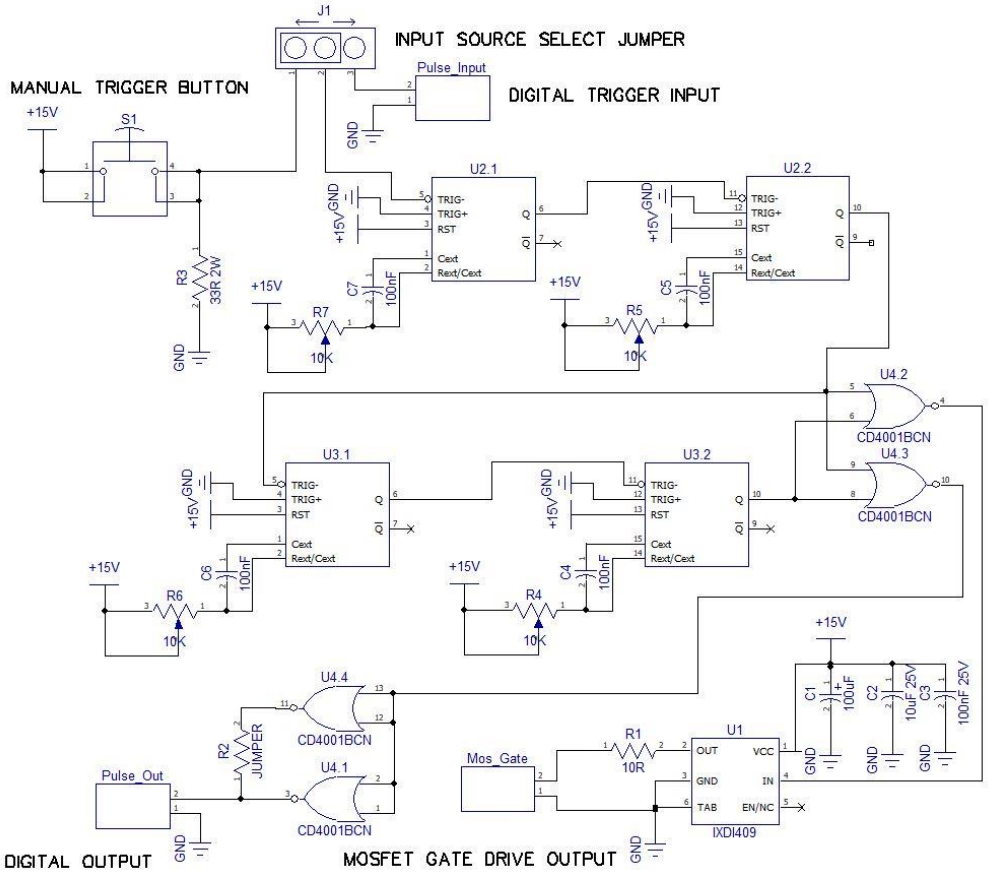


Figure 3.2 Designed double pulse test circuit signal block schematics

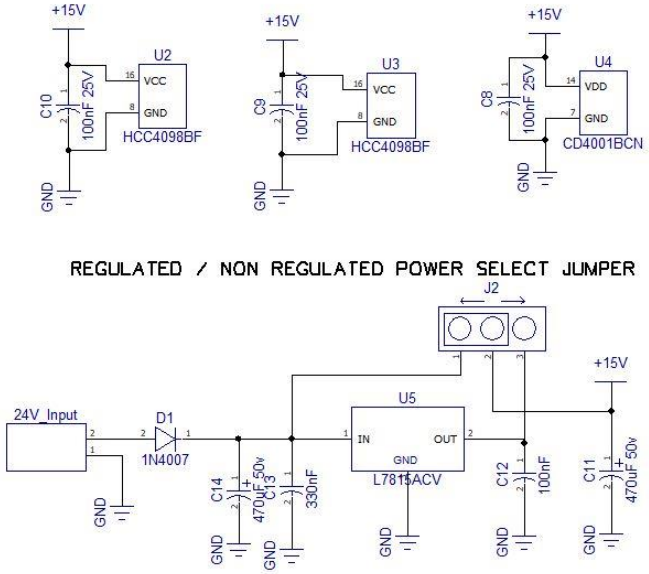


Figure 3.3 Designed double pulse test circuit power supply schematics

3.1.2 Circuit Operation

Designed circuit uses 4098 type multivibrator integrated circuits to create adjustable on and off time double pulse waveform (Schimel,2016). Multivibrators operate in monostable mode and outputs single pulse after every triggering action therefore, a dedicated monostable block is required for each adjustable time step. All the blocks are connected a in daisy chain configuration, which makes them sequentially triggered.

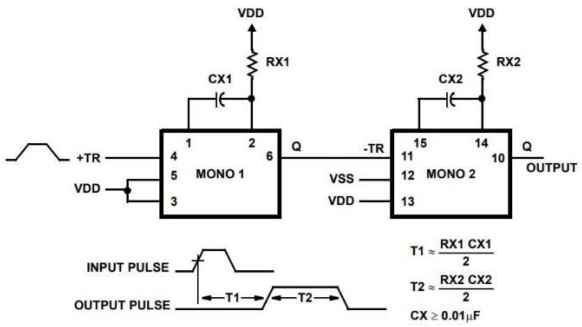


Figure 3.4 Application example from CD4098 datasheet (Intersil, 1992)

The circuit of prototype double pulse tester allows precise timings to be controlled by adjusting the value of charge resistors. In realization, multiple turn trimmers are used to make the system re-adjustable. In addition to pulse shaping circuit, a separate gate driver IXDI409 was included, making the circuit suitable for driving discrete power transistors without additional gate drive setup.

R4, R5, R6, R7 trimmers provide precision adjustment for corresponding timings while C4, C5, C6 and C7 are used for timer capacitors. Button S1 is used as the manual operation button. In addition to this mode, circuit can be operated periodically by using pulse input connector and adjusting input source select jumper. CD4001 Nor gate was configured as an or gate that provides the required combinational logic to construct the double pulse shape. D1 provides reverse polarity protection on the input power supply. 7815 was used as the main regulator which provides regulated +15V to both logic and MOSFET driver. J2 provides an option to by-pass the on-board regulator.

3.1.3 Implemented Double Pulse Test Circuit Layout

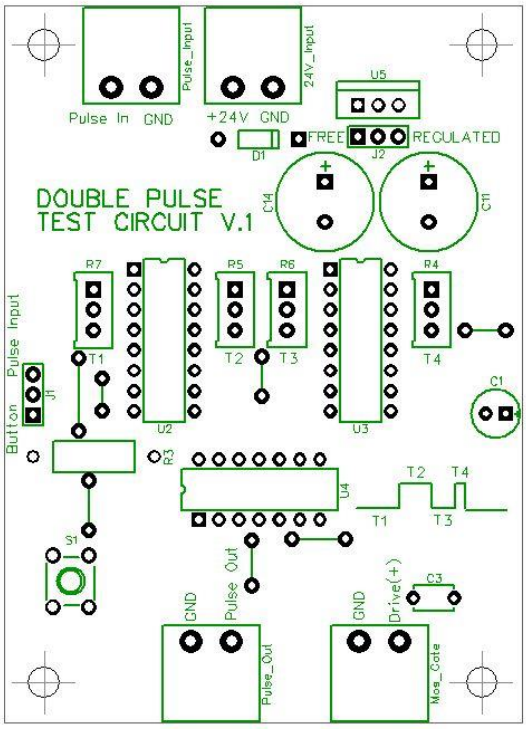


Figure 3.5 Double pulse test circuit top side PCB layout design

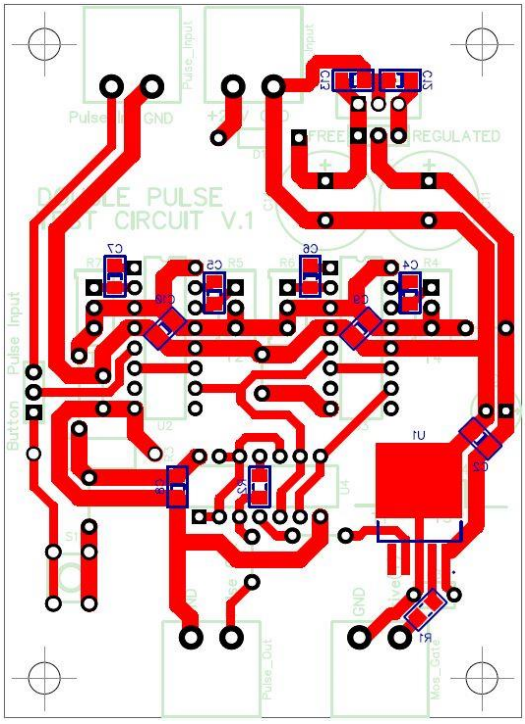


Figure 3.6 Double pulse test circuit bottom side PCB layout design

3.1.4 Implemented Double Pulse Test Circuit PCB Assembly

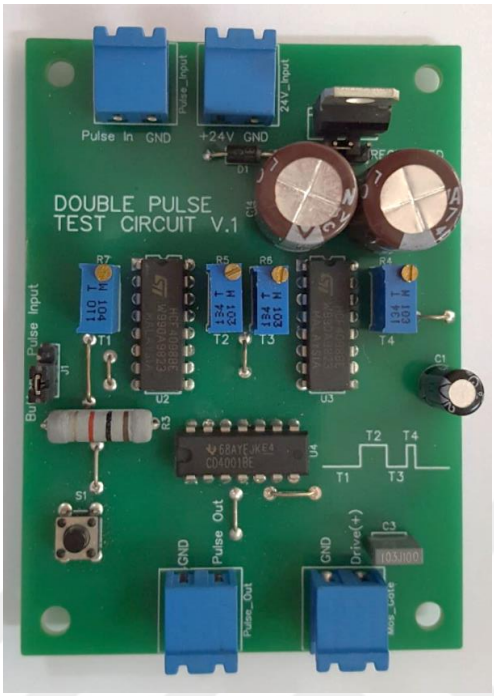


Figure 3.7 Realised double pulse test circuit top side components assembly (Personal archive, 2018)

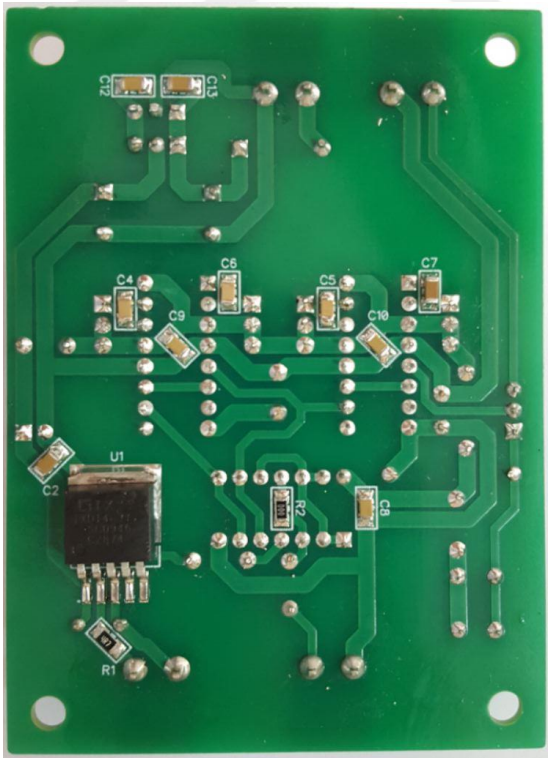


Figure 3.8 Realised double pulse test circuit bottom side components assembly (Personal archive, 2018)

3.1.5 Functionality Testing

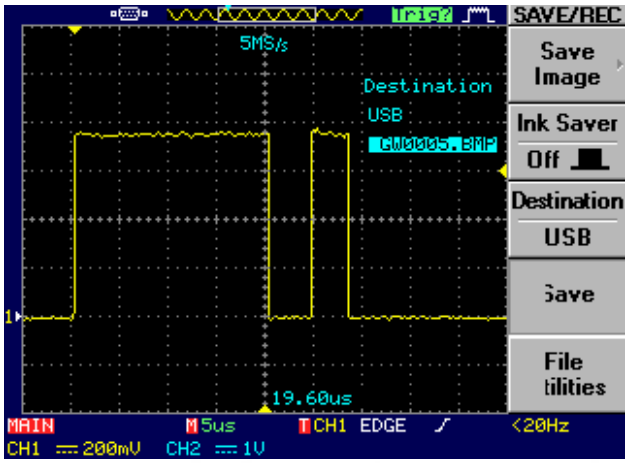


Figure 3.9 Output voltage waveform of the realized double pulse test circuit (Waveform was captured by using oscilloscope in single pulse triggered mode)

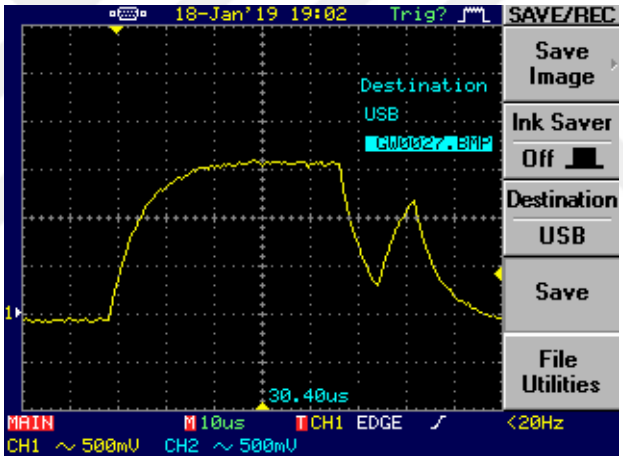


Figure 3.10 Output waveforms of double pulse test circuit with heavy capacitive loading ($1\mu F$) on the MOSFET driver output

Practical testing shows that minimum pulse width is limited to 3 microseconds. The circuit reliably operates beyond this limit. On the other hand, MOSFET's gate charging time should be considered before testing, since the output may not remain active enough to charge or discharge the gate completely. An extreme case for this situation is shown in Figure 3.10, which can result in catastrophic failures. Unfortunately, wires from board to test unit (MOSFET) introduces uncontrollable parasitic inductances to the gate drive path that causes oscillations. Therefore, the circuit was dedicated to use as a signal generator only.

3.2 Designed Class- D Amplifier Circuit

Switching amplifier design is a major challenge, since switching characteristics are dependent on environmental factors such as parasitic components, which can have dramatical effects on the device operation. With careful design, these factors can be eliminated up to a certain point. However, verifying the effectiveness of this design may require some special measurement techniques, especially in high dv/dt and high di/dt systems. In addition, high amplitude currents and voltages combined with high frequency components generally require sophisticated measurement equipment. In order to create a test bed and measure the influence of various combinations of both controlled and environmental variables on the circuit operation, a "Class-D Amplifier Test Board" was designed and prototyped. Circuit and layout design were performed in Diptrace software. Designed circuit is a compact Class-D amplifier power stage which is suitable for high voltage and current operation. The board design incorporates an isolated gate driver and floating gate drive supplies to reduce the noise coupling to the gate drive signals. Layout design was intended to have minimal parasitic inductance to ensure reliable measurements. Moreover, a resistor based current measurement block with co-axial output connector was included to provide interference free high frequency measurement. Specifications of the board is listed below:

- Resistor based current sense block with 50A/30A maximum continuous current (0.001Ω / 0.01Ω sense resistor). 50Ω output impedance
- 200V Maximum DC-Bus Voltage
- Up to 5740µF DC-Bulk Capacitance (can accommodate seven 820µF capacitors)
- Fully isolated gate drive circuit with 4A gate drive capability
- Operates with dual floating power supplies on the gate driver side
- Optional RCD turn-off (Todd, 1993) and DC-Bus snubber component patterns are included in the layout to test the circuit behavior with respect to different configurations
- Optional solder bridge areas to populate externally connected air core inductors to test parasitic effects

3.2.1 Implemented Class-D Amplifier Test Board Schematics

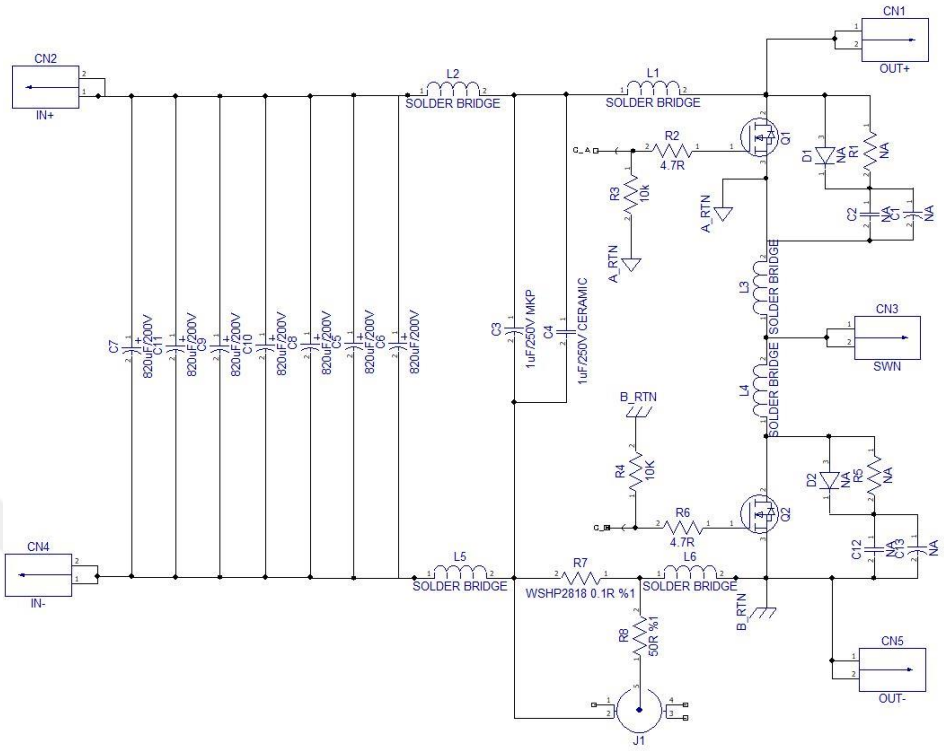


Figure 3.11 Circuit diagram of the Class-D amplifier test board's power block

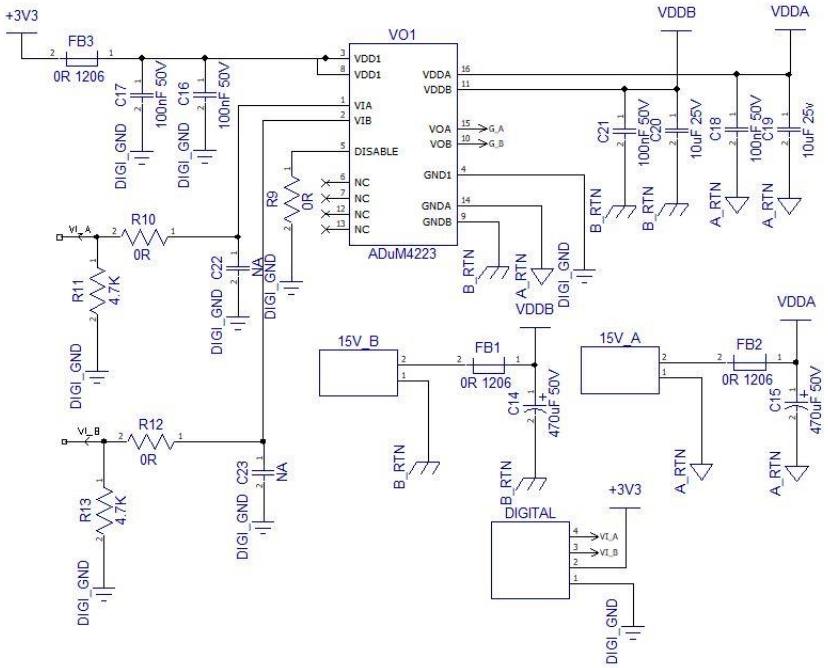


Figure 3.12 Circuit diagram of the Class-D amplifier test board's isolated gate driving circuit

3.2.2 Circuit Operation

Test circuit is a simple switching cell which contains a MOSFET pair with their corresponding gate driver, bulk capacitors, a current sensing layout and optional snubber components. For high noise immunity, ADUM4223 (VO1) from Analog Devices was used as the gate driver, which provides galvanic isolation between all channels and the input. For MOSFETS Q1 and Q2, 2SK3131 from Toshiba Semiconductors was used. An optional, dedicated turn-off snubber is included with each MOSFET to help mitigating the voltage peaks. Current sense circuit consists of a current sense resistor (WSHP2818R0100FEA), a 49.9Ω termination Resistor and an SMA connector to provide extra noise immunity. C5, C6, C7, C8, C9, C10, C11 bulk capacitors were used for reducing the DC-Bus voltage ripples. Addition to these, low ESR MKP and Ceramic DC-Bus snubber capacitors were used and populated near switching devices to cancel out the DC-Bus parasitic inductances. Optional turn-off snubber components D1, C1, C2, R1 and D2, C12, C13, R5 were also included in schematic. The Digital input connector is attached to external 3.3V-5V power supply and provides power to the isolated signal side of the ADUM4223. R11 and R13 pull down resistors are included to pull the inputs to low level in case of a wire break. R10, C22 and R12, C23 RC filters are placed in schematics as optional low pass filters to suppress possible input glitches. 15V_A and 15V_B connectors are attached to external lead-acid batteries to provide noise free power for gate drive side of the ADUM4223. L1 to L6 patterns were included to provide a connection port for air core inductors to simulate the behavior of the trace parasitic inductances (Chen, 2013).

3.2.3 Implemented CLASS-D Amplifier Test Board PCB Layout

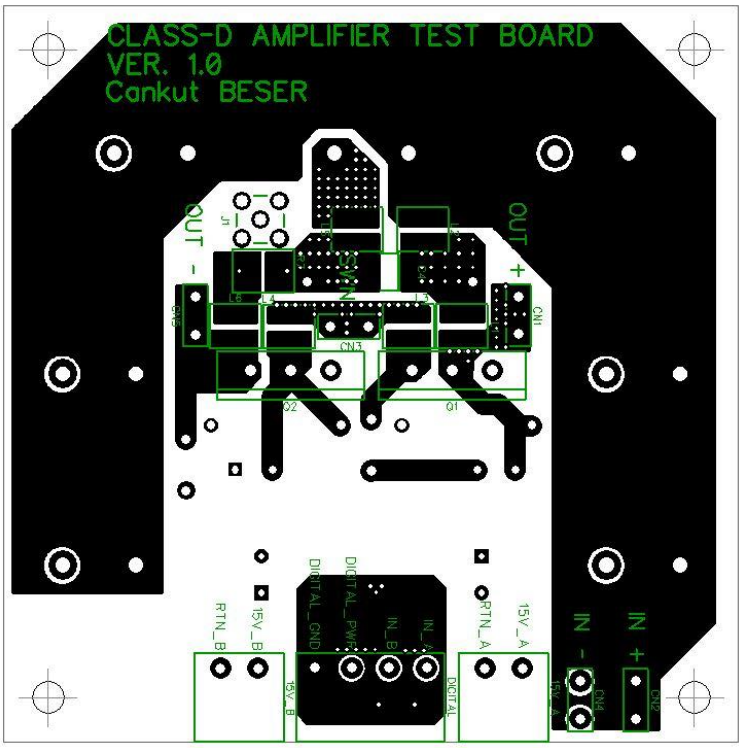


Figure 3.13 Class-D amplifier test board top side PCB layout design

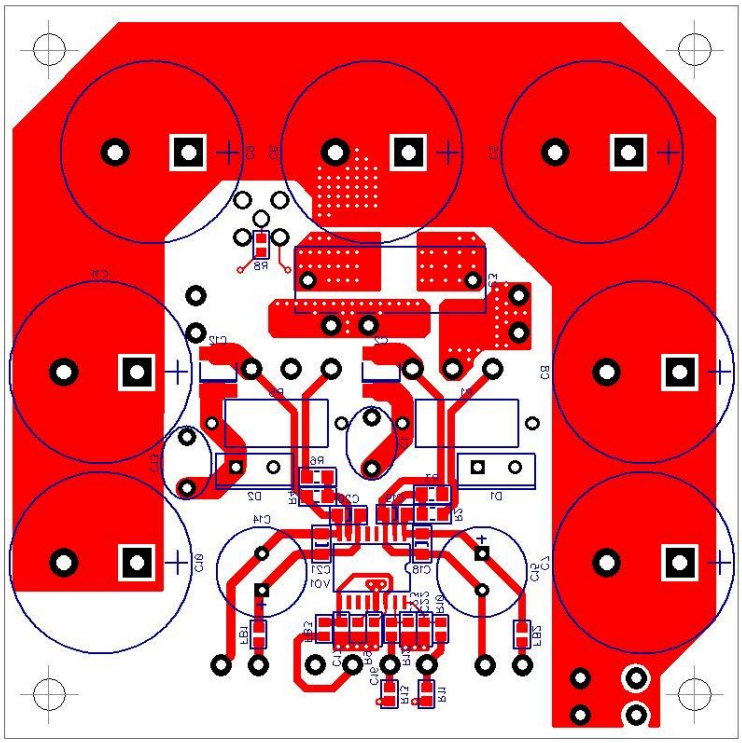


Figure 3.14 Class-D amplifier test bottom side PCB layout design

3.2.4 Implemented CLASS-D Amplifier Test Board PCB Assembly

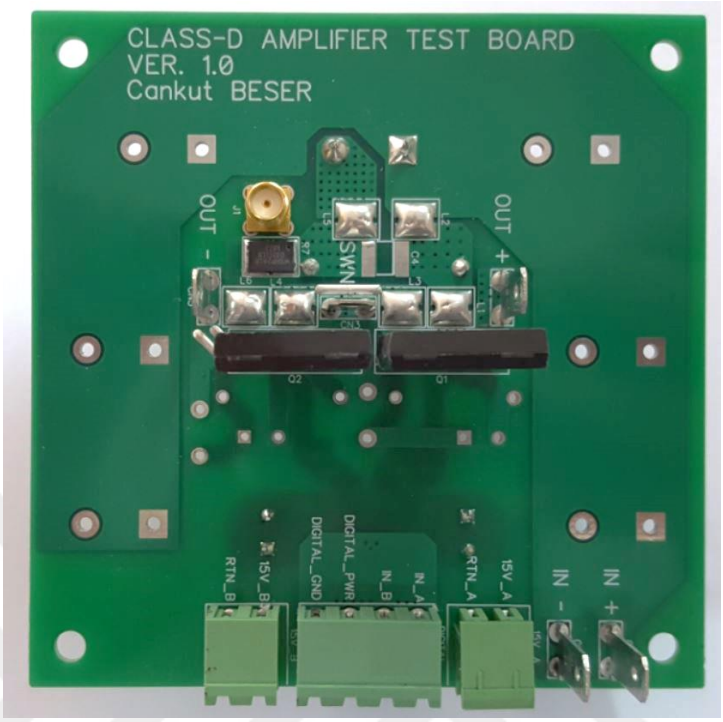


Figure 3.15 Implemented Class-D amplifier test top side component assembly (Personal archive, 2019)

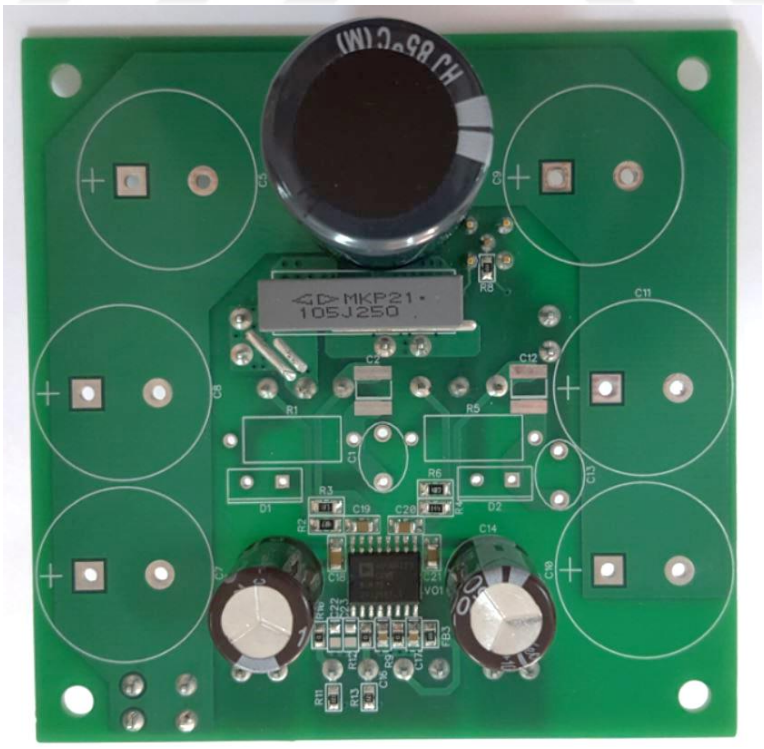


Figure 3.16 Implemented Class-D amplifier test bottom side component assembly (Personal archive, 2019)

3.2.5 PCB Layout Considerations:

Main objective of the layout design is to minimize the parasitic inductance build up. In any application, supply and return currents flow in a loop.

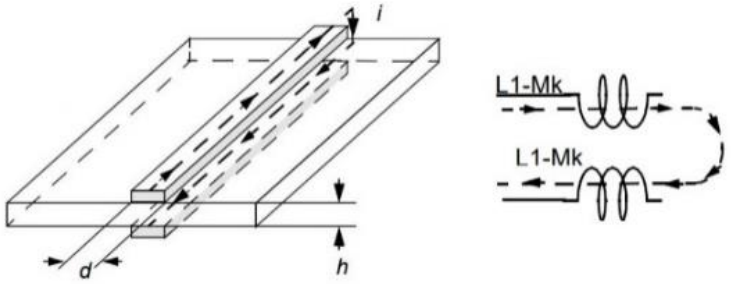


Figure 3.17 Trace and inductance model (Atmel, 2003)

If the current paths are identical, total inductance (Lt) of the loop can be written as (Atmel, 2003):

$$Lt = 2x(L1 - Mk) \tag{3.1}$$

Where Mk is the mutual inductance. If the coupling coefficient is unity, then the mutual inductance is equal to the trace inductance. This results the loop inductance to become 0. Therefore, to reduce the loop inductance, mutual inductance should be maximized by routing the traces in proximity and increasing the coupling coefficient. Another way to reduce the inductance is to increase the trace width (Atmel, 2003).

$$Lt(\mu h) = 0.2 * L * Ln\left(\left(\frac{2*L}{d+e}\right) + 0.5 + 0.22 * \frac{d+e}{L}\right) \tag{3.2}$$

e: PCB trace thickness in mm, 36 microns for typical PCB

d: PCB trace width in mm

L: PCB length in m

The energy stored in the parasitic inductance is problematic because it is transferred to the power switch capacitances, where it can create excessive voltage stress on the power switches, therefore resulting in breakdown and permanent damage. In addition, the resonant circuit formed by the parasitic inductance and power switch capacitances cause voltage ringing, which contributes to EMI problems (Williams, 2001). Resulting voltage (V) on the switch capacitance in a lossless system can be defined as:

$$W = \frac{1}{2}LI^2 \tag{3.3}$$

$$\frac{1}{2}\,LI^2 = \frac{1}{2}\,CV^2 \tag{3.4}$$

$$V = \sqrt{\frac{LI^2}{C}} \tag{3.5}$$

W: Energy (Joules)
L: Inductance
C: Capacitance
I: Current

Trace inductance is directly influenced by the loop area; therefore, all the high current switching traces should be formed by using minimum layout area. The corresponding switching cell consists of several high current loops, which should be carefully routed in order to mitigate the undesirable effects. These loops can be identified as the following:

- Bulk Capacitor Loop
- Snubber Capacitor Loop
- Gate Drive Loops

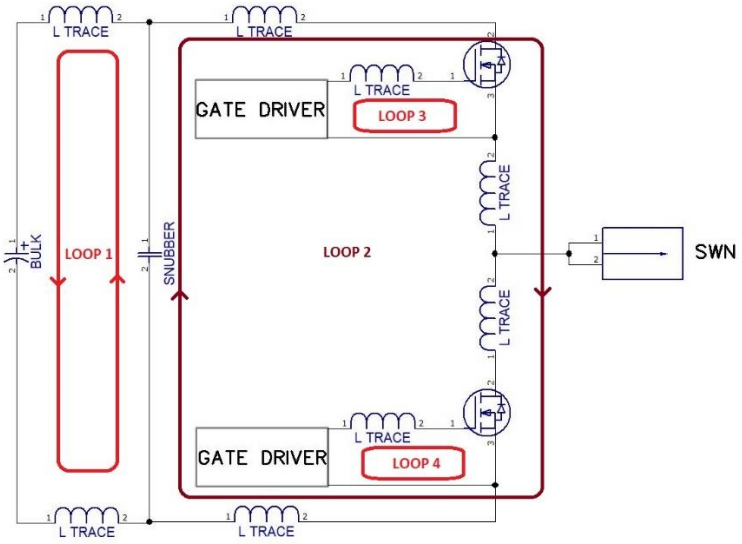


Figure 3.18 Critical current loops of the power stage to be minimized

The following case is an example of large capacitor loop and its effects on the circuit operation. The following circuit in Figure 3.19 shares the same switching cell topology (one switching cell per phase) and uses almost identical MOSFETs with the Designed Class-D Amplifier Test Board:

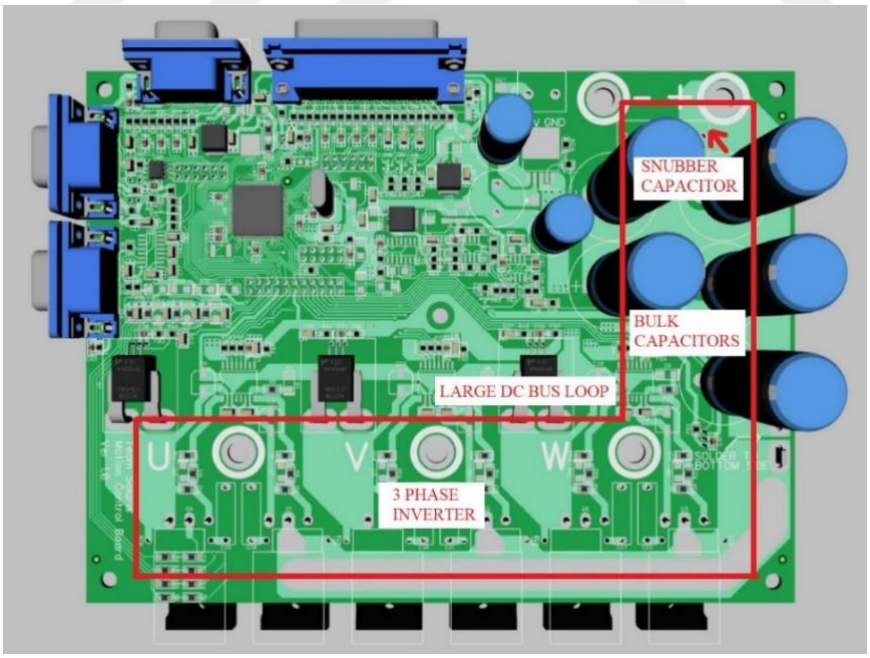


Figure 3.19 Example of large capacitor loop (BLDC Motor Driver, Courtesy of SOLARIS Solar Car Team, Dokuz Eylül University)

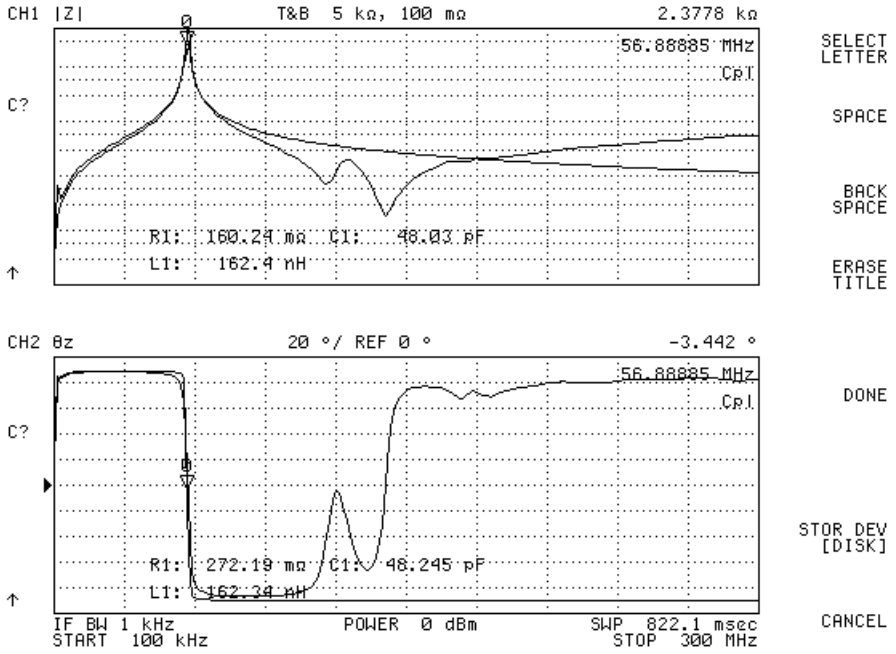


Figure 3.20 Impedance measurement of the bulk capacitor loop, Agilent 4395A indicates 162.4nH parasitic inductance exists (Courtesy of SOLARIS Solar Car Team, Dokuz Eylül University)

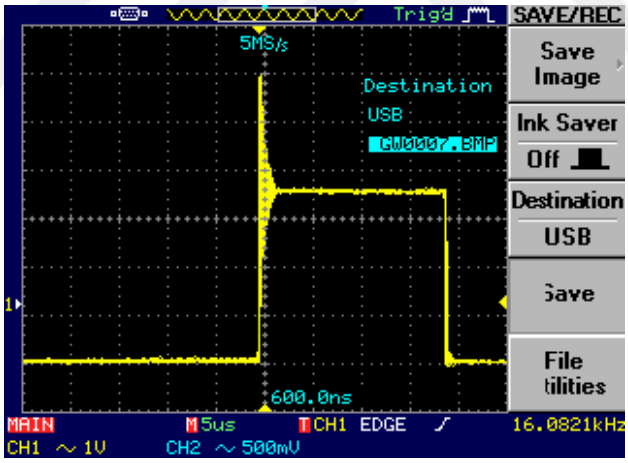


Figure 3.21 Drain- source voltage spikes on switch node caused by parasitic inductances (Courtesy of SOLARIS Solar Car Team, Dokuz Eylül University)

To overcome the problem, additional DC-Bus decoupling capacitors (Snubber) were populated as close as possible to the transistors (in this case, soldered right under the phase leg) to contain the excessive energy stored in the parasitic PCB inductance. As the case above indicates, parasitic inductances are a serious threat which should be eliminated as much as possible. However, it is not possible to completely remove the parasitic components. Even minimized, the existing stored energy can still cause major

problems. To mitigate these issues, a ceramic and an MKP capacitor in parallel were used as layout correction capacitors and placed as close as possible to the power semiconductors of the Class-D Amplifier Test Board. The snubber, path which contains the sense resistor, was routed to have minimal current loop area (Figure 3.22). DC-bus was also routed with overlapping traces to minimize DC-bulk inductance.

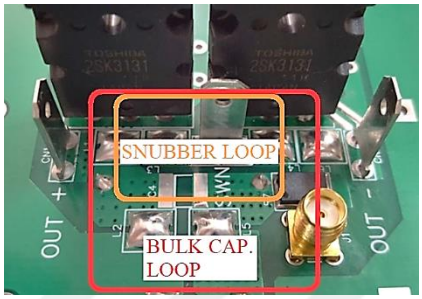


Figure 3.22 Minimized bulk and snubber capacitor loops (Personal archive, 2018)

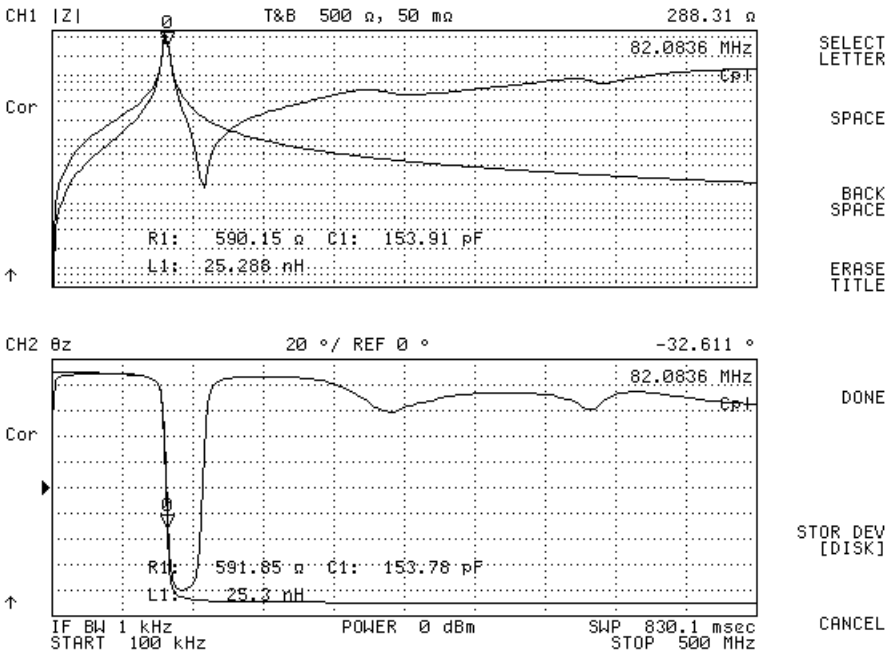


Figure 3.23 Class-D amplifier test board, impedance measurement of the bulk capacitor loop, Agilent 4395A indicates 25.288nH parasitic inductance exists

Impedance analyzer measurement in Figure 3.23 reveals that minimising loop area greatly effects the parasitic inductance build-up. Figure 3.24 shows the effectiveness of the snubber capacitors on mitigating voltage peaks.

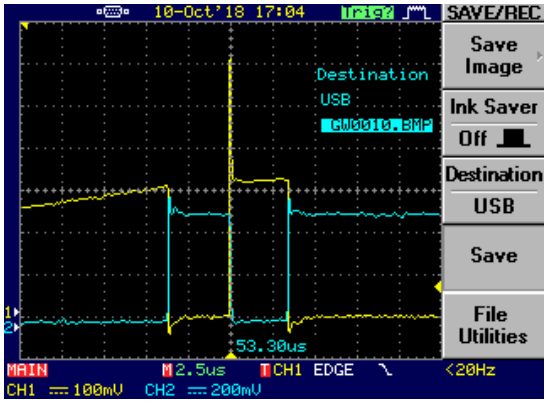


Figure 3.24 Drain- source voltage of the test circuit (channel 2) indicating minimal overshoot while operating at 60A current (channel 1). (Under influence of DC-Link snubber capacitor)

Another important parameter is the gate drive loop inductance. The parasitic build-up on this loop is responsible for gate ringing problems and should also be minimized in order to have a clean transitioning drain-source voltage waveform. The ringing can be effectively damped by introducing a series resistor (Balogh, 2017).

$$R_{GATE}\ Optimal = 2x\sqrt{\frac{L_{TRACE}}{C_{ISS}}} - (R_{Driver} + R_{Gate,\ Internal}) \tag{3.6}$$

The gate resistance is proportional to the parasitic trace inductance. Higher values for gate resistance slow down the transition time, therefore it is beneficial to reduce the parasitic inductance by reducing trace length and gate drive loop area. Figure 3.25 shows the minimised gate drive loops in Class-D amplifier test board.

Figure 3.25 Isolated gate driver circuit and corresponding current loops (Personal archive, 2018)

3.2.6 Transient Current Measurement

One of the most important consideration of the test circuit is to measure the current waveform properly. This is especially problematic because the rise and fall times are extremely narrow, in the order of nanoseconds. Therefore, common applications such as hall effect based current probes or other external devices cannot be used effectively. To deal with this issue, a specific current measurement layout is integrated to the test circuit. It consists of a high power, low inductance current sense resistor (WSHP2818R0100FEA by default), a 49.9Ω series termination resistor and an SMA RF connector. The board is connected to the oscilloscope via a 50Ω transmission line and terminated at the oscilloscope end with a 50Ω termination. The current displayed on the oscilloscope is half of the system current, since the termination resistors act as a voltage divider. By utilizing this method, current measurement bandwidth can easily cover GHz ranges (Langer-emv, n.d).

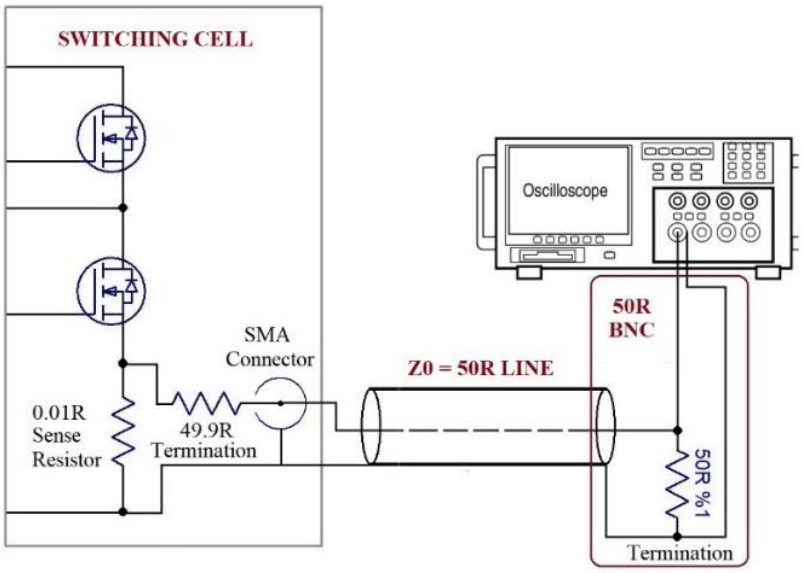


Figure 3.26 Implemented current measurement setup ((Williams, 2009), (Allaboutcircuits, n.d))

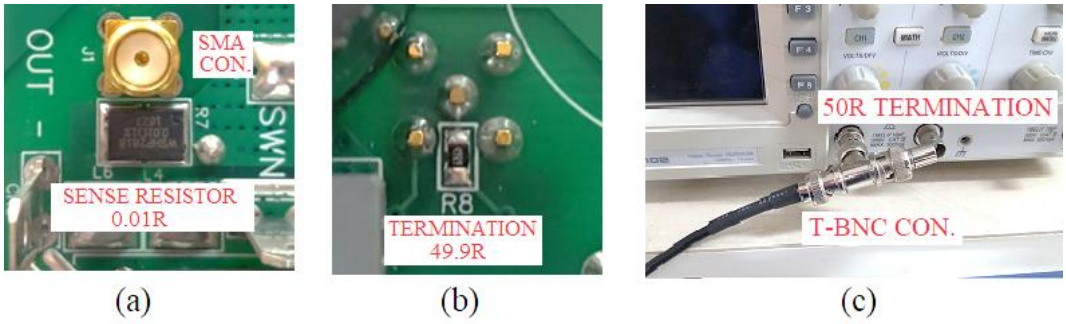


Figure 3.27 Current sense layout, (a) front side, 0.01Ω WSHP2818R0100 sense resistor, SMA connector, (b) back side, chip termination 49.9Ω resistor, (c) oscilloscope input, T-BNC connector and 50Ω termination (Personal archive, 2018)

3.2.7 System Tests

System tests were utilized by incorporating both Double Pulse Test circuit and Class-D Amplifier Test boards. Input power was supplied by a high power 100V output mains transformer. Output consists of a pure inductive load. Similar to current sensing techniques, special measures should be taken in order to capture a clean voltage waveform in single ended measurements.

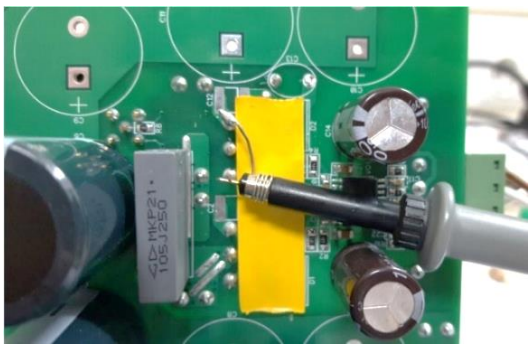


Figure 3.28 Single ended voltage measurement by coiling a wire to the probe return for minimizing probe ground loop area (Personal archive, 2019)

Ordinary 1:10 probe comes with a 4-inch ground lead that forms a loop antenna and disturbs the signal quality when the fast transients are involved. Coiling a wire around the probe ground minimizes the loop area, which significantly improves the signal integrity (Limjoco, 2013). Single ended measurement was used for bottom MOSFET gate measurement. Other high voltage signals were captured by using an active differential probe.

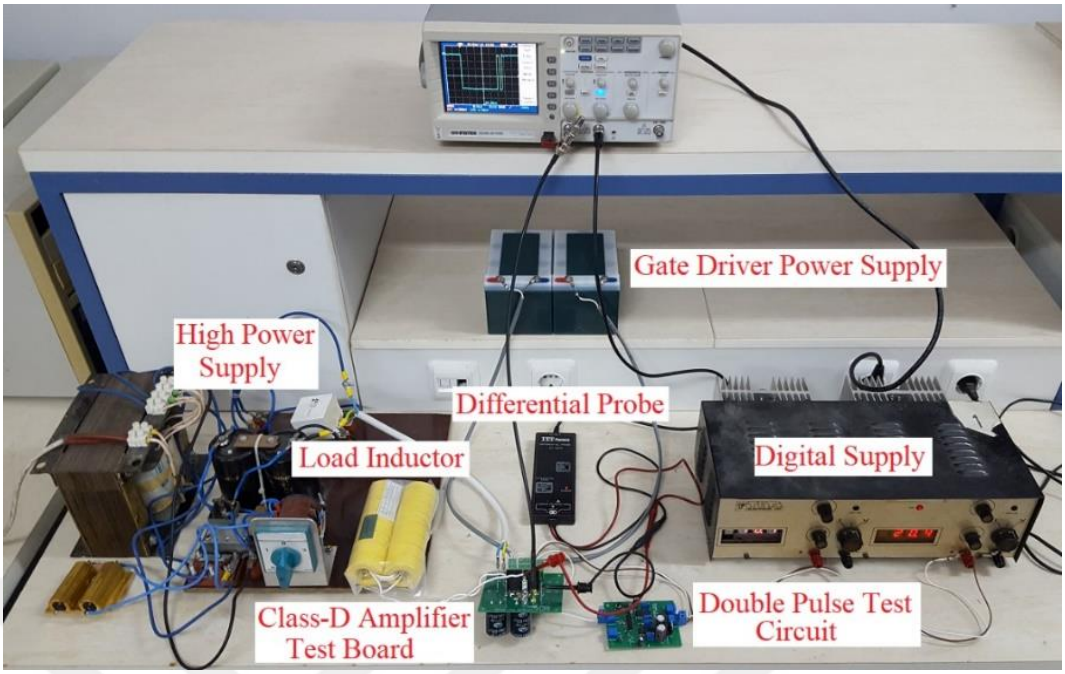


Figure 3.29 Double pulse testing setup (Personal archive, 2019)

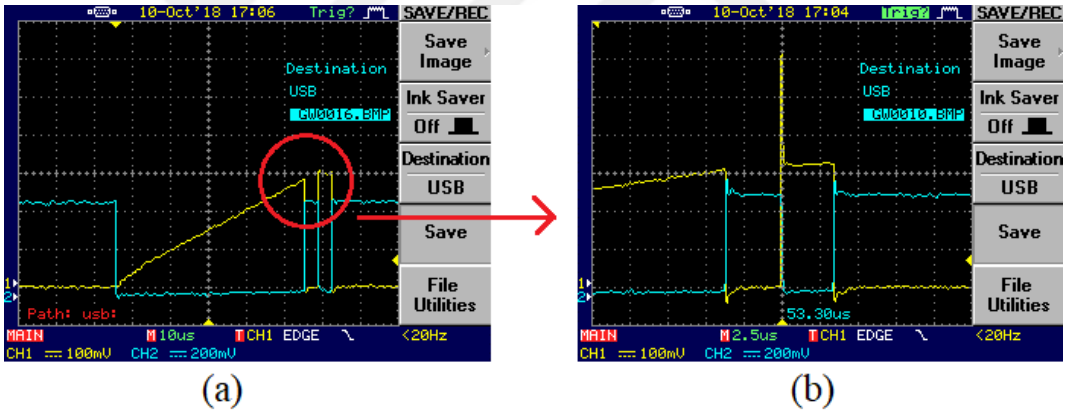
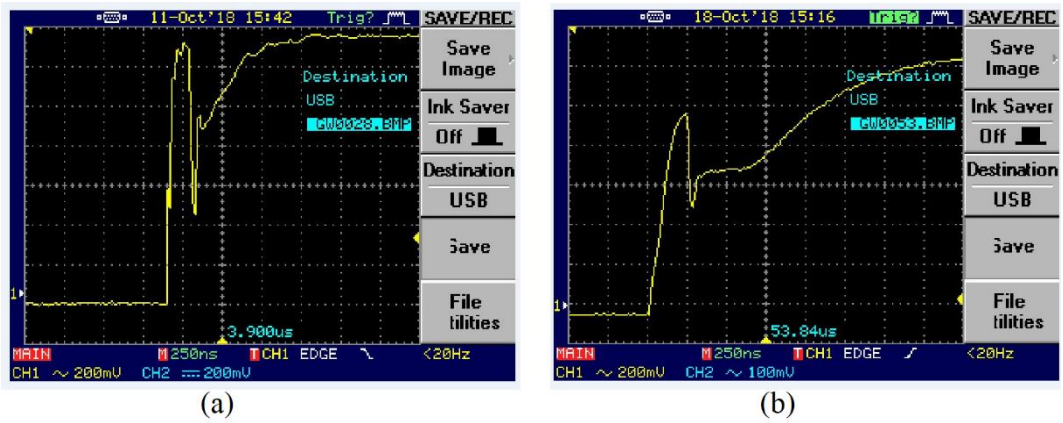


Figure 3.30 Drain- source voltage (channel 2) and current (channel 1) waveforms of Class- D amplifier test board by utilizing the designed double pulse test circuit. (a) 10us/Div showing double pulse waveform, (b) 2.5us/Div focused on the area of interest

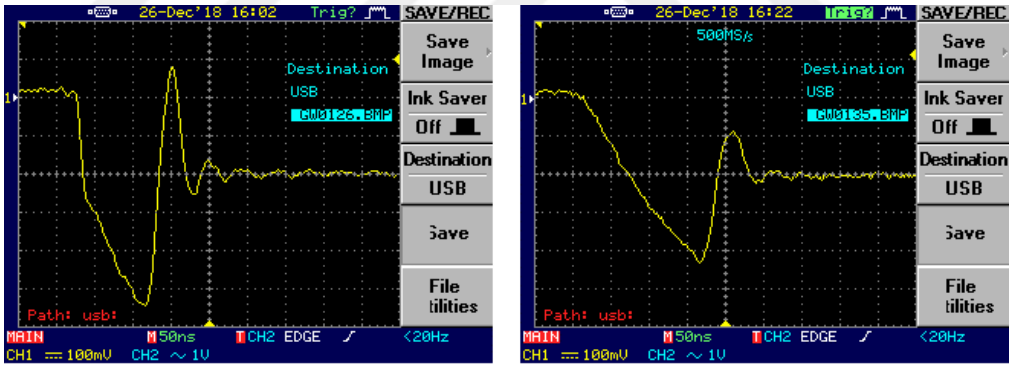
Figure 3.30 indicates the system is working as expected. The drain- source voltage overshoot is almost negligible and reverse recovery current peak can be clearly captured. By altering the gate resistance, switching transition times can be adjusted (Figure 3.31).



(a) (b)

Figure 3.31 Gate ringing waveforms, (a) Tested with 4.7Ω gate resistor, (b) Tested with 22Ω gate resistor

As the measurement indicates, increasing gate resistance dampens the gate oscillations effectively however, compromising from switching performance. Apart from waveform characteristics, increasing transition times also reduces system efficiency by increasing switching losses.



(a) (b)

Figure 3.32 Reverse recovery current, (a) 4.7Ω gate resistor, (b) 22Ω gate resistor

Increasing turn-on time also mitigates the reverse recovery current. Figure 3.32 (b) shows about 20A reduction in reverse recovery current peak.

3.3 Pulse Width Modulated Testing

To be able to spot the reverse recovery problem on the real-world application, a simple pulse width modulator circuit was used to feed the Class-D Amplifier Test Board's input channels. The circuit operates as an open loop PWM modulator, which provides dead time inserted complementary outputs.

3.3.1 Implemented PWM Modulator Circuit Schematics

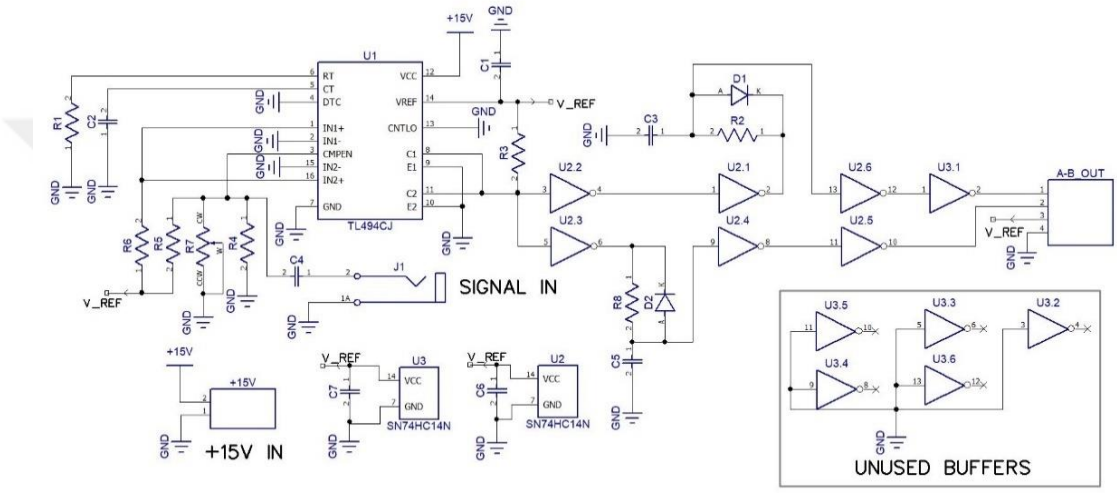


Figure 3.33 Implemented TL494 based PWM modulator circuit schematic

3.3.2 Circuit Operation

The input is a small amplitude AC signal, which passes through coupling capacitor C2. Next, a resistor divider provides a dc-bias near to the %50 duty cycle region. Duty Cycle midpoint can be precisely adjusted with the help of trimmer R2. The circuit consists of a TL494 Voltage Mode PWM controller. The IC is normally used for switch mode converter applications however, it is also suitable for open loop PWM generation by eliminating the input amplifiers with a rail to rail connection of inverting and non-inverting inputs. With this configuration, compensation pin becomes available where the biased input signal can be directly connected in order to have a modulated output.

Apart from the modulator, a dead time insertion is also necessary to prevent shoot-through current in the switching cell. This was achieved by using 74HC14 Schmitt trigger buffers and delaying the output signals with a capacitor- resistor- diode circuit. The capacitor is charged through the resistor and discharged immediately over the diode. Using same circuit for both outputs result in a precise dead-time insertion. Complete test setup is shown in Figure 3.34.

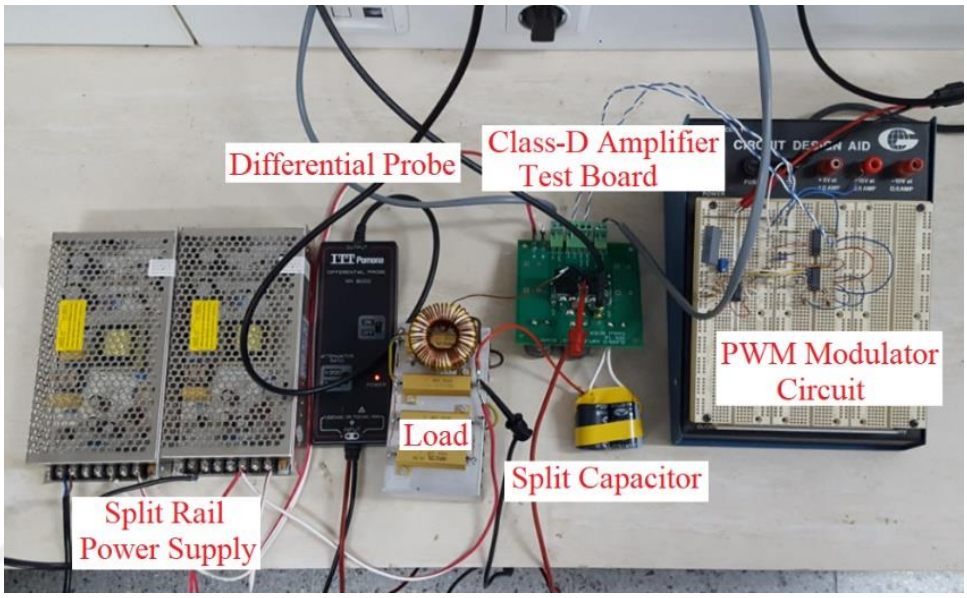


Figure 3.34 PWM modulated test setup (Personal archive, 2019)

3.3.3 Simulations

To verify the captured waveforms, a simulation was performed, which includes both power and the modulator stages. Source V6 simulates the input waveform. The Input is biased to 2.2V to provide a virtual ground for ac input signal. The system contains the best possible matching components to reconstruct the operation of the real-world circuit. For Schmitt trigger buffers, CD4016 was used instead of 74HC14. For gate drivers, LTspice default library includes ADUM4120 and two of them were used instead of single ADUM4023. LTspice default library does not contain TL494 and CD40168 components. These were obtained from other libraries. TL494 was retrieved from ValVol Library (Valvolodin, n.d) and CD4016 was retrieved from CD4000 library (Zpostbox, n.d).

3.3.4 Simulation Circuit Schematics

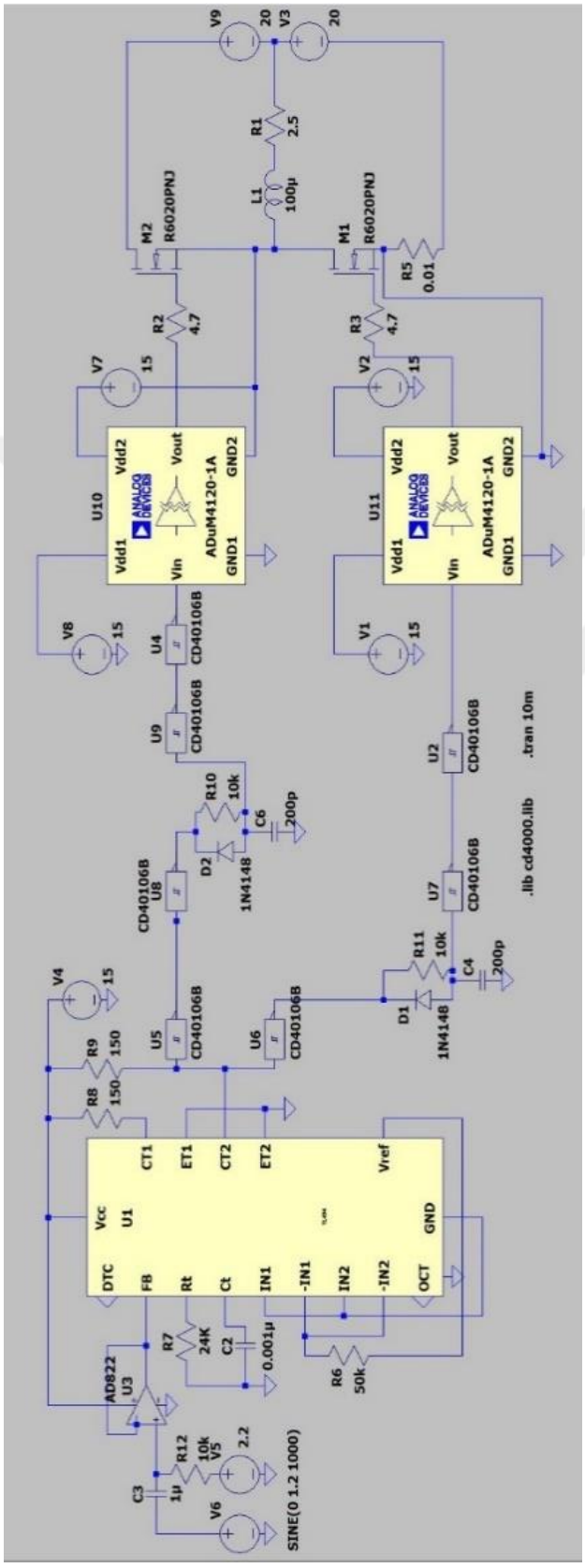


Figure 3.35 Simulation circuit schematic that contains the implemented PWM modulator and implemented switching cell

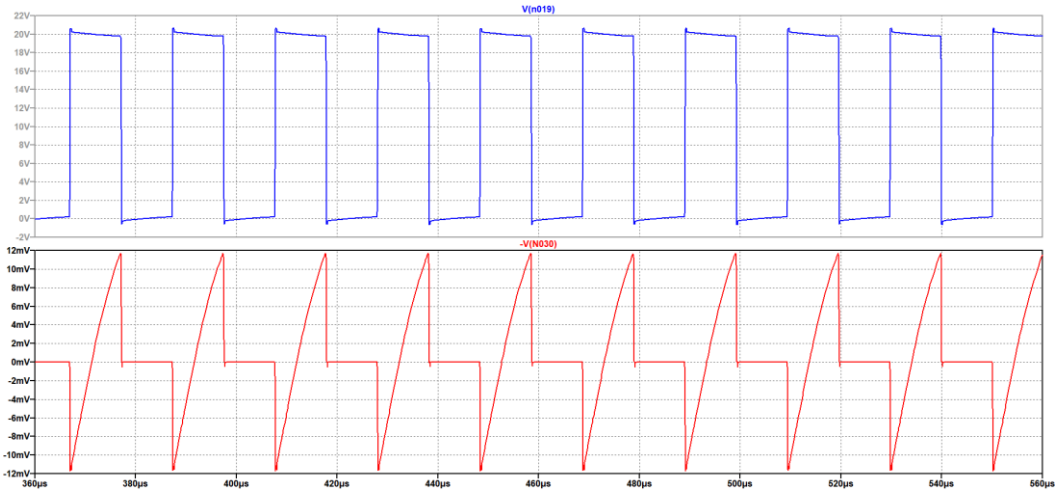


Figure 3.36 Switch node voltage and sense resistor voltage simulated waveforms near %50 duty cycle zone

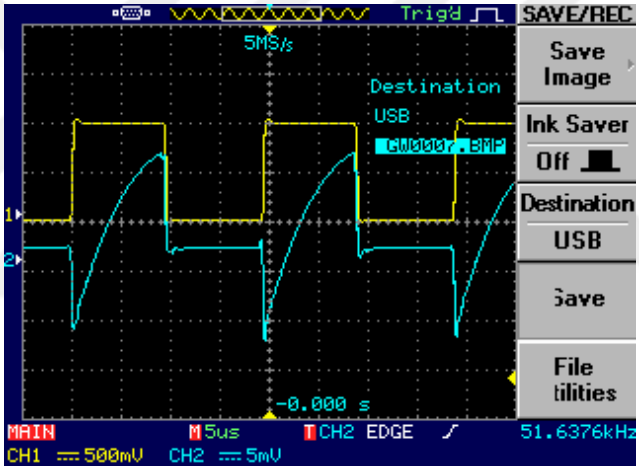


Figure 3.37 Switch node voltage (channel 1) and sense resistor voltage (channel 2) waveforms near %50 Duty Cycle

Simulations (Figure 3.36) and real-world measurement (Figure 3.37) show that reverse recovery does not occur where the system operates around %50 duty cycle, since the net diode current is almost zero.

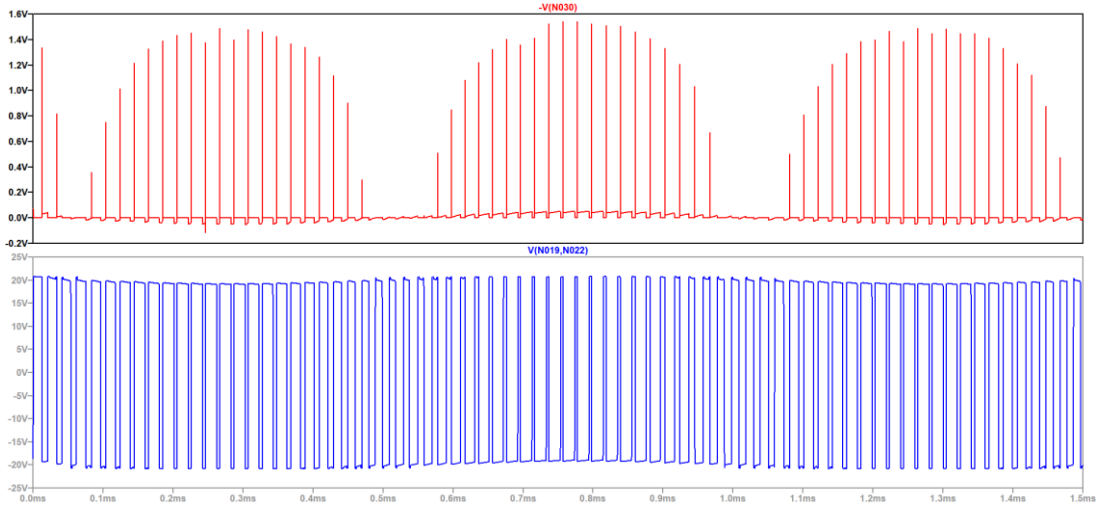


Figure 3.38 Switch node voltage (blue) and sense resistor (red) voltage simulated during modulation

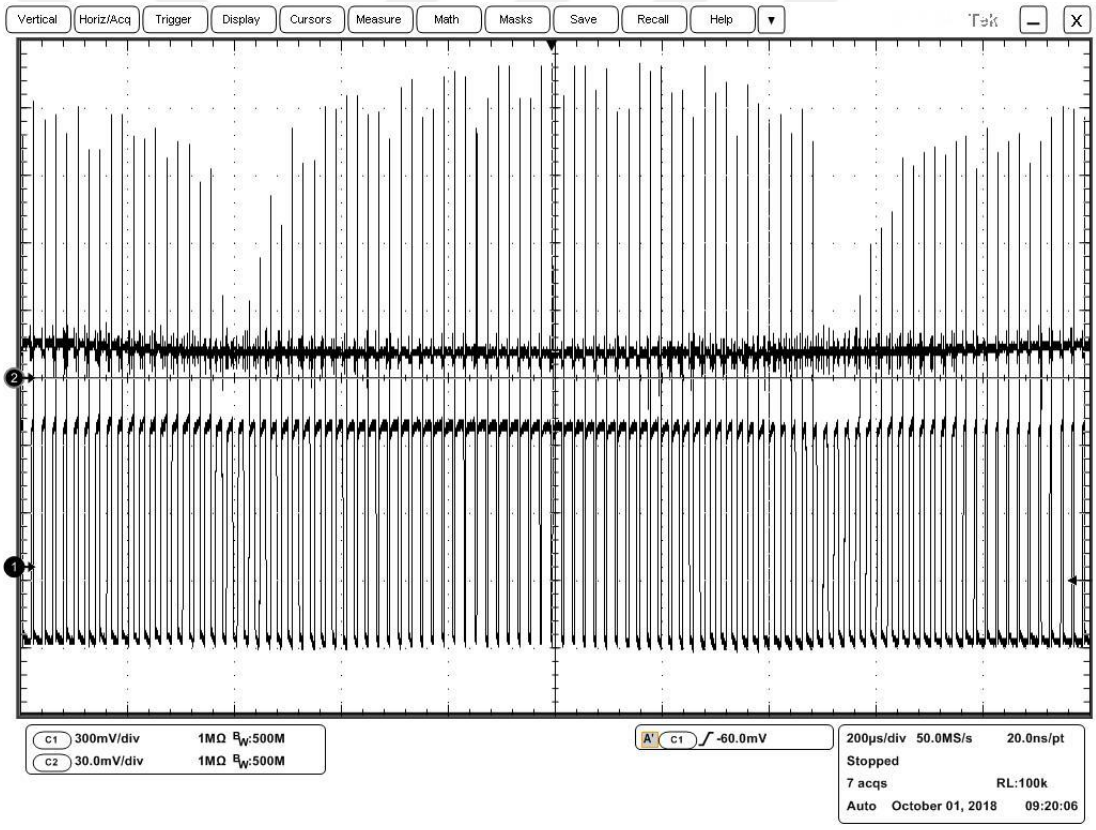


Figure 3.39 Switch node voltage (channel 1) and sense resistor voltage (channel 2) during pulse width modulation (Tektronix DPO7104)

Both simulation (Figure 3.38) and real-world measurement (Figure 3.39) indicates sharp increase of current spikes immediately after %50 duty cycle zones.

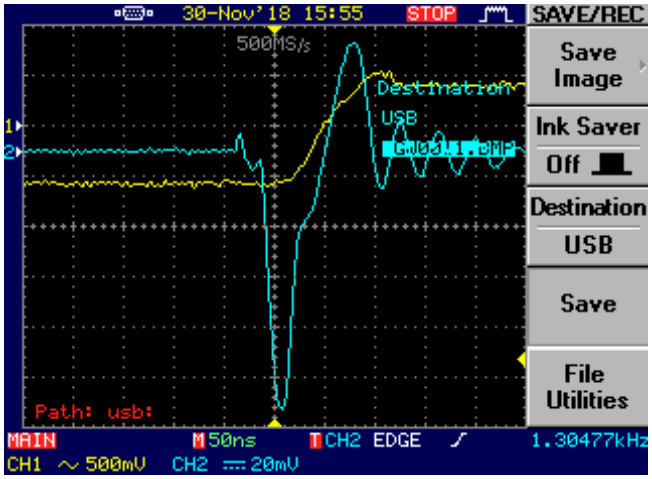


Figure 3.40 Switch node voltage and sense resistor voltage waveforms during reverse recovery event

Waveform in Figure 3.40 displays the reverse recovery event during one of the modulation cycles. However, the waveform indicates Drain Source voltage rise is delayed compared to the reverse recovery spike. This phenomenon is caused by the propagation delay introduced by the active differential probe (Figure 3.41). The current sense setup on the other hand, does not include any sort of reactive signal compensation components, which means significantly lower propagation delay, even compared to the ordinary 1:10 probes.

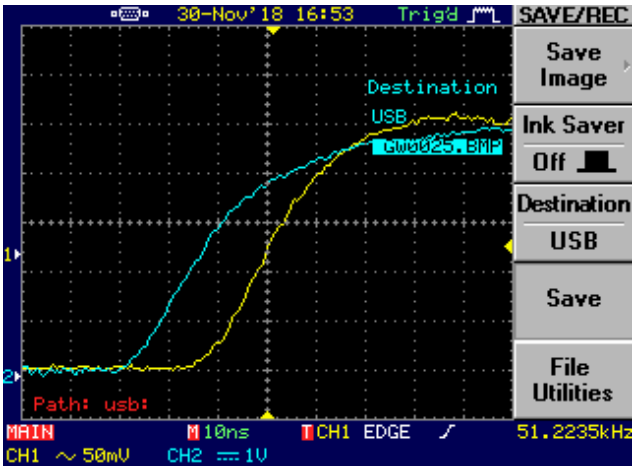


Figure 3.41 Propagation delay caused by active differential probe, passive probe (channel 1), active differential probe (channel 2)

CHAPTER FOUR
CONCLUSION

In switch mode power processing circuits, the major drawback of using silicon diodes is the reverse recovery effect. Reverse recovery charge acts like a short circuit and allows a sharp shoot-through current flowing over the inverter stage. The current overlaps with the power switch voltage and results in a tremendous amount of power dissipation for a short period of time. This becomes especially problematic for the Class-D amplifiers, where the main goal is to fulfill the efficiency requirements. Apart from efficiency, this phenomenon forces designers to use parts with enhanced voltage and current specifications, which increases the semiconductor budget.

Complete system simulation reveals that implemented Class-D amplifier is susceptible for reverse recovery effect beyond %50 duty cycle PWM regions. Power stage simulation proves that reverse recovery current excites the RLC circuit formed by trace inductance, MOSFET capacitance and overall resistance, that results in high voltage peaks and oscillations. Therefore, it becomes clear that there are two distinctive side effects of reverse recovery, voltage overshoot and shoot-through current peaks. In order to show the mitigation of these parameters on a real-world circuit, a specific Class-D amplifier power stage was designed and prototyped. The layout was designed to minimize the parasitic inductances on high di/dt paths. For the measurement integrity, gate drive block and power block were completely isolated from each other by using ADUM4223 isolated gate driver. In addition, a special current sense block was integrated in order to maximize the noise susceptibility of the measurement setup.

To test the designed system under real operating conditions, a PWM modulator circuit was designed and prototyped on circuit design aid (breadboard with integrated power supply). The circuit consists of a voltage mode PWM regulator IC TL494, which was configured as feed-forward mode, therefore its output is a proportionally modulated PWM signal with respect to the voltage level of the input. The circuit also includes a stage which provides dead-time inserted complementary outputs, which can

be directly connected to gate driver inputs of the designed and prototyped Class-D amplifier test board. Combination of these systems was successfully tested with split rail power supplies and RL load to simulate real-world applications. Laboratory tests proved that Class-D amplifier suffers reverse recovery current spikes. A very high bandwidth oscilloscope measurement shows that this is the weakness of Class-D amplifiers. Experiment was indicated that if the PWM modulation level is at its reference value (%50 duty cycle case) then no reverse recovery problem occurs.

To monitor the circuit just under the limiting current specifications, a special double pulse signal generator circuit was designed. The circuit consists of 4098 type monostable multivibrators (in this case HCF4098) to provide precisely adjustable time steps. User interface consists of four multiple turn trimmers to adjust the pulse durations, and a tactile switch to trigger double pulse sequence. To investigate copper path stray inductance effects on the PCB, Prototyped Class-D amplifier test board was configured as a clamped inductive load tester, where the top MOSFET's gate is shorted to source. In this way it functions as the body diode only. Double pulse circuit was connected to the bottom side MOSFET. On switch-node, a pure inductive load was connected. With this method, current peaks were observed as high as 70A. Apart from the magnitude, the current sense circuit is sensitive enough to accurately display rise and fall slopes. It proves that increasing turn on time by increasing MOSFET gate resistor mitigates the current spike problem. In addition, careful layout design techniques to minimize parasitic inductance and addition of DC-Bus snubber capacitor almost completely mitigates voltage overshoots on the switch node.

It concludes to a point that system designers must take reverse recovery current into account prior to determining semiconductor specifications. Semiconductor cost can be lowered by increasing the transition times, however there is a tradeoff between the cost and system efficiency. On the other hand, circuit layout is a critical parameter and parasitic inductances should be avoided as much as possible to minimize voltage overshoots and potential reliability issues.

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APPENDICES

Symbols and Abbreviations

PWM: Pulse Width Modulation

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

BJT: Bipolar Junction Transistor

IGBT: Insulated Gate Bipolar Transistor

IC: Integrated Circuit

PCB: Printed Circuit Board

$R_{DS\ (on)}$: MOSFET Drain Source On Resistance

T_{rr}: Reverse Recovery Time

Q_{rr}: Reverse Recovery Charge

NA: Not Assembled

RTN: Return

C: Capacitor

R: Resistor

L: Inductor

FB: Ferrite Bead

U: Integrated Circuit (IC)

Q: Transistor

J: Jumper

EMC: Electromagnetic Compatibility

ESR: Equivalent Series Resistance

C_{OSS}: MOSFET Output Capacitance