WIDEBAND DISTRIBUTED CHOKE INDUCTOR FOR DISTRIBUTED POWER AMPLIFIERS

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IN
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By
Çağdaş Ballı
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We certify that we have read this dissertation and that in our opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

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ABSTRACT

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January 2023

A method to design a wideband, low-loss, and high-current choke inductor suitable for use in a distributed power amplifier (DPA) is presented. The choke inductor is composed of several parallelled low-current inductors with small parasitics placed in a distributed manner. High-frequency gain-limiting parasitic shunt capacitors of these inductors are absorbed by the series inductors already present between the transistor drain terminals of the distributed amplifier. We also provide an analytical procedure to determine the widths of stage transistors of a non-uniform distributed power amplifier (NDPA). Several example designs are presented to demonstrate the use of our method. The measurement results of a 2–18 GHz NDPA designed using a distributed choke inductor with an equivalent DC resistance of 0.32 Ω are given. The MMIC has fully integrated with the on-chip DC blocking capacitors and bias inductors. The results of the CW mode measurement for the MMIC at 28 V supply voltage show greater than 10 dB of small signal gain, 6 W to 12 W output power, and 15% to 28% power-added efficiency in the bandwidth.

Keywords: distributed power amplifier, choke inductor, non-uniform distributed power amplifier.

ÖZET

DAĞINIK GÜÇ YÜKSELTEÇLER İÇİN GENİŞ BANTLI DAĞINIK ŞOK İNDÜKTÖR

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Dağınık güç yükselteçler için geniş bantlı, düşük kayıplı, yüksek akımlı bir şok indüktör tasarım metodu paylaşılmıştır. Şok indüktör, birden fazla düşük akımlı ve düşük parazitik kapasitanslara sahip indüktörlerin, paralel olarak dağınık biçimde yerleşimiyle oluşturulmuştur. Yüksek frekanslarda kazancı limitleyen parazitik şönt kapasitanslar, dağınık yükselteçteki transistörlerin drain terminalleri arasında hali hazırda bulunmakta olan indüktörler ile etkisiz hale getirilmiştir. Ayrıca düzensiz dağınık güç yükselteçte bulunan transistörlerin kapı genişliklerini belirlemek için analitik bir prosedür sunulmuştur. Bu metodun işlevselliğini göstermek için birden fazla tasarım örneği paylaşılmıştır. Eş değer DC direnci 0.32 Ω olan bir dağınık şok indüktör kullanılarak, $2-18$ GHz bandında tasarlanan düzensiz dağınık güç yükseltece ait ölçüm sonuçları verilmiştir. Çip DC engelleme kapasitörleri ve kutuplama indüktörleri ile beraber tek bir entegre halindedir. 28 V kaynak voltajı ile CW modunda alınan ölçüm sonuçları tüm bantta 10 dB'den fazla kazanç, 6 W ile 12 W arasında güç ve %15 ile %28 arasında eklenen güç verimliliği göstermiştir.

Anahtar sözcükler: dağınık güç yükselteç, şok indüktör, düzensiz dağınık güç yükselteç.

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I would like to thank you,
to those special people who hold this thesis in their hands and read these lines,
to those invaluable people for their unconditional love and support.

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Chapter 1

Introduction

There is a growing need for fully integrated broadband high-power, high-efficiency amplifiers used in many wideband microwave systems, test equipment, and general use. To achieve wideband performance, solid-state amplifiers are usually based on distributed topology. Various broadband amplifiers have been proposed in both GaAs and GaN-based semiconductor technologies. Although GaAs-based amplifiers have superior performance at high frequencies, GaN offers higher power density. It was shown that the same output power and bandwidth could be achieved in a smaller area using GaN technology instead of GaAs [1]. To further improve output power and power-added efficiency (PAE) using a GaN-based process, a non-uniform distributed power amplifier (NDPA) topology is typically used [2–8]. Topology simultaneously provides higher output power and enhanced efficiency over large bandwidths, i.e., 1–8 GHz, 1.5—17 GHz, 2–20 GHz, and 18–40 GHz.

Due to the above benefits, various GaN MMIC NDPAs were proposed to obtain maximum achievable output power in the frequency range of 2–18 GHz. In [9], an NDPA design procedure based on a node analysis was presented, and core NDPA topology was realized more efficiently due to the transformer placed at the output, which is used in lowering the load impedance seen by the last transistor.

In [10], an output power of 9.9 W from 2 to 20 GHz was achieved by combining two identical strings of 15 unit cells. Variation in transistor sizes was implemented by moving line lengths between any two or more unit cells to physical dimension minimums, effectively acting as a larger cell.

In [11], a power amplifier (PA) using the conventional reactive matching technique was demonstrated, covering 3–17 GHz with 20 W of output power. The input return loss was sacrificed to improve all other parameters. The drawback is that it is hard to drive a PA with an input impedance much different than 50 Ω.

In [12], a compact high gain NDPA having 10 W of output power over 2–18 GHz was implemented in 0.1 μm GaN on Silicon (GaN/Si) process by 8-distributed 3-stacked-FET cells. NDPAs, specifically implemented on GaN on Silicon with poor thermal dissipation compared to GaN on SiC, may suffer from a non-uniform thermal distribution that may affect the device lifetime. The RMPA design, which usually provides uniform thermal distribution, was proposed to overcome this issue in [13]. The disadvantage of using stacked FETs is that the large-signal design using stacked FETs in a CAD environment at millimeter-wave frequencies is very complex and may require a couple of iterations to finalize the design making it inefficient in terms of cost and time. Moreover, required transistor models may not be available, and one may need to define their non-linear models on their own, both in common source and common gate configurations.

Single-stage GaN-based power amplifiers (PAs) can be driven into 6–7 dB compression or more to obtain maximum output power, which results in a low large signal gain. Therefore, multiple stages are needed to ensure the desirable large signal gain. However, successive cascading of stages with roll-off at the band edges causes a severe reduction in gain, effectively reducing bandwidth. In [14], this limitation is reduced by removing the DC block capacitor between two NDPA stages and decreasing the number of choke inductors.

In [15], the power and efficiency are maximized by implementing an output transformer that reduces the load impedance from 50 Ω to 12.5 Ω. This way, the inductance required for the output bias choke is significantly reduced, which is

vital to bandwidth.

One of the factors that limit the performance of an NDPA is the drain bias choke inductor. It must handle the high supply current while keeping its series resonance frequency out of the band and have a sufficiently high inductance to provide adequate impedance at the bottom of the band. Moreover, it should have small shunt parasitics not to limit the performance at high frequencies.

Conical inductors as discrete components with high series resonance frequencies are commercially available. However, their use as off-chip inductors is problematic due to the band-limiting effect of the bonding pad capacitance at the drain line. In addition, they are primarily used in low-power applications due to their low current handling capabilities.

Using an on-chip wideband small-size 1:4 Ruthroff output impedance transformer is very advantageous since one can design for a four times lower drain-side impedance to improve the output power and reduce the value of the on-chip choke inductor [15, 16] by the same factor. An on-chip LC branch [17] is needed for the transformation at low frequencies, through which DC drain bias current is supplied.

In many cases, the amplifier bandwidth is determined by the parasitics of the bias choke inductor and not the frequency capability of the core NDPA [18]. This article presents a method to design a wideband, low-loss, and high-current choke inductor suitable for distributed power amplifiers.

In the next section, we present an analytical design procedure for a non-uniform distributed power amplifier for optimal performance. In the following section, we characterize the band-limiting parasitic components of an on-chip spiral inductor. In section IV, we show how to eliminate the parasitic components using a distributed choke inductor integrated with a distributed power amplifier. In section V, we present the measurement results of a non-uniform distributed amplifier containing the proposed distributed choke inductor.

Chapter 2

Distributed Amplifier

2.1 Bandwidth of an Amplifier

The gain of a transistor decreases with frequency. However, most amplifiers require a flat gain response over the designed bandwidth. Therefore, matching networks should have higher losses at the lower frequencies whereas lower losses at the higher frequencies. In other words, gain compensation networks should be employed in the matching networks, designed to provide desired impedances to the devices for optimum performance. For instance, in power amplifiers, the matching networks should be designed so that each transistor sees the desired load impedance for maximum output power and power-added efficiency (PAE) while adding minimum loss at the output and providing the necessary gain slope to obtain flatness over the desired bandwidth. Thus, the critical concept to designing matching networks of a wideband amplifier is to adjust the insertion loss required for each stage to compensate for the gain slope while maintaining the output power and PAE at their optimum values. However, there is a fundamental limit on the bandwidth over which an arbitrarily good impedance match can be obtained [19].

2.2 Theory of Distributed Amplification

It can be shown that for a Bode-Fano limited bandwidth of a transistor, the output impedance matching network is inversely proportional to the parasitic output capacitance of the transistor. This capacitance needs to be reduced to be able to increase the bandwidth. This is the key idea behind distributed amplification.

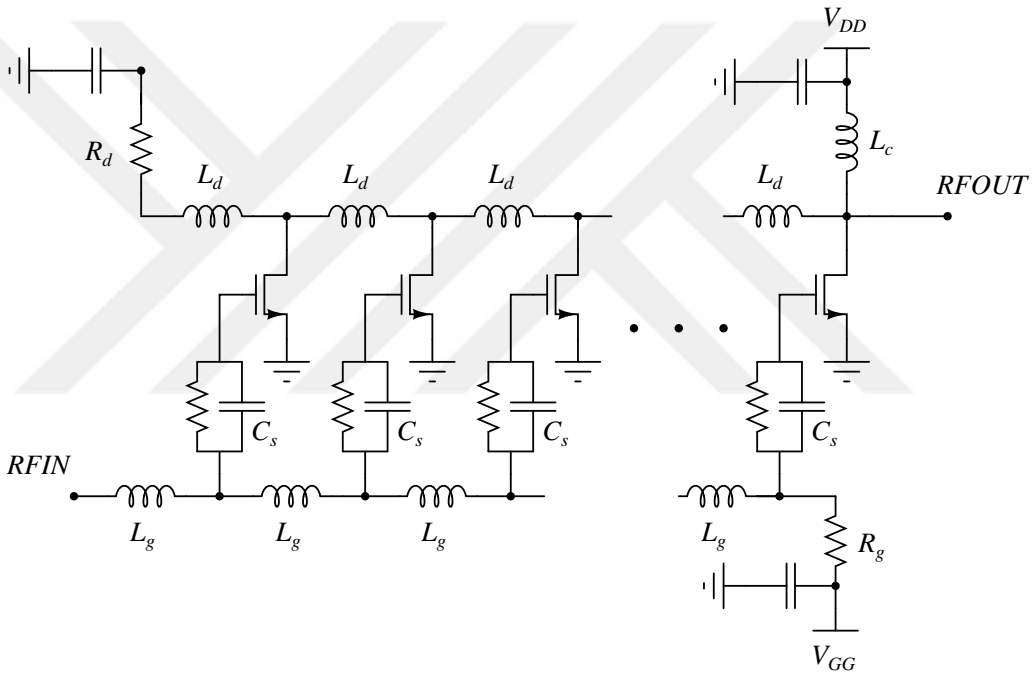

Figure 2.1: A simplified representation for an n-section distributed amplifier.

A conventional N-section distributed amplifier circuit is shown in Fig. 2.1 with equal-size transistors. Input and output capacitances of the transistors are linked through the inductors to form lumped-component artificial transmission lines while currents are combined additively. The additive nature of the distributed amplifier results in a relatively low gain. On the other hand, distributed amplifiers achieve very wide bandwidths since the input and output capacitances of the transistors are absorbed into the artificial transmission lines.

Indeed, the inductors and capacitances of the transistors can be viewed as a filter structure. The capacitances are parts of the filter structure whose bandwidth

is determined by its components, the inductors, and capacitors. Those artificial transmission lines are terminated into their respective characteristic impedance value and therefore matched to absorb waves traveling in the reverse directions. The impedance of the gate line is given by

$$Z_{og} = \sqrt{\frac{L_g}{C_{gs}}} \tag{2.1}$$

and the impedance of the drain line is given by

$$Z_{od} = \sqrt{\frac{L_d}{C_{ds}}} \tag{2.2}$$

When a signal propagates through the gate line, each transistor is excited with phase shifts, the signal is amplified, and each transistor generates a drain current with phase shifts propagating through the drain line. If gate and drain line sections provide equal phase shifts, the drain current waves add up constructively. To provide equal phase shifts, we need to have

$$L_g C_{gs} = L_d C_{ds} \tag{2.3}$$

To increase the gain without compromising the bandwidth, more transistors can be added as long as the proper amount of inductance is placed to form additional filter sections with the parasitic capacitances of the transistors. However, the number of transistors cannot be increased indefinitely. Since the inductors and transistors are lossy, the signal's amplitude attenuates when it passes through the artificial transmission lines. Therefore, the total gain is degraded when more transistors are used, which reveals that an optimum number of transistors maximizes the gain [20].

The cut-off frequency of the artificial transmission lines limits the bandwidth of the distributed amplifier. By the selection in (2.3), the cut-off frequencies of two transmission lines are also equalized, providing a maximized bandwidth

$$f_c = \frac{2}{2\pi\sqrt{L_g C_{gs}}} = \frac{2}{2\pi\sqrt{L_d C_{ds}}} \tag{2.4}$$

However, the input capacitance of a transistor is usually greater than the output capacitance. And therefore, the bandwidth of the amplifier is determined

by the cut-off frequency of the input line, which is given as

$$f_c = \frac{1}{\pi Z_{0g} C_{gs}} \tag{2.5}$$

To increase the bandwidth of a distributed amplifier and maintain a relatively easy phase shift equalization, capacitors in series with the gate of each transistor cell are typically added at the expense of gain. By doing this, it is possible to vary the amount of RF voltage at the gate of each transistor to drive cells equally and, in this way, compensate for the gate line attenuation [21]. Another accomplishment utilizing capacitors is an increase in power-handling capability. Capacitors acting as capacitive voltage dividers reduce the magnitude of the RF voltage swing at the gate of the transistor. If a capacitance C_s is added in series with the gate, the effective gate capacitance becomes

$$C'_{gs} = \frac{q}{1+q} C_{gs} \tag{2.6}$$

$$q = \frac{C_s}{C_{gs}} \tag{2.7}$$

where the first term represents the series combination of C_s and C_g, and the second term is the capacitance of the gate transmission line.

Another technique developed to decrease the input capacitance is to implement RC degeneration on a common-source amplifier [22]. The input impedance of a common source amplifier is given by

$$Z_{in} = R_s + \frac{1}{j\omega C_{gs}} \tag{2.8}$$

When the values of R and C are set properly, the input impedance of the common source amplifier and the transconductance become

$$Z_{in} = \frac{C_{gs}}{1 + g_m R_s} \tag{2.9}$$

$$G_M = \frac{g_m}{1 + g_m R_s} \tag{2.10}$$

and hence, the input capacitance is reduced at the expense of degraded transconductance.

Cascode amplifier topology has been used to realize amplifiers having high gain over a wide bandwidth. It has also been successfully used in distributed amplifiers to boost gain and bandwidth due to low Miller feedback capacitance and high output impedance.

The distributed amplifier is a popular architecture that provides excellent gain performance over a wide bandwidth. However, the performance is degraded when it is intended to be used as a power amplifier. This is because the distributed amplifiers are designed for maximum gain, and good input and output match in the 50 Ω system, which means that each transistor in the amplifier does not see the optimum load impedance for power and PAE. Unlike the amplifiers designed for maximum gain, a power amplifier should be designed so that each transistor sees the load impedance required for maximum power and PAE. Another reason for performance degradation is the output transmission line termination, R_D. Some of the output signals, which could not be added up correctly, propagate to the left of the drain line and are dissipated in the termination, R_D. This directly affects the output power and efficiency because the power is wasted in the output termination. To improve the output power and PAE, a non-uniform distributed power amplifier (NDPA) topology is typically used [2]. Topology simultaneously provides higher output power and enhanced efficiency over large bandwidths, i.e., 1–8 GHz, 1.5—17 GHz, 2–20 GHz, and 18–40 GHz.

Chapter 3

Non-Uniform Distributed Amplifier

3.1 Theory of Operation

To maximize the power output of a distributed power amplifier, the drain load of each transistor should be adjusted to its individual optimum loads. This may be explained by using nodal current analysis to a simplified equivalent circuit for the output side of a four-cell distributed amplifier which is given in Fig. 3.1. Note that the output transmission line termination, R_D, is removed in order to improve the output power and power-added efficiency.

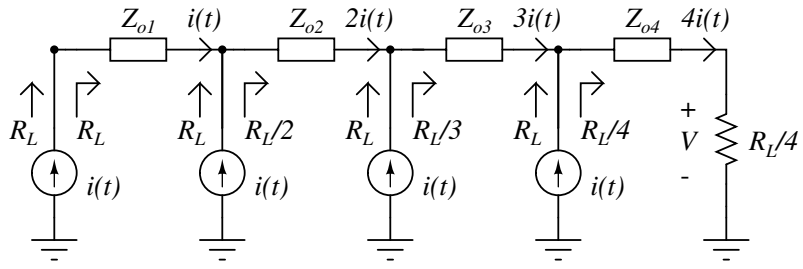

Figure 3.1: A simplified representation for a 4-cell distributed amplifier showing current combining

Let R_L be the desired impedance required for the maximum power and PAE and assume that all four devices have the same size. The characteristic impedance of the transmission line, Z_{o1}, looking from node 1 toward the right should be R_L so that the first device is presented with the optimal load. At node 2, if the current from the first source arrives in phase with the current from the second source, then the characteristic impedance of the transmission line, Z_{o2}, looking from node 2 toward the right should be $R_L/2$ in order to load the second source with the desired impedance R_L. Using similar analysis, the characteristic impedance of the transmission line, Z_{o3}, looking from node 3 toward the right should be $R_L/3$ and the characteristic impedance of the transmission line, Z_{o4}, looking from node 4 toward the right should be $R_L/4$, which would be the system impedance. The resulting structure is a tapered transmission line with decreasing characteristic impedance. In doing so, even the transistor sizes may be varied to set the values of such impedances, and hence such an amplifier is called a non-uniform distributed amplifier.

Note that the characteristic impedance of the first transmission line increases as the number of devices increases which reveals a serious problem. Some of the lines near the first device have very high characteristic impedances that are not realizable for a monolithic implementation. One solution to some extent is to make the first cell larger than the others remaining the same total size of transistors. The more useful and practical solution is to use an impedance transformer.

It is important to note that the phase equalization of artificial transmission lines needs to be satisfied for each section between any two adjacent transistors. By suitably tapering the drain line, we obtain the characteristic impedance of each drain line section differently which results in an efficient combination of transistor currents. This leads to different inductance and capacitance values for each drain line section. We present the design procedure below.

3.2 Design Procedure

The input side of NDPA is designed like a series combination of C-L-C networks, shown in Fig. 3.2, with a cut-off frequency of w_0 which is about 10 % higher than the maximum frequency of NDPA. N is the number of stages.

We first assign impedances, Z_{ei}'s for i=1, ..., $N-1$, as the impedances of the input side network. The values of these impedances can be chosen all to be equal to the source impedance of the NDPA. Since

$$Z_{ei} = \sqrt{\frac{L_{ei}}{C_{ei}}} \text{ for } i = 1, \ldots, N-1 \tag{3.1}$$

The element values, L_{ei} and C_{ei} can be found from

$$L_{ei} = \frac{Z_{ei}}{w_0} \text{ and } C_{ei} = \frac{L_{ei}}{Z_{ei}^2} \text{ for } i = 1, \ldots, N-1 \tag{3.2}$$

To form input network, neighbor capacitors are combined as

$$C_{fi} = \begin{cases} C_{e1} & \text{for } i = 1 \\ C_{e(i-1)} + C_{ei} & \text{for } i = 2, \ldots, (N-1) \\ C_{e(N-1)} & \text{for } i = N \end{cases} \tag{3.3}$$

where C_{fi} represents the input capacitor of the ith node. The sum of all input capacitors, C_{fT}, is given by

$$C_{fT} \triangleq \sum_{i=1}^{N} C_{fi} \tag{3.4}$$

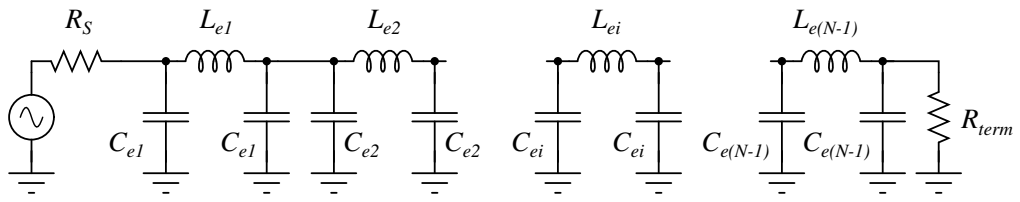

Figure 3.2: The schematic diagram of the intended input circuit

Note that R_{term}, should be nearly equal to R_S to get a small $|S_{11}|$.

The analysis presented in [9] has been adopted here which enables analytical determination of the optimal width of the transistor, W_i, at the ith stage. Assuming the drain capacitances of transistors are absorbed into the transmission lines, the optimum output load resistance, Z_{oi}, of the ith section is given by [9] :

$$Z_{oi} = \frac{\overline{R}_p}{\sum_{j=1}^{i} W_j} \quad \text{for } i = 1, \ldots, N \tag{3.5}$$

where the denominator is the sum of all transistor widths up to the ith stage. $\overline{R}_p$ is constant specifying the product of optimum load resistance and the transistor width, a fabrication process-dependent constant.

For N stages, the output load, R_{out}, of the amplifier should be

$$R_{out} = Z_N = \frac{\overline{R}_p}{\sum_{i=1}^{N} W_i} = \frac{\overline{R}_p}{W_T} \tag{3.6}$$

where W_T is the sum of all transistor widths.

The maximum output power, P_m, is limited by the supply voltage, V_{DD} and the output load resistance, R_L, of the amplifier:

$$P_m = \frac{V_{DD}^2}{2R_{out}} = \frac{V_{DD}^2}{2\overline{R}_p} W_T \tag{3.7}$$

For more power, it is desirable to choose a large W_T, or equivalently a small R_L. However, if R_L is too small compared to 50 Ω, the bandwidth will be reduced by the impedance transformation network at the output. On the other hand, if W_T is too large, the bandwidth will be reduced by the large parasitic capacitors of the transistor. To be able to absorb large parasitic capacitors, large inductors should be used, which leads to a reduction in cut-off frequency. As can be seen, there is always a trade-off between power and bandwidth that one needs to consider carefully.

If C_{gi} represents the gate capacitor of the ith stage, the sum of all gate capacitors, C_{gT}, is given by:

$$C_{gT} \triangleq \sum_{i=1}^{n} C_{gi} = W_T \overline{C_g} \tag{3.8}$$

where $\overline{C_g}$ is the gate capacitor per unit transistor width for the given fabrication process.

If $C_{gT} < C_{fT}$, we need to provide an additional shunt capacitor at the input of each stage. On the other hand, if $C_{gT} > C_{fT}$ we need to insert a series capacitor between the stage input and the transistor gate to reduce the stage input capacitance. The former is not preferable, because it reduces the maximum power, P_m, of the amplifier. Note that C_{gT} is dependent on $\overline{R}_p$, R_{out} and $\overline{C_g}$, but not on N. Fortunately, it is possible to adjust the value of C_{fT} by choosing a proper value for N giving the optimum performance.

We state that all stages must have the same voltage gain for the appropriate addition of output power. Therefore, the gate capacitor of each stage should be proportional to the stage input capacitance with

$$C_{gi} = \frac{C_{gT}}{C_{fT}} C_{fi} \text{ for } i = 1, \ldots, N \tag{3.9}$$

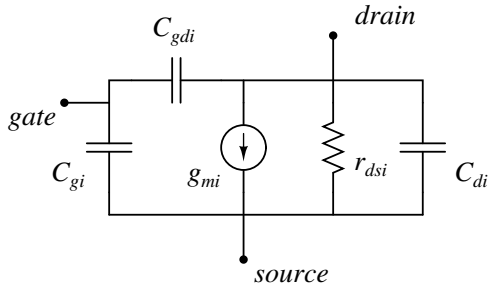

Figure 3.3: Transistor model showing the intrinsic parameters for the ith transistor.

We use the transistor model given in Fig. 3.3. We can determine the size of each transistor as

$$W_i = \frac{C_{gi}}{C_{gT}} W_T \text{ for } i = 1, \ldots, N \tag{3.10}$$

The drain capacitor, C_{di} of each transistor can be found from

$$C_{di} = W_i \overline{C_d} \text{ for } i = 1, \ldots, N \tag{3.11}$$

where $\overline{C_d}$ is the drain capacitor per unit width for the given process. In addition, the transconductance, g_{mi} of each transistor can be found from

$$g_{mi} = W_i \overline{g_m} \text{ for } i = 1, \ldots, N \tag{3.12}$$

where $\overline{g_m}$ is the transconductance per unit width for the given process. The drain-source resistor, r_{dsi} of each transistor can be found from

$$r_{dsi} = W_i \overline{r_{ds}} \text{ for } i = 1, \ldots, N \tag{3.13}$$

where $\overline{r_{ds}}$ is the drain-source resistor per unit width. The gate-drain capacitor, C_{gdi} of each transistor can be found from

$$C_{gdi} = W_i \overline{C_{gd}} \text{ for } i = 1, \ldots, N \tag{3.14}$$

where $\overline{C_{gd}}$ is the gate-drain capacitor per unit width.

The effective gate capacitor of each transistor using Miller effect is given by

$$C_{ei} = C_{gi} + (1 - A_v) C_{gdi} \text{ for } j = 1, \ldots, N \tag{3.15}$$

where voltage gain from gate to drain of the stage, A_v is

$$A_v = -\overline{g_m}(\overline{R_p} \,//\, \overline{r_{ds}}) \tag{3.16}$$

If $C_{ei} > C_{fi}$, which usually is the case, we need series gate capacitors (C_{si}) such that a series combination of C_{si} with C_{ei} gives C_{fi}. Therefore, we have

$$C_{si} = \frac{C_{ei} C_{fi}}{C_{ei} - C_{fi}} \text{ for } i = 1, \ldots, N \tag{3.17}$$

For proper phasing of output currents, the phase shifts at the input should equal the phase shifts at the output side. To determine the condition for phase equalization, nodal analysis is done to two C-L-C networks shown in Fig. 3.4 and Fig. 3.5.

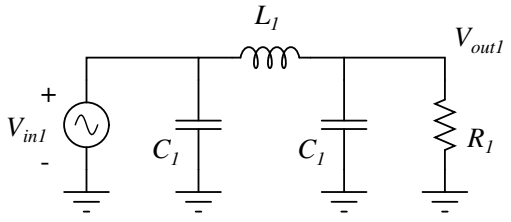

Figure 3.4: The first network used for nodal analysis.

From nodal analysis for the first network given in Fig. 3.4, we have

$$V_{out1}\left(\frac{1}{R_1}+jwC_1+\frac{1}{jwL_1}\right)-V_{in1}\left(\frac{1}{jwL_1}\right)=0 \tag{3.18}$$

$$\frac{V_{out1}}{V_{in1}}=\frac{1}{\frac{jwL_1}{R}-w^2L_1C_1+1} \tag{3.19}$$

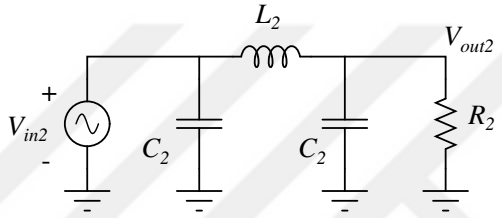

Figure 3.5: The second network used for nodal analysis.

From nodal analysis for the second network given in Fig. 3.5, we have

$$V_{out2}\left(\frac{1}{R_2}+jwC_2+\frac{1}{jwL_2}\right)-V_{in2}\left(\frac{1}{jwL_2}\right)=0 \tag{3.20}$$

$$\frac{V_{out2}}{V_{in2}}=\frac{1}{\frac{jwL_2}{R}}-w^2L_2C_2+1 \tag{3.21}$$

To equalize the phase shifts, we need to make

$$\frac{V_{out1}}{V_{in1}}=\frac{V_{out2}}{V_{in2}} \tag{3.22}$$

therefore, we need to have

$$\frac{L_1}{L_2}=\frac{R_1}{R_2} \tag{3.23}$$

and

$$\frac{C_1}{C_2}=\frac{L_2}{L_1}=\frac{R_2}{R_1} \tag{3.24}$$

Similar to the input C_e-L_e-C_e network, using 3.23 and 3.24, the output side is also formed with C_b-L_c-C_b, shown in Fig. 3.6, of which values can be found from

$$L_{di}=L_{fi}\frac{Z_{oi}}{Z_{ei}}\ \text{ for } i=1,\ldots,N-1 \tag{3.25}$$

$$C_{bi}=C_{fi}\frac{Z_{ei}}{Z_{oi}}\ \text{ for } i=1,\ldots,N-1 \tag{3.26}$$

so that the phase shift at the output is the same as that at the input. To find output node capacitors, neighboring capacitors are combined as

$$C_{ci} = \begin{cases} C_{b1} & \text{for } i = 1 \\ C_{b(i-1)} + C_{bi} & \text{for } i = 2, \ldots, (N-1) \\ C_{b(N-1)} & \text{for } i = N \end{cases} \tag{3.27}$$

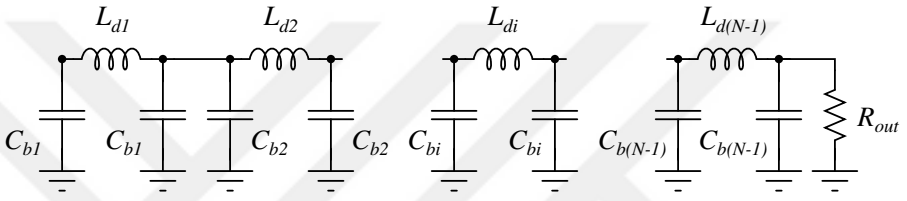

Figure 3.6: The schematic diagram of the intended output network.

To find the additional needed capacitors at the output nodes, we need to subtract the drain capacitors and gate-drain capacitors using Miller effect from the output node capacitors as

$$C_{ai} = C_{ci} - C_{di} - C_{gdi}\left(1 - \frac{1}{A_v}\right) \quad \text{for } i = 1, \ldots, N \tag{3.28}$$

If $C_{ai} < 1$, then we need to set $C_{ai} = 0$. This step creates a non-ideal behavior. To reduce the unwanted consequences of this behavior, it is possible to redefine the input impedances (Z_{ei}'s) in the first step of the procedure. Another approach could be to choose transistors or processes with smaller C_d's or C_{gd}'s. For example, it is possible to have $C_{gd} = 0$ by using cascode-connected transistors.

The final network is as shown in Fig. 3.7. An LC matching network, L_{in} and C_{pin}, is added to enhance S_{11}. To further improve the accuracy of the analysis, the resistive loss of the inductors can be included. If Q of the inductors is given at a certain frequency, the resistance of the inductors can be determined.

It is important to state that if the number of stages is increased, C_{fT} increases, and therefore C_{gi}'s and C_{ei}'s become smaller. In that case, we can use larger C_{si}'s which results in an increased gain. However, if C_{si}'s become too large, the frequency dependence of gain increases.

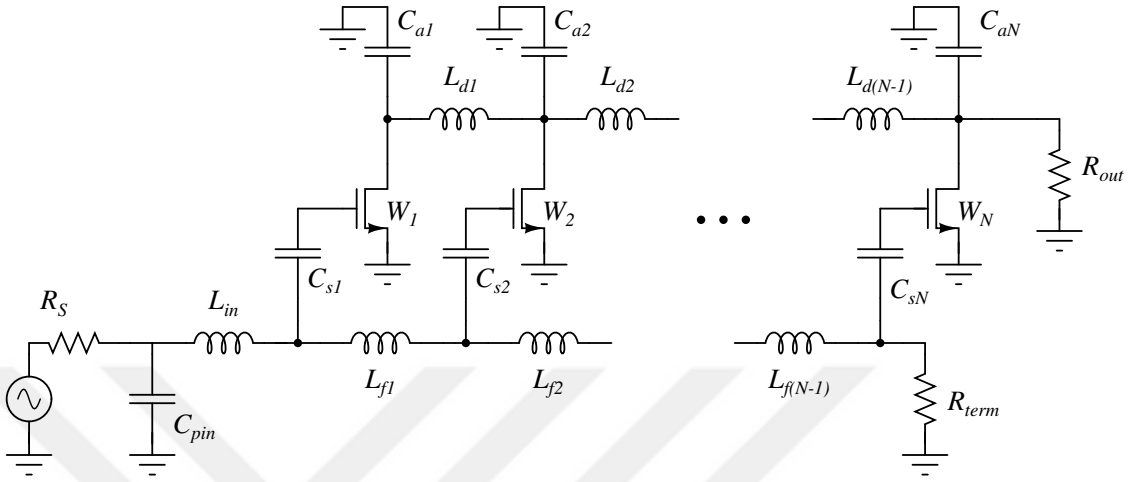

Figure 3.7: The schematic diagram of the final network.

Note that for the last stage, we find the termination impedance of the NDPA as specified in (3.6) as Z_N=R_{out}. This impedance should be transformed to a 50 Ω using a quarter-wavelength transmission line of characteristic impedance

$$Z_P = \sqrt{50 R_{out}} \tag{3.29}$$

3.2.1 Transmission line approximation to C-L-C networks

C-L-C networks can be implemented as transmission lines shown in Fig. 3.8. A C-L-C network acts like an impedance inverter and hence it can be replaced by a quarter-wave long transmission line. The conventional approximation to a C-L-C network is a quarter-wave transmission line of impedance

$$Z = \omega_0 L = \frac{1}{\omega_0 C} \tag{3.30}$$

where w_0 is the frequency of operation.

To have the transmission line (TL) equivalency of a C-L-C network in a large band, the following analysis is done:

For a given transmission line, we have

$$LC = \frac{1}{w_o^2} \text{ and } R = Z = \sqrt{\frac{L}{C}} \text{ when } \frac{l}{\lambda} = \frac{1}{4} \text{ at } w_0 \tag{3.31}$$

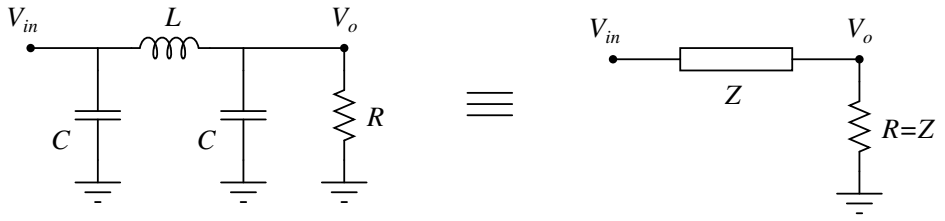

Figure 3.8: The schematic diagram of a C-L-C network.

From a nodal analysis to the C-L-C network in Fig. 3.8,

$$\frac{V_o}{V_{in}} = \frac{1}{1 - \left(\frac{w}{w_0}\right)^2 + j\frac{wL}{R}} \tag{3.32}$$

and from the TL network in Fig. 3.8,

$$\frac{V_o}{V_{in}} = e^{-j\frac{2\pi}{\lambda}l} = \cos\left(\frac{2\pi}{\lambda}l\right) - j\sin\left(\frac{2\pi}{\lambda}l\right) \tag{3.33}$$

To have the equivalency between two networks,

$$\frac{1 - \left(\frac{w}{w_0}\right)^2}{\left(1 - \left(\frac{w}{w_0}\right)^2\right)^2 + \left(\frac{wL}{R}\right)^2} = \cos\left(\frac{2\pi}{\lambda}l\right) \tag{3.34}$$

and

$$\frac{\frac{wL}{R}}{\left(1 - \left(\frac{w}{w_0}\right)^2\right)^2 + \left(\frac{wL}{R}\right)^2} = \sin\left(\frac{2\pi}{\lambda}l\right) \tag{3.35}$$

Note that the equivalency between C-L-C network and transmission line is perfect if $\omega L = R$ and at $\omega = \omega_0$. However, we are interested in a large band of frequencies less than w_0 and the resulting transmission line impedance found above may be unrealizable.

Let Z_m be the maximum TL impedance that can be realized. To realize an inductance of L, we use Z_m as a TL section shown in Fig. 3.9. With an optimization procedure it is possible to find best values of transmission line length to approximate the inductor, L, using this transmission line of impedance Z_m

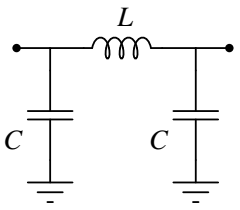

Figure 3.9: A TL section having an impedance of Z_m with cut-off frequency at w_r

with corresponding capacitors on both ends. The transfer functions of C-L-C and optimized TL are given in Fig. 3.10.

Cut-off frequency of this section is found as

$$w_r \approx \frac{1.22 Z_m}{L} \tag{3.36}$$

Corresponding capacitors are

$$C = \frac{1}{w_r^2 L} \tag{3.37}$$

The length of the transmission line in $\frac{l}{\lambda_2}$ units is

$$\frac{l}{\lambda_2} \approx 0.23 \frac{\omega_2}{\omega_r} \tag{3.38}$$

where λ_2 is λ at w_2 which is the highest frequency of operation. The choices above provides the smallest meas-square error between the transmission line and the C-L-C network for the frequencies less than ω_2. For each inductor in the NDPA, transmission lines can be used. The capacitors of approximation will consume some node capacitors. A comparison of real and imaginary parts of transfer function of both networks is given in Fig. 3.10. We note that the factor of 0.23 in Eq. 3.38 should be modified to 0.20 if $w_r \gg w_2$.

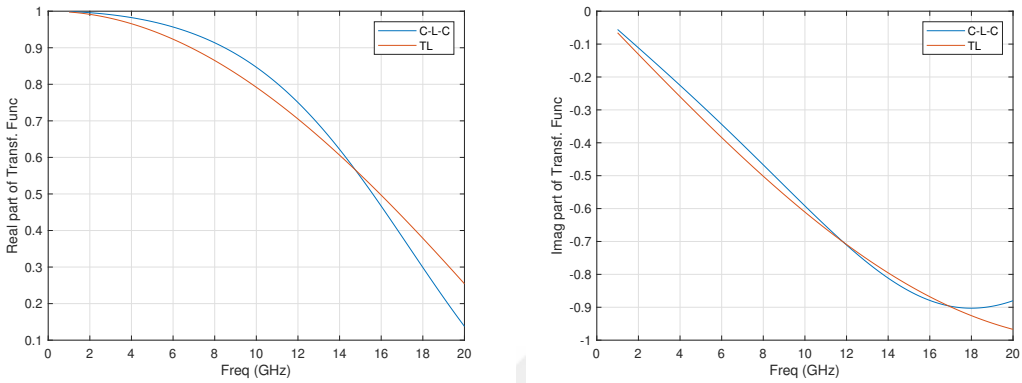

Figure 3.10: Real (left) and imaginary (right) parts of the transfer function of a C-L-C network and a transmission line

3.3 Example Designs

To demonstrate the use of our method, we give a number of NDPA designs as examples.

3.3.1 Example 1

As the first example, following the design procedure given in Section 3.2, we determine the component values of a 2−18 GHz NDPA for N=10, $\overline{R}_p$=120 Ω.mm, $\overline{C}_g$=1.87 pF/mm, $\overline{C}_d$=0.3 pF/mm, $\overline{C}_{gd}$=0.076 pF/mm, $\overline{g}_m$=0.288 mS/mm, $\overline{R}_{ds}$=378 Ω.mm, R_{term} =45 Ω, R_{out} =35 Ω, Z_e=50 (except for the first network, Z_{e1}=35), and f_u=22 GHz. The example designs are realized using both lumped elements (C-L-C networks), and transmission lines.

3.3.1.1 Lumped Element Realization

Corresponding component values of the input side and output side for the lumped element realization are given in Table 3.1. An LC matching with L_{in} and C_{pin} is

done at the input to further improve S_{11}.

Note that some capacitance values are negative which are not realizable. We performed a harmonic balance simulation by setting the negative values to zero and the results are presented in Fig. 3.11. The non-linear transistor models provided by Win Semiconductor are utilized. While the performance of the NDPA degrades towards high frequencies, the results can be considered reasonable since very simple transistor models are used and no optimization is performed.

Input Side Comp.				Output Side Comp.				Tran.	
L_{f1}	0.31	C_{s1}	0.203	C_{a1}	-0.085	L_{d1}	4.07	W_1	260
L_{f2}	0.44	C_{s2}	0.345	C_{a2}	-0.12	L_{d2}	1.51	W_2	441
L_{f3}	0.44	C_{s3}	0.284	C_{a3}	-0.049	L_{d3}	0.99	W_3	363
L_{f4}	0.44	C_{s4}	0.284	C_{a4}	-0.014	L_{d4}	0.74	W_4	363
L_{f5}	0.44	C_{s5}	0.284	C_{a5}	0.022	L_{d5}	0.59	W_5	363
L_{f6}	0.44	C_{s6}	0.284	C_{a6}	0.058	L_{d6}	0.49	W_6	363
L_{f7}	0.44	C_{s7}	0.284	C_{a7}	0.094	L_{d7}	0.42	W_7	363
L_{f8}	0.44	C_{s8}	0.284	C_{a8}	0.13	L_{d8}	0.37	W_8	363
L_{f9}	0.44	C_{s9}	0.284	C_{a9}	0.166	L_{d9}	0.33	W_9	363
		C_{s10}	0.142	C_{a10}	0.092			W_{10}	181

Table 3.1: Input side component values (inductors in nH, capacitors in pF) with L_{in}=0.3 nH and C_{pin}=0.14 pF, output side component values (inductors in nH, capacitors in pF) and the gate width of the transistors (in μm) of Example 1

In most design cases, a lot of effort is made in the optimization step. It is crucial to have reasonable component values to be used for optimization in order not to face with convergence issues. It is indeed even more crucial for the design of distributed amplifiers because usually there are tens of parameters to be optimized. Due to the nature of the operation of distributed amplifiers, nearly all parameters are linked to each other, which makes reaching the optimum solution

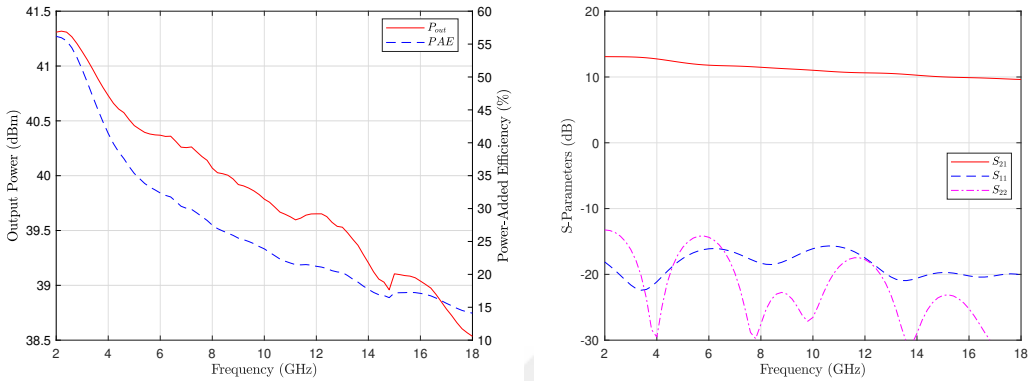

Figure 3.11: Harmonic balance and small signal simulation results of Example 1 implemented using lumped components: Output power and power-added efficiency (left) and s-parameters (right) as a function of frequency.

harder for the optimizer. Without reasonable values, it is very usual that either the optimizer would not reach a convergence or it would reach a less-optimal solution.

However, by following the design procedure given in Section 3.2, we are able to get reasonable values offering promising results. Fig. 3.11 shows more than 10 W of output power while having 20% of power-added efficiency over 2–18GHz without any tuning or optimization. The results can be improved further by optimizer using these component values as initial parameters.

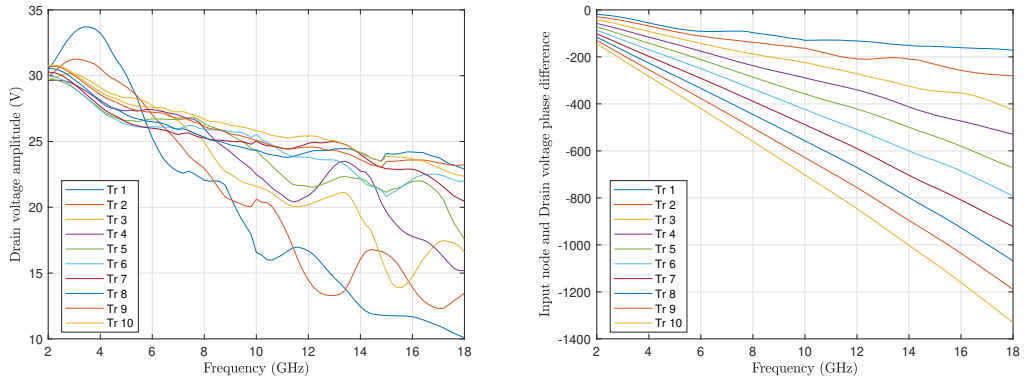

Figure 3.12: Drain voltage amplitude (left) and phase difference between the input node and drain voltage (right) of each transistor in Example 1 implemented using lumped components as a function of frequency.

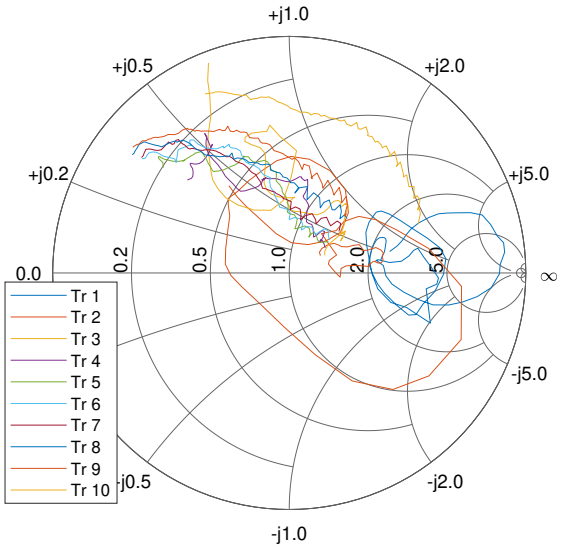

Figure 3.13: Drain impedance experienced by each transistor in Example 1 as a function of frequency parameter for lumped element realization with the Smith chart reference impedance of $Z_{ref} = 200\ \Omega$.

3.3.1.2 Transmission Line Realization

Corresponding component values of the input side and output side for the transmission line realization are given in Table 3.2. We performed a harmonic balance simulation by setting the impedance of the gate and drain transmission lines to 100 Ω, and the results are presented in Fig. 3.14. Drain voltage amplitude and the phase difference between the input node and drain voltage are given in Fig. 3.15. The impedances seen by the transistors are given in Fig. 3.16. Note that the first few transistors experience negative real part load values at high frequencies due to nonideal behavior resulting from zeroing of negative valued capacitors. A negative real part load impedance means that the corresponding transistor absorbs some of the output power rather than contributing to output power. Obviously, this undesired effect reduces the gain and power output of the NDPA at the high-frequency end of the band. The Smith chart presentation for the ideal case when the transistors do not have any drain capacitors ($C_d = 0$) and any gate-to-drain capacitors ($C_{gd} = 0$) are presented in Fig. 3.17.

Input Side Comp.				Output Side Comp.				Tran.	
l_{g1}	0.0573	C_{s1}	0.17	C_{a1}	-0.337	l_{d1}	0.6628	W_1	296
l_{g2}	0.0818	C_{s2}	0.27	C_{a2}	-0.458	l_{d2}	0.2551	W_2	473
l_{g3}	0.0818	C_{s3}	0.2	C_{a3}	-0.195	l_{d3}	0.1747	W_3	354
l_{g4}	0.0818	C_{s4}	0.2	C_{a4}	-0.116	l_{d4}	0.1328	W_4	354
l_{g5}	0.0818	C_{s5}	0.2	C_{a5}	-0.056	l_{d5}	0.1071	W_5	354
l_{g6}	0.0818	C_{s6}	0.2	C_{a6}	-0.005	l_{d6}	0.0898	W_6	354
l_{g7}	0.0818	C_{s7}	0.2	C_{a7}	0.040	l_{d7}	0.0772	W_7	354
l_{g8}	0.0818	C_{s8}	0.2	C_{a8}	0.083	l_{d8}	0.0678	W_8	354
l_{g9}	0.0818	C_{s9}	0.2	C_{a9}	0.124	l_{d9}	0.0604	W_9	354
		C_{s10}	0.1	C_{a10}	0.072			W_{10}	177

Table 3.2: Input side component values (length of the 100 Ω input transmission lines in λ_2 units, capacitors in pF) with L_{in}=0.3 nH and C_{pin}=0.14 pF, output side component values (length of the 100 Ω output transmission lines in λ_2 units with f=18 GHz, capacitors in pF) and the gate width of the transistors (in μm) of Example 1 realized with transmission lines

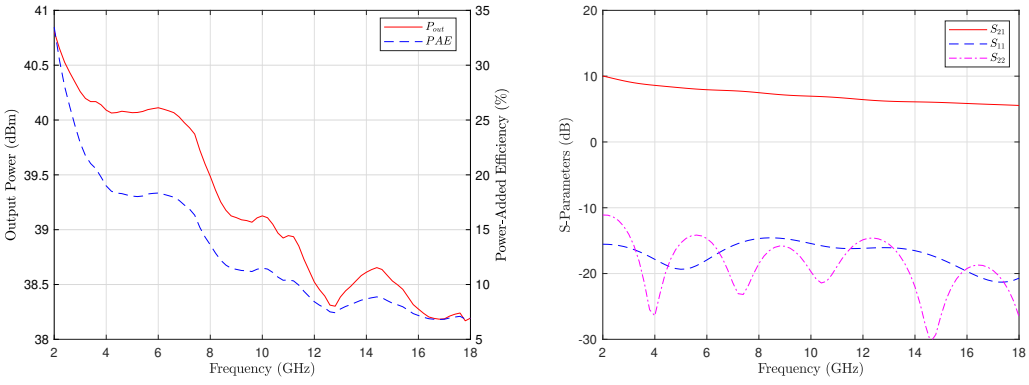

Figure 3.14: Harmonic balance and small signal simulation results of Example 1 implemented using transmission lines: Output power and power-added efficiency (left) and s-parameters (right) as a function of frequency.

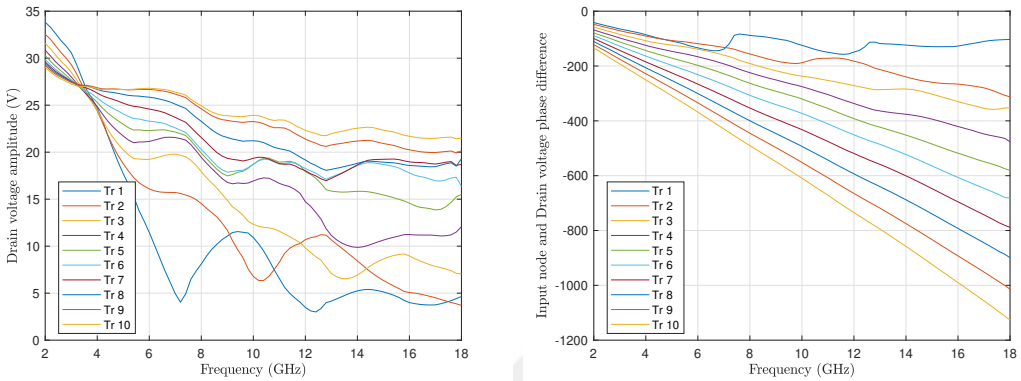

Figure 3.15: Drain voltage amplitude (left) and phase difference between input node and drain voltage (right) of each transistor in Example 1 implemented using transmission lines as a function of frequency.

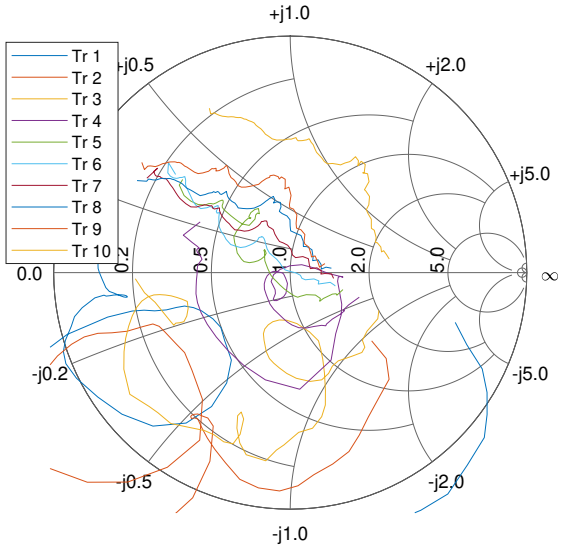

Figure 3.16: Drain impedance seen by each transistor as frequency is varied for transmission line realization with $Z_{ref} = 200\ \Omega$. Note the presence of negative real part impedances for the first few transistors at high frequencies.

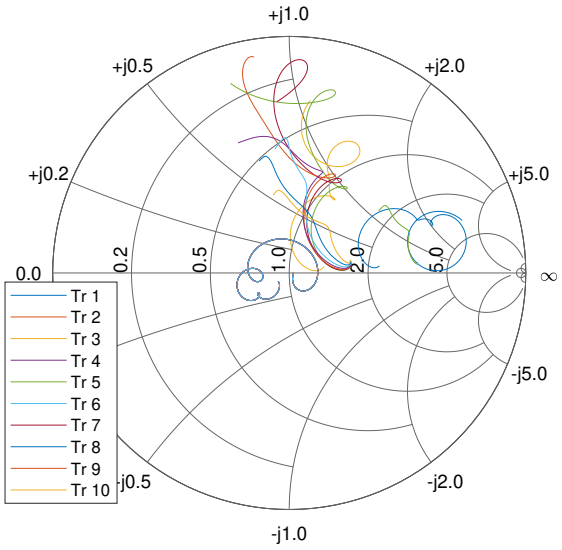

Figure 3.17: Drain impedance experienced by each transistor in Example 1 as a function of frequency parameter for TL realization with $C_d = 0$ and $C_{gd} = 0$, and with $Z_{ref} = 200\ \Omega$.

3.3.2 Example 2

As the second example, following the design procedure given in the previous section, we determine the component values of a 2−6 GHz NDPA for N=6, $\overline{R}_p$=120 Ω.mm, $\overline{C}_g$=1.87 pF/mm, $\overline{C}_d$=0.3 pF/mm, $\overline{C}_{gd}$=0.076 pF/mm, $\overline{g}_m$=0.288 mS/mm, $\overline{R}_{ds}$=378 Ω.mm, R_{term} =45 Ω, R_{out} =35 Ω, Z_e=50 Ω (except for the first network, Z_{e1}=35 Ω), and f_u=8 GHz.

As Example 1, Example 2 design is realized using both lumped elements (C-L-C networks), and transmission lines.

3.3.2.1 Lumped Element Realization

Corresponding component values of the input side and output side for the lumped element realization are given in Table 3.3.

In this example, we encounter negative capacitance values again. The main

reason for this is the drain capacitors of the process. A process or a transistor structure with a smaller drain capacitance will not have this problem. After performing a harmonic balance simulation, we present the large-signal and small-signal results in Fig. 3.18. Again, the results are acceptable as the first step of the design process.

Input Side Comp.				Output Side Comp.				Tran.	
L_{f1}	0.85	C_{s1}	0.631	C_{a1}	-0.108	L_{d1}	6.45	W_1	451
L_{f2}	1.21	C_{s2}	1.07	C_{a2}	-0.061	L_{d2}	2.39	W_2	766
L_{f3}	1.21	C_{s3}	0.884	C_{a3}	0.179	L_{d3}	1.57	W_3	631
L_{f4}	1.21	C_{s4}	0.884	C_{a4}	0.351	L_{d4}	1.17	W_4	631
L_{f5}	1.21	C_{s5}	0.884	C_{a5}	0.522	L_{d5}	0.935	W_5	631
		C_{s6}	0.442	C_{a6}	0.304			W_6	316

Table 3.3: Input side component values (inductors in nH, capacitors in pF) with L_{in}=0.3 nH and C_{pin}=0.14 pF, output side component values (inductors in nH, capacitors in pF) and the gate width of the transistors (in μm) of Example 2

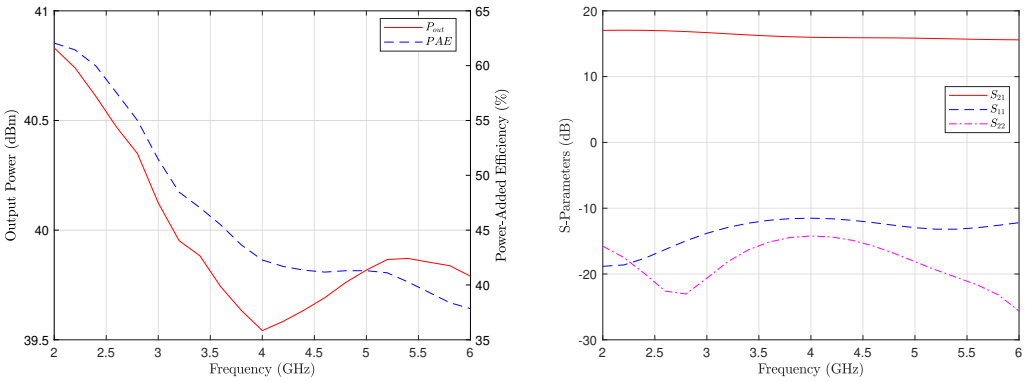

Figure 3.18: Harmonic balance and small signal simulation results of Example 2 implemented using lumped elements: Output power and power-added efficiency (left) and s-parameters (right) as a function of frequency.

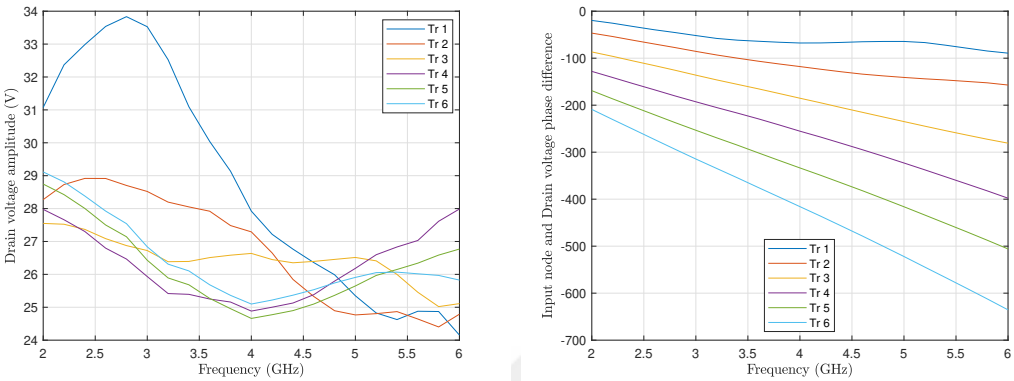

Figure 3.19: Drain voltage amplitude (left) and phase difference between input node and drain voltage (right) of each transistor in Example 2 implemented using lumped elements as a function of frequency.

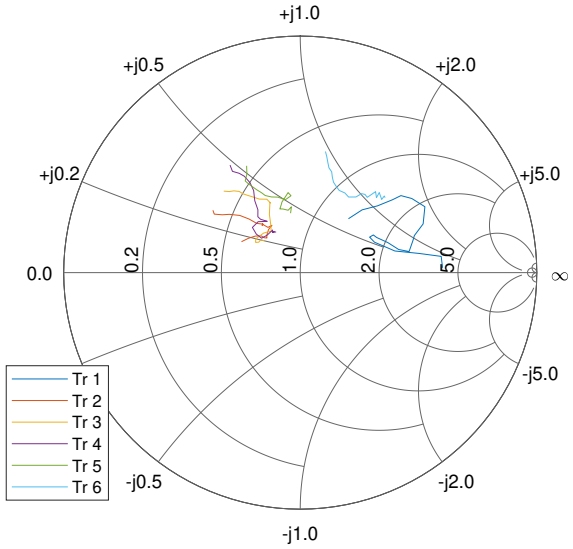

Figure 3.20: Drain impedance experienced by each transistor in Example 2 as a function of frequency parameter for lumped element realization with $Z_{ref} = 200\ \Omega$.

3.3.2.2 Transmission Line Realization

Following the design procedure, corresponding component values of the input side and output side for the transmission line realization are given in Table 3.4. With existing GaN on SiC processes, the maximum realizable characteristic impedance for a microstrip transmission line is usually about 110 Ω. Therefore, the characteristic impedances of gate and drain transmission lines are set to 100 Ω. Harmonic balance simulation is done, and the results are presented in Fig. 3.21. Drain voltage amplitude and the phase difference between the input node and drain voltage are also given in Fig. 3.22. From this figure, it can be seen that the first transistor is poorly loaded due to the large negative capacitance value, which can also be observed as negative impedance in Fig. 3.23.

Input Side Comp.				Output Side Comp.				Tran.	
l_{g1}	0.0525	C_{s1}	0.51	C_{a1}	-0.508	l_{d1}	0.3563	W_1	505
l_{g2}	0.0750	C_{s2}	0.82	C_{a2}	-0.59	l_{d2}	0.1371	W_2	807
l_{g3}	0.0750	C_{s3}	0.61	C_{a3}	-0.039	l_{d3}	0.0939	W_3	604
l_{g4}	0.0750	C_{s4}	0.61	C_{a4}	0.196	l_{d4}	0.0714	W_4	604
l_{g5}	0.0750	C_{s5}	0.61	C_{a5}	0.4	l_{d5}	0.0576	W_5	604
		C_{s6}	0.307	C_{a6}	0.248			W_6	302

Table 3.4: Input side component values (length of the 100 Ω transmission line in λ_2 units, capacitors in pF) with L_{in}=0.3 nH and C_{pin}=0.14 pF, output side component values (length of the 100 Ω transmission line in λ_2 units with f_2=6 GHz, capacitors in pF) and the gate width of the transistors (in μm) of Example 2 realized with transmission lines

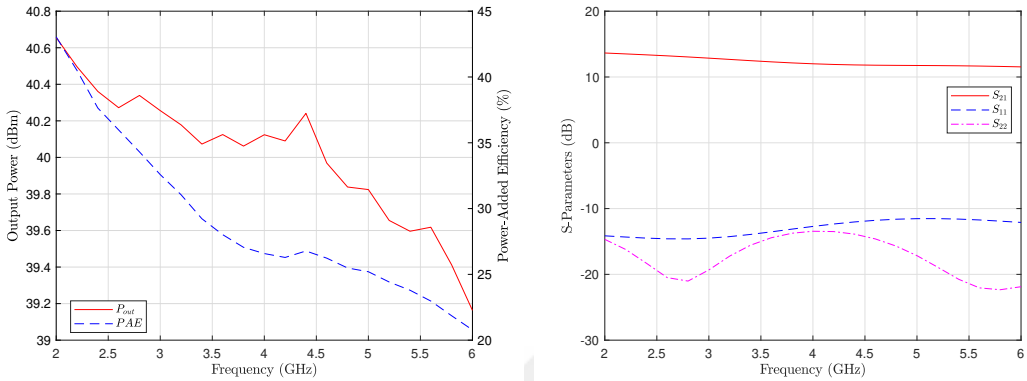

Figure 3.21: Harmonic balance and small signal simulation results of Example 2 implemented using transmission lines: Output power and power-added efficiency (left) and s-parameters (right) as a function of frequency.

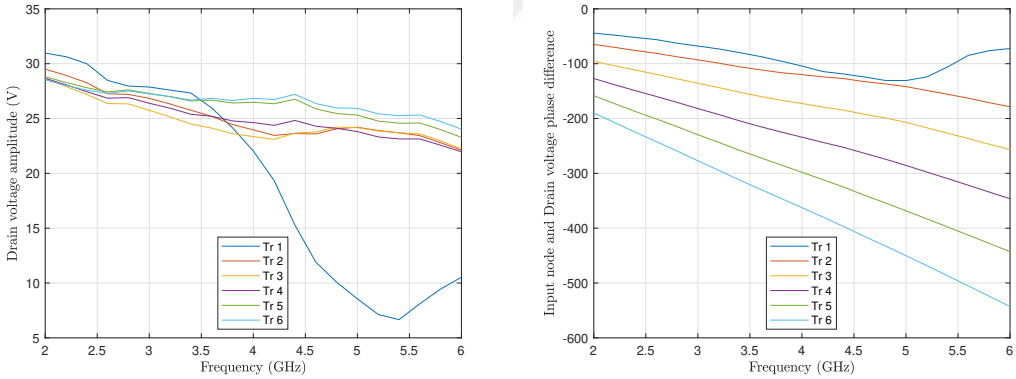

Figure 3.22: Drain voltage amplitude (left) and phase difference between input node and drain voltage (right) of each transistor in Example 2 implemented using transmission lines as a function of frequency.

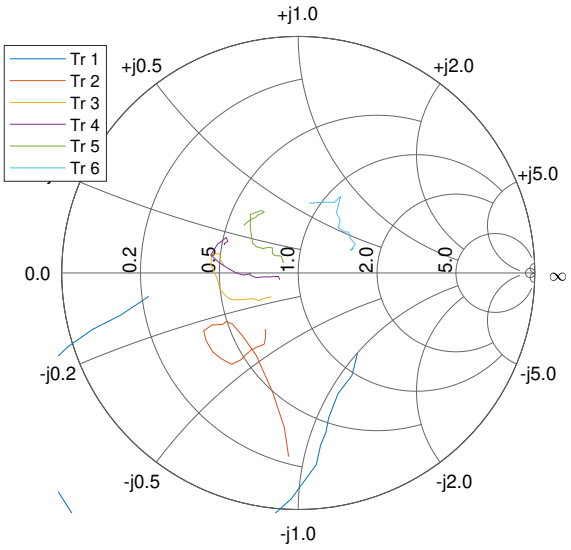

Figure 3.23: Drain impedance experienced by each transistor in Example 1 as a function of frequency parameter for transmission line realization with Z_{ref} = 200 Ω.

3.3.3 Example 3

As the third and last example, following the design procedure given at the beginning of this chapter, we determine the component values of a 1−8 GHz NDPA for N=8, $\overline{R}_p$=120 Ω.mm, $\overline{C}_g$=1.87 pF/mm, $\overline{C}_d$=0.3 pF/mm, $\overline{C}_{gd}$=0.076 pF/mm, $\overline{g}_m$=0.288 mS/mm, $\overline{R}_{ds}$=378 Ω.mm, R_{term} =45 Ω, R_{out} =35 Ω, Z_e=50 Ω (except for the first network, Z_{e1}=35 Ω), and f_u=10 GHz.

The example designs are realized using both lumped elements (C-L-C networks), and transmission lines.

3.3.3.1 Lumped Element Realization

Corresponding component values of the input side and output side for the lumped element realization are given in Table 3.5.

For lumped element realization, it is relatively easy to obtain proper phase matching and absorption of capacitances, which can be seen from the number of negative capacitances in the given table. We need to set those negative capacitances to zero to run a proper harmonic balance simulation, and the results are presented in Fig. 3.24. The scalable non-linear transistor models provided by Win Semiconductor are used.

Input Side Comp.				Output Side Comp.				Tran.	
L_{f1}	0.679	C_{s1}	0.522	C_{a1}	-0.088	L_{d1}	7.07	W_1	330
L_{f2}	0.970	C_{s2}	0.88	C_{a2}	-0.078	L_{d2}	2.61	W_2	560
L_{f3}	0.970	C_{s3}	0.73	C_{a3}	0.070	L_{d3}	1.72	W_3	461
L_{f4}	0.970	C_{s4}	0.73	C_{a4}	0.017	L_{d4}	1.28	W_4	461
L_{f5}	0.970	C_{s5}	0.73	C_{a5}	0.027	L_{d5}	1.02	W_5	461
L_{f6}	0.970	C_{s6}	0.73	C_{a6}	0.371	L_{d6}	0.85	W_6	461
L_{f7}	0.970	C_{s7}	0.73	C_{a7}	0.471	L_{d7}	0.73	W_7	461
		C_{s8}	0.37	C_{a8}	0.26			W_8	231

Table 3.5: Input side component values (inductors in nH, capacitors in pF) with L_{in}=0.3 nH and C_{pin}=0.14 pF, output side component values (inductors in nH, capacitors in pF) and the gate width of the transistors (in μm) of Example 3

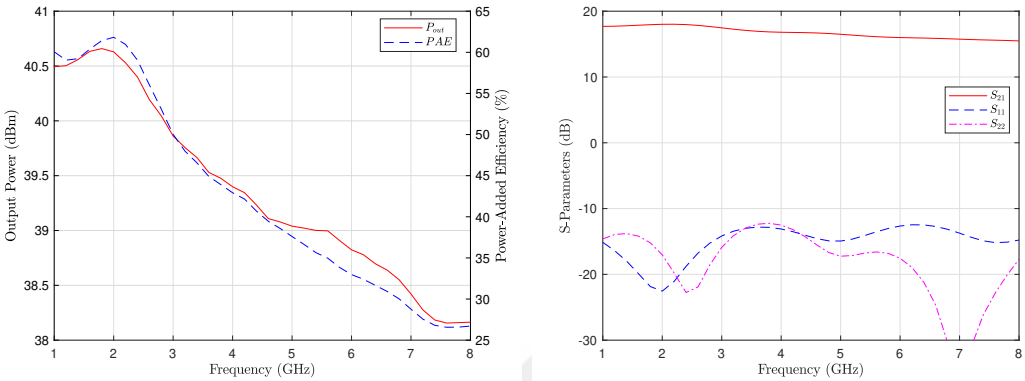

Figure 3.24: Harmonic balance and small signal simulation results of Example 3 implemented using lumped elements: Output power and power-added efficiency (left) and s-parameters (right) as a function of frequency.

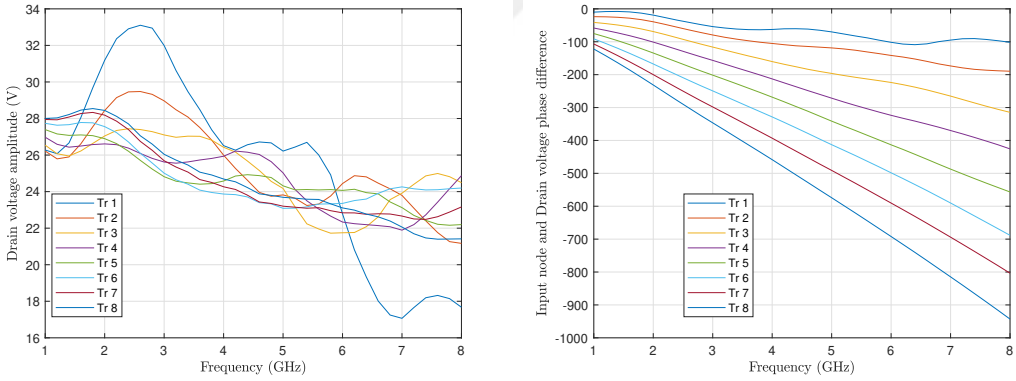

Figure 3.25: Drain voltage amplitude (left) and phase difference between input node and drain voltage (right) of each transistor in Example 3 implemented using lumped elements as a function of frequency.

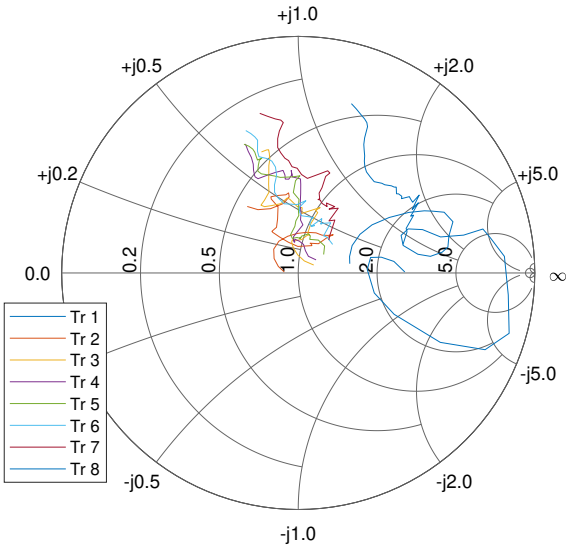

Figure 3.26: Drain impedance experienced by each transistor in Example 3 as a function of frequency parameter for lumped element realization with $Z_{ref} = 200\ \Omega$.

3.3.3.2 Transmission Line Realization

As the last example for transmission line realization, component values of the input side and output side are given in Table 3.6. Note that the number of negative capacitances is doubled compared to the lumped element realization. After running a harmonic balance simulation with a characteristic impedance of 100 Ω for both gate and drain transmission lines, it can be observed that the first two transistors are poorly loaded as expected from the given table. The drain voltage amplitudes in Fig. 3.28 also indicate the corresponding poorly loaded transistors. Furthermore, the drain impedances seen by the transistors are given in Fig. 3.29.

Input Side Comp.				Output Side Comp.				Tran.	
l_{g1}	0.056	C_{s1}	0.42	C_{a1}	-0.52	l_{d1}	0.5141	W_1	373
l_{g2}	0.08	C_{s2}	0.67	C_{a2}	-0.66	l_{d2}	0.1978	W_2	596
l_{g3}	0.08	C_{s3}	0.5	C_{a3}	-0.18	l_{d3}	0.1355	W_3	447
l_{g4}	0.08	C_{s4}	0.5	C_{a4}	-0.005	l_{d4}	0.1030	W_4	447
l_{g5}	0.08	C_{s5}	0.5	C_{a5}	0.13	l_{d5}	0.0831	W_5	447
l_{g6}	0.08	C_{s6}	0.5	C_{a6}	0.26	l_{d6}	0.0696	W_6	447
l_{g7}	0.08	C_{s7}	0.5	C_{a7}	0.37	l_{d7}	0.0599	W_7	447
		C_{s8}	0.25	C_{a8}	0.21			W_8	223

Table 3.6: Input side component values (length of the 100 Ω transmission line in λ_2 units, capacitors in pF) with L_{in}=0.3 nH and C_{pin}=0.14 pF, output side component values (length of the 100 Ω transmission line in λ_2 units with f_2=8 GHz, capacitors in pF) and the gate width of the transistors (in μm) of Example 3 realized with transmission lines

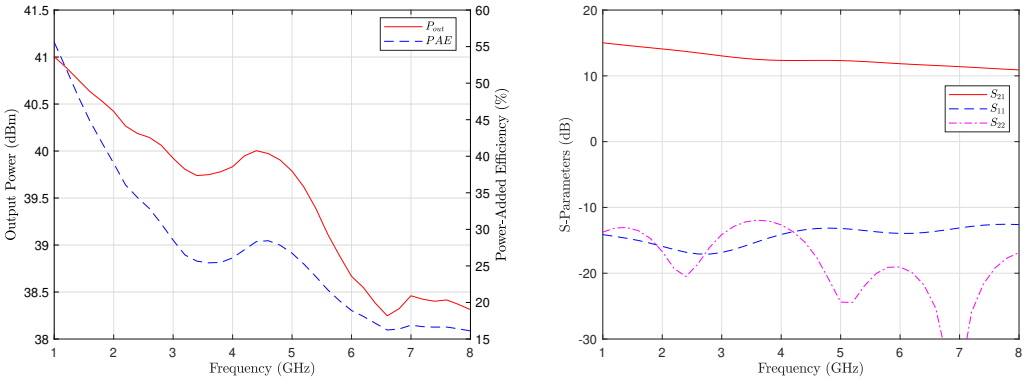

Figure 3.27: Harmonic balance and small signal simulation results of Example 3 implemented using transmission lines: Output power and power-added efficiency (left) and s-parameters (right) as a function of frequency.

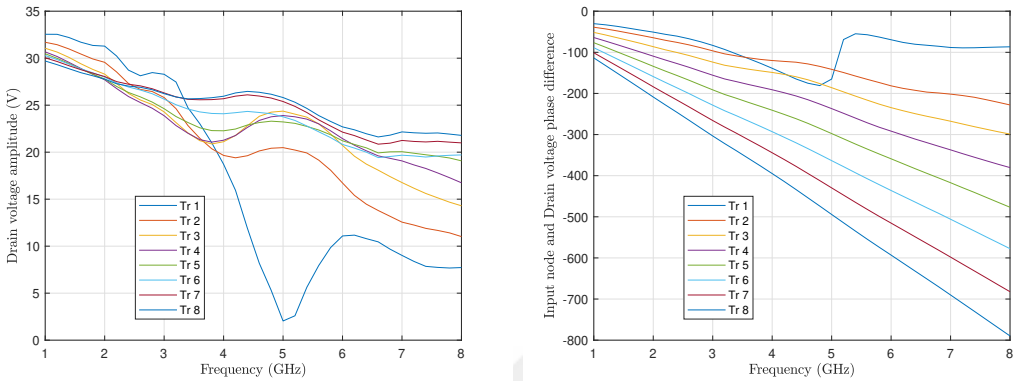

Figure 3.28: Drain voltage amplitude (left) and phase difference between input node and drain voltage (right) of each transistor in Example 3 implemented using transmission lines as a function of frequency.

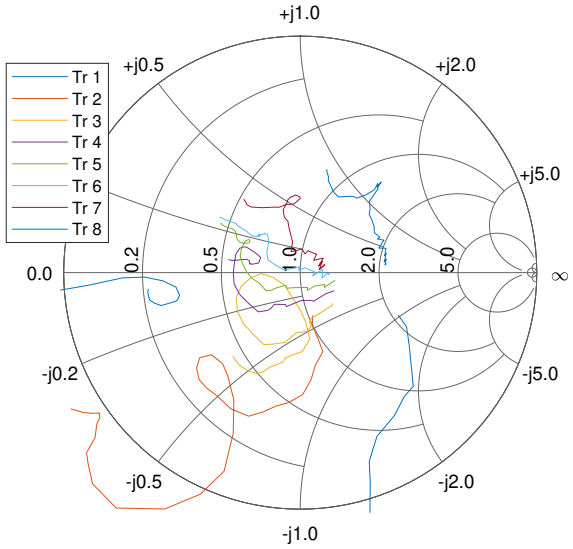

Figure 3.29: Drain impedance experienced by each transistor in Example 3 as a function of frequency parameter for transmission realization with $Z_{ref} = 200\ \Omega$.

Chapter 4

Distributed Choke Inductor

4.1 Spiral Inductor

Any broadband amplifier requires an RF choke with a high inductance value that is resonance-free across the desired frequency range. In most MMIC amplifiers, RF choke is implemented by on-chip inductors. They are also often used as drain bias choke in distributed power amplifiers because of their large bandwidth and relatively small size. Off-chip inductors are not practical because of the band-limiting effect of bonding pad capacitance. A simplified model is necessary to fully analyze how the amplifier bandwidth is actually affected by the bias choke inductor. We chose a circular spiral rather than a rectangular spiral since the current crowding at the corners of the rectangular spiral gives rise to additional parasitic capacitance.

For characterization purposes, several spiral inductors optimized with EM simulations are fabricated using a 0.25μm GaN on SiC process[1], one of which is shown in Fig. 4.1, where air bridges are used to connect to the center of the inductor. Two-port S-parameter measurements are carried out for the complete characterization of inductors.

[1]Win Semiconductors Corp., Taiwan.

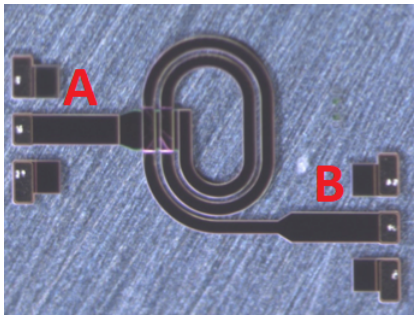

Figure 4.1: A spiral inductor fabricated with a 0.25 μm process.

Subsequently, inductors are simulated in a bias-tee configuration with one port shorted to ground as depicted in Fig. 4.2. Inductor manufacturers prefer the bias-tee configuration to demonstrate their choke inductors intended for biasing an amplifier.

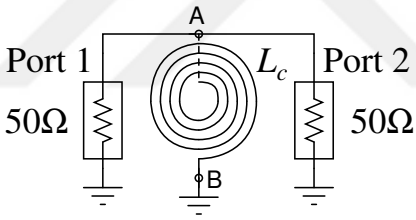

Figure 4.2: Method of characterization for a spiral inductor

A lumped element circuit model for a circular spiral inductor is shown in Fig. 4.3 [23], where L_c is the total inductance, k is the coupling coefficient, and M is the mutual inductance between the two coils given as

$$L_c = L_1 + L_2 + 2M \qquad M = k\sqrt{L_1 L_2} \tag{4.1}$$

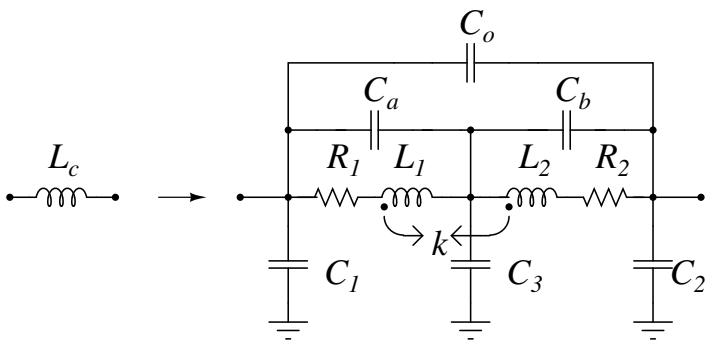

Figure 4.3: Inductor model showing the parasitics.

The model parameters can be found with the aid of a CAD tool by fitting the measurement data. The loss and series resonance frequency (SRF) are easily seen as reductions or dips in $|S_{21}|$ as presented in Fig. 4.4.

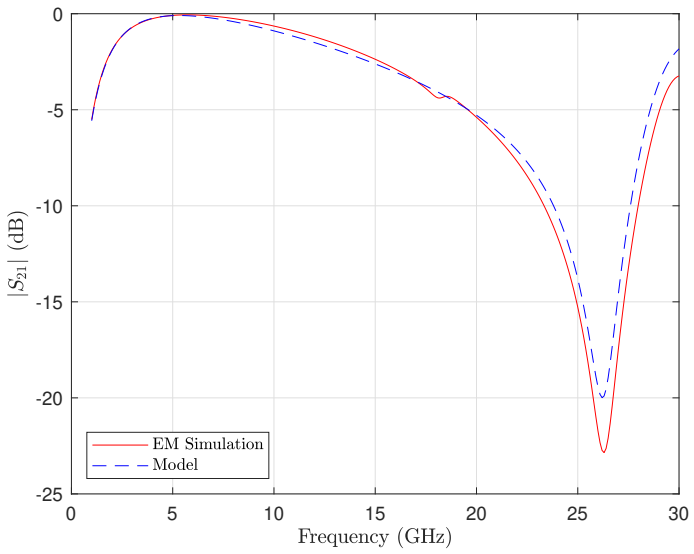

Figure 4.4: Dashed line: $|S_{21}|$ as obtained from EM simulation of S-parameters of a shorted 2.7 nH inductor with a conductor width of $w_c = 60$ μm and parallel connected air bridges having a total width of 109 μm. Solid line: $|S_{21}|$ as obtained from the inductor's model with L_1=0.3 nH, L_2=1.9 nH, k=0.31, $C_o + C_1$=270 fF and $C_a + C_b + C_3$=190 fF.

The figure also shows the calculated $|S_{21}|$ from the model parameters. The

frequency of the SRF dip, f_s, observed in the figure can be found by:

$$f_s = \frac{1}{2\pi}\left(\frac{L_c}{(L_1L_2 - M^2)(C_a + C_b + C_3)}\right)^{1/2} \tag{4.2}$$

Clearly, $C_a + C_b + C_3$ is a critical parasitic factor.

The parasitic capacitors, $C_a + C_b + C_3$, and SRF of a L_c=4.8 nH inductor are plotted as a function of line width in Fig. 4.5.

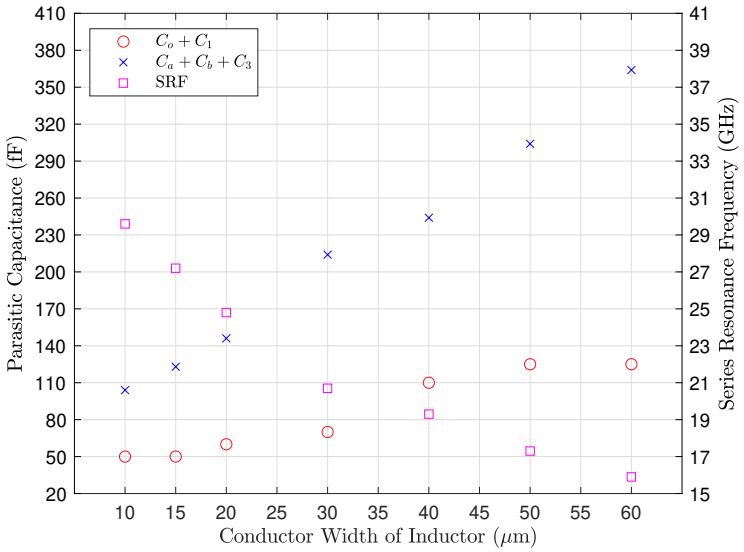

Figure 4.5: Parasitic capacitances, $C_o + C_1$ and $C_a + C_b + C_3$, and SRF for a L_c=4.8 nH inductor as a function of conductor width.

We observe that choosing a small conductor width effectively reduces $C_a + C_b + C_3$ and increases SRF as shown Fig. 4.6.

However, that selection results in higher series resistance, $R_1 + R_2$, and lowers the maximum current it can carry. From all these simulation results of many spiral inductors, we find the series resonance frequency, f_s, as a function of conductor width, w_c (μm), and inductor value, L_c (nH) as

$$f_s \text{ (GHz)} \approx \frac{300}{w_c^{0.4} L_c^{0.8}} \quad \text{for} \quad w_c < 60\mu\text{m} \tag{4.3}$$

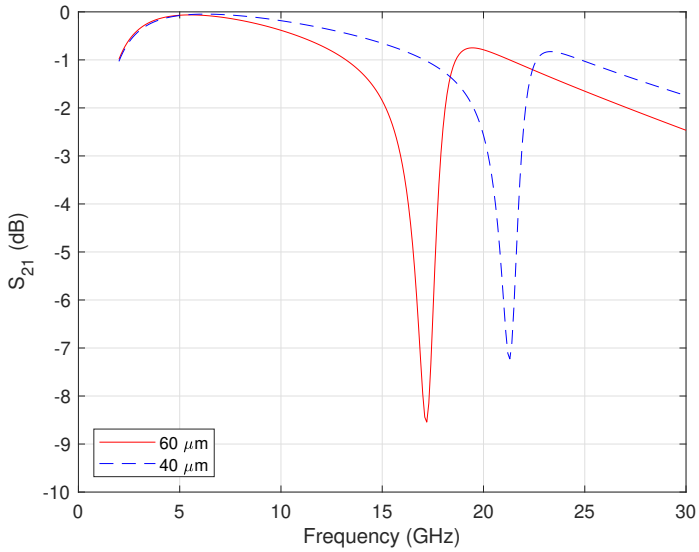

Figure 4.6: Effect of spiral inductor line width on the performance.

Note that for all inductors, the spacing between the conductors is 5 μm, the minimum value for the process technology.

Another source of loss at high frequencies is the total shunt parasitic capacitor of the inductor, $C_p = C_o + C_1$. The values of these parasitics are also given in Fig. 4.5 as a function of conductor width. Furthermore, from these results, C_p can be written for our process as

$$C_p \text{ (fF)} \approx 1.8 w_c^{0.9} L_c^{0.5} \text{ for } w_c < 23\mu\text{m} \tag{4.4}$$

The calculated $|S_{21}|$ for a single inductor when $C_p = C_o + C_1$ is artificially removed from the model is shown in Fig. 4.7. As can be seen, C_p influences the loss at the high-frequency side of the band. Elimination of C_p improves the performance at high frequencies.

For example, with w_c=18 μm and L_c=2.7 nH, f_s=35.5 GHz and C_p=40 fF with a current limit of I_c=0.35 A. Note that the current limit of the inductor is determined by the current limit of the air bridges used to connect to the center of the inductor. The current limit for air bridge metal is 23.44 mA/μm, and its width is 3 μm less than the conductor width w_c.

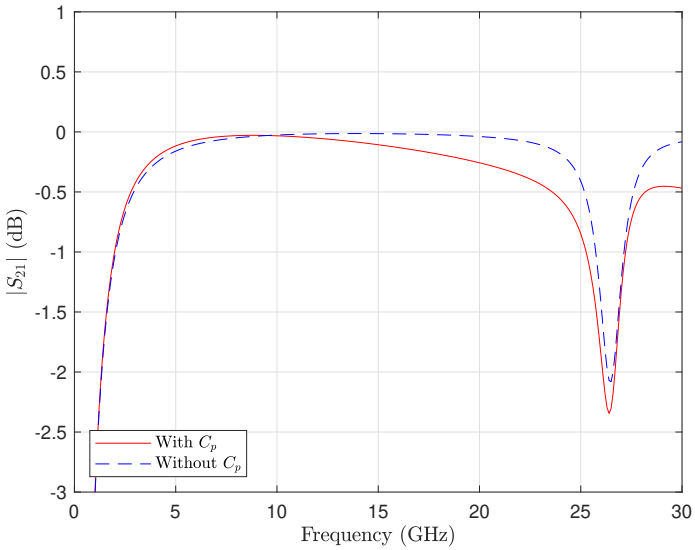

Figure 4.7: $|S_{21}|$ simulation results with (solid) and without (dashed) C_p for a L_c=4.8 nH inductor with a conductor width of 18 μm.

When $I_c > 0.35$ A, we must set $w_c > 23$ μm. In this case, the performance of the inductor degrades severely due to design rule limitations: There are current limits for a maximum-width air bridge and the thinner metal underneath it. Hence several air bridges and undermetals need to be connected in parallel, and consequently, C_p increases dramatically. For $w_c = 60$ μm, a current of 1.78 A is achievable with four parallel air bridges and seven parallel undermetals, of which layout is given in Fig. 4.8, resulting in a footprint of 0.544 mm^2 and C_p=270 fF (see Fig. 4.4). C_p value is much higher than predicted from Eq. 4.4.

As seen from Fig. 4.8, there are seven undermetals on the left-hand side of the air bridge structure of the inductor. The current limit for the undermetal is 6.15 mA/μm which means that the total conductor width of the undermetal needs to be at least 289 μm to be able to handle a current of 1.78 A. An air bridge with that length cannot be fabricated. According to the fabrication rules of the foundry, the maximum air bridge length is 60 μm, and consequently, the maximum width of the corresponding undermetal is 47 μm. While using six undermetals does not satisfy the current specification, seven undermetals achieve more than needed. Therefore, the width of each undermetal is reduced from

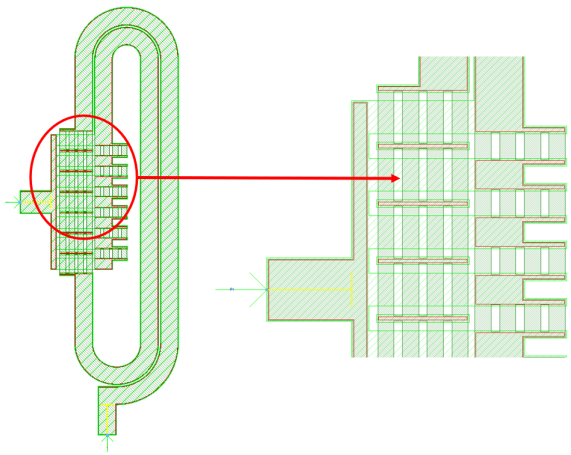

Figure 4.8: Layout of 2.7nH inductor with a conductor width of 60 μm

47 μm to a value so that it can handle a current of 1.78 A without causing additional parasitic capacitances. Using parallel undermetals is the only option to achieve that much current, but it also causes one more issue that needs to be carefully considered. The width of each one of the undermetals is chosen under the assumption that the current is equally divided among the undermetals. Since the current takes the path of least resistance, most of it tends to take the first undermetal. In other words, the amount of current going through the undermetals gradually decreases towards the last undermetal. It is neither desirable nor reliable to have this kind of current distribution.

There is another limitation that needs to be considered for an air bridge. The maximum air bridge width is 20 μm. Therefore, four parallel air bridges must be used for the given current requirement, which causes more parasitic capacitances. From these results, it can be stated that designing and implementing high-current inductor results in relatively high parasitic capacitances compared to a low-current inductor with the same inductance value.

When high inductance values are required, on-chip inductors are not practical. Due to helical structure, high inductance values have low SRFs, which limit their usable bandwidth as chokes. Conical inductors [2], one of which is shown in Fig. 4.9, which provide both high inductance values and simultaneous large resonance-free

[2]from Piconics, Inc.

bandwidth, can be used as RF choke [24]. Conical inductors have demonstrated resonance-free bandwidths from 10 MHz to 40 GHz.

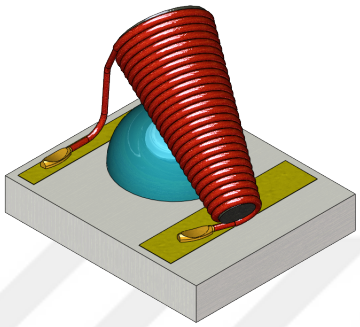

Figure 4.9: Wire bondable conical inductor mounted on an alumina substrate from Piconics, Inc.

The resonance frequency is increased by reducing the inter-turn capacitance using conical geometry. The high inductance is achieved using a high-permeability ferrite material inside the conical coil. However, their current capabilities are limited due to the thin wires used in the conical construction. Conical inductors have current capabilities up to 1 A. Therefore they are used mainly in low-power applications such as biasing a distributed amplifier operating from 10 MHz to 40 GHz while having 200 mW saturated output power.

Another drawback of using conical inductors is that it requires careful assembly. The high-frequency, high-impedance end of the inductor is the end with the smallest coil diameter. The inductor attaches pads must have very low shunt capacitance, and the inductor leads must be carefully attached to those pads in order not to introduce any parasitics which can degrade the inductor performance. In addition, the inductor must be placed sufficiently above the substrate so that no extra parasitics are created that could lower the SRF.

4.2 Distributed Choke Inductor

For high currents, we propose to use n separate low-current spiral inductors, each with a line width $w_c < 23$ μm connected to different stages of the distributed amplifier as shown in Fig. 4.10.

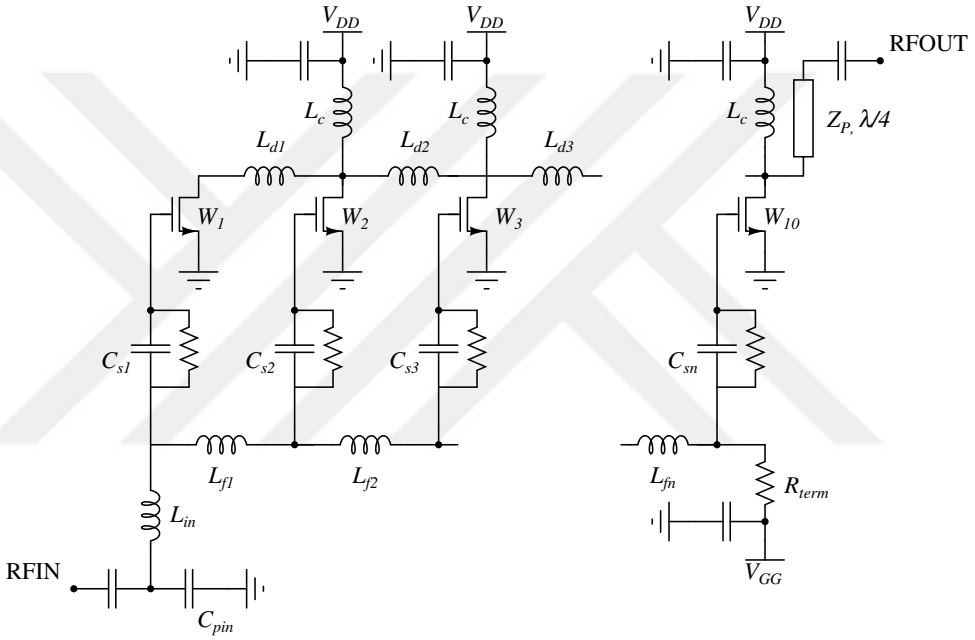

Figure 4.10: Schematic of a distributed amplifier with distributed choke inductors. The resistors in parallel with C_{si}'s provide the gate bias (V_{GG}) of the transistors. The shunt capacitors of transmission lines and parasitic capacitors of choke inductors are not shown in the schematic to reduce the complexity.

There is a need to increase the value of each inductor by a factor of k to keep the lower frequency limit the same. Fortunately, k is less than n due to the presence of drain side inductors between stages contributing to the values of the choke inductors.

With a narrower conductor, each inductor has an SRF above the band despite its larger inductance value. The increase in $R_1 + R_2$ does not pose a problem since the current passing through each inductor is smaller. Hence, the current carrying capacity is increased, and the resistive loss in the drain bias is reduced.

On the other side, the loss due to parasitic capacitors, C_p, shown in Fig. 4.7, will be exacerbated by the increased number of inductors. This loss can be eliminated altogether when the inductors are placed in a distributed manner: The parasitic shunt capacitors are absorbed as part of the drain capacitance, C_{ci}, already needed at the output side of the distributed amplifier if $C_{ci} > C_p$. Note that for small i values, C_{ci} may be smaller or even negative. Those stages can not be used to eliminate the parasitic capacitances in such a case, and a choke inductor should not be connected.

A current limit of I_c=1.78 A can be reached with n=5 inductors with w_c=18 μm each. An example of implementation is shown in Fig. 4.11.

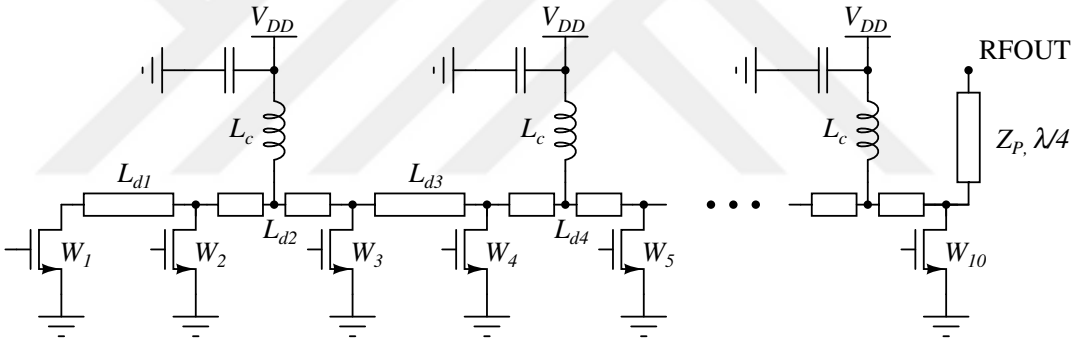

Figure 4.11: Five spiral inductors placed on the drain line of a 10-stage NDPA with $W_1 = W_2 > W_3 = W_4 = ... = W_9 > W_{10}$

.

In this case, each inductance should be increased to 4.8 nH (k ≈1.8, f_s=26.9 GHz, and C_p=53 fF). Since the inductors are placed in a distributed manner, C_ps can be used instead of the needed drain capacitors of an NDPA, eliminating the high-frequency gain degradation.

4.3 Equivalent DC Resistance of Distributed Choke Inductor

As mentioned before, the series resistance, R_1+R_2, of an inductor increases as the conductor width decreases, and using multiple inductors in parallel prevents additional DC loss. However, for the example given above, the DC loss experienced by each inductor might be slightly different due to the placement of the inductors in the amplifier. Since the transistor sizes vary, as shown in Fig. 4.11, the current drawn from each inductor might not be equal. In addition, the DC resistance of the inductors, which are going to be implemented as transmission lines, between the transistors, $L_{D1}, L_{D2}, ..., L_{D9}$, might not be equal as well. Thus, a DC analysis should be done using a CAD tool to analyze the DC loss considering all of these issues properly.

In our NDPA design, the transistor sizes are unequal, the first two transistors are larger than the subsequent transistors, and the last one is the smallest. Therefore, the quiescent transistor currents vary, which results in an unequal current division among the inductors. We performed a DC analysis using ADS at the quiescent bias point of 28 V, 528 mA.

Drain Voltages		Drain Currents	
V_{DQ1}	27.79 V	I_{DQ1}	69.40 mA
V_{DQ2}	27.81 V	I_{DQ2}	69.43 mA
V_{DQ3}	27.82 V	I_{DQ3}	51.16 mA
V_{DQ4}	27.83 V	I_{DQ4}	51.17 mA
V_{DQ5}	27.84 V	I_{DQ5}	51.18 mA
V_{DQ6}	27.85 V	I_{DQ6}	51.18 mA
V_{DQ7}	27.85 V	I_{DQ7}	51.19 mA
V_{DQ8}	27.85 V	I_{DQ8}	51.19 mA
V_{DQ9}	27.85 V	I_{DQ9}	51.19 mA
V_{DQ10}	27.85 V	I_{DQ10}	30.77 mA

Table 4.1: Drain voltage and current of each transistor under the quiescent bias point of $V_{DD} = 28$ V, $I_{DQT} = 528$ mA for our design

As it can be seen from Table 4.1, the drain voltages of the transistors vary between 27.79 to 27.85 even though the first two transistors are larger. Total DC resistive loss, P_{DCL}, is found as

$$P_{DCL} = V_{DD} I_{DQT} - \sum_{n=1}^{10} V_{DQn} I_{DQn} = 0.089\ W \tag{4.5}$$

amounting to 0.60% of the supply power.

The equivalent DC resistance of the choke inductor, R_{DCE}, is found by

$$R_{DCE} = \frac{P_{DCL}}{I_{DQT}^2} = 0.32\ \Omega \tag{4.6}$$

The equivalent resistance can be used as a figure of merit for comparison with other alternatives using the same supply voltage. Note that the equivalent resistance is dependent on the distribution of current among transistors but independent of the absolute value of the total current.

In our design, the DC resistive loss will increase about nine-fold when the full power is applied and the supply current increases to 1.55 A. Under this full-power condition, the DC resistive loss in the choke inductor is only 2% of the supply power.

In the literature, there are some works that present the use of a transformer at the end of a non-uniform distributed amplifier [18]. The most critical purpose of using a transformer is to lower the output impedance. As the output impedance reduces, the power capability increases by the same amount of factor. Furthermore, they are used as a bias injection point in most cases. Consequently, all transistor DC currents flow through drain impedance lines. Since the optimal impedance to be experienced by the first transistor is the largest, its bias current flows in its high impedance, hence narrow, line. The impedances of the drain lines of the second and third transistors are also relatively large while getting smaller at each stage. Hence, their DC currents should be carried by the subsequent drain lines in an additive manner. Since the resistive loss is proportional to the square of the current, the overall DC resistive loss in the drain lines may be significant.

We have made a comparison between our design and a design where a transformer is employed [15]. We do not have the models or the layout information to make a fair and undisputed comparison. Nevertheless, we designed a 10-transistor NDPA amplifier using our 0.25m process and the Ruthroff transformer approach with equal size transistors to make it similar to that reported in [15]. The current is supplied through the inductor of the LC branch to the last transistor.

Then, we performed a DC analysis of this NDPA structure. Under the quiescent bias of 22 V, 1249 mA, the transistor DC drain voltages vary between 21.36 V to 21.72 V as shown in the following table.

Drain Voltages		Drain Currents	
V_{DQ1}	21.36 V	I_{DQ1}	124.5 mA
V_{DQ2}	21.39 V	I_{DQ2}	124.6 mA
V_{DQ3}	21.43 V	I_{DQ3}	124.6 mA
V_{DQ4}	21.49 V	I_{DQ4}	124.8 mA
V_{DQ5}	21.55 V	I_{DQ5}	124.9 mA
V_{DQ6}	21.58 V	I_{DQ6}	125.0 mA
V_{DQ7}	21.61 V	I_{DQ7}	125.1 mA
V_{DQ8}	21.65 V	I_{DQ8}	125.1 mA
V_{DQ9}	21.68 V	I_{DQ9}	125.2 mA
V_{DQ10}	21.72 V	I_{DQ10}	125.3 mA

Table 4.2: Drain voltage and current of each transistor under the quiescent bias point of $V_{DD} = 22$ V, $I_{DQT} = 1249$ mA for the reference design

From the Table 4.2 and using Equation 4.5, the total DC resistive loss is found as 566 mW or 2.06% of the supply power as shown in the following figure. Under the full-power condition, the losses will increase further. For example, with the DC current doubled, the DC resistive loss becomes more than 2 W corresponding to about 4% of the input power. The equivalent DC resistance of this Ruthroff transformer-based network is found as 0.363 Ω.

Since the Ruthroff transformer converts to a lower impedance (12.5 Ω), the current levels should be higher for the same power. To have the same DC loss performance at the same RF power level with a lower supply voltage of 22 V, the

drain network should have had an equivalent DC resistance which is $(22/28)^2 = 0.62$ times lower, or $0.62 \cdot 0.32 = 0.20\ \Omega$. However, we found the equivalent DC resistance to be $0.363\ \Omega$.

Chapter 5

NDPA Design, Implementation and Measurement Results

We built an NDPA using the parameters in Example 1. Note that some capacitance values are negative. A harmonic balance simulation was done by setting those values to zero. We optimized the circuit parameters for maximum power and efficiency over 2−18 GHz bandwidth.

To realize the transformation from 35 Ω to 50 Ω, a quarter-wave transformer is used as depicted in Fig.4.10 and Fig.4.11. Its bandwidth is relatively small, yet it is sufficient to demonstrate the use of our method. In fact, the results can be improved further if a transformer having relatively large bandiwdth is used, which will be discussed in the next section.

A comparison of different choke inductor alternatives for an NDPA is simulated, and the results are presented in Fig. 5.1. If a single high-current L_c=2.7 nH spiral inductor with w_c=60 μm is used, less power is delivered at the high-frequency end since its shunt capacitance is relatively large: C_p=270 fF. The performance of a commercial off-chip conical 425 nH 18 GHz inductor [1] is also

[1] CC21T36K240G5 from Piconics, Inc.

shown. Since the current handling limit for this inductor is 1 A, two such inductors had to be used in parallel. As a result of the capacitance of the bonding pads, the performance at the high-frequency end degraded. In addition, using conical inductors is not usually desirable because handling and proper mounting can be problematic, as well as occupying the additional area for mounting. As shown in the figure, the performance of the distributed inductor composed of five kL_c=4.8 nH low-current inductors with C_ps absorbed as part of the drain line is superior.

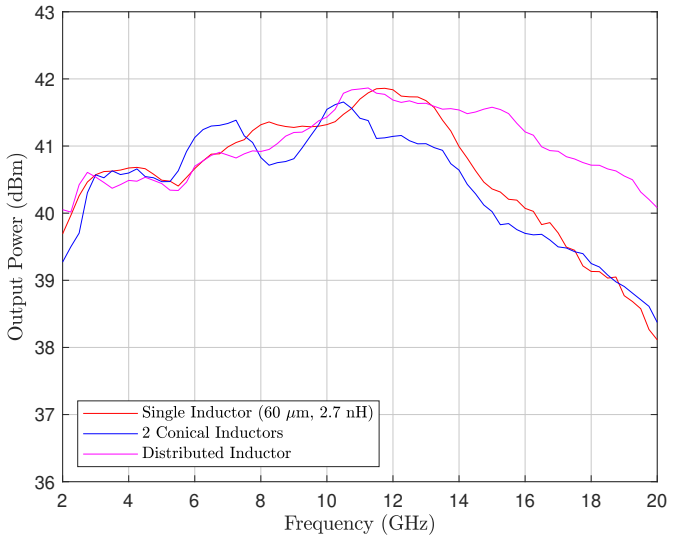

Figure 5.1: Harmonic balance simulation results of the NDPA using different choke inductors.

Optimized NDPA was fabricated using 0.25μm GaN on SiC process of Win Semiconductors Corp. as shown in Fig. 5.2. Using five 4.8 nH inductors was sufficient in terms of bandwidth and current handling. With more than five inductors, no improvement in performance is observed since the limiting factor becomes the process technology. These inductors are connected to later stages of the NDPA, where the needed additional capacitance values are positive.

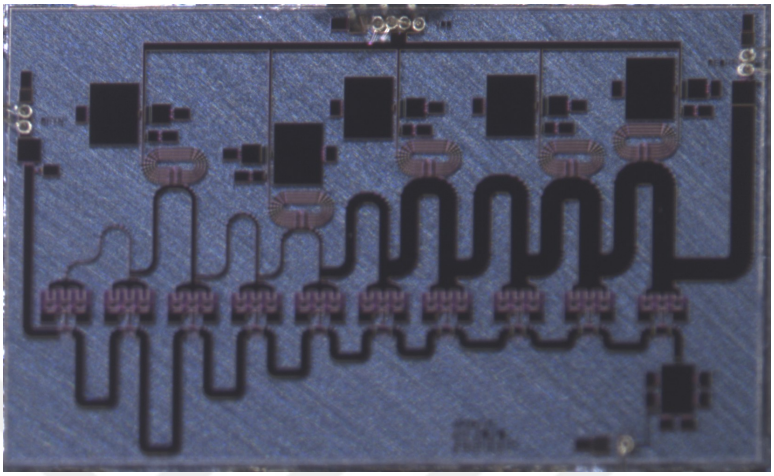

Figure 5.2: Photo of the fabricated MMIC.

5.1 Small Signal Measurements

Firstly, scattering measurements of the fabricated device are carried out. The measurement setup is shown in Fig. 5.3, where Keysight N5242 Network analyzer and Keysight 3634 and 3631 power supplies are used. Measurement was done on-wafer with a CW input. The amplifier was biased at a drain voltage of 28 V and a quiescent bias current of 530 mA.

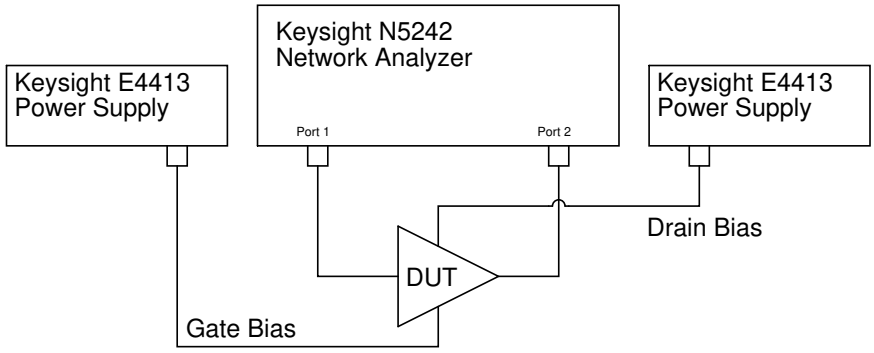

Figure 5.3: Small-signal measurement setup

Measurement was performed in the frequency range of 2–20 GHz. The measured and simulated S-parameters of the amplifier are shown in Fig. 5.4. The amplifier achieves approximately 10 dB of small signal gain over the 2–20 GHz frequency range. The input return loss is greater than 10 dB across 2–20 GHz.

The output return loss degrades to 5 dB at 2 GHz because of the finite choke inductor. The measured S-parameters compare well with the expected results.

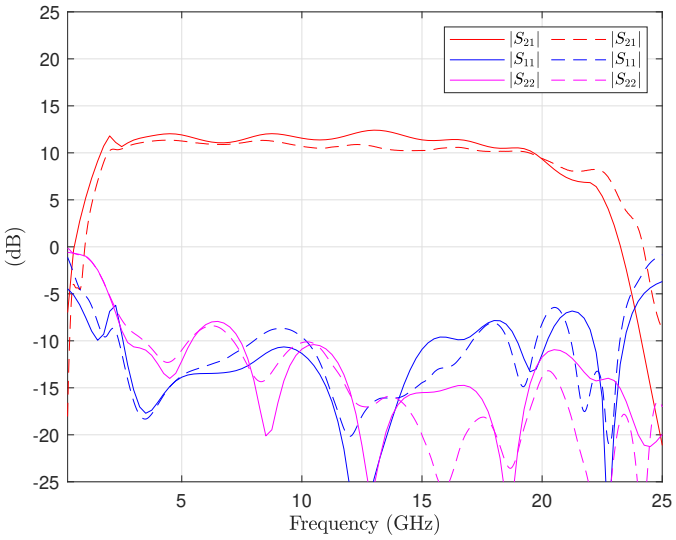

Figure 5.4: Measured (dashed) and simulated (solid) S-parameters

5.2 Large Signal Measurements

One of the main factors to consider in a high-power network analyzer measurement is the power-handling capability of the internal components of the network analyzer, mostly receivers. In addition to receivers, couplers before the receivers can be damaged under high-power levels, and it is costly to repair them. Another issue is that the high-power levels may easily exceed the compression levels of the network analyzer and also have to be considered in a high-power setup. High power levels can damage the network analyzer, and it is costly to repair the internal components of the network analyzer. In addition to damage level, compression level, and noise levels also have to be considered in a high-power setup.

Using an attenuator with the high-power capability to be added at the output of the DUT is a common method in high-power measurement setups. Or one may

use a coupler and terminate the thru port in a high power load. The coupled arm can be fed into the port of the network analyzer.

It is essential to present 50 Ω as precisely as possible to the output of DUT. Since a power amplifier is designed at a 50 Ω system impedance, any shift from the reference impedance causes a destructive or constructive effect on both output power and efficiency. If the device output is well-matched, then the result is probably destructive. Therefore, it is crucial to present 50 Ω to the output of the DUT to see the device's performance. High-power attenuators or couplers usually have 10 dB of input return loss as their lowest performance. To present 50 Ω, we may use a manual impedance tuner to be added at the output of the DUT before the attenuator or the coupler and tune the points having the lowest return loss values. This would be a relatively easy task if we were to measure a narrowband amplifier.

For a wideband amplifier, it is very hard to achieve across the frequency range of 2–20 GHz, for example. Assuming the frequency step is 0.5 GHz, 37 points are needed to be tuned. Even for the narrowband amplifiers, controlling the tuner for each frequency point to be measured is extremely hard. One may need to control the probes precisely, and tuners must be nearly independent electrical results of the mechanical motions. Stepping from one frequency point to the other may take a long time, which will enormously extend the overall measurement time.

Due to the above reasons, it would be a good solution if a load-pull setup is used as a high-power measurement setup. Fig. 5.5 shows the load-pull setup configured as a high-power measurement setup.

The impedance and frequency sweep setup of the load-pull system is configured so that only one impedance point, 50 Ω, is tuned and presented at the output of the DUT at a given frequency. A power sweep is done up to any desired output compression level at that frequency. Then, the system is stepped into the next frequency point. After covering the frequency range of 2–20 GHz, we get raw power sweep data from the small-signal level to the desired output compression level, i.e., 5 dB. After some operations to get useful data, measured output power

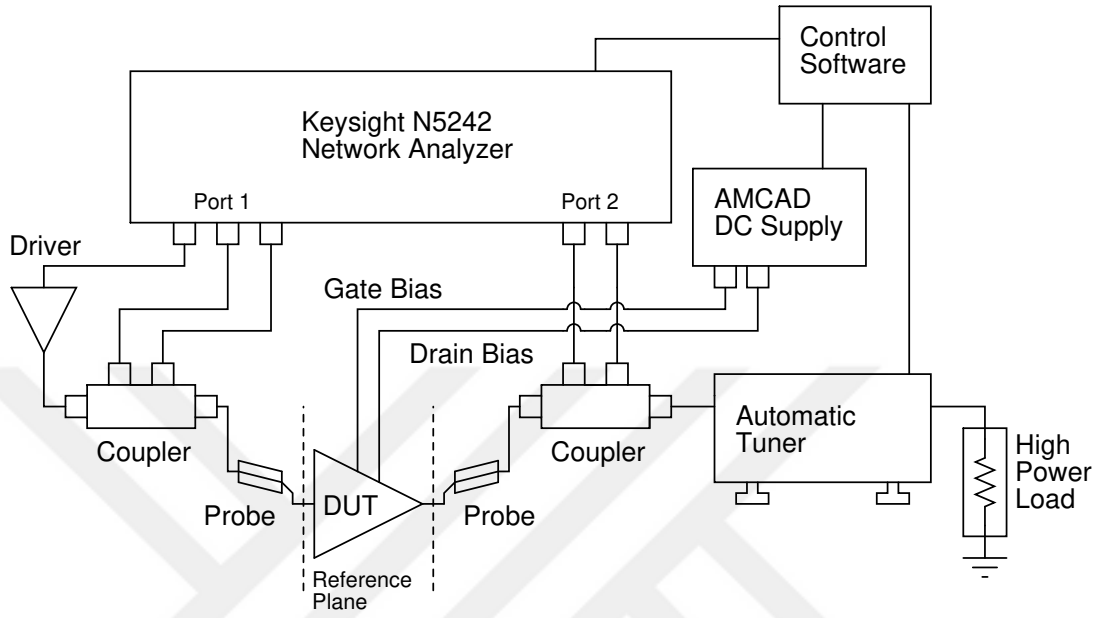

Figure 5.5: On-wafer CW measured power and efficiency of NDPA with V_{DD}=28 V and V_{GG}=−2.14 V.

and power-added efficiency are shown in Fig. 5.6 along with the simulation results. The measured output power varies between 38–41.5 dBm, and the measured power-added efficiency is greater than 15% and peaking up to 35% over the 2–20 GHz frequency range. A comparison of our NDPA design with those given in the literature is presented in Table 5.1.

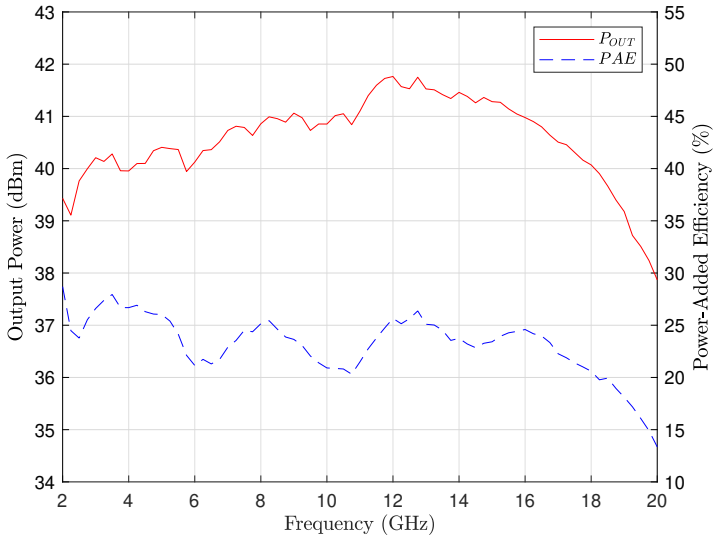

Figure 5.6: On-wafer CW measured power and power-added efficiency of NDPA with V_{DD}=28 V and V_{GG}=−2.14 V.

References	[9]	[12]	[15]	[25]	[16]	T.W.
Process (μm)	0.25	0.10	0.15	0.20	0.15	0.25
f (GHz)	2–18	2–18	2–20	0–20	2–20	2–18
S_{21} (dB)	10	28	19	12	17	10
P_{out} (W)	5.6–12.5	9.1–15.8	10.7–15.8	4	18–30.8	8–15
PAE (%)	15–35	18–38	22–38	10–15	18–29.7	20–28
V_{DD} (V)	30	28	22	30	22	28
Size (mm^2)	15.3	7	10.5	4.8	25.8	13.4

Table 5.1: Summary of this work (T.W.) and five DPA studies from the literature with GaN on SiC

Chapter 6

Conclusion

In this thesis, we present an analytical design procedure for a non-uniform distributed power amplifier and a method to design a wideband, low-loss, and high-current distributed choke inductor suitable for use in a distributed power amplifier.

We first presented the theory of operation of a conventional distributed amplifier. Such an amplifier is not considered to be a high-power amplifier since a significant portion of the power is wasted on the drain termination resistor. To overcome this issue, the drain termination resistor is removed and the impedances of the drain line are tapered so that each transistor sees its optimum load for maximum power. We presented an analytical design procedure using a few parameters of the fabrication process. The procedure starts by determining the coefficients of a C-L-C network. With those coefficients and using the presented procedure, we obtained all required circuit parameters, including the gate width for every single transistor. Using non-linear models provided by the foundry and the circuit parameters resulting from our method, We performed harmonic balance simulations of the NDPA, and we showed that the results are very promising without any tuning or optimization. We gave a number of example designs to demonstrate the use of our method that finds all element values.

In all examples, the drain capacitors of the first few transistors could not be absorbed by the output impedance network, resulting in a non-ideal behavior and reduced gain and power at high frequencies. Initial trials showed that it is possible to reduce the values of this capacitors by an optimized selection of input impedances (Z_{ei}'s). Finding an optimized selection method of input impedances is left as a future work.

The choke inductor of an NDPA can be a limiting factor in the performance of an NDPA. With a simplified model, we analyzed several different kinds of choke inductors to observe how the amplifier bandwidth is actually affected by this inductor. We determined the parameters which affect the loss and the series-resonance frequency and derived equations for those parameters. We introduced the distributed choke inductor to be able to provide a high performance choke inductor for the distributed amplifier without compromising bandwidth or loss.

We used the DC equivalent resistance of the choke inductor to determine the efficiency at DC. We showed that our distributed choke inductor method provides a smaller DC equivalent resistance compared to the alternative Ruthroff transformer approach given in the literature [15]. Our method gives a reduction in DC loss compared to the Ruthroff approach. We note that Ruthroff transformer approach reduces the drain impedance over a large bandwidth, making a high-power amplifier possible. It provides a transformation in one decade of bandwidth, but one decade is also the limit. Our approach can be used with wider bandwidth processes in the future.

Our distributed choke inductor method can be used along with the Ruthroff transformer method to increase the efficiency further. The Ruthroff transformer can be used to lower the impedance of the drain line while the additional distributed choke inductors connected to transistor drains can be used to supply the DC current to reduce the overall resistive loss without increasing the overall chip area. We note that an additional decoupling capacitor for each spiral inductor is not needed since there is already a large decoupling capacitor to which the choke inductors can be connected directly. Since the drain impedance is lower, higher current spiral inductors with smaller values can be used in the drain network to

lower the overall equivalent DC resistance. The parasitic capacitors of the spiral inductors can be easily absorbed by the lower impedance drain LC network. Our method is especially advantageous when the first few transistors of the NDPA chain are larger (as in our NDPA design) and hence draw more current. In such a case, the DC resistive losses in the conventional method with a single choke inductor would be increased, and the equivalent DC resistance would be higher.

If the transistor has a vendor-supplied model, the proposed distributed choke inductor and calculated values from our analytical method can be used as a good starting point for optimization of an NDPA in a harmonic balance simulator. We provided measurement results of an optimized NDPA implementation using distributed choke inductor providing good performance in a wide band.

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Appendix A

Matlab Code

```
% MATLAB code to design a Nonuniform distributed amplifier analytically
% from process parameters and from desired frequency band
% Jan 3, 2023
% input side implemention limitations included by using ZF
clear

N=10; % number of amplifier stages, should be even

% process parameters
Rp=120000; % ohm-um for the load impedance of transistors for a certain current per micron
CgN=1.87e-15; % gate cap per micron
CdN=0.3e-15; % drain cap per micron
CgdN=0.076e-15; % drain-gate cap per micron
gmN=0.288e-3; % gm per micron
RdsN=378000; % ohm-um for the drain-source resistance of the transistor

% amplifier specs
f1=1e9; % lower frequency of the NDPA
f2=20e9; % upper frequency of the NDPA
RF=50; % input side impedance of the LPF (to be transformed by an input transformer from 50 ohm
```

```
Rout=35; % output load impedance (to be transformed later by a
    transformer to 50 ohms
ZS=50; % actual source impedance, can be a complex number
ZL=Rout; % actual load impedance, can be a complex number
Rterm=45; % termination resistance at the input side, can be
    optimized to reduce output ripple or input return loss
VDD=28; % drain bias voltage

% implementation specs
% if needed different values for each stage can be specified here,
    to
% reduce loss in inductors
Zmax=140; % the maximum TL impedance that can be used at the input
    and drain side for inductor realization
Cin=70e-12; % series DC-block cap at the input, has an effect on
    the low frequency cutoff
Lin=0.30e-9; % series input inductance
Cpin=0.14e-12; % shunt tuning capacitor at the input before Lin
Q=5000; % Q of inductors at the specified frequency in the
    implementation
fQ=20e9; % specified frequency of Q
Lchoke=54.7e-9; % choke inductor at the last transistor, with small
     values P1dB suffers at low frequencies
Rchoke=0.4; % series resistance of the choke inductor

Ze=50*ones(1,N-1); % set the input line impedances
Ze(1)=35;
f0=22e9*ones(1,N-1); % set the upper cutoff frequency of the LC
    ladder circuits

% analysis parameters
fstep=1e8; % frequency step size in analysis
f10=1e9; % analysis start frequency
f20=20e9; % analysis end frequency

% no parameters below
Av=-gmN*(Rp*RdsN)/(Rp+RdsN); % this is the voltage gain of each
    transistor from gate to drain.
n1=(f1-f10)/fstep+1;
n2=(f2-f10)/fstep+1;
```

```
RovL=2*pi*fQ/Q; % R/L ratio for all inductors
n=N-1; % number of amplifier stages -1

Le=1.22*Ze./(2*pi*f0); % calculate input inductors and capacitors
Ce=1./(Le.*(2*pi.*f0).^2); % in CF2-LF-CF2 network
Ce(N)=Ce(N-1);

% combine neighbor capacitors to obtain CF capacitors
Cf(1)=Ce(1);
Cf(2:N/2)=Ce(1:N/2-1)+Ce(2:N/2);
Cf(N)=Ce(N);
Cf(N-1:-1:N/2+1)=Ce(N:-1:N/2+2)+Ce(N-1:-1:N/2+1);

RLF=Le*RovL; % series resisntance of inductors
RLin=Lin*RovL; % series resistance of input tuning inductance

% all shunt capacitors are assigned to a transistor gate

% for realization use Zmax as TLs
% find cutoff frequency
wr1=1.22*Zmax./Le; %this is the cutoff frequency of inductor
    realization
CA=1./(wr1.^2.*Le); % capacitors of the equivalent circuit that
    would be consumed by TL realization
LofLambdaIn=0.2*2*pi*f2./wr1; % length of input TLs in terms of
    lambda at the highest frequency of operation, f2

% stage input capacitors
CS=zeros(1,n+1);
CS(1)=Cf(1)-CA(1); % first stage has only one cap
for i=2:n
    CS(i)=Cf(i)-CA(i-1)-CA(i);
end
CS(n+1)=Cf(n+1)-CA(n); % the last stage has only one cap
% CS are the available capacitors that can be used by transistors
CST=sum(CS);

WT=Rp/Rout; % total transistor width in um

CgT=WT*CgN; % total transistor gate cap
```

```
89
90  Cg=CgT/CST*CS; %gate capacitors are proportional to available input
        node capacitors
91
92  W=Cg/CgT*WT; % transistor widths are found from gate capacitors
93  % if there is a nonlinear relation between gate cap and width, it
        should be
94  % used here
95
96  % since width of each transistor is found we can find individual
        transistor
97  % parameters
98  % drain cap of each stage
99  Cd=W*CdN; %
100 gm=W*gmN; % gm of each transistor proportional to the assigned
        width
101 Rds=RdsN./W; % drain-source resistance of each transistor
102 Cgd=W*CgdN; % drain-gate capacitors of each transistor
103 %CgdT=sum(Cgd); % total drain-gate caps
104
105 CG=Cg+(1-Av)*Cgd; % total gate cap including Miller cap at all
        gates
106 Cs=(CS.*CG)./(CG-CS); % series gate caps needed to reduce the
        capacitor value at each input node
107 % it is chosen such that each stage has the same voltage gain.
108 Csh=zeros(1,N); % the remaing caps at the input nodes
109 % normally nothing should be left to maximize the gain
110
111 % find the load resistances that each stage needs to see at the
        drain side
112 Z=zeros(1,n+1);
113 Ws=0;
114 for i=1:n+1
115     Ws=Ws+W(i);
116     Z(i)=Rp/Ws;
117 end
118 % no need for the following step, since Rp is given knowing the
        presence of
119 % Rds
```

```
%Z=Z.*Rds./(Rds-Z); % since Rds is in parallel, remove that
    resistance to find the required output resistance

% realization of drain impedance lines by transmission lines
    modeled by CB1-LD1-CB1 network
% LD1 are drain inductors
% there is a maximum realizable TL impedance, the values must be
    limited by
% this value
% drain inductors and capacitors are proportional to input
    inductors with
% the Z/Zin1 ratio for phase and amplitude matching
Ld=Z(1:N-1).*Le./Ze;
Cb=Ce(1:N-1).*Ze./Z(1:N-1);

wr2=1.22*Zmax./Ld; %this is the cutoff frequency of inductor
    realization
CC=1./(wr2.^2.*Ld); % capacitors of the equivalent circuit that
    would be consumed by TL realization
LofLambdaOut=0.2*2*pi*f2./wr2; % length of input TLs in terms of
    lambda at the highest frequency of operation, f2
CC(N)=CC(N-1);
Cb=Cb-CC(1:N-1);

% combine neighboring capitors to find CB1 capacitors
Cc(1)=Cb(1);
Cc(2:N-1)=Cb(1:N-2)+Cb(2:N-1);
Cc(N)=Cb(N-1);

Cnegative=(1-sign(Cc-Cgd-Cd))/2.*(Cc-Cgd-Cd)
% eliminates negative capacitance if there is
Ca=-(1-sign(Cc-Cgd-Cd))/2.*(Cc-Cgd-Cd)+Cc-Cgd-Cd;

RLD=Ld*RovL; % series resistance of each inductor

%the following code makes AC analysis of the NDPA and plots it
ij=0; % frequency index
Ain=zeros(3*n+4,3*n+4); % nodal analysis matrix
A=zeros(3*n+4,1); % excitation vector
```

```
% one more node is added at the input side to make input tuning
    possible

nm=(f20-f10)/fstep+1; % number of steps in analysis
% reserve space for variables
S11=zeros(1,nm); % input S11
f1=S11; % frequencies
Vd=zeros(nm,N); % complex drain voltages
PhaseDiff=Vd;
Vn=Vd; % complex input filter nodes
Vg=Vd; % complex gate voltages
Zdrain=Vd; % the impedances seen by transistors at different
    frequencies

% the parameters calculated above are used
% the circuit parameters used: ZS, Cin, Lin, Cpin, LF, RLF, Csh, Cs
    , Cgd, gm, LD1,
% RLD, CB1, Rds, Cgd, Lchoke, Rchoke, ZL

% for implementation look at Z for drain side TL impedances
% their length should be


for f=f10:fstep:f20 % frequency range of the analysis
w=2*pi*f;
ij=ij+1;
% form the Ain matrix and A vector to solve node equations at the
    gates
A(3*n+4,1)=2/ZS; % 2 is the excitation phasor at the input, with
    this selection output voltage gives the gain.
Ain(1,1)=1/(1/(1i*w*Cin)+1i*w*Lin+RLin)+1/(1i*w*Le(1)+RLF(1))+1i*w
    *(Csh(1)+Cs(1));
Ain(1,2)=-1/(1i*w*Le(1)+RLF(1));
Ain(1,n+2)=-1i*w*Cs(1);
Ain(1,3*n+4)=-1/(1/(1i*w*Cin)+1i*w*Lin+RLin);
for m1=2:n
    Ain(m1,m1-1)=-1/(1i*w*Le(m1-1)+RLF(m1-1));
    Ain(m1,m1)=1/(1i*w*Le(m1-1)+RLF(m1-1))+1/(1i*w*Le(m1)+RLF(m1))
        +1i*w*(Csh(m1)+Cs(m1));
    Ain(m1,m1+1)=-1/(1i*w*Le(m1)+RLF(m1));
```

```
185      Ain(m1,m1+n+1)=-1i*w*Cs(m1);
186  end
187  Ain(n+1,n)=-1/(1i*w*Le(n)+RLF(n));
188  Ain(n+1,n+1)=1/(1i*w*Le(n)+RLF(n))+1/Rterm+1i*w*(Csh(n+1)+Cs(n+1));
189  Ain(n+1,2*n+2)=-1i*w*Cs(n+1);
190  Ain(3*n+4,3*n+4)=1i*w*Cpin+1/(1i*w*Lin+RLin+1/(1i*w*Cin))+1/ZS; %
        this is the tuning node at the input of NDPA
191  Ain(3*n+4,1)=-1/(1/(1i*w*Cin)+1i*w*Lin+RLin);
192
193
194  for m1=n+2:2*n+2
195      m2=m1-(n+1);
196      Ain(m1,m1)=1i*w*(Cg(m2)+Cgd(m2)+Cs(m2));
197      Ain(m1,m1-(n+1))=-1i*w*Cs(m2);
198      Ain(m1,m1+(n+1))=-1i*w*Cgd(m2);
199  end
200
201  Ain(2*n+3,2*n+3)=1i*w*(Cd(1)+Ca(1)+Cgd(1))+1/(1i*w*Ld(1)+RLD(1))+1/
        Rds(1);
202  Ain(2*n+3,2*n+4)=-1/(1i*w*Ld(1)+RLD(1));
203  Ain(2*n+3,2*n+3-(n+1))=gm(1)-1i*w*Cgd(1);
204  for m1=2*n+4:3*n+2
205      m2=m1-2*n-2;
206      Ain(m1,m1-1)=-1/(1i*w*Ld(m2-1)+RLD(m2-1));
207      Ain(m1,m1)=1i*w*(Cd(m2)+Ca(m2)+Cgd(m2))+1/(1i*w*Ld(m2-1)+RLD(m2
            -1))+1/(1i*w*Ld(m2)+RLD(m2))+1/Rds(m2);
208      Ain(m1,m1+1)=-1/(1i*w*Ld(m2)+RLD(m2));
209      Ain(m1,m1-(n+1))=gm(m2)-1i*w*Cgd(m2);
210  end
211  Ain(3*n+3,3*n+2)=-1/(1i*w*Ld(n)+RLD(n));
212  Ain(3*n+3,3*n+3)=1/ZL+1/(1i*w*Ld(n)+RLD(n))+1i*w*(Cd(n+1)+Ca(n+1)+
        Cgd(n+1))+1/Rds(n+1)+1/(1i*w*Lchoke+Rchoke);
213  Ain(3*n+3,3*n+3-(n+1))=gm(n+1)-1i*w*Cgd(n+1);
214
215
216  % invert the matrix to find all node voltages in V vector
217  % the first N elements of V are the input nodes on the input filter
218  % the next N elements are the gate voltages of transistors
219  % the next N elements are the drain voltages of transistors
220  % the very last element is the input tuning node
```

```
V=Ain\A;
%Vout(ij)=V(n+1);
f1(ij)=f;
% evaluate the S11 parameter at the input of the NDPA with respect
    to RF
% first find the voltage at the input node of the NDPA
Iin=(2-V(3*n+4))/ZS;
Vin=V(3*n+4);
S11(ij)=(Vin/sqrt(RF)-Iin*sqrt(RF))/(Vin/sqrt(RF)+Iin*sqrt(RF)); %
    store S11 values
Vn(ij,:)=V(1:n+1); % store the input node voltages for later use
Vg(ij,:)=conj(V(n+2:2*n+2))'; % store the gate voltages for later
    use
Vd(ij,:)=conj(V(2*n+3:3*n+3))'; % store the drain voltage results
    for later use
Idrain=-(gm.*Vg(ij,:)+(Vd(ij,:)-Vg(ij,:)).*(1i*w*Cgd)+Vd(ij,:).*(1i
    *w*Cd+1./Rds));
Zdrain(ij,:)=Vd(ij,:)./Idrain; % store the drain impedance seen by
    each transistor for later use
Zdrain(ij,1)
end
Nf=ij; % number of frequency points

mse=0;
for m1=1:N
InPhase=unwrap(angle(Vg(:,m1)));
OutPhase=-unwrap(angle(-Vd(:,m1)));
mse=mse+sum((OutPhase-InPhase).^2);
end

% mean square error of phase differences in each transistor
mse;


figure(1)
hold off
% calculate small-signal transducer power gain GT in dB according
    to the actual load
% impedance ZL
% use the last element of Vd (output voltage) to find GT=Pout/Pavs
```

```
GTdB=10*log10(real(conj(Vd(:,N)).*Vd(:,N)/ZL)/(1/real(ZS)));
GTindB=10*log10(real(conj(Vg(:,N)).*Vg(:,N)/Rterm)/(1/real(ZS)));
plot(f1/1e9,GTdB)
hold on
plot(f1/1e9,GTindB)
grid on
ylabel('G_T (dB)')
xlabel('Freq (GHz)')
axis([0,f20/1e9,-10,25]);
GainMax=max(GTdB(n1:n2));
GainMin=min(GTdB(n1:n2));

title('G_T')

dBripple=GainMax-GainMin;


% plot the input reflection coefficient in dB
figure(2)
hold off
plot(f1/1e9,20*log10(abs(S11)))
grid on
ylabel('|S_{11}| (dB)')
xlabel('Freq (GHz)')
axis([0,f20/1e9,-30,0]);
title('Amplifier input |S_{11}|')


% plots the drain impedance seen by each transistor on Smith chart
figure(3)
hold off
Zdr=Rp./W;
for m1=1:N
gamma=z2gamma(Zdrain(:,m1),Zdr(m1));
smithchart(gamma);
hold on
smithchart(S11);
end
```

```
%legend
    (['1'],['2'],['3'],['4'],['5'],['6'],['7'],['8'],['9'],['10'],'
    Location','Southeast')
title('')
title(strcat('Z_0=',num2str(round(Zdr(2))),'\Omega', '          Z_0
    =',num2str(RF),'\Omega'))

% plots the drain voltages of all transistors at frequency
    determined by index
% nf
nf=floor(Nf*1);
figure(4)
hold off
t=0:2/f1(nf)/100:2/f1(nf);
for m1=1:N
    plot(t*1e9,abs(Vd(nf,m1))*cos(2*pi*f1(nf)*t+angle(Vd(nf,m1))))
    hold on
end

grid on
%legend(['Tr 1'],['Tr 2'],['Tr 3'],['Tr 4'],['Tr 5'],['Tr 6'],['Tr
    7'],['Tr 8'],['Tr 9'],['Tr 10'])
title(strcat('f=',num2str(f1(nf)/1e9),' GHz'))
xlabel('t (ns)')

figure(5)
hold off
P1dB=zeros(Nf,N);
Z(N)=Rout;
for m1=1:N
    % estimate P1dB at each frequency by finding the input value
        that
    % causes one of the transistors drain voltage to hit the VDD
        limit
    % the signal level at the input can be increased up to this
        limit
    % without causing any of the transistors to saturate
    % then use GT and Pav at input to determine the power delivered
        to load
    % at that level. Then add 30 to convert to dBm
```

```
    P1dB(:,m1)=10*log10(min((VDD/Rp*W(m1).*abs(Zdrain(:,m1))).^2.*
        real(1./Zdrain(:,m1)),VDD^2./real(Zdrain(:,m1))))+30;
end
plot(f1/1e9,P1dB);
hold on
grid on
ylabel('P1dB (dBm)')
xlabel('Freq (GHz)')
axis([0,f20/1e9,10,38]);


figure(6)
hold off
for m1=1:N
    plot(f1/1e9,abs(Vd(:,m1)))
    hold on
    %plot(f1/1e9,40*abs(Vg(:,m1)))
%     plot(f1/1e9,abs(Vn(:,m1)))
end
ylabel('Drain voltage amplitude')
xlabel('Freq (GHz)')
grid on
%legend(['Tr 1'],['Tr 2'],['Tr 3'],['Tr 4'],['Tr 5'],['Tr 6'],['Tr
    7'],['Tr 8'],['Tr 9'],['Tr 10'],'Location','Northwest')
axis([0,f20/1e9,0,5]);

figure(7)
hold off
for m1=1:N
    PhaseDiff(:,m1)=unwrap(angle(Vn(:,m1)))-(-unwrap(angle(-Vd(:,m1
        ))));
    plot(f1/1e9,PhaseDiff(:,m1))
    hold on
end
ylabel('Input node and Drain voltage phase differenc3e')
xlabel('Freq (GHz)')
grid on
legend(['Tr 1'],['Tr 2'],['Tr 3'],['Tr 4'],['Tr 5'],['Tr 6'],['Tr 7
    '],['Tr 8'],['Tr 9'],['Tr 10'],'Location','Southwest')
axis([0,f20/1e9,-pi/2,pi/2]);
```

```
359
360 PhaseAverage=mean(PhaseDiff,2);
361 msePhase=0;
362 for m1=1:N
363     msePhase=msePhase+sum(abs(PhaseDiff(:,m1)-PhaseAverage).^2);
364 end
365 msePhase
```