

DYNAMIC POWER SUPPLY DESIGN FOR VARYING ENVELOPE SIGNALS USING ENVELOPE TRACKING METHOD

A THESIS

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MASTER OF SCIENCE

By

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July 2012

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in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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M.S. in Electrical and Electronics Engineering

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In modern communication systems, demand for higher data-rate is consistently growing. Higher data-rate within a limited bandwidth tends to require more amplitude modulation (AM) to increase number of symbols per second. Amplitude modulated carriers should be amplified using linear power amplifiers (PAs). Although, linear PAs have good performance in terms of linearity, they are efficient only when they transmit at maximum power. However, modern communication signals have high peak-to-average-power ratio (PAPR), therefore probability of a PA transmitting at maximum power is low. As a conclusion, efficiencies are degraded to alarmingly low values and the problem translates to heat and shorter battery life issues. In this thesis, we investigate how dynamic power supplies (DPS) perform for non-constant envelope RF signals. We have designed a DPS and used it to test efficiency enhancement of two PAs compared to the same PAs operating with constant supply. Our aim was to obtain efficiency increase compared to constant supply case without introducing extra non-linearity. We have obtained satisfying results for both amplifiers.

Keywords: Amplitude Modulation (AM), Power Amplifier (PA), Peak-to-Average-Power Ratio (PAPR), Linearity, Efficiency, Dynamic Power Supply (DPS)

ÖZET

DEĞİŞKEN ZARF SİNYALLERİ İÇİN ZARF TAKİP METODUNU KULLANAN DİNAMİK GÜÇ KAYNAĞI TASARIMI

Muhlis Kenan Özel

Elektrik ve Elektronik Mühendisliği Bölümü Yüksek Lisans

Tez Yöneticisi: Prof. Dr. Abdullah Atalar

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Çağdaş iletişim sistemlerinde, daha yüksek veri hızlarına olan talep sürekli olarak artmaktadır. Daha yüksek veri hızları, kısıtlı bant genişliğinde, saniyedeki sembol sayısını arttırmak için daha fazla genlik kiplemesine ihtiyaç duyarlar. Genlik kiplemesine sahip taşıyıcıları, doğrusal güç yükselteçleri kullanılarak yükseltmek gerekir. Bu güç yükselteçler doğrusallık açısından iyi başarımları gösterse de, yalnızca en yüksek güçte gönderim yaptıklarında verimlidirler. Fakat, çağdaş iletişim sinyalleri yüksek tepeden ortalamaya güç oranına sahiptirler ve bir güç yükseltecin en yüksek güçte gönderme ihtimali çok düşüktür. Sonuç olarak, verimlilikler son derece düşük seviyelere düşmüştür ve bu problem ısı ve daha düşük batarya süresi sorunlarına neden olmaktadır. Biz bu tezde dinamik güç kaynaklarının sabit olmayan genliğe sahip sinyallerde nasıl başarımları gösterdiklerini inceledik. Dinamik bir güç kaynağı tasarladık ve bu güç kaynağıyla çalışan iki güç yükselteci, sabit gerilimle çalışan yine aynı iki güç yükselteciyle verimlilik artışı gözlemlemek amacıyla karşılaştırdık. Amacımız ilave doğrusalsızlığa sebep olmadan verimliliği arttırmaktı. Her iki güç yükselteç için de tatmin edici sonuçlar aldık.

Anahtar Kelimeler: Genlik modülasyonu, Güç Yükselteç, Tepeden Ortalamaya Güç Oranı, Doğrusallık, Verimlilik, Dinamik Güç Kaynağı

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Dedicated to My Parents

Chapter 1

INTRODUCTION

This chapter discusses some important concepts that will be used frequently in the thesis. In addition, the importance of supply modulation and research goals are presented.

1.1 Overview

Wireless communication systems use different standards such as GSM (Global System for Mobile Communications), WCDMA (Wideband Code Division Multiple Access) or LTE (Long Term Evolution). Fig. 1.1 illustrates the evolution path of the wireless communication systems. One common feature of new standards is the capability of supporting higher data-rates and mobility demands of users.

A higher data-rate within a limited bandwidth tends to require more amplitude modulation to increase number of symbols per second [5]. Amplitude modulation with high data rates results in high PAPR (peak-to-average power ratio) and wider bandwidth modulation schemes. Here, PAPR is a measure of peak to average power fed to antenna by a power amplifier (PA). The problem

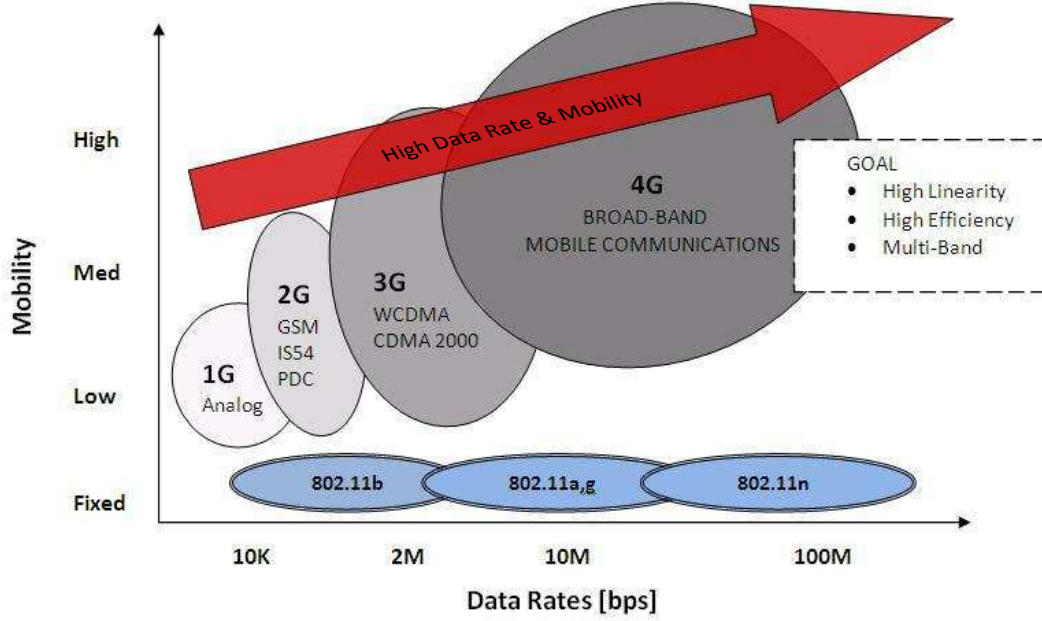


Figure 1.1: Evolution of Wireless Communication Systems [1].

with high PAPR signals is the efficiency of the system. That is because, high PAPR means that the traditional transmitter topologies will be pushed further to operate with lower average efficiencies [6]. This problem should not be underestimated because the energy consumption of telecommunication industry is in increasing trend. Some estimations showed that 1 % of the planet's global power consumption was made by telecommunication industry [7].

1.2 IQ Modulation

Wireless transmitters enable communication over wireless channels. In order to transmit a signal over that channel, the carrier signal must be modulated and then converted to an electromagnetic wave by an antenna.

Conventional modulation strategies use orthogonal vectors to describe a two-dimensional space. These basis vectors are typically referred to as in-phase, I

and quadrature, Q. RF signal trajectory is mapped using $I(t)$ and $Q(t)$ baseband signals and upconverted using quadrature local oscillators:

$$v(t) = I(t) \cos(\omega_c t) + Q(t) \sin(\omega_c t), \quad (1.1)$$

where $I(t)$ is the in-phase vector data, $Q(t)$ is the quadrature vector data, and ω_c is the carrier frequency.

The same RF signal trajectory can be decomposed into Polar form using the amplitude and phase of the RF carrier. With a Polar representation, the modulated RF signal follows:

$$v(t) = A(t) \cos(\omega_c t + \theta_t), \quad (1.2)$$

where $A(t)$ and θ_t are the amplitude and phase of the carrier, respectively. Both Polar and Cartesian representations of amplitude (AM) and phase (PM) modulation suggest the phasor nature of the signal. Importantly, the complex representation of carrier signal allows many ways to encode digital information. Goal

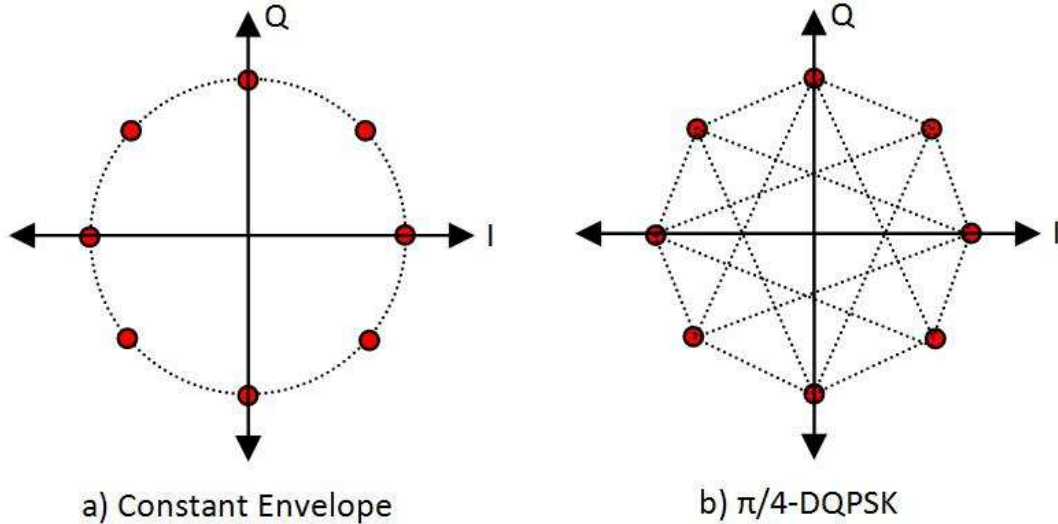


Figure 1.2: Complex and Varying Amplitude Modulation Schemes [2].

of a digital communication system is to send information represented by binary symbols, through a physical channel. I-Q diagrams are used to represent these

symbols. Symbols on these diagrams can be considered as vectors, and each of them have unique amplitude and phase, consequently representing different data sequence or sequences. Increasing bits/symbol results in higher spectral efficiency, or higher data-rate for a given amount of available spectrum.

Fig. 1.2 shows I-Q diagrams of two different modulation schemes. In Fig. 1.2-a, a constant envelope modulation is represented. Symbols are only allowed to follow the path over a circle. This results in constant envelope carrier modulation. However, according to trajectory points shown in Fig. 1.2-b, the symbols are allowed to pass close to origin, which results in a non-constant envelope modulation. The modulation scheme uses both amplitude and phase modulation. The advantage of using both types of modulation is increased data rates for the same spectral utilization. We can see this advantage intuitively by noting that the distance between symbols is shorter. However, constant envelope schemes generally use lower data rates to satisfy spectral mask requirements [8], [9].

1.3 Power Back-off and PAPR

In most modern wireless systems, transmitters are rarely used at maximum power. Fig. 1.3 shows the probability distribution function (pdf) of CDMA signal. According to graph, transmitting RF signal at the maximum power is less probable than transmitting it at 20-25 dB smaller than the maximum power. Therefore, designing PAs more efficient at maximum power does not actually mean that the system efficiency will be high. The efficiency of PA at the most probable power region is more important. The region, where output power is smaller than maximum power is known as the back-off region. The system efficiency will be higher if PA's efficiency is higher at the back-off. A back-off may occur due to two reasons.

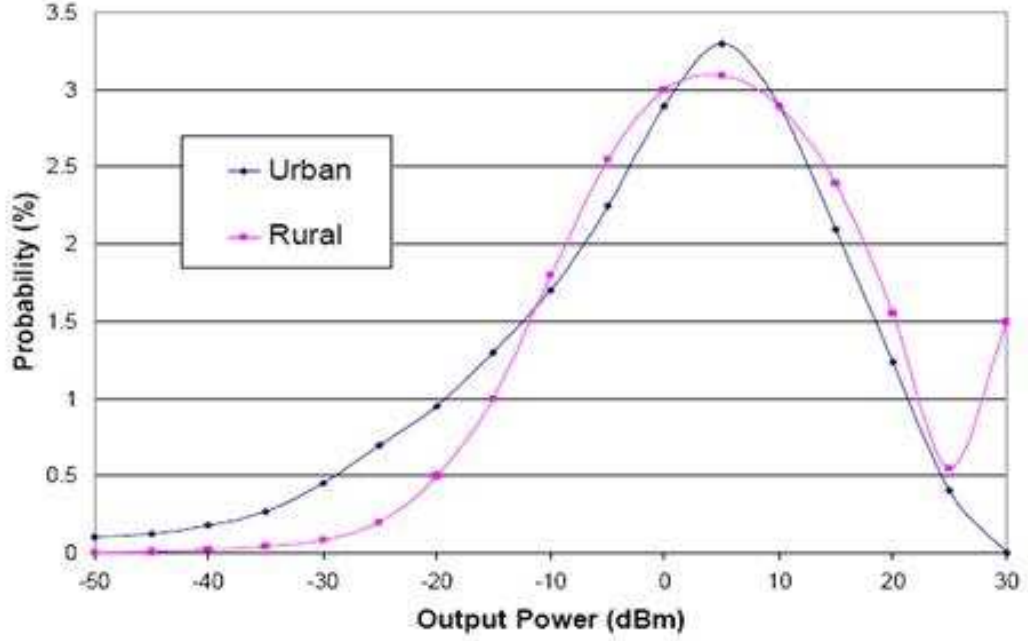


Figure 1.3: Probability Distribution Function for CDMA Applications [2].

The first reason of the back-off is the power control between the mobile unit and the base station. The second and increasingly important cause of power back-off is the high PAPR of the transmitted signal. PAPR is a measurement of signal and defined as

$$PAPR = \frac{PeakPower}{AveragePower} = \frac{\hat{v}^2}{\bar{v}^2} \quad (1.3)$$

where, $\hat{v}$ and $\bar{v}$ are maximum instantaneous voltage and rms voltage values of waveform, respectively. Modern communication systems provide high data rates within limited frequency resource and support increasing number of subscribers. As part of this evolution, new communication standards, such as WCDMA, LTE, and worldwide inter-operability for microwave access (Wi-MAX) are created. Common feature that exists in all the three standards is that they utilize high PAPR caused by complex modulation schemes. High PAPR generates rapid changes in the envelope of signal.

1.4 Role of PA

In a wireless system, PA is the final block of transmitter and interfaces with the antenna. PA must accurately and efficiently amplify input signal while providing a power gain and a minimally distorted signal to the load. Two concerns in PA design are efficiency and linearity. In many cases, these two measures have an inverse relation with each other. In other words, an improved linearity requires more power.

1.5 Previous Research Summary

1.5.1 Adaptive Current Biasing

This technique was proposed by Saleh and Cox in [10] and is one of the oldest techniques for efficiency improvement of PAs operating with varying-envelope signals. Fig. 1.4 shows how this technique works graphically. It involves dynamically controlling gate voltage of PA transistor and therefore the bias current of transistor. Depending on RF Envelope, the gate voltage is controlled. If RF

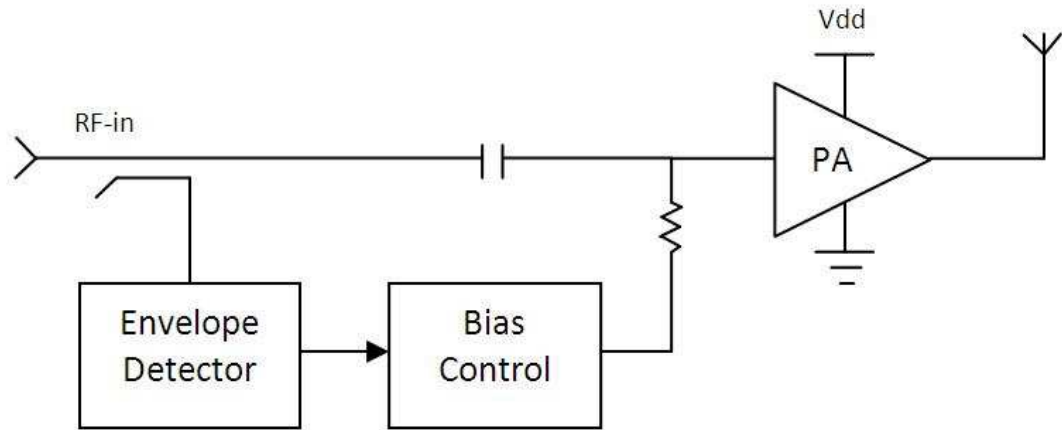


Figure 1.4: Adaptive Current Bias Class-A Transmitter

envelope increases, the gate voltage, therefore bias current of PA transistor increases. If RF envelope decreases, the gate voltage therefore bias current of PA transistor decreases. This technique changes only bias current. A constant supply voltage applied to RF transistor is still a factor of efficiency degradation as envelope varies. Saleh and Cox did not give any information how much efficiency increase did take place compared to without current biasing.

1.5.2 Envelope Tracking (ET) with Switching Amplifier

In an envelope tracking (ET) system, the supply voltage of PA is dynamically adjusted so that PA works saturated in almost all RF input levels. Therefore, PA operates near maximum efficiency even in the power back-off. This operation mainly is done by a supply modulator (SM) and therefore SM must be highly efficient. Due to their high efficiency, switching mode power supplies (SMPS) are mostly preferred for SM design. In order to use this technique for modern wireless communication signals, the switching frequency of SMPS must be high enough to supply current needed by PA, as mentioned in [11], [12] and [13]. Traditionally, linear PAs such as class-AB amplifiers are used in ET transmitters to obtain good linearity with high efficiency [14].

In [11], Hanington designed a boost converter for CDMA application with switching frequency of 10 MHz. By dynamically controlling the supply voltage of GaAs MESFET amplifier, 1.64 times higher efficiency was achieved compared to constant voltage system. The design was capable of tracking 1.22 MHz envelope bandwidth of IS-95 digital cellular standard.

In [12], Schlumpf and Dehollain represented an ET system again used for IS-95 CDMA system. The system uses a buck converter with a switching frequency of 16 MHz and is capable of tracking signals with bandwidth of 2 MHz. Although the average efficiency was not reported, they claim an efficiency increase using

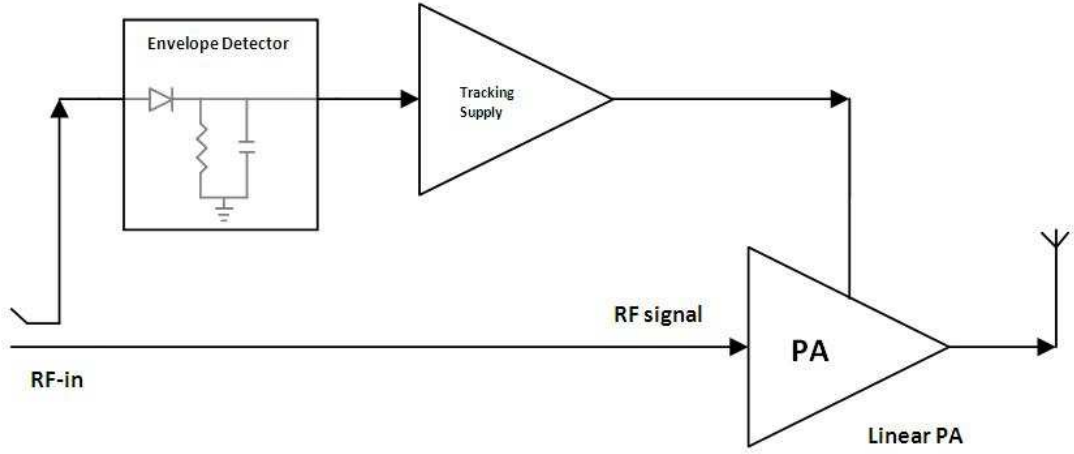


Figure 1.5: Envelope Tracking

dynamic supply PA with respect to a constant supply PA. They also tested SM using class-AB PA due to its high linearity.

1.5.3 Envelope Tracking with Hybrid Switching Amplifier (HSA)

In order to track signals with more than 2 MHz bandwidth, high switching frequencies are required. According to the sampling theory, having switching frequency twice of the bandwidth of the envelope signal is enough to track signal. In practice, a factor of ten is usually required to minimize the effects of filter ripple components [11]. The problem using high switching frequencies is the resulting switching loss.

In [15], Wang used combination of switching and linear regulators. This combination is called as Hybrid Switching Amplifier (HSA). Thanks to HSA, envelope signals up to 20 MHz were able to be tracked. High slew rate currents are supplied by linear amplifier and low slew rate currents are supplied by switching amplifier. The switching amplifier configuration was a buck converter and the supply voltage of supply modulator was 6 V. The maximum output voltage

and average efficiency were 5.2 V 50-60 %, respectively. The reported average switching frequency of the supply modulator was 7 MHz.

In [16], Jeong and Kimball used an ET system utilizing HSA configuration to achieve a high efficiency and high linearity. They tested their SM using WCDMA test signal with PAPR values of 6.6 dB, 7.7 dB and using WiMAX test signal with PAPR value of 8.8 dB. The recorded efficiency values of SM for different test signals are 75, 71 and 61 %, respectively. They concluded that, as PAPR value and envelope bandwidth of test signal increase, the overall efficiency of SM decreases.

1.5.4 Average Tracking

High switching frequency requirement of wideband signals can be eliminated if the average power is tracked. Instead of ET, the average tracking system tracks the average power transmitted. This type of system can significantly increase the efficiency for systems with low PAPR signals but a large power control range.

In [17], Staudinger proposed an average tracking system for IS-95 CDMA system. He used a PA that can transmit 2 W peak power and approximately 10 dBm average power. He used 5 MHz switching frequency for optimum efficiency and an efficiency improvement of greater than 5 times was achieved compared to fixed bias scheme.

In Georgia Institute of Technology, Sahu and Rincon-Mora designed a supply modulator using the buck-boost converter topology for CDMA applications. The converter was able to adjust the output voltage between 0.5–3.6 V using 3 V [18]. They achieved 4.4 times efficiency improvement compared to the constant supply case. Different from other designs, their solution had only 2 kHz bandwidth aimed to respond to an average power change in 200 μ s.

1.6 Research Goal

In this research, we aimed to implement a dynamic power supply (DPS) for varying envelope signals using lumped components. A detailed literature survey was performed and the highest efficient topology has been used. According to our literature survey, due to high bandwidth requirements of modern communication signals, HSA topology is the most suitable topology than the other topologies. A detailed loss mechanism research for supply modulators has been performed. In order to maximize the efficiency of the SM, dozens of power transistor, diode and inductor manufacturers' databases have been searched and some components have been compared in terms of important efficiency parameters using Spice simulations. The highest efficient components have been ordered and have been tested with test signals having two different PAPR values, 4.8 dB and 7.0 dB. Efficiency comparisons of supply modulated PA and constant supply PA have been performed using two PAs, one of which is low and other is high power.

Chapter 2

DYNAMIC POWER SUPPLIES

Supply modulation using envelope tracking (ET) can be achieved with dynamic power supplies (DPS). Linear regulators and switching mode power supplies (SMPS) are two ways of implementing these power supplies. Both have advantages and disadvantages, therefore I have first surveyed both topologies and then have given a detailed explanation of the used configuration.

2.1 Linear Regulators

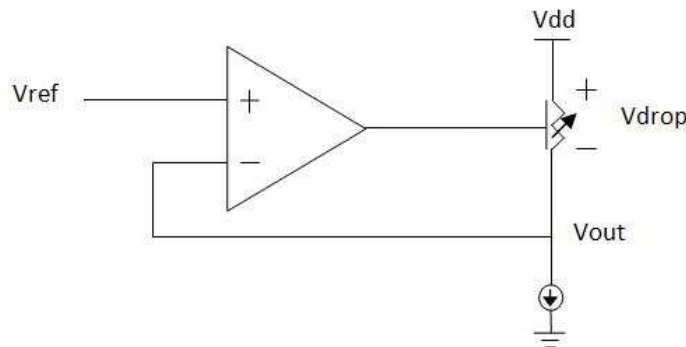


Figure 2.1: Basic Linear Regulator Topology

In Fig. 2.1, a general linear regulator topology is shown. As seen in the figure, linear regulators use controlled resistive voltage drop to regulate output voltage. Therefore, the efficiency of regulator is highly dependent on V_{drop} across the resistive element. The efficiency of a linear regulator is given by

$$\eta = \frac{V_{out}}{V_{dd}}, \quad (2.1)$$

where V_{out} is the output voltage and V_{dd} is the supply voltage. In modern IC technology, wideband linear regulators with small sizes can be implemented. However, if the efficiency is of primary concern for an application, linear regulators can be a bad choice. Especially, linear regulators used as DPSs for modern communication signals can have alarmingly low efficiency values. That is because of the high PAPR values of modern signals. Even an envelope signal having 3 dB PAPR, causes the efficiency of linear regulator to drop 50 % immediately. Therefore, care must be taken while using linear regulators.

2.2 Switching Mode Power Supplies (SMPS)

Compared to linear regulators, SMPSs are efficient even at low voltages. Mainly, there are two different SMPS topologies: Buck and Boost. In order to decide which configuration will be used, we must know the relation between PA supply voltage and battery voltage. If PA operates at nominal voltages greater than battery voltage, boost topology should be chosen. However, for most of the modern portable systems, the opposite is true. Therefore, the emphasis will be on buck converter topology. In our design, we have taken advantage of buck converter topology.

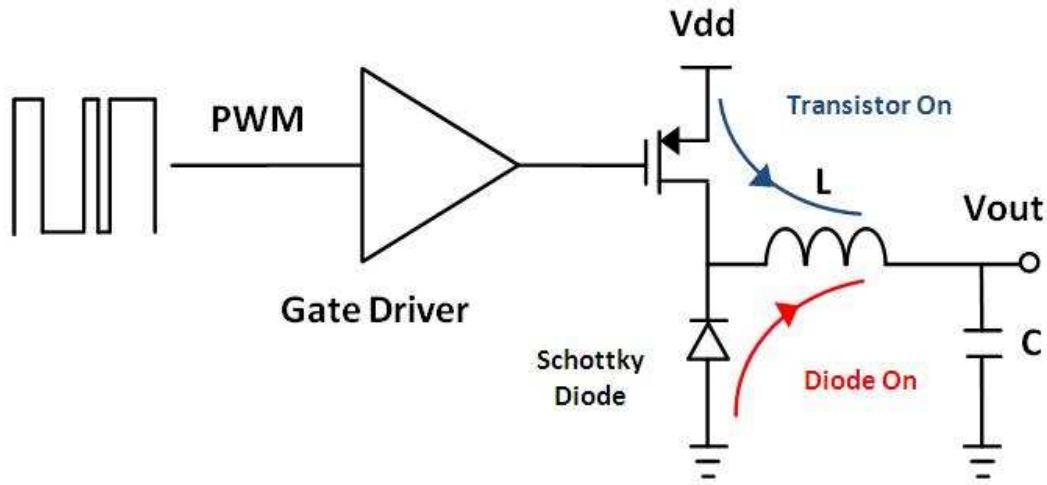


Figure 2.2: Buck Converter Topology

2.2.1 Buck Converters

In Fig. 2.2, a basic buck converter topology is demonstrated. Buck converters create output voltages lower than the supply voltage by changing the duty cycle of pulses fed to the gate of the power transistor. This operation guarantees a high efficiency at all output voltages. That is because, transistor does not carry any current when gate pulse is low. Theoretically, efficiency of a buck converter is therefore 100 %. However, in practice, due to imperfections of components, the efficiency is lower than 100 %. Mainly, there are two loss mechanisms in buck converters or generally in SMPSs: static and dynamic losses. Causes of static loss are the on-resistance of transistors, the forward voltage drop across diodes and the dc resistance of inductors. Dynamic losses are due to the switching operation of transistors and driving circuitry of the power transistor. These loss mechanisms will be discussed in more detail. Before that, the important parameters of a converter's components will be described.

Voltage rating of a transistor: While choosing the right transistor for an application, the voltage rating is one of the first parameters a designer must

check. This is the maximum voltage that a transistor is able to block in its off state. Beyond this voltage, transistor can break down.

Current rating of a transistor: As an important parameter as the voltage rating is the current rating. It is the maximum current that a transistor can carry in its on-state. This parameter is specified as the instantaneous or rms current in data sheets. Beyond this current level, the transistor can get damaged.

Switching speeds of a transistor: According to switching frequency of that converter is going to operate, the designer must pay attention to turn-on and turn-off times of a transistor. Additionally, the total gate charge or input capacitance of the transistor can be used to have an idea about how much power will be dissipated in the driver circuitry. Choosing transistors with lower gate charge provides higher speeds. If a designer plans to operate its converter at high switching frequencies, datasheet of that transistor should be analyzed well for the turn-on/off, rise/fall times and the total gate charge parameters. The drawback of using high switching frequencies is the increase in the dynamical losses. This will be discussed in more detail later.

On resistance of a transistor ($R_{DS(on)}$) : Even if a transistor's state is on, it exhibits an on-state resistance across it. This parameter is specified according to current that the transistor will carry and the gate-to-source voltage of that transistor. If our application requires high currents, in order to lower static losses in our converter, we should choose transistor with a low on-state resistance. This will prevent high on-state voltage across transistor and will increase efficiency of SMPS.

Before starting the concept of the on-state voltage of a diode, let us mention the trade-off between switching speed and the on-state resistance of a power transistor. The logic behind choosing a transistor having a low on-state resistance is obvious. The on-state voltage will be lower and therefore the dissipated power

on the transistor will also be low. The problem with choosing a transistor having the lowest on-state resistance is the high dynamical loss it will represent. That is because, low on-state resistance transistors have high input capacitances, on the other hand, if a low input capacitance transistor is chosen, then the on-state resistance will be higher although the low dynamical loss that converter presents. Therefore, the designer should analyze the application requirements well and choose the transistor according to requirements of that specified application.

On state voltage of a diode: Similar to on-state voltage across a transistor, diodes exhibit forward voltage drop across them. Choosing lower voltage diodes results in higher efficiency in SMPSs. Note that, the on state voltage of a diode is forward current dependent.

Equivalent series resistance of an inductor (ESR): Another important loss mechanism in all SMPS topologies is the dc resistance of the inductor. Higher inductor values represent higher dc resistances due to more winding. This drawback forces us to choose lower inductor values in order to lower the power loss due to the inductor. However, too low inductor values cause an increased dynamic loss and higher voltage ripple problems. A simulation about these problems are given in Chapter 3.

Saturation current of an Inductor: Another application dependent parameter is the saturation current of the inductor. For high power applications, the need for inductors with a high saturation current is inevitable. If an inductor draws a current that is higher than its saturation current, the inductor does not act as an inductor. A designer should pay attention to this specification while choosing an inductor.

2.2.2 Power Losses In A Buck Converter

As we mentioned in Chapter 1, the efficiency of a supply modulator at the back-off is highly important. Therefore, the loss mechanisms in a SMPS must be understood well for the component selection process. The power losses can be generally categorized into two main parts.

Static Loss

Due to imperfections of power transistors, inductors and diodes; converters exhibit a static power loss. These are mainly due to conduction loss of these components.

During the on-state, MOSFET conducts a drain current for an interval of T_{on} during every switching period of T_s . The ratio of $\frac{T_{on}}{T_s}$ is called the duty cycle and represented by D . Assuming that the current is constant and is equal to I_o , the rms value of MOSFET current is

$$I_T(rms) = \sqrt{D}I_o \text{ [3].} \quad (2.2)$$

I_o in this equation is equal to the output current of the converter. The average power loss in a transistor due to the on-state resistance $R_{DS(on)}$ is

$$P_{cond} = R_{DS(on)}DI_o^2. \quad (2.3)$$

One must note that, $R_{DS(on)}$ significantly changes with the junction temperature. $R_{DS(on)}$ given in datasheets are generally for 25°C junction temperature. However, to have more realistic result for conduction loss of a transistor, a designer should use twice of this resistance which corresponds to approximately 120°C junction temperature [3].

Second static loss mechanism is the copper loss of the inductor. Assuming the inductor current is constant and is equal to I_o , the average power loss due to

the inductor is given by

$$P_{ind} = R_{ind}I_o^2, \quad (2.4)$$

where R_{ind} is the equivalent series resistance of the inductor. Note that, the same as $R_{DS(on)}$, ESR also depends on the ambient temperature. Higher temperature results in a higher ESR, therefore a higher inductor loss.

The inductor value in a converter is mainly chosen according to current drawn by the inductor and the ripple requirement of the application. The saturation current level decreases as the inductor value increases. Additionally, ESR of higher inductance values is higher. Therefore, smaller inductance values is more reasonable in terms of the static loss. However, smaller inductance results in a higher ripple voltage and this may cause spectrum emission mask (SEM) problems.

The last static loss mechanism for a buck converter is the forward voltage drop over diode. Diode in a converter conducts current during the transistor is off. Since there exists a finite voltage drop over the diode, a power dissipation occurs. The average power loss due to diode is given by

$$P_{diode} = V_{diode}(1 - D)I_o, \quad (2.5)$$

where V_{diode} is equal to the forward voltage drop across diode. $(1 - D)I_o$ is used for the power calculation because, the diode conducts during the transistor is off and this is equal to $(1 - D)T_s$. Therefore, the average diode current is equal to $(1 - D)I_o$. Using a diode with a lower forward voltage drop is better in terms of the power loss. V_{diode} of Schottky diodes are lower than other diodes. Additionally, fast switching times of Schottky diodes make them a good candidate for switching applications.

Dynamic Loss

Envelope tracking (ET) for modern communication signals requires high switching frequencies due to wide bandwidth of envelope signals. At high switching frequencies, dynamic losses may be dominant. Understanding this loss mechanism is important for designing more efficient supply modulators. We will explain two important dynamic loss mechanisms. One is the switching loss due to transitions of MOSFET and the other is due to driving circuit of MOSFET. One common feature of these two loss mechanisms is that they both depend on switching frequency of the converter.

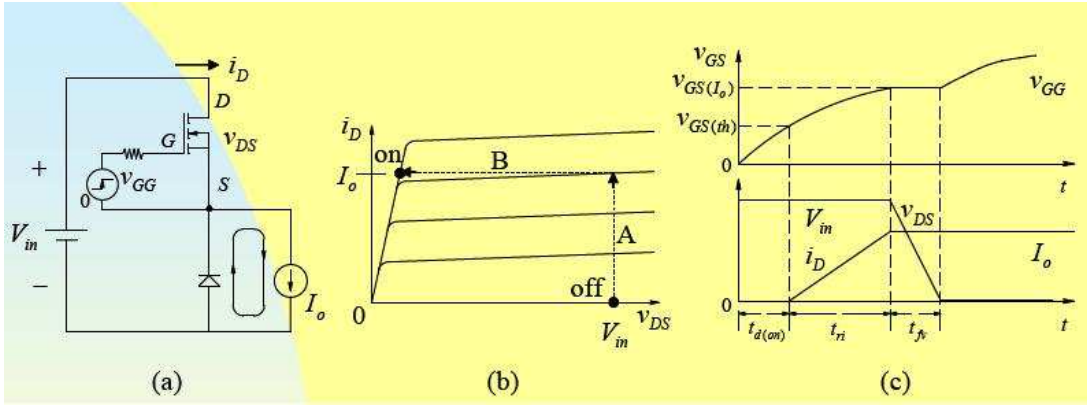


Figure 2.3: Turn-on Characteristic of MOSFET [3]

In Fig. 2.3, the turn-on behavior of a MOSFET transistor is shown. To turn MOSFET on, the gate drive voltage ramps up from 0 to V_{GG} , which requires some time called $t_{d(on)}$ to charge the gate-to-source capacitance through the gate resistance R_{gate} to the threshold voltage value of $V_{GS(th)}$ [3]. During this period, MOSFET remains off and the diode continues conducting current I_o . In order to turn-on MOSFET, i_D starts increasing. However, since the diode still conducts, assuming an ideal diode, the voltage drop across it equals to zero. Therefore, during t_{ri} , the voltage across the transistor still equals to V_{in} . Once MOSFET current reaches I_o at time $t_{d(on)} + t_{ri}$, the diode becomes reverse-biased and MOSFET voltage falls. This whole transition process causes a switching loss.

The turn-off process exhibits the same behavior. The area shown in Fig. 2.4 is

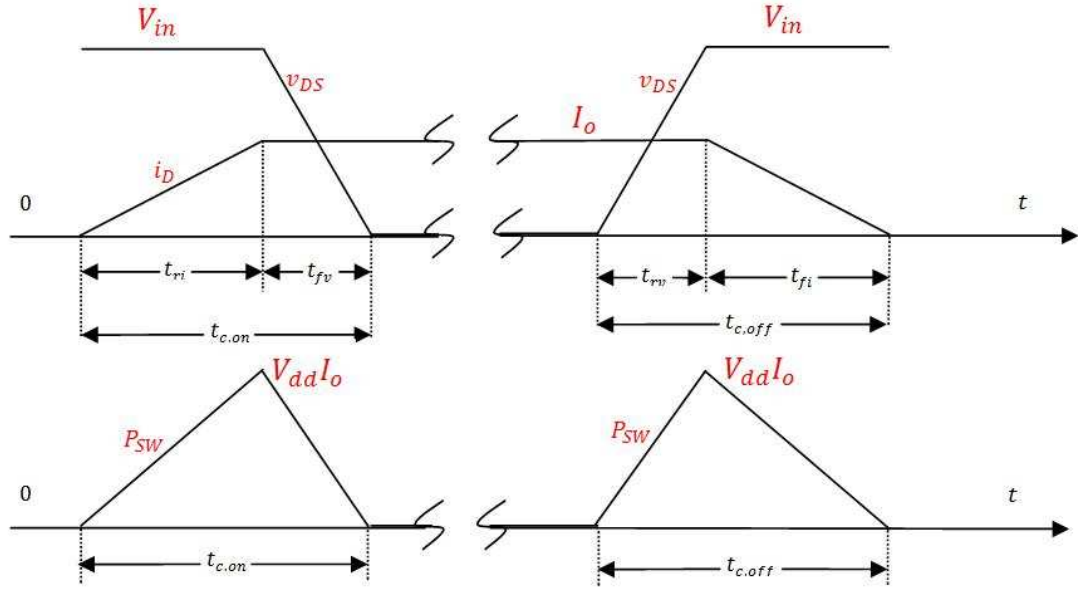


Figure 2.4: Switching loss of a MOSFET [3]

the total dissipated power in one period due to switching process of a transistor. This loss is known as P_{sw} and is given by

$$P_{sw} = \frac{1}{2} V_{in} I_o (t_{c,on} + t_{c,off}) f_s \quad [3], \quad (2.6)$$

where $t_{c,on} = t_{ri} + t_{fv}$, $t_{c,off} = t_{rv} + t_{fi}$ and f_s is switching frequency. Note that, as the switching frequency increases, the switching loss also increases. Therefore, f_s is a limiting factor for efficiency. Remembering this relation between the switching loss and the switching frequency is important throughout this thesis.

Remember that to turn MOSFET on, the gate drive voltage rises from 0 to V_{GG} while charging the gate-to-source capacitance. The charge required for charging gate-to-source capacitance comes from MOSFET driver. Let us derive the dissipated power by driver to turn-on and turn-off MOSFET. When determining the gate drive requirements for a switching device, the key specification to check is the total gate charge specified in data sheets [4]. In Fig. 2.5–(A), the gate model of a MOSFET is shown. The first stage of charging is mainly

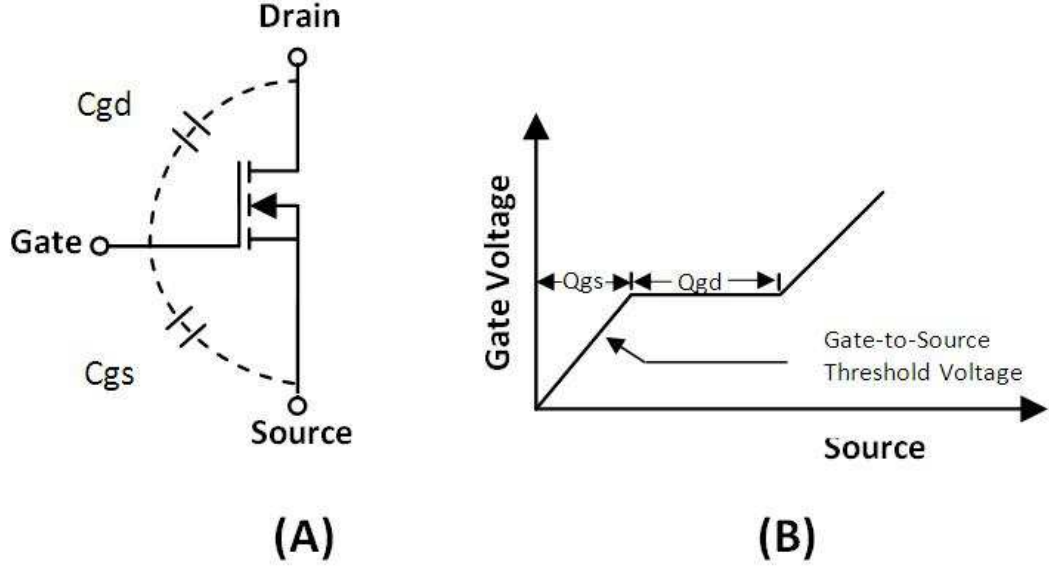


Figure 2.5: Gate Capacitance Model of a MOSFET and Charging-Up Process [4]

charging the gate-to-source capacitance as shown in Fig. 2.5–(B) [4]. Once C_{gs} is charged up to the gate threshold voltage, the transistor starts conducting and the current starts ramping up. Total gate charge, Q_{total} is equal to,

$$Q_{total} = C_{gate} V_{gate} \quad (2.7)$$

and is plotted in datasheets as a function of V_{gate} as shown in Fig. 2.5–(B). Therefore, the power required to charge the gate capacitance in one period is equal to

$$P_{gate} = \frac{1}{2} Q_{gate} V_{gate} f_s. \quad (2.8)$$

The same power will be dissipated in the driver circuitry during the turn-off process. The total power dissipated in the gate driver circuitry in one period equals

$$P_{driver} = Q_{gate} V_{gate} f_s \quad [19]. \quad (2.9)$$

Notice that $Q_{gate} f_s$ term gives the average bias current required to drive the gate of a transistor. Same as switching loss, the driver circuitry loss also increases as switching frequency f_s increases.

While choosing a power MOSFET, depending on switching frequency of application, the dynamic loss due to both switching loss and the driver loss may be dominant. Therefore, giving high importance to the total gate charge and the switching transition time parameters of transistor is crucial.

2.3 Hybrid Switching Amplifier (HSA)

As stated before, tracking of modern communication signals having wide bandwidth requires high switching frequencies for SMPSs. However, using high switching frequencies results in high dynamical losses due to both switching and driver circuitry losses. HSA is a good solution for high switching frequency requirement. It consists of both a linear amplifier and a SMPS. The designed supply modulator (SM) consists of a linear amplifier and a buck converter as SMPS. How this configuration works is described below. As shown in Fig. 2.6, HSA

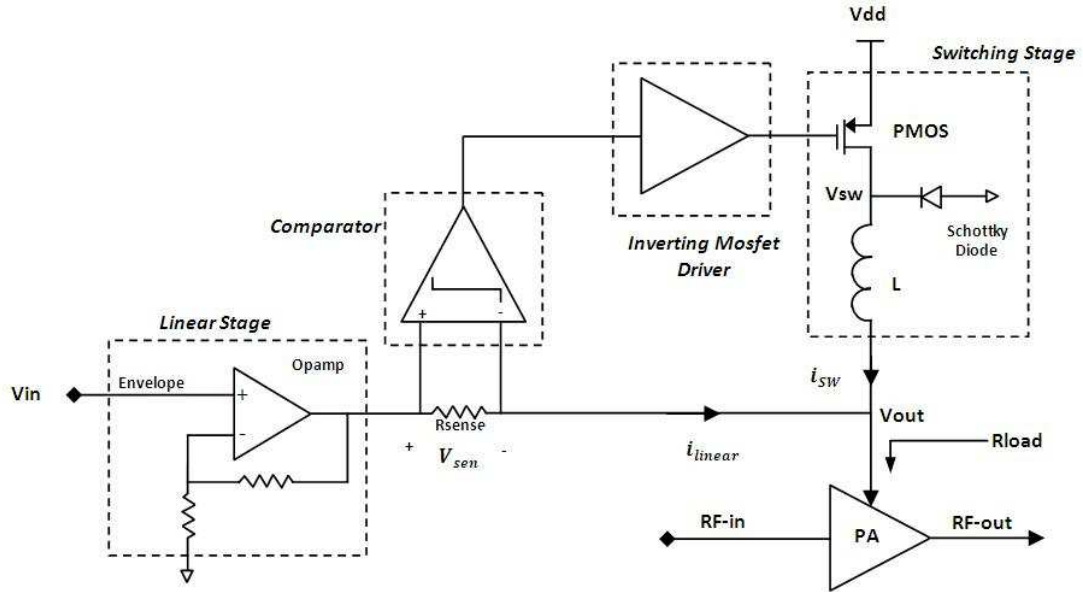


Figure 2.6: HSA configuration

consists of two stages: linear and switching stages. Although low efficiency of linear stage is known, it is used to decrease high switching frequency requirement

of core buck converter topology. In HSA, both linear stage and switching stage provide current to PA. Advantage of linear stage comes from its wide bandwidth. Therefore, at high slew-rate sections of envelope signal, the opamp supplies the current. As it can be seen in Fig. 2.6, the envelope of RF signal is fed into the

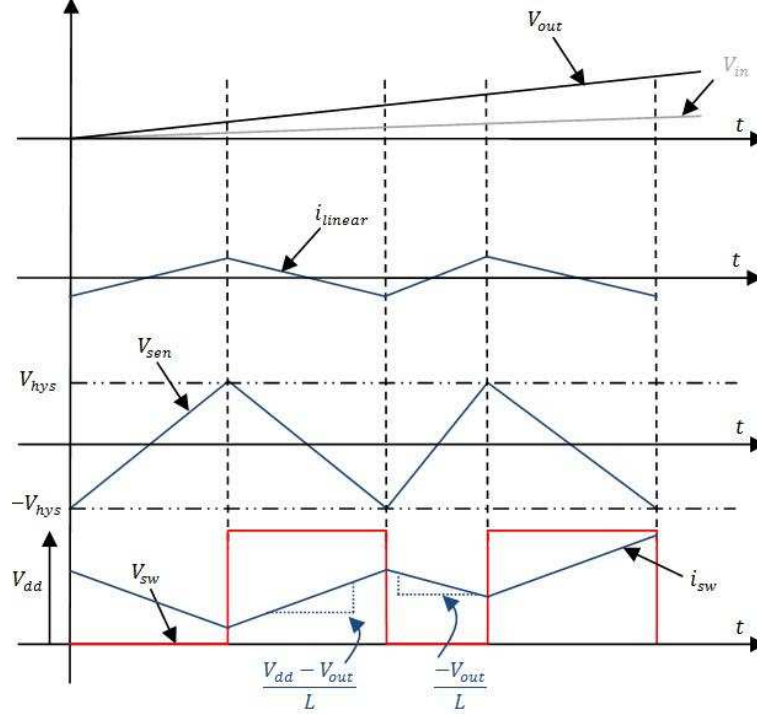


Figure 2.7: MOSFET gate pulse generation

non-inverting input of the linear stage opamp. Let us assume that the envelope increases. As the envelope increases, the output current of opamp also increases and that causes V_{sense} over R_{sense} to increase. After V_{sense} reached $+V_{hysteresis}$ voltage of the comparator, the comparator creates a high voltage and inverting MOSFET driver creates a low voltage. The low voltage at gate, turns P-MOS on. The required PA current starts to be provided by the switching stage at a rate of $\frac{V_{DD}-V_{OUT}}{L}$. The current from the linear stage starts to decrease. This causes V_{sense} to decrease. After V_{sense} reached $-V_{hysteresis}$ voltage of the comparator, the comparator creates a low voltage and the inverting MOSFET driver creates a high voltage. The high voltage at the gate, turns P-MOS off and the current provided by the switching stage starts to decrease at a rate of $\frac{-V_{OUT}}{L}$, assuming

an ideal diode. In general, depending on the envelope in the input and pulse at the gate of the P-MOS, binary pulses, 0 or V_{DD} are generated at the drain. Filtering these pulses by help of an inductor, the input waveform is recovered. Continuing this operation, most of the current is supplied by the switching stage. The value of the inductor that must be used to guarantee that most of the current required for PA is supplied by switching stage will be formulated later. For now, remember that the chosen inductor value changes the switching frequency of the switching stage. Therefore, depending on the bandwidth of the envelope signal, the inductor value should be changed. Switching frequency is given by

$$f_{sw} = \frac{R_{sense} V_{out} (V_{dd} - V_{out})}{2V_{dd} L V_{hysteresis}} [20]. \quad (2.10)$$

Note that, as the inductor value increases the switching frequency decreases. Using HSA configuration and changing L and R_{sense} values, we can limit switching frequency of switching stage and therefore high dynamic losses are prevented. However, due to low efficiency of linear stage, the efficiency of SM degrades. We should choose inductor value carefully. Another important point is that, when V_{out} equals to $\frac{V_{dd}}{2}$, the switching frequency is maximized and is equal to

$$f_{sw,max} = \frac{R_{sense} V_{dd}}{8L V_{hysteresis}}. \quad (2.11)$$

2.3.1 Choosing L value for HSA

In order to provide most of the current through switching stage, the inductor should be able to supply current at any rate of change [20]. Assuming that the output voltage V_{out} is sinusoidal and the drain of PA is resistive, the maximum inductor value can be derived.

$$V_{out} = V_o \sin(2\pi f_s t) \implies I_{out} = \frac{V_o \sin(2\pi f_s t)}{R_{load}} \quad (2.12)$$

$$\frac{di_{out}}{dt} = \frac{2\pi f_s V_o}{R_{load}} \cos(2\pi f_s t) \leq \frac{V_{dd} - V_o \sin(2\pi f_s t)}{L} \quad (2.13)$$

$$L \leq \frac{R_{load} (V_{dd} - V_o \sin(2\pi f_s t))}{2\pi f_s V_o \cos(2\pi f_s t)} \quad (2.14)$$

By differentiating (2.14) and equating it to zero, the required maximum inductance can be found as

$$L = \frac{R_{load} \sqrt{V_{dd}^2 - V_o^2}}{2\pi f_s V_o}. \quad (2.15)$$

Substituting (2.15) into (2.11), the minimum f_{sw} required to provide most of the current through switching stage is

$$f_{sw} = \frac{\pi f_s V_{dd} R_{sense} V_o}{4V_{hysteresis} R_{load} \sqrt{V_{dd}^2 - V_o^2}} [20]. \quad (2.16)$$

The switching frequency satisfying (2.16) is generally too high for modern communication signals. For example, assume you design a SM that tracks 1 MHz sinusoidal signal. In addition, let us assume that all other parameters such as V_{DD} , V_O or R_{sense} are the same as one of my test cases shown in Chapter 3. If these parameters are put into (2.16), the switching frequency is found as 48.25 MHz. As you see even tracking 1 MHz sinusoidal signal requires too high a switching frequency and causes a high dynamic losses. Therefore, in HSA design, the linear stage is used to mitigate the high switching frequency requirement. That is basically succeeded by the value of inductor.

The inductor selection is an important part of HSA design for modern communication signals. Let us use different mode of operation than described in Section 2.3.1. The inductor determined by (2.15) is increased to lower the slew rate of the switching stage [20]. After increasing the inductor value, the slew rate that the switching stage can provide decreases. Remaining current that the load needs is provided by the linear stage with lower efficiency. However, the efficiency degradation using linear amplifier is smaller than the high dynamic loss caused by the switching stage if the whole current was supplied by the switching stage. We have shown this result using one of the simulations in Chapter 3. The linear stage is able to provide high slew rates, because the bandwidth of op-amp used as linear stage is high enough. Therefore, opamp used in linear stage is

also application dependent. For applications with high PAPR and wide envelope bandwidth, in order to compensate current that switching stage is not able to provide, the opamp should have a high unity gain bandwidth.

Efficiency of supply modulator using HSA therefore depends on two major things other than imperfections of parts used. One is PAPR the other is bandwidth of the envelope. In HSA, in order to prevent high switching frequencies for wideband signals, we use a linear amplifier. However, the efficiency of linear amplifier decreases as PAPR increases due to nature of linear amplifiers as stated before. Although, the efficiency of the supply modulator decreases for high PAPR signals, the gain of HSA usage increases compared to the constant supply voltage. Because, for high PAPR signals, the dissipated power also increases for the case of the constant supply case.

2.4 How Supply Modulation Causes Nonlinearity

Although maximizing efficiency of supply modulator is of primary concern, we should not forget that our DPS will be used with a PA and the nonlinear behavior of the output capacitance and transconductance of PA transistor cause an impedance mismatch, nonuniform gain and phase distortion, when the supply voltage changes [21].

AM–AM or AM–PM distortion usually does not matter for low PAPR envelope signals, because the supply voltage of PA is mostly modulated above $V_{dd}/2$ [22]. However, for most of the modern communication signals, PAPR values are considerably high. As PAPR of the signal increases, the average supply voltage of the PA spends most of the time at a low V_{dd} , where the nonlinear effects are significant. In order to mitigate the non-linear effects introduced by

PA characteristics, we have avoided supply voltages lower than $V_{dd}/2$ for DPS. However, we will talk about this problem shortly.

First thing that we should realize is the gain variation caused by the supply modulation of the PA decreases. The gain tends to decrease as the drain voltage of PA decreases. This gain variation also depends on the technology of power transistor. Secondly, the drain-to-source capacitance changes as the drain voltage changes. That allows proper output matching only for a limited voltage range. Therefore, to minimize the impedance matching problem, the PA should be optimized in the most probable region of signal distribution [21].

To mitigate these problems, an envelope shaping could be performed. In this technique, the supply voltage of PA is not allowed to fall below a pre-determined voltage level. In general, using signal processing techniques on envelope signal allows this operation to be performed easily. The envelope shaping is important both to mitigate the nonlinear effects caused by supply voltage variation and also for reducing the voltage losses caused by the dynamic power supply. Predistortion techniques are also deeply analyzed and used with envelope tracking systems to satisfy linearity specs of wireless communication standards [23].

There are no well defined equations related to nonlinear effects of supply modulation. Therefore, while dealing with nonlinear distortion problems that supply modulation causes, best way is to characterize PA well. For different supply voltages that are greater than knee voltage of PA transistor, the gain and P1dB and P3dB points should be determined and then PA must be optimized in the most probable region of signal distribution.

Chapter 3

DYNAMIC POWER SUPPLY DESIGN

In this chapter, we give information about the designed low power PA briefly, and the design procedure of the dynamic power supply (DPS) in detail. The information, formulas and symbols represented in Chapter 2 are going to be used on the design process. The simulations are performed using PSpice and used to decide which components and values to use. In the simulations, a sinusoidal signal and a varying envelope signal having two different PAPR values are used as test signals. We have tried to understand, how bandwidth and PAPR of test signal change the efficiency of the DPS. In addition, the DPS has been tested at two output powers to understand how the drawn current and output voltage change its characteristic. Finally, the effect of inductor value on switching frequency and the efficiency of the DPS have been investigated.

While starting this project, our first aim was to check efficiency improvement provided by DPS taking advantage of envelope tracking. The output power of the supply was not first concern. Therefore, without concerning about the output power we have designed a PA to test the performance of the supply modulator

(SM). Below you will find the simulation results of the PA. After we have seen that the DPS works well, it has been tested with another and more powerful amplifier. We have no simulation results for the higher-power amplifier. The SM design for these two applications will be main focus of this chapter.

3.1 The PA Design

We have designed a PA using low voltage, P-HEMT, ATF-501P8 transistor manufactured by Avago Technologies. As the operation frequency, we have chosen 1.95 GHz. Using Advanced Design System (ADS) simulation program, we have designed the tuning circuits both for load and source. We have used Rogers' RO4003C as a laminate for the PA.

On the transistor's datasheet, the manufacturer specifies Γ_S and Γ_L values for optimum P_{1dB} at 2 GHz. Using ADS's matching tool, we have designed the microstrip matching circuits. Using the matching circuits and the transistor manufacturer's model, we have performed large signal S-Parameter simulations. Below you can find some simulation results of the PA.

In Fig. 3.1, the gain vs input power plot of the PA is seen as simulated in ADS. As can be seen, the input 1dB compression point of the PA is 18.9 dBm, where the gain is almost 12.5 dB. Referring to Fig. 3.2, the output 1dB compression point is therefore 31.4 dBm. In the datasheet, the manufacturer specifies results close to these results. According to the datasheet, the gain and P_{1dB} are 14.7 dB and 30.6 dBm, respectively. At this stage, we believed the PA is ready to manufacture. Remember that, our main concern has been to design a PA to test our supply modulator. The detailed analysis of the PA therefore is not given. The current drawn for a specific output power by PA plays key role in any SM's component selection process. Components of supply modulator

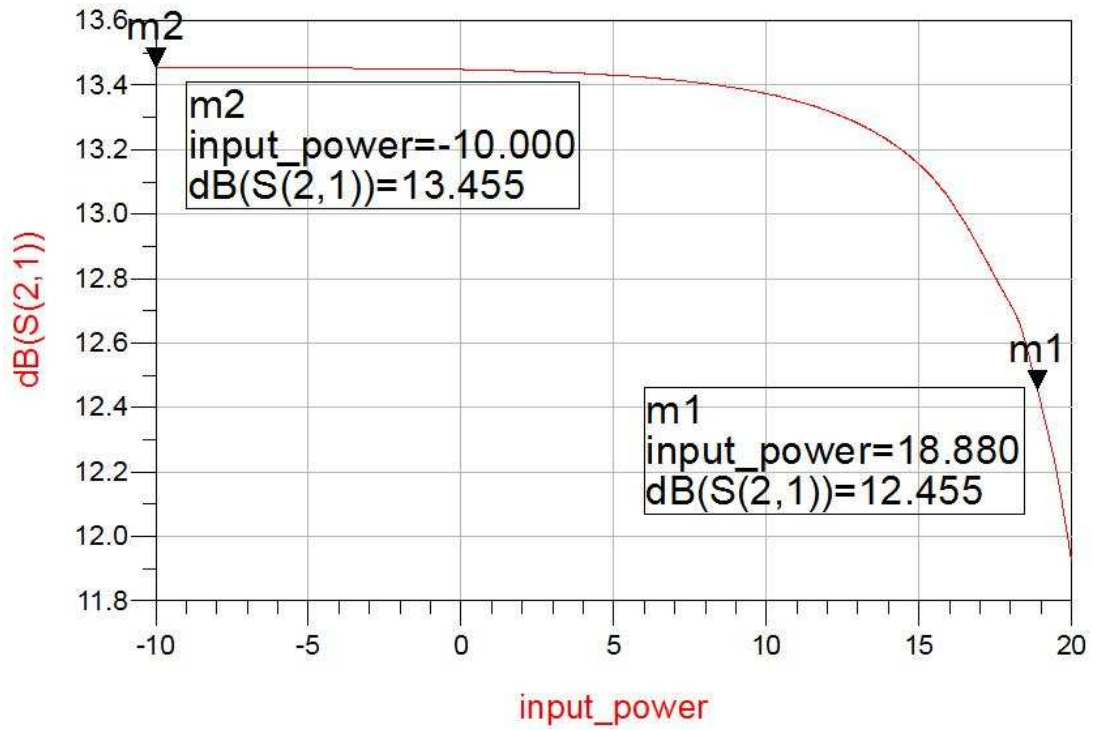


Figure 3.1: $S(2,1)$ response of low power PA

must support maximum required current for PA. The simulations are important to have a rough idea about this concern.

Note that, due to high linearity requirements of new standards, we have to operate the PA roughly at “PAPR” dB back-off than the 1 dB compression point. Even that causes the peak points of envelope to be compressed 1 dB. Depending on the statistics of the envelope signal, this may cause a high non-linearity.

3.2 The Dynamic Power Supply Design

Before starting a DPS design for a modern wireless communication system, the system requirements must be analyzed in detail. The most important parameters are the average output power of PA and the envelope bandwidth of RF signal. Note that, for a specific output power, we should also specify the operating

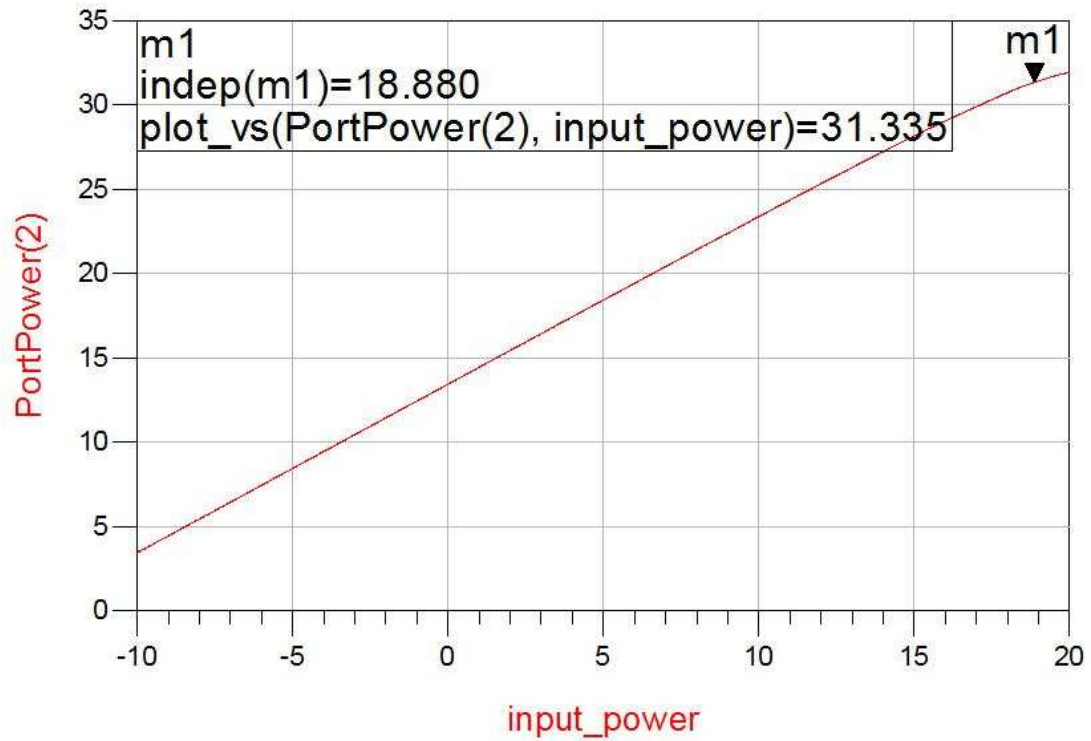


Figure 3.2: 1 dB compression plot of low power PA

voltage to estimate how much current will be drawn by PA. The bandwidth of envelope is important to decide how fast SM should be. In our tests, we have used WCDMA signal as test signal. According to parameters of WCDMA, the channel bandwidth and the chip rate are 5 MHz and 3.84 Mcps, respectively. Therefore, SM should be able to provide current to the PA at these rates. Both specifications play important role in SM design and component selection.

As seen in Chapter 2, the SM consists of two stages: switching and linear. Designing high efficient switching stage is the first task that we need to succeed. Therefore, we have started with the switching stage design first. After that, the linear stage is included in the simulations. For the simulations consisting of the linear stage, we thought that the best is first dealing with a sinusoidal test signal. Therefore, we have started simulating the switching stage assisted with the linear stage first with a sinusoidal signal. The operational amplifier used in the linear part should satisfy some requirements and we have used this

part to show the importance of these requirements. After we have succeeded tracking the sinusoidal signal with high efficiency, we have started to test the power supply with two different PAPR WCDMA signals. The WCDMA test signals are extracted from a RF signal using ADL5511, which is an envelope detector of Analog Devices. The extracted data has been saved and used in the DPS design and simulation procedures. The extraction of envelope from RF signal has resulted in more precise efficiency estimations. Our DPS is planned to operate at both low power and high power applications. Therefore, 6.50 V and 12.0 V are chosen as operating voltages.

In the simulation process, we need to decide what the average output power of the low and high power PAs will be. This is important, because the load connected to the output of the SM in the simulations will be decided according to the average output power. Choosing the right load is important for accurate simulations. Predicting the average power just from simulations may cause non-realistic results. That is because, the RF simulations are performed using single tone signal other than WCDMA signal having same PAPR as test signals. We have performed the RF simulations only to predict the compression point of the PA. In fact, the average output power in real tests depends on how the PA is driven. As long as spectrum emission mask regulations are provided, it can be chosen by user. Therefore, the load connected to output of supply modulator has been decided according to average output power extracted from the measurement results. Of course, the average output power depends on the PAPR of the test signal. Since in measurements two PAPR test signals have been used, we are going to use these two test signals in simulations too.

The 4.8 dB and 7.0 dB PAPR WCDMA signals will be used in the measurements. While detecting the envelope of the signals, ADL5511 does not allow envelope to be 1.10 V and lower values. As a result, the test signals of SM do

not have 4.8 dB and 7.0 dB PAPR but lower PAPRs. The resulting signal is important because rms output voltage can only be determined using the resulting signal at the output of ADL5511. Since this signal cannot be predicted beforehand, rms output voltage information is also extracted from measurements. Therefore, the output voltage of ADL5511 for both WCDMA signal have been saved and used in simulations.

3.2.1 The Switching Stage

The main loss mechanisms for a switching converter are summarized in Chapter 2. Switching frequency and V_{dd} are application dependent and we generally have no control on these parameters. Of course, one can control switching frequency by choosing higher inductor values as stated in (2.15). The simulation results related to the different inductor values will be given later. The component selection will be mainly dependent on turn-on/turn-off times and the total gate charge parameters of transistor. The dynamic losses have been controlled by paying attention to these parameters. Additionally, static losses also play key role. Components such as inductors and diodes mainly dominates the static losses. As it will be seen later, the efficiency of our application mainly depends on the dynamical losses rather than the static losses. Below, you see the low power 4.8 dB case in detail.

According to the measurements, 27.5 dBm average output power at the output of the low power PA has been measured for the 4.8 dB PAPR input signal. In Fig. 3.3, the portion of the signal is seen that belongs to the output of ADL5511 envelope detector, when input signal is the 4.8 dB PAPR WCDMA signal and the PA's average output power is 27.5 dBm. The envelope signal at the output of the envelope detector is input to the SM. For a system of 6.50 Volts, the peak value of envelope must be 6.50 V. According to saved data at the output of ADL5511, the maximum and rms voltages are 3.50 V and 2.45 V, respectively. Therefore, a

gain of 1.85 is provided by the opamp to reach 6.50 V. The estimated rms voltage at the PA's drain is 4.50 V. The output rms voltage is important to decide the load of the SM for simulations.

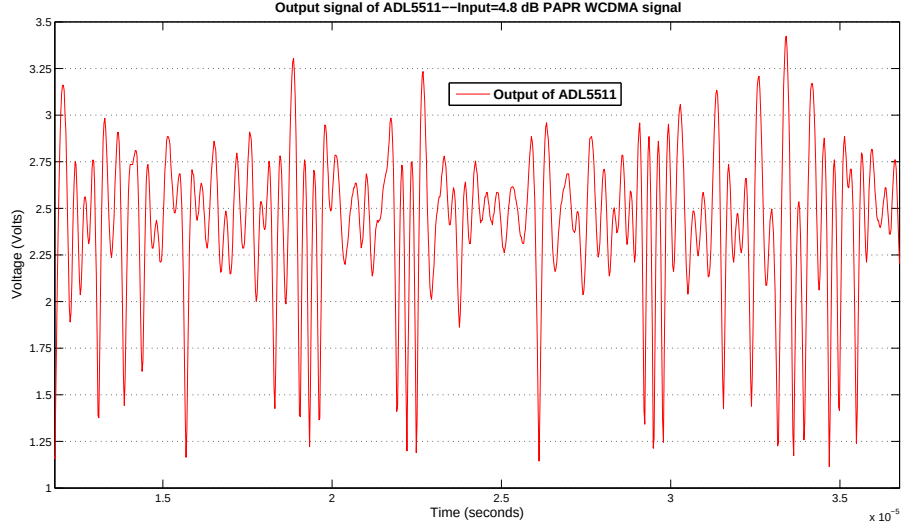


Figure 3.3: A portion of the 4.8 dB PAPR signal at the output of ADL5511

The average output power of the PA is 27.5 dBm, which is about 0.560 W. If the efficiency of the PA was 100 % for a 0.560 W output power, the required output current is about $\frac{0.560}{4.50} = 124 \text{ mA}$. However, the efficiency of the PA is not 100 %. According to the simulation results and datasheet information, the estimated efficiency is about 40 %. Therefore, the required output current is $\frac{124}{0.400} = 311 \text{ mA}$. This means that we can test the dynamic supply by connecting a resistance of $\frac{4.50V}{0.311A} = 14.5 \Omega$ as load. In Table 3.1, you see the results of the same analysis performed for all cases.

Table 3.1: Estimated output statistics of all cases

Output Graph	$P_{outPA}(W)$	$P_{outSM}(W)$	$\eta_{PA}(\%)$	$V_{out}(V)$	$R_{load}(\Omega)$
Low Power-4.8 dB	0.560	1.40	40	4.50	14.5
Low Power-7 dB	0.470	1.17	40	3.90	13.0
High Power-7 dB	3.55	9.00	40	8.10	7.30

In order to test the switching part only, we do not need a varying envelope signal. The square wave having a $100 * \frac{4.50}{6.50} = 69.2 \%$ duty cycle is enough to

create 4.50 V out of 6.50 V. In the example, the frequency of the square wave is 4 MHz. Remember that the switching frequency is related to bandwidth of envelope signal, which is 5 MHz for WCDMA. In summary, we will design a highly-efficient switching stage that creates 4.50 V output voltage and 0.311 A output current. Analyzing switching stage is important in order to understand which components cause efficiency degradation the most.

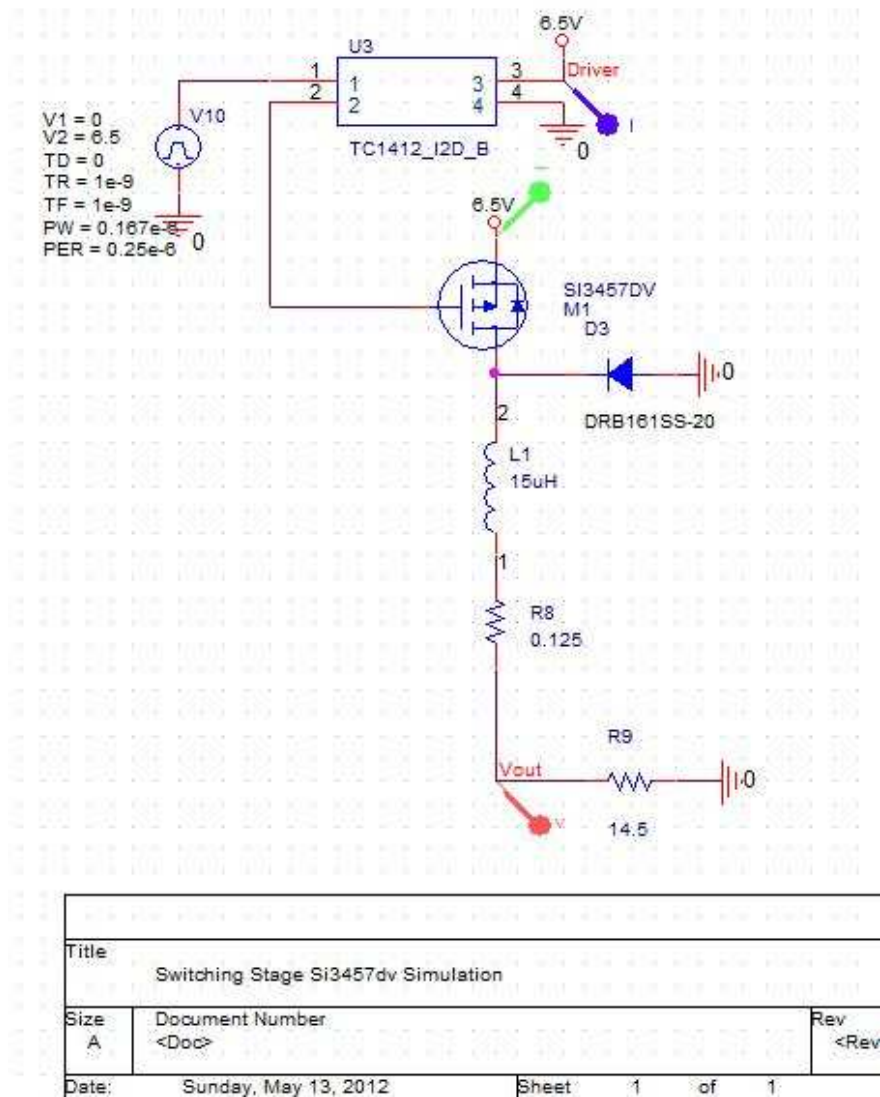


Figure 3.4: Simulation circuit of switching stage with SI3457DV-4.8 dB

The simulation results of the circuit given in Fig. 3.4 are given in Fig. 3.5. The results as given in Fig. 3.5 shows that the average current drawn from the

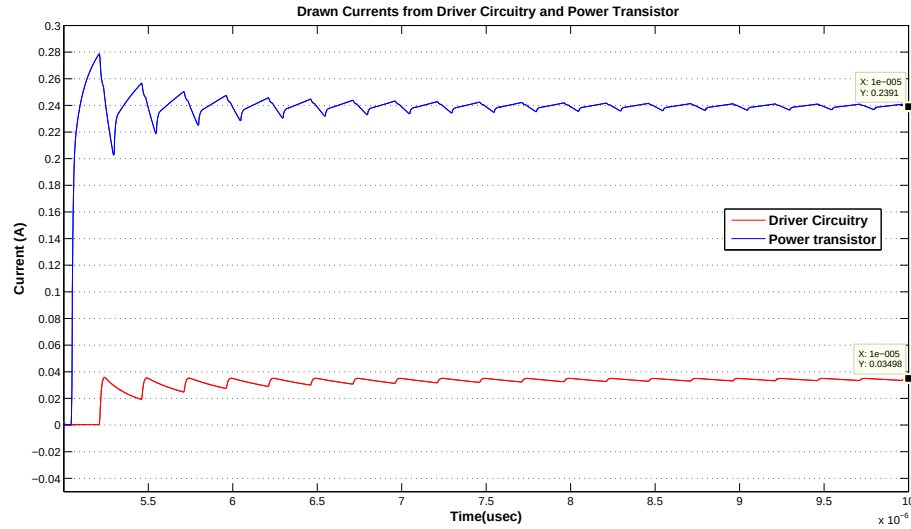


Figure 3.5: Average current simulation results of switching stage-4.8 dB

6.5 V voltage source to create 0.311 A over 14.5 ohms is about 275 mA. 35.0 mA of the current is drawn by the driver circuitry. The total dissipated power to create 1.40 W is about $275e - 3 \times 6.50 = 1.78W$. The total efficiency is therefore $100 \times \frac{1.40}{1.78} = 78.3 \%$. The result of this simulation gives us a rough idea about the efficiency of the switching stage. Which component in the switching stage causes most of the dissipation is not obvious. So we will try to estimate the efficiency using formulas given in chapter 2. This analysis will give us a chance to understand the components with the most dissipation.

For the above simulation and coming analysis, we have used one of the first transistors studied in the design process, called SI3457DV. We have performed this part to show you how important switching parameters of a power transistor. Remember that the analysis does not belong to the final design. The specifications of SI3457DV and other components that will be used in the analysis such as inductor and diode are listed in Table 3.2. Using the specifications given in the Table 3.2 and loss formulas given in Chapter 2, we calculated the total loss as below:

Table 3.2: Component Parameters

Component	$R_{DS(on)}$	$t_{c,on}$	$t_{c,off}$	Q_{gate}	R_{ind}	V_{diode}
SI3457DV	75 $m\Omega$	7 ns	16 ns	9 nC	—	—
FDN352AP	180 $m\Omega$	4 ns	10 ns	3 nC	—	—
Inductor	—	—	—	—	125 $m\Omega$	—
Diode	—	—	—	—	—	0.400V

The static loss is given by:

$$P_{cond} = R_{DS(on)} DI_o^2 = 0.075 \times 0.69 \times 0.311^2 = 5.0 \text{ mW}$$

$$P_{ind} = R_{ind} I_o^2 = 0.125 \times 0.311^2 = 12.1 \text{ mW}$$

$$P_{diode} = V_{diode}(1 - D)I_o = 0.400 \times 0.310 \times 0.311 = 38.6 \text{ mW}$$

The dynamic loss is given by:

$$P_{sw} = \frac{1}{2} V_{in} I_o (t_{c,on} + t_{c,off}) f_s = \frac{1}{2} \times 6.5 \times 0.311 \times (23e - 9) \times 4.0e6 = 93 \text{ mW}$$

$$P_{driver} = Q_{gate} V_{gate} f_s = 9.00e - 9 \times 6.50 \times 4.00e6 = 234 \text{ mW}$$

The total loss is,

$$P_{total} = 382.7 \text{ mW}$$

Remembering that the output power is about 1.40 W, the estimated efficiency is $100 \times \frac{1.40W}{1.40W+0.383W} = 78.7 \%$. In the future, we will add the linear stage to this configuration and the efficiency will decrease further. Note that the power is dissipated mostly due to the driver circuitry and the switching operation of the transistor. The parameters of V_{gate} , f_s , $t_{c,on}$, $t_{c,off}$ and Q_{gate} are main causes for this type of dissipation. V_{gate} and f_s are mainly application dependent and cannot be changed. As stated before, we can use a different transistor with smaller $t_{c,on}$, $t_{c,off}$ times and lower Q_{gate} parameters. In Table 3.3, you see the simulated efficiencies of the switching stages with SI3457DV transistor for the cases of low power 4.8 dB and 7.0 dB and high power 7.0 dB.

Table 3.3: Simulated Efficiency Results of Switching Stage with SI3457DV

Efficiency(Sim.)	$I_{transistor}(mA)$	$I_{driver}(mA)$	$P_{out}(W)$	$\eta(\%)$
Low Power-4.8 dB	245	35.0	1.40	76.7
Low Power-7 dB	210.0	35.0	1.17	73.5
High Power-7 dB	905	63.0	9.00	77.5

In Table 3.2, you see the component specifications of FDN352AP, which is the actual power transistor used in the designed SM. Now let us do the same analysis using FDN352AP. All the other components and the parameters such as duty cycle and switching frequency stay unchanged. In Table 3.4, you see the results of all cases.

Table 3.4: Simulated Efficiency Results of Switching Stage with FDN352AP

Efficiency(Sim.)	$I_{transistor}(mA)$	$I_{driver}(mA)$	$P_{out}(W)$	$\eta(\%)$
Low Power-4.8 dB	240.0	15.0	1.40	84.5
Low Power-7 dB	205	15.0	1.17	81.8
High Power-7 dB	875	27.0	9.00	83.1

The analysis basically shows that dynamic parameters of components are more important than static parameters especially for modern communication signals. We have controlled this result by comparing two transistors with different gate charges and transition times. Compared to the results given in Table 3.3, efficiencies has increased approximately 8 % for all cases by only changing the power transistor.

3.2.2 The Switching Stage Combined with The Linear Stage (Opamp Selection)

Remember that in Chapter 2, we mentioned why the inductor value determined by (2.15) is increased. The reason is to lower the slew rate of the switching stage and as a result to lower the switching frequency. This operation causes the linear stage to supply fast varying sections of envelope. The linear stage is performed via a high bandwidth opamp. The high bandwidth requirement

is needed because the fast changing parts of envelope signal will be supported by the linear regulator. Another highly important specification that the opamp must carry is high output current. The output current of opamp should be high enough to provide current that PA needs. Below you will find the simulations showing how these parameters are important especially for the high power case.

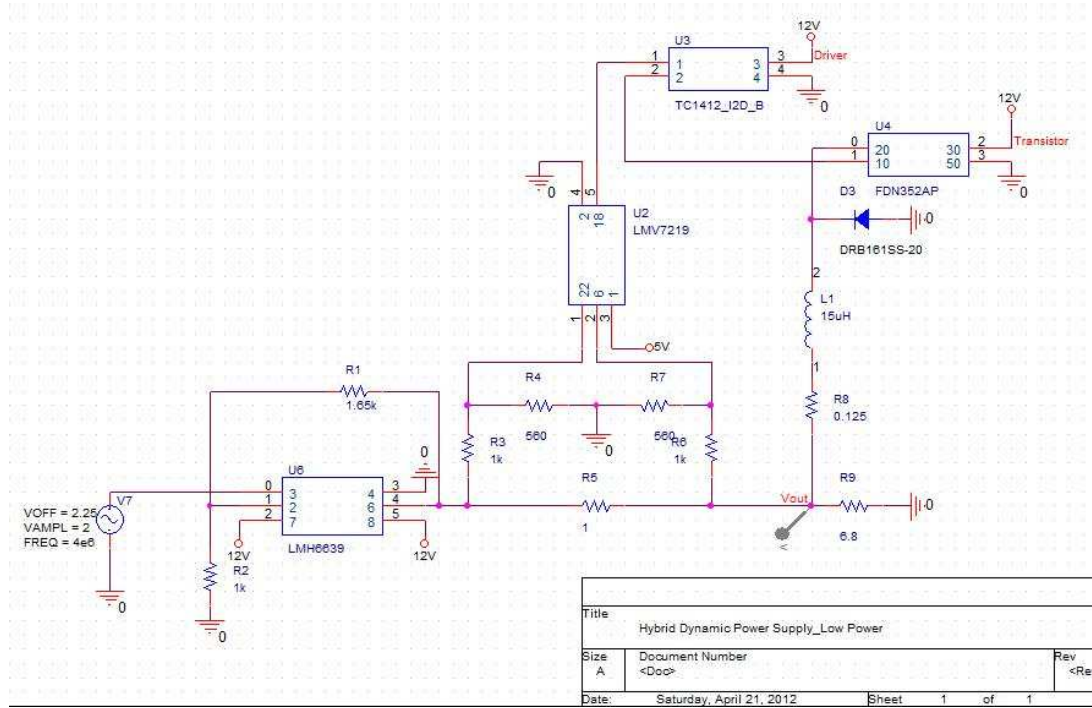


Figure 3.6: Comparison of two opamps used for hybrid switching supply

In this simulation set, we have compared two high bandwidth opamps in terms of their output current. The opamp with part number LMH6639 was the first opamp used for the low power case. However, for high output power case, the output current of the opamp was not sufficient and that was causing distorted WCDMA signal at the output of dynamic power supply. The high output current requirement that the linear regulator must satisfy has been then realized. The opamp we have used that has high bandwidth and high output current is AD8017. Below you will see the comparison of the two opamps with 4 MHz sinusoidal signal. Our aim was to test the high output power case, so the

input voltage and the load resistance shown in Fig. 3.6 were chosen such that the output power is about 6.8–6.9 Watts.

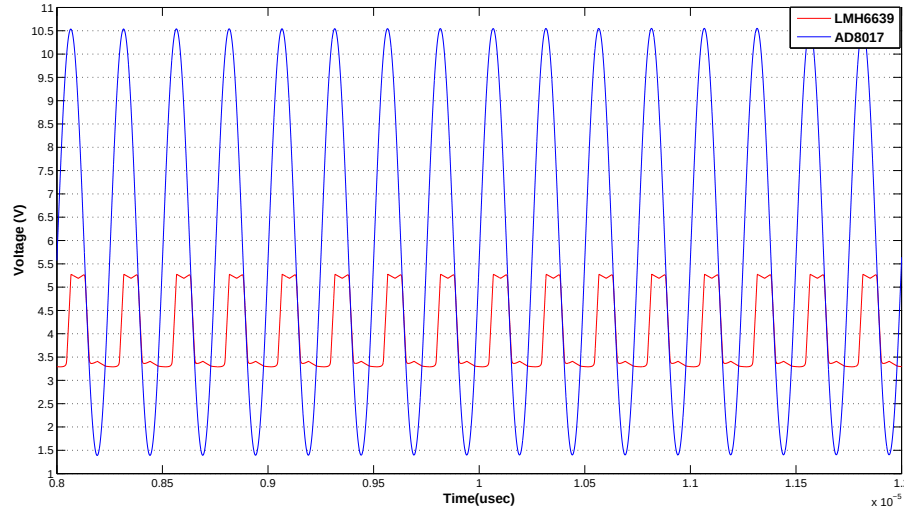


Figure 3.7: Comparison of two opamps used for hybrid switching supply waveforms

In Fig. 3.7, the simulation results of schematic shown in Fig. 3.6 are shown. Note that LMH6639 is not able to provide enough current at high enough rates that load needs. The output voltage is clipped around 3.25 V and 5.25 V. Although the estimated rms voltage of output is about 7 V, the output rms voltage for the LMH6639 case is only 4.30 V. However, AD8017 is able to provide high current at high enough rates.

The power transistor and high bandwidth and current opamp are two the most important components for the DPS. We have tried to explain which parameters are important while selecting these components and how these parameters change the output voltage and the efficiency of system. Two other components that are also important are inductor and diodes. While choosing the inductor, we have checked the saturation current and dc resistance of it. Note that, the average output current might be misleading in the process of inductor selection

because the peak current that inductor draws is higher than average output current, which depends on PAPR of signal.

3.2.3 The Supply Modulator Simulations

After emphasizing important parameters in the SM design and finishing design part, we present the simulation results of the SM with the 4.8 dB and 7.0 dB PAPR WCDMA signals. The simulations are intended to simulate the final test conditions precisely. This time, we give 7.0 dB PAPR case in detail.

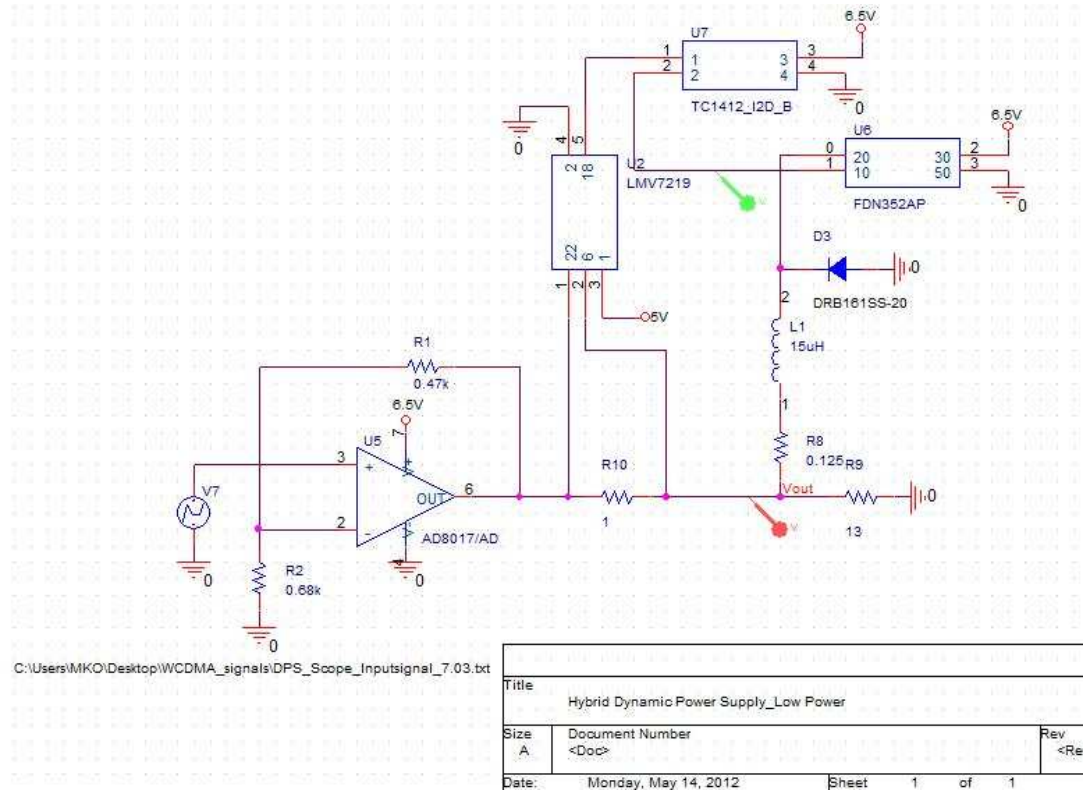


Figure 3.8: Low power HSA schematic-7.0 dB

In Fig. 3.8, you see the schematic of the DPS that belongs to the 7.0 dB PAPR case. In addition, the waveforms that belong to the simulation are given in Fig. 3.9. Some of the important simulation results are summarized in Table 3.5. Note that, although the switching stage has efficiency of 81.8%, the

hybrid configuration has efficiency of 80.4 %. The decrease in efficiency may sound as the wrong design logic. However, by preventing the switching stage to operate at higher switching frequencies, where the dynamic loss can become large, we actually gain in efficiency. Notice that, we have skipped comparator (LMV7219) to include in the efficiency calculations. The reason is that LMV7219 operates from 5.00V and draws current of at most 2.00 mA. It has no significant effect on the system efficiency.

Table 3.5: Simulated Efficiency Results of Supply Modulator

Efficiency(HSA)	$I_{Driver+Transistor}(mA)$	$I_{opamp}(mA)$	$V_{rms}(V)$	$P_{out}(W)$	$\eta_{PA}(\%)$
Low Power-4.8 dB	169	110.0	4.50	1.40	77.2
Low Power-7 dB	161	63.0	3.90	1.17	80.4
High Power-7 dB	747	175	8.10	8.98	81.1

Notice also from Fig. 3.9, when there is a fast change in the input voltage, high pulses are created at the input of P-MOS power transistor so that current is provided by the linear stage, in other words, by the opamp. After that, according to operation procedure explained in Chapter 2, low pulses are created so that current is provided by the switching stage, in other words, by the power transistor. Choosing different inductor and sense resistance values change how often high pulses are created.

3.3 The Inductor Selection

Remember that L value calculated from (2.15) is maximum inductance value to provide most of the current through switching stage when envelope signal is sinusoidal. Remember also that, we have used higher inductor value than inductance decided from this equation. Instead of providing most of the current from switching stage, linear stage is also used. While doing that, we have claimed efficiency being higher compared to other case and output is less distorted since opamp provides enough current at enough rate. Below you can find an analysis

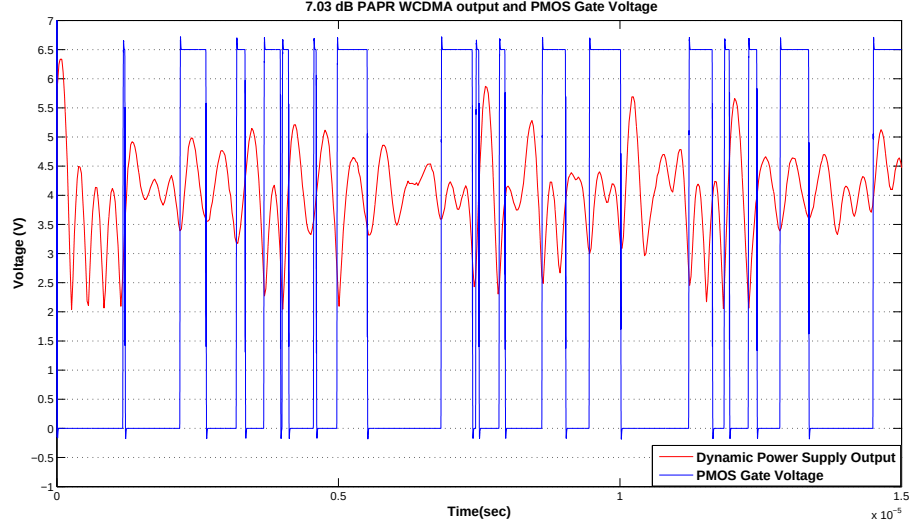


Figure 3.9: Low power HSA simulation results-7.0 dB

about this assumption. As we know, envelope bandwidth of WCDMA signal is 3.84 MHz. If we assume instead of a WCDMA signal, a sinusoidal envelope signal with frequency of 3.84 MHz is used, let me calculate maximum inductor value according to equation (2.15) for the low power case.

$$L \leq \frac{R_{load} \sqrt{V_{dd}^2 - V_o^2}}{2\pi f_s V_o} \leq \frac{13 \times \sqrt{6.5^2 - 3.9^2}}{2\pi \times 3.84 \times 10^6 \times 3.9} \leq 0.72 \times 10^{-6} H$$

The simulation result belongs to the SM with 0.68uH is given in Fig. 3.10. Compared to Fig. 3.9, number of high pulses at the transistor's gate is greater. This is mainly because of faster response time of switching stage to even tiny voltage variances in envelope signal due to low inductance value of the switching stage. When higher inductor value is used, the switching stage basically works as if current source. When small inductance is used, bandwidth requirement of linear stage also increases. Therefore, current drawn by opamp increases. Also note that, output signal is distorted due to high switching frequency and insufficient current support of switching stage. In Table 3.6, simulation results of

Table 3.6: Low Power, Low Inductor HSA simulation results

Dri.Curr.(mA)	Trans.Curr.(mA)	Op-amp Curr.(mA)	V_{rms} (V)	P_{out} (W)	η
10.2	210.0	108	3.90	1.17	54.8 %

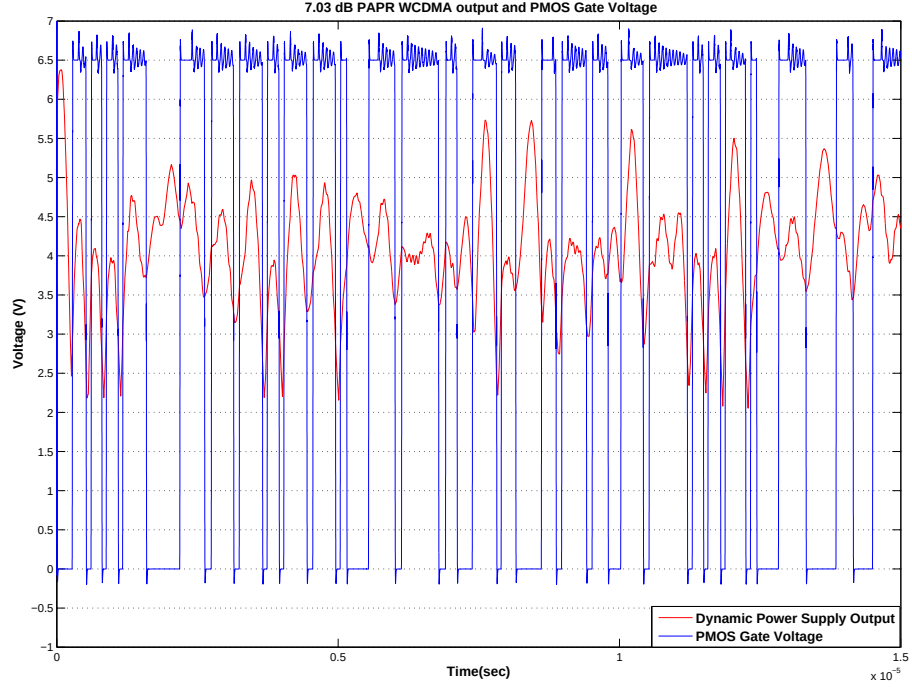


Figure 3.10: Low Power HSA Waveforms with 0.68uH-7.0 dB

schematic given in Fig. 3.8 by only changing inductor value from 15uH to 0.68uH is represented. Notice that, the efficiency has decreased from 81.8 % to 54.8 %.

Chapter 4

EXPERIMENTAL RESULTS

4.1 The PA Measurements

In Fig. 4.1, the P_{in} vs P_{out} graph of the low power PA, which has been designed to test the SM. We have performed compression point analysis to estimate the average output power when the PA is driven by WCDMA signal. Depending on the PAPR and statistics of WCDMA signal, the output power varies. A good estimate about the maximum average output power is “PAPR” dB back-off from the 1 dB compression point. Since only peak points of envelope is compressed 1 dB and probability of envelope signal to be at peak point is small compared to average power region, compression in output signal is limited. In measurements, we have observed that, even 2 dB upper deviation of the input signal power from the input P1dB point does not distort the output signal too much. At this point, one should check spectrum emission mask (SEM) of used signal’s standard. Spectrum emission must lie within the limits given in the standard.

As seen in Fig. 4.1, the 1 dB compression point of the low power PA is 31.4 dBm. The measurement result is the same as the simulation result. In the

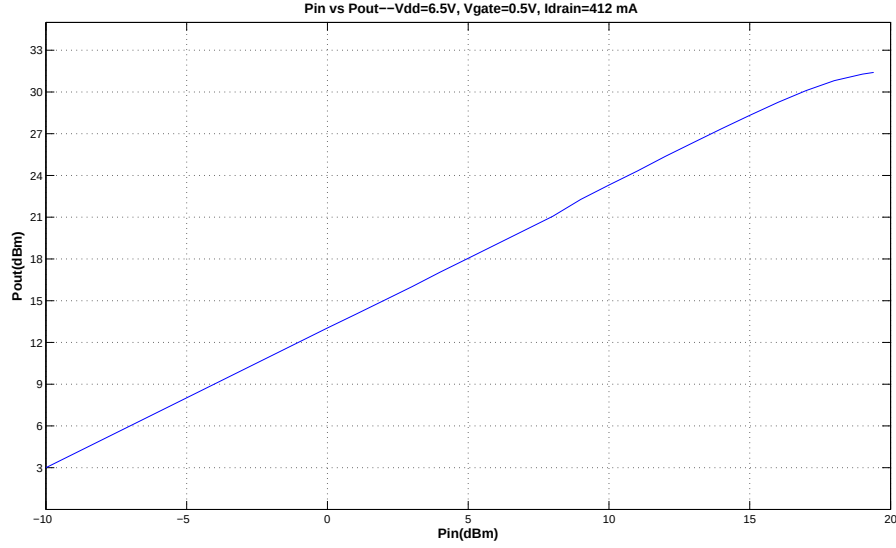


Figure 4.1: Measurement results of Pin vs Pout response of the designed PA

system measurements part, 4.8 dB and 7.0 dB lower deviations than the 1 dB compression point are expected as minimum output powers.

4.2 The Supply Modulator Measurements

In this part, the measurement results belong to the SM have been presented. In Fig. 4.2, you see the picture of designed SM. Each component are shown in circle and their names and function are represented in Table 4.1. Same input signals used in the simulations have been used in the measurements. The load connected to test the SM is the same as simulations. We have used 7.0 dB case to explain the results and analysis.

In Fig. 4.3, the output signal of the SM and drain signal of the transistor are shown. Note that, in simulations, we have plotted gate voltage of the transistor but in measurements drain voltages are represented. Compared to the simulation results given in Fig. 3.9, pulses are more often for the measurement results. In

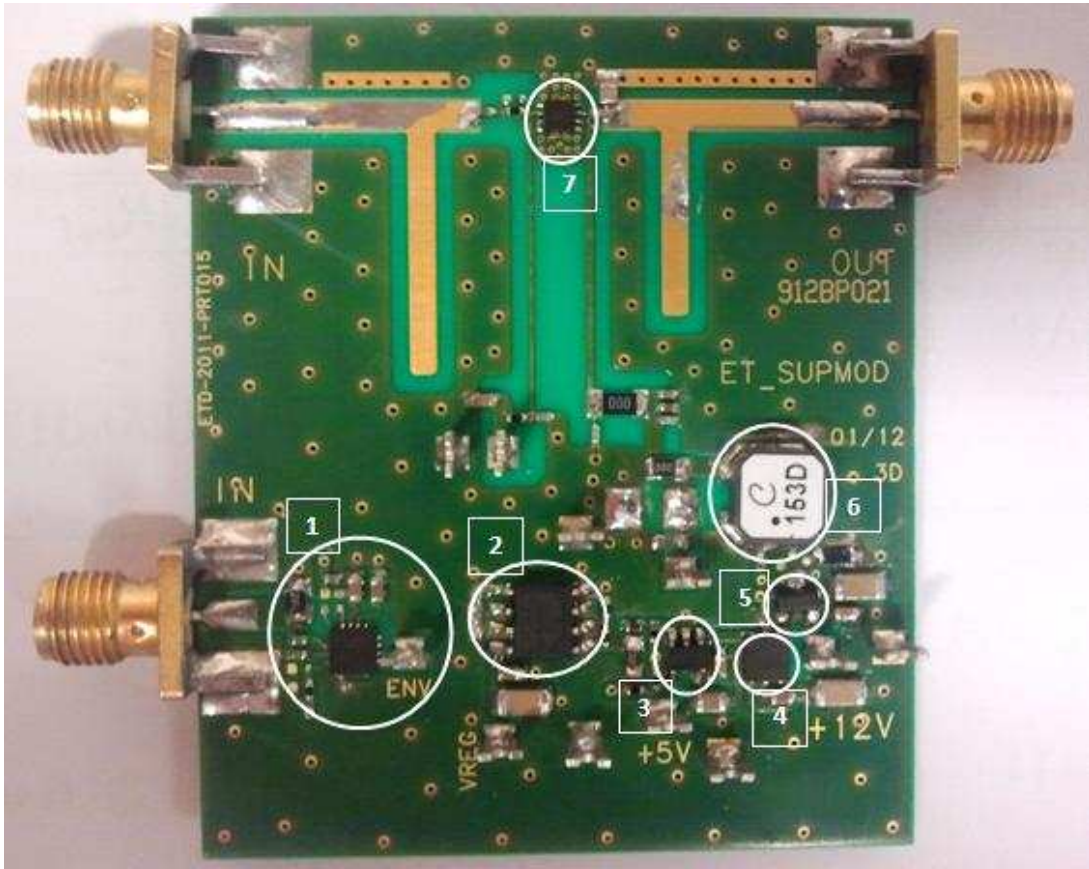


Figure 4.2: PCB Testing Board of Supply Modulator

the simulation part, modelling of LMV7219 comparator is important for pulse generation. Probably, the difference between simulation and measurement is due to modelling error of LMV7219. Resulting higher efficiency compared to simulation is normal because the high efficient switching stage supplies more current compared to simulation.

The measurement results are summarized in Table 4.2. As shown in Table 4.2, for the case of low power 7 dB, the efficiency is 80.0 %, which is highly close to simulation result of 81.8 %. Note that, although close output power and voltage are generated for two different PAPR cases, efficiency of low PAPR case is higher than high PAPR case. The main reason for that is 7.0 dB PAPR signal creates more often pulses and therefore linear part works more frequent to compensate created pulses. You can check this result by observing drawn currents by opamps

Table 4.1: Component Names and Their Function

Number	Component	Function
1	ADL5511	Envelope Detector
2	AD8017	Linear Stage Opamp
3	LMV7219	Comparator
4	LM5112SD	Mosfet Driver
5	FDN352AP	Power Transistor
6	LPS6235 – 153MLB	Power Inductor
7	ATF – 501P8	PA Transistor

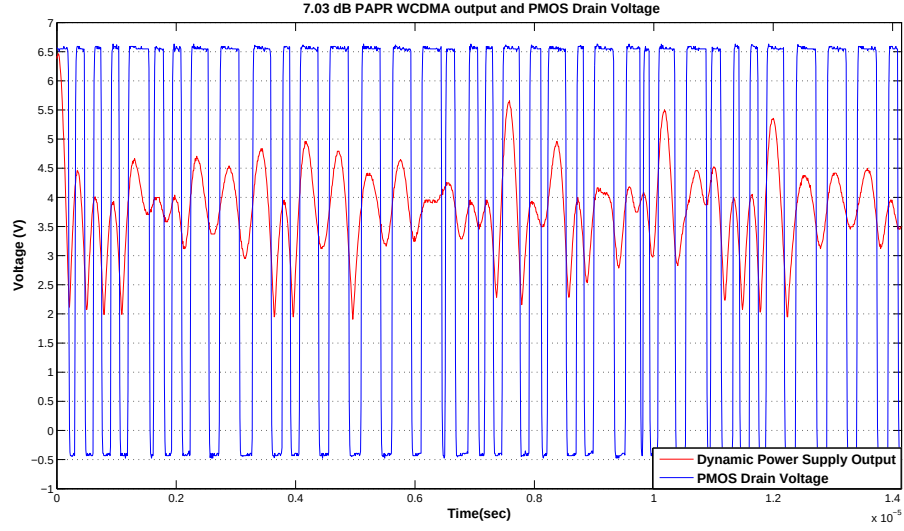


Figure 4.3: Supply Modulator Measurement Results-7.0 dB PAPR

for the two cases. However, although high PAPR SM has lower efficiency, the benefit of SM for high PAPR signals is greater because efficiency degradation occurs more for high PAPR signals compared to PAs operating with low PAPR signals.

4.3 The System Measurements

In this part, the SM and the PA are used to measure the system efficiency compared to constant supply case. Before giving system measurement results, I will try to setup a procedure that predicts system efficiencies in the light of the

Table 4.2: Measured Efficiency Results of Supply Modulator

Efficiency(HSA)	$I_{Driver+Transistor}(mA)$	$I_{opamp}(mA)$	$V_{rms}(V)$	$P_{out}(W)$	$\eta_{PA}(\%)$
Low Power-4.8 dB	177	50.00	4.46	1.33	90.1
Low Power-7 dB	172	33.0	3.85	1.07	80.0
High Power-7 dB	750.0	100.00	8.10	8.98	88.1

SM efficiency measurements and one key measurement. As a key measurement, I have measured the efficiency of the PA when its supply voltage is same as the output rms voltage that the SM planned to work. If we multiply the PA's efficiency with the SM's efficiency at same output voltage, we should reach the total system efficiency.

In other words, the system efficiency is given by,

$$\eta_{sys} = \eta_{supply} \times \eta_{PA} \quad (4.1)$$

Note that, η_{PA} is the efficiency of the PA at the close output power to the output power of the system and at the same rms output voltage as the rms output voltage of the SM. η_{supply} is the efficiency of the SM at the same output voltage and power. The above equation might be a good prediction about the system efficiency. Below you find this procedure has been applied to low power 4.8 dB case.

According to measurements, for the same average output power, the constant supply PA has drawn 320.0 mA from 6.50 V. However, the PA with dynamic power supply has drawn only 240.0 mA. 180.0 mA of the current drawn by the switching stage and driver circuitry, and 60.0 mA of the current drawn by the linear stage namely the opamp. In other words, the drain efficiency of the constant supply PA is 27.0 % but for the case of dynamic supply case it is 34.7 %. Let me try to predict the system efficiency using (4.1).

In Fig. 4.4, you see PA's efficiency at 4.50 V. According to this graph efficiency is % 37.6. Additionally, we have measured the efficiency of the supply modulator

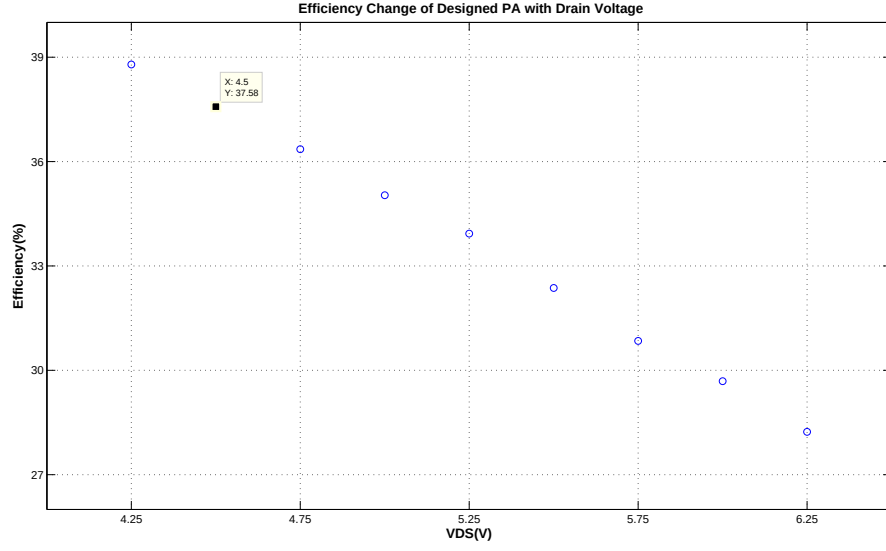


Figure 4.4: Efficiency Change of PA vs Drain Voltage–4.8 dB PAPR case

at 4.46 V as 90.5 %. So the system efficiency is given by

$$\eta_{sys} = \eta_{supply} \times \eta_{PA} = 0.901 \times 0.376 = 33.9\%,$$

which is a close result compared to 34.7 %.

As an efficiency improvement method, envelope tracking should not cause extra nonlinearity. We have compared spectra of two cases as a method of linearity comparison. In Fig. 4.5, you see the spectra of two cases of PA operating with constant PA and varying supply for the case of 4.8 dB PAPR. As you can see from graphs, efficiencies are compared almost at the same linearity points. The spectrum emissions are close to each other. Therefore, we have concluded that, for the 4.8 dB PAPR case, the dissipated power is decreased $6.50 \text{ V} \times 80.00 \text{ mA} = 520.0 \text{ mW}$. For a system of output power 0.560 W, this improvement is highly important. In Table 4.3, you see the measurement results of all cases. Estimating system efficiencies are skipped for the other cases. However, spectra of all cases are given below.

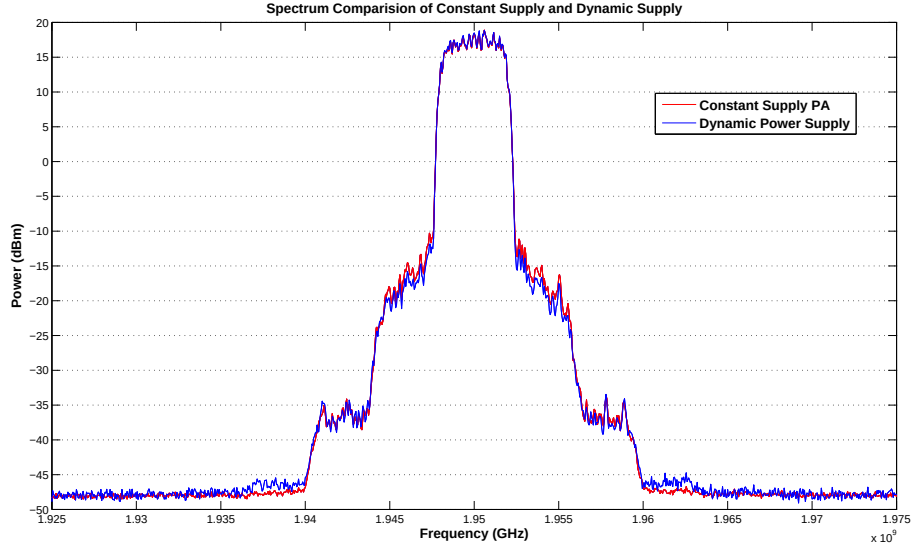


Figure 4.5: Spectra of Constant Supply and Dynamic Power Supply with 4.8 dB Signal

Table 4.3: Improvement introduced by DPS

Efficiency	Constant Supply		Dynamic Supply	
	$Current(mA)$	$\eta_{PA}(\%)$	$Current(mA)$	$\eta_{PA}(\%)$
Low Power-4.8 dB	320.0	27.0	240.0	34.7
Low Power-7 dB	320.0	21.5	210.0	31.7
High Power-7 dB	930.0	31.8	745	39.7

In Fig. 4.6, you see the spectrum comparison of low power 7 dB case. As you can see from figure, the efficiencies are compared at close linearity conditions. As a result, the dissipated power is decreased $6.50 V \times 110 mA = 715 mW$. For a system of output power 0.45 W, this improvement is important.

Finally, in Fig. 4.7, you can find the spectra of constant supply and supply modulator cases. As you can see from graphs, the efficiencies are compared at the same linearity points. The spectrum emissions are again close to each other. As a result, the dissipated power is decreased $12 V \times 185 mA = 2.22 W$. For a system of output power 3.50 W, this improvement is highly important.

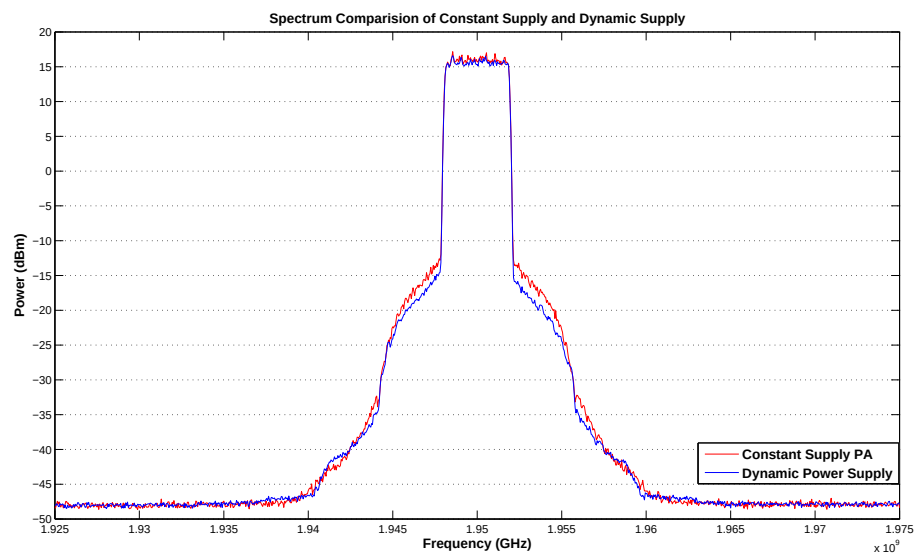


Figure 4.6: Spectra of Constant Supply and Dynamic Power Supply with 7.0 dB Signal

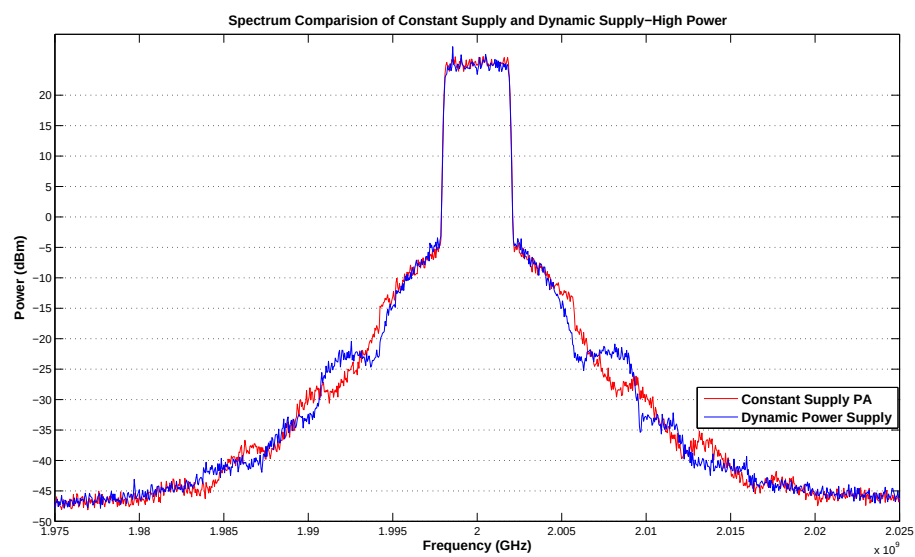


Figure 4.7: Spectra of Constant Supply and Dynamic Power Supply with 7.0 dB Signal

Chapter 5

CONCLUSIONS

In this work, we have designed a dynamic power supply for varying envelope signals with the aim of increasing the efficiency of linear PAs that degrades as a result of varying envelope signals. The proposed method uses lumped components, which are carefully chosen in terms of important parameters to maximize the system efficiency. Our supply is able to track WCDMA signal and slower varying signals.

In the thesis, we have emphasized the increasing importance of supply modulation for modern communication signals. Important parameters such as PAPR, IQ modulation, power back-off have been reviewed. A detailed literature survey is given and HSA using envelope tracking method has been tested in terms of performance.

As switching stage of HSA, a buck converter has been used. Static and dynamic loss mechanisms of buck converters are discussed and formulated in detail. The linear stage of HSA is discussed and important requirements that the linear stage must satisfy has been discussed. A combination of switching stage and linear stage is basically performed using the proper inductor value. We have showed that choosing low inductor values to support current needed by

PA only using switching stage decreases efficiency of system to too low values due to increased dynamic losses. Instead of that, we showed that choosing higher inductor value is a better choice in terms of efficiency. Additionally, operation logic of HSA and nonlinearity caused by supply modulation have been explained.

A low power PA is designed to test the performance of dynamic power supply using ADS. Both switching and linear stage simulations are performed using PSpice. The simulations are performed in order to test selected components and show the importance of parameters such as gate charge of power transistor, bandwidth and output current of linear stage opamp. In order to simulate system simulations better, WCDMA signal with two different PAPR values are recorded and used as test signal in PSpice simulations. In addition, to test the performance of HSA in high power case, a second amplifier is used. This test aimed to show how efficiency changes with drawn current and output voltage.

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