ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES

PhD THESIS

Ömer TÜRKSOY

DESIGN AND ANALYSIS OF HIGH EFFICIENT AC-DC POWER FACTOR CORRECTED CONVERTERS FOR ON-BOARD BATTERY CHARGING SYSTEM IN ELECTRIC VEHICLES

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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ABSTRACT

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On-board chargers (OBCs) in electric vehicles (EVs) must provide more power in a smaller volume to increase the volume allocated to the battery. Increasing the power density of the OBCs largely depends on the improvements to be made in the AC-DC Power Factor Corrected (PFC) converter, which is its most important part. The main purpose of this thesis is to increase the power density of AC-DC PFC converter. For this purpose, two different solutions are presented. In the first of these, a dynamic voltage compensator (DVC) has been proposed to reduce the amount of output voltage ripple of the interleaved PFC boost converter that affects the size and lifetime of the DC-link capacitor in OBCs. Along with the reduction of the amount of the voltage ripple, it is possible to use capacitor technologies with a smaller size and longer life. In this way, the designed OBC will have a high power density and long service life. In the second of the presented solutions, a new soft-switched AC-DC PFC boost converter is proposed to increase the power density. In the proposed converter, thanks to the developed active snubber cell (ASC), switching losses are eliminated by providing soft switching (SS) for all switching elements. In addition, the developed ASC did not cause any voltage and current stress on the circuit elements. These two proposed topologies are the best candidates for the AC-DC conversion part of OBCs due to their advantageous properties.

Key Words: AC-DC PFC Converter, DVC, Electric Vehicles, Soft Switching, On-Board Charger.

ÖZ

DOKTORA TEZİ

ELEKTRİKLİ ARAÇLARDA DÂHİLİ BATARYA ŞARJ SİSTEMİ İÇİN YÜKSEK VERİMLİ AA-DA GÜÇ FAKTÖRÜ DÜZELTİLMİŞ DÖNÜŞTÜRÜCÜLERİN TASARIMI VE ANALİZİ

Ömer TÜRKSOY

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Elektrikli araçlardaki dâhili şarj cihazları (DŞC'ler), bataryaya ayrılan hacmin arttırılması için daha küçük hacimde daha fazla güç sağlaması gerekmektedir. DŞC'lerin güç yoğunluğunun arttırılması büyük ölçüde en önemli kısmı olan AA-DA güç faktörü doğrultulmuş (GFD) dönüştürücüde yapılacak iyileştirmelere bağlıdır. Bu tezin temel amacı, AA-DA GFD dönüştürücünün güç yoğunluğunun arttırılmasını sağlamaktır. Bu amaçla, iki farklı çözüm sunulmuştur. Bunların ilkinde, DŞC'lerdeki DA-bağ kondansatörünün boyutunu ve ömrünü etkileyen, iç içe geçmiş GFD yükselten dönüştürücünün çıkış gerilimi dalgalanma miktarını azaltmak için bir dinamik gerilim kompanzatörü (DGK) önerilmiştir. Gerilim dalgalanma miktarının azaltılması ile birlikte, daha küçük boyutlu ve daha uzun ömürlü kondansatör teknolojilerinin kullanmasına olanak sağlanmaktadır. Bu sayede, tasarlanan DŞC yüksek güç yoğunluğu ve uzun kullanım ömrüne sahip olacaktır. Sunulan çözümlerin ikincisinde, güç yoğunluğunu artırmak için yeni bir yumuşak anahtarlamalı AA-DA GFD yükseltici dönüştürücü önerildi. Önerilen dönüştürücüde, geliştirilen aktif bastırma hücresi (ABH) sayesinde, tüm anahtarlama elemanları için yumuşak anahtarlama sağlanarak anahtarlama kayıpları elimine edilmiştir. Ayrıca, geliştirilen ABH, devre elemanları üzerinde herhangi bir gerilim ve akım stresi meydana getirmemiştir. Önerilen bu iki topoloji, avantajlı özellikleri nedeniyle DŞC'lerin AA-DA dönüşüm kısmı için en iyi adaylardır.

Anahtar Kelimeler: AA-DA GFD Dönüştürücü, DGK, Elektrikli Araçlar, Yumuşak Anahtarlama, Dâhili Şarj Cihazı.

EXTENDED SUMMARY

In recent years, due to the rapid depletion of oil resources, increasing CO_2 emissions, depletion of the ozone layer and the outbreak of the health problems in densely populated areas, clean and environmentally-friendly EVs are becoming the center of attention. EV technologies are attractive solutions to these problems, but the battery performance, which limits the vehicle range, remains the biggest obstacle for the mainstream adoption of EVs. Although only battery technology seems to affect battery performance, the way the battery is used and the quality of charging also greatly affect battery performance. Therefore, battery chargers play a critical role in the development of EV technology. In addition, during the charging of many electric vehicles at the same time, an overload will occur on the grid. Therefore, the performance of the battery charger is also essential to minimize stress on the grid and limit the input current harmonics to meet the international standards.

Battery chargers are designed in two forms such as on-board and off-board depending on their allocations. Off-board chargers are only found at stations such as fuel stations. Although these chargers provide fast charging opportunities, they cause overheating on the battery and the batteries to deteriorate more quickly due to the very high currents passing through the battery during the charging process. On the other hand, on-board chargers (OBCs) are located in the vehicles and provide charging from any electrical outlet in places such as home, office, hospital, shopping mall, alleviating consumer range concerns. OBCs, which prioritize battery health, come to the fore in this context.

OBCs are designed in two structures, as single-stage and two-stage. The single-stage OBCs consist of a diode bridge rectifier, along with an isolated DC-DC converter. The DC-DC converter stage controls both the implementation of the PFC and the regulation of the output voltage according to the battery voltage. Since there is no DC-Link capacitor in this structure as in the two-stage OBC structure,

there is no need to control the voltage of this capacitor. In addition, galvanic isolation is provided by a transformer in the DC-DC converter structure. A large amount of voltage ripple occurs at the output of the DC-DC converter in this topology. To reduce the amount of ripple and provide constant output power, the use of large internal capacitors is required. Although this topology provides high-efficiency results in low power applications, it is insufficient in high power applications due to the limited number of circuit elements. The two-stage OBC structure consists of an AC-DC PFC converter, an isolated DC-DC converter and a DC-link capacitor that provides the connection between these two parts. While the AC-DC PFC stage performs both the rectification of the AC grid voltage and the correction of the input power factor, the DC-DC converter stage regulates the output voltage and provides galvanic isolation to prevent battery damage in case of failure on the grid side. Since this structure includes DC-link control, it has a more complex controller than a single-stage structure and has a higher number of active circuit elements compared to a single-stage structure. However, this topology is a suitable candidate for OBCs as it provides flexible input and output voltage ranges and high-efficiency results in high power applications.

Since AC-DC PFC converters perform both rectification and PFC, they play a major role in improving the performance and power density of the onboard two-stage battery chargers. AC-DC PFC converters suffer from low power density and high output voltage ripple problems affecting the size and lifetime of the DC-link capacitor. By increasing the switching frequency, the circuit element sizes decrease and the power density of the converter increases. However, increasing the switching frequency causes an increase in switching losses. SS techniques have been proposed in the literature to solve this problem. Although some of the proposed soft-switching techniques provide high-efficiency results, they have high-cost design. Methods realized with low-cost designs are also inadequate to reduce switching losses. In some of the methods, extra current and voltage stresses occur on the circuit elements.

On the other hand, some of the methods developed to reduce the output voltage ripple are carried out by controller design, while others are performed by using an extra circuit. A complex controller structure is required in the studies performed with the controller design. In some of the methods performed with the additional circuit, the circuit elements were exposed to high voltage because they were connected parallel to the load and efficient results could not be obtained. In other methods, the circuit elements are connected in series to the load and they are not exposed to high voltage, but the amount of the voltage ripple has not been completely reduced.

In this thesis, two different designs are presented to solve the problems mentioned hereinabove. In the first of the designs, a DVC is proposed to reduce the amount of output voltage ripple of the interleaved PFC boost converter. The proposed DVC aims to reduce the voltage ripple on the DC-link capacitor by creating a reverse voltage as much as the amount of voltage ripple on the capacitor. The performance results of the converter are obtained for variable input voltage and six different load cases specified in European efficiency standards and compared with the traditional circuit (without DVC). It has been observed that with the designed DVC, the amount of output voltage ripple of the converter is substantially reduced under all load conditions. In addition, the designed DVC has made improvements to the input characteristic of the converter. The input power factor has been approximated to the unity power factor, and the input current total harmonic distortion is also greatly reduced. With the designed DVC, higher efficiency results are achieved compared to the traditional circuit (without DVC).

In the second of the designs, a new soft-switched AC-DC PFC boost converter is proposed to increase the power density. Thanks to developed active snubber cell (ASC), the main switch of the proposed converter turns on under zero voltage transition (ZVT) condition and turns off under zero current transition (ZCT) condition. Thus, switching losses of the main switch are eliminated. The ASC switch of the proposed converter turns on under zero current switching (ZCS)

condition and turns off under ZCT condition. The diode of the converter turns on under zero voltage switching (ZVS) condition and turns off under ZCT condition. Also, the diodes of the ASC circuit turn on under ZCS condition and turn off under ZVS condition. Although a small amount of conduction losses occurs with the additional ASC circuit, the converter's switching losses are eliminated, and the converter performance has been improved. Furthermore, the developed ASC has a low-cost design unlike the existing ASCs, as well as did not cause any additional current and voltage on the circuit elements. The performance results of the proposed converter are obtained for different cases studies and compared with the hard-switching counterpart. SS conditions and unity power factor are achieved for all load conditions. In addition, the input current THD values comply with the range given in IEC 61000-3-2 standards and are less than the hard-switched counterpart.

The two designed converter topologies can be good candidates for the AC-DC converter parts of the two-stage OBCs since they have high power density and high efficiency.

GENİŞLETİLMİŞ ÖZET

Son yıllarda petrol kaynaklarının hızla tükenmesi, artan CO_2 emisyonları, ozon tabakasının incelmesi ve yoğun nüfuslu bölgelerde sağlık sorunlarının ortaya çıkması nedeniyle temiz ve çevre dostu EV'ler ilgi odağı haline gelmektedir. EV teknolojileri, bu sorunlara çözüm üretmesi açısından çekici çözümlerdir, ancak araç menzilini sınırlayan pil performansı, EV'lerin yaygın olarak benimsenmesinin önündeki en büyük engel olmaya devam etmektedir. Yalnızca pil teknolojisi pil performansını etkiler gibi görünse de, pilin kullanım şekli ve şarj kalitesi de pil performansını büyük ölçüde etkilemektedir. Bu yüzden, batarya şarj cihazları EV teknolojisinin gelişiminde kritik bir rol almaktadır. Ayrıca, EV sayısındaki artış, şarj işlemi sırasında şebeke üzerinde strese neden olacaktır. Bu nedenle, şarj cihazının performansı, şebeke üzerindeki baskıyı en aza indirmek ve giriş akımı harmoniklerini uluslararası standartları karşılayacak şekilde sınırlamak için de gereklidir.

Batarya şarj cihazları, yerleşim yerlerine bağlı olarak dâhili ve harici olmak üzere iki şekilde tasarlanmaktadır. Harici şarj cihazları, yalnızca akaryakıt istasyonları gibi istasyonlarda bulunmaktadır. Bu şarj cihazları, hızlı şarj olanağı sağlamalarına rağmen, şarj işlemi sırasında batarya üzerinden çok yüksek akımlar geçtiğinden dolayı, batarya üzerinde ısınmalara ve bataryaların daha çabuk bozulmalarına sebep olmaktadır. Dâhili şarj cihazları (DŞC'ler) ise araçların içinde yer almaktadır ve ev, ofis, hastane, alışveriş merkezi gibi yerlerde her türlü elektrik prizinden şarj sağlayarak tüketici menzil endişelerini hafifletmektedir. Pil sağlığını ön planda tutan DŞC'ler bu bağlamda ön plana çıkmaktadır.

DŞC'ler, tek aşamalı ve iki aşamalı olarak iki yapıda tasarlanmaktadır. Tek aşamalı DŞC'ler, bir diyot köprü doğrultucu ve izole edilmiş bir DA-DA dönüştürücüden oluşur. DC-DC dönüştürücü aşaması, hem GFD'nin uygulanmasını hem de çıkış voltajının batarya gerilimine göre düzenlenmesini kontrol eder. Bu yapıda, iki aşamalı DŞC yapısındaki gibi bir DA bağ

kondansatörü bulunmadığından bu kondansatörün geriliminin kontrolüne de ihtiyaç duyulmamaktadır. Ayrıca, DA-DA dönüştürücü yapısındaki bir trafo ile galvanik yalıtım sağlanmaktadır. Bu topolojide DA-DA dönüştürücünün çıkışında büyük miktarda voltaj dalgalanması meydana gelir. Bu dalgalanma miktarını azaltmak ve sabit çıkış gücü sağlamak için dâhili büyük kondansatör kullanımına ihtiyaç duyulmaktadır. Bu topoloji, düşük güçlü uygulamalarda yüksek verimli sonuçlar sağlasa da, devre elemanlarının sınırlı sayıda olması nedeniyle yüksek güçlü uygulamalarda yetersiz kalmaktadır. İki aşamalı DŞC yapısı, bir AA-DA GFD dönüştürücü, bir yalıtımlı DA-DA dönüştürücünden ve bu iki kısım arasındaki bağlantıyı sağlan bir DA-bağ kondansatöründen oluşmaktadır. AA-DA GFD aşaması hem AA şebeke voltajının doğrultulmasını hem de giriş güç faktörünün düzeltilmesi işlemini gerçekleştirirken, DA-DA dönüştürücü aşaması çıkış voltajını düzenlemekte ve şebeke tarafında meydana gelebilecek arıza durumunda batarya hasarını önlemek için galvanik yalıtım sağlamaktadır. Bu yapı DA-bara kontrolü içerdiğinden dolayı tek aşamalı yapıdan daha karmaşık bir denetleyiciye sahiptir ve tek aşamalı yapıya kıyasla daha fazla aktif devre elemanı sayısına sahiptir. Fakat bu topoloji esnek giriş ve çıkış gerilim aralıkları ve yüksek güçlü uygulamalarda yüksek verimli sonuçlar sağladığı için DŞC'ler için uygun bir adaydır.

AA-DA GFD dönüştürücüler hem doğrultma hem de GFD'yi gerçekleştirdiğinden iki aşamalı dâhili batarya şarj cihazlarının performansının ve güç yoğunluğunun iyileştirilmesinde büyük role sahiptir. AA-DA dönüştürücüler düşük güç yoğunluğu ve DA-bağ kondansatörünün boyutunu ve ömrünü etkileyen yüksek çıkış gerilim dalgalanması sorunlarından muzdariptir. Anahtarlama frekansının arttırılmasıyla devre eleman boyutları azalmakta ve dönüştürücünün güç yoğunluğu artmaktadır. Fakat anahtarlama frekansının artması anahtarlama kayıplarının artmasına sebep olmaktadır. Bu sorunun çözümü için literatürde yumuşak anahtarlama teknikleri önerilmiştir. Önerilen yumuşak anahtarlama tekniklerin bir kısmında yüksek verimli sonuçlar sunulmasına rağmen da yüksek maaliyetli tasarıma sahiptirler. Düşük maaliyetli tasarımlar ile gerçekleştirilen

yöntemler de anahtarlama kayıplarını azaltmada yetersiz kalmaktadır. Yöntemlerin bir kısmında ise devre elemanları üzerinde ekstra akım ve gerilim stresleri meydana gelmektedir.

Diğer bir yandan, çıkış gerilim dalgalanmasının azaltılması için geliştirilen yöntemlerin bir kısmı kontrolcü tasarımı ile gerçekleştirilirken diğer bir kısmı ise ekstra devre kullanılarak gerçekleştirilmektedir. Kontrolcü tasarımı ile gerçekleştirilen çalışmalarda karmaşık bir kontrolcü yapısı gerekmektedir. Ek devre ile gerçekleştirilen yöntemlerin bir kısmında devre elemanları yüke paralel olarak bağlandığından dolayı yüksek gerilime maruz kalmışlardır ve verimli sonuçlar elde edilememiştir. Diğer yöntemlerde ise, devre elemanları yüke seri bağlanmıştır ve yüksek gerilime maruz kalmamışlardır fakat dalgalanma miktarı tam olarak azaltılamamıştır.

Bu tez çalışmasında, yukarıda belirtilen sorunların çözümü için iki ayrı tasarım sunulmuştur. Tasarımların birincisinde, iç içe geçmiş GFD yükselten dönüştürücünün çıkış gerilim dalgalanma miktarını azaltmak için bir DGK önerilmektedir. Önerilen DGK, kondansatör üzerindeki gerilim dalgalanması miktarı kadar bir ters gerilim oluşturarak DA-bağ kondansatörü üzerindeki gerilim dalgalanmasını azaltmayı amaçlamaktadır. Dönüştürücünün performans sonuçları, değişken giriş gerilimi ve Avrupa verimliliği standartlarındaki altı farklı yük durumu için alınarak geleneksel (DGK olmayan) devre ile karşılaştırılmıştır. Tasarlanan DGK ile dönüştürücü çıkış gerilimi dalgalanma miktarının bütün yük durumlarında büyük oranda azaltıldığı gözlemlenmiştir. Ayrıca, tasarlanan DGK, dönüştürücünün giriş karakteristiği üzerinde de gelişimler sağlamıştır. Giriş güç faktörü birlik güç faktörüne yaklaştırılmış olup, giriş akım toplam harmonik bozulması da büyük ölçüde azaltılmıştır. Tasarlanan DGK ile geleneksel (DGK olmayan) devreye göre daha yüksek verimli sonuçlar elde edilmiştir.

Tasarımların ikincisinde, güç yoğunluğunu artırmak için yeni bir yumuşak anahtarlamalı AA-DA GFD yükseltici dönüştürücü önerilmiştir. Geliştirilen ABH sayesinde önerilen dönüştürücünün anahtarı, sıfır gerilimde geçiş (SGG) koşulu

altında açılır ve sıfır akımda geçiş (SAG) koşulu altında kapatılır. Böylelikle dönüştürücü anahtarının anahtarlama kayıpları ortadan kaldırılır. Önerilen dönüştürücünün ABH anahtarı sıfır akımda anahtarlama (SAA) koşulu altında açılır ve SAG koşulları altında koşulu altında kapanır. Ana devre diyotu sıfır gerilimde anahtarlama (SGA) koşulu altında açılır ve SAG koşulu altında kapatılır. Ayrıca, ABH devresin diyotları SAA koşulu altında açılır ve SGA koşulu altında kapatılır. Ek ABH devresi ile az miktarda iletim kaybı meydana gelmesine rağmen, dönüştürücünün anahtarlama kayıpları büyük ölçüde ortadan kaldırılır ve dönüştürücü performansı büyük ölçüde iyileştirilir. Ayrıca, geliştirilen ABH, mevcut ABH'lerden farklı olarak düşük maliyetli bir tasarıma sahiptir ve devre elemanları üzerinde herhangi bir ilave akım ve gerilime sebep olmaz. Önerilen dönüştürücünün performans sonuçları, farklı durum çalışmaları için alınmış ve sert anahtarlamalı karşılığı ile karşılaştırılmıştır. Bütün yük koşulları için yumuşak anahtarlama koşulları ve birim güç faktörü elde edilir. Ayrıca giriş akımı toplam harmonik bozulma değerleri IEC 61000-3-2 standartlarında verilen aralığa uygundur ve sabit anahtarlamalı muadilinden daha düşüktür.

Tasarlanan iki dönüştürücü topolojisi de yüksek güç yoğunluğu ve yüksek verime sahip olduklarından dolayı iki aşamalı DŞC'lerin AA-DA dönüştürücü kısımları için en iyi birer aday olabilirler.

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LIST OF ABBREVIATIONS

A	: Amperes
AC	: Alternating Current
ACM	: Average Current Mode
ASC	: Active Snubber Cell
BCM	: Borderline Current Mode
BLIL	: Bridgeless Interleaved
CCM	: Continuous Conduction Mode
CrM	: Critical Conduction Mode
DC	: Direct Current
DCM	: Discontinuous Conduction Mode
DVC	: Dynamic Voltage Compensator
EV	: Electric Vehicle
EMI	: Electromagnetic Interference
G2V	: Grid to Vehicle
HCM	: Hysteresis Current Mode
ICL	: Inrush Current Limiter
N/A	: Not Available
OBC	: On-Board Charger
OCCM	: One Cycle Current Mode
PCM	: Peak Current Mode
PFC	: Power Factor Correction
PLL	: Phase-Locked Loop
RFI	: Radio Frequency Interference
PHEV	: Plug-in Hybrid Electric Vehicle
RMS	: Root Mean Square
SS	: Soft Switching
THD	: Total Harmonic Distortion

TPBL : Totem-Pole Bridgeless

V : Voltage

V2G : Vehicle to Grid

ZCS : Zero Current Switching

ZCT : Zero Current Transition

ZVS : Zero Voltage Switching

ZVS : Zero Voltage Transition

1. INTRODUCTION

In this chapter, the research methodology of the thesis is given. Firstly, the importance of OBCs for the development and adoption of EVs. The structure of the OBCs is presented and expressed in detail. Secondly, detailed information is given about the main tasks of AC-DC PFC converters, which is the most important stage of the OBCs. Further, power quality requirements defined in international standards, which must be complied with during the withdrawal of current from the grid, are presented and some important definitions are provided. At the end of this chapter, the research objectives, the contribution of the thesis and the organization of the thesis are given.

1.1. Background and Motivation

In recent years, the automotive industry has been facing unprecedented changes due to concerns, such as rapid depletion of oil resources, increasing CO_2 emissions, depletion of the ozone layer, and the outbreak of the health problems in densely populated areas (Ahmadi, 2019; Held and Schücking, 2019; Mi and Masrur, 2017). Governments and industries have invested heavily in electric vehicle (EV) and plug-in hybrid electric vehicle (PHEV) technologies that resolve these concerns (Wei et al., 2020; Khaligh and D'Antonio, 2019). With these investments, EV and PHEV technologies are developing year-over-year, and are gaining increasing interest among consumers as seen from Figure 1.1 (IEA, 2020).

EV and PHEV technologies are attractive solutions in that they are environmentally friendly, but battery performances that limit vehicle range are still the biggest barrier for mainstream adoption. Although only battery technology appears to affect battery performance, how to use and charge the battery also greatly affects battery performance. Moving from this standpoint, the efficiency of the battery charger has vital importance on battery performance. On the other hand, the increase in the number of EVs and PHEVs will lead to stress on the grid during

the charging process. Therefore, the efficiency of the charger is also essential to minimize load stress on the grid and limit the input current harmonics to meet the international standards.

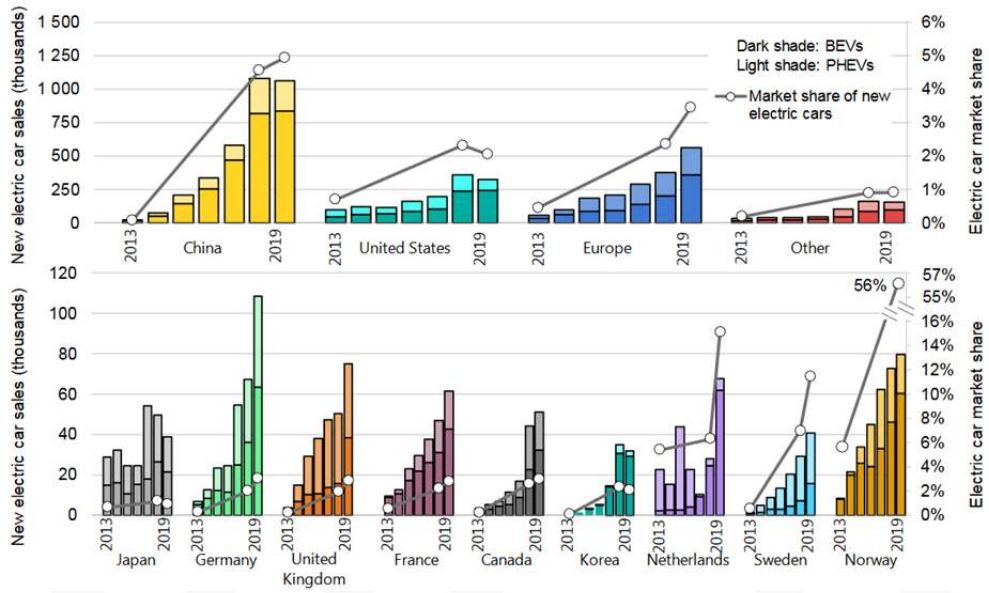

Figure 1.1. Annual sales and market share of EVs in worldwide for 2013-2019 (IEA, 2020)

Battery chargers are available in two different type such as AC charging and DC charging. In addition, AC and DC chargers are divided into three different categories according to their power levels as level 1, level 2 and level 3 as given in Table 1.1 (Kongjeen and Bhumkittipich, 2018). AC chargers offer slow charging, resulting in longer charging times. AC chargers used in both private and public areas. Today, many researchers are concentrating on AC chargers. DC chargers are usually offered at charging stations for commercial purposes because it requires installation costs, infrastructure costs and maintenance cost. DC Level 3 chargers offer fast charging facilities (Yilmaz and Krein, 2013; Xu et al., 2020).

Table 1.1. Charging power levels of the battery chargers

Power Level		Grid connection	Grid Voltage (V)	Current (A)	Charging type
AC	Level 1	1 phase	120	12-16	Slow
	Level 2	1 phase	240	<80	Slow
	Level 3	1, 3 phase	240	>80	Slow
DC	Level 1	-	200-450	80	Slow
	Level 2	-	200-450	200	Medium
	Level 3	-	200-600	400	Fast

Battery chargers can be designed in two forms such as on-board and off-board depending on their allocation with unidirectional and bidirectional power flow options. Unidirectional charger, enabling only energy transfer from network to the vehicle; is an attractive solution with low hardware requirements, easy connectivity and a tendency to reduce battery degradation. The bidirectional battery charger is a solution that enables energy transfer from the grid to the vehicle (G2V) and from the vehicle to the grid (V2G), where battery health is in the background and network security is at the forefront. Bidirectional chargers are not widely preferred because they cause the battery degradation problems. Off-board chargers are located in stations where it is difficult to access such as oil stations despite providing fast charging. On the other hand, on-board chargers (OBCs) are designed built into the vehicle. OBCs alleviate the consumer's range concerns by providing charging from any electrical outlet in places where there is no fast charging station such as home, office, hospital, mall, etc. The comparison of the features of the on-board and off-board chargers are provided in the below table.

Table 1.2. The comparison of the on-board vs. off-board chargers

On-Board	Off-Board
Low power range	High power range
Basic BMS	Complicated BMS
No battery heating problem	Battery heating problem
Add weight to the vehicle	Remove weight from the vehicle
Level 1 and Level 2 charging level	Level 3 charging level

Off-board chargers are an attractive solution from the standpoint of charging time; however, they adversely affect the battery health as they pass high current rates over the battery while charging process. OBCs, which prioritize battery health, come to the fore in this context. The schematic representation of the on-board battery charger on the EV powertrain is given in Figure 1.2.

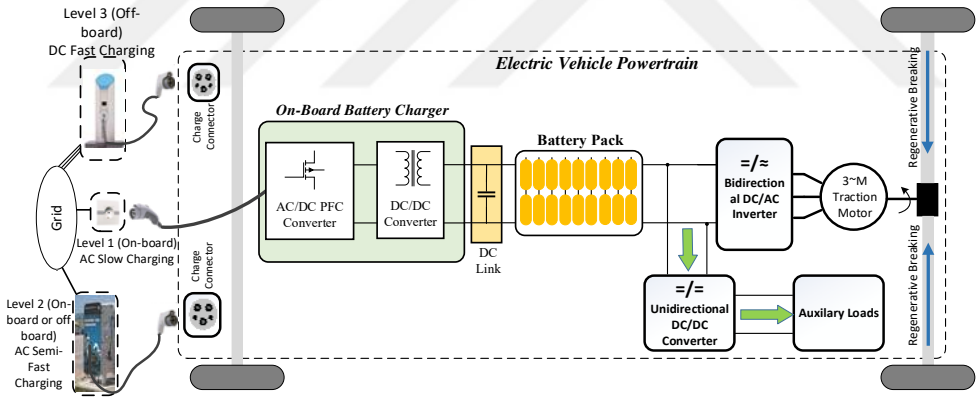

Figure 1.2. The schematic representation of the OBC on the EV powertrain

OBCs are categorized into two main categories such as single-stage and two-stage structure according to their power conversion characteristics. The simple block diagram of the single-stage OBC structure is illustrated in Figure 1.3. Single-stage OBC consists of a diode bridge rectifier and an isolated DC-DC converter. The isolated DC-DC converter stage both controls the implementation of the unity

power factor and regulation of the output voltage. In this structure, there is no need for voltage control of the DC-Link capacitor, which provides the interconnection of the AC-DC and DC-DC converter in the two-stage OBC structure. Also, galvanic isolation is provided with an isolation transformer in its structure. This topology uses the internal bulky capacitor to provide constant output power. This topology provides high efficiency in low power applications, but it is insufficient in high power applications due to the limited number of components.

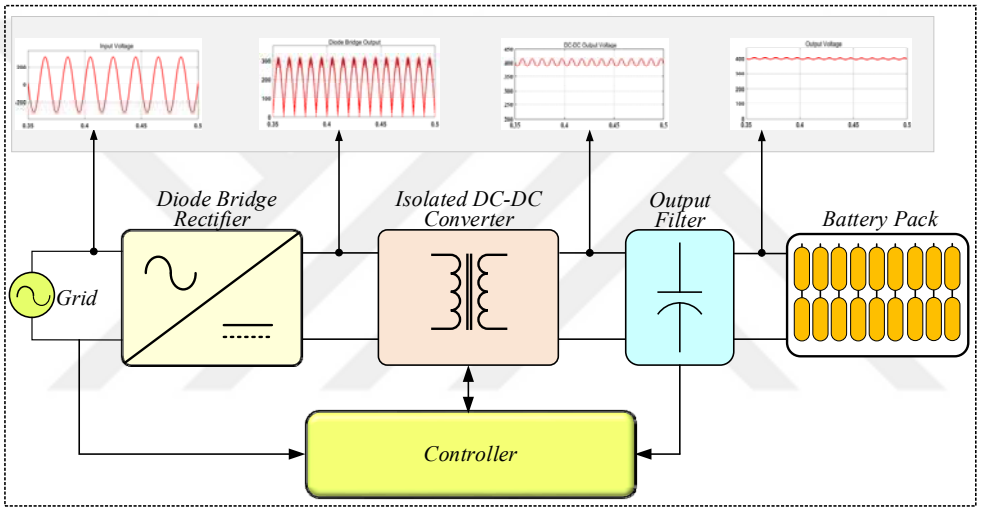

Figure 1.3. Simple block diagram of the single-stage OBC structure

The simple block diagram of the two-stage OBC structure is illustrated in Figure 1.4. The two-stage OBC structure consists of an AC-DC PFC converter and a DC-DC converter with a high-frequency isolation transformer. The AC-DC PFC stage provides both the rectification of the AC grid voltage and implementation of the unity power condition, whereas the DC-DC converter stage is used to regulate the output voltage and provide galvanic isolation to prevent battery damage in the event of a fault on the side of the grid. The controller of this structure is more complicated than the single-stage structure because it contains DC-link control and the number of switches is higher. But, this topology is a proper candidate for OBCs

as it provides flexible input and output voltage ranges and high efficiency at high power levels.

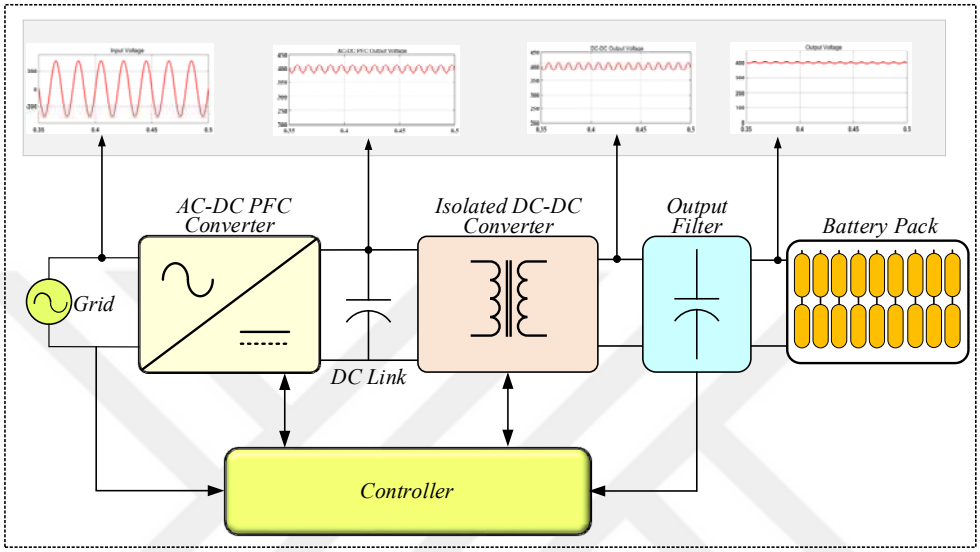

Figure 1.4. Simple block diagram of the two-stage OBC structure

As mentioned above, the first major task of the AC-DC PFC converter is to provide a unity power factor (PF). The PF is defined as the ratio of the active power to apparent power (S) which is the summation of the active and reactive power. Apparent power is calculated by multiplying the root mean square (rms) value of the current drawn from the grid and the rms value of the grid voltage as given in Eq. 1.1.

$$S = V_{rms} I_{rms} \tag{1.1}$$

Active power represents the actual amount of power delivered to the load. It is also known as usable energy quantity. Apparent power drawn from a grid equals active power and reactive power equals to zero if the load is purely resistive. In addition, if active power and apparent power are not equal, reactive power is

consumed by inductive and capacitive elements. In such a case, it means that not all the drawn power is transferred to the load. From an ideal power conversion equipment, it is expected that all the power drawn from the grid will transfer to the load. This is only possible if the current drawn from the grid and the voltage are in the same phase. When the phase difference occurs between them, some of the incoming energy drawn from the grid is consumed reactively and is lost. The PF usually ranges from 0 to 1 and is expected to be close to 1. PFC is provided by bringing the current and voltage to the same phase as shown in Figure 1.5.

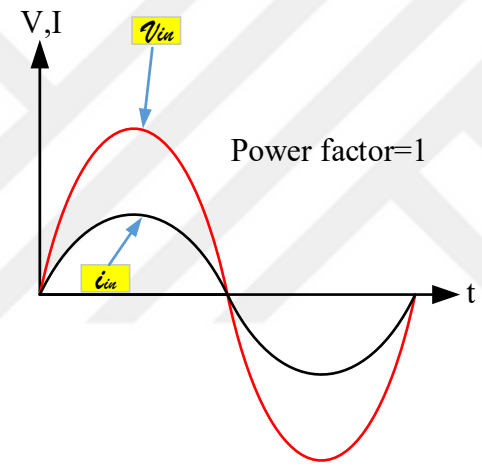

Figure 1.5. The representation of the unity power factor condition

The second major task of the AC-DC PFC converter is to achieve the minimum total harmonic distortion to meet the international standards. During AC-DC conversion, harmonic distortions occur in the current and voltage drawn from the grid due to load and converter. These distortions cause power losses and also create extra stress on the circuit elements. On the other hand, these harmonics have disruptive effects on the grid. Some international standards such as IEC61000-3-2 have been prepared to control these distortions. In its simplest definition, total harmonic distortion (THD) is known as the ratio of the rms values of the non-

fundamental component of the signal to the rms value of the fundamental component. The THD value of any signal can be calculated with the following equation:

$$THD_S = \frac{\sqrt{\sum_{n=2}^{\infty} S_{n,rms}^2}}{S_{1,rms}} \text{ , S: Voltage or current} \quad (1.2)$$

THD value may vary depending on the load and the performance of the converter. However, these values are expected not to exceed the permissible limits specified in the standards for grid security. The permissible current harmonics limits according to the IEC61000-3-2 standards are given in Table 1.3.

Table 1.3. Current harmonics limits according to the IEC61000-3-2 (Class D) standards

Individual odd Harmonic order h	Maximum permissible Harmonic Current per watt (mA/W)	Maximum permissible harmonic current (A)
3	3.4	2.3
5	1.9	1.14
7	1.0	0.77
9	0.5	0.4
11	0.35	0.33
13	0.3	0.21
15≤n≤39 Odd harmonics only	3.85/n	0.15*15/n

Due to the above-mentioned features, the improvement of the AC-DC PFC converters largely affects the performance and the size of two-stage OBCs. For the development of AC-DC PFC converters, challenges such as low conversion efficiency, high output ripple and low power density need to be examined in detail. In order to overcome these shortcomings, many studies have been conducted in the

literature. For improving the efficiency of the converter, studies mainly focused on the topological changes. Numerous circuit topologies are developed to increase efficiency by eliminating the deficiencies of the existed topologies (Jia et al., 2020; Lee and Kim, 2019; Wu et al., 2018; Wu et al., 2017; Alam et al., 2017a; Tang et al., 2015; Alam et al., 2014; Athab et al., 2014; Das et al., 2013; Musavi et al., 2011a, 2011b; Athab and Lu, 2010; Jang and Jovanovic, 2007). The low power density problem can be solved by increasing the switching frequency. As the switching frequency increases, the inductor and capacitor sizes used in the circuit decreased, thus high power density is achieved. However, high operating frequency causes increased switching losses and thus low conversion efficiency. To solve this problem, various soft-switching converters are presented to mitigating the switching losses (Jeong et al., 2020; Valipour et al., 2020a; Cetin and Yenil, 2019; Korada and Ayyanar, 2019; Park et al., 2019; Ting et al., 2019; Yu et al., 2019; Zhen and Qingyun, 2019; Cetin, 2018; Alam et al., 2017b; Du and Bhat, 2016; Lim et al., 2016; Pahlevaninezhad et al., 2012c; Akın and Bodur, 2011; Liu and Chang, 2009; Jang and Jovanovic, 2008; Tsai et al., 2007; Kang et al., 2002). High output ripple causes battery degradation and to mitigate this effect it is required the use of high-value DC-link capacitor. The reduction of the output ripple makes it possible to decrease the size of the DC-link capacitor used. The decreased size of this capacitor allows the usage of the long-life film-capacitors. On the other hand, as the size decreases, space is opened on the vehicle and this space will be used to increase the battery capacity and the range of the vehicle will be extended. From the standpoint of the reduction of the output ripple, many techniques are proposed to compensate the output ripple by an additional circuit (Pan and Zhang, 2015; Wang et al., 2014; Ohnuma and Itoh, 2014; Wang et al., 2011; Li et al., 2011; Shimizu et al., 2000). In addition, many control structures have been presented to enhance the dynamic performance of the converter and reduce controller complexity (Lee et al., 2020; Zhang et al., 2019; Mallik et al., 2018; Badawy et al., 2016; Cao et al., 2016; Chen et al., 2016; Hwu et al., 2015; Park and Park, 2015;

Pahlevani et al., 2014; Musavi et al., 2013a, 2013b; Pahlevaninezhad et al., 2012a, 2012b; El Aroudi and Orabi, 2010).

1.2. Research Objectives

Limited conversion efficiency, high output ripple and low power density are still the issues that need to be resolved for AC-DC PFC converters in OBCs. Therefore, the design of high efficient AC-DC PFC converter topology is needed for the development of the OBCs. In addition to a high-efficiency design, the converter to be designed must be minimal in size and cost when meeting the above-mentioned challenges and must meet the conditions specified in the standards. The high efficiency will reduce the stress on the grid and charging cost, the smaller the charger size will free up space on the vehicle to increase the battery capacity and the vehicle range will be increased by using a higher capacity battery.

The objectives of the presented research have been prepared to overcome the shortcomings mentioned above.

The objectives of the thesis are given as follows:

- AC/DC PFC circuit topologies and their control structures will be examined profoundly and the best proper topology for two-stage OBC will be proposed for wide input and output operation conditions.
- The control structure of the AC-DC PFC converters will be investigated and it is planned to develop a digital control method to reduce the rate of injected harmonics and generated reactive power.
- It is aimed to design a DVC in order to decrease the output ripple of the AC-DC PFC converter. The reduction of the output ripple will allow the use of a smaller sized capacitor, and the volume and weight of the OBC charger will be reduced.
- It is aimed to validate the performances of the DVC and its controller

under different load conditions specified in European efficiency standards.

- It is planned to develop a high-frequency AC-DC PFC converter to reduce the size of the OBCs.
- It is aimed to analyze in detail the traditional soft-switching methods developed to increase the power density of the AC-DC PFC converter.
- A new soft switched AC-DC PFC converter based on active snubber cell (ASC) will be proposed for increasing efficiency by eliminating the switching losses hence achieving the high power density.
- It is aimed to provide a detailed loss analysis to verify the efficiency increase of the proposed soft-switching AC-DC PFC converter.
- A comprehensive comparison between the proposed and existing soft-switching converters in terms of efficiency, cost and size.
- It is aimed to provide a detailed design procedure for proposed designs and their controllers with theoretical analysis and simulation case studies.

1.3. Contribution of the Thesis

The main contributions of this thesis are given as follows:

- A DVC is proposed to reduce the output ripple of the interleaved AC-DC PFC boost converter. With the proposed DVC, the output voltage ripple is reduced to below 0.5V. Thus, it is possible to use the smaller and longer-life film capacitor as a DC-link capacitor.
- The controller performance of the AC-DC interleaved PFC boost converter enhanced to reduce the rate of injected harmonics and transient time.
- A novel soft-switching AC-DC PFC boost converter is proposed to increase efficiency by eliminating switching losses.

- The detailed loss analysis of the proposed converter is conducted to demonstrate the effect of the SS on the efficiency of the traditional AC-DC PFC boost converter.
- A detailed comparison study is presented between the proposed soft-switching AC-DC PFC boost converter and the existing soft-switching AC-DC PFC boost converters in terms of efficiency, cost and advantages.
- A high-frequency AC-DC PFC converter topology is proposed to reduce the size of the OBCs.
- A comprehensive design procedure for proposed controllers and their controllers are presented with theoretical analysis and simulation case studies.
- The proposed AC-DC PFC topologies are the most proper candidates to be commercialized for OBCs due to their advantages properties.

1.4. The Organization of the Thesis

The organization of the thesis is as follows:

Chapter 1: Introduction

The importance and need of AC-DC PFC converters for OBCs, the most important part of EVs, has been introduced and motivation has been provided for this thesis. Also, the research objectives, the contribution of the thesis and the organization of the thesis are given.

Chapter 2: State-of-the-Art AC-DC PFC Converters

In this chapter, the state-of-the-art AC-DC PFC converter topologies and controllers are investigated in detail. In addition, each topology is modeled in the simulation environment and performance results are provided.

Chapter 3: Overview of Soft-Switching Techniques

In this chapter, the SS techniques in the literature are explained in detail for the illustrate the deficiencies of the methods in the literature.

Chapter 4: Design and Analysis of the Proposed DVC for Ripple Reduction of the Interleaved PFC Boost Converter

In this chapter, the operating modes and design criteria of the proposed dynamic voltage compensator (DVC) and its controller are provided in detail, which is recommended to reduce the output voltage ripple of the interleaved PFC boost converter. Also, the performance of the proposed converter and the controller has been tested by different case studies according to the European efficiency standards.

Chapter 5: Design and Analysis of Soft-Switching AC-DC PFC Boost Converter

In this chapter, the description and steady-state operating principles of the proposed soft-switching AC-DC PFC boost converter are explained. The design considerations are provided in depth. Also, the performance of the proposed converter has been tested by case studies according to the European efficiency standards.

Chapter 6: Conclusion and Future work

Concluding remarks and main contributions of the thesis are given in this chapter. Also, the future perspectives of the thesis work are discussed.
The organization of the thesis is illustrated in Figure 1.6.

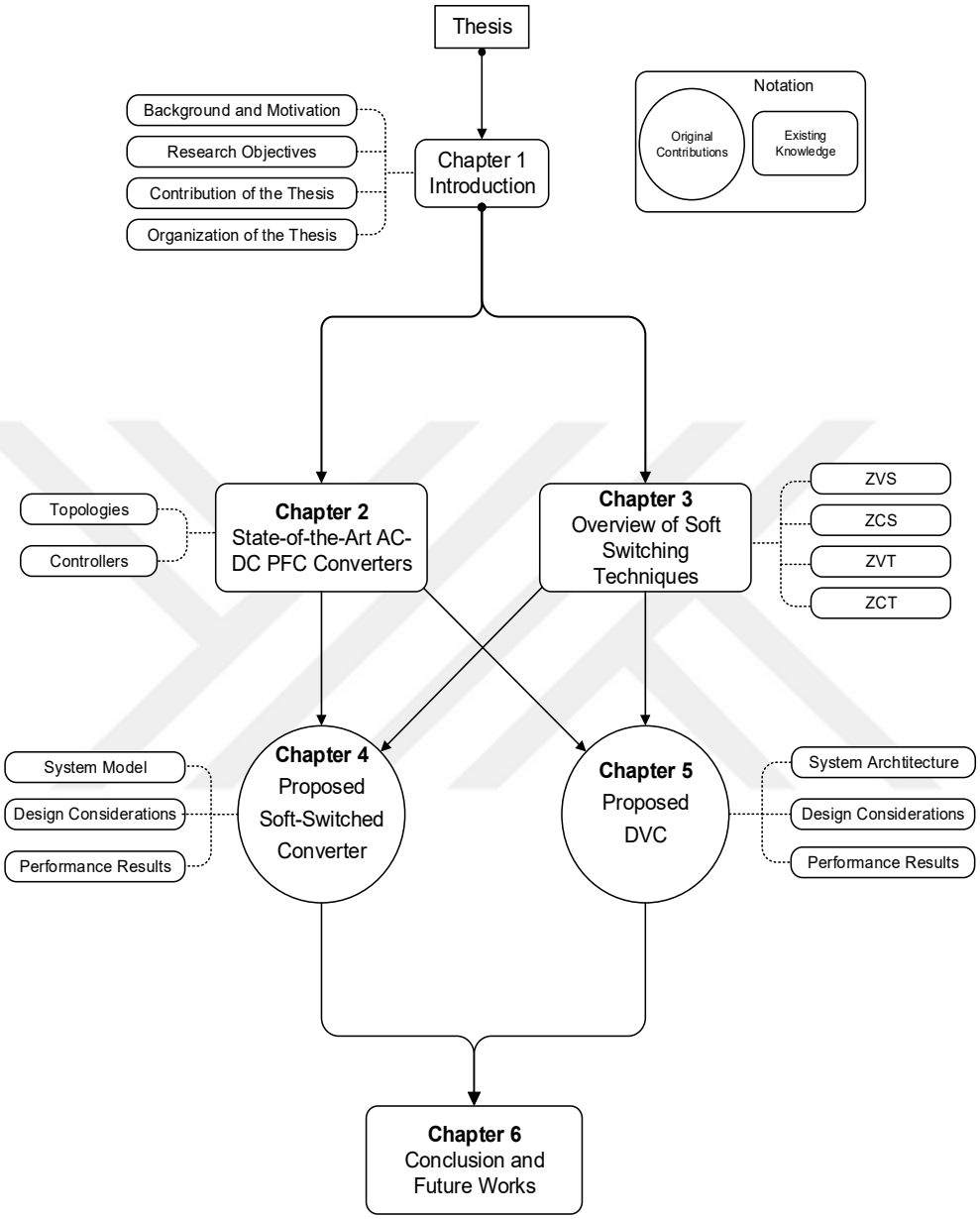

Figure 1.6. The organization of the thesis

1.5. Summary

Firstly, the background and motivation of the thesis are provided in this chapter. Then, based on this information, the research objectives of the thesis are determined and all the contributions of the thesis are presented. Finally, the organization of the thesis has been presented.

2. STATE-OF-THE-ART AC-DC PFC CONVERTERS

In this section, AC-DC PFC converter configurations and control techniques in the literature are presented in detail. The performance of each configuration is evaluated by case studies for load conditions at European efficiency standards. At the end of this section, recent publications on AC-DC PFC converters developed for a battery charging system in EVs are provided in detail.

2.1. Topologies for AC-DC PFC Converters

In the literature, many converter configurations such as buck, boost, buck-boost and their variations have been developed to perform AC-DC PFC conversion. The input current of the boost PFC converter topologies is continuous and therefore does not need a large filter at the input side. Since other topologies have pulsed input current, they need larger filtering at the input sides. Also, boost topology has a wide input voltage range, while other topologies have a more limited input voltage range (Alam, 2017). Due to these mentioned benefits, this thesis has focused on AC-DC PFC Boost converters and their variations.

2.1.1. Traditional PFC Boost Converter

This converter is the most popular among AC-DC PFC converters with its simple structure, low cost and easy controllability. This converter consists of two stages, a diode bridge rectifier and a boost converter, as illustrated in Figure 2.1. The inductor ripple current of the boost circuit directly affects the input current of the converter and requires filtering to comply with electromagnetic interference (EMI) specifications. The output diode current of the boost circuit is discontinuous and it must be filtered by the output capacitor to ensure the continuity of this current.

This converter suffers from low efficiency due to high switching losses in the boost circuit and high conduction losses of the input rectifier bridge. In

addition, at high operating frequencies, reverse recovery problems occur at the diode of the boost circuit, resulting in turn-off losses and EMI. Therefore, reducing switching losses is the basis of studies on this topology (Yao et al., 2020; Luo et al., 2020; Li et al., 2020; Nair and Narasamma, 2019; Kim et al., 2018; Kulasekaran and Ayyanar, 2018). With proper switching and control techniques, close to unity power factor and high efficiency can be achieved.

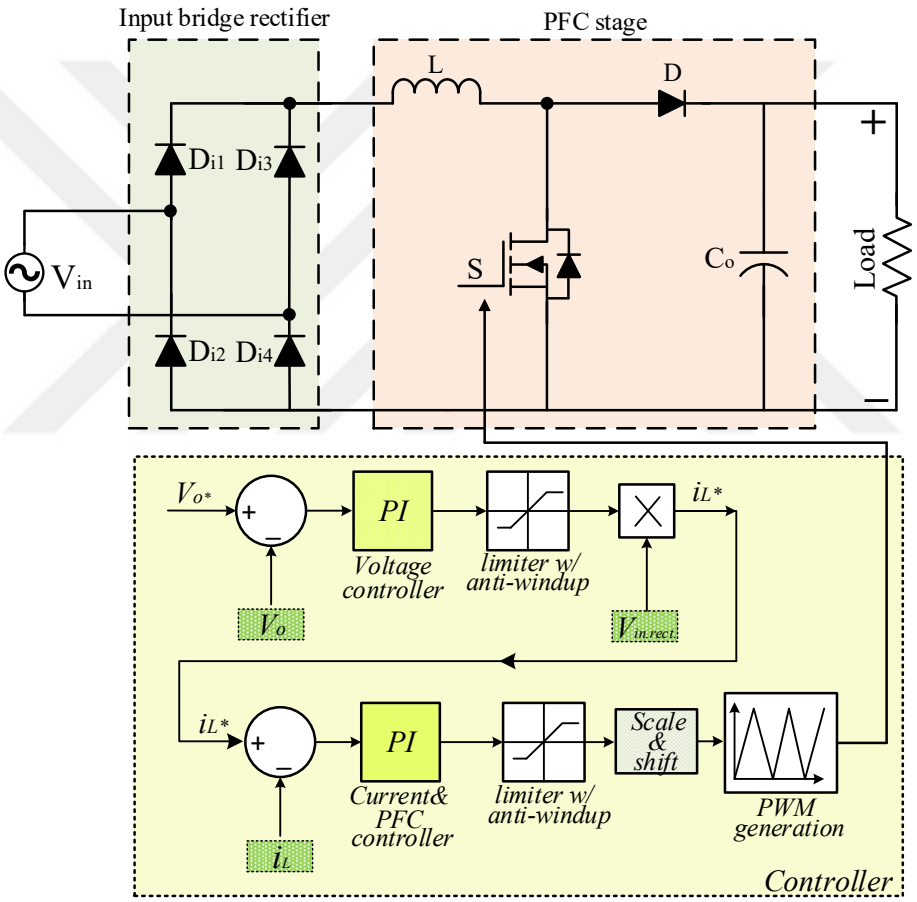

Figure 2.1. Schematic representation of the traditional PFC boost converter and its controller

Equivalent circuits of the operation states in the traditional PFC boost converter are derived from “off-state” and “on-state” of the converter switch as given in Figure 2.2. Based on these equivalent circuits, the mathematical model of the converter is derived by the following equations:

$$\frac{di_L}{dt} = \frac{v_{in}}{L}, \left(t \in \left[0, DT_{sw}\right]\right) \tag{2.1}$$

$$v_{in}(t) = \sqrt{2}V_{in,rms}\sin(wt) = \sqrt{2}V_{in,rms}\sin\left(\frac{2\pi}{T_{sw}}t\right) \tag{2.2}$$

$$\frac{di_L(t)}{dt} = \frac{v_{in}(t) - v_0}{L}, \left(t \in \left[DT_{sw}, T_{sw}\right]\right) \tag{2.3}$$

The minimum value of the boost circuit inductance is calculated by the following equation.

$$L_{min} = \frac{D(1-D)^2}{2f_{sw}}R_{load} \tag{2.4}$$

The minimum value of the output capacitor of the boost circuit is calculated by the following equation.

$$C_{min} = \frac{D}{f_{sw}R_{load}\Delta V_O} \tag{2.5}$$

The duty cycle of the boost circuit switch is defined by the following equation.

$$D = \frac{V_O - V_{in}}{V_O} \tag{2.6}$$

where v_{in} is the input voltage, v_0 is the output voltage, f_{sw} is the switching frequency, T_{sw} is the switching period, D is the duty ratio, R_{load} is the load resistance, ΔV_O is the output voltage ripple, $V_{in,rms}$ is the rms value of the input voltage, i_L is the inductor current.

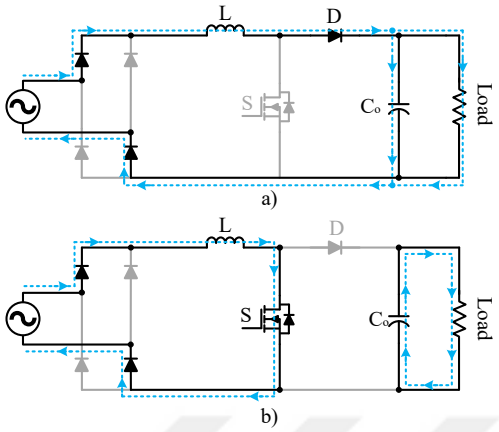

Figure 2.2. Equivalent circuits of the operation states in the traditional PFC boost converter: a) State 1, b) State 2

In order to assess the performance of this topology, a 3.3kW circuit and its controller are constructed in the Matlab/Simulink environment and tested for various load conditions in European efficiency standards. The simulation parameters of the constructed traditional PFC boost converter are provided in the below table.

Table 2.1. The simulation parameters of the constructed traditional PFC boost converter

Parameter	**Value**	**Unit**
Input voltage (V_{in})	220	V_{rms}
Input line frequency (f)	50	Hz
Output voltage (V_{out})	400	Vdc
Output power (P_{out})	3.3	kW
Inductance (L)	150	uH
Switching frequency (f_{sw})	70	kHz
Output capacitor (C_o)	1	mF
PI constants of the voltage controller	$K_p = 0.03$, $K_i = 6$	N/A
PI constants of the current controller	$K_p = 2$, $K_i = 3$	N/A

Figure 2.3 shows the input current and voltage graphs at different load conditions. The total harmonic distortion values occurring in the current drawn

from the network for each load case are indicated on the graphs. Another important parameter to verify the performance of the converter is the PF. The PF values for each load case are measured and indicated on the figure.

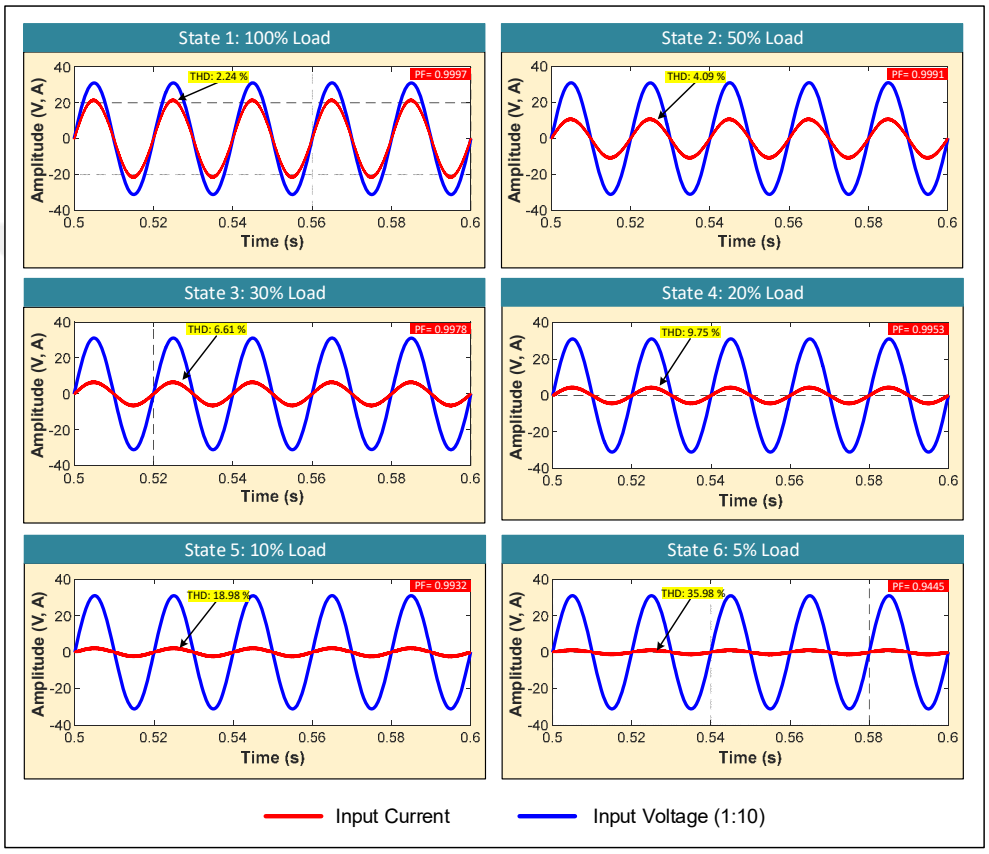

Figure 2.3. The input current and voltage graphs of the traditional PFC boost converter

Output voltage and current graphs for different load conditions are given in Figure 2.4 and Figure 2.5. With these graphs, both the dynamic response of the converter and the amount of the output voltage ripple is tested.

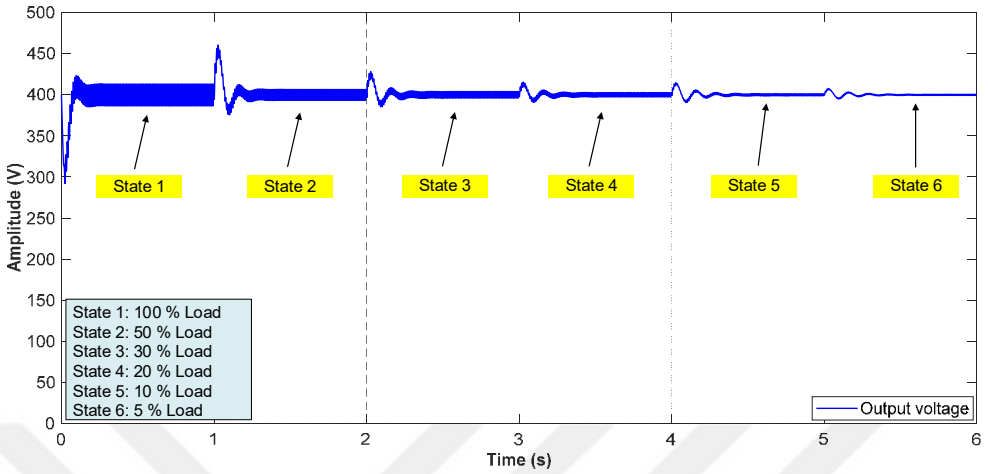

Figure 2.4. The output voltage graph of the traditional PFC boost converter under variable load conditions

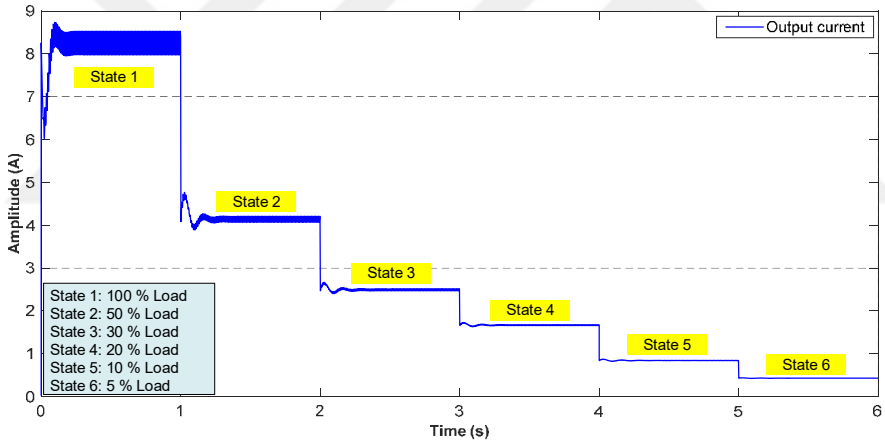

Figure 2.5. The output current graph of the traditional PFC boost converter under variable load conditions

2.1.2. Bridgeless PFC Boost Converter

This topology eliminates the input bridge rectifier in the traditional boost PFC topology but preserves the boost structure as illustrated in Figure 2.6. There is no difference in the size of the passive components compared to the traditional PFC circuit. By eliminating the input bridge rectifier, the total number of semiconductors has decreased from six to four and reduces conduction losses and

the associated heat management problem at the input rectifier bridge (Valipour et al., 2020b; Jappe et al., 2019; Mejía-Ruiz et al., 2017). In addition, this topology has high switching losses due to the hard switching operation of the boost circuit switches. This problem can be overcome with proper SS techniques (Muhammad and Lu, 2015; Tsai et al., 2011). Although switching losses increase in this topology, eliminating the conduction losses of the input bridge ensures more efficient results for high power applications.

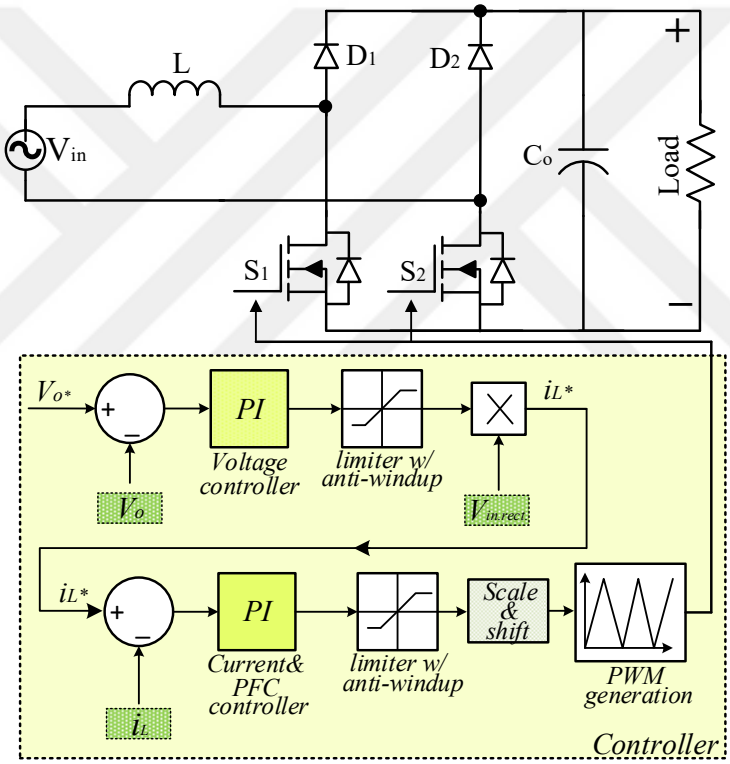

Figure 2.6. Schematic representation of the bridgeless PFC boost converter and its controller

The bridgeless PFC boost converter has four different operating states for the positive and negative cycle of the AC input voltage, depending on whether the

switches S_1 and S_2 are on and off as shown in Figure 2.7. For these different states of S_1 and S_2 switches, both output voltage control and PFC are performed.

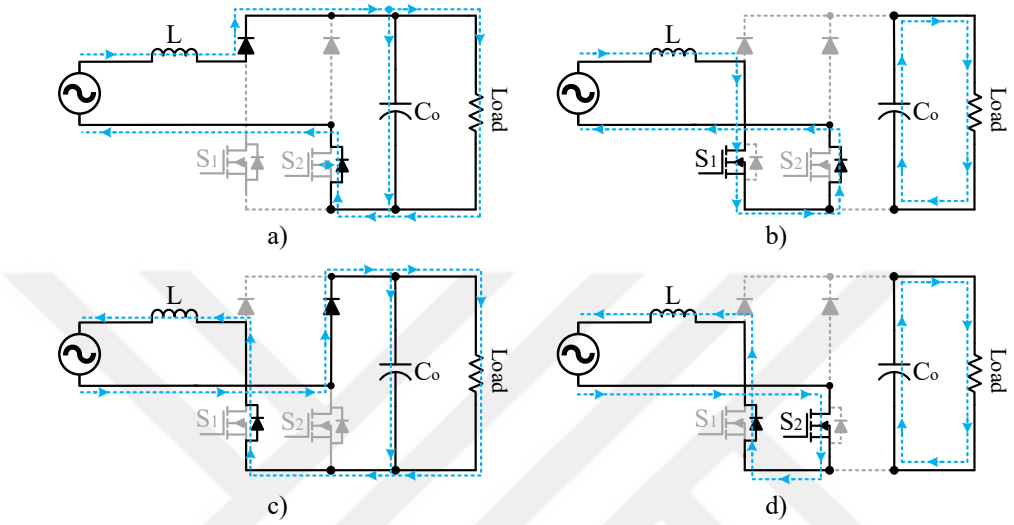

Figure 2.7. Equivalent circuits of the operation states in the bridgeless PFC boost converter: a) State 1, $V_{in}>0$, b) State 2, $V_{in}>0$, c) State 3, $V_{in}<0$, d) State 4, $V_{in}<0$

Since the switches S_1 and S_2 in this topology are driven synchronously, for some cases, the voltage on it becomes zero and some of the switching losses are eliminated since it will be in the on position when current flows through them. Current sensing is more complex than traditional PFC boost topology since the current path does not share the same grounding in every half-line cycle (Frank et al., 2005). It also requires a low-frequency transformer and optical coupler for the measurement of the input voltage since the grid floats compared to the ground of the PFC stage.

In order to assess the performance of this topology, a 3.3kW circuit and its controller are constructed in the Matlab/Simulink environment and tested for various load conditions in European efficiency standards. The simulation

parameters of the constructed bridgeless PFC boost converter are given in Table 2.2.

Table 2.2. The simulation parameters of the constructed bridgeless PFC boost converter

Parameter	**Value**	**Unit**
Input voltage (V_{in})	220	V_{rms}
Input line frequency (f)	50	Hz
Output voltage (V_{out})	400	Vdc
Output power (P_{out})	3.3	kW
Inductance (L)	150	uH
Switching frequency (f_{sw})	70	kHz
Output capacitor (C_o)	1	mF
PI constants of the voltage controller	K_p= 0.03, K_i = 6	N/A
PI constants of the current controller	K_p= 2, K_i = 3	N/A

Input voltage and current graphs for different load conditions are provided in Figure 2.8. In addition, the THD values occurring in the current drawn from the network for each load case are indicated on the graphs. Another important criterion for verifying the performance of the converter is the power factor, its value is calculated separately for each load case and indicated on the figure.

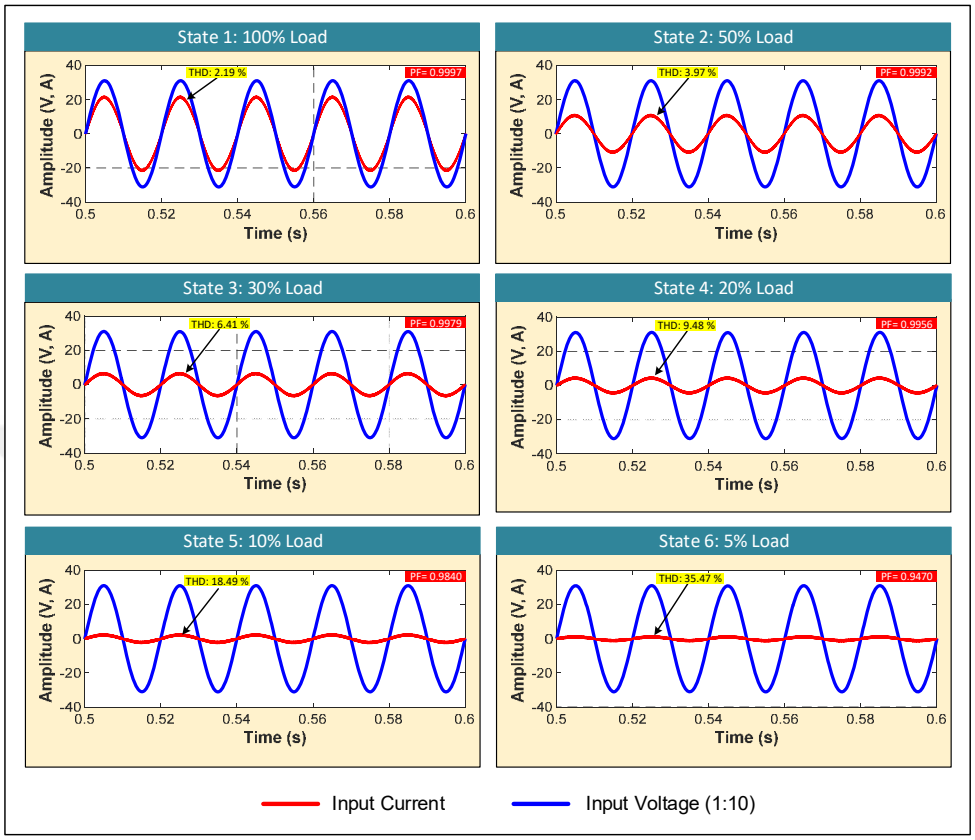

Figure 2.8. The input current and voltage graphs of the bridgeless PFC boost converter

Figures 2.9 and 2.10 illustrate the output voltage and current graphs for different load conditions. With these results, both the dynamic response of the converter and the amount of the output voltage ripple are tested.

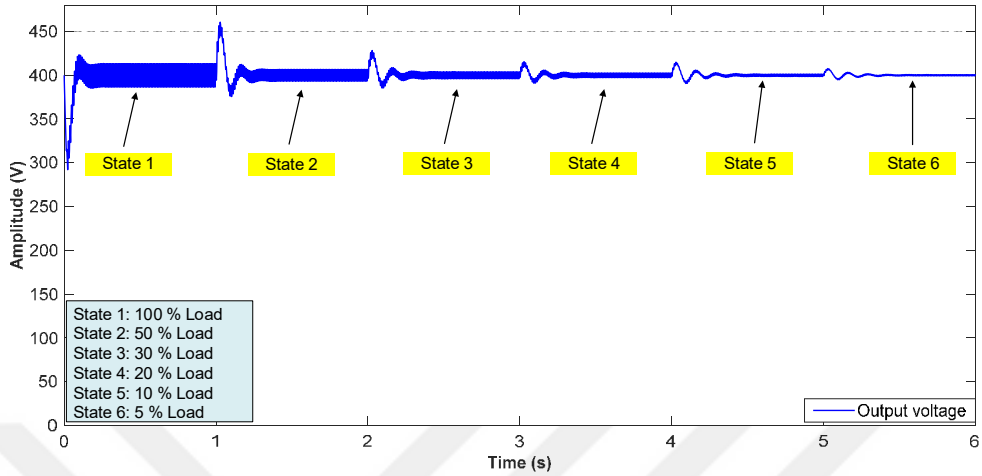

Figure 2.9. The output voltage graph of the bridgeless PFC boost converter under variable load conditions

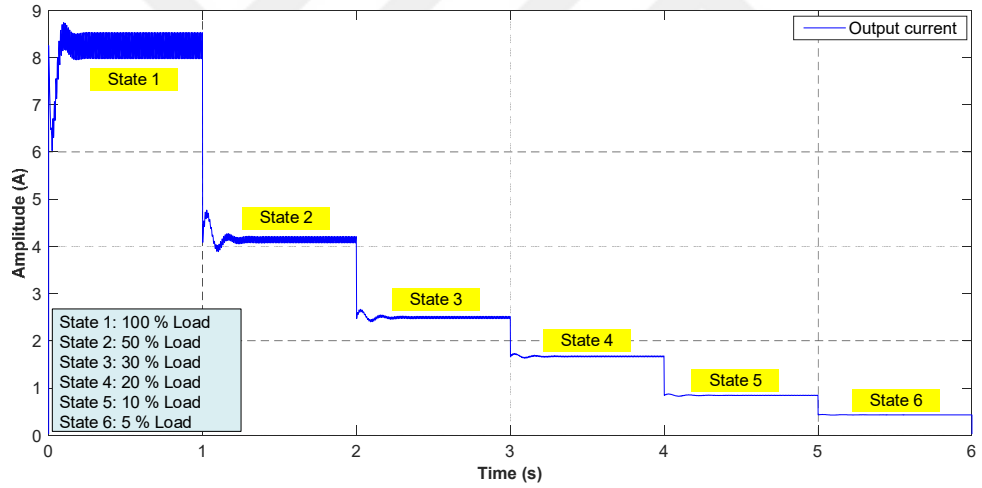

Figure 2.10. Output current graph of the bridgeless PFC boost converter under variable load conditions

2.1.3. Semi-Bridgeless PFC Boost Converter

The main problem of the bridgeless PFC boost converter is EMI noise. The output voltage ground of a bridgeless PFC boost converter always floats relative to the input line. This causes common-mode noise due to the parasitic capacitance of the switching elements. Also, since the connection node of switch S_2 and diode D_2 is directly connected to the mains line, high dv/dt problems occur during the turn-off of the switch. Semi-bridgeless PFC boost topology is introduced to solve these problems. Two slow diodes are added to the input to solve the EMI noise issue. In addition, one inductance has been added to prevent the connection of the S_2 switch and the D_2 diode directly to the grid side as illustrated in Figure 2.11. The added elements do not affect the efficiency, on the contrary, they minimize the current pressure on the switching elements (Perez et al., 2018; Marcos-Pastor et al., 2015; Sudheer et a., 2015; Alam et al., 2012).

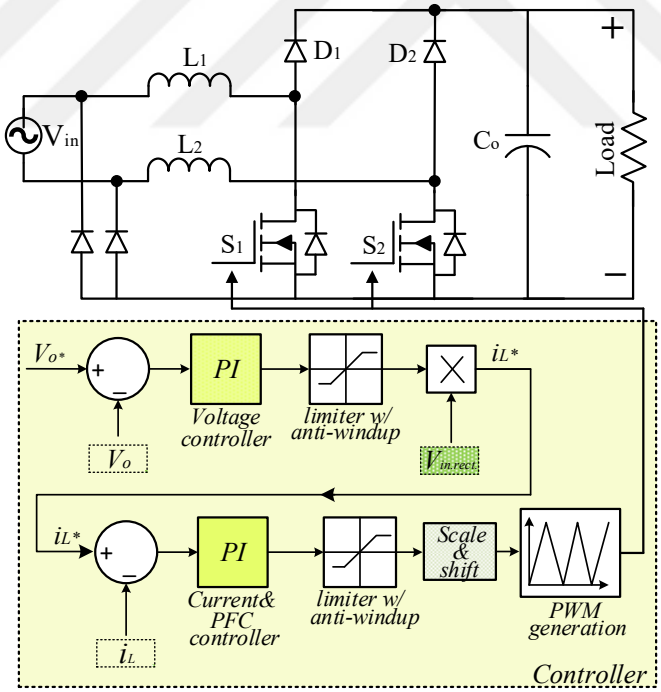

Figure 2.11. Schematic representation of the semi-bridgeless PFC boost converter and its controller

The size of the added inductance is equal to the size of the inductance in the traditional PFC boost circuit. The operating modes of this topology are the same as those of the bridgeless PFC boost topology. There are a parallel diode sharing the current passing through the switch in the return path and a serial inductor in the current path.

The performance of the semi-bridgeless PFC boost converter topology is tested with a constructed 3.3kW circuit and its controller in Matlab/Simulink for various load conditions. The simulation parameters of the constructed semi-bridgeless PFC boost converter are provided in the following table.

Table 2.3. The simulation parameters of the constructed semi-bridgeless PFC boost converter

Parameter	**Value**	**Unit**
Input voltage (V_{in})	220	V_{rms}
Input line frequency (f)	50	Hz
Output voltage (V_{out})	400	Vdc
Output power (P_{out})	3.3	kW
Inductances (L_1, L_2)	150	uH
Switching frequency (f_{sw})	70	kHz
Output capacitor (C_o)	1	mF
PI constants of the voltage controller	K_p= 0.05, K_i = 3	N/A
PI constants of the current controller	K_p= 3, K_i = 0.1	N/A

In Figure 2.12, input current and voltage graphs for different load conditions are illustrated. For each load case, the THD values occurring in the current drawn from the network are calculated and shown on the graphs. In addition, the power factor, which is an important criterion to verify the performance of the converter, is calculated and shown separately for each load case.

The output voltage and current graphs for different load conditions are given in detail in Figures 2.13 and 2.14 to test both the dynamic performance and output characteristics of the converter.

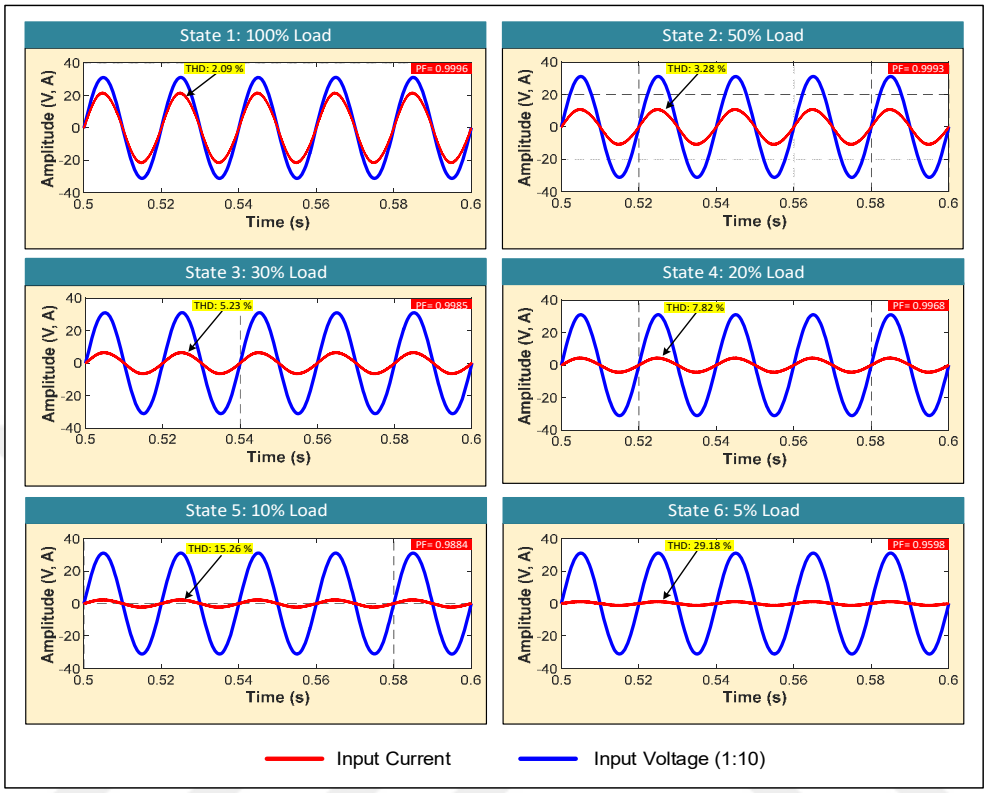

Figure 2.12. The input current and voltage graphs of the semi-bridgeless PFC boost converter

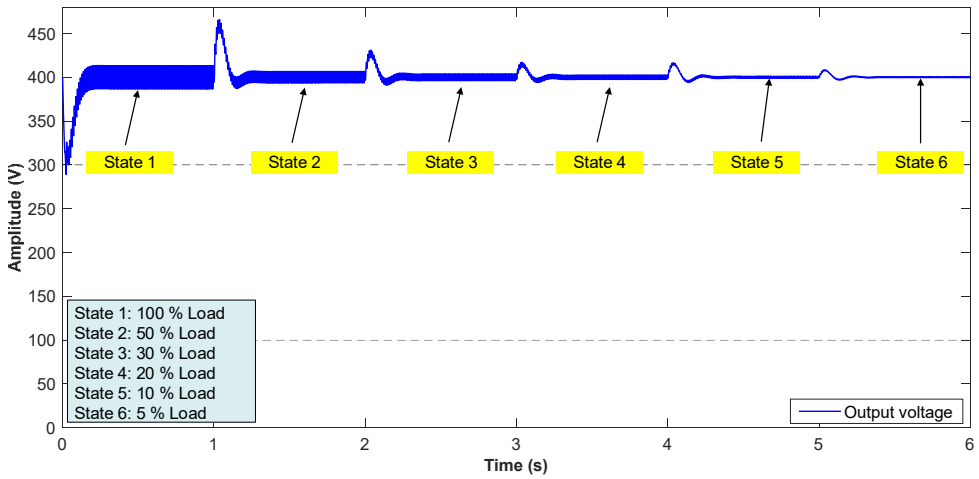

Figure 2.13. The output voltage graph of the semi-bridgeless PFC boost converter under variable load conditions

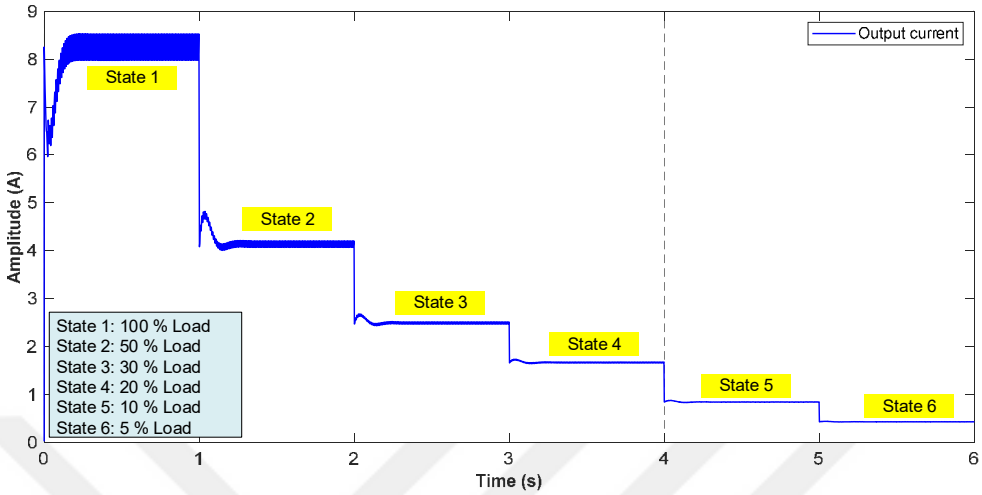

Figure 2.14. The output current graph of the semi-bridgeless PFC boost converter under variable load conditions

2.1.4. Interleaved PFC Boost Converter

This topology consists of two parallel traditional boost converters that operate with 180 phase difference as shown in Figure 2.15.

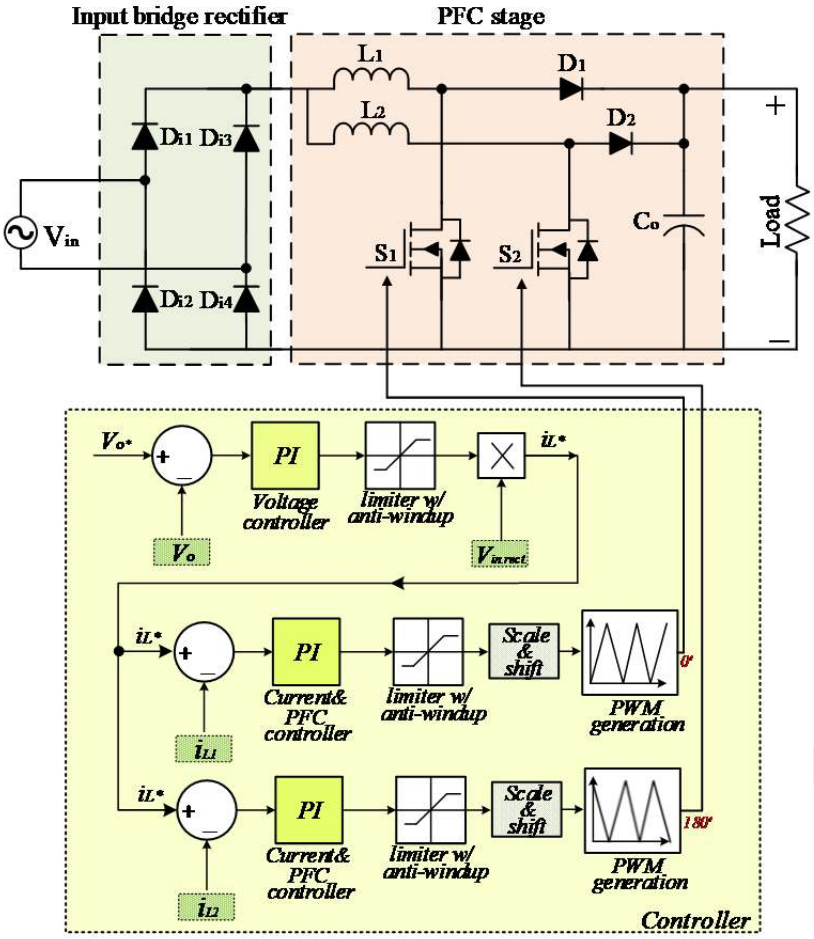

Figure 2.15. Schematic representation of the interleaved PFC boost converter and its controller

The input current of the interleaved PFC boost converter is equal to the sum of the inductor currents of these two boost circuits (Yang et al., 2020; Xu et al., 2019; Marcos-Pastor et al., 2016; Wang et al., 2015a, 2015b). Due to the phase difference between the currents of these inductors, the ripple on the currents eliminates each other and the input current ripple is reduced. The maximum ripple elimination of the input current occurs at a 50% duty cycle (*d*). In the following

equations, the variation of the ratio of the input ripple current to the inductor ripple current ($R(d)$) depends on the duty cycle is shown (O'Loughlin, 2007).

$$R(d)=\frac{\Delta I_{in}}{\Delta I_{L1}} \tag{2.7}$$

$$R(d)=\frac{1-2d}{1-d}\ ,\ d\le 0.5 \tag{2.8}$$

$$R(d)=\frac{2d-1}{d}\ ,\ \ d>0.5 \tag{2.9}$$

The output capacitor current is equal to the sum of the diode currents at the output of the boost converters. Similar to the input current, due to the phase difference between them, the diode ripple currents eliminate each other and the capacitor ripple current is reduced. The variation of capacitor ripple current (I_{Co}) with the duty cycle is given in the equations as follows (O'Loughlin, 2007):

$$I_{Co}(d)=\frac{1}{2}\sqrt{(1-2d)(1-2d)^2}\ \ ,\ \ d\le 0.5 \tag{2.10}$$

$$I_{Co}(d)=\frac{1}{2}\sqrt{(2-2d)(2-2d)^2}\ \ ,\ \ d>0.5 \tag{2.11}$$

For the design of the interleaved PFC boost converter, it can be considered as parallel connection of the two same traditional boost PFC converters with half the total power. Thus, all calculations in the traditional PFC converter apply here as well. This topology eliminates the input current ripple and output voltage ripple. But, input bridge still causes the heat problem and lead to low efficiency under low grid voltages.

There are four different operating states of the interleaved PFC boost converter for each positive and negative cycle of the AC input voltage depending on whether the switches S_1 and S_2 are on and off as shown in Figure 2.16.

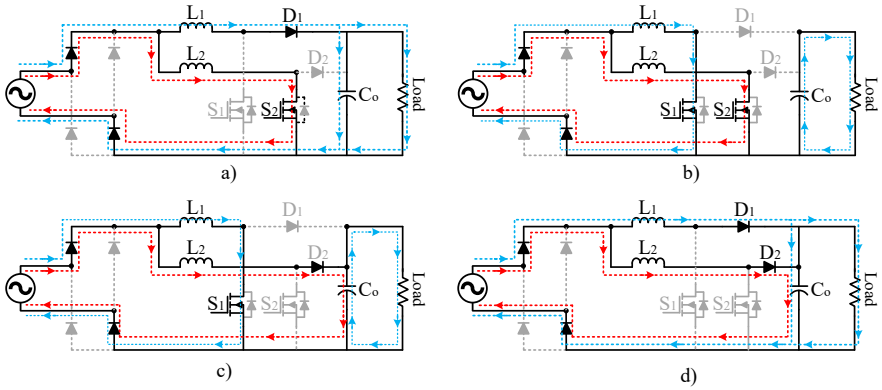

Figure 2.16. Equivalent circuits of the operation states in the interleaved PFC boost converter: a) State 1, b) State 2, c) State 3, d) State 4

In order to assess the performance of this topology, a 3.3kW circuit and its controller is constructed in the Matlab/Simulink environment and tested for various load conditions in European efficiency standards. The simulation parameters of the constructed interleaved PFC boost converter are provided in the following table.

Table 2.4. The simulation parameters of the constructed interleaved PFC boost converter

Parameter	**Value**	**Unit**
Input voltage (V_{in})	220	V_{rms}
Input line frequency (f)	50	Hz
Output voltage (V_{out})	400	Vdc
Output power (P_{out})	3.3	kW
Inductances (L_1, L_2)	150	uH
Switching frequency (f_{sw})	70	kHz
Output capacitor (C_o)	1	mF
PI constants of the voltage controller	K_p = 0.03, K_i = 6	N/A
PI constants of the current controller	K_p = 1.5, K_i = 3	N/A

Figure 2.17 illustrates the input current and voltage graphs for different load conditions. The THD values occurring in the current drawn from the network and the power factor, which is an important criterion to verify the performance of the converter are calculated and shown on the graphs for each load condition.

The output voltage and current graphs for different load conditions are provided in Figure 2.18 and 2.19, respectively.

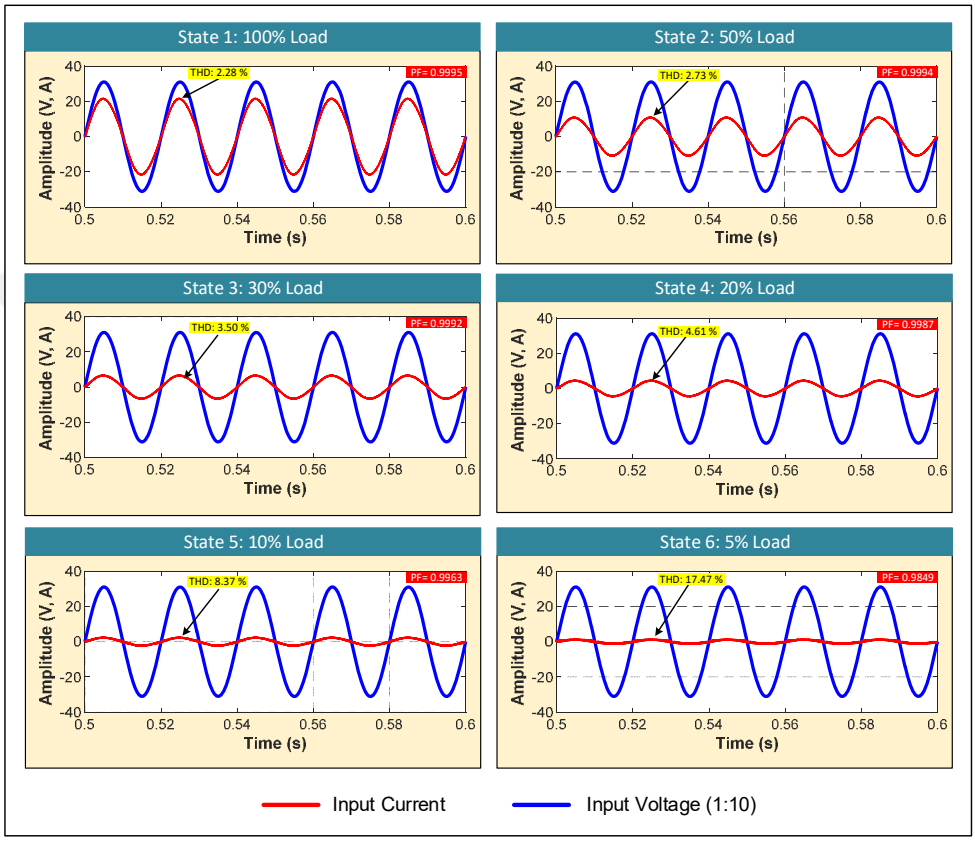

Figure 2.17. The input current and voltage graphs of the interleaved PFC boost converter

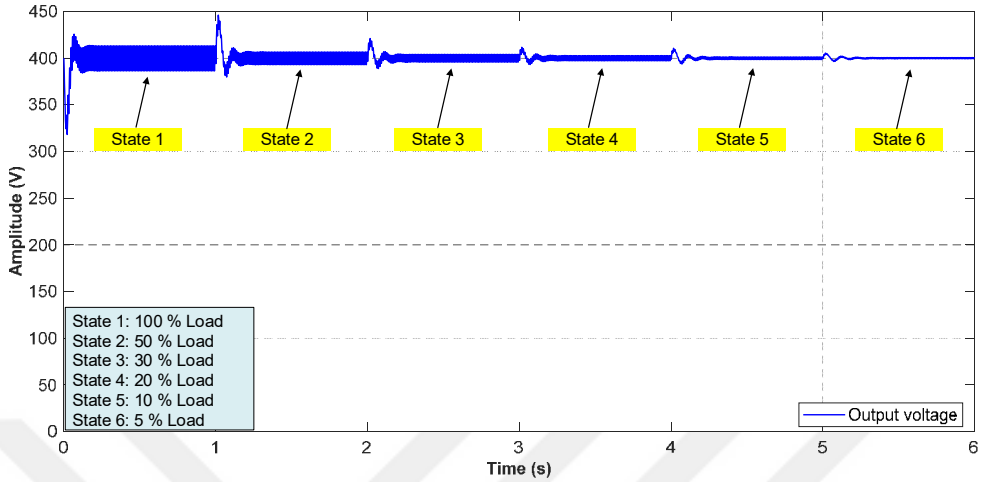

Figure 2.18. The output voltage graph of the interleaved PFC boost converter under variable load conditions

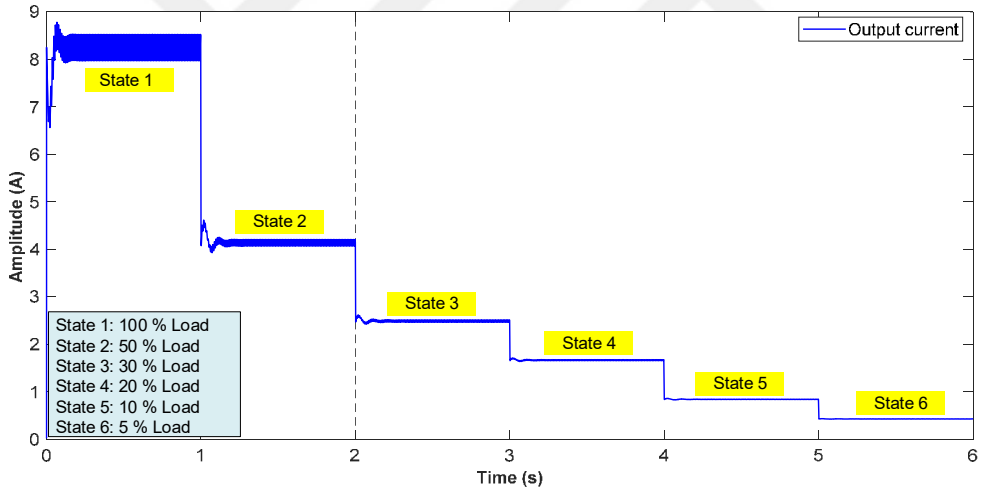

Figure 2.19. The output current graph of the interleaved PFC boost converter under variable load conditions

2.1.5. Bridgeless Interleaved PFC Boost Converter

The bridgeless interleaved (BLIL) PFC boost topology is designed to combine the beneficial features of bridgeless and interleaved PFC boost converter topologies. This topology has a similar structure to the bridgeless PFC boost converter topology, which prevents the input bridge diode heat losses of the

interleaved boost converter topology. In the circuit structure, unlike the interleaved PFC, it contains two extra MOSFETs and inductors, two fast diodes instead of four slow diodes as shown in Figure 2.20. The switches are driven in pairs, synchronously and with a 180^{o} phase difference with the other pair. This converter topology provides solutions to rectifier losses thanks to its bridgeless structure, and input current ripple and output voltage ripple thanks to its interleaved structure. With these aspects, it gives highly efficient results in high power applications. (Gunasekaran, and Thazhathu, 2017; Kannan et al., 2016; Musavi et al., 2011a).

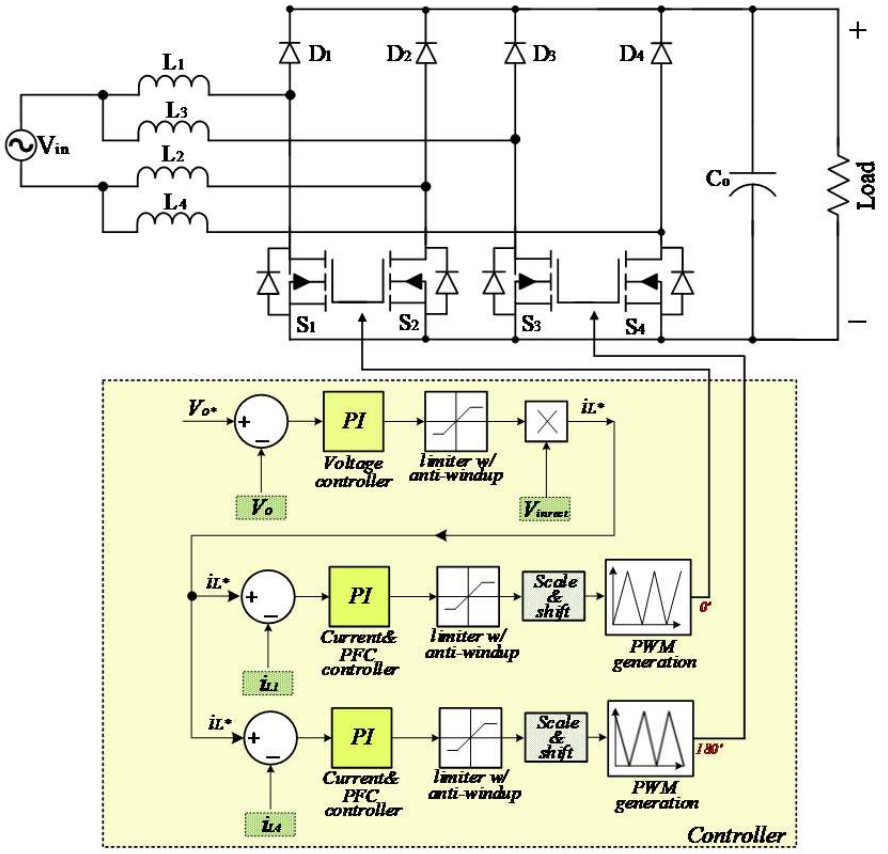

Figure 2.20. Schematic representation of the BLIL PFC boost converter and its controller

Although this topology solved the input bridge rectifier conduction losses, it could not prevent the increased switching losses due to the high number of switches. With SS techniques, these losses can be eliminated, but cost and controller complexity will increase even more.

The circuit operating states differ according to the duty ratio of the switches. The detailed operating states for D>0.5 and D<0.5 in the positive and negative half cycles of the grid voltage are provided in Figure 2.21. Figure 2.21.a-c figures show the operating states for D> 0.5, while Figure 2.21.d-f figures show the operating states for D <0.5.

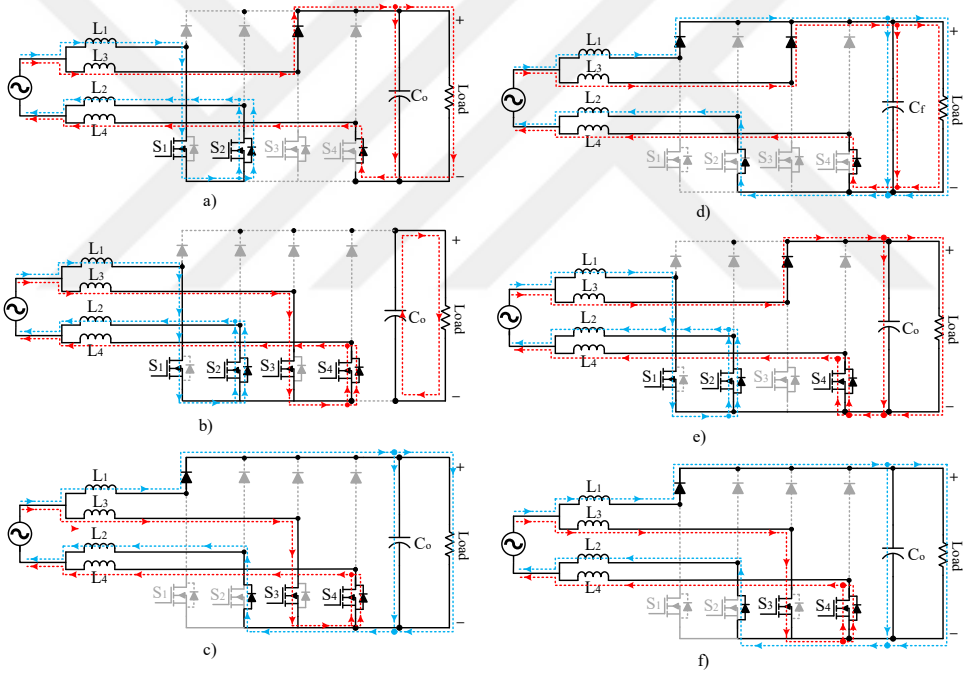

Figure 2.21. Equivalent circuits of the operation states in the interleaved PFC boost converter: a) State 1, D> 0.5, b) State 2, D> 0.5, c) State 3, D> 0.5, d) State 4, D< 0.5, e) State 5, D< 0.5, f) State 6, D< 0.5

In order to assess the performance of this topology, a 3.3kW circuit and its controller is constructed in the Matlab/Simulink environment and tested for various

load conditions in European efficiency standards. The simulation parameters of the constructed BLIL PFC boost converter are given in Table 2.5.

Table 2.5. The simulation parameters of the constructed BLIL PFC boost converter

Parameter	**Value**	**Unit**
Input voltage (V_{in})	220	V_{rms}
Input line frequency (f)	50	Hz
Output voltage (V_{out})	400	Vdc
Output power (P_{out})	3.3	kW
Inductances (L_1, L_2, L_3, L_4)	150	uH
Switching frequency (f_{sw})	70	kHz
Output capacitor (C_o)	1	mF
PI constants of the voltage controller	K_p= 0.03, K_i = 6	N/A
PI constants of the current controller	K_p= 15, K_i = 5	N/A

The input current and voltage graphs of the converter for different load conditions are provided in Figure 2.22. For each load condition, the THD values occurring in the current drawn from the network and the power factor, which is an important criterion to evaluate the performance of the converter are calculated and shown on the graphs.

The output voltage and current graphs for different load conditions are provided in Figure 2.23 and 2.24, respectively.

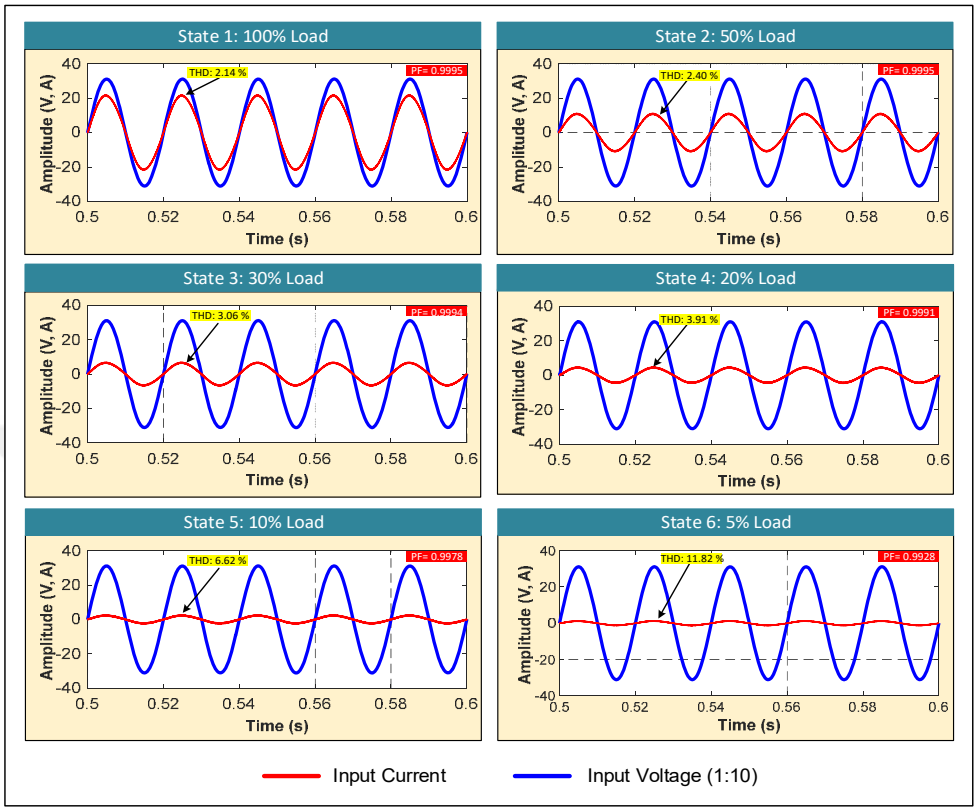

Figure 2.22. The input current and voltage graphs of the BLIL PFC boost converter

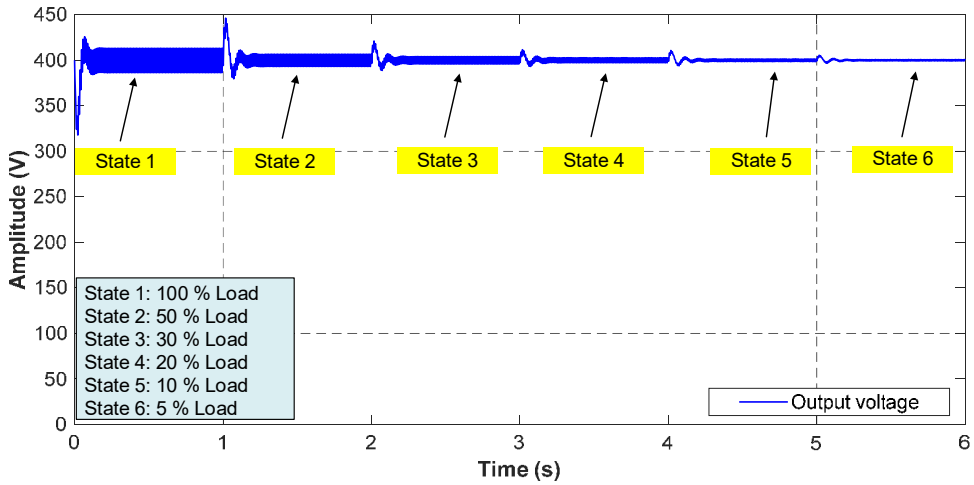

Figure 2.23. The output voltage graph of the BLIL PFC boost converter under variable load conditions

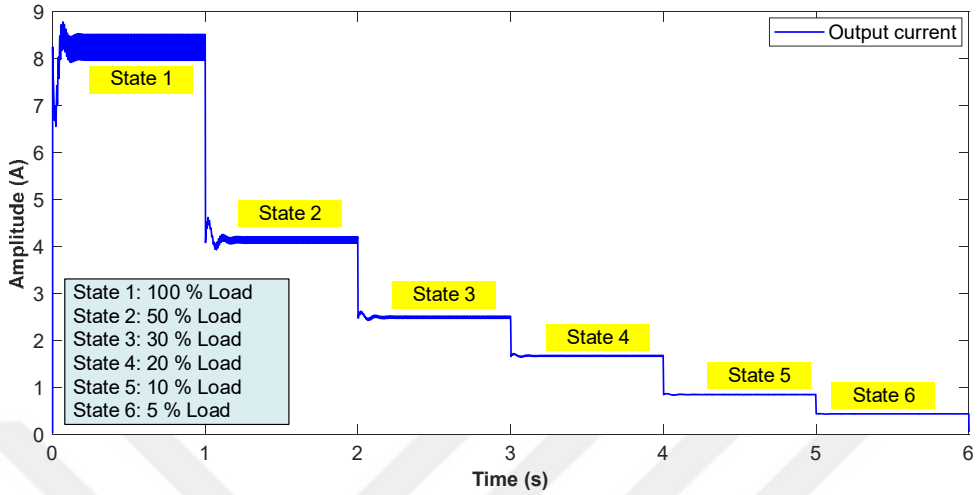

Figure 2.24. The output current graph of the BLIL PFC boost converter under variable load conditions

2.1.6. Totem-Pole Bridgeless PFC Boost Converter

The totem-pole bridgeless (TPBL) PFC boost topology shown in Figure 2.25 is a design obtained by replacing the D_1 diode and S_2 switch of the bridgeless PFC boost topology in Figure 6. This topology is called the totem-pole bridgeless PFC boost because one of the two switches is top of the other. Both diodes D1 and D2 can be selected as slow recovery type. The AC input is connected to the ground of the output through D_2 during the positive cycle and to the positive terminal of the ground line of the output through D_1 during the negative cycle. Since the output never floats compared to the input, the common mode EMI is less and the input voltage measurement becomes easier. In this topology, conduction losses are minimal because only two semiconductor devices operate in each current cycle (Fischer et al., 2020; Jeong et al., 2020; Yu et al., 2019; Liu et al., 2016; Su et al., 2011).

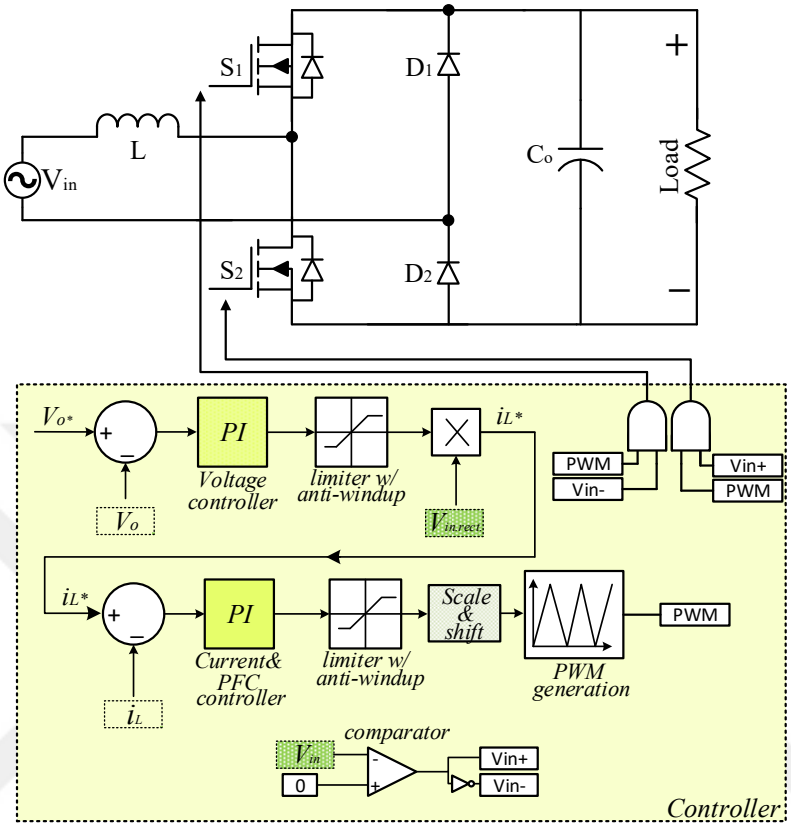

Figure 2.25. Schematic representation of the TPBL PFC boost converter and its controller

With silicon MOSFETs, the TPBL PFC boost converter can only work in discontinuous conduction mode (DCM) or critical conduction mode (CrM) because excessive losses occur due to reverse recovery times of MOSFETs' body diodes in continuous conduction mode (CCM). Although the usage area of the totem-pole bridgeless PFC boost converter is narrow with silicon MOSFETs, it is even preferred in the CCM operation with the emergence of zero reverse recovery conduction switching elements such as silicon carbide and gallium nitride switching elements. Although it is practical to work with CCM with these devices, it is much more useful to operate the circuit in zero voltage switching in CrM because the output capacitance losses are eliminated in this mode. Also, the gate

driver circuit is relatively complicated and should have a high side/low side or insulated structure (Chellappan, 2018).

Because the circuit topology of the TPBL PFC boost converter is similar to the bridgeless PFC boost converter, the design procedure is the same as the traditional PFC converter like the bridgeless PFC boost converter.

The TPBL PFC boost converter has four different operating states for each one cycle of the AC input line, depending on whether the switches S_1 and S_2 are on and off as shown in Figure 2.26.

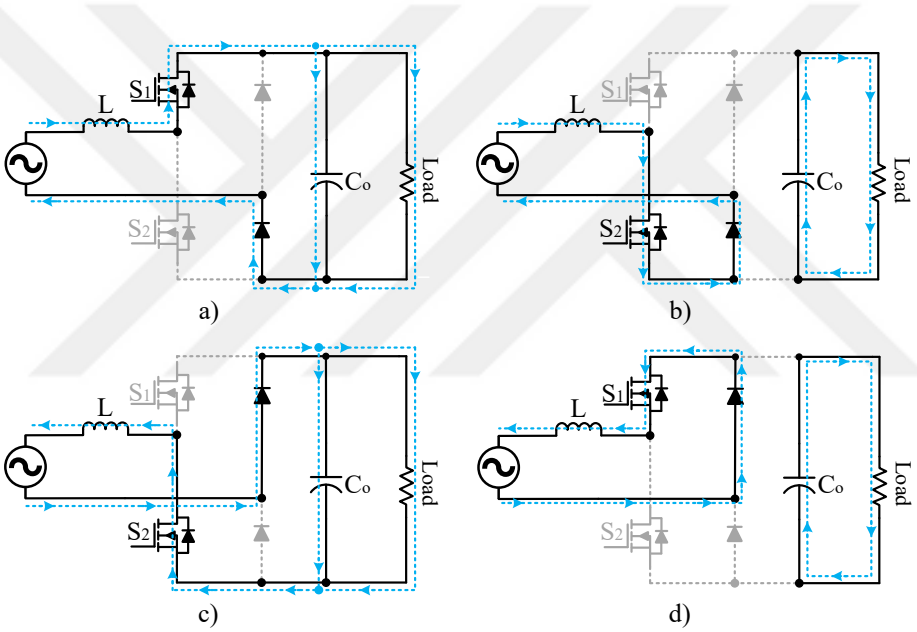

Figure 2.26. Equivalent circuits of the operation states in the interleaved PFC boost converter: a) State 1, $V_{in}>0$, b) State 2, $V_{in}>0$, c) Sate 3, $V_{in}<0$, d) State 4, $V_{in}<0$

The performance of this topology is tested with a constructed 3.3kW circuit and its controller in Matlab/Simulink for various load conditions. The simulation parameters of the constructed TPBL PFC boost converter are given in Table 2.6.

Table 2.6. The simulation parameters of the designed TPBL PFC boost converter

Parameter	**Value**	**Unit**
Input voltage (V_{in})	220	V_{rms}
Input line frequency (f)	50	Hz
Output voltage (V_{out})	400	Vdc
Output power (P_{out})	3.3	kW
Inductance (L)	150	uH
Switching frequency (f_{sw})	70	kHz
Output capacitor (C_o)	1	mF
PI constants of the voltage controller	K_p= 0.03, K_i = 6	N/A
PI constants of the current controller	K_p= 2, K_i = 2	N/A

In Figure 2.27, input current and voltage graphs for different load conditions are illustrated. For each load case, the THD values occurring in the current drawn from the network are calculated and shown on the graphs. In addition, the PF, which is an important criterion to evaluate the performance of the converter, is calculated and shown separately for each load case.

The output current and voltage graphs for different load conditions are given in detail in Figures 2.28 and 2.29 to test both the dynamic performance and output characteristics of the converter.

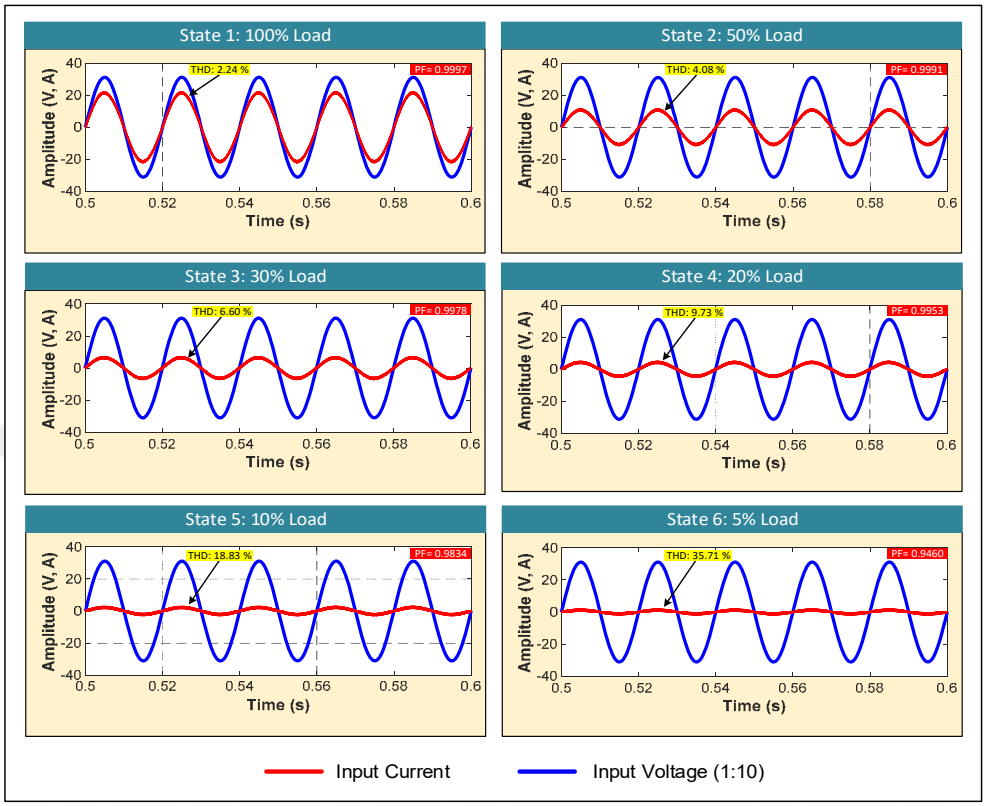

Figure 2.27. The input current and voltage graphs of the TPBL PFC boost converter

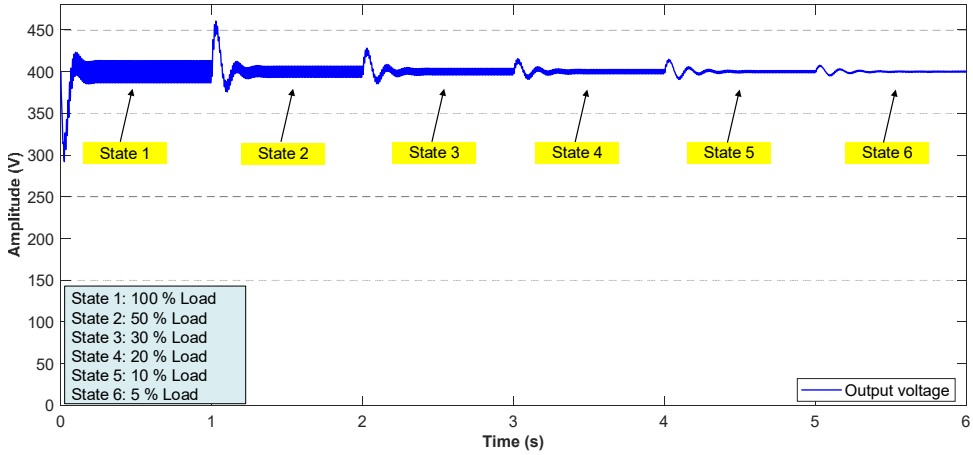

Figure 2.28. The output voltage graph of the TPBL PFC boost converter under variable load conditions

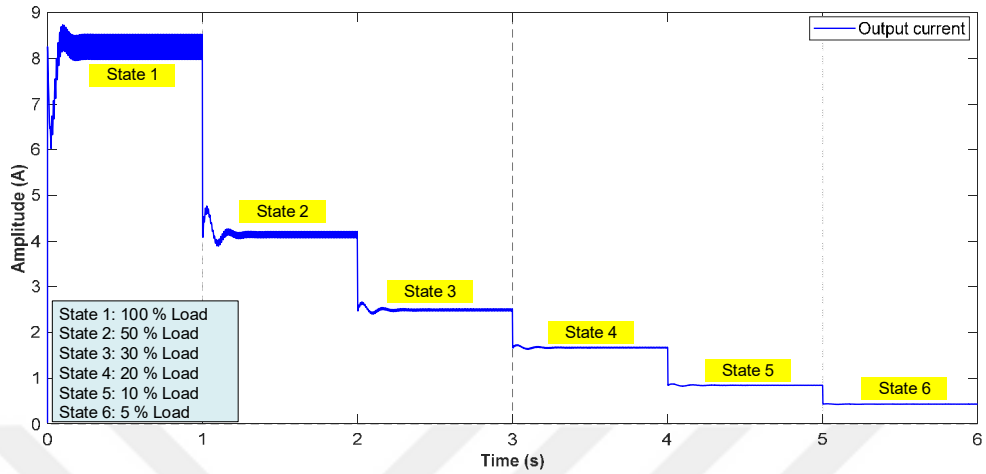

Figure 2.29. The output current graph of the TPBL PFC boost converter under variable load conditions

2.2. Control Techniques for AC-DC PFC Converters

AC-DC PFC converters should be formed to enable the battery charger to deliver power from the grid to the battery with a high power factor and in compliance with the standards. Operation at low power factor values increases the reactive power drawn from the grid and this causes the efficiency of the battery charger to decrease. Increasing the THD of the current drawn from the grid creates stress on the circuit elements and also negatively affects the efficiency of the entire system. In addition, the performance of the AC-DC PFC converter determines the amount of ripple that occurs at its output in rectifying the grid voltage. The amount of these ripple effect both the size and lifetime of the DC-link capacitor. Therefore, the control of the AC-DC PFC converters is a vital task for battery chargers.

The control of AC-DC PFC converters is provided by current mode control techniques consisting of an outer voltage loop that controls the output voltage and an inner current loop that enables the implementation of PFC. With these control techniques, AC-DC PFC converters operate in three different operating modes according to the input inductor current continuity, CCM, DCM and CrM. In CCM operation, the current passing through the inductor does not drop to zero during the

entire switching time, the switch is turned on again before the current drops to zero. The voltage ripple is lower than in DCM operation, resulting in lower conduction losses. In addition, the low ripple current produces lower inductor-core losses. Therefore, CCM operation is preferred at high power levels. The only problem with CCM is that it requires a diode with a very fast recovery feature. The AC-DC PFC boost converter operating in DCM and CrM modes is easier to control than CCM operation, but, it has a higher current ripple, resulting in higher input inductor current, higher losses, and required large size filter. Thus, these modes are more suitable for low power applications.

Current mode control techniques designed for AC-DC PFC converters are peak current mode control, average current mode control, hysteresis current mode control, borderline current mode control, one cycle current mode control and these methods are discussed in the following sections.

2.2.1. Peak Current Mode Control

The control scheme of the peak current mode (PCM) control technique and the current waveforms are given in Figure 2.30 and 2.31, respectively. In this control technique, switch S is turned on by a clock signal which has a constant frequency. When the sum of the positive ramp of the inductor current and external ramp signal equals the reference signal, the switch is turned off. This reference signal is obtained by scaling the rectified input voltage with a gain value and multiplying it with the output of the outer voltage loop that adjusts the amplitude of the current reference. This reference signal, synchronized with line voltage, enables the obtain of the unity power factor.

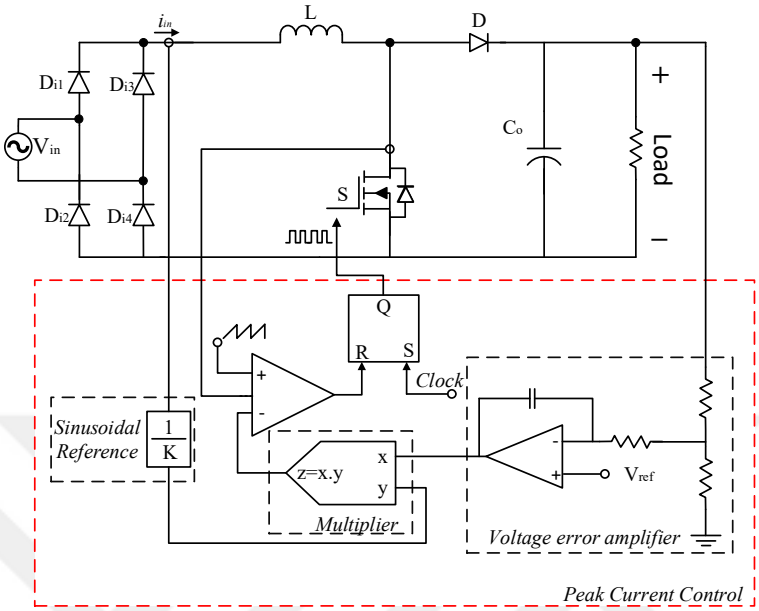

Figure 2.30. The control scheme of the PCM control technique

When the inductor current drops to zero, the switch turns on. When it reaches the reference current value, the flip-flop is reset and the switch turns off. The switch remains in the turned-off position until the next clock signal comes.

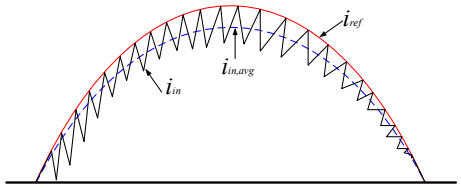

Figure 2.31. The current waveform of the PCM control technique

PCM control technique has advantages of fixed switching frequency, absence of the current error amplifier and its compensation circuit. However, it suffers from harmonic oscillations that will occur if the duty cycle is above 50%. And, at high input voltage and light loads, the distortion of the input current increases and tends to worsen with external ramp. Also, it is very sensitive to

commutation noises. Therefore, this controller is not widely used in AC-DC PFC converter applications.

2.2.2. Average Current Mode control

The control scheme of the average current mode (ACM) control technique and the current waveforms are given in Figure 2.32 and 2.33, respectively. In the PCM control technique, the switch is triggered by comparing the difference of the inductor current with the output of the outer voltage loop directly with the clock signal. This current loop has low gain and therefore causes controller instability when the duty cycle is higher than 50%. The ACM control technique overcomes these problems by adding a high gain current error amplifier to the inner current loop. The sensed output voltage is subtracted from the reference voltage value via a voltage error amplifier and filtered. This filtered signal is then multiplied by the rectified and scaled input voltage and transmitted to the current error amplifier as a current reference signal. The measured inductor current is subtracted from the reference current signal by the current error amplifier and filtered. This signal is then compared to a saw tooth signal and the triggering signal of the switch is generated.

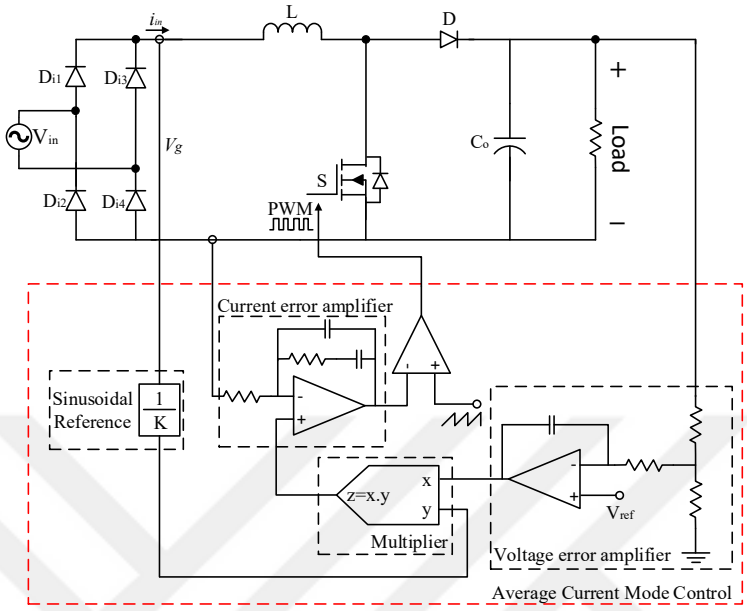

Figure 2.32. The control scheme of the ACM control technique

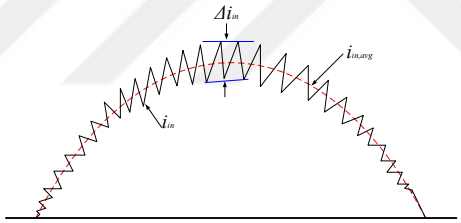

Figure 2.33. The current waveforms of the ACM control technique

ACM control technique has advantages such as constant switching frequency, providing the high input power factor, no need for compensation ramp for inner current loop, having high noise immunity. However, the necessity of current sensors, current fault amplifiers, multipliers and dividers complicates the control circuit. AC-DC PFC converters operate in CCM with this control technique and can also switch to DCM under low load conditions. It is widely used in high power applications due to the above-mentioned features.

2.2.3. Hysteresis Current Mode Control

The control scheme of the hysteresis current mode (HCM) control technique and the current waveforms are given in Figure 2.34 and 2.35, respectively. In the HCM control technique, a hysteresis band is added to the coming current reference signal from the external voltage loop, and two current references are generated as $I_{p(ref)}$ upper reference and $I_{v(ref)}$ lower reference. The switch turned on when the inductor current drops below the lower reference signal $I_{v(ref)}$, turned off when the upper reference signal rises above $I_{p(ref)}$, and this causes variable frequency control. The amount of the input ripple current can be reduced by shrinking the hysteresis band, but the narrower the hysteresis band, the higher the switching frequency, resulting in increased switching losses. Thus, the band value should be chosen optimally, taking into account all parameters (Rossetto et al., 1994).

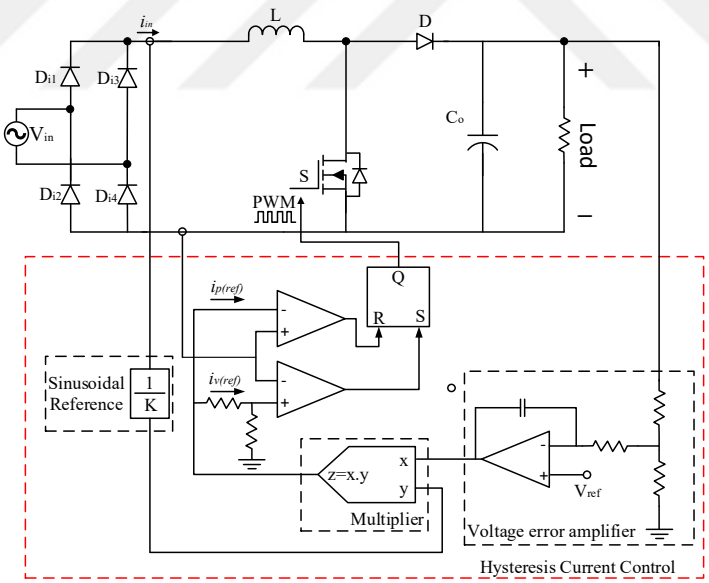

Figure 2.34. The control scheme of the HCM control technique

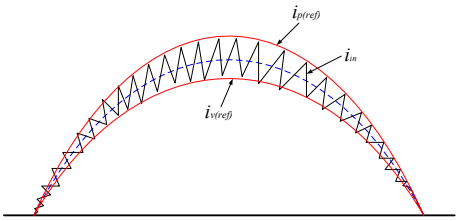

Figure 2.35. The current waveforms of the HCM control technique

In addition, with this control technique, the converter works in CCM. The HCM control technique works fast and also provides excellent dynamic performance. In addition, a natural peak current limiting capacity is also achieved. This control technique does not need a compensation ramp for the internal current loop. Also, the input current distortion of the converter with this controller is less. Having a variable switching frequency is its main disadvantage because the filter inductor must be designed for the lowest frequency.

2.2.4. Borderline Current Mode Control

The control scheme of the borderline current mode (BCM) control technique and the current waveforms are given in Figure 2.36 and 2.37, respectively. In the BCM control technique, the switch remains turned on and constant during the line cycle. The switch turned off when the inductor current drops to zero. The converter operates along the boundary between CCM and DCM operating modes. In this way, the switch turned on with zero current switching, and switching losses are reduced. However, in order to transfer the required power to the output, the peak of the current will increase compared to other topologies and high current peaks increase device stresses and conduction losses.

The case where the lower reference current in the HCM control technique is zero represents the BCM control technique.

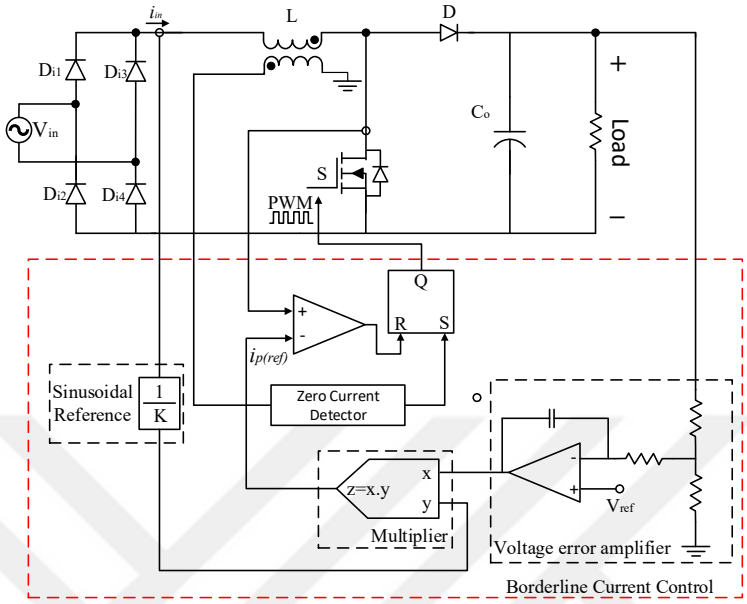

Figure 2.36. The control scheme of the BCM control technique

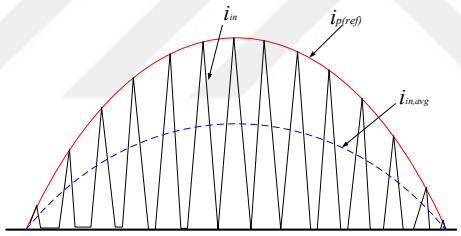

Figure 2.37. The current waveforms of the BCM control technique

BCM control technique has advantages such as no need for compensation ramp and current error amplifier for the inner current loop, having switch current limitation capability. However, having the variable switching frequency and requiring the sensing of the inductor voltage to zero current detection are the main disadvantages of the BCM technique.

2.2.5. One Cycle Current Mode Control

The control scheme of the one cycle current mode (OCCM) control technique is given in Figure 2.38. OCCM control technique does not require

multiplier, input voltage measurement and external ramp. The output voltage of the converter is subtracted from the reference voltage by the voltage error amplifier, filtered and the modulation voltage is produced. Since the voltage loop bandwidth is very narrow, this voltage changes very slowly and can be considered constant throughout a switching cycle. The difference of the measured inductor current and this modulation voltage is compared with the modulation voltage passed through the integrator and the control signal of the switch is generated.

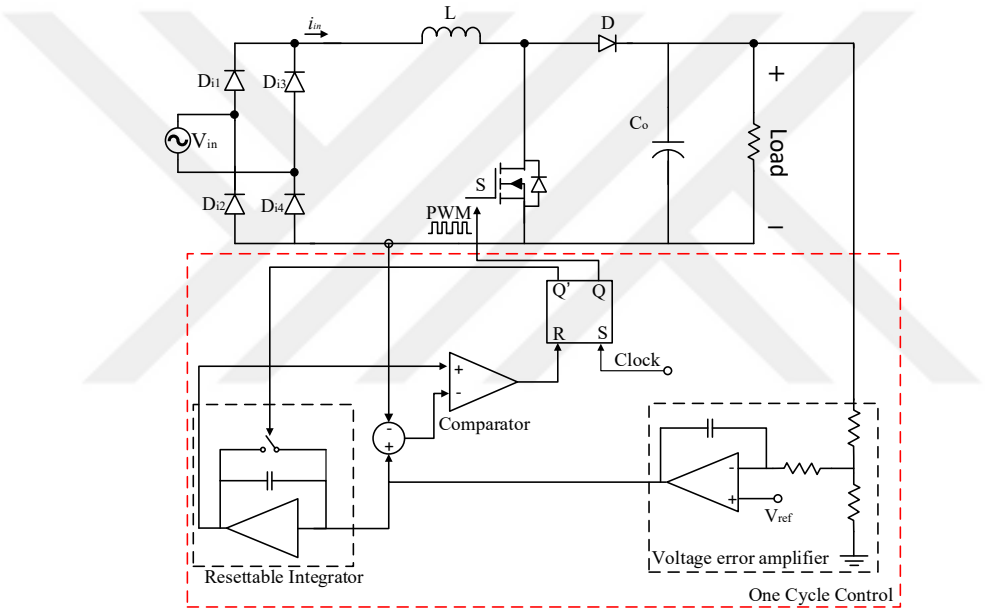

Figure 2.38. The control scheme of the OCCM control technique

The most important advantages of this control technique are that it provides high input power factor, does not need to measure sinusoidal input voltage, operates in CCM, no multiplier and divider, and simplicity of the control system. At high input voltage and light loads, the distortion of the input current increases. Also, it is very sensitive to commutation noises. Therefore, this controller is not widely used in AC-DC PFC converter applications.

2.3. Literature Survey of the AC-DC PFC Converters

The recent publications on AC-DC PFC converter topologies developed for the battery charging system in EVs are provided in detail. The specifications of the developed converter topologies are summarized in Table 2.7. In the table, the studies carried out for each converter topology are presented with features such as power range, input voltage, output voltage, switching frequency and maximum efficiency.

Table 2.7. The conducted studies for AC-DC PFC converters for the battery charging system of EVs in the literature

References	Topology	Power Rate (W)	Input voltage (V_{rms})	Output voltage (V)	Switching Frequency (Hz)	Maximum Efficiency
Luo et al., 2020	Traditional PFC Boost	300	90-132	400	65k	95%
Zhang et al., 2019	Traditional PFC Boost	1000	110	360	50k	N/A
Ting et al., 2019	Traditional PFC Boost	600	85-240	400	100k	95.7%
Kulasekaran and Ayyanar, 2018	Traditional PFC Boost	3300	240	400	500k	97.03%
Cetin, 2018	Traditional PFC Boost	1000	85-230	380	100k	98%
Bodur and Yildirmaz, 2017	Traditional PFC Boost	2000	85-230	400	100k	97.4%
Pahlevani et al., 2014	Traditional PFC Boost	3000	85-246	400	100k	N/A
Valipour et al., 2020b	Bridgeless PFC Boost	2000	90-530	800	60k	98.2%
Cetin and Yenil, 2019	Bridgeless PFC Boost	1000	220	400	100k	%97.4

Table 2.7. Continue

Alam et al., 2017a	Bridgeless PFC Boost	650	85-265	400	70k	97.5%
Alam et al., 2017b	Bridgeless PFC Boost	650	85-265	400	150k	96.95%
Musavi et al., 2013a	Semi-Bridgeless PFC Boost	3400	90-265	400	70k	98.8%
Yang et al., 2020	Interleaved PFC Boost	1000	85-265	400	100k	~97%
Xu et al., 2019	Interleaved PFC Boost	3300	220	400	80k	97.7%
Marcos-Pastor et al., 2016	Interleaved PFC Boost	2000	230	400	60k	~96.5%
Wang et al., 2015a	Interleaved PFC Boost	1000	155	400	40k	93.5%
Wang et al., 2015b	Interleaved PFC Boost	1000	155	400	75k	97.5%
Pahlevaninezhad et al., 2012a	Interleaved PFC Boost	3000	170-267	235-431	50k	~96.5%
Pahlevaninezhad et al., 2012b	Interleaved PFC Boost	3000	170-267	235-431	50k	~96.5%
Pahlevaninezhad et al., 2012c	Interleaved PFC Boost	3000	170-267	235-431	80k	~98.5%
Gunasekaran and Thazhathu, 2017	BLIL PFC Boost	300	110-230	400	70k	97%
Musavi et al., 2011a	BLIL PFC Boost	3400	85-265	400	70k	98.9%
Jeong et al., 2020	TPBL PFC Boost	800	100-240	400	100k	97.81%
Yu et al., 2019	TPBL PFC Boost	2400	240	400	400k	98.35%
Fan et al., 2019	TPBL PFC Boost	1000	85-265	400	45k	~98.75%
Muhammad and Lu, 2015	TPBL PFC Boost	400	90-240	400	45k	~96%
Su et al., 2011	TPBL PFC Boost	350	90-264	400	30k-250k	98.4%

Luo et al. proposed a new control strategy for traditional PFC boost converter operating in CCM. In the structure of the traditional ACM control technique, the bandwidth of the voltage controller should be narrowly designed to reduce the effect of the output voltage variations on the current controller. Increasing the bandwidth of the voltage controller causes poor converter dynamic response. In their study, the effect of the voltage controller on the current controller is eliminated by separating the voltage control loop and the current control loop, thereby improving the dynamic response of the converter. A 300W hardware was presented to validate the performance of the proposed controller. The maximum efficiency of the constructed system has reached 95% (Luo et al., 2020).

Zhang et al. proposed a new cascaded proportional control with an algebraic estimation method to strengthen the poor dynamic response of the traditional PFC boost converter. With the proposed controller, the average dc-bus energy and instantaneous input power of the converter are regulated. In addition, load power, system nonlinearity and uncertainties were estimated by the proposed algebraic estimation method. A 1 kW hardware was designed to assess the efficacy of the proposed control technique (Zhang et al., 2019).

Ting et al. proposed a new ASC to reduce switching losses for the traditional PFC boost converter. The performance of the proposed cell was verified by theoretical studies and experimental studies obtained from a 600W prototype. With the proposed snubber cell, the converter has achieved a maximum efficiency of 95.7% (Ting et al., 2019).

Kulasekaran and Ayyanar have developed a low loss traditional PFC boost converter with the ZVT circuit. With developed ZVT circuit, the turn-on and turn-off switching losses of the converter are minimized and the efficiency of the converter is increased. The effectiveness of the ZVT circuit has been validated by simulation studies and experimental results obtained from the 3.3-kW setup. The converter has reached a maximum efficiency of 97.03% (Kulasekaran and Ayyanar, 2018).

Cetin proposed a soft-switching PFC boost converter topology. The SS in the proposed converter was provided with a developed ASC. The theoretical analyzes of the converter are provided and the performance of the converter has been confirmed experimentally with a 1kW setup. The maximum efficiency of the converter has been measured around 98% and the input current has a power factor of 0.996 at 220 V_{rms} (Cetin, 2018).

Bodur and Yildirmaz have developed an ASC for the traditional PFC boost converter. All switching elements have turned-on and turned-off under SS conditions. With the transformer in the developed ASC structure, the energies in the switching elements are delivered to the output during the ZVT process, thereby significantly reducing the current voltages of the auxiliary components. The performance of the developed converter has been confirmed by extensive theoretical analysis and results obtained from a 2kW experimental setup (Bodur and Yildirmaz, 2017).

Pahlevani et al. presented an adaptive nonlinear observer capable of accurately predicting the inductor current for sensorless control of the PFC boost converter, despite the uncertainties in the load and other parameters. To verify the effectiveness of the proposed adaptive nonlinear observer, a 3kW hardware was constructed and experimental results were obtained (Pahlevani et al. 2014).

Valipour et al. proposed a bridgeless PFC boost converter with a dc-bus voltage of $800V_{DC}$, which provides a wide input voltage range from $90V_{rms}$ to $530V_{rms}$. The proposed converter exhibited an almost flat efficiency for entire input voltage range. Theoretical analyzes are presented in detail and also experimentally confirmed with a 2kw prototype. The proposed converter has reached 98.2% maximum efficiency at V_{in}=$480V_{RMS}$ (Valipour et al., 2020b).

Cetin and Yenil have proposed a soft-switching bridgeless PFC boost converter with a developed ASC. With the designed ASC, the converter switches turn on under ZVT and turn off under ZVS. Also, the switch of the designed ASC turns on and turns off under soft-switching conditions. The performance of the

proposed converter is validated by theoretical and simulation studies (Cetin and Yenil, 2019).

Alam et al. developed an HRPWM bridgeless PFC boost converter topology for the electric vehicle battery charging applications. With the proposed topology, the input diode bridge rectifier, which affects the efficiency of the AC-DC PFC converter, has been eliminated. The resonance tank components in the designed converter are small in size, with this resonance tank the converter operates in hybrid resonant mode and the reverse-recovery losses for the body diodes of the converter are reduced. A 650W prototype was designed and tested. The developed converter has reached the 97.5% maximum efficiency at 240-V input voltage and 205W load (Alam et al., 2017a).

Alam et al. have proposed a new soft-switched bridgeless PFC boost converter topology for the electric vehicle battery charging applications. With the designed resonance tank, ZVS is provided for all switches and switching losses are minimized. In addition, the speed of the di/dt rate of the output diodes is limited, thereby reducing recovery losses. Since the switches of the proposed converter are triggered with the common control signal, it has a simple controller structure. To verify the proof of concept, the detailed theoretical studies and experimental results are taken from a 650W setup are provided (Alam et al., 2017b).

Musavi et al. proposed a new phase-shifted switching circuit to facilitate the sensing of the current in the semi-bridgeless PFC boost converter topology. The proposed converter has exhibit highly efficient results even at light load conditions and lower grid voltage values. Detailed theoretical analyzes of the designed converter were conducted and compared with the results obtained from a 3.4kW hardware. The presented converter has reached the 98.8% maximum efficiency (Musavi et al., 2013a).

Yang et al. presented a detailed theoretical analysis of the interleaved PFC boost converter with the coupled inductor. A 1kW hardware setup was constructed

to validate the analysis. The constructed prototype has exhibit a 97% maximum efficiency (Yang et al., 2020).

Xu et al. developed a novel design optimization technique for high efficiency interleaved PFC boost converter applications, considering current fluctuations, power factor, maximum magnetic flux density and boost inductor volume. To evaluate the effectiveness of the proposed optimization technique, a 3.3 kW hardware was constructed. The experimental results illustrate that the proposed technique was enhanced the efficiency of the interleaved PFC boost converter with low-cost low-performance devices for all load conditions. The constructed converter has exhibit a 97.7% maximum efficiency (Xu et al., 2019).

Marcos-Pastor et al. presented a digitally controlled interleaved PFC boost converter topology based on the sliding mode approach. Both boost cells of the converter are controlled by an independent internal controller based on the discrete-time sliding mode control method that applies lossless resistance behavior to each cell. The performance of the presented design has been confirmed by experimental results taken from the 2kW hardware. The proposed converter has reached 96.5% maximum efficiency (Marcos-Pastor et al., 2016).

Wang et al. proposed an interleaved PFC boost converter with an ASC to provide the ripple reduction and ZCT for the switching elements of the converter. With the developed ASC, the switching losses of the switching elements have been minimized and the diode reverse recovery losses have been removed. The working principle of the proposed converter is provided in detail. In addition, the performance results of the proposed design have been obtained from a 1kW experimental setup. The proposed design has achieved a 93.5% maximum efficiency (Wang et al., 2015a).

Wang et al. proposed an interleaved PFC boost converter with an ASC to provide the ripple reduction and ZVT for the switching elements of the converter. The switching losses of the switching elements have been minimized and also diode reverse recovery losses have been removed. The performance results of the

proposed design have been obtained from a 1kW experimental setup. The proposed design has reached the 97.5% maximum efficiency (Wang et al., 2015b).

Pahlevaninezhad et al. developed a novel control technique to control the input power of the AC-DC PFC converter, based on the differential flatness theory with the charging characteristics of the battery rather than the dc-bus voltage control. The dynamic behavior of the interleaved PFC boost converter has been enhanced with the proposed control technique. With the adaptive regulation of the DC-bus voltage to the load, a highly efficient dc-dc converter is carried out even poor load conditions. The performance of the developed control technique has been evaluated with results obtained from a 3 kW experimental setup. The presented converter has reached the 96.5% maximum efficiency (Pahlevaninezhad et al., 2012a).

Pahlevaninezhad et al. proposed a new control technique based on the Control-Lyapunov function for interleaved PFC boost converter. The proposed controller uses the input power instead of the output voltage as a control variable. Thus, it has been shown that the dynamic characteristic of the converter has been enhanced by removing the influence of the voltage controller on the current controller in the traditional PFC controller. The performance of the developed control technique has been evaluated by results obtained from a 3 kW experimental setup. The designed converter has reached a maximum efficiency of 96.5% (Pahlevaninezhad et al., 2012b).

Pahlevaninezhad et al. proposed a new soft-switched interleaved PFC boost converter topology. SS is provided by a passive snubber circuit. The performance of the developed control technique has been evaluated by results obtained from a 3 kW experimental setup. The proposed converter has reached the 98.5% maximum efficiency (Pahlevaninezhad et al., 2012c).

Gunasekaran and Thazhathu have proposed a digital control technique that uses a resettable integrator to provide a unity power factor. The control approach eliminates the effect of the input voltage and load variations better than linear

feedback control methods. The performance of the developed controller has been confirmed in the simulation environment and by experimental results obtained from a 300W setup. The proposed converter has reached 97% maximum efficiency (Gunasekaran and Thazhathu, 2017).

Musavi et al. proposed a novel BLIL PFC boost converter topology for the electric vehicle battery charging applications. The developed converter provided solutions to problems such as input bridge diode rectifier losses and EMI noise occurring in other topologies. The detailed operational analysis of the converter is provided in detail and verified by results obtained from a 3.4kW experimental setup. The proposed converter has reached 98.9% maximum efficiency at $265V_{rms}$ input voltage and 35% load condition (Musavi et al., 2011a).

Jeong et al. introduced a new soft-switched TPBL PFC boost converter topology. In the proposed converter, the soft-switching operation is provided by the inrush current limiter (ICL) circuit. It also resolved the reverse-recovery problems of converter switches. The fact that the ICL circuit can be integrated enables it to be designed in a smaller size than other SS circuits. The performance of the developed converter topology has been validated by the experimental results obtained from an 800W setup. The proposed converter has reached 97.81% maximum efficiency in the case of 230Vrms input voltage and 80% load (Jeong et al., 2020).

Yu et al. proposed a ZVT ASC for the totem pole PFC boost converter. This ASC circuit consisting of a small inductor and two switches enables ZVS operation for the converter switches. In addition, ZCS operation is provided for the ASC circuit. The performance of the designed ASC circuit has been validated by experimental results obtained from a 2.4kW setup. The presented converter has reached 98.35% maximum efficiency (Yu et al., 2019).

Fan et al. proposed a new hybrid PWM technique to minimize the zero-crossing current distortion in the TPBL PFC boost converter. With the proposed modulation technique, zero-crossing current distortion is effectively reduced,

without having a noticeable effect on power conversion efficiency compared to the traditional one. To observe the effect of the proposed modulation technique on the converter, experimental results are obtained from a 1kW setup (Fan et al., 2019).

Muhammad and Lu have developed a zero current switching TPBL PFC boost converter. Unlike existing studies, SS was performed with a small number of elements in the proposed topology. In addition, a controller combining traditional ACM controller with logic gates and phase detection element is designed to obtained high PF, proper input current form and wide soft-switching operating range. The detailed analysis of the developed converter is conducted and validated by experimental results (Muhammad and Lu, 2015).

Su et al. proposed a new TPBL PFC boost converter that operates in the boundary of the CCM and DCM operations, with features such as zero current detection and ZVS. The performance of the developed topology has been validated experimentally by a 350W setup. The presented converter has reached a 98.4% maximum efficiency (Su et al., 2011).

2.4. Summary

In this section, AC-DC PFC converter topologies used in the battery charging system in EVs and control techniques are addressed in detail. The performance of each topology is evaluated with case studies for load conditions at European efficiency standards. Moreover, AC-DC PFC converter topologies utilized in the battery charging system in EVs are explained by giving a survey of related literature. In light of the studies in the literature and the results of the simulation studies, the superior aspects of topologies and some deficiencies that are open to development are determined. Among the topologies, BLIL PFC boost topology stands out as the best topology in terms of efficiency and input and output characteristics. However, the fact that it contains more circuit elements compared to other topologies and requires a more complex control circuit are the biggest obstacles to the adoption of this topology. Among other topologies, traditional PFC

boost converter and interleaved PFC boost converter topology with low circuit number and simple controller structure are the most commonly used topology in the battery charging system of EVs. The major disadvantages of these topologies are that they have high switching losses and require a high volume output capacitor. Many studies have been done on these issues, but they have many shortcomings. In this thesis study, the solutions to these two issues have been provided by eliminating the shortcomings of the existing studies.

3. OVERVIEW OF SOFT SWITCHING TECHNIQUES

In this section, the concepts of switching, hard switching and SS are introduced first. Then, SS techniques developed for reducing the switching losses are explained in detail. At the end of this section, soft-switched AC-DC PFC converter studies in the literature are presented and discussed with their features such as power range, efficiency, number of circuit elements, cost and disadvantages.

3.1. The Switching Concept and Soft Switching

In its simplest terms, switching can be defined as changing the conduction state of a semiconductor switching element. The switching performed without an additional circuitry is called hard switching (HS). The HS causes some losses in the converters, such as switching losses due to overlap of the voltage and current of the switching element, reverse recovery losses of the diodes and discharge loss of the parasitic capacitance of the power switches. Also, during the HS process, high speed current and voltage rise cause higher EMI noises which adversely affect the control signals of the circuit. SS techniques have been introduced to solve these problems (Ting, 2016).

SS is defined as eliminating or minimizing the switching losses and EMI noises with additional circuitry. Additional circuitries that are designed to provide the SS and are not an essential part of the converters are called snubber cells. Snubber cells provide the functions of minimizing the current and voltage values to which semiconductor switching elements are exposed and decreasing the rate of the current and voltage rises. Snubber cells can create additional current and voltage on circuit elements and create additional switching and transmission losses. These losses should be minimized. In addition, the operating range of the snubber cell should be limited to the opening and closing times of the converter switches

and should not affect the operating modes of the converter. When choosing a snubber cell, the balance of all benefits and additional burdens is very important.

The basic functions expected from SS techniques can be listed as follows:

- To minimize or eliminate the coincidence of current and voltage during the switching of the semiconductor element.
- Providing a noise-free working environment by reducing EMI noise.
- To limit the rate of the current and voltage rises of the switching elements.
- Transferring the energy of the parasitic capacitance of the switch to the load.
- Increasing the efficiency of the converter.
- Reducing the diode reverse recovery losses.
- Maintaining the SS operation for all load conditions.
- To minimize the size and cost of the circuit.

Snubber cells are classified into two categories as active and passive. Passive snubber cells are simpler in nature and are the arrangements that do not require additional active power elements in the circuit. ZCS and/or ZVS techniques can only be achieved with passive snubber cells. Therefore, the switching losses in many passive snubber cells cannot be eliminated. ASCs can achieve ZVT and ZCT techniques, which are advanced SS techniques. In these techniques, it is ensured that switching losses are eliminated. Especially in the case of the semiconductor power element is MOSFET, ZVT techniques and in case of IGBT, ZCT techniques show favorable results.

3.2. Soft Switching Techniques

SS techniques are classified into four main categories such as ZVS, ZCS, ZVT and ZCT. The control signal of a semiconductor power element and the current and voltage graphs of hard switching and SS techniques are given in Figure 3.1.

3.2.1. Zero Voltage Switching (ZVS)

ZVS is a primitive SS technique performed during the turn off process of the semiconductor switching element. This technique is accomplished by connecting a small value parallel capacitor to the switching element. When the turn-off signal is applied, this capacitor limits the voltage increase rate of the switching element. The sudden rise of the voltage on the switch is prevented and it is allowed to the increasing gradually, as shown in Figure 3.1. As a result, the overlap of the voltage and current on the switch is reduced during the turn-off process, thus reducing the turn-off switching energy losses and transferring this energy to the parallel-connected capacitor. This energy in the capacitor is consumed through resistance or is recovered with some snubber cells (Moschopoulos, 2019).

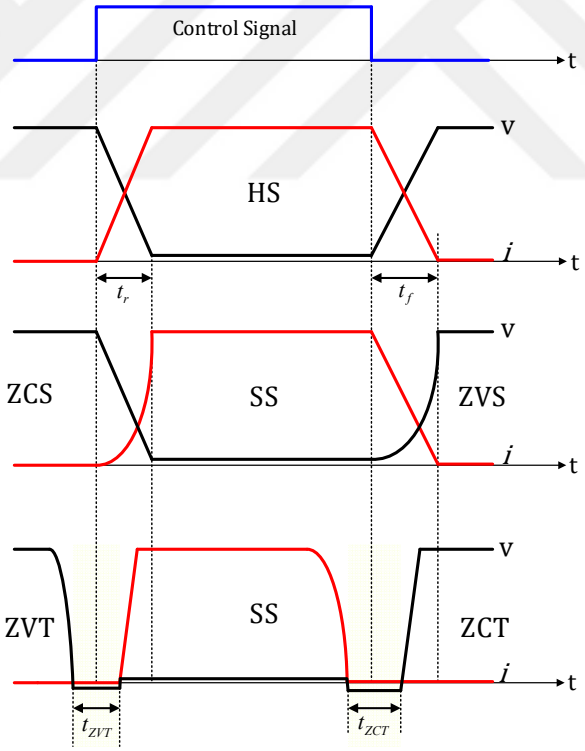

Figure 3.1. The control signal, current and voltage graphs of a switching element at HS and SS operations (Bodur, 2017)

3.2.2. Zero Current Switching (ZCS)

ZCS is a primitive SS technique performed during the turn-on process of the semiconductor switching element. This technique is accomplished by connecting a small series of inductance to the semiconductor switching element and this inductor limits the rate of the current rise passing through the switch as shown in Figure 3.1. When the switch is turned on, the amount of overlap between the voltage and current is reduced, so that the turn-on switching losses can be significantly reduced. This energy in the inductor is consumed through resistance or is recovered with some snubber cells (Moschopoulos, 2019).

In ZVS and ZCS methods, the switching energy losses cannot be eliminated. Therefore, these methods are also called approximate ZVS and approximate ZCS techniques. The inductor element connected in series to the switching element used for the ZCS is called the series snubber element, and the capacitor connected to the ends of the switching element for the ZVS is called the parallel snubber element. Inductor, which is a serial snubber element, causes additional voltage stress during turn-off on the switch, while the capacitor, which is used as a parallel snubber element, causes current stress during turn-on.

3.2.3. Zero Voltage Transition (ZVT)

ZVT is an advanced soft-switching technique that is performed during the turn-on of the semiconductor switching element, ensuring the elimination of switching losses. Before applying the turn-on signal, the voltage across the switch is dropped to zero with a short time partial resonance and kept at zero as shown in Figure 3.1. Meanwhile, by applying the turn-on signal, a perfect turn-on process is provided. As the voltage on the switching element is zero during the turn-on process, the coincidence of current and voltage is completely avoided and losses of turn-on switching are eliminated (Bodur, 2017).

This technique is carried out with ASCs containing an additional switch, and there is no specific circuit for this. Many snubber cells have been designed to implement this technique.

In this technique, since the parasitic capacitor of the switching element is fully discharged during the turn-on process, the application of this technique in converters using switching elements with high parasitic capacitance such as MOSFET provides serious advantages in terms of reducing losses and increasing power density.

3.2.4. Zero Current Transition (ZCT)

ZCT is an advanced SS technique that is realized during the turn-off of the semiconductor switching element, ensuring the elimination of switching losses. Before the trigger signal of the switching element is interrupted, the current passing through it is dropped to zero with a short time partial resonance and kept at zero as shown in Figure 3.1. Meanwhile, the control signal is interrupted, ensuring a perfect turn-off process. Since the current passing through the switching element during the turn-off process is zero, current and voltage coincidence are completely prevented and the turn-off switching losses are eliminated. This technique is carried out with ASCs like the ZVT technique (Cetin, 2011).

Since the switching losses in the turn-off process are eliminated with this technique, the use of the IGBT switching element in the studies performed with this technique provides important advantages for reducing losses and increasing the power density. Because during the turn-off of the IGBT switching element, a current called tail current and causing additional switching losses to occur. With this technique, losses due to this current in the turn-off process can also be eliminated.

3.3. Literature Survey of the Developed Soft Switching Techniques for AC-DC PFC Converters

In the literature, SS techniques have been applied in many areas after the first emergence in the 1980s and contributed to increasing the power density. AC-DC PFC converters in the battery charging system of EVs is the area was increasing the power density is the most important. Many passive and ASCs have been developed to perform the soft switching techniques in AC-DC PFC converters. The recent publications on soft switched AC-DC PFC converters are summarized in Table 3.1.

Table 3.1. The specifications of the developed soft switched AC-DC PFC converters

Ref.	Converter Topology	SS Technique	Power Range (W)	# of Aux. elements	Maximum Efficiency	Cost	Voltage stress	Current Stress
Kim et al., 2015	Traditional PFC Boost	ZVS, ZCS	3300	*L:2/C:2/ R:0/S:0/ D:5/T:0*	97%	M	✗	✗
Muhammad and Lu, 2015	TPBL PFC Boost	ZCS	400	*L:1/C:1/ R:0/S:0/ D:1/T:0*	96%	L	✗	✓
Pahlevaninezhad et al., 2012c	Interleaved PFC Boost	ZVS	3000	*L:1/C:1/ R:0/S:0/ D:0/T:0*	98.5%	M	✗	✗
Mahesh and Panda, 2012;	Traditional PFC Boost	ZVS, ZCS	500	*L:2/C:1/ R:0/S:0/ D:4/T:0*	97%	M	✓	✓
Cetin and Yenil, 2019	Bridgeless PFC Boost	ZVT	1000	*L:2/C:1/ R:0/S:1/ D:5/T:0*	97.4%	H	✗	✓
Yu et al., 2019	TPBL PFC Boost	ZVT	2400	*L:1/C:0/ R:0/S:2/ D:0/T:0*	98.35%	M	✓	✓
Cetin, 2018	Traditional PFC Boost	ZVT	1000	*L:2/C:2/ R:0/S:1/ D:4/T:0*	98%	M	✗	✓

Table 3.1. Continue

Kulasekaran and Ayyanar, 2018	Traditional PFC Boost	ZVT	3300	*L:1/C:1/ R:0/S:1/ D:2/T:0*	97.03%	L	✓	✓
Alam et al., 2017b	TPBL PFC Boost	ZVT	650	*L:1/C:2/ R:0/S:1/ D:1/T:0*	96.95%	L	✓	✓
Bodur and Yildirmaz, 2017	Traditional PFC Boost	ZVT	2000	*L:1/C:2/ R:0/S:1/ D:4/T:1*	97.4%	H	✗	✓
Hua et al., 2016	Bridgeless PFC Boost	ZVT	700	*L:1/C:4/ R:1/S:1/ D:4/T:1*	97.15%	H	✓	✗
Genc and Iskender, 2011	Interleaved PFC Boost	ZVT	600	*L:1/C:2/ R:0/S:1/ D:4/T:0*	96.12%	M	✗	✗
Tsai et al., 2011	Bridgeless PFC Boost	ZVT	600	*L:1/C:4/ R:1/S:1/ D:5/T:1*	97%	H	✗	✗
Mahdavi and Farzanehfard, 2009	Bridgeless PFC Boost	ZCT	500	*L:1/C:1/ R:0/S:1/ D:1/T:0*	97.6%	L	✗	✗
Ting et al., 2019	Traditional PFC Boost	ZVT, ZCT	600	*L:1/C:2/ R:0/S:1/ D:1/T:0*	95.7%	M	✗	✓
Sahin, 2018	Traditional PFC Boost	ZVT, ZCT	500	*L:1/C:2/ R:0/S:1/ D:3/T:1*	98.9%	H	✓	✓
Ting, 2018	Traditional PFC Boost	ZVT, ZCT	500	*L:2/C:2/ R:0/S:1/ D:1/T:0*	95.5%	L	✓	✗
Ting et al., 2016;	Interleaved PFC Boost	ZVT, ZCT	1500	*L:2/C:1/ R:0/S:1/ D:4/T:0*	N/A	M	✗	✗
Altıntaş, 2014	Traditional PFC Boost	ZVT, ZCT	500	*L:2/C:2/ R:0/S:1/ D:3/T:0*	97.9%	M	✗	✓
Akın and Bodur, 2011	Traditional PFC Boost	ZVT, ZCT	300	*L:1/C:2/ R:0/S:1/ D:4/T:1*	98%	H	✗	✓

L: inductor, C: capacitor, R: resistor, S: switch, D: diode, T: transformer, RL: relay
L: Low, M: Medium, H: High

Kim et al. proposed a passive snubber cell to achieve the ZVS and ZCS for the traditional PFC boost converter. The proposed snubber cell provided the turning on and off of the converter switch with ZCS, ZVS and minimized the reverse recovery current of the output diodes owing to the coupling effect of the coupled inductor in its structure. The validity of the proposed snubber cell was confirmed by experimental findings obtained from a 3.3kW design. The proposed circuit has achieved 97% maximum efficiency (Kim et al., 2015).

Muhammad and Lu proposed a soft switched TPBL PFC boost converter with a passive snubber cell. Thanks to the snubber cell consisting of inductor, capacitor and diode, ZCS is provided for the converter switches, but additional current stress has occurred on the converter switches. To verify the proof of concept, a 400W hardware prototype has been developed and tested. The presented converter has reached 96% maximum efficiency (Muhammad and Lu, 2015).

Pahlevaninezhad et al. presented a ZVS interleaved PFC boost converter for the battery charging system of EV. In the proposed converter, soft switching is carried out through a simple passive snubber cell consisting of the inductor and capacitor located between the two phases of the converter. While the converter switch is turned-on with ZVS, it is turned-off with hard switching. To evaluate the performance of the proposed design, a 3kW hardware converter is designed. The experimental results were compared with hard switched counterparts. The proposed converter has achieved 98.5% maximum efficiency (Pahlevaninezhad et al., 2012c).

Mahesh and Panda proposed a soft switched traditional PFC boost converter topology. With the proposed passive snubber cell, the converter switch is turned-on with ZCS and turned-off with ZVS. Also, ZCS and ZVS are provided for other elements. The proposed converter has 97% maximum efficiency (Mahesh and Panda, 2012).

Cetin and Yenil proposed a soft switched bridgeless PFC boost converter with an ASC. The designed ASC provided that the converter switch was switched

on with ZVT and switched off with ZVS. Also, the ASC switch and diodes are switched on with ZCS and switched off with ZVS. No voltage stress exists on any of the circuit elements, but some current stress has occurred on the snubber switch. The efficiency of the developed design has been tested by a configuration of 1kW in the simulation environment. The presented converter has a 97.4% maximum efficiency. The cost of the proposed ASC is high compared to other existing snubber cells (Cetin and Yenil, 2019).

Yu et al. proposed an ASC for the TPBL PFC boost converter, which operated with CCM. The proposed ASC consists of an inductor and two switches in parallel with the input inductor element. The ASC provides the ZVT operation for converter switches. Also, ZCS operation is ensured for the ASC switch. The small proportion of current and voltage stress has occurred for the circuit elements. The effectiveness of the proposed ASC has been confirmed by experimental results obtained from the 2.4 kW laboratory prototype. The proposed converter has reached the 98.35% maximum efficiency (Yu et al., 2019).

Cetin proposed a soft switched traditional PFC boost converter with ASC. ASC provides the converter switch to turn-on with ZVT and turn-off with ZVS. The diode of the converter turned on ZVS and turned off with ZCS. Also, turn on with ZCS and turn off with ZVS is provided for ASC switch. The efficiency of the proposed converter has been checked by the experimental tests of the 1kW prototype and it has reached 98% maximum efficiency (Cetin, 2018).

Kulasekaran and Ayyanar proposed a soft switched traditional PFC boost converter with ASC for the battery charging system in EVs. The ASC consist of an inductor, capacitance, diode and switch. The converter switch is turned on with ZVT and ASC switch is turned-off with ZCS. The efficiency of the proposed converter has been checked by the experimental tests of the 3.3kW prototype and it has reached 97.03% maximum efficiency (Kulasekaran and Ayyanar, 2018).

Alam et al. presented a novel soft switched TPBL PFC boost converter for battery charging applications. ZVT operation is provided for the converter switch

and ZVS operation is achieved for all switches. A 650W laboratory prototype has been constructed and tested. The constructed converter has exhibited a 96.95% maximum efficiency (Alam et al., 2017b).

Bodur and Yildirmaz proposed an ASC for traditional PFC boost converter operating in CCM. The ASC provides the ZVT to turn on and ZVS to turn off of the converter switch. Also, soft switching is provided for the switch and all other auxiliary diodes of the ASC circuit. The converter elements and ASC elements were not exposed to any extra voltage stress but, ASC switch subjected to a small proportion of current stress. The cost of the presented ASC is high compared to other existing snubber cells. The efficiency of the proposed converter has been checked by the experimental tests of the 2kW system. The 97.4% maximum efficiency is measured at full load condition (Bodur and Yildirmaz, 2017).

Hua et al. proposed a soft switched bridgeless PFC boost converter with ASC. With the designed ASC, the converter switch is switched on with ZVT, ASC switch is switched off with ZCS. The voltage stress occurred on the ASC switch. To verify the proof of concept, a 700W laboratory prototype has been constructed and tested. The 97.15% maximum efficiency is achieved (Hua et al., 2016).

Genc and Iskender developed a soft switched interleaved PFC boost converter. The proposed ASC provides the ZVT operation for the converter switch and soft-switching operation for all semiconductor elements. None of the semiconductor components is exposed to current and voltage stress. A 600W laboratory prototype has been constructed and tested. The presented converter has reached 96.12% maximum efficiency (Genc and Iskender, 2011).

Tsai et al. presented an ASC for a bridgeless PFC boost converter to reduce the switching losses. The proposed ASC ensures reducing the turn-on switching losses of the converter switch and turn-off switching losses of the ASC switch. None of the elements is exposed to any voltage stress but some current stress. The proposed design has a high cost compared to counterparts. A 600W laboratory prototype has been constructed and tested to validate the performance of the

proposed converter. The proposed concept has reached a 97% maximum efficiency (Tsai et al., 2011).

Mahdavi and Farzanehfard proposed a soft switched bridgeless PFC boost converter with ASC. The ASC provides the ZCT operation for the converter IGBT switch and also provides the soft switching operation for all semiconductor elements without any voltage and current stress. The efficiency of the proposed converter was checked by simulation tests and experimental data obtained from the 500W prototype. It has reached a 97.6% maximum efficiency.

Ting et al. developed an ASC for a traditional PFC boost converter to eliminate the switching losses. The converter switch is switched on with ZVT and switched off with ZVS. The switch of the ASC is switched on with ZCS and switched off with ZCT. None of the semiconductor elements is exposed to any voltage stress, but the ASC switch is exposed to a small proportion of current stress. Simulation and experimental studies have been carried out with a 600W design to validate the efficacy of the ASC. The proposed converter has achieved a 95.7% maximum efficiency (Ting et al., 2019).

Sahin proposed a novel soft switched traditional PFC boost converter with ASC, which combines the ZVT and ZCT SS techniques. With the designed ASC, the converter switch turned on with ZVT and turned off with ZCT. The ASC switch is turned-on and turned-off with ZCS. All of the semiconductors operate with SS. Thanks to the transformer in ASC, the switching energy is transferred to the output. Current and voltage stress did not occur in any of the converter elements. However, a small proportion of current and voltage stress occurred on ASC elements. The performance of the proposed design has been assessed by theoretical and experimental studies on a 500W design. The proposed converter has reached the 98.9% maximum efficiency (Sahin, 2018).

Ting proposed a fully soft switched traditional PFC boost converter with ZVT-ZCT snubber cell. The designed ASC provides the ZVT turn on and ZCT turn off for the converter switch. The converter diode turned-on with ZVS and turned

off with ZCS. Also, the ASC switch is turned on with ZCS and turned off with ZVS. None of the converter elements was subjected to current and voltage stress. However, a small proportion of voltage stress has occurred on the ASC switch. The performance of the designed converter has been verified by theoretical and experimental studies. It has reached a 95.5% maximum efficiency (Ting, 2018).

Ting et al. proposed an ASC for an interleaved PFC boost converter to minimize the switching losses. The proposed ASC provided ZVT for the turn on operation of the converter switches and ZCT for turn off operation. The converter diodes are turned on with ZVS and turned off with ZCS. Also, the ASC switch is turned on with ZCS and turned off with ZVS. The performance of the proposed converter is assessed with the 1.5kW design in the simulation environment (Ting et al., 2016).

Altıntaş proposed a soft switched traditional PFC boost converter with ASC, which combines the ZVT and ZCT techniques. The converter switch is turned-on with ZVT and turned-off with ZCT. All other semiconductor elements operate under SS. None of the semiconductor elements was subjected to any voltage stress, but the converter switch was subjected to a small proportion of current stress. The performance of the proposed design has been assessed by a 500W experimental setup. It has reached a 97.9% maximum efficiency (Altıntaş, 2014).

Bodur and Akın proposed an ASC for a traditional PFC boost converter. The proposed ASC combines the ZVT and ZCT techniques for reducing the switching losses. The converter switch is turned-on with ZVT and turned-off with ZCT. Also, the ASC switch is turned-on and turned-off with ZCS. The proposed converter has a high cost and contains a coupled inductor. The design of the coupled inductor is very important because it causes leakage inductor losses if not properly designed. The performance of the proposed converter has been confirmed by the results obtained from the 300W experimental setup. The proposed converter has reached a 98% maximum efficiency (Bodur and Akın, 2011).

3.4. Summary

In this section, SS techniques developed to reduce the switching losses of AC-DC PFC converters used in the battery charging system in EVs are addressed in detail. Passive snubber cells developed to perform ZVS and ZCS soft switching techniques, although they greatly reduced switching losses, were not able to eliminate them. In addition, current and voltage stress on the converter switch is transferred to passive snubber cell elements. Active snubber cells developed to perform ZVT and ZCT SS techniques have improved converter performance by eliminating switching losses. However, some of the developed ASCs have a high cost because they contain transformers, some of them contain coupled inductors and cause leakage inductor losses, and some of them have additional current and voltage stress on ASC elements. In this thesis study, a new active snubber cell will be proposed to overcome the aforementioned problems.

4. DESIGN AND ANALYSIS OF THE PROPOSED DVC FOR RIPPLE REDUCTION IN THE INTERLEAVED PFC BOOST CONVERTER

In this section, the design and analysis of the proposed DVC to reduce the output voltage ripple of the interleaved PFC boost converter are presented by providing information about the developed DVC circuit and its operating principles. Furthermore, the design procedure of the entire circuit is meticulously provided. The performance of the designed converter has been tested with various case studies in Matlab/Simulink simulation environment.

4.1. Introduction

The interleaved PFC boost converters stand out among the AC-DC PFC converters developed for battery charging systems in EVs, as they have low switching loss and EMI thanks to their interleaved structure. However, as they work in wide input voltage and wide output load range as in other topologies, high voltage ripple occurs at their outputs at nominal load values. They need large-sized filter capacitors to reduce this voltage ripple. This need is met by electrolytic capacitor technology, which has a shorter lifetime than other capacitor technologies. Reducing the voltage ripple at their output will allow this capacitor size to be reduced and the use of longer-life film capacitors. Many methods have been developed in the literature to reduce this ripple value. These methods are generally carried out using additional circuits or by modifying the switching technique. Of these methods, active power filters are realized with an auxiliary circuit connected in parallel to the filter capacitor (Kyritsis et al., 2007; Li et al., 2009; Pan and Zhang, 2015). Since it is connected parallel to the capacitor, a voltage as much as the output voltage falls on the auxiliary circuit elements. This causes an increase in the size of the elements to be used in the auxiliary circuit. Wang et al. and Li et al. have proposed a series voltage compensator circuit for reducing the ripple voltage in capacitor supported system and grid-tie solar inverter

(Wang et al., 2014; Liu et al., 2015). As the auxiliary circuit used in these methods does not operate dynamically, it has not been successful in reducing ripple under all load conditions.

In this study, a new DVC is developed for reducing the output voltage ripple of the interleaved PFC boost converter. Since the DVC circuit is connected to the load in series, a low voltage falls on it, so the size of the elements to be used in its structure is small. Also, this compensator has a simple structure. This compensator aims to reduce the voltage ripple on the capacitor by creating a reverse voltage as much as the amount of voltage ripple on the capacitor. The proposed compensator has a dynamic operating principle and provides to keep the output voltage ripple under 0.5V at all load conditions. In addition, the DVC allows the converter input current THD to be reduced. Thus, the additional current and voltage stress on the converter elements are decreased and converter efficiency is increased. The power density of the designed interleaved PFC boost converter with the developed DVC has been increased. The proposed converter operates in the universal input voltage range and the input current THD values are compatible with the range given in IEC 61000-3-2 standards.

Steady-state operating principles, design criteria and the performance results of the proposed converter are presented in the following sections.

4.2. Descriptions of the Proposed Converter with Developed DVC

The proposed interleaved AC-DC PFC boost converter with developed DVC circuit is illustrated in Figure 4.1. This converter consists of two-part such as the main circuit and auxiliary DVC circuit. V_i is grid voltage, V_{out} is the output voltage, S_{i1} and S_{i2} is the main switches, D_{i1} and D_{i2} is the main diodes, D_1-D_4 are the bridge rectifier diodes, L_{i1} and L_{i2} are the main circuit inductance, C_{dc} is filter capacitance, in the main circuit. In the DVC circuit, L_C illustrates the filter inductance, C_C corresponds to the filter capacitance, Q_1-Q_4 are the auxiliary switches, V_{dc} is the variable dc input voltage.

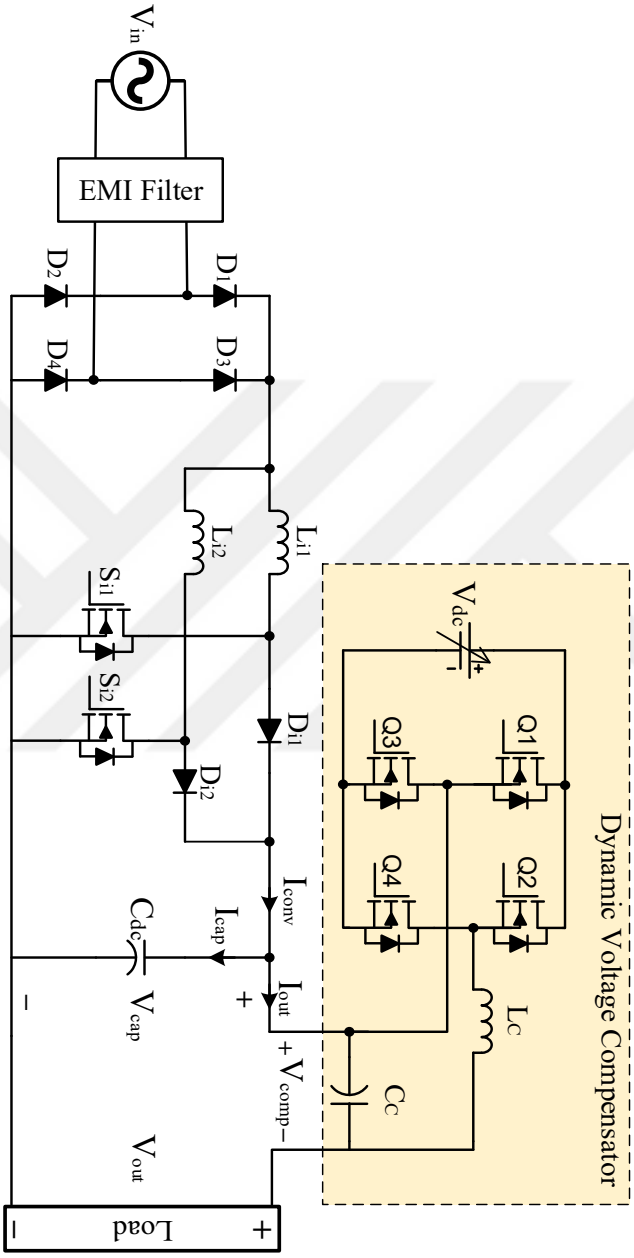

Figure 4.1. The proposed interleaved PFC boost converter with developed DVC

As a controller of the main circuit, the average current mode control method is used, which is a well-known and effective method as illustrated in Figure 4.2. This controller consists of two parts, such as voltage control and current control loops. Firstly, the output voltage (V_{out}) is compared to the reference voltage (V_{out}*) and passed through a PI controller. Then, the signal generated at the output of the PI controller is multiplied by the sensed input voltage (V_{in}) with a phase-locked loop (PLL) and the current reference (I_{ref}) is created. Finally, the generated reference current (I_{ref}) and the inductor currents (I_{Li1}, I_{Li2}) are compared and passed through a PI controller to generate the switching signal of the main switch.

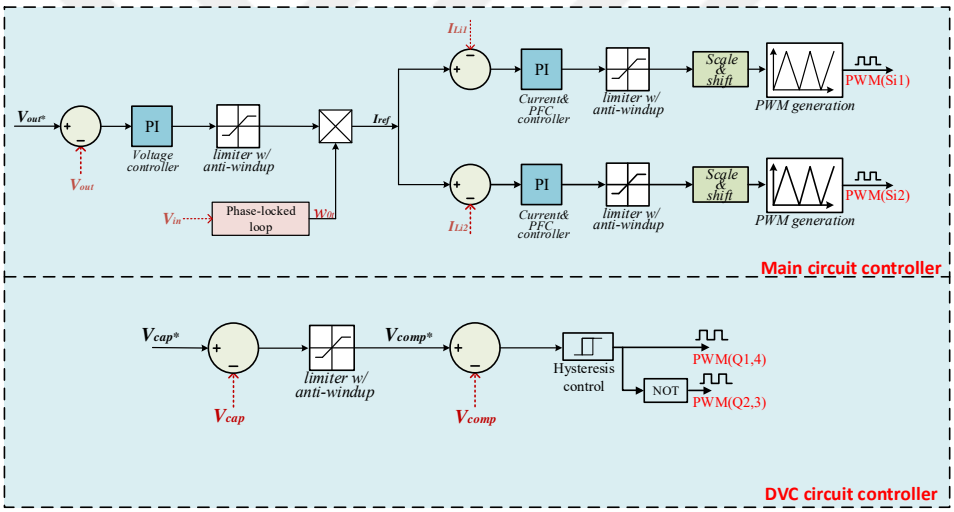

Figure 4.2. Controller of the proposed converter with developed DVC

The control of the DVC circuit is carried out with a hysteresis control technique as shown in Figure 4.2. The gate signals of the switches of the DVC circuit are generated with a bipolar switching technique. Firstly, the capacitor voltage V_{cap} is sensed and compared with a reference voltage value V_{cap}*. Then, the produced error signal is passed through a limiter and a V_{comp}* reference signal is created. Sensed V_{comp} voltage compared with reference signal V_{comp}*. The generated error signal passed through hysteresis control and pulse-width

modulation (PWM) signals are generated. The generated PWM signals have triggered the switches of the DVC circuit.

4.3. Steady-State Operating Principles of the Proposed Converter

The operation states of the proposed converter are the same for the positive and negative cycles of the AC input voltage. For each cycle, where the duty cycle is greater than or less than 0.5, it is determined separately.

For D>0.5, each circuit of the operating states and the current graphs of the operating states are given in Figure 4.3 and Figure 4.4, respectively. The operating cycle of the added DVC circuit is designed not to affect the operating cycle of the main circuit.

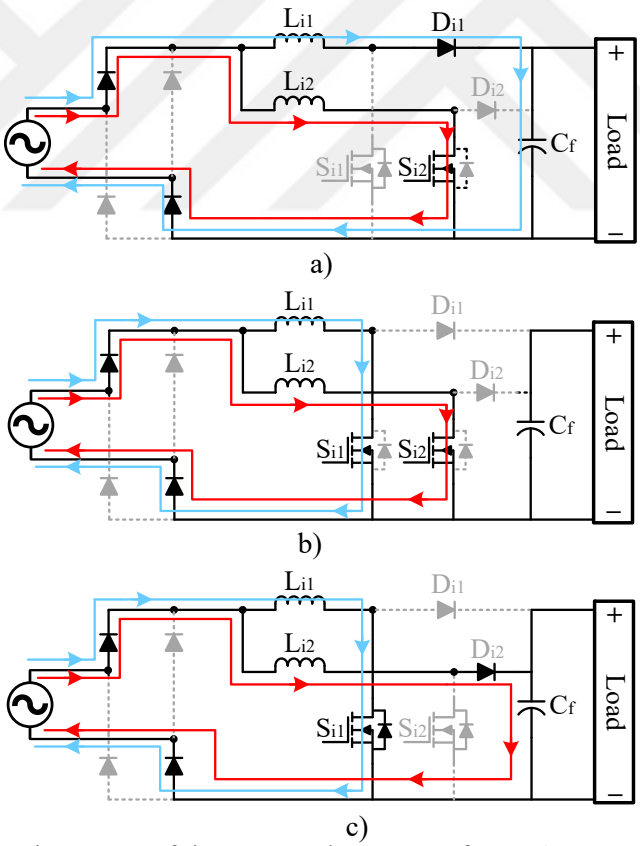

Figure 4.3. Operating states of the proposed converter for D>0.5

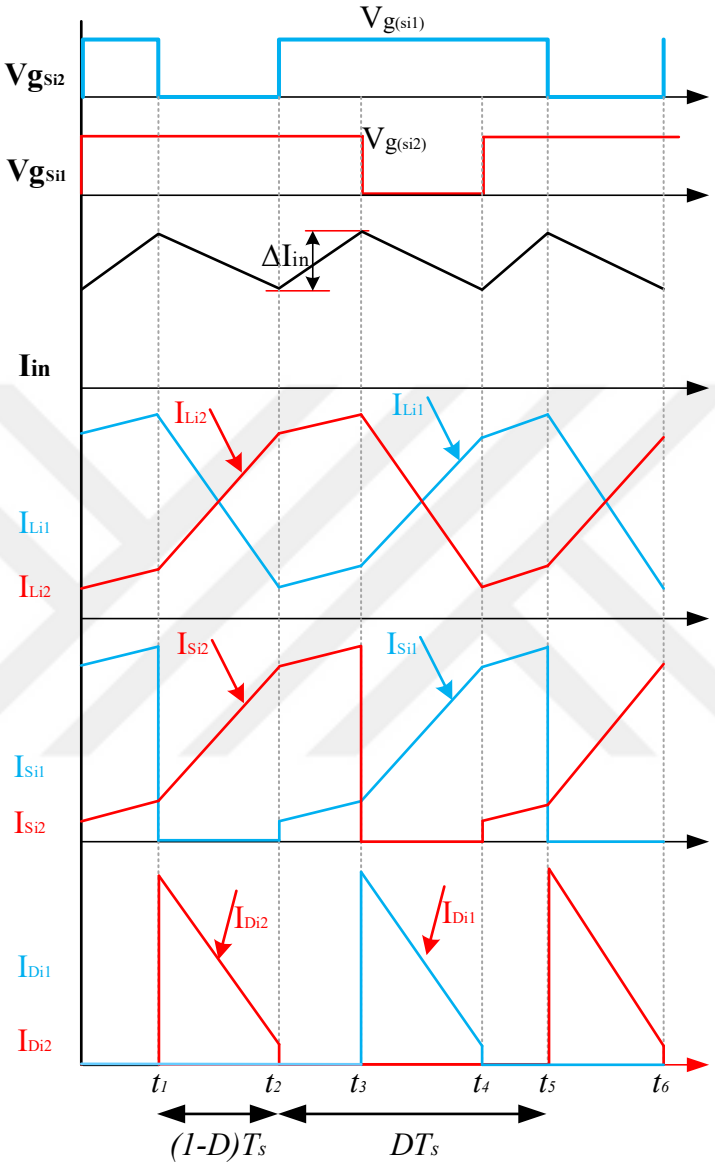

Figure 4.4. The current graphs of the operating states for D>0.5

State 1 ($t_1<t<t_2$)**:** At the beginning of this state, S_{i1} switch is turned-off and S_{i2} switch is turned on as shown in Figure 4.3(a). In this state, the energy stored on L_{i1} is transferred to the load via D_{i1} diode and the current on L_{i1} decreases linearly.

The L_{i2} inductor charges through the S_{i2} switch, and the energy induced on it increases. The corresponding equations for the L_{i1} and L_{i2} are given as follows:

$$\Delta i_{Li1} = \frac{1}{L_{i1}}\left(V_{out} - V_{in}\right)\left(1-D\right)T_s \tag{4.1}$$

$$\Delta i_{Li2} = \frac{1}{L_{i2}}V_{in}\left(1-D\right)T_s \tag{4.2}$$

where L_{i1} and L_{i2} are the main circuit inductors, ΔL_{i1} and ΔL_{i2} are the current changes of the L_{i1} and L_{i2} inductors, V_{out} is the output voltage, D is the duty ratio, T_s is the switching frequency.

Input current ripple of the converter is calculated as follows:

$$\Delta i_{in} = \Delta i_{Li1} + \Delta i_{Li2} \tag{4.3}$$

State 2 **($t_2<t<t_3$, $t_4<t<t_5$):** At the beginning of this state, S_{i1} switch is turned-on and S_{i2} switch continues to flow current as shown in Figure 4.3(b). In this state, L_{i1} and L_{i2} inductors charge through S_{i1} and S_{i2}, respectively. The current of the L_{i1} and L_{i2} increase linearly and the corresponding equations for the L_{i1} and L_{i2} are given as follows:

$$\Delta i_{Li1} = \frac{1}{L_{i1}}V_{in}\left(D-\frac{1}{2}\right)T_s \tag{4.4}$$

$$\Delta i_{Li2} = \frac{1}{L_{i2}}V_{in}\left(D-\frac{1}{2}\right)T_s \tag{4.5}$$

State 3 **($t_3<t<t_4$):** At the beginning of this state, S_{i2} switch is turned-off and S_{i1} switch continues to flow current as shown in Figure 4.3(c). In this state, the energy stored on L_{i2} is transferred to the load via D_{i2} diode and the current on L_{i2} decreases linearly. The L_{i1} inductor charges through the S_{i1} switch, and the energy induced on it increases. The corresponding equations for the L_{i1} and L_{i2} are given as follows:

$$\Delta i_{Li1} = \frac{1}{L_{i1}}V_{in}\left(1-D\right)T_s \tag{4.6}$$

$$\Delta i_{Li2} = \frac{1}{L_{i2}}(V_{out} - V_{in})(1-D)T_s \tag{4.7}$$

For D<0.5, each circuits of the operating states and the current graphs of the operating states are given in Figure 4.5 and Figure 4.6, respectively.

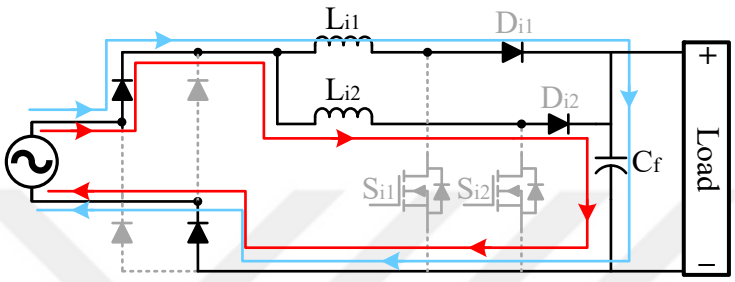

Figure 4.5. Operating states of the proposed converter for D<0.5

For D>0.5, each circuit of the operating states and the current graphs of the operating states are given in Figure 4.3 and Figure 4.4, respectively.

State 1 **($t_1<t<t_2$, $t_3<t<t_4$):** At the beginning of this state, S_{i1} and S_{i2} switches are turned-off as shown in Figure 4.5. In this state, the energy stored on L_{i1} and L_{i2} is transferred to the load via D_{i1} and D_{i2} diodes, respectively. L_{i1} and L_{i2} currents decrease linearly and these current can be calculated as follows:

$$\Delta i_{Li1} = \frac{1}{L_{i1}}(V_{out} - V_{in})\left(\frac{1}{2} - D\right)T_s \tag{4.8}$$

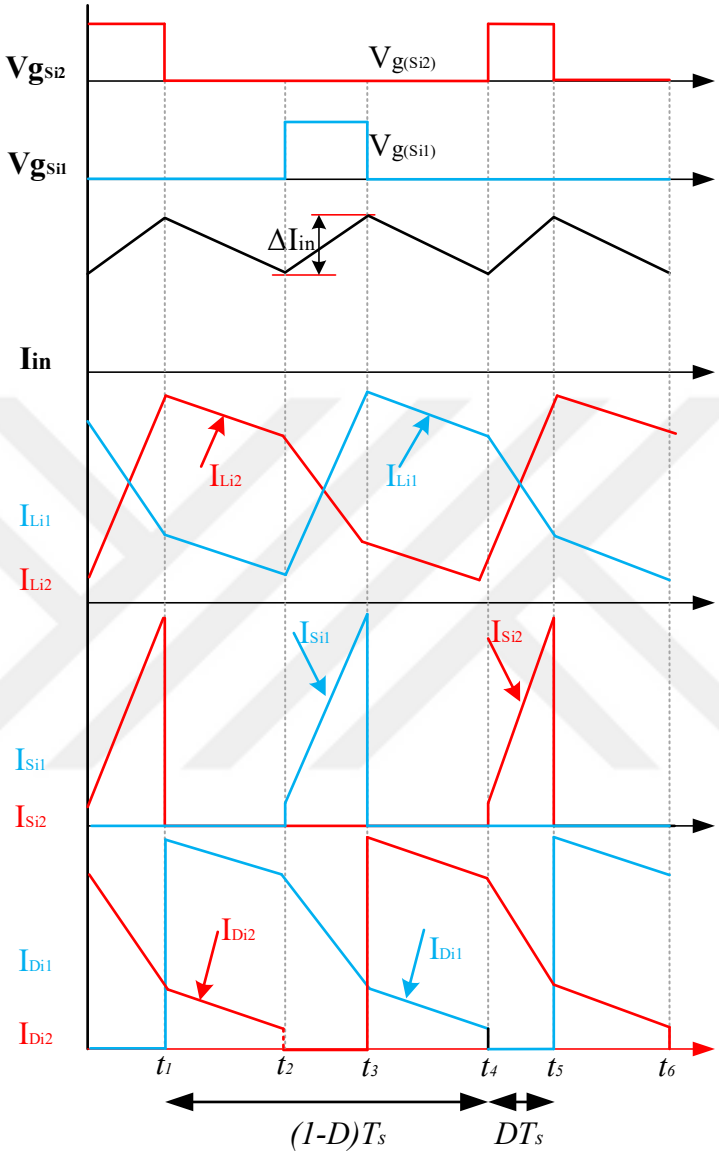

Figure 4.6. The current graphs of the operating states for D<0.5

$$\Delta i_{Li2} = \frac{1}{L_{i2}}\left(V_{out} - V_{in}\right)\left(\frac{1}{2} - D\right)T_s \tag{4.9}$$

State 2 ($t_2<t<t_3$): At the beginning of this state, S_{i2} switch begins the flowing current and S_{i1} switch is still in cut-off condition. This state is similar to state 1 at D>0.5 in terms of switch states. But the amount of change of inductor ripple currents is different from each other. The corresponding equations for the calculation of the current of the L_{i1} and L_{i2} inductors are given as follows:

$$\Delta i_{Li1} = \frac{1}{L_{i1}}\left(V_{out} - V_{in}\right)DT_s \tag{4.10}$$

$$\Delta i_{Li2} = \frac{1}{L_{i2}}V_{in}DT_s \tag{4.11}$$

State 3 ($t_4<t<t_5$): At the beginning of this state, S_{i1} switch is turned on and the S_{i2} switch is turned off. This state is similar to state 3 at D>0.5 in terms of switch states. The current of the L_{i1} inductor and the energy induced on it increase linearly. The current of the L_{i2} inductor decreases linearly and the energy stored on the L_{i2} inductor is transferred to the load via D_{i2} diode. The corresponding equations for the calculation of the current of the L_{i1} and L_{i2} inductors are given as follows:

$$\Delta i_{Li1} = \frac{1}{L_{i1}}V_{in}DT_s \tag{4.12}$$

$$\Delta i_{Li2} = \frac{1}{L_{i2}}\left(V_{out} - V_{in}\right)DT_s \tag{4.13}$$

4.4. Performance Results

To evaluate the performance of the proposed interleaved PFC boost converter with developed DVC, a 3.3kW system has been designed and tested with three different case studies in the MATLAB/Simulink environment. The simulation parameters of the designed system are given in Table 4.1.

Table 4.1. Simulation parameters of the proposed converter

Parameter	**Symbol**	**Value**
Output power	P_{out}	3300W
Input voltage	V_{in}	85-265V_{rms}
Output voltage	V_{out}	400V
Switching frequency	f_{sw}	70kHz
Interleaved inductors	L_{i1}, L_{i2}	150uH
Output filter capacitor	C_o	984uF
DVC inductor	L	1uH
DVC capacitor	C	33uF
Sample time of the simulation	t_s	0.1us
Proportional constant (voltage controller)	K_p^v	0.03
Integral constant (voltage controller)	K_i^v	5
Proportional constant (current controller)	K_p^c	1.5
Integral constant (current controller)	K_i^c	3
Hysteresis band value of the DVC controller	Δx	0.2

In the first of the case studies, the performance results of the converter at 220V_{rms} input voltage are presented for six different load conditions in European efficiency standards as given in Table 4.2. Input voltage and current graphs of the proposed converter are presented to show that the unity power factor of the converter is achieved, and THD results of the input current are provided to show that they are compatible with the THD values in the standards. The output voltage graphs of the proposed converter with DVC and without DVC are presented in separate graphs for each load case to show the effect of the developed DVC circuit on the converter output voltage ripple. In addition, the efficiency, power factor, THD, output voltage ripple results of the converter with DVC and without DVC were compared with graphics for all load cases. In the second of the case studies, the same procedure was repeated for the input voltage of 110V_{rms}. In the third of

the case studies, the converter's performance has been validated in case of disturbances on the network side under six different load cases.

Table 4.2. Load conditions at European efficiency standards

States	State 1	State 2	State 3	State 4	State 5	State 6
Values	%100 Load	%50 Load	%30 Load	%20 Load	%10 Load	%5 Load

Finally, the overall efficiency of the converter is calculated according to the European efficiency standards by the following formula:

$$EU\eta = 0.03\eta_{\%5} + 0.06\eta_{\%10} + 0.13\eta_{\%20} + 0.1\eta_{\%30} + 0.48\eta_{\%50} + 0.2\eta_{\%100} \quad (4.14)$$

4.4.1. Case I

In this case, the performance of the proposed converter has been tested for V_{in}=220V_{rms} under six different load conditions given in European efficiency standards. Figure 4.7 represents the input current and voltage graphs of the proposed converter with developed DVC under six different load conditions. It can be clearly seen from the figure that the proposed converter has achieved nearly unity power factor from light load to full load condition. Also, it is noted that input current harmonics (THD) of the proposed converter is lower than 5% from half load to full load and it is compliant with the IEC 61000-3-2 standards. Figures 4.8-13 illustrate the output voltage graph of the proposed converter with and without developed DVC under six different load conditions for V_{in}=220V_{rms}. It is clearly seen from the figures that the output voltage ripple of the converter proposed with the developed DVC is reduced to below 0.5V in all load cases. Figure 4.14 shows the efficiency curves of the proposed converter with and without developed DVC for different load conditions. It is obvious that developed DVC has increased converter efficiency. The maximum efficiency of the proposed converter has increased from 94.11% to 96.75%. The overall efficiency of the proposed converter

according to European efficiency standards is increased from 93.09% to 95.87%. The reason for the increase in efficiency is the reduction of current and voltage stress on the circuit elements. In Figure 4.15, the power factor results of the proposed converter are provided for all load conditions. It can be seen from the figure that developed DVC has improved the PFC capability of the converter. With the developed DVC, 0.9999 power factor has been achieved at full load condition. Figure 4.16 shows the input current THD results of the proposed converter. It can be observed that input current THD value is decreased from 2.23% to 0.92% at full load condition. In addition, the proposed converter has low input current THD values in all other load cases. The output voltage ripple results of the proposed converter with and without developed DVC are provided in Figure 4.17. It is clear from the figure that the ripple value is kept below 0.5 V in all load cases. In Table 4.3, the comparison of the performance results of the proposed converter with and without developed DVC under six different load conditions are given in detail. It can be concluded from the table that the developed DVC improves converter performance under all load conditions.

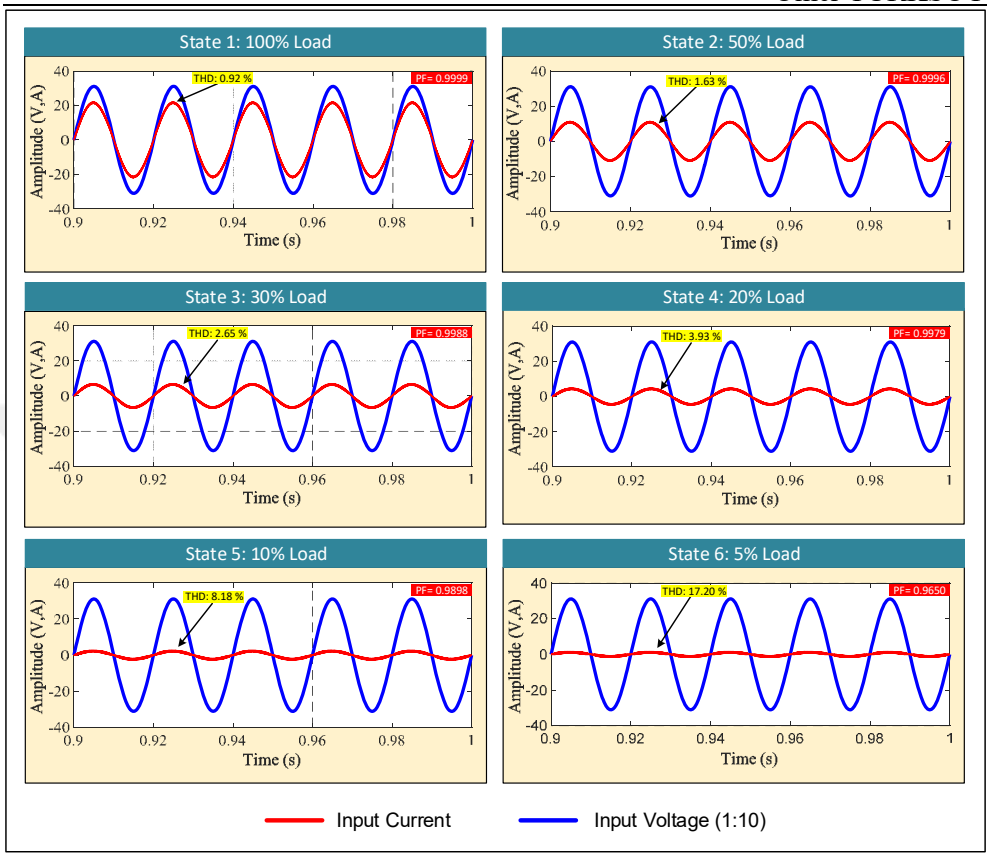

Figure 4.7. The input current and voltage graphs with developed DVC at different load conditions (V_{in}=220V_{rms})

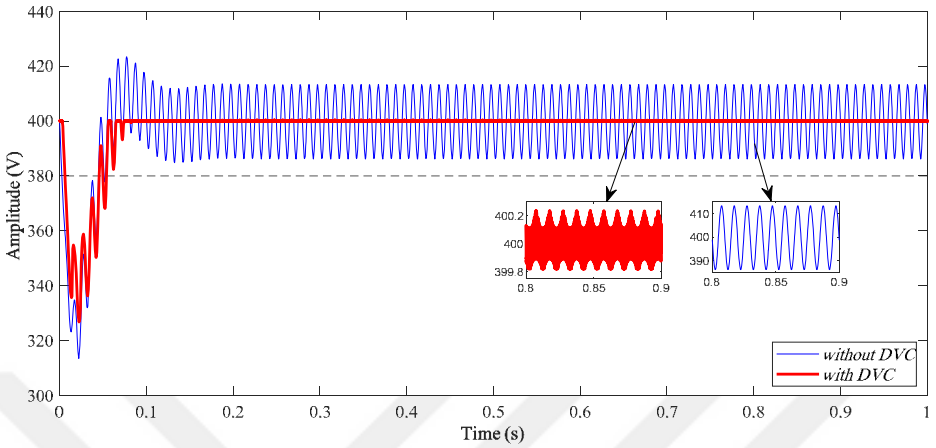

Figure 4.8. The output voltage graphs with and without developed DVC for state 1 (V_{in}=220V_{rms})

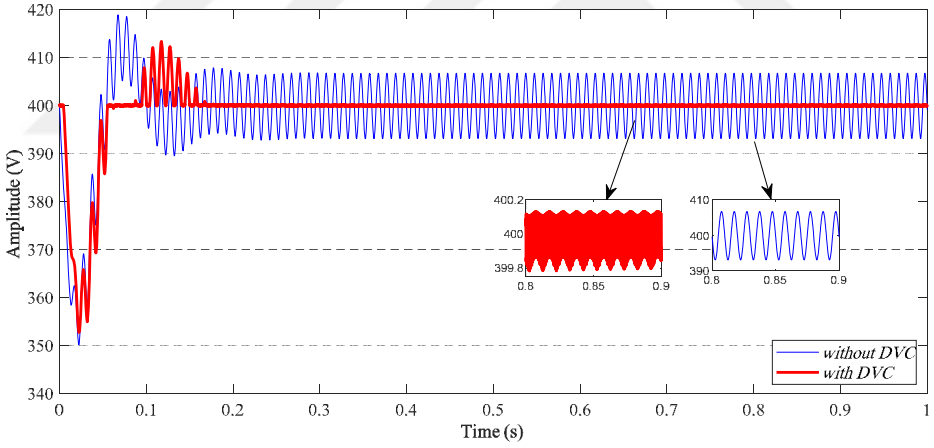

Figure 4.9. The output voltage graphs with and without developed DVC for state 2 (V_{in}=220V_{rms})

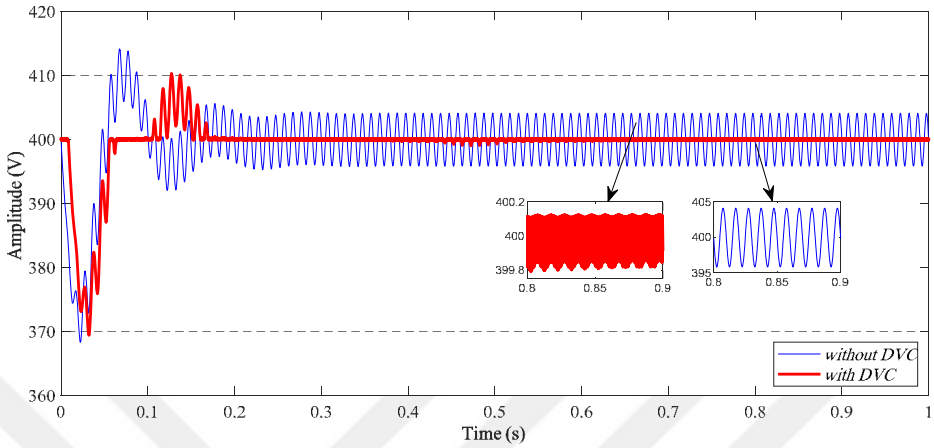

Figure 4.10. The output voltage graphs with and without developed DVC for state 3 (V_{in}=220V_{rms})

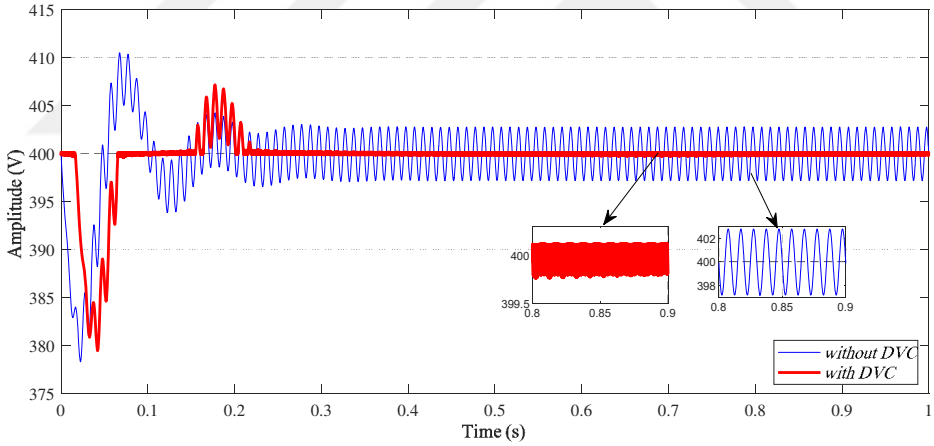

Figure 4.11. The output voltage graphs with and without developed DVC for state 4 (V_{in}=220V_{rms})

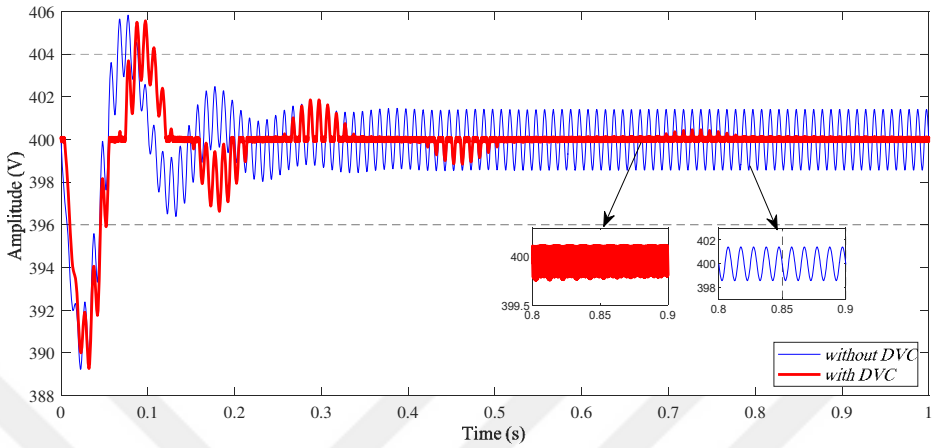

Figure 4.12. The output voltage graphs with and without developed DVC for state 5 (V_{in}=220V_{rms})

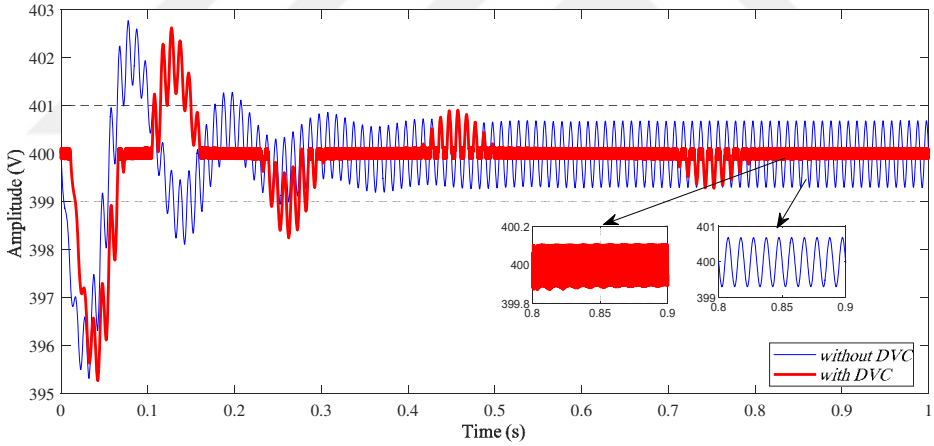

Figure 4.13. The output voltage graphs with and without developed DVC for state 6 (V_{in}=220V_{rms})

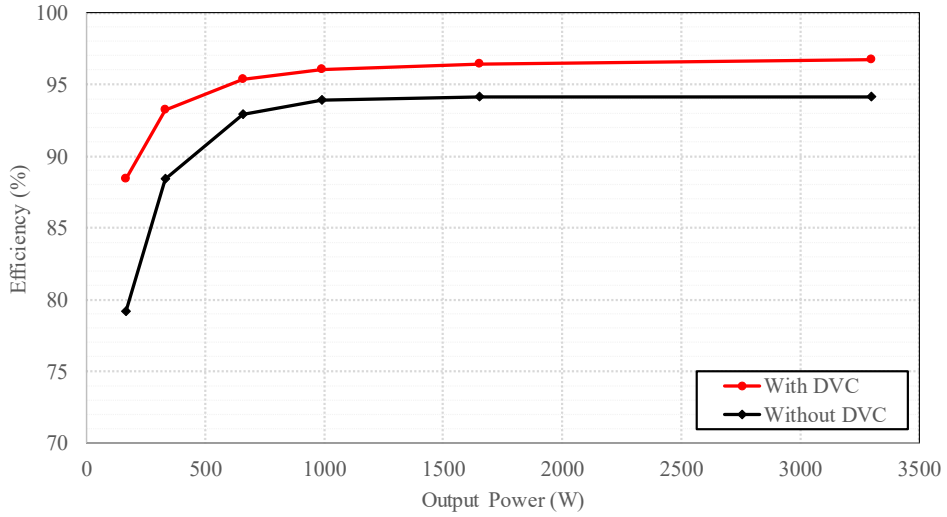

Figure 4.14. The efficiency curves with and without developed DVC at different load conditions (V_{in}=220V_{rms})

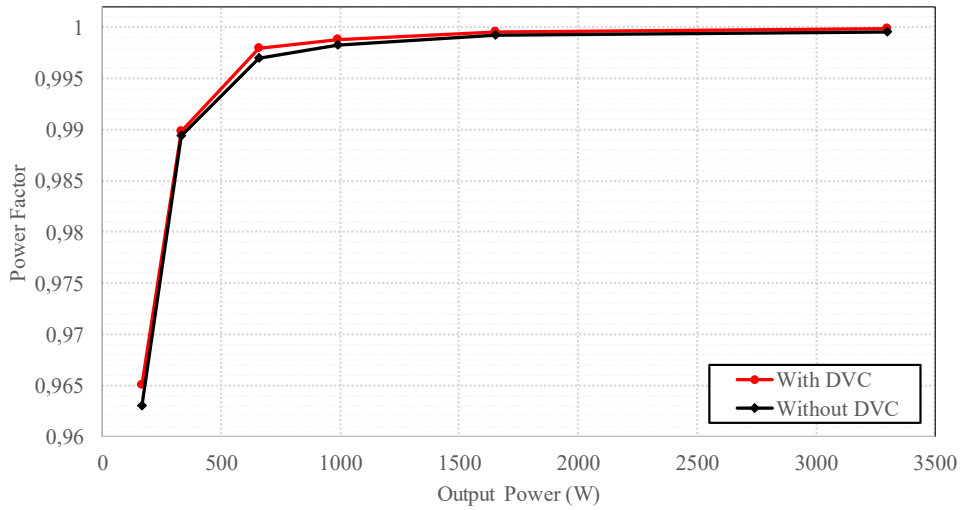

Figure 4.15. The PF results with and without developed DVC at different load conditions (V_{in}=220V_{rms})

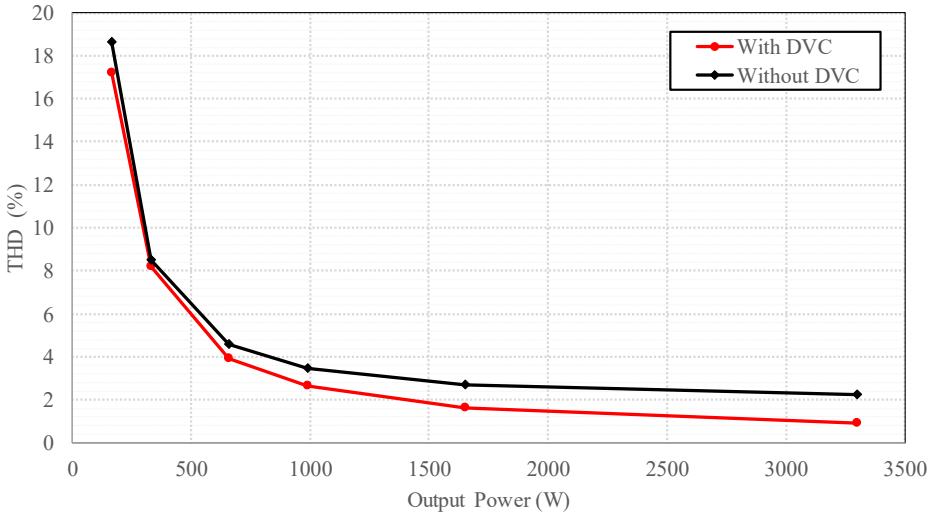

Figure 4.16. The input current THD results with and without developed DVC at different load conditions (V_{in}=220V_{rms})

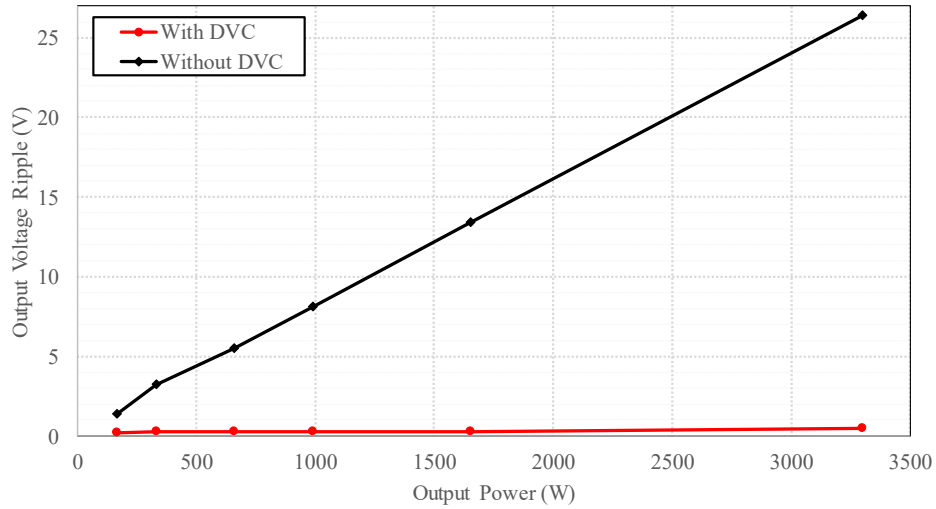

Figure 4.17. The output voltage ripple with and without developed DVC at different load conditions (V_{in}=220V_{rms})

Table 4.3. The performance results with and without developed DVC under six different load conditions (V_{in}=220V_{rms})

States	Efficiency		THD		Output Voltage Ripple	
	Traditional	Proposed	Traditional	Proposed	Traditional	Proposed
State 1	94.11%	96.75%	2.23%	0.92%	26.4V	0.50V
State 2	94.01%	96.41%	2.68%	1.63%	13.4V	0.30V
State 3	93.90%	96.02%	3.46%	2.65%	8.1V	0.30V
State 4	92.87%	95.37%	4.60%	3.93%	5.5V	0.25V
State 5	88.42	93.22%	8.50%	8.18%	3.2V	0.25V
State 6	79.18%	88.42%	18.65%	17.20%	1.4V	0.20V

4.4.2. Case II

In this case, the performance of the proposed converter has been tested for V_{in}=110V_{rms} under six different load conditions given in European efficiency standards. Figure 4.18 represents the input current and voltage graphs of the proposed converter with developed DVC under six different load conditions. It can be clearly seen from the figure that the proposed converter has achieved nearly unity power factor from light load to full load condition. Also, it is noted that input current harmonics (THD) of the proposed converter is lower than 5% from half load to full load and it is compliant with the IEC 61000-3-2 standards. Figures 4.19-24 illustrate the output voltage graph of the proposed converter with and without developed DVC under six different load conditions for V_{in}=110V_{rms}. It is clearly seen from the figures that the output voltage ripple of the converter proposed with the developed DVC is reduced to below 0.4V in all load cases. Figure 4.25 shows the efficiency curves of the proposed converter with and without developed DVC for different load conditions for V_{in}=110V_{rms}. It is obvious that developed DVC has increased converter efficiency. The maximum efficiency of the proposed converter has increased from 93.2% to 95.4%. The overall efficiency

of the proposed converter according to European efficiency standards is increased from 90.77% to 93.77%. The reason for the increase in efficiency is the reduction of current and voltage stress on the circuit elements. In Figure 4.26, the power factor results of the proposed converter are provided for all load conditions. It can be seen from the figure that developed DVC has improved the PFC capability of the converter. With the developed DVC, 0.9999 power factor has been achieved at full load condition. Figure 4.27 shows the input current THD results of the proposed converter. It can be observed that input current THD value is decreased from 2.07% to 0.72% at full load condition. In addition, the proposed converter has low input current THD values in all other load cases. The output voltage ripple results of the proposed converter with and without developed DVC are provided in Figure 4.28. It is clear from the figure that the ripple value is kept below 0.4 V in all load cases. In Table 4.4, the comparison of the performance results of the proposed converter with and without developed DVC under six different load conditions are given in detail. It can be concluded from the table that the developed DVC improves converter performance under all load conditions.

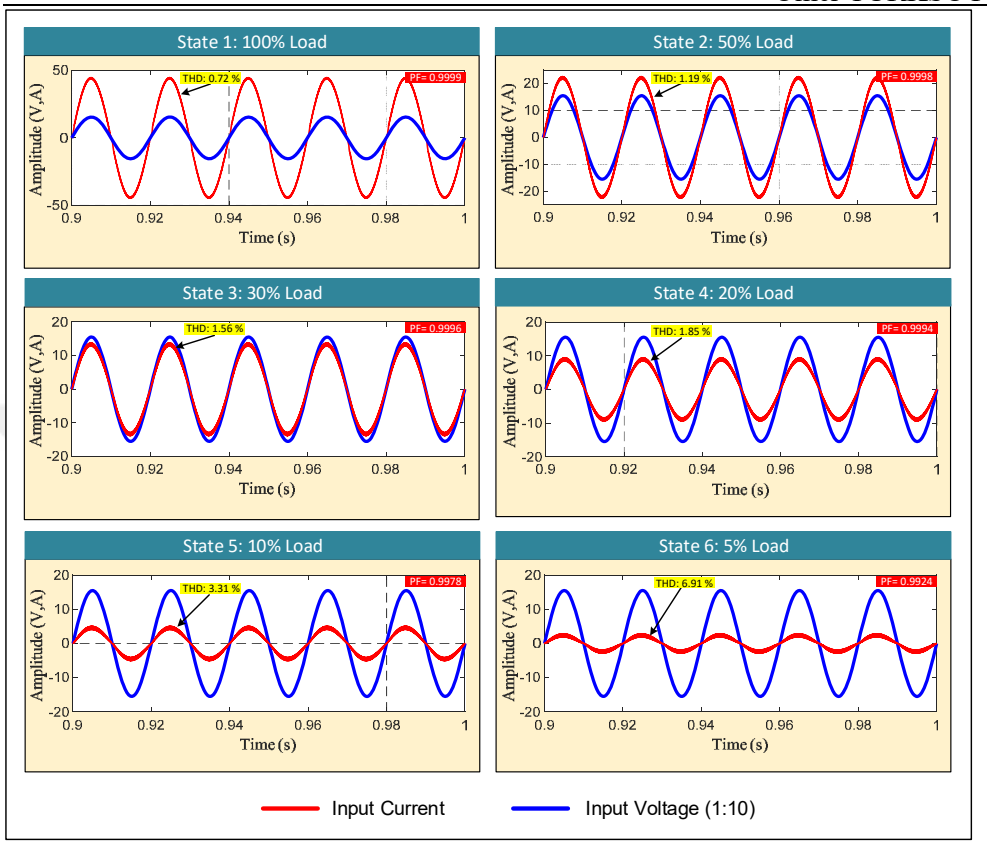

Figure 4.18. The input current and voltage graphs with developed DVC at different load conditions (V_{in}=110V_{rms})

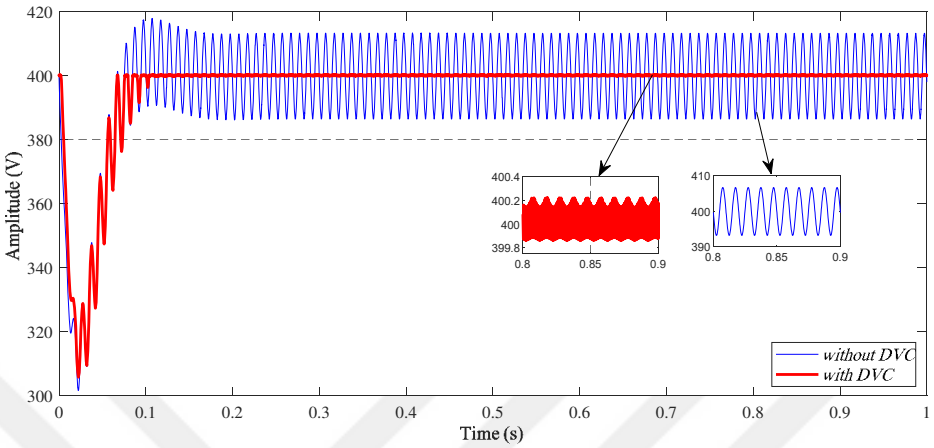

Figure 4.19. The output voltage graphs with and without developed DVC for state 1 (V_{in}=110V_{rms})

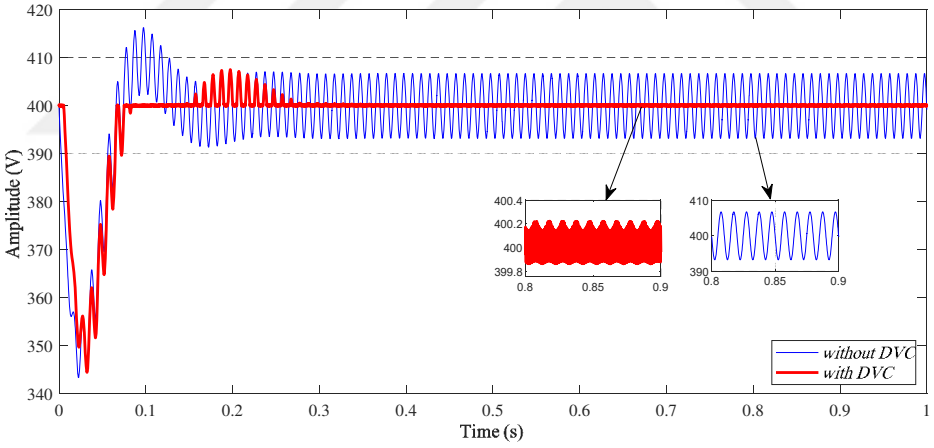

Figure 4.20. The output voltage graphs with and without developed DVC for state 2 (V_{in}=110V_{rms})

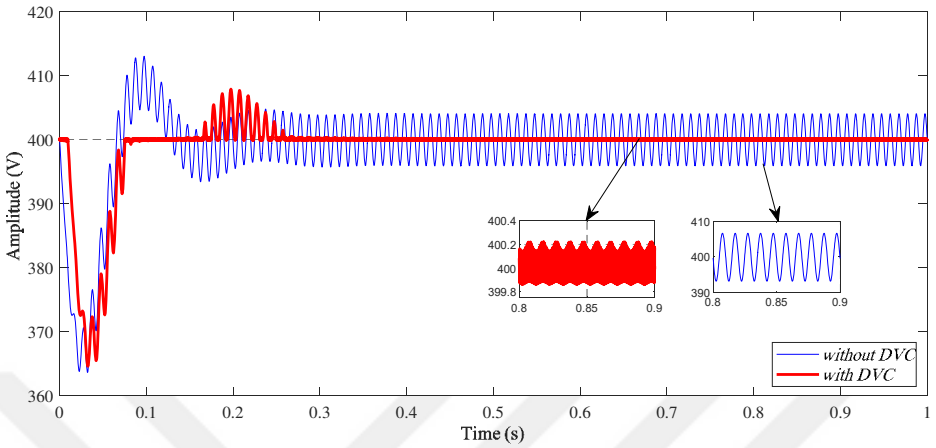

Figure 4.21. The output voltage graphs with and without developed DVC for state 3 (V_{in}=110V_{rms})

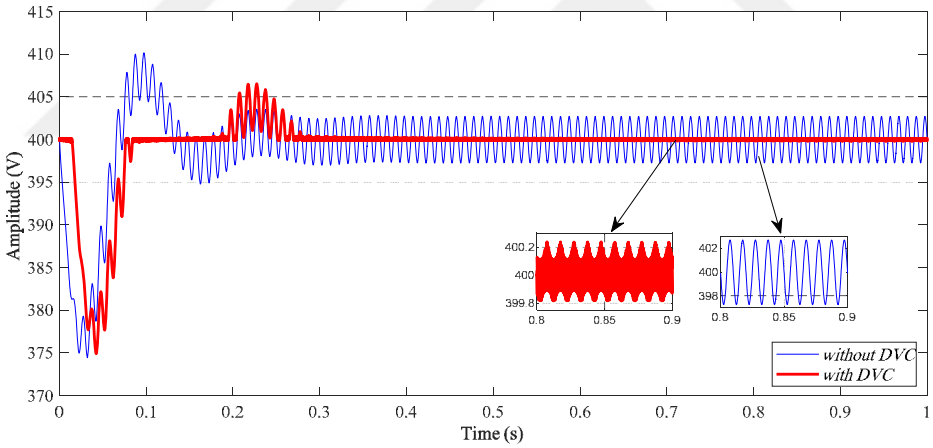

Figure 4.22. The output voltage graphs with and without developed DVC for state 4 (V_{in}=110V_{rms})

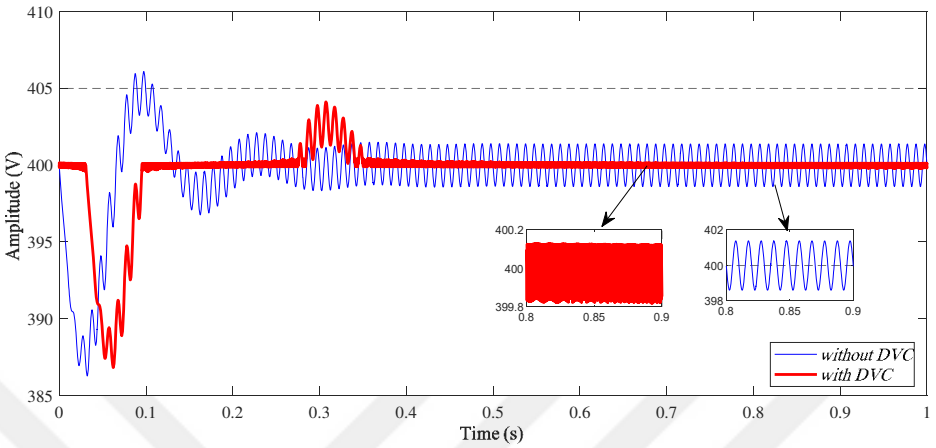

Figure 4.23. The output voltage graphs with and without developed DVC for state 5 (V_{in}=110V_{rms})

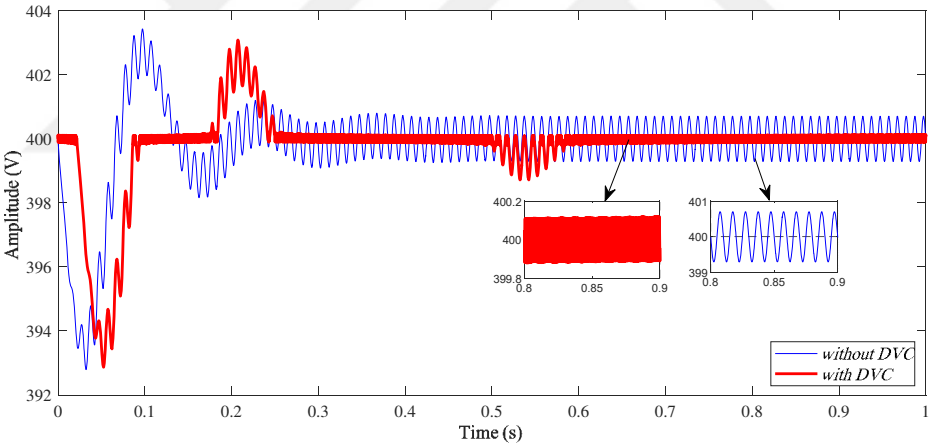

Figure 4.24. The output voltage graphs with and without developed DVC for state 6 (V_{in}=110V_{rms})

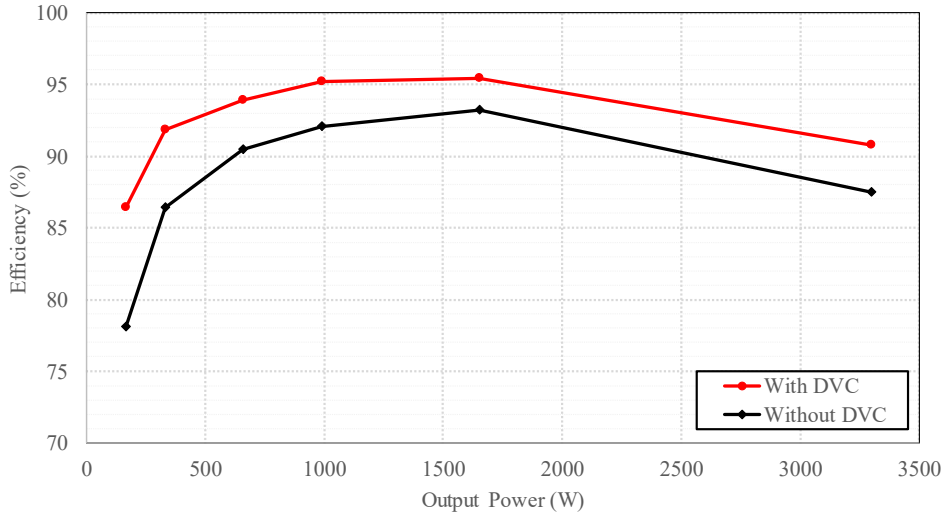

Figure 4.25. The efficiency curves with proposed and without developed DVC at different load conditions (V_{in}=110V_{rms})

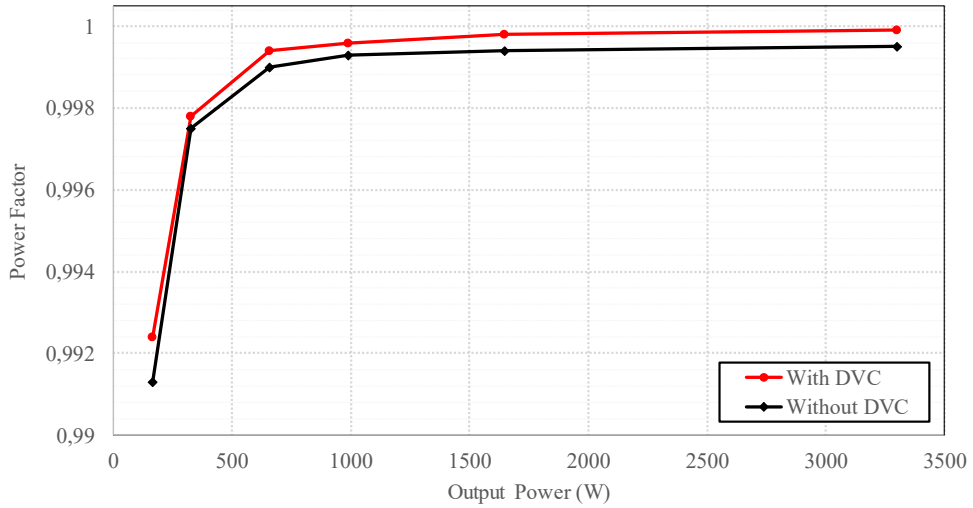

Figure 4.26. The PF results with and without developed DVC at different load conditions (V_{in}=110V_{rms})

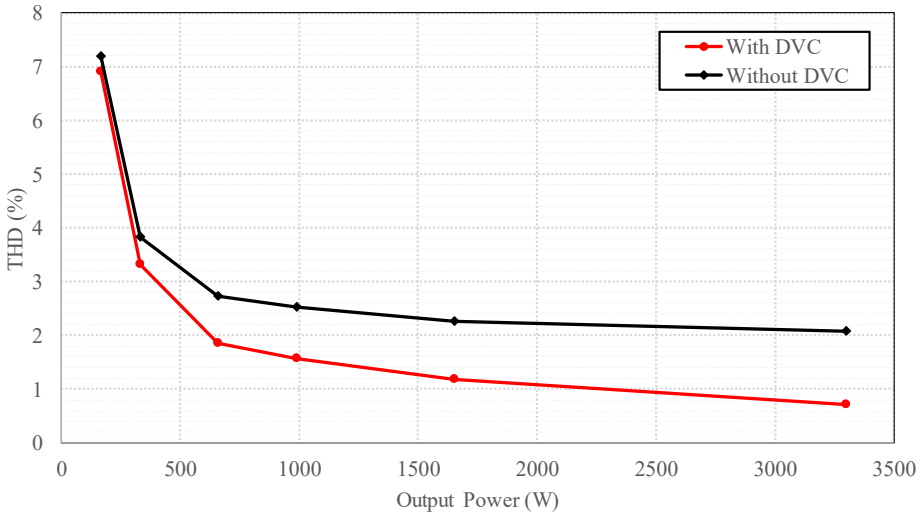

Figure 4.27. The input current THD results with and without developed DVC at different load conditions (V_{in}=110V_{rms})

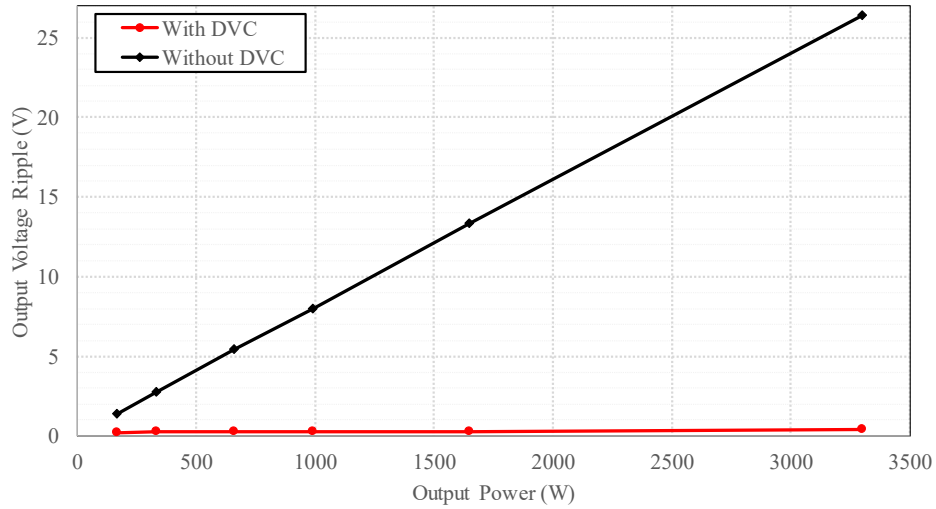

Figure 4.28. The output voltage ripple with and without developed DVC at different load conditions (V_{in}=110V_{rms})

Table 4.4. The performance results with and without developed DVC under six different load conditions (V_{in}=110V_{rms})

States	Efficiency		THD		Output Voltage Ripple	
	Traditional	Proposed	Traditional	Proposed	Traditional	Proposed
State 1	87.5%	90.8%	2.07%	0.72%	26.4V	0.40V
State 2	93.2%	95.4%	2.27%	1.19%	13.3V	0.30V
State 3	92.1%	95.2%	2.52%	1.56%	8V	0.30V
State 4	90.5%	93.9%	2.73%	1.85%	5.4V	0.25V
State 5	86.4%	91.8%	3.83%	3.31%	2.76V	0.25V
State 6	78.1%	86.4%	7.18%	6.91%	1.4V	0.20V

4.4.3. Case III

In this case, it is aimed to test the performance of the proposed converter in case of disturbances on the network side. Therefore, 11V_{rms} 1kHz voltage was injected into the 220V_{rms} 50Hz grid voltage to represent 5% THD distortion in the grid voltage as shown in Figure 4.29. The converter performance results were obtained for six different load conditions at the applied distorted grid voltage. Figures 4.30-35 illustrate the output voltage graphs of the proposed converter with and without developed DVC under six different load conditions. It can be seen from the figures that the output voltage ripple of the converter proposed with the developed DVC is still kept below 0.5V in all load cases despite the distorted grid voltage. The output voltage ripple results of the proposed converter with and without developed DVC are illustrated in Figure 4.36. With the obtained results, it is clearly seen that the designed converter prevents the output voltage from deteriorating by compensating the disturbances on the grid side.

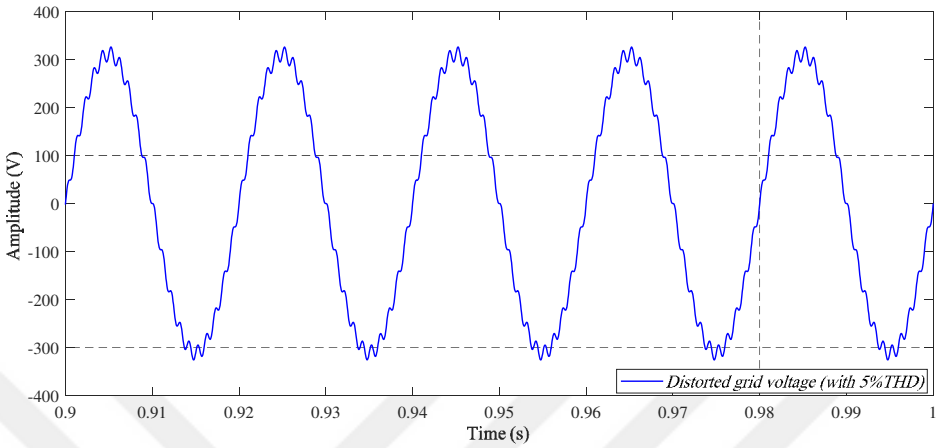

Figure 4.29. The applied distorted grid voltage waveform ($220V_{rms}$ + 5%THD)

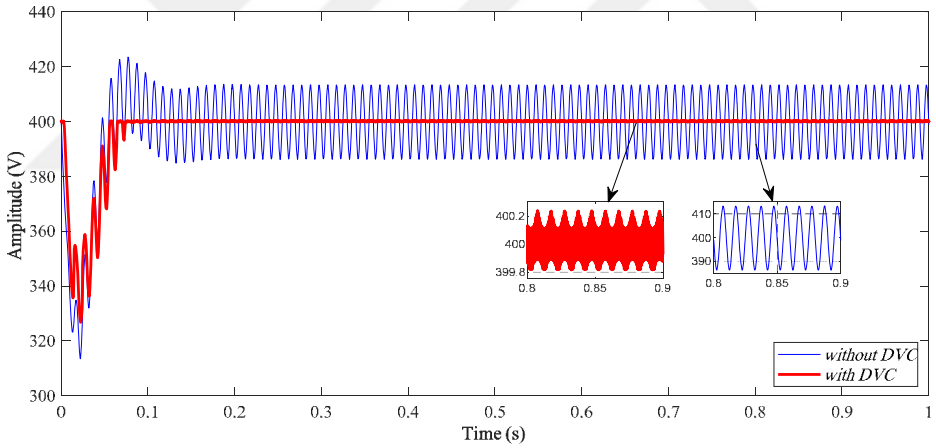

Figure 4.30. The output voltage graphs with and without developed DVC for state 1 (V_{in}=$220V_{rms}$ + 5% THD)

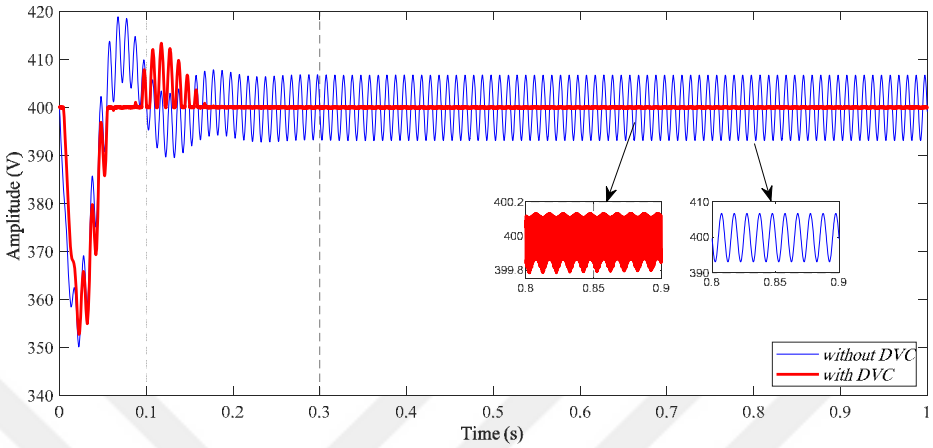

Figure 4.31. The output voltage graphs with and without developed DVC for state 2 (V_{in}=220V_{rms} + 5% THD)

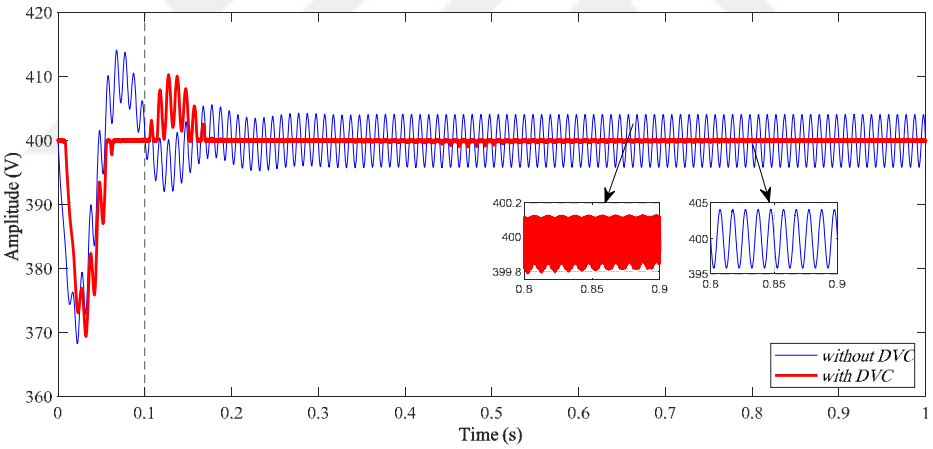

Figure 4.32. The output voltage graphs with and without developed DVC for state 3 (V_{in}=220V_{rms} + 5% THD)

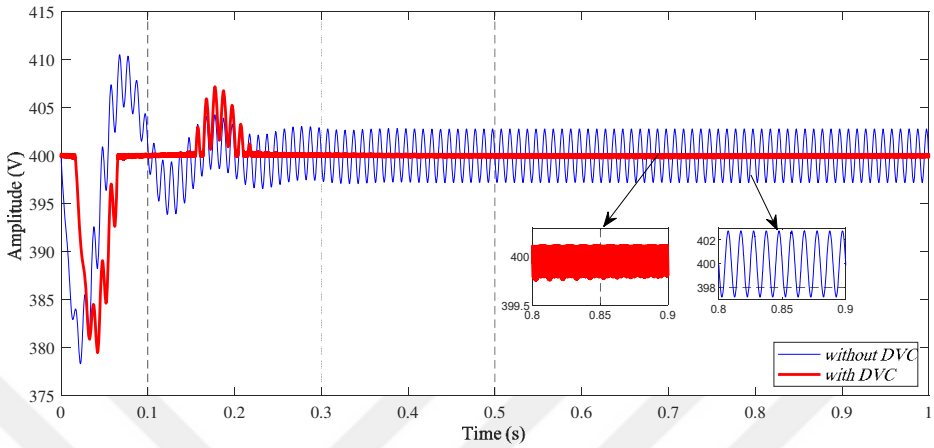

Figure 4.33. The output voltage graphs with and without developed DVC for state 4 (V_{in}=220V_{rms} + 5% THD)

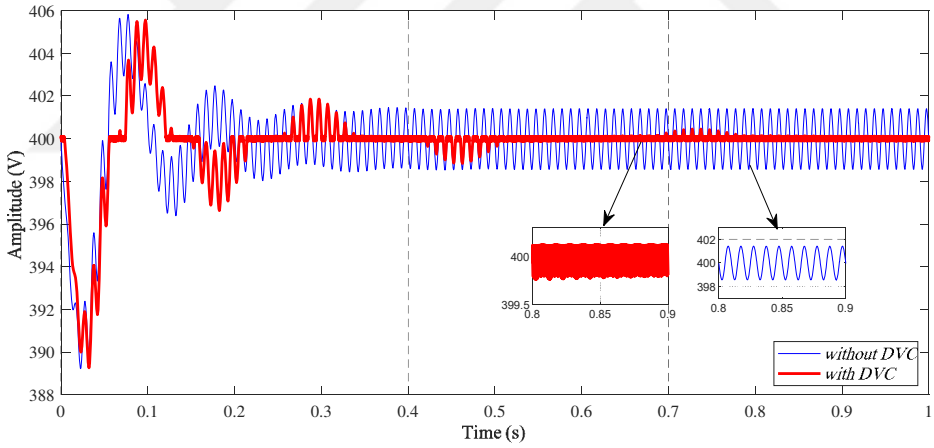

Figure 4.34. The output voltage graphs with and without developed DVC for state 5 (V_{in}=220V_{rms} + 5% THD)

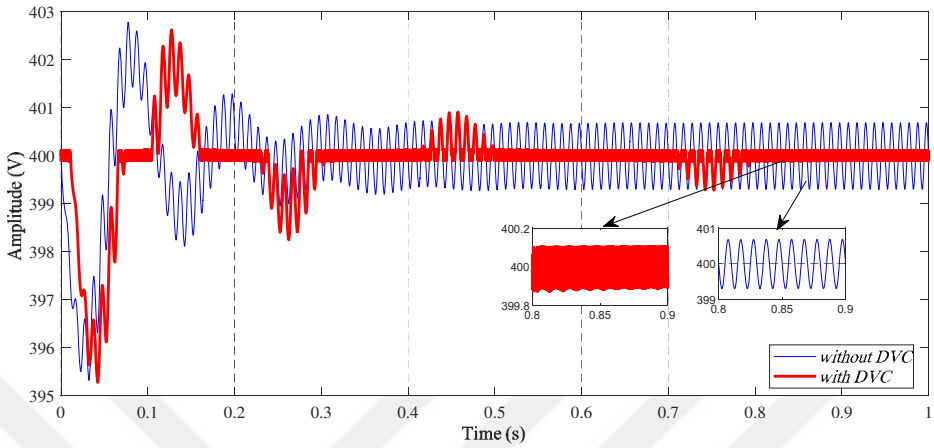

Figure 4.35. The output voltage graphs with and without developed DVC for state 6 (V_{in}=220V_{rms} + 5% THD)

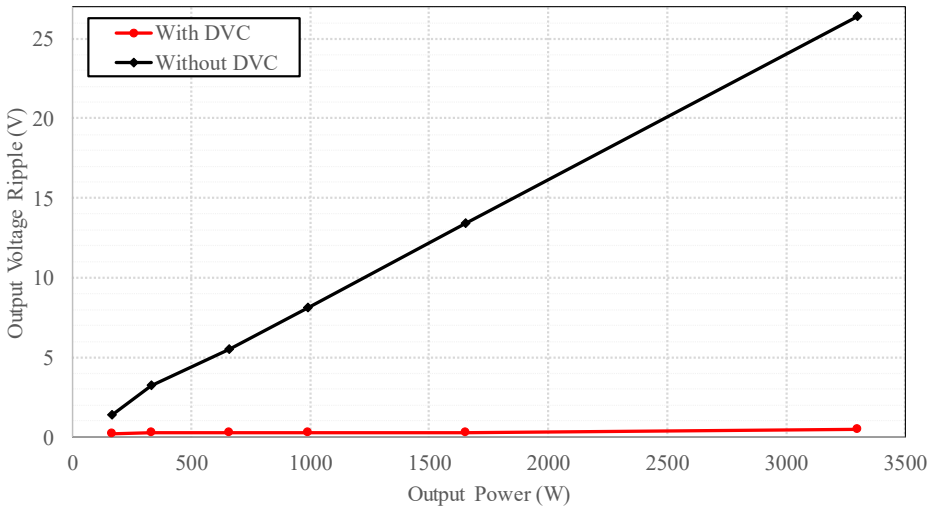

Figure 4.36. The output voltage ripple with and without developed DVC at different load conditions (V_{in}=220V_{rms})

4.5. Summary

In this section, the design and analysis of the proposed interleaved PFC boost converter with developed DVC are presented. The proposed converter has been tested under different input voltage conditions and different load conditions given in European efficiency standards by case studies. The proposed converter has performed high efficient performance. The output voltage ripple is kept below 0.5V from light load to full load conditions. Furthermore, the developed DVC has improved the input current characteristic of the converter. The proposed converter has achieved a nearly unity power factor. The proposed converter operates in the universal input voltage range and the input current THD values are compatible with the range given in IEC 61000-3-2 standards.

4. DESIGN AND ANALYSIS OF THE PROPOSED DVC FOR RIPPLE REDUCTION IN THE INTERLEAVED PFC BOOST CONVERTER

Ömer TÜRKSOY

5. DESIGN AND ANALYSIS OF PROPOSED SOFT-SWITCHING AC-DC PFC BOOST CONVERTER

In this section, the design and analysis of the proposed soft-switched AC-DC PFC boost converter are presented by providing information about the developed ASC and its operating principles. Furthermore, the design procedure of the entire circuit is meticulously presented. The performance of the designed converter has been tested with various case studies in Matlab/Simulink simulation environment.

5.1. Introduction

AC-DC PFC boost converters are the most popular topology among the AC-DC PFC converters developed for battery charging systems in EVs with their simple structure, high power density and easy controllability aspects. Higher power density is possible by increasing the switching frequency. However, increased switching frequency causes increased switching losses and EMI problems. SS methods have been developed for the solution of these problems. ZVS and ZCS techniques are one of the most basic methods to greatly reduce switching losses by limiting the intersection of current and voltage in the switching element during the turn on/off operations in AC-DC PFC boost converters. These methods not only eliminate switching losses but also create extra voltage and current stress on the additional passive snubber cell. Advanced SS techniques have been developed to overcome the shortcomings of these methods. ZVT techniques have been developed to eliminate losses during turn-on and ZCT techniques to eliminate losses during turn-off. These techniques are implemented with ASC and there are many ASC designs in the literature. Although some of these ASC managed to eliminate switching losses, they could not become widespread due to their high cost. In some studies, it has managed to eliminate switching losses with low-cost designs but created extra voltage and current stress on the switching elements.

In this study, a new soft-switching AC-DC PFC boost converter is developed with a novel ASC. The converter switch is turned on and turned off with ZVT and ZCT thanks to developed ASC, respectively. Thus, switching losses of the converter switch are eliminated. The ASC switch is turned on and turned off with ZCS and ZCT, respectively. The main circuit diode is turned-on with ZVS and turned-off with ZCT. Also, ASC circuit diodes are turned-on and turned-off with ZCS and ZVS, respectively. Although a small amount of conduction losses occurs with the additional ASC circuit, the converter's switching losses are largely eliminated, and the converter performance is greatly improved. Furthermore, the developed ASC has a low-cost design unlike the existing ASCs, as well as does not create any current and voltage stress on the circuit elements. The proposed converter has a high power density in these aspects. The proposed converter operates in the universal input voltage range and the input current THD values are compatible with the range given in IEC 61000-3-2 standards. SS conditions and unity power factor are achieved from light load to full load conditions.

Steady-state operating principles, design criteria and detailed loss analysis of the proposed converter are presented in the following sections.

5.2. Descriptions of the Proposed Converter

The proposed soft switched AC-DC PFC boost converter with developed ASC is illustrated in Figure 5.1. This converter consists of two-part such as the main circuit and auxiliary ASC circuit. V_i is grid voltage, V_{out} is the output voltage, S_1 is the main switch, D_2 is the body diode of the main switch, D_{i1}-D_{i4} are the bridge rectifier diodes, L_1 is boost inductance, D_1 is the main diode, C_o is filter capacitance, in the main circuit. In the ASC circuit, L_2, L_3 and C_1 illustrate the resonance inductances and capacitance, C_2 corresponds the parasitic capacitance of the main circuit switches, S_2 represents the auxiliary switch, D_3 is the body diode of the auxiliary switch, D_4-D_5 are the reverse blocking diodes and D_6 is the energy transferring diode.

As a controller of the main circuit, the average current mode control method is used, which is a well-known and effective method. This controller consists of two parts, such as voltage control and current control loops. Firstly, the output voltage (V_{out}) is compared to the reference voltage (V_{out}^{*}) and passed through a PI controller. Then, the signal generated at the output of the PI controller is multiplied by the rectified input voltage ($V_{in.rect.}$) and the current reference (I_L^{*}) is created. Finally, the generated reference current (I_L^{*}) and the inductor current (I_L) are compared and passed through a PI controller to generate the switching signal of the main switch.

The ASC circuit is controlled to operate on switch S_1 opening and closing times. The auxiliary switch is triggered by adding a calculated time delay to the signal of the main switch.

L_1 and C_o inductance and capacitance values are calculated as enough to keep the CCM operation, switching and resonance elements are chosen ideal and reverse recovery time, small enough to be neglected, diodes are selected for steady-state analysis.

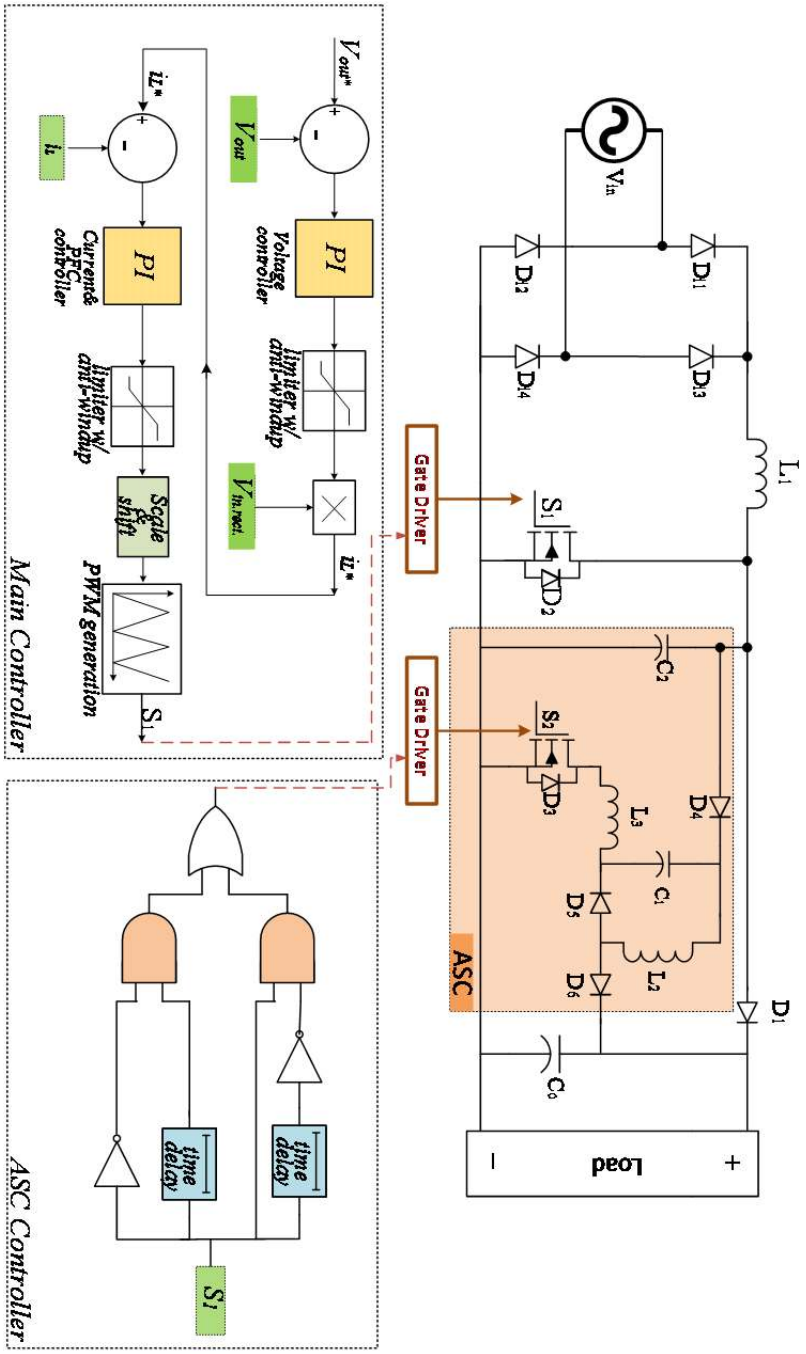

Figure 5.1. The proposed AC-DC PFC boost converter with developed ASC

5.3. Steady-State Operating Principles

There are eleven different operating states in a switching cycle. Each circuit of the operating states and the graphs of the operating states are given in Figure 5.2 and Figure 5.3, respectively. The operating cycle of the added ASC is designed not to affect the operating cycle of the main circuit.

State 1 ($t_0<t<t_1$): The initial conditions at the beginning of this state are as follows: $v_{C1}=0,\ v_{C2}=V_{out}, i_{L2}=0,\ i_{L3}=0,\ i_{D1}=i_{in}, i_{S1}=0, i_{s2}=0.$ Before $t=t_0$, the S_1 main switch and S_2 auxiliary switch are in the off state and the input voltage V_{in} feeds the output via boost diode D_1. At $t=t_0$, for turn-on of the switch S_2, the turn-on signal is given to its gate. S_2 switch and D_4, D_5 diodes are turn-on with ZCS due to series-connected L_2 and L_3 inductances. With this state, auxiliary ASC are turn-on and resonance occurs between L_2, L_3 and C_1. This resonance increases the voltage on C_1 and the current passing through S_2. Meanwhile, the current of the D_1 decreases. At the end of this state, the current of the S_2 becomes equal to the input current. At that time the current of the D_1 diode drops to zero, and this diode becomes turn-off with ZCT. The corresponding equations for the elements are given as follows:

$$i_{L2}=\frac{1}{L_2}V_{C1}(t-t_0) \tag{5.1}$$

$$i_{L3}=\frac{1}{L_3}(V_{out}-V_{C1})(t-t_0) \tag{5.2}$$

$$v_{C1}=\frac{1}{C_1}(i_{L3}-i_{L2})(t-t_0) \tag{5.3}$$

The final conditions at the end of this state are as follows: $v_{C1}=v_{C1}^{t1}$, $v_{C2}=V_{out}, i_{L2}=i_{L2}^{t1}, i_{L3}=i_{in},\ i_{D1}=0, i_{S1}=0, i_{s2}=i_{in}.$

State 2 ($t_1<t<t_2$): The initial conditions at the beginning of this state are as follows: $v_{C1}=v_{C1}^{t1}, v_{C2}=V_{out},\ \ i_{L2}=i_{L2}^{t1}, i_{L3}=i_{in}, i_{D1}=i_{in}, i_{S1}=0, i_{s2}=i_{in}.$ At the beginning of this state, resonance starts between the C_2 parasitic capacitor and C_1,

L_2 and L_3. This resonance increases the current of L_2 and L_3 and the voltage of C_1 but decreases the voltage of C_2. When $t = t_2$, the C_2 capacitor voltage falls to zero and this state ends. The corresponding equations for the elements are given as follows:

$$i_{L2} = \frac{1}{L_2} V_{C1}(t - t_1) \tag{5.4}$$

$$i_{L3} = \frac{1}{L_3}(V_{C2} - V_{C1})(t - t_1) \tag{5.5}$$

$$v_{C1} = \frac{1}{C_1}(i_{L3} - i_{L2})(t - t_1) \tag{5.6}$$

$$v_{C2} = \frac{1}{C_2}(i_{in} - i_{L3})(t - t_1) \tag{5.7}$$

The final conditions at the end of this state are given as follows: $v_{C1} = v_{C1}^{t2}$, $v_{C2} = 0$, $i_{L2} = i_{L2}^{t2}$, $i_{L3} = i_{L3}^{t2}$, $i_{D1} = 0$, $i_{S1} = 0$, $i_{s2} = i_{L3}^{t2}$.

State 3 (t_2<t<t_3): The initial conditions at the beginning of this state are as follows: $v_{C1} = v_{C1}^{t2}$, $v_{C2} = 0$, $i_{L2} = i_{L2}^{t2}$, $i_{L3} = i_{L3}^{t2}$, $i_{D1} = 0$, $i_{S1} = 0$, $i_{s2} = i_{L3}^{t2}$. At the beginning of this state, as the voltage of the C_2 parasitic capacitor falls to zero, D_2 diode turn in conduction mode. While the D_2 body diode is in the conduction, the control signal of the S_1 main switch is applied.

Thus, the S_1 switch becomes turn-on with ZVT. As the switch S_1 starts to flow current, the current of the inductance L_3 begins to decrease. And with this current falling to the level of the input current, the D_2 body diode turns-off under ZCS condition. When the current of the S_1 switch increases and reaches the input current level, the S_2 auxiliary switch is turn-off under ZCT. As soon as the S_2 turn-off, the body diode D_3 turn-on for a while. After passing the reverse recovery current, the diode D_3 switched off with ZCS and this state ends. The corresponding equations for the elements are given as follows:

$$i_{L2} = \frac{1}{L_2} V_{C1}(t - t_2) \tag{5.8}$$

$$i_{L3} = -\frac{1}{L_2} V_{C1}(t - t_2) \tag{5.9}$$

$$v_{C1} = \frac{1}{C_1}(i_{L3} - i_{L2})(t - t_2) \tag{5.10}$$

The final conditions at the end of this state are given as follows: $v_{C1} = v_{C1}^{t3}$, $v_{C2} = 0$, $i_{L2} = i_{L2}^{t3}$, $i_{L3} = 0$, $i_{D1} = 0$, $i_{S1} = i_{in}$, $i_{s2} = 0$.

State 4 ($t_3<t<t_4$): The initial conditions at the beginning of this state are as follows: $v_{C1} = v_{C1}^{t3}$, $v_{C2} = 0$, $i_{L2} = i_{L2}^{t3}$, $i_{L3} = 0$, $i_{D1} = 0$, $i_{S1} = i_{in}$, $i_{s2} = 0$. At the beginning of this state, resonance occurs between C_1 and L_2, with the switch S_2 and the body diode D_3 turn-off. With this resonance, the current of the L_2 inductance decreases and the capacitor C_1 charges. The current of L_2 falls to zero and this state ends. The transfer of energy stored in capacitor C_1 to the inductance L_2 or the capacitor C_2 is prevented by diodes D_4 and D_5. The corresponding equations for the elements are given as follows:

$$i_{L2} = \frac{1}{L_2} V_{C1}(t - t_3) \tag{5.11}$$

$$v_{C1} = -\frac{1}{C_1} i_{L2}(t - t_3) \tag{5.12}$$

The final conditions at the end of this state are given as follows: $v_{C1} = v_{C1}^{t4} = \sqrt{\left(v_{C1}^{t3}\right)^2 + \left(i_{L2}\sqrt{L_2/C_1}\right)^2}$, $v_{C2} = 0$, $i_{L2} = 0$, $i_{L3} = 0$, $i_{D1} = 0$, $i_{S1} = i_{in}$, $i_{s2} = 0$.

State 5 ($t_4<t<t_5$): In this state, only the S_1 main switch is in conduction. All other elements are in turn-off. The initial and final conditions are the same and given as follows: $v_{C1} = v_{C1}^{t5} = v_{C1}^{t4}$, $v_{C2} = 0$, $i_{L2} = 0$, $i_{L3} = 0$, $i_{D1} = 0$, $i_{S1} = i_{in}$, $i_{s2} = 0$.

State 6 ($t_5<t<t_6$): The initial conditions at the beginning of this state are as follows: $v_{C1} = v_{C1}^{t5}$, $v_{C2} = 0$, $i_{L2} = 0$, $i_{L3} = 0$, $i_{D1} = 0$, $i_{S1} = i_{in}$, $i_{s2} = 0$. At the beginning of this range, the turn-on signal of S_2 is applied and its current is

restricted by L_3 and turn-on with ZCS. With the turn-on of the S_2 switch, a series of resonance occurs between C_1 and L_3. Due to this resonance, the current of the S_1 and S_2 switches decreases and increases, respectively. As the S_1 current falls to zero, D_2 body diode turn-on with ZCS. Diode D_2 keeps the current of switch S_1 at zero, and the control signal of switch S_1 is interrupted. Thus, S_1 switch turns-off under ZCT condition. The resonance between C_1 and L_3 continues through the D_2 body diode with switch S_1 turn-off. At the end of this state, the voltage of C_1 falls to zero. The corresponding equations for the elements are given as follows:

$$i_{L3} = -\frac{1}{L_3} V_{C1}(t - t_5) \tag{5.13}$$

$$v_{C1} = \frac{1}{C_1} i_{L3}(t - t_5) \tag{5.14}$$

The final conditions at the end of this state are given as follows: $v_{C1} = 0$, $v_{C2} = 0$, $i_{L2} = 0$, $i_{L3} = i_{L3}^{t6} = \left(v_{C1}^{t5} / \sqrt{L_3 / C_1} \right)$, $i_{D1} = 0$, $i_{S1} = 0$, $i_{s2} = i_{L3}^{t6}$.

State 7 ($t_6 < t < t_7$)**:** The initial conditions at the beginning of this state are as follows: $v_{C1} = 0$, $v_{C2} = 0$, $i_{L2} = 0$, $i_{L3} = i_{L3}^{t6}$, $i_{D1} = 0$, $i_{S1} = 0$, $i_{s2} = i_{L3}^{t6}$. At the beginning of this state, when the voltage of the C_1 capacitor is positive, D_5 becomes turn-on with ZCS. With the turn-on of D_5, resonance occurs between C_1, L_2 and L_3, and the current of L_3 begins to decrease. When the current of the L_3 inductance reaches the level of the input current, the diode D_2 turn-off with ZCS. The corresponding equations for the elements are given as follows:

$$i_{L2} = \frac{1}{L_2} V_{C1}(t - t_7) \tag{5.15}$$

$$i_{L3} = \frac{1}{L_3} (V_{out} - V_{C1})(t - t_6) \tag{5.16}$$

$$v_{C1} = \frac{1}{C_1} (i_{L3} - i_{L2})(t - t_6) \tag{5.17}$$

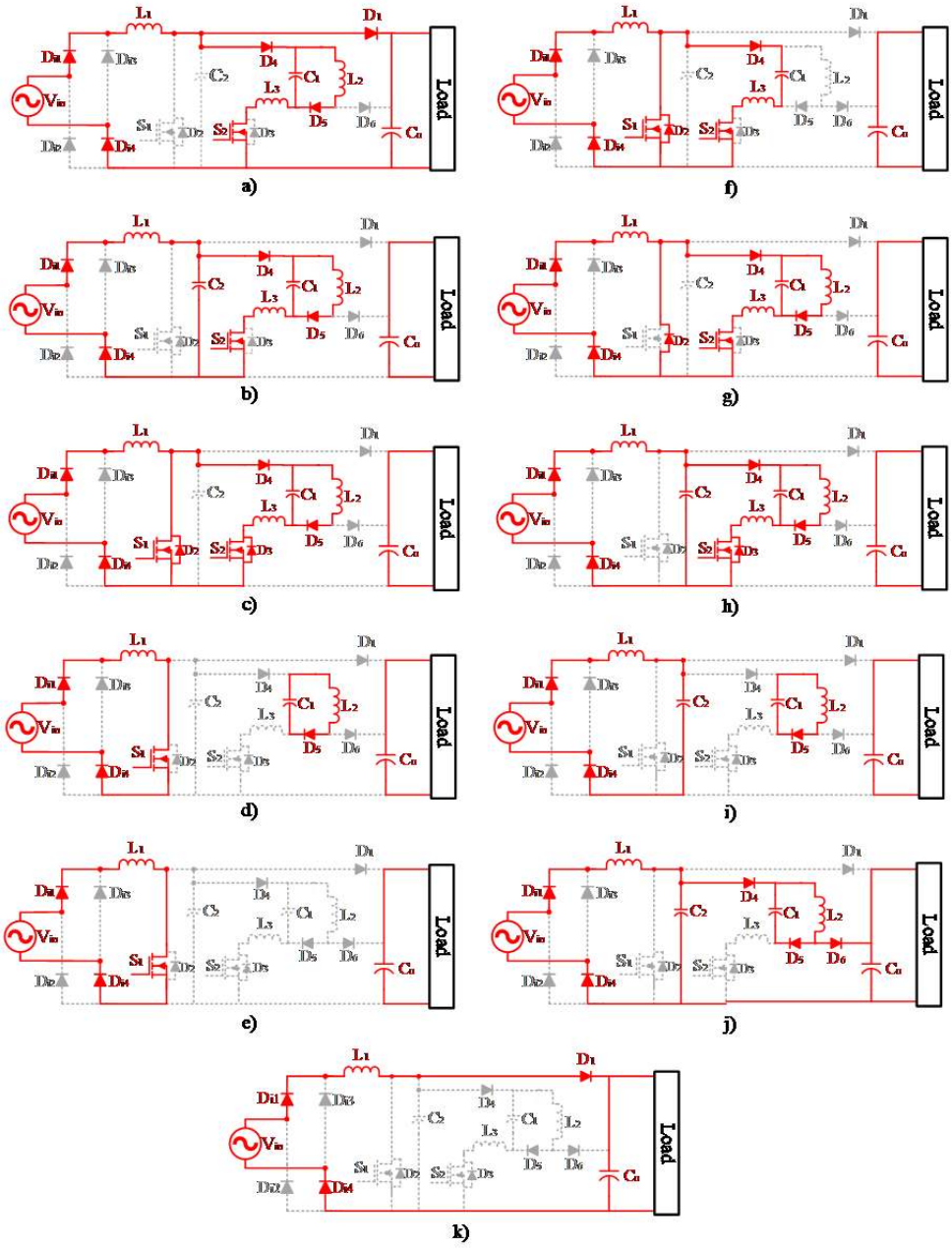

Figure 5.2. Operating states of the proposed converter

The final conditions at the end of this state are given as follows: $v_{C1}=v_{C1}^{t7}$, $v_{C2}=0,\ i_{L2}=i_{L2}^{t7},\ i_{L3}=i_{in},\ i_{D1}=0,\ i_{S1}=0,\ i_{s2}=i_{in}$.

State 8 ($t_7<t<t_8$): The initial conditions at the beginning of this state are as follows: $v_{C1}=v_{C1}^{t7},\ v_{C2}=0,\ i_{L2}=i_{L2}^{t7},\ i_{L3}=i_{in},\ i_{D1}=0,\ i_{S1}=0,\ i_{s2}=i_{in}$. At the beginning of this state, with the turn-off of the D_2 diode, a resonance begins between C_1, L_2, L_3 and C_2, and the current of the L_3 inductance decreases, at the same time, the voltage of the capacitor C_2 increases due to this resonance. With the current of the L_3 inductance dropping to zero, the switch S_2 becomes turn-off and the D_3 diode turn-on. After some current has passed through diode D_3, it's current falls to zero and is closed with D_4 together with ZCS. The corresponding equations for the elements are given as follows:

$$i_{L2}=\frac{1}{L_2}V_{C1}(t-t_7) \tag{5.18}$$

$$i_{L3}=\frac{1}{L_3}(V_{C2}-V_{C1})(t-t_7) \tag{5.19}$$

$$v_{C1}=\frac{1}{C_1}(i_{L3}-i_{L2})(t-t_7) \tag{5.20}$$

$$v_{C2}=\frac{1}{C_2}(i_{in}-i_{L3})(t-t_7) \tag{5.21}$$

The final conditions at the end of this state are given as follows: $v_{C1}=v_{C1}^{t8}$, $v_{C2}=v_{C2}^{t8},\ i_{L2}=i_{L2}^{t8},\ \ i_{L3}=0,\ i_{D1}=0,\ i_{S1}=0,\ i_{s2}=0.$

State 9 ($t_8<t<t_9$): The initial conditions at the beginning of this state are as follows: $v_{C1}=v_{C1}^{t8},\ v_{C2}=v_{C2}^{t8},\ i_{L2}=i_{L2}^{t8},\ i_{L3}=0,\ i_{D1}=0,\ i_{S1}=0,\ i_{s2}=0$. In this state, C_2 charges, and resonance occurs between C_1 and L_2. After a while, the sum of the voltages of the capacitors C_1 and C_2 become V_{out}, and

the diodes D_4 and D_6 turns-on with ZVS and this state end. The corresponding equations for the elements are given as follows:

$$i_{L2} = \frac{1}{L_2} V_{C1}(t - t_8) \tag{5.22}$$

$$V_{C1} = -\frac{1}{C_1} i_{L2}(t - t_8) \tag{5.23}$$

$$v_{C2} = \frac{1}{C_2} i_{in}(t - t_8) \tag{5.24}$$

The final conditions at the end of this state are given as follows: $v_{C1} = v_{C1}^{t9},\ v_{C2} = V_{out} - v_{C1}^{t9},\ i_{L2} = i_{L2}^{t9},\ i_{L3} = 0,\ i_{D1} = 0,\ i_{S1} = 0,\ i_{s2} = 0.$

State 10 ($t_9<t<t_{10}$): The initial conditions at the beginning of this state are as follows: $v_{C1} = v_{C1}^{t9},\ v_{C2} = V_{out} - v_{C1}^{t9},\ i_{L2} = i_{L2}^{t9},\ i_{L3} = 0,\ i_{D1} = 0,\ i_{S1} = 0,\ i_{s2} = 0.$ In this state, which starts with the turning-on the D_4 and D_6 diodes, resonance occurs between L_2, C_1 and C_2 and the switching energy stored in the inductance of L_2 and the capacitor of C_1 are transferred to the battery. At $t=t_{10}$, L_2 inductance current and C_1 capacitor voltage drop to zero. D_4, D_5 and D_6 turn-off with ZVS and D_1 turn-on with ZVS.

$$i_{L2} = \frac{1}{L_2}(v_{C2} - V_{out})(t - t_9) \tag{5.25}$$

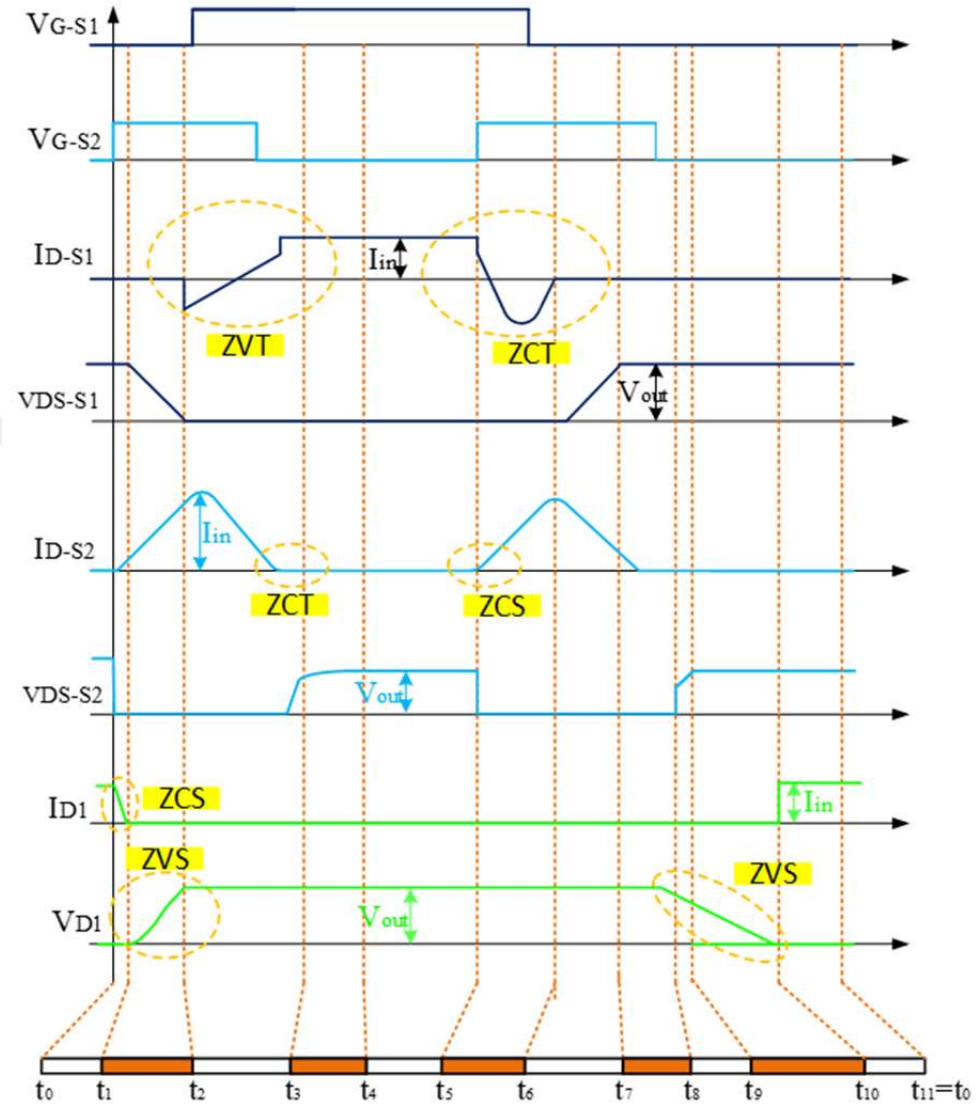

Figure 5.3. The current and voltage graphs of the switching elements in the operating states

$$v_{C2} = \frac{1}{C_1 + C_2}\left[\left(i_{in} - i_{L2}\right)\left(t - t_9\right) - C_1 V_{out}\right] \tag{5.26}$$

The final conditions at the end of this state are given as follows: $v_{C1} = 0,\ v_{C2} = V_{out},\ i_{L2} = 0,\ i_{L3} = 0,\ i_{D1} = i_{in},\ i_{S1} = 0,\ i_{s2} = 0.$

State 11 ($t_{10}<t<t_{11}$): The initial conditions at the beginning of this state are as follows: $v_{C1} = 0,\ v_{C2} = V_{out},\ i_{L2} = 0,\ i_{L3} = 0,\ i_{D1} = i_{in},\ i_{S1} = 0,\ i_{s2} = 0.$ In this state, only D_1 diode is in conduction. All other switching elements are turn-offs. With the end of this state, a switching period is completed.

The final conditions at the end of this state are given as follows: $v_{C1} = 0,\ v_{C2} = V_{out},\ i_{L2} = 0,\ i_{L3} = 0,\ i_{D1} = i_{in},\ i_{S1} = 0,\ i_{s2} = 0.$

5.4. Design Considerations

In this section, the design constraints of the presented converter are provided. Circuit elements of the converter the are calculated to following input and output specifications: Output power: P_{out}=3300W, Grid voltage: V_{in}=85-265V_{rms}, Output voltage: V_{out}=400V, switching frequency: f_{sw}=100kHz.

5.4.1. Selection of Main Circuit Components

Boost circuit inductor value is calculated based on parameters such as maximum duty cycle, inductor ripple current, lowest input voltage and maximum load current as given in following equations (Abdel-Rahman et al., 2016; Batarseh and Harb, 2018):

$$D_{\max} = \frac{V_{out} - V_{rect.in(\min)}}{V_{out}} \tag{5.27}$$

$$V_{rect.in(\min)} = \sqrt{2} V_{in(\min)} \tag{5.28}$$

$$I_{in(\max)} = \frac{2\mathrm{P}_{out}}{\sqrt{2} \times V_{in(\min)}} \tag{5.29}$$

$$\Delta I_{in} = I_{in(\max)} \times k_d \tag{5.30}$$

$$L_1 \geq \frac{V_{rect.in}(\min) T_{sw} D_{\max}}{\Delta I_{in}} \tag{5.31}$$

where D_{max} is the maximum duty ratio of the converter switch, V_{out} is the output voltage, $V_{rect.in(min)}$ is the minimum rectified input voltage, $I_{in(max)}$ is the maximum input current, P_{out} is the nominal output power, $V_{in(min)}$ is the minimum input voltage, k_d is the ripple ratio, T_{sw} is the switching period, ΔI_{in} is the inductor ripple current.

The output capacitor is calculated according to parameters such as output voltage, voltage ripple and hold-up time. The capacitor value should be chosen to be large enough to provide the following two equations.

$$C_o \geq \frac{2 \cdot P_{out} \cdot t_{hold}}{V_{out}^2 - V_{out}^2(\min)} \tag{5.32}$$

$$C_o \geq \frac{P_{out}}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_{out} \cdot V_{out}} \tag{5.33}$$

where ΔV_{out} is the output voltage ripple, t_{hold} is the hold-up time, $V_{out(min)}$ is the minimum output voltage, f_{line} is the input frequency. According to the above equations output filter capacitor C_o is selected 984uH, L_1 inductor is selected 1mH for CCM operation.

The voltage and current range of the boost switch, input rectifier diodes and boost diode are designed as in a traditional boost converter as follows (Akhlaghi et al., 2018):

$$V_{DS_{1(\max)}} = V_{D_{1(\max)}} = V_{out} \tag{5.34}$$

$$V_{D_{i1-4(\max)}} = V_{in} \tag{5.35}$$

$$I_{S_{1(\max)}} = I_{D_{1(\max)}} = I_{D_{i1-4(\max)}} = I_{in} + \frac{\Delta I_{L_1}}{2} \tag{5.36}$$

where ΔI_{L1} is the ripple current of the L_1 inductance. This parameter is selected to ensure the CCM operation. According to these boundary conditions, the maximum voltage of the boost switch and boost diode is calculated 400V and their maximum current is calculated 45A. Also, the maximum voltage of the input rectifier diodes is calculated as 311V and the maximum current is calculated as 45A. With these calculations, MOSFET IPB60R040CFD7 from Infineon has been selected as a boost switch. The technical properties of IPB60R040CFD7 are given in the following table.

Table 5.1.The technical properties of IPB60R040CFD7

$V_{DS(max)}$	$I_{D(max)}$	$R_{DS(on),max}$	$t_{d(on)}$	$t_{d(off)}$	t_r	t_f	C_{oss}
600 V	50A	40mΩ	36ns	112ns	19ns	6ns	85pF

The boost diode of the converter FFH50US60S from Fairchild Semiconductor has been selected due to its proper technical properties. The technical properties of FFH50US60S are given in the following table.

Table 5.2. The technical properties of FFH50US60S

Maximum DC Blocking Voltage	Average Rectified Forward Current	Instantaneous Forward Voltage	Reverse Recovery Time
600 V	50 A	1.38 V	113ns

The input bridge rectifier diodes of the converter KBPC5000 from EICSEMI has been selected because of the proper technical properties. The technical properties of KBPC5004 are given in the following table.

Table 5.3.The technical properties of KBPC5004

Maximum Recurrent Peak Reverse Voltage	Maximum RMS Voltage	Maximum Average Forward Current	Maximum Forward Voltage
400 V	280 V	50 A	1.1 V

5.4.2. Selection of ASC Circuit Components

L_3 inductance is calculated according to the rise time of the S_2 switch, as it functions to restrict the di/dt of the S_2 switch during the turn-on time. It also affects the current that will pass over the S_2 switch. Therefore, in its design, attention should be paid to parameters such as voltage on S_2 switch, the current through it and rise time.

$$L_{3_{cirt}} = \frac{V_{out}}{I_{in_{\max}}} t_{rise_{S_2}} \tag{5.37}$$

For the turn-off the S_2 switch under ZCT condition, while this switch flows the current, with the resonance that occurs, the body diode D_3 of this switch should turning-on and the control signal should be interrupted in the range where this diode is in the conduction. For the turn-on of D_3, the L_2 value must be at least three times of the L_3 value.

$$L_{2_{cirt}} \geq 3L_3 \tag{5.38}$$

From the (4.37) and (4.38), L_2 and L_3 inductances are selected 3uH and 1uH, respectively.

C_1 capacitor significantly changes ZVT and ZCT times with resonances created by both L_2 and L_3 inductances. As the size of the C_1 capacitor increases, ZVT and ZCT times increase. However, these times should be chosen optimally so that they do not affect the switching times of the main converter. This value is chosen as 25nF for the designed circuit.

C_2 represents the parasitic capacitances of all switching elements in the circuit. Since the switching elements are considered ideal in the analyses, this capacitor was added to observe the effect of parasitic capacitance in the analyses. This value is chosen as 2nF.

Since there is no current and voltage stress on the elements in the ASC circuit, the same diodes and switches used in the main circuit can also be used in the ASC circuit.

5.5. Loss Analysis

To perform the loss analysis of the proposed converter, the loss of power on each element must be calculated. The losses of main switch S_1 used as the switching element consist of conduction, switching and capacitive turn-on losses as given in the following equation:

$$P_{S_1} = P_{cond.} + P_{sw} + P_{cap.} \tag{5.39}$$

where $P_{cond.}$ is the conduction loss of the S_1 switch, P_{sw} is the switching loss of the S_1 switch and $P_{cap.}$ is the capacitive turn-on loss of the S_1 switch.

Switching loss of the S_1 switch is consist of turn-on switching losses and turn-off switching losses and they can be calculated as follows:

$$P_{sw-on} = f_{sw}\left(\frac{1}{2}V_{S_1(\max)}I_{S_1(\max)}\left(t_{d(on)} + t_r\right)\right) \tag{5.40}$$

$$P_{sw-off} = f_{sw}\left(\frac{1}{2}V_{S_1(\max)}I_{S_1(\max)}\left(t_{d(off)} + t_f\right)\right) \tag{5.41}$$

where f_{sw} is the switching frequency, $V_{S1(max)}$ is the maximum switch voltage, $I_{S1(max)}$ is the maximum switch current, $t_{d(on)}$ is the turn-on delay time, t_r is the rise time of the switch, $t_{d(off)}$ is the turn-off delay time, t_f is the fall time of the switch.

The turn-on capacitive loss of S_1 switch is a loss caused by the output capacitor in the structure and is calculated by the following equation:

$$P_{cap.} = \frac{1}{2}f_{sw}C_{oss}V_{S_1(\max)}^2 \tag{5.42}$$

where C_{oss} represents the output capacitance of the S_1 switch.

The loss that occurs during conduction on the S_1 switch is calculated with the formula below.

$$P_{cond.} = R_{DS_{1(on)}}I_{S_1(rms)} \tag{5.43}$$

where $R_{DS1(on)}$ represents the on-resistance of the S_1 switch, $I_{s1(rms)}$ represents the rms value of the S_1 switch current.

The switching losses of the auxiliary switch S_2 are calculated by the formula below.

$$P_{sw-on} = f_{sw(S_2)}\left(\frac{1}{2}V_{S_2(\max)}I_{S_2(\max)}\left(t_{on}+t_{off}\right)\right) \tag{5.44}$$

The turn-on capacitive loss of S_2 switch is a loss caused by the output capacitor in the structure and is calculated by the following equation:

$$P_{cap.} = \frac{1}{2}f_{sw}C_{oss}V_{S_2(\max)}^2 \tag{5.45}$$

where C_{oss} represents the output capacitance of the S_1 switch.

The loss that occurs during conduction on the S_2 switch is calculated with the following equation:

$$P_{cond.} = R_{DS_{2(on)}}I_{S_2(rms)} \tag{5.46}$$

where $R_{DS2(on)}$ represents the drain-source on-state resistance of the S_2 switch, $I_{s2(rms)}$ represents the rms value of the S_2 switch current.

Conduction loss of the boost diode D_1 is calculated by the following equation:

$$P_{cond.} = V_F I_{D_1(avg.)} \tag{5.47}$$

where V_F is the forward voltage of the boost diode D_1, $I_{D1(avg.)}$ is the average current of the boost diode D_1.

Conduction losses of the ASC circuit diodes D_3, D_4, D_5, D_6 are calculated by the following equation:

$$P_{cond.} = V_F I_{D_{3,4,5,6}(avg.)} \tag{5.48}$$

where V_F is the forward voltage of the ASC circuit diodes $D_{3,4,5,6}$, $I_{D1(avg.)}$ is the average current of the ASC circuit diode D_1.

The bridge rectifier total power loss is calculated using the average input current passing through bridge rectifier diodes as in the following equation (Abdel-Rahman et al., 2016):

$$I_{D_{i1,2,3,4}(avg.)} = \frac{2\sqrt{2} \cdot P_{out}}{\pi \cdot V_{in}} \tag{5.49}$$

$$P_{brid.} = 4 \cdot V_F \cdot I_{Di1,2,3,4(avg.)} \tag{5.50}$$

where V_F is the forward voltage of the rectifier bridge diodes $D_{3,4,5,6}$, $I_{D1(avg.)}$ is the average current of the rectifier bridge diodes $D_{3,4,5,6}$.

5.6. Performance Results

In order to assess the performance of the presented converter, the case studies were performed in the MATLAB/Simulink environment. The simulation parameters of the proposed converter are given in Table 5.1.

Table 5.4. Simulation parameters of the proposed converter

Parameter	**Symbol**	**Value**
Output power	P_{out}	3300W
Input voltage	V_{in}	85-265V_{rms}
Output voltage	V_{out}	400V
Switching frequency	f_{sw}	100kHz
Boost inductor	L_1	1mH
Output filter capacitor	C_o	984uF
Upper resonance inductor	L_2	3uH
Lower resonance inductor	L_3	1uH
Resonance capacitor	C_1	25nF
Parasitic capacitor	C_2	2nF
Sample time of the simulation	t_s	20ns
Time delay value for ASC switch	t_d	300ns
Proportional constant (voltage controller)	K_p^v	0.08
Integral constant (voltage controller)	K_i^v	5e-3
Proportional constant (current controller)	K_p^c	6
Integral constant (current controller)	K_i^c	1e-3

Three case studies are presented to evaluate the performance of the proposed soft switched AC-DC PFC boost converter. In the first of these case studies, the performance results of the converter at $220V_{rms}$ input voltage are presented for six different load conditions in European efficiency standards as given in Table 5.2. Input voltage and current graphs of the proposed converter are presented to show that the unity power factor of the converter is achieved, and THD results of the input current are provided to show that they are compatible with the THD values in the standards. In addition, the current and voltage graphs of the switching elements are presented in detail to show that SS, the main contribution of the study, is achieved under all load conditions. Output voltage and current are presented to show the transient-state and steady-state characteristics of the converter. Finally, the power losses for each element of the converter are listed in detail for the full load condition. In the second of the case studies, the same procedure was repeated for the input voltage of $110V_{rms}$. In the third of the case studies, the performance of the proposed converter has been tested in case of disturbances on the network side under six different load cases.

Table 5.5. Load conditions at European efficiency standards

States	State 1	State 2	State 3	State 4	State 5	State 6
Values	%100 Load	%50 Load	%30 Load	%20 Load	%10 Load	%5 Load

Finally, the overall efficiency of the converter is calculated according to the European efficiency standards by the following formula:

$$EU\eta = 0.03\eta_{\%5} + 0.06\eta_{\%10} + 0.13\eta_{\%20} + 0.1\eta_{\%30} + 0.48\eta_{\%50} + 0.2\eta_{\%100} \quad (5.51)$$

5.6.1. Case I

In this case, the performance of the proposed converter has been tested for V_{in}=$220V_{rms}$ under six different load conditions given in European efficiency standards. Figure 5.4, Figure 5.5 and Figure 5.6 represent the effect of the load

variations on the input characteristic of the proposed converter. It can be clearly seen from Figure 5.5 that the proposed converter has achieved nearly unity power factor from light load to full load condition. Also, it is noted that input current harmonics (THD) is lower than 5% from half load to full load and it is compliant with the IEC 61000-3-2 standards as shown in Figure 5.6. Figure 5.7 illustrates the gate control signals of the converter switch S_1 and ASC switch S_2 for six different load conditions. The ASC switch S_2 converter switch is activated during the turn-on and turn-off moments of S_1, allowing the SS of the S_1 switch. The ASC switch S_2 converter switch is activated during the turn-on and turn-off moments of S_1, allowing the SS of the S_1 switch. Figure 5.8 shows the current and voltage graphs of the converter switch S_1. It can be clearly seen from the figure that the ZVT turn-on and ZCT turn-off operation of the converter switch S_1 is achieved over the entire load range. In addition, no current and voltage stress occurred on the switch. The voltage and current graphs of the ASC switch S_2 are shown in Figure 5.9. It can be seen from the figure that turn-on and turn-off operations of the S_2 switch under all load conditions are performed with ZCS and ZCT, respectively. The current and voltage graphs of converter diode D_1 are given in Figure 5.10. In all load cases, turn-on transition is realized with ZVS and turn-off transition is realized with ZCT. Figure 5.11 and Figure 5.12 represent the output voltage and current graphs of the proposed converter under six different load conditions. It is noted that the proposed converter has a robust controller characteristic in both transient-state and steady-state conditions. Efficiency curves of the proposed soft switched converter vs. hard switched counterpart are shown in Figure 5.13 for all load conditions. It can be obviously seen from the figure that the proposed converter has high efficiency compared to the hard switched counterpart over the entire load range and the proposed converter has achieved 97.82% maximum efficiency. The overall efficiency of the proposed converter is calculated as 96.66% according to European efficiency standards. In Table 5.3, the comparison of the losses of the proposed converter and hard switching counterpart is provided.

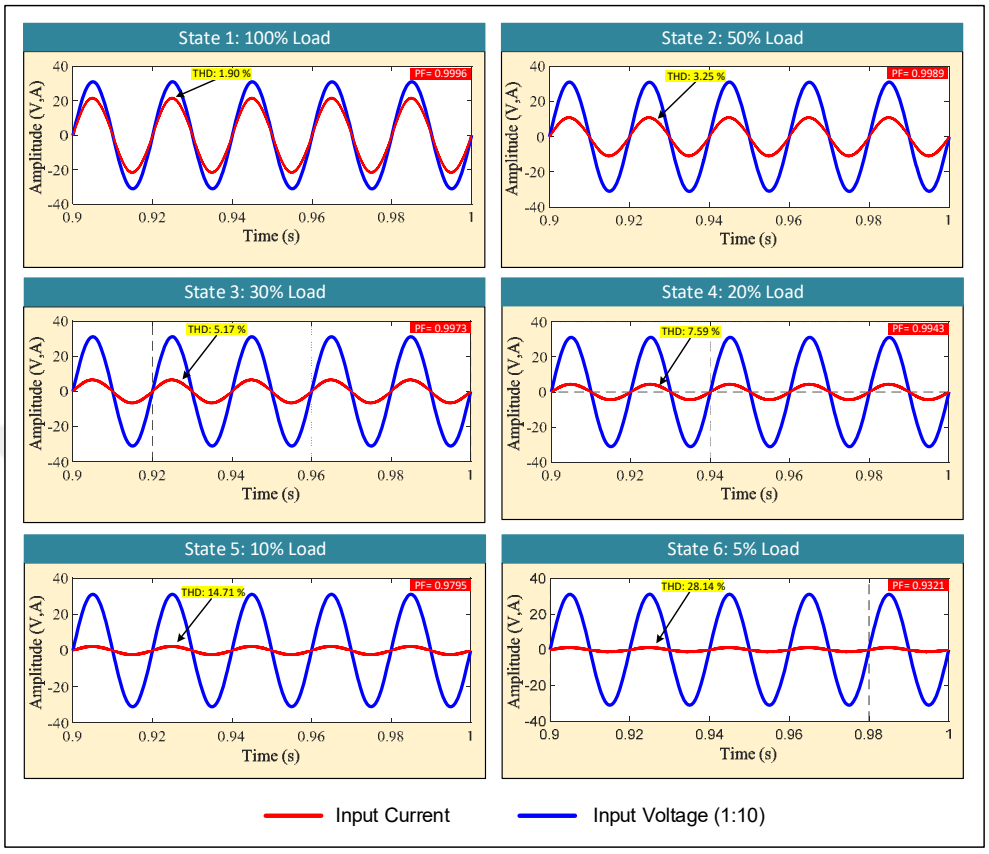

Figure 5.4. The input current and voltage graphs for different load conditions (V_{in}=220V_{rms})

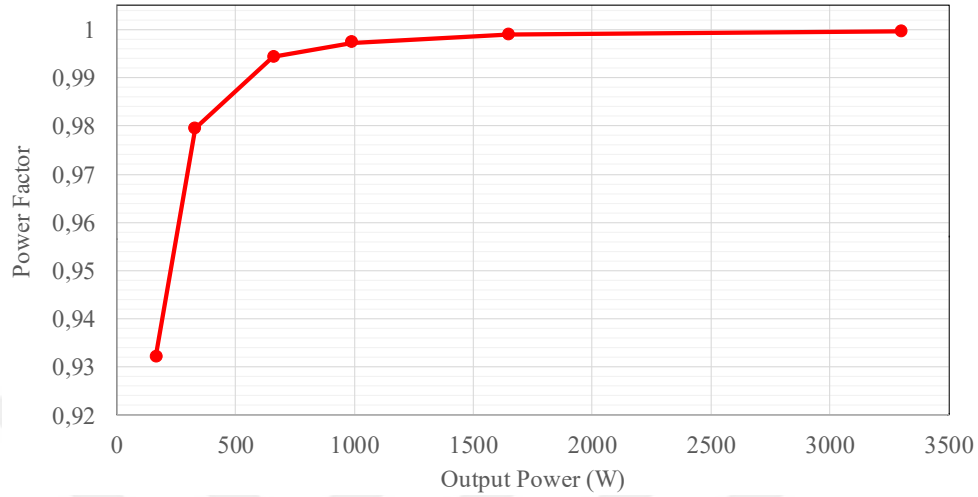

Figure 5.5. The input PFs of the proposed converter at all load cases (V_{in}=220V_{rms})

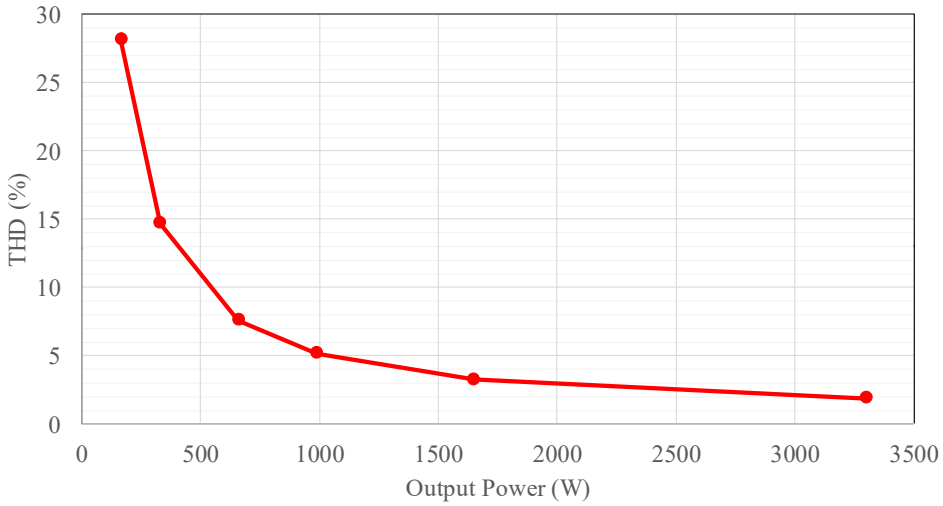

Figure 5.6. The input current THD results for all load cases (V_{in}=220V_{rms})

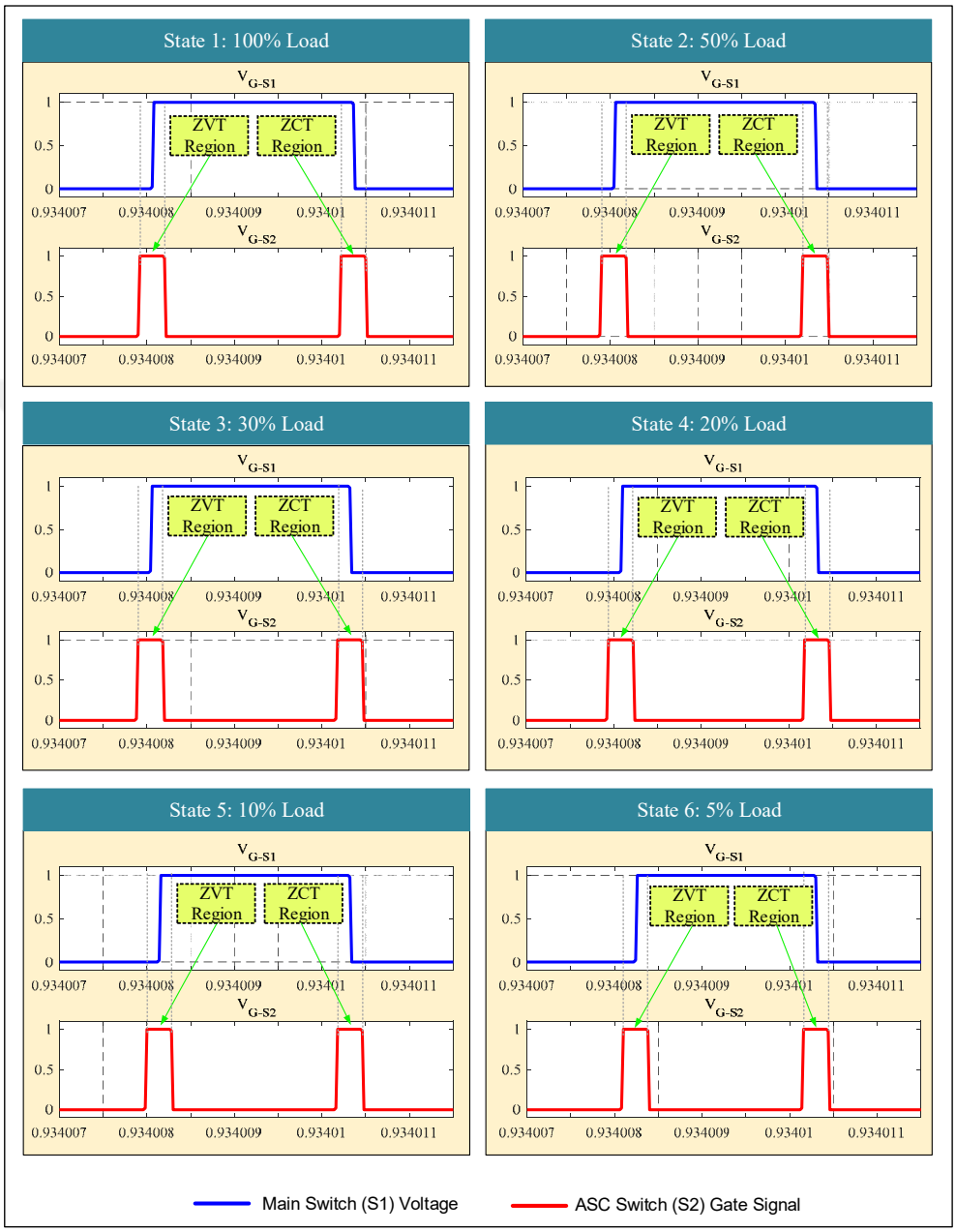

Figure 5.7. The trigger signals of converter switches (V_{in}=220V_{rms})

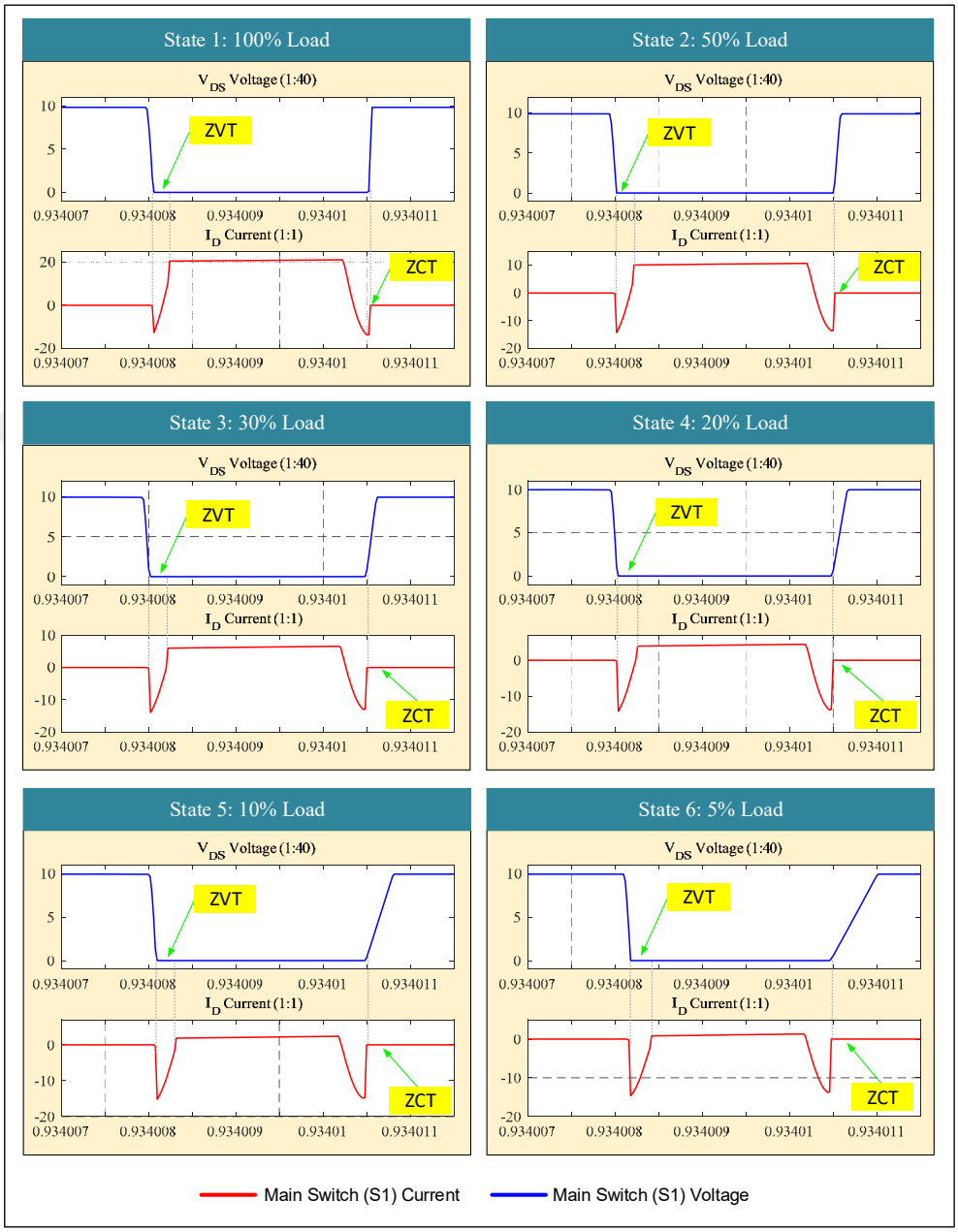

Figure 5.8. I_D current and V_{DS} voltage of the S_1 switch at different load conditions (V_{in}=220V_{rms})

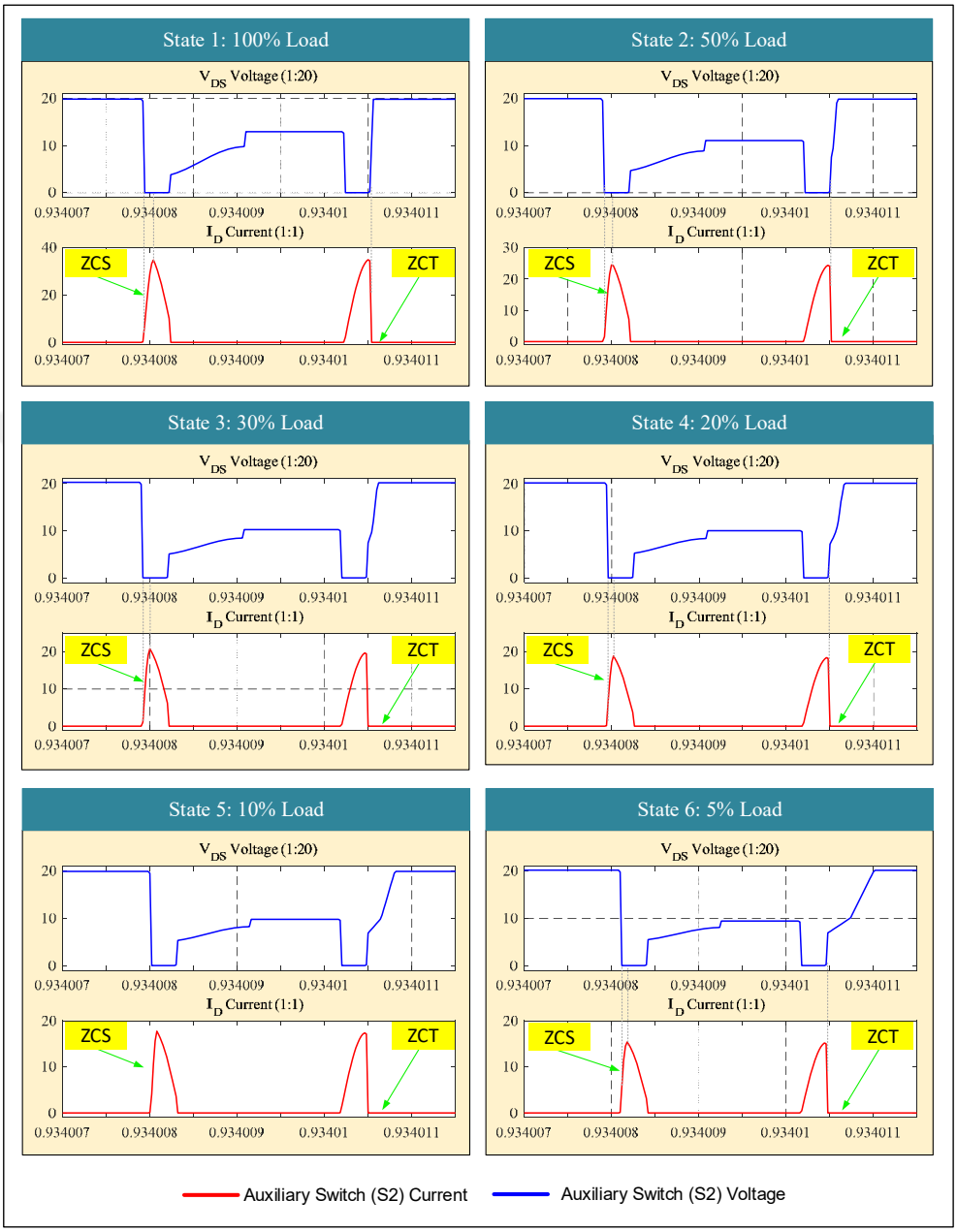

Figure 5.9. I_D current and V_{DS} voltage of the S_2 switch at different load conditions (V_{in}=220V_{rms})

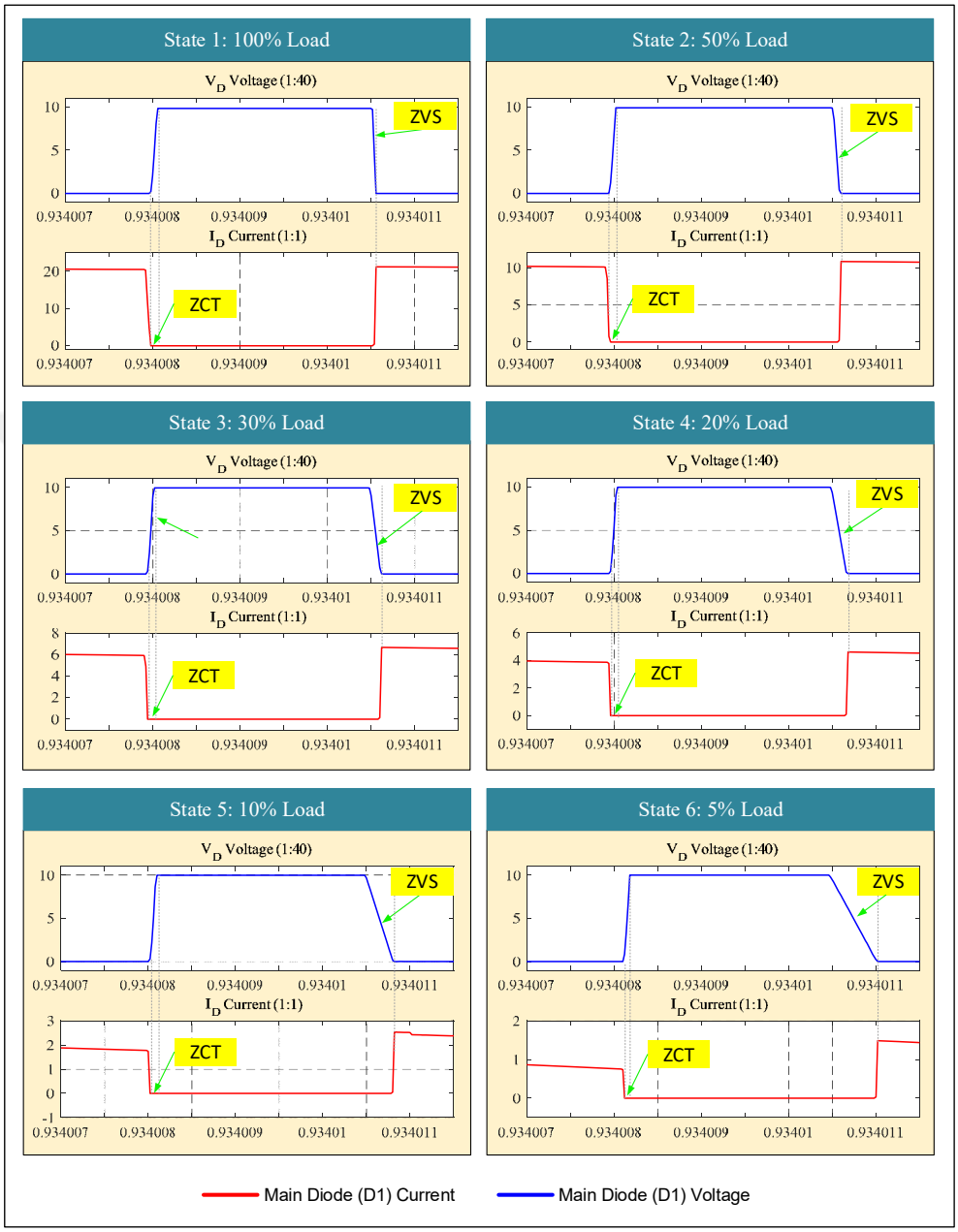

Figure 5.10. I_D current and V_D voltage of the D_1 diode at different load conditions (V_{in}=220V_{rms})

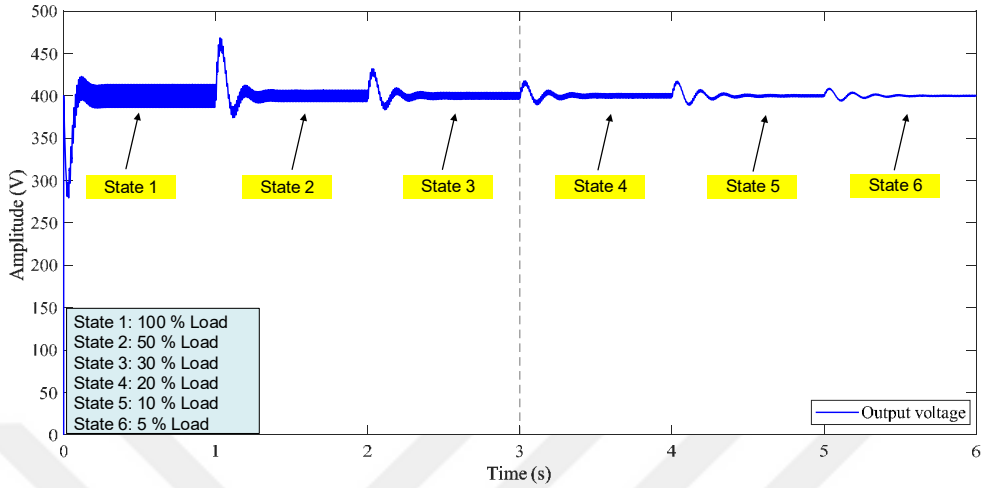

Figure 5.11. The output voltage graph of the proposed converter at different load conditions (V_{in}=220V_{rms})

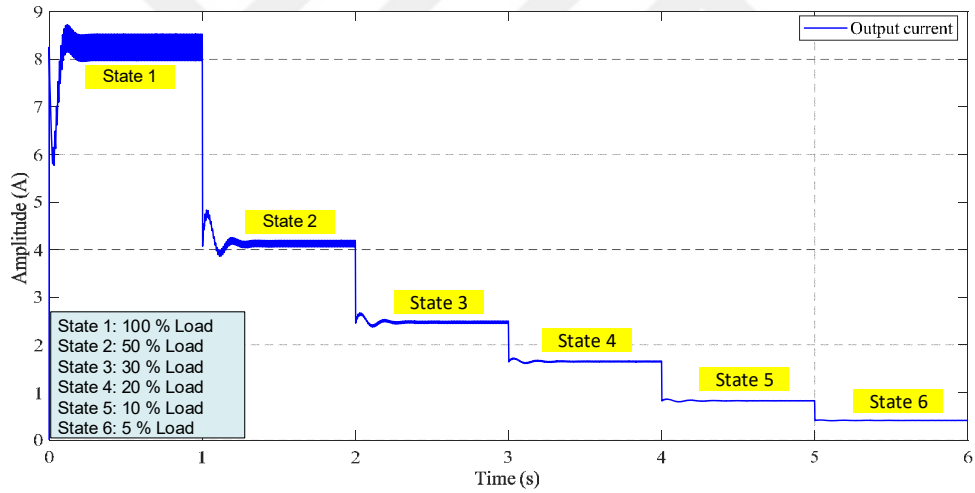

Figure 5.12. The output current graphs of the proposed converter at different load conditions (V_{in}=220V_{rms})

Table 5.6. The list of the losses of the proposed converter and hard switching counterpart (V_{in}=220V_{rms}, P_{out}=3300W)

				Hard switching counterpart	Proposed converter
Switches	V_{max}	S_1		400V	400V
		S_2		N/A	400V
	I_{rms}	S_1		15.63A	15.28A
		S_2		N/A	15.28A
Diodes	V_F	D_{1-2}		1.38V	1.38V
		D_{3-6}		N/A	1.38V
	I_{avg}	D_{1-2}		8.25A	8.25A
		D_{3-6}		N/A	0.2A
	V_F	D_{i1-4}		0.9V	0.9V
	I_{rms}	D_{i1-4}		16.39A	16.39A
Losses	S_1	Capacitive turn-on loss		0.68W	0
		Switching loss	turn-on	19.89W	0
			turn-off	52.16W	
		Conduction loss		0.63W	0.61W
	S_2	Capacitive turn-on loss		N/A	0
		Switching loss		N/A	0
		Conduction loss		N/A	0.30W
	D_{1-2}	Conduction loss		2x11.38W	2x11.38W
	D_{3-6}	Conduction loss		N/A	4x0.27W
	D_{i1-4}	Conduction loss		4x12.65W	4x12.15W
Total Loss				146.72W	73.35W

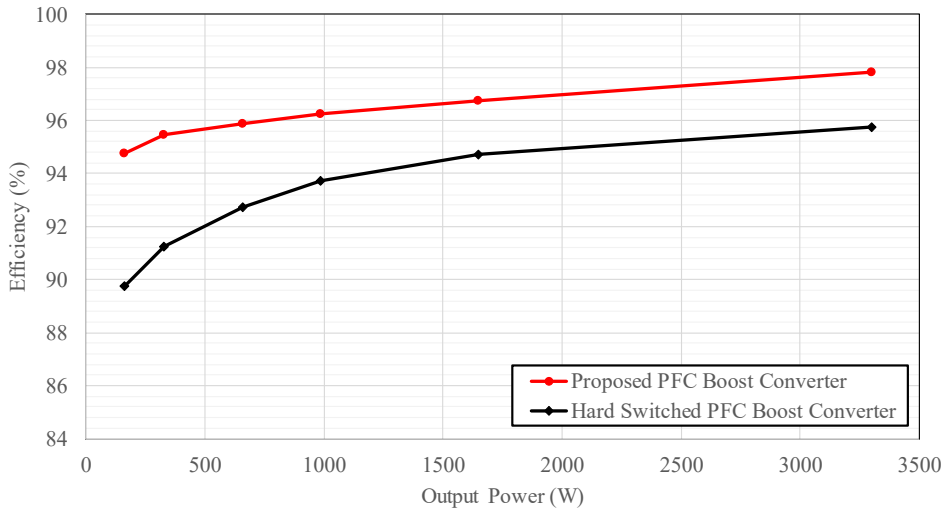

Figure 5.13. The efficiency of the proposed converter and hard switched counterpart (V_{in}=220V_{rms})

5.6.2. Case II

In this case, the performance of the proposed converter has been tested for V_{in}=110V_{rms} under six different load conditions given in European efficiency standards. Figure 5.14, Figure 5.15 and Figure 5.16 represent the effect of the load variations on the input characteristic of the proposed converter. It can be clearly seen from Figure 5.15 that the proposed converter has achieved nearly unity power factor from light load to full load condition. Also, it is noted that input current harmonics (THD) is lower than 5% from half load to full load and it is compliant with the IEC 61000-3-2 standards as shown in Figure 5.16. Figure 5.17 illustrates the gate control signals of the converter switch S_1 and ASC switch S_2 for six different load conditions. The ASC switch S_2 converter switch is activated during the turn-on and turn-off moments of S_1, allowing the SS of the S_1 switch. The ASC switch S_2 converter switch is activated during the turn-on and turn-off moments of S_1, allowing the SS of the S_1 switch. Figure 5.18 shows the current and voltage graphs of the converter switch S_1. It can be clearly seen from the figure that the

ZVT turn-on and ZCT turn-off operation of the converter switch S_1 is achieved over the entire load range. In addition, no current and voltage stress occurred on the switch. The voltage and current graphs of the ASC switch S_2 are shown in Figure 5.19. It can be seen from the figure that turn-on and turn-off operations of the S_2 switch under all load conditions are performed with ZCS and ZCT, respectively. The current and voltage graphs of converter diode D_1 are given in Figure 5.20. In all load cases, turn-on transition is realized with ZVS and turn-off transition is realized with ZCT. Figure 5.21 and Figure 5.22 represent the output voltage and current graphs of the proposed converter under six different load conditions. It is noted that the proposed converter has a robust controller characteristic in both transient-state and steady-state conditions. Efficiency curves of the proposed soft switched converter vs. hard switched counterpart are shown in Figure 5.23 for all load conditions. It can be obviously seen from the figure that the proposed converter has high efficiency compared to the hard switched counterpart over the entire load range and the proposed converter has achieved 96.96% maximum efficiency at half load conditions. The full load efficiency of the proposed converter is decreased from 97.82% to 95.99% at V_{in}=110V_{rms}. The overall efficiency of the proposed converter is calculated as 96.07% according to European efficiency standards. Because as the input voltage decreases, the input current increases and therefore the input bridge rectifier losses increase. In Table 5.4, the comparison of the losses of the proposed converter and hard switching counterpart is given.

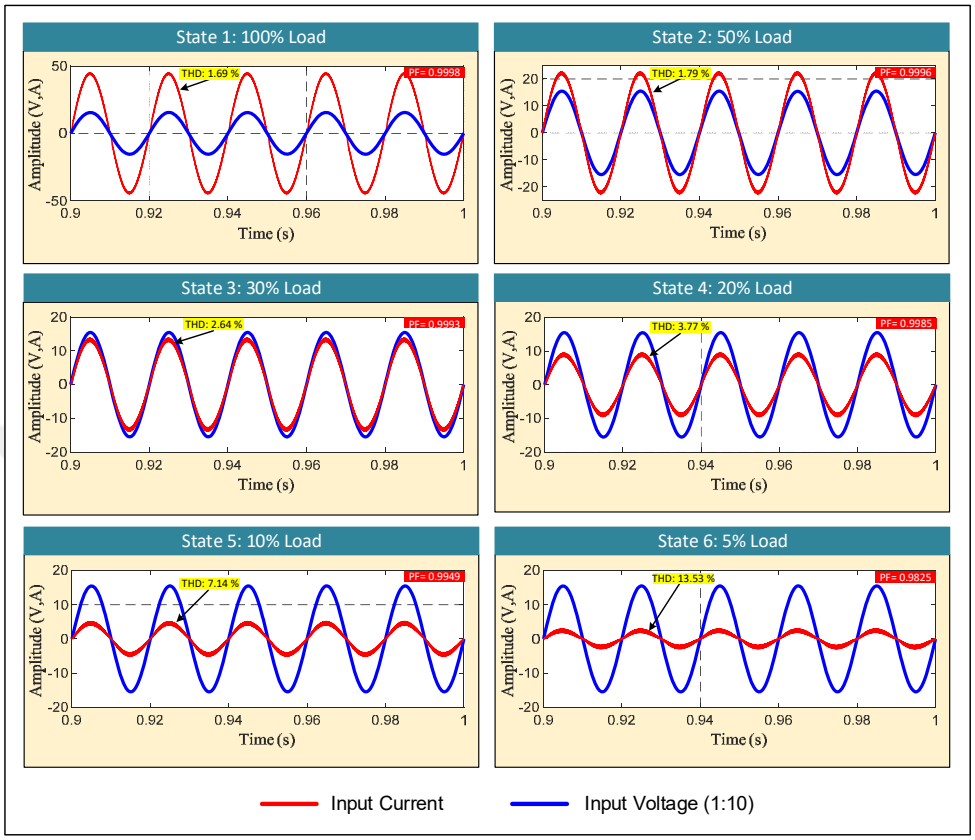

Figure 5.14. The input voltage and current graphs of the proposed converter at different load conditions (V_{in}=110V_{rms})

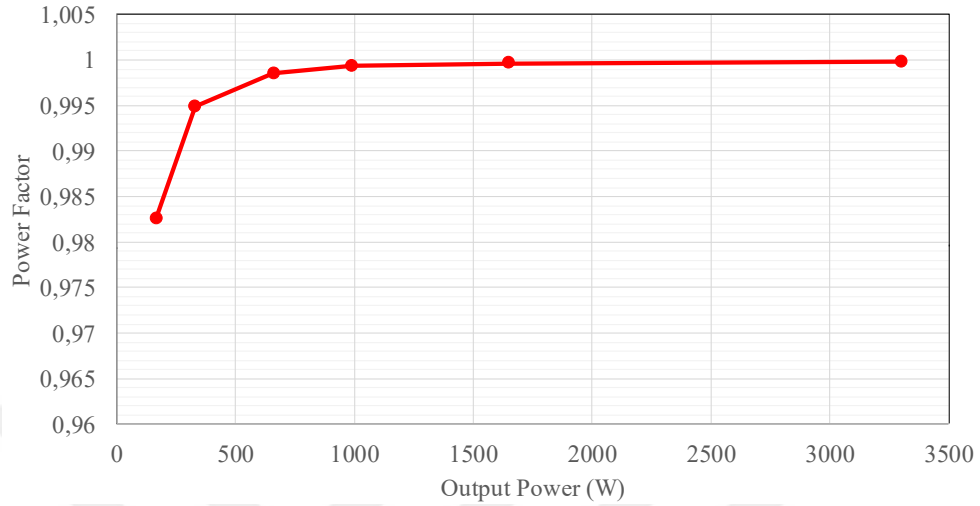

Figure 5.15. The input PFs of the proposed converter at all load cases (V_{in}=110Vrms)

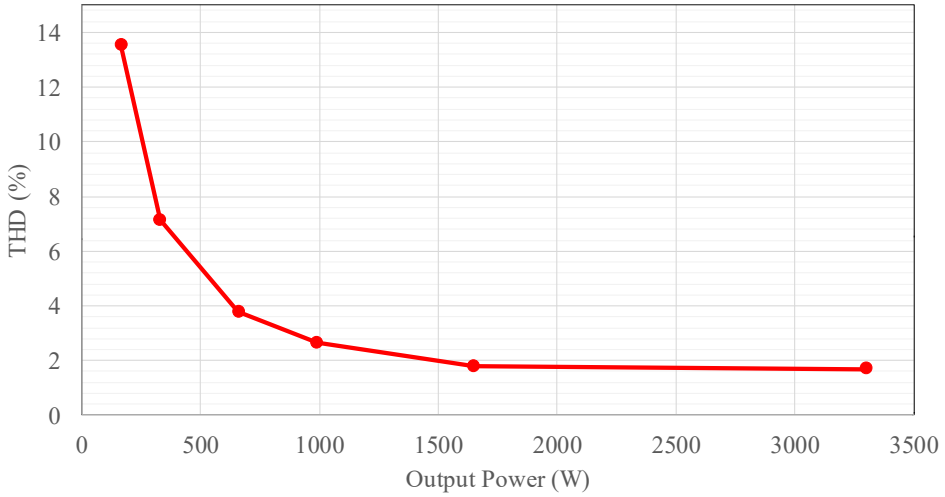

Figure 5.16. The input current THD results of the proposed converter at all load cases (V_{in}=110V_{rms})

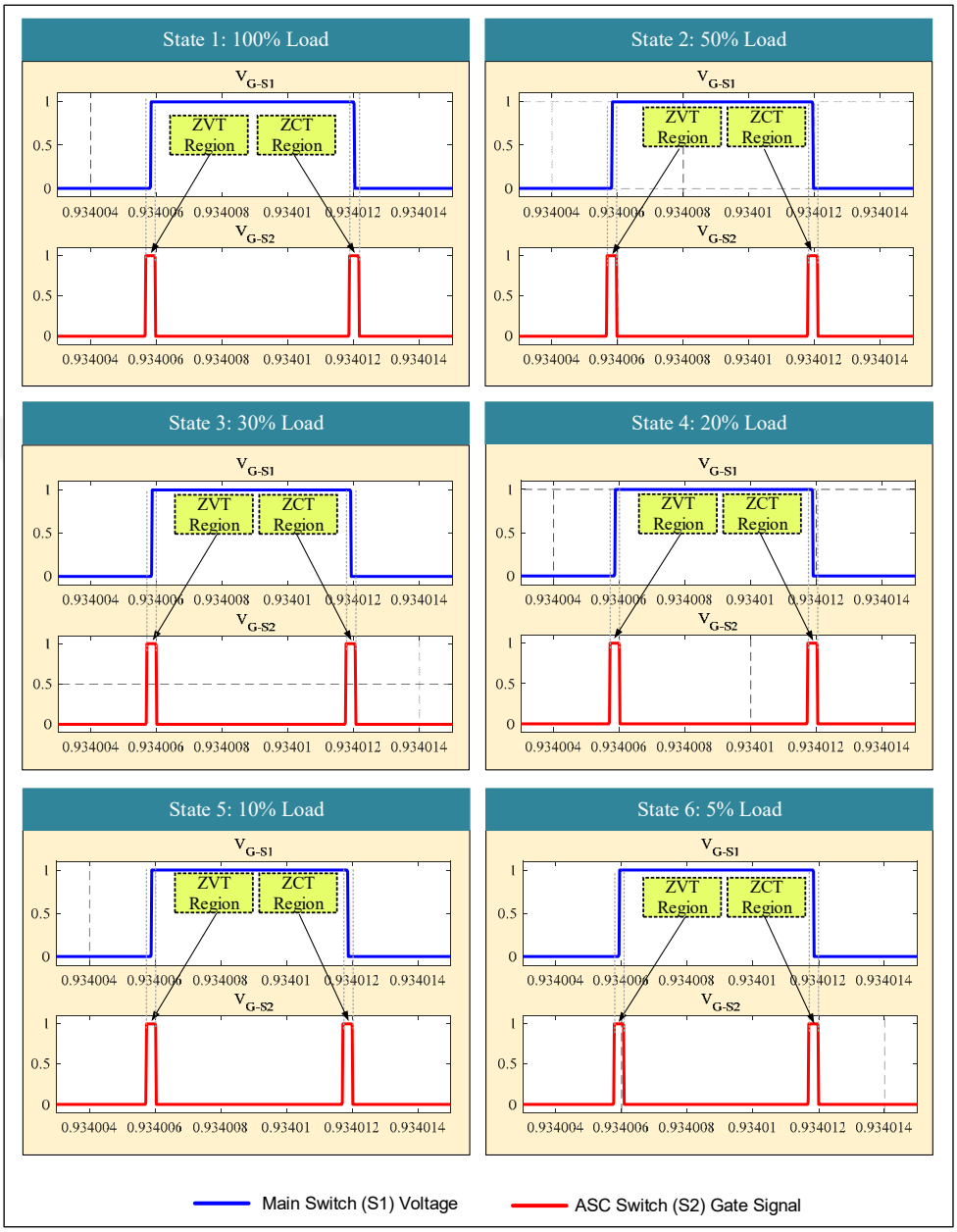

Figure 5.17. The trigger signals of the converter switches (V_{in}=110V_{rms})

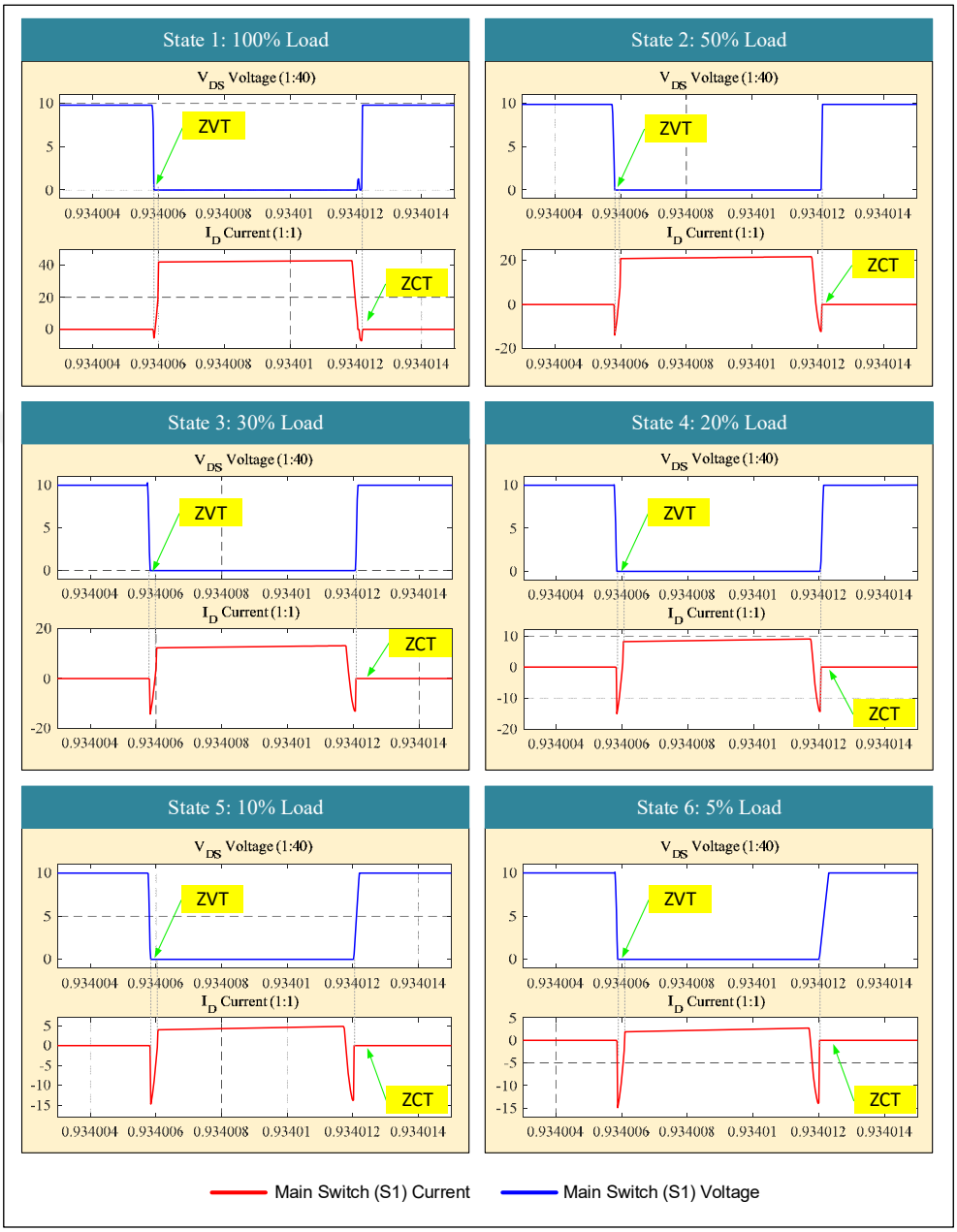

Figure 5.18. I_D current and V_{DS} voltage of the S_1 switch at different load conditions (V_{in}=110V_{rms})

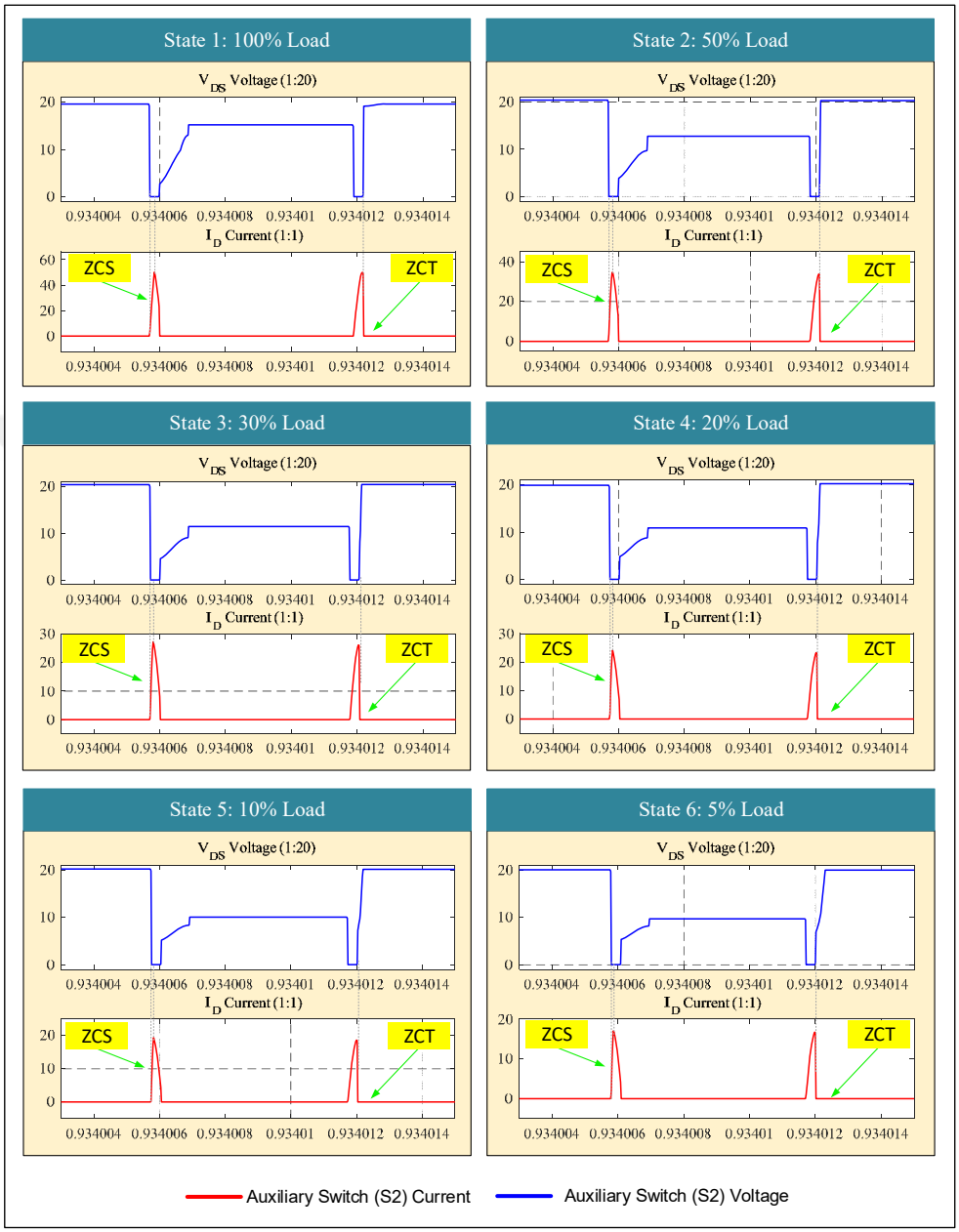

Figure 5.19. I_D current and V_{DS} voltage of the S_2 switch at different load conditions (V_{in}=110V_{rms})

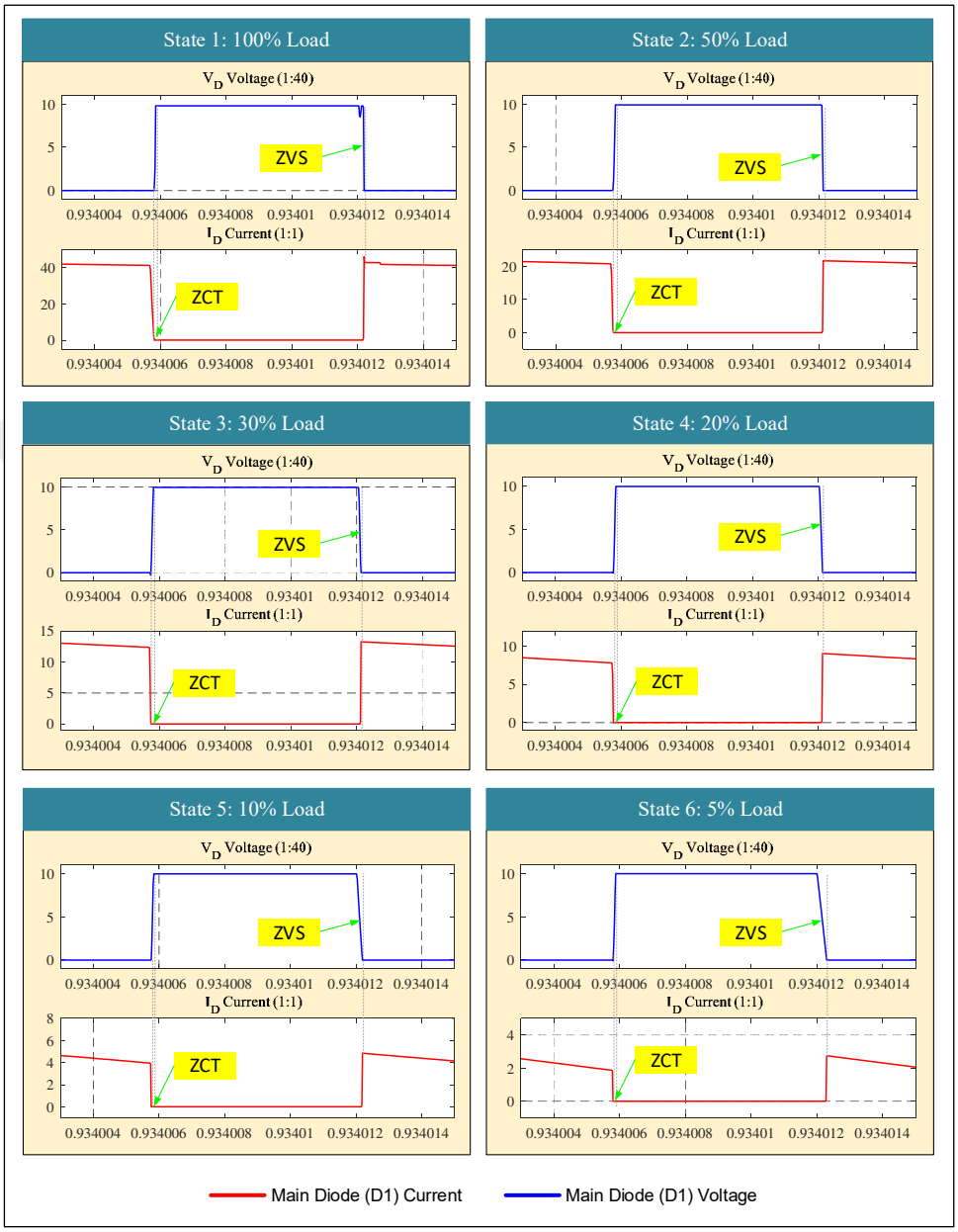

Figure 5.20. I_D current and V_D voltage of the D_1 diode at different load conditions (V_{in}=110V_{rms})

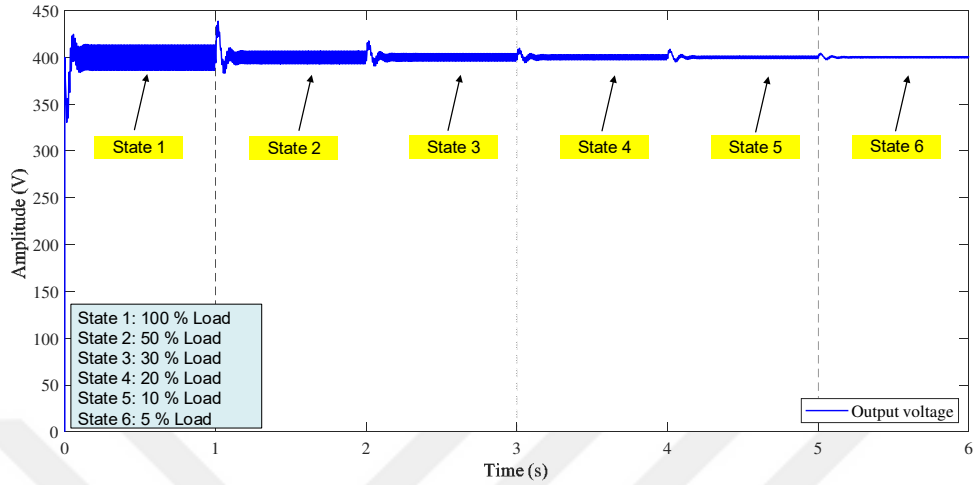

Figure 5.21. The output voltage graph of the proposed converter at different load conditions (V_{in}=110V_{rms})

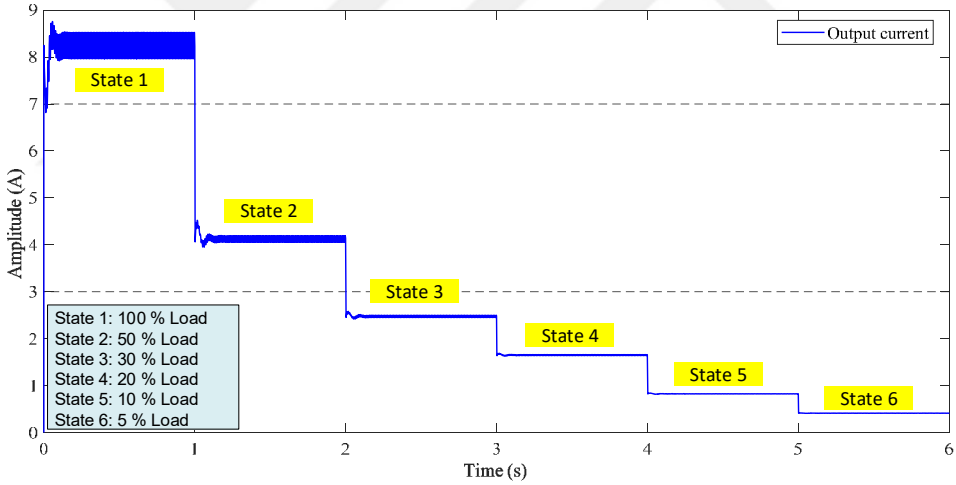

Figure 5.22. The output current graph of the proposed converter at different load conditions (V_{in}=110V_{rms})

Table 5.7. The list of the losses of the proposed converter and hard switching counterpart (V_{in}=110V_{rms}, P_{out}=3300W)

				Hard switching counterpart	Proposed converter
Switches	V_{max}	S_1		400V	400V
		S_2		N/A	400V
	I_{rms}	S_1		35.29A	31.84A
		S_2		N/A	31.84A
Diodes	V_F	D_{1-2}		1.38V	1.38V
		D_{3-6}		N.A	1.38V
	I_{avg}	D_{1-2}		8.25A	8.25A
		D_{3-6}		N/A	0.2A
	V_F	D_{i1-4}		1V	1V
	I_{rms}	D_{i1-4}		35.29A	31.84A
Losses	S_1	Capacitive turn-on loss		0.68W	0
		Switching loss	turn-on	44.91W	0
			turn-off	117.78W	
		Conduction loss		1.41W	1.27W
	S_2	Capacitive turn-on loss		N/A	0
		Switching loss		N/A	0
		Conduction loss		N/A	0.636W
	D_{1-2}	Conduction loss		2x11.38W	2x11.38W
	D_{3-6}	Conduction loss		N/A	4x0.27W
	D_{i1-4}	Conduction loss		4x29.34W	4x28W
Total Loss				304.9W	137.74W

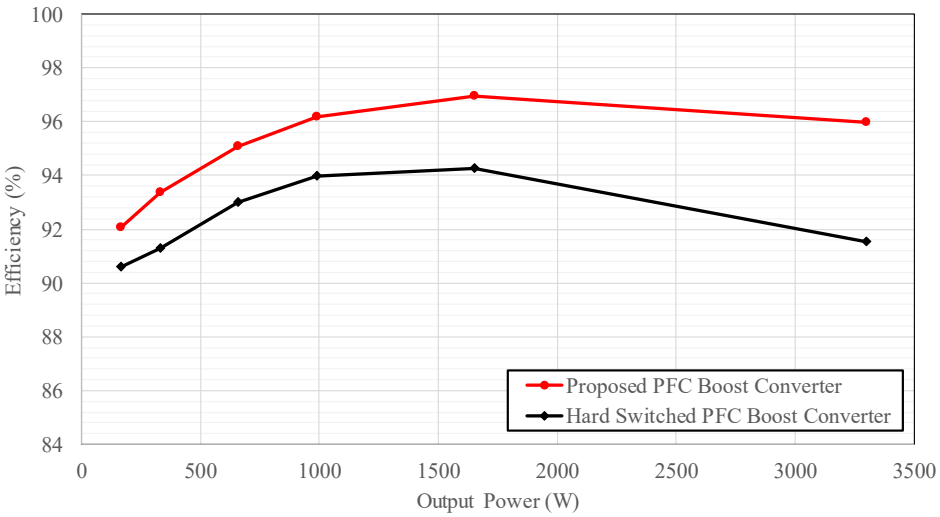

Figure 5.23. The efficiency of the proposed converter and hard switched counterpart (V_{in}=110V_{rms})

5.6.3. Case III

In this case, it is aimed to test the performance of the proposed converter in case of disturbances on the network side. Therefore, 11V_{rms} 1kHz voltage was injected into the 220V_{rms} 50Hz grid voltage to represent 5% THD distortion in the grid voltage as shown in Figure 5.24. In order to show that the proposed converter still performs soft-switching during this disturbance condition, and provides a stable output power, output voltage and current graphs and current and voltage of the converter elements are provided. The converter performance results were obtained for six different load conditions at the applied distorted grid voltage. Figure 5.25 illustrates the gate control signals of the converter switch S_1 and ASC switch S_2 for six different load conditions. The ASC switch S_2 converter switch is activated during the turn-on and turn-off moments of S_1, allowing the SS of the S_1 switch. The ASC switch S_2 converter switch is activated during the turn-on and turn-off moments of S_1, allowing the SS of the S_1 switch. Figure 5.26 shows the current and voltage graphs of the converter switch S_1. It can be clearly seen from

the figure that the ZVT turn-on and ZCT turn-off operation of the converter switch S_1 is achieved over the entire load range. In addition, no current and voltage stress occurred on the switch. The voltage and current graphs of the ASC switch S_2 are shown in Figure 5.27. It can be seen from the figure that turn-on and turn-off operations of the S_2 switch under all load conditions are performed with ZCS and ZCT, respectively. The current and voltage graphs of converter diode D_1 are given in Figure 5.28. In all load cases, turn-on transition is realized with ZVS and turn-off transition is realized with ZCT. Figure 5.29 and Figure 5.30 represent the output voltage and current graphs of the proposed converter under six different load conditions. It is noted that the proposed converter has a robust controller characteristic in both transient-state and steady-state conditions. With the obtained results, it is clearly seen that the proposed converter maintains soft-switching states and provides a stable output power despite the grid side disturbances.

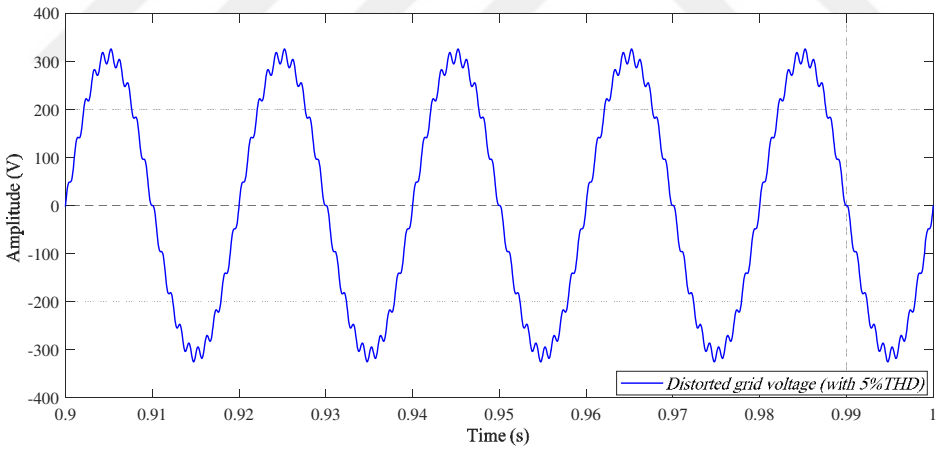

Figure 5.24. The applied distorted grid voltage waveform ($220V_{rms}$ + 5%THD)

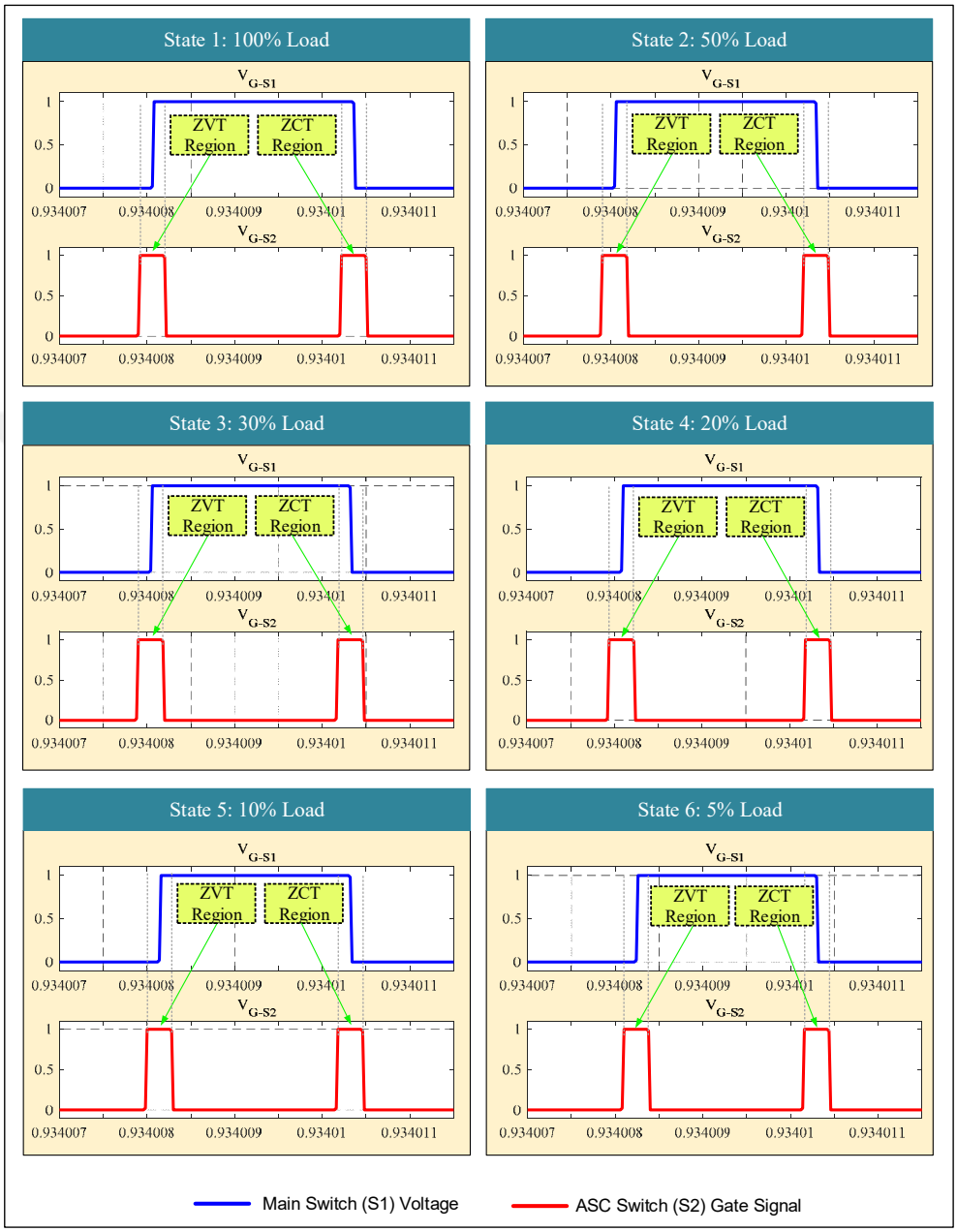

Figure 5.25. The trigger signals of the converter switches ($220V_{rms}$ + 5%THD)

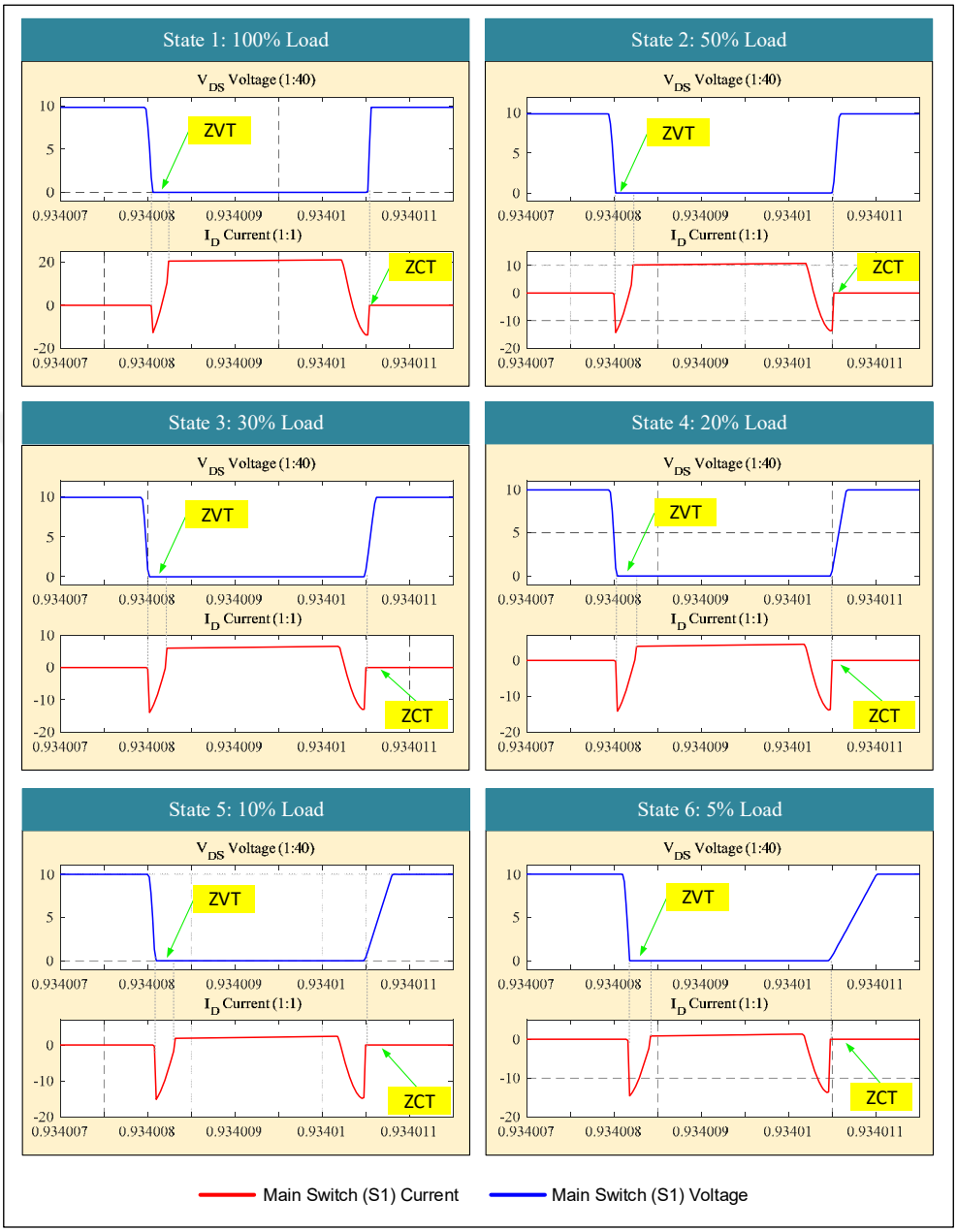

Figure 5.26. I_D current and V_{DS} voltage of the S_1 switch at different load conditions ($220V_{rms}$ + 5%THD)

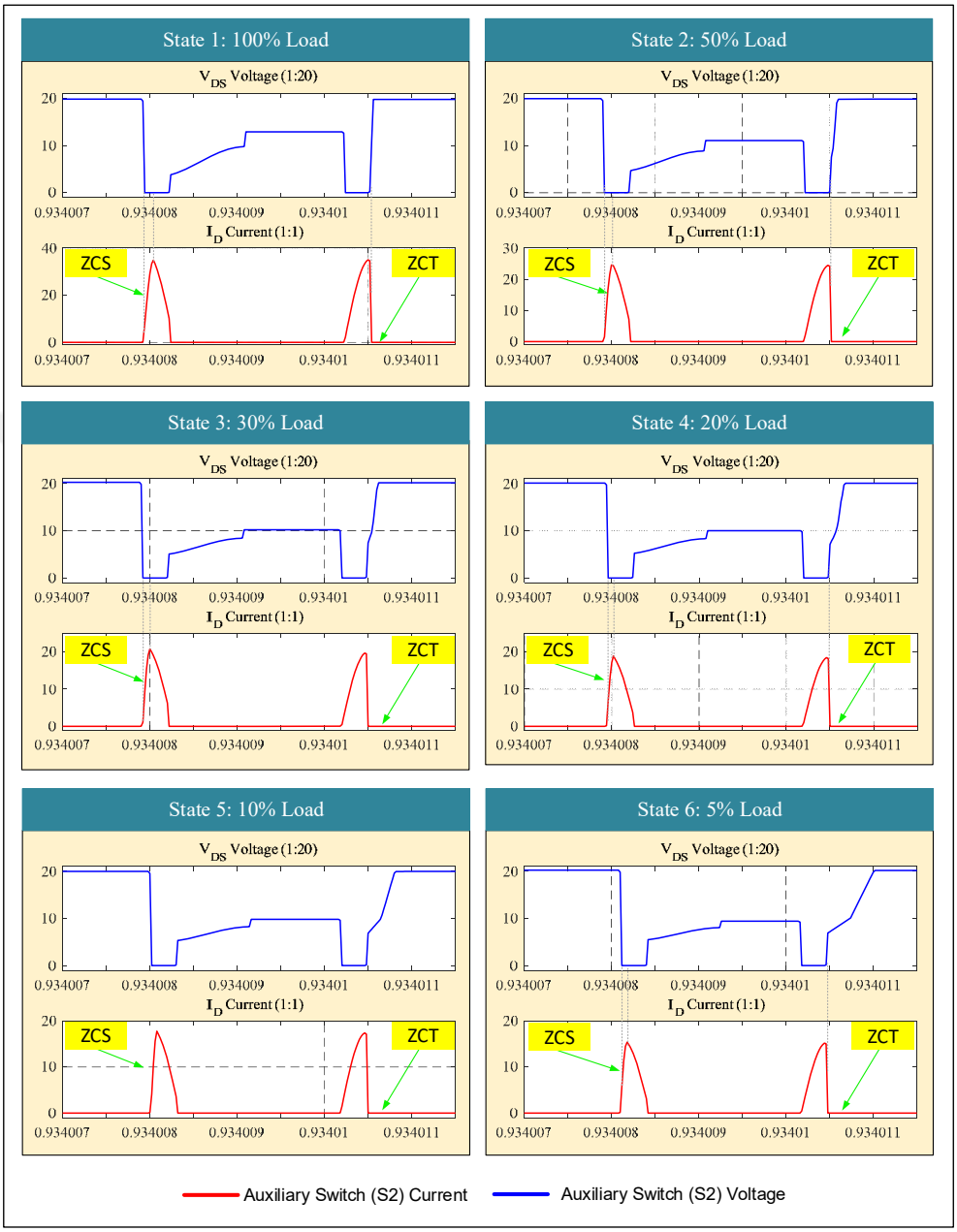

Figure 5.27. I_D current and V_{DS} voltage of the S_2 switch at different load conditions ($220V_{rms}$ + 5%THD)

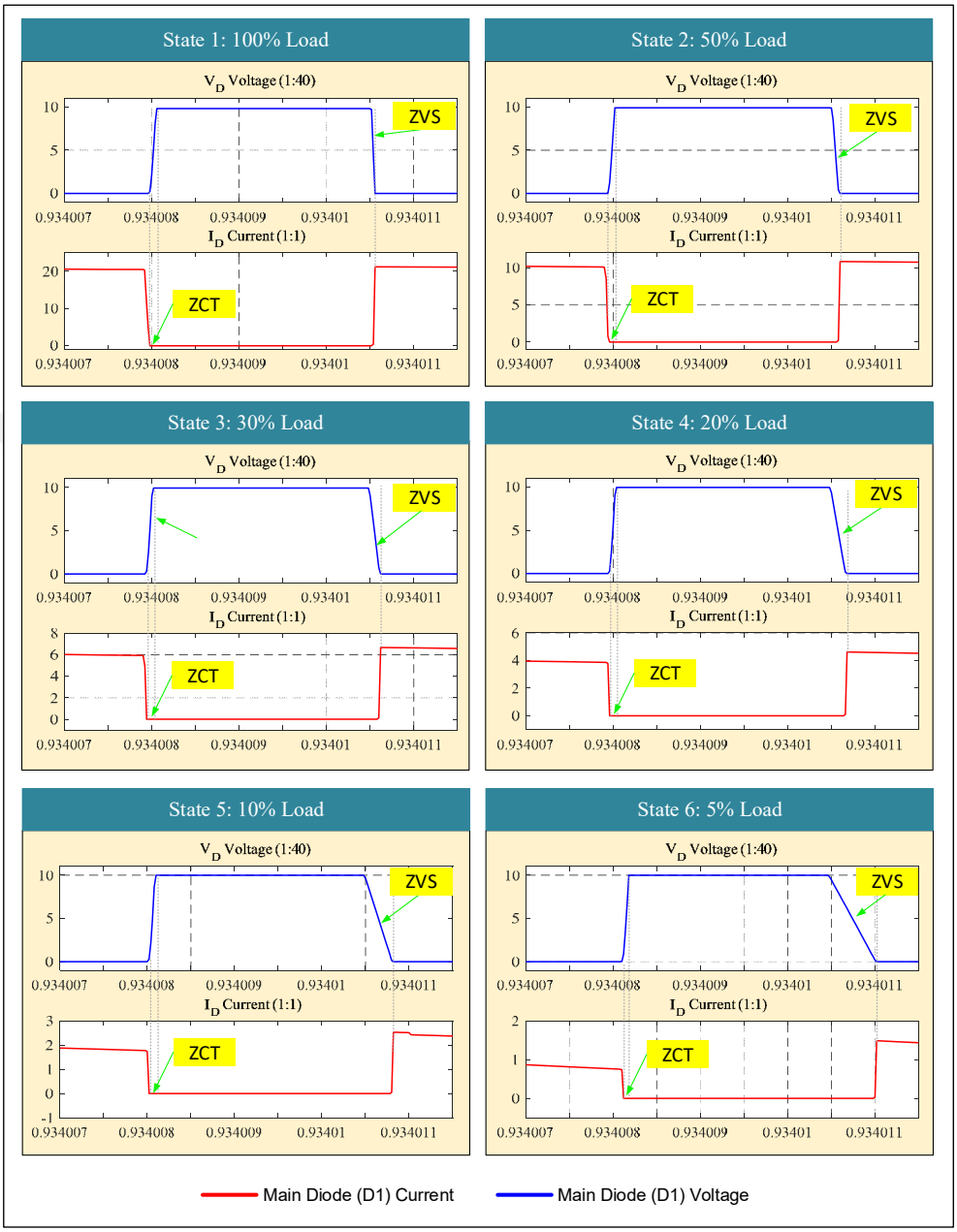

Figure 5.28. I_D current and V_D voltage of the D_1 diode at different load conditions ($220V_{rms}$ + 5%THD)

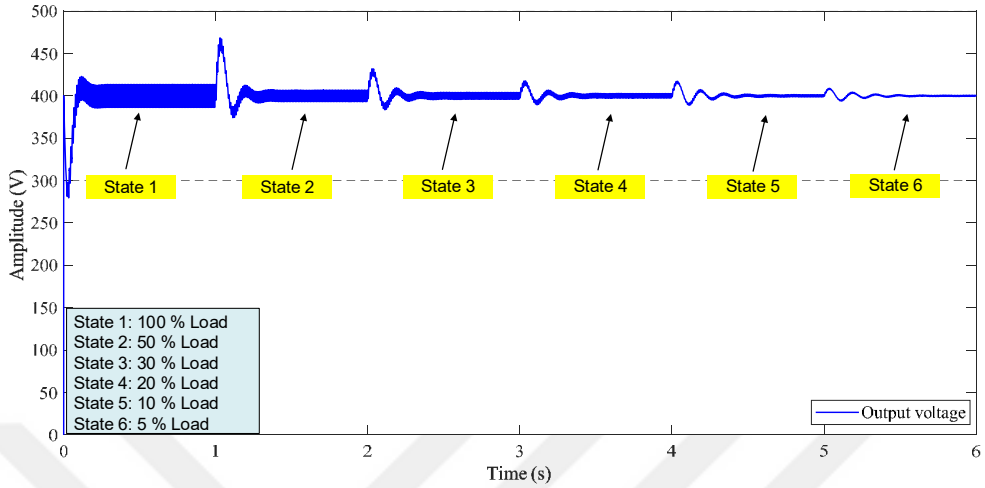

Figure 5.29. The output voltage graph of the proposed converter at different load conditions ($220V_{rms}$ + 5%THD)

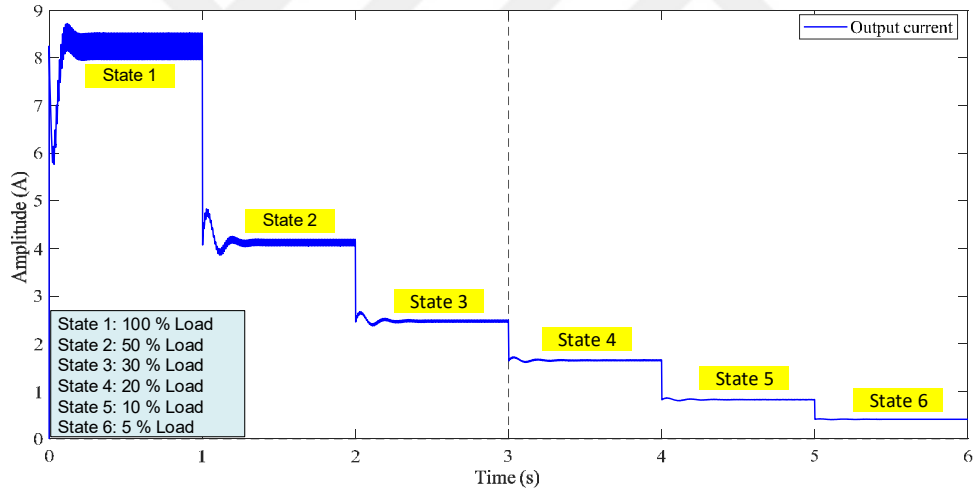

Figure 5.30. The output current graph of the proposed converter at different load conditions ($220V_{rms}$ + 5%THD)

5.7. Summary

In this section, the design and analysis of the proposed AC-DC PFC Boost converter with developed ASC are presented for the battery charger in EVs. The proposed converter has been tested under different input voltage range and different load conditions given in European efficiency standards by case studies. The proposed converter has performed high efficient performance compared to the hard switching counterpart in all conditions. SS operation and unity power factor implementation are achieved from light load to full load conditions. Furthermore, the developed ASC has a low-cost design unlike the existing ASCs, as well as does not create any current and voltage stress on the circuit elements. The proposed converter has a high power density in these aspects. The proposed converter operates in the universal input voltage range and the input current THD values are compatible with the range given in IEC 61000-3-2 standards.

6. CONCLUSION AND FUTURE WORK

In this section, the main contributions of the thesis are summarized, the concluding remarks related to the thesis are emphasized, and the aspects of the thesis for future studies are discussed.

6.1. Concluding Remarks and Discussion

The interest in EV technology has been increasing in recent years due to its superiority over traditional internal combustion engine vehicles. However, battery performance, which limits vehicle range, is still the biggest obstacle to their proliferation. Although only battery chemistry seems to affect battery performance, battery charge quality also greatly affects battery performance. Therefore, battery chargers have a critical role in the development of EV technology.

The development of battery chargers depends largely on the performance of the AC-DC PFC converter, it's the most important part. AC-DC PFC converters suffer from low power density and high output voltage ripple problems affecting the size and lifetime of the DC-link capacitor in the battery charger. To solve these problems, two different designs have been proposed in this thesis.

In the first of the proposed designs, a DVC is developed to reduce the amount of output voltage ripple of the interleaved PFC boost converter. The developed DVC aims to reduce the voltage ripple on the DC-link capacitor by creating a reverse voltage as much as the amount of voltage ripple on the capacitor. The performance results of the converter are obtained for different case studies and compared with the results of the traditional circuit (without DVC). With these case studies, it is aimed to test the performance of the converter for variable input voltages and variable load conditions at these voltage levels. In the traditional interleaved PFC boost converter, the maximum output voltage ripple occurred as 26.4V at $220V_{rms}$ input voltage and full load condition. With the developed DVC, this ripple value has been reduced to 0.5V. In addition, it has been observed that

the ripple value is kept below 0.5 for all other load conditions. In addition to reducing the amount of output voltage ripple with the proposed DVC, improvements have been observed in the efficiency of the converter and the input current characteristic. In traditional interleaved PFC boost converter, the maximum efficiency is measured as 94.11% at $220V_{rms}$ input voltage and full load, while this value has been increased to 96.75% with the developed DVC. The overall efficiency of the converter is calculated as 93.77% according to the European efficiency standards. Input PF of the converter is measured as greater than 0.99 over the entire load range. The input current THD value is maintained less than %5, which is compatible with the IEC 61000-3-2 THD standard, from half load to full load conditions. Further, to test the performance of the proposed converter in case of grid side disturbances, 5% THD was added to the grid voltage and applied to the input of the circuit. The converter performance results were obtained for six different load conditions at the applied distorted grid voltage. With the obtained results, it is concluded that the designed converter prevents the output voltage from deteriorating by compensating the disturbances on the grid side.

In the second of the designs, a new soft-switched AC-DC PFC boost converter with active snubber cell (ASC) is proposed to increase efficiency and power density. The converter switch is turned on and turned off with ZVT and ZCT thanks to developed ASC, respectively. Thus, switching losses of the converter switch are eliminated. The ASC switch is turned on and turned off with ZCS and ZCT, respectively. The main circuit diode is turned-on with ZVS and turned-off with ZCT. Also, ASC circuit diodes are turned-on and turned-off with ZCS and ZVS, respectively. Although a small amount of conduction losses occurs with the additional ASC circuit, the converter's switching losses are largely eliminated, and the converter performance is greatly improved. Furthermore, the developed ASC has a low-cost design unlike the existing ASCs, as well as does not create any current and voltage stress on the circuit elements. The performance results of the proposed converter are obtained for different case studies and

compared with the hard-switching counterpart. With these case studies, it is aimed to test the performance of the converter for variable input voltages and variable load conditions at these voltage levels. While in traditional AC-DC PFC boost converter under $220V_{rms}$ input voltage and full load 146.72W total loss occurs, this value was reduced to 73.35W in the developed soft-switched AC-DC PFC converter by eliminating the switching losses. With the elimination of switching losses, the converter's maximum efficiency increased from 95.74% to 97.82%. The overall efficiency of the proposed converter is calculated as 96.66% according to European efficiency standards. SS conditions are maintained from light load to full load conditions. Input PF of the converter is measured as greater than 0.99 over the entire load range. The input current THD value is maintained less than %5, which is compatible with the IEC 61000-3-2 THD standard and is less than the hard-switched counterpart, from half load to full load conditions. Further, to test the performance of the proposed converter in case of grid side disturbances, 5% THD was added to the grid voltage and applied to the input of the circuit. The converter performance results were obtained for six different load conditions at the applied distorted grid voltage. It is noted that the proposed converter has a robust controller characteristic in both transient-state and steady-state conditions. With the obtained results, it is clearly seen that the proposed converter maintains soft-switching states and provides a stable output power despite the grid side disturbances.

The proposed two converter topologies provide many advantages such as high power density and high efficiency. It can be clearly concluded that the proposed converter topologies can be a serious candidate for the AC-DC converter parts of the two-stage OBCs.

6.2. Future Work

Possible study topics related to this thesis planned to be carried out in the future are listed below.

- It is planned to verify the two designs whose performance is tested with theoretical and simulation studies with an experimental prototype.
- In order to improve the performance of the AC-DC PFC converter in light loads, different control methods will be applied.
- The developed SS circuit will be modified to reduce the number of elements.
- The DVC circuit will be modified and implemented with a simpler and easily controllable circuit.

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