DESIGN AND FABRICATION OF MOS SOLAR CELLS

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BY
HAYRİYE TÜTÜNCÜLER
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Approval of the Graduate School of Natural and Applied Science

Prof. Dr. Mazhar ÜNSAL
Director

I certify that this thesis satisfies all the requirements as a thesis for degree of Master of Science in Physics Engineering.

Assoc. Prof. Dr. Ata SELÇUK
Chairman of Department

We certify that we have read this thesis and in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Physics Engineering.

Assoc. Prof. Dr. M. Sadettin ÖZYAZICI
Supervisor

Examining Committee in Charge

Assoc. Prof. Dr. M. Sadettin ÖZYAZICI

Assoc. Prof. Dr. Ata SELÇUK

Assist. Prof. Dr. Zihni ÖZTÜRK

ABSTRACT

DESIGN AND FABRICATION OF MOS SOLAR CELLS

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In this thesis, effects of insulating (oxide) layer on Schottky barrier (metal-semiconductor contact) has been investigated. To make this investigation more specific minority carrier metal-oxide-semiconductor (MOS) solar cells were designed and fabricated in the form of Al-oxide-p-type silicon crystal. Resistivity of samples were measured before fabricating MOS solar cells. Aluminum coating was made by Vacuum Coater System with Diffusion Pumping System. To maximize the efficiency of the MOS solar cell, the open circuit photovoltage, short circuit photocurrent and the fill factor must be as high as possible when the total incident light energy is kept constant. But these factors depend on the same parameters and related to each other. When one parameter is increasing as a function of certain parameter, the others may be decreasing. Therefore, straightforward maximization of efficiency is not possible.

To see the effects of insulating layer thickness on the short circuit current, different oxidation techniques were used.

After device fabrication was completed I-V and C-V

characteristics of solar cells have been measured. Open circuit voltage(V_{oc}) and short circuit current (I_{sc}) which affect the conversion efficiency have been determined.

Experimental results showed that presence of positive charges in oxide layer enhance the V_{oc} as indicated by the increase in barrier height. High barrier height decreases the dark current altering the I-V characteristics in the dark.

Efficiencies of MOS solar cells were calculated as 7.3 %. This value is low as compared to published results. The reasons of getting low conversion efficiencies have been also discussed.

Key words: MIS/MOS solar cells, photocurrent, photovoltage, efficiency.

ÖZET

MOS GÜNEŞ PİLLERİNİN TASARIM VE YAPIMI

TÜTÜNCÜLER, Hayriye
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Bu tezde, oksit tabakasının metal-yarıiletken güneş pillerindeki etkisi incelenmiştir. Bu amaçla metal-oksit-yarıiletken (MOS) güneş pili, alimünyum-oksit-p-tipi silisyum kristali kullanılarak elde edilmiştir. Silisyum kristalinin özdirenci güneş pili yapımından önce belirlenmiştir. Metal kaplama işlemi vakum sisteminde yapılmıştır. Verimi yükseltmek için, ışık enerjisi sabit iken, kısa devre akımını (I_{sc}), açık devre voltajı (V_{oc}) ve düzeltme faktörünün (FF) mümkün olduğunca büyütülmesi gerekmektedır. Ancak, bu faktörler aynı parametrelere ve birbirlerine bağlı olarak değişmektedir. Bir parametre, herhangi bir parametrenin fonksiyonu olarak büyürken diğerleri küçülebilmektedir ve dolayısıyla verimin doğrudan maksimum yapılması mümkün değildir.

Oksit kalınlığının, kısa devre akımına etkisini gözleyebilmek için değişik oksitleme teknikleri kullanılmıştır. Yapılan güneş pillerinin analizi için I-V ve C-V karakteristikleri elde edilmiştir. Böylece verimi doğrudan etkileyen I_{sc} ve V_{oc} belirlenmiştir.

Oksit tabakasındaki pozitif taşıyıcıların açık devre

voltajını artırdığı deneysel sonuçlardan gözlenmiştir. Açık devre voltajının artmasıyla; bariyer yüksekliği (barrier height) artıp, karanlık akım (dark current) azalmaktadır.

MOS güneş pillerinin verimi yaklaşık % 7.3 olarak bulunmuştur. Bu değer yayınlanmış sonuçlara göre düşüktür. Elde edilen düşük verimin sebepleri de tartışılmıştır.

Anahtar Kelimeler: MIS/MOS güneş pilleri, fotoakım, fotovoltaj, verim.

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LIST OF SYMBOLS

A	Active area of the solar cell
C_{ox}	Oxide capacitance
C_{min}	Minimum capacitance
D_n	Diffusion coefficients of electrons
D_p	Diffusion coefficients of holes
E_F	Fermi level
E_{Fi}	Intrinsic Fermi level
E_C	Valance band level
E_{ox}	Electric field in the oxide
E_V	Conduction band level
E_g	Band gap of semiconductor
E_g	Energy level between vacuum level and valance band level
E_s	Energy level between vacuum level and valance band level
FF	Fill factor
$f(E)$	Fermi disribution function
G	Recombination rate
I_D	Dark current
I_{sc}	Short circuit current
I_o	Saturation Current
I_{ms}	Current flow through the metal to the semiconductor
I_p	Photocurrent
J_p	Photocurrent density
L_n	Diffusion length for electrons
L_p	Diffusion length for holes
m_e	Effective electron mass
m_p	Effective hole mass
$M(\lambda)$	Incident photon flux

n	Ideality factor
n_s	Surface electron concentration
n_{no}	Electron concentration at the top of the barrier
N_0	Electron concentration in neutral semiconductor
n_{op}	Equilibrium electron concentration in p-type substrate
N_c	Effective density of states in conduction band
N_v	Effective density of states in valance band
N_D	Donor doping density
N_A	Acceptor doping density
P_{in}	Incident light density
p_s	Surface hole concentration in the substrate
Q_b	Charge stored per unit area in depletion region
Q_s	Total charge stored in a semiconductor
Q_G	Charge density at the metal gate
R^*	Richardson constant for holes
R_s	Series resistance
R_{sh}	Shunt resistance
R_L	Load Resistance
t_{ox}	Oxide thickness
$T(\lambda)$	Transmittance into surface layer
V_b	Potential drop between metal and semiconductor
V_d	Potential drop in depletion region
V_{dif}	Diffused (built-in) potential
V_i	Potential drop in insulating layer
V_{oc}	Open circuit photovoltage
V_{gb}	Gate voltage
V_a	Applied voltage
W	Depletion region width
W_{max}	Maximum depletion region width
X_l	Collection distance for photon generated charge carriers
τ	Lifetime
ρ	Resistivity of substrate
λ_g	Wavelength of photons
ϕ_b	Energy differences between actual Fermi level and intrinsic Fermi Level

ϕ_m	Metal work function
ϕ_s	Semiconductor work function
ϕ_{bn}	Barrier height for n-type solar solar cells
ϕ_{bp}	Barrier height for p-type solar cells
ψ_s	Potential drop acroos the semiconductor
ψ_{ox}	Potential drop acrooss the oxide layer
ϵ_{ox}	Permittivity of oxide layer
μ_n	Electron mobility
μ_p	Hole mobility
η	Conversion efficiency

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CHAPTERS

CHAPTER I

INTRODUCTION

Energy need increases with an increase in housing and population. A greater part of this energy requirements is supplied from fossil fuels (coal, petroleum etc.) and electrical energy. It is now widely appreciated that the fuels and resources presently used in generating electricity may not be either sufficient or suitable to keep pace with ever increasing world demand for electrical energy. The prospects for meeting this demand would be improved if alternative energy sources were to be developed. The sun is one such source and conversion of sunlight directly into electricity via the photovoltaic effect is one method of generating solar electricity. The heart of any photovoltaic system is solar cell. It is the transducer that converts the sun's radiant energy directly into electricity.

Applications of solar cell as power supply units are given below.
1-Warning lights (railroad signals airport, light beacon etc.).
2-Communication systems (remote communications, portable radio, stations for TV etc.).
3-Water systems (water purification, pumps in desert region).
4-Security systems.

Metal oxide semiconductor (MOS) solar cell has properties which are in general intermediate between those of Schottky

barrier (metal semiconductor contact) and p-n junction. The dark current in MOS device may be dominant either by majority carriers or by minority carriers. This creates two types of MOS solar cells, the so called majority-carrier and minority carrier cells. The photocurrent, of course, is in both cases due to excess carriers.

MOS solar cells have been studied by many workers as a low cost alternative to the p-n junction solar cells and they are significantly simpler to fabricate. They are also formed at low temperature without any appreciable degradation in the bulk properties of the semiconductor.

MOS structures with ultrathin oxide layers exhibit many interesting properties by the virtue of direct tunnelling current which flow between metal and semiconductor.

The insertion of a very thin insulating layer between the metal and semiconductor of a Schottky contact can make a dramatic difference to its operation. The insulator must be thin enough that appreciable current can flow through it by tunnelling and other mechanisms. The presence of native oxide on the surface of the semiconductor produces interface states whose nature and density depends on the oxide semiconductor combination. A number of experimental investigation [1-4] shows that presence of a thin oxide layer between metal and semiconductor increases open circuit voltage of Schottky barrier without any appreciable decrease in short circuit current. A number of theories [5-9] has been advanced in the recent past to explain the characteristic of these cells. In MOS solar cells the oxide energy band gap is considered to be too high to lead to any sunlight absorption and, providing that the insulator is kept thin enough (15-20 Å), tunnelling through the oxide does not cause photocurrent bottleneck. Thus in the absence of photocarrier recombination via surface states introduced at the semiconductor-oxide interface, the factors that govern the attainable value of short circuit

current can be same in MOS cells for intimate metal semiconductor solar cells. This results in a net increase in the efficiency of MOS cell.

It was established by Green et al.[8]-[10] that if the insulator was thin enough (<20 A^0), then;
(a) the dominant carrier flow for a given semiconductor type can be controlled by selection of the metal work function;
(b) if the contact metal work function and substrate dopant type (p or n) are chosen so that minority-carrier current flow is dominant, the MOS diode so formed is electrically equivalent to a conventional p-n junction diode. For Si substrate, minority carrier operation can be obtained if the insulating layer is kept <16 A^0, and low work function metals (Al, Be, Mg) are used with p-type substrate and high work function metals with n-type.

In contrast to Schottky devices, such minority carrier MOS devices possess the same photovoltaic abilities as p-n junction solar cells [3]. Early indication of this was provided when electron voltaic efficiencies for minority MOS devices were found to be better than comparable diffused p-n junction devices [10]. The work of Green et al. [8]-[10], several groups [11-15] have reported results for MOS cells, with varying degrees of successes.

To couple the light into the semiconductor surface, two approaches have been used. In the transparent metal structure, the top metal layer is made very thin (typically <100 A^0) to let light through , and a conventional coarse grid is put over this to reduce series resistance. For the grating structure [8]-[15], the metal contact is not continuous but consists of thick metal lines spaced closely enough together to collect a majority of the carriers generated between them. The first reported results which showed reasonable experimental cell parameters by applying this approach. Active area efficiencies up to 13 percent were

projected from measured values of I_{sc} and V_{oc}. Using modified approach, fabricated cells have much higher efficiency [16]-[17].

The enhancement of Schottky-barrier height by charges within the SiO_2 layer on p-type silicon substrate is discussed in [18]. A comprehensive MIS solar-cell theory based on the majority-carrier dark current is discussed in [19-21]. Current transport theory in minority-carrier MIS device is discussed in [22]. The role of interface states is analyzed in [5]-[7], assuming these states are in equilibrium with the metal or with majority carriers in the semiconductor. Arguments indicating that the interface states are in equilibrium with minority carriers under conditions of (solar) illumination are presented in [7] and experimental evidence is shown in [15]-[23]. Numerical analysis of MIS solar-cell performance is presented in [8]-[24].

The first aim of this thesis is to design and to fabricate MOS structure solar cell. The second aim is to improve the performance and the stability of MOS solar cell. Parameters which are related to the device efficiency is analyzed by using the I-V and C-V characteristics of MOS solar cell. Effects of the oxide charges and interface states in the Si-SiO_2 interface are investigated. Barrier height modification caused by interfacial layer containing positive charge is demonstrated and this effect is seen as a possible explanation for the high barrier heights recorded.

This thesis starts from the above point of view at first and gives review about the metal semiconductor contacts in chapter II. Chapter III, starts from explanation of sun and sunlight and description of photovoltaic effect. Then it analyses MOS silicon solar cells and presents calculation of solar cell performance. After discussion of material parameters for determining the efficiency, the electrical characteristics of silicon solar cell are derived.

In chapter IV, design and construction of minority carrier MOS solar cell is given. The theory of experimental sets are explained in this chapter. The experimental results are obtained from fabricated MOS structure solar cells and design criterions are also discussed in this chapter.

Finally, last chapter is dedicated to overall conclusions and remarks.

CHAPTER II

REVIEW OF METAL-SEMICONDUCTOR CONTACT

2.1 INTRODUCTION

In order to observe electric current, it is necessary to make contacts with crystals by suitable metals. Metal semiconductor junctions are both the simplest and the oldest of semiconductor devices. Metal semiconductor junctions have long been known by the alternative name of Schottky barriers or Schottky diodes in recognition of German Physicists Walter Schottky, who did much to develop theory of these devices and investigate techniques for their fabrication in 1930s.

2.2 BAND MODEL OF SOLID CRYSTAL

According to the band theory the energy level diagram of a semiconductor (or insulator) crystal is shown in Figure 2.1. There, the bottom of the conduction band is taken as the reference level and "vacuum level" represents the energy of an electron at rest far away from the crystal.

"Fermi level" is the energy level that the probability of an electron to occupy it is 1/2. It can be defined as the energy level above which there is no electron at absolute zero. The probability that an electronic state with energy E is occupied by an electron is given by the Fermi-Dirac distribution function

$$F(E) = \frac{1}{[1+\exp[-q(E_F-E)/kT]]} \qquad (2.1)$$

where k is the Boltzmann constant, T is absolute temperature in degrees Kelvin, and E_F is the Fermi level.

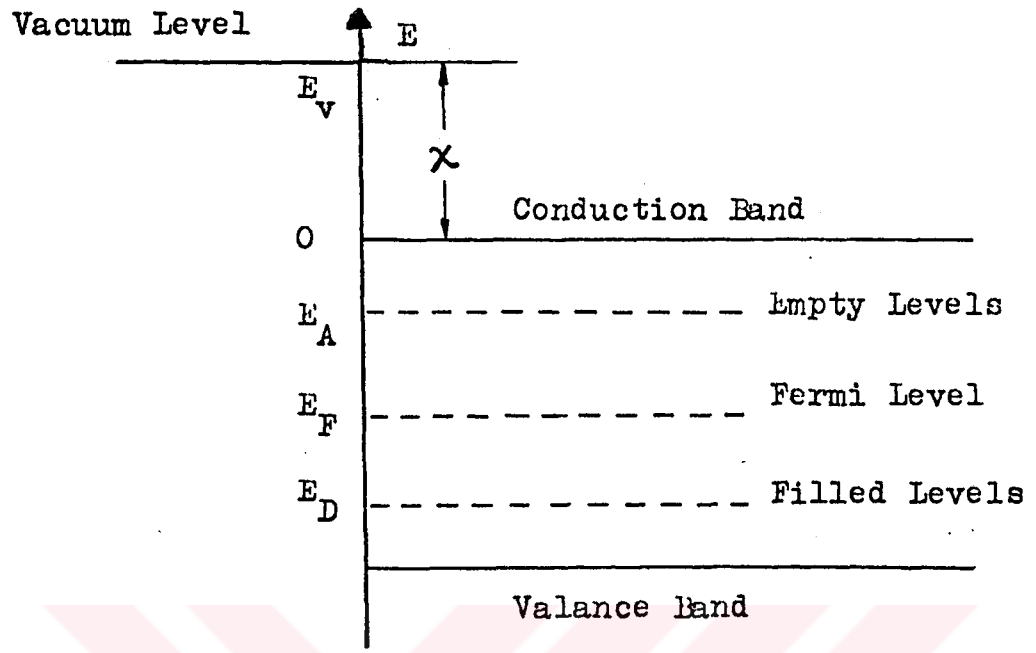

Figure 2.1 Energy band diagram of semiconductor.

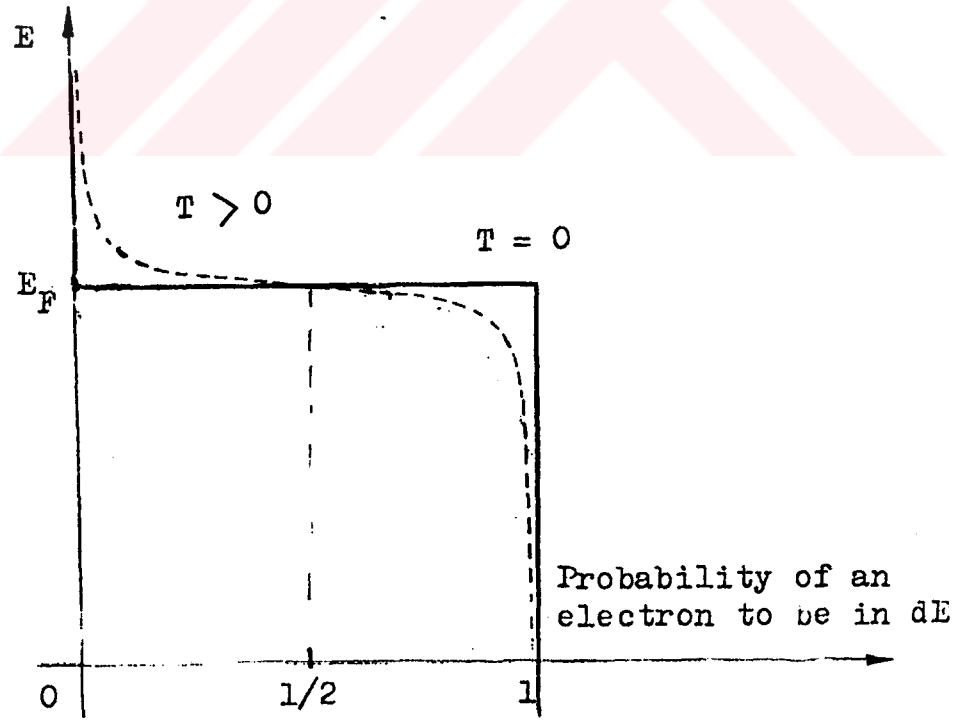

Figure 2.2 Probability of an occupation of electron in a specified energy level.

"Work Function", ϕ is defined as the energy needed for an electron to jump from Fermi level to the vacuum level is given as

$$\phi = E_v - E_F = \chi - E_F \qquad (2.2)$$

where E_v is the energy level of valance band, and χ is the electron affinity which is the energy difference between the vacuum level and the bottom of conduction band.

2.3 ENERGY BAND RELATION AT METAL-SEMICONDUCTOR CONTACTS

When two substances are brought into contact, a redistribution of charge occurs, finally a new equilibrium condition is reached in which the Fermi levels of two substances are at equal heights. This rule holds true not only for contacts between a metal and n-type or p-type semiconductor but also contacts between metal and metal.

Owing to the redistribution of charge, a dipole layer will be formed at the contact. In a metal-metal contact this dipole layer is always caused by surface charges on both sides of the contact; such a contact is an ohmic contact, since the electrons can move easily from the one metal into the other.In a metal-semiconductor contact, however, the contact may either be ohmic or rectifying. The latter is a contact in which the current flows much more easily in one direction than in opposite. We shall see that this is intimately connected with electronic-energy level diagram of two substances.

Consider a contact between metal and an n-type semiconductor as shown in Figure 2.3. Let the donor concentration in the semiconductor be relatively large, and let almost all donors be ionized at room temperature. Let ϕ_m be the work function of the metal, ϕ_s the work function of the semiconductor, and χ_s the electron affinity of the semiconductor.

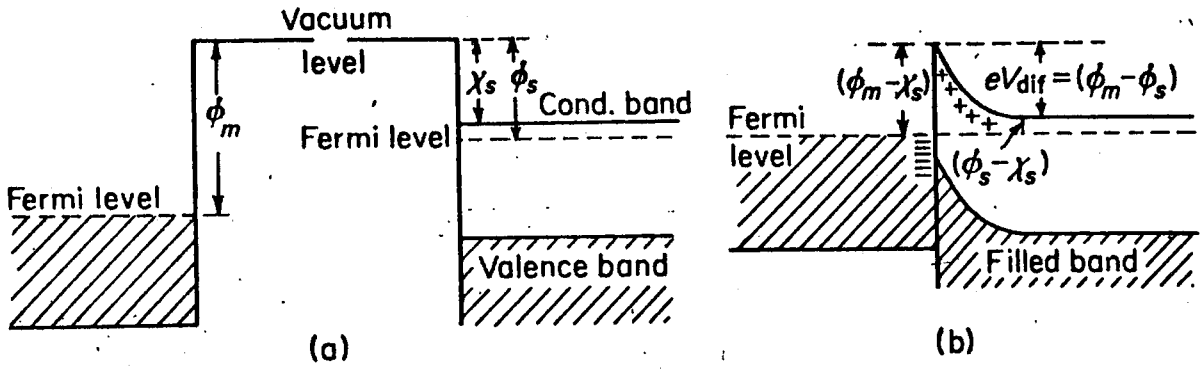

Figure 2.3 Energy-level diagram of a metal n-type semiconductor with $\phi_m>\phi_s$.(a) Energy-level diagram before contact. (b) Energy-level diagram after contact.

Let us first consider the case $\phi_m>\phi_s$. The situation before contact is shown in Figure 2.3a; the Fermi level of the semiconductor is then above the Fermi level of the metal by an amount $\phi_m-\phi_s$. After contact, an exchange of charge is completed, the Fermi levels in both materials are at same height; this means that the energy levels in the bulk semiconductor are lowered by the amount $\phi_m-\phi_s$; on the metal side, since the Fermi levels are at the same height of the barrier is $(\phi_m-\phi_s)+(\phi_s+X_s)=(\phi_m-X_s)$ as in Figure 2.3.b. Expressed in volts, the height of barrier follows from

$$eV_{dif}=\phi_m-\phi_s \qquad (2.3)$$

The quantity V_{dif} is known as diffusion potential(built in). The potential at the interior of the semiconductor, taken with respect to metal surface, is V_{dif}.

This potential difference is maintained by the electric dipole layer at the contact. Since the positive charge at the semiconductor side of contact is caused by ionized donor atoms in a metal, and these donors are bound to fixed positions, the positive charge does not occur as a surface charge but as distributed charge instead. For that reason the

surface charge layer of this metal-semiconductor contact is called the space charge layer. Because of the potential barrier at the contact, the surface layer is also known as barrier layer. The thickness of this layer depends upon the concentration of ionized donors and upon the value of the diffusion potential.

Owing to thermal agitation, some electrons of the metal will have enough energy to cross the potential barrier into the metal. In equilibrium, this gives rise to equal and opposite current crossing the barrier.

If a voltage $-V_a$ is applied to the semiconductor as shown in Figure 2.4, the barrier for electrons going from left to right has not changed, and hence the corresponding current from right to left has not changed either. But since the energy levels in the conduction band have been raised to left, the barrier for electrons going from right to left has been lowered by an amount eV_a; as a consequence the corresponding current from left to right has changed by a factor $\exp(qV_a/kT)$. Consequently, the characteristic is

$$I_D = I_o[\exp(qV_a/kT) - 1] \qquad (2.4)$$

This is rectifying contact;for $V_a >> kT/q$ the current is large and positive and $V_a << kT/q$ the current is small and almost equal to $-I_0$. The first bias condition is called forward bias and the second bias is called reverse bias.

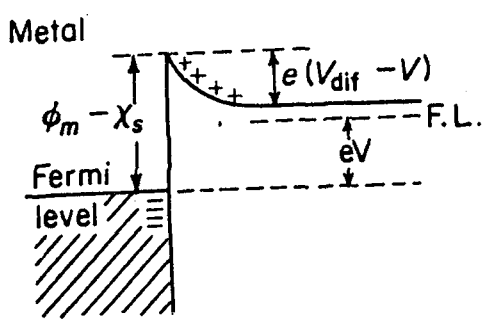

Figure 2.4 A voltage -V is applied to the semiconductor.

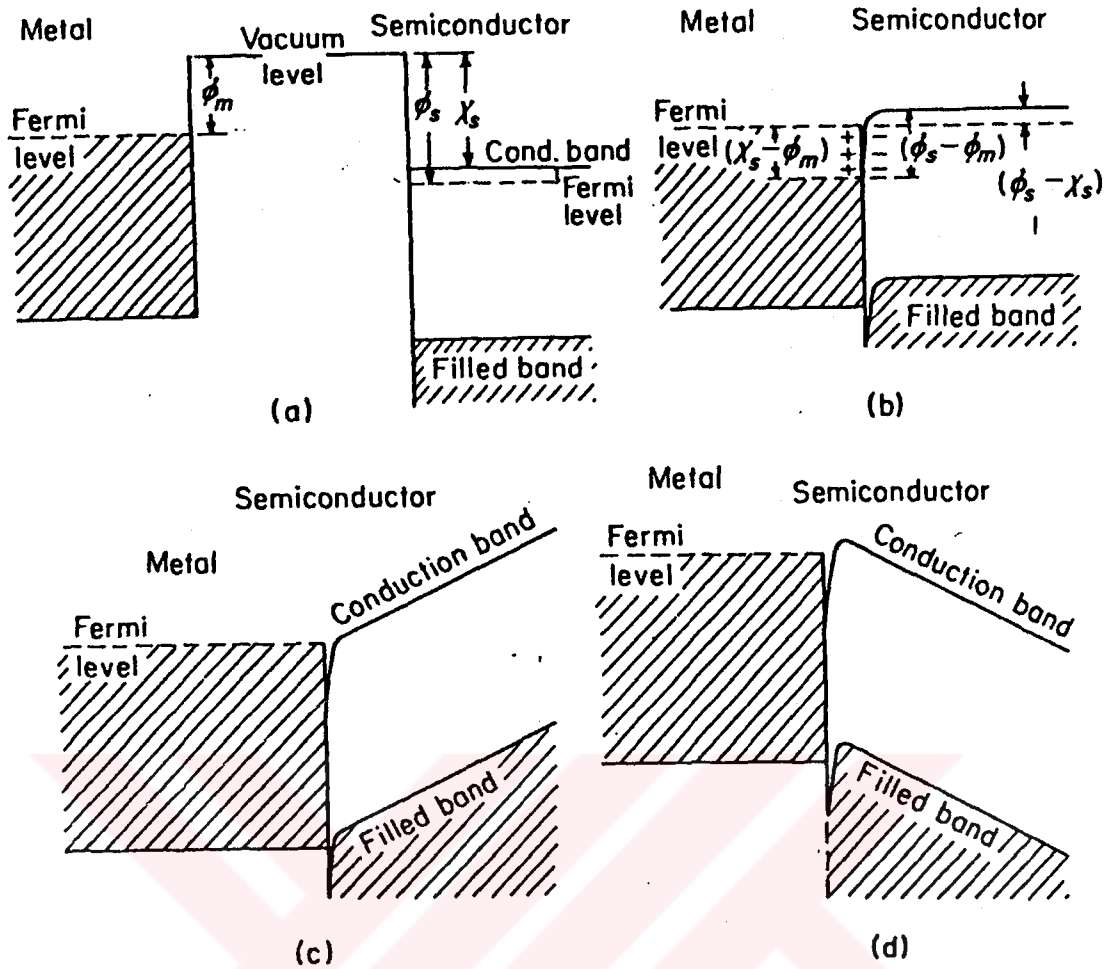

Figure 2.5 Energy-level diagram of a metal n-type semiconductor contact (ohmic). (a) Energy-level diagram before contact. (b) Energy-level diagram after contact. (c) A negative voltage is applied to the contact. (d) A positive voltage is applied to the contact.

Up to now we have considered the case $\phi_m > \phi_s$. If $\phi_m < \phi_s$, no rectifying barrier formed. The situation before contact is shown in Figure 2.5a. An exchange of charge takes place after contact, electrons flow from the metal into the surface layer of the semiconductor, leaving a positive surface charge at the semiconductor side of the contact. The Fermi level in the semiconductor bulk material is thereby raised by an amount $\phi_s - \phi_m$, as in Figure 2.5b. If a voltage V is applied, this potential difference not taken up the contact area as in previous case, but is distributed across the bulk semiconductor. (Figures 2.5c and d)

We see that electrons can move across the barrier without much difficulty, especially if $\phi_s-\chi_s$ is relatively small. The contact may thus be considered an ohmic contact.

After our discussion of the metal n-type semiconductor contact, the discussion of the metal p-type semiconductor contact will be as follows. Let E_s is the depth of the top of the filled band of the semiconductor below the vacuum level. The contact is now rectifying if $\phi_m<\phi_s$ and ohmic is $\phi_m>\phi_s$

Consider the latter case first. The situation before contact is shown in Figure 2.6a; the Fermi level in the semiconductor is above the Fermi level in the metal by an amount $\phi_m-\phi_s$. After contact, an exchange of charge takes place; electrons flow out of semiconductor, leaving a positive surface charge(due to holes) behind on the semiconductor by an amount $\phi_m-\phi_s$ is shown in Figure 2.6b. Holes from the semiconductor can readily move into the metal and be neutralized almost instantly (because of the high electron concentration), and for opposite polarity of the applied voltage the holes formed thermally in the conduction band of the metal can readily move into the semiconductor. The contact is thus ohmic.

We now consider the case $\phi_m<\phi_s$. After contact , electrons flow from the metal into the semiconductor until the fermi levels of the semiconductor and the metal are at equal height. The surface layer of the semiconductor will thereby become negatively charged, and since this negative charge is caused by ionized acceptors, the charge is distributed through a space charge layer of thickness d. Since the energy levels in the bulk semiconductor have been raised by an amount $\phi_s-\phi_m$, the surface barrier for holes on the semiconductor side is shown in Figure 2.7a. In this case, V_{dif} is given as

$$\phi_s-\phi_m=eV_{dif} \qquad (2.5)$$

Owing the thermal agitation, some holes of the semiconductor will gain enough energy to cross the potential barrier into

the metal, and some of the holes generated thermally in the metal will have enough energy to cross the potential barrier into the semiconductor, thus giving rise to two equal and opposite current I_0 crossing the barrier.

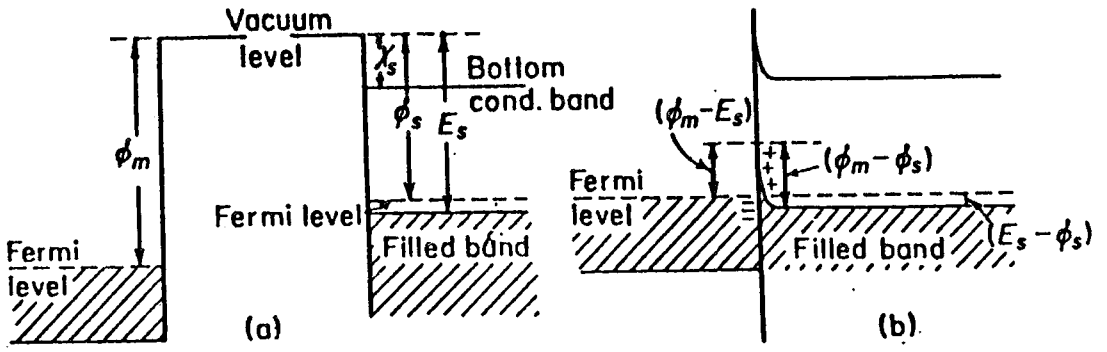

Figure 2.6 Energy-level diagram of a metal p-type semiconductor (ohmic). (a) Energy-level diagram before contact. (b) Energy-level diagram after contact.

As shown in Figure 2.7b, if a voltage V_a is applied to the semiconductor, the hole current flowing from left to right has not changed; but the hole current flowing from right to left has changed by a factor $\exp(qV_a/kT)$, since all the energy levels in the semiconductor have been lowered by an amount eV_a. Hence the barrier height for holes going from right to left has been lowered by an amount eV_a.

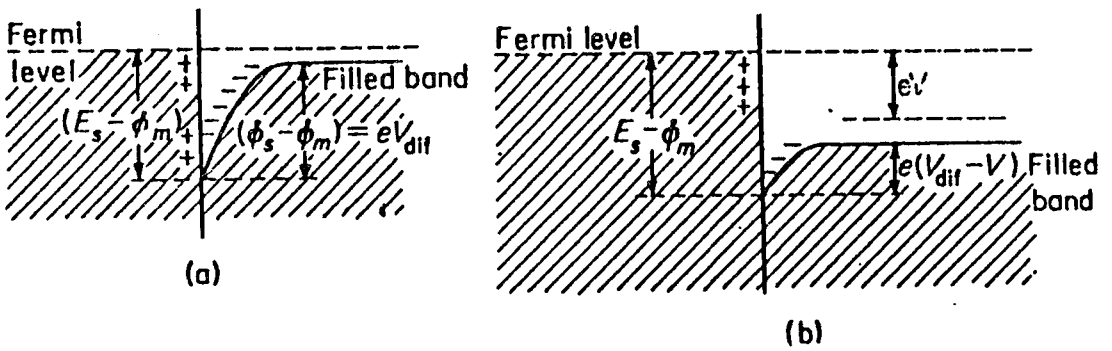

Figure 2.7 The energy-level diagram of a metal p-type semiconductor contact if $\phi_m < \phi_s$. (a) No voltage applied. (b) A voltage V>0 is applied to the semiconductor.

2.4. TRANSPORT OF CURRENT IN SCHOTTKY DIODES

There are various ways in which current can be transported

a metal-semiconductor contact under forward bias (the inverse process occur under reverse bias). The mechanisms are:
(a) thermionic emission of electrons from the semiconductor over the top of the barrier into a metal
(b) quantum mechanical tunnelling through the barrier
(c) recombination in the space charge region
(d) recombination in neutral region

Thermionic emission is usually the dominant current mechanism in Si and GaAs Schottky diodes and leads to the ideal diode characteristic. Tunnelling and carrier generation and recombination in depletion region cause a departure from the ideal behaviour. Therefore, we will take into account only thermionic emission in here.

Before an electron is emitted into the metal over the barrier, it has to pass through the depletion region in the semiconductor. The electron motion with in the depletion region is governed by the drift and diffusion processes, while its emission into metal is determined by the density of available states in the metal. The two processes are essentially in series, and the one that causes the larger impediment to the electron flow determines the current. In high mobility semiconductor like Ge, Si, and GaAs, the current is limited by thermionic emission over the barrier. Consequently, we will ignore the effect of drift and diffusion in the barrier region in the following discussion.

Electrons that have energy higher than $q(V_{dif}-V_a)$ can reach the top of barrier. Assuming a Maxwellian distribution of velocities [26], we observe that the electron concentration at the top of the barrier is given by

$$n_{no}=N_o\exp\left[-q(V_{dif}-V_a)/kT\right] \qquad (2.6)$$

where N_0 is the electron concentration in the neutral semiconductor. It is equal to for n-type material

$$N_o=N_c\exp\left[-q(E_c-E_F)/kT\right]=N_c\exp(q\phi_{bn}/kT) \qquad (2.7)$$

$$n_{no}=N_c\exp\left[-q(\phi_{bn}-V_a)/kT\right] \qquad (2.8)$$

where

$$N_c=\sqrt[2]{(2\pi m^*kT/h^2)^3} \qquad (2.9)$$

If the electrons have an isotropic distribution of velocities, then from the kinetic theory of gases the electron flux incident on the barrier is $vn_{no}/4$. Assuming that all electrons incident on the barrier cross into metal, we see that the current I_{sm} flowing from metal to semiconductor becomes

$$I_{ms}=-qA\frac{v}{4}N_c\exp\left[-q(\phi_{bn}/kT)\right] \qquad (2.10)$$

Here v is the average thermal velocity of the electrons in the semiconductor.

Since the barrier height for electrons moving from the metal into the semiconductor remains the same, the current flowing into the semiconductor must therefore be equal to the current flowing from the semiconductor into the metal under thermal equilibrium, when $V_a=0$. Since no net current flows in this situation, we must have

$$I_{sm}=-qA\frac{v}{4}N_c\exp\left[-q\phi_{bn}/kT\right] \qquad (2.11)$$

When voltage V_a is applied, the barrier height $q\phi_{bn}$ remains practically unchanged, and thus I_{sm} becomes constant. Writing $I_{sm}=I_o$ and combining Eq.(2.9)and(2.10) lead to

$$I_D=I_o\left[\exp(qV_a/kT)-1\right] \qquad (2.12)$$

For a Maxwellian distribution, v is given as [26]

$$v=\sqrt{\frac{8kT}{\pi m_e}} \qquad (2.13)$$

Substituting for N_c from Eq.(2.9), we can write the saturation current I_0 as

$$I_o=AR^*T^2\exp(-q\phi_{bn}/kT) \qquad (2.14)$$

where

$$R^*=\frac{(4\pi m_e qk^2)}{h^3} \qquad (2.15)$$

R^* is the Richardson constant for the thermionic emission of electrons from the metal into semiconductor having electron effective mass 'm_e'.

Richardson constant for the thermionic emission of holes (p-type semiconductor) from the metal into the semiconductor having hole effective mass 'm_p', is

$$R^{**}=\frac{(4\pi m_p k^2)}{h^3} \qquad (2.16)$$

The metal-semiconductor contact is simpler in principle (because it also provides the device electrode which will be connected to the external circuit) but in fact it is difficult to be realized with the desired properties.

Metals on highly doped semiconductors form good ohmic contacts (for practical purposes we shall consider a contact to be ohmic even itself does not obey Ohm's Law, provided that this contact can supply the required current with a sufficiently small voltage drop). However, a number of wide-band-gap semiconductors present contacting problems. Because they cannot be doped heavily enough.

CHAPTER III

THEORY OF MOS SOLAR CELLS

3.1 INTRODUCTION

Solar cells make use of photovoltaic effect, namely the absorbtion of photons to create equal numbers of positive and negative charges which then can be separated to develop a photovoltage and photocurrent, so allowing power to be delivered to an external load.

All of MOS cell, the metal-SiO_2-Si cell is the most extensively studied. There are number of phenomena so far neglected in the analysis of an ideal MOS structure and these are:

1- The existence of metal-semiconductor work function difference.

2- The mobile electric charge trapped in surface states localized at the insulator-semiconductor interface

3- The electric charge within the insulator layer.In a real MOS structure , these phenomena must be taken into consideration. In this chapter, theory of an ideal MOS solar cell is discussed.

3.2 THE SUN AND SUNLIGHT

Any discussion of solar cell and solar energy should begin with a look at the energy source. In our case it is the sun that has a mass of about 10^{24} tons, a diameter of 865,400 miles, and radiates energy at a rate of approximately $3.8*10^{20}$ MW. Present theories predict that this output will

continue essentially unchanged for several billion years.

Between the sun and earth there is a hard vacuum and a distance which varies from 92 million to 95 million miles. The distance variation implies, using the inverse-square law, that the light energy reaching the earth in June is 94% of the light energy reaching the earth in December. This quantity is called solar constant, and it is equal to,

$$SC=0.1353\ W/cm^2$$

This power density is available 24 hours a day, each day of the year, yielding annual energy flux of 1.186 kWh/cm^2.

Once the sunlight has reached the earth's atmosphere a number of additional effects becomes important. Those effects resulting from weather and light absorption by water vapour, ozone, and other atmospheric constituents are reducing the energy density of sunlight at earth's surface.

The optical air mass, m, is defined as the path length of radiation through the atmosphere considering vertical path at sea level as unity. Air mass zero (m=0), written as AMO is obviously the condition in space. Air mass one, AM1, is the condition at the sea level with zenith on a clear day. Optical air mass m also can be defined by m=1/cosZ where Z is the angle between a line vertical to observer and a line through the observer and the sun; Z=0 gives m=1,AM1 condition, Z=60 gives m=2,AM2 condition [28].

The solar spectral irradiance, is defined as the power density per unit wavelength, may be presented as a time and wavelength.

3.3 THE PHOTOVOLTAIC EFFECT

The photovoltaic effect is a process by which a voltage is produced at the junction of two different materials (e.g., a metal-semiconductor or a p-n junction) through an incident photon flux. In a p-n junction photons of sufficient energy incident upon the semiconductor produce hole-electron pairs. Some of these holes and electrons diffuse toward the junction and if they are created sufficiently close to it, have a high probability of reaching it before they recombine. At the junction they are separated by the barrier. If they are created at the p-side of the junction and diffuse toward the junction, the electrons will be swept across the junction into the n-side whereas the holes will be blocked by the barrier. If the hole-electron pairs diffuse in from the n-side of the junctions, the holes are swept into the p-side by the barrier while the electrons are blocked.

The carriers which are swept across the barrier are the minority carriers in the region in which they are generated and their flow through the barrier constitutes reverse current. If there are no exterior connections to the device (open circuit condition) the charge which accumulates on either side of the junction reduces the barrier height. This reduction causes the forward current to increase. The forward current results from the passage of thermally produced majority carriers across the barrier. An equilibrium condition is quickly established which results in an open circuit voltage intermediate between zero and full barrier voltage. If the illumination is sufficiently intense to annihilate the barrier , the photovoltage has reached its saturation value.

In order to obtain a high photovoltaic efficiency the following requirements have to be met:
(a) The energy per photon has to be slightly greater than the band gap energy.
(b) The impurity concentration has to be high and temperature low.

(c) The surface reflectivity has to be small.

The product of photovoltage and photocurrent represents the net flow of energy from the solar cell to the external load, energy coming from the sun and converted from photon-energy to the electrical energy with in the solar cell.

3.4 BASIC STRUCTURE OF MOS SOLAR CELL

At the surface of any solid there is an energy barrier holding the electron in. This barrier exists simply because it is energetically more favourable for electrons to be close to the positively charged ion cores in the solid's interior. The energy required to take an electron from inside the solid and release it to exterior is an important property of any material. Naturally, since electrons in the solid can have range of energies, more precise definition of this energy barrier is required. For a semiconductor, it is useful to work with the electron affinity $q\chi$, which is defined as the energy needed to take an electron from the bottom of the conduction band and deposit it at rest in vacuum just outside solid. When dealing with a metal, it is more convenient to work with the energy required to remove an electron at the Fermi energy and place it at rest outside. This energy difference is the work function $q\phi_m$ of the metal. Since there are large number of electrons in the metal with the energies close to the E_F, $q\phi_m$ is a good measure of the minimum energy required to tree en electron from the metal. Energy band diagrams for the surface regions of a metal, a semiconductor and a SiO_2 are shown in Figure 3.1.

The basic structure of MOS solar cell is shown in Figure 3.2 The device consists of a thin metal gate overlying an oxide layer and thick metal underlying the semiconductor.

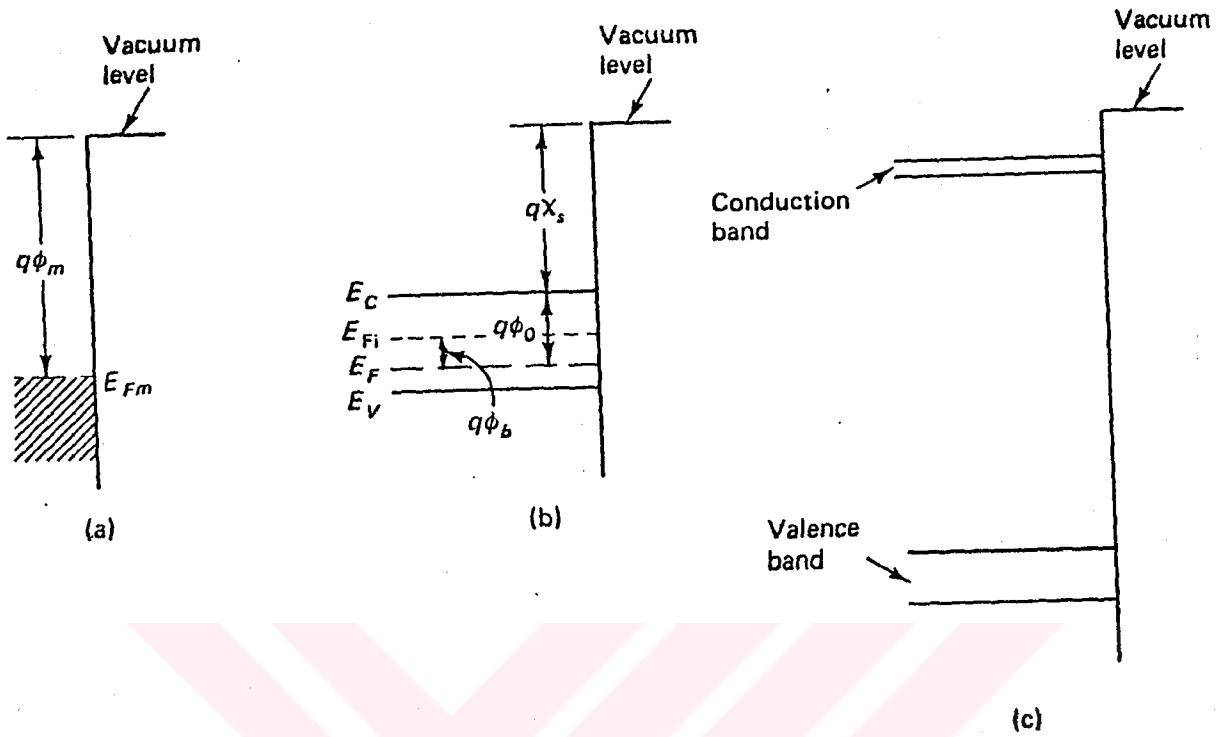

Figure 3.1 Energy band diagrams for surface regions (a) a metal, (b) silicon, and (c) silicon dioxide

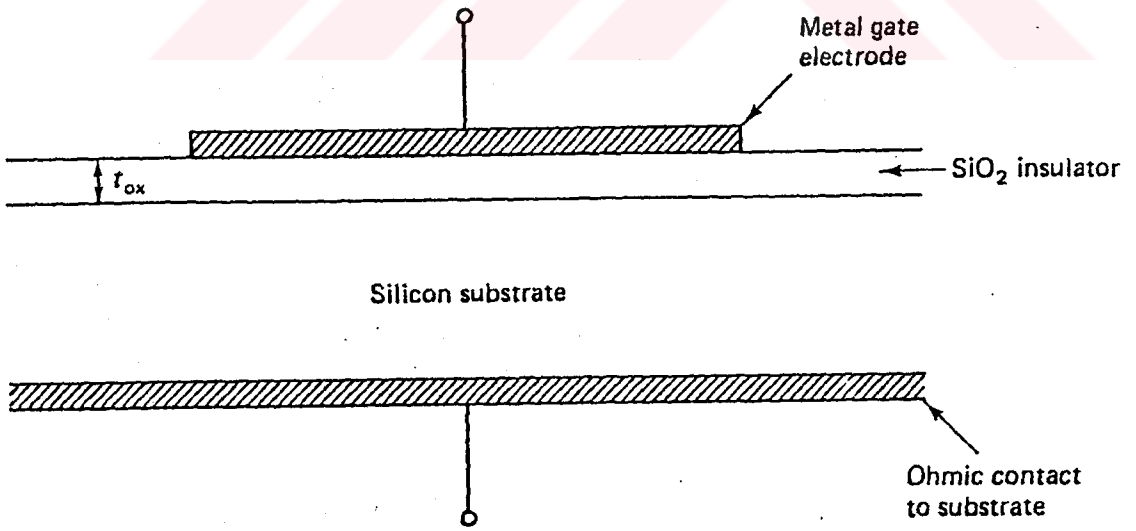

Figure 3.2 Structure of MOS solar cell.

A complete energy band diagram for a MOS solar cell formed on a p-type silicon substrate is shown in Figure 3.3a. For most

purposes it is possible to represent the solar cell with the simplified band diagram of Figure 3.3b, which shows only the conduction and valence band diagram, the metal work function $q\phi_m$ is replaced with a modified work function $q\phi_m'$ defined by

$$\phi_m' = \phi_m - \chi_{SiO_2} \tag{3.1}$$

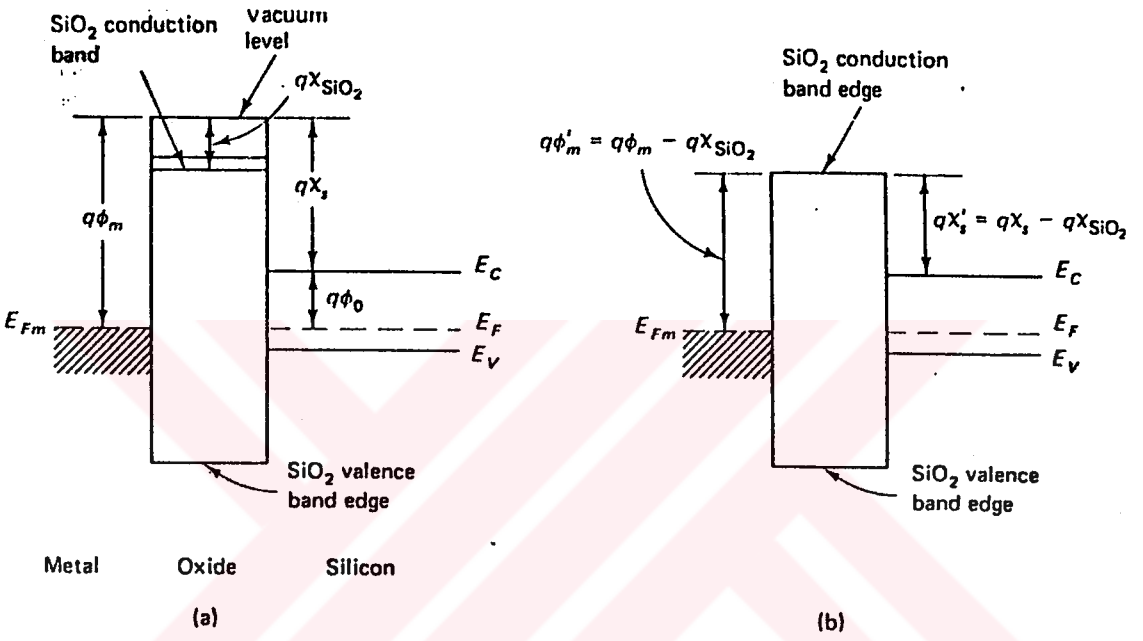

Figure 3.3 (a) Complete band diagrams for MOS cell, showing energy band structure of SiO_2. (b) Simplified band diagram.

Before proceeding further with analysis of MOS solar cell, it is useful to introduce two parameters related to doping level in the substrate. The first of these is energy difference $q\phi_0$ between the conduction band edge and the Fermi level measured in deep in the bulk substrate, well away from the influence of the gate electrode.

$$\phi_o = \frac{kT}{q} \ln\left(\frac{N_C}{N_o}\right) \tag{3.2}$$

where N_0 is the equilibrium electron concentration in the substrate. ϕ_0 is illustrated in Figure 3.3b. Technically work

function of a semiconductor is defined as

$$\phi_s=\chi_s+\phi_o \tag{3.3}$$

which emphasizes the dependence of the ϕ_s on doping. A second useful parameter is the energy difference $q\phi_b$ between the actual Fermi level E_F and intrinsic Fermi level E_{Fi}. For p-type substrate with acceptor doping N_A, ϕ_b is given

$$\phi_b=\frac{kT}{q}\ln\left(\frac{N_A}{N_i}\right) \tag{3.4}$$

Similarly for n-type substrate with donor doping N_D,

$$\phi_b=\frac{kT}{q}\ln\left(\frac{N_i}{N_D}\right) \tag{3.5}$$

It should be noted that in this case ϕ_b has been defined as a negative quantity. The band diagram of Figure 3.3 implies to the situation in which $V_{gb}=0$. So that Fermi energies in the gate and substrate coincide. In drawing this figure it has been assumed that the work functions of the metal and semiconductor are equal, and there is no trapped charge in the silicon at zero applied bias.

When positive bias is applied to the gate, holes are repelled from semiconductor surface, so band bends as shown in Figure 3.4. As holes leave the surface, ionized acceptor ions are left behind, forming a surface depletion region. The applied bias V_{gb} can be viewed as splitting into two parts: a potential drop Ψ_{ox} across the oxide layer and potential drop Ψ_s across the semiconductor. These quantities are defined to be positive when the direction of bending is that shown in Figure 3.4. Adding up energy differences on moving from left to right in Figure 3.4, we find that

$$\phi_m'+\psi_{ox}=V_{gb}+\phi_o-\psi_s+\chi_s'=V_{gb}+\phi_s'-\psi_s \tag{3.6}$$

so, since we are assuming that $\phi_m'=\phi_s'$

$$V_{gb}=\psi_s+\psi_{ox} \tag{3.7}$$

It is important to note that the Fermi energy E_F has been drawn flat across the semiconductor in Figure 3.4. This comes about since there can be no net current through the oxide layer, in consequence, no steady state current in the substrate.

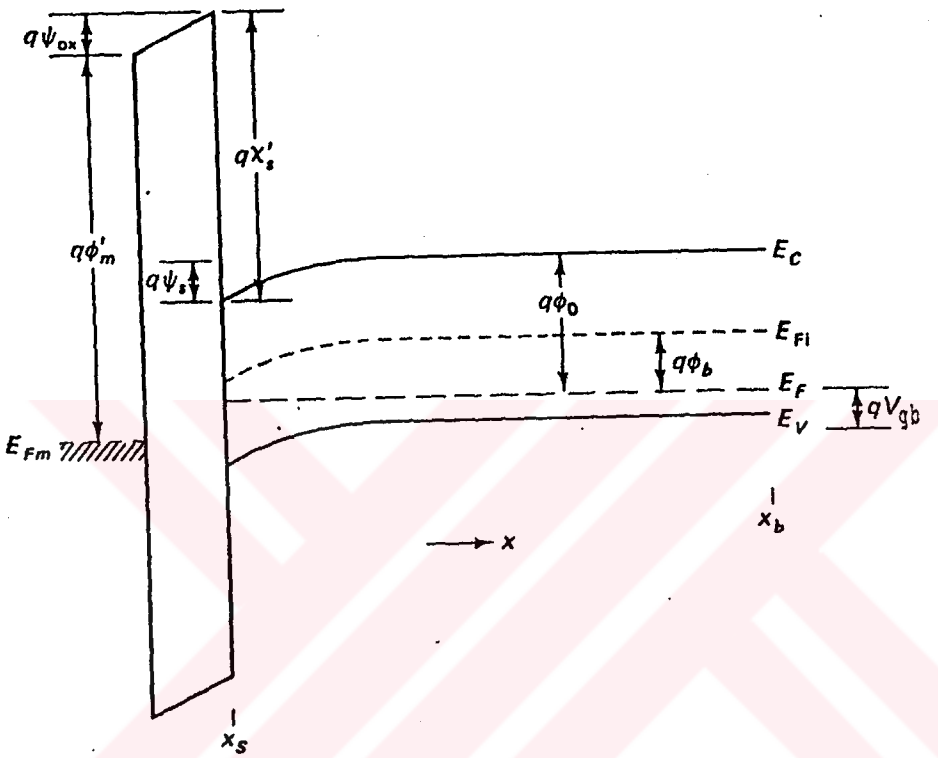

Figure 3.4 MOS cell band diagram for positive applied bias.

The potential drop Ψ_{ox} across the oxide can be related to the total charge per unit area Q_s stored in the semiconductor through the Gauss's law.

Deep in the semiconductor substrate the electric field should go to zero, so there is no contribution to flux through the Gaussian volume from the bottom surface. Also there is no flux contribution from the sides of Gaussian volume, since the electric field lines run parallel to the sides. Letting E_{ox} be electric field in the oxide, we have

$$\epsilon_{ox}E_{ox}=-Q_s \tag{3.8}$$

where ϵ_{ox} is the permittivity of the oxide. (Here E_{ox} has been defined to be positive when pointing in the positive x-direction in Figure 3.4) Since $\Psi_{ox}=E_{ox}t_{ox}$, we find

$$\Psi_{ox}=-\frac{t_{ox}}{\epsilon_{ox}}Q_s \tag{3.9}$$

or in terms of oxide capacitance

$$\Psi_{ox}=-\frac{Q_s}{C_{ox}}$$
$$C_{ox}=\frac{\epsilon_{ox}}{t_{ox}} \tag{3.10}$$

C_{ox} is usually termed the oxide capacitance;it is the capacitance per unit area one would measure in MOS solar cell

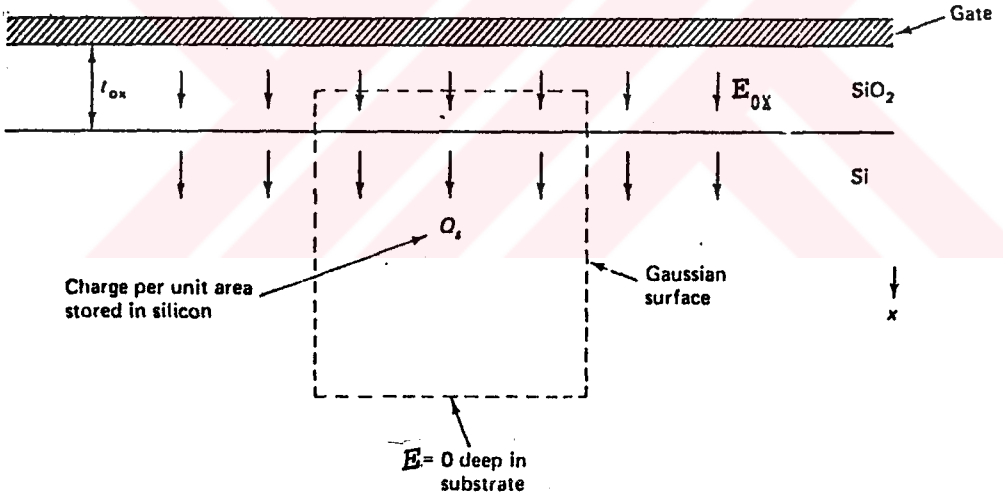

Figure 3.5 Gaussian volume used to relate charge Q_s stored in semiconductor to field ϵ_{ox} in the oxide.

If V_{gb} is increased further, the bands in the semiconductor will continue to bend downward, as suggested in Figure 3.6a. At this point the surface concentration n_s is equal to hole concentration p_s. Further increase in V_{gb} will make n_s greater than the p_s, so this bias point is said to mark the onset of inversion. At inverted semiconductor surface the minority

carrier concentration is greater than the majority carrier concentration.

The surface electron concentration is given by

$$n_s = N_C \exp\left[\left[E_F - E_C(x_s)\right]/kT\right] \qquad (3.11)$$

where $E_C(x_s)$ is the energy of conduction band edge at the semiconductor surface x_s. From Figure 3.4, $E_C(x_s) = E_C(x_b) - q\Psi_s$, where $E_C(x_b)$ is the conduction band energy at the semiconductor contact x_b. So

$$\begin{aligned} n_s &= N_C \exp\left[\left[E_F + q\psi_s - E_C(x_b)\right]/kT\right] \\ &= N_C \exp\left[\left[E_F - E_C(x_s)\right]/kT\right] \exp\left[q\psi_s/kT\right] \\ &= n_{op} \exp\left(q\psi_s/kT\right) \end{aligned} \qquad (3.12)$$

where n_{op} is the equilibrium electron concentration in the p type substrate. Since inversion requires that $n_s > N_i$, at the onset of inversion

$$N_i = n_{op} \exp\left[q\psi_s/kT\right] = \frac{N_i^2}{N_A} \exp\left[q\psi_s/kT\right] \qquad (3.13)$$

therefore

$$\psi_s = \frac{kT}{q} \ln\left(\frac{N_A}{N_i}\right) = \phi_b \qquad (3.14)$$

If V_{gb} is increased further, the bands in the semiconductor will bend still more, the conduction band edge at the surface will move closer to E_F, and the surface electron concentration will increase. The total charge per unit area Q_s stored in the semiconductor must therefore split into a part Q_b associated with ionized acceptor ions in the depletion region, and a part Q_n associated with electrons near the surface; that is.

$$Q_s = Q_n + Q_b \qquad (3.15)$$

The ionized acceptor ions are of course, fixed in lattice, but the electrons are mobile and can move in response to an electric field to the silicon surface.

As V_{gb} is increased, the electron concentration near the surface will at first be insignificant compared to the acceptor ion concentration. In this regime, the semiconductor is said to be weak inversion. In depletion or weak inversion, it is possible to compute the width of the depletion region using the depletion approximation [26]. Thus we have

$$W = \sqrt{\frac{2\epsilon_s \psi_s}{qN_A}} \qquad (3.16)$$

where ϵ_s is the permittivity of the semiconductor. However, if V_{gb} is increased sufficiently, a point will eventually be reached at which surface electron concentration exceeds the acceptor ion concentration, as suggested in Figure 3.6c. This bias is said to mark the onset of strong inversion, and the region at the semiconductor surface with this concentration of electrons is called inversion layer.

Once strong inversion sets in further increase in V_{gb} are absorbed almost entirely as changes in the potential drop ψ_{ox} across the oxide while the band bending ψ_s across the semiconductor remains relatively constant. The depletion region width therefore saturates at a maximum value W_{max}. The reason for this is as follows. Eqn.(3.13) shows that a relatively small change in ψ_s produces a large change in n_s. In fact, it is easy to show that an increase in ψ_s of only 60 mV will increase n_s by an order of magnitude at room temperature. In strong inversion, a large increase in the charge Q_s stored in the semiconductor. However, since ψ_s is related to Q_s by Eqn.(3.10), a relatively small increase in

Ψ_s must therefore produce a large increase in Ψ_{ox} while Ψ_s increases very little. Physically, the electrons in inversion layer can be thought of as a screening the semiconductor from changes of in potential at gate electrode.

The value of V_{gb} that must be applied to just create a condition of strong inversion at the silicon surface is known as the threshold voltage V_T, and is one of the most important parameters describing any MOS solar cell. To obtain strong inversion, we need $n_s=N_A$, or

$$N_A=\frac{N_i^2}{N_A}\exp\left[q\psi_s/kT\right] \tag{3.17}$$

so

$$\psi_s=2\frac{kT}{q}\ln\frac{N_A}{N_i}=2\phi_b \tag{3.18}$$

The depletion region width at threshold is therefore given by

$$W_{max}=\sqrt{\frac{2\varepsilon_s(2\phi_b)}{qN_A}} \tag{3.19}$$

so the ionized acceptor charge per unit area Q_b stored in the depletion region is given by

$$Q_B=-qN_AW_{max} \tag{3.20}$$

Although at threshold the electron concentration at the silicon surface is equal to the acceptor ion concentration, throughout most of the depletion region, it assumed that, $Q_s=Q_b$, so

$$V_T=\psi_s+\psi_{ox}=2\phi_b+\frac{\sqrt{(2\varepsilon_s qN_A 2\phi_b)}}{C_{ox}} \tag{3.21}$$

If V_{gb} is made negative, holes are attracted to the silicon surface, and the band diagram appears as shown in Figure 3.6d. In this case surface is accumulated, with the excess holes forming an accumulation layer. The surface concentration is given by

$$p_s = p_o \exp[-q\psi_s/kT] \qquad (3.22)$$

where $p_0 = N_A$ is the equilibrium hole concentration in the bulk Just as in the case of the strong inversion , once an accumulation layer forms, further increase in the magnitude of V_{gb} lead to very little change in Ψ_s. The high density of charge in the accumulation layer screens in the interior of the semiconductor, so that increase in V_{gb} are absorbed entirely by changes in Ψ_{ox} rather than Ψ_s.

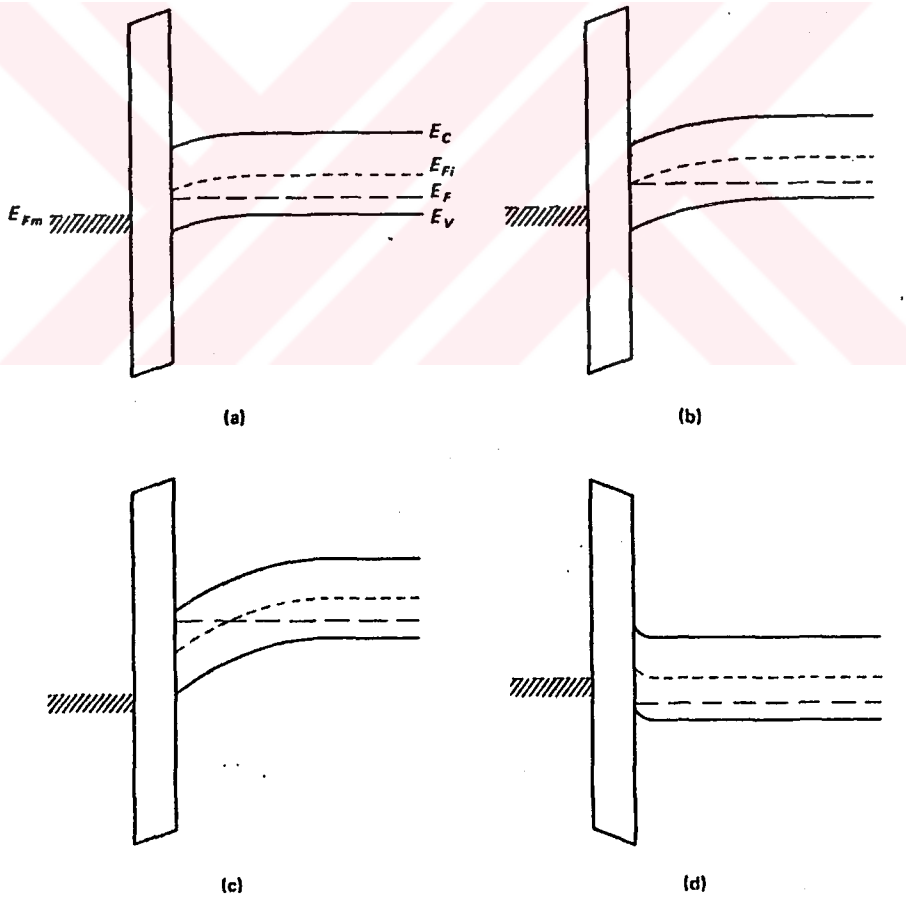

Figure 3.6 Band diagrams for various bias conditions in the MOS cell: (a) depletion, $0<\psi_s<\phi_s$; (b) onset of inversion, $\psi_s=\phi_b$; (c) strong inversion, $\psi_s=2\phi_b$; (d) accumulation, $\psi_s<0$.

At this point it is worth summarizing that may be encountered in the MOS solar cell. For $\Psi_s<0$, the surface is in accumulation. If $0<\Psi_s<\phi_b$, the surface is depleted. The surface is becomes inverted once $\Psi_s>0$. For $0<\Psi_s<2\phi_b$, the surface is only in weak inversion, with free electrons making a negligible contribution to ϕ_s. For $\Psi_s>2\phi_b$ the surface becomes strongly inverted.

3.5 SOLAR CELL EQUIVALENT CIRCUIT

By connecting a load across the terminals of a solar cell a current I_L can flow through the load and develop a voltage V_L across it. The values of V_L and I_L, besides depending on the nature of the load, will be related to the photogenerated current I_p and properties of MOS diode. These relationships and properties can be established by reference to the simple equivalent circuit shown in Figure 3.7, where imperfections in the diode leading the current leakage are represented by shunt resistance R_{sh} and parasitic resistance effects are represented by R_s. From the Figure 3.7, it is seen that

$$I_L\left(1+\frac{R_s}{R_{sh}}\right)=I_p-I_D-\frac{V_L}{R_s} \qquad (3.23)$$

which shows that both diode current and voltage are effected by the presence of R_s and R_{sh}.

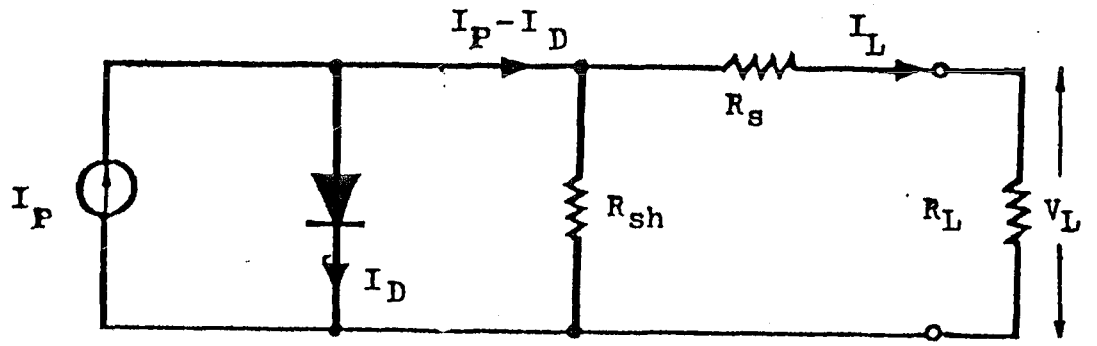

Figure 3.7 Simple equivalent circuit of solar cell.

It is important for R_s to be small and for R_{sh} to be large.

Typical desired values for silicon cells are R_s<0.5 Ohm, R_{sh}>500 Ohm

The actual operating point of a given solar cell I-V characteristic is determined by the value of the load resistance R_L such that biasing occurs at the maximum power (I_m,V_m) shown in Figure 3.8. The energy conversion efficiency can be described by

$$\eta = \frac{I_m V_m}{P_i A} \qquad (3.24)$$

where P_i is the incident solar power density and A is the active area of solar cell. Defining the ratio of $I_m.V_m$ to $I_{sc}.V_{oc}$ as the fill factor "FF", a further expression for η can be written as where I_{sc} is the short circuit current, V_{oc} is the open circuit voltage

$$\eta = \frac{(FF)\, I_{sc} V_{oc}}{P_i A} \qquad (3.25)$$

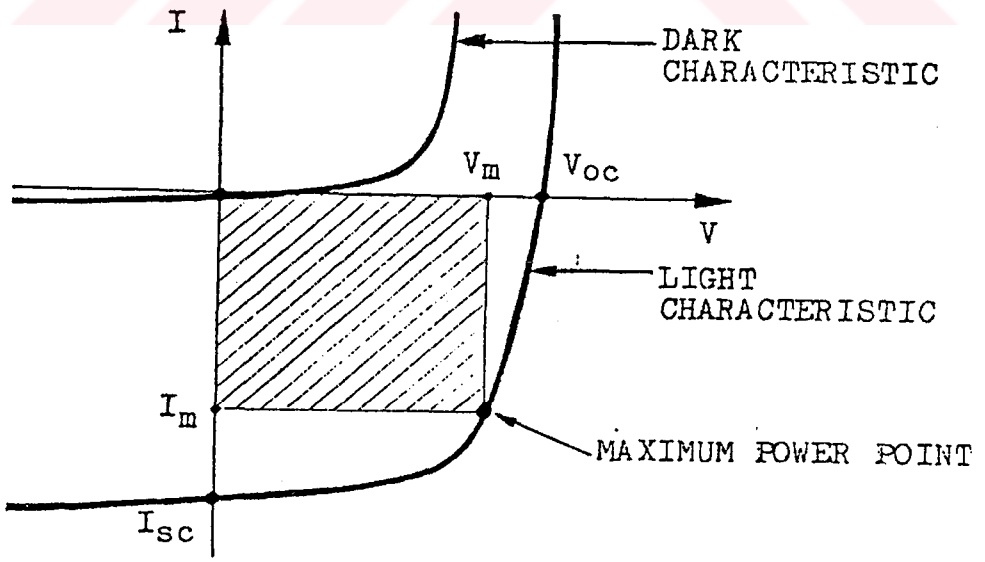

Figure 3.8 Solar cell I-V characteristics.

3.6 IMPORTANT MATERIAL PARAMETERS FOR SOLAR CELL DESIGN

To relate the terminal properties of solar cell, designer should examine some parameters for getting high efficiency.

3.6.1 Energy Gap

The energy gap of pure silicon is accurately known. At room temperature, 300K, it is 1.120 eV. In the range near and somewhat above room temperature where solar cells are usually operated, the energy gap decreases linearly with temperature as described by

$$E_g=1.120-2.8*10^4(T-300) \qquad (3.26)$$

3.6.2 Intrinsic Carrier Concentration

The intrinsic carrier concentration is instrumental in determining the dark saturation current and hence open circuit voltage of a solar cell. Its variation with absolute temperature is given by

$$N_i=3.87*10^{16}T^{3/2}\exp(-E_{go}/kT) \qquad (3.27)$$

where E_{go}=1.120 eV and k is Boltzmann's constant. At room temperature this expression gives $N_i=1.37x10^{10}$. It increases by a factor of 2.23 in the next 10 K.

3.6.3 Mobilities and Diffusion Coefficients

The electron and hole mobilities in pure silicon are given by

$$\mu_n=1360\left(\frac{T}{300}\right)^{-2.42} \qquad (3.28)$$

$$\mu_p = 495\left(\frac{T}{300}\right)^{-2.20} \qquad (3.29)$$

In doped silicon these parameters are described by impurity scattering, falling roughly a factor of 10 as the impurity concentration increases from 10^{16} to 10^{19} /cm3. At higher donor or acceptor concentrations, the semiconductor behaves "metallic" and mobilities assume nearly constant values, $\mu_n = 90 cm^2/V/sec$ and $\mu_p = 48 cm^2/V/sec$

The output of a solar cell is derived from the diffusive flow of minority carriers to some form of collecting junction so the diffusion coefficient D is more direct concern than the mobility. They are connected by Einstein relation $D = \mu kT/q$.

$$D_n = 35.1\left(\frac{T}{300}\right)^{-1.42} \qquad (3.30)$$

$$D_p = 12.7\left(\frac{T}{300}\right)^{-1.20} \qquad (3.31)$$

3.6.4 Minority Carrier Lifetime

The minority carrier lifetime, the mean time interval between generation and recombination of charge carrier, is a major property that is fundamental in determining the effectiveness of a semiconductor as a photovoltaic candidate. By a recombination process excess electrons and holes in a semiconductor recombine and tend to restore the system to the thermal equilibrium condition given by

$$pn = N_i^2 \qquad (3.32)$$

The lifetime (τ) also depends upon the quality of the starting material and upon many details of the cell fabrication.

3.6.5 Diffusion Length

The photogenerated carriers in the absorbed semiconductor must be able to move across that region of the junction. Carriers that recombine before arriving at the junction are lost the photovoltaic effect and cannot take part in the generation of photocurrent. Diffusion is mechanism with which the minority carriers move to the depletion region. Therefore, minority carrier diffusion length is a most important material parameter. Electrons and holes have characteristic diffusion lengths (L_n and L_p, respectively that are material dependent.

The diffusion lengths can be expressed in terms of basic material parameters and they depend on the impurity concentration, crystallinity, crystal orientation, defect concentration and stoichiometry. The decrease of minority carrier diffusion length with doping density in silicon is shown Fig. 3.9 [30].

$$L_n=\sqrt{D_n\tau_n} \qquad (3.33)$$

$$L_p=\sqrt{D_p\tau_p} \qquad (3.34)$$

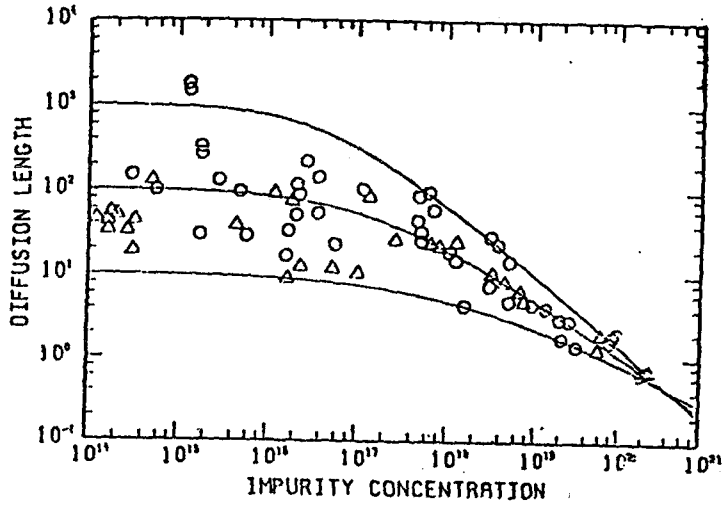

Figure 3.9 Variation of diffusion length with impurity concentration in Si.

The decrease of minority carrier diffusion length with doping density in silicon is shown in Figure 3.9. Two regions of Figure 3.9 are of particular interest. The substrate, or base region, typically has a thickness of 100-200 micrometers and doping level in the range 10^{15}-10^{17} /cm^3.

Efficient current collection from the base region requires a diffusion length that is greater than the cell thickness.

3.7 THE EFFECTS OF INSULATING LAYER

Silicon has become the principal semiconductor material primarily because SiO_2 is film can be grown on it. Band gap of SiO2 is 8.2 eV. These oxide films are dense, uniform and stable over wide range of temperatures. This allows the use of this oxide as a barrier to selectively mask against the diffusion or ion implantation of dopants. Furthermore, this oxide film and the Si-SiO_2 interface determine the electrical characteristics of devices built in the silicon substrate. The various charges that may be present in insulating layer are illustrated in Figure 3.10. As seen from there are positive charges in insulating layer due to bond structure.

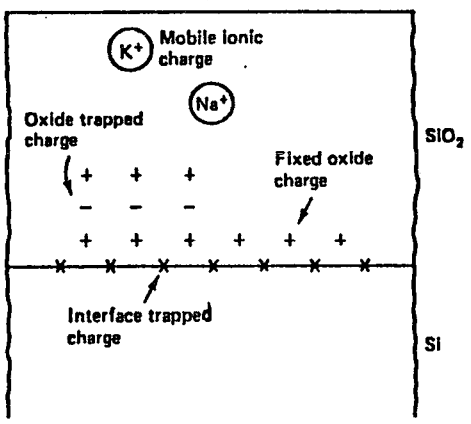

Figure 3.10 Various oxide charges in insulating layer.

The insulating layer (SiO_2) has two effects:
1- Because of potential drop in the layer, the zero-bias barrier height is higher than it would be in Schottky diode.
2- When a bias is applied, part of the bias is dropped across the insulating layer so that the barrier height is a function of the bias voltage. The effect of this bias dependence of the barrier height is to change the shape of current-voltage characteristics.

Silicon dioxide films can be either grown or growth on silicon substrate.The essential aim of oxide preparation, including subsequent treatments, is to produce films with the following characteristics.
1- Ideal interface or an interface characterized by an ideal C-V curve shifted along the voltage axis .
2- Good insulating properties, i.e; high breakdown strength, high dielectric constant, and low dielectric losses.
3- Resistance to ambient stress.
4- Resistance to attack by the atmosphere.
5- Resistance to the radiation.

The oxide layer protects the surface from environmental contamination, and acts as a barrier against the diffusion of impurities into the semiconductor underneath, thus improves device performance.

The tunnelling is the dominant current mechanism for all the heterojunctions. Tunnelling can occur either as a field emission (FE) or as thermionic field emission (TFE). Tunnelling would have a significant increase in diode current because it represents in parallel with thermionic emission. At low temperature, electrons near the Fermi level of semiconductor can tunnel into the metal through the thin oxide layer. This process known as field emission. If the temperature is increased, electrons are excited to higher energy levels and these electrons can tunnel into the metal before reaching the top of the barrier. This process known as

thermionic field emission.

Consider p-type MOS solar cell, at zero bias (thermal equilibrium). In this condition, solar cell has depletion or inversion layer depending on the insulating layer properties and substrate doping density. Under the small applied positive gate voltage depletion layer width becomes wider than in thermal equilibrium and capacitance decreases below its thermal equilibrium saturation value. This nonequilibrium condition is called deep depletion because silicon surface is depleted to a greater depth than it would be thermal equilibrium. Because the minority carrier density at the surface is larger than in thermal equlibrium.

As the gate bias is made increasingly positive, depletion layer width continuous to widen and capacitance to decrease until onset of oxide breakdown carriers. Additional generation of minority carriers occurs when electron-hole pairs are created by tunnelling between silicon valence and conduction bands. At a gate bias such that tunnelling occurs, an inversion layer forms. Beyond this gate bias, depletion layer width no longer increases.

Deep depletion can occur in thin oxide MOS cell with oxides less than 10 A^0 thick. In such devices an inversion layer cannot form because minority carriers tunnel through the oxide to gate electrode, easily.

3.8 ELECTRICAL CHARACTERISTICS OF MOS SOLAR CELL

3.8.1 Current-Voltage Characteristics

The total potential difference V_b between the metal and the semiconductor may be divided into two parts: V_i and V_d, where V_i is the voltage drops across the insulating (oxide) layer and V_d is the voltage drops in the space charge layer of semiconductor. This can be written as

$$V_b = V_i + V_d \qquad (3.35)$$

When external voltage V_a is applied across the junction (or when it is developed by the photovoltaic effect) we have

$$V_a = \Delta V_i + \Delta V_d \qquad (3.36)$$

Communication between the surface states, metal, valence and conduction bands of semiconductor may follow six ways:

1-Direct transition of electrons from valence band of semiconductor to the conduction band. The reverse process is radiative recombination that is negligibly small.

2-Holes tunnel through from the valence band of semiconductor to the filled state of metal. In thermal equilibrium, equal current flows from the metal to the semiconductor. When light is incident on the semiconductor under the influence of space charge layer photogenerated holes reach the semiconductor oxide interface.

3-An electron current flows from the conduction band of the semiconductor to the metal.

4-Current due to tunnelling of electrons flows from the surface states to vacant states in metal. The current is balanced by thermal equilibrium by an equal tunnelling current from metal to surface states.

5-Electrons are captured from conduction band by the surface states. At the same time to maintain an equilibrium, there is reemission of electrons from the filled surface states states to the conduction band. At thermal equilibrium both processes balance each other. When external voltage is applied, an electron capture rate exists.

6-In a similar process holes in valence band are captured by surface states and reemmitted.

The current through the cell is equal to the algebraic sum of hole and electron current and current by tunnelling at the surface states.

A typical energy-band diagram for MOS solar cell (p-type substrate) is given in Figure 3.11 in which p-type semiconductor is biased positively with respect to top metal contact by a voltage V_a.

The band gaps of the insulator and semiconductor are represented by E_{gi} and E_{gs}, respectively. The energy difference between oxide and semiconductor conduction band edges is represented by ϕ_{si}. The metal insulator barrier height is represented by ϕ_{mi}.

Under the bias conditions shown in Figure 3.11, there are net current flows J_{ct} and J_{vt}, from conduction and valence band edges of semiconductor to the metal contact due to electron tunnelling transitions between the metal and these bands. Similarly a net current J_{st} flows to metal from the surface states considered localized at the semiconductor oxide interface. The effective current flows due to interchange of the charge between the conduction and valence bands of semiconductor and these states by recombination-generation processes are represented by J_{ci} and J_{vi}, respectively.

When appreciable tunnel current starts to flow, if insulator thickness is below about 60 A^0, the current is initially of such small magnitude that semiconductor is in thermal equilibrium. If insulator thickness is further decreased, the tunnel current increases to point where they are sufficiently large enough to disturb the semiconductor from thermal equilibrium. This occurs around the 28 A^0 for Al-SiO_2 (p-type) Si. Thus, in general below some critical value of the oxide thickness nonequilbrium tunnel MOS diode formed.

If oxide thickness is between (15-20 A^0) dark I-V characteristic can be taken as

$$I_D = I_o[\exp(qV_a/nkT) - 1] \qquad (3.37)$$

where I_0 dark saturation current,

$$I_o = AR^{**}T^2 \exp(q\phi_{bp}/kT) \qquad (3.38)$$

V_a is applied voltage, n is ideality factor, A is active area, ϕ_{bp} is barrier height and R^{**} is Richardson constant($R^{**}=32 Amp/cm^2K^2$) [25].

The case of tunnel conduction has been treated theoretically by Card and Rhoderick [37] and more recently Green [8]. This theory assumes that, in thin insulator is in tunnel conduction mode with negligible voltage drop across it and that the thermionic emission diffusion theory of Crowelland Sze describes current like in Eqn. (3.37) and (3.38).

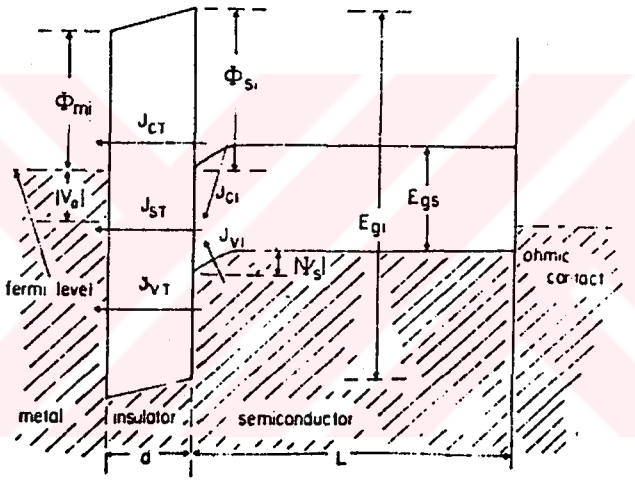

Figure 3.11 Energy band diagram of metal-oxide-p-type silicon solar cell.

3.8.2 Short Circuit Photocurrent

When light shines on a solar cell the incoming photons generate electron-hole pairs that are collected and become a photocurrent, I_p. The process of collecting the holes and electrons gives rise the photovoltage that is biased as to generate a diode current, I_D, that is in opposing direction to the photocurrent and whose properties given in Eqn. (3.39). The absolute value of photocurrent density generated

by incoming light may be written as

$$J_p = qX_1 G \tag{3.39}$$

where G is the generation rate that can be written as

$$G = \int_0^{\lambda} \alpha(\lambda)\, T(\lambda)\, M(\lambda) \exp[-\alpha(\lambda)\, x]\, d\lambda \tag{3.40}$$

where $T(\lambda)$ is transmittance into the surface layer, $M(\lambda)$ is the incident photon flux and λ_g is the wavelength of photons with the incident energy equal to the band gap energy E_g. This photon or photocurrent, depends strongly on the factor, X_1, that is the collection distance for photogenerated charge carriers.

In MOS solar cells the semiconductor side of the cell is the controlling factor and the metal or oxide portions affect the interface recombination of holes and electrons in the solar cell.

I-V characteristics of MOS solar cell under illumination,is given as

$$I = I_o[[\exp(qV_a/nkT) - 1] - I_p] \tag{3.41}$$

where I_p is the photocurrent. The short circuit photocurrent of an ideal solar cell is dependent primarily on the intensity of illumination and material parameters. It is given by [28]

$$I_{sc} = -\frac{I_p}{1 + \frac{qR_s I_o}{n}} \tag{3.42}$$

3.8.3 Open Circuit photovoltage

If the solar cell is illuminated but the load is disconnected, no net current can flow and to balance the photocurrent component there must be an increase in dark

current which flows in the direction opposite to that of photocurrent.

Under open circuit conditions I=0, $V_a=V_{oc}$

$$0=I_o[\exp(qV_{oc}/nkT)]-I_{sc} \qquad (3.43)$$

By neglecting the effects of R_s and R_{sh} and assuming largest value of the photocurrent $I_p=I_{sc}$. It follows that

$$V_{oc}=\frac{nkT}{q}\ln[\frac{I_p}{I_o}+1] \qquad (3.44)$$

since I_0 is always very small as compared to I_p, V_{oc} can be written as

$$V_{oc}=\frac{nkT}{q}\ln\frac{I_p}{I_o} \qquad (3.45)$$

It is clear from Eqn. (3.44) to obtain high value of open circuit photovoltage for a given photocurrent, the saturation values of dark current components must be rendered small.

The higher V_{oc} values at higher base layer doping densities are a direct consequence of layer dark current. However, this capability of developing high V_{oc} must be weighted against the reduced carrier lifetimes in the base which will reduce I_{sc}. Thus, overall cell conversion efficiency will not increase indefinitely with an increase in base layer doping density. Furthermore voltage reducing effects also serve to reduce Voc at high base layer doping levels. The high short circuit current are thus seen to be conflicting. However, high open circuit photovoltage are possible in solar cell with high resistivity base layers.

3.8.4 Fill Factor and Efficiency

The fill factor ,FF, of a solar cell is a measure of the "sharpness of knee" in output current-voltage curve of

Figure 3.12. I-V characteristic of a solar cell under illumination indicating the effects of series and shunt resistances is shown in Figure 3.12. It is clear that FF will be adversely affected by R_s and R_{sh} but dependences are other properties of the cell may not be obvious.

Consider the I-V characteristic of MOS solar cell under illumination as shown in Figure 3.7. It is

$$I_L = I_o[\exp(qV_L/nkT) - 1] - I_p \qquad (3.46)$$

and therfore the output power $P_{out} = I_L.V_L$. Its maximum value

$$P_{max} = I_{mp}V_{mp} \qquad (3.47)$$

when dP_{out}/dV_L and equating $V_L = V_{mp}$, we get

$$(1+\frac{qV_{mp}}{nkT})\exp(\frac{qV_{mp}}{nkT}) = \frac{I_p}{I_o}+1 \qquad (3.48)$$

Eqn. (3.48) can be solved numerically to find V_{mp} and

$$I_{mp} = [I_o\exp(\frac{qV_{mp}}{nkT}-1) - I_p] \qquad (3.49)$$

or

$$I_{mp} = I_o(\frac{qV_{mp}}{nkT})\exp(\frac{qV_{mp}}{nkT}) \qquad (3.50)$$

Maximum power can obtained as

$$P_{max} = [I_o(\frac{qV_{mp}}{nkT})\exp(\frac{qV_{mp}}{nkT})]\,V_{mp} \qquad (3.51)$$

The fill factor becomes

$$FF = \frac{I_{mp}V_{mp}}{I_{sc}V_{oc}} \qquad (3.52)$$

$$FF=\frac{I_o\left(\frac{qV_{mp}}{nkT}\right)\exp\left(\frac{qV_{mp}}{nKT}\right)V_{mp}}{I_{sc}V_{oc}} \qquad (3.53)$$

The efficiency of a solar cell is the ratio of electric power which can be abstracted at the maximum power point and input power density.

$$\eta=\frac{P_{max}}{P_iA} \qquad (3.54)$$

P_{max} can be written as

$$P_{max}=I_{sc}V_{oc}(FF) \qquad (3.55)$$

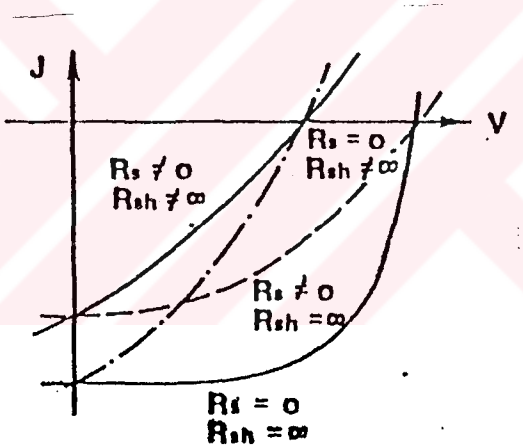

Figure 3.12 J-V characteristics of solar cell indicating the effects of series and shunt resistances.

3.8.5 Capacitance Voltage Characteristics

In process control applications of MOS solar cell, C-V characteristics are normally measured in response to an ac small signal with a frequency of 1 MHZ and an amplitude of a few millivolts while a slowly varying large-signal "DC" bias is applied between the gate and substrate.

Since the MOS cell must be electrically neutral overall, any charge Q_s stored on the substrate must be balanced by an equal and opposite charge Q_g stored on the gate. The small signal capacitance per unit area is given by

$$C=\frac{dQ_g}{dV_{gb}}=-\frac{dQ_s}{dV_{gb}} \tag{3.56}$$

Therefore,

$$\frac{1}{C}=-\frac{dV_{gb}}{dQ_s}=-\frac{d\psi_s}{dQ_s}-\frac{d\psi_{ox}}{dQ_s}=\frac{1}{C_s}+\frac{1}{C_{ox}} \tag{3.57}$$

where the semiconductor component C_s of the total capacitance is defined by

$$C_s=-\frac{dQ_s}{d\psi_s} \tag{3.58}$$

C_s is a measure of how charge stored in the semiconductor and changes with changes in the band bending Ψ_s across the semiconductor. Eqn. (3.57) suggests that MOS cell can be thought of as consisting of the oxide capacitance C_{ox} in series with semiconductor capacitance C_s.

It is possible to solve exactly for Q_s as a function of ψ_s on MOS cell and thereby to obtain exact expressions for C_s and the total capacitance C. However, the exact solution is rather involved, so much simpler but still relatively accurate approach to determining C_s will be taken in here.

When the cell is in accumulation, the hole concentration at the silicon surface depends exponentially on Ψ_s as specified in Eqn.(3.22). This implies that a small change in Ψ_s will produce a very large change in Q_s, so that C_s approaches infinity. In this case $C=C_{ox}$. Physically, this result can be explained by noting that the high density of charge carriers in accumulation layer makes the semiconductor electrode behave almost like a metal plate. In accumulation, then, the MOS cell is electrically equivalent to a capacitor with two

inverted, Q_s results almost entirely from dopant ion charge in the depletion region. In this case. using Eqn.(3.16) to determine the depletion region width W, Q_s can be written as

$$Q_S=-\sqrt{2\varepsilon_s qN_A\psi_s} \tag{3.59}$$

So, the depletion region width is related to capacitance as

$$C_s=\sqrt{\frac{\varepsilon_s qN_A}{2\psi_s}}=\frac{\varepsilon_s}{W} \tag{3.60}$$

It is worth noting that this is just the junction capacitance one would expect for a pn diode with depletion width W. With C_s specified by Eqn.(3.60), the total capacitance is given by

$$\frac{1}{C}=\frac{1}{C_{ox}}+\frac{W}{\varepsilon_s} \tag{3.61}$$

As V_{gb} is increased the depletion region widens and capacitance falls. Eventually, the strong inversion condition $V_{gb}=V_T$ is reached, at this point the depletion region stops expanding. The minimum capacitance is given by

$$\frac{1}{C_{min}}=\frac{1}{C_{ox}}+\frac{W_{max}}{\varepsilon_s} \tag{3.62}$$

where W_{max} is given by Eqn.(3.19).

It might be expected that once the semiconductor surface becomes strongly inverted C_s would again become extremely large. After all, from Eqn.(3.12) the surface electron concentration has the exponential dependence on Ψ_s as the surface hole concentration, so a small change in Ψ_s should produce a very large change in the electron concentration, and hence in Q_s. This is in fact the case provided that Ψ_s and V_{gb} change slowly. However, electrons in the surface inversion layer cannot respond to rapid changes in V_{gb} , and in particular cannot respond to 1 MHZ frequency usually used to measure C. This comes about because in MOS cell electrons can

only be supplied to the inversion layer from thermal generation process in depletion region. Unless the minority carrier lifetime is abnormally short, these generation processes are rather slow. For example, in a MOS cell fabricated using present processing technology on a high quality silicon substrate, it normally takes many seconds for the surface inversion layer to form after the capacitor is biased into what should be a strong inversion condition.

Putting together the results above, we expect the complete C-V_{gb} characteristic of MOS cell to appear as shown in Figure 3.13. C is largest in accumulation, drops as V_{gb} increases and the width of depletion region grows, and saturates at C_{min} in strong inversion.

If V_{gb} is increased very rapidly starting from a condition of accumulation, there may not be time for an inversion layer to form at the silicon surface. In this case the depletion region width will grow indefinitely as V_{gb} is increased, and the capacitance will fall in accordance with Eqn.(3.61). This possibility is illustrated by the dashed line in Figure 3.13. When W is made greater than W_{max} in this kind of transient situation, the capacitor is said to be deep depletion.

As noted above, a great deal of information can be obtained from a single MOS cell C-V_{gb} curve. For example, the thickness of the gate oxide can be computed from Eqn.(3.10)by noting that the maximum capacitance measured in accumulation is just C_{ox}. If C_{min} is then obtained from the strong inversion region of characteristic, the maximum steady-state depletion region width W_{max} can be computed from Eqn.(3.19). Using Eqn.(3.19)and Eqn.(3.4), the substrate doping N_A can be found once W_{max} is known. It is not possible to solve Eqn.(3.19) and Eqn.(3.4) explicitly for N_A in terms of W_{max} . The threshold voltage of cell can be obtained by simply determining the value of V_{gb} at which the capacitance first reaches its minimum value, as shown in Figure 3.13.

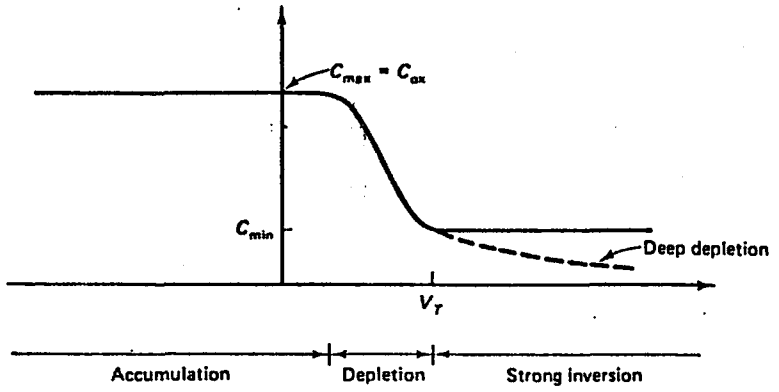

Figure 3.13 MOS cell C-V characteristics.

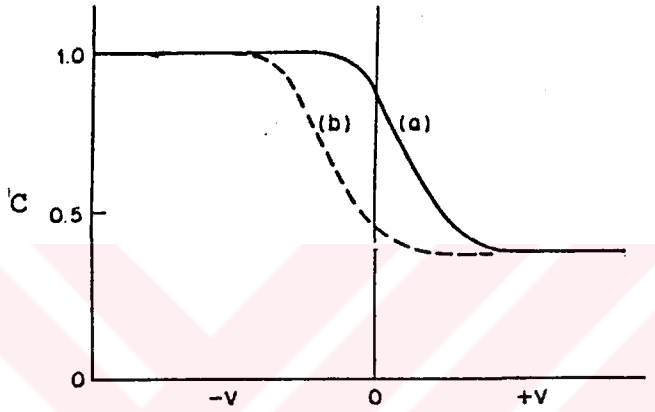

Figure 3.14 Effect of interface traps on MOS cell characteristics. (a) ideal MOS C-V curve (b) C-V curve with interface and oxide charges.

If the silicon-silicon dioxide contains large number of interface traps,the MOS cell C-V characteristic will be altered as shown in Figure 3.14. In general, interface traps "smear out" the characteristic, increasing the voltage spread between the accumulation and inversion regimes. The distortion of the interface traps increases the change in V_g required to produce a given change in Ψ_s. The interface traps themselves do not normally contribute to the capacitance at frequencies as high as 1 MHz.

CHAPTER IV

EXPERIMENTAL PROCEDURE AND RESULTS

4.1 INTRODUCTION

Device fabrication presumes the availability of an appropriately doped semiconductor. Before the device processing begins, the starting material has to be characterized in terms of its basic electrical parameters. The parameters of main interest are the conductivity type (n or p) and the resistivity. This chapter provides the laboratory techniques for measuring these parameters. The methods used in fabricating MOS solar cells (using p-type silicon crystal) and the results of experiments revealing their physical characteristics are given.

The electrical characteristics of the SiO_2-Si system approach those of ideal MOS cell. However, in MOS structure, the work function difference is generally not zero. There are various charges inside oxide and SiO_2-Si interface states in thermal equilibrium which affect the ideal MOS characteristics. In this chapter these phenomenon are also taken into consideration.

4.2 GENERAL INFORMATION ON VACUUM DEPOSITION SYSTEM

A metal layer on a wafer is not often obtained using a vacuum deposition system. There are many types of vacuum deposition systems, but they have the same characteristics in common.

In our experimental work, metal coating was made by Edwards

(model Auto 306) Vacuum Coater with Diffusion Pumping System which is shown in Figure 4.1. The Auto 306 is microprocessor controlled vacuum coater that can be configured to perform a variety of coating tasks.It has the following main elements:
1- Vacuum pumping system (vapour diffusion pump and rotary pump).
2- A microprocessor control system and control panel
3- Chamber that may be evacuated to provide a sufficient vacuum for the deposition to take place.
4- Water cooled crystal holder to measure the thickness of the coating layer using (model FTM5) Film Thickness Monitor.
5- A baseplate.
6- Cabinet.

The baseplate of the coater provides an interface between the process chamber and the system. It is manufactured from stainless steel and is machined with a number of holes to enable the mounting of optional vacuum electrodes.

The rotary pump uses a rotor that is sealed against the leakage by a vacuum system,vapour that enters the pump through the inlet part, is compressed, and is ejected to the atmosphere through the exhaust or discharge part.

In the diffusion pump, vapour from a boiler passes through a series of nozzles in a downward direction carrying residual atoms in the chambers with it. Atmospheric pressure can be reduced up to 1.10^{-7} by diffusion pump.

The instrumementation of a vacuum deposition system provide a method of
1- determining the vacuum level in the chamber
2- measuring the status of all valves, etc., in the system
3- determining the thickness of any deposited layer.

For vacuum deposition, filament evaporation technique is used. In this technique, current flows through a filament.

Filament evaporation is the simplest and least expensive deposition method. Evaporation takes place from filament or boat heated by thermal resistance heating. Evaporation is accomplished by gradually increasing the current flowing through the filament (care must be taken to choose a filament compatible with material to be evaporated). Filament evaporation systems are easy to set up and many materials can be evaporated using them. However, the contamination level of the deposited materials is often sufficiently high to interfere with the functioning of the device. Contamination may cone from the filament or from poor handling techniques. For this reason filament evaporation of aluminum is not common [32], but in our experimental work, this technique was used. Because there is no device to apply another deposition technique.

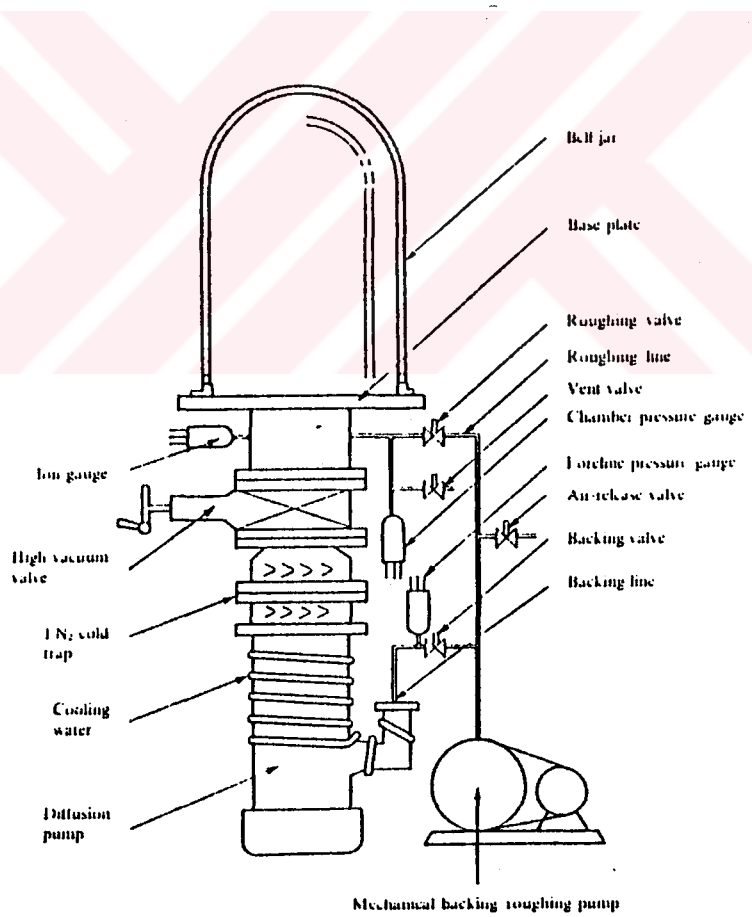

Figure 4.1 Schematic figure of vacuum coating system.

The metal which is used for deposition must meet or exceed all of the requirements:

1- The metal must make a low-resistance electrical contact with the silicon.

2- The metal must have a limited reactivity with silicon in order to produce stable contact.

3- The metal must have a high electrical conductivity, so that high current is easily carried without any voltage drops.

4- The metal must adhere well to the underlying silicon, silicon dioxide.

5- The metal coating must not exhibit electromigration (Electromigration is the migration of atoms in the deposition of metal caused by flow of current).

6- The metal coating must not corrode under normal operating conditions.

No metal perfectly meets all of these requirements. However, aluminum does meet all of them satisfactorily.

4.3 FABRICATION OF SOLAR CELLS

At laboratory MOS solar cells fabricated were from silicon available as 400-560 micron thick, 76.2 diameter slices. the slices were cut from single crystal silicon <111> metallurgical plane. They are slightly p-type and according to manufacturer's specification, resistivity of wafer is 2-20 Ohm-cm.

The process involved in the fabricating of the MOS solar cells can be grouped under five headings:

1- Determination of the resistivity.

2- Preparation of crystals.

3- Oxidation of silicon.

4- Preparation of mask

5- Application of ohmic contact

4.3.1 Determination of the Resistivity

The most commonly used technique in the semiconductor industry for measuring resistivity is the four-point probe method. The arrangement is shown in Figure 4.2. Four collinear metal probes with sharpened tips are placed on a semiconductor. A constant current I is passed through the two outer probes, and the potential difference V developed across the inner two probes is measured using high input impedance volmeter. In this way the metal-semiconductor contact resistance does not affect the results. For collinear probes with separation s_0 placed on a semi-infinite medium, the resistivity ρ is given by

$$\rho = 2\pi s_o \frac{V}{I} \qquad (4.1)$$

This relation is also valid for a finite dimension, provided that the specimen thickness d is larger than $5s_0$, and all edges of the sample are away from the probes by a distance larger than $10s_0$.

If the sample is in the form of wafer and for probes centered in a circular wafer of finite diameter d, resistivity is obtained from the relation

$$\rho = \frac{V}{I} . d . CF \qquad (4.2)$$

where d is the wafer thickness and CF is the correction factor.

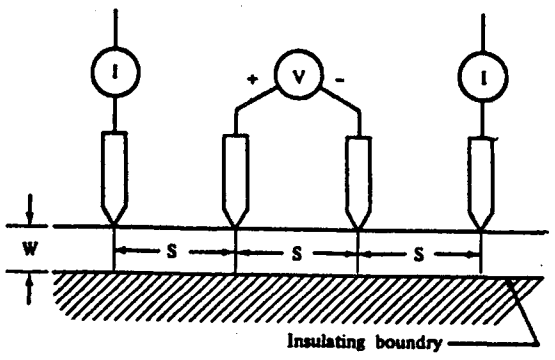

Figure 4.2 Arrangement of Four-Point-Probe method.

For the case when the wafer thickness d is small compared to s_0, as in our experimental work Eqn.(4.2) becomes

$$\rho=\frac{\pi}{ln2}\frac{V}{I}d=4.53\frac{V}{I}d \qquad (4.3)$$

4.3.2 Preparation of Crystals

The silicon slice was cut into wafers of 15x15 mm^2 of dimension. The square wafers were immersed in an hydrofluoric acid (HF 40 % pure) about five minutes. The hydrofluoric acid rinses and etches away any oxide that may have been initially present and any contamination from silicon surface. Then, they are rinsed with trichlorethylen, acetone and isopropyl alcohol using the Ultrasonic Cleaner (Bransonic 221), respectively. This cleaning procedure guarantees that any greases or waxes that might be insoluble in subsequent cleaning steps are removed. After then, they are dried to get wafers ready for the next step by the Vacuum System (Solitec).

4.3.3 Oxidation of Silicon

The ability to grow a chemically stable protective layer of silicon dioxide on a silicon wafer makes silicon the most widely used semiconductor substrate.
In our experimental work, optimum oxide thickness is 10-25 A^0 [17]. For such thin oxide growth on the polished surface of the wafer, the natural oxide thechnique that forms at room temperature was used. Figure 4.3 shows oxidation time versus film thickness for cleaved silicon crystal with a <111>-oriented surface as for an etched silicon surface, in air at room temperature [29]. To get optimum oxide thickness silicon slices are held in air for 24-30 hours at room temperature.

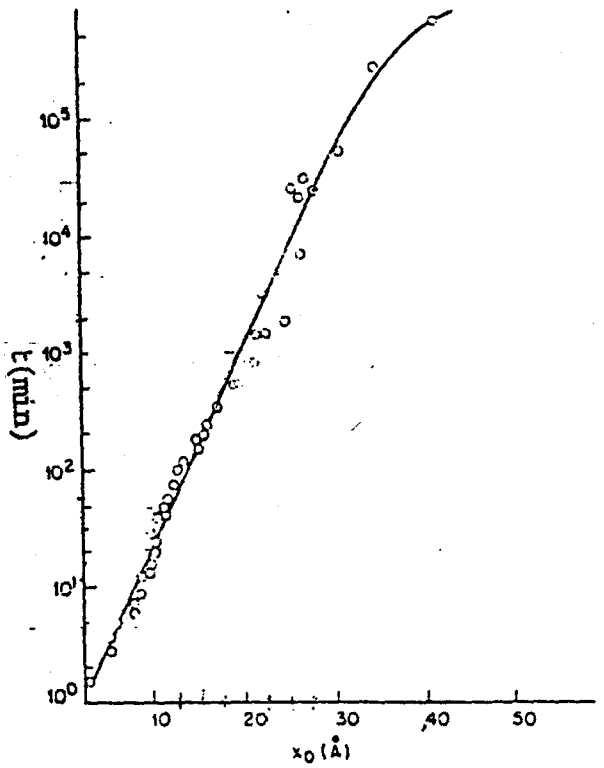

Figure 4.3 Oxidation time versus film thickness graph in air at room temperature.

Another way to grow thin oxide on a silicon is to expose the silicon surface to nitric acid at room temperature. This technique is also used in our experimental work.

4.3.4 Preparation of Mask

A mask must be used to determine the active area of the cell and to have electrical connection between the contacts and terminals.

Mask is prepared from copper board whose other face is fiber. Mask is cut into 15x15 mm^2 dimension as in silicon wafers. A circle which has a diameter of 10 mm was drilled from the centre of square wafer. The dimension of the circle is also the dimension of the active area. After then, masks are cut like an inclined plane from the end of the circle to get electrical connection between contacts and terminals as shown in Figure 4.4.

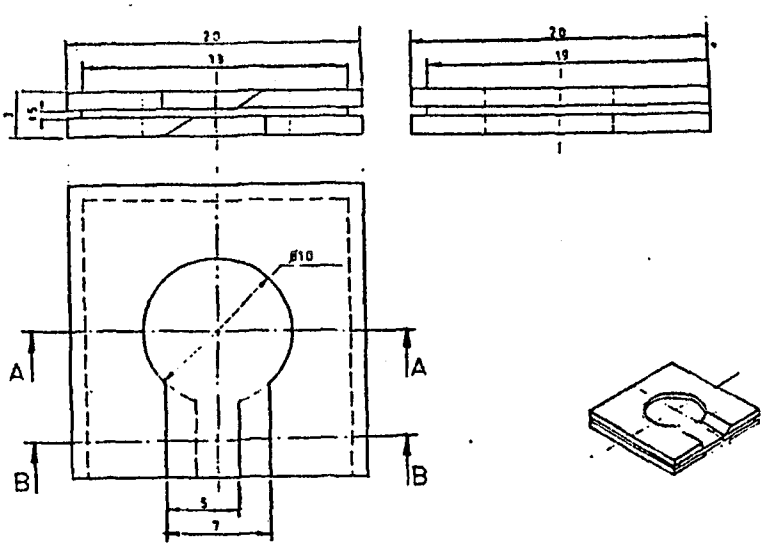

Figure 4.4 Perspective and three dimensinal view of MOS solar cell.

Silicon slices which are cleaned were placed between two masks and adhered by Bally. The nail polished was coated on the inclined plane and copper side of the mask to support electrical connection. After this process, they are waited in air at room temperature, for different time durations (10 -48 hours) to get thin oxide layer.

4.3.5 Application of Ohmic Contacts

Ohmic contacts to silicon are made by evaporating Aluminum to silicon using Edwards Auto 306 Vacuum Coater With Diffusion Pumping System. Since, Aluminum dopes silicon into p-type and it occupies an acceptor level in silicon only 0.057 eV above the valance band, it is suitable for making ohmic contacts to silicon.

Before oxidation, a thick Aluminum layer was evaporated on the back side of cleaned silicon slice providing Ohmic contact. Aluminum is evaporated by the resistance heating method in which a tungsten wire wound in the form of a basket (or spiral) is used as heating element. Evaporation temperature of aluminum is 900 ^{0}C at 10^{-5} Torr and the vapour pressure of Tungsten is very low (10^{-16} Torr). Purity of aluminum is not degraded by any tungsten vapour. After

oxidation in air or in a furnace at room temperature, silicon slice is annealed in furnace containing dry N_2 for 10 minutes at 500 ^{0}C. This is one of the most important steps in the fabrication. In this procedure, oxide trapped charges in insulating layer, trapped charges in surface states (recombination centres) are reduced by neutralizing charges in these states [27]. This process alloys the back side to reduces the SiO_2 and affects ohmic contact between the Si and the Al. Dry N_2 gas prevents the contamination which may otherwise diffuse on the specimen during heating. The top Al (70-100 A^0) is deposited on the active area through a solid mask using deposition rate of 1-10 A^0/sec at $4x10^{-5}$ Torr. Solar cell was completed by evaporating the thick Al (1000 A^0) layer on the inclined plane of copper board to get electrical contacts, easily. The coating details of MOS cell is given in Figure 4.5.

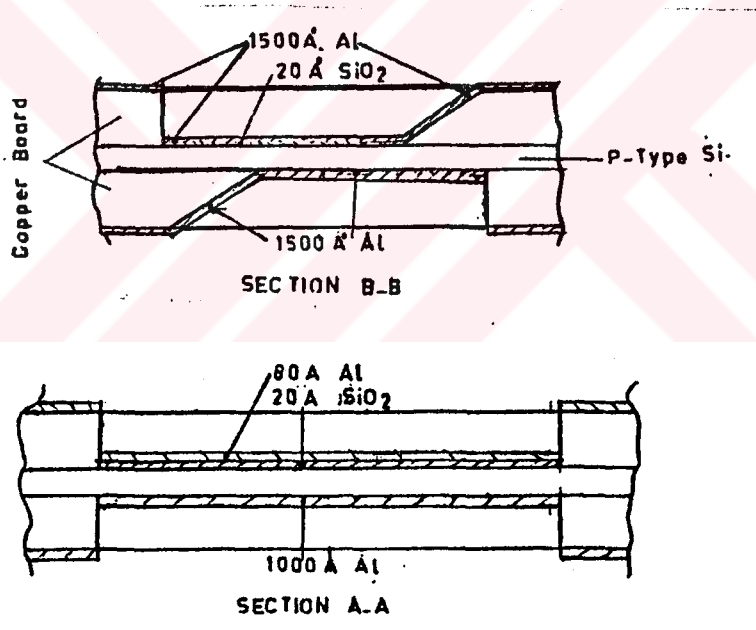

Figure 4.5 Details of metal coating.

Experimental results showed that, solar cells which are produced without annealing gives high short circuit current.

4.4 MEASUREMENT OF I-V CHARACTERISTICS

I-V characteristics of solar cell were measured by using (Keithley Model 230) Programmable Voltage Source and (Keithley Model 199) System DMM Scanners. These measurements were done in dark and under the illumination.Intensity of light source which is used in measurement of I-V characteristic under illumination is 3.4 mW/cm^2

Current-voltage characteristics of near ideal Schottky diode is given by Eqn.(3.37). Plot of lnI against voltage is used to determine both ideality factor and barrier height. The appropriate relations derived from Eqn.(3.37) for these calculations are given below

$$n=\left(\frac{d(lnI)}{dV}\right)^{-1}\frac{qA}{kT} \qquad (4.4)$$

from the slope and

$$\phi_{bp}=\frac{kT}{q}\ln\left(\frac{R^*AT^2}{I_0}\right) \qquad (4.5)$$

from the intercept. The value of I_0 determined from I-V characteristics from the intercept can only be accurate if ideality factor is equal to unity. From the practical point of view the condition $n\leq 1.5$ is often taken as the requirement for a reasonable accurate calculation of barrier height.

A negative voltage $V_{gb}<0$ will bend the bands as shown in Figure 3.6d. The majority holes are attracted towards the semiconductor, thus forming accumulation surface layer. On the other side of the oxide there is a negative electron charge on the other side . There is no depletion region in this voltage range, thus current increases.

A positive bias on the gate $V_{gb}>0$ repels the holes to the oxide-semiconductor interface, hence the surface layer is depleted of mobile charge. In this voltage range, current starts to decrease as seen from dark I-V characteristics of MOS solar cells 77, 78.

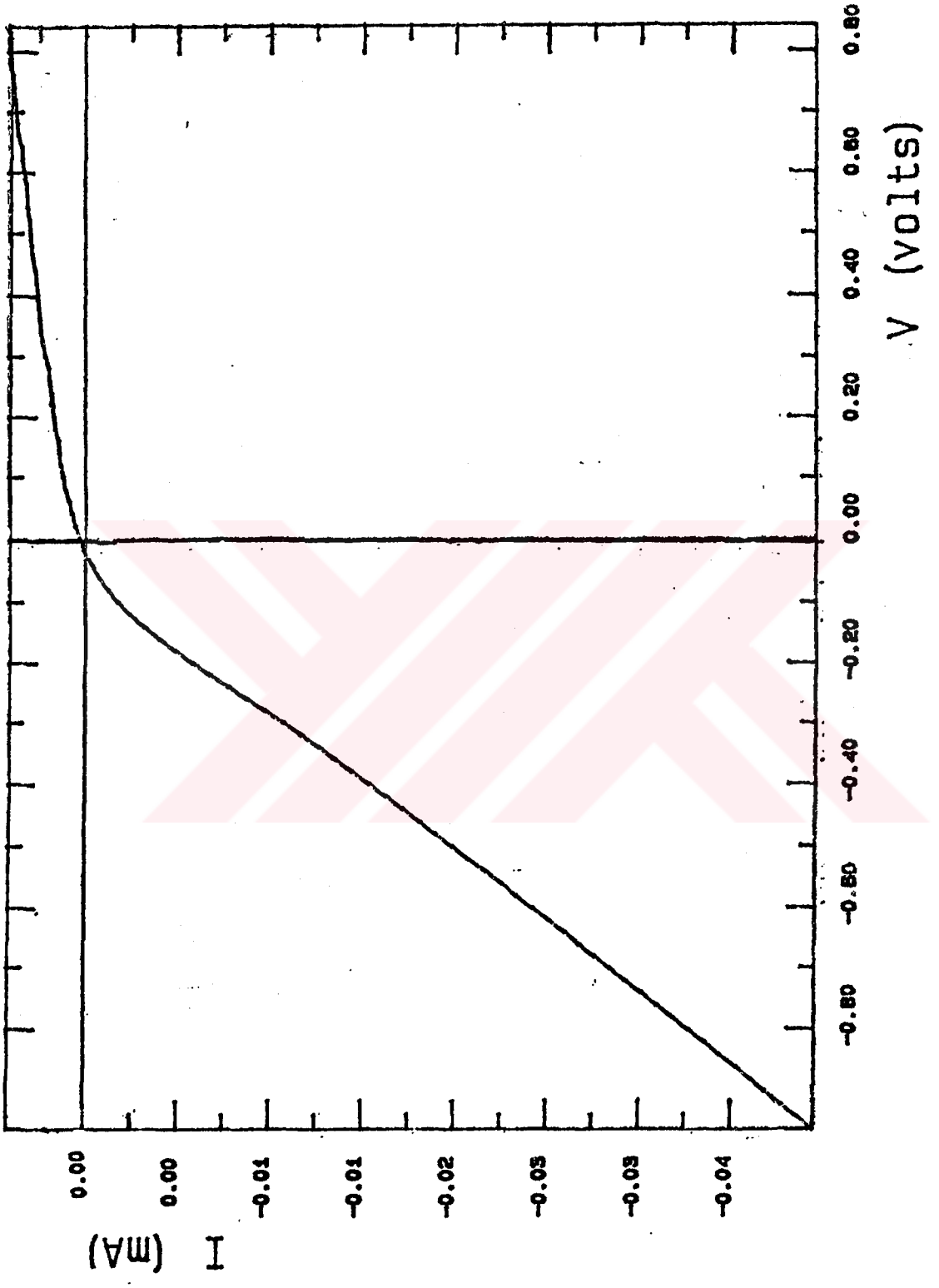

Figure 4.6 Dark I-V characteristic of MOS solar cell No: 78.

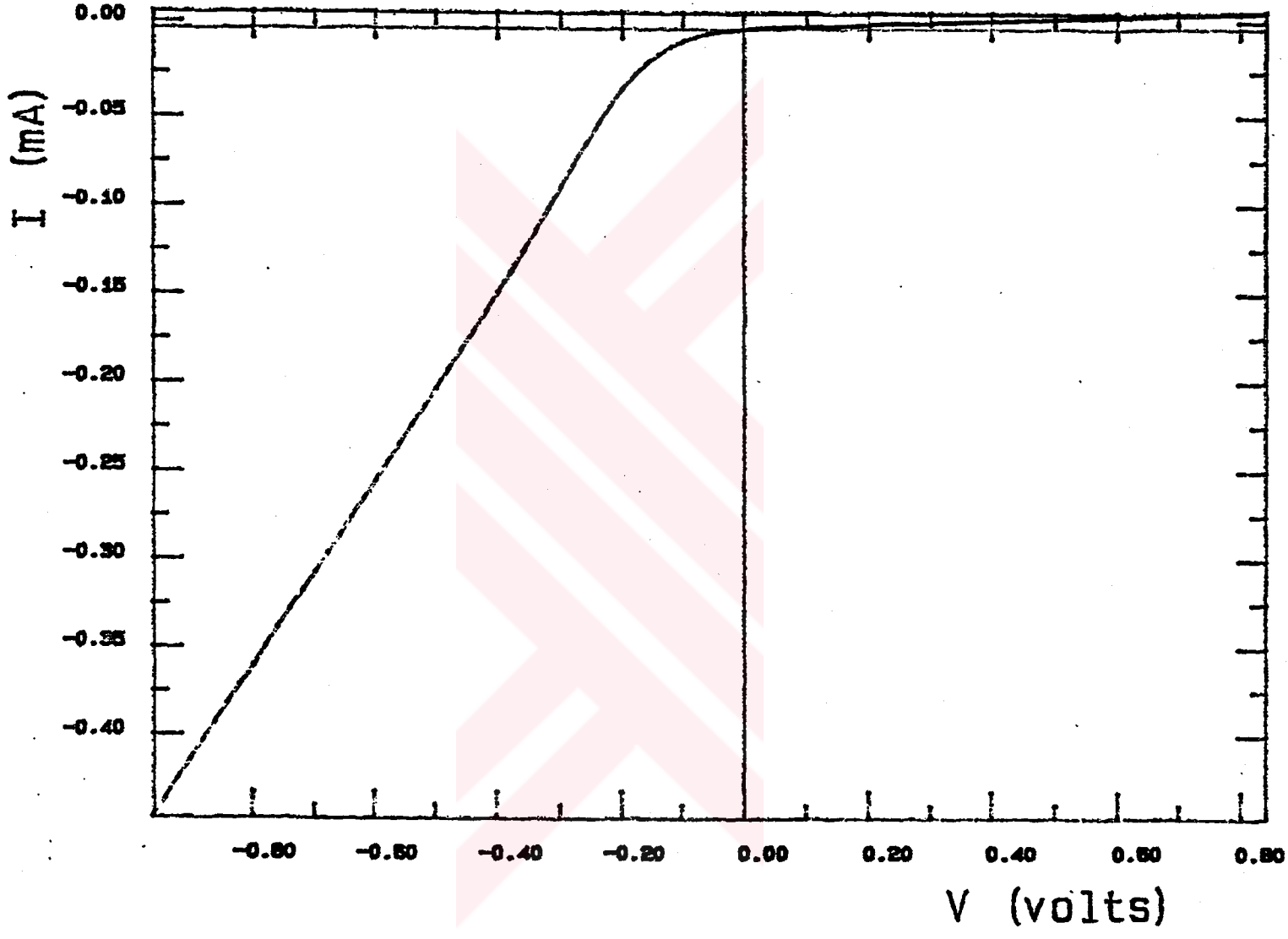

Figure 4.7 Dark I-V characteristic of MOS solar cell No: 77.

These characteristics are given in Figures 4.6, and 4.7, respectively. They are the same as the I-V characteristic of MOS solar cell given in Figure 4.8 [36]. I-V characteristics of solar cells 17, 67, 69, 70, 77 under illumination are given Figures 4.9, 4.10, 4.11, 4.12, and 4.13, respectively. Resistivity of cell 17 is 7.2 Ohm-cm and dopant concentration is 1.10^{15} cm^3. Other cells were fabricated from same samples whose resistivities are 3.8 Ohm-cm and dopant concentrations are 4.10^{15} $/cm^3$. Dopant concentration is found from curve which is given in Figure 4.14 [32].

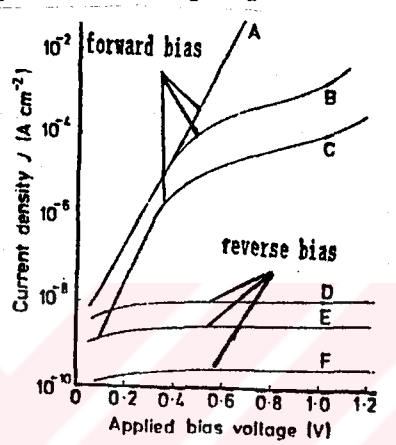

Figure 4.8 Theoretical I-V Characteristic in dark.

A higher positive gate voltage will bend down further the energy diagram thus moving the conduction band edge closer to the Fermi level. The surface will be inverted. Minority electrons are pilled up at the surface and form an inversion layer which is separated from the neutral bulk by a widened depletion region.

Cell No.	I_p(A)	I_{sc}(A)	V_{oc}(V)	Φ_{bp}(V)	n
17	$5.5x10^{-5}$	$5.3x10^{-4}$	0.180	0.257	2.11
67	$2.3x10^{-6}$	$6.7x10^{-4}$	0.210	0.540	4.8
70	$5.1x10^{-8}$	$5.2x10^{-8}$	0.490	0.693	13
77	$2.3x10^{-5}$	$1.1x10^{-3}$	0.350	0.503	8.4

Table 4.1 Calculated cell parameters.

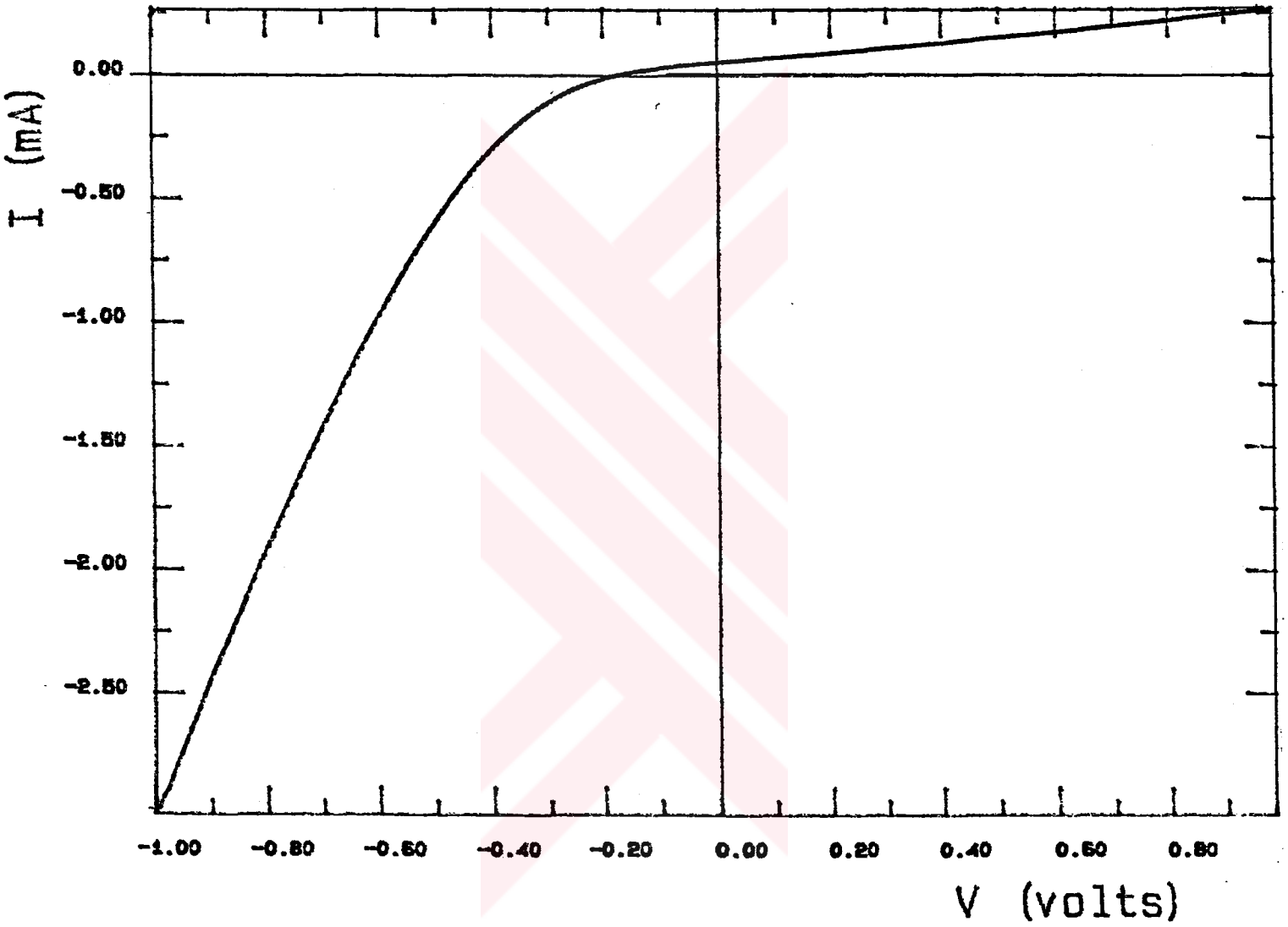

Figure 4.9 I-V characteristic of MOS solar cell No:17, under illumination.

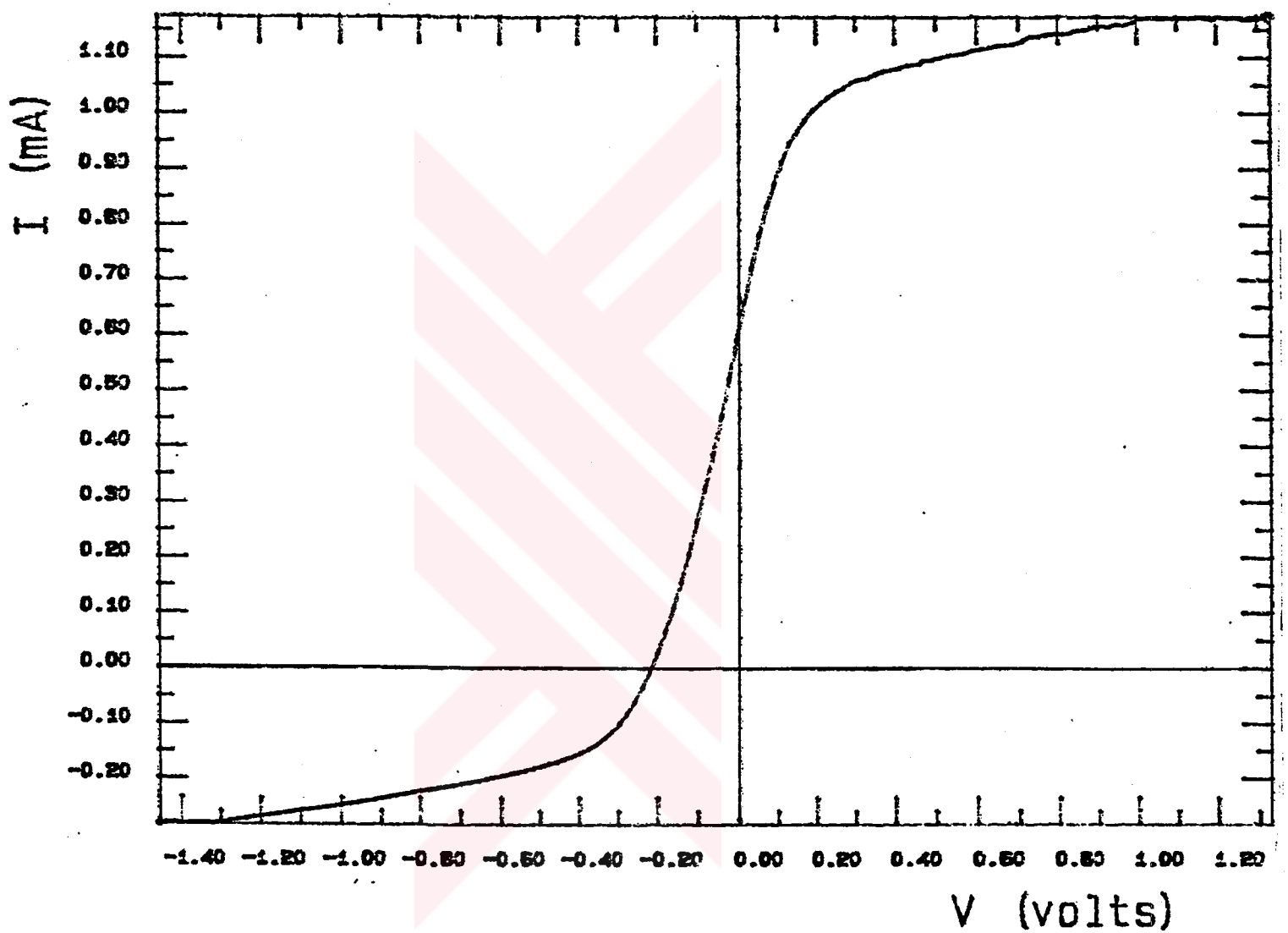

Figure 4.10 I-V characteristic of MOS solar cell No:67, under iilumination.

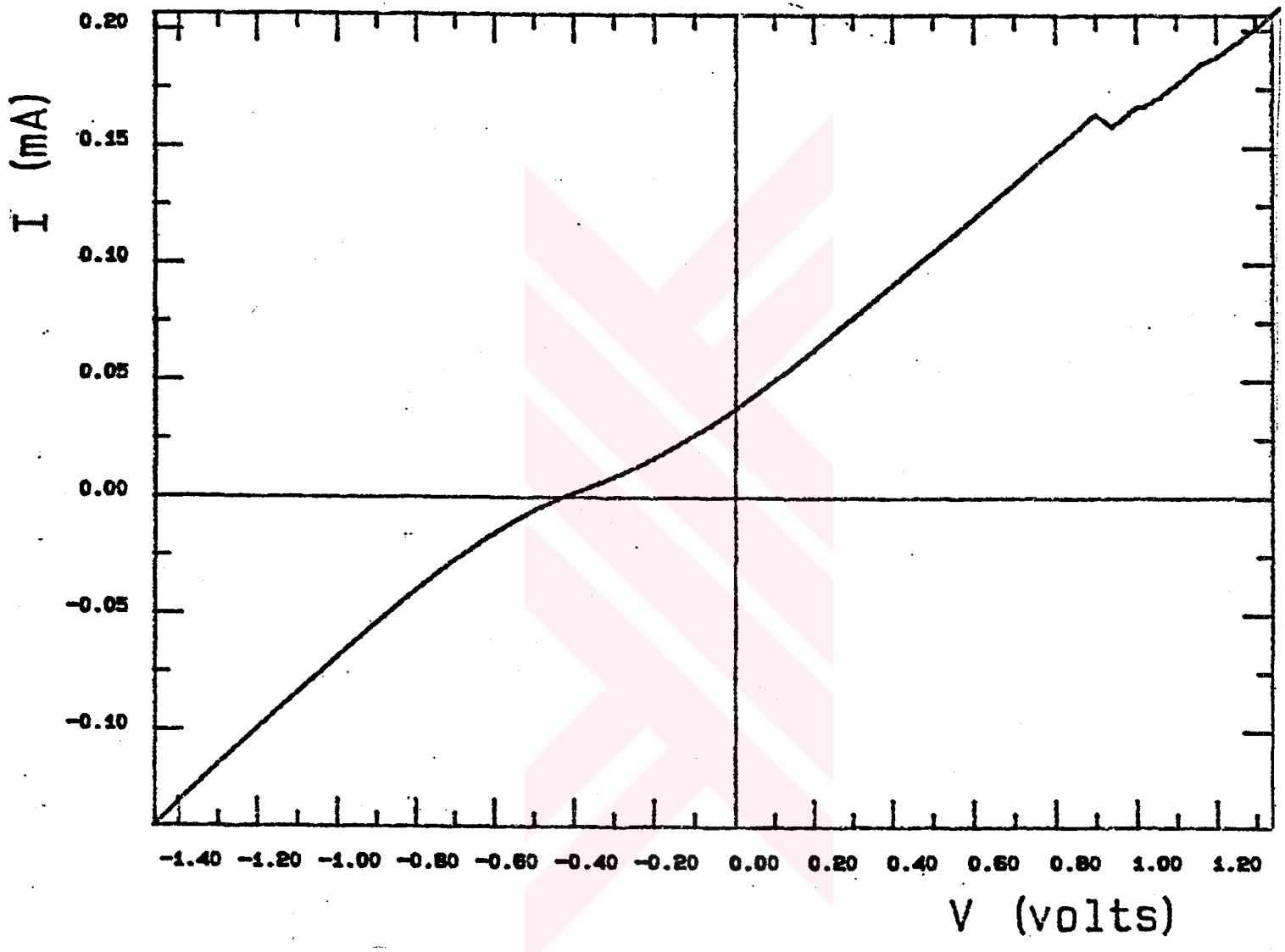

Figure 4.11 I-V characteristic of MOS solar cell No: 69, under illumination.

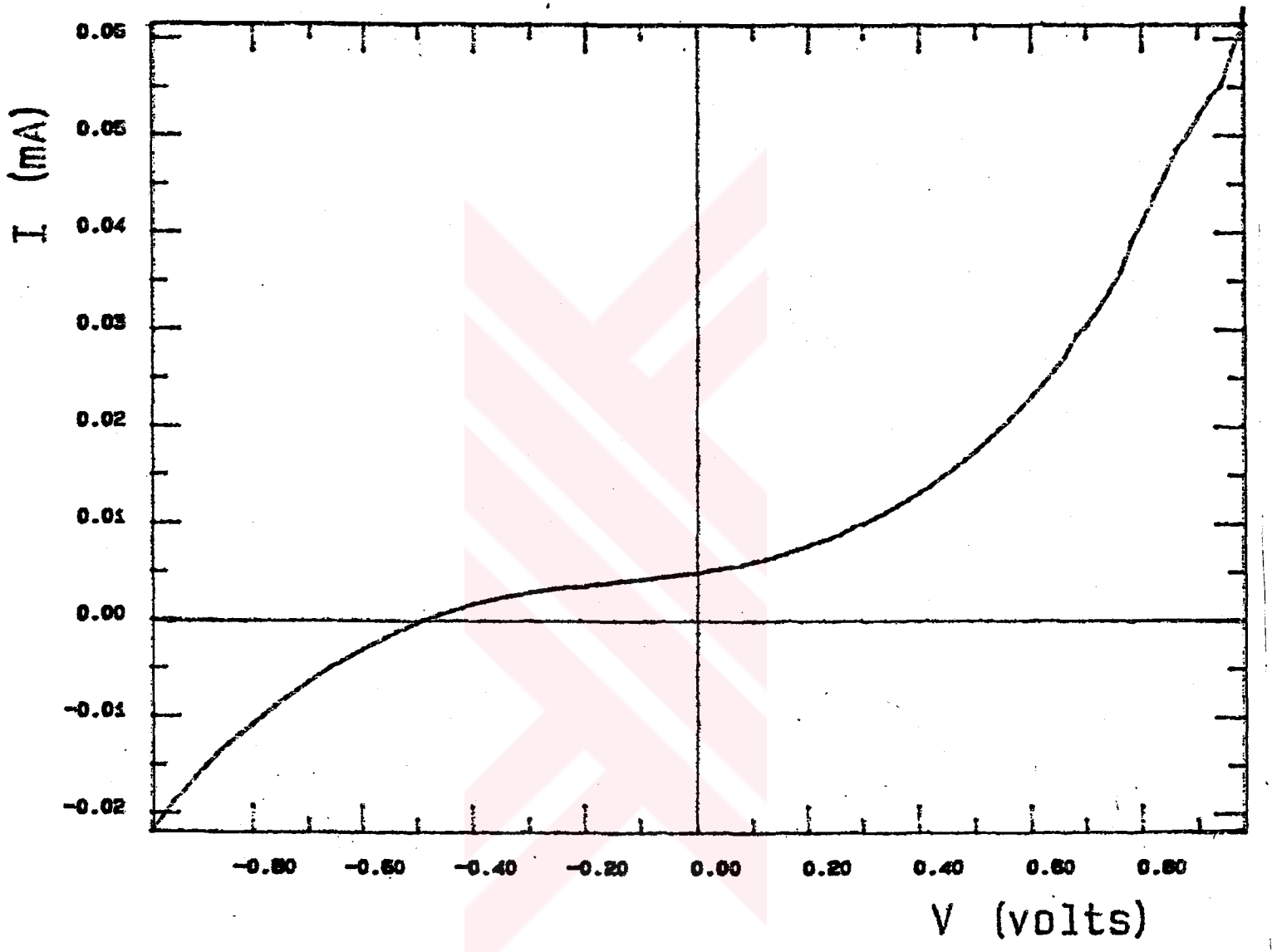

Figure 4.12 I-V characteristic of MOS solar cell No:70, under illumination.

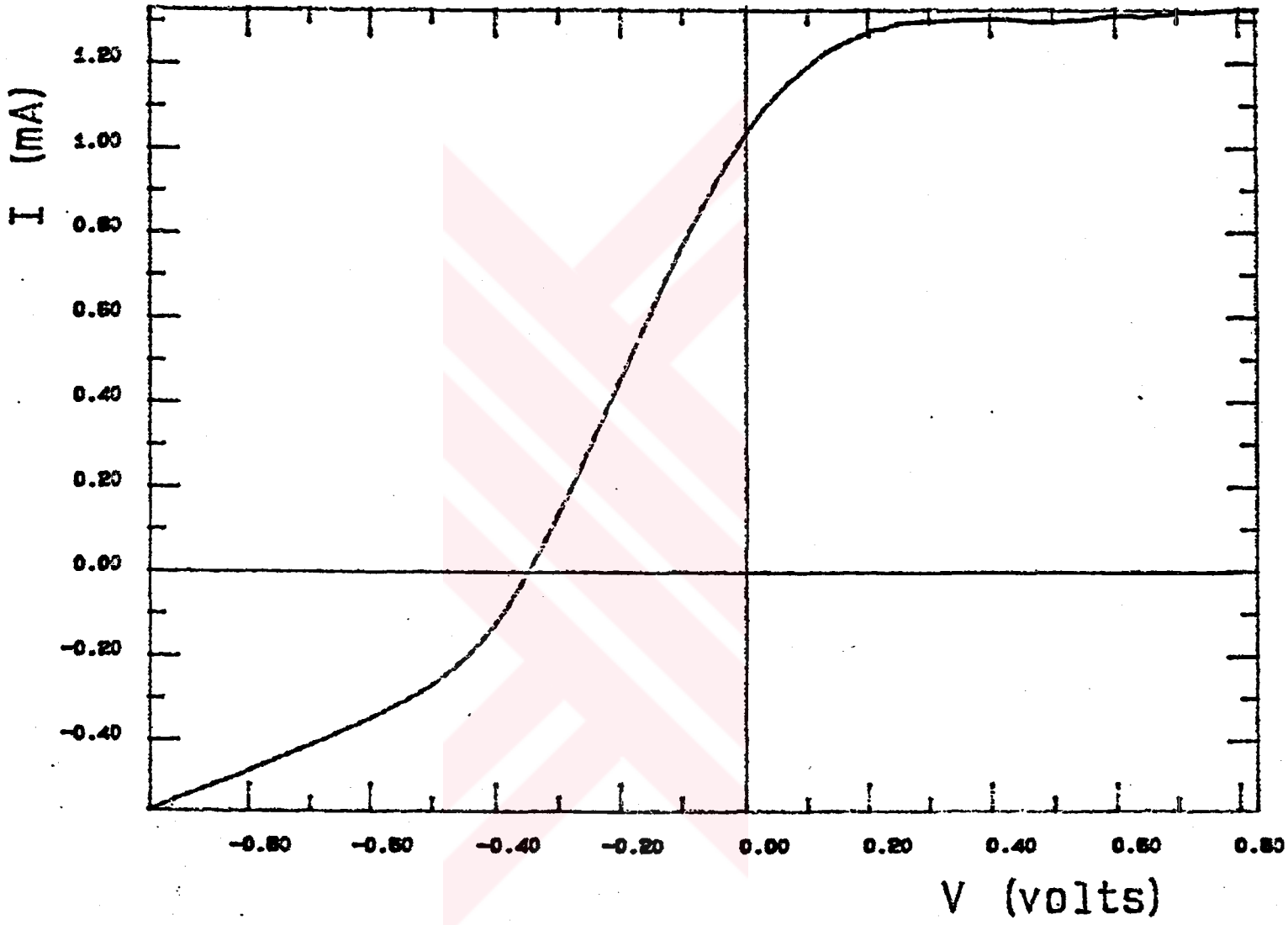

Figure 4.13 I-V characteristic of MOS solar cell No:77, under illumination.

From the I-V curves obtained under the illuminated light short circuit current (I_{sc}) and open circuit voltage (V_{oc}) can be determined. V_{oc} and I_{sc} are affected by charges in the oxide and the surface states in the $Si-SiO_2$ interface. These parameters are important to get high efficiency MOS solar cells. Other parameters (R_{sh}, R_s, I_p, FF) which are related to the measurement of efficiency were calculated using A Computer Program Modelling of MOS Cells [33]. The parameters that are calculated using computer program are given in Table 4.1. Efficiency of solar cell 77 is greater than the other cells which is equal to 7.3 %.

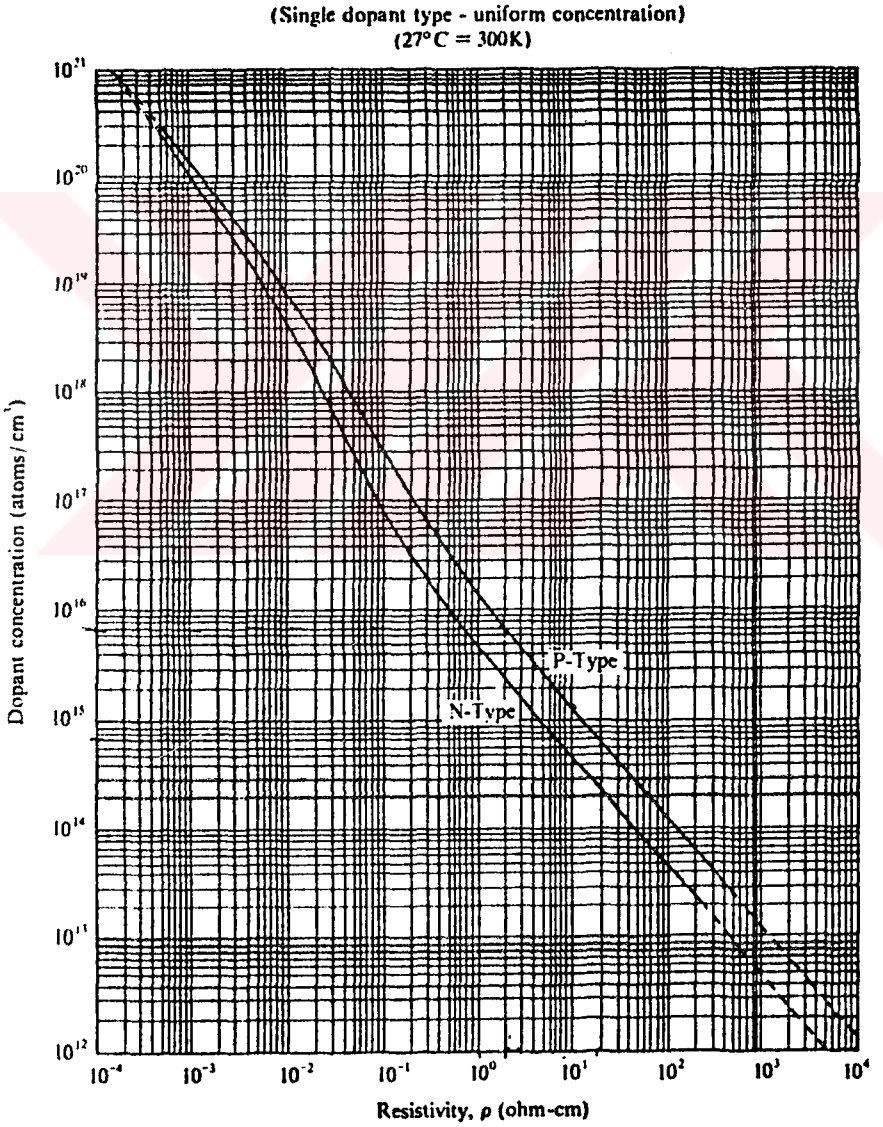

Figure 4.14 Resistivity versus doping concentration graph for silicon just n and p-type silicon

4.5 MEASUREMENT OF C-V CHARACTERISTICS

High frequency capacitance-voltage measurement was made by using (Keithley Model 590) C-V analyzer.

C-V characteristics of MOS solar cell are affected by positive charges in the oxide and interface charge is usually assumed to be electronic charge localized in surface states (interface states) and its surface density is denoted by Q_{ss}. These states in thermal equilibrium, would have acceptor-type and donor type charges (recombination centres). The surface of p-type semiconductor is inverted due to interface states and oxide charges, at zero bias.

Experimental C-V curve of MOS solar cell, No:68 is given in Figure 4.15. This curve is translated towards the left minimizing the capacitance as compared to the C-V curve of without interface states and oxide charges as shown in Figure 3.14. When capacitance decreases, dark current also decreases indicating the high barrier height.

Barrier height can be measured, easily using formula [11] which is given by

$$\phi_{bp}=V_{dif}+V_p-\Delta\phi \qquad (4.6)$$

where V_{dif} is the built-in potential, V_p is the energy difference between the intrinsic energy level and valence band edge (0.235 eV) and $\Delta\phi$ is the image force barrier lowering (0.0138 eV). Built-in potential is found from the extrapolation of $1/C^2$ versus V curve. The intercept V_I is equal to

$$V_I=V_{dif}-kT/q \qquad (4.7)$$

where kT/q is the correction for the effect of mobile carriers on the electric field in the depletion region.
The capacitance of solar cell arises from the charge due to

ionized acceptors in the depletion region and equal but opposite charge on metal surface. The differential capacitance C=dQ/dV of this system is usually measured by superimposing a small alternating voltage on to D.C bias.

An increase in reverse bias (positive bias) rises to a wider depletion width and reducing the capacitance. In depletion approximation, effect of majority carries are neglected. Because in the strong inversion condition, there are many minority carriers (ionized acceptor charge) as compared to majority carriers in surface of the silicon. The ionized acceptor charge per unit area Q_b, is given by Gauss's law in Eqn.(3.16). Substituting Q_b in the differential capacitance equation and solving gives

$$C=\frac{dQ_b}{dV}=\sqrt{\frac{q\epsilon_s N_A}{2(V_{dif}-V_{gb})}} \qquad (4.8)$$

Eqn (4.8) can be written in the form

$$\frac{1}{C^2}=\frac{2(V_{dif}-V_{gb})}{q\epsilon_s N_A} \qquad (4.9)$$

or

$$\frac{d(1/C^2)}{dV}=\frac{2}{q\epsilon_s N_A} \qquad (4.10)$$

The graph of C^{-2} as a function of V_{gb} should give a straight line with an intercept $-V_I$ which implies that the acceptor concentration is constant throughout the depletion region. Thus, measurement of the capacitance per unit area as a function of voltage can provide impurity distribution, directly. Experimental C^{-2}-V curve of MOS solar cell No:68 is given in Figure 4.16.

If the differential capacitance is measured with high frequency signal in strong inversion, the semiconductor

capacitance is equal to the depletion capacitance [28]. This is given in Eqn.(3.62).

In strong accumulation, the total capacitance is practically equal to the oxide capacitance. This occurs because the semiconductor capacitance C_s is very large and negligible in series with Cox.

Comparison of the theoretical and experimental C-V characteristics which are given in Figure 3.14 and Figure 4.15 are in good agreement.

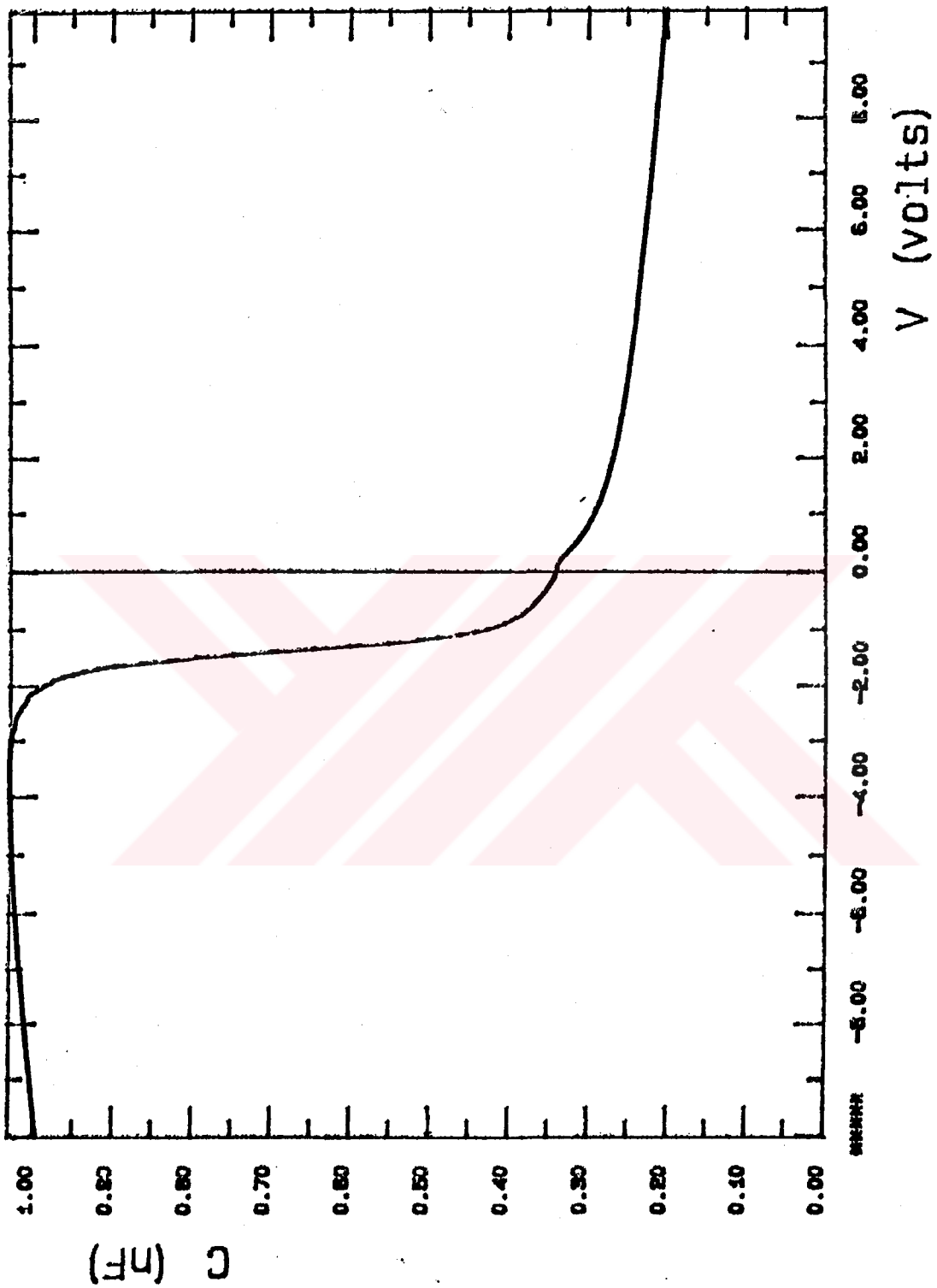

Figure 4.15 Experimental C-V characteristic of MOS solar cell No:68.

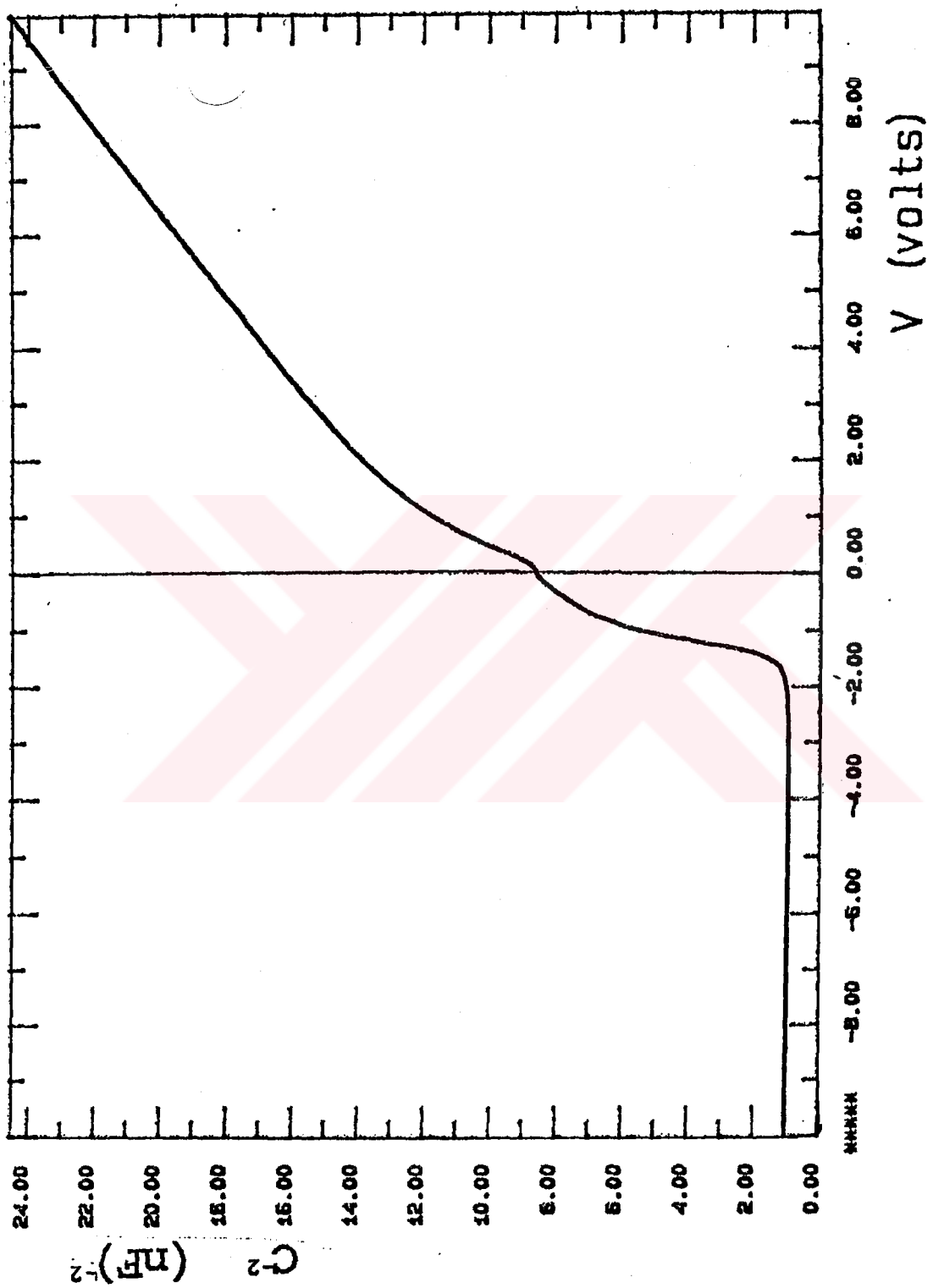

Figure 4.16 Experimental C^{-2}-V curve of MOS solar cell No:68.

CHAPTER V

CONCLUSIONS AND REMARKS

The work presented in this thesis was aimed to investigate the photovoltaic properties of minority-carrier MOS solar cells. The role of the interfacial layer in minority-carrier MOS solar cell was analyzed as a function of open circuit voltage.

In order to achieve this, a number of metal-oxide solar cells are constructed in the form of aluminum-oxide-p-type silicon substrate. Measurements were performed on thesolar cells to clarify the physical phenomena governing the electrical characteristics. The experimental results obtained are generally in good agreement with the results obtained from previous workers.

Al-SiO_2-P-Si structure has a sufficiently strong inversion to become minority carrier device. This is a consequence of the fixed positive charge in oxide layer associated with excess Si. In these cells, the dark current is determined by minority carriers. In majority carrier MOS cells (Au-SiO_2-n Si) gives lower open circuit voltage than the minority-carrier MOS cells. Since the opposite excess charge (electrons) in silicon with respect to oxide layer reduces the built-in potential indicating the low barrier height.

Minority carrier MOS cells are fabricated in different techniques to understand the photovoltaic properties of devices. Solar cell 17 is fabricated using annealing procedure. As seen from Table 4.1, open circuit voltage of this cell is low. This is the consequence of the reduced

interface trap density (surface states) in annealing procedure. Solar cells which were fabricated without annealing cycle give higher open circuit voltages than the cell 17, 68. As seen from the Table 4.1 open circuit voltages of solar cells 69 and 70 are higher as compared the open circuit voltages of other cells. Oxidation of cells 69, and 70 are made in a furnace containing oxygen gaseous, and HNO_3 (Nitric) acid, respectively. In these two techniques oxidation thicknesses are greater than oxidation that grown at room temperature. Thick oxide thickness reduces the short circuit current, and does not obey MOS tunnelling theory. Thick oxide layer contains large positive charges which improves open circuit voltages.

Solar cell 17 shows low short circuit current although it is annealed. This is due to fact that, furnace is not isolated very well from the environment. Contamination and oxide gas that enter the furnace and diffuse into the semiconductor with increasing recombination centres and thus reduce short circuit current.

In theoretical analysis, positive charges and surface states enhance the open circuit voltage and reduce the dark saturation current at zero bias. In addition surface states act as recombination-generation centres and provide additional tunnelling paths between the metal and the semiconductor. Thus, short circuit current is affected by surface charges. Short circuit current also depends on the material parameters such as diffusion length, minority carrier lifetime which are mentioned in Section 3.6. These parameters vary with silicon substrate resistivity.

Capacitance of solar cell is also affected from surface state charges. As seen from Figure 4.15 which capacitance voltage characteristics of MOS solar cell 68 is shifted toward the left as compared in Figure 3.14 [27]

Although the physical origin of surface states and insulator charge is still not completely understood, surface states occur due to lattice imperfection, absorbed and adsorbed impurity atoms, and oxide layer.The surface states (traps) can have acceptor-type charges or donor-type charges. For minority carrier MOS cell, donor type surface states would be advantageous to improve open circuit voltage which indicates high barrier height.

The experimental behaviour of MOS solar cells, and in particular dependence of photovoltaic parameters on the thickness of insulating layer, is in substantial agreement with theory of MOS tunnelling structures. This is due to taking proper account of $Si-SiO_2$ interface states, their electrostatic effect as well as their dynamic effects as recombination and tunnelling centres. Communication of the interface states is greatly enhanced under illumination conditions so that (voltage dependent) population of these states differs greatly from the dark.

Resistivity of the silicon substrate affects the efficiency. Silicon which has low resistivity (high doping density) gives high short circuit with increasing efficiency as compared to silicon that has high resistivity (fabricated with the same procedure), in this work

In this work, efficiency of solar cells are very low as compared to the results given in [11]. There are many factors which decrease conversion efficiency. These are:
1-Intensity of halogen tungsten lamp which is used for the measurement of I-V characteristics under illumination is very low as compared to [11].
2- Aluminum is well known for its high reflectivity in the optical spectrum. Early works on this subject show that at 100 A^0 thickness of aluminum layer only 18-20 % transmittance can be expected. Thus, for efficient light conversion with these cells, antireflection coating is used to maximize the

transmittance. But in this work, antireflection coating is not used. Literature on antireflection coating is extensive but no single technology has emerged as prefable to date.
3- Determination of oxide thickness from the graph given in Figure 4.3 without using ellipsometry would not give an accurate thickness of oxide layer. The oxide thickness would be greater than as it is assumed. During the oxidation of silicon surface at room temperature in air, contaminations would be also grown on silicon surface. This also lowers efficiency.
4-Ohmic losses due to preparation methods.

In micro electronic device technology, the working environment must be very clean to avoid contaminations that affect the stability of device and photovoltaic response.

One of the unresolved questions concerning these cells are their long term stability, because chemicals in air and sunlight reduces their efficiencies. Therefore MOS solar cells must be stored in vacuum, but this would not be practical.

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