OCTOBER 2018 M.Sc. in Electrical and Electronics Engineering AHMET EREN

UNIVERSITY OF GAZİANTEP

GRADUATE SCHOOL OF

NATURAL & APPLIED SCIENCES

DESIGN AND IMPLEMENTATION OF A LOW COST, LOW LOSS ENERGY QUALITY REGULATOR FOR ENERGY DISTRIBUTION SYSTEMS

M. Sc. THESIS

IN

ELECTRICAL AND ELECTRONICS ENGINEERING

BY

AHMET EREN

OCTOBER 2018

Design and Implementation of a Low Cost, Low Loss Energy Quality Regulator for Energy Distribution Systems

M.Sc. Thesis

in

Electrical and Electronics Engineering

University of Gaziantep

Supervisor

Associate Prof. Dr. Ahmet Mete VURAL

by

Ahmet EREN

October 2018

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Ahmet EREN

REPUBLIC OF TURKEY
UNIVERSITY OF GAZIANTEP
GRADUATE SCHOOL OF NATURAL & APPLIED SCIENCES
ELECTRICAL AND ELECTRONICS ENGINEERING

Name of the thesis : Design and Implementation of a Low Cost, Low Loss Energy Quality Regulator for Energy Distribution Systems

Name of the student : Ahmet EREN

Exam Date : October 22, 2018

Approval of the Graduate School of Natural and Applied Sciences.

Prof. Dr. A. Necmeddin YAZICI

Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

Prof. Dr. Ergun ERÇELEBİ

Head of Department

This is to certify that we have read this thesis and that in our consensus opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

Assoc. Prof. Dr. Ahmet Mete VURAL

Supervisor

Examining Committee Members:	Signature
Assoc. Prof. Dr. Ahmet Mete VURAL	.....
Asst. Prof. Dr. Serkan ÖZBAY	.....
Asst. Prof. Dr. Bilal Monueir Saed EID	.....

ABSTRACT

DESIGN AND IMPLEMENTATION OF A LOW COST, LOW LOSS ENERGY QUALITY REGULATOR FOR ENERGY DISTRIBUTION SYSTEMS

EREN, Ahmet

M.Sc. in Electrical–Electronics Engineering

Supervisor: Associate Prof. Dr. Ahmet Mete VURAL

September 2018, 137 pages

The Energy Quality Regulator (EQR) is the solution for reactive power compensation, neutral current compensation, load balancing and harmonic current mitigation. In this thesis, design and simulation of a distribution type, voltage source inverter (VSI) based having two level inverter topologies have been carried out. The thesis is dedicated to detailed analysis, design, control, simulation and implementation of EQR for a three-phase four-wire nonlinear, unbalanced, and non-resistive loads. The power stage of VSI based EQR is composed of naturel air forced discrete IGBT modules switch at 5 kHz to reduce switching losses. The three-leg four-wire VSI topology utilizes a standard three phase PWM inverter bridge and the neutral wire is connected to the midpoint of the dc-link. Properly designed, the LCL supply filter is used instead of L type filter in this work since it provides a much better suppression at the modulation frequency. Whole compensation reference currents are extracted in the synchronous reference frame. Control has been carried out in selective manners.

The proposed VSI based EQR has been implemented after the PQ measurement for the reactive power compensation, neutral current compensation, load balancing and 3., 5., 7., harmonics current elimination of the distribution type transformer station which is 400kVA, %4 uk belongs to the Mediterranean Electricity Distribution Company.

Keywords: Reactive Power Compensation, Neutral Current Compensation, Load Balancing, Zero and Negative Sequence Compensation, Harmonic Current Mitigation, Synchronous Reference Frame, Proportional-Resonant Controller (PR)

ÖZET

ENERJİ DAĞITIM SİSTEMLERİ İÇİN DÜŞÜK KAYIPLI DÜŞÜK MALİYETLİ ENERJİ KALİTESİ DÜZENLEYİCİSİ TASARIMI VE UYGULAMASI

EREN, Ahmet

Yüksek Lisans Tezi, Elektrik-Elektronik Mühendisliği Bölümü

Tez Yöneticisi: Doç. Dr. Ahmet Mete VURAL

Eylül 2018, 137 sayfa

Enerji Kalitesi Düzenleyicisi (EKD) reaktif güç, nötr akım, düşük dereceli harmonik akım kompanzasyonu ve yük dengeleme yapması için tasarlanmıştır. Bu tezde, dağıtım tip iki seviyeli gerilim kaynaklı evirgeç dizaynı ve simülasyonu çalışılmıştır. Gerilim kaynaklı evirgeç (GKE) yapısına dayalı EKD'nin güç katı anahtarlama kayıplarını azaltabilmek için 5 kHz anahtarlama frekansında tetiklenmiş olup IGBT'lerin bu anahtarlama esnasında aşırı ısınmasını engellemek adına doğal cebri hava soğutma yöntemi kullanılmıştır. Üç-faz dört-telli gerilim kaynaklı evirgeç yapısı standart 3 faz DGM evirici yapısıyla oluşturulmuşken, kullanılan ayrık kapasitörlerin orta noktası dördüncü tel olan nötr teline bağlanmıştır. Düzgün bir şekilde tasarlanan LCL tipi besleme filtresinin modülasyon frekansında L tipi bir filtreden daha iyi bir sönümleme yapabilmesinden ötürü bu çalışmada LCL filtre tercih edilmiştir. Tüm ihtiyaç duyulan referans akımlar senkron referans çatıda üretilmiş olup, seçilimli bir kontrol mekanizması benimsenmiştir.

GKE tabanlı EKD, reaktif güç kompanzasyonu, nötr akım kompanzasyonu, yük dengeleme ve 3.,5.,7. Harmoniklerin kompanzasyonu yapması için yapılan ölçümler sonucunda ihtiyaç duyulan Akdeniz Elektrik Dağıtım Şirketine ait %4 uk, 400kVA dağıtım trafolarında test edilmiştir.

Anahtar Kelimeler: Reaktif Güç Kompanzasyonu, Nötr Akım Kompanzasyonu, Yük Dengeleme, Sıfır ve Negatif Bileşen Dengeleme, Harmonik Akım Kompanzasyonu, Senkron Referans Çatı, Oransal-Rezonatör Kontrolcüsü

"To my mother & father"

ACKNOWLEDGEMENTS

I would like to thank my supervisor Associate Prof. Dr. Ahmet Mete VURAL for his support and guidance throughout this study.

I would like to express my deepest gratitude to my honorary team leader Çağın Barış Cengiz for his guidance, criticism, encouragements, and insight throughout this research, and his unforgettable and valuable contributions to my career.

I would like to acknowledge ENDOKS Energy Systems for allowing this research work and my colleagues for their crucial contributions to this research work: Kaan Aydın for his contribution to design and implementation the HMI system and control panel design, Serbay Özkan for his contribution to programming the communication system, Bahadır Durdubaş and Kevser Duran for his contribution to control card layout design and finally Renan Mehmet Saraçoğlu for his contribution to the production and construction of the developed EQR.

I would also like to thank my managers Dr. Alper Çetin and Ç. Adnan Açık at ENDOKS Energy Systems for their understanding, help and support.

The prototype system, developed within the scope of this research work, is a part of the industrial R&D project support program project (Project No: 3151199). I would like to express my special thanks to the TÜBİTAK for their financial support. Special thanks to AKDENIZ EDAŞ A.Ş. for their courage to give us a chance to apply this technology.

I feel a deep sense of gratitude for my uncle E. Ersel Eren who formed a part of my vision and taught me the good things that really matter in my life. I would like to also express my deepest gratitude to him for his unforgettable contributions to my education life and my career.

I would like to express my very profound gratitude to my mother F. Hilal Eren, my father Mustafa Eren, my sister N. Yüsra Eren and my brother M. Erdem Eren. They all kept me going, and this thesis would not have been possible without them.

Finally, I would like to special thanks to my wife Canan Eren for her endless love, presence, patience, sacrifice, encouragement, and endless support.

TABLE OF CONTENTS

Page

LIST OF FIGURES

Page

LIST OF TABLES

Page

LIST OF SYMBOLS/ABBREVIATIONS

EQR	Energy Quality Regulator
VSI	Voltage Source Inverter
kHz	Kilo Hertz
PWM	Pulse Width Modulation
PQ	Power Quality
FACTS	Flexible AC Transmission Systems
APF	Active Power Filter
TVSS	Transient Voltage Surge Suppress
UPS	Uninterruptible Power Supply
SVC	Static VAR Compensators
UPQC	Unified Power Quality Conditioner
DSTATCOM	Distribution Static Compensator
DVR	Dynamic Voltage Regulator
ASD	Adjustable Speed Drives
SRF	Synchronous Reference Frame
MSRF	Multiple Synchronous Reference Frame
DSRF	Double Synchronous Reference Frame
AC	Alternative Current
DC	Direct Current
LV	Low Voltage
IGBT	Insulated Gate Bipolar Transistor
Hz	Hertz
FFT	Fast Fourier Transform
DFT	Discrete Fourier Transform
DSP	Digital Signal Processor
RDFT	Recursive Discrete Fourier Transform
PLL	Phase Locked Loop
LPF	Low Pass Filter

ICC	Indirect Current Control
PCC	Point of Common Coupling
PR	Proportional Resonator
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
HB	Hysteresis Band
DS	Distribution Station
SCADA	Supervisory Control and Data Acquisition
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
GTO	Gate Turn Off
IGCT	Integrated Gate Commutated Thyristor
CAD	Computer Aided Design
PSCAD	Power System Computer Aided Design
EMTDC	Electromagnetic Transient Simulation Engine
mF	Millifarad
nH	Nanohenry
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance
OrCAD	Oregon Computer Aided Design
FEA	Finite Element Analyze
Db	Decibel
RMS	Root Mean Square
MCU	Microcontroller Unit
SPI	Serial Peripheral Interface
HMI	Human Machine Interface
RTU	Remote Terminal Unit
CPU	Central Processing Unit
FPU	Floating-Point Unit
DMIPS	Dhrystone Million Instruction per Second
DSP	Digital Signal Processor
ADC	Analog Digital Converter
MSPS	Million Sample per Second
DMA	Direct Memory Access

FIFO	First In, First Out
IRP	Instantaneous Reactive Power
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
SDIO	Secure Digital Input / Output
$\boldsymbol{\mu s}$	Microsecond
PI	Proportional Integrator

CHAPTER 1

INTRODUCTION

1.1 Background and Research Motivation

An electric distribution system is a part of an electric system between the bulk power sources and the end users. The bulk power sources are located far away from the load center and are served to the consumer via the the distribution system. The widespread use of non-linear loads and power electronic converters has increased the generation non-sinusoidal and non-periodic currents and voltages in distribution systems. These loads draw currents with the lag power factor and rise harmonics and reactive power in an electric power supply. This behavior leads to a voltage distortion and effects on other loads connected to the same point. Also, this situation becomes worse when excessive current passes through the neutral wire in three-phase four-wire distribution systems because of unbalanced loads [1].

Power quality issues given above are arising and increasing day by day in the distribution system and electricity distribution companies suffer from these issues. For example, harmonic currents pollute the voltage of upstream bus in the distribution system also harmonic amplification of some harmonics may cause parallel or series resonance in network and the other issues reactive power drawn by some loads may cause voltage dips or due to excessive neutral current, neutral conductor may be bursting in the system [2].

Mainly, there are two approaches to solving power quality problems: the first one is load conditioning, which is done from the customer side, and the second one is line conditioning, which is usually done from the utility side [3]. The power quality approaches in a distribution system is concerned with load compensation to maintain power quality for each load in the distribution system. Over the years, many types of power conditioning methodologies and equipment have been developed and used to

solve power quality problems [4]. Some mitigation equipment such as active power filter (APFs), transient voltage surge suppressors (TVSS), isolation transformers, voltage regulators, uninterruptible power supply (UPS), static VAR compensators (SVC), thyristor-based static switch, Unified power quality conditioner (UPQC), distribution static compensator (DSTATCOM), dynamic voltage regulator (DVR) have been used to isolate the loads from disturbances in the distribution network [4].

In this thesis, there is a specific care implemented for some power quality problems measured from Mediterranean Electricity Distribution Company's distribution type transformers, using the advanced developments in power semiconductor technology and a VSI based compensator has been presented in selective manners than it was named as Energy Quality Regulator (EQR).

1.2 Power Quality Issues

Nowadays, power quality problems need to be considered since it is very important to maintain the electric power quality (PQ) within the standard limits. In recent times, power quality issues and custom solutions have generated a tremendous amount of interest. However, with the widespread usage of power electronic devices (nonlinear loads) and motor loadings, such as converters, adjustable speed drives (ASDs), arc furnaces, bulk rectifiers, power supplies, computers, fluorescent lamps, elevators, escalators, large air conditioning systems, and compressors, etc. [5-12], it is becoming more complex and difficult to achieve this aim. In Table 1.1 some common usage of power electronics and motor application loads are listed [5, 13].

It is the fact that, power electronic devices and electromechanical devices applications increase the distortion and disturbance on the current and voltage signals in the power network and cause a phase shift between the current and voltage.

The mentioned distortion current and voltage phase shift phenomena are in charge for reducing the power quality in the transmission and distribution power systems. It is obvious that power quality improvement is unavoidable for both utilities and customers. Therefore, power quality has become a more popular issue that is of increasing importance to electricity consumers at all levels of usage since [14-16].

Table 1.1 Power electronics and motor applications [13]

Residential	Refrigeration and freezes
	Space heating
	Air conditioning
	Cooking
	Lighting
	Electronics (personal computers, other entertainment equipment)
	Elevators, escalators
Commercial	Heating, ventilating, and air conditioning
	Central refrigeration
	Lighting
	Computers and office equipment
	Uninterruptible power supplies (UPS)
	Elevators, escalators
Industrial	Compressors
	Blowers and fans
	Machine tools (robots)
	Arc furnaces, induction furnaces
	Lighting
	Industrial lasers
	Induction heating
	Welding
	Elevators, escalators
Telecommunications	Battery chargers
	Power supplies (DC and UPS)
Transportation	Traction control of electric vehicles
	Battery charges for electric vehicles
	Electric locomotives
	Streetcars, trolley buses
	Subways
	Automotive electronics including
	Engine controls

- Nowadays there is a tremendous alteration in the load characteristic from electromechanical to computer applications. Large computer systems are used in many commercial and business areas. Power quality is more important for these

new equipment than the equipment applied before since these new equipment are more sensitive to power quality abnormality.

- Modern production manufacturers demand robust and stable power supplies. Any power quality issues happened means large economic loss especially in semiconductor production.
- The increasing importance of overall power system efficiency has resulted in a continued growth in the application of devices such as high-efficiency, adjustable-speed motor drives and shunt capacitors for power factor correction to reduce losses, resulting in increasing harmonic levels on power systems.
- The removal of imposed of power industry gives customers the right to demand higher power quality.

When these needs take into account, two common international standards relating to the voltage and current distortion as shown below may considerable.

IEEE 519:2014: IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems [14].

IEEE 1159:1995: IEEE Recommended Practice for Monitoring Electric Power Quality [15].

If we detailed analyzed power quality problems in the distribution system dominant problems can be seen as low power factor, low-frequency harmonics, neutral and unbalance currents problem.

1.2.1 Low Power Factor – Reactive Current Problem

Generally, the usage of the induction motor as an inductive loading will cause a phase shift between the voltage and current in the power systems vice versa capacitive loads also cause a phase shift between voltage and currents and it means that low power factor. Low power factor means that more reactive current and more reactive current means much losses. If reactive current increases the system,

- It means the system draws a higher internal current and excessive heat generated will damage and/or shorten equipment life.

- Increased reactive loads can reduce output voltage and damage voltage sensitive equipment
- Low power factor equipment to be constructed heavier to absorb internal energy requirements
- A system designer looks to increase power factor to lower system costs, increase reliability and increase the system's life cycle
- Utilities will charge a higher cost to industrial and commercial clients having a low power factor.

1.2.2 Current Harmonics Problem

Harmonics are sinusoidal voltages or currents having frequencies that are integer multiples of the frequency at which the supply system is designed to operate (e.g. 50 or 60 Hz). Nonlinear loads known as originates of the harmonics in the power systems and these loads can be modeled as a current source for their harmonic spectrum. In the distribution level, some equipment harmonic levels are listed in Table 1.2.

Table 1.2 Result of harmonic performance test [18]

Load	Mode	Fundamental current (A)	THD-F (%)	Dominating	
Computer with monitor	On	0.54	110	3rd	58%
Laser printer	Print	0.34	113	3rd	55%
	Idle	0.11	160	3rd	52%
Fax machine	Send	0.16	120	3rd	87%
	Print	3.74	6	3rd	5%
	Idle	0.11	98	3rd	54%
Photocopier	Copy	5.56	26	3rd	20%
	Idle	0.35	106	5th	42%
UPS #1	Server	40	35	3rd	25%
UPS #2	PC	4.3	130	3rd	89%
Magnetic ballast w/cap	On	0.21	30	3rd	18%
Electronic ballast #1	On	0.19	34	3rd	26%
Electronic ballast #2	On	0.23	10	3rd	9%
Sodium lamp	On	0.24	64	7th	44%
Compact fluorescent lamp	On	0.1	136	3rd	49%
Fan coil	On	8.5	5	5th	4.80%
Lift	Run	39	36	5th	28%

The main disadvantages of harmonics are [16, 17]

- Extra losses and overheating in capacitors, transformers and rotating machines
- Malfunction of control devices, protective relays, and signaling systems
- Telephone interface
- Additional noises for the electronic systems.

1.2.3 Excessive Neutral and Unbalance Currents Problem

The third harmonic is the most common problem for three-phase four-wire distribution systems. Third harmonic and the other multiple of third harmonics returns in the neutral wire, which can result in a current flowing in the neutral wire. In addition, the third harmonic effect, unbalanced load array for each phase can cause the excessive neutral current in the distribution system. Excessive neutral current can cause the following problems [19].

- Neutral to earth voltages that create common-mode noise problems
- Circulating currents flowing in transformers
- Unbalance phase voltages
- High voltage drops at loads
- Failure of the neutral conductor
- Overheating of the neutral line

In the distribution systems, single-phase loads are commonly used and these loads placed equally as far as possible for each phase in order to prevent the system any unbalance currents since excessive unbalance currents may cause

- The possibility of overloading the neutral conductor and it means a potential of causing a fire
- Increase the transformer losses
- Double line frequency ripple occurs in the three-phase power, and this line frequency may cause torque pulsation in three-phase generators [20].
- In [21] it was reported that the negative sequence current induced by voltage unbalance and this imbalance voltage increases the losses in the stator and rotor and decreases the net torque produced on the shaft.

1.3 Literature Review Related to the Study

Wong, Man-Chung, Dai, Ning-Yi, Lam, Chi-Seng (2016). This book describes parallel power electronic filters for 3-phase 4-wire systems, focusing on the control, design and system operation. It presents the basics of power-electronics techniques applied in power systems as well as the advanced techniques in controlling, implementing and designing parallel power electronics converters. The power-quality compensation has been achieved using active filters and hybrid filters, and circuit models, control principles and operational practice problems have been verified by principle study, simulation and experimental results [19].

Mohammed Barghi Latran, Ahmet Teke, Yeliz Yoldaş (2015) presents a comprehensive review of the various DSTATCOM configurations about single phase (2-wire) or three phase (3 or 4 -wire) systems and control strategies. Operating principles, classification of DSTATCOM based on the ower structure, reference signal extraction techniques and modulation techniques are detailed analyzed. In the final of this work, DSTATCOMs are classified according to the compensated variables [22].

Ningyun Zhang, Houjun Tang and Chen Yao (2014) have proposed a systematic method for designing PR controller and active damping of the LCL filter for single-phase grid-connected PV inverters. In this paper proposed method is supported using a numerical model, numerical simulations, and experimental results. Control scheme about the PR controller is given in this paper. Proposed PR control strategy is used to eliminate the third harmonic in this thesis [23].

Sukin Park, Soo-Bin Han, Bong-Man Jung, Soo-Hyun Choi, Hak-Geun Jeong (2000). In this paper, fifth and seventh harmonic currents are extracted using Synchronous reference frame (SRF) theory and low pass filters. The presence of fifth and seven harmonics belongs the load currents are measured separately. Proposed hybrid active filter model can be achieved dc-link regulation, fifth and seventh current harmonic compensation simultaneously [24].

Quanwei Liu, Yong Tao, Xunhao Liu, Yan Deng, Xiangning He (2013) present voltage unbalance and harmonics compensation strategy for the VSIs in the islanded microgrid. The proposed method is used synchronous reference frame (SRF) theory to

compensate for voltage unbalance and current harmonics problems. In this study impedance model of the VSI is given and analytical solutions are done by using this model. Analytical solutions are supported and validated simulations and experiments. [25].

Marco Chiadò Caponet, Francesco Profumo, Rik W. De Doncker, and Alberto Tenconi (2002). They have proposed new and innovative solutions to minimize noise and common mode conducted electromagnetic interference (EMI), in power electronic circuits using ultra-low inductive planar bus bar. This study is used to reduce the high voltage spikes during switching and designing a laminated bus bar for this thesis [26].

Yi Tang, Poh Chiang Loh, Peng Wang, Fook Hoong Choo, Feng Gao, and Frede Blaabjerg (2012). Authors are mainly focused on design, control, and implementation of an LCL-filter-based shunt active power filter to compensate harmonic currents for the three-phase four-wire power system. The general model of the LCL filter and design procedure are given with an example in this paper [27].

1.4 Objectives and Scope of the Thesis

Within the scope of this thesis, VSI based EQR employing Selective Harmonic Elimination using “Multiple Synchronous Reference Frame” MSRF technique, having simplest two-level converter topology with IGBT modules are investigated. Different reactive power control techniques are studied and Synchronous rotating (dq0) frame current controller with decoupled direct, quadrature and zero components are selected to generating the control signals for the reactive power control technique. In this method direct component of fundamental current is used for dc-link voltage regulation with the same manner quadrature component of fundamental current is used for reactive power compensation and finally, zero component of the fundamental current is used for mains neutral current compensation. Many load balancing methods are investigated and finally “Double Synchronous Reference Frame” DSRF technique is decided. With this method, negative sequence components of the fundamental current are obtained with the help of low pass filters.

A prototype EQR system is designed to be used in low voltage applications by using this theoretical work. The designed system will implement in AKDENİZ EDAŞ distribution type power transformer and connected to the system as a parallel to solve the mentioned power quality problems. Theoretical work was verified by PSCAD/EMTDC analysis, laboratory, and field tests.

1.5 Thesis Outline

The outline of the thesis is given below:

Chapter 1: Introduces power quality problems, harmful effects of these problems and preventable measures.

Chapter 2: Operating principles of EQR is presented in this chapter. System description and single line diagram is depicted to visualize the system also reference signal extraction techniques, dc-link voltage control strategy, whole compensation strategies for mentioned PQ problems and some suitable modulation techniques are presented in Chapter 2.

Chapter 3: This chapter deeply explains how to design EQR. Chapter 3 mainly focused on power stage design and selecting component size of EQR. In this chapter also gives information about electronic and electromechanical systems of EQR.

Chapter 4: It mentions about AKDENİZ EDAS measurements results and which problems are important for them. It gives information about priority selection for selective control strategy and Chapter 4 gives information about laboratory and field test results.

Chapter 5: It contains about the thesis conclusion and future works to develop the EQR system.

CHAPTER 2

OPERATING PRINCIPLE OF EQR

2.1 System Description

Figure 2.1 shows a single line diagram of a Distribution type Energy Quality Regulator (EQR) based on two level Voltage Source Inverter (VSI). It is shown to be connected to the Low Voltage (LV) distribution system via distribution type transformer.

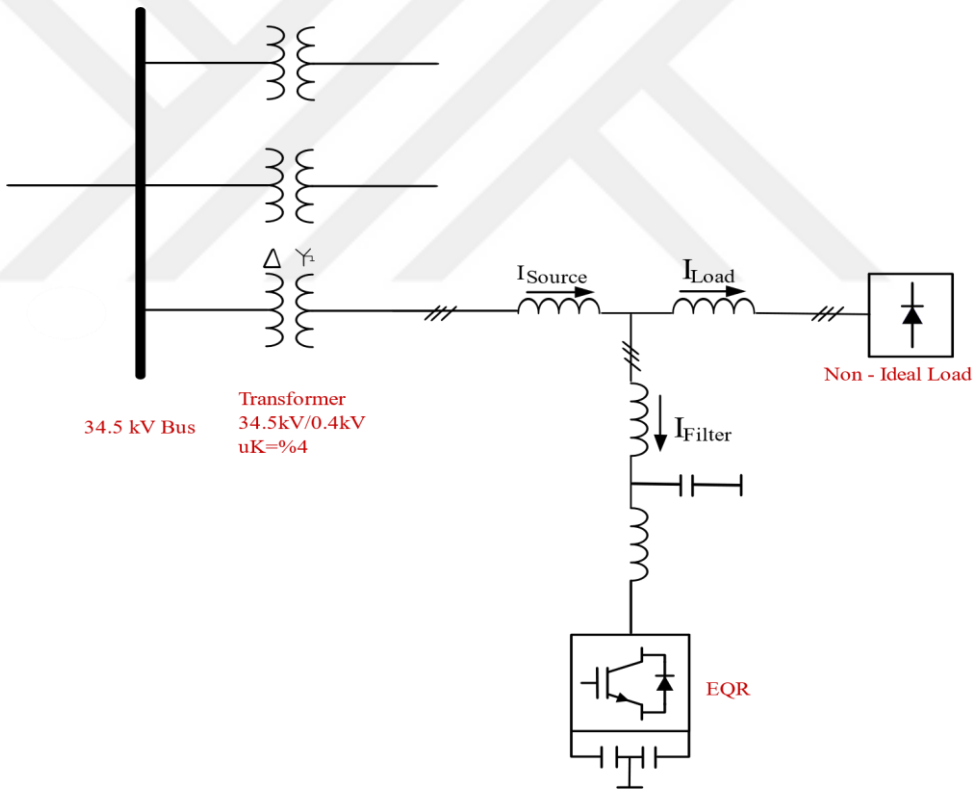

Figure 2.1 Single Line Diagram of EQR

Waveforms of source currents are distorted due to non-ideal loads. EQR is connected to the system as a parallel to produce compensating currents using LCL type filter. The midpoint of dc-link capacitors of EQR and LCL type filter capacitors are

connected to each other to create a path for neutral current and finally, both are connected to transformer neutral point.

Circuit diagram of EQR consisting of IGBT based two level VSI, dc-link capacitors, charge-discharge resistors, laminated busbar, snubbers, IGBTs & drivers and a pre-charge circuit. An EQR system operates at power frequency of 50 Hz. EQR generates reactive power compensating currents and harmonic currents in which 150 Hz, 250 Hz and 350 Hz spectrum that is opposite and in phase to eliminate harmonic components of load currents in a selective manner. Beside these features shunt compensator injects unbalanced and neutral current compensating currents using additional control loops for this purpose two level three phase neutral point clamped shunt EQR observes negative sequence and zero sequence of source currents.

To achieve these duties important factors are specify the circuit topology, reference signal extraction techniques, current control techniques and finally modulation techniques thus next stages attributes of compensator are investigated and then suitable of them are selected to obtain sufficient compensation capability of the mentioned power quality problems.

2.2 Circuit Topologies Of VSI

The voltage related PQ disturbances have similar characteristics for both single-phase and three-phase systems. In single-phase systems, reactive power and current harmonics are the main drawbacks. In three-phase three-wire (3P 3W) system, one must consider the current unbalance expected from the reactive current and current harmonics. In addition, in three-phase four-wire (3P 4W) system, an extra neutral current compensation loop should be applied to eliminate the neutral current since, in some situation, its value can take up 1.73 times of the phase current [28]. To figure out whole aforementioned problems there are many circuit configurations in the literature [22] but in this thesis most common three phases four wire VSI topologies three leg and four leg topologies are discussed since the number of switching device and passive components can be minimized and easy implementation of control and modulation strategy.

2.2.1 Three Leg 3P-4W Based Topology

In this topology, dc-link consists of number of capacitors which are equally grouped and connected as split as shown in Fig. 2.2. The midpoint of the capacitors provides a path for neutral current and fourth wire is connected here. The advantage of the three-leg topology we can reduce the number of switching devices and number of gate drivers. Besides these, this topology simplifies the modulation method.

However, in this topology, the voltage on the capacitor must be balanced to avoid circulating current on the fourth wire so it means that an additional control loop is required for this balancing work.

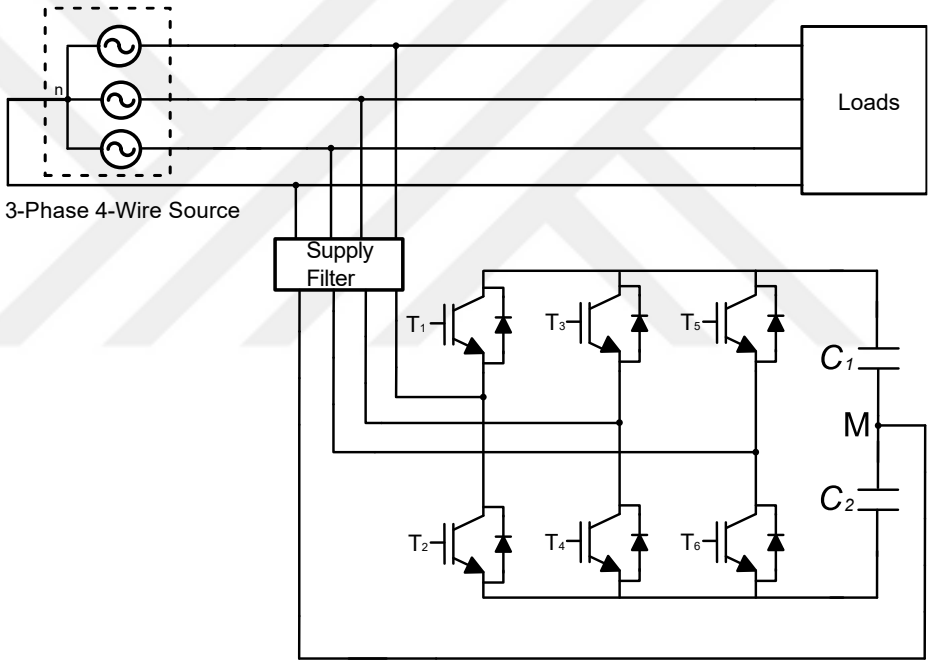

Figure 2.2 3 Leg Inverter Based 3P 4W VSC configuration with LCL filter [33]

2.2.2 Four Leg 3P-4W Based Topology

In this topology of VSI, the midpoint of the fourth leg is connected to the neutral terminal and it is controlled in such a way that the source neutral current is forced to be zero [29].

Additional power switches, gate drivers, switching losses and more complex control strategy may seem as a drawback but it offers different advantages, this type of inverter

can produce three independent output voltages for each phase for fundamental harmonics and they can reach up to $dc/\sqrt{3}$. Thanks to this feature dc-link capacitors rated voltage values and capacitance of the capacitors can be reduced. Also, lower AC rated current passing through to dc-link capacitor will reduce the number of dc-link capacitors.

Finally, reduction of neutral currents and the possibility of neutral point voltage control can be the main advantages of this type of inverter [30].

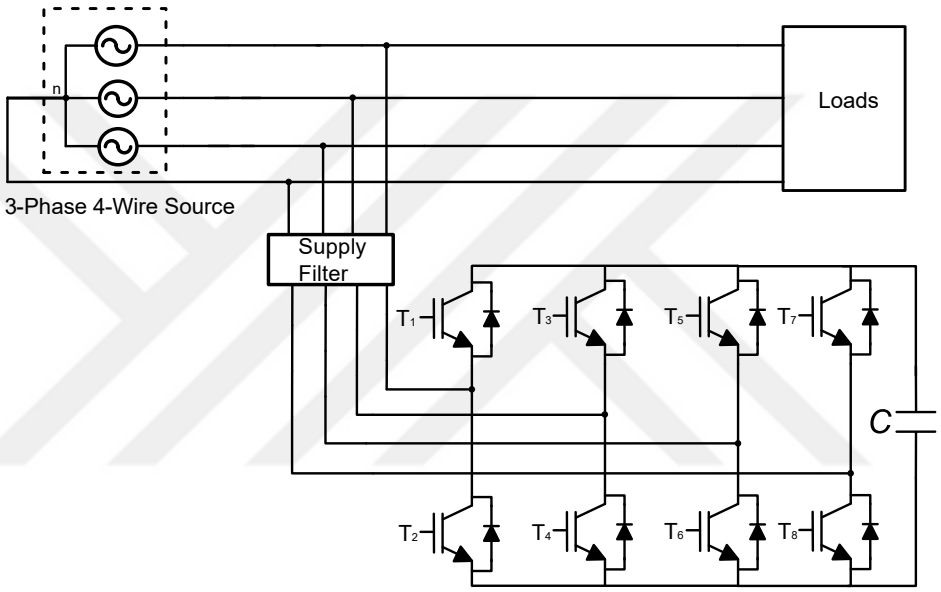

Figure 2.3 4 Leg Inverter Based 3P 4W VSC Configuration with LCL filter [33]

2.3 Reference Signal Extraction Methods & Control Techniques

In order to calculate the quality of power and to prevent the harmful effect of disturbances, many real-time methods are developed. These methods are useful for analyzing and detect properties of signals. The performance of the regulator is strictly depending on the power of the reference signal extraction techniques. Real-time reference signal extraction techniques in the literature separated mainly frequency domain methods and time domain methods. The time-domain methods are faster and easy to implement than the frequency-domain methods, but they present worse detection performance than the frequency-domain methods [22]. In this thesis, most, popular frequency domain methods and time domain methods are carried out.

2.3.1 Frequency-Domain Methods

Frequency-domain methods are applicable for both single and three-phase systems. They are mainly derived from the Fourier analysis and applying some customization it can be used for real-time systems.

2.3.1.1 Fast Fourier Transform (FFT)

An FFT is used to compute the discrete Fourier transform (DFT) and the inverse of it. A Fourier transform converts functions from time to frequency domains and vice versa. FFT computes such transformations by factorizing the DFT matrix into a product of sparse factors. In this type of applications, FFT is used to extract the harmonic components from the harmonic polluted signals. Owing to excessive computation in the online application of FFT, it has a high response time [31, 32]. With this method, DFT transform of x[n] signal can be expressed as equation (2.2).

$$X[k] = \sum_{n=0}^{N-1} x[n] e^{-\frac{j2\pi kn}{N}} = \sum_{n=0}^{N-1} x[n]\, W_N^{-kn} \qquad k = 0,1,2 \dots N-1 \tag{2.2}$$

Where N is the sample number taking from one period of the time domain. X[k] is the complex frequency component which is obtained after DFT and can be expressed as (2.3).

$$X[k] = X_r[k] + jX_{\mathrm{I}}[k] \tag{2.3}$$

As expressed in equation (2.3) $X[k]$ have real and imaginary parts. $X[k]$ includes phase and amplitude information of corresponding frequency component.

$$|X[k]| = \sqrt{X_r[k]^2 + X_j[k]^2} \tag{2.4}$$

$$\emptyset[k] = tan^{-1}\left(\frac{X_i[k]}{X_r[k]}\right) \tag{2.5}$$

With this way depending on index k, reference compounds obtained in the time domain using inverse transform of DFT.

$$X[n] = \frac{1}{N}\sum_{k=0}^{N-1} X[k]e^{-\frac{j2\pi kn}{N}} = \frac{1}{N}\sum_{k=0}^{N-1} x[n]\, W_N^{-kn} \quad n = 0,1,2 \ldots N-1 \tag{2.6}$$

In order to generate reference current using this method, just for one frequency component, N number complex multiply and $(N-1)$ complex summing is necessary. If this method expands whole spectrum, number of complexes will multiply N^2 and number of complexes sum will be $N(N-1)$. Especially in high sample frequency situation it is very hard to use DFT method for DSP applications. Many algorithms are developed to reduce complexity of DFT. FFT is the most famous of them. In this method W_N^{-kn} is periodical and symmetrical so it is not necessary to calculate W_N^{-kn} again each cycle.

Besides these features with the decimation methods calculation can be reduced sum and multiplying blocks. Most known of these methods is radix-2 decimation in the time domain and as an example for 8 sample signal application shown in Figure 2.4. With this method, the number multiplying number will reduce from N^2 to $(\frac{N}{2})\log_2 N$ [33].

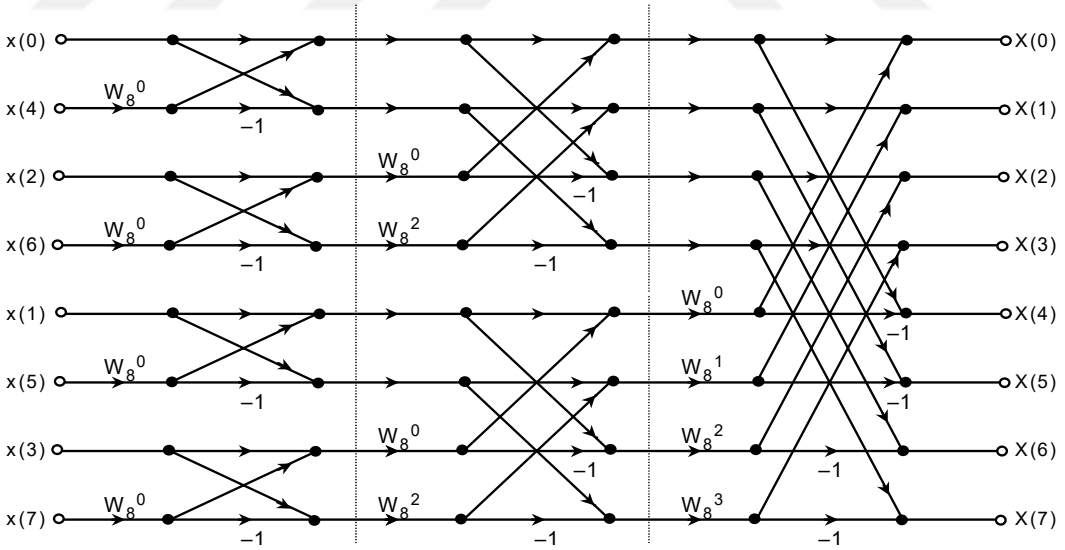

Figure 2.4 FFT with decimation in 8-dotted time domain [33]

2.3.1.2 Recursive Discrete Fourier Transform (RDFT)

The RDFT is similar to the DFT, except that the samples are obtained within a moving window of the sampled data. The RDFT has been developed at first to simplify the

computational complexity of DFT since then it was widely employed in frequency detection and phasor calculations. RDFT is very fast solution when comparing other DFT methods. There are only two multiplication processes required when calculating a new value and there is no need to whole data set, which will cause a time reduction during the calculation of the DFT, which means minimum lag during synchronization. The application scheme of RDFT methods is shown in Figure 2.5. With every new sample, frequency spectrum data will refresh, and it can be explained like equation (2.7).

$$X(k,m+1) = \sum_{n=0}^{N-1} x_{m+1}[n] W_N^{kn} = \sum_{n=0}^{N-1} x_m[n]\, W_N^{kn}$$

$$= \sum_{n=0}^{N-1} x_m[n+1] W_N^{k(n+1)} W_N^{-k} \xrightarrow{(n+1\to n)} \sum_{n=1}^{N} x_m[n]\, W_N^{kn} W_N^{-k}$$

$$= \Big(\sum_{n=0}^{N-1} x_m[n] W_N^{kn} + x[n] - x[0]\Big) W_N^{-k}$$

$$= (X(k,m) + x[N] - x[0]) W_N^{-k} = (X(k,m) + x_e) W_N^{-k} \qquad (2.7)$$

When $X(k,m+1)$ in equation 2.7 demonstrates frequency spectrum output related with new sample, $X(k,m)$ demonstrates old sample frequency spectrum output. Together with these x_e demonstrates difference between new sample and one period former sample as shown in Figure 2.5 [34-36].

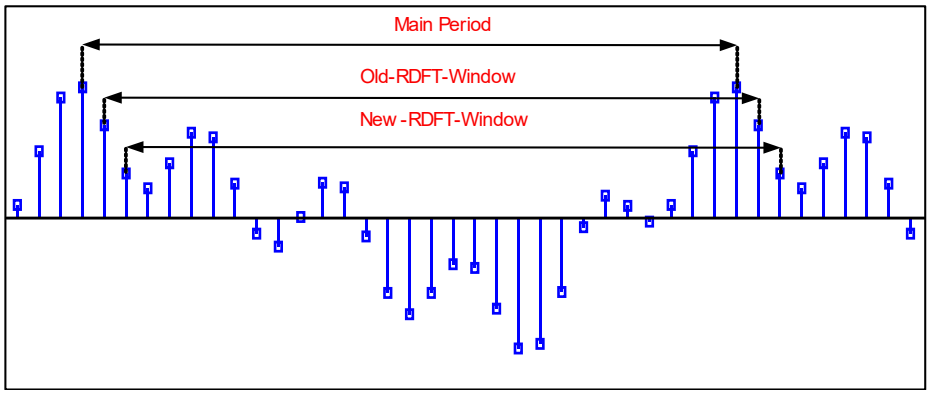

Figure 2.5 RDFT sliding window example [33]

Using this method reference current can be extracted with zero phase shift and unity gain. With this method fundamental and the other (harmonics) components of the source or load currents' frequency and gain information can be obtained.

On the other hand, the same situation is valid for positive, negative and zero sequence component of load or source currents. Reference signal extraction technique for shunt voltage source converter using RDFT method is given in Figure 2.6.

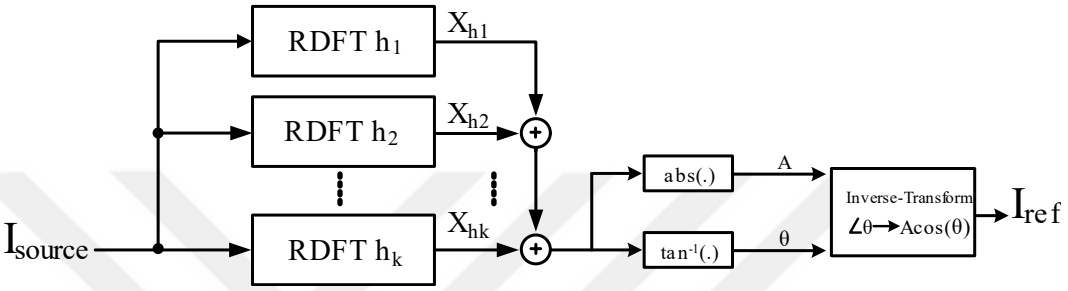

Figure 2.6 Reference Signal Extraction & Control Scheme using RDFT method [33]

As seen in Figure 2.6. each parallel RDFT branch produce harmonic component as a complex magnitude X_h obtained from each phase of source or load currents. Each X_h refers related harmonic component phase and magnitude information and these reference signals are mathematically summable. Final reference signal I_{ref} can be obtained from magnitude A and phase angle θ which are decomposition of total sum of reference signals and this summation can be inverted to the time domain from frequency domain. This calculation methods also reduce the processing load of DSP or microcontroller.

2.3.2 Time-Domain Methods

The following time-domain approaches are mainly used for three-phase systems. With some special arrangement time domain methods can be used in single phase systems.

2.3.2.1 Instantaneous Reactive Power Theory (p-q Theory)

The p-q theory is based on a set of instantaneous powers defined in the time domain. This methodology may be applied on the toltage or current waveform, and it can be

applied to three-phase system with neutral wire or without neutral wire. This technique is valid not only in the steady state but also in the transient state.

The p-q Theory first transforms voltages and currents from the ABC to αβ0 coordinates and then defines instantaneous power on these coordinates. Hence, this theory always considers the three-phase system as a unit, not a superposition or sum of three single-phase circuits [37].

The p-q theory uses the αβ0 transformations, also known as the Clarke transformation maps the three-phase instantaneous voltages in the ABC phases are transformed to the instantaneous voltages on the αβ0-axes. The Clarke transformation and its inverse transformation of three-phase generic voltages are given by using 'C' matrix [38].

$$\begin{bmatrix} v0 \\ v\alpha \\ v\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} va \\ vb \\ vc \end{bmatrix} = C \begin{bmatrix} va \\ vb \\ vc \end{bmatrix} \tag{2.8}$$

$$\begin{bmatrix} va \\ vb \\ vc \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v0 \\ v\alpha \\ v\beta \end{bmatrix} = C^{-1} \begin{bmatrix} v0 \\ v\alpha \\ v\beta \end{bmatrix} \tag{2.9}$$

Similarly, three-phase generic instantaneous line currents ia, ib and ic can be transformed to the αβ0 axes by above transformation matrix C^{-1}. The p-q Theory is defined in three phase systems with or without a neutral conductor. Three instantaneous powers are defined from the instantaneous phase voltages and line currents on the αβ0 axes as (2.10) [37].

$$\begin{bmatrix} p0 \\ p \\ q \end{bmatrix} = \begin{bmatrix} v0 & 0 & 0 \\ 0 & v\alpha & v\beta \\ 0 & v\beta & -v\alpha \end{bmatrix} \begin{bmatrix} i0 \\ i\alpha \\ i\beta \end{bmatrix} \tag{2.10}$$

2.3.2.1.1 The Zero-Sequence Power in a Three-Phase Sinusoidal Voltage Source

There are no zero-sequence current components in three-phase, three-wire systems, that is, $i0 = 0$. In this case, there will be no zero-sequence power. If there is zero-sequence power in a three-phase sinusoidal voltage source, the symmetrical components of this voltage source were calculated based on their phasors according to (2.11) and (2.12). Although this analysis is valid only for the steady state condition [37].

$$va = \sqrt{2}\,V_+ \sin(wt + \varphi_{v+}) + \sqrt{2}\,V_0 \sin(wt + \varphi_{v0})$$

$$vb = \sqrt{2}\,V_+ \sin\left(wt - \frac{2\pi}{3} + \varphi_{v+}\right) + \sqrt{2}\,V_0 \sin(wt + \varphi_{v0})$$

$$vc = \sqrt{2}\,V_+ \sin\left(wt + \frac{2\pi}{3} + \varphi_{v+}\right) + \sqrt{2}\,V_0 \sin(wt + \varphi_{v0}) \quad (2.11)$$

$$ia = \sqrt{2}\,I_+ \sin(wt + \varphi_{i+}) + \sqrt{2}\,I_0 \sin(wt + \varphi_{i0})$$

$$ib = \sqrt{2}\,I_+ \sin\left(wt - \frac{2\pi}{3} + \varphi_{i+}\right) + \sqrt{2}\,I_0 \sin(wt + \varphi_{i0})$$

$$ic = \sqrt{2}\,I_+ \sin\left(wt + \frac{2\pi}{3} + \varphi_{i+}\right) + \sqrt{2}\,I_0 \sin(wt + \varphi_{i0}) \quad (2.12)$$

The subscripts + and 0 are used to define the positive and zero-sequence components. Applying the Clarke Transformation, the following voltages and currents on the αβ0 reference frames are obtained:

$$v\alpha = \sqrt{3}\,V_+ \sin(wt + \varphi_{v+})$$

$$v\beta = -\sqrt{3}\,V_+ \cos(wt + \varphi_{v+})$$

$$v0 = \sqrt{6}\,V_0 \sin(wt + \varphi_{v0}) \quad (2.13)$$

and

$$i\alpha = \sqrt{3}\, I_{+}\sin(wt + \varphi_{i+})$$

$$i\beta = -\sqrt{3}\, I_{+}\cos(wt + \varphi_{i+})$$

$$i0 = \sqrt{6}\, I_0 \sin(wt + \varphi_{i0}) \tag{2.14}$$

Therefore zero-power will be;

$$p_0 = 3V_0 I_0 \cos(\varphi_{v0} - \varphi_{i0}) - 3V_0 I_0 \cos(2wt + \varphi_{v0} + \varphi_{i0}) = \overline{p_0} + \widetilde{p_0} \tag{2.15}$$

This power has an average value and an oscillating component at twice the line frequency. The average value $\overline{p_0}$ represents a unidirectional energy flow. The oscillating component $\widetilde{p_0}$ also trnasfers energy instantaneously and it is oscillating part average value is zero. The average zero-sequence power $\overline{p_0}$ is always associated to the oscillating component $\widetilde{p_0}$. Therefore, there is no way to eliminate the oscillating component and keep the average part alone [37].

2.3.2.1.2 Presence of Negative - Sequence Components

For a three-phase, balanced, positive sequence voltage, the presence of the negative – sequence component may be a serious problem. If the voltages are sinusoidal waveforms with a frequency w, consisting positive, negative, and zero sequence components as given below:

$$va = \sqrt{2}\, V_{+} \sin(wt + \varphi_{v+}) + \sqrt{2}\, V_{-} \sin(wt + \varphi_{v-}) + \sqrt{2}\, V_0 \sin(wt + \varphi_{v0})$$

$$vb = \sqrt{2}\, V_{+} \sin(wt - 2\pi/3 + \varphi_{v+}) + \sqrt{2}\, V_{-} \sin(wt - 2\pi/3 + \varphi_{v-}) + \sqrt{2}\, V_0 \sin(wt - 2\pi/3 + \varphi_{v0})$$

$$vc = \sqrt{2}\, V_{+} \sin(wt + 2\pi/3 + \varphi_{v+}) + \sqrt{2}\, V_{-} \sin(wt + 2\pi/3 + \varphi_{v-}) + \sqrt{2}\, V_0 \sin\left(w + \frac{2\pi}{3} + \varphi_{v0}\right) \tag{2.16}$$

and the currents consist of

$$ia = \sqrt{2}\, I_{+} \sin(wt + \varphi_{i+}) + \sqrt{2}\, I_{-} \sin(wt + \varphi_{i-}) + \sqrt{2}\, I_0 \sin(wt + \varphi_{i0})$$

$$ib = \sqrt{2}\, I_+ \sin(wt - 2\pi/3 + \varphi_{i+}) + \sqrt{2}\, I_- \sin(wt - 2\pi/3 + \varphi_{i-}) + \sqrt{2}\, I_0 \sin(wt - 2\pi/3 + \varphi_{i0})$$

$$ic = \sqrt{2}\, I_+ \sin(wt + 2\pi/3 + \varphi_{i+}) + \sqrt{2}\, I_- \sin(wt + 2\pi/3 + \varphi_{i-}) + \sqrt{2}\, I_0 \sin\left(wt + \frac{2\pi}{3} + \varphi_{i0}\right) \quad (2.17)$$

Applying the Clarke Transformation yields the following voltages and currents:

$$v\alpha = \sqrt{3}\, V_+ \sin(wt + \varphi_{v+}) + \sqrt{3}\, V_- \sin(wt + \varphi_{v-})$$

$$v\beta = -\sqrt{3}\, V_+ \cos(wt + \varphi_{v+}) + \sqrt{3}\, V_- \cos(wt + \varphi_{v-})$$

$$v0 = \sqrt{6}\, V_0 \sin(wt + \varphi_{v0}) \quad (2.18)$$

and

$$i\alpha = \sqrt{3}\, I_+ \sin(wt + \varphi_{i+}) + \sqrt{3}\, I_- \sin(wt + \varphi_{i-})$$

$$i\beta = -\sqrt{3} I_+ \cos(wt + \varphi_{i+}) + \sqrt{3}\, I_- \cos(wt + \varphi_{i-})$$

$$i0 = \sqrt{6}\, I_0 \sin(wt + \varphi_{i0}) \quad (2.19)$$

If there is an imbalance on the system negative sequence component will occur on the system. Therefore, power equations must rewrite as equation 2.20 below,

$$\overline{p} = 3V_+ I_+ \cos(\varphi_{v+} - \varphi_{i+}) + 3V_- I_- \cos(\varphi_{v-} - \varphi_{i-})$$

$$\overline{q} = 3V_+ I_+ \sin(\varphi_{v+} - \varphi_{i+}) + 3V_- I_- \sin(\varphi_{v-} - \varphi_{i-})$$

$$\tilde{p} = -3V_+ I_- \cos(2wt + \varphi_{v+} + \varphi_{i-}) - 3V_- I_+ \cos(2wt + \varphi_{v-} + \varphi_{i+})$$

$$\tilde{q} = -3V_+ I_- \sin(2wt + \varphi_{v+} + \varphi_{i-}) + 3V_- I_+ \sin(2wt + \varphi_{v-} + \varphi_{i+}) \quad (2.20)$$

2.3.2.1.3 Presence of Fifth Harmonic Component

Three phase balanced voltage may consist of both fundamental positive-sequence components and large harmonic spectrum. In this case, only fifth harmonic component will be considered. Since the fifth harmonic has only negative sequence component,

$$i_{a5}(t) = \sqrt{2}\, I_{-5}\sin(5wt + \delta_{-5})$$

$$i_{b5}(t) = \sqrt{2}\, I_{-5}\sin\left(5wt + \delta_{-5} + \frac{2\pi}{3}\right)$$

$$i_{c5}(t) = \sqrt{2}\, I_{-5}\sin\left(5wt + -\frac{2\pi}{3}\right) \quad (2.21)$$

The subscript '-' indicates a negative sequence component and subscript '5' indicates fifth harmonic frequency. The Clarke Transformation of the currents in the 2.22

$$i_{\alpha 5} = \sqrt{3}\, I_{-5}\sin(5wt + \delta_{-5})$$

$$i_{\beta 5} = \sqrt{3}\, I_{-5}\cos(5wt + \delta_{-5}) \quad (2.22)$$

The real and imaginary powers are calculated as the following oscillating components:

$$\tilde{p} = -3V_{+1}I_{-5}\cos(6wt + \delta_{-5})$$

$$\tilde{q} = -3V_{+1}I_{-5}\sin(6wt + \delta_{-5}) \quad (2.23)$$

2.3.2.1.4 Presence of Seventh Harmonic Component

Since the seventh-harmonic is the positive-sequence harmonic calculation must be like (2.24),

$$i_{a7}(t) = \sqrt{2}\, I_{+7}\sin(7wt + \delta_{+7})$$

$$i_{b7}(t) = \sqrt{2}\, I_{+7}\sin\left(7wt + \delta_{+7} - \frac{2\pi}{3}\right)$$

$$i_{c7}(t) = \sqrt{2}\, I_{+7}\sin\left(7wt + \delta_{+7} + \tfrac{2\pi}{3}\right) \quad (2.24)$$

The Clarke transformation of the currents are

$$i_{\alpha 7} = \sqrt{3}\, I_{+7}\sin(7wt + \delta_{+7})$$

$$i_{\beta 7} = -\sqrt{3} I_{+7} \cos(7wt + \delta_{+7}) \tag{2.25}$$

The real and imaginary power oscillating parts are

$$\tilde{p} = 3V_{+1} I_{+7} \cos(6wt + \delta_{+7})$$

$$\tilde{q} = -3V_{+1} I_{+7} \sin(6wt + \delta_{+7}) \tag{2.26}$$

In both case, the real and imaginary powers have only oscillating components at six times the system frequency.

Reference Signal extraction & control technique for shunt voltage source converter using p-q theory is given in Figure 2.7.

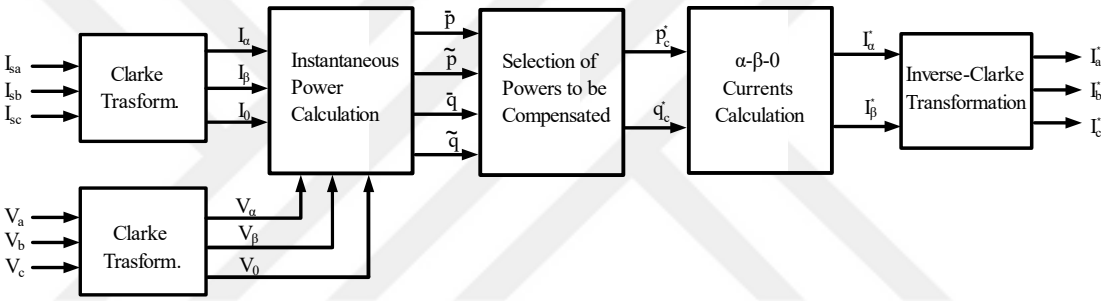

Figure 2.7 Reference Signal Extraction & Control Scheme using Instantaneous Reactive Power Theory [37]

Figure 2.7. demonstrates a general control technique to be employed in the controller of a shunt compensator. Calculated real power p is composed average ($\overline{p}$) and oscillating ($\tilde{p}$) parts. Likewise, imaginary power q is also composed average ($\overline{q}$) and oscillating part ($\tilde{q}$). Then unwanted parts of the real and imaginary parts of the source that ought to be compensated are chosen. Selected powers to be compensated p_c^* and q_c^* are undesired powers on the system and for the compensation mission -p_c^* and -q_c^* are the inputs for the inverse transformation. After the inverse transformation instantaneous three-phase compensating currents I_a^*, I_b^* and I_c^* are obtained. Inverse – Clarke transformation calculation is carried out using C^{-1} expressed in (2.9).

2.3.2.2 Synchronous Frame-Based Theory (d-q-0 Theory)

In this method symmetrical three-phase voltage or current are transformed direct, quadrature and zero sequence component in a synchronously rotating frame using transformation matrix 'T' in (2.27) also known as 'Park Transform'. In the space, the frame will synchronize to the phase angle of the AC utility voltage and for 50 Hz system the corresponding rotating frame angular speed $w_p(t)$ will be $2\,x\,\pi\,x\,50 = 314\,radians/second$ as shown in Figure 2.8. The direct and quadrature components are symbolized active and reactive components of the system. Despite, main aim is to obtain dc quantities in a rotating frame, but higher-order harmonics will remain if there are harmonics in the phase voltage or current.

Basically, this transformation calculating by using transformation matrix 'C' given (2.8) and synchronizing to the phase angle θ of the AC utility voltage. Using matrix 'T' transformation is calculated for three phases voltages can be performed as (2.27),

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & sin(\theta) & 0 \\ -sin(\theta) & cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = T \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} \tag{2.27}$$

where the transformation matrix 'T' is shown in equation (2.28).

$$\mathrm{T} = \begin{bmatrix} \cos(\theta) & sin(\theta) & 0 \\ -sin(\theta) & cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{2.28}$$

The equation (2.27) describes the general convention of the Park Transform for Synchronous Reference Frame Theory. This convention based on 'cosine' function as reference. However, in this thesis the matrix T is redefined as 'sine' function-based transformation is used. To achieve this mission $\pi/2$ is subtracted from the θ since 'sine' function lags the 'cosine' function by $\pi/2$ rad.

$$\theta = \theta - \frac{\pi}{2} \tag{2.29}$$

In this case, the T matrix (2.28) becomes as

$$T = \begin{bmatrix} \cos(\theta - \pi/2) & sin(\theta - \pi/2) & 0 \\ -sin(\theta - \pi/2) & cos(\theta - \pi/2) & 0 \\ 0 & 0 & 1 \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -cos(\theta) & 0 \\ cos(\theta) & sin(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (2.30)$$

Transformation angle and magnitude of the balanced three-phase system can be calculated according to Figure 2.8. then can be calculated in (2.31) and (2.32) respectively,

$$\theta_p = \arctan(v_\beta / v_\alpha) \quad (2.31)$$

$$|V| = \sqrt{{v_\alpha}^2 + {v_\beta}^2} \quad (2.32)$$

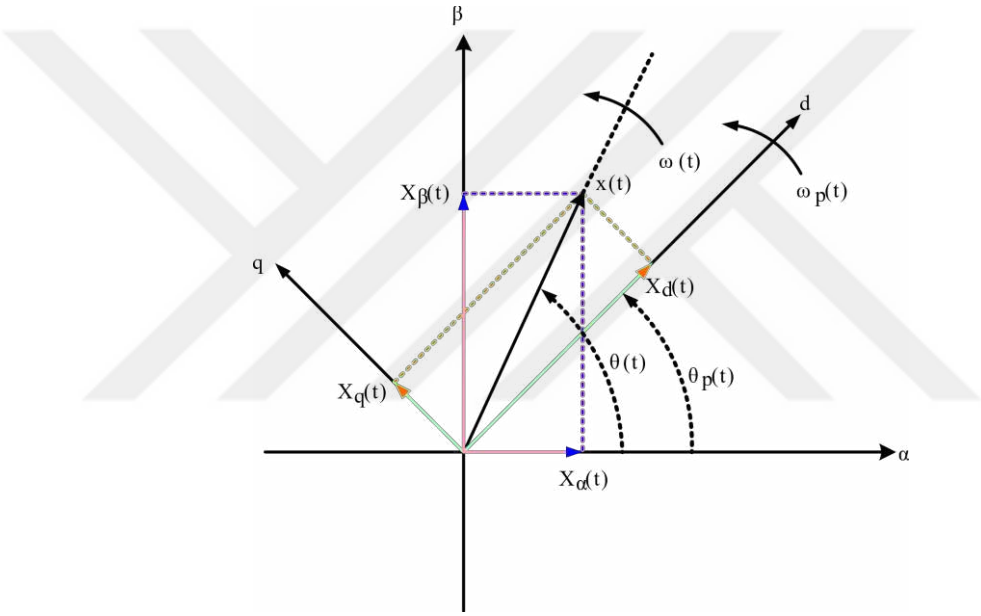

Figure 2.8 Space vectors representation of alpha-beta vector to d-q vector transformation [33]

If the transformation angle is equal to the phase angle $\theta_p = \theta$, and d and q vectors are represented as dc quantities, thanks to these features using low level compensators, high performance control systems can be developed [33].

Phase angle θ is obtained using Phase Locke Loop (PLL) algorithm. Many PLL algorithm represented in the literature and they can be classified into three phase PLL methods and single phase PLL methods [39-46]. According to this review, Inverse Park PLL structure is chosen due to more effective and stable than the others. The block scheme of Inverse Park PLL structure is given in Figure 2.9. In the three-phase system reference signals for the mentioned problems can be generated using

synchronous reference-based theory except third harmonic currents. Third harmonic compensation techniques will have discussed the following pages.

After the reference signal extraction calculation, matrix T^{-1} given in (2.33) is used in order to transformed back to alpha-beta axes.

$$T^{-1} = \begin{bmatrix} \sin(\theta) & cos(\theta) & 0 \\ -cos(\theta) & sin(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{2.33}$$

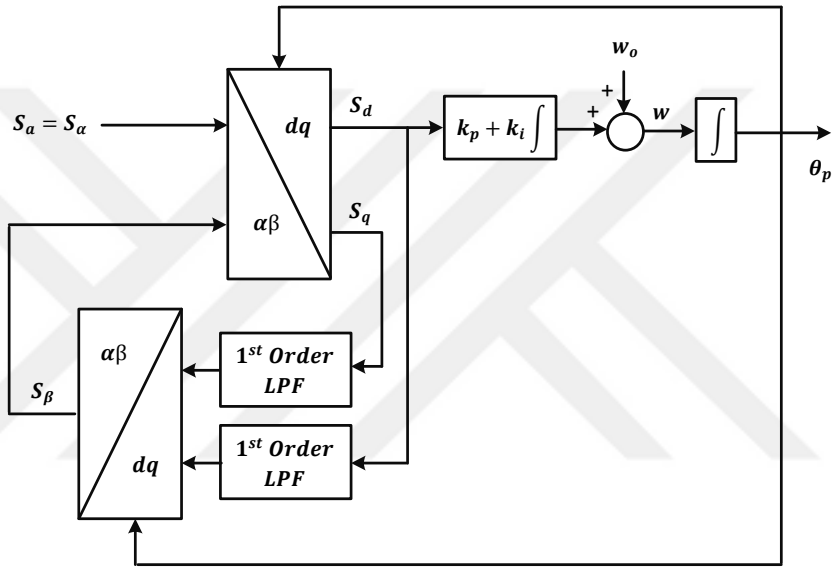

Figure 2.9 Inverse Park PLL structure block scheme

2.3.2.2.1 Presence of Zero Sequence Component

The zero-sequence component in the three-phases four-wire system can be represented zero component of the Park Transformation. These zero components can be obtained directly from zero component of the Clarke Transformation.

$$\begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & sin(\theta) & 0 \\ -sin(\theta) & cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = T \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \tag{2.34}$$

As seen in (2.34) $I_0 = i_0$ therefore voltage or current zero sequence components are handled by Clarke Transformation of the voltage or current. This component will be

used for neutral current compensation and split capacitor-based dc-link capacitors' voltage balance control of the system and control methodology will discuss in the next sections.

2.3.2.2.2 Presence of Negative - Sequence Components

It is commonly known that when the unbalance occurrs in the three-phase system negative sequence component will appear in the system. The negative sequence component in the system can be found using the Synchronous Reference Frame Theory. Matrix T of (2.28) utilizing - θ instead of θ and then using this angle negative sequence fundamental frequency components of load or source current appear as dc quantities if there is no harmonic component in the currents. If there are harmonic components in load or source current it will appear as AC quantities in this case using LPF structure negative sequence fundamental frequency components can be extracted [47].

$$\begin{bmatrix} I_{dneg} \\ I_{qneg} \end{bmatrix} = \begin{bmatrix} \sin(-\theta) & -\cos(-\theta) \\ \cos(-\theta) & \sin(-\theta) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = T_- \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.35}$$

If there is no harmonic component in the (2.35), the equation will be (2.36).

$$\begin{bmatrix} I_{dneg} \\ I_{qneg} \end{bmatrix} = I_+ \begin{bmatrix} cos(2\theta + \varphi_+) \\ sin(2\theta + \varphi_+) \end{bmatrix} + I_- \begin{bmatrix} cos(\varphi_-) \\ sin(\varphi_-) \end{bmatrix} \tag{2.36}$$

As understood from (2.36) fundamental components of the current appears at 100 Hz for 50 Hz utility after this transformation and also it means it is an AC quantity. If we eliminate this component, fundamental negative components of the system will occur as a dc quantity.

2.3.2.2.3 Presence of Fifth Harmonic Component

The fifth harmonic AC component can be represented as dc component using matrix T in (2.28) utilizing - 5θ instead of θ. There is a minus sign in the theta since fifth harmonic component is negative sequence harmonic and magnitude '5' is the order of harmonic which want to be extracted.

$$\begin{bmatrix} I_{d5} \\ I_{q5} \end{bmatrix} = \begin{bmatrix} \sin(-5\theta) & -\cos(-5\theta) \\ \cos(-5\,\theta) & \sin(-5\,\theta) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = T_5 \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (2.37)$$

After the transformation given in (2.37), the equation will be (2.38)

$$\begin{bmatrix} I_{d5} \\ I_{q5} \end{bmatrix} = I_+ \begin{bmatrix} cos(6\theta + \varphi_+) \\ sin(6\theta + \varphi_+) \end{bmatrix} + I_5 \begin{bmatrix} cos(5\varphi_-) \\ sin(5\varphi_-) \end{bmatrix} \quad (2.38)$$

As seen in (2.37) AC and DC quantities appear in the signal. AC quantities represented in (2.37) appears at 300 Hz for 50 Hz utility and these components can be subtracted from the signal by using a suitable LPF structure.

2.3.2.2.4 Presence of Seventh Harmonic Component

The seventh harmonic reference can be generated with the same manner of the fifth harmonic extraction techniques, but it is the fact that seventh harmonic is the positive sequence harmonic, so matrix T utilize 7θ instead of -5θ. Magnitude '7' represents the harmonic order of the signal.

$$\begin{bmatrix} I_{d7} \\ I_{q7} \end{bmatrix} = \begin{bmatrix} \sin(7\theta) & -\cos(7\theta) \\ \cos(7\,\theta) & \sin(7\,\theta) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = T_7 \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (2.39)$$

After the transformation given in (2.39), the equation will be (2.40)

$$\begin{bmatrix} I_{d7} \\ I_{q7} \end{bmatrix} = I_+ \begin{bmatrix} cos(6\theta + \varphi_+) \\ -sin(6\theta + \varphi_+) \end{bmatrix} + I_7 \begin{bmatrix} cos(7\varphi_+) \\ sin(7\varphi_+) \end{bmatrix} \quad (2.40)$$

again, AC quantities appear at 300 Hz for 50 Hz utility so the selected LPFs should have maximally flat and unity gain characteristic at their pass-band region and should provide adequate attenuation for the harmonic components which appear at 300 Hz. After these explanations general reference current extraction technique can be explained as the shunt voltage source converter in the synchronous reference frame is like in Figure 2.10.

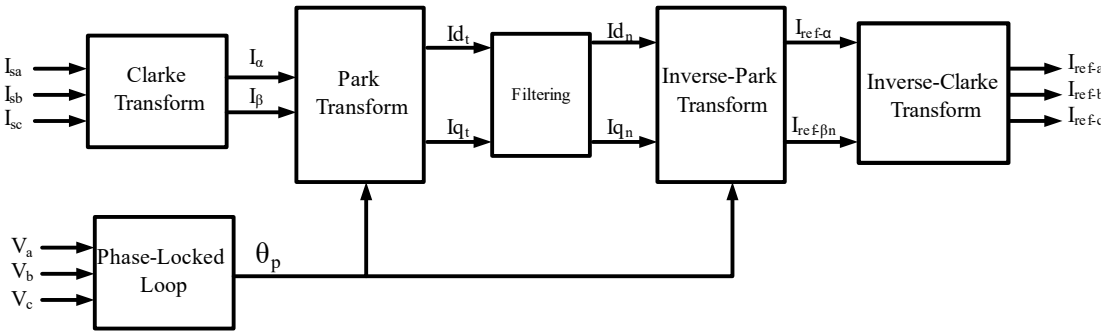

Figure 2.10 Reference Signal Extraction & Control Scheme using Synchronous Reference Frame Theory [33]

Figure 2.10 is the basic reference current extraction scheme for the synchronous reference-based theory. This scheme can be rearranged according to needs for the reference signal extraction. With the help of the PLL the scheme locks the utility phase and using the 'Park Transform' Id and Iq components are obtained. These components have AC and DC quantities as mentioned before. After the proper filtering stage, final reference signals can be used for the controlling next 'Inverse Park Transform' is calculated by the help of inverse matrix T^{-1} with suitable θ. Finally, 'Inverse Clarke Transform' is used with the help of matrix C^{-1} and reference currents are generated.

2.4 Control Strategies Of EQR

In this thesis, the current controller is realized in the synchronous reference frame for generating reference signals which are further used to produce switching signals. This section generally includes about how EQR follows extracted reference signals and how switching signals transfer to the power stage with minimum errors and as a summary how EQR is controlled to achieve compensation mission. All about this control strategies for EQR are discussed in this section.

2.4.1 Voltage Control of DC-Link Capacitor

Sufficient dc-link voltage level is required to achieve compensation mission as capacitive energy storage element is used in the dc-link. The EQR needs to draw certain amount of active power from the supply to cover its power loss (due to the switching) and to maintain the desired dc-link voltage level. If the supply voltage is sinusoidal, symmetrical and balanced, the d component of the supply voltage V_{sd} will be constant and peak value of the phase to neutral voltage. Additionally, in this

condition the q component of the phase to neutral voltage V_{sq} will be zero so instantaneous active power equation can be written like (2.41).

$$P_{EQR,3\emptyset} = \frac{3}{2} V_{sd} I_{fd} = \frac{3}{2} \widehat{U_S} I_{fd} \tag{2.41}$$

In this equation $\widehat{U_S}$ refers peak value of the phase to neutral voltage of the supply voltage so this value cannot be controlled. According to the (2.41) the three-phase instantaneous active power of the EQR only be controlled by the d component of the EQR current. In this manner the dc-link control of the EQR is given in the Figure 2.11.

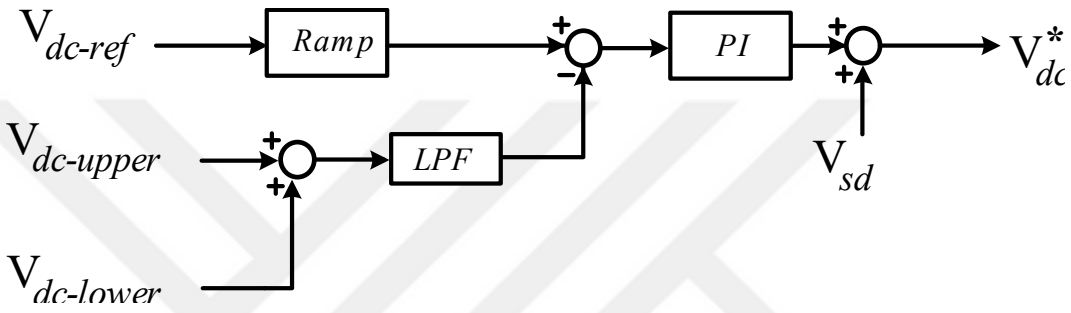

Figure 2.11 DC-link Voltage Control Block

Proposed control algorithm is shown in Figure 2.11. creates a reference to regulate the DC bus voltage to its reference value V_{dc-ref} . To prevent instantaneous over current problem the Ramp block is used. This block increases V_{dc-ref} value slowly from end of the pre-charge state dc-link value to desired final reference value. This block can be described as a smoother for unexpected overcurrent problems. The feedback signal of the dc-link voltage is the summation of the upper capacitors voltage signal $V_{dc-upper}$ of the split dc-link and the lower capacitors voltage signal $V_{dc-lower}$ of the split dc-link. The total feedback signal requires filtering since dc-link voltage has voltage ripple at 100 Hz. Because, the EQR has a two-level topology each of half bridges produces ripple at the twice of the fundamental frequency. Thus, first order 20-100 Hz LPFs can be utilized in the feedback path. Feedback control is combined with feedforward term of source voltage d component V_{sd} to improve performance over simple feedback control since feedforward control can eliminate the effect of the measured disturbance on the output. The final reference V_{dc}^{*} added to the d component of the current reference extraction scheme is shown in Figure 2.66. In the split capacitor topology, the main drawback is balancing voltage level of the upper

capacitor group and lower capacitor group to prevent this problem another control loop is used shown in Figure 2.12.

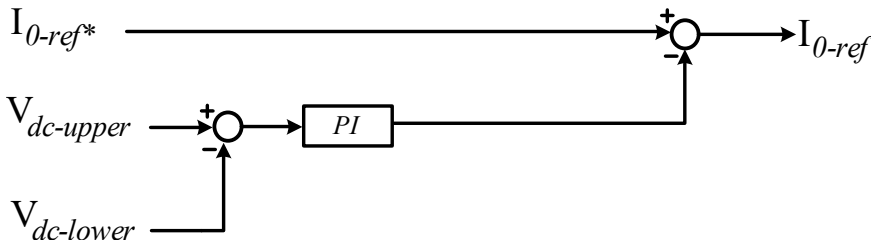

Figure 2.12 DC-link Voltage Balance Control Block

The zero component of the current reference extraction scheme is used for this control since zero-sequence current flows through to split capacitors. According to the Figure 2.12 upper and lower dc voltages are read separately and their differences are an input for another PI controller to control unbalance voltage level of upper and lower dc voltages. The output of the PI controller will subtract from reference zero sequence component to obtain final zero sequence reference. Applied control block output is given in Figure 2.13. according to the PSCAD analysis which EQR PSCAD model is

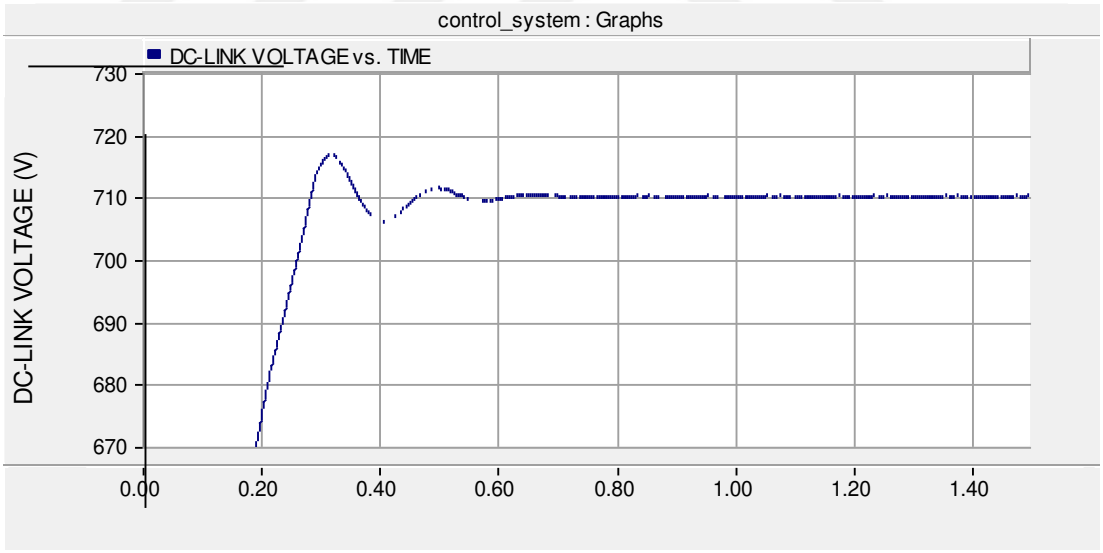

Figure 2.13 DC-link Voltage Control Analysis in PSCAD/EMTDC

given in Appendix A, first overshoot occurs at 717 V and it is in the applicable limits. After the second overshoot dc-link voltage is stabilized.

2.5 Reactive Power Compensation Controller

EQR is a VSI based system that can be injected or absorbed reactive current I_R, independent from grid voltage V_s. Figure 2.14. shows the basic block diagram of the EQR. It is the fact that, grid node voltage will extremely be influenced from this reactive current flow. To control the reactive current flow between source and EQR indirect current control (ICC) strategy [48] has been chosen since whole reference signals are extracted in synchronous reference frame. In order to prevent complexity in the control system and the dynamic response of the SRF technique, it was thought that ICC method is applicable for this compensator.

In the ICC control strategy, q component of the source current is calculated with the help of SRF method. The reactive power of the mains is calculated according to the (2.42).

$$Q_{source,3\emptyset} = \frac{3}{2} x\left(V_{sq} x I_{sd} - V_{sd} x I_{sq}\right) \tag{2.42}$$

If the supply voltage is sinusoidal, symmetrical and balanced than q component of the source voltage V_{sq} will be zero. In this case to calculate the reactive power of the source

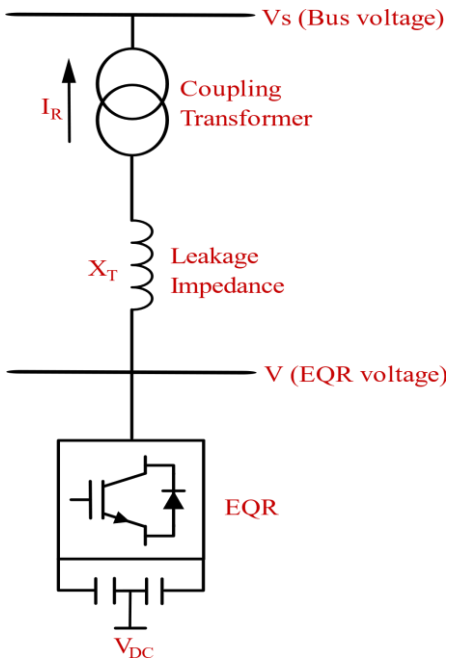

Figure 2.14 Basic EQR model

two important parameters are necessary, these are d component of the source voltage V_{sd} and q component of the source current I_{sq}. In this thesis non-ideal supply voltage conditions take care and the control technique takes advantage of (2.42) to produce desired reactive power (Q_{ref}) at the Point of Common Coupling (PCC), q component of the EQR current I_{fq} is given in (2.43) can be used to produce reference I_{sq-ref} to compare I_{fq} and control reactive power flow on the system.

$$I_{sq-ref} = \frac{-{}^{2}/_{3}\, xQ_{ref} + V_{sq} x I_{sd}}{V_{sd}} \tag{2.43}$$

I_{sq-ref} is obtained from (2.43) which represents desired reactive power (Q_{ref}) current q component at the PCC. To obtain desired reactive power at the PCC, control algorithm shown in Figure 2.15. is used.

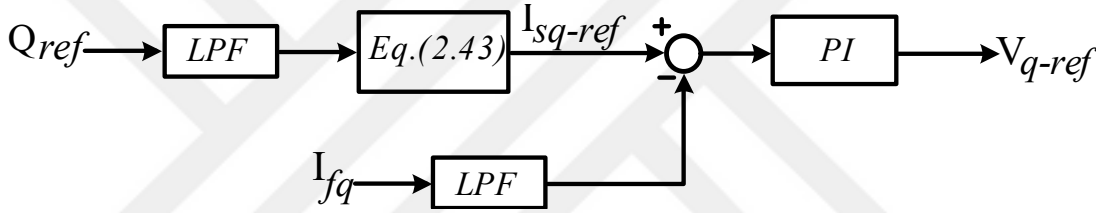

Figure 2.15 Reactive Power Control Block

In the reactive power control block given in Figure 2.15., Q_{ref} is calculated according to (2.42) and using first order 100 Hz LPF and using (2.43) the reactive component of the source current I_{sq-ref} can be applied to reactive power control block as a reference. To compensate whole reactive power at the PCC, Q_{ref} must be reverse of mains reactive power since according to this controller EQR will try to produce reference reactive power Q_{ref}. If Q_{ref} is variable according to the load the controller will detect reactive power at the PCC and produce magnitude of required voltage reference signal to accomplish dynamic reactive power control. However, important thing is here EQR must generate a fundamental frequency voltage which is in the same phase with grid voltage only the magnitude of the EQR voltage may change to control reactive power flow on the system.

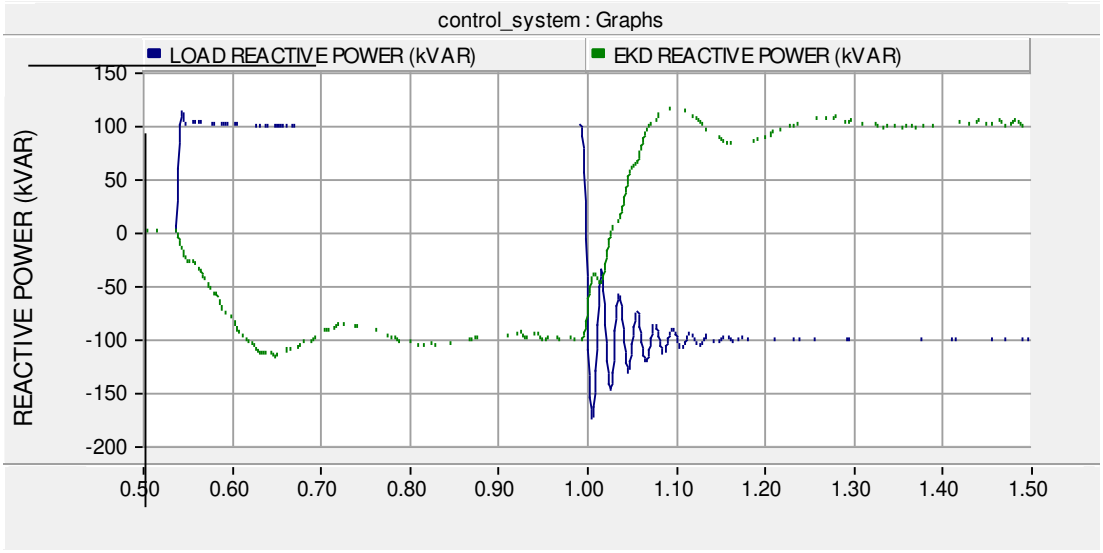

Figure 2.16 Reactive Power Control Block Dynamic Analysis in PSCAD/EMTDC

According to the PSCAD/EMTDC analysis of the reactive power control block given in Figure 2.16, system can response reactive power change at the PCC. This analysis is done according to the ±100 kVAR load reactive power change since these limits are EQR power limits. In the Figure 2.16 blue line demonstrates load reactive power and green line is the response of the EQR. Response time of the EQR can be increased by using integrator constant. Response time of the EQR seems to be slow. However, reactive power is calculated according to the 2.42 and first order 100 Hz LPF is used to measure reactive power at the PCC. Due to the filter reactive power response time printed with filter delay.

2.6 3rd Harmonic Currents Compensation Controller

3rd harmonic and multiply of the third harmonics are called as triplen harmonics. These triplens are in phase with each other and directionless so in the synchronous reference frame reference current cannot extract. Due to the complexity and the other drawbacks, Fourier transform based algorithms aren't used to control third harmonic. In such situation according to the internal model principle [49], Proportional Resonator (PR) regulator is the best solution for tracking the sinusoidal reference signal and harmonic elimination. An ideal form of PR regulator is given in (2.44).

$$G_{PR}(s) = K_p + \frac{2K_r s}{s^2 + w_h^2} \tag{2.44}$$

Where K_p and K_r are the proportional and the resonant control gain respectively, w_h is the fundamental angular frequency of the source. The PR controller enhances an infinite gain at the selected frequency (resonant frequency) with zero phase shift. The ideal PR controller bode diagram is given in Figure 2.17. but this type of controller cannot be applied in a physical circuit because the controller given in (2.44) is a lossless controller.

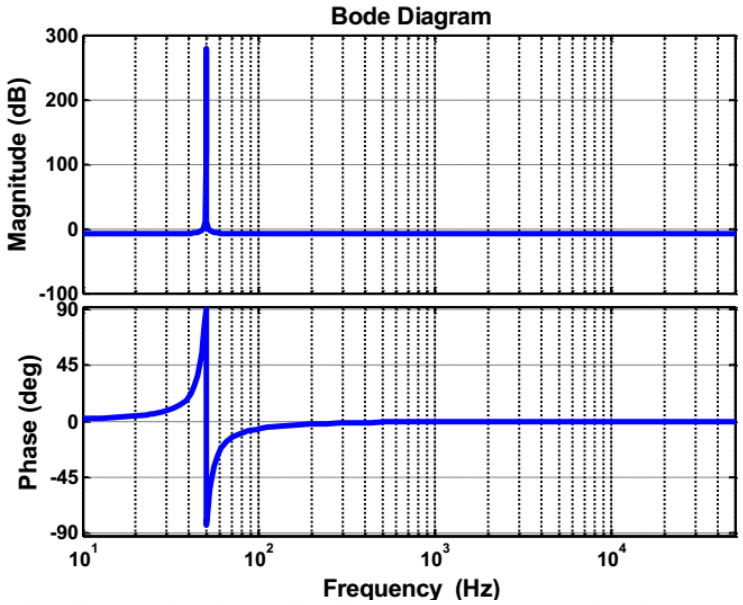

Figure 2.17 Ideal PR controller Bode diagram [23]

The block diagram of $G_{PR}(s)$ can be demonstrate in Figure 2.18. also, it is internal structure of used PR control block in this thesis.

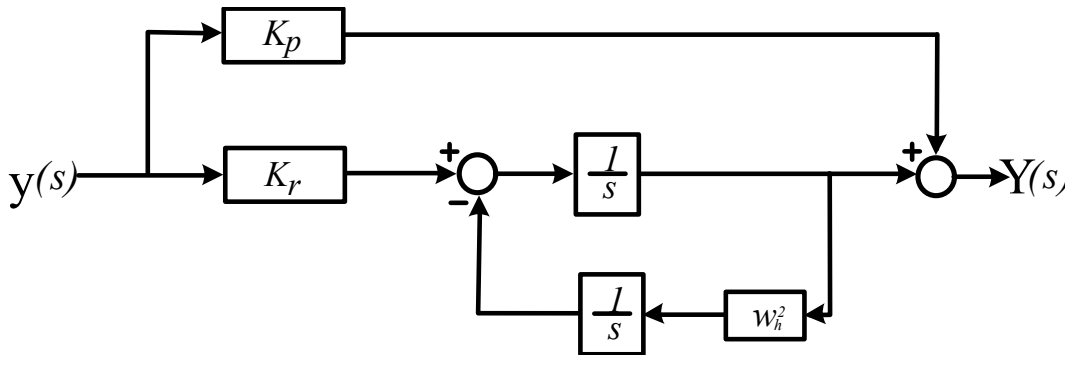

Figure 2.18 PR controller block diagram

In this controller integral term also behaves high-gain low-pass filter. The proportional gain K_p primarily controls the dynamics of the controller, while K_r regulate the

amplitude of the gain at the selected frequency and controls the band with around it [23]. To tracking and eliminating third harmonic at the PCC, controller tuned to 150 Hz and the control mechanism shown in Figure 2.19. is used.

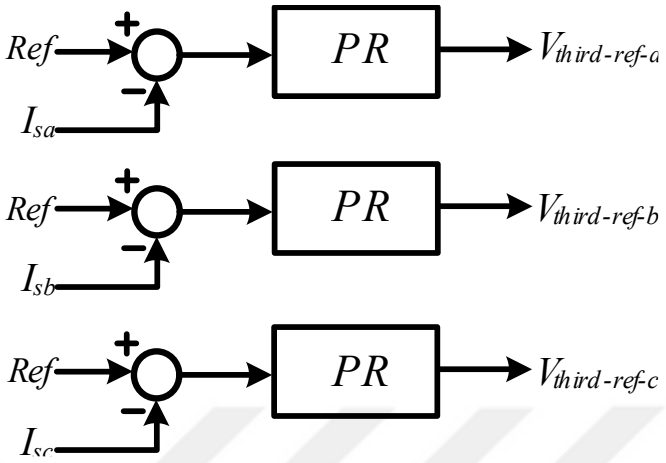

Figure 2.19 Third Harmonic Control Block Diagram

Because of the non-linear single-phase loads third harmonic is the main problem for distribution system so the third harmonic wants to be canceled since it is very harmful both distribution transformer and the neutral conductor due to this reasons reference value Ref will be zero. It means that there is no more third harmonic wants to be in the system. Firstly, third harmonic controller will extract third harmonic component from the source currents I_{sa}, I_{sb} and I_{sc} and than it will try to produce third harmonic reference voltage to eliminate third harmonic from the system. PSCAD/EMTDC analysis results of the PR controller for the third harmonic current compensation are given in Figure 2.20-2.28.

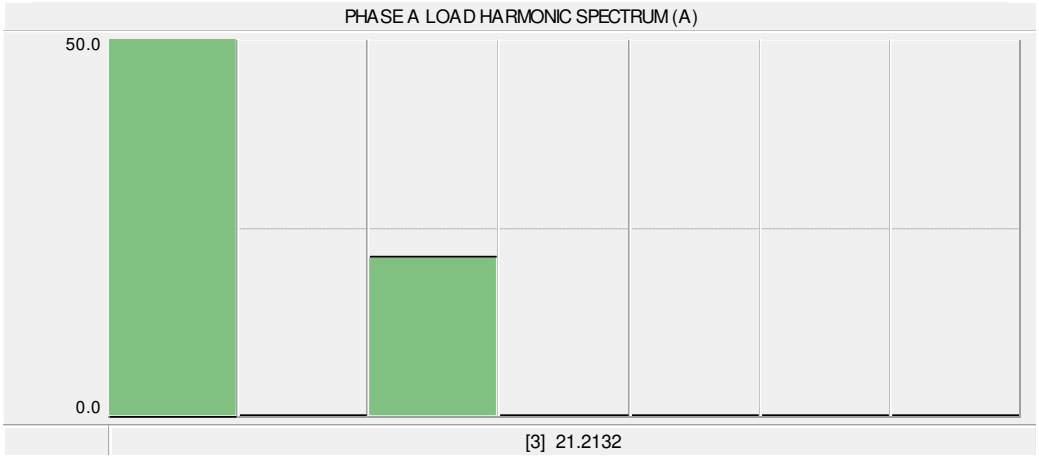

Figure 2.20 Phase A Load Harmonic Current Spectrum

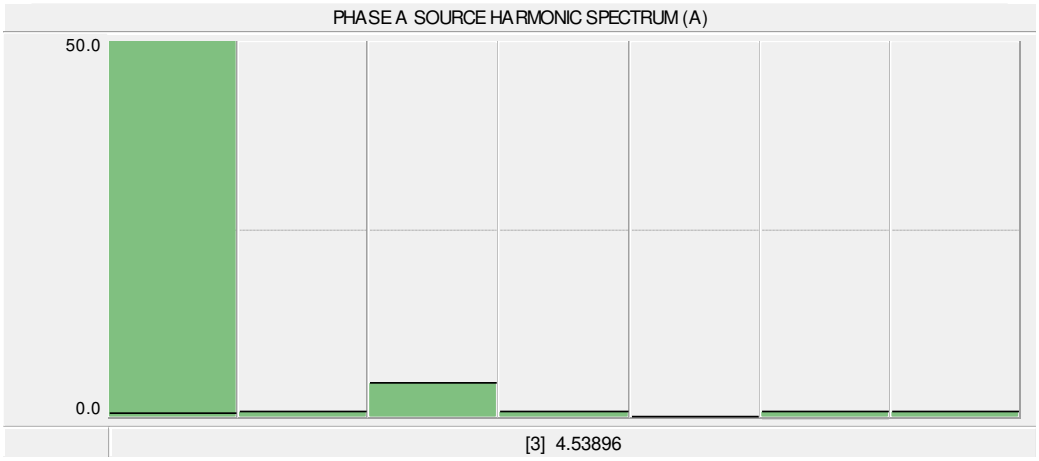

Figure 2.21 Phase A Source Harmonic Current Spectrum

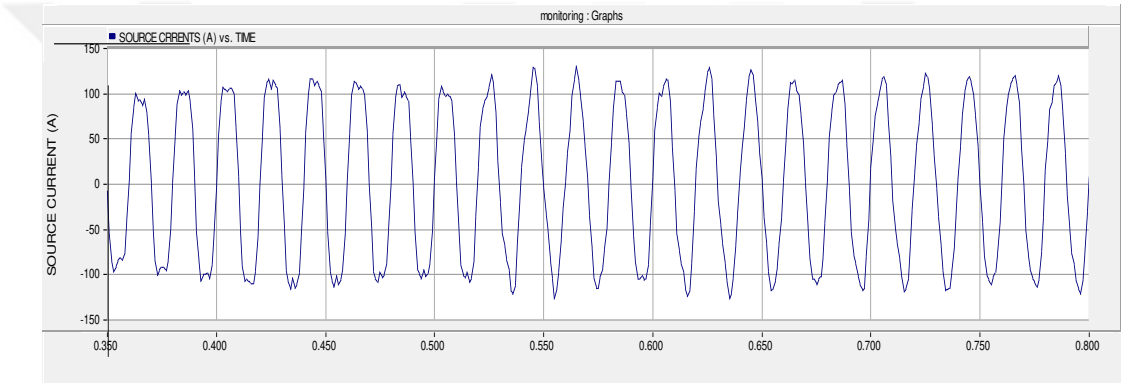

Figure 2.22 Phase A Source Current Waveform

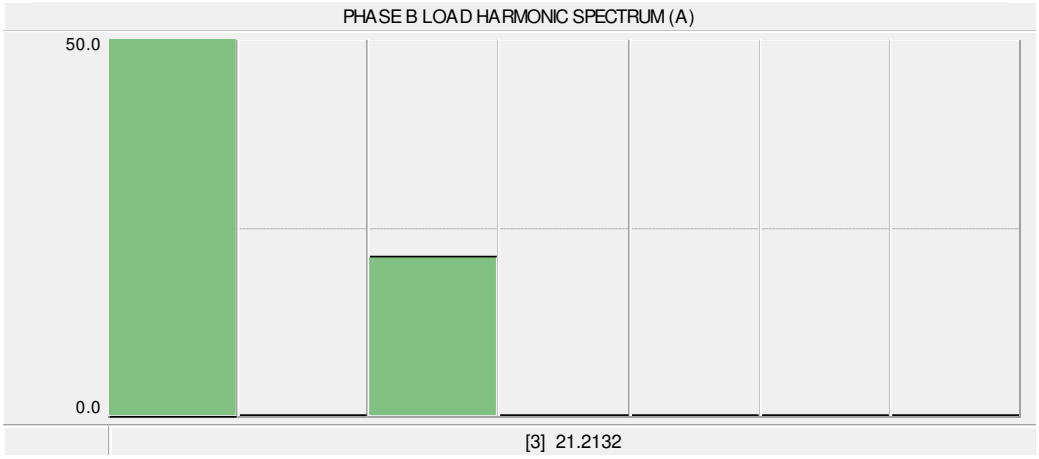

Figure 2.23 Phase B Load Harmonic Current Spectrum

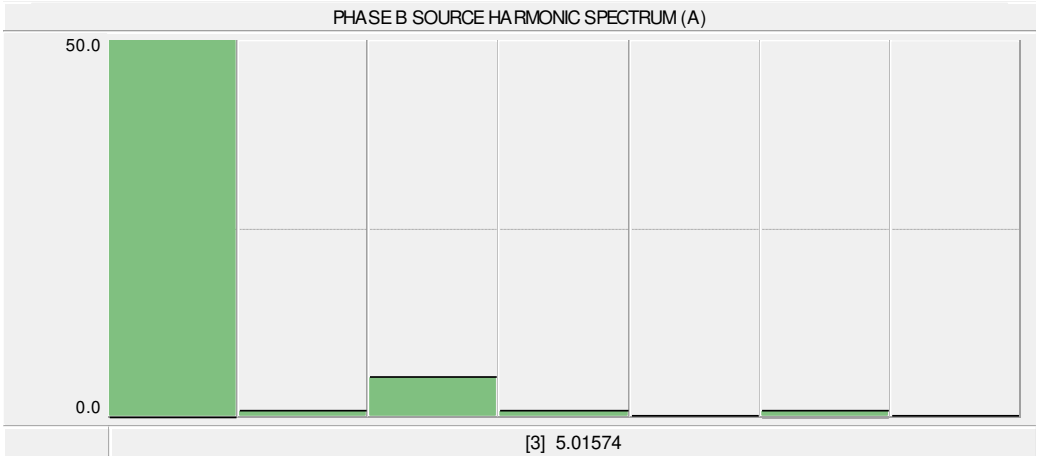

Figure 2.24 Phase B Source Harmonic Current Spectrum

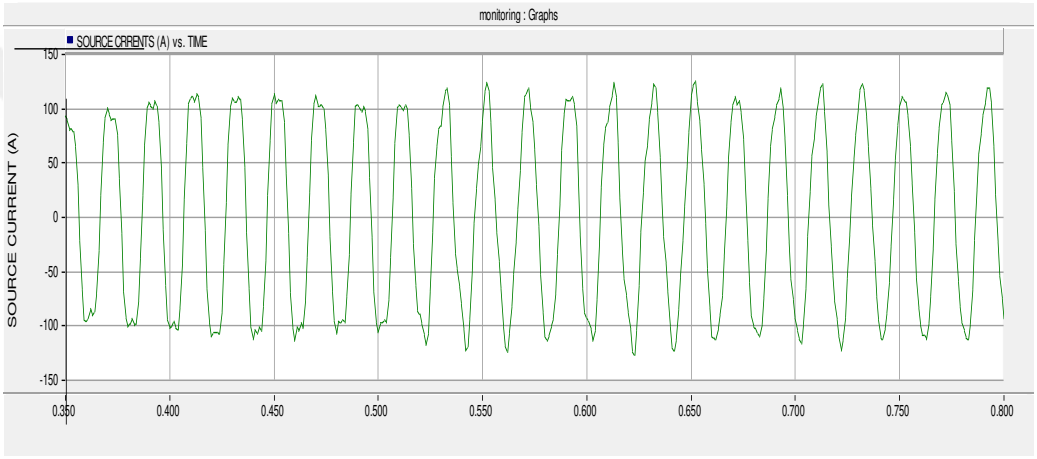

Figure 2.25 Phase B Source Current Waveform

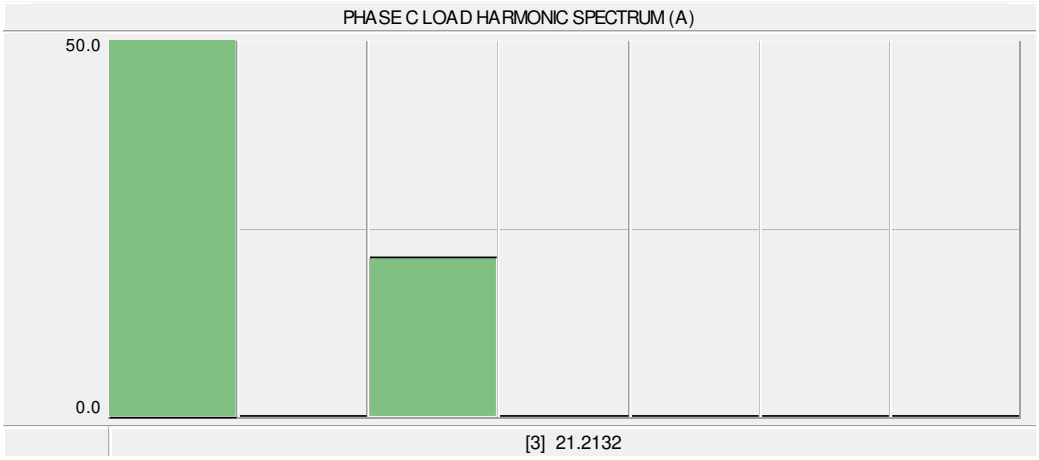

Figure 2.26 Phase C Load Harmonic Current Spectrum

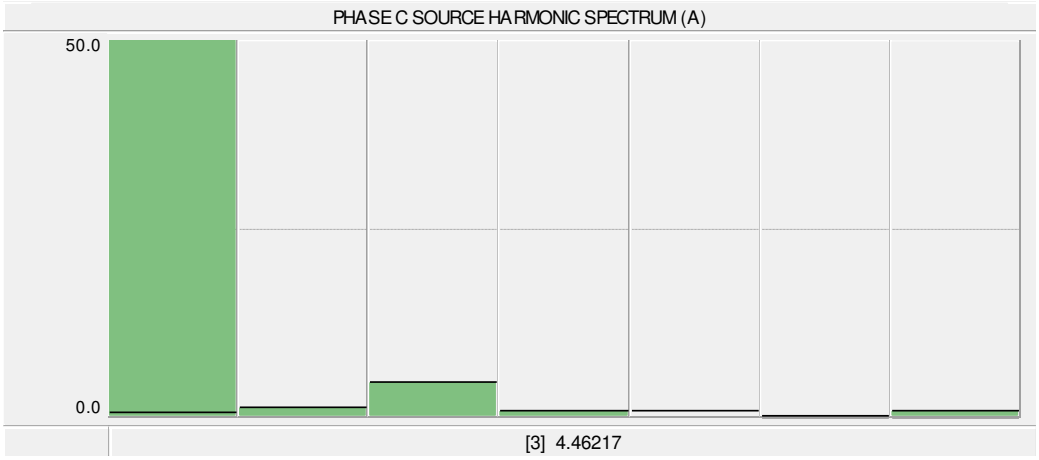

Figure 2.27 Phase C Source Harmonic Current Spectrum

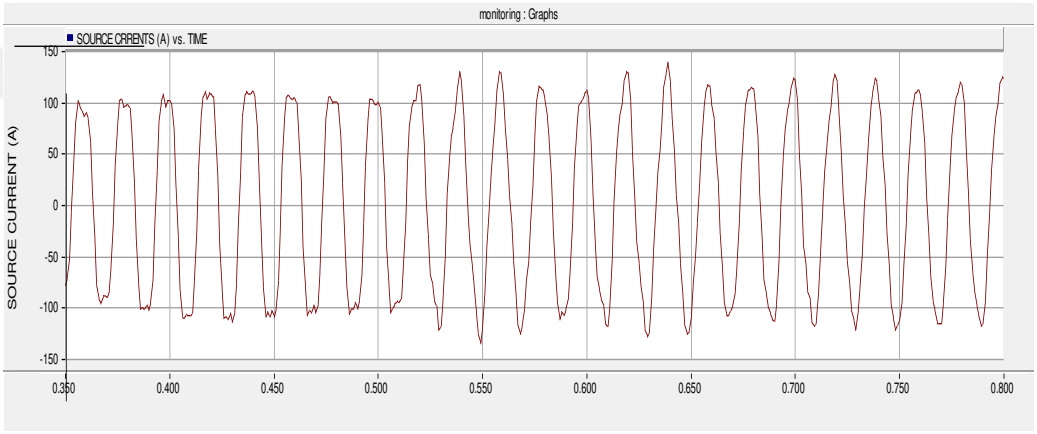

Figure 2.28 Phase C Source Current Waveform

Phase A, B and C are loaded with 21 A third harmonic current to examine third harmonic capability of the EQR device. After the compensation third harmonic current reduces to 4.53 A, 5.01 A and 4.45 A for phase A, B and C respectively. EQR third harmonic compensation is started at 500 ms. of the simulation nearly 50 ms. later compensator regulates the third harmonic current dips as seen in Figure 2.22, Figure 2.25, and Figure 2.28.

2.7 5^{th} Harmonic Currents Compensation Controller

The produced fifth order harmonic current by load canceled out using EQR. EQR is able to inject fifth order harmonic currents for three phases which are in phase with load currents but inverse direction. In the synchronous reference frame which rotates at $2\ x\ \pi\ x\ 250 = \ 1570\ radians/second$ the fifth harmonic appears as DC. Hence, using source current fifth harmonic d and q components as a feedback and zero

reference, fifth harmonic current compensation controller block can compensate fifth harmonic. The 5th harmonic current reference generation and proposed control methods are represented in Figure 2.29. and Figure 2.30. respectively

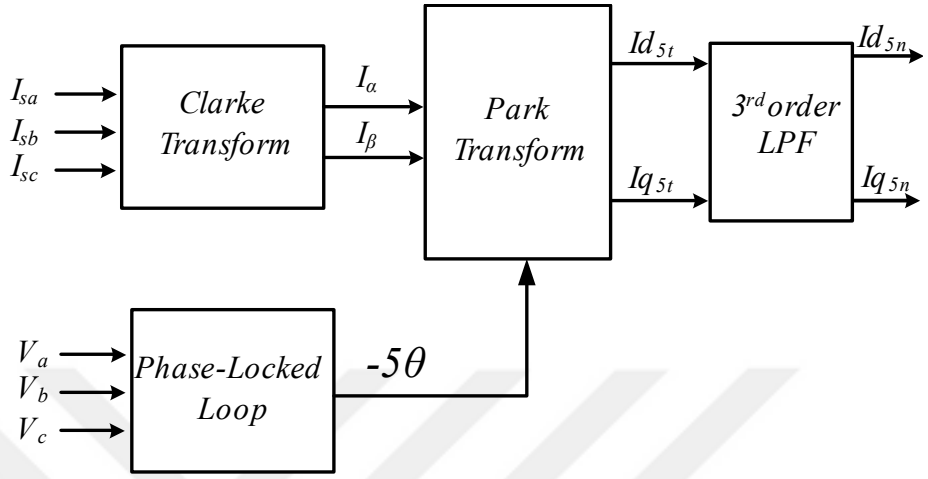

Figure 2.29 5th harmonic current reference generation

To eliminate ripples and obtain purely fifth harmonic reference currents 3rd order 20 Hz low pass filter is used for signals Id_{5t} and Iq_{5t} which are outputs of the park transformation. The output of the filter Id_{5n} and Iq_{5n} are compared reference value. For the ideal case reference values must be zero. The compared signals will be inputs for the PI controller and PI controller will produce reference voltages Vd_{5n} and Vq_{5n}. As seen in Figure 2.30. to obtain reference voltages in the a-b-c frame the output of the controller must pass through Inverse-Park transform block and Inverse-Clarke transform block.

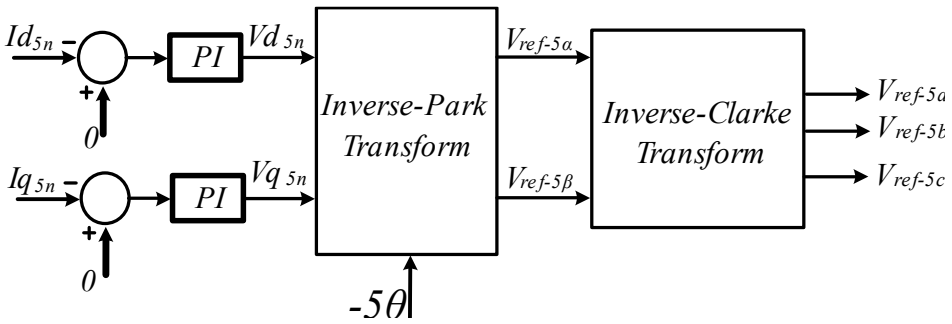

Figure 2.30 5th harmonic reference voltage generation

This control block is also called multiple synchronous reference frame-based control [24]. According to this control method, feedback controller is utilized with the feedback loops to eliminate individual harmonics using conventional PI controller.

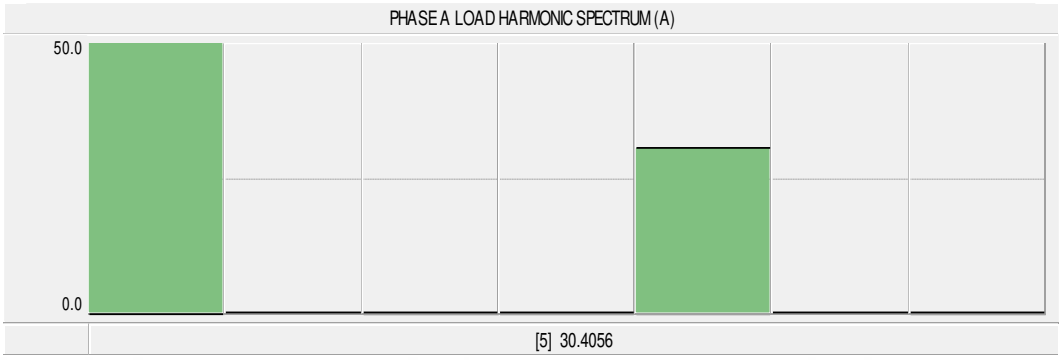

Figure 2.31 Phase A Load Harmonic Current Spectrum

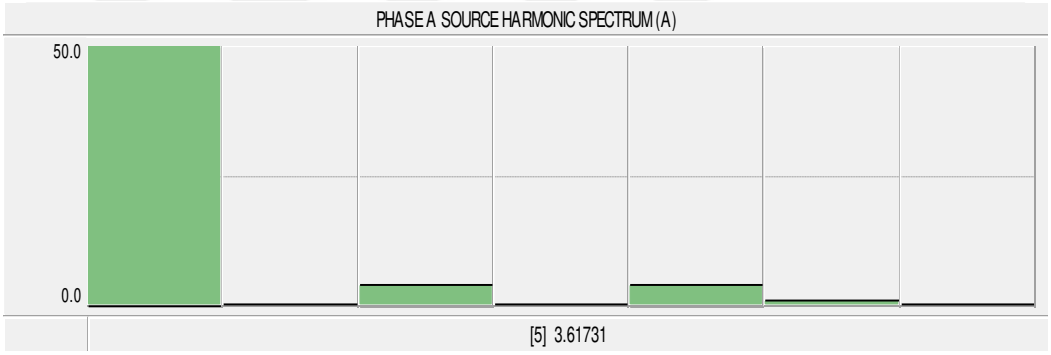

Figure 2.32 Phase A Source Harmonic Current Spectrum

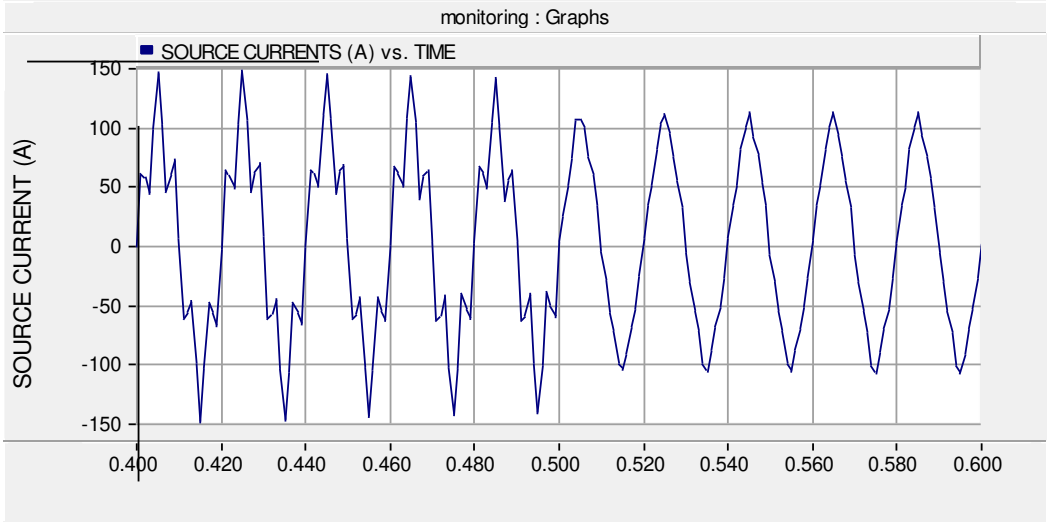

Figure 2.33 Phase A Source Current Waveform

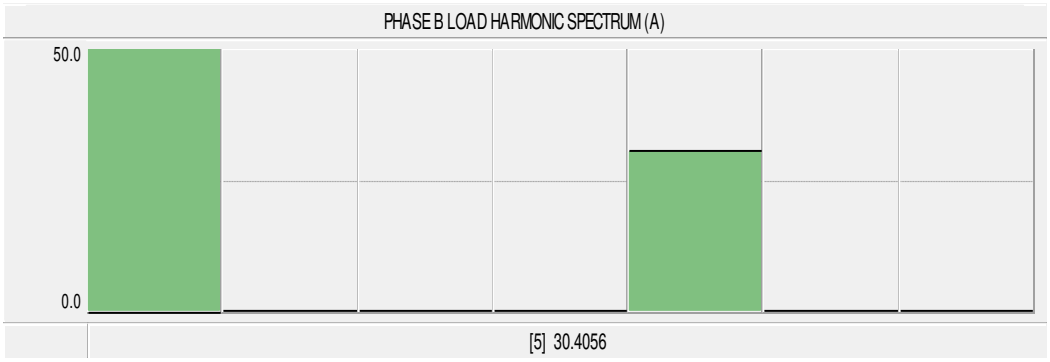

Figure 2.34 Phase B Load Harmonic Current Spectrum

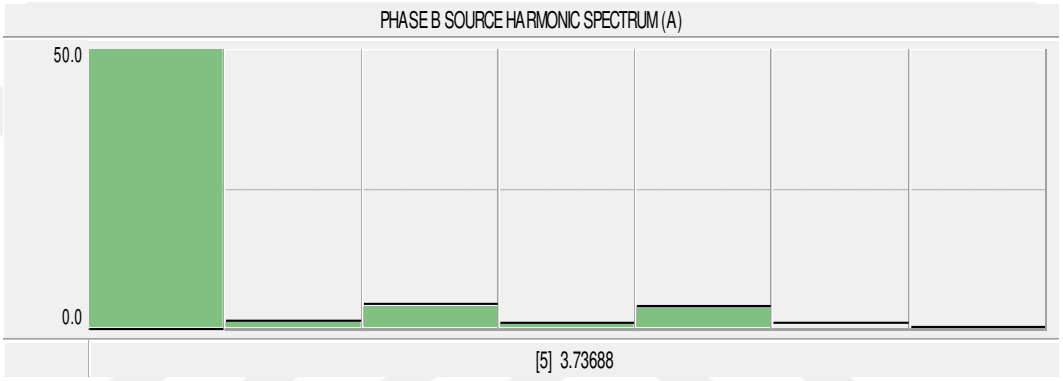

Figure 2.35 Phase B Source Harmonic Current Spectrum

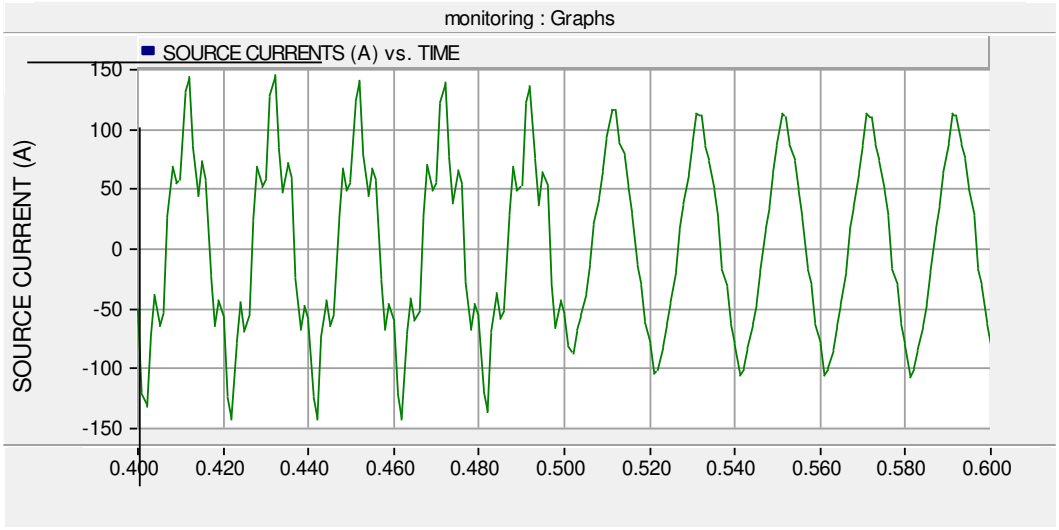

Figure 2.36 Phase B Source Current Waveform

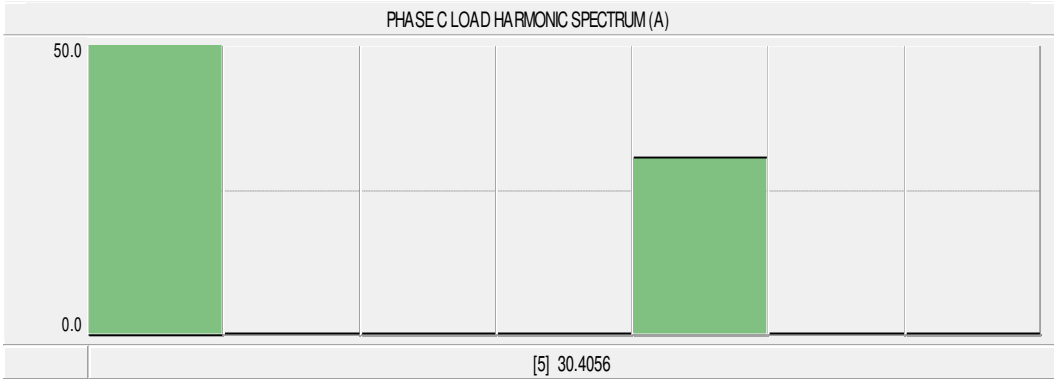

Figure 2.37 Phase C Load Harmonic Current Spectrum

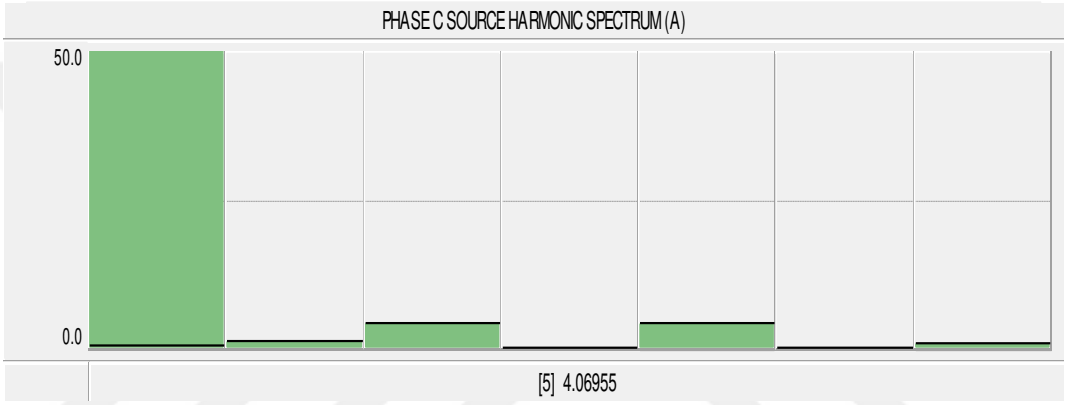

Figure 2.38 Phase A Source Harmonic Current Spectrum

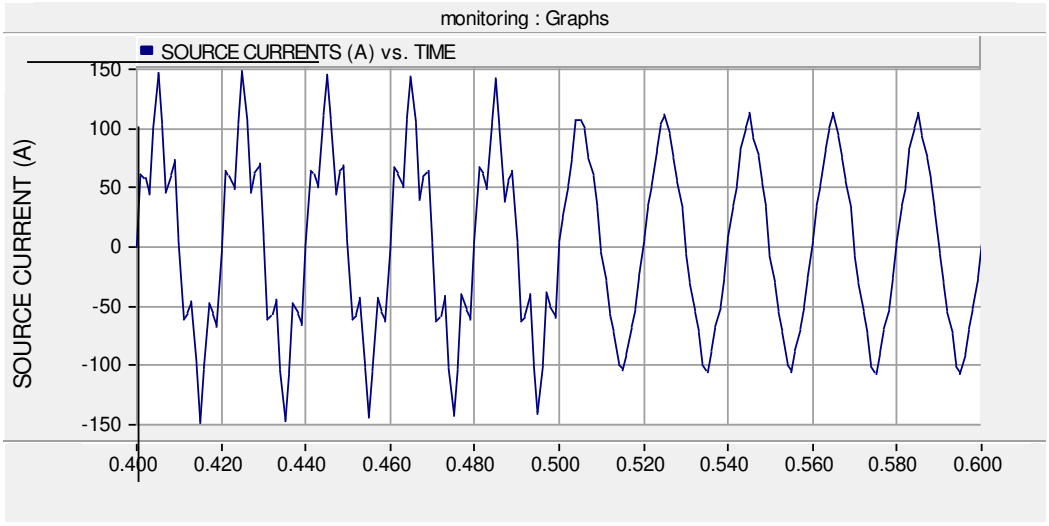

Figure 2.39 Phase C Source Current Waveform

Phase A, B and C are loaded with 30 A fifth harmonic current as an extreme case to examine fifth harmonic capability of the EQR device. After the compensation fifth harmonic current reduces to 3.61 A, 3.73 A and 4.06 A for phase A, B and C respectively. EQR third harmonic compensation is started at 500 ms. of the simulation nearly 40 ms. later compensator regulates the fifth harmonic current distortion as seen in Figure 2.33, Figure 2.36, and Figure 2.39.

2.8 7th Harmonic Current Compensation Controller

As seen in Figure 2.40. seventh harmonic current reference can be extracted in multiple synchronous reference frame like fifth harmonic. 3rd order 20 Hz LPF is used again to prevent ripples. Both fifth harmonic and seventh harmonic occurs at 300 Hz in the reference frame so LPF can be characterized up to this level. Due to simplicity, reliability and applicability PI controller is used again to control seventh harmonic as seen in Figure 2.41.

Seventh harmonic reference voltages are obtained using Inverse-Park transform and Inverse-Clarke transform blocks. These reference voltages will be inputs for the modulator block.

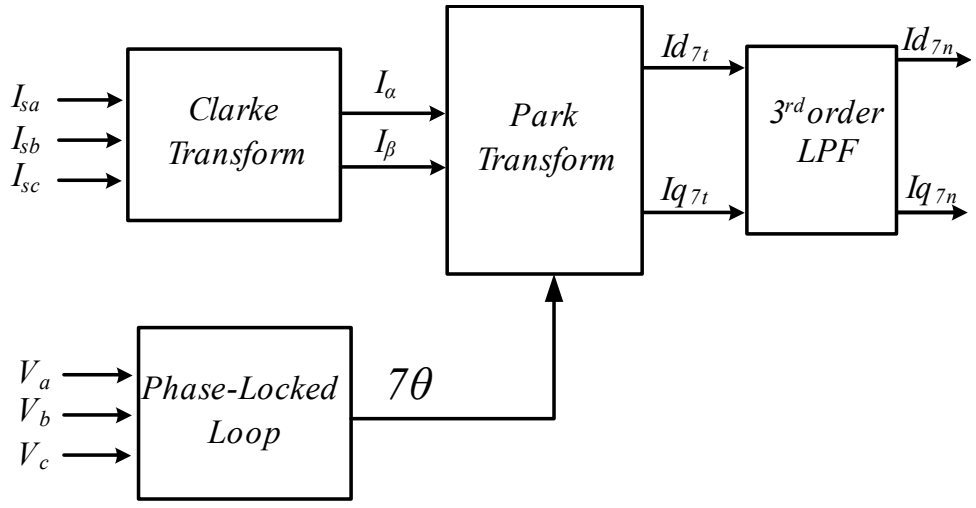

Figure 2.40 7th harmonic current reference generation

Seventh harmonic reference voltages V_{ref-7a}, V_{ref-7b} and V_{ref-7c} can be summed with fifth harmonic reference voltages V_{ref-5a}, V_{ref-5b} and V_{ref-5c} respectively since plant is linear and superposition law is valid.

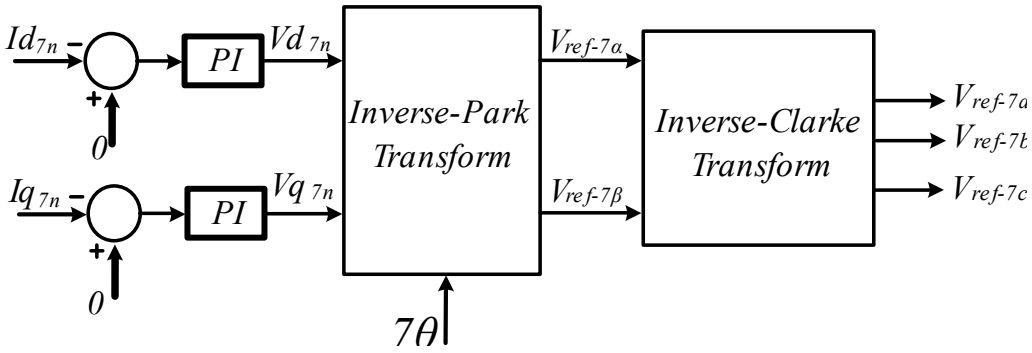

Figure 2.41 7th harmonic reference voltage generation

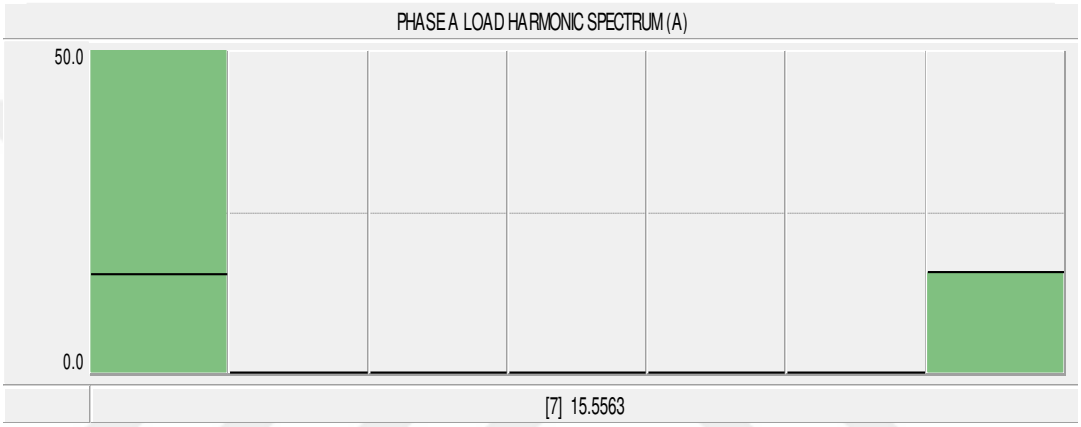

Figure 2.42 Phase A Load Harmonic Current Spectrum

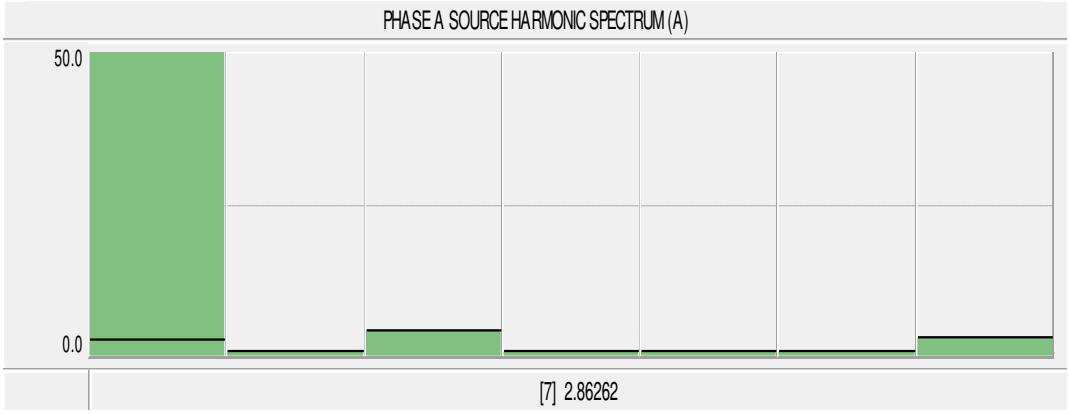

Figure 2.43 Phase A Source Harmonic Current Spectrum

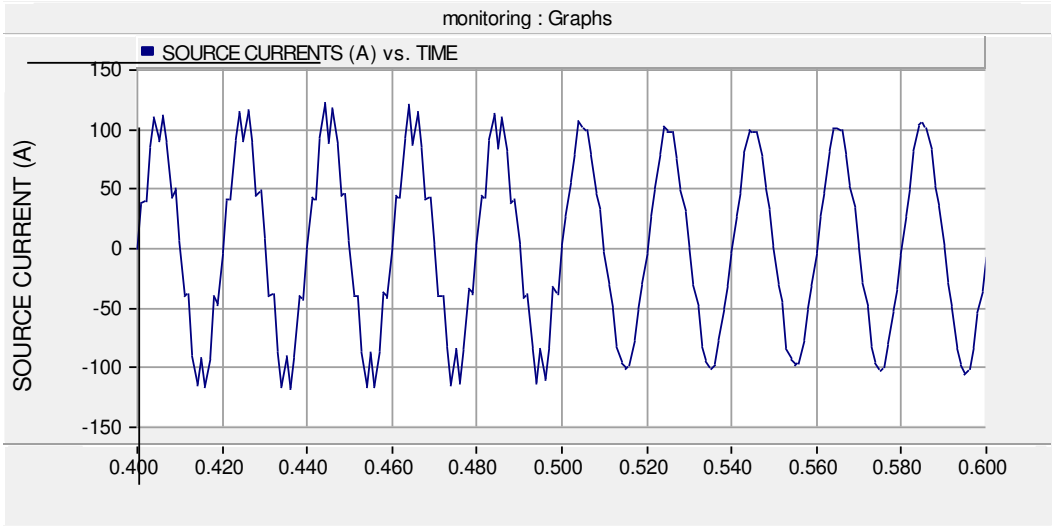

Figure 2.44 Phase A Source Current Waveform

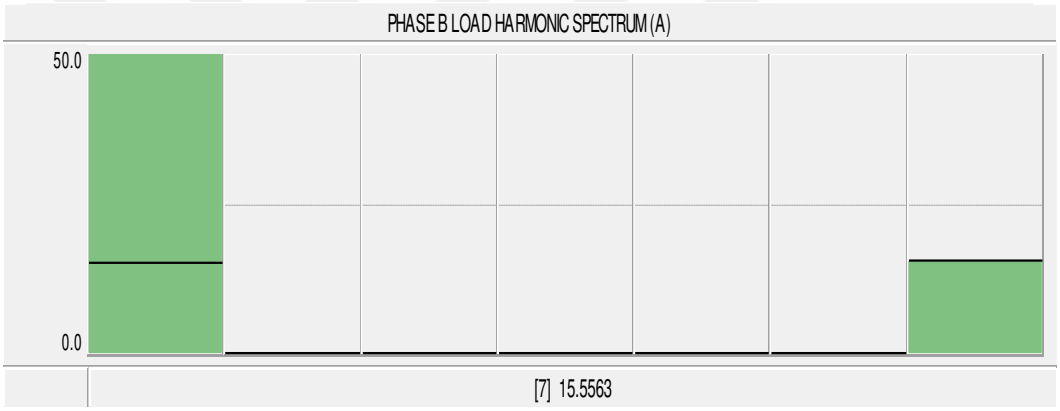

Figure 2.45 Phase B Load Harmonic Current Spectrum

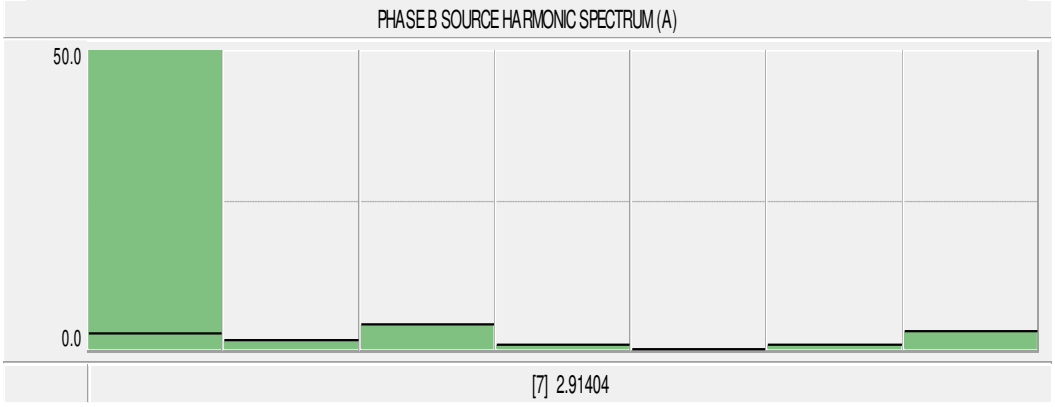

Figure 2.46 Phase B Source Harmonic Current Spectrum

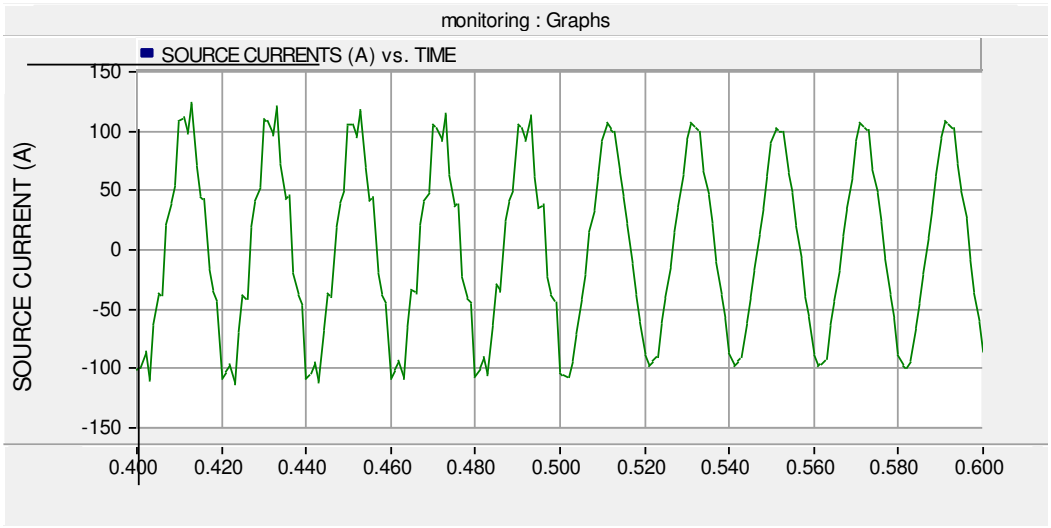

Figure 2.47 Phase B Source Current Waveform

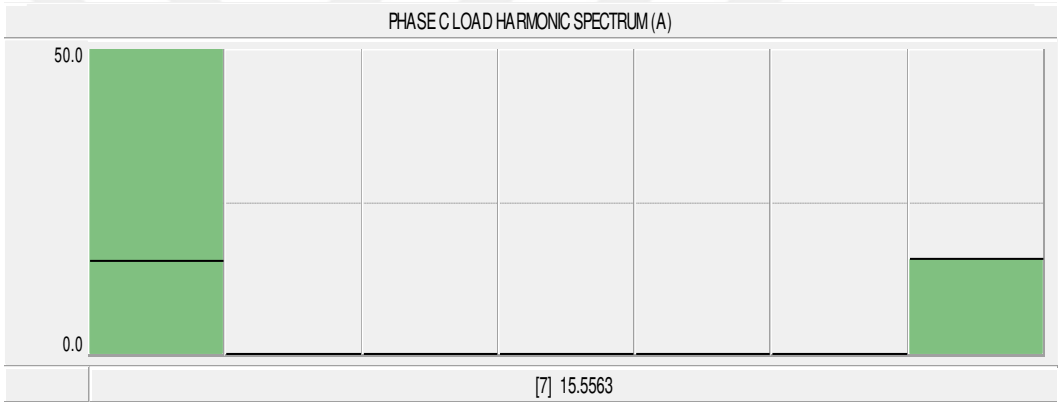

Figure 2.48 Phase C Load Harmonic Current Spectrum

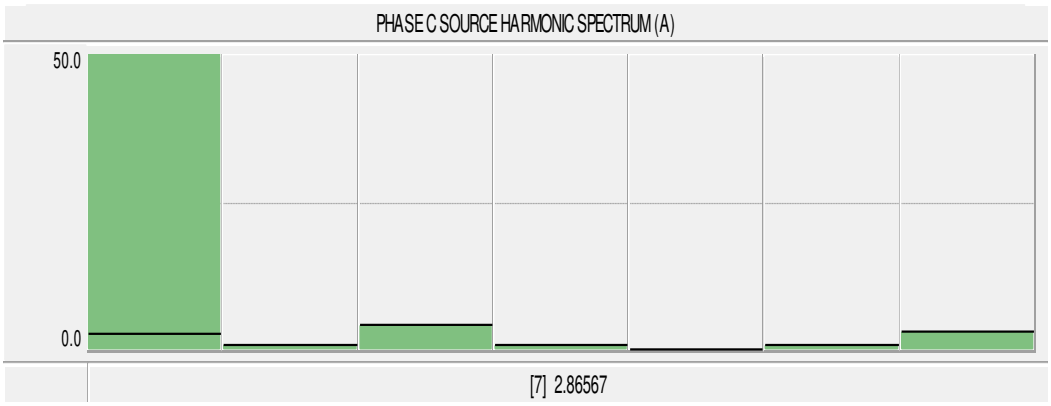

Figure 2.49 Phase C Source Harmonic Current Spectrum

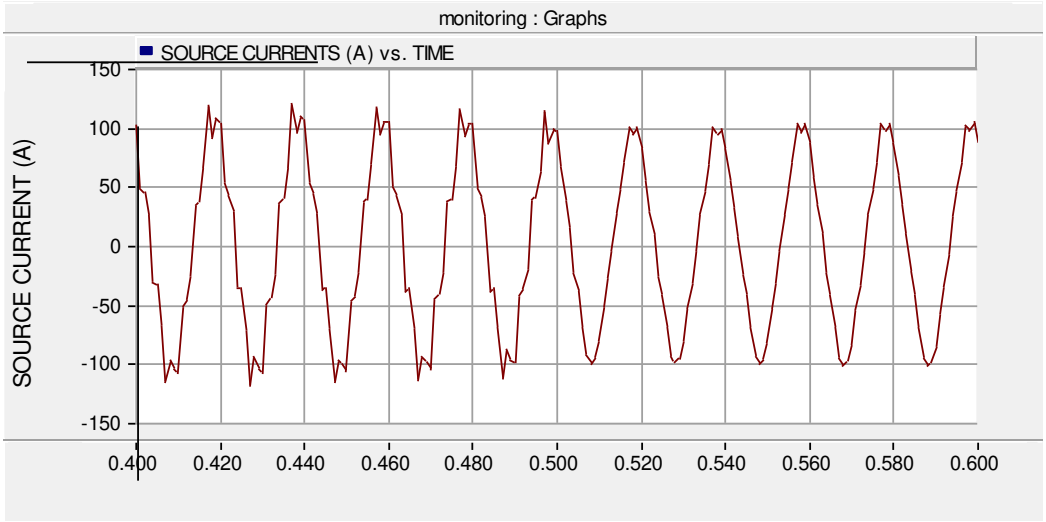

Figure 2.50 Phase C Source Current Waveform

Phase A, B and C are loaded with 15 A fifth harmonic current as an extreme case to examine seventh harmonic capability of the EQR device. After the compensation seventh harmonic current reduces to 2.86 A, 2.91 A and 2.86 A for phase A, B and C respectively. EQR third harmonic compensation is started at 500 ms. of the simulation nearly 40 ms. later compensator regulates the seventh harmonic current distortion as seen in Figure 2.44, Figure 2.47, and Figure 2.50.

2.9 Current Unbalance Compensation Controller

There are several factors which may cause unbalance. These can be sorted as single-phase distributed generation, asymmetric fault, open conductors, untransposed lines and single-phase loads [25]. In this thesis current unbalance due to the single-phase loads has mentioned which are the most commonly reason for current unbalance. In an unbalanced operation not only, positive sequence current components are occurred, but also negative sequence and zero sequence vector components are occurred as seen in Figure 2.51.

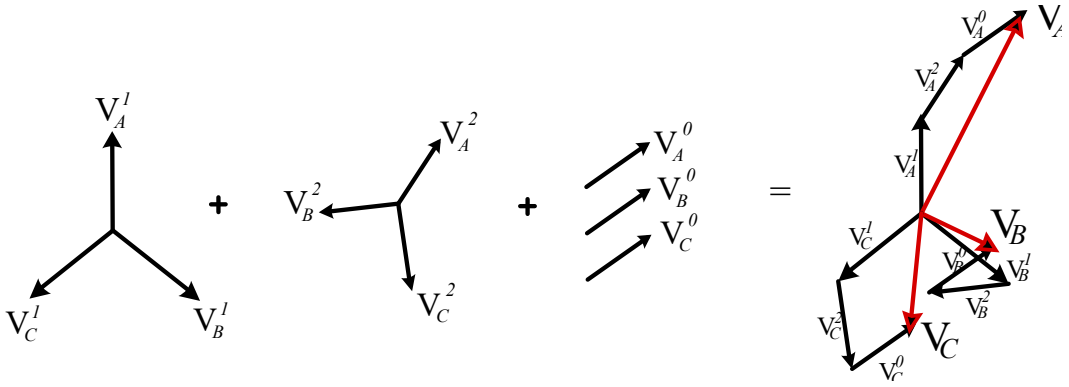

Figure 2.51 Symmetrical component of unbalanced vector

Negative and zero sequence components can be easily found by using vector a = $e^{j\frac{2}{3}\pi}$ also known as Fortescue's Theorem [50]. However, in this thesis negative sequence components in the system are extracted by using Double Synchronous Reference Frame Theory (DSRF). This theorem basics are explained in section 2.3.2.2.2.

In this reference frame negative sequence components occurs at 100 Hz and 3rd order 10 Hz filter can be used to extract negative sequence components (Id_{un} and Iq_{un}) as seen in Figure 2.52.

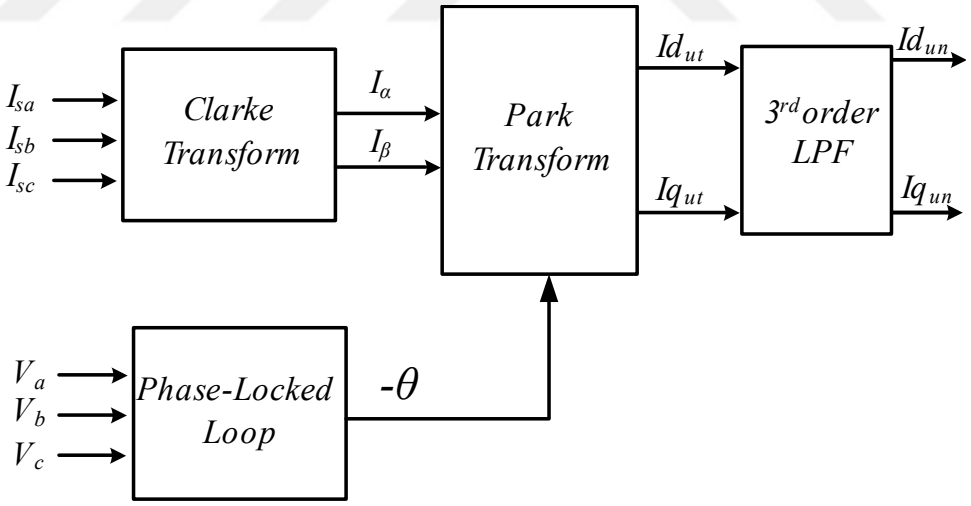

Figure 2.52 Unbalanced current reference generation

To suppress negative sequence current at the PCC, PI controller is used. Id_{un} and Iq_{un} are compared with reference values which must be zero to suppress negative sequence currents. Compared values are inputs for the PI controller to control unbalanced current at the PCC. The output of the PI controller is stated as voltage magnitude since the current inputs are multiply by scalar numbers. These outputs Vd_{un} and Vq_{un} are

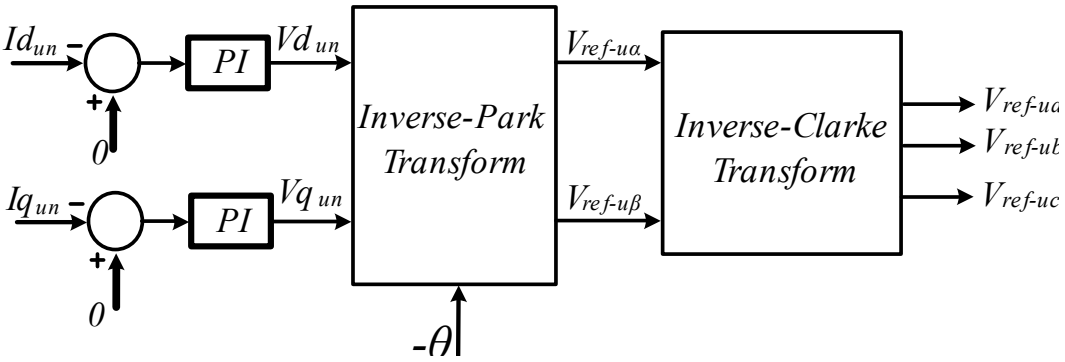

Figure 2.53 Unbalanced current reference voltage generation

also called as negative sequence reference voltages and these are inputs for the inverse transform blocks to obtain 3-phases voltage magnitude in ABC frame as seen in Figure 2.53.

Unbalanced current compensation capability of the EQR is analyzed for three cases. These are extremely unbalanced case, over unbalanced case and normal unbalanced case. Figure 2.54 shows extremely unbalanced case that is an abnormal situation since one of the phases extremely overloaded and the other phases magnitudes far away from this value. To measure EQR performance in this case is created in the PSCAD/EMTDC software.

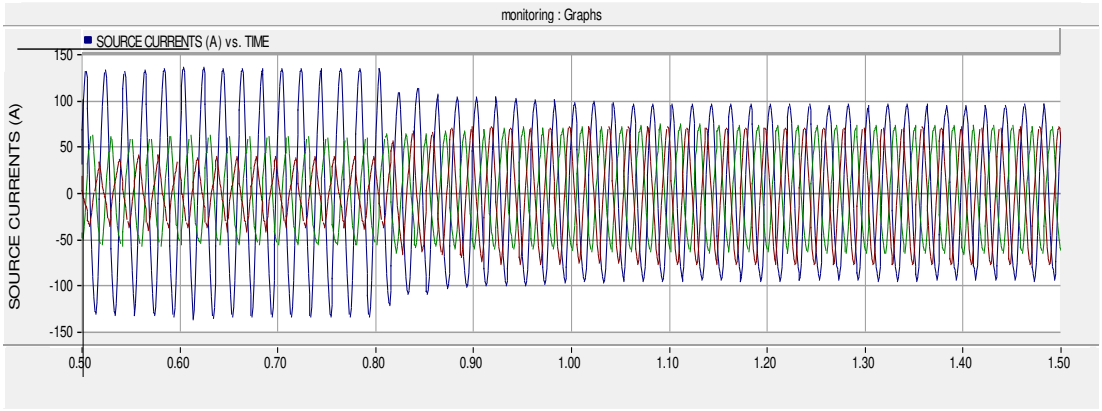

Figure 2.54 Unbalance Current Compensation for Extremely Unbalanced Case

According to the PSCAD/EMTDC analysis phase A, B and C currents have 140 A, 55 A and 30 A peak values. These currents are nearly balanced after compensation at the 800 ms. of the simulation. According to the Figure 2.54. new compensated source currents peak values have become 95 A, 60 A and 60 A for phase A, B and C

respectively.

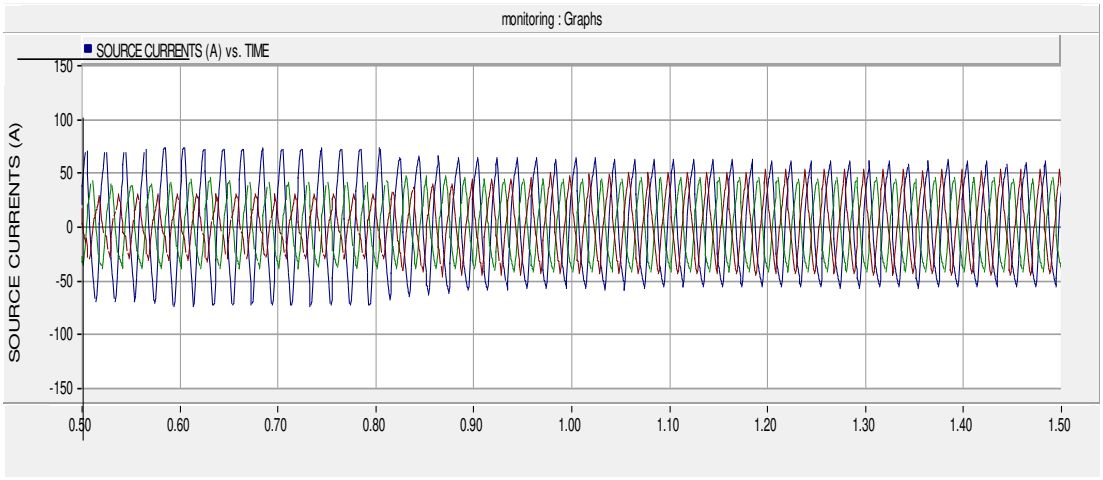

Figure 2.55 Unbalance Current Compensation for Over Unbalanced Case

Unbalanced currents are given in Figure 2.55. have a 60 A, 45 A and 30 A peak values it can be named as over unbalanced case and with the compensation these values are balanced at the 53 A, 50 A and 48 A.

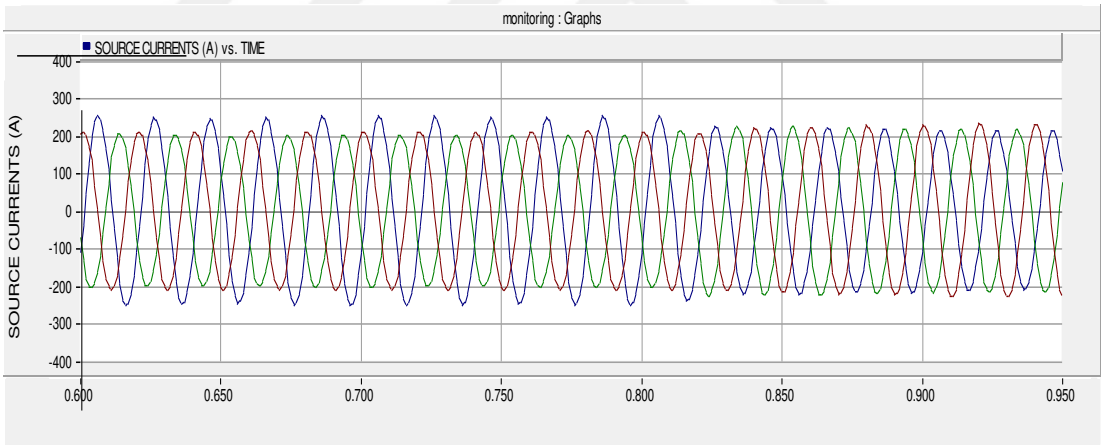

Figure 2.56 Unbalance Current Compensation for Normal Unbalanced Case

As seen in Figure 2.56. the currents are guaranteed to be balanced with given unbalanced compensation strategy. The scenario given in in Figure 2.56 is a normal unbalanced case and it can be observed every distribution type transformer. Nearly 230 A, 205 A and 210 A peak values are balanced after compensation at the 215 A peak value.

2.10 Neutral Current Compensation Controller

In three-phase four-wire distribution system zero sequence currents flow through the neutral wire. Therefore, to achieve neutral current compensation zero-sequence current components in the system must be separated and suppressed. Zero sequence currents are composed of third harmonic with multiply of third harmonic and zero sequence currents due to unbalance operation. Since third harmonic compensation technique is discussed in **2.6.** in this section only zero sequence compensation technique will describe. In the three-phases four-wire system zero sequence current components can be represented using directly from zero component of the Clarke Transformation by (2.8).

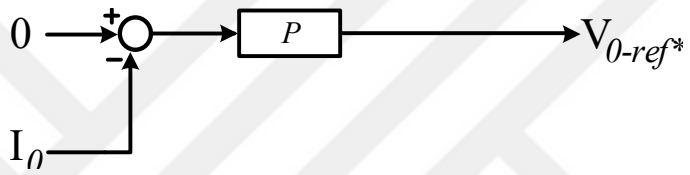

Figure 2.57 Zero sequence current control block

Zero sequence current component of the system is feedback signal for this closed loop control system to compare reference value. To suppress zero sequence currents from the system completely, reference value must be zero. Zero sequence current is controlled using only P controller since it is enough for suppression. The block diagram of the zero-sequence current control block is given in Figure 2.57 to obtain V_{0-ref}^{*}.

Neutral current compensation capability of the EQR is analyzed in PSCAD/EMTDC environment with third harmonic current compensation and without third harmonic compensation since third harmonic also passes through neutral wire.

As seen in Figure 2.58 neutral current has 60 A peak value and this value is reduced to 40 A peak value using only zero sequence control block given in Figure 2.57. However, using third harmonic compensation block this value is reduced to nearly 25 A as seen in Figure 2.59.

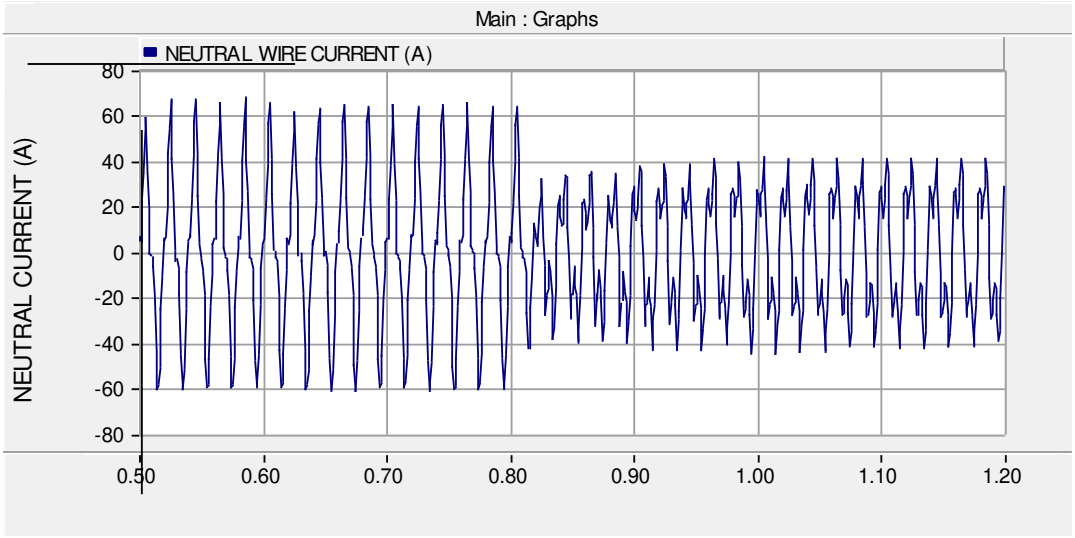

Figure 2.58 Neutral Current Compensation without Third Harmonic Compensation

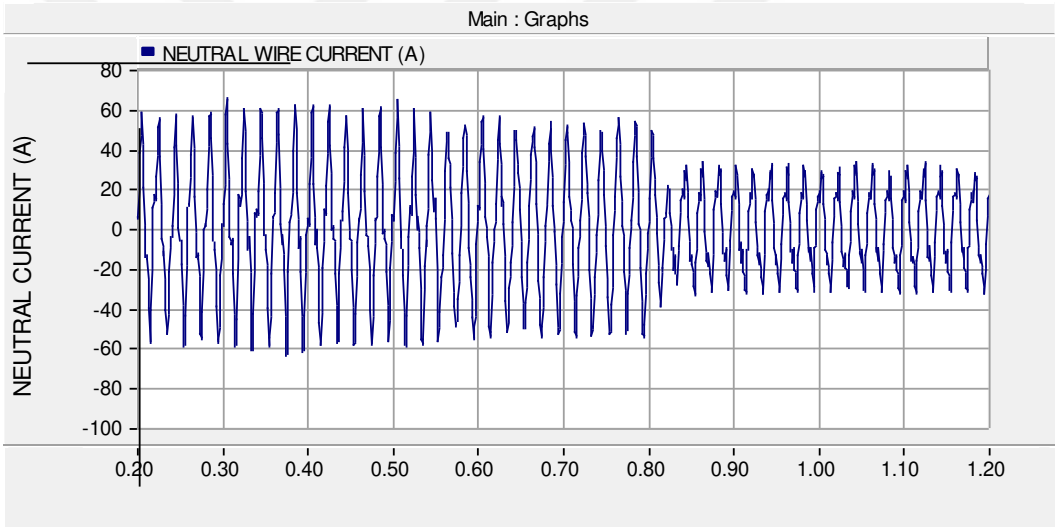

Figure 2.59 Neutral Current Compensation with Third Harmonic Compensation

2.11 Modulation Techniques

Modulation is the most important part of the control system and it is directly affecting the compensation performance. PWM (Pulse Width Modulation) technique is the most common and reliable way to create needed output voltage wave shape [51]. To obtain reliable signal, switching frequency must be much greater than intended output frequency. PWM methods can be categorized as open loop and closed loop modulation techniques [22].

2.11.1 Open-Loop PWM Techniques

2.11.1.1 Sinusoidal Pulse Width Modulation (SPWM)

In this method reference sinusoidal signal is compared with a high frequency triangular 'carrier' wave shape to produce desired reference waveform (modulating signal) as depicted in Figure 2.60.

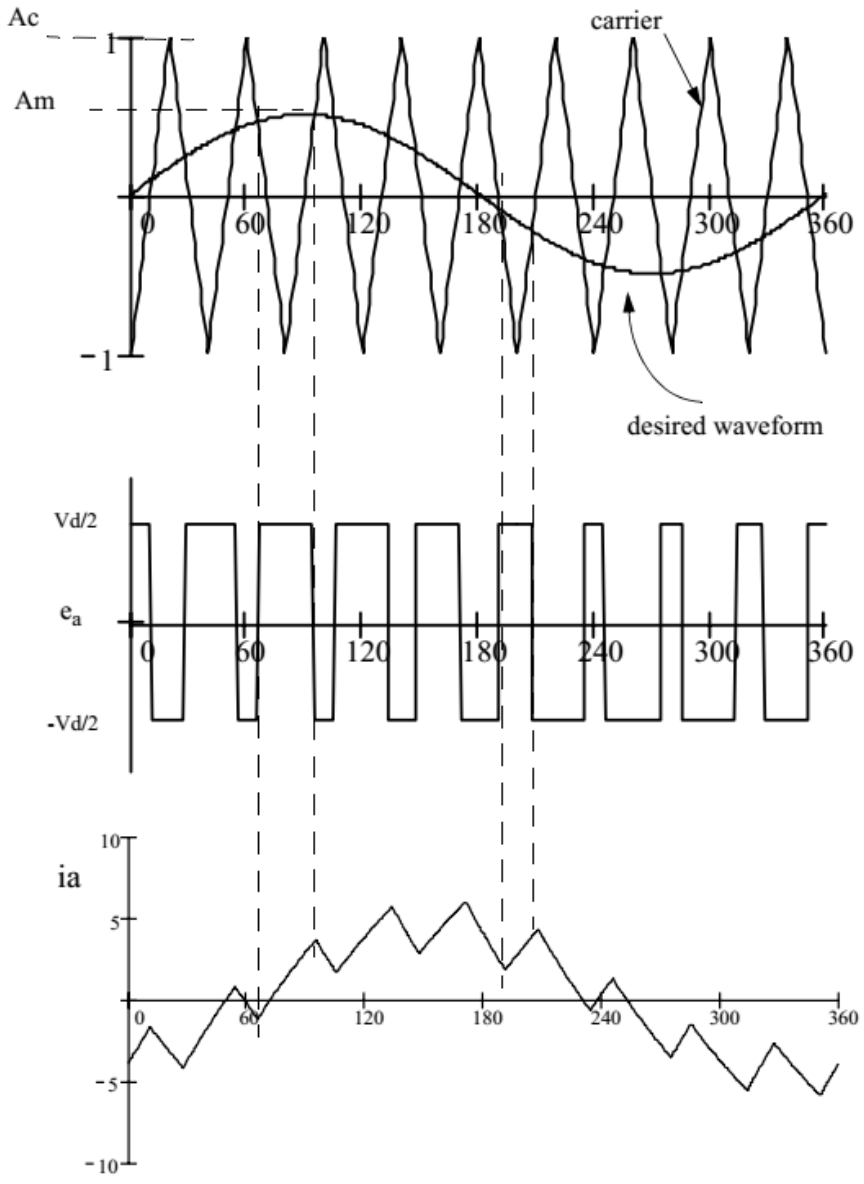

Figure 2.60 Principal of SPWM [52]

Both the positive or negative DC bus voltage is applied to output according to whether the reference voltage signal or desired waveform is larger or smaller than carrier

waveform. During this switching period, average voltage applied to the load is proportional to the amplitude of the signal. Amplitude of the signal mean is duration state (high or low level) of the square wave which is obtain from comparation between reference voltage and carrier. This square wave contains replica of the reference voltage so with the elimination of high frequency component from this wave desired waveform can be obtain. With a high carrier frequency, in the AC network high frequency component will be decrease. However, high switching frequency means high power loss so in power system application 2-15 kHz carrier frequency carry out adequate performance [52].

If A_m is the amplitude of the sinusoid modulating signal, A_c is the amplitude of carrier signal than modulation index 'm' can be represented as (2.38), and the amplitude of the output voltage can adjust controlling modulation index 'm'.

$$m = \frac{Am}{Ac} \tag{2.38}$$

Modulation index can be lower, equal or greater than 1. Modulation index greater than 1 means "overmodulation" and it is used when larger AC output voltage is needed but if modulation index much greater than 1 there will be no intersection between carrier and reference voltage signal and modulation performance will be close to zero so in practical application modulation index is often used lower than 1.

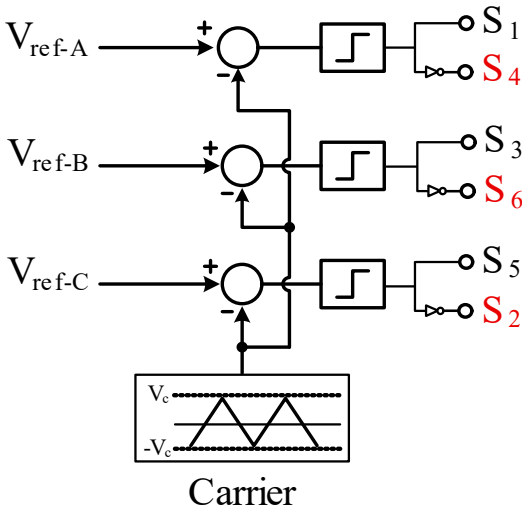

Figure 2.61 Application scheme of SPWM

The general application scheme of SPWM technique is depicted in in Figure 2.61 and using this method produced maximum phase voltage is given in (2.39).

$$V_{RMS} = m\frac{V_{DC}}{2\sqrt{2}} \tag{2.39}$$

As seen in from (2.38) output voltage is directly related with modulation index. To prevent harmonic effect and gain maximum modulation performance, modulation index must be closed to 1. However, in this case produced voltage peak value is lower and DC-link voltage cannot be utilized its total performance so to gain high performance using SPWM method, third harmonic is injected to the modulated signal but this method only valid three-phase three-wire systems. This method doesn't applicable for three-phase four-wire systems since zero-sequence third harmonic currents flows through neutral wire [33].

2.11.1.2 Space Vector Pulse Width Modulation (SVPWM)

Space Vector Pulse Width Modulation (SVPWM) technique has become more popular in recent years since it has higher utilization rate of DC voltage and smaller output waveform distortion unlike SPWM method [53]. This method is applicable for both 3-phase 3-wire systems and 3-phase 4-wire VSI systems. However, application methods are different from each other. In this thesis SVPWM is discussed for 3-phase 4-wire system. In this method, reference signals in abc coordinate system are transformed to normalized vectors in αβ0 coordinates using transformation matrix given in (2.40).

$$T_{abc-\alpha\beta 0} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.40}$$

Using neutral point clamped 3-phase 4-wire topology different inverter output voltages can be produced at different phases angle and different magnitudes for each phase. This topology has eight different switching states vectors. This switching vectors and

normalized output voltages vectors according to these switching states in ABC and αβ0 coordinates are given in Table 2.1. The output vectors in αβ0 frame due to the switching states are depicted in Figure 2.62. As a difference from 3-phase 3-wire topology in this topology zero sequence output voltages can be produced thanks to the neutral wire. Due to this reason vectors formed in switching states have three dimensional components as seen in Figure 2.63.

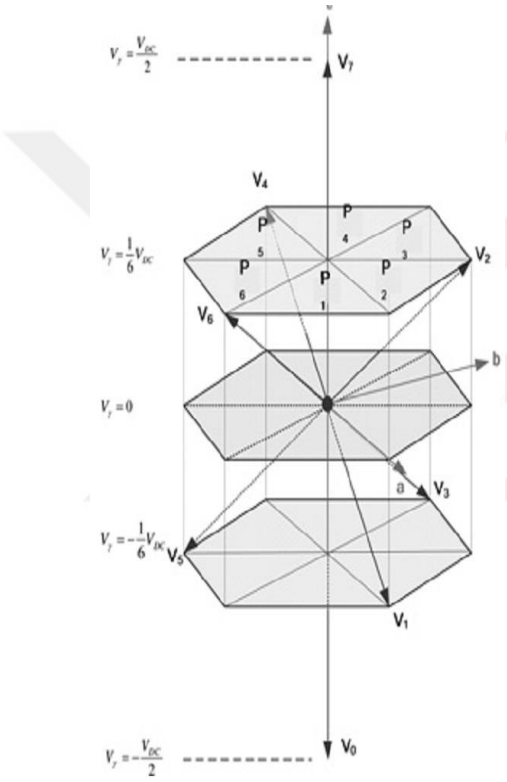

Figure 2.62 Three-Dimensional Space Vectors

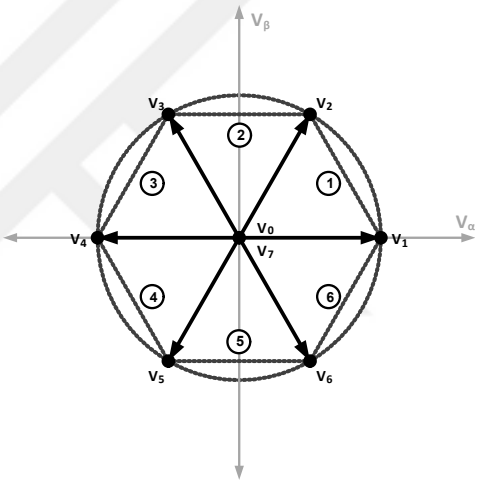

Figure 2.63 αβ Axes Top View

There are six different stages between space vectors which are called as sectors. Mainly SVPWM is applied using three basic steps.

Step 1: Reference voltages in abc frame is transformed into normalized space vectors in αβ0 frame and according to the projection of αβ frame rotating angle θ is detected. To find normalized space vectors and rotating angle below formulas are used to complete Step 1.

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \tag{2.41}$$

Table 2.1 Switching States & Normalized Output Voltages

Vectors	Switching States			Normalized Output Line – Neutral Voltages			Normalized Output Line - Line Voltages			Normalized αβ0 Voltages		
	S1	S3	S5	VA/VDC	VB/VDC	VC/VDC	VAB/VDC	VBC/VDC	VCA/VDC	Vα/VDC	Vβ/VDC	V0/VDC
V0	0	0	0	-1/2	-1/2	-1/2	0	0	0	0	0	-1/2
V1	1	0	0	1/2	-1/2	-1/2	1	0	-1	$2/3$	0	-1/6
V2	1	1	0	1/2	1/2	-1/2	0	1	-1	$1/3$	$1/\sqrt{3}$	1/6
V3	0	1	0	-1/2	1/2	-1/2	-1	1	0	$-1/3$	$1/\sqrt{3}$	-1/6
V4	0	1	1	-1/2	1/2	1/2	-1	0	1	$-2/3$	0	1/6
V5	0	0	1	-1/2	-1/2	1/2	0	-1	1	$-1/3$	$-1/\sqrt{3}$	-1/6
V6	1	0	1	1/2	-1/2	1/2	1	-1	0	$1/3$	$-1/\sqrt{3}$	1/6
V7	1	1	1	1/2	1/2	1/2	0	0	0	0	0	1/2

$$|V_{ref}| = \sqrt{V_\alpha^2 + V_\beta^2 + V_0^2} \tag{2.42}$$

$$\theta = tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \tag{2.43}$$

$$V_{ref,norm} = \frac{|V_{ref}|}{V_{dc}} \quad V_{\alpha,norm} = \frac{|V_\alpha|}{V_{dc}} \quad V_{\beta,norm} = \frac{|V_\beta|}{V_{dc}} \quad V_{0,norm} = \frac{|V_0|}{V_{dc}} \tag{2.44}$$

Step 2: Reference vector stage is defined and to form reference voltages timing interval is determined.

Reference vector sector selection:

$0° \leq \theta < 60°$ → Sector 1

$60° \leq \theta < 120°$ → Sector 2

$120° \leq \theta < 180°$ → Sector 3

$180° \leq \theta < 240°$ → Sector 4

$240° \leq \theta < 300°$ → Sector 5

$300° \leq \theta < 360°$ → Sector 6

Calculation of application times of vectors in switching states are given in Appendix B.

Step 3: Switching is performed according to the order of application of the vectors in the switching states.

Application Sequence of Vectors in Switching States:

Application sequence and form of vectors are directly affecting the output voltage and switching frequency. In this thesis symmetric switching method is tried to explain. The application sequence of these vectors are given in Table 2.2. In this method, the deterioration of output voltage is the minimum level.

Table 2.2 Application Sequence of Vectors

Sector 1	V_0 - V_1 - V_2 - V_7 - V_7 - V_2 - V_1 - V_0
Sector 2	V_0 - V_3 - V_2 - V_7 - V_7 - V_2 - V_3 - V_0
Sector 3	V_0 - V_3 - V_4 - V_7 - V_7 - V_4 - V_3 - V_0
Sector 4	V_0 - V_5 - V_4 - V_7 - V_7 - V_4 - V_5 - V_0
Sector 5	V_0 - V_5 - V_6 - V_7 - V_7 - V_6 - V_5 - V_0
Sector 6	V_0 - V_1 - V_6 - V_7 - V_7 - V_6 - V_1 - V_0

2.11.2 Closed-Loop PWM Techniques

2.11.2.1 Hysteresis Band PWM (HB Controller)

The principle scheme of Hysteresis Band Current Control (HB control) is shown in Figure 2.64. To control output current of the inverter reference currents i_{cx}^{*} are compared with output currents i_{cx}. Obtained error signals are applied to hysteresis controller and switching signals are generated.

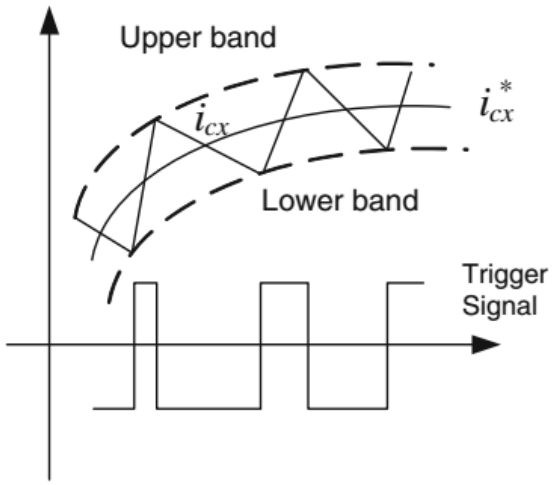

Figure 2.64 Principle Scheme of HB Control [19]

The hysteresis controller of each phase determines the current error of that phase to produce a switching signal to hold it in a tolerance band. In this method whether switching signal change or not error signal keeps between hysteresis band limit so output current tracks reference signal [54].

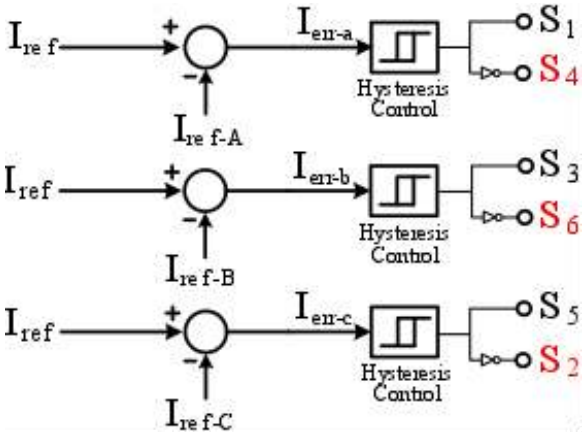

Figure 2.65 Application Scheme of HB Control

The application scheme of hysteresis band current control is simple, and it has a high performance given in Figure 2.65. However, variable switching frequency is significant disadvantage for this method. This method is applicable both three-phase three-wire and three-phase four-wire systems. In the power stage output voltage of each phases is related according to another phase switching position. Phase current can be reduced or increased due to upper switching with respect to sign of source voltage, but lower switching always reduces phase currents. Switching speed depends on, hysteresis band width, output filter inductance, source and dc-link voltages. While high filter inductance, high hysteresis band width and low dc-link voltage means low switching frequency, switching frequency will increase in opposite situation of this. If switching frequency is higher enough high order harmonics can be compensated.

2.12 General Control Scheme of EQR

General Control Scheme of EQR is given in Figure 2.66. mode selection block enables to compensation mode selection and it operates as a switch for the reference signals and allows only selected compensation. This method enables power save for the converter. Selected reference voltages send to modulator block to produce firing signals for IGBTs. Due to ease of application and reliability SPWM method is used in the modulator block. Control system and power stage of EQR is detailed analyzed and whole control system parameters are simulated in the PSCAD/EMTDC given in Appendix A. After completed the simulation work power stage and electrical panel is built.

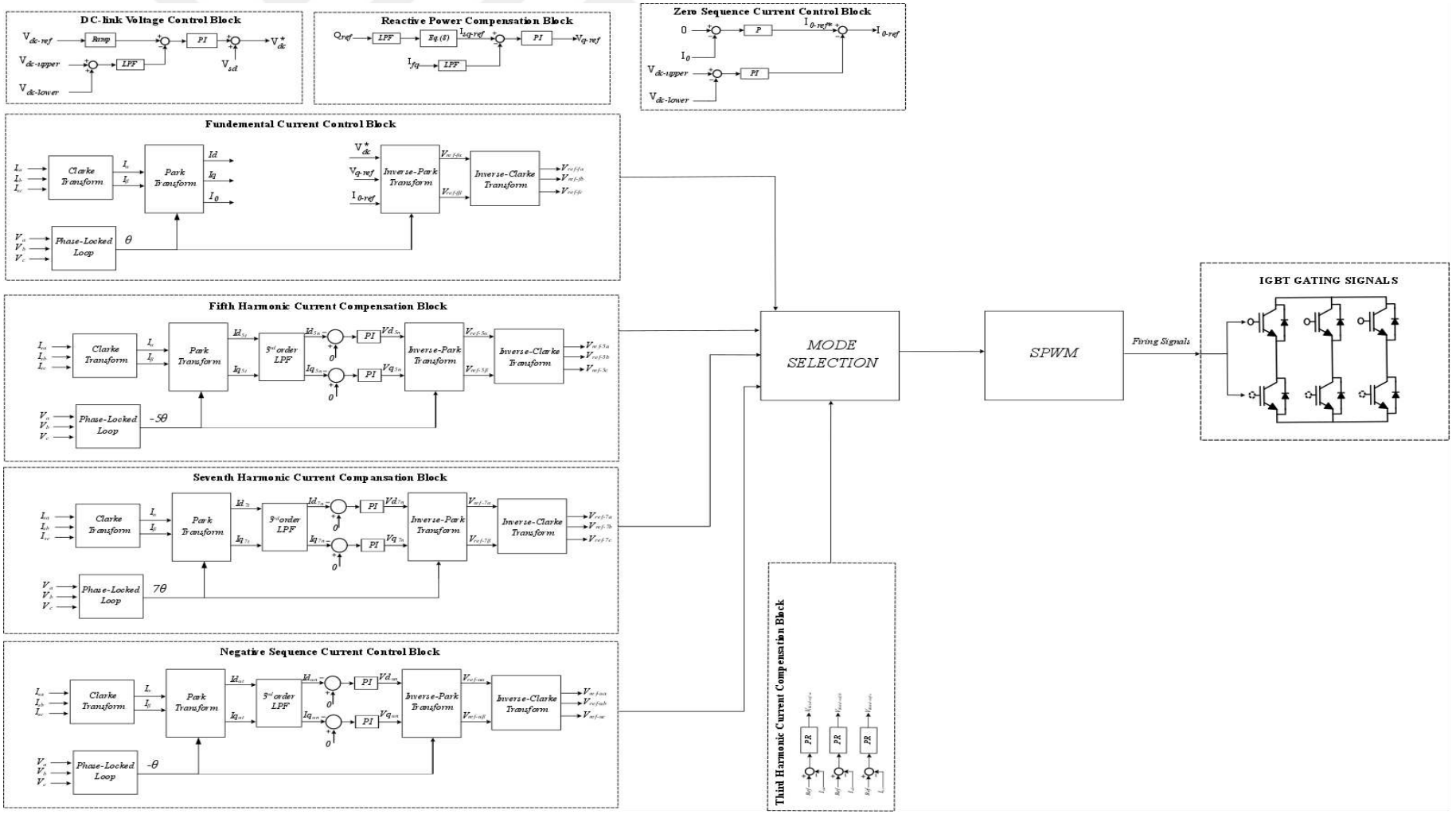

Figure 2.66 General Control Scheme of EQR

CHAPTER 3

DESIGN OF EQR

3.1 Design Specifications

A prototype VSI based EQR employing SPWM technique and having simplest 2 level, 3 leg neutral point clamped topology with half bridge IGBT modules. Prototype testing was carried out in AKDENIZ EDAS distribution type transformers to solve reactive power, low-order harmonic current, neutral current compensation and load balancing problem.

Because of single phase and non-linear loads, distribution type transformers suffer from basic energy quality problems. To specify magnitude of this problems Schneider ION 7650 Class A Power Analyzer is used to take measurement from the different distribution type transformers belong to AKDENİZ EDAS. To specify application place of EQR, measurements are taken from twenty different distribution type transformers and the measurement results are analyzed by each day for six months. The measurement points are taken from the distribution transformers are given Table 3.1. Data are taken from transformers observed using INAVITAS SCADA system shown in Figure 3.1.

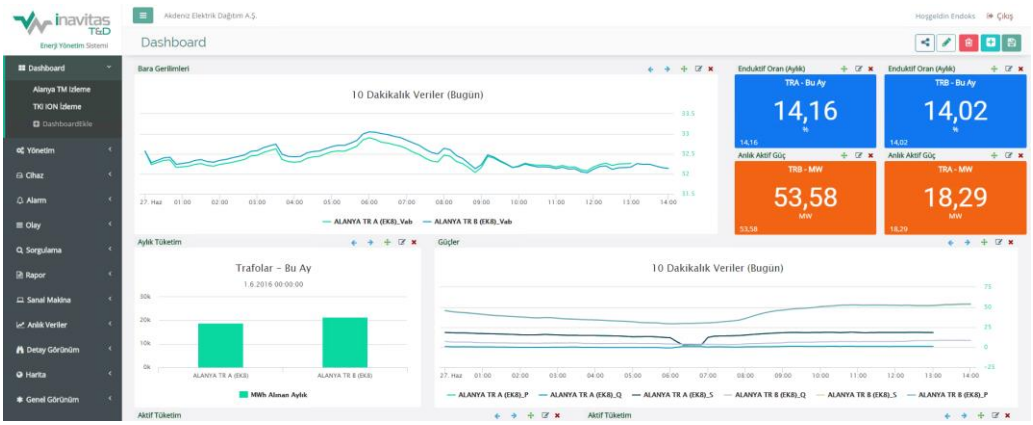

Figure 3.1 INAVITAS SCADA System

Table 3.1 Measurement points are taken from the field

#	Org. Name	Single Line Code & Name	Field Coordinates	IP	CT -Ratio
1	Muratpaşa	192270_1551 VE 1590 SOKAK KESISIMI UGUR MUMCU STADI	36°53'2"-30°43'52"	5.26.170.6	1000/5
2	Konyaaltı	201140_75. YIL DM	36°54'3"-30°39'6"	5.26.133.57	600/5
3	Kepez	542289_YENİ EMEK MH CEYHANCD-SAKARYA BLV KESİŞİMİ BİNA TR	36°53'8"-30°41'46"	5.26.125.131	600/5
4	Kepez	542309 YENİ MH ŞEHİTLER PARKI İÇİ BETON KÖŞK	36°55'9"-30°42'24"	5.26.125.134	600/5
5	Konyaaltı	202222_ÇAKIRLAR KAVŞAĞI BT	36°52'32"-30°34'4"	5.26.136.193	600/5
6	Konyaaltı	202224_JANDARMA YANI BT	36°52'7"-30°33'26"	5.26.153.139	600/5
7	Muratpaşa	192744_GAZİ BULVARI 786 SOKAK KESİŞİMİ	36°54'44"-30°42'25"	5.26.125.132	600/5
8	Kepez	541080_DÜDENDM	36°58'08"-30°43'24"	5.26.125.132	600/6
9	Kepez	542455_GÜNDOĞDU MH.2488-89 SK. BİNA TR	36°55'49"-30°42'33"	5.26.133.57	600/5
10	Kepez	542119_KANAL MH 4703-4699 KESİŞİMİ BİNA TR	36°55'16"-30°40'29"	5.26.153.139	600/5
11	Muratpaşa	192665_SINANOGLU CADDESI SHELL YANI	36°51'55"-30°44'29"	5.26.170.6	600/5
12	Aksu	181130_PINARLI DM	36°56'44"-30°48'45"	5.26.153.139	600/5
13	Kepez	542363 FEVZİ ÇAKMAK MH. 6152 SK. BİNA TR	36°51'55"-30°44'29"	5.26.125.134	600/5
14	Kepez	542765_FEVZİ ÇAKMAK MH. 6176 SK. MUHTARLIK YANI BETON KÖŞK	36°56'29,7"-30°42'27,9"	5.26.125.131	600/5
15	Kepez	542263_ FATİH MH. 3353 BETON KÖŞK	36°56'23"-30°39'0"	5.26.136.193	600/5
16	Muratpaşa	192737_2325 SOKAK CAMDIBI SITESI	36°51'33"-30°48'52"	5.26.136.193	600/5
17	Muratpaşa	192547_MARTI SITESI	36°50'56"-30°47'58"	5.26.170.6	600/5
18	Muratpaşa	192506_2028-2032 SOKAK KAPALI PAZAR	36°51'15"-30°46'20"	5.26.125.131	600/5
19	Muratpaşa	192593_BULENT ECEVIT BULVARI 2088 SOKAK	36°51'27"-30°46'7"	5.26.125.134	1000/5
20	Muratpaşa	192606_1524 VE 1492 SOKAK KESİSİMİ CAG. KOOP. SITESI	36°51'52"-30°44'25"	5.26.133.57	600/5

The measurement results include phase currents, current and voltage harmonics (10 minutes interval according to the IEEE Std. 519-2014 [14]), active and reactive power consumption, and load unbalance of transformers. According to the worst-case (according to the EN and IEE standards) measurement results and load profile of

transformers given in Table 3.2. are selected as design criteria of EQR. As seen from Table 3.2. domestically loads are widely used.

Table 3.2 Load profile of transformers

Single Line Code & Trans. Name	Field Coordinates	Domestic	Office	Industry	Lighting	Agricultural Irrigation	Other
192270_1551 VE 1590 SOKAK KESISIMI UGUR MUMCU STADI	36°53'2"-30°43'52"	80%	10%	0%	10%	0%	0%
192744_GAZİ BULVARI 786 SOKAK KESİŞİMİ	36°54'44"-30°42'25"	70%	20%	0%	10%	0%	0%
192665_SINANOGLU CADDESI SHELL YANI	36°51'55"-30°44'29"	80%	10%	0%	10%	0%	0%
192737_2325 SOKAK CAMDIBI SITESI	36°51'33"-30°48'52"	70%	0%	0%	10%	20%	0%
192547_MARTI SITESI	36°50'56"-30°47'58"	80%	10%	0%	10%	0%	0%
192506_2028-2032 SOKAK KAPALI PAZAR	36°51'15"-30°46'20"	80%	10%	0%	10%	0%	0%
192593_BULENT ECEVIT BULVARI 2088 SOKAK	36°51'27"-30°46'7"	60%	10%	0%	10%	20%	0%
192606_1524 VE 1492 SOKAK KESİSİMİ CAG. KOOP SITESI	36°51'52"-30°44'25"	100%	0%	0%	0%	0%	0%
542289_YENİ EMEK MH CEYHANCD-SAKARYA BLV KESİŞİMİ BİNA TR	36°53'8"-30°41'46"	70%	20%	0%	10%	0%	0%
542309_YENİ MH ŞEHİTLER PARKI İÇİ BETON KÖŞK	36°55'9"-30°42'24"	70%	20%	0%	10%	0%	0%
541080_DÜDENDM	36°58'08"-30°43'24"	80%	10%	0%	10%	0%	0%
542455_GÜNDOĞDU MH.2488-89 SK. BİNA TR	36°55'49"-30°42'33"	90%	0%	0%	10%	0%	0%
542119_KANAL MH 4703-4699 KESİŞİMİ BİNA TR	36°55'16"-30°40'29"	80%	10%	0%	10%	0%	0%
542363_FEVZİ ÇAKMAK MH. 6152 SK. BİNA TR	36°51'55"-30°44'29"	60%	20%	0%	10%	0%	0%
542765_FEVZİ ÇAKMAK MH. 6176 SK. MUHTARLIK YANI BETON KÖŞK	36°56'29,7"-30°42'27,9"	80%	10%	0%	10%	0%	0%
542263_ FATİH MH. 3353 BETON KÖŞK	36°56'23"-30°39'0"	90%	0%	0%	10%	0%	0%
201140_75. YIL DM	36°54'3"-30°39'6"	0%	50%	0%	30%	0%	20%
202222_ÇAKIRLAR KAVŞAĞI BT	36°52'32"-30°34'4"	50%	10%	0%	10%	30%	0%
202224_JANDARMA YANI BT	36°52'7"-30°33'26"	60%	10%	0%	10%	20%	0%
181130_PINARLI DM	36°56'44"-30°48'45"	70%	0%	0%	10%	20%	0%

Because of these loads, excessive neutral currents, loads unbalance and third harmonic will be problem for these transformers. According to the measurement results maximum reactive power consumption are measured at the distribution transformer 192270 as 112 kVAR. 3.,5., 7. harmonics are measured as 42.4 A, 23.2 A and 7.65 A respectively at the distribution transformer 192270. According to the NEMA standard current unbalance is measured as 23.4 % at the distribution transformer 192270. Maximum reactive power consumption, maximum current harmonics and maximum current unbalance values for distribution transformer 192270 are given in Table 3.3.

Table 3.3 Maximum values for distribution transformer 192270

Transformer Name	**Maximum Reactive Power (kVAR)**	**Maximum Current Harmonics (A)**			**Maximum Current Unbalance**
		3.	**5.**	**7.**	
192270	112	42,4	23,2	7,65	%23,4

The important point is here these results shows only maximum values for any time, in other words these problems didn't occur at the same time. When the maximum demand occurs at the transformer for any problem the other problem's maximum values are given in Table 3.4. for distribution type transformer 192270.

Table 3.4 Measurement results according to the maximum values

	Reactive Power (kVAR)	**Current Harmonics (A)**			**Current Unbalance**
		3.	**5.**	**7.**	
Maximum reactive power occurs	112	24,7	5,5	2	%8
Maximum current harmonics occurs	69	42.4	4.2	1.15	%10,6
Maximum current unbalance occurs	67	24,25	9,25	3	%23,4

According to this measurement and analysis of EQR measurement report technical specifications are determined and they are listed in Table 3.5. In the following sections equipment selecting criteria and calculation methods are also discussed.

Table 3.5 Technical specification of implemented EQR

Reactive power generation capacity	±100 kVAR
Third Harmonic injection capacity	50 A
Fifth Harmonic injection capacity	30 A
Seventh Harmonic injection capacity	15 A
Neutral current compensation capacity	432 A
Circuit Topology	3P-4W
Operating Frequency	50 Hz
Maximum input voltage	440 V
DC link voltage	710 V
Maximum DC link current	432 A
Maximum peak IGBT voltage	1200 V
Nominal IGBT current	450 A
DC link capacitor	30 mF/900V
LCL filter reactor inverter side	300uH/200A
LCL filter grid side	100uH/168A
LCL filter capacitor	100 uF
Laminated busbar inductance	<75 nH
Forced-Air Cooling System	630 m3/h
Switching frequency	5kHZ
Heat Sink Thermal Impedance	0.03 k/W

3.2. Design of EQR Power Stage

Power stage of EQR is responsible for producing suitable switched voltage to compensate PQ problems. It consists of mainly below equipment;

1. IGBTs
2. IGBT Drivers
3. DC-Link Capacitors
4. Pre-charge & Discharge Circuit
5. Laminated Busbar
6. Snubber Capacitors
7. Heat Sink & Fan

To identify technical specification of this equipment mainly Table 3.3. and Table 3.4. are used as a reference. According to the reactive power demand at worst case, 100 kVAR EQR design seems suitable since maximum demand is 112 kVAR. If we redefine capacity of EQR as a current, we can say that it has 144 A current injection

capacity at 400 V for each phase. To make possible overload compensation EQR is designed to compensate 10% overload condition. Harmonic currents injection capacity of EQR is selected according to again Table 3.3. and Table 3.4. Maximum values of these tables are criteria for this selection. However, to enhance compensation performance of the EQR and to avoid any load growing effect, these values are multiplying by a correction factor and tolerance values are used as a reference which are given in Table 3.5. Because of the neutral current compensation features EQR maximum dc-link current selected as 432 A since at the limit values for unbalanced neutral wire current case can be reached up to 3 times of phase current. Neutral wire compensation mission makes compulsory 3-phase 4-wire topology has mentioned in section 2.2. Since this device will be used in Turkey network, operating frequency is selected as 50 Hz and operating line to line voltage selected as 400 V with 10% tolerance.

3.2.1 Selection of Power Semiconductor

Combination of power electronic components and a driver circuit can be defined as actively switchable power semiconductors. There are many power semiconductors can be found on the market and present current and voltage limits for controllable power semiconductors are given Figure 3.2. IGBT (Insulated Gate Bipolar Transistor), MOSFET (Metal Oxide Semiconductor Field Effect Transistor), GTO (Gate Turn Off-) thyristors and IGCT (Integrated Gate Commutated Thyristor) became more popular for the line-commutated application compared with thyristor. These products have many advantages such as operation without snubbers, active turn-off in the event of short circuit, short switching time and relatively low switching losses. IGBT products are more common since usage of IGBT is comparatively simple, readily available on the market and it has low-priced when compared with other devices in the same voltage and current range [55].

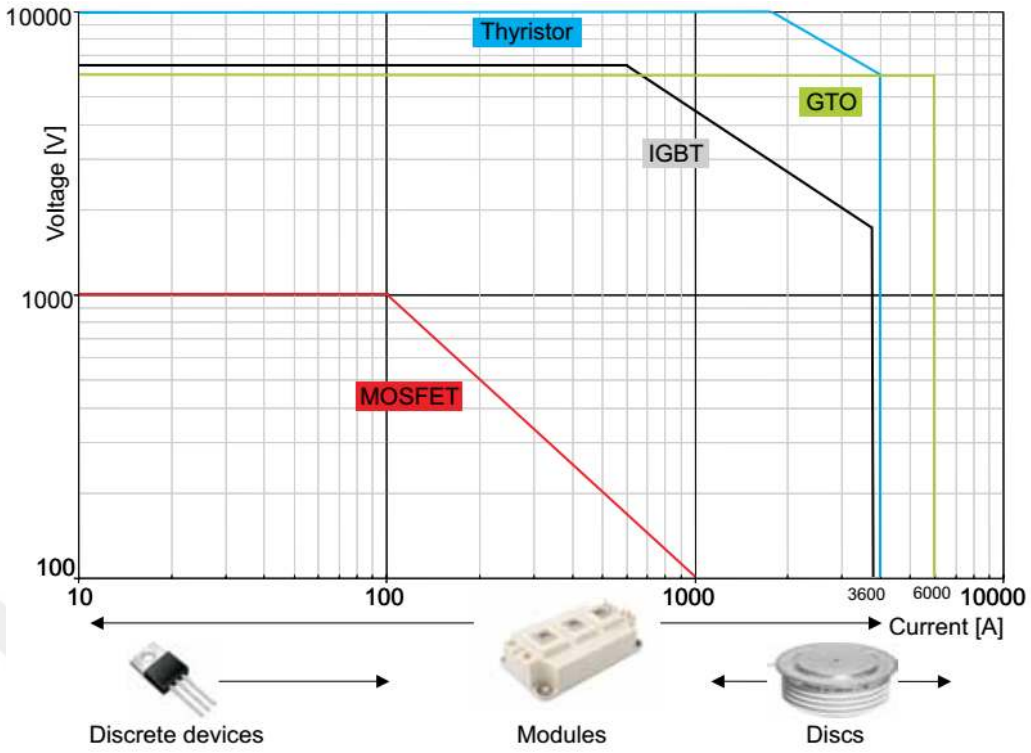

Figure 3.2 Current and voltage limits for controllable power semiconductors [55]

Power electronic switch system generally consist of interfaces to external electric circuitry and the control unit (information processing, auxiliary power supply) whether optical or inductive transmitter are used. General power electronic switch system is depicted in Figure 3.3.

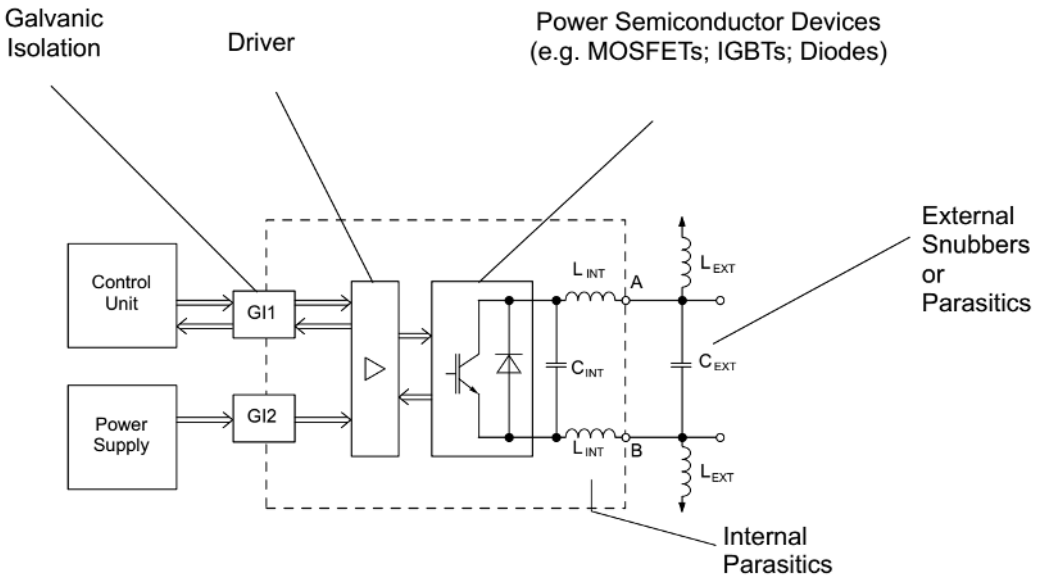

Figure 3.3 Power electronic switch system [55]

Due to mentioned features IGBT is selected as a power semiconductor. Mainly three factors are taking care to select size of IGBT. First one is frequency limits. In this thesis 400 V EQR will be operated by using SPWM technique. To prevent high switching losses within IGBT boundaries 5000 Hz is selected as an optimum switching frequency. Secondary voltage level of EQR must be specified. For 400 V line to line phase voltage, minimum peak value of voltage between the terminal of the power semiconductor can be calculated in 3.1. [56] where $L_{total} = L_{grid} + L_{inv.}$, as a result the minimum voltage rating of power semiconductor for EQR should be taken as 875.52 V (with 50% safety factor) or higher. Finally, current rating of IGBT is measured according to the fault case while neutral current compensation is (calculated as 432 A in section 3.2) figured out. As a result, 1200V 450A SEMIX453GB12E4p half-bridge IGBT module is selected as a power semiconductor with suggested driver SKYPER 12 press-fit 450A driver as seen in Figure 3.4.

$$V_{peak} = \sqrt{2}\, x\, 400\, V + \frac{100000\, VAr}{400\, Vx\sqrt{3}}\, x\, 2\, x\, \pi\, x\, 50\, x\, 0.4\, mH = 583.68\, V \qquad (3.1)$$

Figure 3.4 SEMIX453GB12E4p & SKYPER 12 press-fit

Basic specification of SEMIX453GB12E4p is given in Table 3.6.

Table 3.6 Basic specification of SEMIX453GB12E4p

Item	Symbol	Conditions	Ratings
Collector-emitter voltage	V_{CES}	$T_j = 25\,°C$	1200 V
Gate-emitter voltage	V_{GES}	-	-20…20 V
Collector Current	I_C	$T_c = 25\,°C$	678 A
		$T_c = 80°C$	521 A
	I_{Cnom}	-	450 A
Emitter Current	I_E	-	450 A
Isolation Voltage	V_{iso}	AC sinus 50Hz, t = 1 min	4000 V
Junction Temperature	T_j	-	-40…175 °C
Collector-emitter saturation voltage	$V_{CE(sat)}$	$T_j = 25\,°C$	2.05 V
		$T_j = 150\,°C$	2.40 V
Emitter -collector voltage (FWDi)	V_{EC}	$T_j = 25\,°C$	2.46 V
		$T_j = 150\,°C$	2.38 V
Turn-On switching energy	E_{on}	$V_{CC} = 600\,V$ $I_C = 450\,A$ $V_{GE} = 15/-15\,V$ $R_{G\,on} = 1.1\,\Omega$ $R_{G\,off} = 1.1\,\Omega$ $d_i\,/\,dt_{on} = 7000A/us$ $d_i\,/\,dt_{off} = 3300A/us$ $d_u\,/\,dt = 4800\,V/us$ $T_j = 150\,°C$	25 mJ
Turn-Off switching energy	E_{off}		57 mJ

3.2.2 DC-Link Capacitor Selection

The compensation performance of the EQR is directly depends on storage element dc-link capacitor voltage level (V_{dc}) and capacitance value (C_{dc}). To drive the enough compensation currents to the system minimum capacitor voltage level is calculated according to the compensation parameters. To make stable compensation it is not allowed peak-to-peak voltage ripple higher than 1-3% on the dc-link voltage level. Minimum dc-link voltage level is EQR is figured out under reactive power and current harmonics compensation condition as a worst case. Referring to Table 3.5., required EQR fundamental output voltage (V_{EQRf}) and EQR harmonic output voltage (V_{EQRn}) at each harmonic order can be found. As V_{EQRf} and V_{EQRn} are in RMS values, to

calculate required EQR dc-link level fundamental reactive current component and nth order harmonic current component peak values must be calculated in which $V_{dcf} = \sqrt{2}V_{EQRf}, V_{dcn} = \sqrt{2}V_{EQRn}$. These peak values can be considered as superimposed since required dc-link voltage requirement V_{dcx} can be calculated for single phase circuit model of EQR can be calculated as equation (3.2).

$$V_{dcx} = \sqrt{|\mathrm{V_{dcf}}|^2 + \sum_{\mathrm{n=2}}^{\infty} |\mathrm{V_{dcn}}|^2} \tag{3.2}$$

To make compensation simultaneously, required EQR fundamental output voltage (V_{EQRf}) and EQR harmonic output voltage (V_{EQRn}) can be calculated in equation (3.3) and (3.4).

$$V_{EQRf} = V_{p-n} + Z_{n=1}\, x\, I_{cn=1} \tag{3.3}$$

$$V_{EQRn=3,5,7} = Z_{n=3,5,7}\, x\, I_{cn=3,5,7} \tag{3.4}$$

Z_n denotes LCL filter impedance at fundamental and nth. order harmonic frequency and it can be expressed as:

$$Z_n = n\, x\, 2\, x\, \pi\, x\, f\, x\, L_{total} \tag{3.5}$$

Table 3.7 Sufficient voltage levels to make compensation

Frequency (Hz)	**Inductance (Ltotal)**	**Impedance (Zc, n = 1,3,5,7)**	**Current (Icn, n = 1,3,5,7)**	**Voltage (VEQRf,n)**
50	0.4 mH	0.125 Ω	144 A	230V +18 V
150	0.4 mH	0.377 Ω	50 A	18.85 V
250	0.4 mH	0.628 Ω	30 A	18.84 V
350	0.4 mH	0.874 Ω	15 A	13.11 V

According to the worst-case compensation parameters, required voltage level which must be produced by EQR is given in Table 3.7. In this table PQ problems for each phase assumed to be balanced. Using equation (3.2) V_{dcx} according to the Table 3.7.

calculated as 353.22 V. Minimum dc-link voltage level V_{dc} for three-phase four-wire EQR can be found as $2\,x\,V_{dcx} = 706.45\,V$. In the EQR project dc-link value is selected as 710 Vdc.

To select suitable capacitance value firstly allowed ripple voltage is decided. In this project around 1-3% ripple level is selected and ripple voltage level is used as maximum 8V verified by PSCAD/EMTDC. According to this value dc-link capacitance value ($\boldsymbol{C_{dc}}$) is calculated using equation (3.6).

$$C_{dc} = \frac{I_d}{2\,x\,w\,x\,V_{dc-ripple}} \tag{3.6}$$

In which I_d demonstrates EQR supply current and $w = 2\,x\,\pi\,x\,f$ is calculated in fundamental frequency

$$I_d = \frac{EQR\ power\ rating = 100000\ VAr}{dc - link\ voltage\ level = 710\ Vdc} \tag{3.7}$$

Using equation (3.6) and (3.7) required dc-link capacitance is calculated as 28 mF.

450 V 10mF EPCOS very high ripple current (72 A @40 °C) B437 series aluminum electrolytic dc capacitor is selected and to provide dc-link capacitor design criteria, 432 A fault current condition and three-phase four-wire topology connection which is depicted in Figure 3.5. is used.

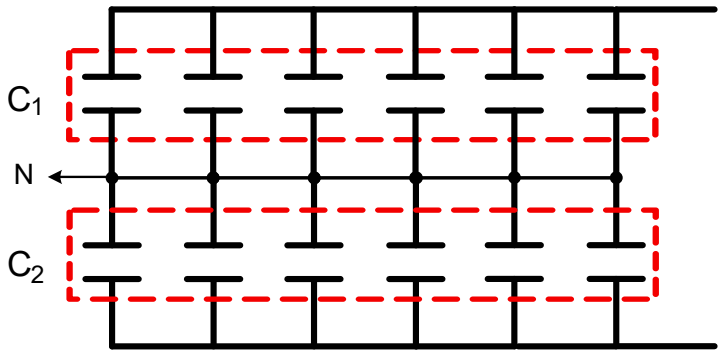

Figure 3.5 DC-Link capacitor configuration

Two capacitors group (C1 and C2) is connected as a series. Using this connection created mid-point of the capacitors is used for a path for zero-sequence compensation

and 450 Vdc voltage level is increased up to 900 Vdc. Each group contains six discrete capacitors, and these are connected to each other as a parallel to increase current capability of the dc-link by this way total dc-link reach to 432 A. Total capacitances is 30 mF according to this final design.

Beside these calculations another important factor is low inductive dc-link design since due to stray inductance in the dc path, voltage overshoots occur during switch off of the IGBT according to the equation (3.8). These voltage overshoots may destroy the IGBT module because they are added to the dc-link voltage and may lead to $V_{CE} > V_{CEmax}$. B437 series aluminum electrolytic dc capacitor has very low ESL value (<23 nH) in the parallel branch this value is reduces to one in six, due to series branch these value increases two times. Finally, equivalent ESL value will be one in three of 23 nH (~7.6 nH). With low inductive dc-link design these voltage overshoots can be reduced significantly.

$$V_{overshoot} = L_{stray}\, x\, \frac{d_i}{d_t} \tag{3.8}$$

3.2.3 Pre-charge & Discharge Circuit

To avoid any inrush current problem, EQR pre-charge circuit increases dc-link voltage level up to line to line phase voltage peak value before the switching. When system is stopped, discharge circuit reduce to dc-link voltage to safety level. While pre-charge circuit consist of resistors, full bridge rectifier module and relay, discharge circuit only contains of discharge resistors. Pre-charge circuit and discharge resistors of the capacitors is depicted in Figure 3.6. and corresponding circuit is simulated using OrCAD Capture.

Charging circuit shown in Figure 3.6 employees a full bridge rectifier connected to the dc-link through pre-charging resistors. Pre-charging resistors is used in the ac side to limit the charging current. Electromechanical relay contacts represented in the OrCAD model as U1 and U2. These contacts switched off with start command through pre-charge time. When pre-charge time is ended, these contacts again switched on.

Discharging resistors shown in Figure 3.6 provides rapid discharge. Electrical specification of charging and discharging circuit is given in Table 3.8.

Table 3.8 Electrical specification of charging and discharging circuit

Aim of Usage	Brand-Name	Model	Specification
Full-Bridge Rectifier	SEMIKRON	SKB 30/12	1200V, 30 A
Pre-Charge Resistor	ARCOL	HS100	330 Ω, 100W
Pre-Charge Relay	OMRON	MY4IN	10 A, 24Vdc
Discharge Resistor	ROYAL	263 P	23.5 kΩ, 20W (2-47 kΩ,10W)

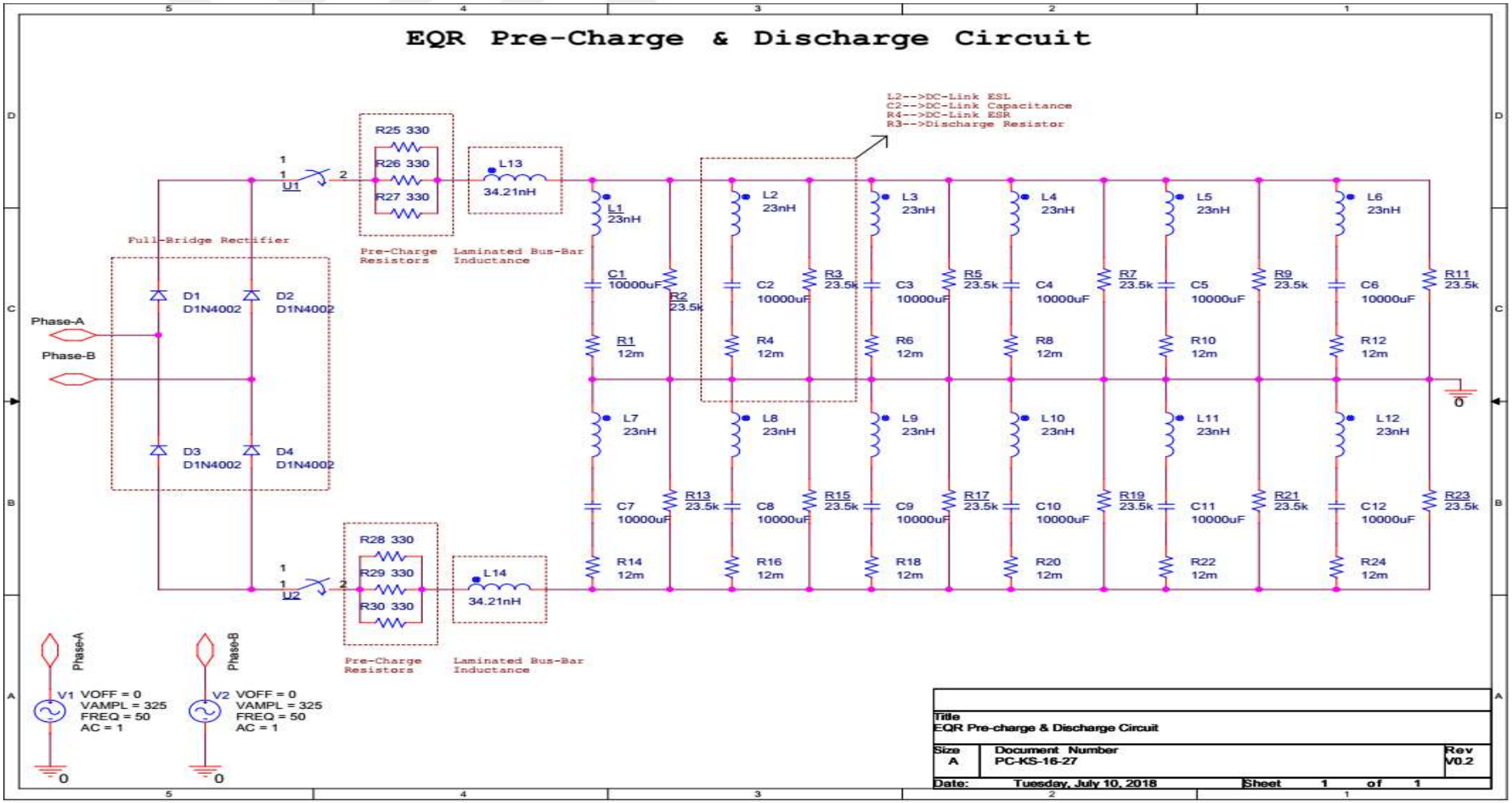

Figure 3.6 Pre-Charge & Discharge Circuit OrCAD Model

3.2.4 Laminated Busbar Design

DC path inductance caused by the distance between dc storage element and power switch is one of the majors constrain to develop power stage. High dc path inductance leads to non-ideal inverter operation, voltage overshoot, voltage droop and resonance with snubber capacitors [57].

Laminated busbar inductance plays an important role when calculating total dc path inductance. This inductance value can be calculated by analytically or by using Finite Element Analyze (FEA) tools and it can be limited using some approximations. The mechanical design has a significant influence to reduce the inductance of the dc path and approximations are described according to these design criteria.

1. The conductors must be parallel, and they must be overlapped. There must not be any space between conductors since each additional 1 cm² space adds nearly 10 nH additional inductance to total stray inductance as shown in Figure 3.7.

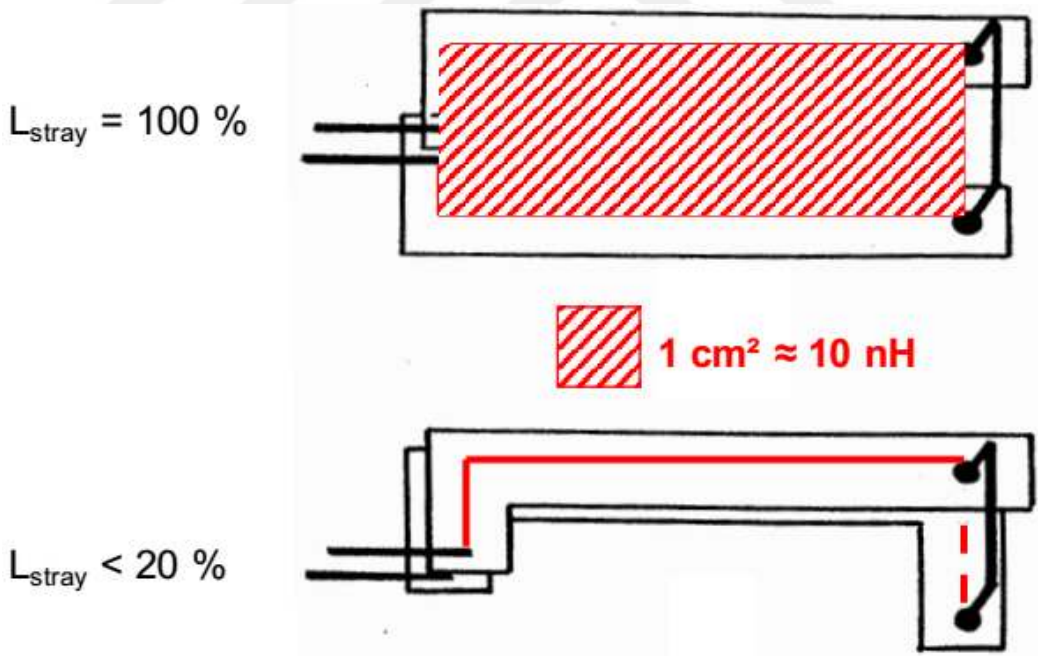

Figure 3.7 Laminated busbar conductor's placement

2. Capacitor terminals connections must be in line with the main current flow as shown in Figure 3.8. This connection reduces total inductance nearly 70 % when compared with opposite case.

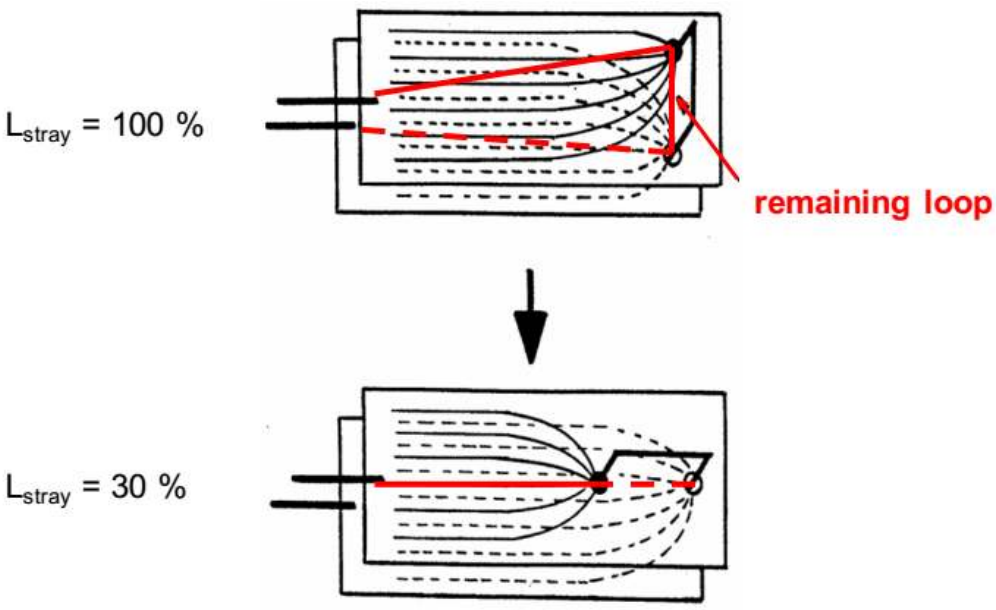

Figure 3.8 Suitable DC-Link Capacitor terminals direction

Because of more than one capacitor is used, final placement must be designed as Figure 3.9.

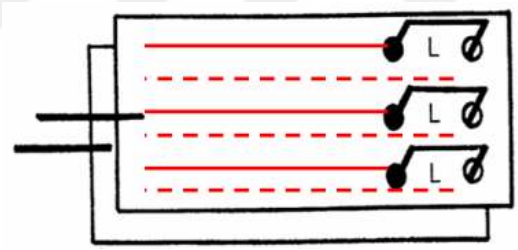

Figure 3.9 Suitable DC-Link capacitor terminal placement

3. Laminated busbars orientation also must be taken into regard. Current distribution between '+' busbar and '-' busbar are directly affects the stray inductance, so this distribution must be designed as Figure 3.10.

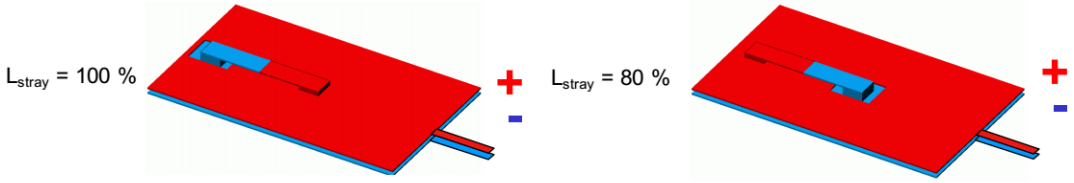

Figure 3.10 Suitable orientation of planer busbars

4. To obtain low inductive power stage above restriction must be taken into attention also as much as possible parallel current paths must be created. Large current path loops mean large inductance as shown in Figure 3.11.

+

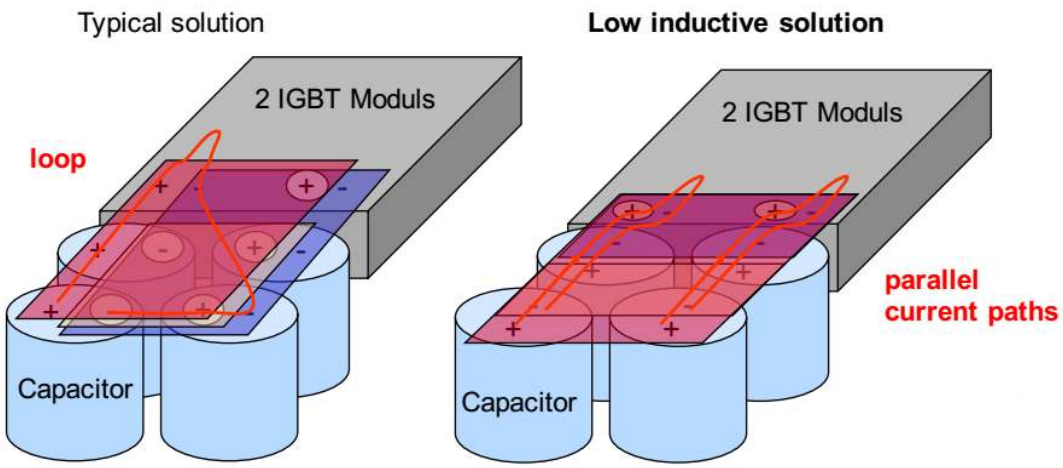

Figure 3.11 Low inductance power stage design

5. Dielectric material is used between two conductors to isolate conductors. Thickness of this material effects laminated busbar inductance. Laminated busbar inductance increases by increasing dielectric thickness or vice versa.
6. Copper plates are used to produce laminated busbar. The width of this conducting plates plays important role on the laminated busbar inductance. Laminated busbar inductance decreases by increased conductor width.
7. IGBT's switching frequency also impacts laminated busbar inductance. Higher switching frequency reduces laminated busbar inductance.

However, these experiential approaches do not guarantee the minimum inductance.

Many numerical modelling tools is available to calculate this complex inductance model. However, in this thesis inductance situated on the dc path is calculated mathematically regarding inductive elements on the dc path. In this section laminated busbar inductance is calculated with internal inductance L_i and external inductance L_e. The other components inductance values are taken from manufacturer catalog than added to laminated busbar inductance to obtain total stray inductance on the dc path. Finally, the result obtained from calculation is verified by experimental setup.

Laminated busbar rough model and physical representation is depicted in Figure 3.12. In this model dimensional quantities are given to make calculation.

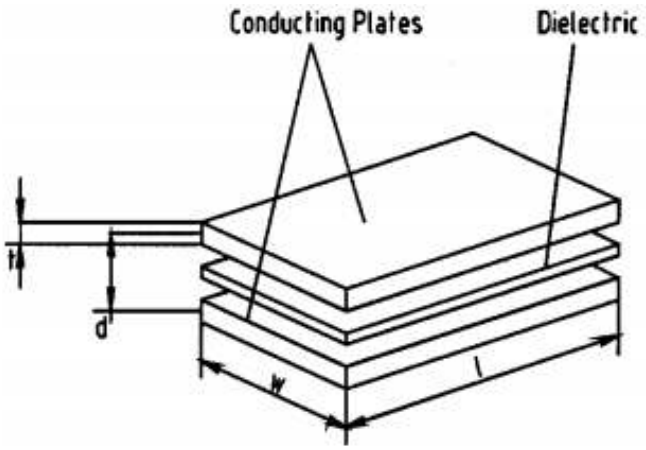

Figure 3.12 Physical representation of the bar, showing dimensional quantities [26]

According to the Figure 3.12. l [m] represents length, w [m] represents width of the busbar, t [m] represents thickness of the plates and d [m] represents distance between the two plates.

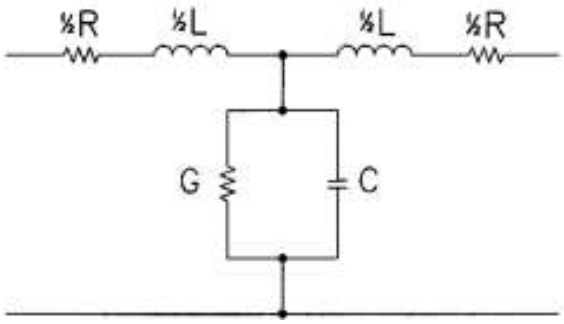

Figure 3.13 Electrical equivalent circuit to model EQR busbar [26]

The mechanical dimensions of the busbar are determined according to the number of capacitors, capacitor mechanical dimensions, heat sink and IGBT dimensions, and considering low inductance design suggestions. Eventually, designed is completed in the CAD program than inductance of the busbar is calculated according to these dimensions. Mechanical properties of the laminated busbar and some other properties related with busbar are given in Table 3.9.

Table 3.9 Mechanical properties of busbar

Description	Abbreviation	Value
Length of the busbar	l	69 cm
Width of the busbar	w	16 cm
Thickness between busbar plates	d=$t_{dielectric}$	0.05 cm
Thickness of busbar (copper plate)	t	2 mm
Permittivity of air	ε_0	8.85419e-12
Relative permittivity of material	ε_r	3.3
Permeability of air	μ_0	1.25664e-06
Relative permeability of air	μ_r	0.9999999
Resistivity of the busbar (pure copper)	ρ	1.72e-08 Ωm

To make calculation firstly, model must be selected. Lumped parameter model or transmission line model can be applied. To make this decision highest frequency component of the EQR power stage must be defined [26]. Highest critical frequency defined as:

$$f_c = \frac{1}{2x\pi x t_f} \tag{3.9}$$

where t_f represents the device fall time for SEMIX453GB12E4p IGBT pack. For SEMIX453GB12E4p model IGBT pack, device fall time is 115 ns so highest critical frequency is ~1.4 MHz.

The wavelength is defined in (3.10).

$$\lambda = \frac{c}{f_c} \tag{3.10}$$

Since $\lambda/4 = 54$ m and is not comparable with the dimension of the busbar, lumped stray inductance model shown in Figure 3.13 can be used. Figure 3.13 contains four lumped parameters, these are the busbar inductance L, capacitance C and resistance R. The dielectric losses are represented by the conductance G.

The capacitance C between busbars and dielectric losses G can be calculated according to the (3.11) and (3.12) respectively,

$$C = \varepsilon_0 \varepsilon_r \frac{w\ x\ l}{t_{dielectric}} \tag{3.11}$$

$$G = \sigma \frac{w\ x\ l}{t_{dielectric}} \tag{3.12}$$

Laminated busbar inductance composes of internal inductance and external inductances. Due to the flux linkages between busbar plates internal inductance is occurred. Skin and proximity effect impact internal inductance value and for low frequency application internal inductance is more important. Internal inductance for low frequency application can be calculated in equation (3.13).

$$L_i = \frac{\mu_0\ x\ \mu_r}{8\pi}\ x\ l \tag{3.13}$$

Because of the geometry of the busbar external inductance occurs and this inductance value is frequency independent inductance. External inductance can be calculated in equation (3.14).

$$L_e = \mu_0 \frac{t_{dielectric}}{w} \tag{3.14}$$

δ to be skin effect for switching frequency f. It can be expressed as:

$$\delta = \sqrt{\frac{\rho}{\pi\ x\ f\ x\ \mu_0}} \tag{3.15}$$

Since $t > 2\delta$ resistance of the busbar R can be calculated according to the equation (3.16).

$$R = \rho \frac{4l}{w\ x\ \delta} \tag{3.16}$$

According to the related calculations laminated busbar, calculated electrical parameters are given in Table 3.10.

Table 3.10 Electrical parameter of laminated busbar

Description	Abbreviation	Value
Capacitance between busbars	C	6.45 nF
Internal inductance of busbar	L_i	34.5 nH/m
External inductance of busbar	L_e	3.92 nH/m
Skin depth	δ	0.93 mm
Resistance of the busbar	R	0.3 Ωm

To obtain total dc path inductance analytically other inductances like IGBT inductance, capacitor ESL value, screw and spacers inductances must be added to summation of the internal and external inductance. According to the datasheets of this material

Equivalent IGBT part inductance L_{IGBT} = 20 nH

Equivalent capacitor ESL value L_{ESL} = 7.6 nH

Screw and spacer inductance L_{ss} = 10 nH

Internal Inductance of busbar L_i = 34.5 nH

External Inductance of IGBT L_e= 3.92 nH and total stray inductance is:

$$L_{stray} = L_{IGBT} + L_{ESL} + L_{ss} + L_i + L_e = 76.02\ nH \quad (3.17)$$

The produced laminated busbar is given in Figure 3.14.

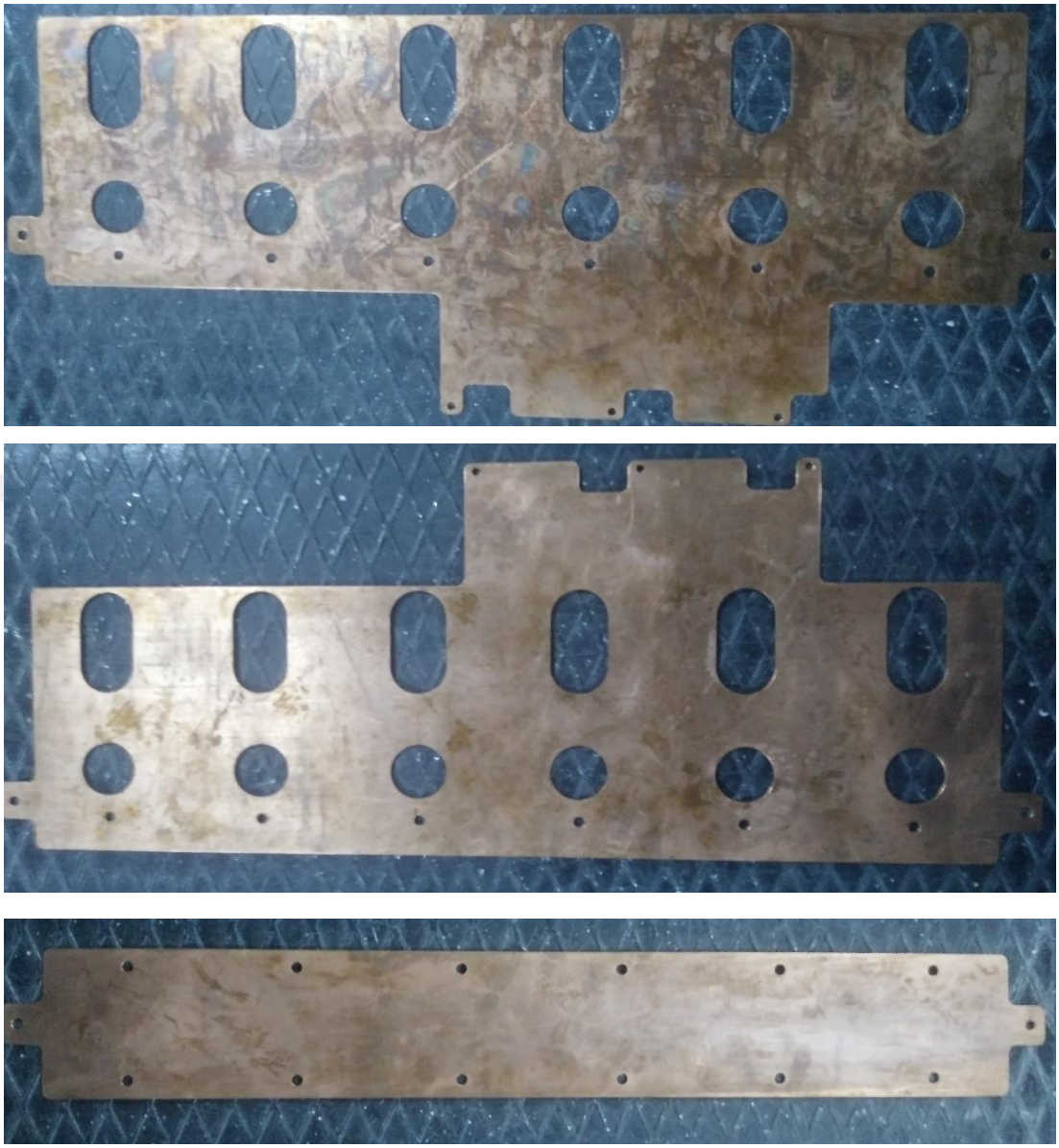

Figure 3.14 '+', '-' and 'neutral' busbar plates

Total stray inductance on the dc path is verified using experimental setup given in Figure 3.15.

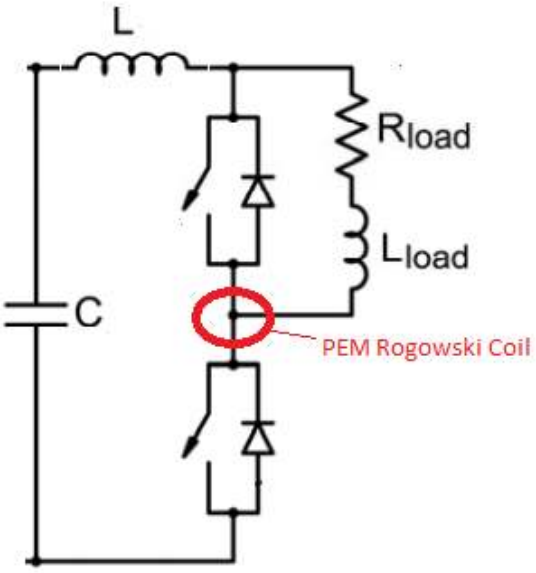

Figure 3.15 Total stray inductance test circuit

Bottom IGBT is switched off for a short time (1 ms.) in the circuit given in Figure 3.15. Using PEM rogowski coil and voltage probe, current and voltage waveforms are taken. Corresponding results are given in Figure 3.16.

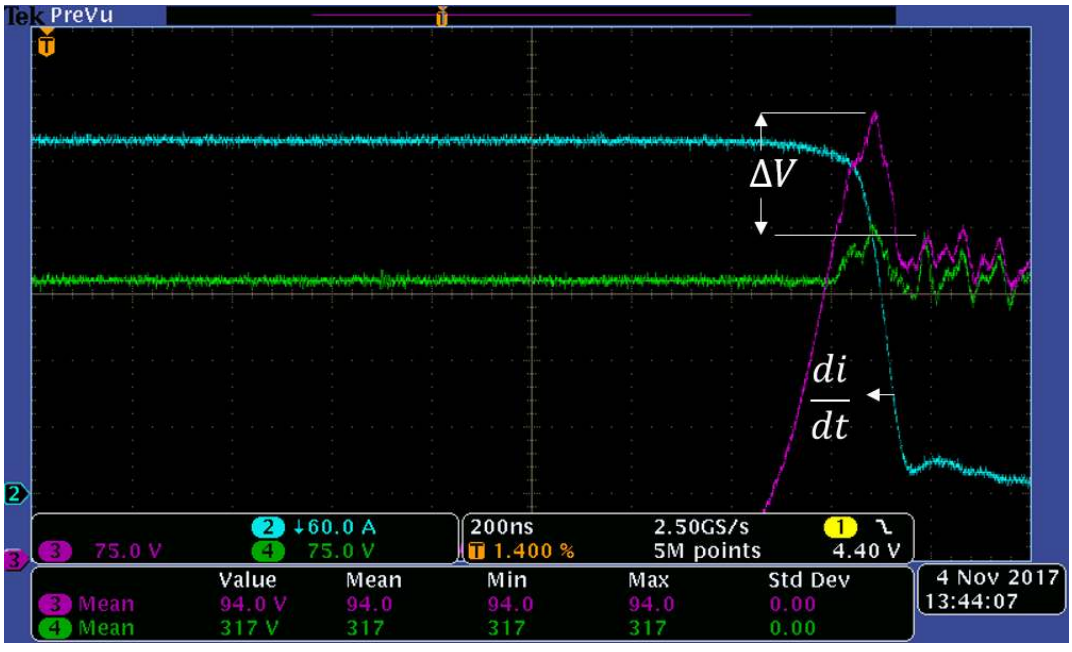

Figure 3.16 Load current and voltage waveform

$$\Delta V = L\, x\, \frac{di}{dt} \tag{3.18}$$

ΔV is the instantaneous voltage change between the load terminals and is equal to 135V and it is demonstrated as a magenta line for Figure 3.16.

$\frac{di}{dt}$ can be defined as time dependent current change and according to the Figure 3.16. cyan line its value is 1.8 A/nsec. Using these values dc path total stray inductance calculated as:

$$L\ = \Delta V\ /\ \frac{di}{dt} = 75\ nH \tag{3.19}$$

Equation (3.19) shows that theoretical work is verified by experimental work and recommended maximum 100 nH stray inductance limit condition is provided.

3.2.5 Snubber Capacitor Selection

To provide voltage overshoots during the switch off, snubber capacitors are used to protect IGBT module. The snubber circuits work as a low pass filter and prevents voltage overshoot caused bay stray inductance on the dc path. There are many types of snubber circuits to protect IGBT as depicted in Figure 3.17.

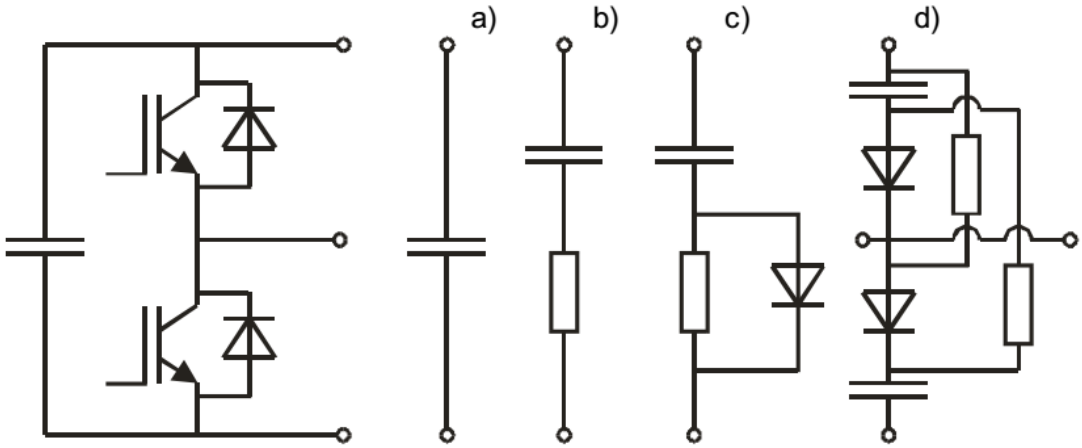

Figure 3.17 Different type of snubber circuit

Due to the simplicity and manufacturer recommendation only, parallel connected high voltage film capacitors can be used as a snubber circuit as shown in Figure 3.18. Important things here is snubber capacitor must be located directly at dc terminals of the IGBT module.

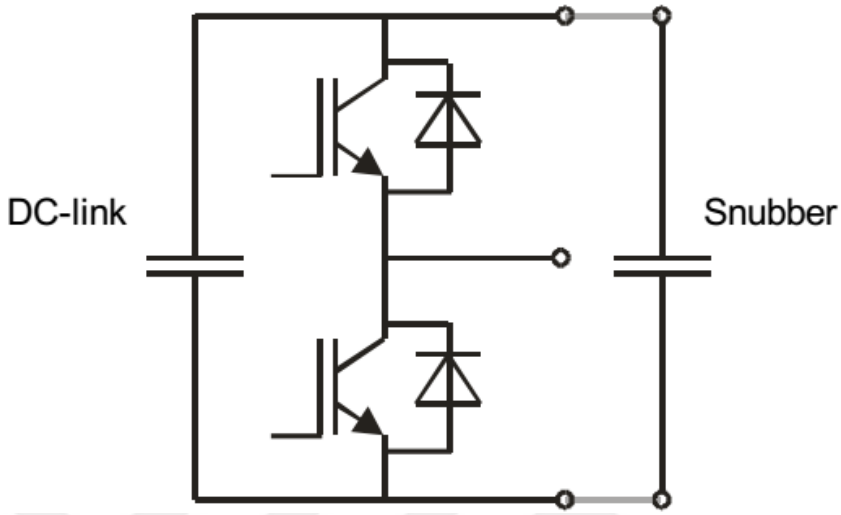

Figure 3.18 Selected snubber circuit

To select correct snubber capacitor value below calculation must be done otherwise snubber does not reduce the voltage overshoots and dc-link oscillation can occur.

$$L_{stray} = \frac{\Delta Vs^2 \; x \; C_{snubber}}{I_c^2} \tag{3.20}$$

ΔVs is the second voltage overshoot level which is calculated as 60 V from the Figure 3.19. I_c is the nominal current and for 100 kVAR operation calculated as 144 A. Using equation (3.20) $C_{snubber}$ value is calculated as 0.432 uF.

Because of the IGBT blocking voltage level is 1200V and dc-link voltage level is 710 V according to the manufacturer application note minimum snubber capacitor voltage level must be 1000V. According to these explanations on the power stage of prototype EQR, VIMA FKP series 0.47 uF 1600 V snubber capacitor is selected to use as snubber capacitor.

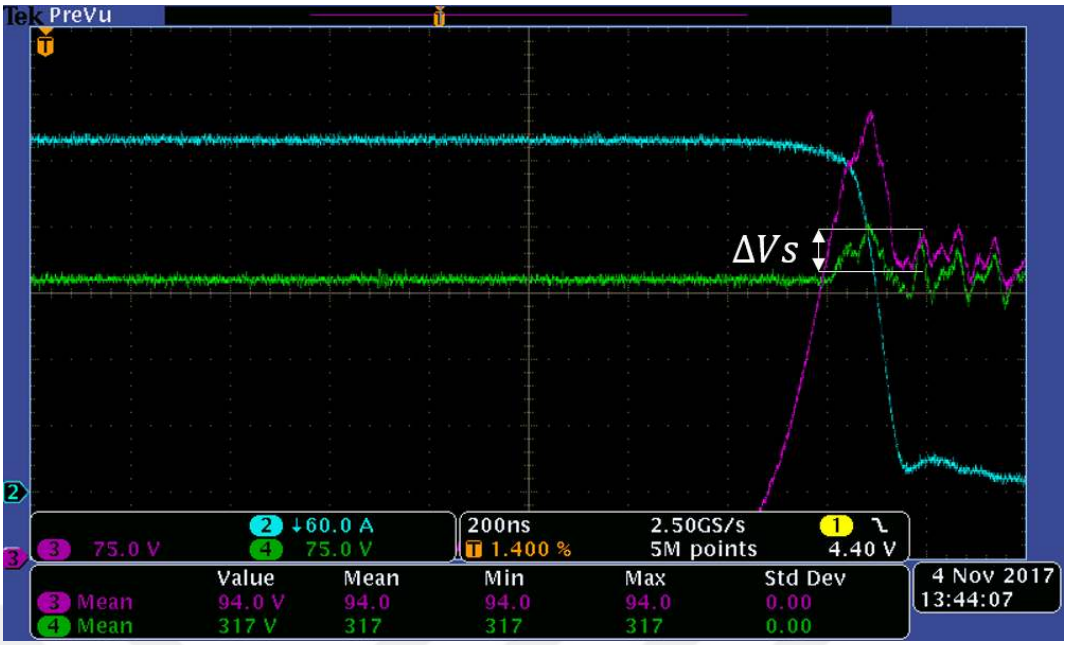

Figure 3.19 Second voltage overshoot

3.2.5 Heat Sink & Fan Selection

Thermal restrictions are one of the most important parameters for power stage design. Power electronic devices always faced with thermal problems due to interaction between the heat flow paths of individual die within the power module [58]. This thermal problem for switching devices leads to malfunction operation and lifetime reduction. To prevent thermal issue thermal sinks are used. According to the needs thermal sinks are cooled via water or air to reduce thermal impedance. To make heat sink selection power dissipation must be calculated according to the inverter maximum output current and modulation technique.

When power switch started to switch two losses occurs. These are switching losses and conduction losses both IGBT and diode. The sum of these total losses gives total power dissipation. To make power dissipation calculation corresponding formulas are given IGBT manufacturer application note for SPWM technique and three-phase four wire inverter [55]. Using power dissipation magnitudes, steady-state thermal analysis can be achieved. According to this analysis junction temperature can be found with related ambient temperature. Conduction losses both IGBT and diode can be calculated according to (3.21) and (3.22) respectively,

$$P_{cond(IGBT)} = \left(\frac{1}{2\pi} + \frac{m\ x \cos(\varphi)}{8}\right) V_{CE0}(T_j)\ x\ \hat{I} + \left(\frac{1}{8} + \frac{m\ x \cos(\varphi)}{3\pi}\right) r_{CE}(T_j)\ x\ \hat{I}^2 \quad (3.21)$$

$$P_{cond(D)} = \left(\frac{1}{2\pi} - \frac{m\ x \cos(\varphi)}{8}\right) V_{F0}(T_j)\ x\ \hat{I} + \left(\frac{1}{8} - \frac{m\ x \cos(\varphi)}{3\pi}\right) r_F(T_j)\ x\ \hat{I}^2 \quad (3.22)$$

Switching losses both IGBT and diode can be calculated according to (3.23) and (3.24) respectively,

$$P_{sw(IGBT)} = f_{sw}\ x\ E_{on+off}\ \frac{\sqrt{2}}{\pi}\ \frac{I_{out}}{I_{ref}} \left(\frac{V_{cc}}{V_{ref}}\right)^{K_v} \left(1 + TC_{Esw}(T_j - T_{ref})\right) \quad (3.23)$$

$$P_{sw(D)} = f_{sw}\ x\ E_{rr}\ x\ \frac{\sqrt{2}}{\pi} \left(\frac{\hat{I}}{I_{ref}}\right)^{K_i} \left(\frac{V_{cc}}{V_{ref}}\right)^{K_v} \left(1 + TC_{Err}(T_j - T_{ref})\right) \quad (3.24)$$

Corresponding parameters and results are given in Table 3.11.

Table 3.11 Corresponding parameters and results of power dissipation calculation

Description	Abbreviation	Value
Modulation index	m	1
Power factor	$\cos(\varphi)$	1
Collector-emitter threshold voltage	V_{CE0}	0.8 V
Peak of the EQR output current @100kVAr, 400V	$\hat{I}$	203.64 A
On-state slope resistance of IGBT	r_{CE}	3.6 mΩ
Threshold voltage of an inverse diode	V_{F0}	1.1 V
Forward slope resistance of an inverse diode	r_F	2.8 mΩ
Switching frequency	f_{sw}	5000 Hz
Dissipated switching energy during turn on and turn off	E_{on+off}	0.082 J
EQR maximum output current @100kVAr, 400V	I_{out}	144 A
Reference current values for loss calculation	I_{ref}	432 A
DC link voltage	V_{CC}	710 V
Reference voltage values for loss calculation	V_{ref}	718 V
Exponents for the voltage dependency of switching losses	K_v (IGBT)	~1.3…1.4
Temperature coefficients of the switching losses	TC_{Esw}	~0.003 1/K
Reference temperature values for loss calculation	T_{ref}	125 °C
Energy dissipation during reverse recovery	E_{rr}	0.037 J
Exponents for the voltage dependency of switching losses	K_v (Diode)	~0.6
Exponents for the current dependency of switching losses	K_i (Diode)	~0.6
Temperature coefficients of the switching losses	TC_{Err}	~0.006 1/K

According to the Table 3.11. one IGBT and one diode power dissipation inside the SEMIX453GB12E4p calculated as:

$$P_{total(IGBT)} = P_{cond(IGBT)} + P_{sw(IGBT)} = 157\ Watt \tag{3.25}$$

$$P_{total(D)} = P_{cond(D)} + P_{sw(D)} = 56\ Watt \tag{3.26}$$

The total losses of the EQR power stage $P_{total(M)}$ are obtained by multiplying the individual losses with the number of switches n integrated in the power switch:

$$P_{total(M)} = n\ x\left(P_{total(IGBT)} + P_{total(D)}\right) = 6\ x\ 213\ W = 1278\ W \tag{3.27}$$

Junction temperature T_J is critical design parameter for heat seat designing since junction temperature directly affects the IGBT life time. Thanks to development of power electronic technology IGBT modules give flexibility for junction temperature and they allow 175 °C junction temperature. However, manufacturers advise maximum 100~125 °C allowable junction temperature. Steady state thermal model of the power stage is given in Figure 3.20 and it must be extracted to calculate junction temperature of the power switch. Necessary information about junction temperature calculation is given in Table 3.12.

Table 3.12 SEMIX453GB12E4p half bridge IGBT pack thermal parameters

Description	Abbreviation	Value
Thermal resistance junction to case	$R_{th(j-c)IGBT}$ $R_{th(j-c)Diode}$	0.066 K/W 0.1 K/W
Thermal resistance case to fin	$R_{th(c-f)}$	0.03 K/W
Thermal resistance fin to ambient	$R_{th(f-a)}$	0.03 K/W
Ambient temperature	T_a	40 °C

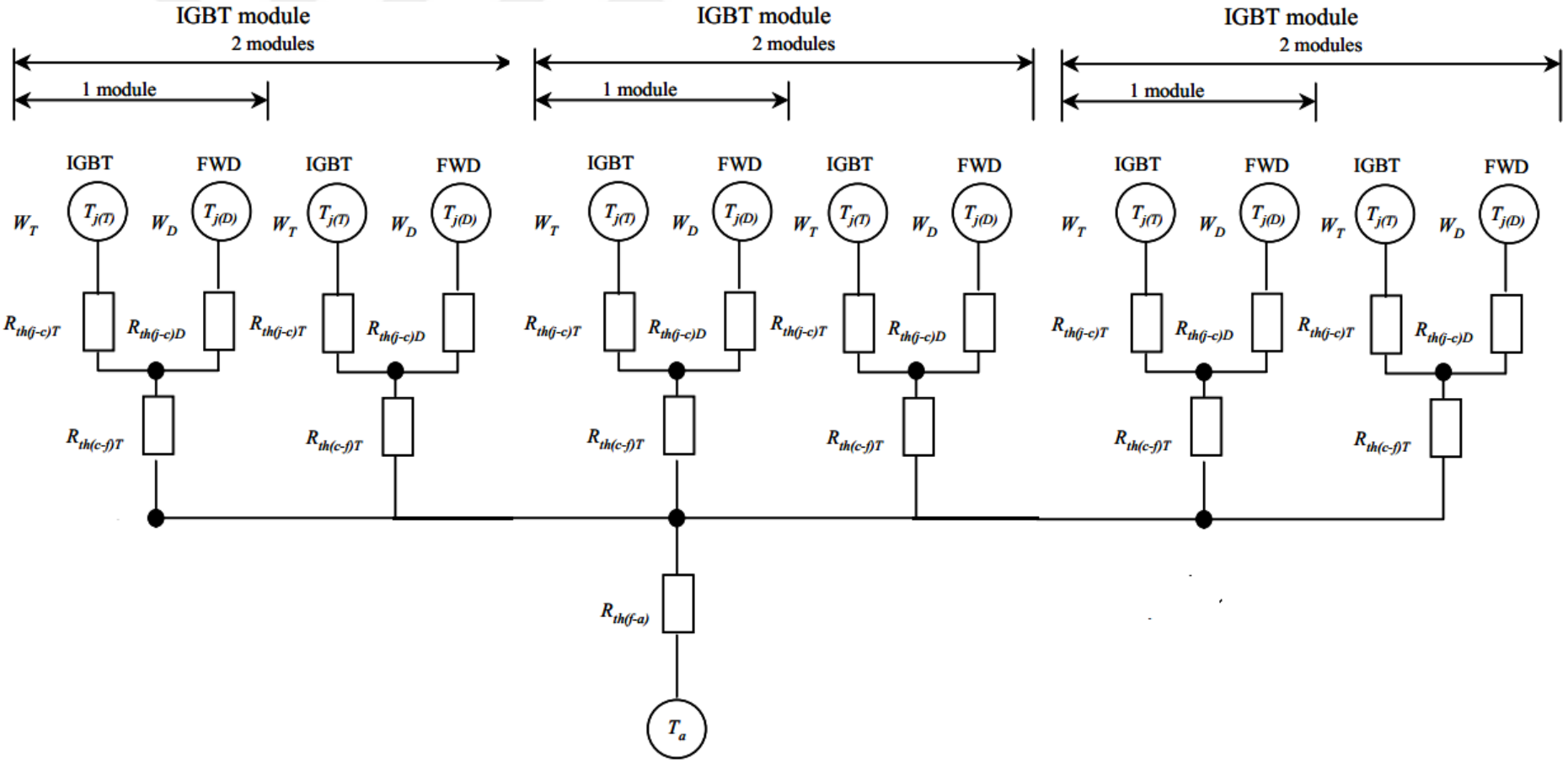

Figure 3.20 Steady-state thermal model of EQR power stage [58]

$$T_{j(IGBT)} = P_{total(IGBT)} x\, R_{th(j-c)IGBT} + \left[\left(P_{total(IGBT)} + P_{total(D)}\right) x R_{th(c-f)}\right] + \left[\left(6P_{total(IGBT)} + 6P_{total(D)}\right) x R_{th(f-a)}\right] + T_a \quad (3.28)$$

$$T_{j(Diode)} = P_{total(Diode)} x\, R_{th(j-c)Diode} + \left[\left(P_{total(IGBT)} + P_{total(D)}\right) x R_{th(c-f)}\right] + \left[\left(6P_{total(IGBT)} + 6P_{total(D)}\right) x R_{th(f-a)}\right] + T_a \quad (3.29)$$

As a heatsink SEMIKRON P-16-300-16B aluminum thermal fin is selected with 630 m³/h blower fan. This combination serves $R_{th(f-a)}$ = 0.03 K/W thermal impedance. Using this forced air-cooling system IGBT and diode junction temperatures state as 95 °C and 90 °C in steady state condition. This design seems safe according to manufacturer datasheet. Heat sink, and blower fan 3D drawing is shown in Figure 3.21.

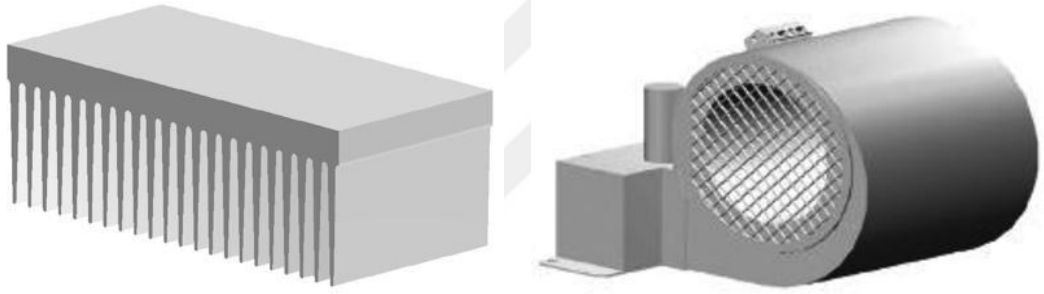

Figure 3.21 Heat sink and blower fan 3D drawing

IGBT placement on the heat sink is given Figure 3.22. and final power stage design top view drawing is given in Figure 3.23.

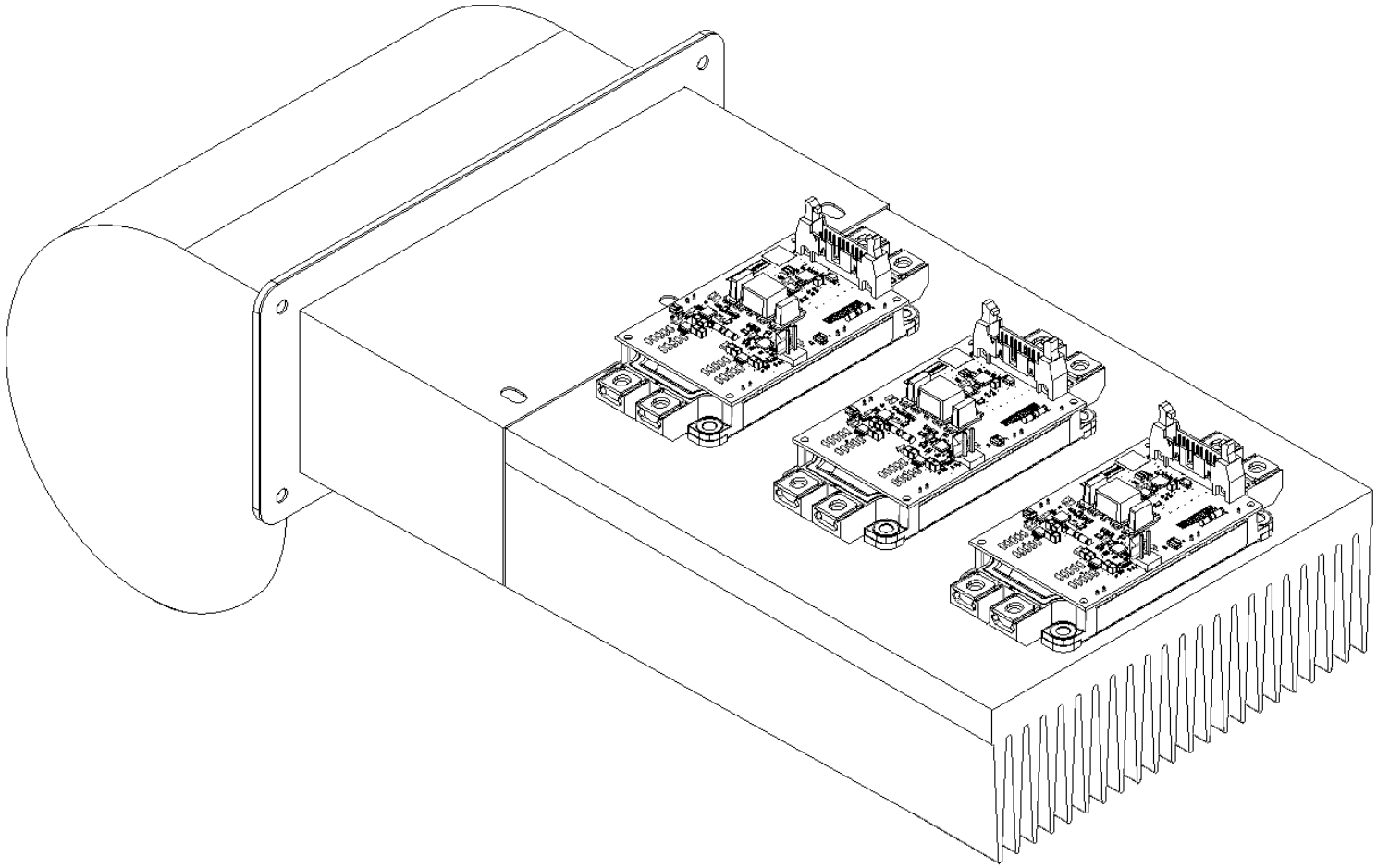

Figure 3.22 IGBT placement on the heat sink

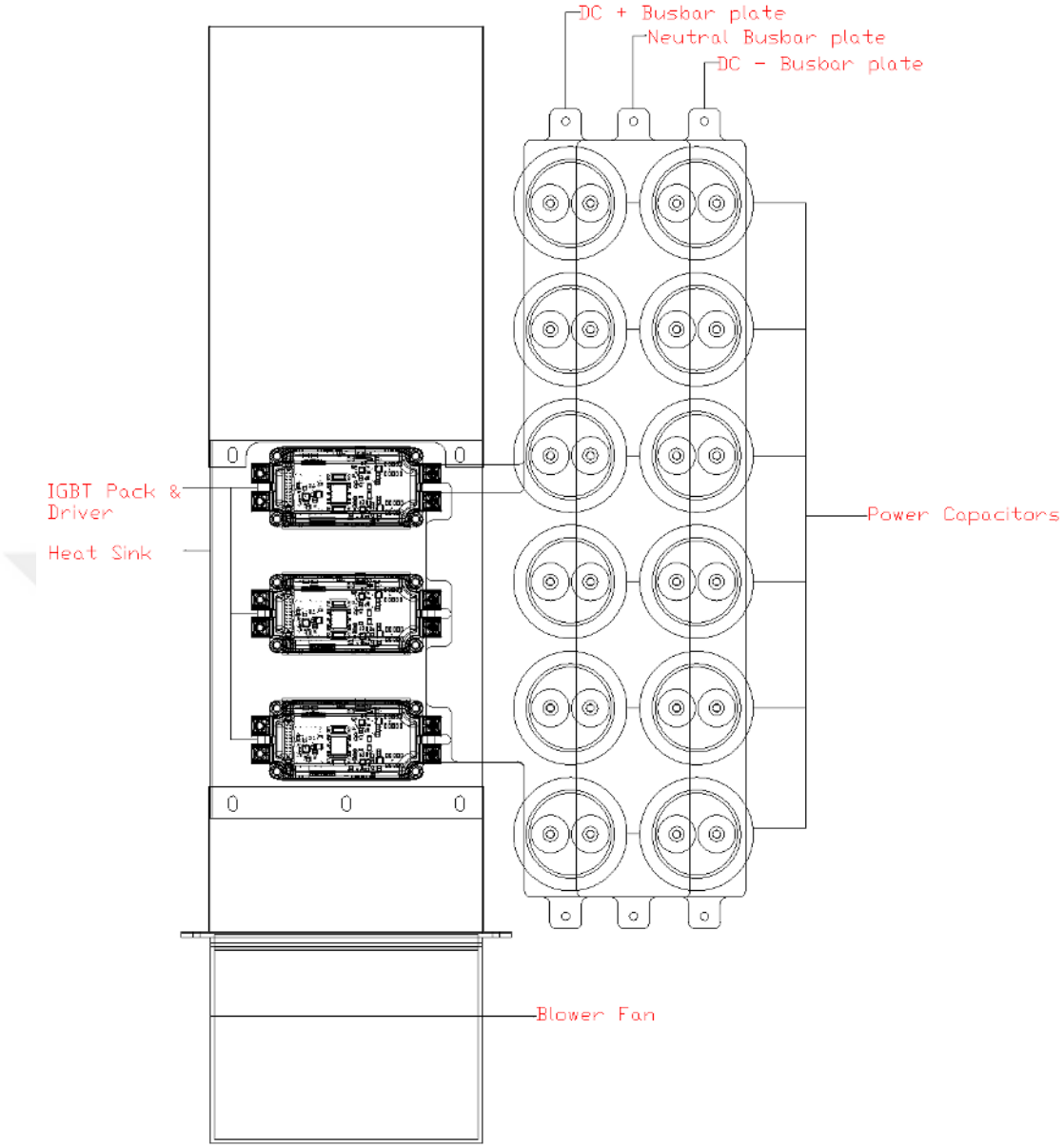

Figure 3.23 Top view of final power stage design

3.3 LCL Filter Design

LCL type filter is a third-order filter and it has a common usage and better performance than L type and LC type filter since compared with other two types filter it has smaller inductance and capacitance value and shows better harmonic attenuation performance. Moreover, the voltage drop across the filter is less than the mentioned two type filters [27]. Three-phase four-wire EQR single phase equivalent circuit diagram with LCL filter is given in Figure 3.24, where subscript x denotes a, b and c phases, subscript 'i'

denotes inverter side, subscript 'g' denotes grid side and subscript 'f' denotes filter. Inverter output voltage V_{ix}, the capacitor voltage V_{cx} and grid voltage at the PCC V_{gx} are related voltage definitions. Inverter side reactors used for high frequency current cancellation therewithal grid side reactor uses as interface between grid and EQR at the fundamental frequency.

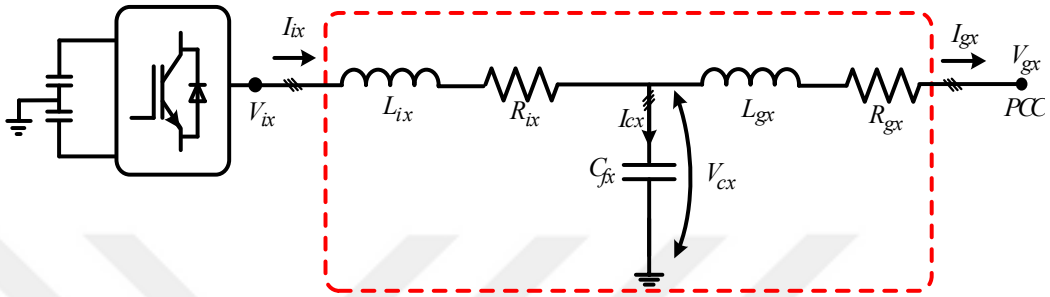

Figure 3.24 Three-Phase Four-Wire EQR single phase equivalent circuit diagram with LCL filter

Filter parameters must be chosen according to the Table 3.13 to prevent over-amplification and switching frequency harmonics effects.

Table 3.13 LCL filter parameter limitation

Parameter	Limitation	Reason
Total Inductance ($L_i + L_g$)	<0.1 (p.u.)	To avoid extreme voltage drop
Reactive power consumed by the capacitor	<5% of rated power	Power factor limit
Resonance frequency	$10w_g \leq w_{res} \leq 0.5w_{sw}$	To prevent the grid from serious resonance problems

where, w_g is the fundamental frequency of the grid, w_{sw} is switching frequency of the system and w_{res} is the resonance frequency of the system which is given in (3.30).

$$w_{res} = \frac{1}{2\pi}\sqrt{\frac{L_i + L_g}{L_i L_g C_f}} \tag{3.30}$$

To analyze LCL filter behavior, frequency response of the filter without any damping may be expressed in (3.31) when internal resistance of the inductors R_i and R_g are neglected.

$$T_{LCL}(s) = \frac{I_g(s)}{V_i(s)} = \frac{1}{L_i L_g C_f s^3 + (L_i + L_g)s} \tag{3.31}$$

According to the Table 3.13, PSCAD/EMTDC analyze and producibility in Turkey, LCL filter parameter selected as: $L_i = 300\ uH$, $L_g = 100\ uH$ *and* $C_f = 100\ uF$.

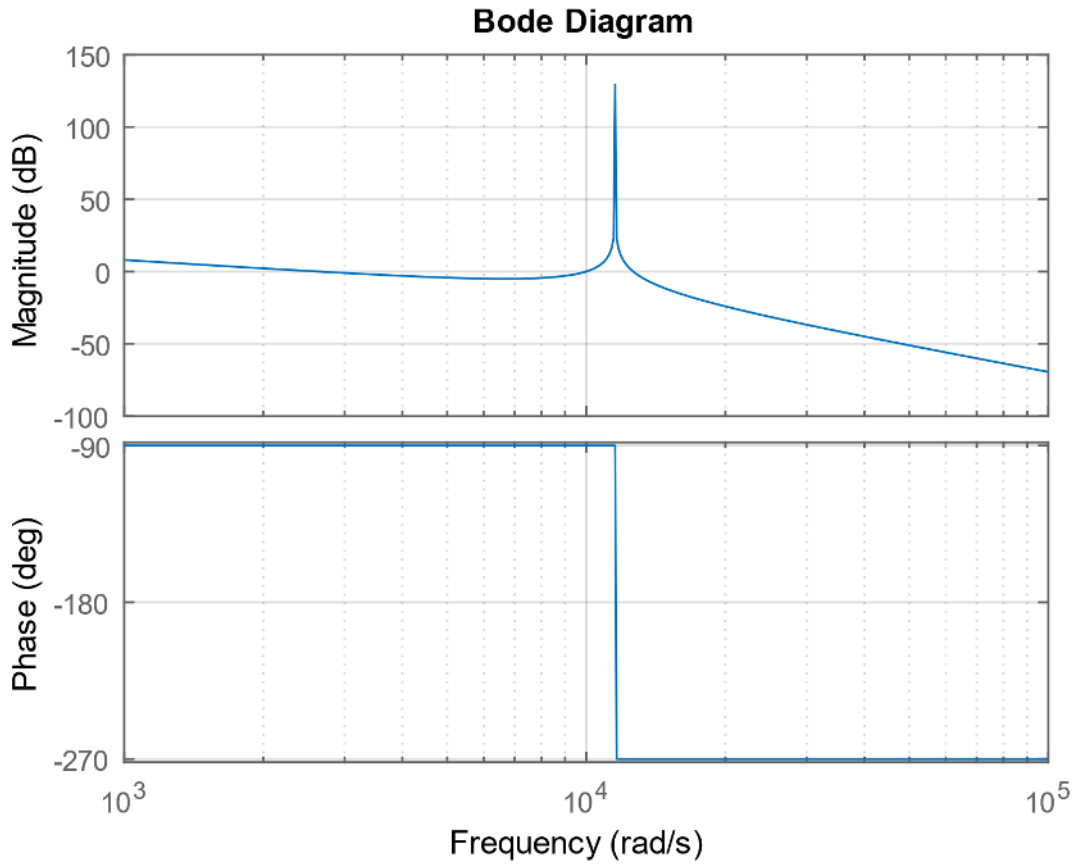

Figure 3.25 Frequency response of the designed LCL type filter

It is clearly seen that resonance frequency is 1837 Hz at the selected filter parameters and for the further values from the resonance frequency there is nearly -60 db/decade attenuation.

High frequency currents and integer multiply of this current pass through the inverter side reactor so inverter side reactor must be produced properly to prevent overheating and saturation problems.

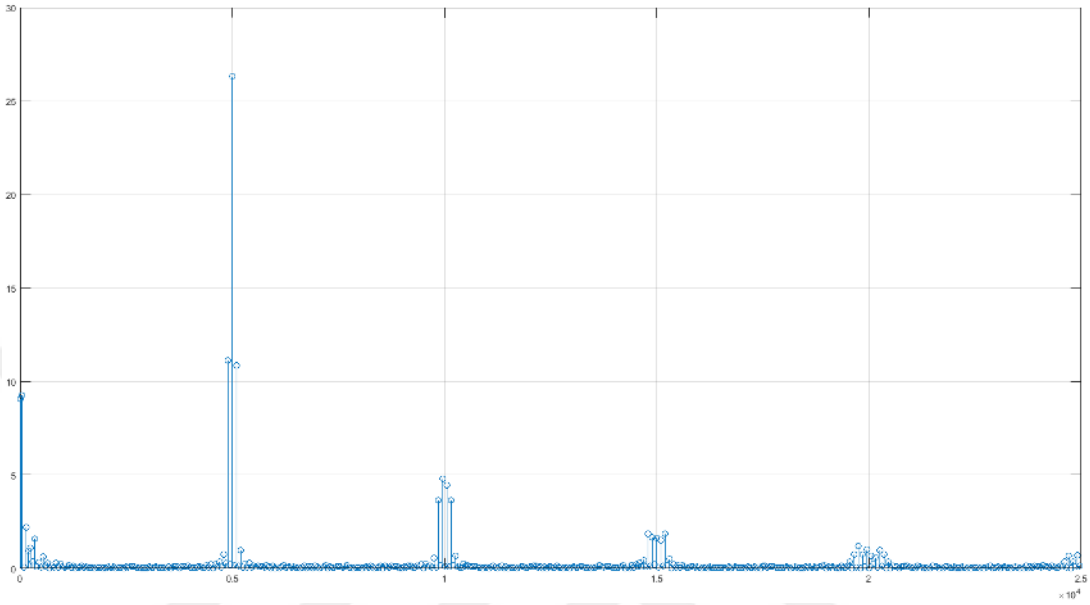

Figure 3.26 Inverter side reactor current spectrum at no-load condition

As shown in Figure 3.26. nearly 27A current will pass through to inverter side reactor at the 5 kHz (switching frequency) also 5A @ 10A kHz, 2.5 @ 15 kHz, 1A @20 kHz and 0.5A @25 kHz current will pass through to inverter side reactor. These values can be reduced with increasing switching frequency as shown in Figure 3.27. As shown in Figure 3.27. high frequency currents shifted to changed switching frequency and integer multiply of the new switching frequency. As an example, 7 kHz switching frequency is selected as a new frequency and examined. It is clearly seen that high frequency currents are reduced to 19A @7kHz, 4A @14kHz and 1.5A @21 kHz. However, it means high losses for the power stage. Producibility of this reactor is proper both frequencies so 5 kHz switching frequency is selected to prevent higher power losses.

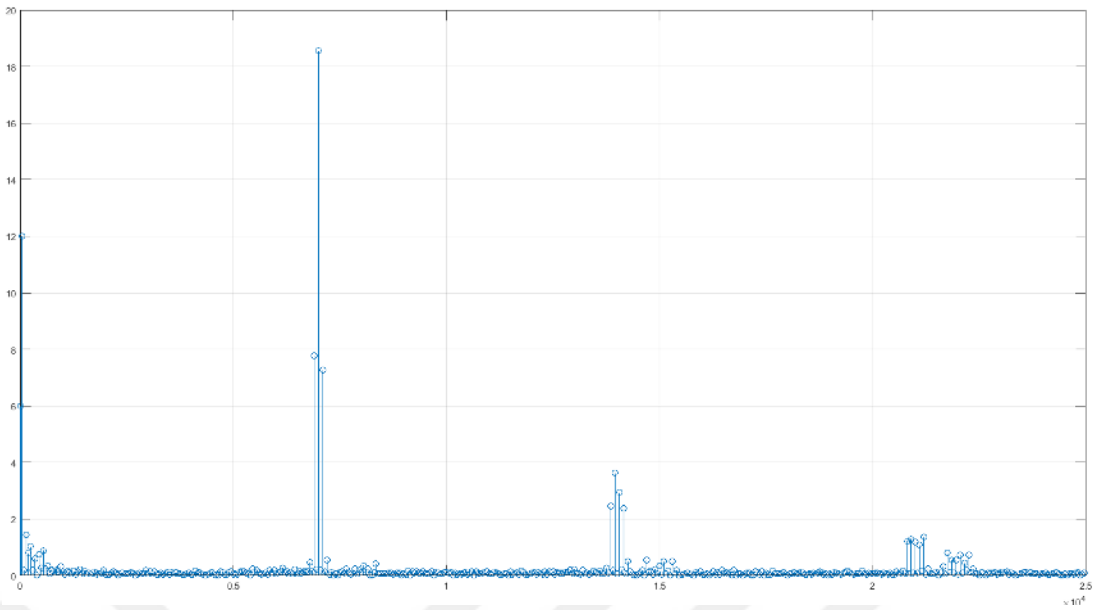

Figure 3.27 Inverter side reactor current spectrum at no-load condition

3.4 EQR Control Card Design

EQR control card has an integrated structure. EQR card reads analog data and peripheral digital inputs and produces suitable switching signal and digital outputs. This card also has a serial interface to communicate HMI (Human Machine Interface) system. EQR control card main power supply is 24 Vdc and isolated power supplies on the card converts this voltage to ±15 Vdc and ± 5Vdc. The other necessary voltage level 3.3 Vdc is produced by linear circuits on the card. This card has 12 digital inputs and 12 digital outputs with this feature, card can be managed and protect EQR panel. EQR control card has two MCU one of them is main MCU and the other one is auxiliary MCU. Main MCU employees processing analog data and control algorithm, driving IGBT switching signals, determination of protection levels, real time RMS calculation, alarm and fault state detection, active and reactive power calculation, PLL algorithm management, transformation and inverse transformation blocks and SPI communication with auxiliary MCU. Auxiliary MCU utilize management of digital inputs and digital outputs, serial communication with HMI and SPI communication with main MCU. General structure of the EQR control card is given in Figure 3.28.

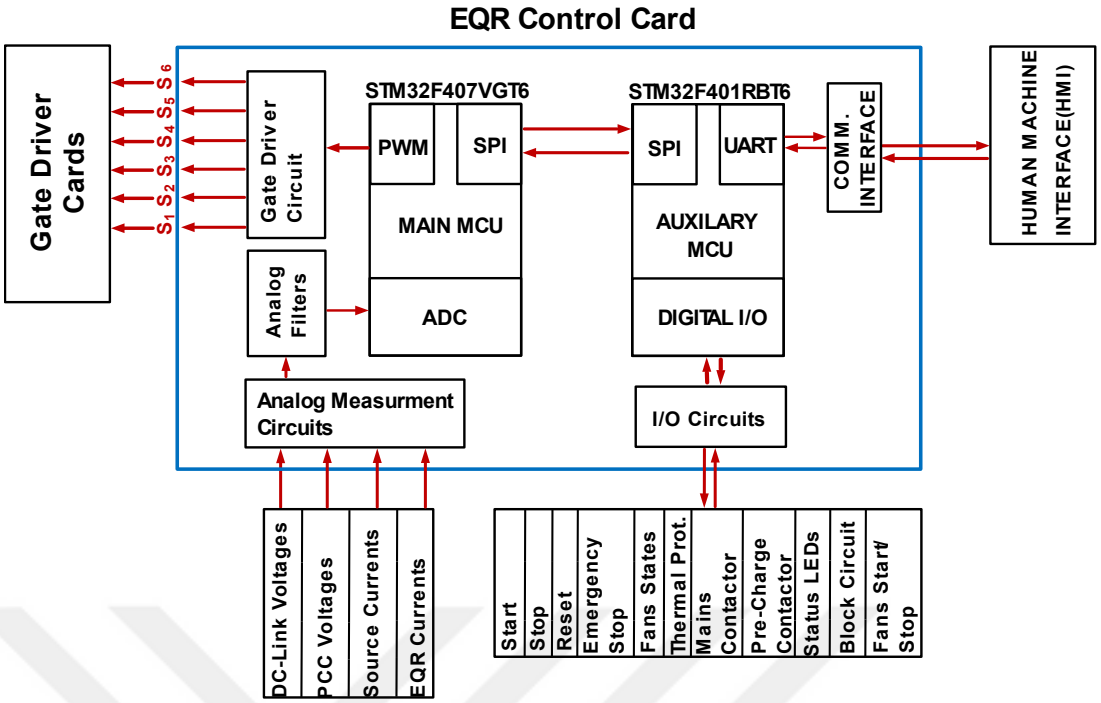

Figure 3.28 EQR control card general structure

Main specification of the designed EQR control card are listed below:

- 18-36 Vdc Power Supply < 20 W
- 12 Digital Inputs
- 12 Digital Outputs
- Current measurement …/5A or …/1A
- DC voltage measurement max. 1000 Vdc
- AC voltage measurement max 360 Vac, PN
- Discrete IGBT driving
- Modbus RTU communication
- SPI communication

General 3D view and produced card are given in Figure 3.29. and Figure 3.30. respectively

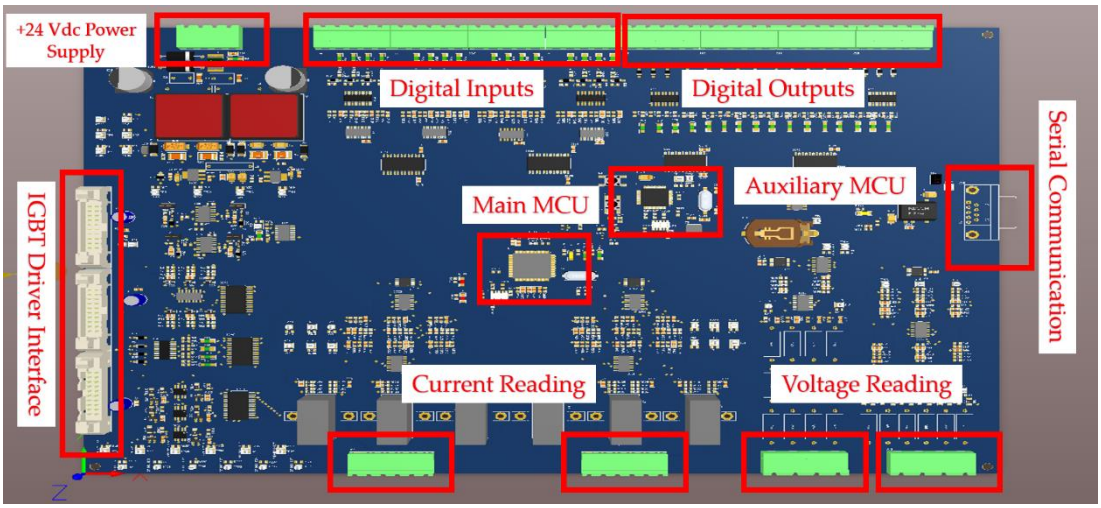

Figure 3.29 3D model of EQR control card

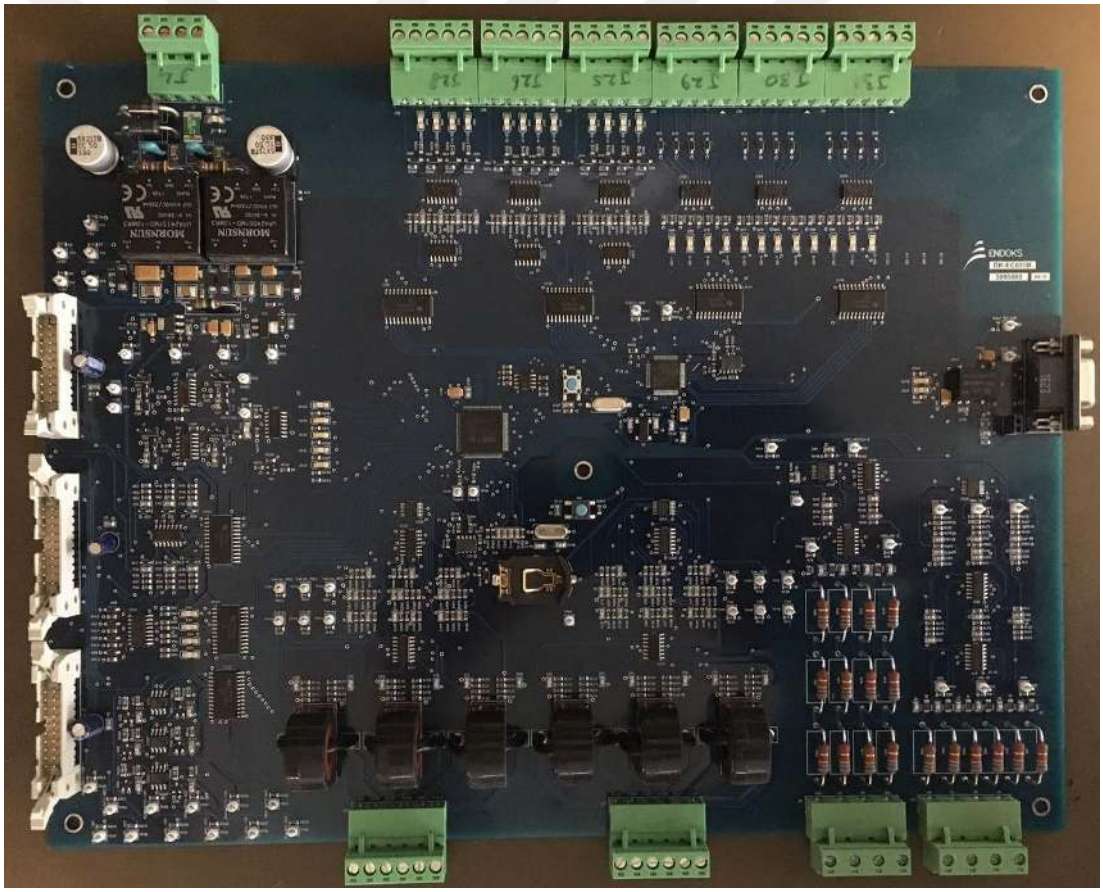

Figure 3.30 Produced EQR control card

STM32F407VGT6 is selected as main MCU since F4 series has more advantage like:

- ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 168 MHz, memory protection unit, 210 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions 210 DMIPS
- 3×12-bit, 2.4 MSPS A/D converters: up to 24 channels and 7.2 MSPS in triple interleaved mode
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32- bit timers up to 168 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input and low cost etc.
- Up to 140 I/O ports with interrupt capability
  - Up to 136 fast I/Os up to 84 MHz
  - Up to 138 5 V-tolerant I/O s
- Up to 15 communication interfaces
  - Up to 3 × I2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/2 UARTs (10.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 3 SPIs (42 Mbits/s), 2 with muxed full-duplex I2S to achieve audio class accuracy via internal audio PLL or external clock
  - 2 × CAN interfaces (2.0B Active) – SDIO interface

Sampling frequency is selected as 25 kHz at this sampling frequency each current and voltage variable are sampled every 40 μs respectively and calculations are made in the control blocks every 40 μs. Finally, switching signals are produced. With this way PWM signals are updated each sampling period according to the new variable and calculations. According to these information flowcharts of the main MCU is derived as the Figure 3.31.

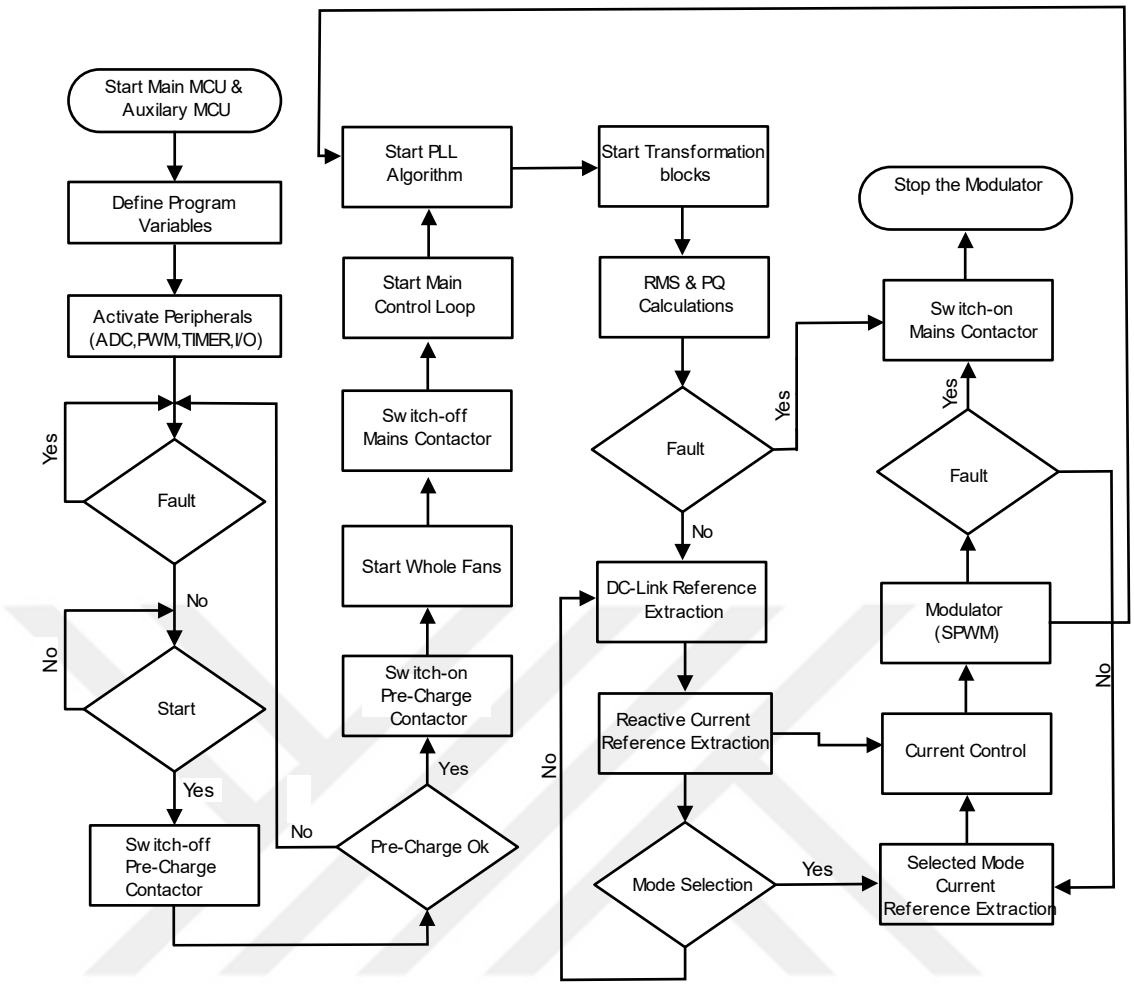

Figure 3.31 EQR control system flowchart

As seen from the EQR control system flowchart after the system initialize program variables and peripherals activated. If there is no error pre-charge state starts up to peak value of the PCC voltage than panel fans start to prevent overheating condition during switching. These states are pre-condition to close main contactor before the main control loop. PLL algorithm must work properly since it is more important for accuracy of the transformation block. RMS and PQ calculation blocks follows mains to protect EQR any overcurrent or overvoltage case. If there is an error occurs mains contactor switches on to protect EQR. Control blocks produces reference voltages for modulation block and switching signals are produced according to these references block after the mode selection. If there are any fault at the switching state mains contactor are switches on and switching signals are stopped.

3.5 Power Stage Components

The details of the EQR power stage and general connection scheme is given in Figure 3.32 EQR is connected to the mains via 200 A NH 00 fuses and 200 kW contactor.

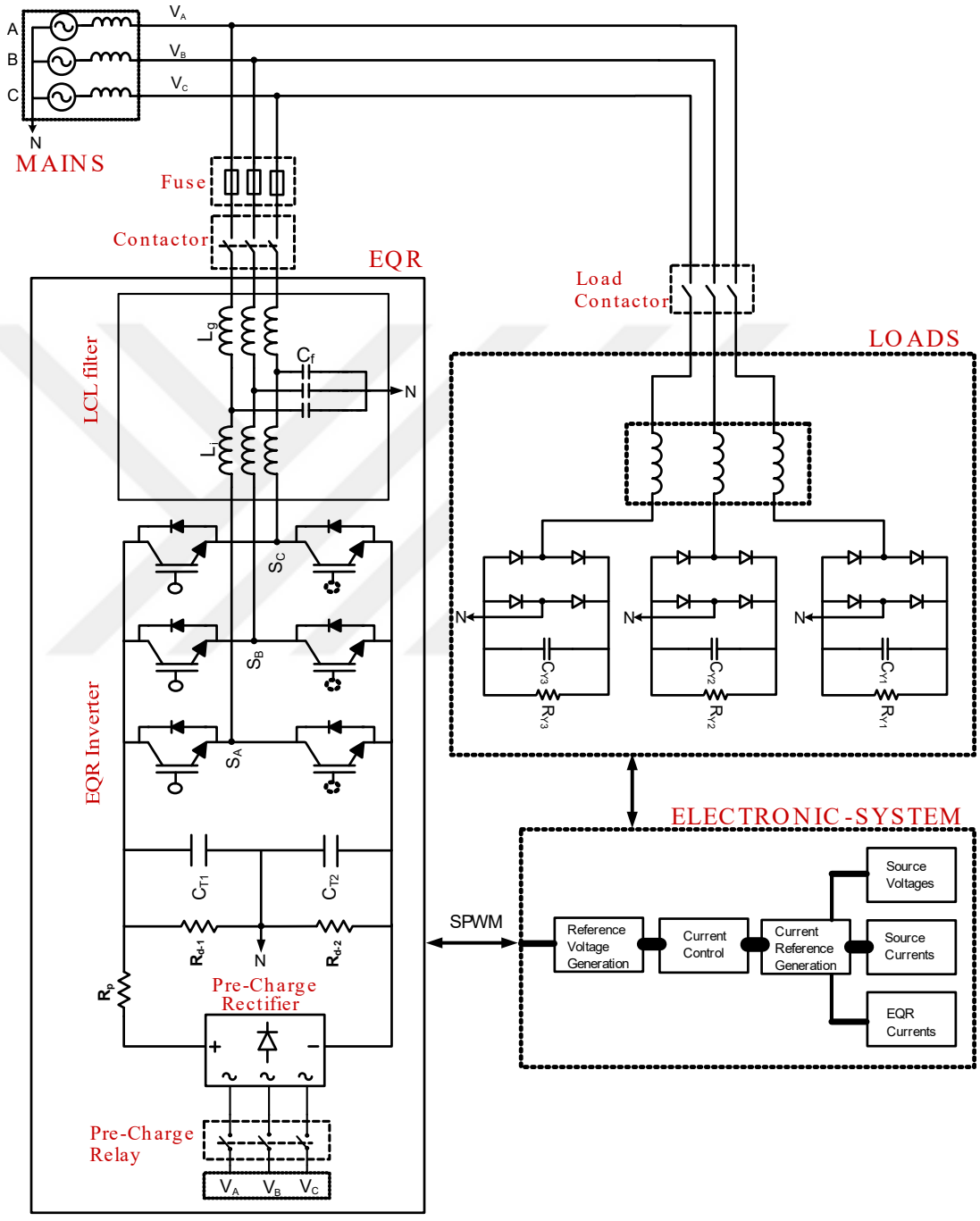

Figure 3.32 EQR general structure

Contactor employees commissioning of the EQR and two level three-phase four-wire voltage source inverter topology with LCL filter is used to create main structure where C_{T1} and C_{T2} demonstrates split capacitors, R_p demonstrates pre-charge resistor which is $2x110\Omega$, R_{d-1} and R_{d-2} are discharge resistors and their equivalent values are ~4kΩ. Final prototype EQR is build up as shown in Figure 3.33.

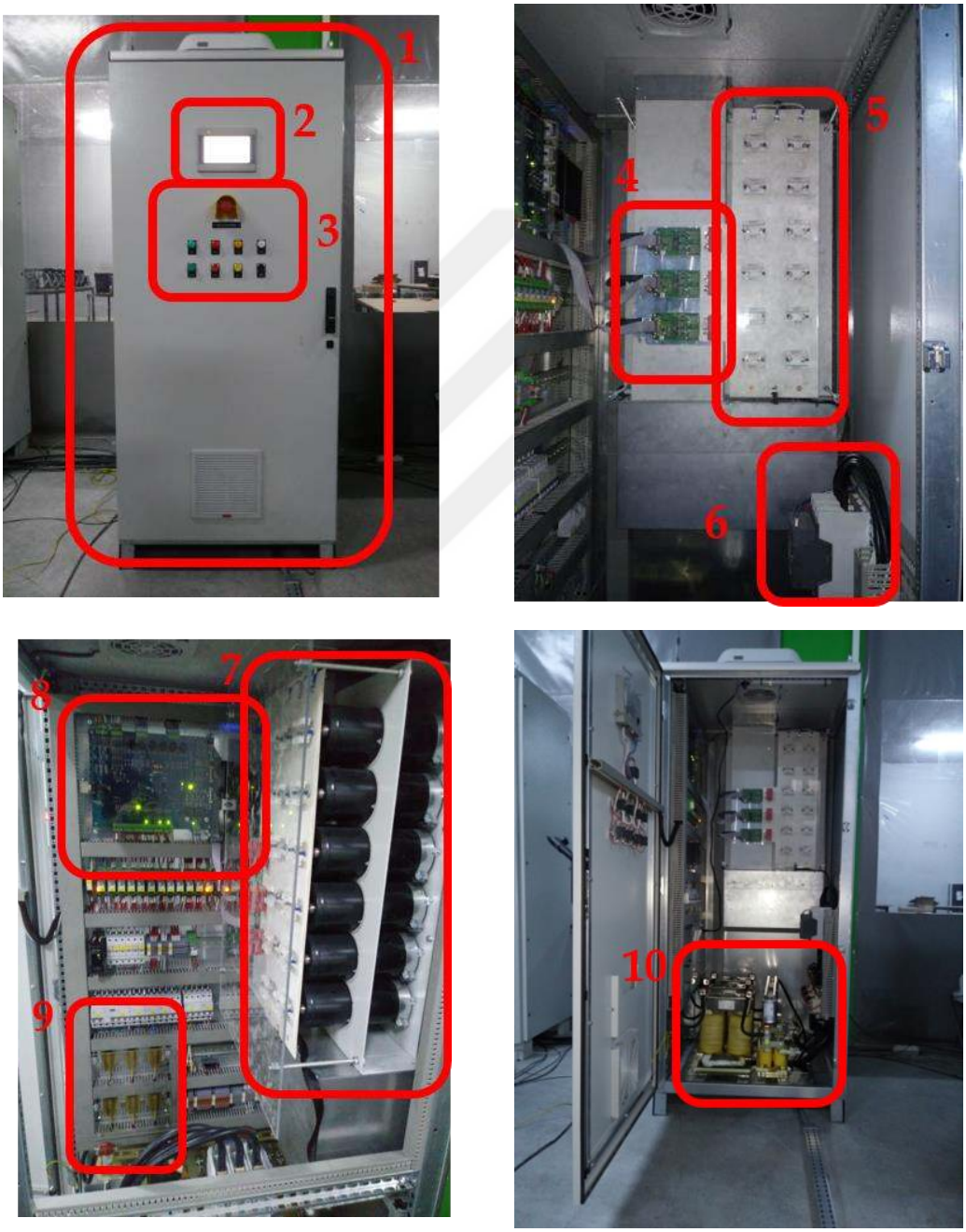

Figure 3.33 EQR general view

Figure 3.31 shows general view and components of the designed EQR. Numbered components can be described as:

1. EQR control panel
2. Human Machine Interface (HMI)
3. Control buttons and LEDs
4. IGBTs and drivers
5. Laminated busbar and discharge resistors
6. Mains contactor
7. DC-Link Capacitors
8. EQR control card
9. Pre-charge resistors
10. LCL filter

CHAPTER 4

FIELD TESTS & RESULTS

4.1 Introduction

A ± 100 kVAR EQR is designed according to the specifications given Chapter 3. The developed system is applied to AKDENİZ EDAŞ #181150 Distribution station to regulate power quality at the PCC is given in Figure 4.1.

Figure 4.1 Distribution Station of AKDENIZ EDAS

In order to verify theoretical results and PSCAD/EMTDC analyzes, implemented system has been applied to AKDENİZ EDAŞ distribution transformer given in Figure 4.2. During the test different scenario have been applied to EQR device to

analyze compensation capability of the EQR. Whole control algorithm given in Chapter 2 have been tested and related results are given in this section.

Figure 4.2 Distribution Transformer of AKDENIZ EDAS DS

Not only field tests are observed but also some properties are verified in the laboratory using experiment setup. The records have been obtained by measuring apparatus which are listed in Appendix C. Measurements have been taken from the main distribution panel of distribution station is given in Figure 4.3. Two different power quality analyzer and one 200 MHz oscilloscope have been used to take measurement results. Reactive power compensation capability of the device has been tested in the laboratory since in the field reactive power was very low and corresponding results are recorded using Chauvin Arnoux 8335 Portable Power & Quality Analyzer. To analyze reactive power compensation capability of the EQR 100 kVAR three phase capacitive load bank have been used. Dc-link regulation and neutral current compensation capabilities of the EQR have been recorded using TEKTRONIX MDO3024 – 200 MHz oscilloscope. These measurements have been recorded in the laboratory case since extreme scenarios have been applied to the device. Fifth and seventh harmonic current

compensation capability of the device has been tested used three phase rectifier circuit in the laboratory. Third harmonic compensation capability and load balancing capability of the device is tested in the field and related results have been recorded using HIOKI PW3198 Power Quality Analyzer.

Figure 4.3 Main Distribution Panel of AKDENIZ EDAS DS

The implemented system is shown in Figure 4.4. This is also called as EQR control panel. This panel covers whole system like EQR control card, LCL filter, dc-link capacitors, laminated busbar, IGBTs, snubber capacitors, mechanical relays, fuses, MCBs, contactor and wirings. This panel has control functions of the device to start and stop the system. Using panel buttons or HMI panel can be commissioned or stopped. Voltages, currents, reactive and active powers for source and load sides are also observed using HMI panel.

Figure 4.4 EQR Control Panel

4.2 DC-Link Regulation Performance

DC-link voltages and balance algorithm is measured using TEKTRONIX MDO3024 – 200 MHz oscilloscope and PINTEK DP100 High Voltage Probe. Total dc-link voltage is nearly 715 Vdc when the system has run. Total dc-link voltage is given in Figure 4.5. To check voltage balance algorithm another measurement is taken between plus and neutral conductor of the split capacitors and related measurement result is given Figure 4.6.

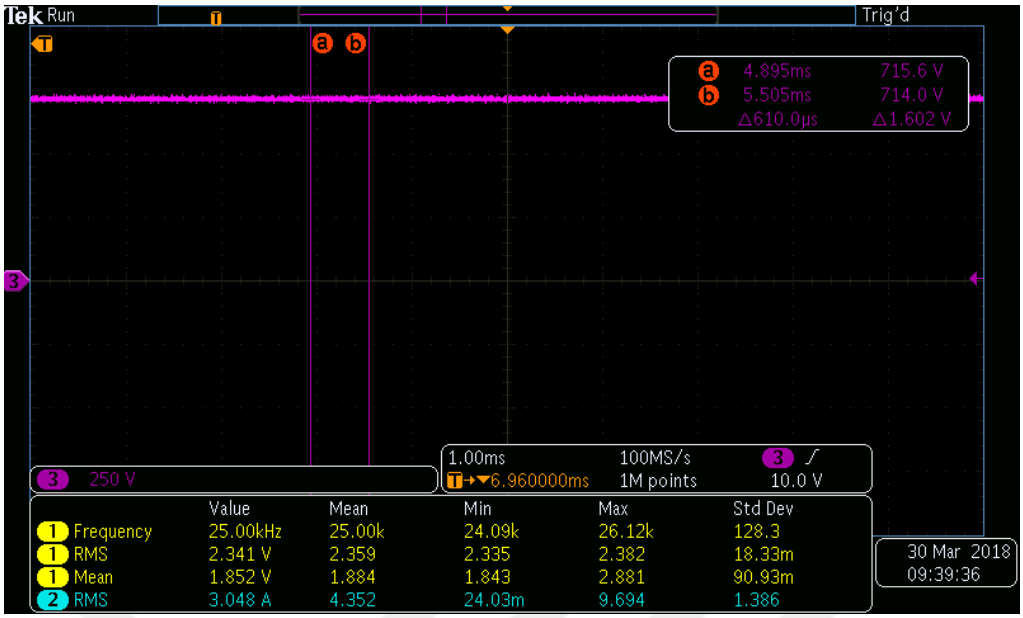

Figure 4.5 Total DC-Link Voltage

Taken value is nearly 356 Vdc and it means that balancing algorithm works well. To prevent any circulating current problems voltage balance between lower and upper capacitor is very important. This unbalance condition also causes excessive neutral current problems.

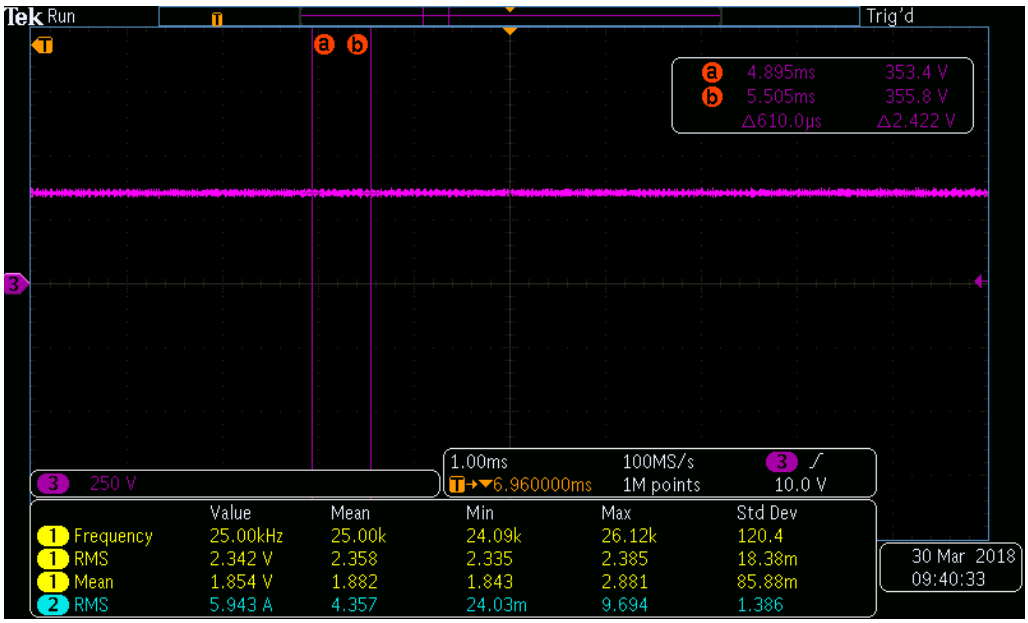

Figure 4.6 DC-Link Voltage Between Terminals

4.3 Reactive Power Compensation

Reactive power compensation performance is measured from inductive side and 80 kVAR capacitive load is trying to be compensated. To measure compensation capability of the EQR three phase 100 kVAR capacitive load bank is used in the laboratory given Figure 4.7.

Figure 4.7 100 kVAR Three Phase Capacitive Load Bank

Because of the minimum sampling period of the Chauvin Arnoux 8335 Portable Power & Quality Analyzer is 1 sn, response time of the EQR hasn't been observed clearly. However, system has been response reactive power change at the PCC as seen in Figure 4.8.

Relative performance graph is given in Figure 4.8. Section 1 given in Figure 4.8. demonstrates before reactive power compensation when reactive power compensation starts the reactive power at the PCC is reduce dramatically can be seen in Figure 4.8. section 2 for three phases.

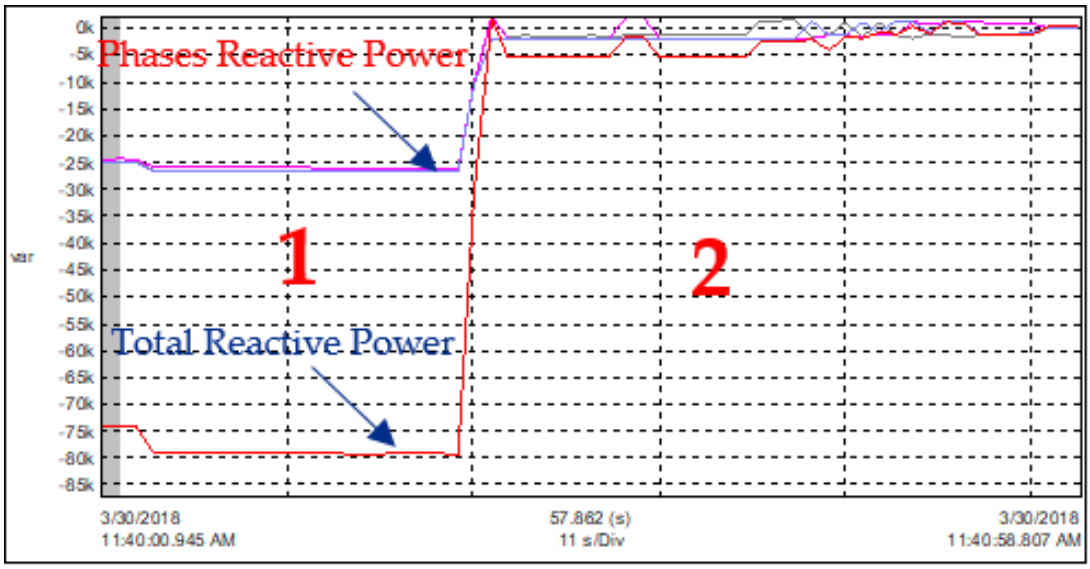

Figure 4.8 Reactive Power Compensation Performance

4.4 Third Harmonic Compensation Capability

Third harmonic compensation capabilities of the EQR has been tested in the field since in the laboratory used three phase rectifier circuit produces only positive and negative sequence harmonics.

Third harmonic current compensation capability is measured using HIOKI PW3198 Power Quality Analyzer. For the phase A 4A third harmonic current, for phase B 4A third harmonic current and for phase C 9A third harmonic current is reduced to 1A, 2A and 4A respectively after third harmonic compensation mode enable as seen in Figure 4.9-4.14.

Third harmonic compensation performance of the device can be seen low but for this topology third harmonic currents circulated on dc-link capacitors, so this is very hard to compensate third harmonic current for this type systems. Nevertheless, this performance is acceptable for distribution systems since for the worst case there is nearly 60% attenuation for third harmonic currents.

Figure 4.9 Phase A 3rd harmonic Current Before Compensation

Figure 4.10 Phase A 3rd harmonic Current After Compensation

Figure 4.11 Phase B 3rd harmonic Current Before Compensation

Figure 4.12 Phase B 3rd harmonic Current After Compensation

Figure 4.13 Phase C 3rd harmonic Current Before Compensation

Figure 4.14 Phase C 3rd harmonic Current After Compensation

4.5 Fifth and Seventh Harmonic Compensation Capability

To produce fifth and seventh harmonic prototype load is used in the laboratory related circuit diagram is given in Figure 4.15 and implemented circuit is given in Figure 4.16.

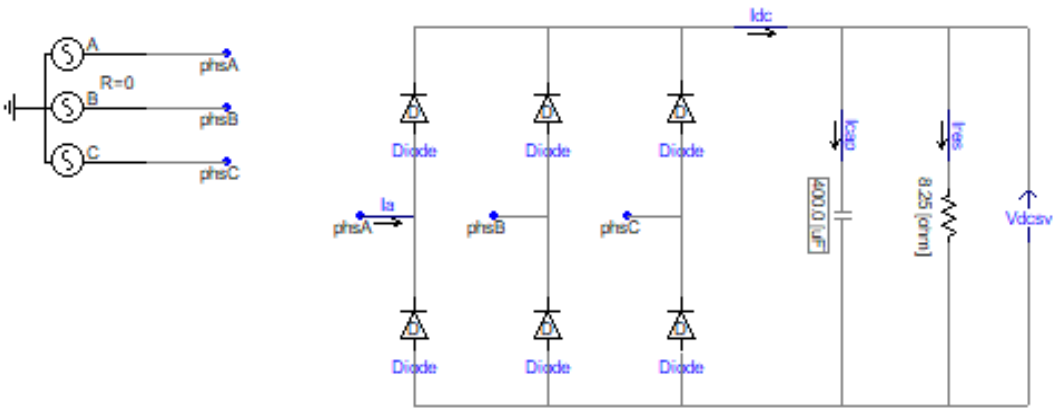

Figure 4.15 Three Phase Rectifier Circuit Diagram

400 uF capacitor and 8.25 Ω have been used in the three-phase rectifier through a three-phase variac to produce 8.5 A fifth harmonic and 3 A seventh harmonic currents.

Figure 4.16 Three Phase Rectifier Implemented Circuit

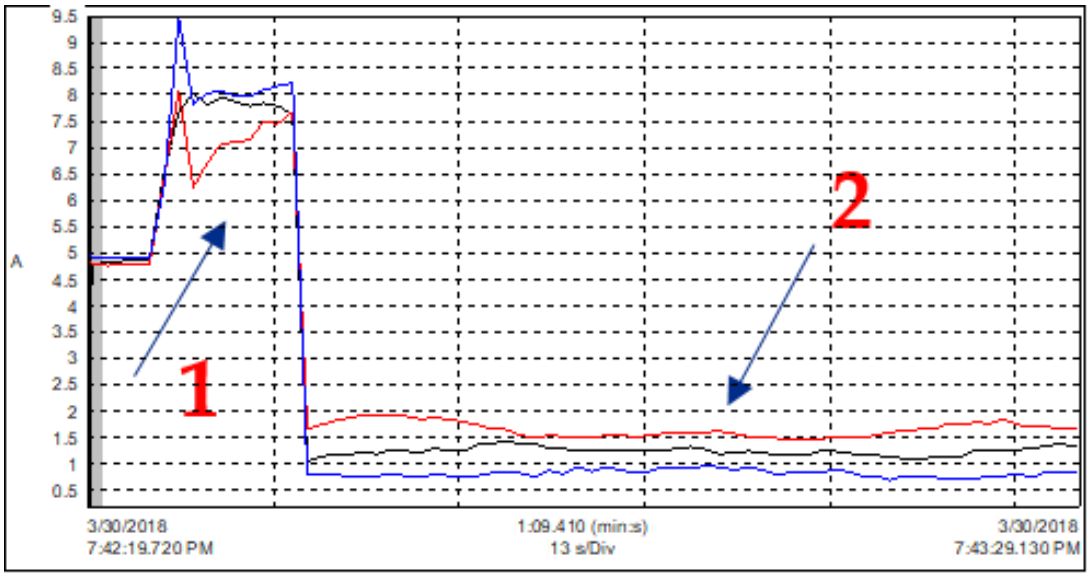

Figure 4.17 Fifth Harmonic Current Compensation Capability

To produce mentioned harmonics variac has been adjusted to 300 V phase-to-phase voltage. Main reason of this adjustment is resistors power loss. Three phase rectifier circuit produces nearly 8.5 A fifth harmonic and 3 A seventh harmonic when EQR is run with no mode selection. After fifth and seventh harmonic mode selection fifth harmonic is reduced nearly 1 A and seventh harmonic current is reduced 0.5 A. As seen in Figure 4.17 section 2 and Figure 4.18 section 2 respectively. These results are satisfying for the EQR device since unwanted fifth and seventh harmonic currents at the PCC have been compensated completely.

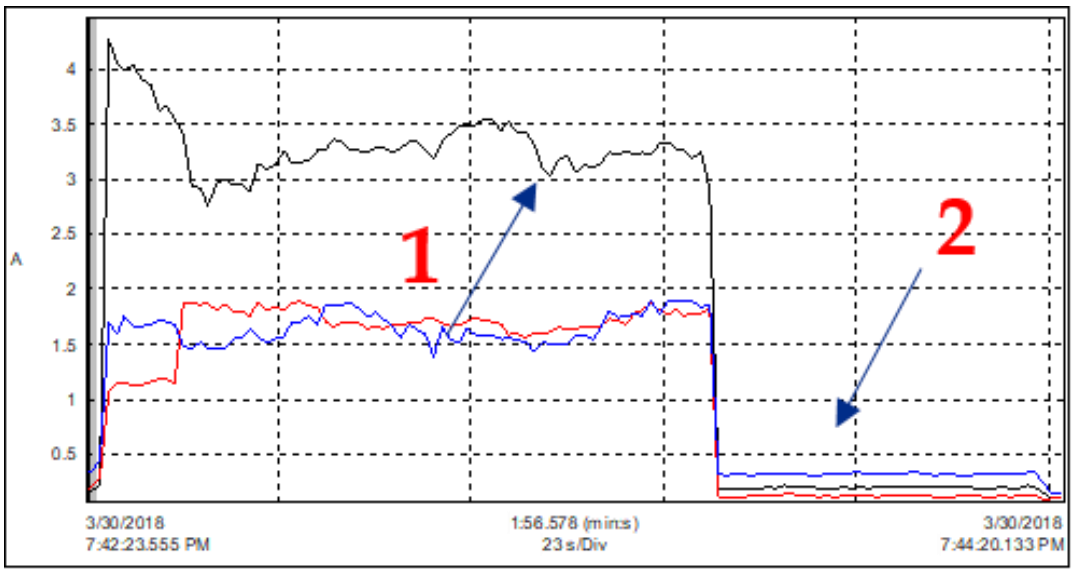

Figure 4.18 Seventh Harmonic Current Compensation Capability

4.6 Unbalanced Current Compensation Capability

Unbalanced current compensation capability of the EQR device has been tested both laboratory and field. In this section only, field test results are shared since three phases are observed simultaneously only field test equipment. Unbalanced current compensation capacity has been measured using HIOKI PW3198 Power Quality Analyzer and source currents are unbalanced up until load balancing mode selection as shown in Figure 4.19.

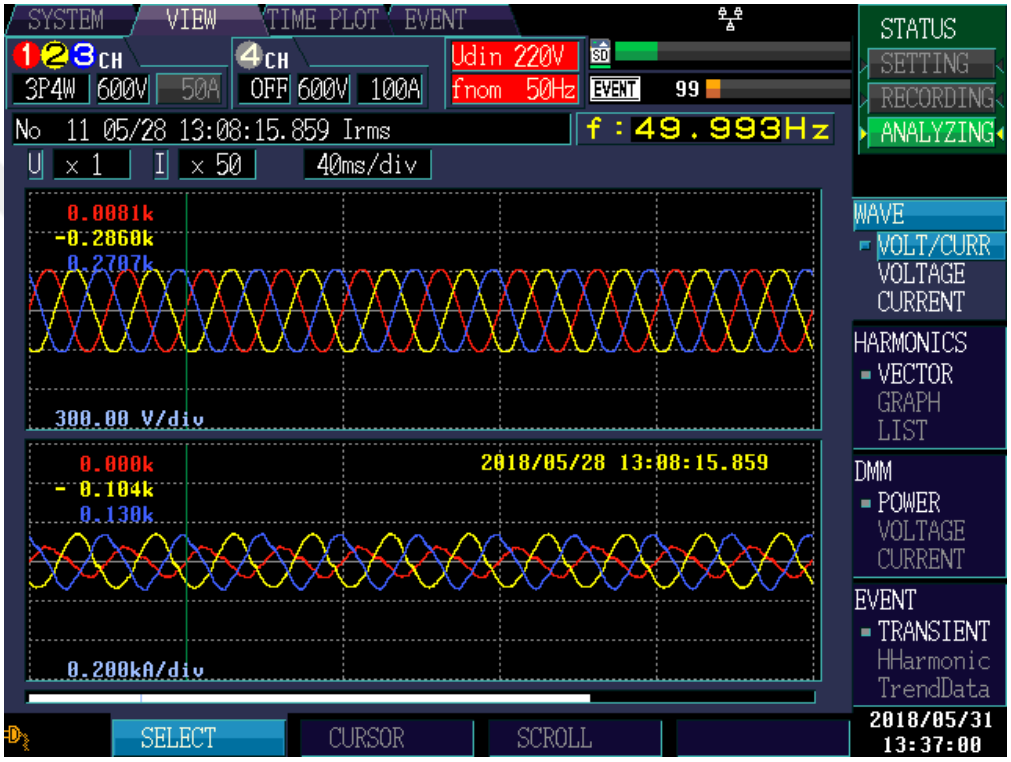

Figure 4.19 Source Currents Before Unbalance Compensation

Before the load balancing mode selection phase currents have been 90 A, 168 A and 135 A peak value for phase A, B and C respectively. After mode selection these currents balanced around 133 A peak values as shown in Figure 4.20. since both negative sequence and zero sequence compensation control blocks have been activated with the unbalanced current compensation mode and only positive sequence current are observed with this compensation. This compensation seems to be satisfactory and it can be selected as proper for this application.

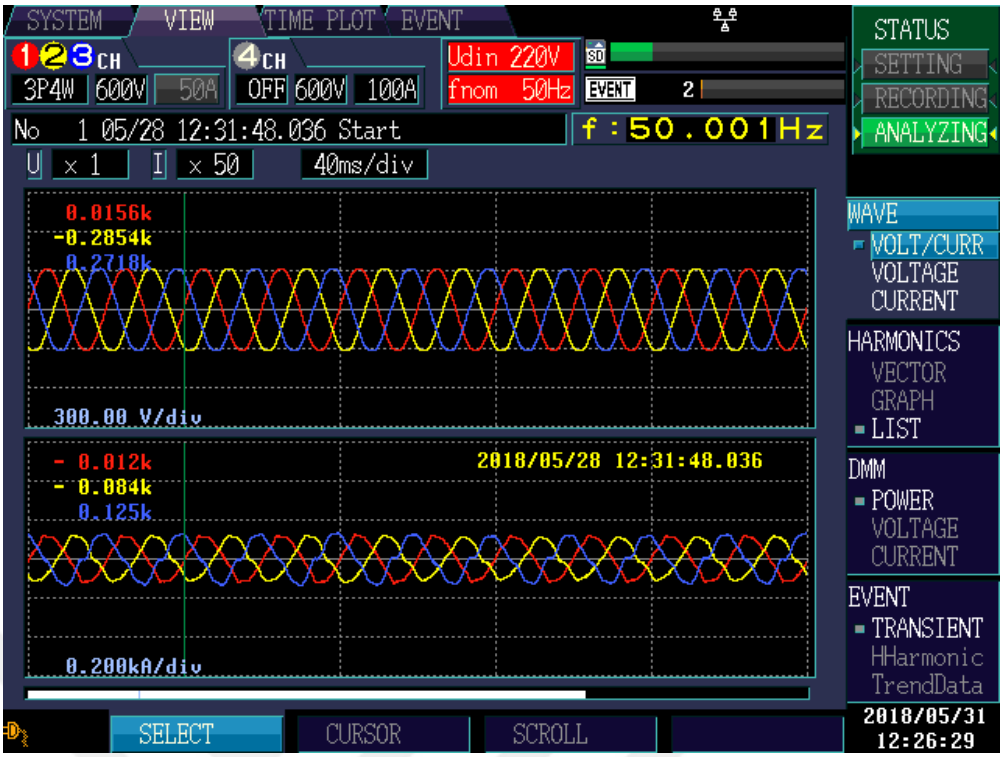

Figure 4.20 Source Currents After Unbalance Compensation

4.7 Neutral Current Compensation Capability

Neutral current compensation capability of the EQR device has been tested in the laboratory. Neutral current compensation capacity has been measured using TEKTRONIX MDO3024 – 200 MHz oscilloscope.

The neutral current capacity of the EQR has been tested using unbalance loads using single phase 5 kVAR, 7.5 kVAR and 12.5 kVAR capacitive loads. When the loads are unbalanced related waveform about mains neutral currents have been observed as shown in Figure 4.21.

Before the neutral current compensation, mains neutral current is measured as 29.16 A. Then neutral current compensation mode has been selected and with this selection zero sequence compensation, and third harmonic compensation mode have been activated simultaneously by the control algorithm and this value have been reduced to 5.142 A. This value seems to be satisfactory and applicable for EQR application since neutral currents is attenuated nearly 82.37%.

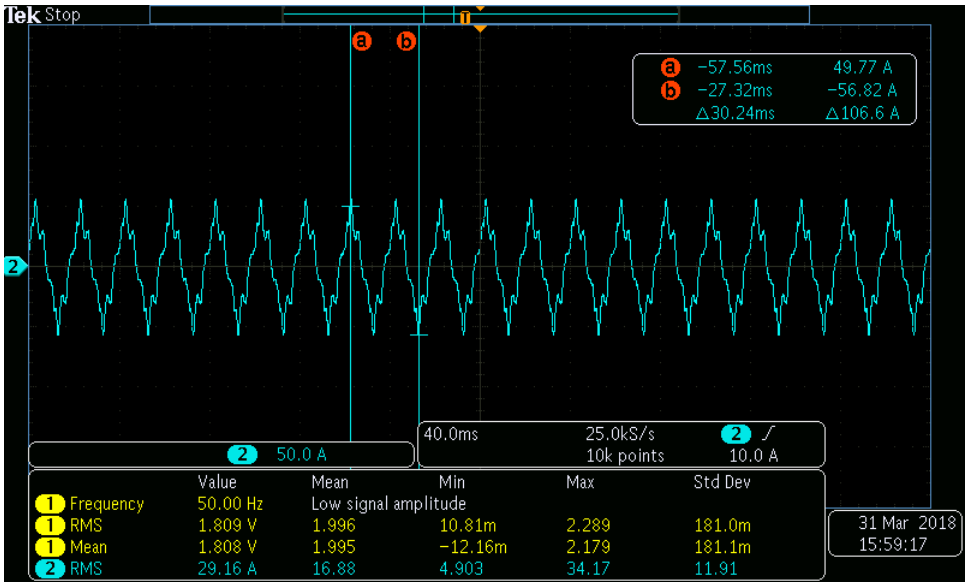

Figure 4.21 Neutral Current Before Compensation

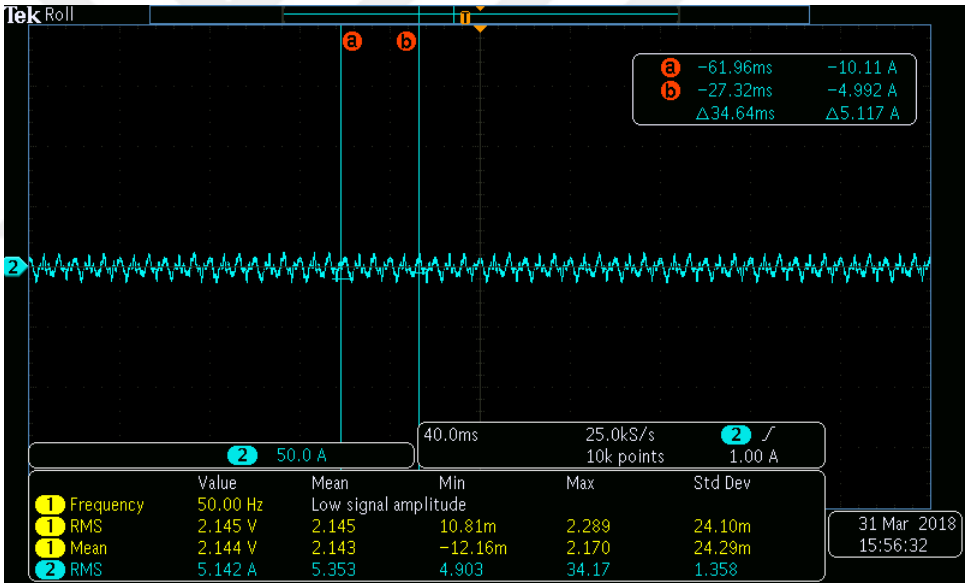

Figure 4.22 Neutral Current After Compensation

CHAPTER 5

CONCLUSION

In this paper, three-phase four-wire neutral point clamped VSI-based EQR operated in parallel and connected to LV bus between 400 kVA 400V %4 uk distribution type transformer and loads through LCL filter. System proposed solution to typical distribution transformer problems. A case study has been carried out for AKDENİZ EDAS 181450 DS which was subject to the reactive power compensation, low order harmonic mitigation, unbalance and neutral current compensation.

Reactive power flow and harmonic currents lead to power losses on the distribution transformers also these losses cause to thermal overloading especially in summer. Main power quality problems and the necessity of the project are mentioned in Chapter 1. There are many Active Filter and STATCOM works in the literature and these are capable of reactive power compensation, harmonic mitigation and load balancing. However, in this thesis mentioned problems are solved locally and using selective manner to reduce cost of the device. Also, power losses of the device are reduced with reducing switching frequency of the IGBTs.

Many control algorithms have been searched and compared to extract reference currents to control the system. Finally, synchronous reference frame-based theory and derivative of this theory MSRF and DSRF have been selected to extract reference currents since ease of implementation and applicable for real time systems. There are many circuit topologies in the literature about three-phase four-wire inverter systems. To reduce cost and ease of implementation neutral point clamper 2-level topology is selected in this work. Although design and implementation of PR controller is not easy, third harmonic current compensation is done by using PR controller since at the tuned frequency it allows to selective harmonic elimination. The other harmonic currents unbalanced current and neutral current are controlled by using PI controller. The

general control scheme of EQR is enabled to selective control for chosen problems. Whole control algorithms are tested in the PSCAD/EMTDC environment and related results are shared. P and I constant of the controllers, ramp block and modulation block are selected and tested according to simulation work for the system. Open loops and closed loops modulation strategies are searched and some of them are explained in Chapter 2. Due to adequate performance SPWM is selected and used.

Design specifications and design of power stage are explained in the Chapter 3. According to the field measurement results EQR design criteria are determined. Extreme conditions are taken into account for this determination. Suitable power semiconductors, dc-link capacitor, pre-charge and discharge circuit, laminated busbar, snubber capacitor and cooling unit is selected and designed to create EQR power stage. Due to insufficient attenuation for the current ripple caused by the PWM voltage L type supply filter does not used in this work. Properly designed, the LCL filter provides a much better suppression for the modulation frequency current ripple compared to the L type supply filter so LCL supply filter is used instead of L type filter in this work.

To control EQR power stage and panel control card is designed. The developed control card has an integrated structure so there is no need rack structure. Used two STMFx microcontrollers accomplish control, protection, communication and firing missions.

Field and laboratory test results are shared in the Chapter 4. Dc-link regulation performance and neutral current compensation capability is tested using TEKTRONIX MDO3024 – 200 MHz oscilloscope. Reactive power compensation performance, five and seven harmonic current compensation performances are tested using Chauvin Arnoux 8335 Portable Power & Quality Analyzer. Unbalanced current compensation capability and third harmonic current compensation performance is measured using HIOKI PW3198 Power Quality Analyzer.

In this research work, compensation performance of EQR is adequate for mentioned problems except third harmonic compensation. As a future work third harmonic

compensation capability of the device will be modified. Another future work can be the modification of the adaptive control mode selection instead of selective mode selection.

REFERENCES

[1] Rohani, A., Joorabian, M., & Rahimi, S. (2014, May). Power quality improvement in three-phase four-wire distribution systems by DSTATCOM and using adaptive hysteresis band current controller. In Electrical Engineering (ICEE), 2014 22nd Iranian Conference on (pp. 616-621). IEEE.

[2] Kant, K., Arya, S. R., & Singh, B. (2015, December). Current sensorless control algorithm of DSTATCOM for power quality improvement. In India Conference (INDICON), 2015 Annual IEEE (pp. 1-5). IEEE.

[3] Singh, M., & Tiwari, V. (2009). Modeling analysis and solution of Power Quality Problems. doi: http://eeeic. org/proc/papers/50. pdf.

[4] Gao, M., & Awodele, K. (2015, September). Investigation of power electronics solutions to power quality problems in distribution networks. In AFRICON, 2015 (pp. 1-6). IEEE.

[5] Bose, B. K. (1992). Power electronics-a technology review. Proceedings of the IEEE, **80(8)**, 1303-1334.

[6] Akagi, H. (1996). New trends in active filters for power conditioning. IEEE transactions on industry applications, **32(6)**, 1312-1322.

[7] Fujita, H., & Akagi, H. (1991). A practical approach to harmonic compensation in power systems-series connection of passive and active filters. IEEE Transactions on industry applications, **27(6)**, 1020-1025.

[8] Peng, F. Z., Akagi, H., & Nabae, A. (1990). A new approach to harmonic compensation in power systems-a combined system of shunt passive and series active filters. IEEE Transactions on Industry Applications, **26(6)**, 983-990.

[9] Chen, L., & von Jouanne, A. (2001). A comparison and assessment of hybrid filter topologies and control algorithms. In Power Electronics Specialists

Conference, 2001. PESC. 2001 IEEE 32nd Annual (**Vol. 2**, pp. 565-570). IEEE.

[10] Peng, F. Z., Akagi, H., & Nabae, A. (1989, October). Compensation characteristics of the combined system of shunt passive and series active filters. In Industry Applications Society Annual Meeting, 1989., Conference Record of the 1989 IEEE(pp. 959-966). IEEE.

[11] Salmeron, P., & Litran, S. P. (2010). A control strategy for hybrid power filter to compensate four-wires three-phase systems. IEEE Transactions on Power Electronics, **25(7)**, 1923-1931.

[12] Salmeron, P., & Litran, S. P. (2010). Improvement of the electric power quality using series active and shunt passive filters. IEEE transactions on power delivery, **25(2)**, 1058-1067.

[13] Dai, N. Y., Wong, M. C., & Han, Y. D. (2007). A generalized 3D pulse width modulator for multi-level voltage source inverters in three-phase four-wire power systems (Doctoral dissertation, Ph. D. dissertation, Electrical and Electronics Engineering of University of Macau, Macau SAR).

[14] IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, 2014, IEEE Standard 519-2014

[15] IEEE Recommended Practice on Monitoring Electric Power Quality, 1995, IEEE Standard 1159-1995

[16] Arrillaga, J., Watson, N. R., & Chen, S. (2000). Power system quality assessment (pp. 0-471). New York: Wiley.

[17] Conroy, E. (2001). Power monitoring and harmonic problems in the modern building. Power Engineering Journal**, 15(2)**, 101-107.

[18] Chiang, T. K., Law, C. K., To, V., & Kwan, H. F. (2002). Power quality case studies: CLP power's experience. In Proceedings of Symposium on Power Quality and You: Managing Pollution in Electric Supply Systems.

[19] Wong, M. C., Dai, N. Y., & Lam, C. S. (2016). Parallel Power Electronics Filters in Three-Phase Four-Wire Systems. Springer Singapore.

[20] Elmitwally, A., & Rashed, M. (2011). Flexible operation strategy for an isolated PV-diesel microgrid without energy storage. IEEE transactions on energy conversion, **26(1)**, 235-244.

[21] Gafford, B. N., Duesterhoeft, W. C., & Mosher, C. C. (1959). Heating of induction motors on unbalanced voltages. Transactions of the American Institute of Electrical Engineers. Part III: Power Apparatus and Systems, **78(3)**, 282-286.

[22] Latran, M. B., Teke, A., & Yoldaş, Y. (2015). Mitigation of power quality problems using distribution static synchronous compensator: a comprehensive review. IET power electronics, **8(7)**, 1312-1328.

[23] Zhang, N., Tang, H., & Yao, C. (2014). A systematic method for designing a PR controller and active damping of the LCL filter for single-phase grid-connected PV inverters. Energies, **7(6)**, 3934-3954.

[24] Park, S., Han, S. B., Jung, B. M., Choi, S. H., & Jeong, H. G. (2000). A current control scheme based on multiple synchronous reference frames for parallel hybrid active filter. In Power Electronics and Motion Control Conference, 2000. Proceedings. IPEMC 2000. The Third International (**Vol. 1**, pp. 218-223). IEEE.

[25] Liu, Q., Tao, Y., Liu, X., Deng, Y., & He, X. (2013). Voltage unbalance and harmonics compensation for islanded microgrid inverters. IET Power Electronics, **7(5)**, 1055-1063.

[26] Caponet, M. C., Profumo, F., De Doncker, R. W., & Tenconi, A. (2002). Low stray inductance bus bar design and construction for good EMC performance in power electronic circuits. IEEE Transactions on Power Electronics, **17(2)**, 225-231.

[27] Tang, Y., Loh, P. C., Wang, P., Choo, F. H., Gao, F., & Blaabjerg, F. (2012). Generalized design of high performance shunt active power filter with output LCL filter. IEEE Transactions on Industrial Electronics, **59(3)**, 1443-1452.

[28] Khadkikar, V. (2012). Enhancing electric power quality using UPQC: A comprehensive overview. IEEE transactions on Power Electronics, **27(5)**, 2284-2297.

[29] Kumar, S., & Singh, B. (2009, December). Control of 4-leg VSC based DSTATCOM using modified instantaneous symmetrical component theory. In Power Systems, 2009. ICPS'09. International Conference on (pp. 1-6). IEEE.

[30] Bellini, A., & Bifaretti, S. (2006, May). A simple control technique for three-phase four-leg inverters. In Power Electronics, Electrical Drives, Automation and Motion, 2006. SPEEDAM 2006. International Symposium on (pp. 1143-1148). IEEE.

[31] Singh, B., Al-Haddad, K., & Chandra, A. (1998). A review of active filters for power quality improvement.

[32] Massoud, A. M., Finney, S. J., & Williams, B. W. (2004, September). Review of harmonic current extraction techniques for an active power filter. In Harmonics and Quality of Power, 2004. 11th International Conference on (pp. 154-159). IEEE.

[33] Cengiz, Ç. B. (2014). 3 Faz 4 Telli Paralel Aktif Güç Filtresi Tasarımı ve Gerçekleştirilmesi.

[34] Srianthumrong, S., & Sangwongwanich, S. (1998, October). An active power filter with harmonic detection method based on recursive DFT. In Harmonics and Quality of Power Proceedings, 1998. Proceedings. 8th International Conference On (**Vol. 1**, pp. 127-132). IEEE.

[35] Hartley, R.; Welles, K. (1990). An active power filter with harmonic detection method based on recursive DFT IEEE International Symposium On (**Vol. 3**, pp. 1792-1795)

[36] Yang, W. Y., Chang, T. G., Song, I. H., Cho, Y. S., Heo, J., Jeon, W. G., & Lee, J. W. (2009). Jae K. Kim Digital Signal Processing with MATLAB Springer.

[37] Akagi, H., Watanabe, E. H., & Aredes, M. (2017). Instantaneous power theory and applications to power conditioning (**Vol. 62**). John Wiley & Sons.

[38] Clarke, E. (1943). Circuit analysis of AC power systems (Vol. 1). Wiley.

[39] Kaura, V., & Blasko, V. (1997). Operation of a phase locked loop system under distorted utility conditions. IEEE Transactions on Industry applications, **33(1)**, 58-63.

[40] Dos Santos Filho, R. M., Seixas, P. F., & Cortizo, P. C. (2006). A comparative study of three-phase and single-phase PLL algorithms for grid-connected systems. In Proc. INDUSCON Conf. Rec.

[41] Nicastri, A., & Nagliero, A. (2010, July). Comparison and evaluation of the PLL techniques for the design of the grid-connected inverter systems. In Industrial Electronics (ISIE), 2010 IEEE International Symposium on (pp. 3865-3870). IEEE.

[42] Ferreira, R. J., Araújo, R. E., & Lopes, J. P. (2011, July). A comparative analysis and implementation of various PLL techniques applied to single-phase grids. In Energetics (IYCE), Proceedings of the 2011 3rd international Youth Conference on (pp. 1-8). IEEE.

[43] Gao, S., & Barnes, M. (2012). Phase-locked loop for AC systems: Analyses and comparisons.

[44] Kesler, M., & Ozdemir, E. (2011). Synchronous-reference-frame-based control method for UPQC under unbalanced and distorted load conditions. IEEE transactions on industrial electronics, **58(9)**, 3967-3975.

[45] Meral, M. E. (2012). Improved phase-locked loop for robust and fast tracking of three phases under unbalanced electric grid conditions. IET generation, transmission & distribution, **6(2)**, 152-160.

[46] Ciobotaru, M., Teodorescu, R., & Blaabjerg, F. (2006, June). A new single-phase PLL structure based on second order generalized integrator. In Power Electronics Specialists Conference, 2006. PESC'06. 37th IEEE (pp. 1-6). IEEE.

[47] Özkaya, H. (2007). Parallel active filter design, control, and implementation (Doctoral dissertation, MS Thesis Electrical and Electronics Engineering Middle East Technical University).

[48] Tan, A., Köroğlu, T., Demırdelen, T., İncı, M., Cuma, M. U., Bayindir, K. Ç., & Tümay, M. (2015, June). Performance investigation of shunt hybrid active power filter with a synchronous reference frame based controller. In Power Electronics for Distributed Generation Systems (PEDG), 2015 IEEE 6th International Symposium on (pp. 1-8). IEEE.

[49] Marconi, L., & Teel, A. R. (2013). Internal model principle for linear systems with periodic state jumps. IEEE Transactions on Automatic Control, **58(11)**, 2788-2802.

[50] Paap, G. C. (2000). Symmetrical components in the time domain and their application to power network calculations. IEEE Transactions on power systems, **15(2)**, 522-528.

[51] Ghosh, A., & Ledwich, G. (2012). Power quality enhancement using custom power devices. Springer Science & Business Media.

[52] Gole, A. M. (2000). HVDC course notes. Manitoba HVDC Research Centre, Canada.

[53] YingYing, J., XuDong, W., LiangLiang, M., ShuCai, Y., & HaiXing, Z. (2011, August). Application and Simulation of SVPWM in three phase inverter. In Strategic Technology (IFOST), 2011 6th International Forum on (**Vol. 1**, pp. 541-544). IEEE.

[54] Mutlu, H. H. (2011). DSP tabanlı paralel aktif güç filtresi ile harmonik ve reaktif güç kompanzasyonu (Doctoral dissertation, Selçuk Üniversitesi Fen Bilimleri Enstitüsü).

[55] Wintrich, A., Nicolai, U., Reimann, T., & Tursky, W. (2011). Application manual power semiconductors. ISLE.

[56] Bilgin, H. F., & Ermis, M. (2010). Design and implementation of a current-source converter for use in industry applications of D-STATCOM. IEEE Transactions on Power Electronics, **25(8)**, 1943-1957.

[57] Beukes, H. J., Enslin, J. H. R., & Spee, R. (1997, June). Busbar design considerations for high power IGBT converters. In Power Electronics Specialists Conference, 1997. PESC'97 Record., 28th Annual IEEE (**Vol. 2**, pp. 847-853). IEEE.

[58] Wood, P., Battello, M., Keskar, N., & Guerra, A. (2002). Application Note AN-1044–IPM Application Overview.

APPENDIX

APPENDIX – A: PSCAD/EMTDC MODEL FOR EQR

EQR is simulated in PSCAD/EMTDC software. EQR waveforms, input filter waveforms, line currents are analyzed and closed loop control of EQR system is tested. EQR configuration and single line diagram is given in Figure A.1.

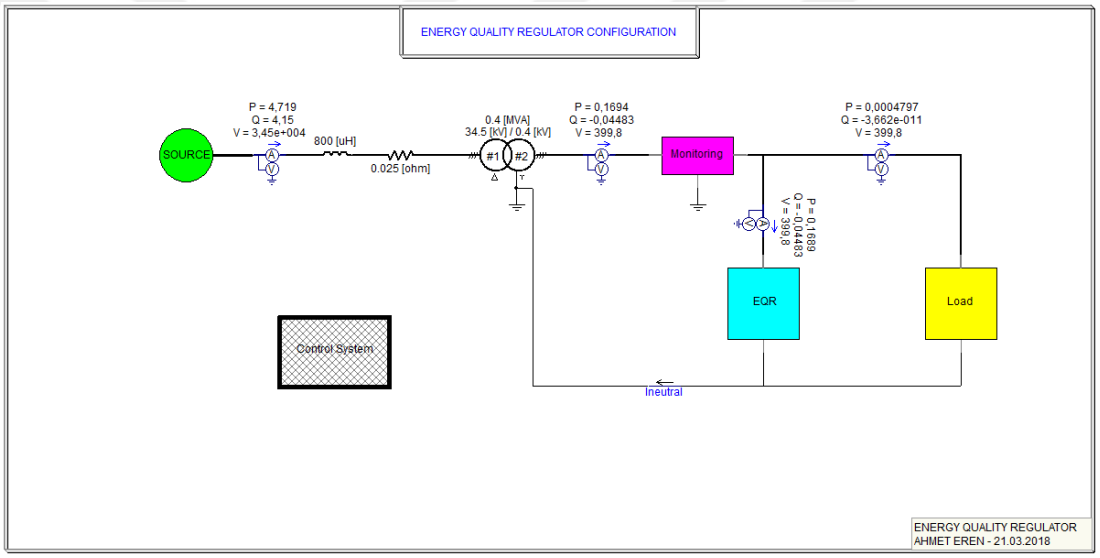

Figure A.1 EQR Configuration

Unbalanced resistive load model, 100 kVAR inductive, 100 kVAR capacitive and harmonic loads models are given in Figure A.2.

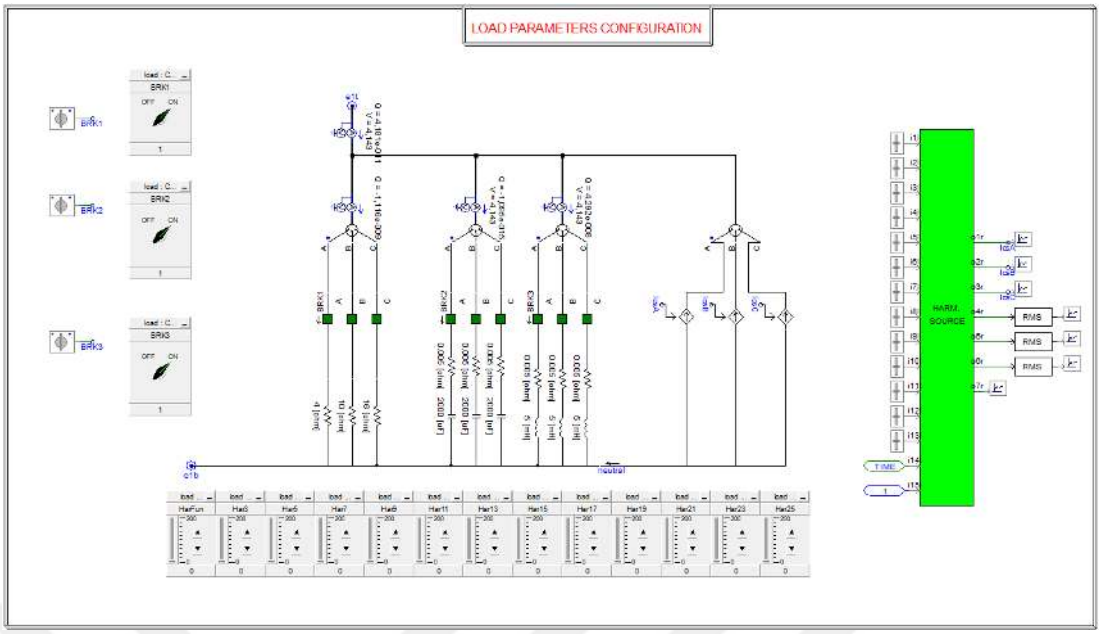

Figure A.2 Load Model

EQR inverter model with LCL filter and dc-link capacitors are given in Figure A.3.

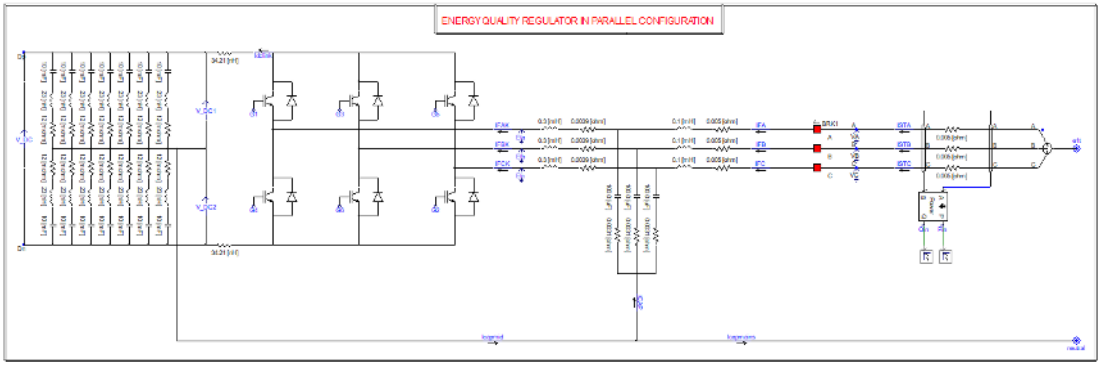

Figure A.3 EQR Inverter Model

Source voltage parameters can be set using source voltage settings page is given in Figure A.4.

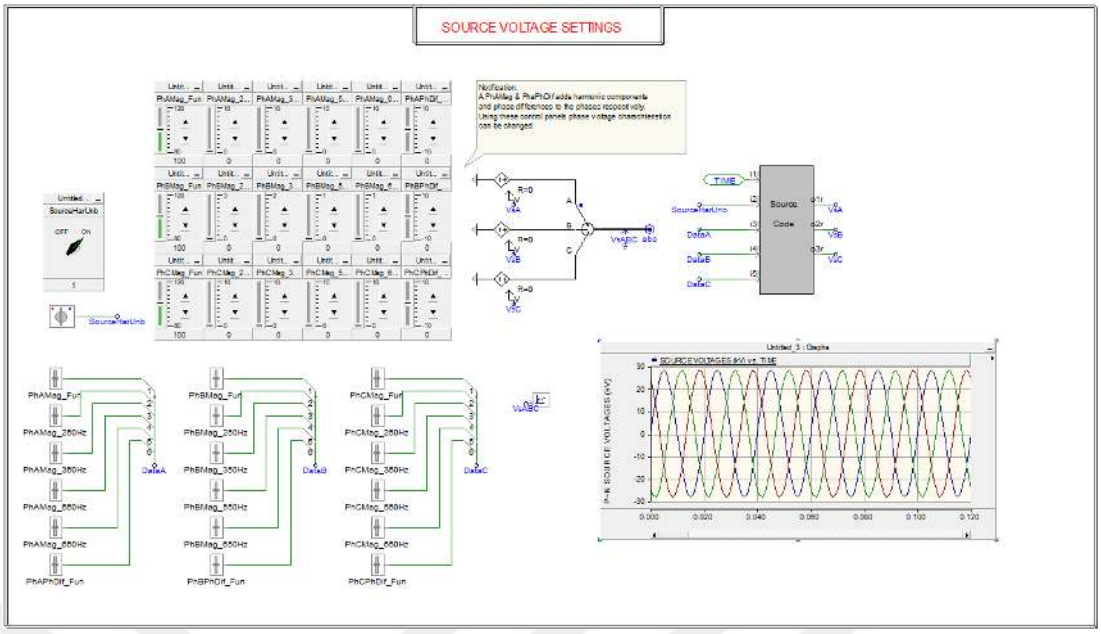

Figure A.4 EQR Supply Voltage Source Model

Monitoring page is given in Figure A.5.

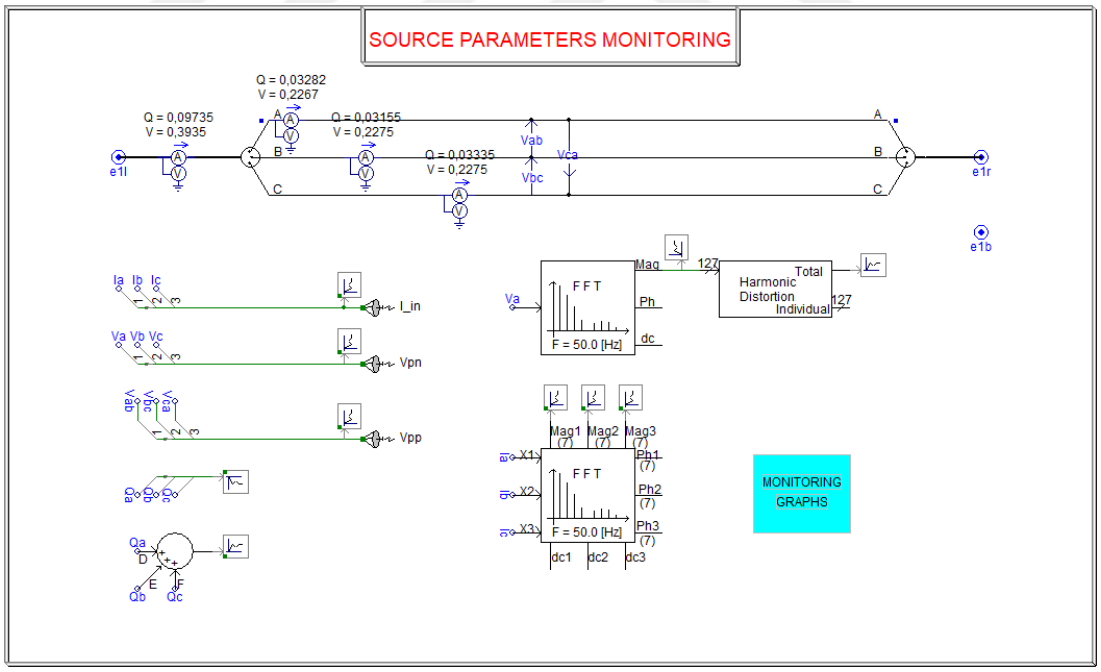

Figure A.5 EQR PSCAD/EMTDC Simulation Monitoring Page

APPENDIX- B: CALCULATION OF APPLICATION TIMES OF VECTORS IN SWITCHING STATES FOR SVPWM METHOD

Sector 1:

$$T_s V_{ref,norm} = T_1 V_1 + T_2 V_2 + T_0 V_0 + T_7 V_7 \quad (B.1)$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \\ V_{0,norm} \end{bmatrix} = T_1 \begin{bmatrix} 2/3 \\ 0 \\ -1/6 \end{bmatrix} + T_2 \begin{bmatrix} 1/3 \\ 1/\sqrt{3} \\ 1/6 \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \\ -1/2 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \\ 1/2 \end{bmatrix} \quad (B.2)$$

$$T_1 = \frac{3}{2} T_s \, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} \quad (B.3)$$

$$T_2 = \sqrt{3} T_s \, V_{\beta,norm} \quad (B.4)$$

$$T_0 = -T_s \, V_{\alpha,norm} - T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.5)$$

$$T_7 = -\frac{1}{2} T_s \, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} + T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.6)$$

Sector 2:

$$T_s V_{ref,norm} = T_2 V_2 + T_3 V_3 + T_0 V_0 + T_7 V_7 \quad (B.7)$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \\ V_{0,norm} \end{bmatrix} = T_2 \begin{bmatrix} 1/3 \\ 1/\sqrt{3} \\ 1/6 \end{bmatrix} + T_3 \begin{bmatrix} -1/3 \\ 1/\sqrt{3} \\ -1/6 \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \\ -1/2 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \\ 1/2 \end{bmatrix} \quad (B.8)$$

$$T_2 = \frac{3}{2} T_s \, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} \quad (B.9)$$

$$T_3 = -\frac{3}{2} T_s \, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} \quad (B.10)$$

$$T_0 = \frac{1}{2} T_s \, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} - T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.11)$$

$$T_7 = -\frac{1}{2} T_s \, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} + T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.12)$$

Sector 3:

$$T_s V_{ref,norm} = T_3 V_3 + T_4 V_4 + T_0 V_0 + T_7 V_7 \quad (B.13)$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \\ V_{0,norm} \end{bmatrix} = T_3 \begin{bmatrix} -1/3 \\ 1/\sqrt{3} \\ -1/6 \end{bmatrix} + T_4 \begin{bmatrix} -2/3 \\ 0 \\ 1/6 \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \\ -1/2 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \\ 1/2 \end{bmatrix} \quad (B.14)$$

$$T_3 = \sqrt{3} T_s \, V_{\beta,norm} \quad (B.15)$$

$$T_4 = -\frac{3}{2} T_s \, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} \quad (B.16)$$

$$T_0 = \frac{1}{2} T_s \, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} - T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.17)$$

$$T_7 = T_s \, V_{\alpha,norm} + T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.18)$$

Sector 4:

$$T_s V_{ref,norm} = T_4 V_4 + T_5 V_5 + T_0 V_0 + T_7 V_7 \quad (B.19)$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \\ V_{0,norm} \end{bmatrix} = T_4 \begin{bmatrix} -2/3 \\ 0 \\ 1/6 \end{bmatrix} + T_5 \begin{bmatrix} -1/3 \\ -1/\sqrt{3} \\ -1/6 \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \\ -1/2 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \\ 1/2 \end{bmatrix} \quad (B.20)$$

$$T_4 = -\frac{3}{2} T_s \, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} \quad (B.21)$$

$$T_5 = -\sqrt{3} T_s \, V_{\beta,norm} \quad (B.22)$$

$$T_0 = \frac{1}{2} T_s \, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} - T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.23)$$

$$T_7 = T_s \, V_{\alpha,norm} + T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.24)$$

Sector 5:

$$T_s V_{ref,norm} = T_5 V_5 + T_6 V_6 + T_0 V_0 + T_7 V_7 \quad (B.25)$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \\ V_{0,norm} \end{bmatrix} = T_5 \begin{bmatrix} -1/3 \\ -1/\sqrt{3} \\ -1/6 \end{bmatrix} + T_6 \begin{bmatrix} 1/3 \\ -1/\sqrt{3} \\ 1/6 \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \\ -1/2 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \\ 1/2 \end{bmatrix} \quad (B.26)$$

$$T_5 = -\frac{3}{2} T_s \, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} \quad (B.27)$$

$$T_6 = \frac{3}{2} T_s \, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} \quad (B.28)$$

$$T_0 = \frac{1}{2} T_s \, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} - T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.29)$$

$$T_7 = -\frac{1}{2} T_s \, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} + T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.30)$$

Sector 6:

$$T_s V_{ref,norm} = T_6 V_6 + T_1 V_1 + T_0 V_0 + T_7 V_7 \quad (B.31)$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \\ V_{0,norm} \end{bmatrix} = T_6 \begin{bmatrix} 1/3 \\ -1/\sqrt{3} \\ 1/6 \end{bmatrix} + T_1 \begin{bmatrix} 2/3 \\ 0 \\ -1/6 \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \\ -1/2 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \\ 1/2 \end{bmatrix} \quad (B.32)$$

$$T_6 = -\sqrt{3} T_s \, V_{\beta,norm} \quad (B.33)$$

$$T_1 = \frac{3}{2} T_s \, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} \quad (B.34)$$

$$T_0 = -T_s \, V_{\alpha,norm} - T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.35)$$

$$T_7 = -\frac{1}{2} T_s \, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm} + T_s \, V_{0,norm} + \frac{1}{2} T_s \quad (B.36)$$

APPENDIX - C: MEASURMENT APPARATUS

- TEKTRONIX MDO3024 – 200 MHz oscilloscope
- Chauvin Arnoux 8335 Portable Power & Quality Analyzer
- HIOKI PW3198 Power Quality Analyzer
- PEM, Rogowski Current Waveform Transducer
- Fluke 267 TRMS Multimeter
- PINTEK DP100 High Voltage Probe