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REPUBLIC OF TÜRKİYE

GAZİANTEP UNIVERSITY

GRADUATE SCHOOL OF NATURAL & APPLIED SCIENCES

DESIGN AND IMPLEMENTATION OF SINGLE-PHASE AC-AC MATRIX CONVERTER

M.Sc. THESIS

IN

ELECTRICAL AND ELECTRONICS ENGINEERING

BY

OSAMAH AYMEN JASSIM AL-DORI

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Prof. Dr. Ahmet Mete VURAL

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Osamah Aymen Jassım AL-DORI

September 2023

DESIGN AND IMPLEMENTATION OF SINGLE-PHASE AC-AC MATRIX CONVERTER

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Osamah Aymen Jassım AL-DORI

ABSTRACT

DESIGN AND IMPLEMENTATION OF SINGLE-PHASE AC-AC MATRIX CONVERTER

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M.Sc. in Electrical and Electronics Engineering
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September 2023

133 pages

In this thesis, the design and experimental implementation of a direct bipolar buck single-to-single-phase matrix converter (SSMC) were studied. A novel control method for SSMCs that improves the performance parameters such as voltage transfer ratio (VTR), output voltage total harmonic distortion (THD), and input current THD was suggested. Secondly, a synchronization algorithm was developed that synchronizes the triggering signals of the power semiconductors with the grid regardless of the synthesized output frequency. Thirdly, the effects of four different carrier-based pulse width modulation (PWM) techniques (sinusoidal PWM, multiple PWM, staircase PWM, and trapezoidal PWM) on the performance parameters of the SSMC were compared in terms of VTR, output voltage THD, output current THD, and input current THD. The simulation and experimental studies were carried out under the conditions when the output frequency is lower, equal, and higher to the input frequency. According to the experimental results, the proposed control method increases the VTR by around 10% and decreases the output voltage THD and input current THD by around 34% and 54%, respectively, for all output frequencies.

Key Words: AC-AC Converters, Carrier-Based PWM, Frequency Converters, Single-Phase Matrix Converter, Voltage Controllers.

ÖZET

TEK FAZLI AC-AC MATRİS DÖNÜŞTÜRÜCÜSÜNÜN TASARIMI VE GERÇEKLEŞTİRİLMESİ

AL-DORI, Osamah Aymen Jassım
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Danışman: Prof. Dr. Ahmet Mete VURAL
Eylül 2023
133 sayfa

Bu tezde, doğrudan iki kutuplu düşürücü tek faz-tek faz matris dönüştürücü (TTMD)'nün tasarımı ve deneysel uygulaması çalışılmıştır. TTMD'ler için gerilim aktarım oranı (GAO), çıkış gerilimi toplam harmonik bozulması (THB) ve giriş akımı THB gibi TTMD'lerin performans parametrelerini iyileştiren yeni bir kontrol yöntemi önerilmiştir. İkinci olarak, sentezlenen çıkış frekansından bağımsız olarak güç yarıiletkenlerinin tetikleme sinyallerini şebeke ile senkronize eden bir senkronizasyon algoritması geliştirilmiştir. Üçüncü olarak, dört farklı taşıyıcı tabanlı darbe genişlik modülasyonu (DGM) tekniğinin (sinusoidal DGM, çoklu DGM, merdiven DGM ve yamuk DGM) TTMD'nin GAO, çıkış gerilimi THB, çıkış akımı THB ve giriş akımı THB gibi performans parametreleri üzerine etkileri karşılaştırılmıştır. Benzetim ve deneysel çalışmalar çıkış frekansının giriş frekansından düşük, eşit ve yüksek olduğu koşullarda yürütülmüştür. Deneysel sonuçlara göre, önerilen kontrol yöntemi tüm çıkış frekanslarında GAO'yu yaklaşık %10 artırmış, çıkış gerilimi THB ve giriş akımı THB'yi ise yaklaşık olarak %34 ve %54 oranında azaltmıştır.

Anahtar Kelimeler: AC-AC Dönüştürücüleri, Taşıyıcı Tabanlı DGM, Frekans Dönüştürücüleri, Tek Fazlı Matris Dönüştürücü, Gerilim Kontrolörleri.

“Dedicated to my family”

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my supervisor, Prof. Dr. Ahmet Mete VURAL, for his kindness, prompt responses, guidance, and support throughout the study. I was too lucky to study under his supervision.

I would like to thank Dr. Fatih EROĞLU and Asst. Prof. Dr. Ali Osman ARSLAN for their guidance in performing the experimental part of this study and for generously sharing their experience and knowledge.

I would like to express my gratitude to Asst. Prof. Dr. Atilla DÖNÜK for his unwavering support and willingness to help.

Finally, and most importantly, I would like to express my love and gratitude to my family for their endless support. Without their support, no part of this thesis would be possible.

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LIST OF SYMBOLS

A_r	Reference amplitude
A_{cr}	Carrier amplitude
v_{in}	Instantaneous input voltage
V_{in}	Input voltage RMS value
v_o	Instantaneous output voltage
V_o	Output voltage RMS value
v_r	Reference signal
v_{cr}	Carrier signal
v_p	Pulse signal
v_{com}	Commutation signal
v_{tra}	Trapezoidal signal
i_{in}	Instantaneous input current
I_{in}	Input current RMS value
i_r	Instantaneous reference current
i_o	Instantaneous output current
V_{op}	Peak output voltage
V_{rp}	Peak reference voltage
I_{op}	Peak output current
I_{rp}	Peak reference current
f_r	Reference frequency
f_{cr}	Carrier frequency
f_{sw}	Switching frequency
f_{in}	Input frequency
f_o	Output frequency
T_{cr}	Carrier period
T_{sw}	Switching period

T_{sca}	Staircase signal period
T_{tra}	Trapezoidal signal period
t_d	Dead time
t_l	Low time
t_r	Rise time
t_m	Middle time
t_h	High time
t_f	Fall time
m_a	Modulation index
P	Pulses per half-cycle
q	Source waveform half-cycles
R_{sn}	Snubber resistor
C_{sn}	Snubber capacitor
R_{cl}	Clamp resistor
C_{cl}	Clamp capacitor
C_{in}	Input filter capacitor
L_{in}	Input filter inductor
C_f	Output filter capacitor
L_f	Output filter inductor
D	Duty ratio
n	Harmonic order
ω	Angular frequency
α	Switching angle
k	Ratio of trapezoidal signal rise and fall time to high time

LIST OF ABBREVIATIONS

AC	Alternating Current
DC	Direct Current
RMS	Root Mean Square
MC	Matrix Converter
TT	Three-to-Three-Phase
SS	Single-to-Single-Phase
TTMC	Three-to-Three-Phase Matrix Converter
SSMC	Single-to-Single-Phase Matrix Converter
SCR	Silicon-Controlled Rectifier
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
GTO	Gate Turn-off Thyristor
IGCT	Integrated Gate Commutated Thyristor
JFET	Junction-Gate Field-Effect Transistors
MTO	Metal-Oxide-Semiconductor Turn-Off Thyristor
MCT	Metal-Oxide-Semiconductor Controlled Thyristor
DB	Diode Bridge
CE	Common Emitter
CC	Common Collector
RB-IGBT	Reverse Blocking IGBT
RL	Inductive
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
MPWM	Multiple Pulse Width Modulation
SCPWM	Staircase Pulse Width Modulation
TPWM	Trapezoidal Pulse Width Modulation
VTR	Voltage Transfer Ratio

THD	Total Harmonics Distortion
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching
PI	Proportional-Integral
ZCD	Zero-Crossing Detection
RED	Rising Edge Detection
TVS	Transient Voltage Suppressor
VHDL	Very High-Speed Integrated Circuit Hardware Description Language

CHAPTER 1
INTRODUCTION

1.1 Motivation

Throughout the past years, the role of power electronics has undergone a fundamental transformation, shifting from a mere tool that facilitates emerging trends to a pivotal technology that plays a critical role in promoting sustainable development and progress in society [1]. This transformation can be attributed to two major developments: the rise in renewable energy generation capabilities and the growing adoption of electric-powered end-use devices. Consequently, the design and control of reliable and efficient power electronics converters have become a continuous research and development area.

Having controlled alternating current (AC) power from an uncontrolled AC source is required for many applications, such as motor drive and induction heating. Power electronic-based AC-AC converters can be mainly divided into three categories: indirect AC-direct current (DC)-AC converters, direct AC-AC pulse width modulation (PWM) converters, and matrix converters (MCs). Indirect AC-DC-AC converters are able to regulate the output voltage and provide variable output frequency. However, they require bulky passive energy storage devices: DC-link inductor or capacitor, which in turn increases the cost, volume, and losses and decreases the reliability and life span of the converter [2]. Electrolytic capacitors, which are usually used in DC-links, have the highest failure rate in power electronics circuits [3], [4]. Direct AC-AC PWM converters, on the other hand, do not require energy storage devices while featuring compact topologies and simple control. However, although PWM converters are able to provide variable output voltage, generally, they are not able to step up and down the source frequency. On the other hand, MCs can provide variable output voltage and frequency without the need for energy storage devices. Moreover, MCs offer various favorable characteristics that make them preferred for many applications. These features include regeneration capability, bidirectional power flow, simple and compact power circuit, and unity power factor operation regardless of the load [5].

1.2 Aim of Thesis and Contributions

In this thesis, the design and implementation of a single-to-single-phase MC (SSMC) is held. This thesis studies the conventional SSMC topology. The thesis aims to understand the shortcomings of the SSMC open-loop control methods in the literature and propose a new method that overcomes them. Moreover, it is aimed to understand the influence of carrier-based PWM techniques on the key performance parameters of SSMCs, including voltage transfer ratio (VTR) and output voltage and input current total harmonics distortion (THD).

This thesis offers several contributions to the field of SSMC. The key contributions of the thesis are listed as follows:

- Proposing a new open-loop control method for SSMC. The method has several advantages over the methods in the literature. The key advantages are listed as follows:
  - ❖ The proposed method maximizes source voltage utilization, enabling the SSMC to achieve high VTRs (>0.98). It also enhances the overall performance by reducing THD in the output voltage and source input current.
  - ❖ The proposed method offers soft-switching of power switches during commutation instances by ensuring zero-current switching (ZCS) for all synthesized output frequencies.
  - ❖ The proposed control scheme simplifies the generation of the output signal with the desired frequency as it only requires prior knowledge of the output frequency without the need to modify the control scheme.
  - ❖ The proposed control scheme ensures safe current commutation when the PWM signal is low and when changing the current path. Moreover, it allows the utilization of various modulation techniques without encountering current commutation problems.
  - ❖ The proposed control scheme allows connecting an inductive (RL) load to the output terminals of the SSMC without encountering current commutation issues when the PWM signal is low or significant output voltage transients when changing the current path. In this way, the need for

a dissipative circuit (e.g., clamp circuit) when dealing with relatively inductive RL loads is eliminated.

- Proposing a new synchronization algorithm that synchronizes the PWM gate-triggering pulses with the source (grid). The algorithm ensures synchronization for output frequencies lower, higher, and equal to the source frequency.
- Analyzing and comparing the influence of four carrier-based PWM techniques on the key performance parameters of the SSMC. The carrier-based PWM techniques under consideration in this thesis are the sinusoidal PWM (SPWM), multiple PWM (MPWM), staircase PWM (SCPWM), and trapezoidal PWM (TPWM).

1.3 Layout of Thesis

This thesis consists of seven chapters, including this introductory chapter. The content of the remaining chapters is as follows:

Chapter 2 provides general background on AC-AC power electronics converters. First, the different topologies of three-phase and single-phase AC-AC converters are discussed. The favorable features of MCs that distinguish them from the rest of the converters are also discussed. Then, the different topologies of the bidirectional switches, which are the main switching components in MCs, are discussed along with the pros, cons, and requirements of each topology. Later, the current commutation problem that MCs encounter when connected to an RL load is discussed. Then, the protection approaches of MCs against overvoltage damage are highlighted. Finally, the generally utilized control techniques of MCs are summarized.

Chapter 3 discusses the step-changed and voltage buck operations of the SSMC. First, the different operation states of the SSMC and its ability to generate a bipolar voltage gain are demonstrated. Then, the switching strategies for step-changed frequency operation are discussed. Finally, the principles of different carrier-based PWM techniques are discussed for the voltage control operation of the SSMC.

Chapter 4 presents the proposed SSMC open-loop control method and synchronization algorithm. First, the proposed control scheme is discussed. Then, the importance of utilizing an adjustable trapezoidal reference signal in the modulation process is

discussed. Later, the proposed synchronization algorithm is discussed. Finally, the key contributions of the proposed method are highlighted.

Chapter 5 covers the findings of the simulation studies. First, a simulation study with three case studies is performed to demonstrate the superiority of the proposed control method over the counterpart methods in the literature. Then, a simulation study is carried out to analyze and compare the influence of four carrier-based PWM techniques on the key performance parameters of the SSMC.

Chapter 6 covers the findings of the experimental studies. First, an experimental study with two case studies is carried out to experimentally verify the superiority of the proposed method over the counterpart methods in the literature. Then, another study is carried out to experimentally analyze and compare the SSMC performance under different carrier-based PWM techniques.

Finally, Chapter 7 presents the main conclusions drawn from this study, along with the key contributions of this study and the suggested future work.

CHAPTER 2
BACKGROUND

2.1 Introduction

In this chapter, a general background on AC-AC voltage conversion is presented. Different three-phase and single-phase converter topologies with their advantages and disadvantages are presented in Section 2.2. Section 2.3 presents the different configurations of bidirectional switches, their advantages and disadvantages, and some commercially available options. Section 2.4 discusses one of the main problems MCs have when connected to RL loads due to the lack of a freewheeling path: the current commutation problem. Section 2.5 discusses the commonly used solutions to protect MCs against overvoltage, which can happen due to many reasons, including breaking the RL load current, failure of some parts of the system, and source perturbation. Section 2.6 presents an overview of the control techniques used to control the performance of MCs.

2.2 Topology Overview

Power electronic converters can be generally categorized according to their conversion as AC-DC, DC-AC, DC-DC, and AC-AC converters. The main purpose of AC-AC converters is to produce a controlled AC output. This includes controlled voltage/current and frequency. AC-AC converters can be classified into numerous and diverse categories due to ongoing advancements in converter technologies. The technology advancements are mainly in three-to-three-phase (TT) and single-to-single-phase (SS) AC-AC converters. The following subsections overview the different TT and SS converter topologies.

2.2.1 Three-to-Three-Phase Converters

TT converters can be broadly classified into four categories: two-stage converters (AC-DC-AC), voltage controllers, MCs, and hybrid converters, as depicted in Figure 2.1 [2], [4], [6]. Any type of converter inside these categories can be a voltage source or current source converter. This thesis focuses on voltage source converters.

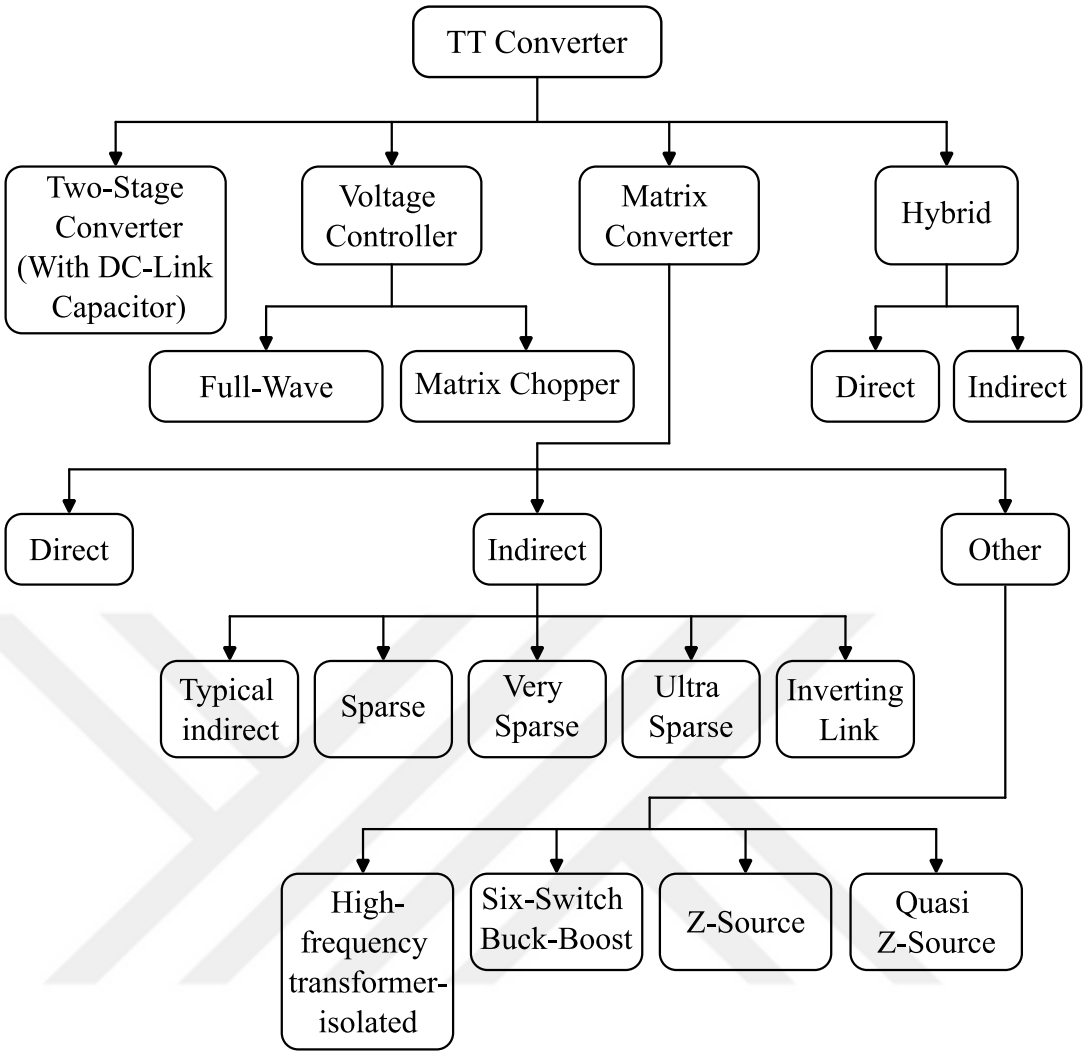


Figure 2.1 A general classification of TT converter topologies.

Two-stage converters with semiconductor power switches are one of the solutions used prior to the invention of MCs to obtain a controlled output voltage and frequency [7]–[9]. A general example of a two-stage converter is the back-to-back converter shown in Figure 2.2, where A, B, and C represent the three-phase input terminals and a, b, and c represents the three-phase output terminals. First, the AC voltage is converted to DC and then back to AC by properly switching the unidirectional switches. The problem with these converters is the requirement of a high number of power switches and a bulky energy storage element [2]. Usually, electrolytic capacitors are used at the DC-link to buffer the energy, and these capacitors are known to have the highest failure rate in power electronics circuits, as shown in Figure 2.3 [3], [4]. Furthermore, these capacitors are bulky.

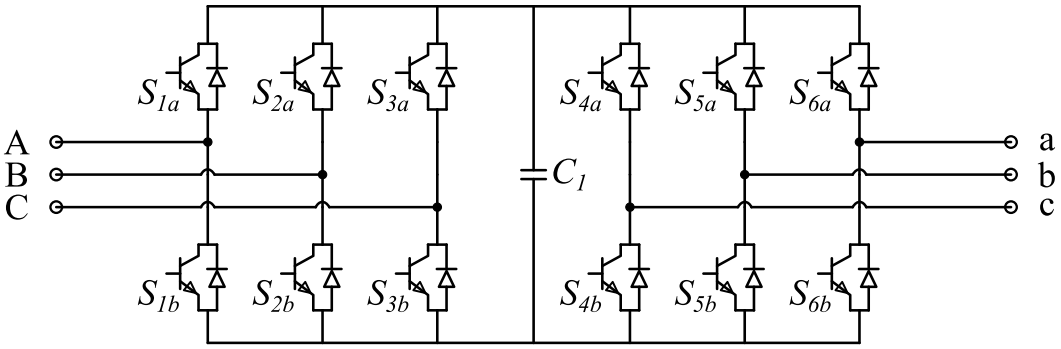


Figure 2.2 Typical TT back-to-back converter topology.

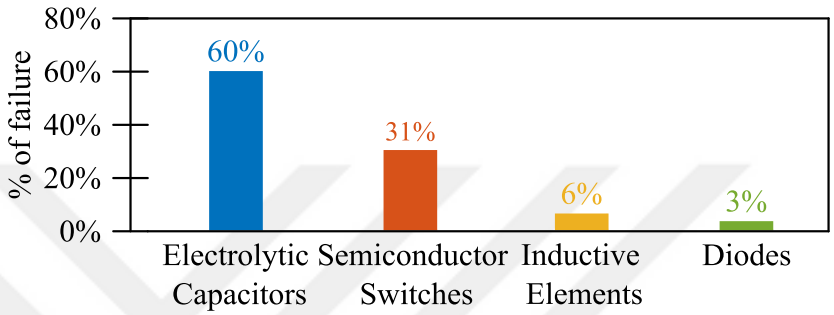


Figure 2.3 Failure percentage of power components [3], [4].

AC voltage controllers, as their name indicates, can only control the output voltage and cannot control the output frequency. They include full-wave controllers [10], [11] and matrix choppers [12]. Cycloconverters with forced commutation circuits, on the other hand, can control the output voltage and frequency [13]–[15]. However, it is a bulky solution and provides poor performance. Further, cycloconverters can only step-down the source frequency, which limits their utilization to low-speed applications. Both the AC voltage controllers and cycloconverters are constructed using silicon-controlled rectifiers (SCRs).

The development of bidirectional switches using insulated gate bipolar transistors (IGBTs) and other power transistors made it simple to realize the MCs. The work of Venturini and Alesina is where the evolution of the MC began, where they proposed a mathematical analysis and developed the idea of a low-frequency modulation matrix to characterize the MC's low-frequency behavior [16]–[18]. Thus, it is possible to acquire the output voltages through a multiplication of the input voltages and the modulation or transfer matrix. A typical direct TTMC topology is shown in Figure 2.4, where it is clear that no intermediate DC-link capacitor is required to complete the AC-AC conversion. This decreases the complexity and volume of the power circuit and

increases the lifespan and efficiency of the TTMC. A total of nine bidirectional switches are arranged in a 3×3 matrix form to construct the TTMC topology, as shown in Figure 2.4. An input filter is usually used to minimize the effect of high-frequency components in the source input current and the perturbations of the source input voltage [19].

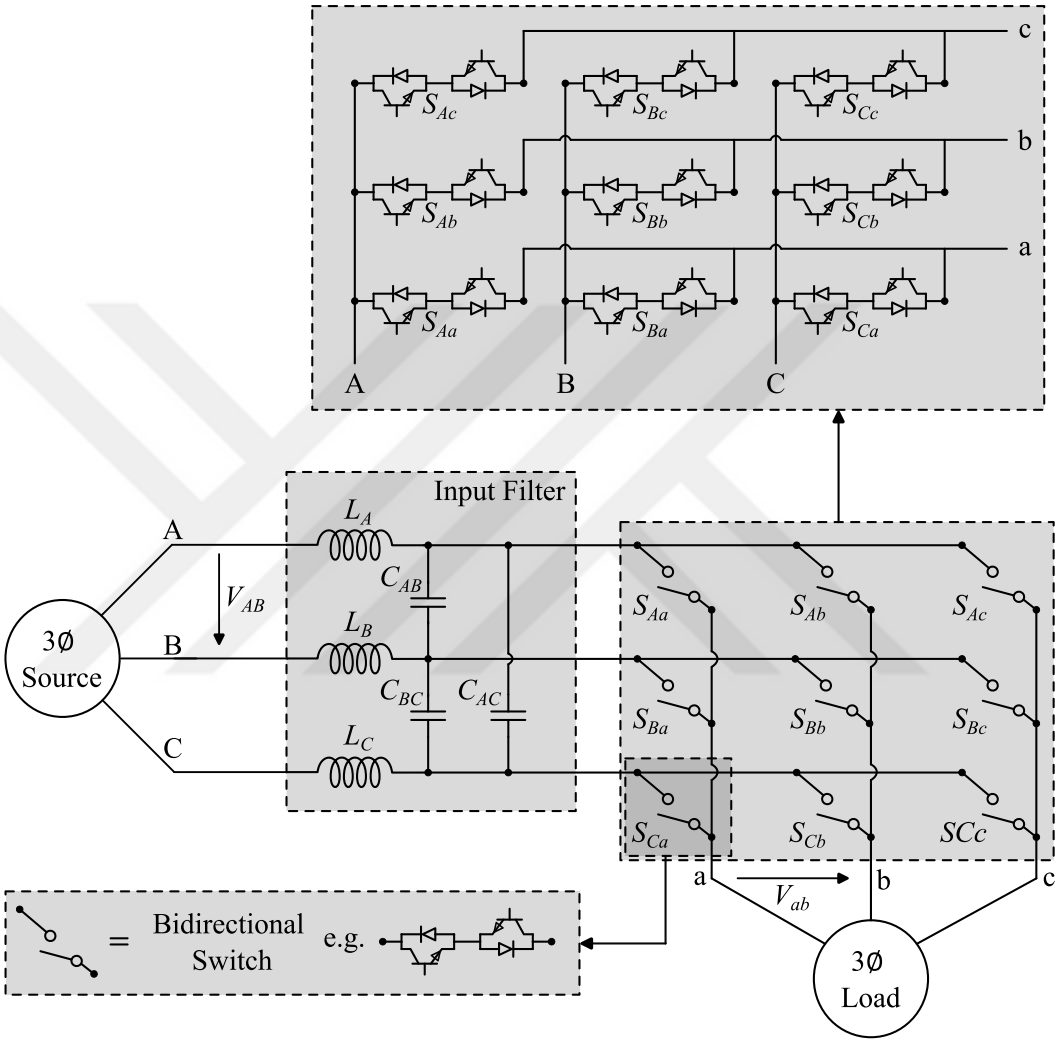


Figure 2.4 Typical direct TTMC topology.

The indirect TTMCs perform the AC-AC conversion by converting the AC first to DC using a bidirectional switch rectifier and then the DC back to AC using a unidirectional switch inverter. The typical topology of an indirect TTMC is shown in Figure 2.5 [20], [21]. It is noteworthy that although this topology involves DC-link, it does not use a DC-link capacitor. In [21], the performance of direct and indirect topologies for induction motor drives have been compared, and it has been concluded that direct MCs provide higher VTR and, in general, less power losses. The indirect topology can be

improved using an auxiliary voltage supply to allow for more VTR and invulnerability to an imbalanced voltage supply, however, at the expense of higher conduction losses [22].

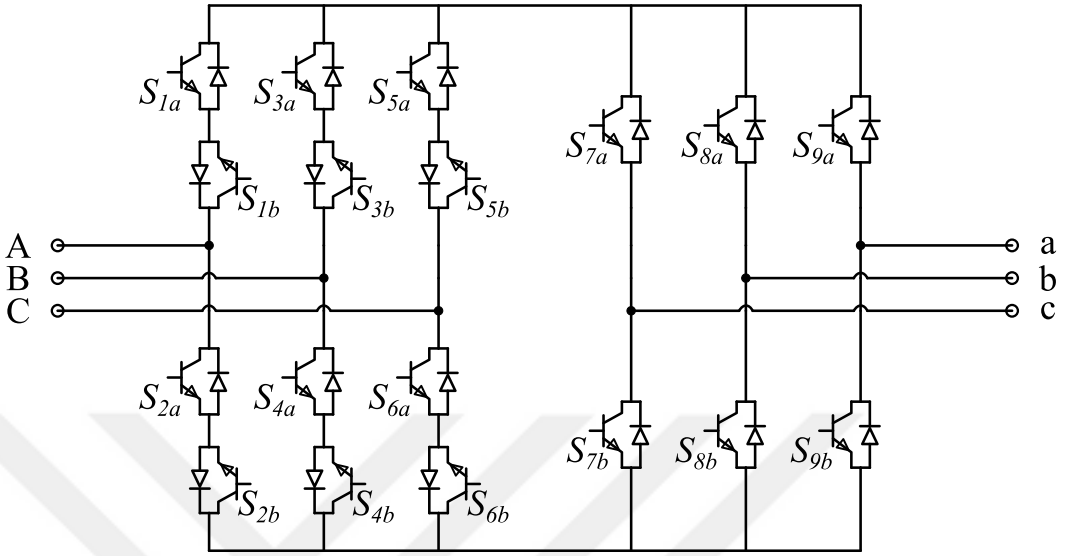


Figure 2.5 Typical indirect TTMC topology.

Unlike the typical indirect TTMC, which utilizes eighteen semiconductor power switches, the indirect sparse TTMC only utilizes fifteen switches with the same number of diodes, as shown in Figure 2.6. Nevertheless, the indirect sparse TTMC topology suffers from high power losses because more semiconductor devices are utilized in the conduction path [2].

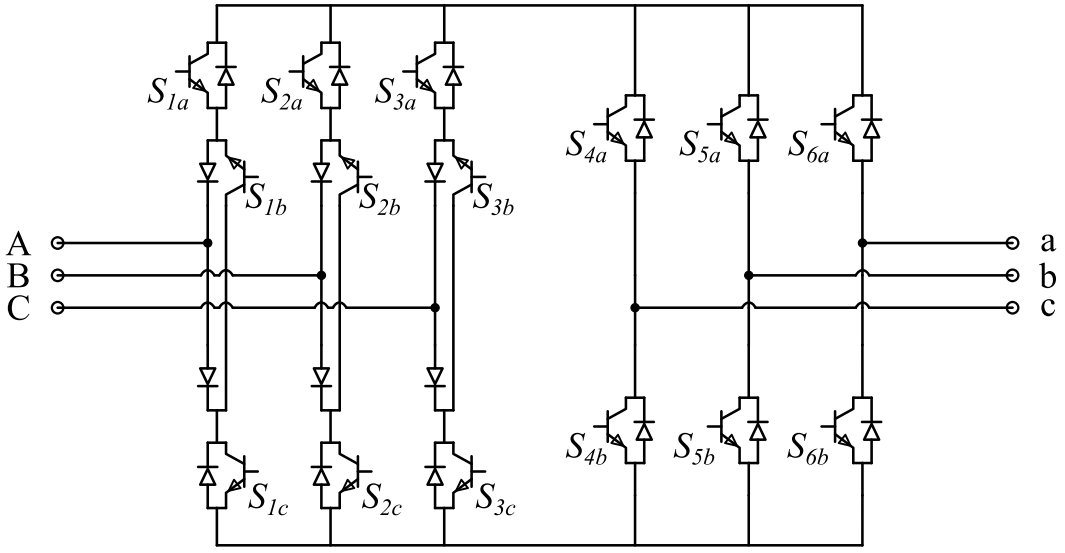


Figure 2.6 Indirect sparse TTMC topology.

The topology of indirect very sparse TTMS, shown in Figure 2.7 [6], [23], [24], decreases the number of semiconductor power switches from fifteen to twelve. Nevertheless, it increases the number of diodes to thirty, which increases the conduction losses [2].

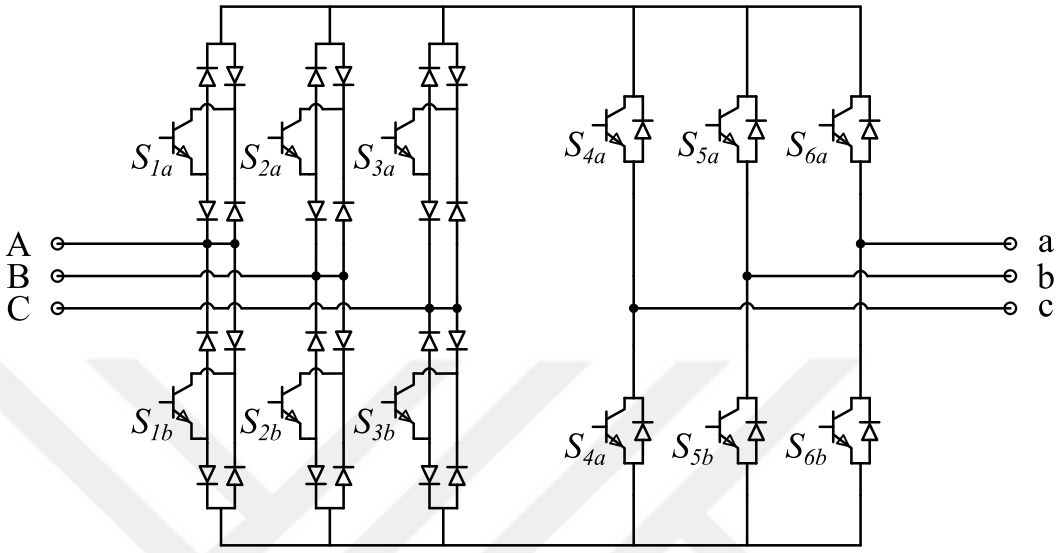


Figure 2.7 Indirect very sparse TTMC topology.

One more indirect topology from the sparse family is the ultra sparse MC, shown in Figure 2.8 [6], [25], [26]. This topology only allows for unidirectional power flow and limits the fundamental phase displacement at the input and output to $\pm \pi/6$ [25]. The source bridge consists of only three semiconductor power switches and twelve diodes. Therefore, a total of nine switches and eighteen diodes are used to construct the topology of indirect ultra sparse TTMC.

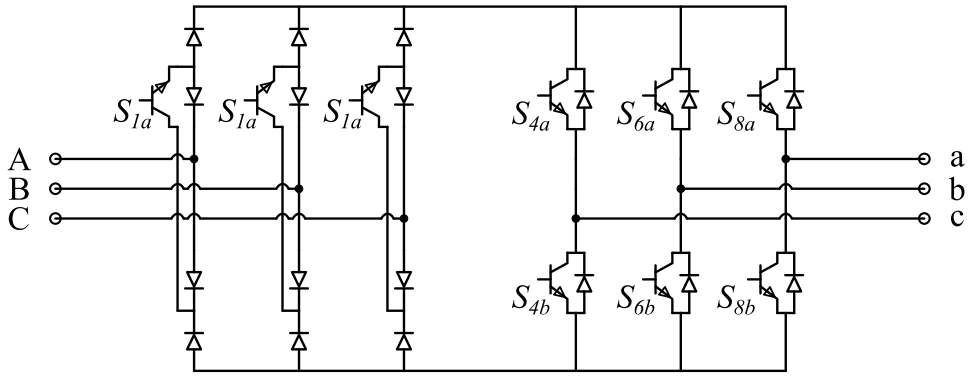


Figure 2.8 Indirect ultra sparse TTMC topology.

The inverting link MC topology, shown in Figure 2.9, allows for bidirectional power flow with zero DC-link current commutation [27]. The DC-link stage consists of two

unidirectional power switches and two diodes. This topology limits the switching frequency to be at high levels. As a result, high switching losses are associated with the use of this topology of indirect TTMCs. The VTR of indirect MCs, including the sparse family MCs and inverting link MC, can maximumly reach 0.866 with linear modulation techniques [6].

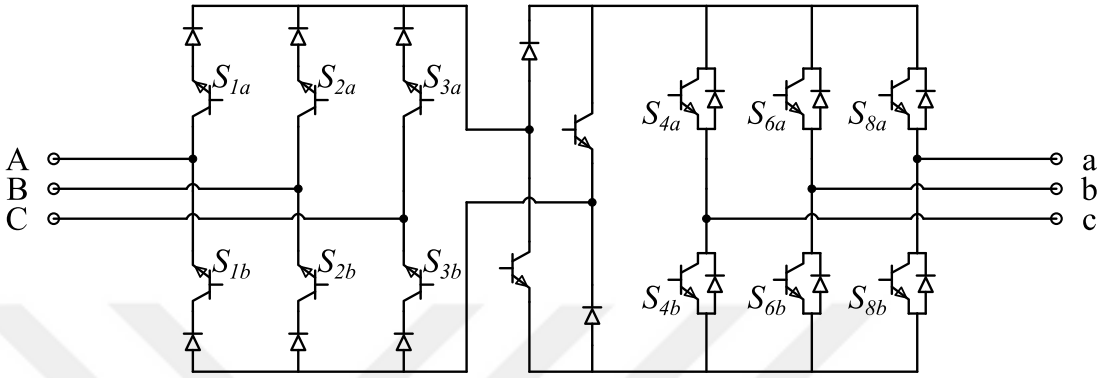


Figure 2.9 Indirect inverting link TTMC topology.

To obtain a VTR higher than unity, hybrid TTMCs topologies are used. These topologies utilized one or more small DC-link capacitors or DC-DC choppers. In [28], the first hybrid AC-AC converter topology has been proposed. The converter is obtained by replacing the bidirectional switches of direct TTMC with single-phase H-bridge inverters. The topology is referred to as modular MC [29] and is shown in Figure 2.10. This topology divides the bulky DC-link capacitor into several small capacitors. It is clear that the number of active and passive devices increases with this topology. Many other hybrid TTMCs are discussed in [6].

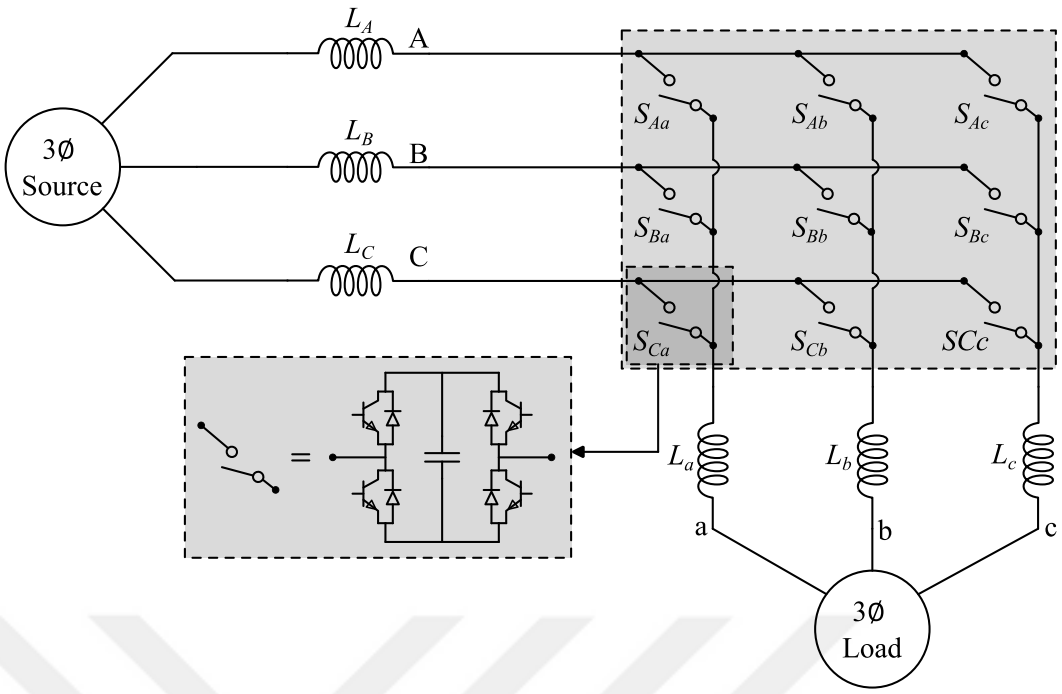


Figure 2.10 Modular TTMC topology.

2.2.2 Single-to-Single-Phase Converters

A general classification of SS converters is shown in Figure 2.11. Intuitively, one can achieve controlled SS conversion by means of a DC-link capacitor [30]. Nevertheless, as discussed above, this involves a short life span and a bulky design. Phase-controlled converters, also known as full-wave converters, are simple AC-AC converters that can control the output voltage by controlling the firing angle of the SCRs. They are not capable of controlling the output frequency. There are various topologies of these converters, however, the topology shown in Figure 2.12 is the most common one.

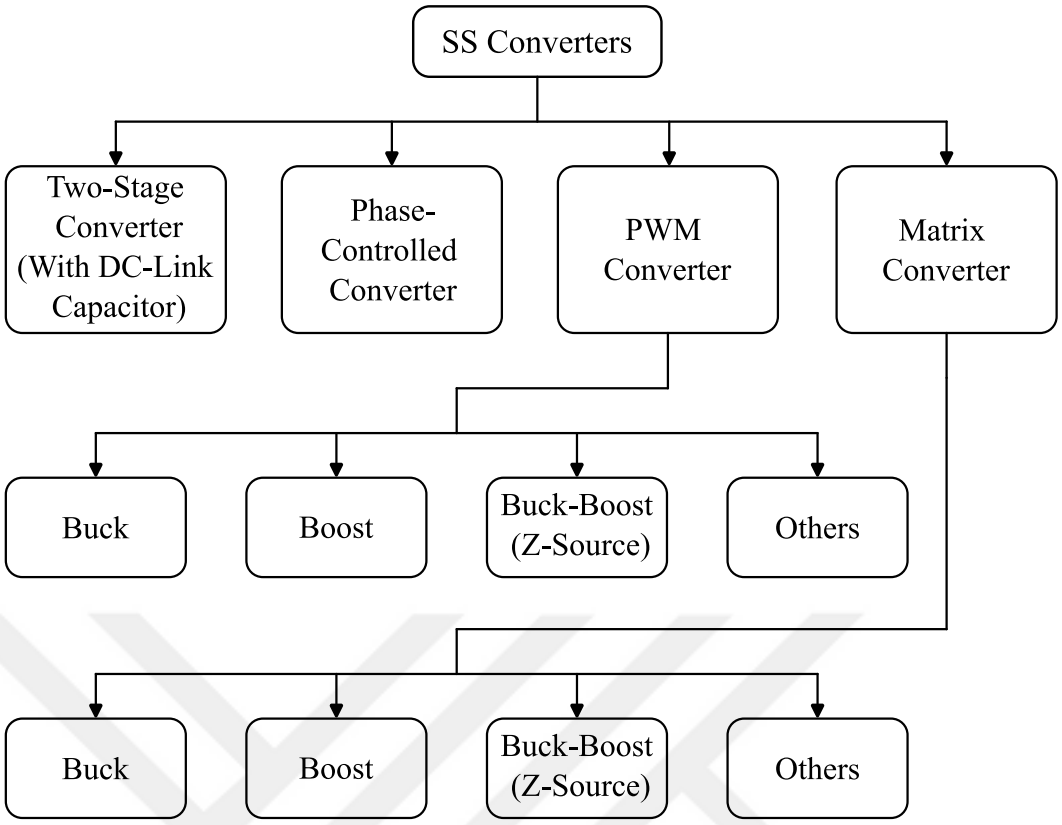


Figure 2.11 A general classification of TT converter topologies.

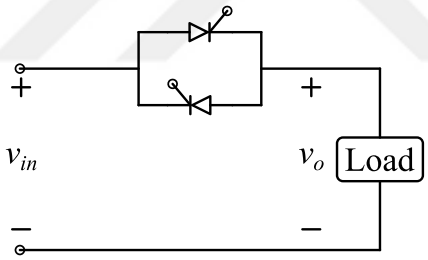


Figure 2.12 A typical phase-controlled converter topology.

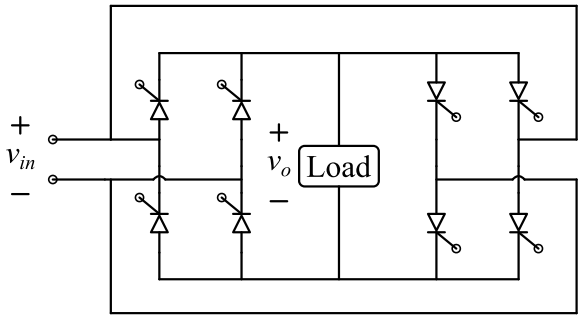


Figure 2.13 A typical cycloconverter topology.

With cycloconverters, the output frequency can be controlled. Nevertheless, since SCRs are used, the frequency can only be stepped down from the source input

frequency. This limits the utilization of cycloconverters to low-speed control applications. A typical SS cycloconverter topology is shown in Figure 2.13.

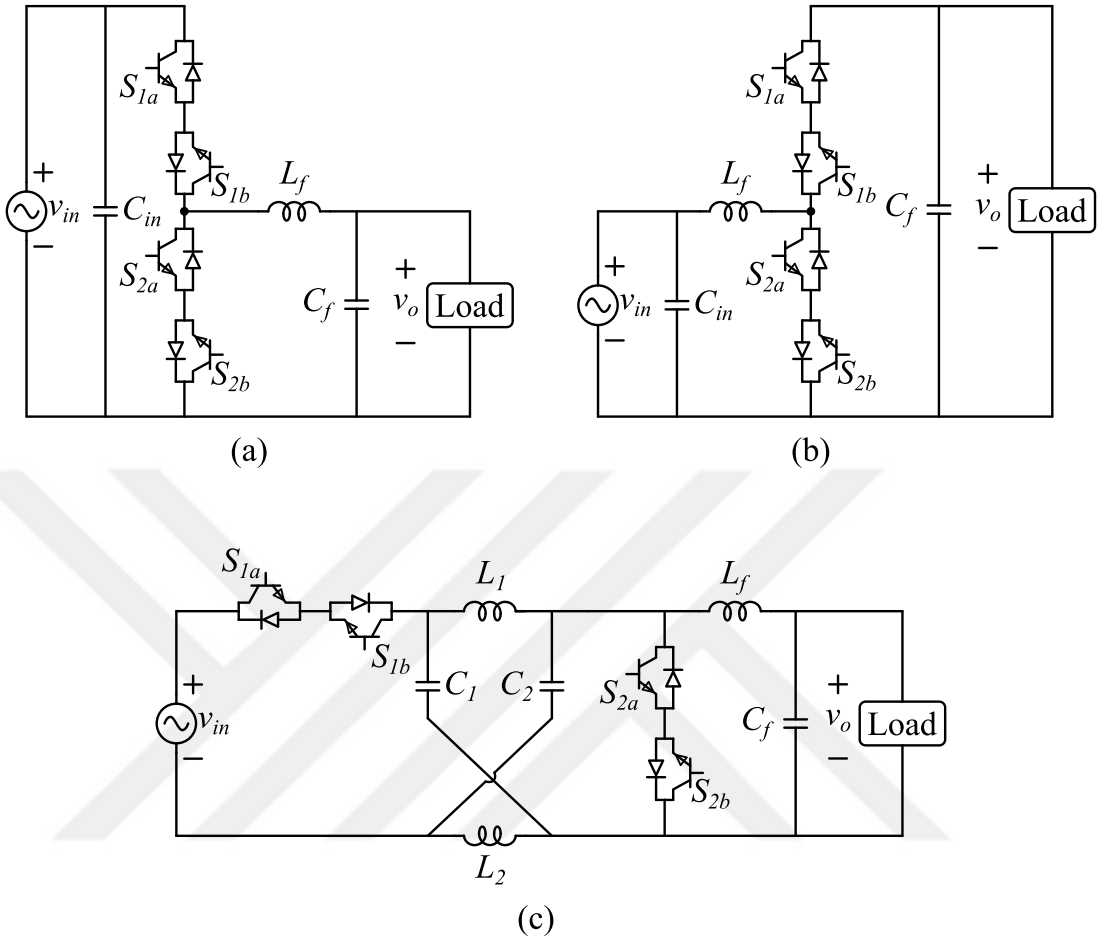


Figure 2.14 Typical SS PWM converter topologies. (a) Buck [31]. (b) Boost [31]. (c) Buck-boost (Z-source) [32].

PWM converters have a wide range of topologies [31], [33]–[46]. The most common SS PWM converters are shown in Figure 2.14. These types of converters provide enhanced performance over cycloconverters. However, they are usually only able to control the output voltage. Nevertheless, with topology advancements, some recent PWM converters with and without switching cells are able to control the output frequency along with the voltage. Further, some of them are able to buck and boost the input voltage while producing inverting and non-inverting output voltage. An inverting output voltage is a voltage out-of-phase with the input voltage, whereas the non-inverting output voltage is in-phase with the input voltage. Converters that provide both inverting and non-inverting output voltage are known to have "bipolar voltage gain." The bipolar gain enables the converters to step up and down the source input

frequency and thus be used in various applications, including dynamic voltage restoration [37], [47]–[49].

SSMCs are able to control both the output voltage and frequency. They have a symmetric bipolar voltage gain, allowing them to step up and down the source input frequency in discrete steps. There are mainly three types of SSMC, shown in Figure 2.15. They are distinguished by their ability to buck, boost, or buck and boost the source input voltage. The conventional topology, shown in Figure 2.15(a), is only able to buck the input voltage [50]. It is worth noting that it is the topology adopted in this thesis. The boost SSMC, shown in Figure 2.15(b), has the same matrix topology, yet with a boost inductor connected in series with the source [51]. Similarly, the Z-source SSMC, shown in Figure 2.15(c), has the same matrix topology, yet with the addition of four passive elements and one bidirectional power switch, which allows it to operate in buck and boost modes [49], [52]. It can be recognized that the bidirectional switches of all topologies in Figure 2.15 are arranged in a matrix form (2×2), which interprets their classification under SSMCs. Nevertheless, sometimes other topologies are referred to as MC due to their ability to control the output voltage, provide a bipolar voltage gain, and step the source frequency up and down, which are the main characteristics of MCs [38], [53], [54]. It is also worth mentioning that the matrix topology allowed MCs not only to be employed as AC choppers but also to be employed as a rectifier [55]–[59] and inverter [60], [61].

The symmetric bipolar voltage gain of SSMCs makes them useful for applications such as dynamic voltage restoration [62]–[64]. Further, their ability to provide waveforms with step-changed frequency makes them useful for several applications, even though these waveforms are not purely sinusoidal. Such applications include traction drive [65], [66], induction heating [67], [68], and AC motor drive [69]. SSMC also got involved in a DC motor drive thanks to its regeneration capability [70]. Further, SSMCs got involved in other systems, such as battery energy storage [71], isolated DC-AC converter [72]–[75], bidirectional battery charger [76], active power filtering [77], energy saving for street lighting [78], and renewable energy [79], [80].

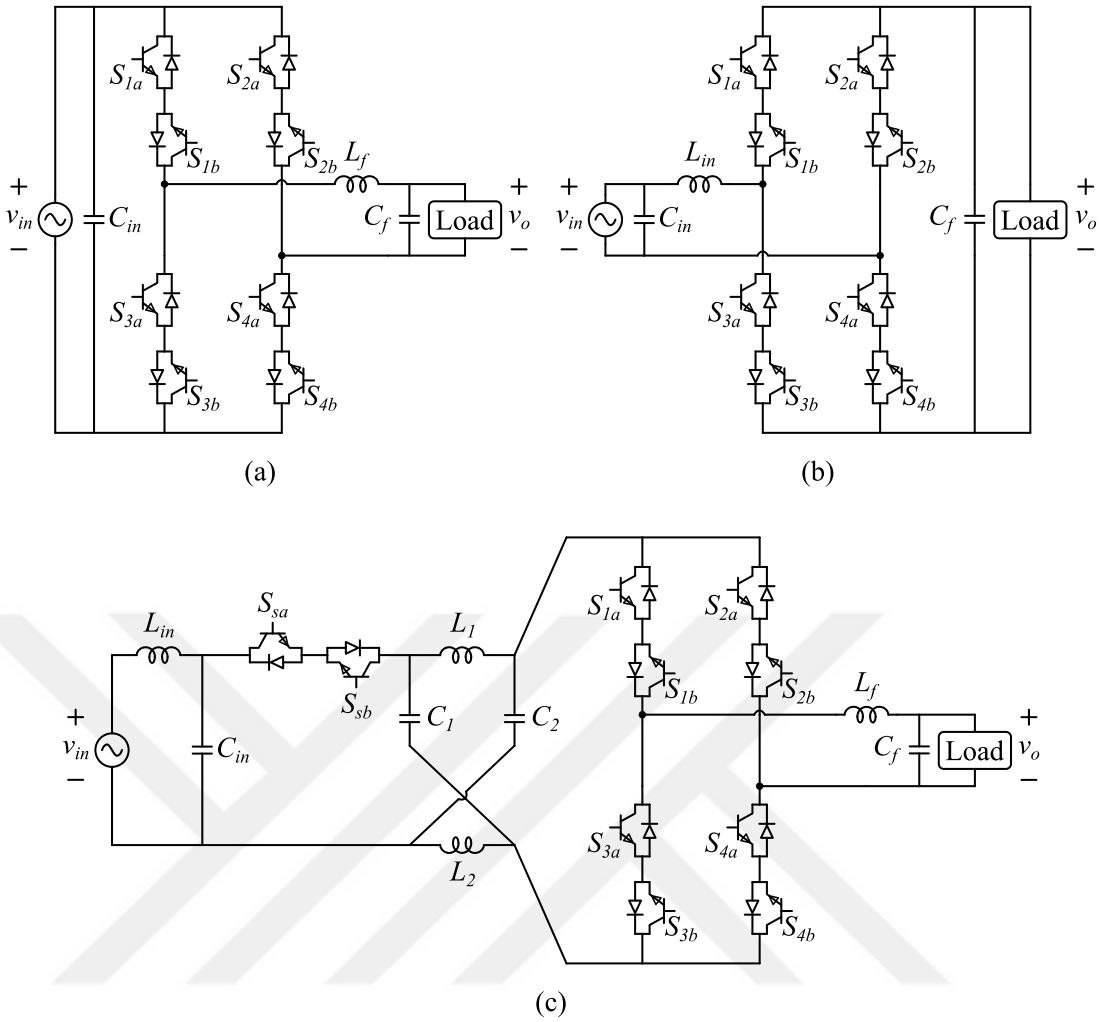


Figure 2.15 Typical SSMC topologies. (a) Buck [50], [81]. (b) Boost [51], [82]. (c) Buck-boost (Z-source) [49], [52].

Other than TTMCs [19], [83]–[86] and SSMCs [50], [81], the matrix topology of MCs allowed them to be modified to realize diverse input-output phases. Such realization includes three-to-single-phase [87]–[89], three-to-five-phase [90], three-to-seven-phase [91], [92], single-to-two-phase [93], and two-to-single-phase [94]–[97].

2.3 Bidirectional Switches

As discussed above, MCs are composed of an array of controlled bidirectional switches that convert energy directly without the help of bulky energy storage components as an intermediary connection. These bidirectional switches are one of the main reasons behind the efficient operation of MCs, and they are the main reason behind their ability to have a bidirectional power flow. Bidirectional switches are characterized by their ability to conduct current and block voltage in both directions. Currently, a single small device that can conduct current and block voltage in both

directions is not commercially available [6], [98]. As a result, bidirectional switches are often constructed by properly coupling discrete unidirectional components.

In the early stages of MCs developments, the bipolar junction transistor was the most often utilized controlled switch [99]. The utilization of other controlled switches, such as metal-oxide-semiconductor field-effect transistors (MOSFETs), gate turn-off thyristors (GTOs), integrated gate commutated thyristors (IGCTs), metal-oxide-semiconductor turn-off thyristor (MTO), and metal-oxide-semiconductor controlled thyristor (MCT), might not be a good choice for MC applications [98]. The limited available blocking voltage of MOSFETs usually confines their utilization to low-power applications, while the switching frequency limitation of GTOs, IGCTs, and MTOs confines their utilization to applications other than MCs. Nevertheless, MCs have been built using MOSFETs in [72], [100]–[102], MTOs in [8], and MCTs in [103], [104].

Most MC applications today employ IGBTs to construct bidirectional switches due to their high voltage blocking and switching capabilities. There are many possible bidirectional switch topologies, where Figure 2.16 depicts the most common ones. The number of IGBTs and diodes might change depending on the topology, and the arrangement of the components changes with the topology. Thus, the losses, gate driver circuits, gate driver power supplies, and control of each topology might change.

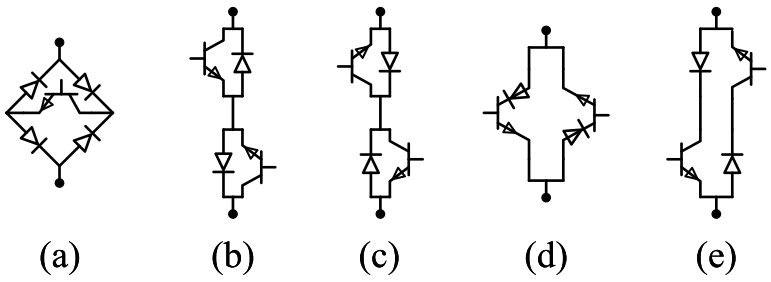


Figure 2.16 Topologies of bidirectional switches: (a) diode bridge (DB), (b) common emitter (CE), (c) common collector (CC), (d) two antiparallel reverse blocking IGBTs (RB-IGBTs), (e) two antiparallel IGBTs in series with diodes.

The DB topology (Figure 2.16(a)) uses one active switching device, thus, only one gate drive circuit is required for each bidirectional switch. However, the conduction losses of this topology are higher than other topologies because the current flows through one switch and two diodes. The same switch conducts both the positive and

negative currents. Therefore, this topology precludes the possibility of applying some commutation techniques (e.g., [105], [106]). It requires one isolated gate driver power supply per switch, therefore a total of nine for TTMC. MC prototypes have been built using this topology in [50], [99]. Topologies consisting of two switching elements can generally control the current flow direction, providing versatility for current commutation.

The CE and CC topologies facilitate bidirectional power control. The CE topology (Figure 2.16(b)) is one of the most commonly used bidirectional switch topologies in MCs. It is worth noting that the CE topology is adopted in this thesis. It is easy to implement and has the ability to control the current direction. Although the conduction losses are not too low in this configuration, it does not need snubber circuits for safe commutation since proper modulation techniques can be applied. It requires one isolated gate drive power supply for each bidirectional switch (a total of nine in TTMC and four in SSMC). The CC topology (Figure 2.16(c)) requires only six isolated gate drive power supplies for TTMC, which makes it cheap and preferable in some applications [107]. However, with SSMC, similar to the CE, the CC topology requires four isolated gate drive power supplies. Nevertheless, the topology of CC is mostly avoided to prevent the issue of parasitic inductances between collectors [108].

The topology of Figure 2.16(d) consists of two antiparallel RB-IGBTs that can conduct current and block voltage in both directions. This configuration has low conduction losses due to the use of only two power devices per bidirectional switch. The switching performance of the intrinsic diode in an RB-IGBT is poor [109]. This topology requires two gate driver circuits per bidirectional switch. This means eighteen and eight gate drive circuits for TTMC and SSMC, respectively. Nevertheless, it only requires six gate drive power supplies for TTMC. For SSMC, it requires four gate drive power supplies.

Although the CC topology has higher conduction losses compared to RB-IGBTs, the switching losses increase rapidly in a MC with RB-IGBTs. In other words, for low switching frequencies (below 25 kHz) a MC with RB-IGBTs might perform better than a MC with CC bidirectional switch configuration [107], [109]. However, the CC configuration might perform better for higher switching frequencies despite the voltage drop on the diodes [107], [109].

For the topology of Figure 2.16(e), the series-connected diodes are essential to support reverse bias due to the lack of reverse blocking capability of conventional IGBTs [110]. However, the series-connected diodes cause additional conduction losses. The gate drive power supplies count required for this topology is the same as the CC topology.

The characteristics of converters, such as switching frequency, voltage, and power ratings, are influenced by advancements in semiconductor device technology. Fast power switches enable the use of high switching frequencies, thus, the filter size can be reduced [105]. Initial research has been conducted to replace IGBTs with junction-gate field-effect transistors (JFETs) made of carbon-silicon since JFET has low losses and can operate at high temperatures [111], [112].

In recent years, bidirectional switches have been made commercially available. An example is the DIM400PBM17-A000 bidirectional switch module made by Dynex Semiconductor, shown in Figure 2.17. Some manufacturers have produced integrated power modules of bidirectional switches for TTMC applications. Some power modules are only for a single-phase leg, as the one depicted in Figure 2.18, which is constructed using 600V/100A RB-IGBTs. Some power modules are manufactured for all the phase-phase legs, as the model in Figure 2.19, which is constructed using CC bidirectional switch configuration, and the model in Figure 2.20, which is constructed using antiparalleled RB-IGBT bidirectional switch configuration.

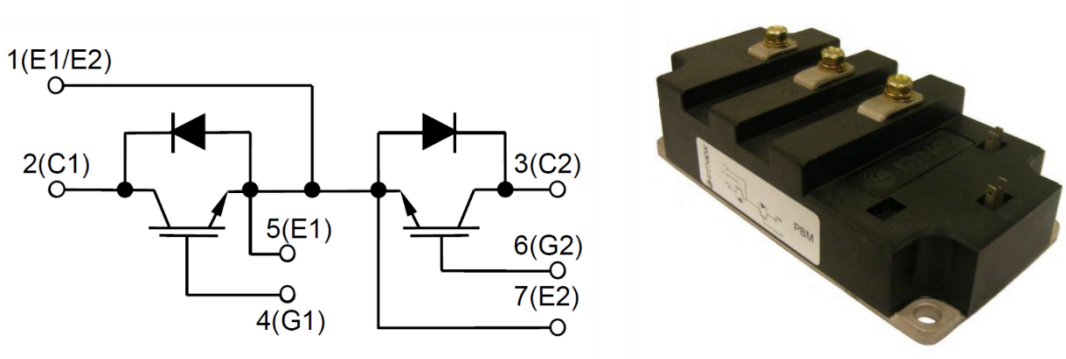
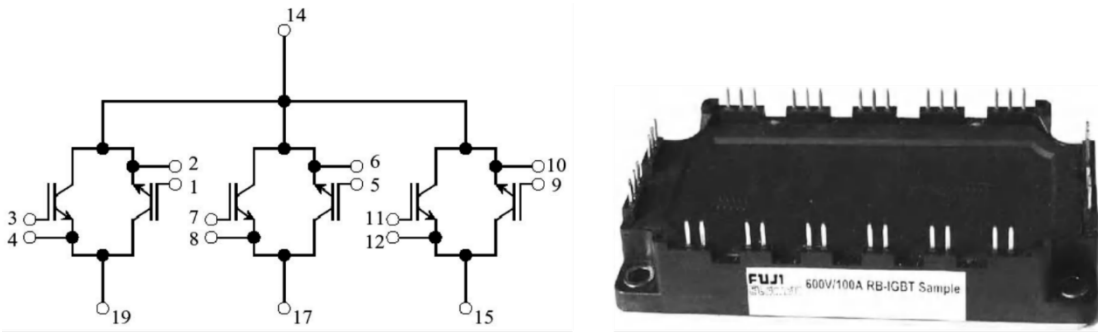
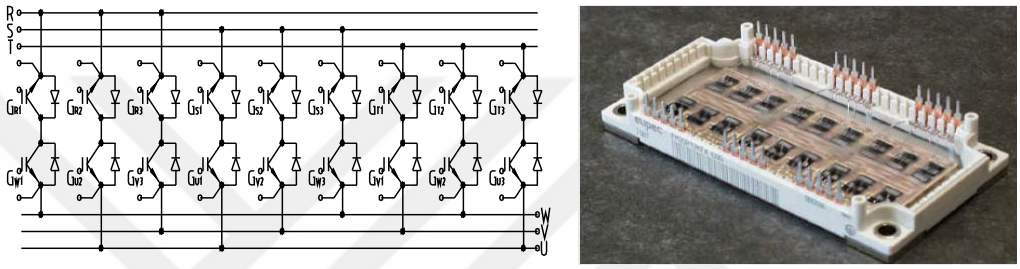


Figure 2.17 A commercially available CE-configured bidirectional switch module: (a) circuit configuration, (b) outside structure [113].



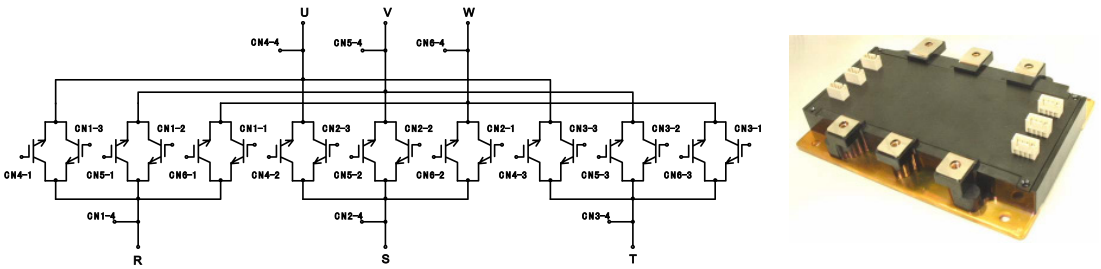
(a) (b)

Figure 2.18 A RB-IGBT-configured bidirectional switch module for a single-phase leg: (a) circuit configuration, (b) outside structure [114], [115].



(a) (b)

Figure 2.19 TTMC module using CC bidirectional switch configuration: (a) circuit configuration, (b) outside structure [116], [117].



(a) (b)

Figure 2.20 TTMC module using RB-IGBT bidirectional switch configuration: (a) circuit configuration, (b) outside structure [118].

2.4 Commutation Problem

In theory, the switching elements in a MC turn ON and OFF instantaneously. However, switches take time to turn ON and OFF in practice due to their inherent characteristics. Moreover, the drive system might have some delays. Unlike indirect AC-DC-AC converters, most MC topologies lack the existence of a freewheeling path that enables safe RL current commutation during dead time or when the PWM signal is low [119]–[122].

When we wish to commutate the current to flow through other switches, if the other switches are triggered while the source/load current continues to conduct through the first switches during their turn-OFF period, a short circuit path can be established which causes current overshoots (di/dt) [106], [123]. On the other hand, with driver delay, during dead time, when the PWM signal is low, or any other moment where no switch is triggered, the RL load current finds no path to flow through, which causes voltage spikes (dv/dt) [106], [123].

Two fundamental rules should be considered for safe current commutation: the RL load current should always find a path to flow through, and the source should not be short-circuited. These commutation rules can be fulfilled using external dissipative circuits or by adopting modulation strategies. In [69], [124], snubber and clamp circuits are used, and in [54], [65], [125]–[128], modulation strategies are adopted. Figure 2.21 shows a general overview of snubber and clamp circuits. Snubber and clamp circuits increase the number of components in the circuit and the losses. Modulation strategies, on the other hand, increase the control complexity.

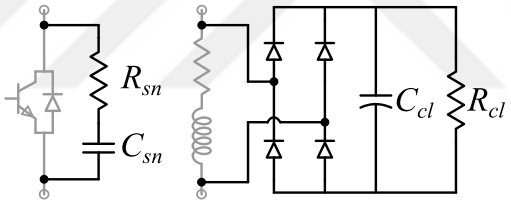


Figure 2.21 Typical topologies of (a) snubber and (b) clamp circuits.

2.5 Overvoltage Protection

In a conventional two-stage converter, there exist rectifier diodes, a DC-link capacitor, and inverter freewheeling diodes. All of these components contribute to the circuit protection. However, this is not the case with direct MCs, as they do not possess a freewheeling path, nor do they have a DC-link capacitor. This, in turn, increases the complexity of the protection system [129].

Many sources can suscept MCs to overvoltage, such as grid perturbation, faults at the load terminals, and driver system faults. To deal with the overvoltage issue, clamp circuits (shown in Figure 2.21(b)) are usually used [130], [131]. A clamp circuit consists of a bridge rectifier that is connected to a capacitor paralleled with a resistor.

The rectifier converts the overvoltage from AC to DC so that the capacitor can store it. The resistor, on the other hand, discharges the capacitor voltage and limits the maximum clamping current. In this way, the capacitor and resistor maintain the voltage at a safe level. Bridge rectifiers are connected across the source and load terminals to overcome the overvoltage from both the source and RL load. The capacitor and resistor are usually shared between the source and load rectifiers [132], [133]. Two types of capacitors are usually used in the clamp circuit: electrolytic and polypropylene, where the electrolytic capacitor is used to store the bulk energy while the polypropylene capacitor is used for transient response [99]. It is important to keep the capacitor voltage rating below the rating of the other devices in the circuit [69]. The use of voltage clamp circuits allows for the use of low voltage rating IGBTs, and lower snubber capacitor magnitude [99]. The clamp circuit energy can be used to power up other auxiliary circuits in the system, such as gate drives and transducers [99], [134]. In [99], powering the gate drive circuits using the clamp circuit energy improved the efficiency by 1%.

Usually, in the case where all switches are turned OFF (e.g., fault in the drive system, emergency shut OFF, etc.), the RL load (e.g., motor) current finds no path to flow through, which breaks the commutation rules discussed above. In this way, the energy stored in the RL load can cause serious overvoltage problems. With the existence of a clamp circuit at the RL load terminal, this issue can be solved. The RL load current finds a path through the clamp circuit, thus, discharging its energy. This solution is effective, however, it requires a relatively large number of passive components, especially with TTMCs.

Another method that protects the converter from overvoltage is connecting a varistor across the source and load terminals. This approach reduces the passive components in the system and has negligible losses during normal operation conditions, however, it may cause issues with delayed voltage blocking [130], [131]. The use of varistors for overvoltage protection usually accompanies the use of additional circuits to protect each power switch in order to increase the reliability and life span of the MC. A general structure of power switch protection circuits is depicted in Figure 2.22. The Z-diode is a suppressor diode with a breakdown voltage that is less than the maximum blocking voltage of the power switch [130], [131]. Assuming that the power switch is an IGBT,

then if the collector-emitter voltage raises above the Z-diode breakdown voltage, the Z-diode gets activated, clamping the IGBT to the clamping voltage of the Z-diode. At that time, a short but high current pulse is given to the gate of the IGBT, turning it ON to operate in the non-saturated region. In this way, current passes through the IGBT collector-emitter terminals eliminating the destructive collector-emitter overvoltage.

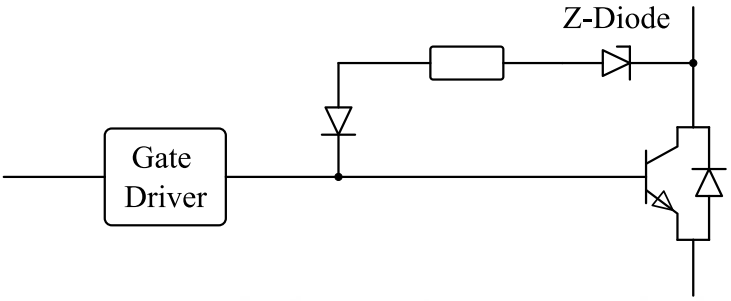


Figure 2.22 A single IGBT protection circuit using suppressor diode [130], [131].

2.6 Control Techniques

The direct conversion of the source power needs to be controlled in MCs in order to obtain the desired output power. To do that, the triggering activity of the power switches needs to be controlled. Such a control can be performed by means of control techniques. The utilized control technique determines the performance profile of the MC. This includes the VTR and THD of the waveforms. Figure 2.23 shows a general classification of the control techniques for MCs [135], [136]. Some of these techniques are dedicated to TTMCs. In general, the control methods can be categorized as PWM techniques, scaler techniques, and other closed-loop control techniques [135], [136]. PWM techniques include carrier-based techniques [137]–[139] and the space vector modulation technique [19], [86], [140]–[143]. Scaler techniques include the direct transfer function technique [144]–[146], indirect transfer function technique [99], [147], and Roy scaler technique [148]. Other control techniques include predictive current control [87], [149]–[152], predictive torque control [153]–[155], sliding mode control [156], and direct torque control [157]–[160].

Carrier-based PWM techniques are one of the simplest and most effective techniques to control MCs. They have the ability to generate several pulses in each half-cycle of the output waveform, which decreases harmonic contents and increases harmonic frequencies to decrease the size and expense of filters. Controlling SSMCs is mostly performed using these techniques. They generate gate-triggering pulses by comparing

a reference signal with a high-frequency carrier signal. Carrier-based PWM techniques include SPWM, MPWM, SCPWM, and TPWM.

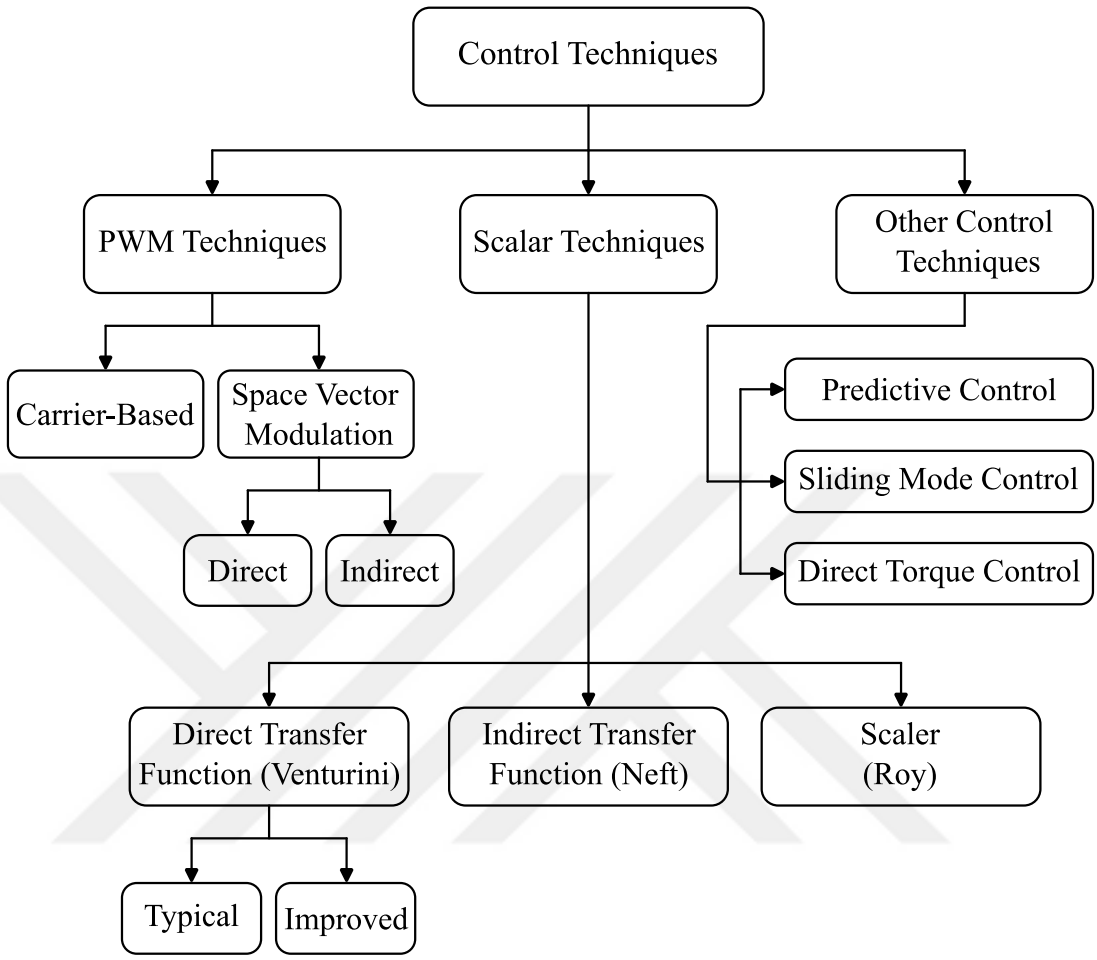


Figure 2.23 Commonly utilized control techniques for MCs.

SSMCs are usually closed-loop controlled using two methods. The first method, depicted in Figure 2.24, is by measuring the source current or load voltage/current and comparing it with the reference value to generate the error. Then, feeding the error to a proportional-integral (PI) controller and using the output of the PI controller as a reference signal in the modulation process. Using this approach, the input current is controlled in [161], and the output voltage is controlled in [162]. The second method, depicted in Figure 2.25, is by detecting the peak output voltage/current [163], [164] and comparing it with the peak reference value to generate the error. Then, similar to the latter method, feed the error to a PI controller to minimize it and use the generated control reference signal in the modulation process. This approach is implemented in [34], [42], [53] by detecting the output voltage peak value and in [165] by detecting the output current peak value.

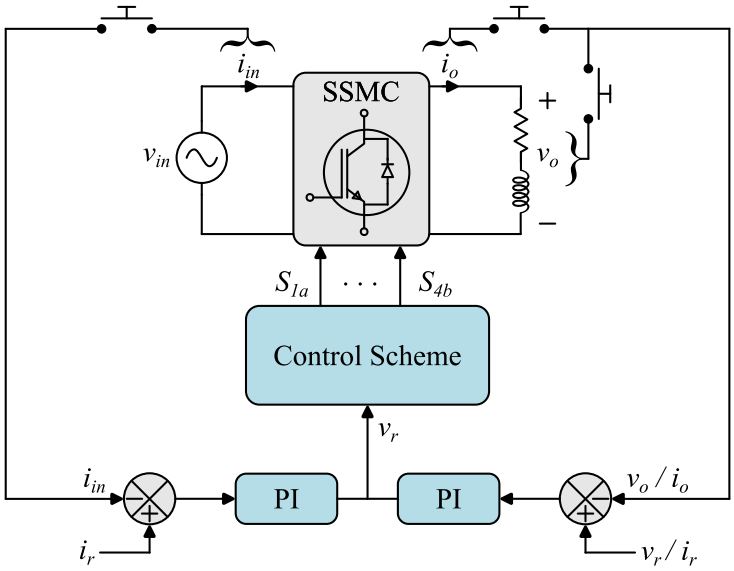


Figure 2.24 General structure of SSMC source current or load voltage/current closed-loop control scheme.

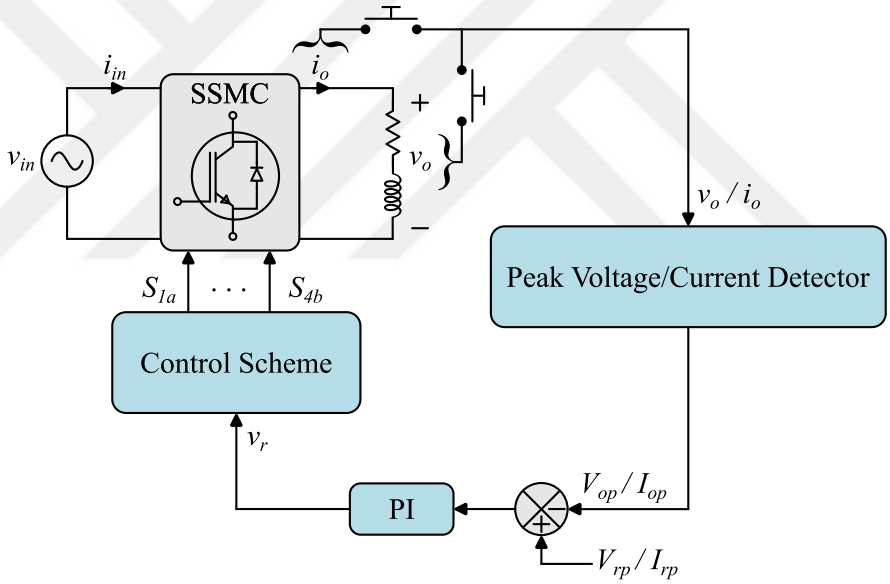


Figure 2.25 General structure SSMC load voltage/current peak value detection-based closed-loop control scheme.

2.7 Conclusion

In this chapter, first, a brief background about TT and SS AC-AC converters is given. In this context, the characteristics that make MCs a preferred choice for AC-AC conversion are explained. Then, the different topologies of bidirectional switches, which are one of the main reasons behind the ability of MCs to provide symmetric bipolar voltage gain and to have bidirectional power flow, are discussed along with the pros and cons of each topology in terms of gate drive requirements and losses.

Later, the commutation problem which is encountered by MCs when connected to RL load, is discussed along with the commonly used solutions. Then, the protection of MCs against overvoltage, which is caused by many reasons, including grid perturbation, lack of RL load freewheeling path, and driver system faults, is discussed along with the commonly utilized protection approaches. Finally, the commonly employed control techniques to regulate the switching activity of the bidirectional power switches and the overall performance of the MC are briefly presented.

CHAPTER 3
OPERATION AND CONTROL OF SINGLE-TO-SINGLE-PHASE MATRIX CONVERTER

3.1 Introduction

This chapter presents the operation and control of SSMC operating as an AC-AC converter. First, the SSMC step-changed frequency operation is investigated. In that context, the adopted four-step safe current commutation strategy is discussed. Then, mathematical representations of the output voltage are presented. Finally, the principle of several carrier-based PWM techniques is examined to control the SSMC output voltage in open-loop operation conditions.

3.2 Frequency Conversion

SSMCs can step-change the source frequency in discrete steps by proper triggering of the power switches. The conventional direct SSMC topology, shown in Figure 2.15(a), has mainly four operation states, shown in Figure 3.1, enabling the topology to achieve symmetric bipolar voltage gain. In each state, a particular pair of switches is activated. In state 1 (Figure 3.1(a)), S1a and S4a are activated, allowing the current to flow in the forward direction to generate positive output during the positive half-cycle of the source. In state 2 (Figure 3.1(b)), S2a and S3a are activated, allowing the current to flow in the reverse direction to generate negative output during the positive half-cycle of the source. In state 3 (Figure 3.1(c)), S3b and S2b are activated, allowing the current to flow in the forward direction to generate positive output during the negative half-cycle of the source. In state 4 (Figure 3.1(d)), S4b and S1b are activated, allowing the current to flow in the reverse direction to generate negative output during the negative half-cycle of the source.

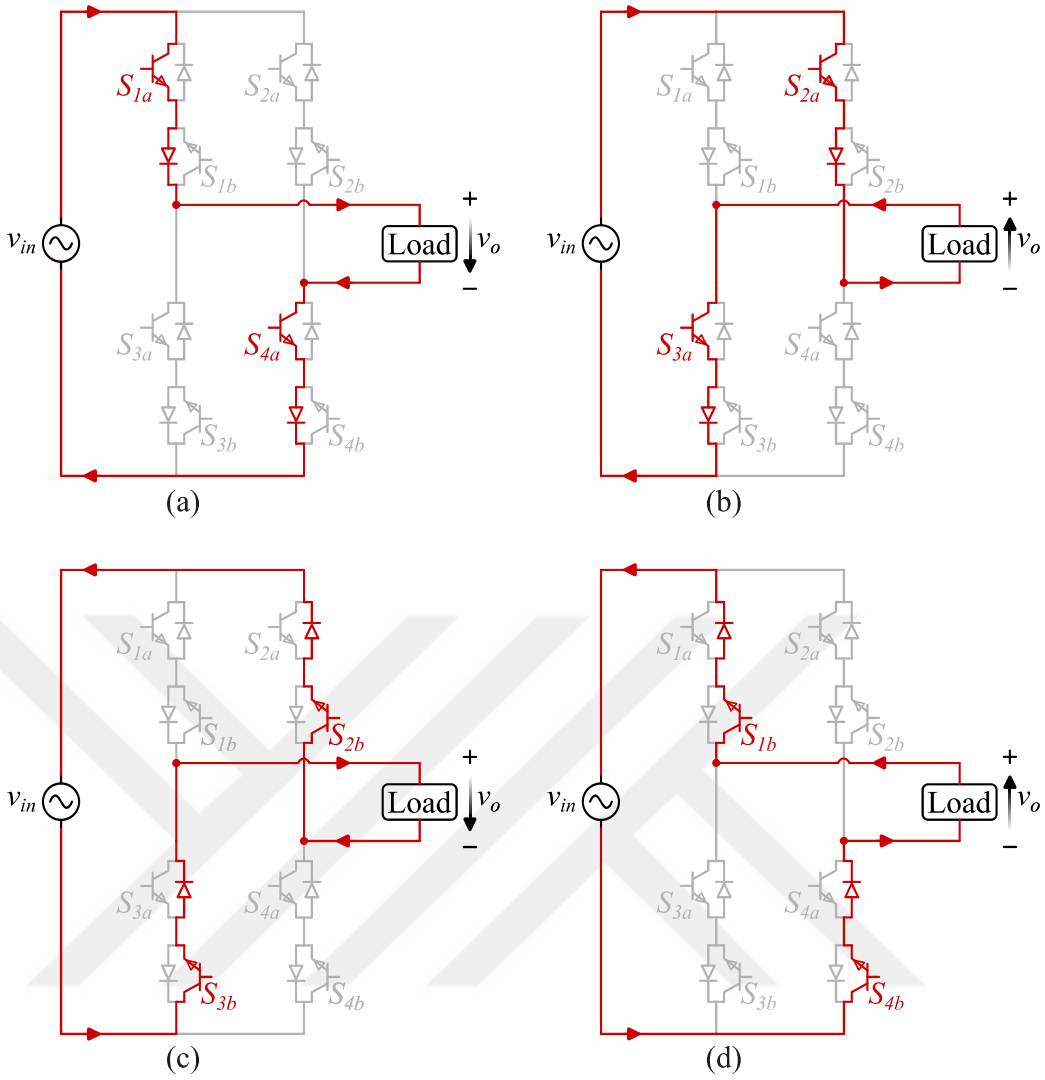


Figure 3.1 Operation states of SSMC. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

Generating an output with an acceptable waveform requires ensuring that its frequency is an integer multiple or a fraction of the source voltage frequency. In this thesis, the source sinusoidal waveform of 50 Hz is converted to 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz. The number of source waveform half-cycles needed to synthesize the desired output waveform can be determined using equation (3.1).

$$q = \frac{f_{in}}{f_o} \times 2 \tag{3.1}$$

Where f_{in} and f_o are the frequency of the input and output waveforms, respectively.

Eight half-cycles of the source waveform ($q = 8$) are required to synthesize an output frequency of 12.5 Hz. Therefore, during the first four half-cycles of the source waveform, the output waveform is positive and negative during the next four half-

cycles. Thus, the SSMC operates at states 1 and 3 during the first four half-cycles of the source waveform and at states 2 and 4 during the other four half-cycles.

Four half-cycles of the source waveform ($q = 4$) are required to synthesize an output frequency of 25 Hz. Therefore, during the first two half-cycles of the source waveform, the output waveform is positive and negative during the next two half-cycles. Thus, the converter operates at states 1 and 3 during two half-cycles of the source waveform and at states 2 and 4 during the other two half-cycles.

Two half-cycles of the source waveform ($q = 2$) are required to synthesize an output frequency of 50 Hz. Therefore, during the first half-cycle of the source waveform, the output waveform is positive, and it is negative during the next half-cycle. Thus, the converter operates at state 1 during one half-cycle of the source waveform and at state 4 during the other half-cycle.

One half-cycle of the source waveform ($q = 1$) is required to synthesize an output frequency of 100 Hz. Therefore, during the first half-half-cycle of the source waveform, the output waveform is positive and negative during the next half-half-cycle. Thus, the converter operates at states 1 and 2 during the first half-cycle of the source waveform when it is positive and at states 3 and 4 during the other half-cycle when the source waveform is negative.

Two-thirds half-cycle of the source waveform ($q = 2/3$) is required to synthesize an output frequency of 150 Hz. Therefore, during the first one-third half-cycle of the source waveform, the output waveform is positive, and it is negative during the next one-third half-cycle. Thus, the SSMC operates at states 1 and 2 during the first half-cycle of the source waveform and at states 3 and 4 during the other half-cycle.

One-third half-cycle of the source waveform ($q = 1/3$) is required to synthesize an output frequency of 300 Hz. Therefore, during the first one-sixth half-cycle of the source waveform, the output waveform is positive and negative during the next one-sixth half-cycle. Thus, the converter operates at states 1 and 2 during the first half-cycle of the source waveform and at states 3 and 4 during the other half-cycle.

The above switching states are sufficient to drive a purely resistive load. However, as discussed in Section 2.4, most loads in practice are RL. Therefore, a freewheeling path

should be provided for the RL load current during the dead time or when the PWM signal is low in order to drive an inductive load without current commutation problems. This freewheeling path can be provided through an external circuit or by adopting a proper commutation strategy, as discussed in Section 2.4. Commutation strategies provide a freewheeling path by proper switching of the power switches. In this thesis, the four-step current commutation strategy illustrated in Figure 3.2 is employed. The dead time t_{d1} is added between the high-frequency PWM switching signals for the lower switches (S3a, S3b, S4a, and S4b) and t_{d2} is added between the switching signals for the upper switches (S1a, S1b, S2a, and S2b). To ensure uninterruptible RL load current, t_{d2} is kept relatively small.

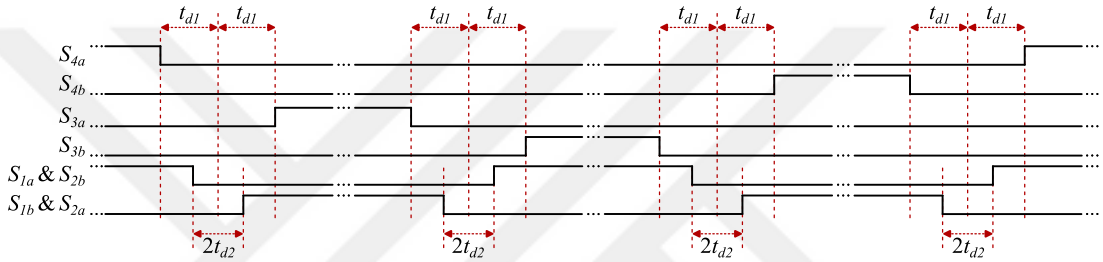


Figure 3.2 Safe current commutation strategy.

In this thesis, a freewheeling path is provided by activating one more switch in every state. Therefore, a total of three switches are activated in each switching state. The summary of the SSMC switching strategies to step-change the source input frequency while connected to an RL load is shown in Figure 3.3 to Figure 3.8. In the figures, D is the duty ratio and T_{sw} is the switching period. The switching states of the SSMC for step-changed frequency operation are given in Table 3.1.

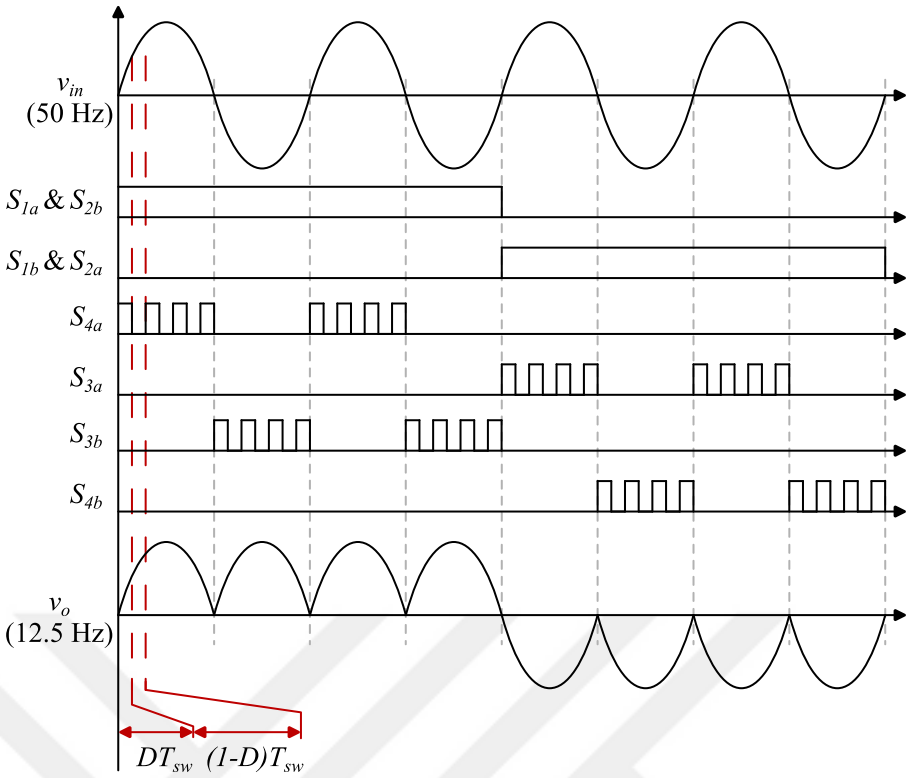


Figure 3.3 Switching strategy and key waveforms for 12.5 Hz output frequency.

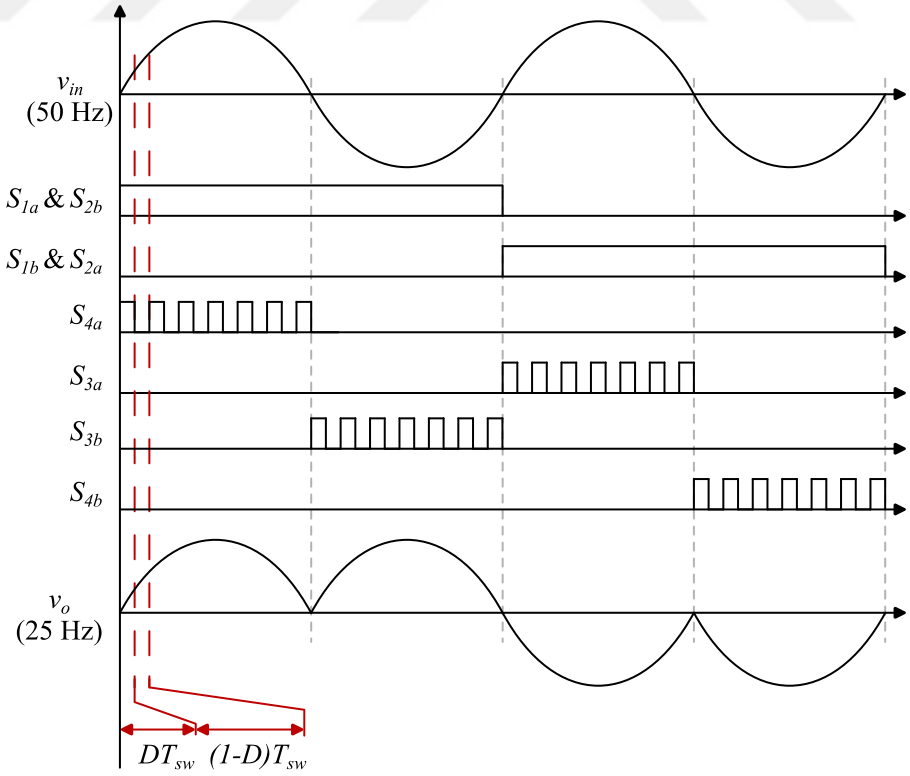


Figure 3.4 Switching strategy and key waveforms for 25 Hz output frequency.

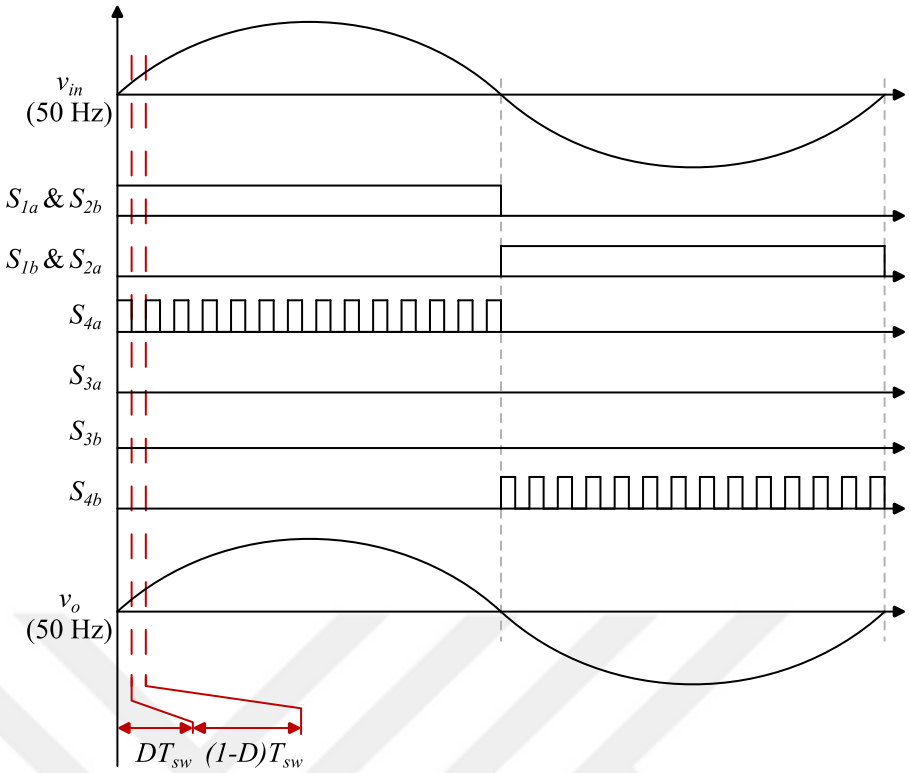


Figure 3.5 Switching strategy and key waveforms for 50 Hz output frequency.

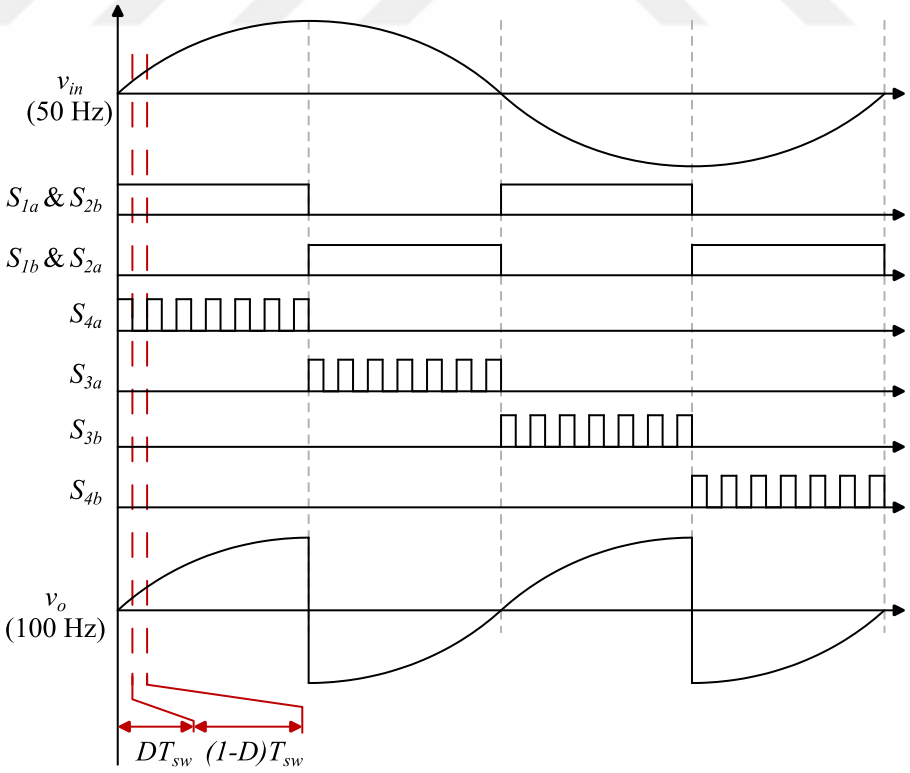


Figure 3.6 Switching strategy and key waveforms for 100 Hz output frequency.

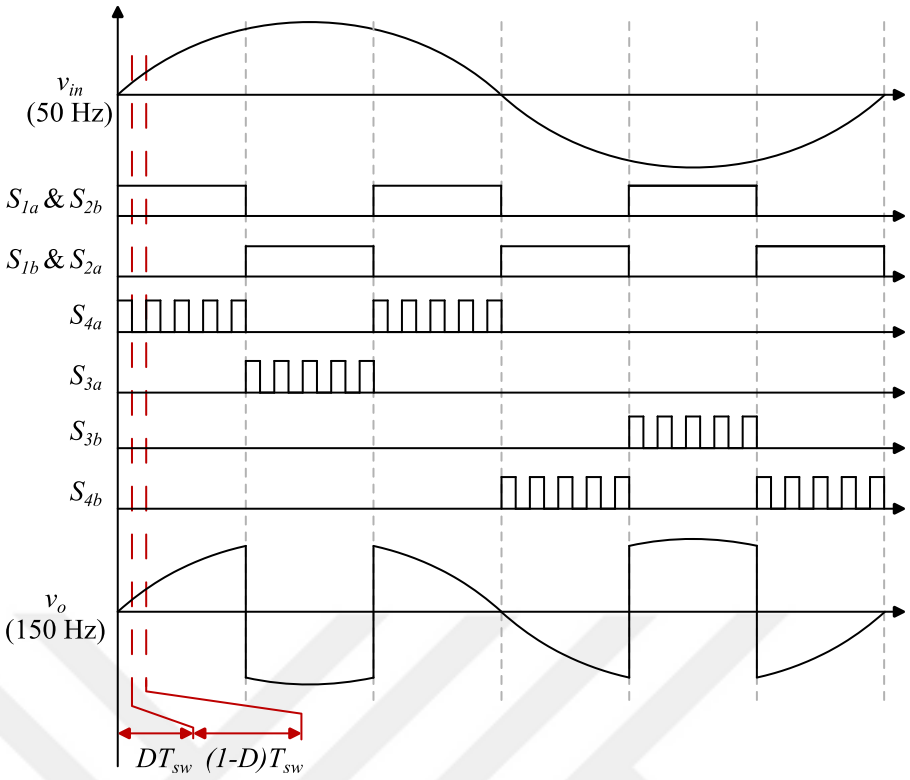


Figure 3.7 Switching strategy and key waveforms for 150 Hz output frequency.

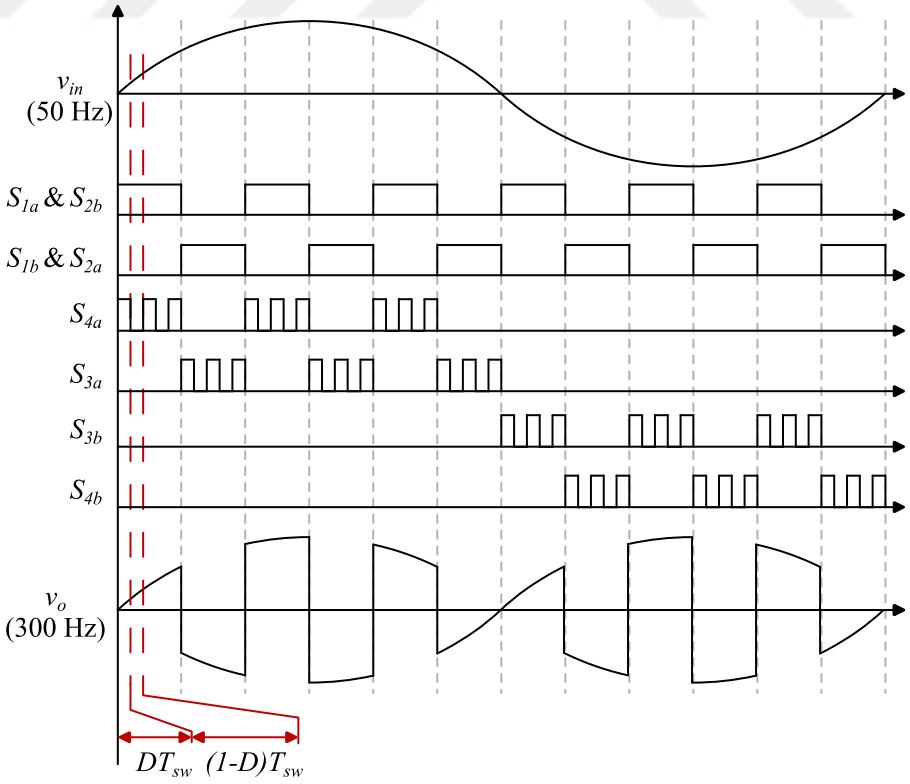


Figure 3.8 Switching strategy and key waveforms for 300 Hz output frequency.

Table 3.1 Switching states of SSMC for step-changed frequency operation with source frequency of 50 Hz.

f_o (Hz)	State	Trigger Pulses							
		S_{1a}	S_{1b}	S_{2a}	S_{2b}	S_{3a}	S_{3b}	S_{4a}	S_{4b}
12.5	1	1	0	0	1	0	0	1	0
	3	1	0	0	1	0	1	0	0
	1	1	0	0	1	0	0	1	0
	3	1	0	0	1	0	1	0	0
	2	0	1	1	0	1	0	0	0
	4	0	1	1	0	0	0	0	1
	2	0	1	1	0	1	0	0	0
	4	0	1	1	0	0	0	0	1
25	1	1	0	0	1	0	0	1	0
	3	1	0	0	1	0	1	0	0
	2	0	1	1	0	1	0	0	0
	4	0	1	1	0	0	0	0	1
50	1	1	0	0	1	0	0	1	0
	4	0	1	1	0	0	0	0	1
100	1	1	0	0	1	0	0	1	0
	2	0	1	1	0	1	0	0	0
	3	1	0	0	1	0	1	0	0
	4	0	1	1	0	0	0	0	1
150	1	1	0	0	1	0	0	1	0
	2	0	1	1	0	1	0	0	0
	1	1	0	0	1	0	0	1	0
	4	0	1	1	0	0	0	0	1
300	3	1	0	0	1	0	1	0	0
	4	0	1	1	0	0	0	0	1
	1	1	0	0	1	0	0	1	0
	2	0	1	1	0	1	0	0	0
	1	1	0	0	1	0	0	1	0
	2	0	1	1	0	1	0	0	0
	1	1	0	0	1	0	0	1	0
	2	0	1	1	0	1	0	0	0
	3	1	0	0	1	0	1	0	0
	4	0	1	1	0	0	0	0	1
	3	1	0	0	1	0	1	0	0
	4	0	1	1	0	0	0	0	1
	3	1	0	0	1	0	1	0	0
	4	0	1	1	0	0	0	0	1

The root mean square (RMS) value of the output voltage V_o may vary depending on the synthesized output frequency f_o. For a sinusoidal source voltage of (3.2), the output voltage can be represented as in (3.3).

$$v_{in}(t) = A_{in}\sin(\omega_{in}t) \tag{3.2}$$

$$v_o(t) = A_o\sin(\omega_o t) \tag{3.3}$$

Where t represents time, ω_{in} and ω_o are the angular frequencies and A_{in} and A_o are the voltage amplitudes of the source and load, respectively. The voltage amplitudes of the source and load can be represented as flows:

$$A_{in} = \sqrt{2}V_{in} \tag{3.4}$$

$$A_o = \sqrt{2D}V_{in} \tag{3.5}$$

where V_{in} and V_o are the RMS values of the source and load voltages, respectively. The unfiltered pulsating output signal has an amplitude equal to the amplitude of the input signal. Nevertheless, the RMS value of the output signal depends on the duty ratio.

In an ideal case, where there is no voltage drop across any semiconductor device in the circuit, for an output frequency of 12.5 Hz, the RMS value of the output voltage can be represented as in (3.6).

$$V_o = \left[\frac{D}{\pi}\int_0^{\pi}\left(\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t)\right]^{\frac{1}{2}} \tag{3.6}$$
$$V_o = \sqrt{D}V_{in}$$

For an output frequency of 25 Hz, the RMS value of the output voltage can be represented as in (3.7).

$$V_o = \left[\frac{D}{\pi}\int_0^{\pi}\left(\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t)\right]^{\frac{1}{2}} \tag{3.7}$$
$$V_o = \sqrt{D}V_{in}$$

For an output frequency of 50 Hz, the RMS value of the output voltage can be represented as in (3.8).

$$V_o = \left[\frac{D}{\pi}\int_0^{\pi}\left(\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t)\right]^{\frac{1}{2}} \tag{3.8}$$
$$V_o = \sqrt{D}V_{in}$$

For an output frequency of 100 Hz, the RMS value of the output voltage can be represented as in (3.9).

$$V_o = \left[\frac{D}{\pi}\left[\int_0^{\frac{\pi}{2}} \left(\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t) + \int_{\frac{\pi}{2}}^{\pi} \left(-\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t)\right]\right]^{\frac{1}{2}} \tag{3.9}$$

$$V_o = \sqrt{D}V_{in}$$

For an output frequency of 150 Hz, the RMS value of the output voltage changes every output period due to the nature of the source waveform, as shown in Figure 3.7. For the first cycle, the RMS value of the output voltage can be represented as in (3.10), and for the second cycle, the RMS value of the output voltage can be represented as in (3.11).

$$V_o = \left[\frac{D}{2\pi/3}\left[\int_0^{\frac{\pi}{3}} \left(\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t) + \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} \left(-\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t)\right]\right]^{\frac{1}{2}} \tag{3.10}$$

$$V_o = \left[\frac{3DV_{in}^2}{2\pi}\left(\frac{2\pi}{3} + \frac{\sqrt{3}}{4}\right)\right]^{\frac{1}{2}}$$

$$V_o = \left[\frac{D}{2\pi/3}\left[\int_{\frac{2\pi}{3}}^{\frac{4\pi}{3}} \left(\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t)\right]\right]^{\frac{1}{2}} \tag{3.11}$$

$$V_o = \left[\frac{3DV_{in}^2}{2\pi}\left(\frac{2\pi}{3} + \frac{\sqrt{3}}{2}\right)\right]^{\frac{1}{2}}$$

For an output frequency of 300 Hz, the RMS value of the output voltage changes every output period due to the nature of the source waveform, as shown in Figure 3.8. For the first cycle, the RMS value of the output voltage can be represented as in (3.12), for the second cycle, the RMS value of the output voltage can be represented as in (3.13), and for the third cycle, the RMS value of the output voltage can be represented as in (3.14).

$$V_o = \left[\frac{D}{\pi/3}\left[\int_0^{\frac{\pi}{6}} \left(\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t) + \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} \left(-\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t)\right]\right]^{\frac{1}{2}} \tag{3.12}$$

$$V_o = \left[\frac{3DV_{in}^2}{\pi}\left(\frac{\pi}{3} - \frac{\sqrt{3}}{4}\right)\right]^{\frac{1}{2}}$$

$$V_o = \left[\frac{D}{\pi/3}\left[\int_{\frac{\pi}{3}}^{\frac{\pi}{2}} \left(\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t) + \int_{\frac{\pi}{2}}^{\frac{2\pi}{3}} \left(-\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t)\right]\right]^{\frac{1}{2}} \tag{3.13}$$

$$V_o = \left[\frac{3DV_{in}^2}{\pi}\left(\frac{\pi}{3} + \frac{\sqrt{3}}{2}\right)\right]^{\frac{1}{2}}$$

$$V_o = \left[\frac{D}{\pi/3}\left[\int_{\frac{2\pi}{3}}^{\frac{5\pi}{6}} \left(\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t) + \int_{\frac{5\pi}{6}}^{\pi} \left(-\sqrt{2}V_{in}\sin(\omega t)\right)^2 d(\omega t)\right]\right]^{\frac{1}{2}} \tag{3.14}$$

$$V_o = \left[\frac{3DV_{in}^2}{\pi}\left(\frac{\pi}{3} - \frac{\sqrt{3}}{4}\right)\right]^{\frac{1}{2}}$$

Therefore, a general representation of the RMS value of the output voltage can be given in (3.15).

$$V_o = \begin{cases} [DV_{in}^2]^{\frac{1}{2}}, & f_o \leq 100 \text{ Hz} \\ \left[\frac{3DV_{in}^2}{2\pi}\left(\frac{2\pi}{3} + \frac{\sqrt{3}}{4}\right)\right]^{\frac{1}{2}}, & f_o = 150 \text{ Hz for } 0 \leq \omega t \leq 2\pi/3 \\ \left[\frac{3DV_{in}^2}{2\pi}\left(\frac{2\pi}{3} + \frac{\sqrt{3}}{2}\right)\right]^{\frac{1}{2}}, & f_o = 150 \text{ Hz for } 2\pi/3 \leq \omega t \leq 4\pi/3 \\ \left[\frac{3DV_{in}^2}{\pi}\left(\frac{\pi}{3} - \frac{\sqrt{3}}{4}\right)\right]^{\frac{1}{2}}, & f_o = 300 \text{ Hz for } 0 \leq \omega t \leq \pi/3 \text{ and } 2\pi/3 \leq \omega t \leq \pi \\ \left[\frac{3DV_{in}^2}{\pi}\left(\frac{\pi}{3} + \frac{\sqrt{3}}{2}\right)\right]^{\frac{1}{2}}, & f_o = 300 \text{ Hz for } \pi/3 \leq \omega t \leq 2\pi/3 \end{cases} \tag{3.15}$$

3.3 Open-Loop Control

The direct conversion of source power needs to be controlled in order to obtain the desired output power. This can be achieved by controlling the triggering pulses of the power switches. Carrier-based PWM techniques are one of the most effective and easy-to-implement techniques to control the triggering pulses of the SSMCs. These techniques include SPWM, MPWM, SCPWM, and TPWM. They are based on comparing a high-frequency carrier signal with a reference signal to generate switching patterns. The ratio between the reference signal amplitude A_r to the carrier signal amplitude A_{cr} is defined as the modulation index, which can be represented in (3.16).

$$m_a = \frac{A_r}{A_{cr}} \tag{3.16}$$

By manipulating the modulation index ($m_a = D$), the triggering pulse width can be altered, thus, the converter output voltage can be controlled.

A typical pulsating output voltage waveform with equal pulse width is illustrated in Figure 3.9. Generally, multiple pulses are generated within each half-cycle of the output voltage to decrease harmonic contents and increase harmonic frequencies, thereby decreasing the size and cost of filtering. The number of pulses in each half-cycle P, is mainly determined by the frequency of the carrier signal and the occupied modulation technique.

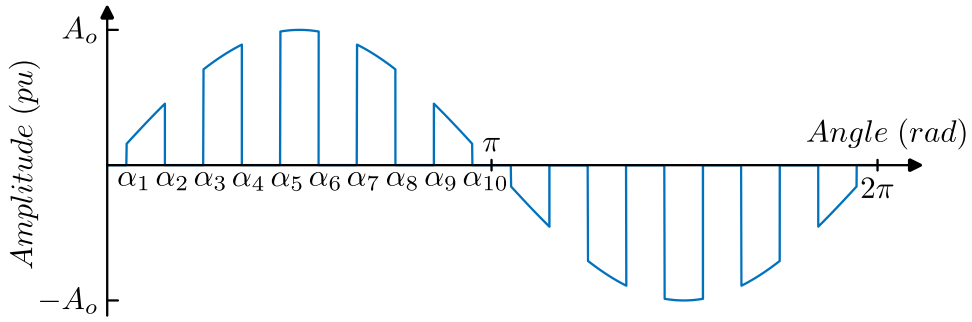


Figure 3.9 Typical SSMC output voltage waveform.

Using Fourier series, the output voltage can be expressed as in (3.17).

$$v_o(\omega t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} [a_n \cos(n\omega t) + b_n \sin(n\omega t)] \tag{3.17}$$

Where n is the harmonic order, ω is the angular frequency, and the Fourier series coefficients can be expressed as in (3.18).

$$\begin{cases} a_0 = \dfrac{1}{\pi}\left[\displaystyle\int_0^{2\pi} v_o(\omega t)\, d(\omega t)\right] \\ a_n = \dfrac{1}{\pi}\left[\displaystyle\int_0^{2\pi} v_o(\omega t)\cos(n\omega t)\, d(\omega t)\right] \\ b_n = \dfrac{1}{\pi}\left[\displaystyle\int_0^{2\pi} v_o(\omega t)\sin(n\omega t)\, d(\omega t)\right] \end{cases} \tag{3.18}$$

Due to the half-wave symmetry of the output voltage along the x-axis, (3.17) can be expressed as in (3.19).

$$v_o(\omega t) = \sum_{i=1}^{\infty} b_n \sin(n\omega t) \tag{3.19}$$

The Fourier coefficient for a pair of pulses, if the positive pulse of the ith pair begins at $\omega t = \alpha_i$ and ends at $\omega t = \alpha_{i+1}$, can be expressed as in (3.20).

$$b_n = \frac{1}{\pi}\left[\int_{\alpha_i}^{\alpha_{i+1}} v_o(\omega t)\sin(n\omega t)\, d(\omega t) + \int_{\pi+\alpha_i}^{\pi+\alpha_{i+1}} v_o(\omega t)\sin(n\omega t)\, d(\omega t)\right] \tag{3.20}$$

Or, by reorganizing (3.20), the magnitude of the harmonics components can be expressed as in (3.21).

$$b_n = \frac{A_o}{\pi}\left[\sum_{i=0}^{P-1}\left[\frac{\sin\left(\alpha_{2i+2}(n-1)\right) - \sin\left(\alpha_{2i+1}(n-1)\right)}{n-1} - \frac{\sin\left(\alpha_{2i+2}(n+1)\right) - \sin\left(\alpha_{2i+1}(n+1)\right)}{n+1}\right]\right] \tag{3.21}$$

Where α_i is the ith switching angle, which ranges from zero to $P-1$, where P depends on the switching frequency and the occupied modulation technique.

In SSMCs, zero-voltage switching (ZVS) is achieved by turning ON and OFF the power switches when the voltage across them (collector-emitter voltage) is zero. Ensuring ZVS reduces the stress on the switches and eliminates the output voltage spikes at the commutation instances. As depicted in Figure 3.3 to Figure 3.8, with

direct SSMC, ZVS at the commutation instances can only be ensured with synthesized output frequencies lower than or equal to the source frequency. This is due to the inherent waveform characteristics of the AC source. Nevertheless, an appropriate modulation technique can ensure ZCS at the commutation instances for synthesized output frequencies higher than the source input frequency. The ZCS is achieved by ensuring that the triggering pulses (gate-emitter voltage) of the switching elements are OFF or maintained at a low duty ratio during the commutation instances. This ensures that the energy of the RL load is maintained low, thus, the current direction can be reversed. The RL load should be gradually discharged at the commutation instances to ensure ZCS. This is crucial in mitigating output voltage spikes at the commutation instances, reducing power losses, and preventing damage to the switching elements. Modulation techniques that do not ensure ZCS at the commutation instances require dissipative circuits that store and discharge the excessive RL load energy during commutation. A clamp circuit is one of the most utilized circuits for this purpose.

The carrier signals used in the modulation process can be mainly divided into two categories, one with an amplitude range between -1 and 1 per unit ($v_{cr(-11)}$) and one with an amplitude range between 0 and 1 per unit ($v_{cr(01)}$). Both carrier signals are represented as follows:

$$v_{cr(-11)}(t) = 2\left|2\left(\frac{t}{T_{cr}} - \left\lfloor\frac{t}{T_{cr}} + \frac{1}{2}\right\rfloor\right)\right| - 1 \tag{3.22}$$

$$v_{cr(01)}(t) = 2\left|\frac{t}{T_{cr}} - \left\lfloor\frac{t}{T_{cr}} + \frac{1}{2}\right\rfloor\right| \tag{3.23}$$

Where T_{cr} is the fundamental period of the carrier signal and $\lfloor\ \rfloor$ represents the floor function. Using $v_{cr(-11)}$ limits the variation in the performance parameters with the change of the modulation index. Additionally, it inhibits the SSMC from achieving the minimum possible VTR, limiting flexibility over the output parameters. On the other hand, $v_{cr(01)}$ firms the grasp over the SSMC performance parameters, enabling it to achieve the maximum and minimum possible VTRs. Achieving ZCS at the commutation instances depends on both the carrier and reference signals. With $v_{cr(-11)}$, it is not possible to achieve ZCS since even at zero modulation index, relatively high duty ratio pulses are generated at the commutation instances. On the other hand, $v_{cr(01)}$ can achieve achieving ZCS at the commutation instances

depending on the utilized reference signal. The frequency of the reference signal is set according to (3.24).

$$f_r = \begin{cases} 2f_{in}, & \text{for } f_o \leq f_{in} \\ 2f_o, & \text{for } f_o > f_{in} \end{cases} \tag{3.24}$$

Where f_r is the frequency of the reference signal. The following subsections discuss the principle of the carrier-based PWM techniques under consideration in this thesis.

3.3.1 SPWM

The SPWM is a widely used technique to control the conventional direct SSMC topology for open-loop operation [72]–[75], [81], [127], [166]–[170]. This technique is not able to provide the maximum possible VTR with unity modulation index due to the occupied sinusoidal reference signal. Nevertheless, it can ensure ZCS for output frequencies higher than the source frequency. Therefore, no clamp circuit is needed when utilizing the SPWM technique. However, a clamp circuit might be needed when synthesizing output frequencies higher than three times the source frequency. The reference and carrier signals used to realize this technique are depicted in Figure 3.10. The sinusoidal reference signal is compared with the triangular carrier signal, and if, at any time, the amplitude of the reference signal A_r is greater than or equal to that of the carrier signal A_{cr}, an ON gate pulse is generated. Otherwise, an OFF gate pulse is generated.

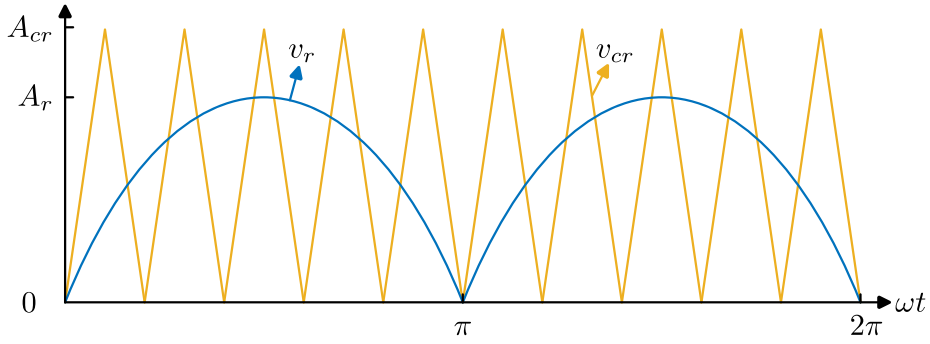


Figure 3.10 Reference and carrier signals utilized to realize the SPWM technique.

3.3.2 MPWM

The MPWM technique utilizes a constant reference signal v_r to generate the PWM triggering pulses, as shown in Figure 3.11. This technique offers the distinct advantage of providing the maximum and minimum possible VTRs thanks to the occupied

reference and carrier signals. Nevertheless, the utilized reference signal inhibits achieving ZCS for output frequencies higher than the source frequency. Therefore, this technique requires a clamp circuit to store and discharge the excessive energy by the RL load when synthesizing output frequencies higher than the source frequency. This technique is utilized in [68], [69], [171].

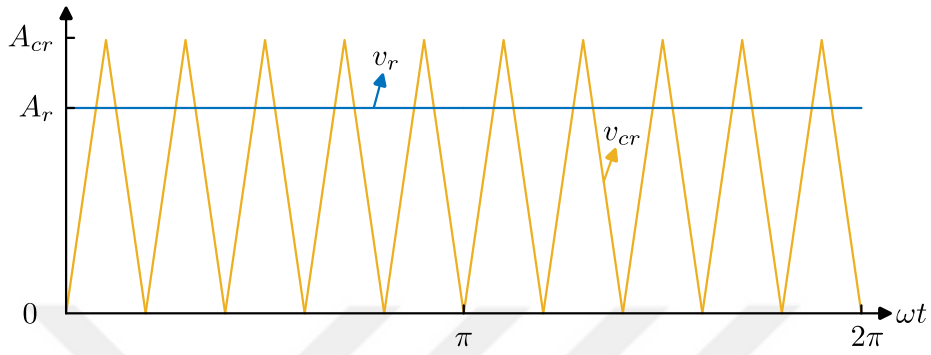


Figure 3.11 Reference and carrier signals utilized to realize the MPWM technique.

3.3.3 SCPWM

The SCPWM technique utilizes a staircase reference signal v_r to generate the PWM triggering pulses, as shown in Figure 3.12. The nature of the reference signal this technique occupies, along with the carrier signal, enables this technique to achieve relatively high VTRs while ensuring ZCS for output frequencies higher than the source frequency. Staircase signals can take on numerous waveforms depending on the number of stairs and the rise time of each stair. A single-stair signal can be further subdivided into three time components: low time t_l, middle time t_m, and high time t_h. The fundamental period of the staircase reference signal T_{sca} is formed by summing all the time components as in (3.25).

$$T_{sca} = t_l + t_m + t_h \tag{3.25}$$

The higher the number of stairs and the higher the duration of the stairs (t_m), the more gradually the RL load is discharged, and therefore, the more ZCS is ensured at the commutation instances. However, as t_l and t_m increase beyond the necessary threshold, a proportionally greater amount of voltage is excised from the output voltage, thus lowering the VTR. It is also worth noting that the higher t_h is, the more voltage is transferred to the output terminals. By adjusting the staircase waveform time components, this technique can eliminate the need for a clamp circuit while achieving relatively high VTRs. This modulation technique is utilized in [172], [173].

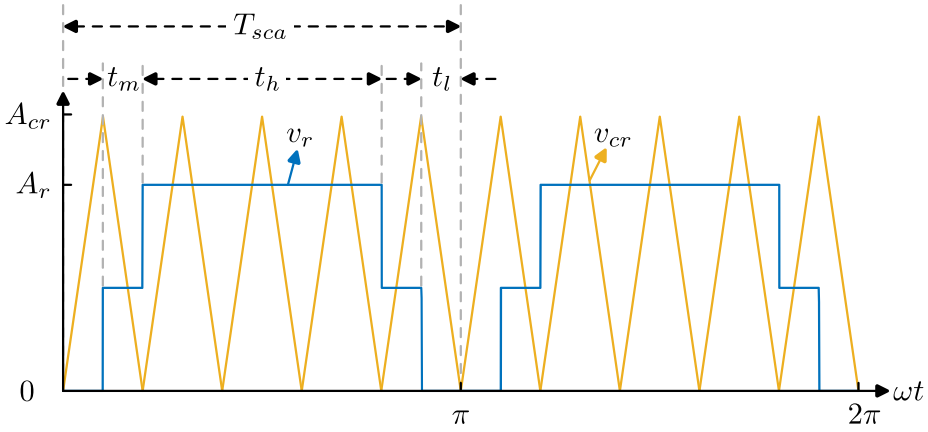


Figure 3.12 Reference and carrier signals utilized to realize the SCPWM technique.

3.3.4 TPWM

The TPWM technique utilizes a trapezoidal reference signal v_r to generate the PWM triggering pulses, as shown in Figure 3.13. The nature of the reference signal allows this technique to achieve relatively high VTRs while ensuring ZCS for output frequencies higher than the source frequency. However, it exhibits limitations in voltage transfer when operating with frequencies that exceed the source frequency. This issue can be solved by adjusting the ratio between the rise t_r and fall t_f to high time t_h. The smaller the ratio, the more voltage is transferred, however, the less chance to maintain ZCS. Excessive details on this modulation technique are presented in Section 4.2. This modulation technique is utilized in [174]–[176].

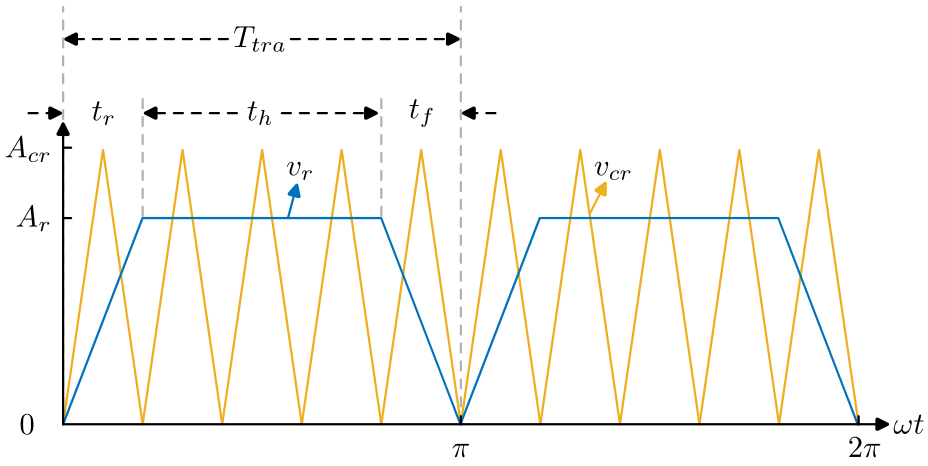


Figure 3.13 Reference and carrier signals utilized to realize the TPWM technique.

3.4 Conclusion

This chapter demonstrated the step-changed frequency and voltage control operations of the SSMC. First, the SSMC operation states are presented, where the ability of the

SSMC to generate symmetric bipolar voltage gain is demonstrated. Then, the switching strategies of the SSMC for step-changed frequency operation are illustrated. Later, the principles of several carrier-based PWM techniques are discussed to control the output voltage.

CHAPTER 4
THE PROPOSED CONTROL METHOD FOR SSMC

4.1 Introduction

This chapter describes the proposed control method for SSMCs. In this context, the importance of utilizing an adjustable trapezoidal reference waveform in the modulation process is addressed. Moreover, the importance of performing the commutation operation when the RL load is discharged is discussed. The ability of the trapezoidal signal to discharge the RL load to achieve safe current commutation and avoid output voltage spikes during commutation while being able to provide relatively high VTRs is highlighted. Furthermore, the ability of the proposed control scheme to adapt to any carrier-based PWM technique is discussed. Later, the proposed synchronization algorithm is presented. Finally, the key advantages and contributions of the proposed SSMC control method are highlighted.

4.2 Description of the Proposed SSMC Control Method

In general, the RMS values of the input and output voltages can be related to each other using the expression of (4.1), where it can be recognized that the topology under consideration in this thesis serves as a buck converter.

$$V_o = \sqrt{D} V_{in} \tag{4.1}$$

The VTR, which plays a significant role in determining the reliability of MCs, can be expressed in (4.2).

$$\text{VTR} = \frac{V_o}{V_s} \tag{4.2}$$

From (4.1) and (4.2), it should be recognized that the VTR should be equal to $\sqrt{D}$, however, this relation is hard to achieve without the expense of affecting other performance parameters. This is one of the main disadvantages of the topology under consideration. Moreover, as shown in (3.15), for output frequencies higher than three

times the source frequency, V_o cannot be equal to V_{in} due to the direct power conversion.

The generalized structure of the proposed control scheme is shown in Figure 4.1, where v_{p1} and v_{p2} are pulse signals that have the frequency of the source f_{in}, and v_{com1} and v_{com2} are commutation signals that have the frequency of the synthesized output signal f_o. The source voltage is compared to the ground voltage in order to generate pulse signals (v_{p1} and v_{p2}) that are synchronized with the source. When working with frequency conversion, the SSMC power switches need to be triggered at specific instants depending on the synthesized output frequency f_o. To synchronize the PWM triggering signals with the sinusoidal source, v_{com1} and v_{com2} needs also to be synchronized with the source. It is quite challenging to do that since the latter signals may have a frequency other than the source voltage frequency f_{in}. To achieve synchronization between v_{com1} and v_{com2} and the source, the top part of Figure 4.1 comes into play, which will be explained later in this section.

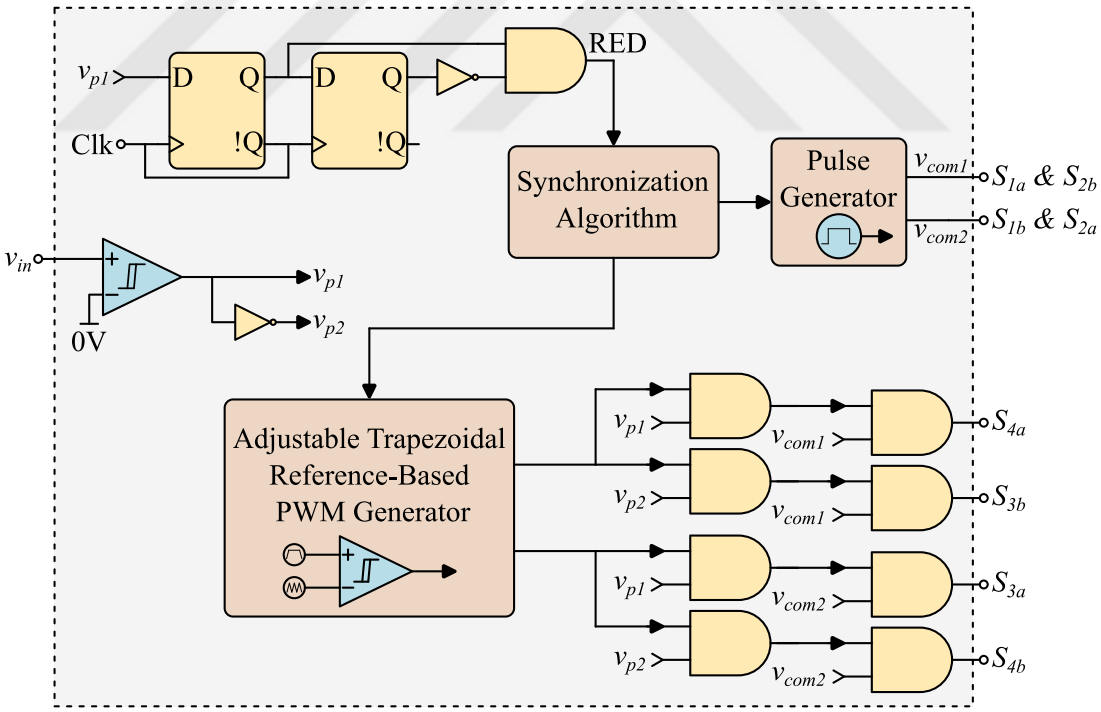


Figure 4.1 Block diagram of the proposed SSMC control scheme.

The proposed control method utilizes an adjustable trapezoidal signal, depicted in Figure 4.2, as the reference signal to control the modulation process. This trapezoidal signal can be divided into three components, namely, rise time t_r, high time t_h, and

fall time t_f. During t_h, the signal remains at its highest level defined by m_a. The signal increases and decreases linearly from zero to m_a during t_r and from m_a to zero during t_f, respectively. The sum of these three components is the fundamental period of the trapezoidal signal T_{tra} which can be represented in (4.3).

$$T_{tra} = t_r + t_h + t_f \tag{4.3}$$

For a symmetrical waveform, the rise and fall components should satisfy the condition of (4.4).

$$t_r = t_f \tag{4.4}$$

It should be noted that the frequency of the trapezoidal reference signal f_{tra} depends on the fundamental frequency of the synthesized output signal f_o as expressed in (4.5). To synthesize one cycle of an output signal having a frequency higher than the source frequency f_{in}, two cycles of the trapezoidal reference signal of Figure 4.2 are required.

$$f_{tra} = \begin{cases} 2f_{in}, & \text{for } f_o \leq f_{in} \\ 2f_o, & \text{for } f_o > f_{in} \end{cases} \tag{4.5}$$

A triangular signal is acquired when $t_r = t_f = T_{tra}/2$ implying that $t_h = 0$, whereas a square wave signal is acquired when $t_r = t_f = 0$. In any other scenario, a trapezoidal waveform is acquired [177]. The trapezoidal signal of Figure 4.2 can be represented in (4.6).

$$v_{tra}(t) = \begin{cases} m_a \dfrac{t}{t_1}, & 0 \leq t < t_1 \\ m_a, & t_1 \leq t < t_2 \\ m_a \dfrac{t + t_2 - t_3}{t_2 - t_3}, & t_2 \leq t < t_3 \end{cases} \tag{4.6}$$

Generally, with SSMC, ZVS of the power switches at the commutation instances is achieved for synthesized output frequencies lower than or equal to the source frequency. Nevertheless, ZVS at the commutation instances is not achieved for output frequencies higher than the source frequency due to the inherent characteristic of the source AC waveform. Alternatively, ZCS at the commutation instances can be achieved for output frequencies higher than the source frequency by ensuring that no PWM pulse is sent to the switches at the commutation instances or that the pulse width is too small. In this way, we ensure that the RL load is discharged and the load current

direction will not be reversed. Ensuring ZCS significantly mitigates the output voltage spikes during commutation. Achieving ZCS depends on the carrier and reference signals utilized in the carrier-based PWM technique. Carrier signals that range between -1 and 1 per unit cannot ensure ZCS because the duty ratio of the PWM signal stays relatively high even at zero modulation index. On the other hand, carrier signals that range between 0 and 1 per unit can ensure ZCS when an adequate reference signal is utilized. A sinusoidal reference signal can achieve ZCS as its amplitude passes through zero and gradually increase/decrease near the zero crossing points, providing a relatively low pulse width of the switching PWM signal at the zero crossing points. However, a sinusoidal reference signal is not able to extract the maximum voltage out of the SSMC, resulting in low VTRs. In contrast, the reference signal should stay at the maximum level (1 per unit) as a square wave to obtain the maximum possible VTR. However, this comes with the expense of hard switching because ZCS is not ensured for $f_o > f_{in}$. Thus, the output voltage signal will present spikes at the commutation instances. Therefore, a combination between the square and sinusoidal signals, so called trapezoidal, is utilized. A staircase reference signal with low steps' height near the commutation instant may discharge the RL load and ensure ZCS. However, it may not provide the maximum VTR. Therefore, utilizing trapezoidal waveform as a reference signal for carrier-based PWM enables extracting the maximum performance out of the SSMC while mitigating output voltage spikes at the commutation instances. Nevertheless, relatively small values of t_r and t_f might not mitigate output voltage spikes, and large values inhibit extracting the maximum performance. The ratio between t_r and t_f to t_h is defined as in (4.7).

$$k = \frac{t_r}{t_h} = \frac{t_f}{t_h} \tag{4.7}$$

The value of k depends on many parameters, including the load inductance, output frequency, source voltage, and load power. The reference signal associated with the proposed method is an adjustable trapezoidal signal. Meaning that by adjusting k, the trapezoidal reference signal can be adjusted to adapt the system parameters and operating conditions to obtain the desired results. If the amplitude of the trapezoidal signal of Figure 4.2 bounces between $-m_a$ and m_a, when t_r and t_f are equal to zero (k = 0) and $t_h = T_{tra}$ (square wave), the fundamental frequency component is equal to $4/\pi$ = 1.27, and when $t_r = t_f$ and t_h is equal to zero (triangular wave), the fundamental

frequency component is equal to $8/\pi^2 = 0.81$. Therefore, by controlling k, the fundamental frequency component of the output voltage and the THD of the output waveforms can be controlled. Therefore, k should be chosen objectively depending on the power, frequency, and load of the system. With the increase of f_o, it is better for k to decrease in order to mitigate the voltage spikes. This is because with the increase of f_o, ensuring ZCS at the commutation instances becomes harder because adequate RL loads require more time to be discharged. There should be no current commutation problems when the SSMC is connected to a purely resistive load, thus, k can be set to zero ensuring a constant reference signal having an amplitude equal to m_a in order to achieve the maximum VTR.

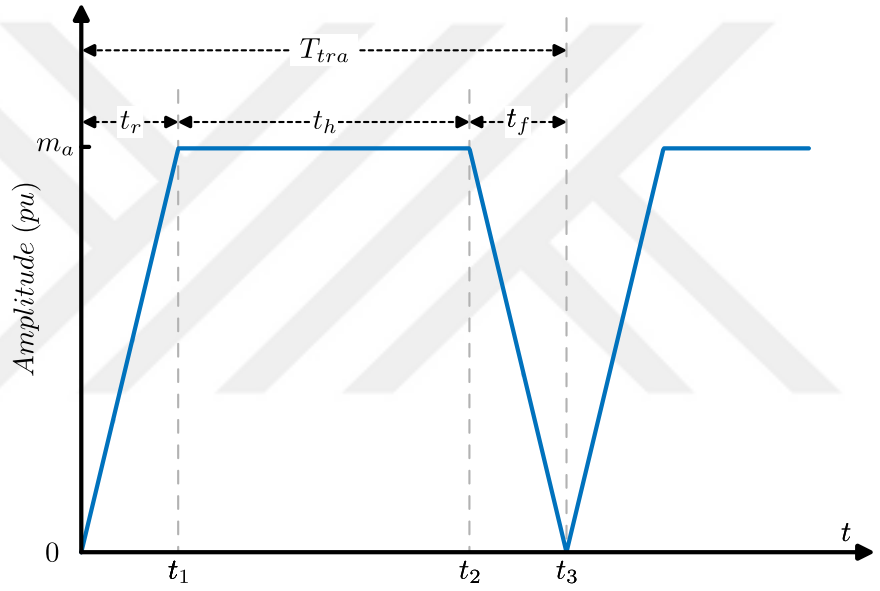


Figure 4.2 General structure of a trapezoidal reference signal.

The carrier signal v_{cr} associated with the proposed method is a triangular signal of (3.23). Since this carrier signal ranges between 0 and 1 per unit, it allows for a wide range of control over the output parameters, unlike the carrier signal of (3.22), whose amplitude ranges between -1 and 1 per unit. Employing the carrier signal of (3.23) thereby firms the grasp over the output power.

In the proposed method, three switches are triggered at each state, but only two switches conduct current simultaneously. In order to minimize the switching losses of the semiconductor switches, only one switch is triggered with a high-frequency PWM signal, and the other two switches are triggered with a relatively low-frequency pulse signal of v_{com1} and v_{com2}. The lower switches (S3a, S3b, S4a, and S4b) are dedicated

to PWM signals, and the upper switches (S1a, S1b, S2a, and S2b) to v_{com1} and v_{com2} signals. One switch of the upper switches is used to conduct current, and the other one is used to provide a freewheeling path for the RL load current, as depicted in Figure 3.3 to Figure 3.8.

Synchronizing the PWM generator unit with the AC source is extremely important. Otherwise, undesired output waveforms will be obtained, and the source may get short-circuited. In order to achieve synchronization, the proposed method utilizes the zero-crossing detection (ZCD) along with the rising-edge detection (RED) principles. The ZCD circuit converts the sinusoidal source voltage into a pulse signal (v_{p1}) that is high when the source waveform is in its positive half cycle and low when the source waveform is in its negative half cycle. In this way, a pulse signal having the source frequency is generated that indicates the state of the source. Nevertheless, this ZCD signal is not enough for synchronization when stepping up and down the source frequency. Therefore, a RED circuit is employed. As the name indicates, the RED circuit detects the rising instant of the source waveform. The pulse signal generated by the ZCD circuit v_{p1} is supplied to the RED circuit, which generates a small high ('1') pulse indicating the beginning (zero-crossing point) of the source waveform. In other words, the RED signal stays low during the source period, and when the source starts a new cycle, it becomes high for a very short time. The RED circuit in this work is implemented using a field programmable gate array (FPGA). Therefore, the short high time period is determined by the master clock period of the FPGA. The generated RED signal is then processed using the synchronization algorithm shown in Figure 4.3 where T_o represents the fundamental period of the output signal. The FPGA is programmed to reset the modules when the reset signal is low ('0'). This synchronization algorithm synchronizes the PWM signals and the commutation signals (v_{com1} and v_{com2}), which have a frequency of the synthesized output frequency f_o, with the source (grid). This synchronization method also takes into account variations in the source frequency f_{in}, which is a critical point, especially when the SSMC is connected directly to the grid, where small signal disturbances can fluctuate the line frequency. The proposed synchronization method takes into account the variations in the source frequency f_{in} by resetting the FPGA modules every source cycle for $f_o \geq f_{in}$ and every output cycle $f_o < f_{in}$. The term g in the proposed synchronization method of Figure 4.3 is added to compensate for the delay in the ZCD

circuit, driver circuits, and PWM generator unit. Moreover, adding the term g helps with distorted source waveforms where the ZCD circuit can wrongly detect the zero crossing points of the AC voltage source. The value of g is determined based on many factors, including the RMS value of the source voltage, distortion amount of source voltage, load power, and the speed of the ZCD circuit and PWM generator unit. In this study, it is taken as 20 ns.

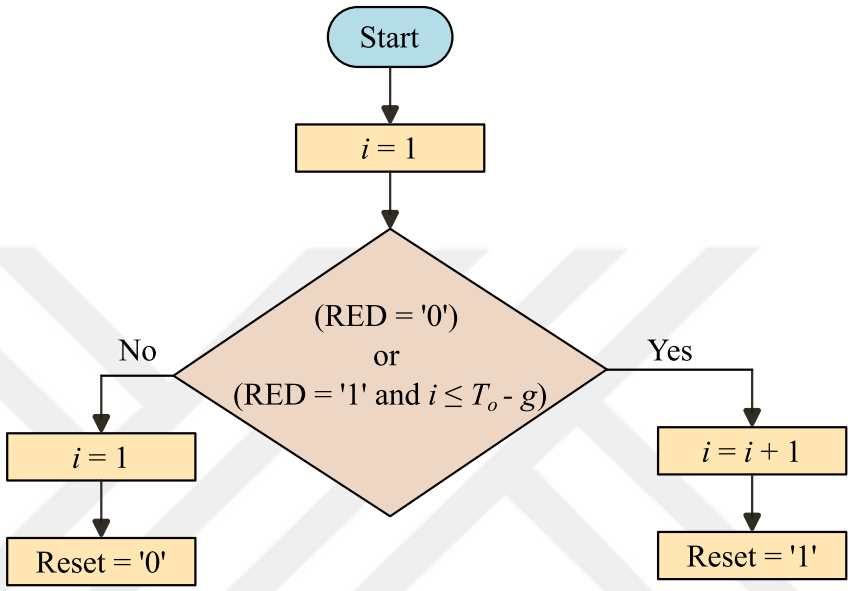


Figure 4.3 Flowchart of the proposed synchronizing algorithm.

4.3 Key Contributions

In Section 4.2, the proposed SSMC control method is described. The method offers multiple significant features compared to existing methods in the literature. The main contributions of the proposed control method are as follows:

1. Compared with the counterpart control methods in the literature, the proposed method allows for maximum utilization of the source voltage by enabling the SSMC to achieve relatively high VTRs (>0.98). It also improves the overall performance by reducing the THD of the output voltage and source input current.
2. By means of the proposed method, soft-switching of the power switches at the commutation instances can be achieved by ensuring ZCS for all synthesized output frequencies.

3. The proposed control scheme facilitates the synthesis of the output signal with the desired frequency as it only necessitates the previous knowledge of the output frequency without any control scheme modification burden.
4. The proposed control scheme accommodates any modulation technique without encountering current commutation issues. Further, it synchronizes the power switches PWM triggering pulses with the source (grid) regardless of the synthesized output frequency.
5. The proposed control scheme permits connecting an RL load at the output terminals of the SSMC while experiencing no current commutation issues or significant output voltage transients. Thus, removing the necessity for dissipative circuits (e.g., clamp) for relatively poorly resistive or highly inductive RL loads.

4.4 Conclusion

In this chapter, the proposed SSMC control method, along with the synchronization algorithm, is presented. First, the trapezoidal reference signal used in the modulation process is discussed. The ability of the trapezoidal signal to ensure ZCS at the commutation instances is reviewed. Then, the advantages of the proposed control scheme over the schemes in the literature are discussed. Next, the proposed synchronization algorithm, which synchronizes the triggering pulses with the AC source, is presented. Finally, the key contributions of the proposed control method are highlighted.

CHAPTER 5
SIMULATION STUDIES

5.1 Introduction

This chapter covers the findings of simulation studies performed on the conventional direct buck SSMC. First, the proposed control method is tested and compared to counterpart methods in the literature under different operation conditions. Then, another study is held to compare the influence of several carrier-based modulation techniques on key performance parameters of the SSMC. The four modulation techniques discussed in Section 3.3 are employed for the comparison. The studies are held concerning various performance parameters, including the VTR, output voltage THD (v_o THD), and source current THD (i_{in} THD). The simulations are performed under the simulation conditions of Table 5.1. The general structure of the simulation model is shown in Figure 5.1.

Table 5.1 Simulation parameters.

Parameter	**Value**
Output Power (P_o)	530 W
Source voltage (V_s)	230 Vrms
Source frequency (f_{in})	50 Hz
Time-stepping	100 ns
R-Load	100 Ω
RL-Load	100 Ω + 15 mH
Switching frequency (f_{sw})	5 kHz
Clamp capacitor (C_{cl})	1 nF
Clamp resistor (R_{cl})	1 kΩ
IGBT forward voltage	1 V
Diode forward voltage	0.8 V

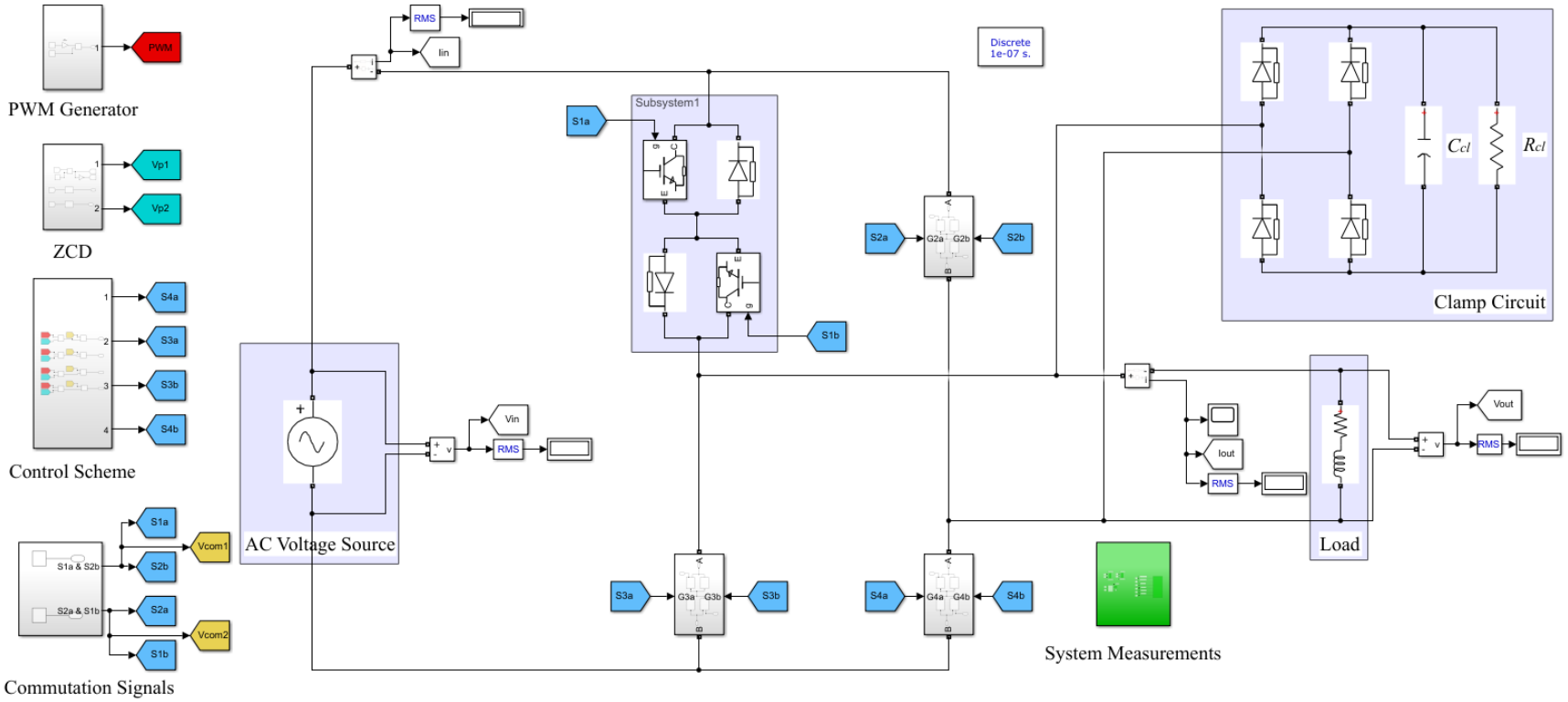


Figure 5.1 General simulation model including measurement blocks.

5.2 Verification of the Proposed SSMC Control Method

In the following subsubsections, several case studies are performed to show the superiority of the proposed control method over counterpart methods in the literature. The counterpart methods are the following:

- Method #1: [127], [128]
- Method #2: [178], [179]
- Method #3: [174], [180]
- Method #4: [68], [171]

5.2.1 Case Study 1: Operation Under a Purely Resistive Load

In this case study, the SSMC is connected to a purely resistive load of 100 Ω. The purpose of this case study is to show the superiority of the proposed method in driving a purely resistive load. The comparison between the proposed method and counterpart methods in controlling the SSMC is performed concerning the VTR and output voltage and source input current THD. Throughout this case study, k is taken as zero since there is no fear of voltage spikes with purely resistive loads. Therefore, a constant reference signal having the amplitude defined by the modulation index is utilized to generate the PWM signal for the proposed method.

The output voltage waveforms obtained for 100 Hz output frequency using the proposed control technique and counterpart techniques at 0.6 modulation index are shown in Figure 5.2 to Figure 5.7. The source current waveforms are shown in Figure 5.8 to Figure 5.13. It can be recognized that all the methods provide acceptable waveforms with a purely resistive load. The VTR variation with modulation index obtained using the proposed and counterpart control methods are shown in Figure 5.14. It is clear from Figure 5.14 that the proposed method provides higher VTRs than the methods of [127], [128], [174], [178]–[180] at all modulation indexes and for all output frequencies. When compared with the method of [174], [180], the proposed method offers further VTR at unity modulation index by around 14.31%, 7.98%, 2.32%, 14.47%, 14.34%, and 14.35% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively. On the other hand, the method of [68], [171] provides

close VTRs to the proposed method, which is expected since similar carrier and reference signals are occupied in the modulation process.

Nevertheless, the method of [68], [171] offers relatively high output voltage THDs when compared to the proposed method, as illustrated in Figure 5.15. More preciously, at 0.5 modulation index, the proposed method offered less output voltage THD by around 12.33%, 13%, 18.87%, 13.11%, 13.35%, and 13.36% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively. Generally, the highest output voltage THD is offered by the method of [178], [179]. When compared with the proposed method, the proposed method offers less output voltage THD at 0.5 modulation index by around 33.41%, 32.98%, 34.11%, 10.65%, 13.62%, and 14.49% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively.

Figure 5.16 illustrates the variation of the source input current THD with modulation index obtained using different SSMC control methods, where the method of [68], [171] offers the lowest percentages among the counterpart methods. Nevertheless, when compared to the proposed method, it offers more source current THD at 0.5 by around 10.98%, 10.95%, 10.89%, 11.23%, 11.3%, and 11.69% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively. Thus, we deduced that with a purely resistive load the proposed method offers enhanced performance.

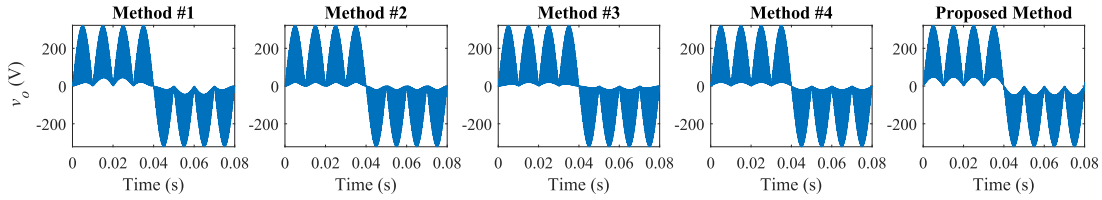


Figure 5.2 Output voltage waveforms for 12.5 Hz output frequency at 0.6 modulation index with a purely resistive load.

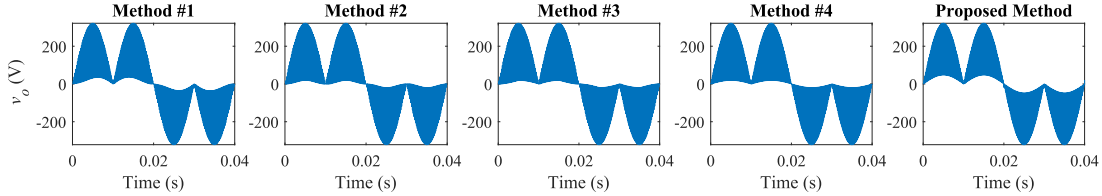


Figure 5.3 Output voltage waveforms for 25 Hz output frequency at 0.6 modulation index with a purely resistive load.

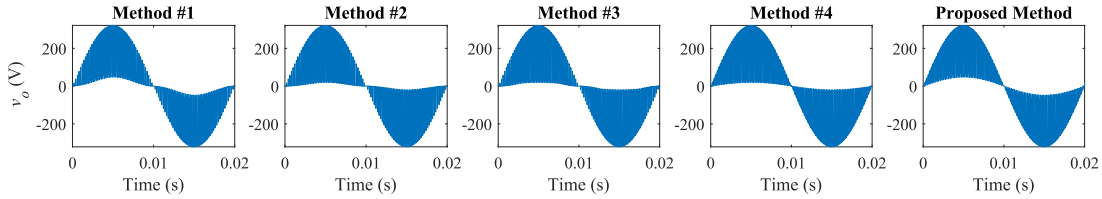


Figure 5.4 Output voltage waveforms for 50 Hz output frequency at 0.6 modulation index with a purely resistive load.

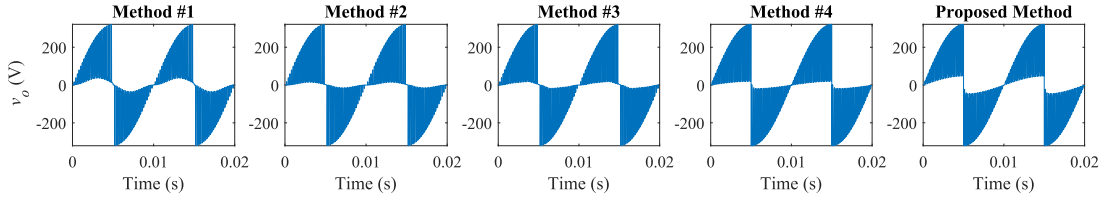


Figure 5.5 Output voltage waveforms for 100 Hz output frequency at 0.6 modulation index with a purely resistive load.

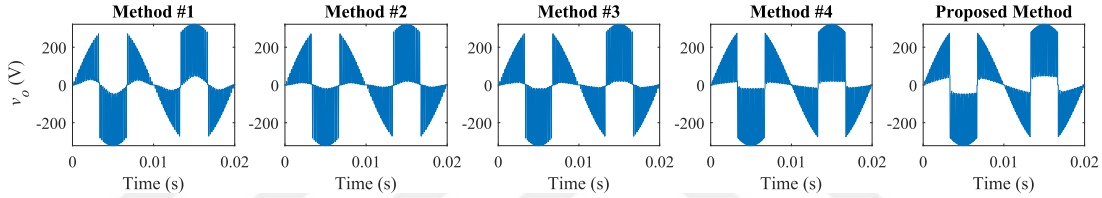


Figure 5.6 Output voltage waveforms for 150 Hz output frequency at 0.6 modulation index with a purely resistive load.

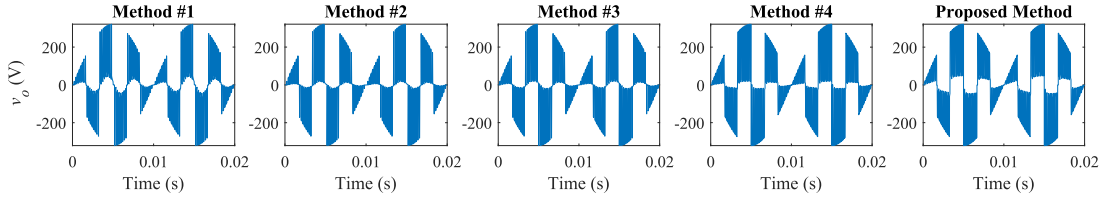


Figure 5.7 Output voltage waveforms for 300 Hz output frequency at 0.6 modulation index with a purely resistive load.

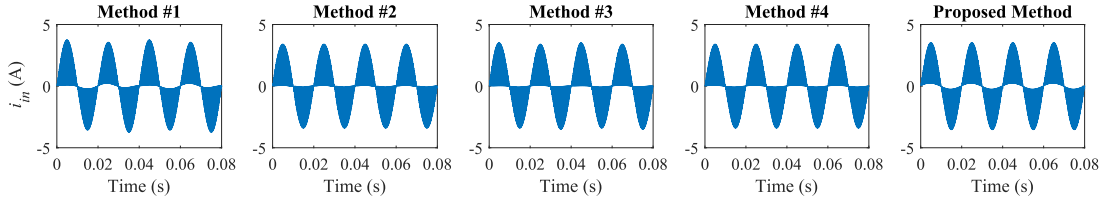


Figure 5.8 Source input current waveforms for 12.5 Hz output frequency at 0.6 modulation index with a purely resistive load.

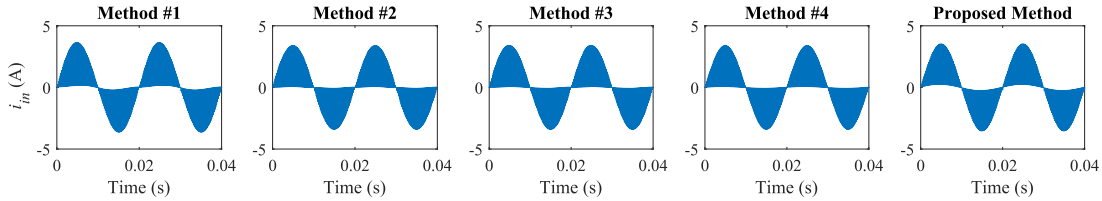


Figure 5.9 Source input current waveforms for 25 Hz output frequency at 0.6 modulation index with a purely resistive load.

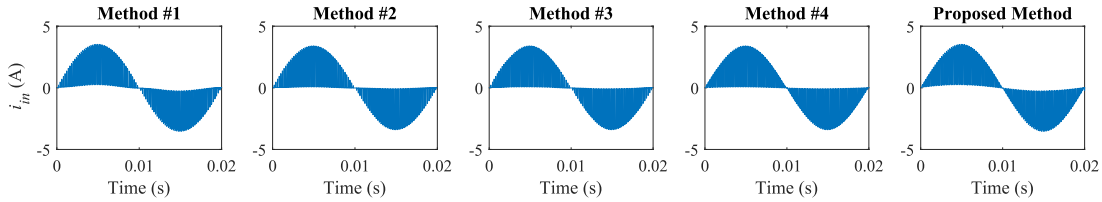


Figure 5.10 Source input current waveforms for 50 Hz output frequency at 0.6 modulation index with a purely resistive load.

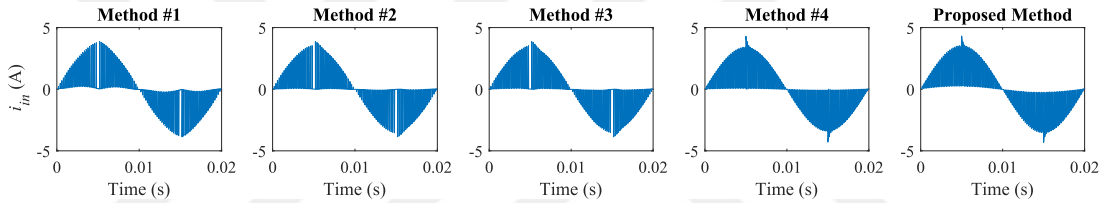


Figure 5.11 Source input current waveforms for 100 Hz output frequency at 0.6 modulation index with a purely resistive load.

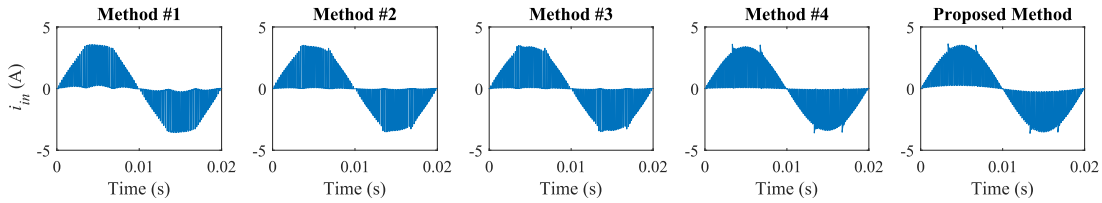


Figure 5.12 Source input current waveforms for 150 Hz output frequency at 0.6 modulation index with a purely resistive load.

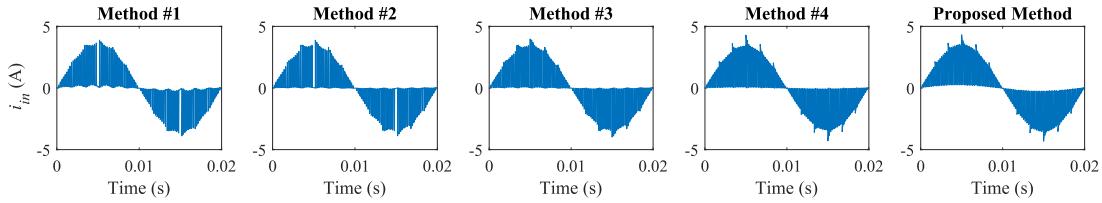


Figure 5.13 Source input current waveforms for 300 Hz output frequency at 0.6 modulation index with a purely resistive load.

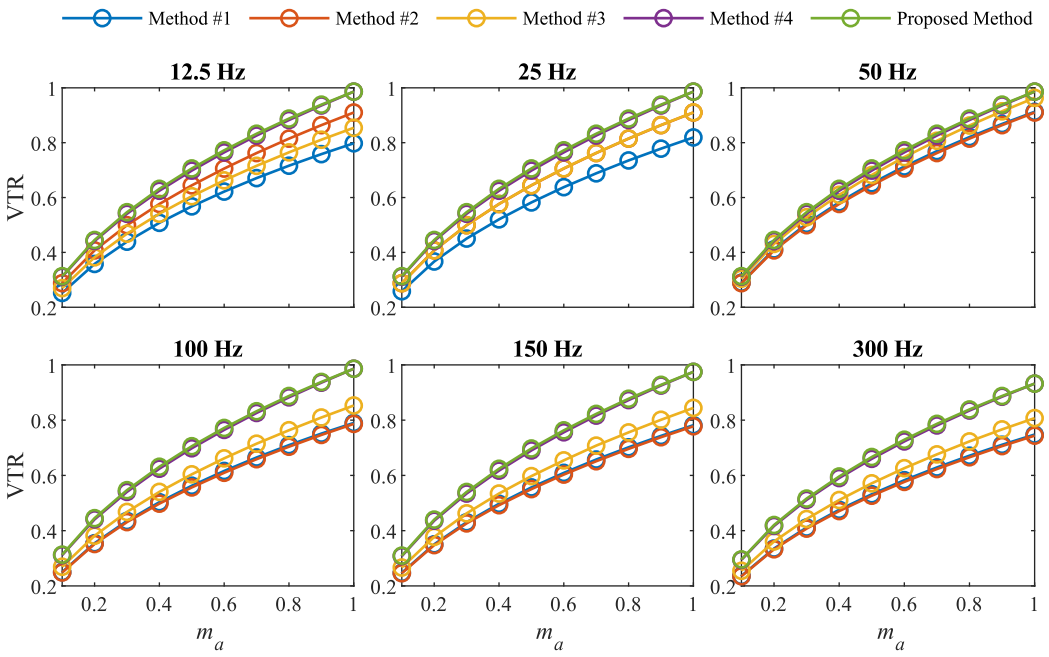


Figure 5.14 Comparison of VTR under different modulation indexes with a purely resistive load.

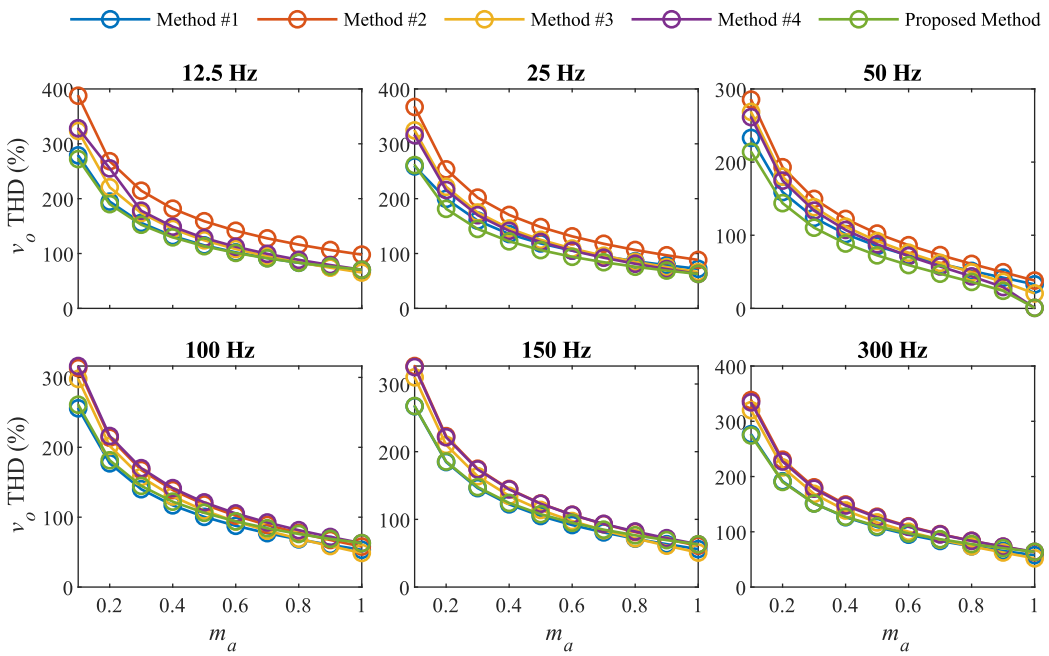


Figure 5.15 Comparison of output voltage THD under different modulation indexes with a purely resistive load.

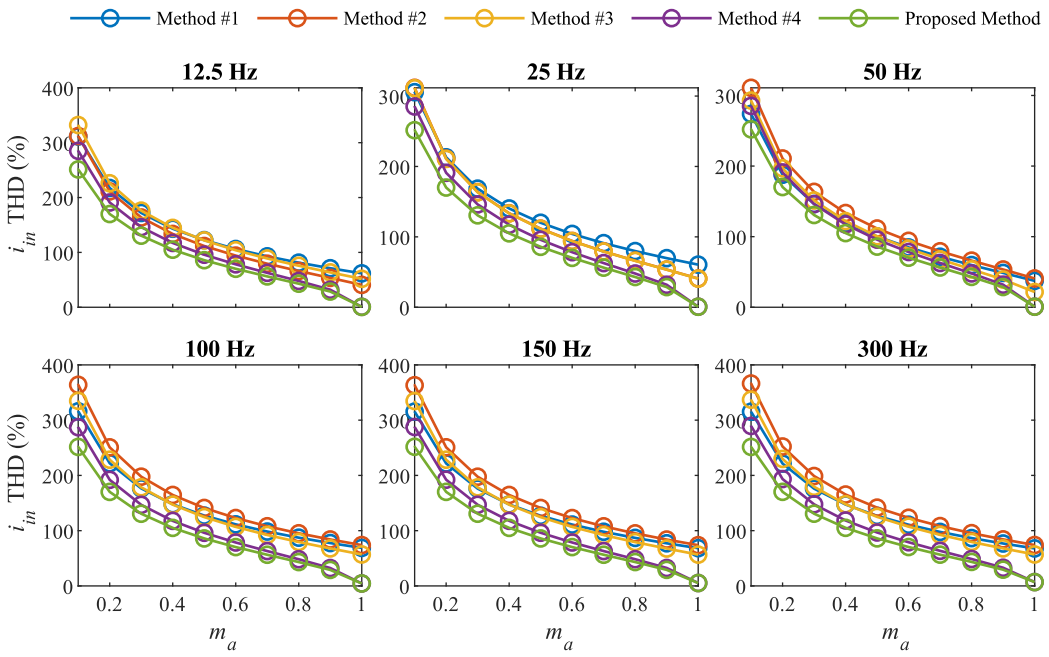


Figure 5.16 Comparison of source input current THD under different modulation indexes with a purely resistive load.

5.2.2 Case Study 2: Operation Under an RL Load

As loads are rarely purely resistive in practice, this case study demonstrates the superiority of the proposed method over the counterpart methods when the SSMC is connected to an RL load. The comparison is performed concerning the VTR, output voltage THD, and source input current THD. Throughout this case study, k is taken to be 1/3 as it is found that it is the optimal ratio for the given operating conditions to mitigate the voltage spikes and extract the maximum RMS value of the output voltage.

While the SSMC is connected to a constant RL load of 100 Ω + 15 mH, the obtained output voltage waveforms are shown in Figure 5.17 to Figure 5.22, output current waveforms in Figure 5.23 to Figure 5.28, and source current waveforms in Figure 5.29 to Figure 5.34. It can be recognized that the methods of [68], [171], [174], [178]–[180] provide output voltage spikes at each switching cycle. This is because the inductive current finds no path to flow through when the PWM signal is low, as discussed earlier. Therefore, the methods of [68], [171], [174], [178]–[180] cannot be used with adequate RL loads without the use of some external dissipative circuits, such as a clamp circuit. Hence, in this case study, the performance variation of the SSMC with the modulation index is compared only using the proposed method and the method of [127], [128] without the use of a clamp circuit.

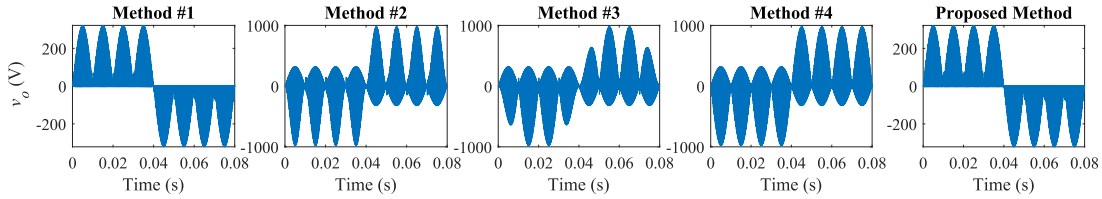


Figure 5.17 Output voltage waveforms for 12.5 Hz output frequency at 0.6 modulation index with an RL load.

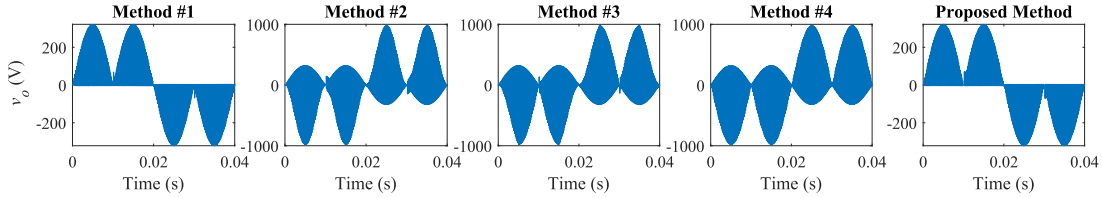


Figure 5.18 Output voltage waveforms for 25 Hz output frequency at 0.6 modulation index with an RL load.

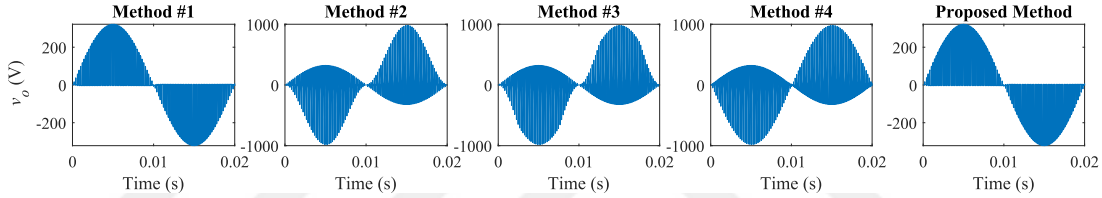


Figure 5.19 Output voltage waveforms for 50 Hz output frequency at 0.6 modulation index with an RL load.

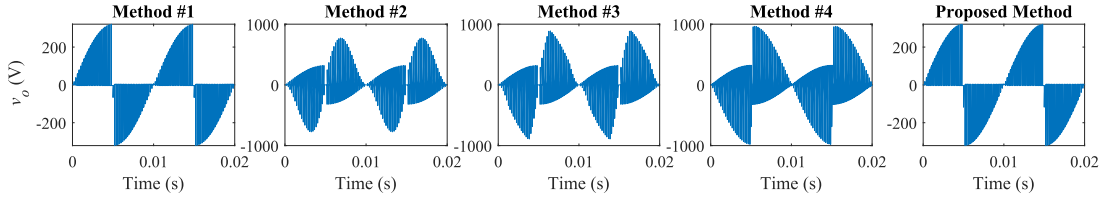


Figure 5.20 Output voltage waveforms for 100 Hz output frequency at 0.6 modulation index with an RL load.

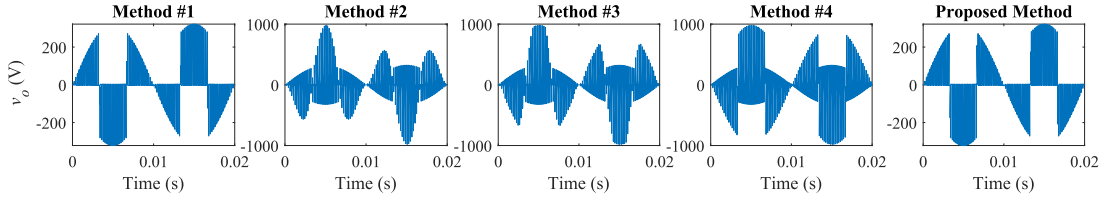


Figure 5.21 Output voltage waveforms for 150 Hz output frequency at 0.6 modulation index with an RL load.

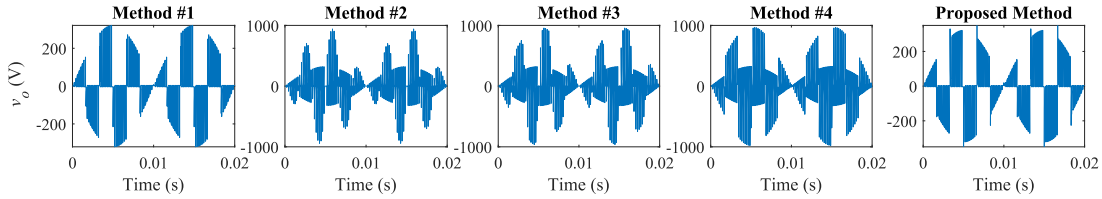


Figure 5.22 Output voltage waveforms for 300 Hz output frequency at 0.6 modulation index with an RL load.

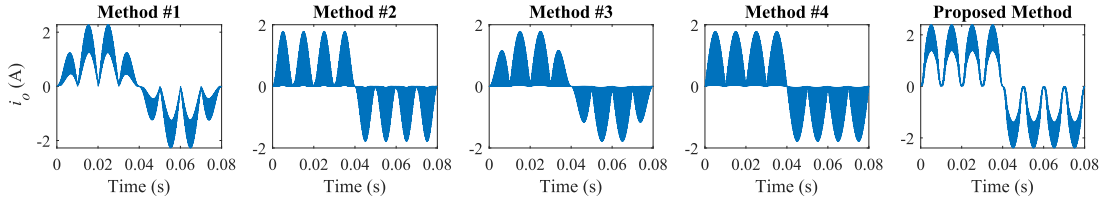


Figure 5.23 Output current waveforms for 12.5 Hz output frequency at 0.6 modulation index with an RL load.

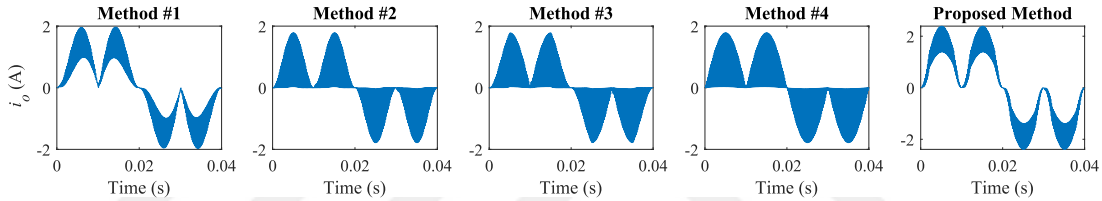


Figure 5.24 Output current waveforms for 25 Hz output frequency at 0.6 modulation index with an RL load.

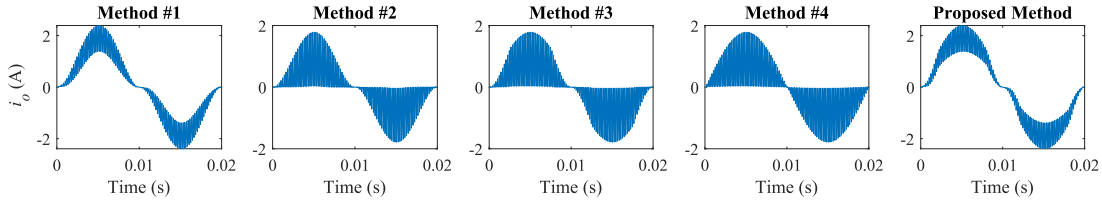


Figure 5.25 Output current waveforms for 50 Hz output frequency at 0.6 modulation index with an RL load.

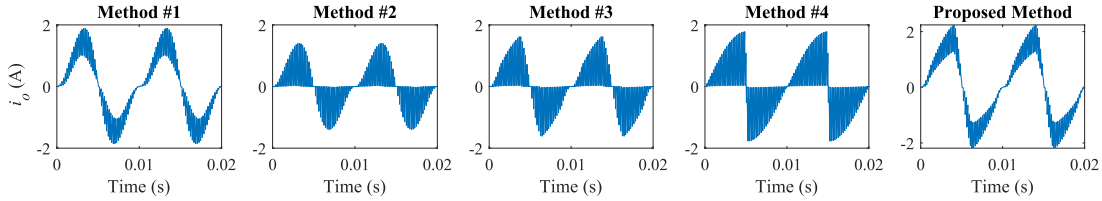


Figure 5.26 Output current waveforms for 100 Hz output frequency at 0.6 modulation index with an RL load.

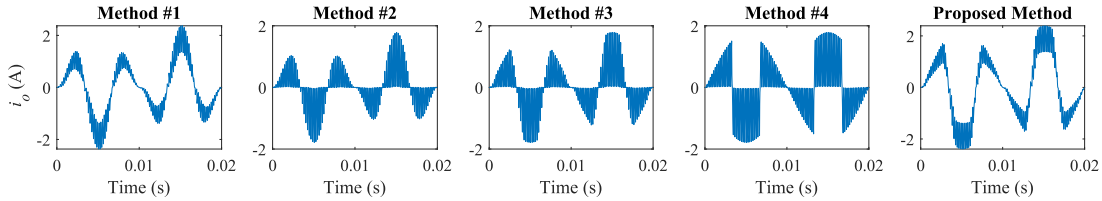


Figure 5.27 Output current waveforms for 150 Hz output frequency at 0.6 modulation index with an RL load.

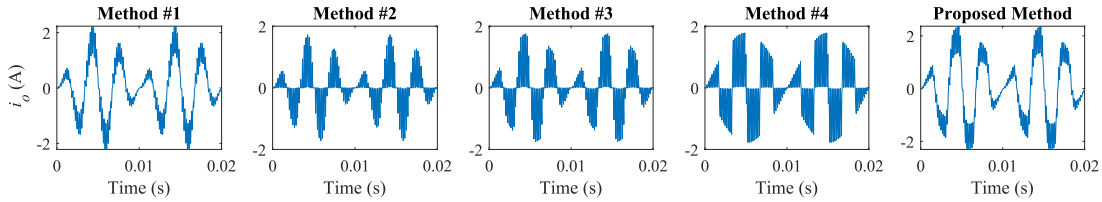


Figure 5.28 Output current waveforms for 300 Hz output frequency at 0.6 modulation index with an RL load.

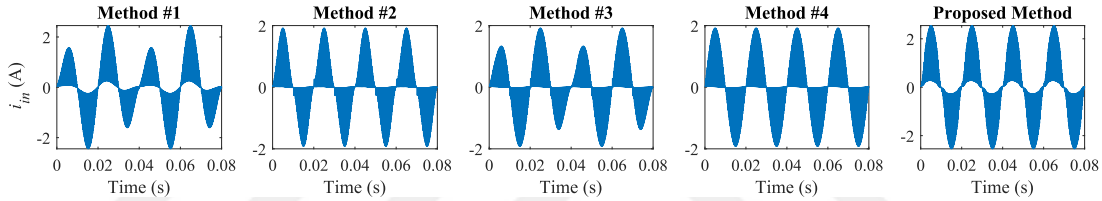


Figure 5.29 Source input current waveforms for 12.5 Hz output frequency at 0.6 modulation index with an RL load.

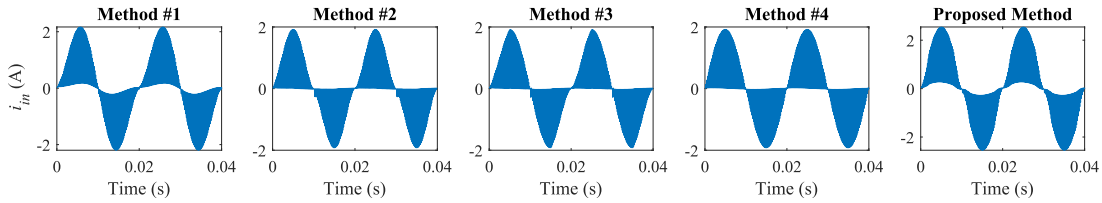


Figure 5.30 Source input current waveforms for 25 Hz output frequency at 0.6 modulation index with an RL load.

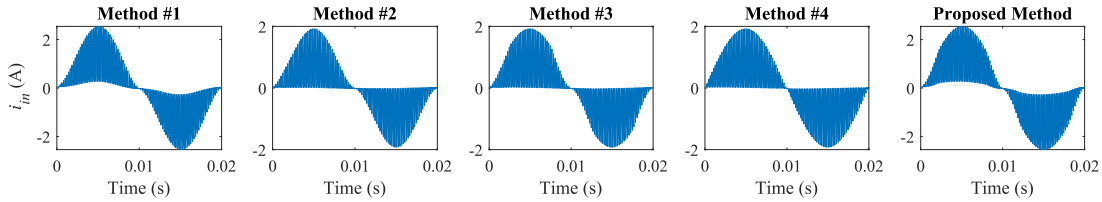


Figure 5.31 Source input current waveforms for 50 Hz output frequency at 0.6 modulation index with an RL load.

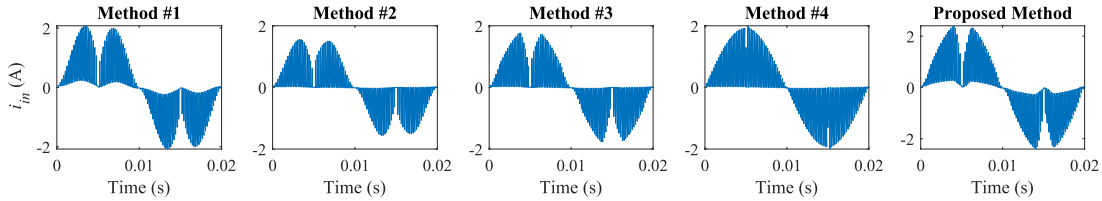


Figure 5.32 Source input current waveforms for 100 Hz output frequency at 0.6 modulation index with an RL load.

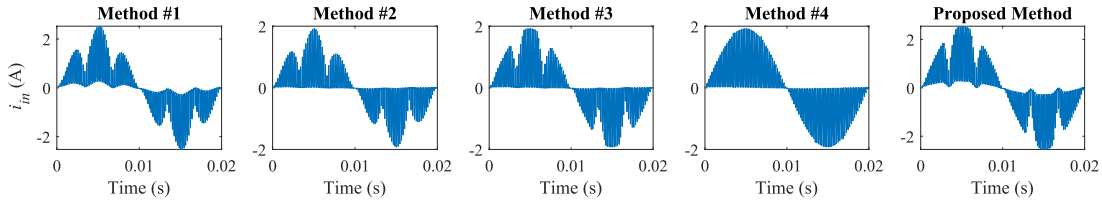


Figure 5.33 Source input current waveforms for 150 Hz output frequency at 0.6 modulation index with an RL load.

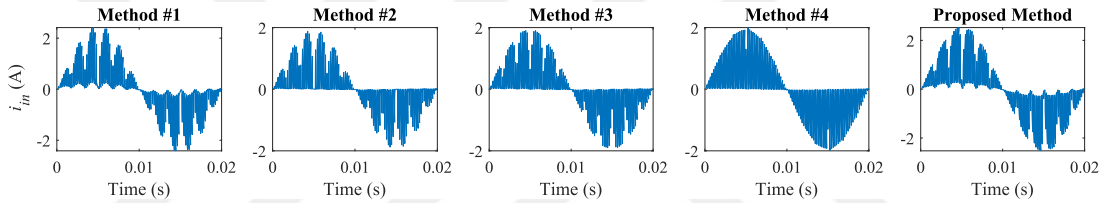


Figure 5.34 Source input current waveforms for 300 Hz output frequency at 0.6 modulation index with an RL load.

Figure 5.35 illustrates the variation in the VTR of the SSMC when the proposed method and the counterpart method are used. It is clear that the proposed method outperforms the counterpart method at all modulation indexes and for all output frequencies. More specifically, at unity modulation index, the proposed method provides more output voltage by around 20.47%, 18.06%, 6.88%, 11.37%, 11.63%, and 12.37% for 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively.

In terms of output voltage THD, the proposed method shows generally superior results at all modulation indexes, as shown in Figure 5.36. The proposed method offers less output voltage THD by around 14.46%, 88.96%, 22.62%, 23.37%, and 20.2% at unity modulation index and 10.63%, 8.73%, 7.72%, 8.35%, and 8.87% at 0.1 modulation index for 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively.

In addition to the aforementioned favorable characteristics, the proposed method reduces the source input current THD for all output frequencies and at all modulation indexes, as shown in Figure 5.37. More specifically, compared to the counterpart method of [127], [128], the proposed method reduces the source input current THD by around 113.39%, 117.48%, 84.15%, 35.7%, 35.8%, and 34.32% at unity modulation index and by around 11.98%, 10.34%, 4.8%, 6.54%, 6.43%, and 6.35% at 0.1 modulation index for 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively.

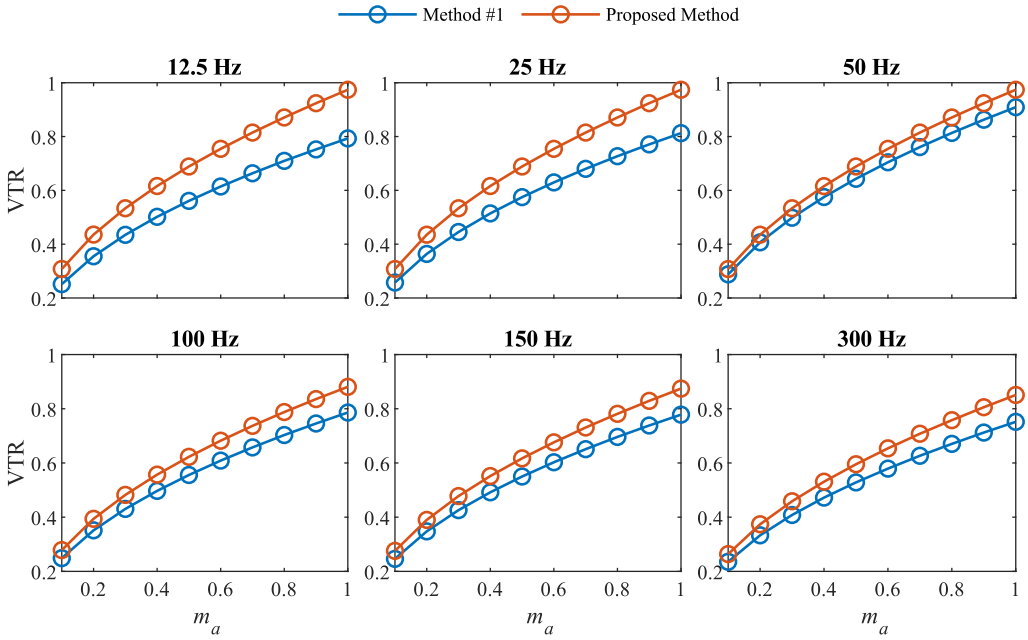


Figure 5.35 Comparison of VTR under different modulation indexes with an RL load.

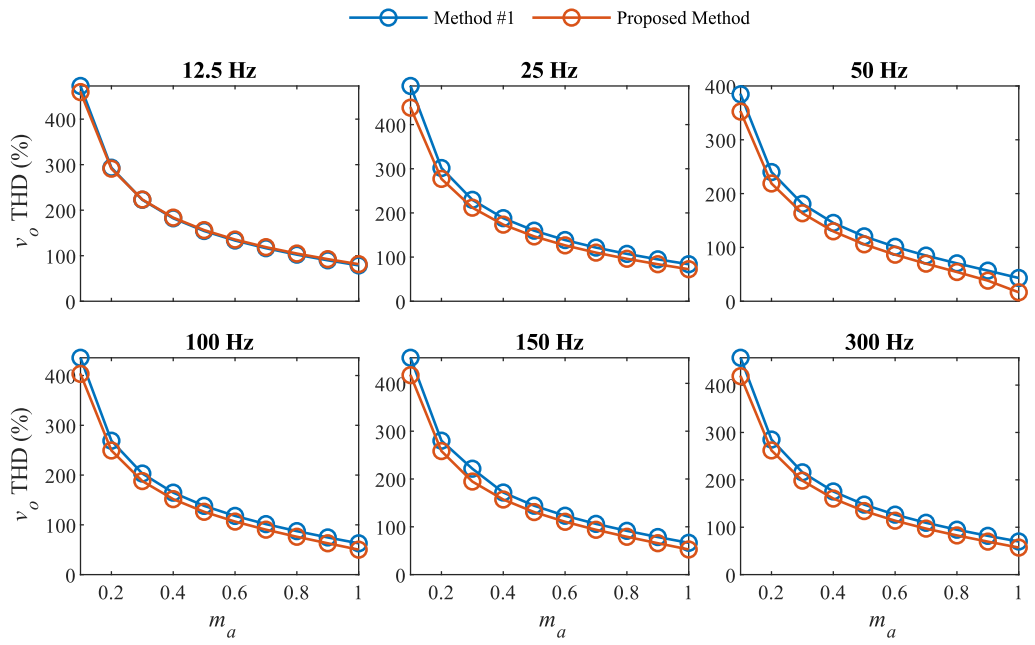


Figure 5.36 Comparison of output voltage THD under different modulation indexes with an RL load.

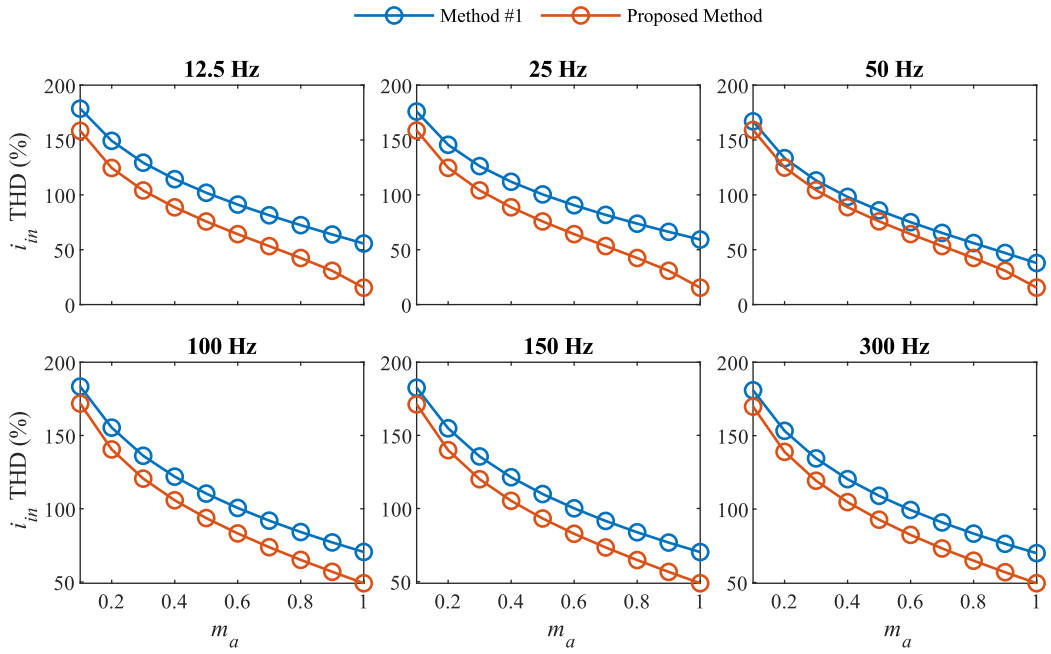


Figure 5.37 Comparison of source input current THD under different modulation indexes with an RL load.

5.2.3 Case Study 3: Operation Under an RL Load with a Clamp Circuit

The previous case study showed that the SSMC could drive an adequate RL load using the proposed method at k = 1/3 with increased VTRs and mitigated output voltage

spikes. Nevertheless, relatively high VTRs are not achieved for output frequencies higher than the source frequency. This case study shows that by setting k to zero, relatively high VTRs can be achieved using the proposed control scheme for frequencies higher than the source frequency. Nevertheless, it comes with the expense of some voltage spikes at the commutation instances because ZCS is not ensured when k is set to zero. Therefore, the use of a clamp circuit is necessary. This clamp circuit is connected in parallel with the RL load. It consists of a diode bridge rectifier supplying a small capacitor and a resistor, as shown in Figure 2.21. The circuit stores and discharges the excessive RL load energy. The bridge rectifier converts the voltage from AC to DC so that the clamp capacitor can store it. The resistor, on the other hand, discharges the capacitor. It is important to choose the value of the clamp circuit components objectively. Figure 5.38 shows the influence of the clamp circuit parameters on the performance of the SSMC, where I_{in} is the RMS value of the source input current, R_{cl} is the calmp resistor, and C_{cl} is the clamp capacitor. A large resistance would impede the flow of current, and thus, it would be hard for the capacitor to discharge. Small resistance, on the other hand, would be helpful in decreasing the output voltage spikes. However, it would draw further current from the source, thus, high current rated components should be chosen. Additionally, the clamp circuit capacitor value plays an essential role in determining the amplitude of the output voltage spikes and the output current THD. The higher the capacitance is, the higher amplitude of current spikes in the source input current, and thus, the higher the THD of the input current. Nonetheless, small capacitance would increase the amplitude of output voltage spikes. In this study, the parameters of the clamp circuit passive components are chosen such that the voltage spikes are significantly mitigated, and the source input current does not exceed 10% of its nominal value. The employed clamp circuit consists of 1 nF capacitor and a 1 kΩ resistor.

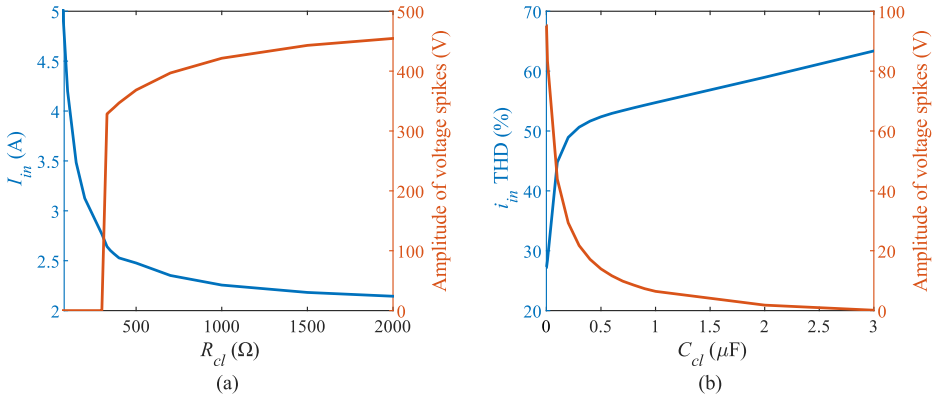


Figure 5.38 The influence of clamp circuit components on the SSMC performance. (a) The effect of the clamp resistor value on the source current and amplitude of voltage spikes. (b) The effect of the clamp capacitor value on the source current THD and amplitude of voltage spikes.

The same clamp circuit is connected in parallel with the 100 Ω + 15 mH RL load for all the simulation cases. The obtained output voltage waveforms are shown in Figure 5.39 to Figure 5.44, output current waveforms in Figure 5.45 to Figure 5.50, and source current waveforms in Figure 5.51 to Figure 5.56, using the proposed control scheme and counterpart schemes at 0.6 modulation index. It is clear that even with a clamp circuit, the methods of [68], [171], [174], [178]–[180] still show voltage spikes when the PWM signal is low. Therefore, the resistance of R_{cl} should decrease to eliminate the voltage spikes when the control methods of [68], [171], [174], [178]–[180] are employed. However, as mentioned above, this will come with the expense of high source input current amplitude, which may exceed the ratings of the circuit components. On the other hand, the method of [127], [128] provides huge source input current spikes at each switching cycle because the source gets short-circuited when the PWM signal is low. Therefore, with RL loads, all of the counterpart control schemes in the literature may not be able to achieve high VTRs. Figure 5.57 shows the variation of the VTR with modulation index for several output frequencies. It is clear that the proposed control scheme enables achieving roughly unity VTRs. However, in the case of output frequencies higher than $3f_s$, unity VTR is not achieved, which is due to the inherent nature of the source AC voltage, and it can be interpreted by (3.15). This is one of the drawbacks of direct power conversion. When the results of this case ($k = 0$) are compared with the previous case ($k = 1/3$), it is found that at unity modulation

index the VTR in this case is increased by around 1.24% for $f_o \leq f_{in}$ and 10% for $f_o > f_{in}$.

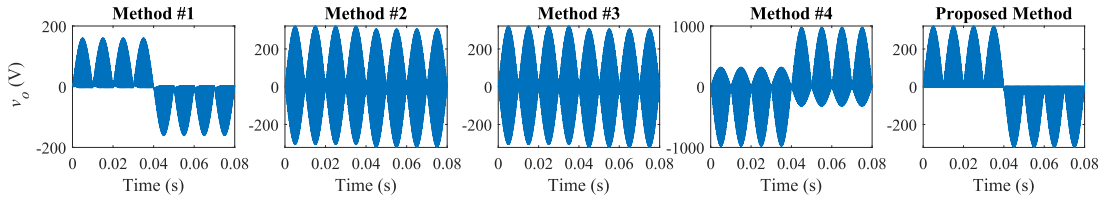


Figure 5.39 Output voltage waveforms for 12.5 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

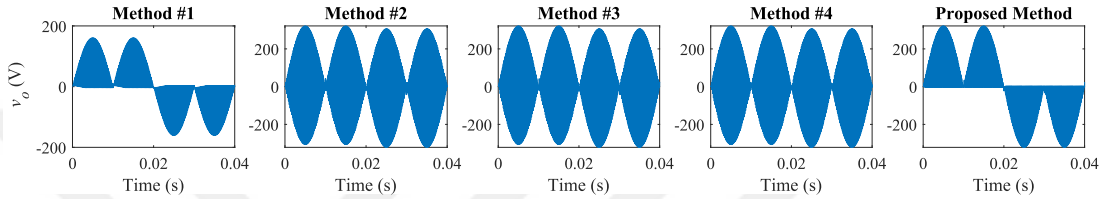


Figure 5.40 Output voltage waveforms for 25 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

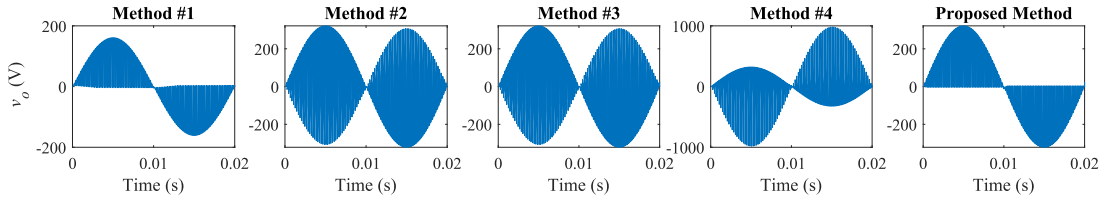


Figure 5.41 Output voltage waveforms for 50 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

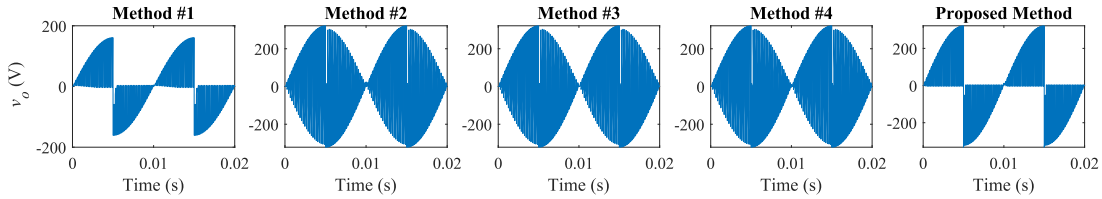


Figure 5.42 Output voltage waveforms for 100 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

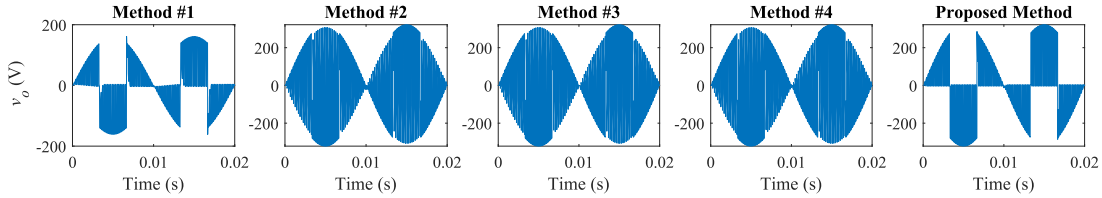


Figure 5.43 Output voltage waveforms for 150 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

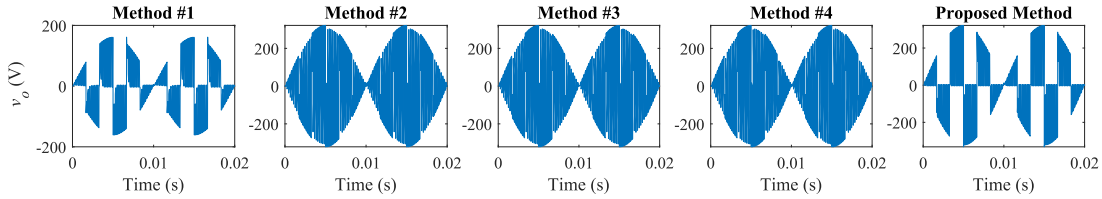


Figure 5.44 Output voltage waveforms for 300 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

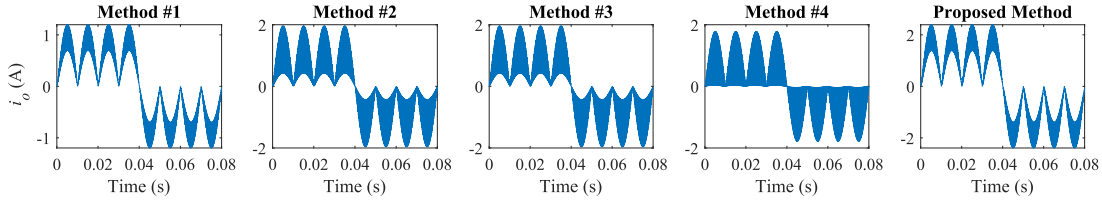


Figure 5.45 Output current waveforms for 12.5 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

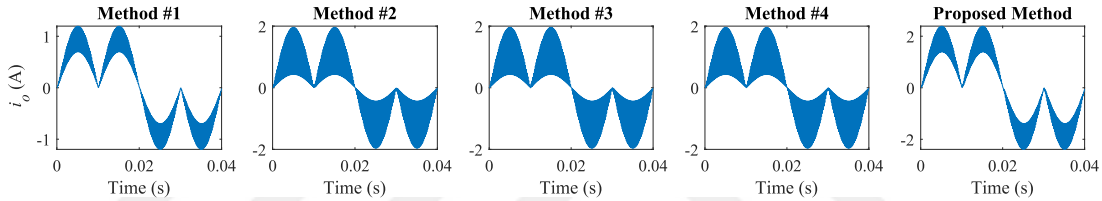


Figure 5.46 Output current waveforms for 25 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

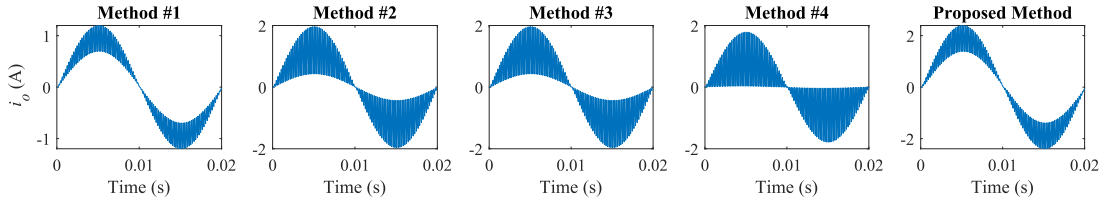


Figure 5.47 Output current waveforms for 50 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

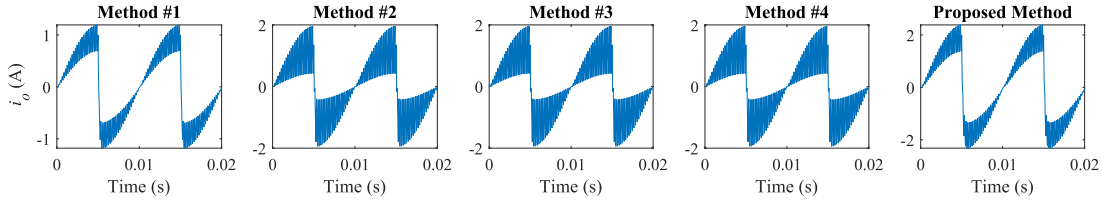


Figure 5.48 Output current waveforms for 100 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

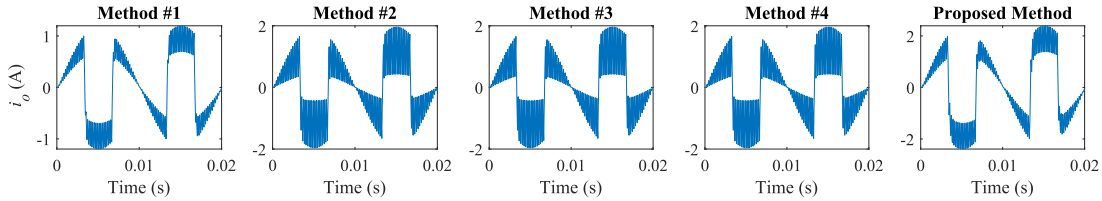


Figure 5.49 Output current waveforms for 150 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

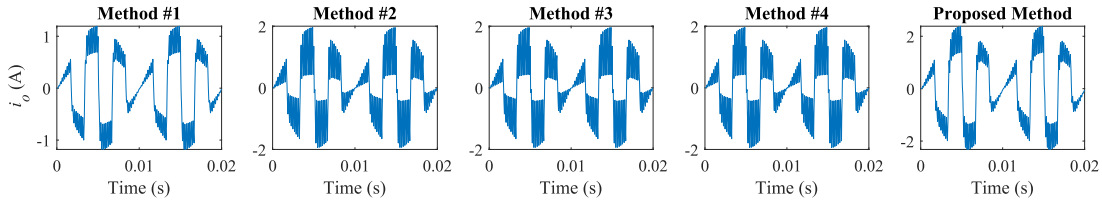


Figure 5.50 Output current waveforms for 300 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

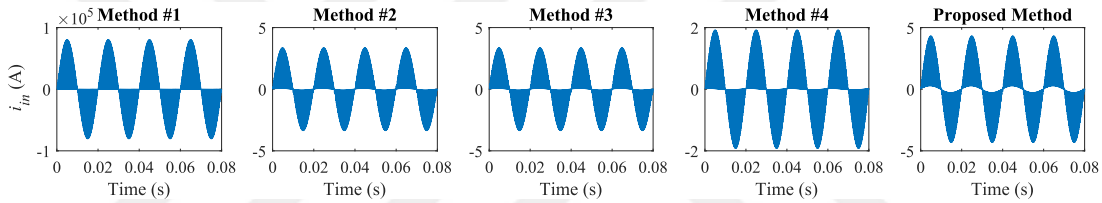


Figure 5.51 Source input current waveforms for 12.5 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

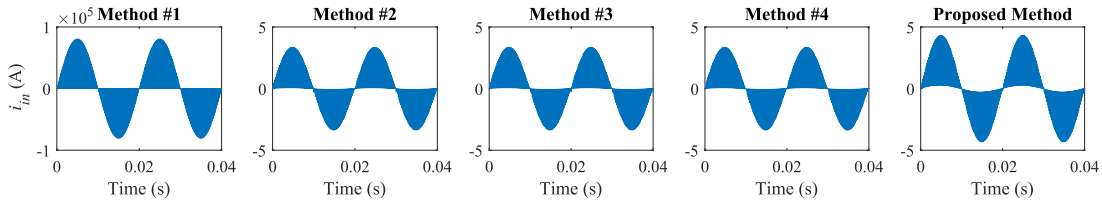


Figure 5.52 Source input current waveforms for 25 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

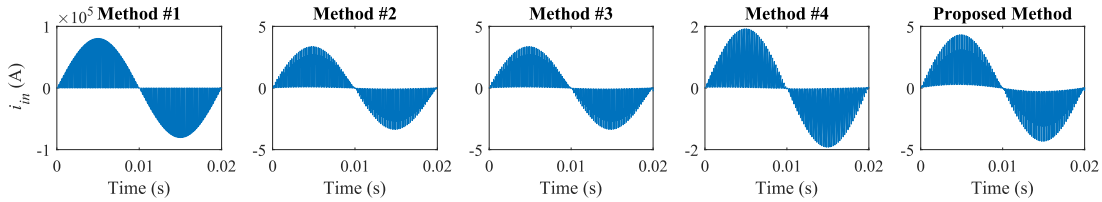


Figure 5.53 Source input current waveforms for 50 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

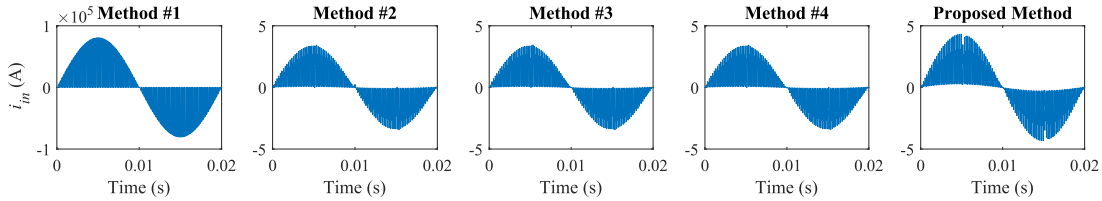


Figure 5.54 Source input current waveforms for 100 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

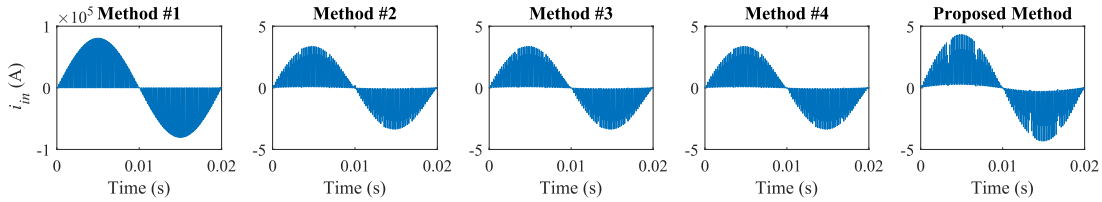


Figure 5.55 Source input current waveforms for 150 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

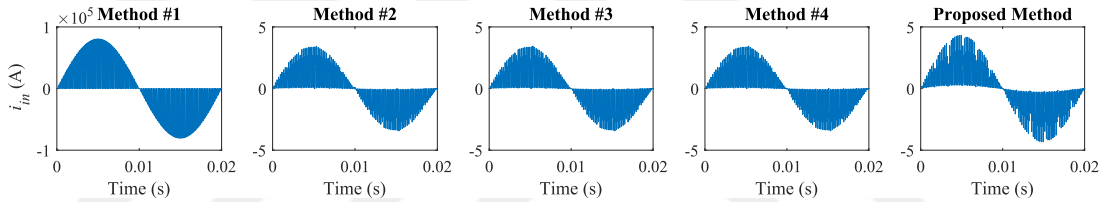


Figure 5.56 Source input current waveforms for 300 Hz output frequency at 0.6 modulation index with an RL load and a clamp circuit.

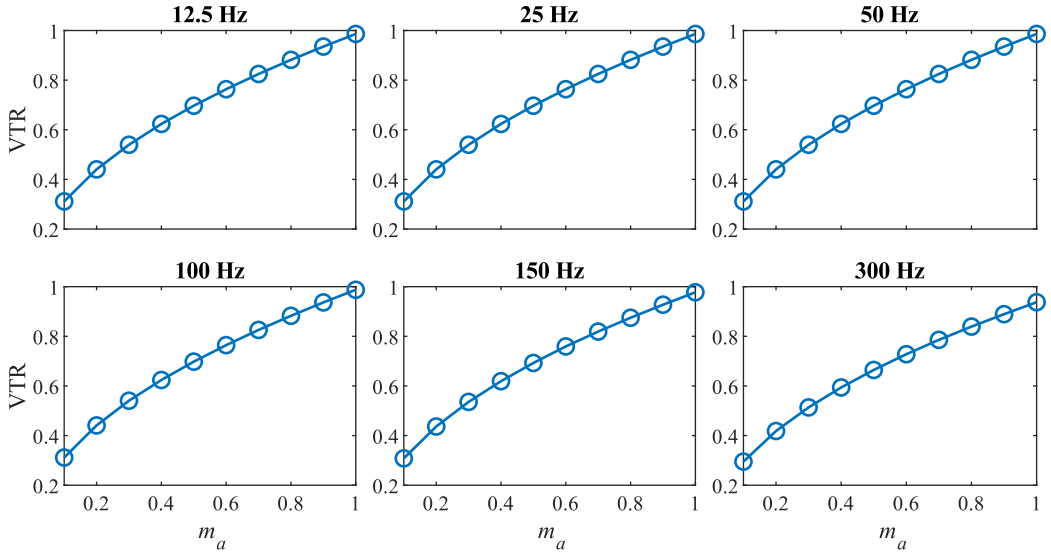


Figure 5.57 Variation of VTR under different modulation indexes with an RL load and a clamp circuit using the proposed control scheme.

5.2.4 Conclusion

In Section 5.2, various simulation case studies are presented to show the superiority of the proposed methods over the methods in the literature in controlling the SSMC. First, the SSMC is tested when connected to a purely resistive load. Results showed that all methods provide similar accepted waveforms. Nevertheless, the proposed control method showed superiority in terms of VTR, output voltage THD, and source input current THD. Then, the control methods are tested when the SSMC is connected to an RL load. Results revealed that only Method #1 is capable of driving RL loads without current commutation problems. When comparing the proposed method with Method #1, results revealed that the proposed control method can significantly increase the VTR and decrease the output voltage and input current THD. Finally, the ability of the proposed control method to achieve relatively high VTRs with a clamp circuit and the inability of Method #1 to adapt with certain modulation techniques is demonstrated, where the proposed control methods enabled the SSMC to achieve roughly unity VTRs for output frequencies lower than the source frequency and higher than the source frequency for frequencies up to three times the source frequency.

5.3 Performance Analysis of SSMC With Carrier-Based PWM Techniques

In this section, the carrier-based PWM techniques discussed in Section 3.3, namely, SPWM, MPWM, SCPWM, and TPWM, are employed to analyze their influence on the performance of the SSMC in the simulation environment. The proposed control scheme shown in Figure 4.1 is used to employ all modulation techniques. Given that purely resistive loads are rarely encountered in practical applications, this section investigates the performance of the SSMC under an RL load of 100 Ω + 15 mH. The simulations are performed under the simulation conditions of Table 5.1, however, with a time-stepping of 1 µs. The VTR, output voltage v_o THD, output current i_o THD, and source input current i_{in} THD, are the key parameters considered to evaluate the SSMC performance. Subsections 5.3.1 to 5.3.4 present selected results to show the influence of each carrier-based PWM technique on the input and output waveforms and their associated harmonics. Subsection 5.3.5 presents the comparison results between the performance parameters obtained using the different carrier-based PWM techniques for various output frequencies and modulation indexes.

5.3.1 SPWM

Figure 5.58 shows the gate-triggering signals used to employ the SPWM technique and the sinusoidal reference v_r and triangular carrier v_{cr} signals used to generate them for 100 Hz output frequency.

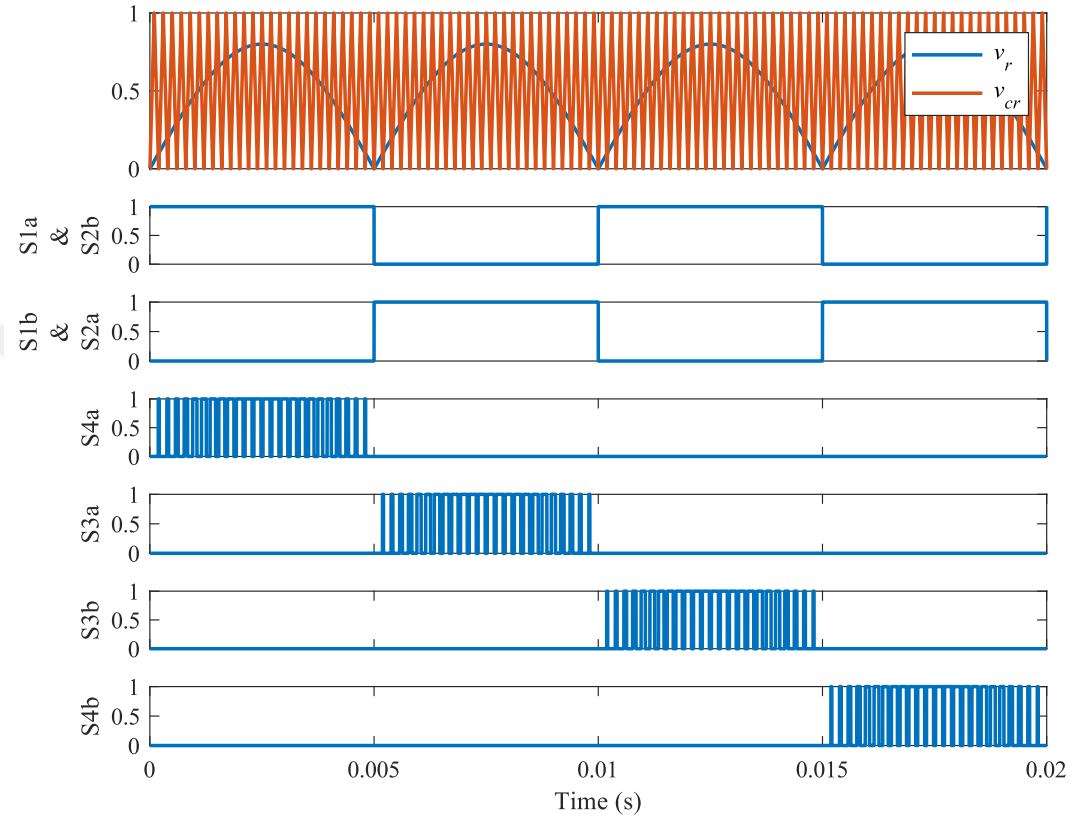


Figure 5.58 Reference, carrier, and switching signals for 100 Hz output frequency employing the SPWM technique at 0.8 modulation index.

The output voltage, output current, and source current waveforms and their harmonics for 25 Hz and 100 Hz output frequencies employing the SPWM technique are shown in Figure 5.59 and Figure 5.60, respectively. The harmonics analyses clearly show that the SPWM technique results in harmonic components showing around frequencies that are multiples of the switching frequency. Thus, the higher the output frequency, the more low-order harmonics are present. For output frequencies lower than the source frequency, the output voltage and current THD increase proportionally with the synthesized output frequency. Nevertheless, the source current THD is inversely proportional to the synthesized output frequency. On the other hand, for output frequencies lower than the source frequency, the output voltage and current THD are

inversely proportional to the synthesized output frequency. No significant variation in the source current THD is recognized for output frequencies lower than the source.

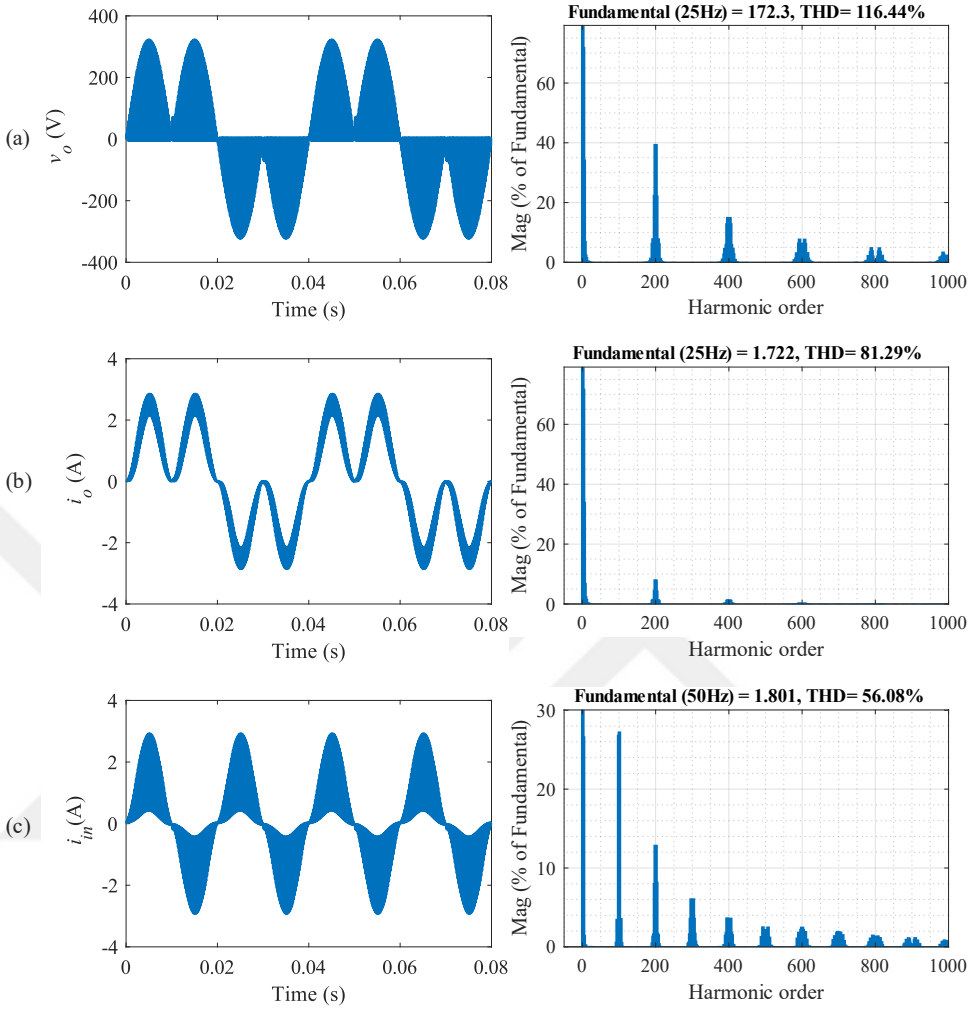


Figure 5.59 (a) Output voltage, (b) output current, and (c) source current waveforms and their harmonics for 25 Hz output frequency employing the SPWM technique at 0.8 modulation index.

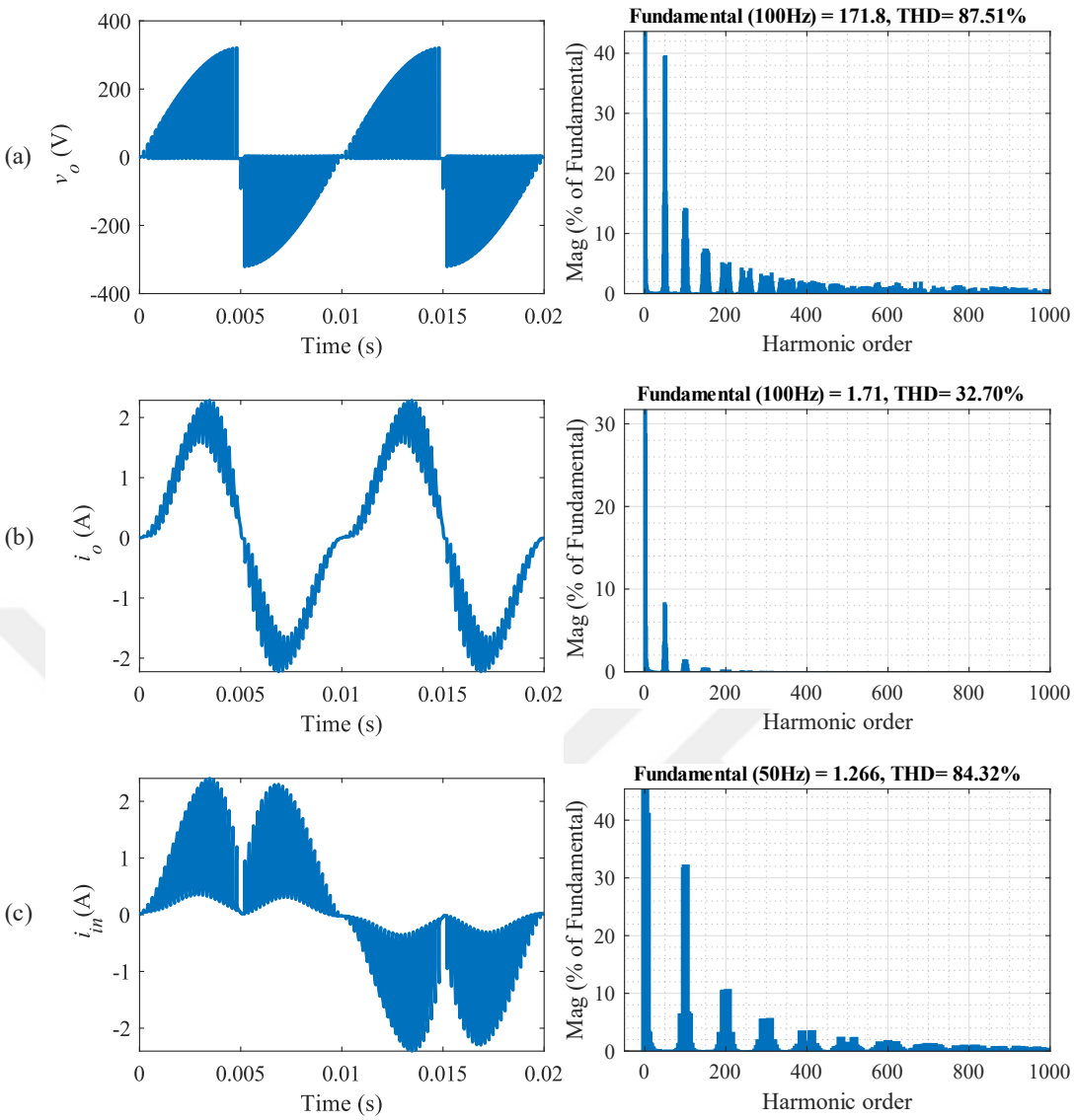


Figure 5.60 (a) Output voltage, (b) output current, and (c) source current waveforms and their harmonics for 100 Hz output frequency employing the SPWM technique at 0.8 modulation index.

5.3.2 MPWM

The MPWM technique utilizes a constant reference signal v_r to generate the PWM gate-triggering signals, as shown in Figure 5.61.

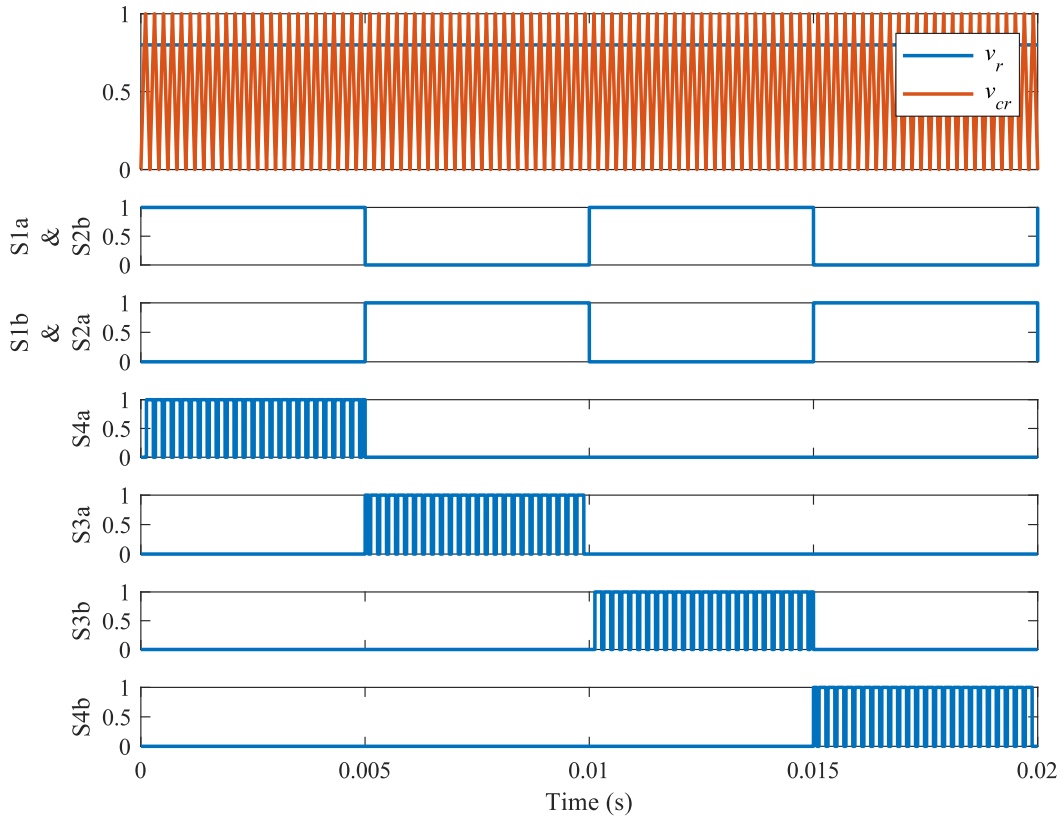


Figure 5.61 Reference, carrier, and switching signals for 100 Hz output frequency employing MPWM technique at 0.8 modulation index.

The output voltage, output current, and source input current waveforms and their harmonics for 25 Hz and 100 Hz output frequencies employing the MPWM technique are shown in Figure 5.62 and Figure 5.63, respectively. The harmonics analyses show that the MPWM technique results in harmonic components showing around frequencies that are multiples of the switching frequency. The output voltage THD increases proportionally to the variation of the synthesized output frequency from the source frequency. The output current THD, on the other hand, is inversely proportional to the synthesized output frequency.

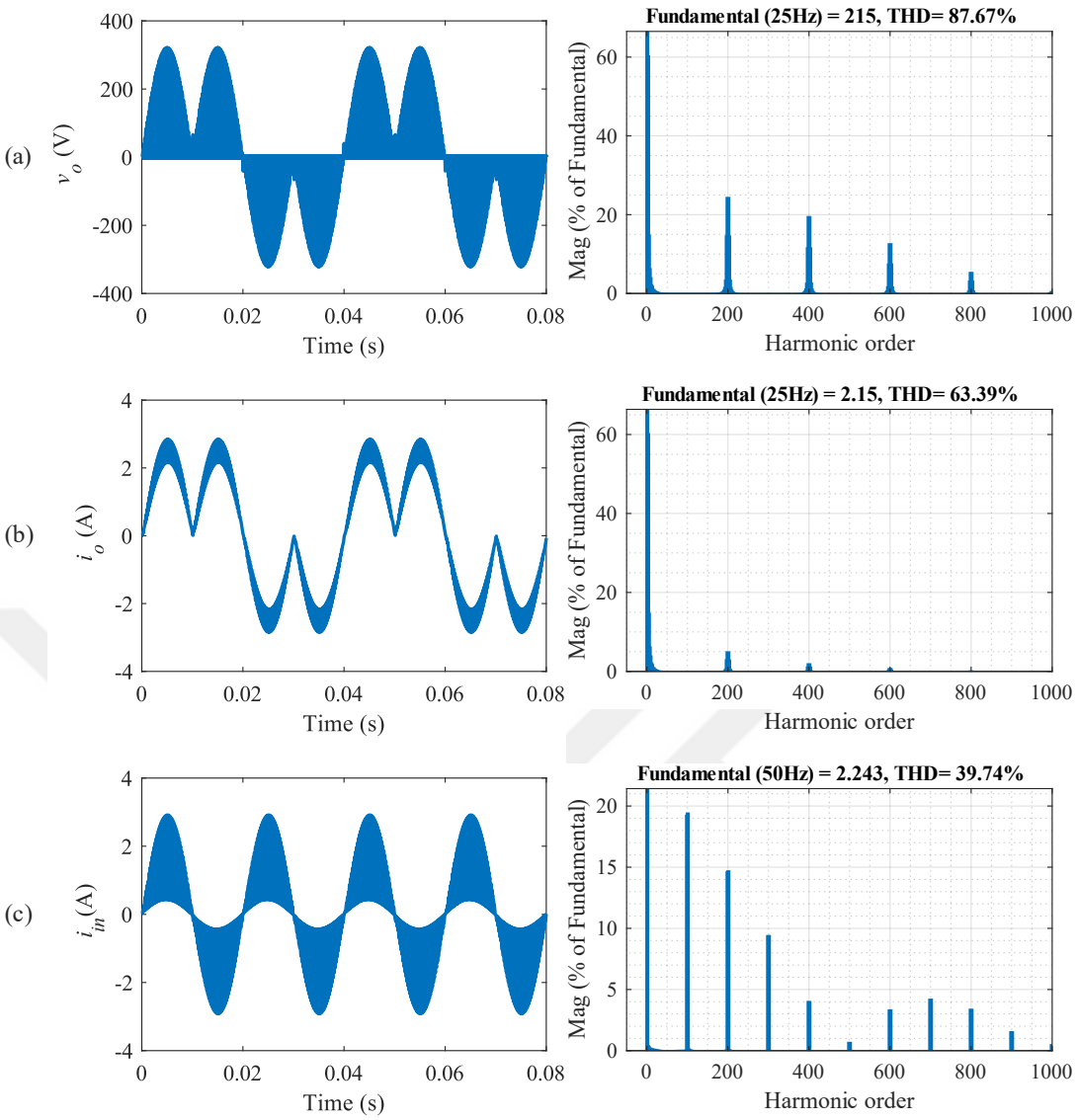


Figure 5.62 (a) Output voltage, (b) output current, and (c) source current waveforms and their harmonics for 25 Hz output frequency employing the MPWM technique at 0.8 modulation index.

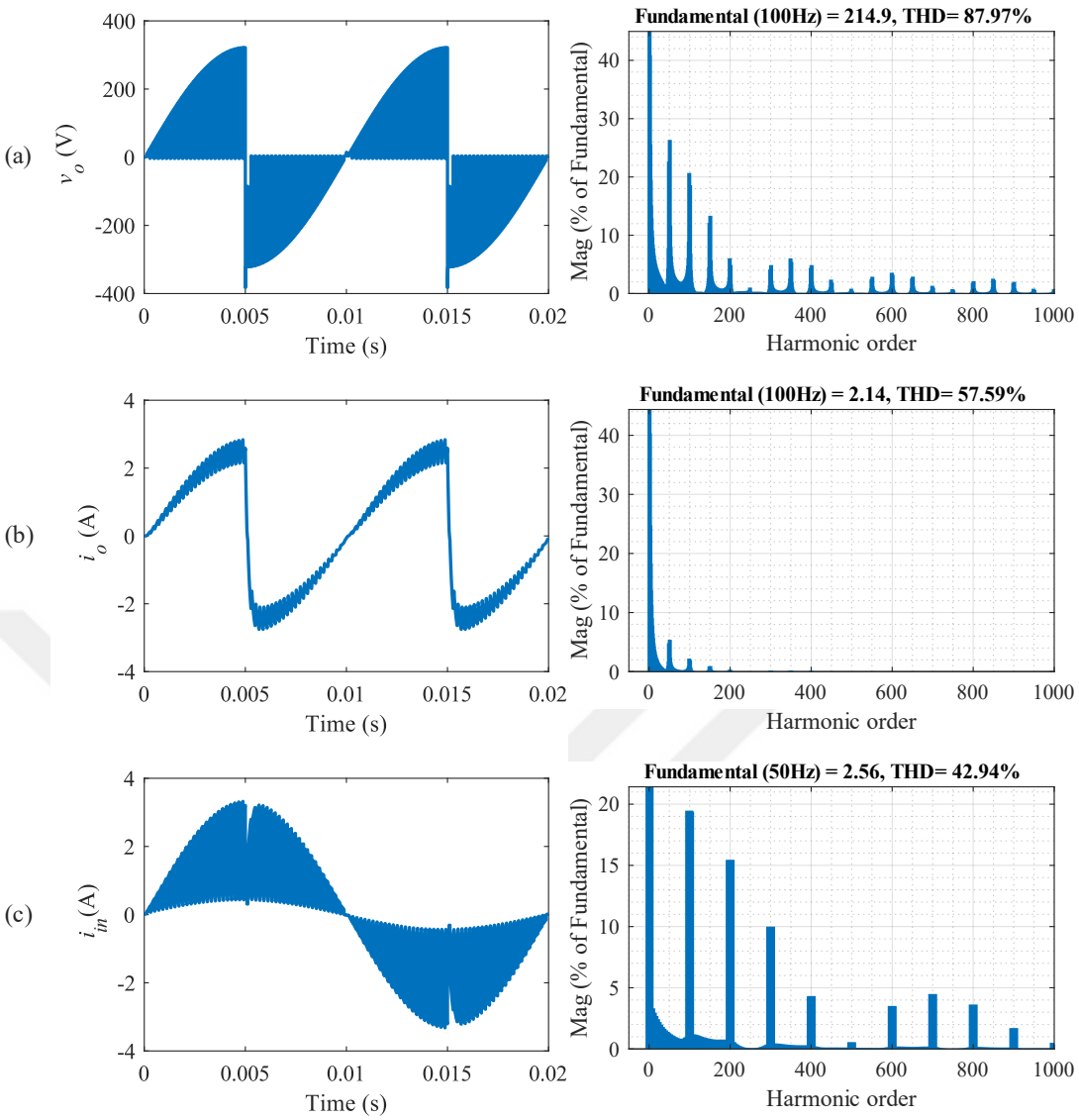


Figure 5.63 (a) Output voltage, (b) output current, and (c) source current waveforms and their harmonics for 100 Hz output frequency employing the MPWM technique at 0.8 modulation index.

5.3.3 SCPWM

Figure 5.64 shows the gate-triggering signals used to employ the SCPWM technique and the staircase reference v_r and triangular carrier v_{cr} signals used to generate them for 100 Hz output frequency. In this thesis, a single-stair reference signal is used, where the low time t_l is taken as 1/20 T_{sca}, middle time t_m is taken as 3/20 T_{sca}, and high time t_h is taken as 3/5 T_{sca}. The amplitude of the stair during the middle time t_m is taken to be 0.5 per unit.

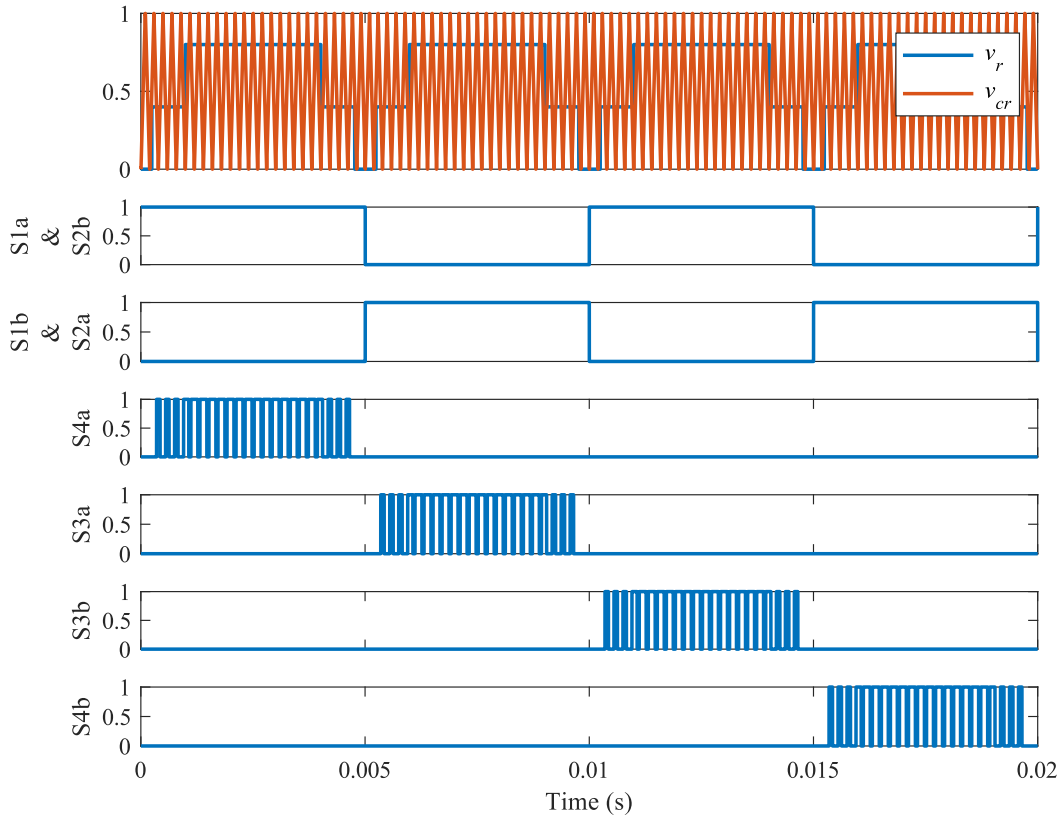


Figure 5.64 Reference, carrier, and switching signals for 100 Hz output frequency employing SCPWM technique at 0.8 modulation index.

Figure 5.65 and Figure 5.66 depict the output voltage, output current, and source current waveforms and their associated harmonics for 25 Hz and 100 Hz output frequencies, respectively, achieved employing the SCPWM technique. The harmonics analyses indicate that the SCPWM technique produces harmonic components predominantly at frequencies that are multiples of the switching frequency. As a result, an increase in the output frequency is accompanied by a rise in the low-order harmonics. The output voltage and current THD results exhibit a direct proportionality to output frequencies higher than the source frequency and an inverse proportionality to output frequencies lower than the source frequency. There is an inverse proportionality between the source current THD and the frequencies of the synthesized outputs that are higher than the frequency of the source. Specifically, as the synthesized output frequency increases above the source frequency, the THD of the source current decreases proportionally.

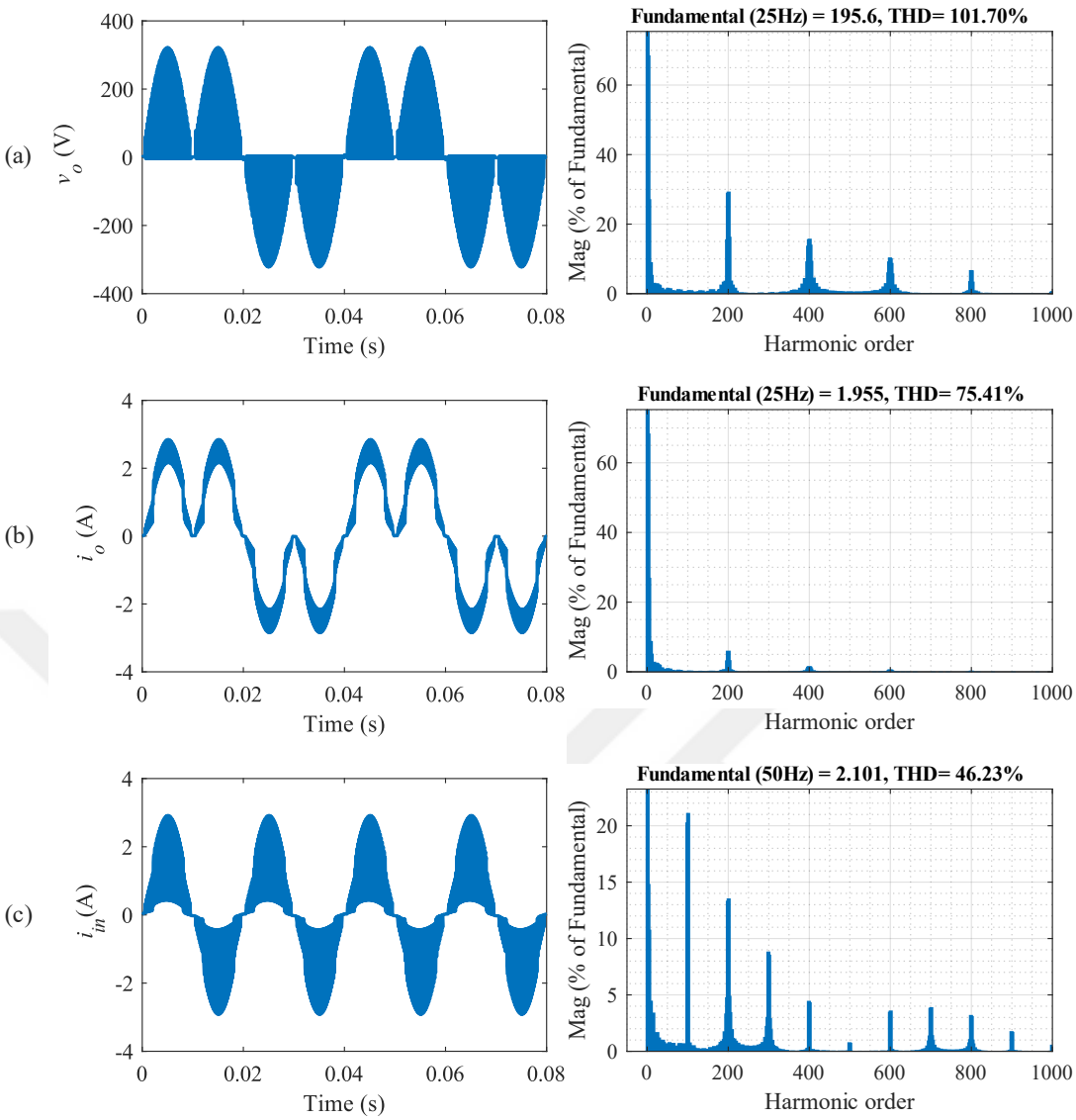


Figure 5.65 (a) Output voltage, (b) output current, and (c) source current waveforms and their harmonics for 25 Hz output frequency employing the SCPWM technique at 0.8 modulation index.

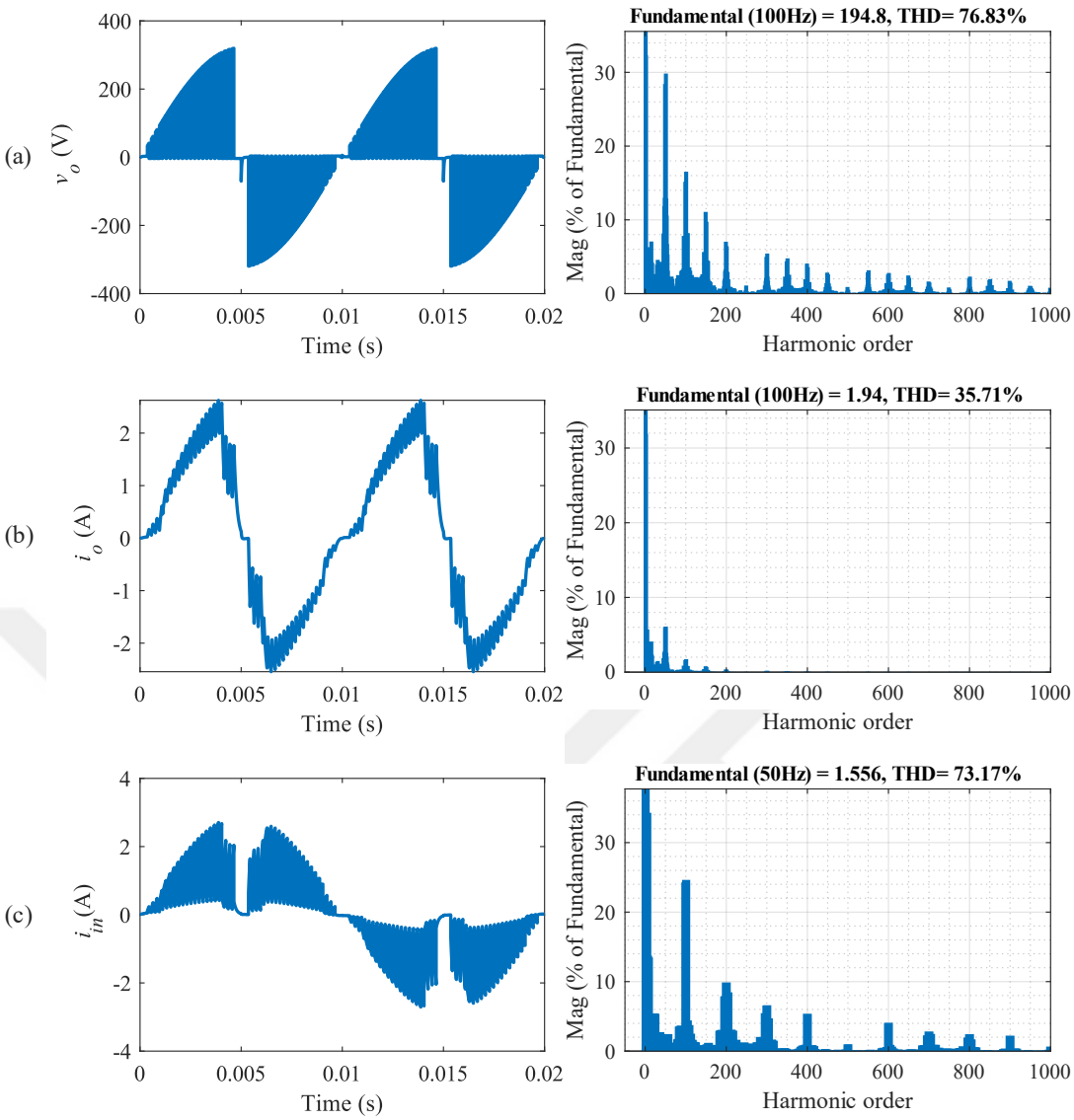


Figure 5.66 (a) Output voltage, (b) output current, and (c) source current waveforms and their harmonics for 100 Hz output frequency employing the SCPWM technique at 0.8 modulation index.

5.3.4 TPWM

The TPWM technique utilizes a trapezoidal reference signal v_r to generate the PWM gate-triggering signals, as shown in Figure 5.67. Throughout the simulations, k is kept at 1/3.

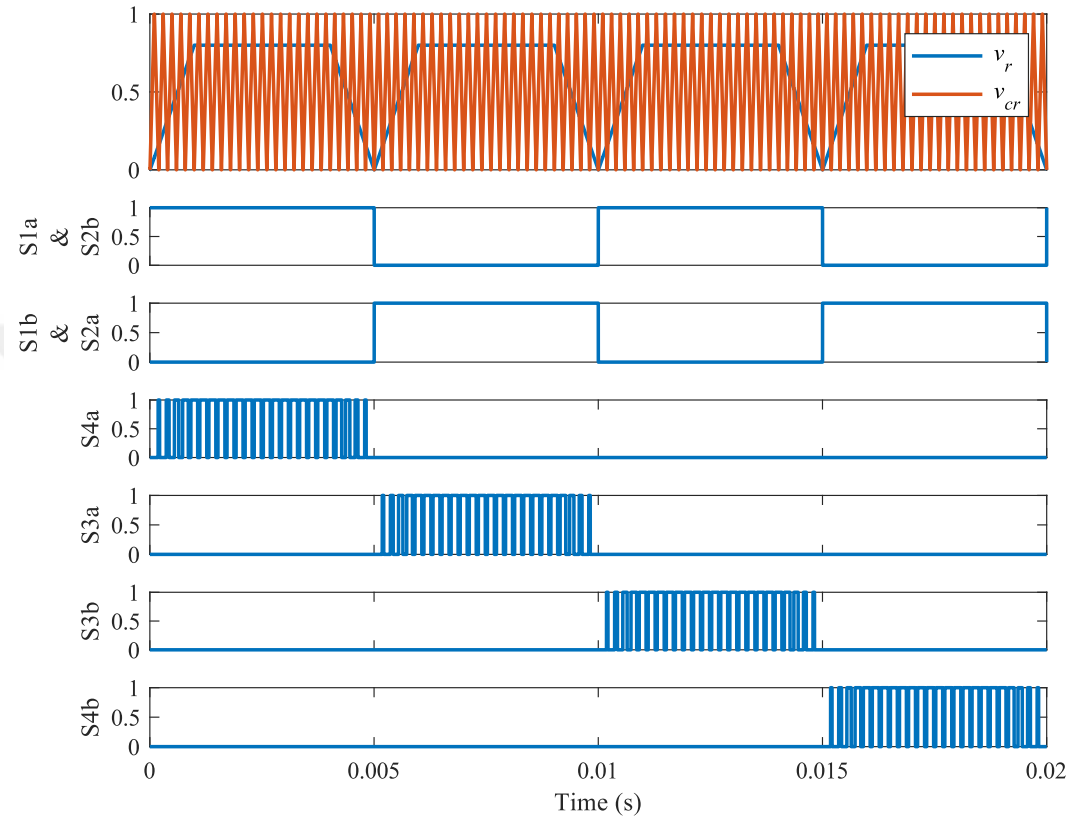


Figure 5.67 Reference, carrier, and switching signals for 100 Hz output frequency employing TPWM technique at 0.8 modulation index.

The output voltage, output current, and source input current waveforms and their associated harmonics at 25 Hz and 100 Hz output frequencies using the TPWM technique are illustrated in Figure 5.68 and Figure 5.69, respectively. The harmonics analysis indicates that the TPWM technique produces harmonic components predominantly at frequencies that are multiples of the switching frequency. As a result, an increase in the output frequency is accompanied by a rise in the low-order harmonics. The THD of the output voltage and current increases proportionally with the output frequency deviation from the source frequency.

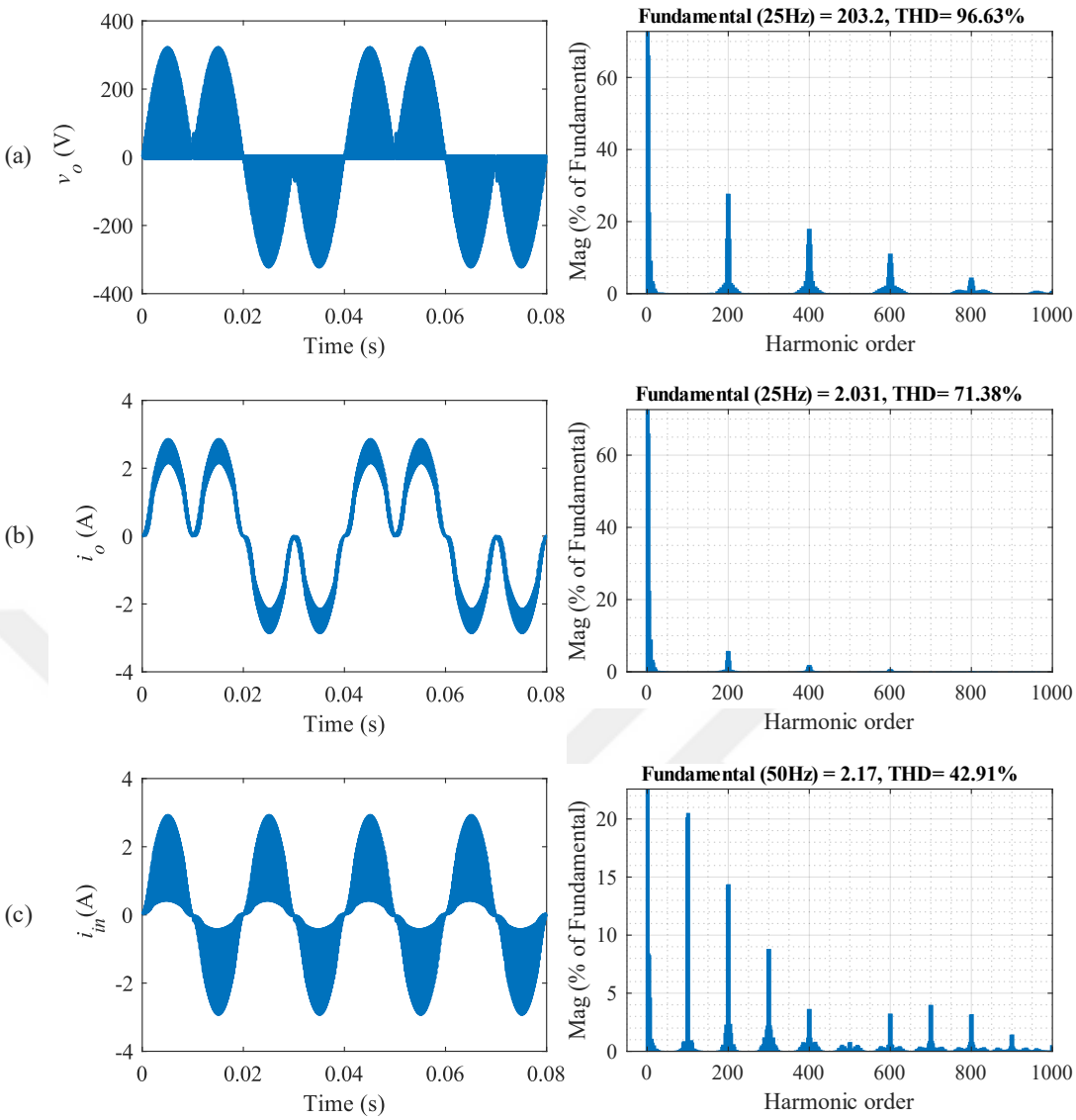


Figure 5.68 (a) Output voltage, (b) output current, and (c) source current waveforms and their harmonics for 25 Hz output frequency employing the TPWM technique at 0.8 modulation index.

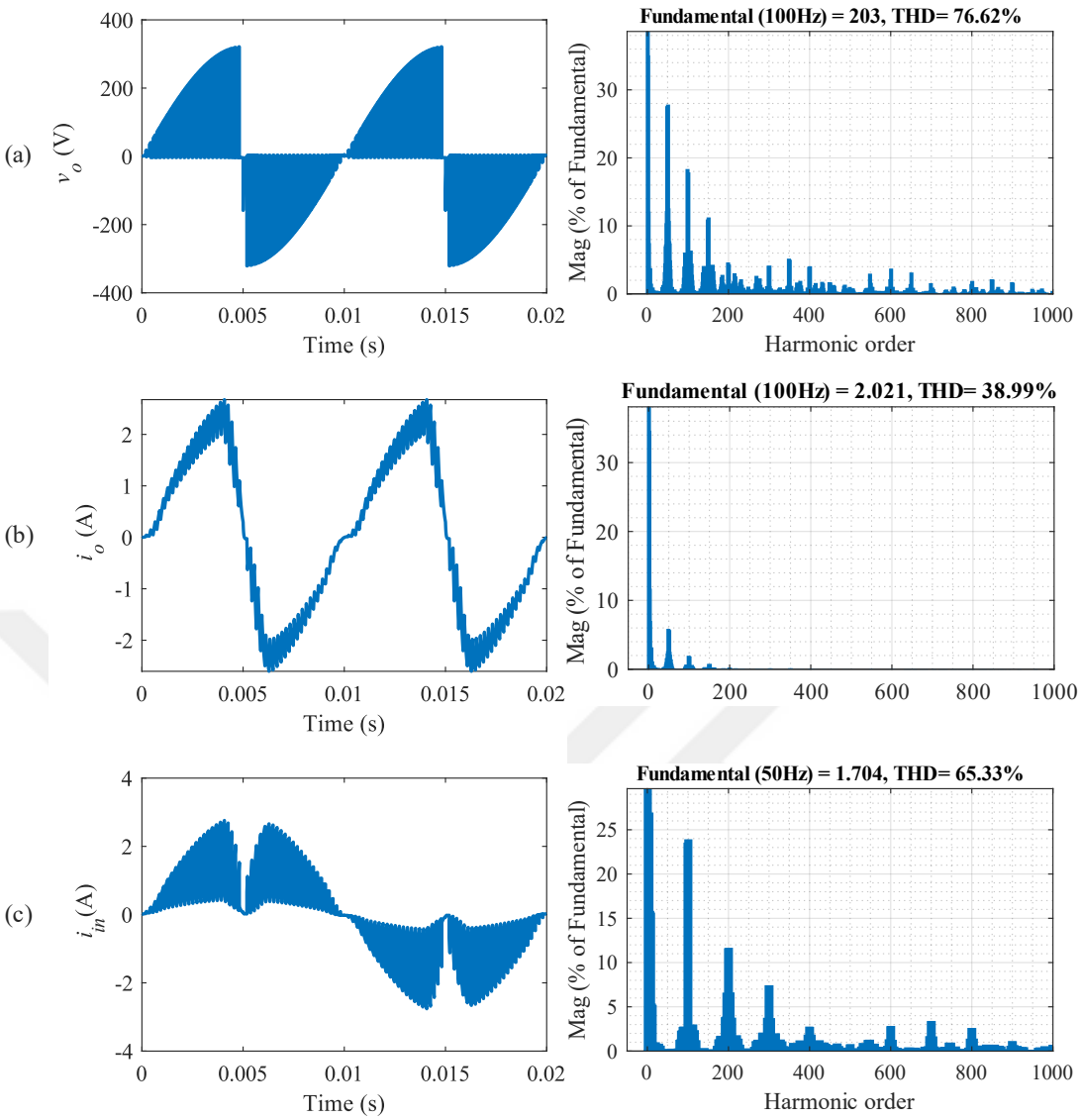


Figure 5.69 (a) Output voltage, (b) output current, and (c) source current waveforms and their harmonics for 100 Hz output frequency employing the TPWM technique at 0.8 modulation index.

5.3.5 Comparison of SSMC Performance Parameters with Carrier-Based PWM Techniques

The variation of the VTR with modulation index using the different carrier-based PWM techniques is shown in Figure 5.70. As expected, the MPWM technique provides the highest VTRs across all output frequencies and modulation indexes. When the MPWM technique results are compared with the SPWM, it is found that the MPWM increases VTR at unity modulation index by around 8.12% and 22% at output frequencies less than or equal to the source and higher than the source frequency, respectively. Comparing MPWM with SCPWM reveals an increase in VTR in favor of MPWM by approximately 2.5% and 14.44% for output frequencies lower than or

equal to the source frequency and higher than the source frequency, respectively, at unity modulation index. On the other hand, MPWM yields an increase in VTR of approximately 1.24% and 10.73% for output frequencies less than or equal to and greater than the source frequency, respectively, when compared to TPWM at unity modulation index. Hence, it can be concluded that the TPWM provides the highest VTRs after the MPWM technique. However, as mentioned above, unlike the MPWM, the TPWM showed no need for a clamp circuit for most output frequencies.

The variation of output voltage THD with modulation indexes is shown in Figure 5.71. The SPWM technique presented the highest output voltage THD percentages for all output frequencies. The lowest percentages are exhibited by the MPWM and TPWM for output frequencies lower than and equal to the source frequency and output frequencies higher than the source frequency, respectively. When comparing the MPWM with TPWM, results reveal that the MPWM provides lower output voltage THD by around 14.33%, 14.32%, and 175.98% at 12.5 Hz, 25 Hz, and 50 Hz output frequencies, respectively, where the TPWM provides lower THD by around 23.17%, 19.32%, and 13.07% at 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively.

The variation of output current THD with modulation index is shown in Figure 5.72. It is clear that no method provides stable results for all output frequencies. The SPWM and MPWM techniques provided the highest and lowest output current THD percentages for output frequencies lower than or equal to the source frequency, respectively. However, this situation is reversed for output frequencies higher than the source frequency, as MPWM and SPWM techniques provided the highest and lowest percentages, respectively. More precisely, when the MPWM and SPWM techniques are compared at unity modulation index for output frequencies lower than the source frequency, the MPWM provides less output current THD by around 24.63%. However, for output frequencies higher than the source, the MPWM provides higher output current THD by around 59.18%, 47.38%, and 29.73% for 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively.

When it comes to the source current THD, all techniques provide similar behavior for all output frequencies, as shown in Figure 5.73. Generally, the SPWM and MPWM techniques provided the highest and lowest source current THD percentages, respectively. A comparison between the MPWM and SPWM techniques reveals that,

for output frequencies lower than or equal to the source frequency, MPWM reduces the THD in the source current by around 189.56%, and for output frequencies higher than the source frequency, the reduction in THD is around 120.8%. Table 5.2 summarizes the outcomes of the comparisons. It is clear that each modulation technique has its set of advantages and disadvantages, and determining the optimal technique depends on the application.

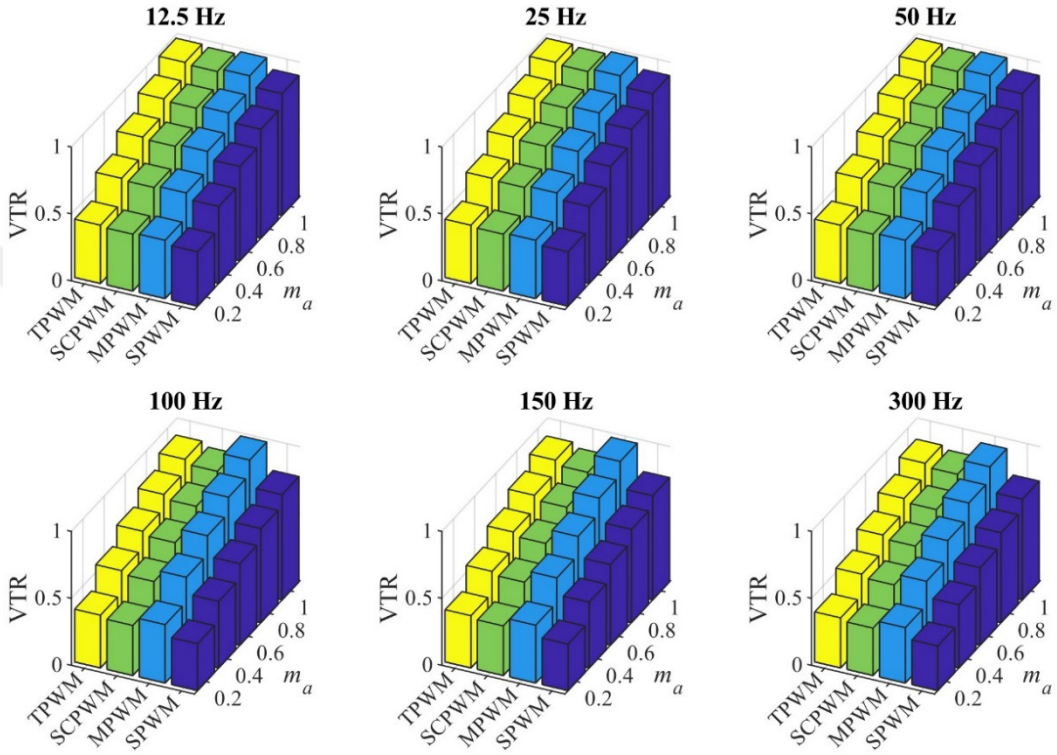


Figure 5.70 Variation of voltage transfer ratio with modulation indexes employing several modulation techniques.

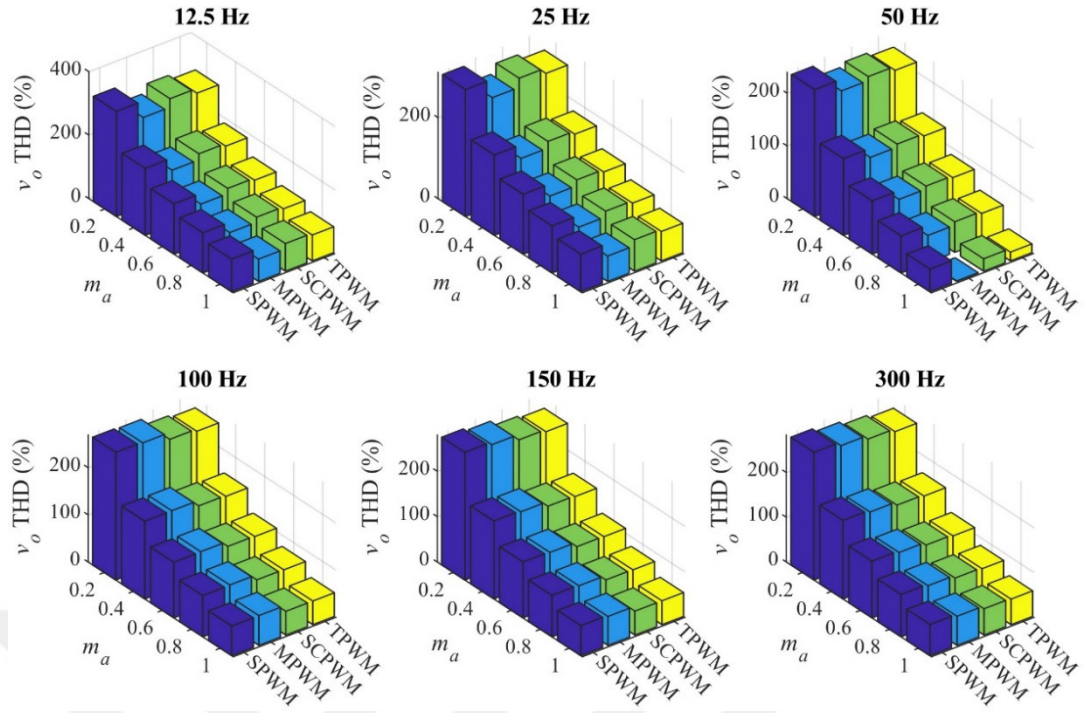


Figure 5.71 Variation of output voltage THD with modulation indexes employing several modulation techniques.

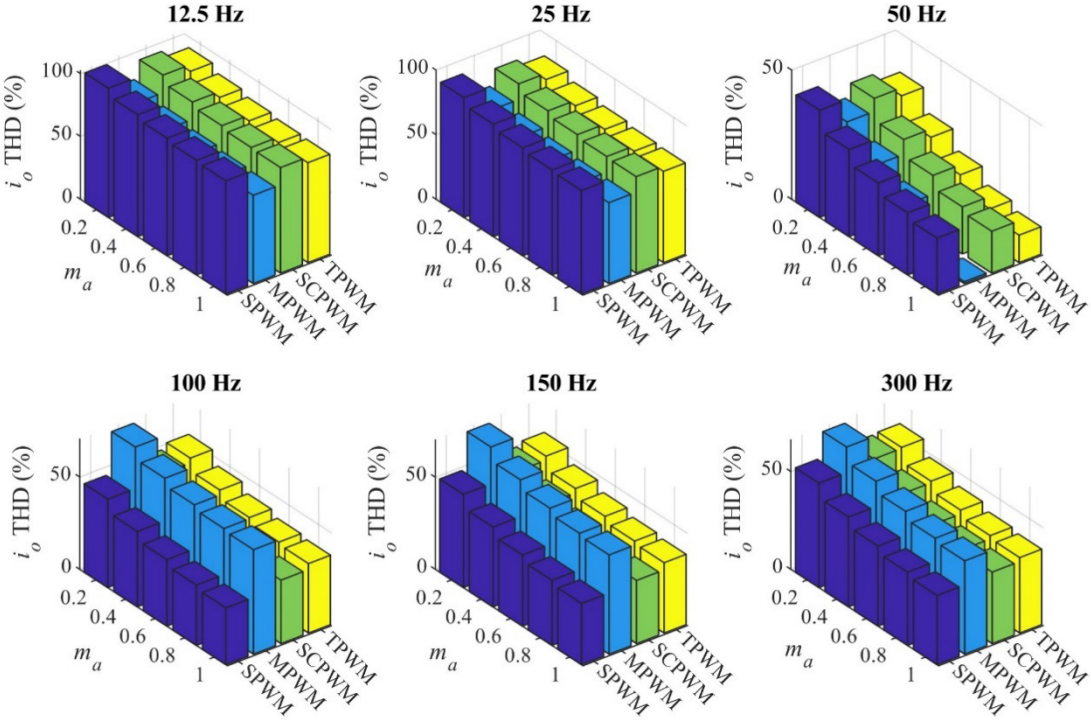


Figure 5.72 Variation of output current THD with modulation indexes employing several modulation techniques.

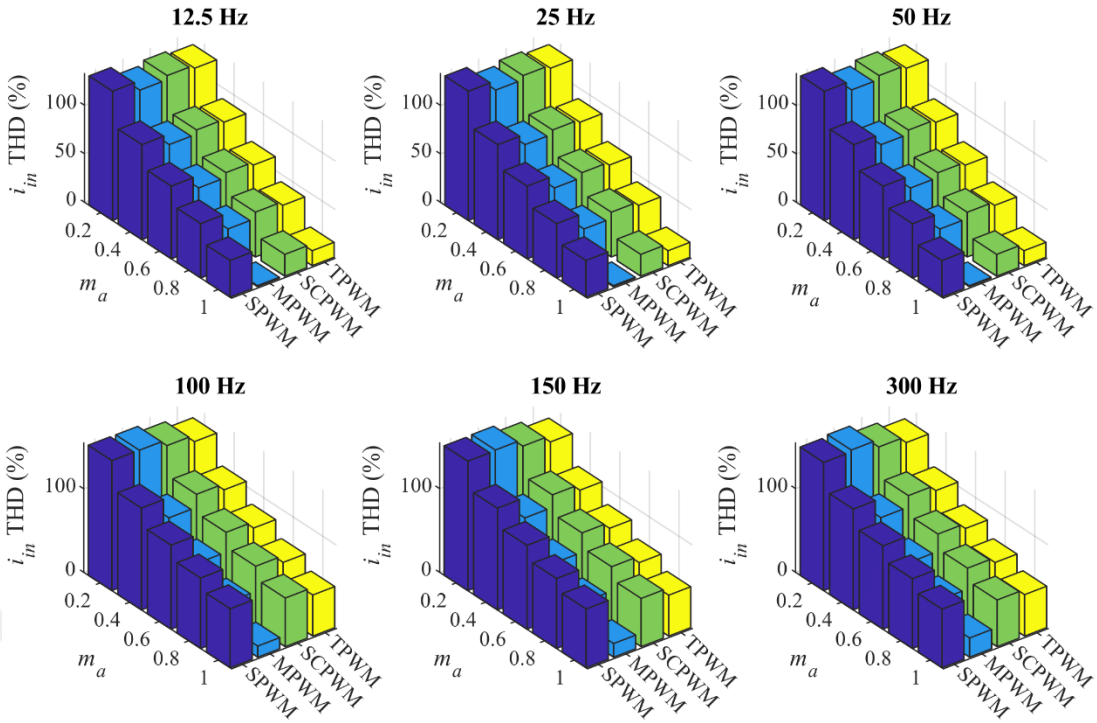


Figure 5.73 Variation of source input current THD with modulation indexes employing several modulation techniques.

Table 5.2 Comparison summary of carrier-based PWM techniques.

Modulation Technique	ZCS for $f_o > f_{in}$	Clamp circuit	VTR for $f_o f_{in}$	VTR for $f_o > f_{in}$	v_o THD for $f_o \leq f_{in}$	v_o THD for $f_o > f_{in}$	i_o THD for $f_o \leq f_{in}$	i_o THD for $f_o > f_{in}$	i_{in} THD
SPWM	Yes	For $f_o > 3f_{in}$	> 0.9	> 0.75	High	High	High	Low	High
MPWM	No	For $f_o > f_{in}$	> 0.98	> 0.93	Low	High	Low	High	Low
SCPWM	Yes	For $f_o > 3f_{in}$	> 0.96	> 0.82	High	Low	High	Low	Low
TPWM	Yes	For $f_o > 3f_{in}$	> 0.97	> 0.85	Low	Low	High	Low	Low

5.4 Conclusion

In this chapter, the results of the simulation studies are presented. First, the results of a simulation study containing three case studies that shows the superiority of the proposed SSMC control method over the counterpart methods in the literature are demonstrated. Then, the results of a simulation study that analyzes and compares the key performance parameters of the SSMC when controlled by different carrier-based PWM techniques are demonstrated.

CHAPTER 6
EXPERIMENTAL STUDIES

6.1 Introduction

This chapter presents the results of the experimental studies on the SSMC. For this purpose, a laboratory prototype is built. Similar to the simulation studies presented in Chapter 5, the superiority of the proposed SSMC control method (presented in Chapter 4) over the counterpart method in the literature is verified experimentally. A variety of output frequencies are synthesized, and multiple modulation indexes are considered to demonstrate the effectiveness of the proposed method. Among the experimental studies, analysis and comparison of the SSMC performance under four different carrier-based PWM techniques is carried out. In the following sections, first, the experimental setup components, along with its functional structure, are described. Then experimental studies results are presented.

6.2 Description of the Experimental Setup

The experimental setup is shown in Figure 6.1. The functional structure of the experimental setup is illustrated in Figure 6.2. The operation conditions, along with the utilized components, are given in Table 6.1. The source voltage RMS value is controlled using a variac. An input filter is used to filter the source input voltage before being supplied to the SSMC power circuit. IHW20N135R5 IGBTs with monolithic body diode are used as the SSMC power switches [181]. Figure 6.3 shows the SSMC circuit board. The output terminals of the SSMC are connected to the RL load. The load consists of a constant inductor that is connected in series with an adjustable resistive load. A DC power supply is used to supply the LM358P operational amplifier for the ZCD circuit [182]. The power switches gates are driven using TLP250 gate driver and photodetector [183]. The gate drivers are supplied using an isolated DC power supply, which is formed by stepping down the grid AC voltage using a step-down transformer and then supplying it to a full-wave rectifier to be converted to DC, where it is filtered using a smoothing capacitor. Basys 3 Artix-7 FPGA board is responsible for generating the gating signals which are given to the gate drivers [184].

The input and output waveforms are visualized using AA Tech ADS-3204A digital storage oscilloscope. The input and output voltage waveforms are measured using differential probes, whereas the current waveforms are measured using current clamp probes.

To protect each IGBT from overvoltage transients, an anti-series transient voltage suppressor (TVS) diode P6KE440CA is connected between the gate and collector of each IGBT [185]. The P6KE440CA TVS has a maximum reverse stand-off voltage of 376 V and a maximum clamp voltage of 602 V which is below the maximum collector-emitter voltage of the IGBTs and body diodes.

The ZCD circuit detects the state (zero-crossing points) of the source AC input voltage by generating a pulse signal that is high when the source voltage is in its positive half cycle and low when it is in its negative half circuit. The ZCD pulse signal is given to an ATmega328P-based microcontroller [186], where it generates two complementary pulse signals (v_{p1} and v_{p2}) that are given to the FPGA. Figure 6.4 shows the input and output signals to the ZCD circuit and microcontroller.

In this work, FPGA is used as the main control unit, where it generates the IGBTs gate pulse signals. The proposed control scheme is implemented on the FPGA. The overall architectural design is depicted in Figure 6.5. Each of the design modules is programmed using very high-speed integrated circuit hardware description language (VHDL). Xilinx Vivado Design Suite 2021.1v is used to simulate the design and to implement it on the FPGA board. Dead times t_{d1} and t_{d2} are added inside the comparator module and commutation signals generator module, respectively.

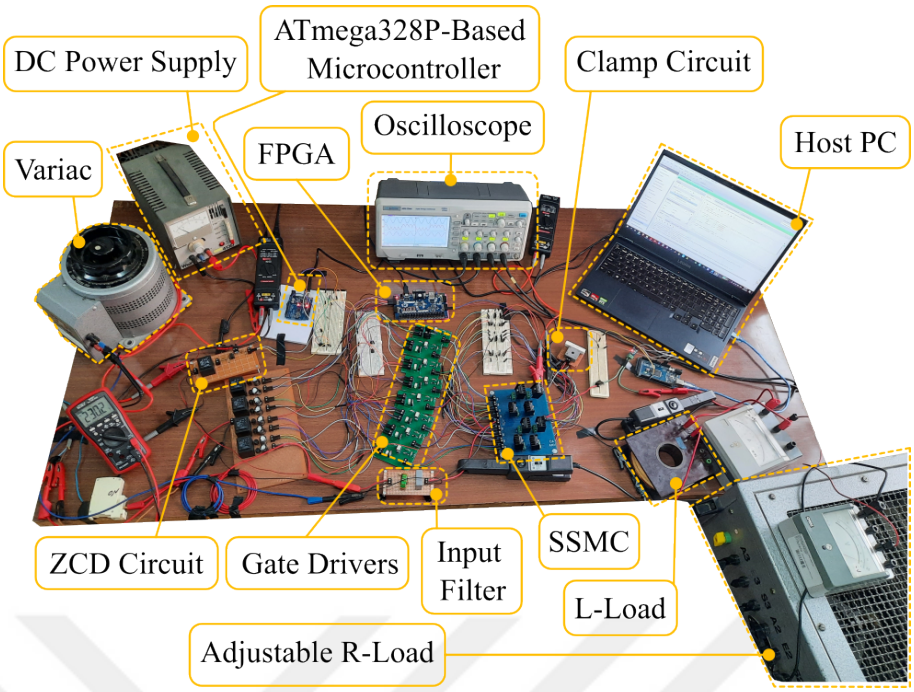


Figure 6.1 The experimental setup.

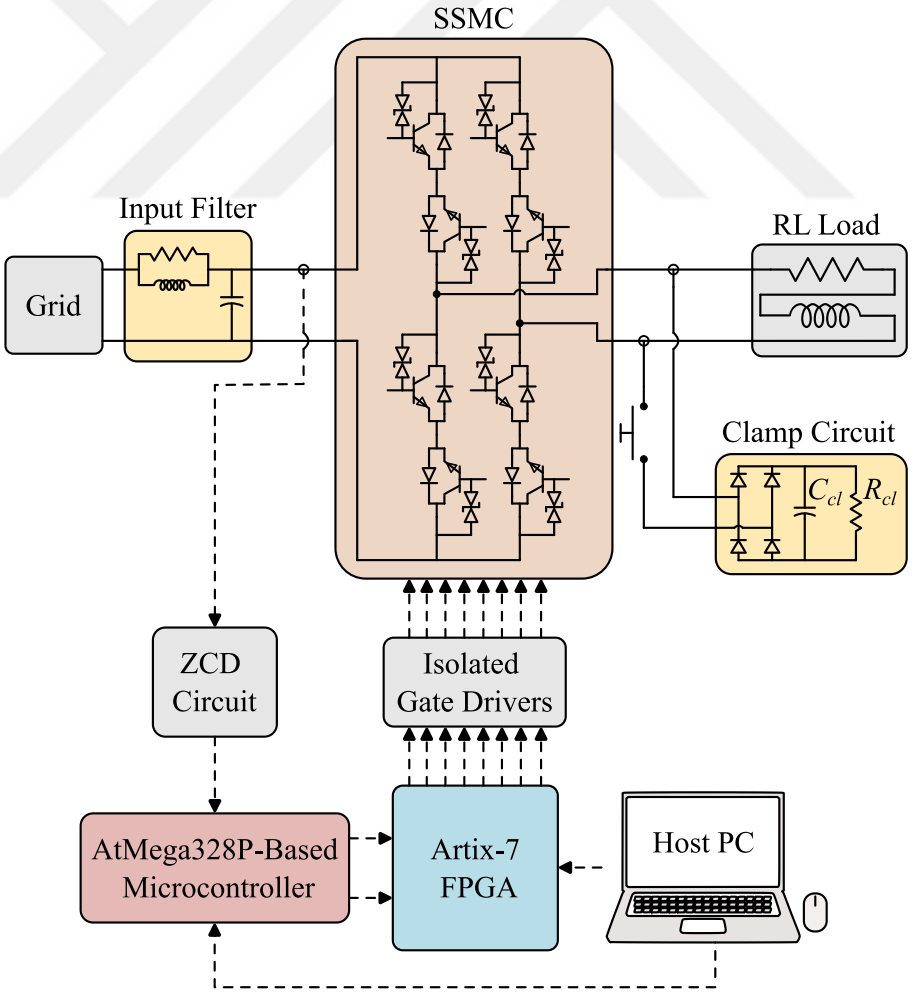
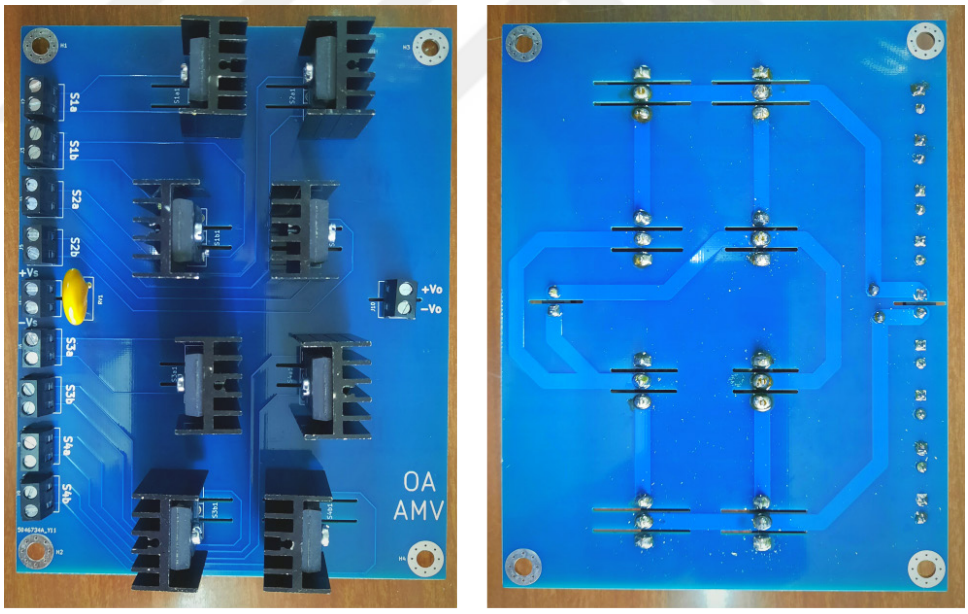


Figure 6.2 Functional structure of the experimental setup.

Table 6.1 Specifications of the experimental system.

Operating Conditions	
Output power	530 W
Source voltage	230 Vrms
Source frequency	50 Hz
Switching frequency	5 kHz
RL-Load	100 Ω + 15 mH
Clamp resistor	1 k Ω
Clamp capacitor	1 nF
Input filter inductance	1 mH
Input filter capacitance	10 μF
Input filter resistance	47 Ω
Utilized Components	
IGBT	IHW20N135R5
Operational amplifier	LM358P
ZCD microprocessor	ATmega328P
FPGA	Basys 3 Artix-7
Gate driver	TLP250
TVS diode	P6KE440CA
Clamp rectifier	MB3510



(a) (b)

Figure 6.3 SSMC power circuit: (a) front and (b) back view.

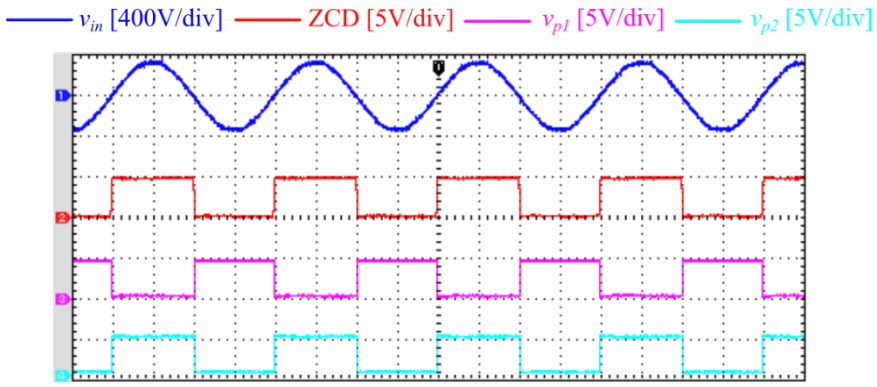


Figure 6.4 Input and output signals to the ZCD circuit and ATmega328P-based microcontroller t [5 ms/div].

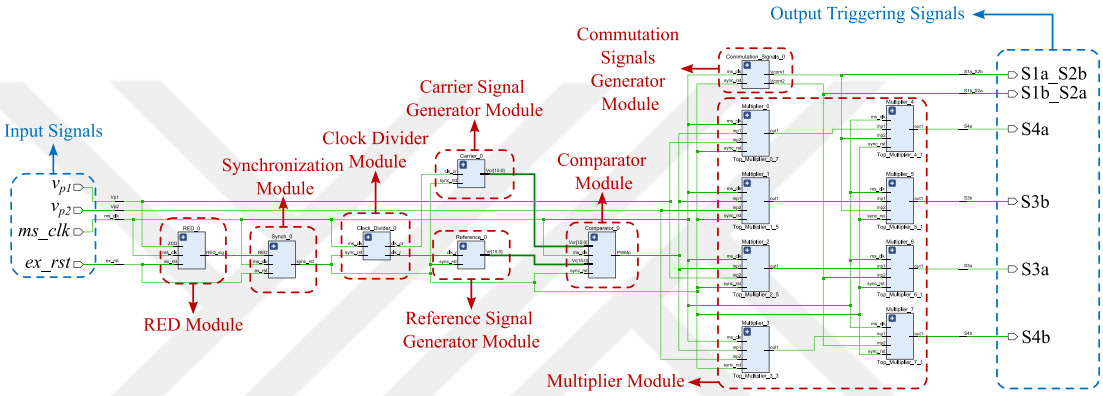


Figure 6.5 Overall architectural design structure of FPGA implementation of the proposed SSMC control scheme.

6.3 Experimental Verification of the Proposed SSMC Control Method

In this section, two case studies are conducted to experimentally show the superiority of the proposed control method, presented in Chapter 4, over the counterpart method in the literature. The operation conditions of the simulation study, presented in Section 5.2, are preserved in the experimental study.

6.3.1 Case Study 1: Operation Under RL Load

In this case study, the SSMC is tested without using a clamp circuit when connected to an RL load of 100 Ω + 15 mH in order to show the effectiveness of the proposed method in mitigating the output voltage spikes during commutation. The instantaneous power transfer with discontinuous input current makes the use of an input filter necessary to obtain acceptable waveforms. Similar to the simulation, k in this case study, is taken as 1/3. Figure 6.6 and Figure 6.7 show the input and output waveforms for this case obtained using the proposed and counterpart methods, respectively. It is

clear that at unity modulation index, the proposed method offers less waveform distortion when compared with the counterpart method of [127], [128]. With this in mind, Figure 6.8 and Figure 6.9, show the output voltage and source input current THD, respectively, using the proposed method and the counterpart method. The proposed method surpasses the counterpart method for all output frequencies. More specifically, the proposed method reduces the output voltage THD at unity modulation index by around 20.22%, 24.43%, 86.03%, 23.07%, 21.65%, and 25.69% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively. The proposed method also reduces the source input current THD by around 76.05%, 72.37%, 75.45%, 34.81%, 33.55%, and 33.37% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively. The variation in the VTR with the modulation index obtained using the proposed method and the counterpart method is shown in Figure 6.10. The proposed method offers further voltage transfer by around 9.1%, 7.55%, 8.1%, 9.84%, 10.59%, and 14.66% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively.

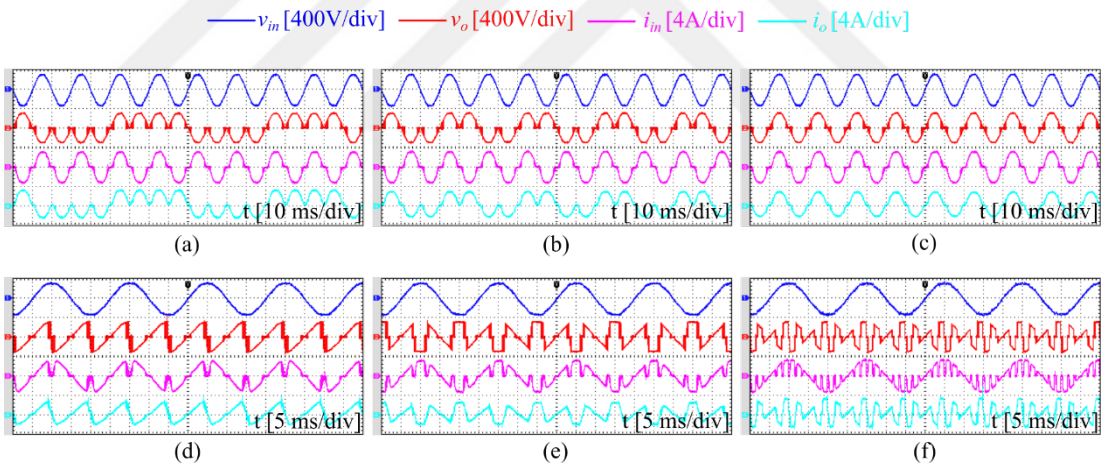


Figure 6.6 Experimentally obtained input and output waveforms using the proposed method (k = 1/3) at unity modulation index for (a) 12.5 Hz, (b) 25 Hz, (c) 50 Hz, (d) 100 Hz, (e) 150 Hz, and (f) 300 Hz output frequencies.

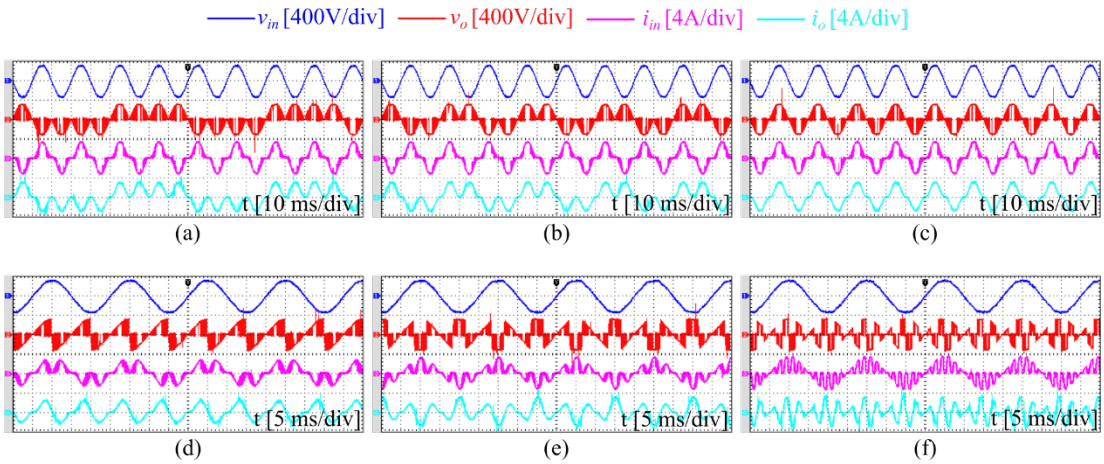


Figure 6.7 Experimentally obtained input and output waveforms using the counterpart method of [127], [128] at unity modulation index for (a) 12.5 Hz, (b) 25 Hz, (c) 50 Hz, (d) 100 Hz, (e) 150 Hz, and (f) 300 Hz output frequencies.

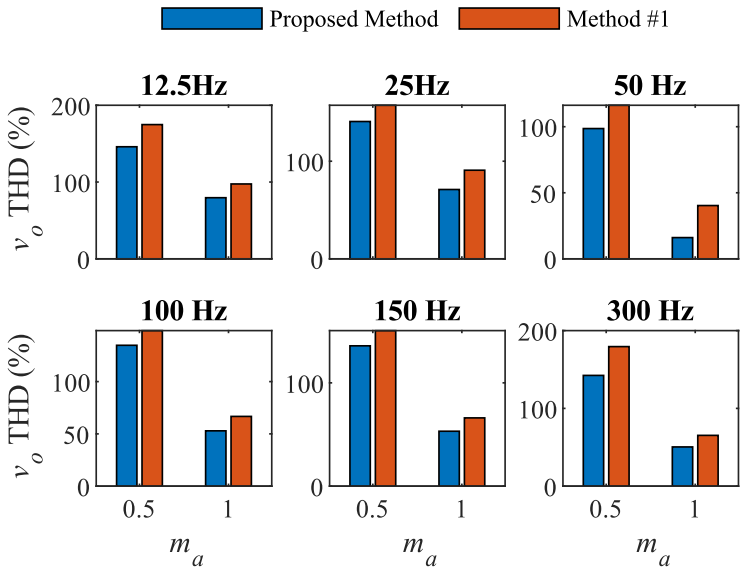


Figure 6.8 Comparison of experimental output voltage THD results.

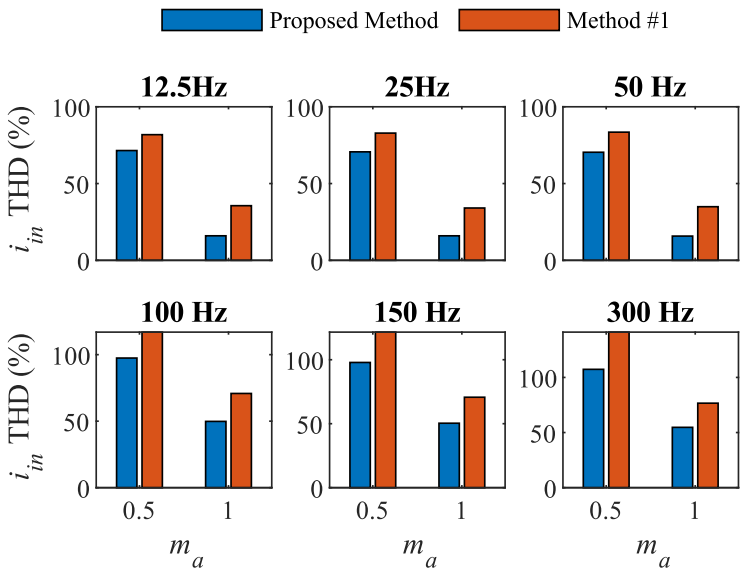


Figure 6.9 Comparison of experimental source current THD results.

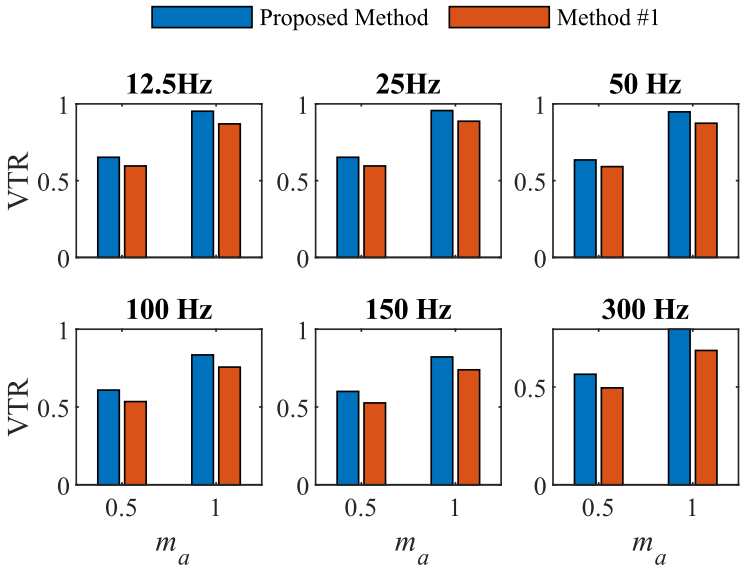


Figure 6.10 Comparison of experimental VTR results.

6.3.2 Case Study 2: Operation Under RL Load with a Clamp Circuit

This case study demonstrates the effectiveness of the proposed method in controlling the SSMC to achieve roughly unity VTRs. The SSMC is tested under the same operating conditions of the previous case, however, with k set to zero. Further, a clamp circuit is connected in parallel with the RL load to eliminate output voltage transients. Figure 6.11 demonstrates the input and output waveforms for this case study. The obtained results for the output voltage THD, source input current THD, and VTR for

this case study are illustrated in Figure 6.12, Figure 6.13, and Figure 6.14, respectively. Results show the effectiveness of the proposed method in suppressing the output voltage and source input current THD and achieving roughly unity VTRs. When the results of this case (k = 0) are compared with the previous case (k = 1/3) at unity modulation index, this case shows an increase in the voltage transfer by around 1.81%, 1.35%, 0.91%, 10.84%, 11.47%, and 7.87% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively. Thus, it is clear that it significantly improves the voltage transfer for synthesized output frequencies higher than the source frequency.

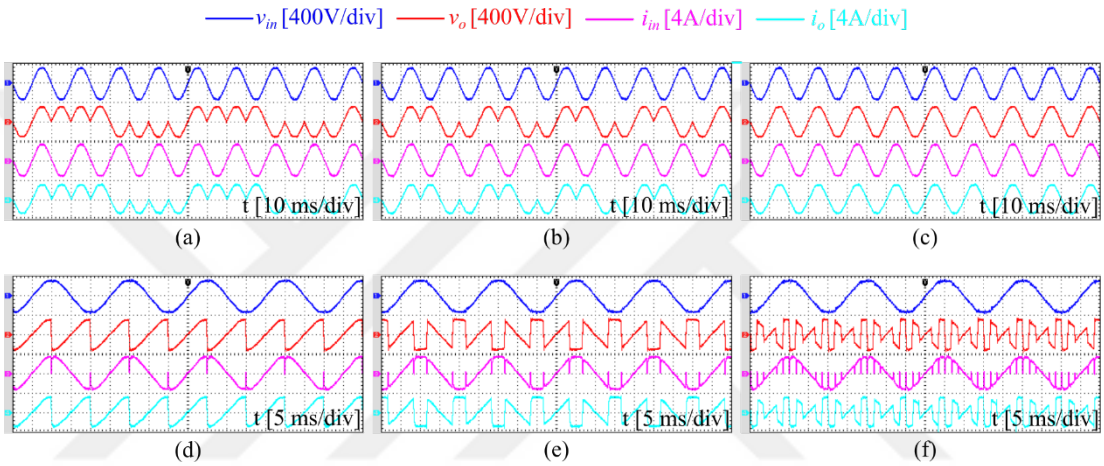


Figure 6.11 Experimentally obtained input and output waveforms using the proposed method (k = 0) with a clamp circuit at unity modulation index for (a) 12.5 Hz, (b) 25 Hz, (c) 50 Hz, (d) 100 Hz, (e) 150 Hz, and (f) 300 Hz output frequencies.

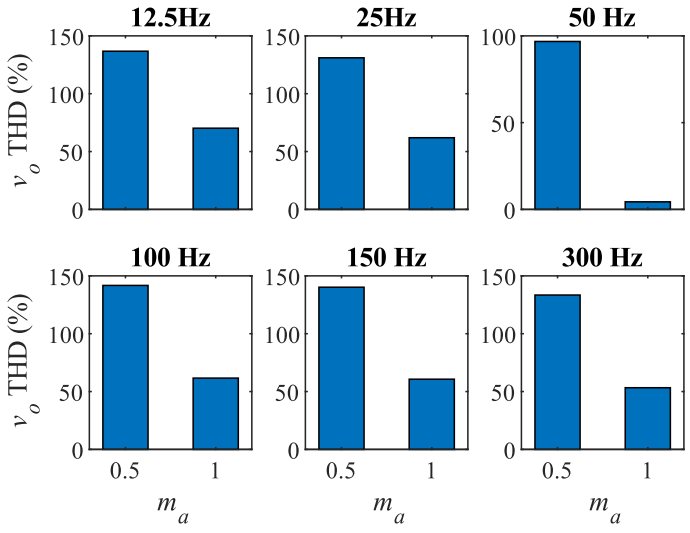


Figure 6.12 Experimental output voltage THD results using the proposed method when k = 0.

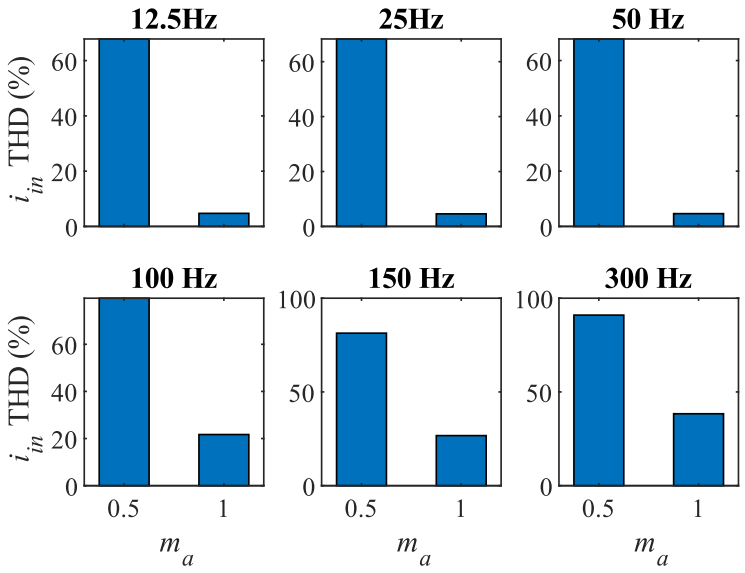


Figure 6.13 Experimental source current THD results using the proposed method when $k = 0$.

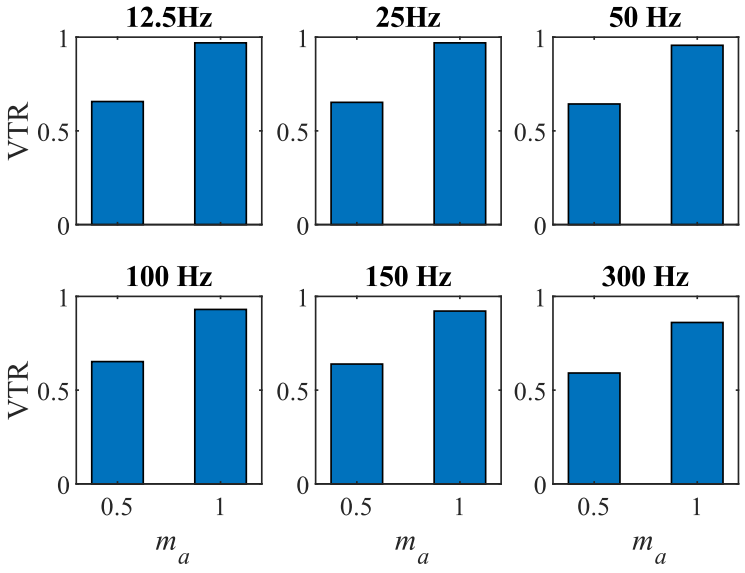


Figure 6.14 Experimental VTR results obtained using the proposed method when $k = 0$.

6.4 Experimental Comparison of SSMC Performance Parameters with Carrier-Based PWM Techniques

The input and output waveforms obtained for 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies employing the different carrier-based PWM techniques at unity modulation index are shown in Figure 6.15 to Figure 6.20, respectively. The influence of the modulation technique on the performance characteristics is evident.

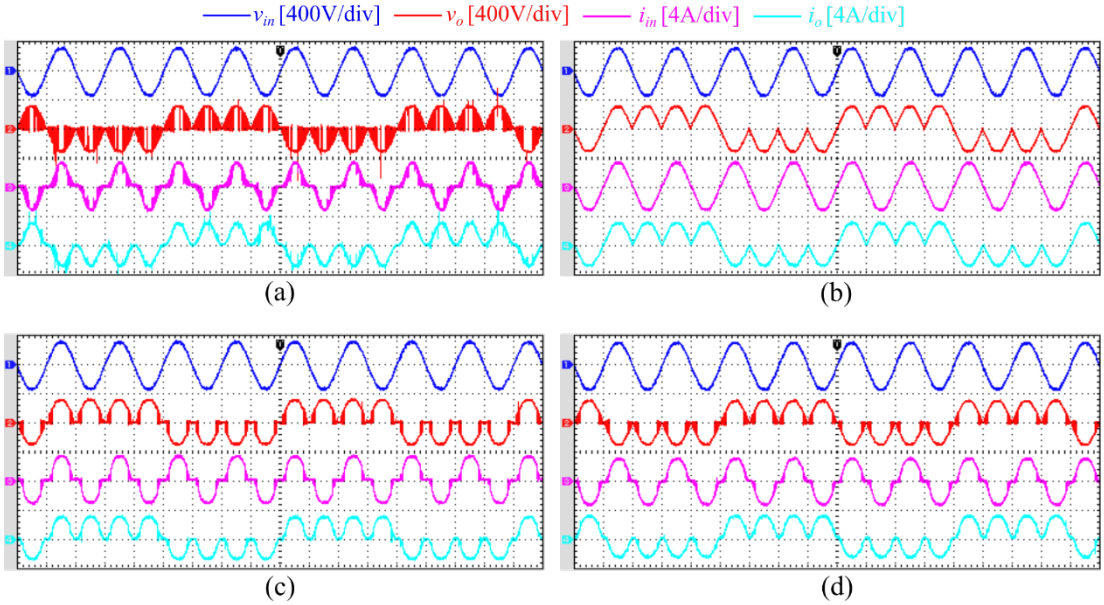


Figure 6.15 Experimental input and output waveforms for $f_o = 12.5$ Hz at $m_a = 1$ employing the (a) SPWM, (b) MPWM, (c) SCPWM, (d) TPWM techniques. t [10 ms/div].

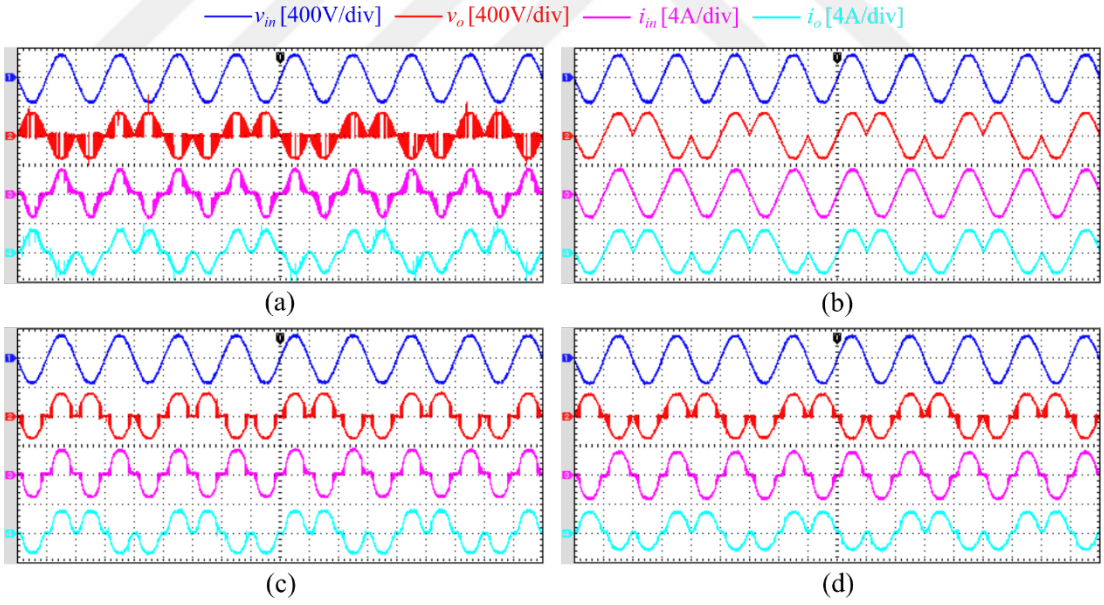


Figure 6.16 Experimental input and output waveforms for $f_o = 25$ Hz at $m_a = 1$ employing the (a) SPWM, (b) MPWM, (c) SCPWM, (d) TPWM techniques. t [10 ms/div].

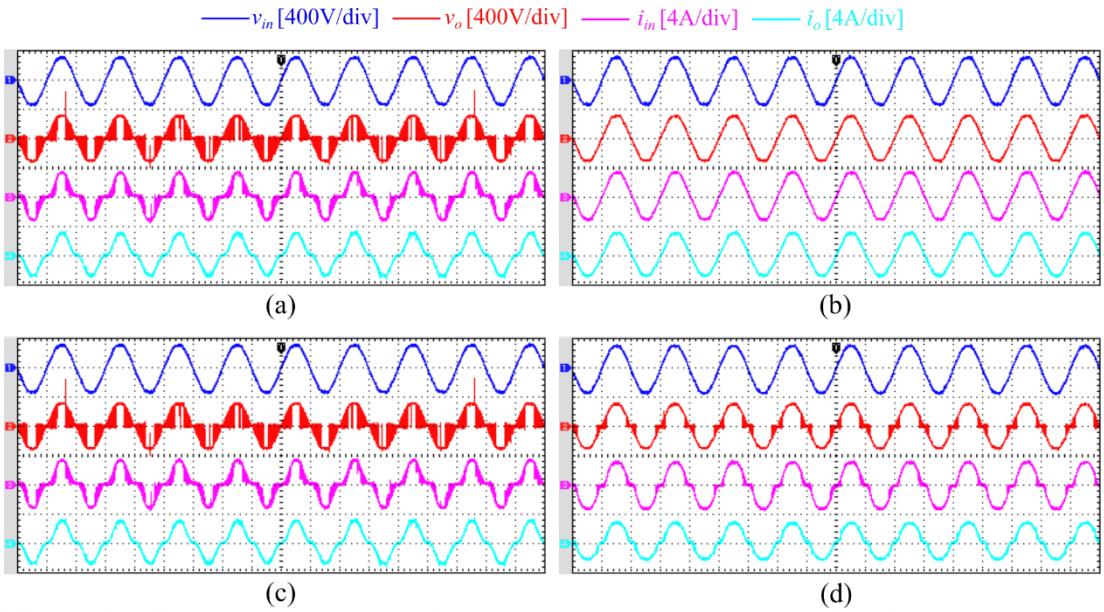


Figure 6.17 Experimental input and output waveforms for $f_o = 50$ Hz at $m_a = 1$ employing the (a) SPWM, (b) MPWM, (c) SCPWM, (d) TPWM techniques. t [10 ms/div].

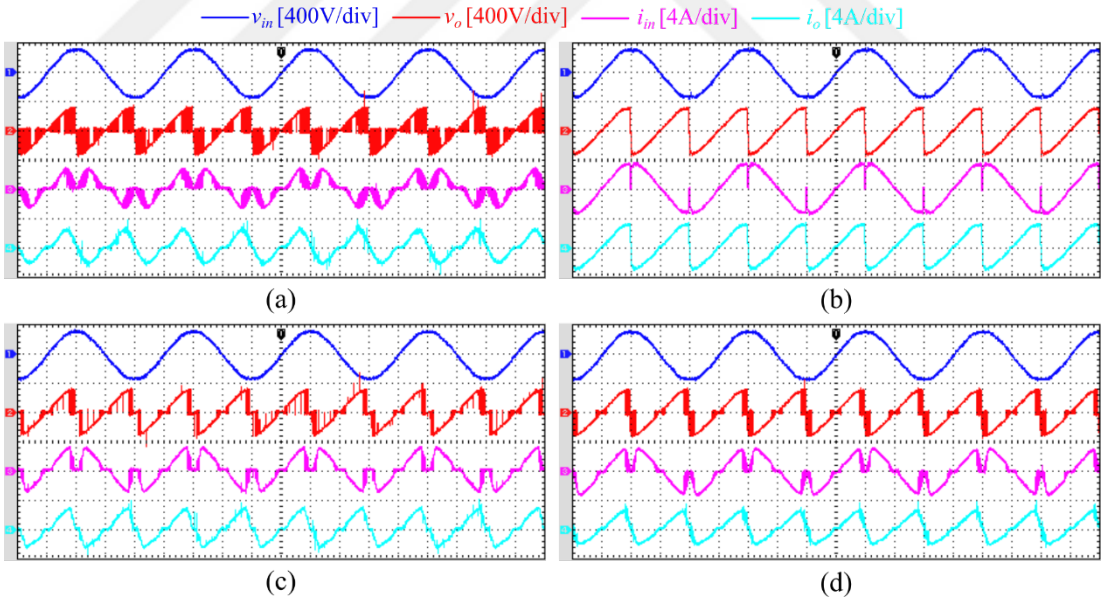


Figure 6.18 Experimental input and output waveforms for $f_o = 100$ Hz at $m_a = 1$ employing the (a) SPWM, (b) MPWM, (c) SCPWM, (d) TPWM techniques. t [5 ms/div].

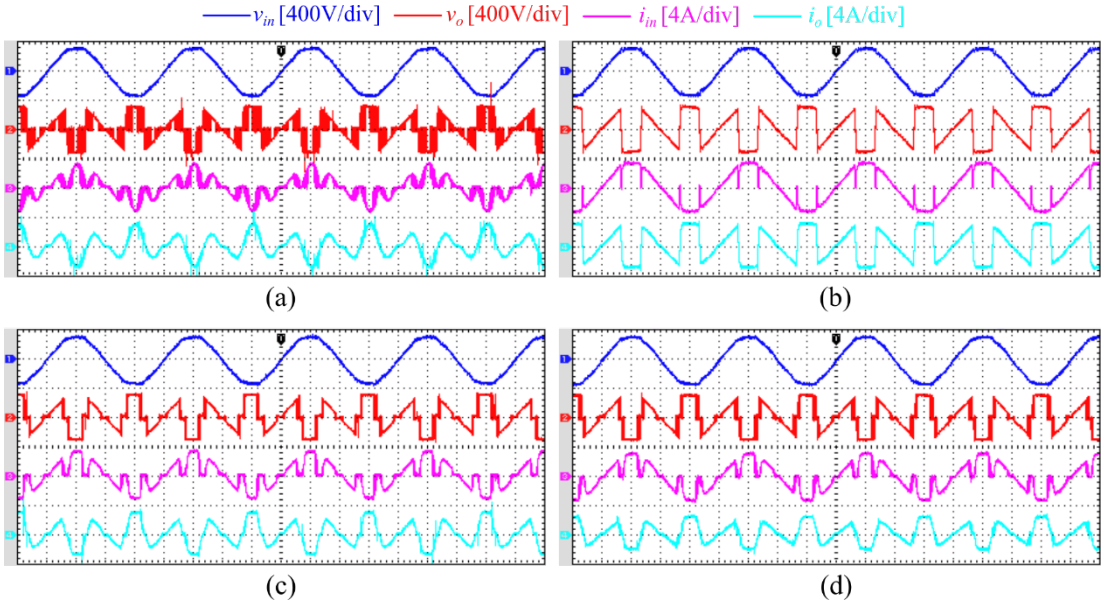


Figure 6.19 Experimental input and output waveforms for $f_o = 150$ Hz at $m_a = 1$ employing the (a) SPWM, (b) MPWM, (c) SCPWM, (d) TPWM techniques. t [5 ms/div].

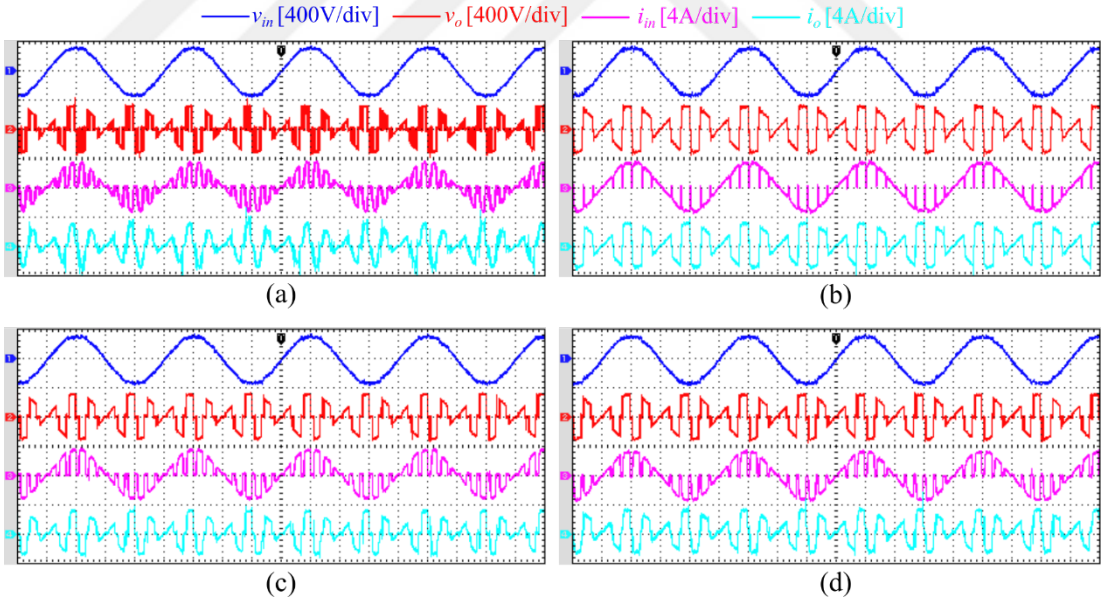


Figure 6.20 Experimental input and output waveforms for $f_o = 300$ Hz at $m_a = 1$ employing the (a) SPWM, (b) MPWM, (c) SCPWM, (d) TPWM techniques. t [5 ms/div].

The experimentally obtained variation of VTR with modulation indexes is depicted in Figure 6.21. As expected, the maximum VTRs are obtained using the MPWM technique. When the MPWM technique is compared with the SPWM technique at unity modulation index, an increase in the VTR in favor of the MPWM is achieved by around 9.34%, 11.2%, 8.54%, 21.91%, 21.31%, and 22.11% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively. The MPWM technique also increases the VTR when compared to SCPWM technique by around 4.05%, 4.5%, 4.65%, 18.31%, 16.94%, and 18.85% at output frequencies of 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz, respectively at unity modulation index. On the other hand, when the MPWM technique is compared with the TPWM technique, an increase in the VTR in favor of the MPWM is obtained by around 4.8%, 4.5%, 3.19%, 12.14%, 12.22%, and 13.17% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively at unity modulation index. Thus, compared to the SCPWM technique, the TPWM technique provides further increase in the VTR for output frequencies higher than the source frequency.

The experimentally obtained variation of output voltage THD with modulation indexes is depicted in Figure 6.22. The SPWM technique yielded higher output voltage THD percentages for all considered output frequencies and modulation indexes. For synthesized output frequencies lower than or equal to the source frequency, the lowest percentages are achieved using the MPWM technique. When the MPWM and SPWM techniques are compared at unity modulation index, results revealed that the MPWM technique reduces the output voltage THD by around 35.47%, 34.49%, 161.05%, 7.42%, 10.73%, and 20.23% at 12.5 Hz, 25 Hz, 50 Hz, 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively.

The experimentally obtained variation of output current THD with modulation indexes is depicted in Figure 6.23. The SPWM technique provides the highest output current THD percentages for output frequencies lower than or equal to the source frequency, and the MPWM provides the highest percentages for most output frequencies higher than the source frequency at unity modulation index. More precisely, compared to the SPWM technique, MPWM provides less output current THD by around 24.47% for output frequencies less than the source frequency and around 127.08% for output frequency equal to the source frequency at unity modulation index. Nevertheless, for

100 Hz, 150 Hz, and 300 Hz output frequencies, the SPWM technique provides less percentages by around 52.19%, 42.97%, and 9.08%, respectively.

The experimentally obtained variation of source input current THD with modulation indexes is depicted in Figure 6.24. The SPWM and MPWM techniques provide the highest and lowest source input current THD percentages for all output frequencies, respectively. More precisely, at unity modulation index, the MPWM technique reduces input current THD percentages when compared with the SPWM by around 153.97% for 12.5 Hz, 25 Hz, and 50 Hz output frequencies, and around 97.67%, 84.06%, and 61.02% for 100 Hz, 150 Hz, and 300 Hz output frequencies, respectively.

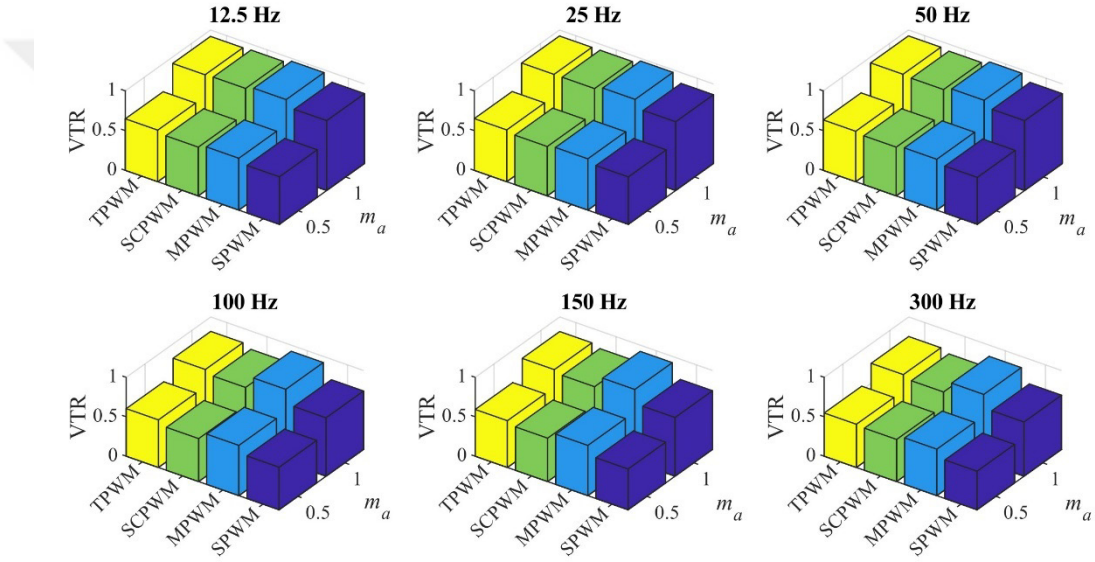


Figure 6.21 Experimental variation of VTR with modulation indexes employing several modulation techniques.

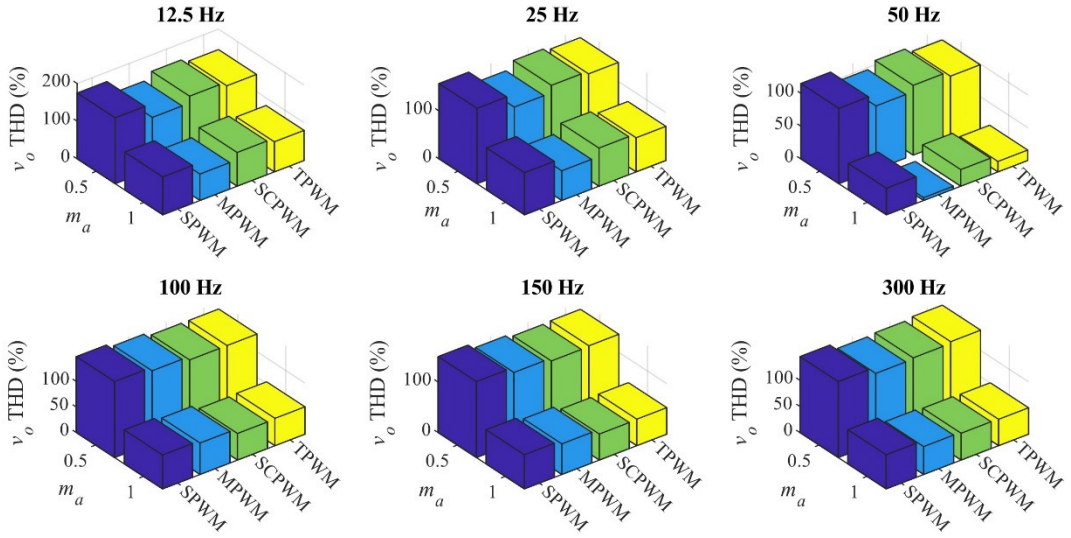


Figure 6.22 Experimental variation of output voltage THD with modulation indexes employing several modulation techniques.

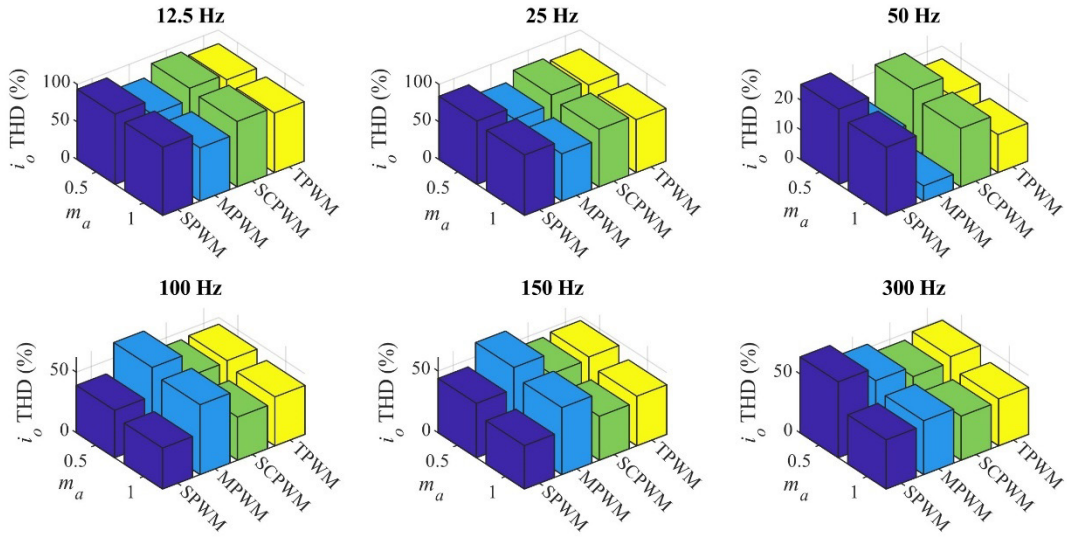


Figure 6.23 Experimental variation of output current THD with modulation indexes employing several modulation techniques.

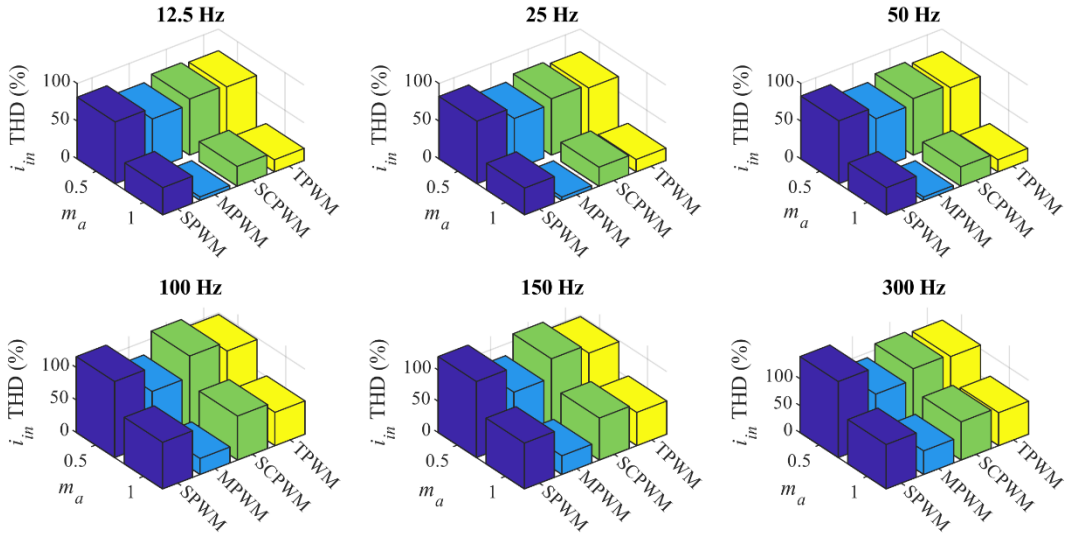


Figure 6.24 Experimental variation of source input current THD with modulation indexes employing several modulation techniques.

6.5 Conclusion

In this chapter, the results of the experimental studies are presented. First, a general overview and description of the laboratory experimental setup are provided. Then, the results of an experimental study with two case studies showing the superiority of the proposed SSMC control method over the counterpart method in the literature are presented. Lastly, the results of an experimental study analyzing the performance of the SSMC with the different carrier-based PWM techniques are presented.

CHAPTER 7
CONCLUSIONS

MCs are getting involved in a wide range of applications due to their favorable features, such as regeneration capability, bidirectional power flow, simple and compact power circuit, step-change frequency operation, and bipolar voltage gain. They mainly distinguish themselves from other AC-AC converters by directly converting the source power without the need for bulky energy storage elements as an intermediate connection. In the context of this thesis, the design and implementation of a SSMC is held. First, a review of commonly used TT and SS AC-AC power electronics converters is presented, highlighting the advantages of MCs over the other topologies. Then, a review of commonly used bidirectional switch topologies is presented, discussing the advantages, disadvantages, and requirements of each topology. Later, the current commutation problem encountered by MCs when connected to RL loads is discussed, along with the commonly utilized solutions. Then, the protection approaches of MCs against source/load overvoltage are discussed. Later, the control techniques of MCs are presented. Then, the different operation states of the SSMC that allow it to achieve a bipolar voltage gain are investigated. Next, the SSMC switching strategy for step-changed frequency operation is demonstrated. Later, the principles of carrier-based PWM techniques for controlled voltage operation of the SSMC are investigated. Then, the proposed SSMC control method and synchronization algorithm are presented. Later in the thesis, the simulation studies outcomes are presented, where a comparison between the proposed control scheme and other control schemes in the literature is carried out through three case studies, and a comparison between the carrier-based PWM techniques on the key performance parameters of the SSMC is carried out. Finally, the experimental studies outcomes performed on a laboratory setup are presented, where first, the superiority of the proposed control method over counterpart methods in the literature is demonstrated, then, the effect of carrier-based PWM techniques on the performance profile of the SSMC is demonstrated.

7.1 Summary of Contributions

The following are the significant contributions of this thesis:

- A general overview of three-phase and single-phase AC-AC power electronics converters is provided. The advantages and disadvantages of the circuit topologies, along with the distinguishing features of MCs, are discussed.
- An overview of different four-quadrant bidirectional switches is presented. This includes the advantages, disadvantages, gate drive requirements, and losses of each switch.
- A new control method for SSMCs is proposed. The method provides several advantages over the existing methods in the literature, such as increasing the VTR and reducing the output voltage and source input current THD. More specifically, according to the experimental results, the proposed method offers around 10% increase in VTR, 34% reduction in output voltage THD, and 54% reduction in source input current THD.
- Proposing a new synchronization algorithm that synchronizes the gate-triggering pulses of the power switches with the grid. The algorithm is implemented on FPGA and proved its effectiveness in the synchronization regardless of the synthesized output frequency.
- Thanks to the proposed control scheme that accommodates any carrier-based PWM technique, analyzing and comparing the influence of different carrier-based PWM techniques on the performance profile of the SSMC is performed in this thesis. This allows for an in-depth understanding of the techniques and their ability to achieve high VTRs and ensure ZCS.

7.2 Future Expectations

Significant research efforts on new circuit topologies of single-phase AC-AC converters have been undertaken in recent years. These topologies aim to reduce the passive and active devices, losses, volume, and complexity and provide symmetric bipolar voltage gain with voltage buck-boost operations. Throughout this study, the following topics have been recognized to require further research attention:

- Comprehensive literature survey on the various single-phase AC-AC power electronics converters. This includes the features of each topology, such as its

ability to step-change the source frequency, produce symmetric bipolar voltage gain, operate in buck-boost modes, and continuity of its input and output currents. Further, the losses, volume, and reliability of each circuit topology should be considered.

- Single-phase induction motor drive using new SSMC circuit topologies and control schemes.
- Analyzing the existing closed-loop control methods used with SSMCs, such as PI controller-based source/load voltage/current control and peak voltage/current detection, and identifying their limitations and areas for improvement.
- Developing new closed-loop control strategies that address the shortcomings of existing methods and testing their robustness under dynamic operation conditions and for different applications.
- Filter design and optimization for SSMCs to obtain pure sinusoidal outputs with a wide range of output frequencies and modulation indexes.
- Developing a new isolated single-phase AC-AC converter with buck-boost inverting and non-inverting operations, continuous input and output currents, and reduced power device count.

REFERENCES

[1] J. Rodriguez, F. Blaabjerg, and M. P. Kazmierkowski, “Energy Transition Technology: The Role of Power Electronics,” *Proc. IEEE*, vol. 111, no. 4, pp. 329–334, Apr. 2023, doi: 10.1109/JPROC.2023.3257421.

[2] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, “Review of Three-Phase PWM AC–AC Converter Topologies,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, Nov. 2011, doi: 10.1109/TIE.2011.2159353.

[3] P. Venet, F. Perisse, M. H. El-Husseini, and G. Rojat, “Realization of a smart electrolytic capacitor circuit,” *IEEE Ind. Appl. Mag.*, vol. 8, no. 1, pp. 16–20, 2002, doi: 10.1109/2943.974353.

[4] P. Szcześniak, J. Kaniewski, and M. Jarnut, “AC–AC power electronic converters without DC energy storage: A review,” *Energy Convers. Manag.*, vol. 92, pp. 483–497, Mar. 2015, doi: 10.1016/j.enconman.2014.12.073.

[5] N. P. R. Iyer, *AC to AC Converters: Modelling, Simulation, and Real-Time Implementation Using SIMULINK®*. CRC Press, 2019.

[6] P. Szcześniak, *Three-phase AC-AC Power Converters Based on Matrix Converter Topology*. London: Springer London, 2013. doi: 10.1007/978-1-4471-4896-8.

[7] A. Carlsson, “The back-to-back converter,” *Lund Dep. Ind. Electr. Eng. Autom. Lund Inst. Technol.*, vol. 7, pp. 1002–1016, 1998.

[8] L. M. Tolbert, Fang Zheng Peng, and T. G. Habetler, “Multilevel converters for large electric drives,” *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, 1999, doi: 10.1109/28.740843.

[9] L. Malesani, L. Rossetto, P. Tenti, and P. Tomasin, “AC/DC/AC PWM converter with reduced energy storage in the DC link,” *IEEE Trans. Ind. Appl.*, vol. 31, no. 2, pp. 287–292, 1995, doi: 10.1109/28.370275.

[10] M. S. Smiai, S. E. Haque, N. H. Malik, and W. Shepherd, “Analysis and performance of hybrid thyristor-controlled three-phase resistive loads,” in

Conference Record of the IEEE Industry Applications Society Annual Meeting, 1989, pp. 1801–1807. doi: 10.1109/IAS.1989.96885.

[11] M. S. Smiai, S. Lesan, and W. Shepherd, "Analysis and performance of hybrid thyristor controlled three-phase resistive-inductive loads," in *Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting*, 1993, pp. 879–885. doi: 10.1109/IAS.1993.299002.

[12] A. Mozdzer and B. K. Bose, "Three-Phase AC Power Control Using Power Transistors," *IEEE Trans. Ind. Appl.*, vol. IA-12, no. 5, pp. 499–505, Sep. 1976, doi: 10.1109/TIA.1976.349460.

[13] B. R. Pelly, *Thyristor phase-controlled converters and cycloconverters: operation, control, and performance*. Wiley, 1971.

[14] L. Huber, N. Burány, and D. Borojević, "Analysis, design and implementation of the space-vector modulator for forced-commutated cycloconvertors," *IEE Proc. B (Electric Power Appl.*, vol. 139, no. 2, pp. 103–113, 1992, doi: 10.1049/ip-b.1992.0014.

[15] A. Ishiguro, T. Furuhashi, and S. Okuma, "A novel control method for forced commutated cycloconverters using instantaneous values of input line-to-line voltages," *IEEE Trans. Ind. Electron.*, vol. 38, no. 3, pp. 166–172, Jun. 1991, doi: 10.1109/41.87583.

[16] A. Alesina and M. Venturini, "Solid-state power conversion: A Fourier analysis approach to generalized transformer synthesis," *IEEE Trans. Circuits Syst.*, vol. 28, no. 4, pp. 319–330, Apr. 1981, doi: 10.1109/TCS.1981.1084993.

[17] A. Alesina and M. Venturini, "Intrinsic amplitude limits and optimum design of 9-switches direct PWM AC-AC converters," in *PESC '88 Record., 19th Annual IEEE Power Electronics Specialists Conference*, 1988, pp. 1284–1291. doi: 10.1109/PESC.1988.18273.

[18] A. Alesina and M. G. B. Venturini, "Analysis and design of optimum-amplitude nine-switch direct AC-AC converters," *IEEE Trans. Power Electron.*, vol. 4, no. 1, pp. 101–112, Jan. 1989, doi: 10.1109/63.21879.

[19] L. Huber and D. Borojevic, "Space vector modulated three-phase to three-phase matrix converter with input power factor correction," *IEEE Trans. Ind. Appl.*, vol. 31, no. 6, pp. 1234–1246, 1995, doi: 10.1109/28.475693.

[20] K. Iimori, K. Shinohara, O. Tarumi, Zixum Fu, and M. Muroya, “New current-controlled PWM rectifier-voltage source inverter without DC link components,” in *Proceedings of Power Conversion Conference - PCC ’97*, 1997, vol. 2, pp. 783–786. doi: 10.1109/PCCON.1997.638317.

[21] M. Jussila and H. Tuusa, “Comparison of Direct and Indirect Matrix Converters in Induction Motor Drive,” in *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*, Nov. 2006, pp. 1621–1626. doi: 10.1109/IECON.2006.347423.

[22] C. Klumpner, “A Hybrid Indirect Matrix Converter Immune to Unbalanced Voltage Supply, with Reduced Switching Losses and Improved Voltage Transfer Ratio,” in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC ’06.*, 2006, pp. 133–139. doi: 10.1109/APEC.2006.1620528.

[23] M. Baumann, F. Stogerer, and J. W. Kolar, “Part II: experimental analysis of the very sparse matrix converter,” in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, 2002, vol. 2, pp. 788–791. doi: 10.1109/APEC.2002.989334.

[24] F. Schafmeister, C. Rytz, and J. W. Kolar, “Analytical calculation of the conduction and switching losses of the conventional matrix converter and the (very) sparse matrix converter,” in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005.*, 2005, vol. 2, pp. 875–881. doi: 10.1109/APEC.2005.1453085.

[25] J. W. Kolar, F. Schafmeister, S. D. Round, and H. Ertl, “Novel Three-Phase AC–AC Sparse Matrix Converters,” *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1649–1661, Sep. 2007, doi: 10.1109/TPEL.2007.904178.

[26] M. Yuhendri, Ahyanuardi, and Aswardi, “Direct torque control strategy of PMSM employing ultra sparse matrix converter,” *Int. J. Power Electron. Drive Syst.*, vol. 9, no. 1, pp. 64–72, 2018, doi: 10.11591/ijpeds.v9n1.pp64-72.

[27] J. W. Kolar, M. Baumann, F. Schafmeister, and H. Ertl, “Novel three-phase AC-DC-AC sparse matrix converter,” in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, 2002, vol. 2, pp. 777–791. doi: 10.1109/APEC.2002.989333.

[28] R. W. Erickson and O. A. Al-Naseem, “A new family of matrix converters,” in *IECON’01. 27th Annual Conference of the IEEE Industrial Electronics Society (Cat. No.37243)*, 2001, vol. 2, pp. 1515–1520. doi: 10.1109/IECON.2001.976015.

[29] S. Angkititrakul and R. W. Erickson, “Control and implementation of a new modular matrix converter,” in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC ’04.*, 2004, vol. 2, pp. 813–819. doi: 10.1109/APEC.2004.1295916.

[30] I. S. de Freitas, C. B. Jacobina, and E. Cipriano dos Santos, “Single-Phase to Single-Phase Full-Bridge Converter Operating With Reduced AC Power in the DC-Link Capacitor,” *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 272–279, Feb. 2010, doi: 10.1109/TPEL.2009.2031225.

[31] B.-H. Kwon, B.-D. Min, and J.-H. Kim, “Novel topologies of AC choppers,” *IEE Proc. - Electr. Power Appl.*, vol. 143, no. 4, p. 323, 1996, doi: 10.1049/ip-epa:19960374.

[32] X. P. Fang, Z. M. Qian, and F. Z. Peng, “Single-phase Z-source PWM AC-AC converters,” *IEEE Power Electron. Lett.*, vol. 3, no. 4, pp. 121–124, Dec. 2005, doi: 10.1109/LPEL.2005.860453.

[33] E. Babaei, S. M. J. Mousavi, M. Alami, and D. Alizadeh, “A Review on Single-Phase AC-AC Z-Source Converters,” *AUT J. Electr. Eng.*, vol. 54, no. 1, pp. 137–162, 2022, doi: 10.22060/eej.2022.20936.5446.

[34] U. A. Khan, A. A. Khan, H. Cha, H.-G. Kim, J. Kim, and J.-W. Baek, “Dual-Buck AC–AC Converter With Inverting and Non-Inverting Operations,” *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9432–9443, Nov. 2018, doi: 10.1109/TPEL.2018.2799490.

[35] H. F. Ahmed and H. Cha, “A New Class of Single-Phase High-Frequency Isolated Z-Source AC–AC Converters With Reduced Passive Components,” *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1410–1419, Feb. 2018, doi: 10.1109/TPEL.2017.2686903.

[36] L. He, J. Nai, and J. Zhang, “Single-Phase Safe-Commutation Trans-Z-Source AC–AC Converter With Continuous Input Current,” *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5135–5145, Jun. 2018, doi:

10.1109/TIE.2017.2764876.

[37] H. F. Ahmed, M. S. El Moursi, B. Zahawi, and K. Al Hosani, “A High-Frequency Isolated Multilevel Cascaded-Type Bipolar Direct PWM AC–AC Converter for Utility Voltage Compensation,” *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 3188–3201, May 2021, doi: 10.1109/TIA.2020.3021371.

[38] H. F. Ahmed, H. Cha, A. A. Khan, J. Kim, and J. Cho, “A Single-Phase Buck–Boost Matrix Converter With Only Six Switches and Without Commutation Problem,” *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1232–1244, Feb. 2017, doi: 10.1109/TPEL.2016.2553044.

[39] H. F. Ahmed, M. S. El Moursi, H. Cha, K. Al Hosani, and B. Zahawi, “A Reliable Single-Phase Bipolar Buck–Boost Direct PWM AC–AC Converter With Continuous Input/Output Currents,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 12, pp. 10253–10265, 2019, doi: 10.1109/TIE.2019.2958290.

[40] C. Liu *et al.*, “Novel Bipolar-Type Direct AC–AC Converter Topology Based on Non-Differential AC Choppers,” *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9585–9599, Oct. 2019, doi: 10.1109/TPEL.2018.2890581.

[41] S. Sharifi, M. Monfared, M. Babaei, and A. Pourfaraj, “Highly Efficient Single-Phase Buck–Boost Variable-Frequency AC–AC Converter With Inherent Commutation Capability,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 5, pp. 3640–3649, 2020, doi: 10.1109/TIE.2019.2914644.

[42] F. Ahmed, M. ElMoursi, B. Zahawi, K. Al Hosani, and A. Khan, “Single-Phase Symmetric-Bipolar-Type High-Frequency Isolated Buck-Boost AC–AC Converter With Continuous Input and Output Currents,” *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11579–11592, Oct. 2021, doi: 10.1109/TPEL.2021.3073236.

[43] H. F. Ahmed, C. H. Chung, A. A. Khan, Z. Aleem, F. Akbar, and O. Alzaabi, “Nondifferential AC Choppers Based Identical Bipolar Buck–Boost AC–AC Converter Without Commutation Issue,” *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4988–4999, Apr. 2023, doi: 10.1109/TPEL.2022.3231367.

[44] H.-H. Shin, H. Cha, H.-G. Kim, and D.-W. Yoo, “Novel Single-Phase PWM AC–AC Converters Solving Commutation Problem Using Switching Cell Structure and Coupled Inductor,” *IEEE Trans. Power Electron.*, vol. 30, no. 4,

pp. 2137–2147, Apr. 2015, doi: 10.1109/TPEL.2014.2330351.

[45] H. F. Ahmed, H. Cha, A. A. Khan, and H.-G. Kim, “A Highly Reliable Single-Phase High-Frequency Isolated Double Step-Down AC–AC Converter With Both Noninverting and Inverting Operations,” *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 4878–4887, Nov. 2016, doi: 10.1109/TIA.2016.2592466.

[46] P. Li and Y. Hu, “Unified Non-Inverting and Inverting PWM AC–AC Converter With Versatile Modes of Operation,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 1137–1147, Feb. 2017, doi: 10.1109/TIE.2016.2615593.

[47] M.-K. Nguyen, Y.-G. Jung, and Y.-C. Lim, “Voltage swell/sag compensation with single-phase Z-source AC/AC converter,” in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–8.

[48] I. Abdoli, H. F. Ahmed, and A. Mosallanejad, “A high-frequency transformer-based buck-boost AC-AC converter with high efficiency and wide range conversion ratio for DVR application,” *IET Power Electron.*, Mar. 2023, doi: 10.1049/pel2.12487.

[49] M. K. Nguyen, Y. G. Jung, and Y. C. Lim, “Single-phase AC/AC buck-boost converter with single-phase matrix topology,” in *2009 13th European Conference on Power Electronics and Applications, EPE ’09*, 2009, pp. 1–7.

[50] A. Zuckerberger, D. Weinstock, and A. Alexandrovitz, “Single-phase matrix converter,” *IEE Proc. - Electr. Power Appl.*, vol. 144, no. 4, p. 235, 1997, doi: 10.1049/ip-epa:19970848.

[51] C.-M. Young, M.-H. Chen, S.-H. Yeh, and K.-H. Yuo, “A Single-Phase Single-Stage High Step-Up AC–DC Matrix Converter Based on Cockcroft–Walton Voltage Multiplier With PFC,” *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4894–4905, 2012, doi: 10.1109/TPEL.2012.2192450.

[52] M. K. Nguyen, Y. G. Jung, Y. C. Lim, and Y. M. Kim, “A Single-Phase Z-Source Buck–Boost Matrix Converter,” *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 453–462, Feb. 2010, doi: 10.1109/TPEL.2009.2028890.

[53] H. F. Ahmed, M. S. El Moursi, B. Zahawi, and K. Al Hosani, “High-Efficiency Single-Phase Matrix Converter With Diverse Symmetric Bipolar Buck and Boost Operations,” *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4300–4315, Apr. 2021, doi: 10.1109/TPEL.2020.3024785.

[54] H. F. Ahmed, H. Cha, and A. A. Khan, "A Single-Phase Buck Matrix Converter With High-Frequency Transformer Isolation and Reduced Switch Count," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 6979–6988, Sep. 2017, doi: 10.1109/TIE.2017.2686329.

[55] R. Baharom, A. S. A. Hasim, M. K. Hamzah, and M. F. Omar, "A New Single-Phase Controlled Rectifier Using Single-Phase Matrix Converter," in *2006 IEEE International Power and Energy Conference*, Nov. 2006, pp. 453–458. doi: 10.1109/PECON.2006.346694.

[56] R. Baharom, M. K. Hamzah, A. Saparon, S. Z. M. Noor, and N. R. Hamzah, "A New Single-Phase Controlled Rectifier using Single-Phase Matrix Converter with Regenerative Capabilities," in *2007 7th International Conference on Power Electronics and Drive Systems*, Nov. 2007, pp. 1477–1482. doi: 10.1109/PEDS.2007.4487899.

[57] R. Baharom, M. K. Hamzah, A. Saparon, and N. R. Hamzah, "Single-phase matrix converter operating as buck and boost rectifier," in *2009 4th IEEE Conference on Industrial Electronics and Applications*, May 2009, pp. 3338–3342. doi: 10.1109/ICIEA.2009.5138821.

[58] R. Baharom and M. K. Hamzah, "A New Single-Phase Controlled Rectifier Using Single-Phase Matrix Converter Topology Incorporating Active Power Filter," in *2007 IEEE International Electric Machines & Drives Conference*, May 2007, vol. 1, pp. 874–879. doi: 10.1109/IEMDC.2007.382784.

[59] K. S. Muhammad, R. Baharom, and M. K. Hamzah, "Advance battery charger topology using SPMC incorporating active power filter," in *2010 International Conference on Science and Social Research (CSSR 2010)*, 2010, pp. 548–553. doi: 10.1109/CSSR.2010.5773839.

[60] S. Zaliha, M. Noor, M. K. Hamzah, R. Baharom, and N. Y. Dahlan, "A New Single-Phase Inverter with Bidirectional Capabilities Using Single-Phase Matrix Converter," in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 464–470. doi: 10.1109/PESC.2007.4342032.

[61] M. K. Hamzah, S. Z. M. Noor, and S. F. A. Shukor, "A New Single-Phase Inverter using Single-Phase Matrix Converter Topology," in *2006 IEEE International Power and Energy Conference*, 2006, pp. 459–464. doi: 10.1109/PECON.2006.346695.

[62] J. Perez, V. Cardenas, L. Moran, and C. Nunez, “Single-Phase AC-AC Converter Operating as a Dynamic Voltage Restorer (DVR),” in *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*, 2006, pp. 1938–1943. doi: 10.1109/IECON.2006.347637.

[63] S. A. Rahman, S. B. Mule, E. D. Mitiku, G. T. Aduye, and C. Gopinath, “Highest Voltage Sag and Swell Compensation using Single Phase Matrix Converter with Four Controlled Switches,” *PRZEGLĄD ELEKTROTECHNICZNY*, vol. 1, no. 4, pp. 136–140, Mar. 2021, doi: 10.15199/48.2021.04.24.

[64] J. Kaniewski, P. Szczesniak, M. Jarnut, and G. Benysek, “Hybrid Voltage Sag/Swell Compensators: A Review of Hybrid AC/AC Converters,” *IEEE Ind. Electron. Mag.*, vol. 9, no. 4, pp. 37–48, Dec. 2015, doi: 10.1109/MIE.2015.2404350.

[65] P. Drabek, Z. Peroutka, M. Pittermann, and M. Cedl, “New Configuration of Traction Converter With Medium-Frequency Transformer Using Matrix Converters,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5041–5048, Nov. 2011, doi: 10.1109/TIE.2011.2138114.

[66] B. Bednar, P. Drabek, and M. Pittermann, “Algorithm implementation of traction converter topology based on MFT and single phase matrix converter,” *Electr. Eng.*, vol. 99, no. 4, pp. 1305–1315, Dec. 2017, doi: 10.1007/s00202-017-0607-2.

[67] N. Nguyen-Quang, D. A. Stone, C. M. Bingham, and M. P. Foster, “Single phase matrix converter for radio frequency induction heating,” in *International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2006. SPEEDAM 2006*, 2006, pp. 614–618. doi: 10.1109/SPEEDAM.2006.1649844.

[68] A. Kumar, P. Kumar Sadhu, D. Kumar Mohanta, and M. Bharata Reddy, “An Effective Switching Algorithm for Single Phase Matrix Converter in Induction Heating Applications,” *Electronics*, vol. 7, no. 8, p. 149, Aug. 2018, doi: 10.3390/electronics7080149.

[69] S. Sünter and Ö. Aydoğmuş, “Implementation of a single-phase matrix converter induction motor drive,” *Electr. Eng.*, vol. 90, no. 6, pp. 425–433, Jun. 2008, doi: 10.1007/s00202-007-0093-z.

[70] M. Boydak, A. Orhan, and A. Caliskan, “Speed Control of DC Motor Under Load Condition Using Single Phase Matrix Converter,” in *2020 2nd Global Power, Energy and Communication Conference (GPECOM)*, Oct. 2020, pp. 76–80. doi: 10.1109/GPECOM49333.2020.9247897.

[71] N. Takaoka, H. Takahashi, and J. Itoh, “Isolated Single-Phase Matrix Converter Using Center-Tapped Transformer for Power Decoupling Capability,” *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1523–1531, Mar. 2018, doi: 10.1109/TIA.2017.2774760.

[72] P. Nayak, K. Rajashekara, and S. K. Pramanick, “Soft-Switched Modulation Technique for a Single-Stage Matrix-Type Isolated DC–AC Converter,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7642–7656, Nov. 2019, doi: 10.1109/TIA.2018.2889977.

[73] N. Kummari, S. Chakraborty, and S. Chattopadhyay, “An Isolated High-Frequency Link Microinverter Operated with Secondary-Side Modulation for Efficiency Improvement,” *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2187–2200, Mar. 2018, doi: 10.1109/TPEL.2017.2699945.

[74] S. Norrga, “Experimental Study of a Soft-Switched Isolated Bidirectional AC–DC Converter Without Auxiliary Circuit,” *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1580–1587, Nov. 2006, doi: 10.1109/TPEL.2006.882969.

[75] M. Wang, Q. Huang, S. Guo, X. Yu, W. Yu, and A. Q. Huang, “Soft-Switched Modulation Techniques for an Isolated Bidirectional DC–AC,” *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 137–150, Jan. 2018, doi: 10.1109/TPEL.2017.2661965.

[76] D. Varajão, R. E. Araújo, L. M. Miranda, J. P. Lopes, and N. D. Weise, “Control of an isolated single-phase bidirectional AC-DC matrix converter for V2G applications,” *Electr. Power Syst. Res.*, vol. 149, pp. 19–29, Aug. 2017, doi: 10.1016/j.epsr.2017.04.004.

[77] D. Barater, G. Buticchi, C. Concari, L. Concari, and G. Franceschini, “Single-phase matrix converter for active power filter applications,” in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Nov. 2013, pp. 8528–8533. doi: 10.1109/IECON.2013.6700564.

[78] L. V Venugopal and R. Jayapal, “Matrix converter based energy saving for

street lights," in *2015 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2015]*, Mar. 2015, pp. 1–6. doi: 10.1109/ICCPCT.2015.7159258.

[79] K. M. Raja, K. Vijayakumar, and S. Kannan, "Matrix converter based solar photo voltaic system for reactive power compensation using sinusoidal pulse width modulation," in *2014 IEEE International Conference on Computational Intelligence and Computing Research*, Dec. 2014, pp. 1–5. doi: 10.1109/ICCIC.2014.7238524.

[80] T. Sigamani, R. P. Ponraj, and V. Ravindran, "Modified Single Phase Matrix Converter with Z-Source for Renewable Energy Systems," in *2020 Third International Conference on Smart Systems and Inventive Technology (ICSSIT)*, Aug. 2020, pp. 601–607. doi: 10.1109/ICSSIT48917.2020.9214138.

[81] Z. Idris, M. K. Hamzah, and M. F. Saidon, "Implementation of Single-Phase Matrix Converter as a direct AC-AC converter with commutation strategies," in *2006 37th IEEE Power Electronics Specialists Conference*, Jun. 2006, pp. 1–7. doi: 10.1109/pesc.2006.1712106.

[82] C.-M. Young, H.-L. Chen, and M.-H. Chen, "A Cockcroft–Walton Voltage Multiplier Fed by a Three-Phase-to-Single-Phase Matrix Converter With PFC," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1994–2004, May 2014, doi: 10.1109/TIA.2013.2287479.

[83] T. N. Mir, B. Singh, and A. H. Bhat, "Predictive Delta Sigma Modulation for Three-Phase to Three-Phase Matrix Converters," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 968–976, Jan. 2020, doi: 10.1109/TPEL.2019.2910586.

[84] L. Huber, D. Borojevic, X. F. Zhuang, and F. C. Lee, "Design and implementation of a three-phase to three-phase matrix converter with input power factor correction," in *Proceedings Eighth Annual Applied Power Electronics Conference and Exposition,* 1993, pp. 860–865. doi: 10.1109/APEC.1993.290683.

[85] A. M. Bozorgi, M. Monfared, and H. Rajabi Mashhadi, "Two simple overmodulation algorithms for space vector modulated three-phase to three-phase matrix converter," *IET Power Electron.*, vol. 7, no. 7, pp. 1915–1924, Jul. 2014, doi: 10.1049/iet-pel.2013.0740.

[86] L. Helle, K. B. Larsen, A. H. Jorgensen, S. Munk-Nielsen, and F. Blaabjerg, "Evaluation of Modulation Schemes for Three-Phase to Three-Phase Matrix Converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 1, pp. 158–171, Feb. 2004, doi: 10.1109/TIE.2003.821900.

[87] M. Rivera, S. Rojas, C. Restrepo, J. Muñoz, C. Baier, and P. Wheeler, "Control Techniques for a Single-Phase Matrix Converter," *Energies*, vol. 13, no. 23, p. 6337, Dec. 2020, doi: 10.3390/en13236337.

[88] L. Guan, Z. Wang, P. Liu, and J. Wu, "A Three-Phase to Single-Phase Matrix Converter for Bidirectional Wireless Power Transfer System," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2019, pp. 4451–4456. doi: 10.1109/IECON.2019.8927585.

[89] N. Nguyen-Quang, D. A. Stone, C. M. Bingham, and M. P. Foster, "A three-phase to single-phase matrix converter for high-frequency induction heating," in *2009 13th European Conference on Power Electronics and Applications, EPE '09*, 2009, pp. 1–10.

[90] S. M. Ahmed, H. Abu-Rub, Z. Salam, and A. Iqbal, "Space vector PWM technique for a direct five-to-three-phase matrix converter," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Nov. 2013, vol. 48, no. 2, pp. 4943–4948. doi: 10.1109/IECON.2013.6699935.

[91] S. M. Ahmed, H. Abu-Rub, and Z. Salam, "Model Predictive Control of a Direct Three-to-Seven Phase Matrix Converter," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2014, pp. 1059–1063. doi: 10.1109/ECCE.2014.6953516.

[92] S. M. Ahmed, Z. Salam, and H. Abu-Rub, "An Improved Space Vector Modulation for a Three-to-Seven-Phase Matrix Converter With Reduced Number of Switching Vectors," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 1–1, 2014, doi: 10.1109/TIE.2014.2381158.

[93] Y. Kudoh *et al.*, "Single to two-phase matrix converter using GaN-based monolithic bidirectional switch for driving symmetrical two-phase motor," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2014, pp. 3186–3191. doi: 10.1109/ECCE.2014.6953833.

[94] Z. Malekjamshidi, M. Jafari, J. Zhang, and J. Zhu, "Design and analysis of

protection circuits for safe operation of direct matrix converters," in *2017 20th International Conference on Electrical Machines and Systems (ICEMS)*, Aug. 2017, pp. 1–4. doi: 10.1109/ICEMS.2017.8056429.

[95] S. Safari, A. Castellazzi, and P. Wheeler, "Experimental and Analytical Performance Evaluation of SiC Power Devices in the Matrix Converter," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2584–2596, May 2014, doi: 10.1109/TPEL.2013.2289746.

[96] A. Deihimi and F. Khoshnevis, "Implementaion of Current Commutation Strategies of Matrix Converters in FPGA and Simulations Using Max + PlusII," *Int. J. Recent Trends Eng.*, vol. 2, no. 5, pp. 91–95, 2009.

[97] A. Yousefi-Talouki, G. Pellegrino, M. Mengoni, and L. Zarri, "Self-commissioning algorithm for matrix converter, nonlinearity compensation," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2015, pp. 4077–4083. doi: 10.1109/ECCE.2015.7310235.

[98] L. Empringham, J. W. Kolar, J. Rodriguez, P. W. Wheeler, and J. C. Clare, "Technological Issues and Industrial Application of Matrix Converters: A Review," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4260–4271, Oct. 2013, doi: 10.1109/TIE.2012.2216231.

[99] C. L. Neft and C. D. Schauder, "Theory and design of a 30-hp matrix converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 3, pp. 546–551, 1992, doi: 10.1109/28.137434.

[100] K. You, D. Xiao, M. F. Rahman, and M. N. Uddin, "Applying Reduced General Direct Space Vector Modulation Approach of AC–AC Matrix Converter Theory to Achieve Direct Power Factor Controlled Three-Phase AC–DC Matrix Rectifier," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 2243–2257, May 2014, doi: 10.1109/TIA.2013.2285956.

[101] A. Trentin, L. Empringham, L. de Lillo, P. Zanchetta, P. Wheeler, and J. Clare, "Experimental Efficiency Comparison Between a Direct Matrix Converter and an Indirect Matrix Converter Using Both Si IGBTs and SiC mosfets," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4135–4145, Sep. 2016, doi: 10.1109/TIA.2016.2573752.

[102] P. Resutík and S. Kaščák, "Compact 3 × 1 Matrix Converter Module Based on

the SiC Devices with Easy Expandability," *Appl. Sci.*, vol. 11, no. 20, p. 9366, Oct. 2021, doi: 10.3390/app11209366.

[103] K. G. Kerris, "Implementation of a matrix converter using p-channel MOS-controlled thyristors," in *8th International Conference on Power Electronics and Variable Speed Drives*, 2000, pp. 35–39. doi: 10.1049/cp:20000216.

[104] P. W. Wheeler, J. C. Clare, and L. Empringham, "A vector controlled MCT matrix converter induction motor drive with minimized commutation times and enhanced waveform quality," in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, 2002, vol. 1, pp. 466–472. doi: 10.1109/IAS.2002.1044127.

[105] J. Szczepanik and T. Sienko, "New Control Strategy for Multiphase Matrix Converter," in *2008 19th International Conference on Systems Engineering*, Aug. 2008, pp. 121–126. doi: 10.1109/ICSEng.2008.44.

[106] N. Burany, "Safe control of four-quadrant switches," in *Conference Record of the IEEE Industry Applications Society Annual Meeting*, 1989, pp. 1190–1194. doi: 10.1109/IAS.1989.96794.

[107] S. Bernet, T. Matsuo, and T. A. Lipo, "A matrix converter using reverse blocking NPT-IGBTs and optimized pulse patterns," in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, 1996, vol. 1, pp. 107–113. doi: 10.1109/PESC.1996.548567.

[108] L. Rmili, S. Rahmani, H. Vahedi, and K. Al-Haddad, "A comprehensive analysis of Matrix Converters: Bidirectional switch, direct topology, modeling and control," in *2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE)*, Jun. 2014, pp. 313–318. doi: 10.1109/ISIE.2014.6864631.

[109] C. Klumpner and F. Blaabjerg, "Using reverse-blocking IGBTs in power converters for adjustable-speed drives," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 807–816, May 2006, doi: 10.1109/TIA.2006.872956.

[110] K. Shimoyama, M. Takei, Y. Souma, A. Yajima, S. Kajiwara, and H. Nakazawa, "A New Isolation Technique for Reverse Blocking IGBT with Ion Implantation and Laser Annealing to Tapered Chip Edge Sidewalls," in *2006 IEEE International Symposium on Power Semiconductor Devices & IC's*, 2006, pp. 1–4. doi: 10.1109/ISPSD.2006.1666063.

[111] D. Domes, W. Hofmann, and J. Lutz, “A first loss evaluation using a vertical SiC-JFET and a conventional Si-IGBT in the bidirectional matrix converter switch topology,” in *2005 European Conference on Power Electronics and Applications*, 2005, pp. 10 pp.-P.10. doi: 10.1109/EPE.2005.219281.

[112] D. Domes and W. Hofmann, “SiC JFET in Contrast to High Speed Si IGBT in Matrix Converter Topology,” in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 54–60. doi: 10.1109/PESC.2007.4341961.

[113] “DIM400PBM17-A000 IGBT Bi-Directional Switch Module,” *Dynex Semiconductor*, 2010. https://www.dynexsemi.com/Portals/0/assets/downloads/DNX_DIM400PBM17-A000.pdf

[114] K. Sun, D. Zhou, L. Huang, K. Matsuse, and K. Sasagawa, “A Novel Commutation Method of Matrix Converter Fed Induction Motor Drive Using RB-IGBT,” *IEEE Trans. Ind. Appl.*, vol. 43, no. 3, pp. 777–786, 2007, doi: 10.1109/TIA.2007.895769.

[115] D. Zhou, K. Sun, Z. Liu, L. Huang, K. Matsuse, and K. Sasagawa, “A Novel Driving and Protection Circuit for Reverse-Blocking IGBT Used in Matrix Converter,” *IEEE Trans. Ind. Appl.*, vol. 43, no. 1, pp. 3–13, 2007, doi: 10.1109/TIA.2006.886422.

[116] P. Gamboa, S. F. Pinto, J. F. Silva, and E. Margato, “A flywheel energy storage system with Matrix Converter controlled Permanent Magnet Synchronous Motor,” in *2008 18th International Conference on Electrical Machines*, Sep. 2008, pp. 1–5. doi: 10.1109/ICELMACH.2008.4799861.

[117] M. Hornkamp, M. Loddenkötter, M. Münzer, O. Simon, and M. Bruckmann, “EconoMAC the first all-in-one IGBT module for matrix converters,” in *Proc. PCIM*, 2001, pp. 1–6.

[118] E. R. Motto, J. F. Donlon, M. Tabata, H. Takahashi, Y. Yu, and G. Majumdar, “Application characteristics of an experimental RB-IGBT (reverse blocking IGBT) module,” in *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, 2004, vol. 3, pp. 1540–1544. doi: 10.1109/IAS.2004.1348675.

[119] A. Ecklebe, A. Lindemann, and S. Schulz, “Bidirectional Switch Commutation

for a Matrix Converter Supplying a Series Resonant Load," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1173–1181, May 2009, doi: 10.1109/TPEL.2008.2011737.

[120] H. She, H. Lin, B. He, X. Wang, L. Yue, and X. An, "Implementation of Voltage-Based Commutation in Space-Vector-Modulated Matrix Converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 154–166, Jan. 2012, doi: 10.1109/TIE.2011.2130497.

[121] P. W. Wheeler, J. C. Clare, L. Empringharn, M. Bland, and M. Apap, "Gate drive level intelligence and current sensing for matrix converter current commutation," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 382–389, Apr. 2002, doi: 10.1109/41.993271.

[122] Jang-Hyoun Youm and Bong-Hwan Kwon, "Switching technique for current-controlled AC-to-AC converters," *IEEE Trans. Ind. Electron.*, vol. 46, no. 2, pp. 309–318, Apr. 1999, doi: 10.1109/41.753769.

[123] B.-H. Kwon, B.-D. Min, and J.-H. Kim, "Novel commutation technique of AC–AC converters," *IEE Proc. - Electr. Power Appl.*, vol. 145, no. 4, p. 295, 1998, doi: 10.1049/ip-epa:19981869.

[124] G. Boztas, S. Sünter, and O. Aydogmus, "Design of a novel single-phase in two-phase out matrix converter driving an induction motor," *IET Power Electron.*, vol. 9, no. 7, pp. 1391–1397, Jun. 2016, doi: 10.1049/iet-pel.2015.0568.

[125] W. Deng and S. Li, "Direct Torque Control of Matrix Converter-Fed PMSM Drives Using Multidimensional Switching Table for Common-Mode Voltage Minimization," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 683–690, Jan. 2021, doi: 10.1109/TPEL.2020.2998686.

[126] T. N. Mir, B. Singh, and A. H. Bhat, "FS-MPC-Based Speed Sensorless Control of Matrix Converter Fed Induction Motor Drive With Zero Common Mode Voltage," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9185–9195, Oct. 2021, doi: 10.1109/TIE.2020.3020031.

[127] Z. Idris, S. Z. Mohammad Noor, and M. K. Hamzah, "Safe Commutation Strategy in Single Phase Matrix Converter," in *2005 International Conference on Power Electronics and Drives Systems*, 2005, vol. 2, pp. 886–891. doi: 10.1109/PEDS.2005.1619813.

[128] M. K. Hamzah, Z. Idris, A. Saparon, and M. . Yunos, “FPGA design of single-phase matrix converter operating as a frequency changer,” in *2008 IEEE 2nd International Power and Energy Conference*, Dec. 2008, pp. 1124–1129. doi: 10.1109/PECON.2008.4762644.

[129] J. Andreu, I. Kortabarria, E. Ormaetxea, E. Ibarra, J. L. Martin, and S. Apinaniz, “A Step Forward Towards the Development of Reliable Matrix Converters,” *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 167–183, Jan. 2012, doi: 10.1109/TIE.2011.2146217.

[130] J. Mahlein, M. Bruckmann, and M. Braun, “Passive protection strategy for a drive system with a matrix converter and an induction machine,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 297–303, Apr. 2002, doi: 10.1109/41.993262.

[131] J. Mahlein and M. Braun, “A matrix converter without diode clamped over-voltage protection,” in *Proceedings IPEMC 2000. Third International Power Electronics and Motion Control Conference (IEEE Cat. No.00EX435)*, 2000, vol. 2, pp. 817–822. doi: 10.1109/IPEMC.2000.884609.

[132] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and A. Weinstein, “Matrix converters: a technology review,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 276–288, Apr. 2002, doi: 10.1109/41.993260.

[133] E. Ibarra *et al.*, “New fault tolerant matrix converter,” *Electr. Power Syst. Res.*, vol. 81, no. 2, pp. 538–552, Feb. 2011, doi: 10.1016/j.epsr.2010.10.028.

[134] C. Klumpner and F. Blaabjerg, “Short Term Braking Capability During Power Interruptions for Integrated Matrix Converter—Motor Drives,” *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 303–311, Mar. 2004, doi: 10.1109/TPEL.2003.823175.

[135] J. Rodriguez, M. Rivera, J. W. Kolar, and P. W. Wheeler, “A Review of Control and Modulation Methods for Matrix Converters,” *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 58–70, Jan. 2012, doi: 10.1109/TIE.2011.2165310.

[136] D. Varajão and R. E. Araújo, “Modulation Methods for Direct and Indirect Matrix Converters: A Review,” *Electronics*, vol. 10, no. 7, p. 812, Mar. 2021, doi: 10.3390/electronics10070812.

[137] Y.-D. Yoon and S.-K. Sul, “Carrier-Based Modulation Technique for Matrix Converter,” *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1691–1703, Nov.

2006, doi: 10.1109/TPEL.2006.882935.

[138] P. C. Loh, R. Rong, F. Blaabjerg, and P. Wang, “Digital Carrier Modulation and Sampling Issues of Matrix Converters,” *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1690–1700, Jul. 2009, doi: 10.1109/TPEL.2009.2016423.

[139] S. Thuta, K. K. Mohapatra, and N. Mohan, “Matrix converter over-modulation using carrier-based control: Maximizing the voltage transfer ratio,” in *2008 IEEE Power Electronics Specialists Conference*, Jun. 2008, pp. 1727–1733. doi: 10.1109/PESC.2008.4592192.

[140] L. Huber and D. Borojevic, “Space vector modulator for forced commutated cycloconverters,” in *Conference Record of the IEEE Industry Applications Society Annual Meeting*, 1989, pp. 871–876. doi: 10.1109/IAS.1989.96746.

[141] F. Blaabjerg, D. Casadei, C. Klumpner, and M. Matteini, “Comparison of two current modulation strategies for matrix converters under unbalanced input voltage conditions,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 289–296, Apr. 2002, doi: 10.1109/41.993261.

[142] O. Simon, J. Mahlein, M. N. Muenzer, and M. Bruckmarm, “Modern solutions for industrial matrix-converter applications,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 401–406, Apr. 2002, doi: 10.1109/41.993273.

[143] D. Casadei, G. Serra, A. Tani, and L. Zarri, “Matrix converter modulation strategies: a new general approach based on space-vector representation of the switch state,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 370–381, 2002, doi: 10.1109/41.993270.

[144] M. Venturini and A. Alesina, “The generalised transformer: A new bidirectional, sinusoidal waveform frequency converter with continuously adjustable input power factor,” in *1980 IEEE Power Electronics Specialists Conference*, Jun. 1980, pp. 242–252. doi: 10.1109/PESC.1980.7089455.

[145] L. Zhang, C. Watthanasarn, and W. Shepherd, “Control of AC-AC matrix converters for unbalanced and/or distorted supply voltage,” in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, 2001, vol. 2, pp. 1108–1113. doi: 10.1109/PESC.2001.954267.

[146] S. Lopez Arevalo, P. Zanchetta, P. W. Wheeler, A. Trentin, and L. Empringham, “Control and Implementation of a Matrix-Converter-Based AC

Ground Power-Supply Unit for Aircraft Servicing," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2076–2084, Jun. 2010, doi: 10.1109/TIE.2009.2034180.

[147] J. Rodríguez, E. Silva, F. Blaabjerg, P. Wheeler, J. Clare, and J. Pontt, "Matrix converter controlled with the direct transfer function approach: analysis, modelling and simulation," *Int. J. Electron.*, vol. 92, no. 2, pp. 63–85, Feb. 2005, doi: 10.1080/00207210512331337686.

[148] G. Roy and G.-E. April, "Cycloconverter operation under a new scalar control algorithm," in *20th Annual IEEE Power Electronics Specialists Conference*, 1989, pp. 368–375. doi: 10.1109/PESC.1989.48511.

[149] S. Muller, U. Ammann, and S. Rees, "New time-discrete modulation scheme for matrix converters," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1607–1615, 2005, doi: 10.1109/TIE.2005.858713.

[150] R. Vargas, U. Ammann, and J. Rodriguez, "Predictive Approach to Increase Efficiency and Reduce Switching Losses on Matrix Converters," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 894–902, Apr. 2009, doi: 10.1109/TPEL.2008.2011907.

[151] R. Vargas, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive Strategy to Control Common-Mode Voltage in Loads Fed by Matrix Converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4372–4380, Dec. 2008, doi: 10.1109/TIE.2008.2007016.

[152] R. Vargas, J. Rodriguez, U. Ammann, and P. W. Wheeler, "Predictive Current Control of an Induction Machine Fed by a Matrix Converter With Reactive Power Control," *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4362–4371, Dec. 2008, doi: 10.1109/TIE.2008.2006947.

[153] J. Rodriguez *et al.*, "Predictive direct torque control of an induction motor fed by a matrix converter," in *2007 European Conference on Power Electronics and Applications*, 2007, pp. 1–10. doi: 10.1109/EPE.2007.4417295.

[154] J. Rodriguez, J. Kolar, J. Espinoza, M. Rivera, and C. Rojas, "Predictive torque and flux control of an induction machine fed by an indirect matrix converter with reactive power minimization," in *2010 IEEE International Symposium on Industrial Electronics*, Jul. 2010, pp. 3177–3183. doi: 10.1109/ISIE.2010.5637561.

[155] R. Vargas, U. Ammann, B. Hudoffsky, J. Rodriguez, and P. Wheeler, "Predictive Torque Control of an Induction Machine Fed by a Matrix Converter With Reactive Input Power Control," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1426–1438, 2010, doi: 10.1109/TPEL.2010.2040839.

[156] S. Pinto and J. Silva, "Sliding mode direct control of matrix converters," *IET Electr. Power Appl.*, vol. 1, no. 3, pp. 439–448, 2007, doi: 10.1049/iet-epa:20060257.

[157] A. Sivaprakasam and J. D. Anunciya, "A Survey on Matrix Converter fed Direct Torque Control Techniques for AC Machines," *IETE J. Res.*, vol. 68, no. 1, pp. 42–58, Jan. 2022, doi: 10.1080/03772063.2019.1583082.

[158] I. Takahashi and T. Noguchi, "A New Quick-Response and High-Efficiency Control Strategy of an Induction Motor," *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 5, pp. 820–827, Sep. 1986, doi: 10.1109/TIA.1986.4504799.

[159] D. Casadei, G. Serra, and A. Tani, "The use of matrix converters in direct torque control of induction machines," *IEEE Trans. Ind. Electron.*, vol. 48, no. 6, pp. 1057–1064, 2001, doi: 10.1109/41.969384.

[160] C. Ortega, A. Arias, C. Caruana, J. Balcells, and G. M. Asher, "Improved Waveform Quality in the Direct Torque Control of Matrix-Converter-Fed PMSM Drives," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2101–2110, Jun. 2010, doi: 10.1109/TIE.2009.2033084.

[161] M. F. Mohd Zin, M. N. Seroji, and N. Hamzah, "Design of closed-loop current control for high power factor AC-AC SPMC," in *2012 IEEE International Conference on Power and Energy (PECon)*, Dec. 2012, pp. 536–541. doi: 10.1109/PECon.2012.6450272.

[162] M. F. M. Zin, N. Hamzah, and M. N. Seroji, "Voltage controlled SPMC with unity voltage conversion ratio and low total harmonic distortion," in *2014 2nd International Conference on Electrical, Electronics and System Engineering (ICEESE)*, Dec. 2014, pp. 140–145. doi: 10.1109/ICEESE.2014.7154595.

[163] H. Y. Chu, H. L. Jou, and C. L. Huang, "Transient response of a peak voltage detector for sinusoidal signals," *IEEE Trans. Ind. Electron.*, vol. 39, no. 1, pp. 74–79, 1992, doi: 10.1109/41.121914.

[164] B.-H. Kwon, G.-Y. Jeong, S.-H. Han, and D.-H. Lee, "Novel line conditioner

with voltage up/down capability," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1110–1119, Oct. 2002, doi: 10.1109/TIE.2002.803236.

[165] O. Al-Dori and A. M. Vural, "A novel control method for enhanced performance of single-phase matrix converters," *Int. J. Circuit Theory Appl.*, pp. 1–26, Aug. 2023, doi: 10.1002/cta.3752.

[166] Z. Idris, M. K. Hamzah, and A. M. Omar, "Implementation of Single-Phase Matrix Converter as a Direct AC-AC Converter Synthesized Using Sinusoidal Pulse Width Modulation with Passive Load Condition," in *2005 International Conference on Power Electronics and Drives Systems*, 2005, vol. 2, pp. 1536–1541. doi: 10.1109/PEDS.2005.1619932.

[167] J. Burhanudin *et al.*, "Simulation of AC/AC Converter using Single Phase Matrix Converter for Wave Energy Converter," in *2022 IEEE International Conference in Power Engineering Application (ICPEA)*, Mar. 2022, pp. 1–6. doi: 10.1109/ICPEA53519.2022.9744651.

[168] S. K. Rasappan and V. Chenniappan, "A Novel Switching Strategy for Realization of Single Phase Matrix Converter As a Universal Power Electronic Converter," *J. Electr. Eng.*, vol. 18, no. 3, p. 9, 2018.

[169] K. T. Maheswari, R. Bharanikumar, and D. Lavanya, "Modeling and analysis of single phase quasi Z source matrix converter fed induction motor drives," *Mater. Today Proc.*, vol. 45, pp. 1717–1721, 2021, doi: 10.1016/j.matpr.2020.08.616.

[170] K. Vijayakumar, R. S. Raj, and S. Kannan, "Application of Sinusoidal Pulse Width Modulation Based Matrix Converter as Revolutionized Power Electronic Converter," in *Lecture Notes in Electrical Engineering*, vol. 326, IEEE, 2015, pp. 9–17. doi: 10.1007/978-81-322-2119-7_2.

[171] A. Anand kumar and P. R. Thakura, "Hardware development and implementation of single phase matrix converter as a cycloconverter and as an inverter," in *2014 IEEE 6th India International Conference on Power Electronics (IICPE)*, Dec. 2014, pp. 1–6. doi: 10.1109/IICPE.2014.7115835.

[172] A. Biswas, J. L. Jaiswal, and V. Agarwal, "A study of staircase modulation technique for single phase matrix converter," in *2012 2nd International Conference on Power, Control and Embedded Systems*, Dec. 2012, pp. 1–6. doi:

10.1109/ICPCES.2012.6508096.

[173] A. Agarwal and V. Agarwal, “Staircase modulated AC to AC converter,” in *2010 International Conference on Power, Control and Embedded Systems*, Nov. 2010, pp. 1–5. doi: 10.1109/ICPCES.2010.5698660.

[174] A. Agarwal and V. Agarwal, “FPGA Realization of Trapezoidal PWM for Generalized Frequency Converter,” *IEEE Trans. Ind. Informatics*, vol. 8, no. 3, pp. 501–510, Aug. 2012, doi: 10.1109/TII.2012.2193406.

[175] A. Agarwal and V. Agarwal, “Harmonic reduction in AC to AC converter by trapezoidal modulation technique,” in *2009 International Conference on Power Systems*, 2009, pp. 1–6. doi: 10.1109/ICPWS.2009.5442659.

[176] I. Ahmad Khan, A. Flah, A. Agarwal, and H. Kumar, “Trapezoidal Modulated Direct Matrix Converter: For Higher Frequency AC/AC Conversion,” *Indian J. Pure Appl. Phys.*, vol. 59, no. 3, pp. 211–215, 2021, doi: 10.56042/ijpap.v59i3.67754.

[177] M. Kurtoğlu and A. M. Vural, “A Novel Nearest Level Modulation Method with Increased Output Voltage Quality for Modular Multilevel Converter Topology,” *Int. Trans. Electr. Energy Syst.*, vol. 2022, pp. 1–17, Jan. 2022, doi: 10.1155/2022/2169357.

[178] V. Agarwal and S. Gupta, “An efficient algorithm for generalised single-phase converter,” *IET Power Electron.*, vol. 3, no. 1, p. 138, 2010, doi: 10.1049/iet-pel.2008.0316.

[179] A. K. Gola and V. Agarwal, “Implementation of an efficient algorithm for a single phase matrix converter,” *J. Power Electron.*, vol. 9, no. 2, pp. 198–206, 2009.

[180] A. Agarwal and V. Agarwal, “FPGA based variable frequency AC to AC power conversion,” *Electr. Power Syst. Res.*, vol. 90, pp. 67–78, Sep. 2012, doi: 10.1016/j.epsr.2012.04.003.

[181] Infineon, “IHW20N135R5,” 2019. https://www.infineon.com/dgdl/Infineon-IHW20N135R5-DataSheet-v02_02-EN.pdf?fileId=db3a304343bec32d0143d3809a56321c (accessed May 25, 2023).

[182] Texas Instruments Incorporated, “Industry-Standard Dual Operational

Amplifiers," 2022. https://www.ti.com/lit/ds/symlink/lm358.pdf (accessed May 25, 2023).

[183] Toshiba Electronic Devices & Storage Corporation, "TLP250," 2019. https://toshiba.semicon-storage.com/info/datasheet_en_20190617.pdf?did=16821 (accessed May 25, 2023).

[184] Digilent, "Basys 3™ FPGA Board Reference Manual," 2019. https://digilent.com/reference/_media/reference/programmable-logic/basys-3/basys3_rm.pdf (accessed May 25, 2023).

[185] STMicroelectronics, "Transil™, transient voltage surge suppressor (TVS)," 2012. https://cdn.ozdisan.com/ETicaret_Dosya/406199_5497037.pdf (accessed May 25, 2023).

[186] Atmel, "ATmega328P." https://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-7810-Automotive-Microcontrollers-ATmega328P_Datasheet.pdf (accessed May 25, 2023).

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PUBLICATIONS

Journal Papers (SCI/SCIE):

1. **O. Al-Dori** and A. M. Vural, "A novel control method for enhanced performance of single-phase matrix converters," *International Journal of Circuit Theory and Applications*, pp. 1–26, 2023, doi: 10.1002/cta.3752.
2. **O. Al-Dori** and A. Dönük, "Short-Circuit Performance Analysis of a Distribution Transformer Using Coupled Field-Circuit Approach," *Electric Power Components and Systems*, pp. 1-12, 2023, doi: 10.1080/15325008.2023.2228787.
3. **O. Al-Dori**, B. Şakar, and A. Dönük, "Optimal Design and Performance Analysis of Three-phase Distribution Transformer with Variable Loading," *Electric Power Components and Systems*, vol. 50, no. 9–10, pp. 458–468, 2022, doi: 10.1080/15325008.2022.2136301.
4. **O. Al-Dori**, B. Şakar, and A. Dönük, "Comprehensive Analysis of Losses and Leakage Reactance of Distribution Transformers," *Arabian Journal for Science and Engineering*, vol. 47, no. 11, pp. 14163–14171, 2022, doi: 10.1007/s13369-022-06680-1.

Journal Papers (Other Indexes):

1. A. Dönük and **O. Al-Dori**, "Performance and Harmonic Analysis of a Three-Phase Induction Motor with Various Coil Pitch Configurations," *Yuzuncu Yil University Journal of the Institute of Natural and Applied Sciences*, vol. 28, no. 1, pp. 38–47, 2023, doi: 10.53433/yyufbed.1105237.

Conference Proceedings:

1. **O. Al-Dori** and A. Dönük, "Precise Estimation of Eddy Current Losses in Distribution Transformer Windings Using FEM," in *International Congress of Engineering and Natural Sciences Studies (ICENSS)*, 2021, pp. 414–425.