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DESIGN AND PROTOTYPING OF A NEW SWITCHED-MODE POWER SUPPLY FOR AN ELECTRICAL VEHICLE

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ARJAN HUSSEIN FADHIL FADHIL

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DESIGN AND PROTOTYPING OF A NEW SWITCHED-MODE POWER SUPPLY FOR AN ELECTRICAL VEHICLE

By Arjan Hussein Fadhil FADHIL

December 2022

We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science

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Arjan Hussein Fadhil FADHIL

ABSTRACT

DESIGN AND PROTOTYPNG OF A NEW SWITCHED-MODE POWER SUPPLY FOR AN ELECTRICAL VEHICLE

Arjan Hussein Fadhil FADHIL

Master of Science in Electrical - Electronics Engineering

Advisor: Asst. Prof. Dr. İsmail TOPALOĞLU

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In this study, we explain several well-known topologies (the basic elementary building blocks) that are widely used to design and implement linear and switching power supply. For each topology there are common and unique characteristics, so an experienced designer will choose the most suitable structure for the intended application. In general, the choice maybe difficult, so it ought to spend a few times to create an essential understanding of the properties, since the right initial choice will dodge sitting around idly on a structure that will not be the most excellent for the application. In this work, some topologies used in switch mode power supply SMPS are described in detail, and each topology is described with the specified mathematical equations for each of its components, and the output of these topologies is shown. A comparison of isolated and non-isolated topology types and the characterization of voltages and currents in each part of the design are presented. In the end, the simulation was carried out using the Python language, and the practical results of the studied designs were presented, and they matched with the theoretical study.

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Keywords: SMPS, Circuit topology, Isolated SMPS, Non-isolated SMPS, Python power circuit.

ÖZET

ELEKTRİKLİ OTOMOBİLLER İÇİN YENİ BİR YERLEŞİK ŞARJ BİRİMİ (SMPS) TASARIMI VE UYGULAMASI

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Bu projede, doğrusal ve anahtarlamalı güç kaynağı tasarlamak ve uygulamak için yaygın olarak kullanılan birkaç iyi bilinen topolojiler (temel temel yapı taşları) açıklanmıştır. Her topoloji için ortak ve benzersiz özellikler vardır, bu nedenle deneyimli bir tasarımcı amaçlanan uygulama için en uygun yapıyı seçecektir. Genel olarak, seçim zor olabilir, bu nedenle, doğru ilk seçim, uygulama için en mükemmel olmayacak bir yapı üzerinde boş boş oturmaktan kaçınacağından, özelliklerin temel bir anlayışını oluşturmak için birkaç kez harcamak gerekir. Bu çalışmada, anahtarlamalı güç kaynağı SMPS'de kullanılan bazı topolojiler detaylı olarak anlatılmış ve her bir topoloji, bileşenlerinin her biri için belirtilen matematiksel denklemlerle anlatılmış ve bu topolojilerin çıktıları gösterilmiştir. İzole edilmiş ve izole edilmemiş topoloji türlerinin bir karşılaştırması ve tasarımın her bir bölümündeki gerilim ve akımların karakterizasyonu sunulmaktadır. Son olarak Python dili kullanılarak simülasyon gerçekleştirilmiş ve çalışılan tasarımların pratik sonuçları sunulmuş ve teorik çalışma ile eşleştirilmiştir.

2022, 117 sayfa

Anahtar Kelimeler: SMPS, Devre topoloji, Ayrılmış SMPS, Ayrılmamış SMPS, Python güç devresi.

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I would like to thank my thesis advisor, Assoc. Prof. Dr. İsmail TOPALOĞLU, for his patience, guidance and understanding. I would like to thank Asst. Prof. Dr. Mervan BAYRAKTAR for helping. Finally, I would like to express my gratitude to my mother, father, my wife Saynar and my children Ali and Memed for their moral support.

Arjan Hussein Fadhil FADHIL
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CONTENTS

LIST OF SYMBOLS

D	Duty cycle
f_{switch}	Switching frequency of the power supply's FET
I_{out}	Output current
t_1	Time, when the FET is conducting and current in the inductor is increasing.
t_2	Time, when the FET is not conducting and current in the inductor is decreasing
t_3	Time, when the FET is not conducting and constant current or no current flows through the inductor for non-interleaved switching topologies.
t_{ad}	Time after demagnetization
t_d	Demagnetization time
t_{ph}	Phase shift time
T_{switch}	Switching period
V_f	Diode forward voltage

LIST OF ABBREVIATIONS

AC	Alternating current
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
RHPZ	Right half plane zero
RMS	Root mean square
SR	Synchronous rectifier
SMPS	Switch mode power supply
PWM	Pulse width modulation

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1. INTRODUCTION

1.1 General View

The term switch mode power supply (SMPS) first came to light in the seventies when Hewlett Packard used it in its first pocket calculator. Since then, SMPS design has become a precise engineering science. The unstoppable development in electronic component miniaturization has led to an urgent demand for small and efficient power supply units. As a result, SMPS has become a new research topic that caught the attention of some expert electronic engineers around the world. This intensive research has led to the emergence of baffling SMPS topologies (Buisson *et al.* 2002).

Of course, there is no ideal design that meets the requirements of all systems. Every topology has its own advantages and also suffers from certain limitations. So it is up to the power supply designer to choose which topology most matches the desired system requirements and define the preferred technique for a particular application (Tan *et al.* 2006).

Any SMPS is a small part of a complex processing system. It is responsible for providing the system with all the voltages and currents needed. Additionally, it must provide other functions such as power good signal, which is an indicator that shows whether the output voltage and current signals are within their required limits. And the power failure warning signals that give an advanced warning of line failure, as well as the overtemperature protection which is responsible for shutting down the system to avoid any component damage. In some designs, the SMPS might respond to an external signal to turn the power on and off. Overcurrent protection is provided by a current limit circuitry to protect both the supply and load from fault conditions, and overvoltage protection is used to protect sensitive loads from overvoltage conditions. Some applications require synchronization between the switching frequency and an external desired one (Alfarra *et al.* 2004, Alfarra *et al.* 2006).

Designing a modern power processing system is a simple matter, for there are many topologies to consider and the user must be well aware of the advantages and limitations of every technique. Understanding this will allow the engineer to define the power supply requirements so that the final design meets all the desired requirements and is guaranteed to be cost-effective and reliable (Allan *et al.* 2003).

Depending on the user's needs, the system engineer can change and rearrange the power distribution system to produce a much more reliable and cost-effective solution. This means that the power supply specifications must be an interactive exercise between both the designer and the user (Allan *et al.* 2004).

Power supply specifications have their inflexible boundaries and limitations which may result in high cost, high complexity, and lower reliability. So the user must understand those limitations to be on the safe side and eventually obtain reliable and cost-effective solutions.

1.2 SMPS Technology

The study and analysis of power switches and their control vary in difficulty according to the complexity of each switch. The physical structure of such systems changes with time according to the circuit breaker situation and due to the sudden switching of the loads used. Besides, the difficulty increases if there is more than one effective circuit breaker (Bahreini *et al.* 2005). Because of the nonlinear nature of the switching elements, the application of linear control laws to such systems does not achieve satisfactory performance in the event of a significant change in the system parameters. Research and articles agreed that the traditional controllers are unable to adapt to external disturbances and changes in the internal parameters of the system (Verma *et al.* 2013).

In turn, it reduces the voltage regulation (Perry *et al.* 2004). The majority of classical control techniques for power switches are based on pulse width modulation technology (PWM), which in turn depends on the average model that achieves

optimum performance only for specific conditions. In the presence of the non-linear working conditions that we mentioned earlier, it is necessary to search for alternative theories to control the power switches to achieve the desired performance and the required response. Figure 1.1 shows the control methodologies used to deal with this type of systems (Tan *et al.* 2018, Tse and Adams 1990, So *et al.* 1996, Aghababaie *et al.* 2015, Laszlo and Geza 2014, Verma *et al.* 2013, Edwards *et al.* 1998, Chan *et al.* 1992).

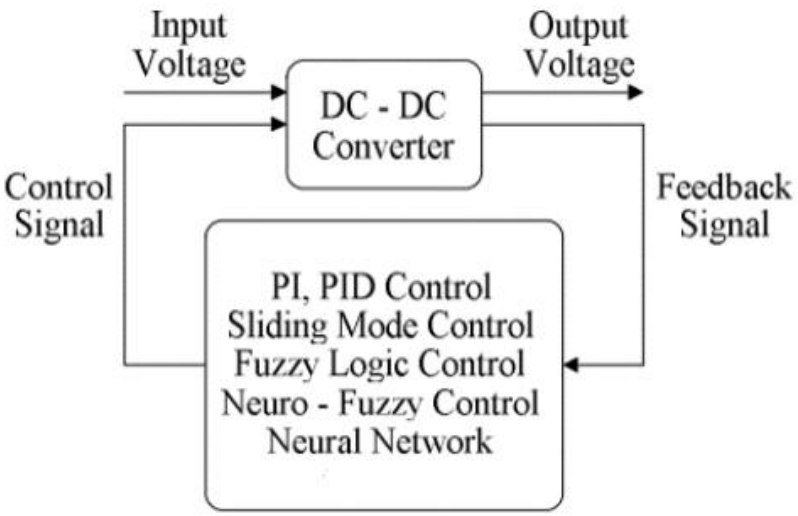


Figure 1.1 Smps control methodologies

1.3 The Aim of Thesis

Switching power converters are well known to researchers working in this field. The buck, boost, and buck-boost are the three simplest, most common, and widely used SMPS in electrical power regulation. These switches in their assortment consist of a single active switch that can be opened and closed (power MOSFET) and an uncontrolled switch (Diode) in addition to the energy storage elements represented by the (coil) and the filter capacitor. In this thesis, we introduce the intermittent power switches, methods of designing and selecting the components of these switches, and explain the working principle. The design is implemented using Python language and simulation results are illustrated and compared.

1.4 The Porpuse of Thesis

This paper presents an overview of the most important DC-DC converter topologies. The main object is to guide the designer in selecting the topology with its associated power semiconductor devices. The DC-DC converter topologies can be divided in two major parts, depending on whether or not they have galvanic isolation between the input supply and the output circuitry.

1.5 Literature Review

In the following, we focus on the references related to the modeling and design of command laws used to control switching mode power supplies, with particular reference to the synchronous buck converter. Recent studies have paid good attention to deducing a method for modeling the switching process for all power converters, including the synchronous buck converter (Hassanzadeh *et al.* 2011, Priewasser *et al.* 2014, Abaali 2016, Allain *et al.* 2009, Kanimozhi *et al.* 2017, Yildiz and Sumer 2009, Middlebrook and Cuck 1976, Scherpen *et al.* 2000).

Hassanzadeh *et al.* (2011), (Abaali 2016) represented SMPS model as a Linear Time-Invariant System (LTIS), and in the study of (Allain *et al.* 2009, Kanimozhi *et al.* 2017), the work is continued and the system identification is completed by finding the state space model for the system

On the other hand, a group of researchers suggested a mapping between electrical power systems and mechanical systems, and they concluded with the discontinuous Euler-Lagrange model (Yildiz and Sumer 2009, Scherpen *et al.* 2000).

As for the control methodologies, they have been widely applied to all power switches, both linear and non-linear. But with regard to the modern synchronous buckregulator, research is still limited, unlike other power converters in which research and work have been going on since 1976.

In this section, we present research related to the control of the synchronous buck regulator (Priewasser *et al.* 2010, Priewasser *et al.* 2011, Lindiya and Palani 2012, Wilson *et al.* 2012, Priewasser *et al.* 2013, Ayyappa and Reddy 2015, Thamaraiselvi and Baskaran 2018).

These studies can be classified into three categories depending on the following criteria:

a. According to the control approach: (The regulator type)

Ayyappa and Reddy (2015), (Thamaraiselvi and Baskaran 2018), the SMPS model is linearized in order to be able to use a linear regulator to obtain the transformation function in the time domain and apply the concepts of optimal control through the application of the controller (LQR) or working in the frequency domain by the application of the controller (MultiPID) using the concept of Loop Shaping (Priewasser *et al.* 2010, Priewasser *et al.* 2011). This resulted in a good regulation of the output voltage and high-level dynamic performance.

For the non-linear control methodologies implemented in studies (Wilson *et al.* 2012, Thamaraiselvi and Baskaran 2018), the non-linearsliding mode control was adopted with a variable switching frequency. Thanks to this approach, the output voltage rippleissignificantly reduced, and the effect of the transient stateisbrought down to a minimum, along witha high level ofrobustness against the changes in the input voltage level and the load resistance.

Another approach of nonlinear control is fuzzy control with a minimum number of membership functions is also implemented in the study (Lindiya and Palani 2012).

Finally, a comparison is presented between the results obtained by the non-linear fuzzy control regulator and the linear PID whose three parameters were tuned using two methods, the Internal Mode Control and the Zegler Nicholas.

Compared to the linear PID regulator, the non-linear fuzzy control regulator gave a faster dynamic response, lower overshoot, and minimum changes in output voltage when there were disturbances in the input voltage and load resistance.

b. According to the development environment:

As for previous studies and research, the simulation partwas achieved within different development environments, mostly in the MatLab Simulink tool (Ayyappa and Reddy 2015, Thamaraiselvi and Baskaran 2018). Other studies also used this environment but with the "simpower" library (Lindiya and Palani 2012).

As for the implementation, an FBGA kit was used for research purposes only. The use of the FBGA is justified because the research requires applying both optimal and robust control regulators. These modern theory regulators require complex mathematical equations, and consequently, memory capacity and processing speed that may not be provided by microcontrollers (Priewasser *et al.* 2013).

c. According to the state space variables:

The choice of state space variables depends on the control approach (i.e. the regulator type), so here we have two cases:

- When using a linear PID:

In the modeling and identification of the SMPS system, and depending on the mathematical equations of the system, the state space variables used are usually represented by the instantaneous output voltage and the instantaneous coil current (Lindiya and Palani 2012, Priewasser *et al.* 2013).

- When using non-linear sliding-mode control:

Here we have two approaches:

- The firstapproach

A sliding-mode controller is designed to regulate the output voltage of the two-phase synchronous buck regulator (Wilson *et al.* 2012).

In this study, the single-phase sliding mode controller was designed according to the methodology followed by the asynchronous buck regulator, and the adoption of state variables represented by the output voltage error and the derivative and integration of this error as in the study (Tan *et al.* 2018).

Then it was modified to work in two phases, and this resulted in the definition of two sliding surfaces for each phase, and each surface was characterized by four state space variables, where a fourth variable, a function of time, was added to the previous three to expressthe phase difference.

As a result of this article, the output voltage ripple and the effect of transients were reduced, hence the sliding mode was found to be highly effective in multi-phase electrical systems.

- The secondapproach

A sliding-mode controller is designed to control the coil current of the synchronous buck regulator with a variable switching frequency in order to regulate the output voltage (Thamaraiselvi and Baskaran 2018).

This study gave a fast dynamic response and as a result, led to a reduction in the coil current ripple and thus achieving good regulation of the output voltage and efficiency of around 95%.

2. COMPARISON OF SMPS AND LINEAR POWER SUPPLIES

There are two basic types of regulated power supplies available: SMPS and linear. In the following table is a comparison between the linear and the SMPS power supplies with switching regulators in general (Table 2.1).

Table 2.1 Smps vs linear power supplies

Parameter	Linear power supplies	SMPS power supplies	Notes
Size and weight	Heatsinks for high power linear regulators increase both size and weight. Transformers, if used, are large due to the low operating frequency (mains frequency 50 or 60 Hz)	Smaller transformer (if used; otherwise inductor) due to higher operating frequency (typically 50 kHz - 1 MHz). The size and weight of adequate RF shielding can be significant.	The power rating of a transformer of a given size and weight increases with frequency provided that the hysteresis loss can be reduced. Therefore, a higher operating frequency means either more power or a smaller transformer.
Output voltage	When using a transformer, any voltage is available; if no transformer is used, then limited to what can be achieved with a voltage doubler. In the unregulated state, the voltage is highly dependent on the load.	Any voltage available, limited only by the breakdown voltages of transistors in many circuits. The voltage varies little with load.	The SMPS can usually handle a wider input signal change before the output voltage changes.
Efficiency, heat, and power dissipation	If adjustable: efficiency largely depends on the voltage difference between the input and output. The output voltage is regulated by dissipating excess power as heat, resulting in a typical efficiency of 30-40%. If left unregulated, losses in transformer steel and copper can be the only significant sources of inefficiency.	The output is regulated by duty cycle control; the transistors are fully on or completely off, so there is very little resistive loss between the input and the load. The only heat is generated in non-ideal components and quiescent current in the control circuit.	Switching losses in transistors (especially in the short part of each cycle when the device is partially turned on), on-state resistance of switching transistors, equivalent series resistance in the inductor and capacitors, and core losses in the inductor and rectifier voltage drop. contribute to a typical efficiency of 60–70%. However, by optimizing the design of the SMPS (such as choosing the optimal switching frequency, avoiding inductor saturation, and active rectification), the amount of power and heat loss can be kept to a minimum; a good design can be 95% efficient.

Table 2.1 Smps vs linear power supplies (Continued)

Parameter	Linear power supplies	SMPS power supplies	Notes
RF interference	Weak high frequency noise can be produced by AC rectifier diodes under high current load, while most other types of power supplies do not create high frequency noise. Some induction of main noise into unshielded cables, which is problematic for weak audio signals.	EMI/RFI occur due to sudden on / off currents. Therefore, EMI filters and RF shielding are needed to reduce interference.	Long wires between components can reduce the effectiveness of the high pass filter provided by the input and output capacitors. A stable switching frequency may be important.
Electronic noise at output terminals	Unregulated power supplies can have small AC fluctuations superimposed on the DC component at twice the main frequency (100–120 Hz). This can cause audible main hum in audio equipment, brightness fluctuations, or band distortion in analog CCTV cameras.	More noisy due to the switching frequency of the SMPS. An unfiltered output can cause glitches in digital circuits or noise in audio circuits.	This can be suppressed with capacitors and other filtering circuits in the output stage. With a switching power supply, the switching frequency can be selected so that the noise does not fall into the operating frequency band of the circuits (for example, for audio systems above the range of human hearing).
Electronic noise at input terminals	Causes harmonic distortion in the AC input, but relatively little or no high frequency noise.	A very cheap SMPS can feed electrical switching noise back into the power line, interfering with audio/video equipment connected to the same phase. SMPS without power factor correction also cause harmonic distortion.	This can be avoided by connecting a (properly grounded) EMI/RFI filter between the input terminals and the bridge rectifier
Acoustic noise	Weak, usually inaudible hum in the mains, usually due to vibration of the transformer windings or magnetostriction.	Usually inaudible to most people unless they have a fan, or are not loaded/failed, or are using a switching frequency within the audio range, or the coil plates are vibrating at a sub-harmonic of the operating frequency.	The operating frequency of an unloaded SMPS is sometimes in the audible human range and can subjectively sound quite loud to people whose hearing is very sensitive to the corresponding frequency range.

Table 2.1 Smps vs linear power supplies (Continued)

Parameter	Linear power supplies	SMPS power supplies	Notes
Strength factor	Low for a regulated power supply because current is drawn from the mains at the peaks of the voltage sine wave, unless the inductor input or resistor input circuit follows a rectifier (rare now).	Very low to medium range as a simple SMPS without PFC draws bursts of current at the peaks of the AC sine wave.	Active/passive power factor correction in SMPS can solve this problem and is even required by some electricity regulators, especially in the EU. The internal resistance of low power transformers in linear power supplies typically limits the peak current in each cycle and thus gives a better power factor than many switching power supplies that directly rectify a network with little series resistance.
Starting current	High current when mains powered equipment is turned on until the transformer flux stabilizes and the capacitors are fully charged, unless a slow start circuit is used.	Extremely high peak surge current limited only by the impedance of the input power supply and any series resistance of the filter capacitors	Empty filter capacitors initially draw a large amount of current when charging, while larger capacitors draw more peak current. Being many times the normal operating current, this heavily stresses overvoltage-prone components, makes fuse selection difficult to avoid unwanted fuse tripping, and can cause problems with equipment using overcurrent protection, such as uninterruptible power supplies. Reduced by using a suitable soft start circuit or series resistor.

Now, because it is still a modern technology, the high component count of SMPS made this technology more expensive than linear power supplies. However, with the fast development of electronics, the cost of electronic components has dropped so low that the high cost of raw material content of copper and iron present in the linear transformer has made the SMPS technology much more cost effective.

Although SMPS suffers from many disadvantages like being more complex and requiring more need to control EMI, its advantages far outweigh linear power supplies in a few niche applications.

3. SWITCHED-MODE POWER SUPPLIES TOPOLOGIES (NON-ISOLATED SWITCHING REGULATORS)

In SMPS circuits, we have energy storage units like inductors (to store electro-magnetic energy), capacitors (to store electrical energy), in addition to power transistors and rectifiers.

Although there is a wide variety of power converter topologies, only about a dozen basic ones are used in practical power design.

Depending on the principle of operation, these topologies can be categorized into two main families: buck and flyback. In the first, that is the buck regulator, energy is transferred from the input to the load during the conduction cycle of a switching transistor. Whereas, in the latter, the flyback, energy is stored and accumulated during the "on-state" of a power transistor and then delivered to the output or the load during the "off-state" of the switch. Any practical power circuit belongs to one of these two configurations or is a combination of both. The forward and bridge converters are two examples of the buck type and the boost, buck-boost, and transformer-isolated flyback regulators can be considered examples of the boost type.

Output signals: output voltage/current in each configuration:

- According to the output voltages:

✓ The buck converter is a step down converter, in other words, the output voltage value is less than the input voltage.
✓ The boost converter is a step-up converter in which the output voltage is greater than the input voltage.
✓ Buck-boost converter performs both these functions based on the range of duty cycle. If the duty cycle ratio is less than 0.5, then it functions as a buck regulator while for a duty cycle ratio greater than 0.5, it works as a boost regulator.

Moreover, in this buck-boost configuration, the output voltage has a polarity reversal with respect to the input voltage unlike in the other two converters.

- According to the nature of currents:

In the buck converter, the input current is discontinuous whereas the output current is continuous. On the contrary, the input current in the boost converter is continuous whereas the output current is discontinuous. Finally, in the buck-boost converter both input and output currents are discontinuous in nature.

3.1 The Buck Converter: (Step-Down Voltage Regulator)

There are two types of DC-to-DC buck regulators, the non-synchronous and the synchronous.

Figure 3.1 illustrates the non-synchronous DC-DC buck converter circuit diagram, which is often referred to as a chopper circuit.

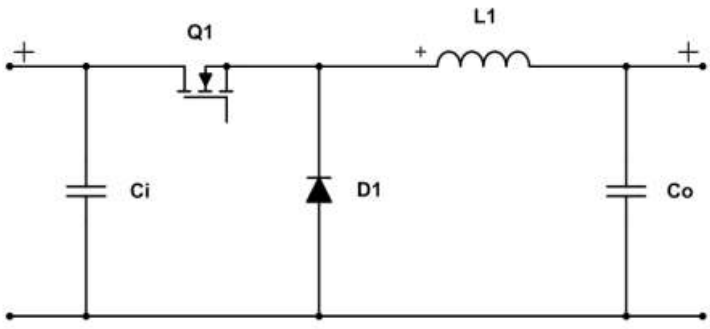


Figure 3.1 The schematic of a non-synchronous dc-to-dc buck converter

For desining and calculating a synchronous DC-DC buck converter, we set Vf = 0V. The waveforms for the synchronous DC-DC buck converter show the operation in a forced PWM scenario, where a non-synchronous buck converter would enter DCM. For normal operation, there is an additional positive DC offset for the current of the FET transistor and the inductor. The CCM waveforms can be used as reference. In

case of the synchronous rectifier current the additional DC offset would be negative as shown in Figure 3.2.

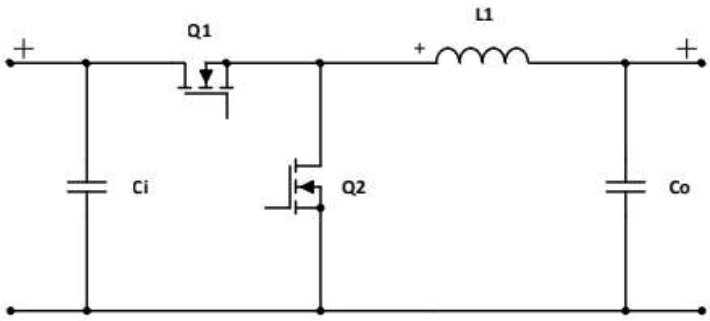


Figure 3.2 The schematic of a synchronous dc-to-dc buck converter

3.1.1 The equations of the general buck converter

The inductor current ripple I_{ripple} in general is given by the Equation (3.1)

$$I_{ripple} = \frac{1}{L_1}(V_{in} - V_{out})t_1 \tag{3.1}$$

First: The Continuous Conduction Mode with Synchronous forced PWM

When the FET transistor is on, then the increasing current time is Equation (3.2)

$$t_1 = \frac{1}{f_{switch}} \frac{V_{out} + V_f}{V_{in} + V_f} \tag{3.2}$$

When the FET transistor is off, then the decreasing current time is Equation (3.3)

$$t_2 = \frac{1}{f_{switch}} - t_1 \tag{3.3}$$

The minimum inductor current in this case Equation (3.4)

$$I_{\min} = I_{out} - \frac{I_{ripple}}{2} \tag{3.4}$$

The maximum inductor current in this case Equation (3.5)

$$I_{\max} = I_{out} + \frac{I_{ripple}}{2} \tag{3.5}$$

The average input current Equation (3.6)

$$I_{in,avg} = \frac{V_{out} I_{out}}{V_{in}} + \frac{V_f}{V_{in}} \frac{I_{\min} + I_{\max}}{2} t_2 f_{switch} \tag{3.6}$$

Second: The Discontinuous Conduction Mode

When the FET transistor is on, then the increasing current time is Equation (3.7)

$$t_1 = \sqrt{2 I_{out} L_1 \frac{V_{out} + V_f}{f_{switch}(V_{in} + V_{out})(V_{in} + V_f)}} \tag{3.7}$$

When the FET transistor is off, then the decreasing current time is Equation (3.8)

$$t_2 = t_1 \left(\frac{V_{in} + V_f}{V_{out} + V_f} - 1\right) \tag{3.8}$$

In the case of the FET transistor is off (current equals to zero) Equation (3.9)

$$t_3 = \frac{1}{f_{switch}} - t_1 - t_2 \tag{3.9}$$

The minimum inductor current in this case Equation (3.10)

$$I_{\min} = 0\ A \tag{3.10}$$

The maximum inductor current in this case Equation (3.11)

$$I_{\max} = \frac{1}{L_1}(V_{in} - V_{out})t_1 \tag{3.11}$$

The average input current is given as Equation (3.12)

$$I_{in,avg} = \frac{V_{out} I_{out}}{V_{in}} + \frac{V_f}{V_{in}} \frac{I_{\min} + I_{\max}}{2} t_2 f_{switch} \tag{3.12}$$

3.1.2 Buck converter components

- **The Inductor L_1**

  Figure 3.3 shows the inductor L_1 voltage waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and synchronos forced PWM.

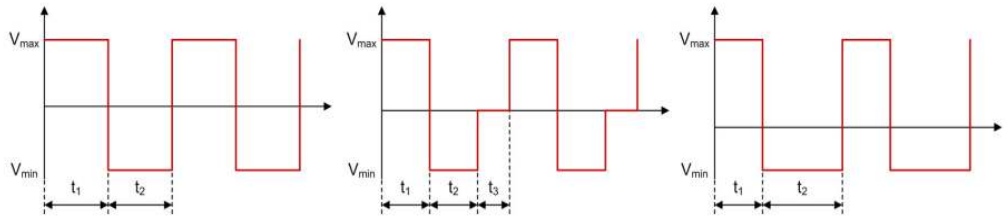


Figure 3.3 Buck - inductor l_1 voltage waveforms in CCM, DCM and synchronous forced pwm

The Figure 3.4 shows the inductor L_1 current waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and synchronos forced PWM.

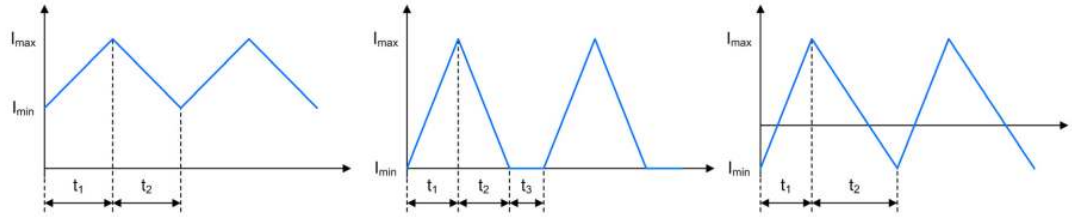


Figure 3.4 Buck - inductor l_1 current waveforms in CCM, DCM and synchronous forced pwm

The average inductor current Equation (3.13)

$$I_{L_1,avg} = \frac{I_{\min} + I_{\max}}{2}(t_1 + t_2) f_{switch} \tag{3.13}$$

The minimum inductor voltage Equation (3.14)

$$V_{L_1,\min} = -V_{out} - V_f \tag{3.14}$$

The maximum inductor voltage Equation (3.15)

$$V_{L_1,\max} = V_{in} - V_{out} \tag{3.15}$$

The inductor voltage during time t_3 Equation (3.16)

$$V_{L_1,t_3} = 0\,V \tag{3.16}$$

- **FET transistor Q_1**

Figure 3.5 shows the transistor Q_1 voltage waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and synchronos forced PWM.

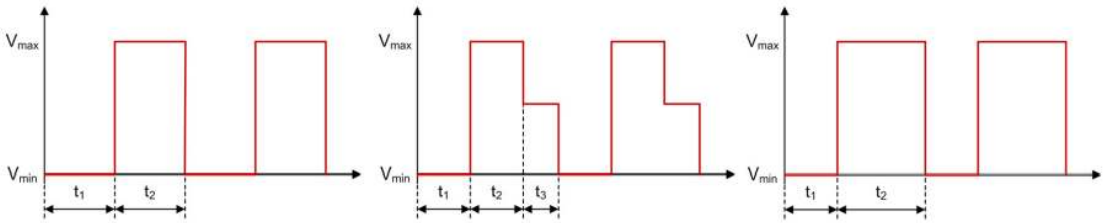


Figure 3.5 Buck - fet q_1 voltage waveforms in CCM, DCM and synchronous forced pwm

Figure 3.6 shows the transistor q_1 current waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and synchronos forced PWM.

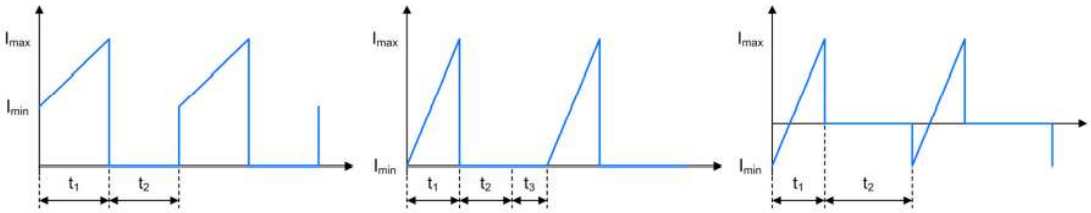


Figure 3.6 Buck - fet q_1 Current Waveforms in CCM, DCM and synchronous forced pwm

The average transistor current Equation (3.17)

$$I_{Q_1,avg} = \frac{I_{\min} + I_{\max}}{2} t_1 f_{switch} \tag{3.17}$$

The minimum FET transistor voltage Equation (3.18)

$$V_{Q_1,\min} = 0\,V \tag{3.18}$$

The maximum FET transistor voltage Equation (3.19)

$$V_{Q_1,\max} = V_{in} + V_f \tag{3.19}$$

The transistor voltage during time t_3 Equation (3.20)

$$V_{Q_1,t_3} = V_{in} - V_{out} \tag{3.20}$$

- **Diode D_1**

Figure 3.7 shows the diode d_1 voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

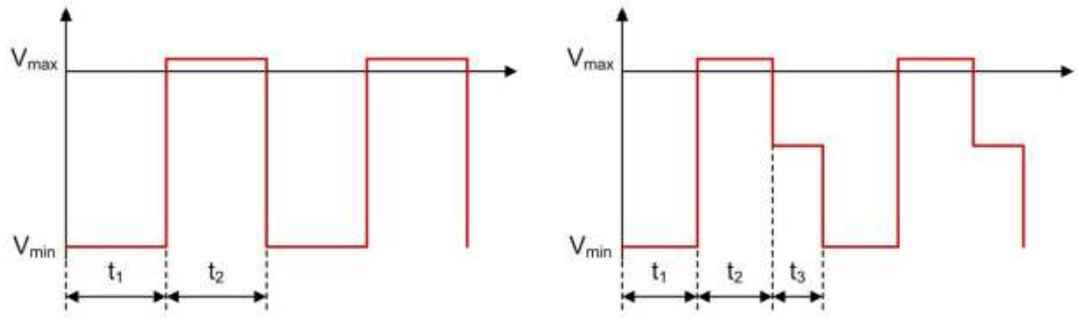


Figure 3.7 Buck - diode d_1 voltage waveforms in CCM, and DCM

Figure 3.8 shows the diode D_1 current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

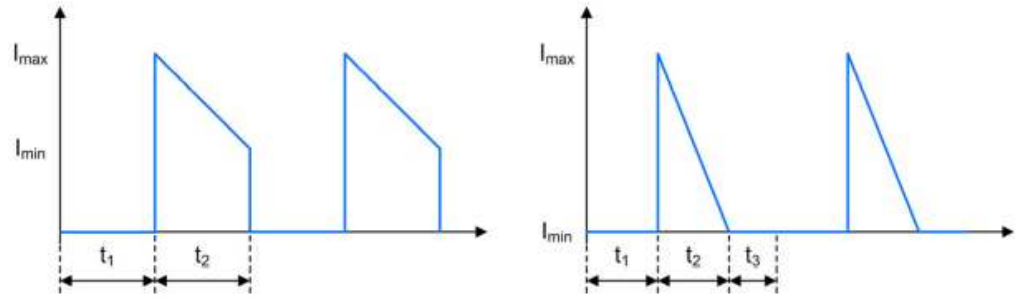


Figure 3.8 Buck - diode d_1 current waveforms in CCM, and DCM

The average diode current Equation (3.21)

$$I_{D_1,avg} = \frac{I_{\min} + I_{\max}}{2} t_2 f_{switch} \tag{3.21}$$

The minimum diode voltage Equation (3.22)

$$V_{D_1,\min} = -V_{in} \tag{3.22}$$

The maximum diode voltage Equation (3.23)

$$V_{D_1,\max} = V_f \tag{3.23}$$

The diode voltage during time t_3 Equation (3.24)

$$V_{D_1,t_3} = -V_{out} \tag{3.24}$$

- **Input Capacitor C_i**

Figure 3.9 shows the input capacitor C_i voltage waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and synchronous forced PWM.

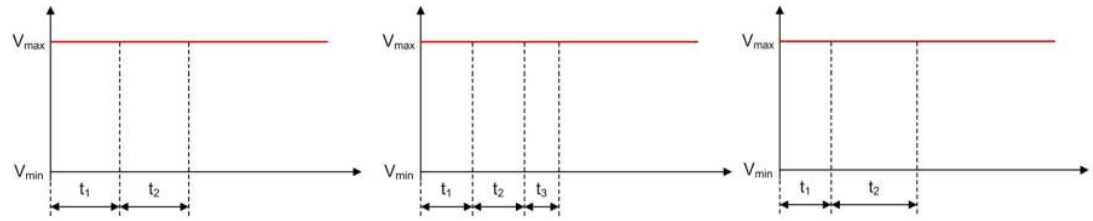


Figure 3.9 Buck – input capacitor c_i voltage waveforms in CCM, DCM, and synchronous forced pwm

Figure 3.10 shows the input capacitor C_i current waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and synchronous forced PWM.

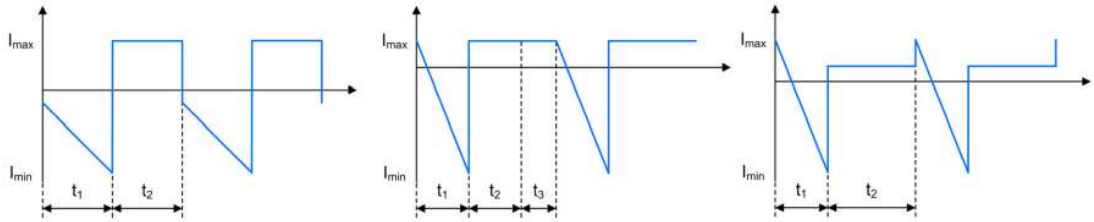


Figure 3.10 Buck - input capacitor c_i current waveforms in CCM, and DCM.

The minimum input capacitor current during time t_1 Equation (3.25)

$$I_{C_i,\min,t_1} = -I_{\max} + I_{in,avg} \tag{3.25}$$

The maximum input capacitor current during time t_1 Equation (3.26)

$$I_{C_i,\max,t_1} = -I_{\min} + I_{in,avg} \tag{3.26}$$

The input capacitor current during time interval t_2 and t_3 Equation (3.27)

$$I_{C_i,\max,t_{2/3}} = I_{in,avg} \tag{3.27}$$

The average input capacitor current Equation (3.28)

$$I_{C_i,avg} = 0A \tag{3.28}$$

The input capacitor voltage Equation (3.29)

$$V_{C_i} = V_{in} \tag{3.29}$$

The Output capacitor C_0

Figure 3.11 shows the output capacitor C_o voltage waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and synchronous forced PWM.

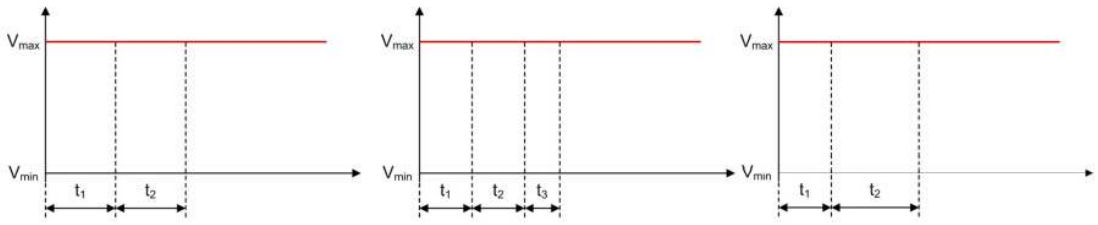


Figure 3.11 Buck – output capacitor c_o voltage waveforms in CCM, DCM, and synchronous forced pwm

Figure 3.12 shows the output capacitor C_o current waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and synchronous forced PWM.

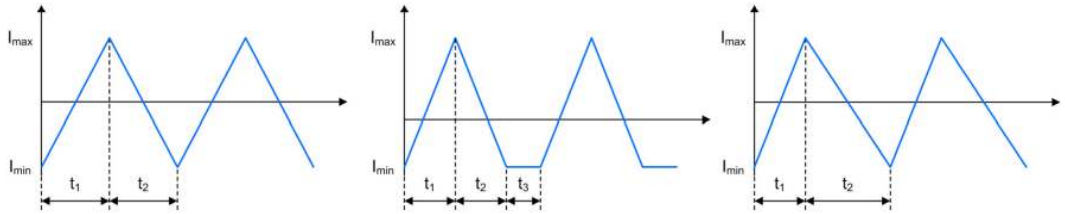


Figure 3.12 Buck - output capacitor c_o current waveforms in CCM, DCM, and synchronous forced pwm

The minimum output capacitor C_o current Equation (3.30)

$$I_{C_o,\min} = I_{\min} - I_{out} \tag{3.30}$$

The maximum output capacitor C_o current Equation (3.31)

$$I_{C_o,\max} = I_{\max} - I_{out} \tag{3.31}$$

The average output capacitor C_o current Equation (3.32)

$$I_{C_o,avg} = 0A \tag{3.32}$$

The output capacitor C_o voltage Equation (3.33)

$$V_{C_o} = V_{out} \tag{3.33}$$

Buck converters are considered one of the simplest, cheapest and most common DC-DC converters topologies. Although it is not suited for applications requiring isolation, buck topology is ideal as a DC-to-DC converter to step down voltages. Because not only can you achieve high efficiency, but also high-power levels using a buck converter, especially with poly-phase topologies. The downside to buck converters is that the input current is always discontinuous, which causes higher (Electro-Magnetic

Interference) EMI. However, EMI issues can be solved using filters such as chip beads, common mode chokes, and filter chokes.

The buck topology only requires one single inductor in single-phase applications, and inductors with standard values are available for a wide range of applications. In addition, custom inductors can be developed for special inductance versus current values that are required for applications requiring extra windings for sensing or supplying power to the controller.

3.2 The Boost Converter: (Step Up Voltage Regulator)

A Boost converter steps up an input voltage to a higher output voltage level, the typical boost circuit schematic is shown in Figure 3.13. The energy is transferred to the output when the FET transistor is not conducting.

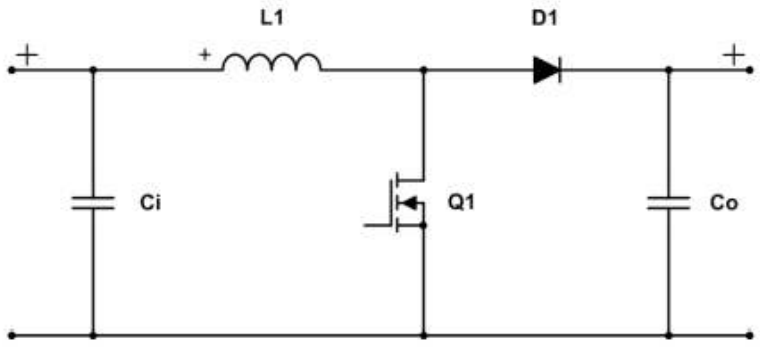


Figure 3.13 The typical schematic of a boost dc-to-dc converter

3.2.1 The equations of a general boost DC-to-DC converter

The inductor current ripple I_{ripple} is given by the Equation (3.34)

$$I_{ripple} = \frac{1}{L_1} V_{in} t_1 \tag{3.34}$$

The right half plane zero Equation (3.35)

$$f_{rhpz} = \frac{V_{out}(1-D)^2}{2\pi L_1 I_{out}} \tag{3.35}$$

The Continuous Conduction Mode (CCM)

When the transistor is on, the increasing current time is Equation (3.36):

$$t_1 = \frac{1}{f_{switch}} \frac{V_{out} + V_f - V_{in}}{V_{out} + V_f} \tag{3.36}$$

And when the transistor is off, the decreasing current time is the same as in the Buck converter.

The minimum inductor current in this case Equation (3.37)

$$I_{\min} = I_{in} - \frac{I_{ripple}}{2} \tag{3.37}$$

And the maximum inductor current is Equation (3.38)

$$I_{\max} = I_{in} + \frac{I_{ripple}}{2} \tag{3.38}$$

While the average input current Equation (3.39)

$$I_{in,avg} = I_{out} \frac{V_{out} + V_f}{V_{in}} \tag{3.39}$$

The Discontinuous Conduction Mode (DCM)

When the transistor is on, then the increasing current time is Equation (3.40)

$$t_1 = \sqrt{2I_{out}L_1 \frac{V_{out} / (V_f V_{in})}{f_{switch} V_{in}^{\ 2}}} \tag{3.40}$$

And when the transistor is off, then the decreasing current time is Equation (3.41)

$$t_2 = t_1 \left(\frac{V_{iout} + V_f}{V_{out} + V_f - V_{in}} - 1\right) \tag{3.41}$$

In the case of the FET transistor is off, no current flows through the circuit and the time t_3 is given by Equation (3.9).

Also, the minimum inductor current is given by Equation (3.10).

The maximum inductor current in this case Equation (3.42)

$$I_{\max} = \frac{1}{L_1} V_{in} t_1 \tag{3.42}$$

The average input current is given by Equation (3.43)

$$I_{in,avg} = I_{out} \frac{V_{out} V_f}{V_{in}} \tag{3.43}$$

3.2.2 Basic components of the boost DC-to-DC converter

- **Inductor L_1**

Figure 3.14 shows the Boost – Inductor L_1 voltage waveforms in CCM and DCM, and Figure 3.15 shows the Boost – Inductor L_1 current waveforms in CCM and DCM.

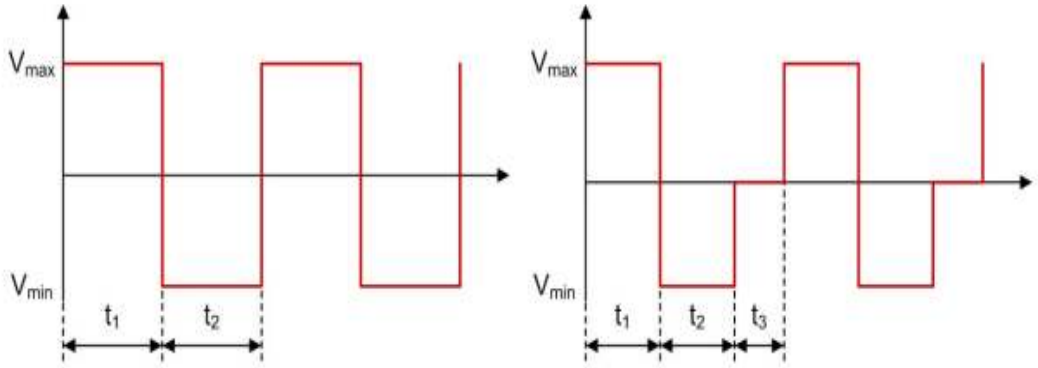


Figure 3.14 Boost – Inductor l_1 voltage waveforms in CCM, and DCM

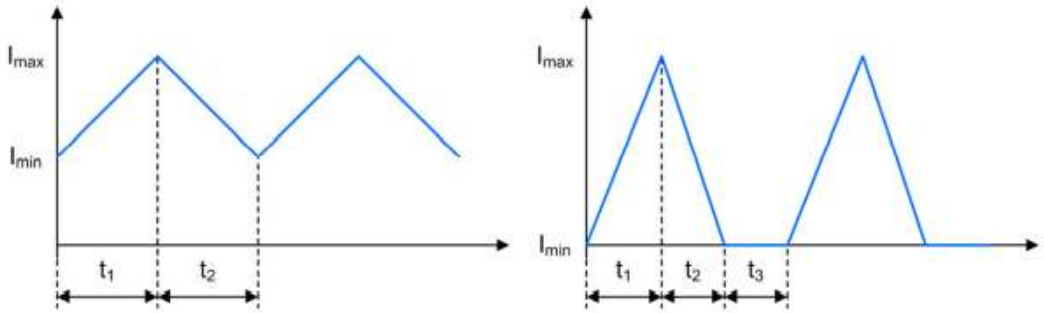


Figure 3.15 Boost – Inductor l_1 current waveforms in CCM, and DCM

The average inductor current is given by Equation (3.44)

$$I_{L_1,avg} = \frac{I_{\min} + I_{\max}}{2}(t_1 + t_2) f_{switch} \tag{3.44}$$

And the minimum inductor voltage is Equation (3.45)

$$V_{L_1,\min} = V_{in} - V_{out} - V_f \tag{3.45}$$

While the maximum inductor voltage is Equation (3.46)

$$V_{L_1,\max} = V_{in} \tag{3.46}$$

Now the inductor voltage during time t_3 Equation (3.47)

$$V_{L_1,t_3} = 0V \tag{3.47}$$

- **FET transistor Q_1**

Figure 3.16 shows the FET transistor Q_1 voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

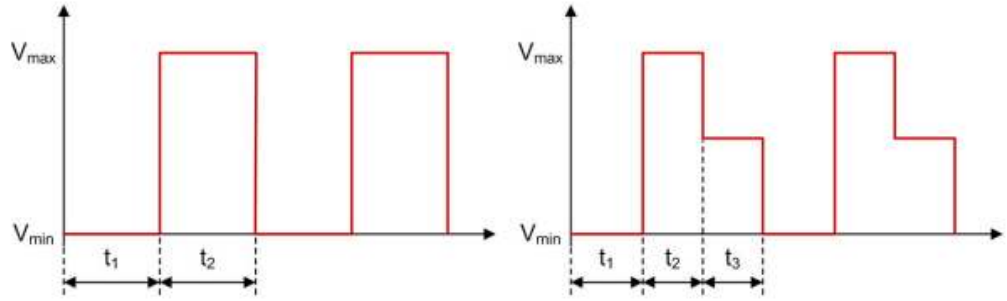


Figure 3.16 Boost - fet q_1 voltage waveforms in CCM, DCM

Figure 3.17 shows the transistor Q_1 current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

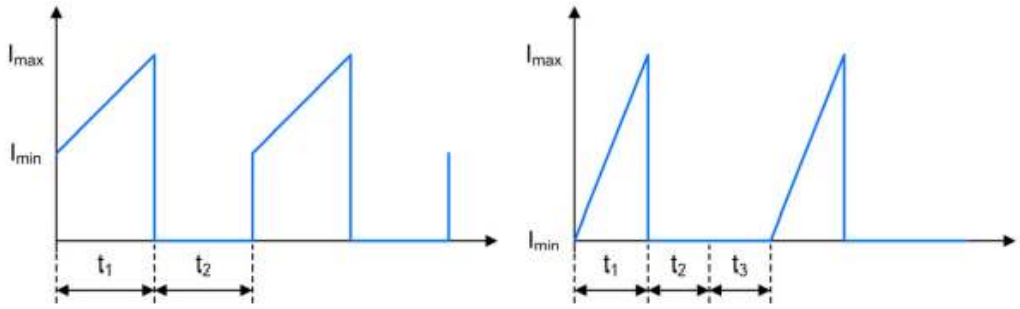


Figure 3.17 Boost - fet transistor q_1 current waveforms in CCM, and DCM

The average FET transistor current is given by Equation (3.17), and the minimum FET voltage is null as in Equation (3.18).

The maximum FET transistor voltage Equation (3.48)

$$V_{Q_1,\max} = V_{out} + V_f \tag{3.48}$$

The FET voltage during time t_3 Equation (3.49)

$$V_{Q_1,t_3} = V_{in} \tag{3.49}$$

- **Diode D_1**

The Figure 3.18 shows the diode D_1 voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

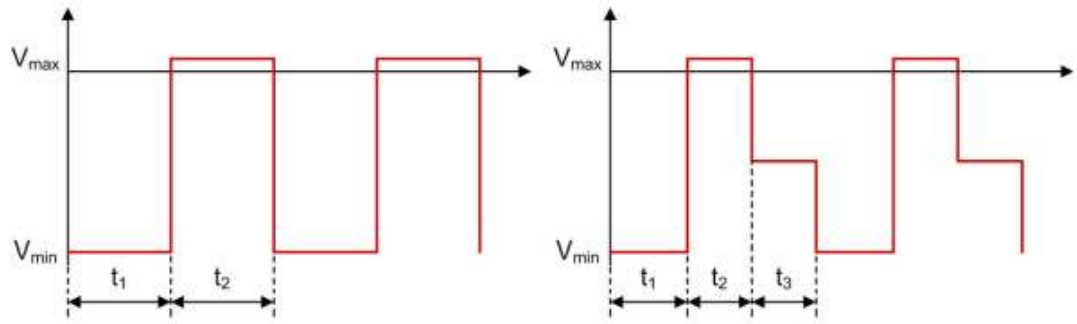


Figure 3.18 Boost - diode d_1 voltage waveforms in CCM, and DCM

Figure 3.19 shows the diode D_1 current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

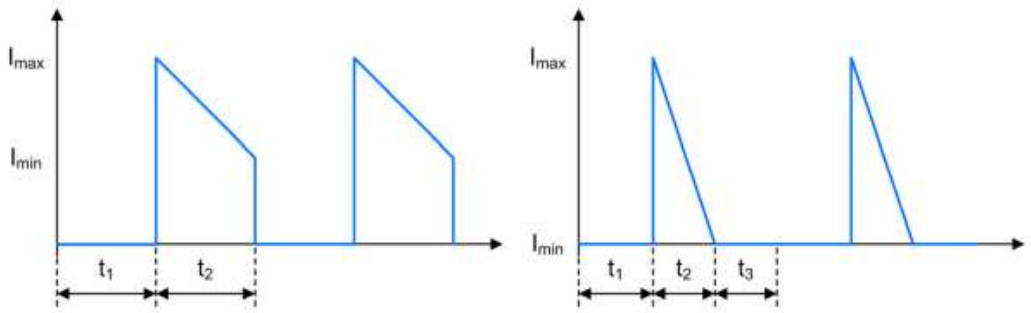


Figure 3.19 Buck - diode d_1 current waveforms in CCM, and DCM

The average diode current is given by Equation (3.21), and the minimum diode voltage Equation (3.50)

$$V_{D_1,\min} = -V_{out} \tag{3.50}$$

The maximum transistor voltage is given by Equation (3.23), but diode voltage during t_3 is given by the Equation (3.51)

$$V_{D_1,t_3} = V_{in} - V_{out} \tag{3.51}$$

- **Input capacitor C_i**

Figure 3.20 shows the input capacitor C_i voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

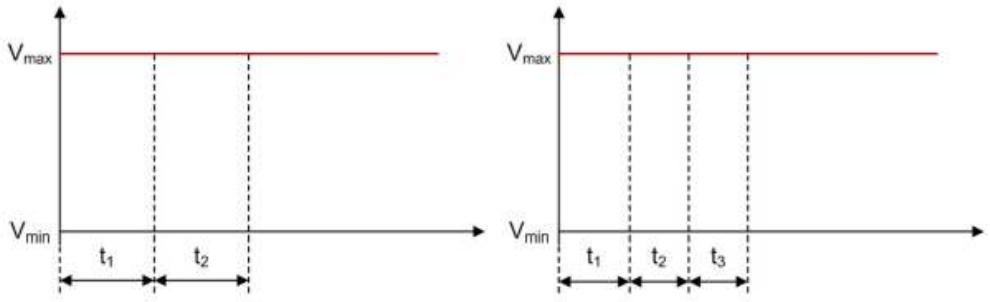


Figure 3.20 Boost – input capacitor c_i voltage waveforms in CCM, and DCM

Figure 3.21 shows the input capacitor C_i current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

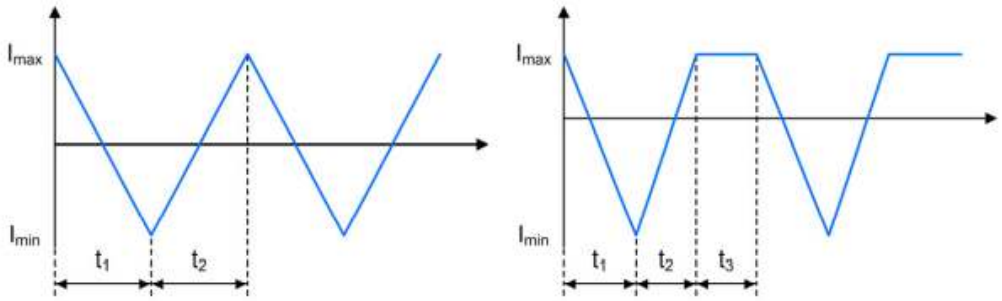


Figure 3.21 Boost - input capacitor c_i current waveforms in CCM, and DCM

The minimum input capacitor current during t_1 Equation (3.52)

$$I_{C_i,\min,t_1} = -I_{\max} + I_{in} \tag{3.52}$$

The maximum input capacitor current during t_1 Equation (3.53)

$$I_{C_i,\max,t_1} = -I_{\min} + I_{in} \tag{3.53}$$

The average input capacitor current is null, and the input capacitor voltage is given by the Equation (3.29).

- **Output capacitor C_0**

Figure 3.22 shows the output capacitor C_o voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

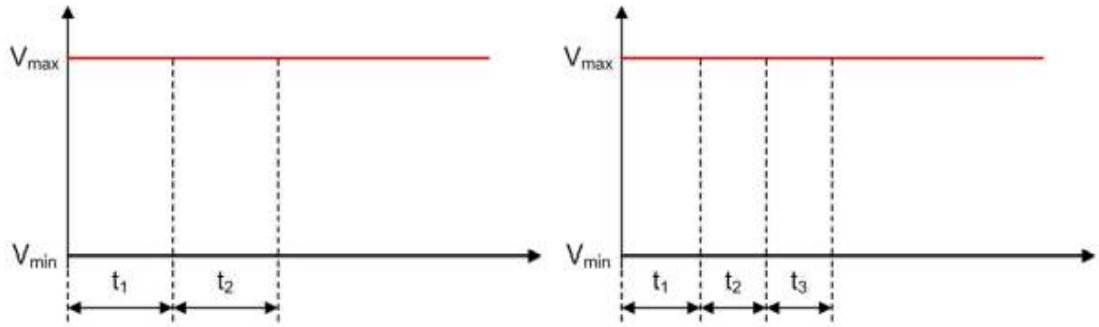


Figure 3.22 Boost – output capacitor c_o voltage waveforms in CCM, and DCM

Figure 3.23 shows the output capacitor C_o current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

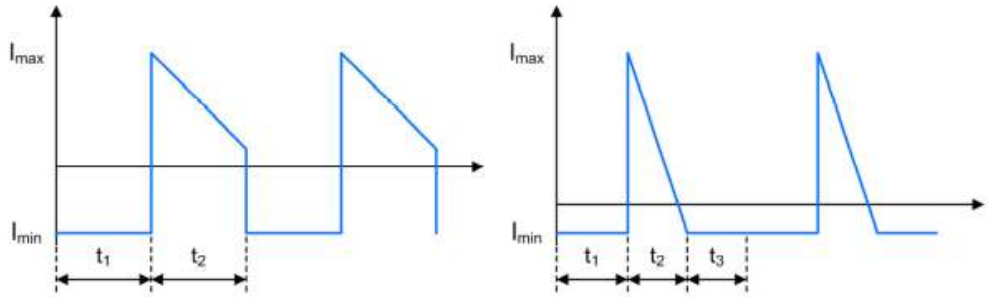


Figure 3.23 Boost - output capacitor c_o current waveforms in CCM, and DCM

The minimum output capacitor current during time interval t_2 and t_3 Equation (3.54)

$$I_{C_o,\min,t_{2/3}} = I_{\min} - I_{out} \tag{3.54}$$

The maximum output capacitor current during time interval t_2 and t_3 Equation (3.55)

$$I_{C_o,\max,t_{2/3}} = I_{\max} - I_{out} \tag{3.55}$$

And The average output capacitor current Equation (3.56)

$$I_{C_o,avg} = 0A \tag{3.56}$$

While the output capacitor voltage is given by Equation (3.33).

Just like the case in the buck topology, the boost power converter is non-isolating. However, unlike the buck topology, the boost steps up the voltage rather than stepping it down. Due to the fact that the boost topology draws current in a continuous even manner when operating in CCM mode, it is considered an ideal choice for Power Factor Correction circuits. And like the buck topology, there are many choices for inductor standard values used in boost circuits. If, in some applications, there is a special need, custom inductors are available as well.

3.3 Inverting Buck-Boost Converter

An Inverting Buck-Boost regulator converts a positive input voltage to a higher or lower negative output voltage. The energy is transferred to the output when the FET transistor is not conducting. Figure 3.24 shows the schematic of an inverting Buck-Boost converter.

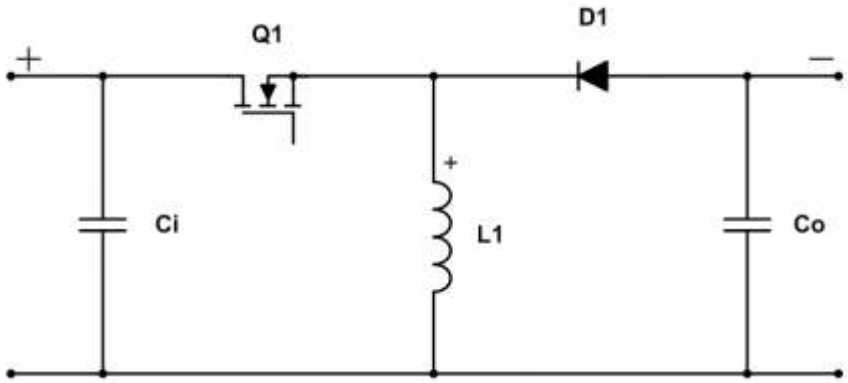


Figure 3.24 The schematic of an inverting buck-boost converter

- **Advantages**:

Step-up and/or step-down of voltage is possible with minimum component count. (Cuk, SEPIC, Zeta uses almost double component count).

Less costly compared to most of the other converters.

- **Disadvantages**:

Both input current and output capacitor charging current are discontinuous resulting in larger filter size and much more EMI issues.

The output is inverted which introduces complexity in the sensing and feedback circuit. More specifically, the sensed voltage is negative so an inverting operational amplifier (op-amp) is required for feedback and closed loop control.

The efficiency is poor for high gain; therefore, high gain operation cannot be achieved with this converter.

Efficiency can be as poor as 60% for a duty cycle of 0.7 or 0.3, whereas it has 90% efficiency for duty cycle of 0.5.

There is no isolation from input to output which is very critical in some applications like the power supply of gate driver of power semiconductors.

This converter is quite difficult to control. The transfer function of this converter contains a right half plane zero which introduces the control complexity.

It is still so important in spite of so many disadvantages: This converter is one of the three basic converters (buck, boost, and buck-boost). There are multitudes (a few thousand would be the exact figure) of other converters which are derived from these

basic converters. Flyback, buck-boost converter, is one of the most widely used DC-to-DC converters.

3.3.1 The equations of general inverting buck-boost converter

The inductor current ripple I_{ripple} in general is given by the Equation (3.57)

$$I_{ripple} = \frac{1}{L_1} V_{in} t_1 \tag{3.57}$$

The right half plane zero is given by the Equation (3.58)

$$f_{rhpz} = \frac{V_{out}(1-D)^2}{2\pi D L_1 I_{out}} \tag{3.58}$$

The Continuous Conduction Mode (CCM)

When the FET transistor is on, then the increasing current time is Equation (3.59)

$$t_1 = \frac{1}{f_{switch}} \frac{-V_{out} + V_f}{V_{in} + V_f - V_{out}} \tag{3.59}$$

The minimum inductor current when the FET transistor is off Equation (3.60)

$$I_{\min} = -I_{out} \frac{V_{in} + V_f - V_{out}}{V_{in}} - \frac{I_{ripple}}{2} \tag{3.60}$$

The maximum inductor current in this case is given by Equation (3.61)

$$I_{\max} = -I_{out}\frac{V_{in}+V_f-V_{out}}{V_{in}}+\frac{I_{ripple}}{2} \tag{3.61}$$

Finally, the average input current is given by Equation (3.6).

The Discontinuous Conduction Mode (DCM)

When the FET transistor is on, then the increasing current time is as follows Equation (3.62)

$$t_1 = \sqrt{-2I_{out}L_1\frac{-V_{out}+V_f}{f_{switch}V_{in}^2}} \tag{3.62}$$

When the transistor FET is off, then the decreasing current time is as follows Equation (3.63)

$$t_2 = t_1(\frac{V_{in}+V_f-V_{out}}{-V_{out}+V_f}-1) \tag{3.63}$$

In the case of FET transistor is off, no current is given by Equation (3.9), and the minimum inductor current is null.

The maximum inductor current in this case is given by the Equation (3.64)

$$I_{\max} = \frac{1}{L_1}(V_{in})t_1 \tag{3.64}$$

And the average input current is Equation (3.65)

$$I_{in,avg} = \frac{V_{out} I_{out}}{V_{in}} + \frac{V_f}{V_{in}} \frac{I_{\max}}{2} t_2 f_{switch} \tag{3.65}$$

3.3.2 The basic components of a boost converter

- **Inductor L_1**

Figure 3.25 shows the inverting Buck Boost – Inductor L_1 voltage waveforms in CCM and DCM, and Figure 3.26 shows the inverting Buck Boost – Inductor L_1 current waveforms in CCM and DCM.

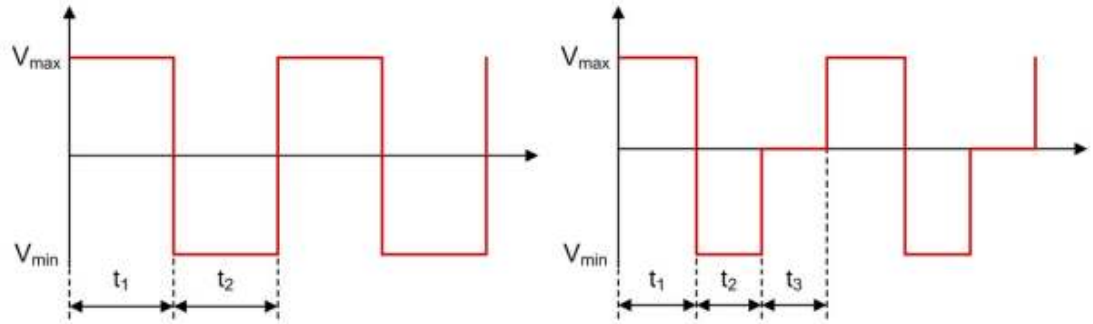


Figure 3.25 Inverting buck boost – inductor l_1 voltage waveforms in CCM, and DCM

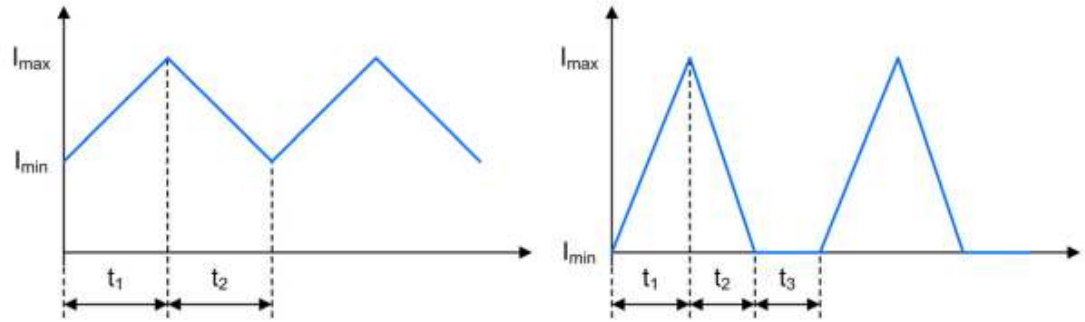


Figure 3.26 Inverting buck boost – inductor l_1 current waveforms in CCM, and DCM

The average inductor current is given by Equation (3.44), but minimum inductor voltage Equation (3.66)

$$V_{L_1,\min} = V_{out} - V_f \tag{3.66}$$

The maximum inductor voltage and the inductor voltage during time t_3 are the same as in the boost converter and is given by Equations (3.46), (3.47), respectively.

- **Transistor FET Q_1**

Figure 3.27 shows the inverting Buck Boost FET Q_1 voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

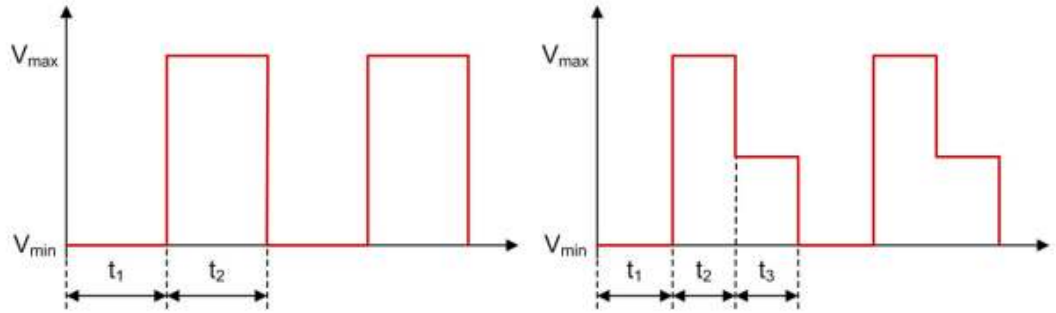


Figure 3.27 Inverting buck boost - fet q_1 voltage waveforms in CCM, DCM

Figure 3.28 shows the Inverting Buck Boost FET Q_1 current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

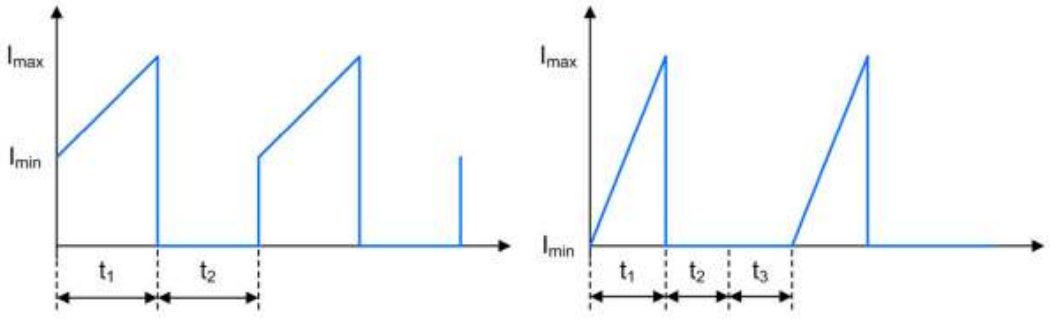


Figure 3.28 Inverting buck boost - fet q_1 current waveforms in CCM, and DCM

The average transistor current is given by Equation (3.17), and the minimum transistor voltage is null as in Equation (3.18).

The maximum transistor voltage Equation (3.67)

$$V_{Q_1,\max} = V_{in} - V_{out} + V_f \tag{3.67}$$

The FET transistor voltage during time t_3 Equation (3.68)

$$V_{Q_1,t_3} = V_{in} \tag{3.68}$$

- **Diode D_1**

Figure 3.29 shows the diode D_1 voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

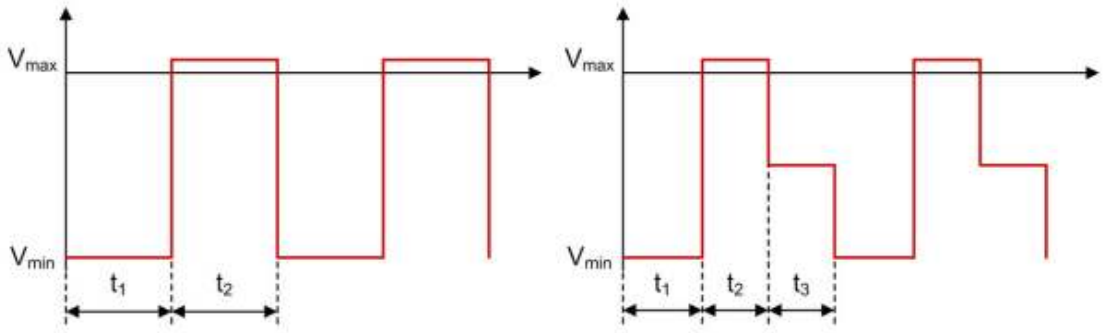


Figure 3.29 Inverting buck boost - diode d_1 voltage waveforms in CCM, and DCM

Figure 3.30 shows the diode D_1 current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

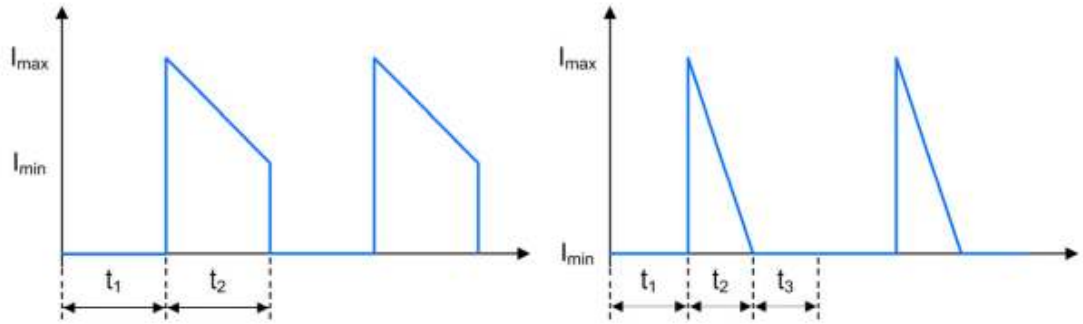


Figure 3.30 Inverting buck boost - diode d_1 current waveforms in CCM, and DCM

The average diode current is given by Equation (3.21), and the minimum diode voltage is given by Equation (3.69)

$$V_{D_1,\min} = V_{out} - V_{in} \tag{3.69}$$

The maximum FET transistor voltage is given by Equation (3.23), but the diode voltage during t_3 is given by the Equation (3.70)

$$V_{D_1,t_3} = V_{out} \tag{3.70}$$

- **Input capacitor C_i**

Figure 3.31 shows the inverting Buck-Boost input capacitor C_i voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

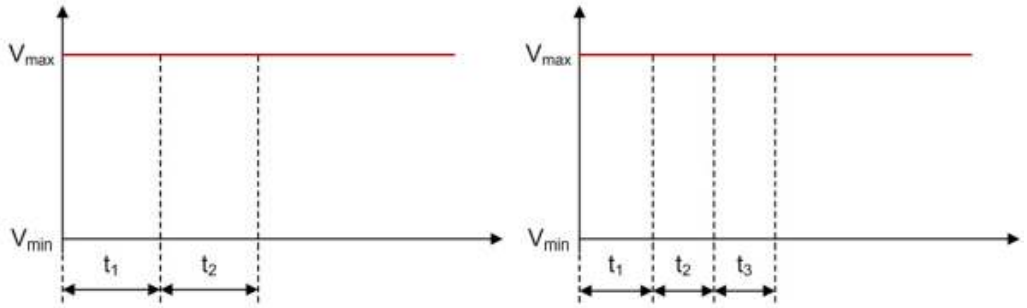


Figure 3.31 Inverting buck-boost – input capacitor c_i voltage waveforms in CCM, and DCM

Figure 3.32 shows the input capacitor C_i current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

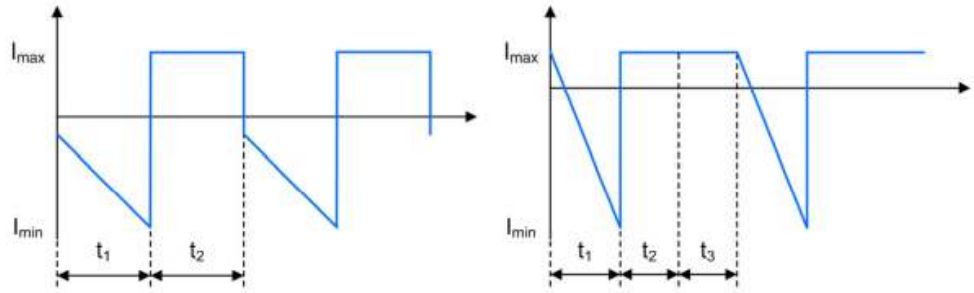


Figure 3.32 Inverting buck-boost - input capacitor c_i current waveforms in CCM, and DCM

The minimum input capacitor current during time t_1 is given by Equation (3.52), and (3.53) gives the maximum input capacitor current during t1. The average input capacitor current is null, and the input capacitor voltage is given by Equation (3.29).

- **Output capacitor C_0**

Figure 3.33 shows the inverting Buck-Boost output capacitor C_o voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

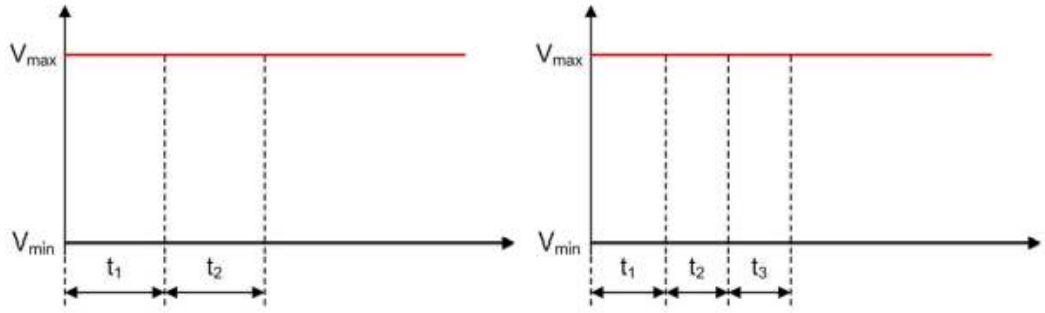


Figure 3.33 Inverting buck-boost – output capacitor c_o voltage waveforms in CCM, and DCM

Figure 3.34 shows the output capacitor C_o current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

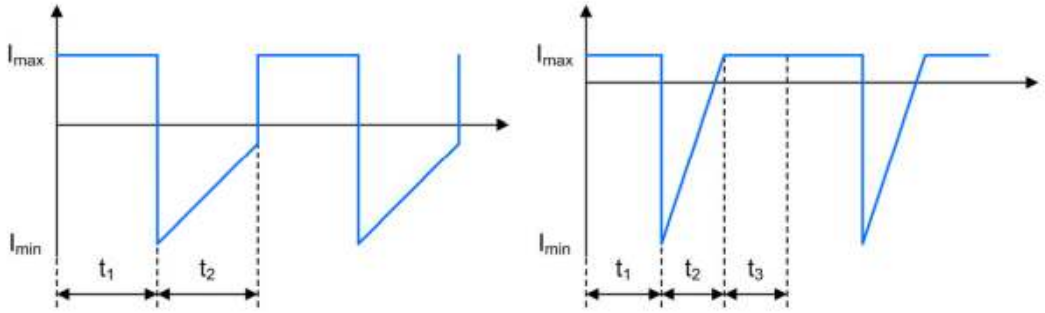


Figure 3.34 Inverting buck-boost output capacitor c_o urrent Waveforms in CCM, and DCM

The minimum output capacitor current during t_2 and t_3 Equation (3.71)

$$I_{C_o,\min},t_{2/3} = -I_{\min} - I_{out} \tag{3.71}$$

The maximum output capacitor current during t_2 and t_3 Equation (3.72)

$$I_{C_o,\max,t_{2/3}} = -I_{\max} - I_{out} \tag{3.72}$$

The average output capacitor current is given by Equation (3.73)

$$I_{C_o,avg} = 0A \tag{3.73}$$

The output capacitor voltage is given by Equation (3.33).

The buck-boost topology can either step the voltage up or down. This topology is particularly useful in battery powered applications, where the input voltage varies over time but has the disadvantage of inverting the output voltage. Another disadvantage to the buck-boost topology is that the switch does not have a ground, which complicates the drive circuit. Using only a single inductor like the buck and the boost topologies, the buck-boost inductor and EMI components are readily available.

3.4 Single-Ended Primary Inductor Converter (SEPIC)

A Single-Ended Primary Inductor Converter (SEPIC) steps up/down an input voltage to a higher/lower output voltage level Figure 3.35. The energy is transferred to the output when the FET transistor is not conducting.

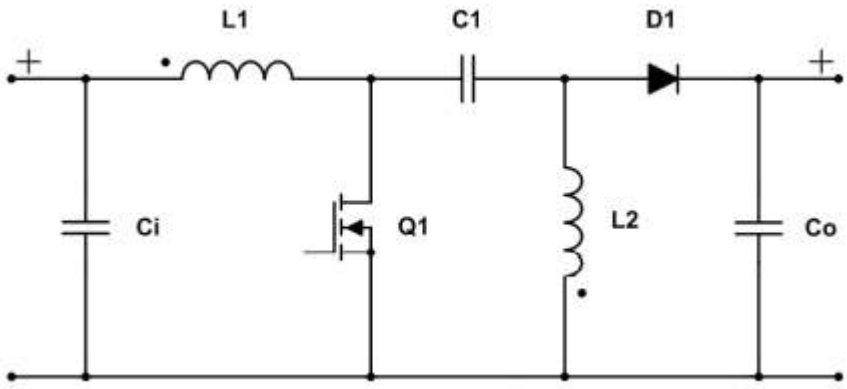


Figure 3.35 The schematic of a SEPIC dc-to-dc converter

3.4.1 SEPIC converter equation

The right half plane zero Equation (3.74)

$$f_{rhpz} = \frac{V_{out}(1-D)^2}{2\pi D^2 L_1 I_{out}} \tag{3.74}$$

- **Continuous Conduction Mode (CCM)**

When the FET transistor is on, then the increasing current time is Equation (3.75):

$$t_1 = \frac{1}{f_{switch}} \frac{V_{out} + V_f}{V_{out} + V_f + V_{in}} \tag{3.75}$$

When the FET transistor is off, then the decreasing current time is the same as in Buck converter Equation (3.3).

Inductor L_1 current ripple Equation (3.76)

$$I_{L_1,ripple} = V_{in} - \frac{t_1}{L_1} \tag{3.76}$$

Inductor L_2 current ripple Equation (3.77)

$$I_{L_2,ripple} = V_{in} - \frac{t_1}{L_2} \tag{3.77}$$

The average input current is given by Equation (3.39), but the coupling capacitor C_1 voltage ripple is given by Equation (3.78)

$$V_{C_1,ripple} = I_{in,avg} \cdot \frac{1-D}{C_1 f_{switch}} \tag{3.78}$$

• **Discontinuous Conduction Mode (DCM)**

When the FET transistor is on, then the increasing current time is Equation (3.79):

$$t_1 = \sqrt{\frac{2I_{out}L_1L_2(V_{out}+V_f)f_{switch}(L_1+L_2)}{f_{switch}V_{in}(L_1+L_2)}} \tag{3.79}$$

When the FET transistor is off, then the decreasing current time is Equation (3.80):

$$t_1 = \sqrt{\frac{2I_{out}L_1L_2(V_{out}+V_f)f_{switch}(L_1+L_2)}{(V_{out}+V_f)f_{switch}V_{in}(L_1+L_2)}} \tag{3.80}$$

In the case of the FET transistor is off, then the time t_3 Equation (3.81)

$$t_3 = \frac{1}{f_{switch}} - t_1 - t_2 \tag{3.81}$$

The average input current Equation (3.82):

$$I_{in,avg} = \frac{V_{out}+V_f}{V_{in}} I_{out} \tag{3.82}$$

Inductor L_1 ripple, and inductor L_2 ripple are the same as in CCM and given by Equations (3.76), (3.77). The coupling capacitor C_1 voltage ripple is given by Equation (3.78).

3.4.2 SEPIC converter components

. Inductor L_1in CCM & DCM.

Figure 3.36 shows the Boost – Inductor L_1 voltage waveforms in CCM and DCM, and Figure 3.37 shows the Boost – Inductor L_1 current waveforms in CCM and DCM.

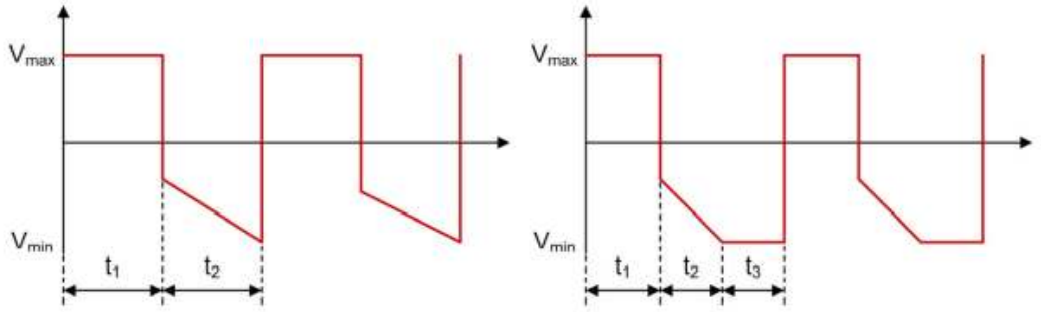


Figure 3.36 SEPIC – inductor l_1 voltage waveforms in CCM, and DCM

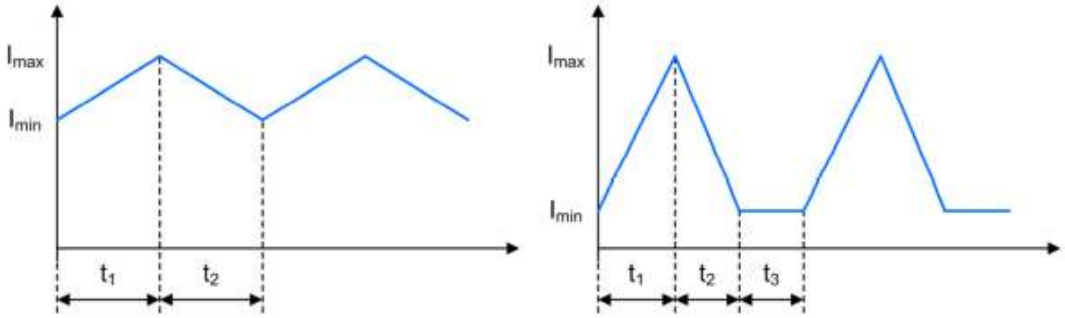


Figure 3.37 SEPIC – inductor l_1 current waveforms in CCM, and DCM

The average inductor current Equation (3.83)

$$I_{L_1,avg} = I_{in,avg} \tag{3.83}$$

The minimum inductor current Equation (3.84)

$$I_{L_1,\min} = I_{in,avg} - 0.5 I_{L_1,ripple}(t_1 + t_2) f_{switch} \tag{3.84}$$

The maximum inductor current Equation (3.85)

$$I_{L_1,\max} = I_{L_1,\min} + I_{L_1,ripple} \tag{3.85}$$

The inductor Voltage during time t_1 Equation (3.86)

$$V_{L_1,t_1} = V_{in} \tag{3.86}$$

The minimum inductor voltage during time t_2 Equation (3.87)

$$V_{L_1,\min,t_2} = -V_{out} - V_f - \frac{V_{C_1,ripple}}{2} \tag{3.87}$$

The maximum inductor voltage during time t_2 Equation (3.88)

$$V_{L_1,\max,t_2} = -V_{out} - V_f + \frac{V_{C_1,ripple}}{2} \tag{3.88}$$

The inductor voltage during time t_3 Equation (3.89)

$$V_{L_1,t_3} = 0V \tag{3.89}$$

The offset in DCM during t_3 is dependent on the input voltage and can be positive or negative.

- **Inductor L_2 in CCM & DCM.**

Figure 3.38 shows the SEPIC – Inductor L_2 voltage waveforms in CCM, and DCM. Figure 3.39 shows the Boost – Inductor L_1 current waveforms in CCM and DCM.

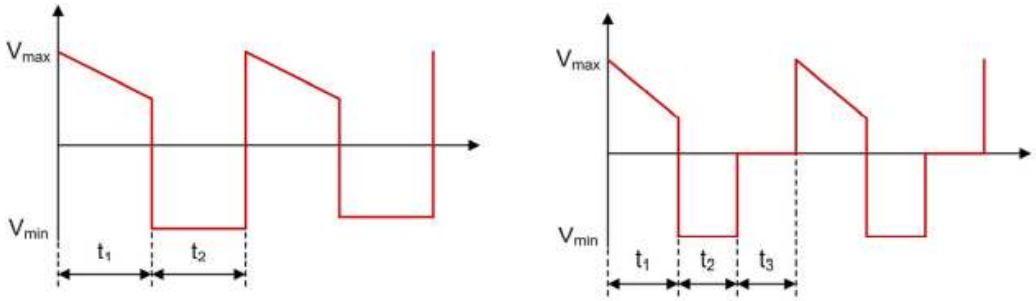


Figure 3.38 SEPIC – inductor l_2 voltage waveforms in CCM, and DCM

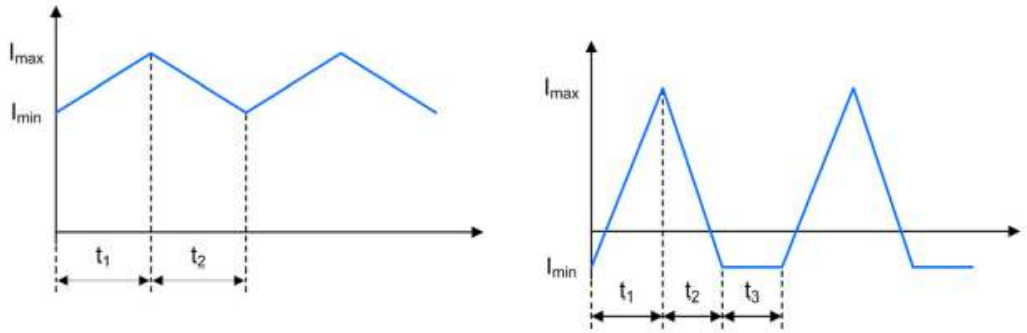


Figure 3.39 SEPIC – inductor l_2 current waveforms in CCM, and DCM

- **CCM**

The average inductor current Equation (3.90)

$$I_{L_2,avg} = I_{out} \tag{3.90}$$

The minimum inductor current Equation (3.91)

$$I_{L_2,\min} = I_{out} - 0.5 * I_{L_2,ripple} \tag{3.91}$$

The maximum inductor current Equation (3.92)

$$I_{L_2,\max} = I_{L_2,\min} + I_{L_2,ripple} \tag{3.92}$$

The inductor Voltage during time t_2 Equation (3.93)

$$V_{L_2,t_2} = -V_{out} - V_f \tag{3.93}$$

The minimum inductor voltage during t_1 Equation (3.94)

$$V_{L_2,\min,t_1} = V_{in} - \frac{V_{C_1,ripple}}{2} \tag{3.94}$$

The maximum inductor voltage during time t_2 Equation (3.95)

$$V_{L_2,\max,t_1} = V_{in} + \frac{V_{C_1,ripple}}{2} \tag{3.95}$$

The inductor voltage during time t_2 Equation (3.96)

$$V_{L_2,t_2} = -V_{out} - V_f \tag{3.96}$$

- **DCM**

The average inductor current is given by Equation (3.90), but the minimum inductor current Equation (3.97)

$$I_{L_2,\min} = -I_{L1,\min} \tag{3.97}$$

The maximum inductor current is given by Equation (3.92), and the inductor voltage during t_2 is given by (3.93).

The minimum inductor voltage during t_1 is given by Equation (3.94), and the maximum inductor voltage during t_2 and the inductor voltage during t_3 in CCM are given by Equations (2.95) and (2.96), respectively. The offset in DCM during time t3 is dependent on the input voltage and can be positive or negative.

- **FET transistor Q_1**

Figure 3.40 shows the SEPIC - FET Q_1 voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

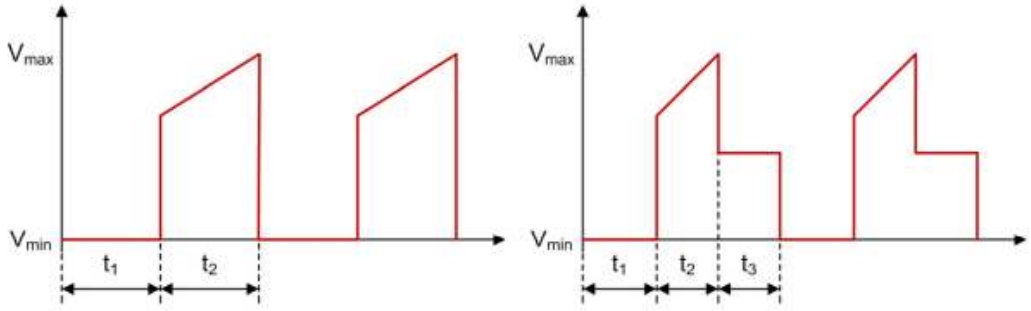


Figure 3.40 SEPIC - fet q_1 voltage waveforms in CCM, DCM

Figure 3.41 shows the SEPIC - FET Q_1 current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

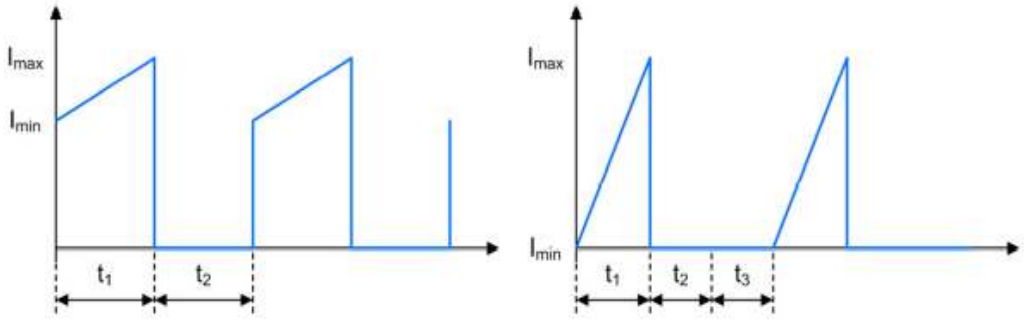


Figure 3.41 SEPIC - fet q_1 current waveforms in CCM, and DCM

The minimum FET current Equation (3.98)

$$I_{Q_1,\min} = I_{L_1,\min} + I_{L_2,\min} \tag{3.98}$$

The maximum FET current Equation (3.99)

$$I_{Q_1,\max} = I_{L_1,\max} + I_{L_2,\max} \tag{3.99}$$

The average FET transistor current Equation (3.100)

$$I_{Q_1,avg} = I_{in,avg} \tag{3.100}$$

The FET voltage during time t_1 is null, but the minimum FET voltage during t_2 Equation (3.101)

$$V_{Q_1,\min} = V_{in} + V_{out} + V_f - \frac{V_{c_1,ripple}}{2} \tag{3.101}$$

The maximum FET voltage during t_2 Equation (3.102)

$$V_{Q_1,\max} = V_{in} + V_{out} + V_f + \frac{V_{c_1,ripple}}{2} \tag{3.102}$$

The FET transistor voltage during t_3 Equation (3.103)

$$V_{Q_1,t_3} = V_{in} \tag{3.103}$$

- **Diode D_1**

Figure 3.42 shows the SEPIC diode D_1 voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

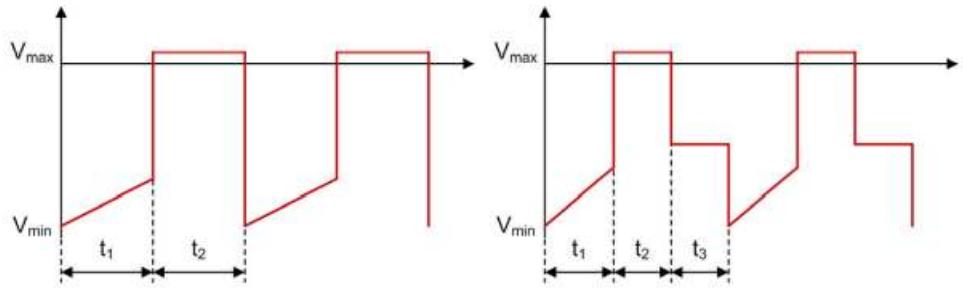


Figure 3.42 SEPIC - diode d_1 voltage waveforms in CCM, and DCM

Figure 3.43 shows theSEPIC diode D_1 current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

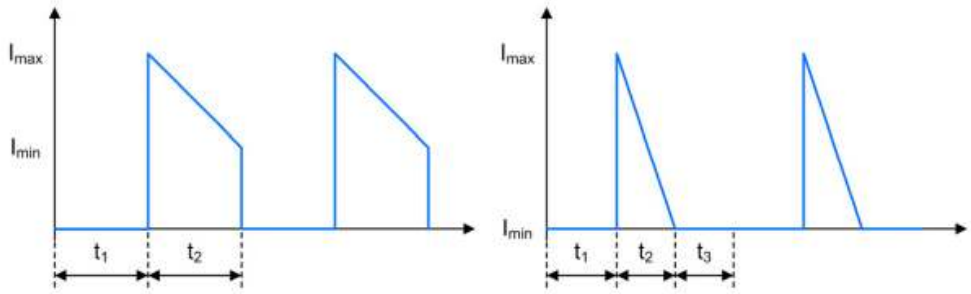


Figure 3.43 SEPIC - diode d_1 current waveforms in CCM, and DCM

The average diode current Equation (3.104)

$$I_{D_1,avg} = I_{out} \tag{3.104}$$

The minimum diode current Equation (3.105)

$$I_{D_1,\min} = I_{L_1,\min} + I_{L_2,\min} \tag{3.105}$$

The maximum diode current Equation (3.106)

$$I_{D_1,\max} = I_{L_1,\max} + I_{L_2,\max} \tag{3.106}$$

The minimum diode voltage during t_1 Equation (3.107)

$$V_{D_1,\min,t_1} = -V_{in} - V_{out} - \frac{V_{c_1,ripple}}{2} \tag{3.107}$$

The maximum diode voltage during t_1 Equation (3.107):

$$V_{D_1,\max,t_1} = -V_{in} - V_{out} + \frac{V_{c_1,ripple}}{2} \tag{3.107}$$

The diode voltage during t_2 Equation (3.108):

$$V_{D_1,t_2} = V_f \tag{3.108}$$

The diode voltage during t_3 Equation (3.109):

$$V_{D_1,t_3} = -V_{out} \tag{3.109}$$

- **Coupling capacitor C_i**

Figure 3.44 shows the SEPIC input capacitor C_i voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

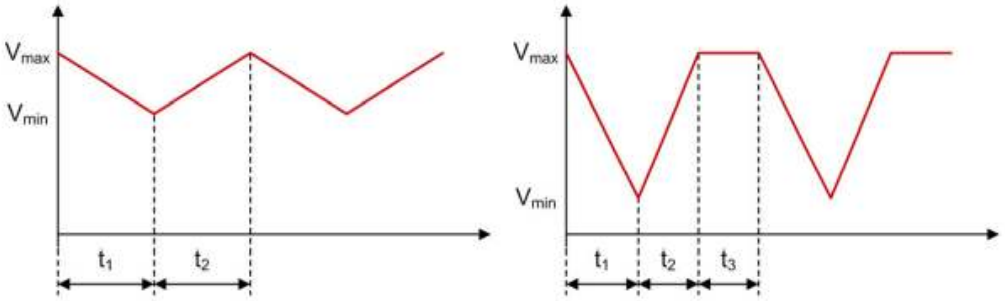


Figure 3.44 SEPIC – input capacitor c_i voltage waveforms in CCM, and DCM

Figure 3.45 shows the SEPIC input capacitor C_i current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

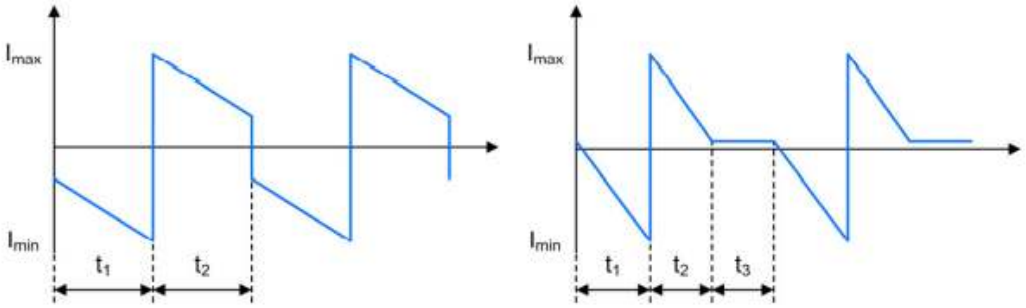


Figure 3.45 SEPIC - input capacitor c_i current waveforms in CCM, and DCM

The minimum coupling capacitor current during t_1 Equation (3.110)

$$I_{C_1,\min,t_1} = -I_{fet,\max} + I_{L_1,\max} \tag{3.110}$$

The maximum coupling capacitor current during t_1 Equation (3.111)

$$I_{C_1,\max,t_1} = -I_{fet,\max} + I_{L_1,\min} \tag{3.111}$$

The minimum coupling capacitor current during t_2 Equation (3.112)

$$I_{C_1,\min,t_2} = I_{L_1,\min} \tag{3.112}$$

The maximum coupling capacitor current during t_2 Equation (3.113)

$$I_{C_1,\max,t_1} = I_{L_1,\max} \tag{3.113}$$

The coupling capacitor current during t_3 Equation (3.114)

$$I_{C_1,t_3} = I_{L_1,\min} \tag{3.114}$$

The average coupling capacitor current is null, and the minimum coupling capacitor voltage Equation (3.115)

$$V_{C_1,\min} = V_{in} - \frac{V_{c_1,ripple}}{2} \tag{3.115}$$

The maximum coupling capacitor voltage Equation (3.116)

$$V_{C_1,\max} = V_{in} + \frac{V_{c_1,ripple}}{2} \tag{3.116}$$

The coupling capacitor voltage during t_3 Equation (3.117)

$$V_{C_1,t_3} = V_{in} \tag{3.117}$$

- **Output capacitor C_0**

Figure 3.46 shows the SEPIC output capacitor C_o voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

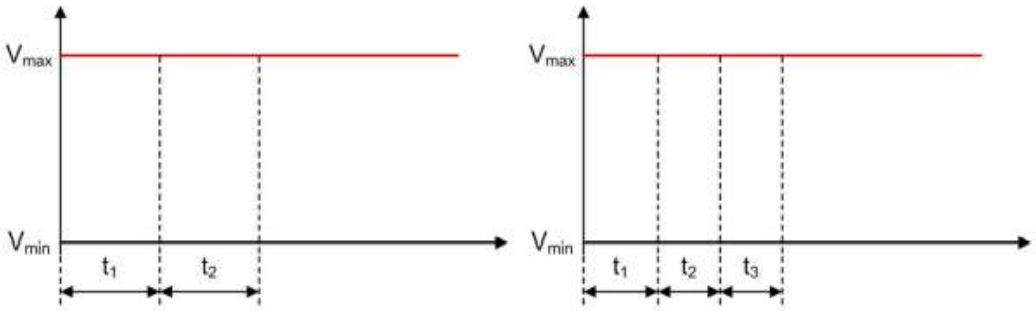


Figure 3.46 SEPIC – output capacitor c_o voltage waveforms in CCM, and DCM

Figure 3.47 shows the SEPIC output capacitor C_o current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

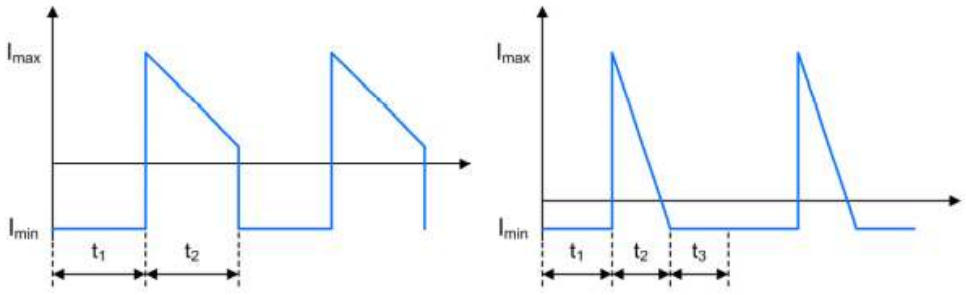


Figure 3.47 SEPIC - output capacitor c_o current waveforms in CCM, and DCM

The output capacitor current during t_1 Equation (3.118)

$$I_{C_o,t_1} = -I_{out} \tag{3.118}$$

The minimum output capacitor current during time interval t_2 and t_3 Equation (3.119)

$$I_{C_o,\min,t_{2/3}} = I_{L_1,\min} + I_{L_2,\min} - I_{out} \tag{3.119}$$

The maximum output capacitor current during time interval t_2 and t_3 Equation (3.120)

$$I_{C_o,\max,t_{2/3}} = I_{L_1,\max} + I_{L_2,\max} - I_{out} \tag{3.120}$$

The average output capacitor current is null, and Output capacitor voltage is V_{out}

The SEPIC and Ćuk topologies both use capacitors for energy storage in addition to two inductors. The two inductors can be either separate inductors or a single component in the form of a coupled inductor. Both topologies are similar to the buck-boost topology in that they can step-up or step-down the input voltage, making them ideal for battery applications.

The SEPIC has the additional advantage over both the Ćuk and the buck-boost in that its output is non-inverting. An advantage to the SEPIC/ Ćuk topologies is that the capacitor can offer some limited isolation. Catalog coupled inductors are available for the SEPIC and Ćuk topologies, and custom inductors are readily available for special needs.

4. TOPOLOGIES FOR SWITCHED MODE POWER SUPPLIES ISOLATED SWITCHING REGULATORS

The section discusses in detail the popular topologies of power converters: flyback, forward, and bridge. For each of those topologies, several areas of application are indicated. Also, explanatory diagrams and comments are presented.

When it comes to choosing a power stage circuit, many people are primarily interested in the output power. This criterion is, of course, very important, but it is not the only one. In addition to the output power, the input and output voltages, output current, type of load, required energy efficiency, weight and size, and isolated or non-isolated converter are important.

A forward converter is a switch-mode power supply circuit that transfers the energy from the primary to the secondary while the switching element is "on," which is the opposite of a flyback converter.

Forward and flyback converters are the two commonly used topologies used to either increase or decrease DC voltages, or convert a single voltage to multiple DC output voltages. A typical forward converter consists of:

- A transformer that is either a step-up or step-down with a single or multiple secondary windings. The type used depends on the available input voltage and desired output voltage. It also provides isolation between the load and the input voltage.
- A transistor, such as a MOSFET, which acts as a switching device.
- Diodes
- Capacitors
- Inductors

Energy is passed directly through the transformer during the transistor's conduction phase. The output voltage is determined by the input voltage, the output voltage, the

transformer turns ratio, and the duty cycle. The two commonly used topologies are the single switch, and two-switch forward converters.

4.1 The Flyback Converter

Using a flyback and a forward converter is quite common at power levels less than 1 kW. One of its advantages is that its circuit is quite simple (the schematic is shown in Figure 4.1). In such a converter, the key element is the transformer, although in this case it plays the role of an energy storage device and acts as a choke - with a closed key, the secondary winding gives off energy to the load, which is stored with an open key when the primary winding is connected to the network.

In this configuration, galvanic isolation is provided between the primary and secondary circuits. Flyback converter is convenient whenever a high output voltage is required at a relatively low current. Of course, this circuit can also be used at low voltages and high currents, but they are characterized by high current ripples and peak currents. Therefore, high requirements are placed on the filter components, which increases their cost. The voltage ripple is also large, so it is better to use an output smoothing filteras well.

At a duty cycle of 50%, the amplitude of the current ripple through the output capacitor is approximately 1.6 times greater than the rectified load current. So, the equivalent series resistance (ESR) of this capacitor must be significantly low. This means that for reliable operation, up to 5 electrolytic capacitors should be connected in parallel or expensive ceramic capacitors should be used. However, most likely, at least one electrolytic capacitor must be used, and its resistance should be small enough to ensure the converter stability. Therefore, at high output currents, for example, 5 V, 10 A, PP should be preferred.

The transformer primary winding leakage inductance must be as small as possible. When the switch is open, energy is stored within the inductance and is not transferred to the secondary winding. While, when the switch is closed, an overvoltage surges

present themselves. Therefore, a switch with an increased maximum allowable voltage should be used along with snubber chains, which, in turn, reduce the energy efficiency of the converter.

Another drawback of the flyback converter is that the ratio of the peak current to its average value is very much larger than in other topologies. This means you have to choose a power switch, whose maximum allowable current is greater than in other converters, which increases its cost. The switch current in the flyback converter is about 1.5 to 2 times greater than in the PP and half-bridge converter. The current in the rectifier diode is 3 to 4 times greater than the average current.

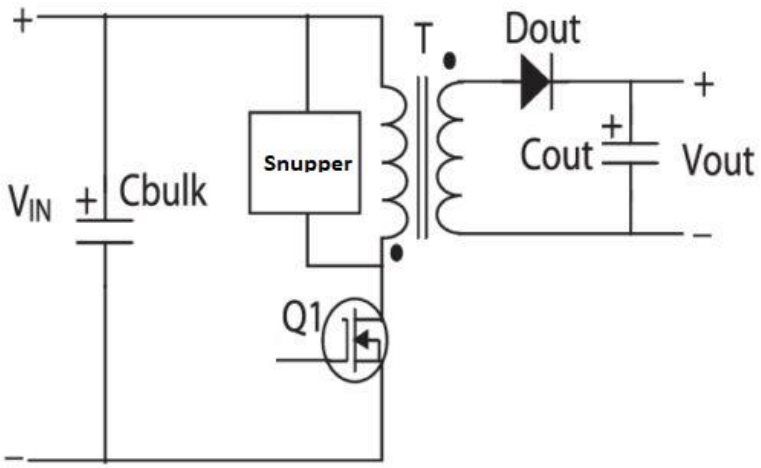


Figure 4.1 The flyback converter schematic

4.1.1 General flyback converter equation

The secondary Inductance Equation (4.1)

$$L_s = \frac{L_p}{(\frac{n_p}{n_s})^2} \tag{4.1}$$

The primary Current Ripple Equation (4.2)

$$I_{ripple} = \frac{1}{L_p} V_{in} t_1 \tag{4.2}$$

The right Half Plane Zero Equation (4.3)

$$f_{rhpz} = \frac{V_{out}(1-D)^2}{2\pi D L_s I_{out}} \tag{4.3}$$

Continuous Conduction Mode (CCM)

When the FET transistor is on, then the increasing current time is Equation (4.4)

$$t_1 = \frac{1}{f_{switch}} (V_{out} + V_f) \frac{\frac{n_p}{n_s}}{V_{in} + (V_{out} + V_f)\frac{n_p}{n_s}} \tag{4.4}$$

When the FET transistor is off, then the decreasing current time is the same as in Buck converter Equation (3.3).

The minimum primary current Equation (4.5)

$$I_{pre,\min} = \frac{(V_{out} + V_f) I_{out}}{V_{in} f_{switch} t_1} - \frac{I_{ripple}}{2} \tag{4.5}$$

The maximum primary current Equation (4.6)

$$I_{pri,\max} = I_{pri,\min} + I_{ripple} \tag{4.6}$$

The average input current Equation (4.7)

$$I_{in,avg} = I_{out} \frac{V_{out} + V_f}{V_{in}} \tag{4.7}$$

The minimum secondary current Equation (4.8)

$$I_{\text{sec,min}} = I_{pri,\text{min}} n_p / n_s \tag{4.8}$$

The maximum secondary current Equation (4.9)

$$I_{\text{sec,max}} = (I_{pri,\text{min}} + I_{ripple}) n_p / n_s \tag{4.9}$$

Discontinuous Conduction Mode (DCM)

When the FET transistor is on, then the increasing current time is Equation (4.10)

$$t_1 = \sqrt{2 I_{out} L_p \frac{V_{out} + V_f}{f_{switch} V_{in}^{\ 2}}} \tag{4.10}$$

When the FET transistor is off, then the decreasing current time is Equation (4.11)

$$t_2 = t_1 \left(\frac{V_{in} + (V_{out} + V_f) \frac{n_p}{n_s}}{\frac{n_p}{n_s} (V_{out} + V_f)} - 1 \right) \tag{4.11}$$

In the case of the FET transistor is off, no current flows through the circuit, time t_3 is given by Equation (3.9), and the minimum primary current is null, but the maximum primary current is Equation (4.12)

$$I_{pri,\max} = I_{ripple} \tag{4.12}$$

The average input current is given by Equation (4.7), but the minimum secondary current is null.

The maximum secondary current Equation (4.13)

$$I_{\sec,\max} = I_{pri,\max} n_p / n_s \tag{4.13}$$

The transition mode Equation (4.14):

The average input current

$$I_{in,avg} = \frac{(V_{out} + V_f) I_{out}}{V_{in}} \tag{4.14}$$

The switching frequency Equation (4.15)

$$f_{switch,transition} = \frac{V_{in}}{2(\frac{\sqrt{8} V_{in}}{\frac{n_p}{n_s} \pi V_{out}} + 1)^2 I_{in} L_p} \tag{4.15}$$

When the FET transistor is on, then the increasing current time is Equation (4.16)

$$t_1 = \frac{2 I_{in,avg} L_p V_{in}}{V_{in}} [(\frac{\sqrt{8} V_{in}}{\frac{n_p}{n_s} \pi V_{out}} + 1)] \tag{4.16}$$

When the FET transistor is off, then the decreasing current time is Equation (4.17)

$$t_2 = -t_1 + \frac{1}{f_{switch,transition}} \tag{4.17}$$

In the case of the minimum primary current and minimum secondary current are null; and maximum primary current is given by Equation (4.12).

The maximum secondary current Equation (4.18)

$$I_{\text{sec,max}} = I_{pri,\max} n_p / n_s \tag{4.18}$$

4.1.2 Basic components of the flyback converter

- **Primary side inductor N_p in CCM, DCM and Transition Mode**

Figure 4.2 shows the Flyback - primary side inductor Np voltage waveforms in CCM, DCM and transition mode during t_1, t_2, and t_3.

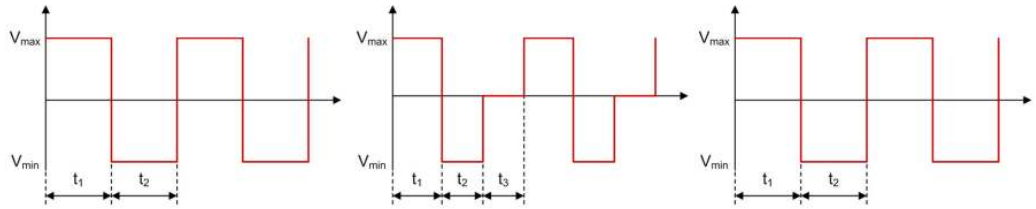


Figure 4.2 Flyback - primary side inductor np voltage waveforms in CCM, DCM and Transition Mode

Figure 4.3 shows the Flyback - primary side inductor Np current waveforms in CCM, DCM and transition mode during t_1, t_2, and t_3.

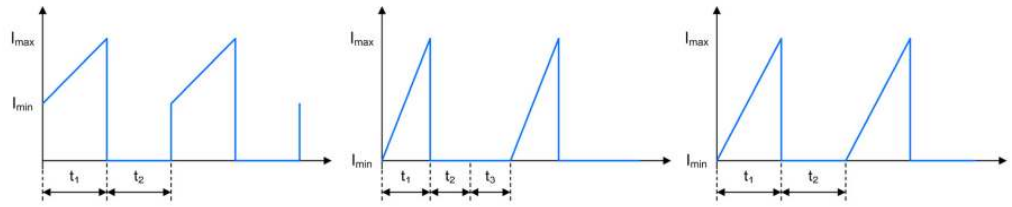


Figure 4.3 Flyback - primary side inductor np current waveforms in CCM, DCM and Transition Mode

The average primary current of inductor Equation (4.19)

$$I_{N_p,avg} = \frac{(I_{pri,\min} + I_{pri,\max})}{2} t_1 f_{switch} \tag{4.19}$$

The minimum primary current of inductor Equation (4.20)

$$I_{N_p,\min} = I_{pri,\min} \tag{4.20}$$

The maximum primary current of inductor Equation (4.21)

$$I_{N_p,\max} = I_{pri,\max} \tag{4.21}$$

The minimum primary voltage of inductor Equation (4.22)

$$V_{N_p,\min} = -(V_{out} + V_f)\frac{n_p}{n_s} \tag{4.22}$$

The maximum primary voltage of inductor Equation (4.23)

$$V_{N_p,\max} = V_{in} \tag{4.23}$$

The primary voltage of the inductor in the time t_3 is null.

- **FET Transistor Q_1**

Figure 4.4 shows the Flyback - FET Q1 voltage waveforms in CCM, DCM and Transition Mode.

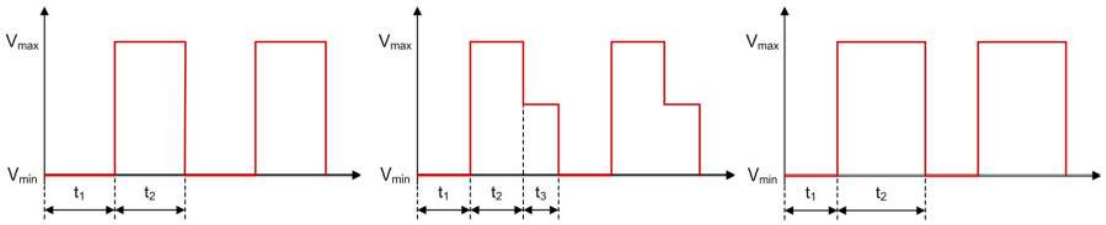


Figure 4.4 Flyback - fet q_1 voltage waveforms in CCM, DCM and transition mode

Figure 4.5 shows Flyback - FET Q1 current signals in CCM, DCM and Transition Mode.

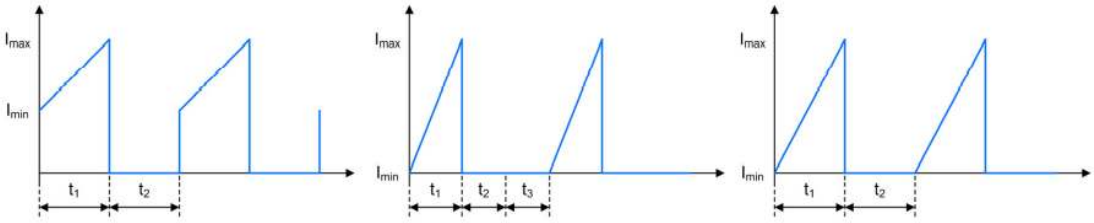


Figure 4.5 Flyback - fet q_1 current waveforms in CCM, DCM and transition mode

The average FET current Equation (4.24)

$$I_{Q_1,avg} = I_{N_p,avg} \tag{4.24}$$

The minimum FET current Equation (4.25)

$$I_{Q_1,\min} = I_{pri,\min} \tag{4.25}$$

The maximum FET transistor current Equation (4.26)

$$I_{Q_1,\max} = I_{pri,\max} \tag{4.26}$$

The minimum FET voltage is null, but the maximum FET voltage is Equation (4.27)

$$V_{Q_1,\max} = V_{in} + (V_{out} + V_f)\frac{n_p}{n_s} \tag{4.27}$$

The FET transistor voltage during time t_3 Equation (4.28)

$$V_{Q_1,t_3} = V_{in} \tag{4.28}$$

- **Diode D_1**

Figure 4.6 shows the diode D_1 voltage waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and transition mode.

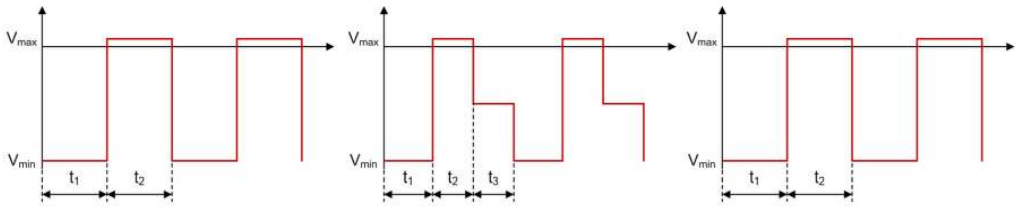


Figure 4.6 Flyback - diode d_1 voltage waveforms in CCM, DCM and transition Mode

Figure 4.7 shows the diode D_1 current waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and transition mode.

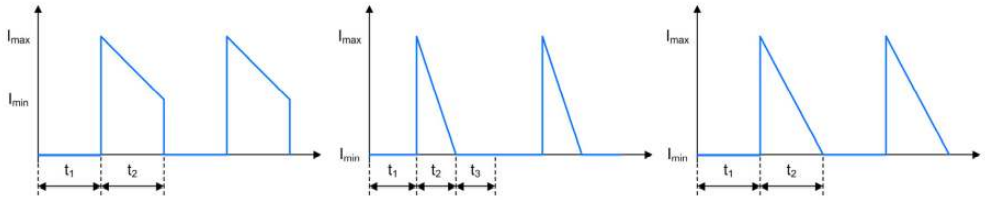


Figure 4.7 Flyback - diode d_1 current waveforms in CCM, DCM and transition mode

The average diode current is Equation (4.29)

$$I_{D_1,avg} = I_{N_s,avg} \tag{4.29}$$

The minimum current of diode is given by Equation (4.30)

$$I_{D_1,\min} = I_{\sec,\min} \tag{4.30}$$

The maximum current of diode Equation (4.31)

$$I_{D_1,\max} = I_{\sec,\max} \tag{4.31}$$

The minimum diode voltage Equation (4.32)

$$V_{D_1,\min} = -\frac{n_s}{n_p} V_{in} - V_{out} \tag{4.32}$$

The maximum voltage of diode Equation (4.33)

$$V_{D_1,\max} = V_f \tag{4.33}$$

The diode voltage during t_3 Equation (4.34)

$$V_{D_1,t_3} = -V_{out} \tag{4.34}$$

- **Input capacitor C_i**

Figure 4.8 shows the input capacitor C_i voltage waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and transition mode.

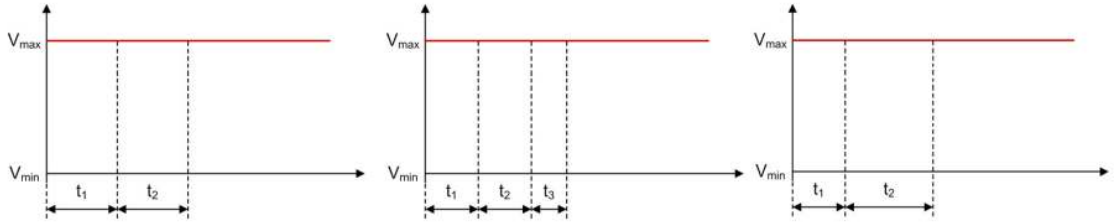


Figure 4.8 Flyback – input capacitor c_i voltage waveforms in CCM, DCM, and transition mode

Figure 4.9 shows the input capacitor C_i current waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and transition mode.

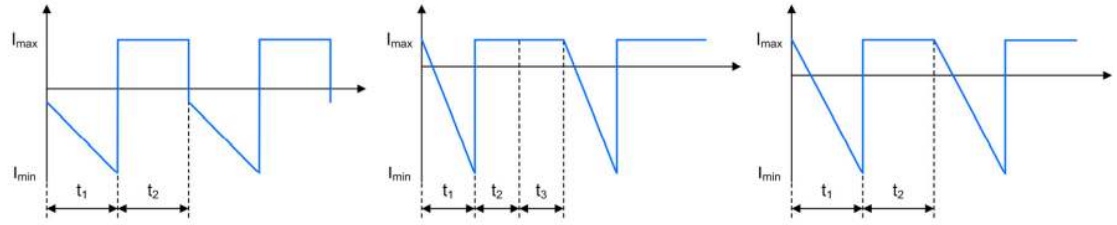


Figure 4.9 Flyback- input capacitor c_i current waveforms in CCM, and DCM

The minimum input capacitor current during t_1 Equation (4.35)

$$I_{C_i,\min,t_1} = -I_{pri,\max} + I_{in,avg} \tag{4.35}$$

The maximum input capacitor current during t_1 Equation (4.36):

$$I_{C_i,\max,t_1} = -I_{\min} + I_{in,avg} \tag{4.36}$$

The input capacitor current during t_2 and t_3 Equation (4.37):

$$I_{C_i,\max,t_{2/3}} = I_{in,avg} \tag{4.37}$$

The average input capacitor current is null, and input capacitor voltage is equal to input voltage.

- **Output capacitor C_0**

Figure 4.10 shows the Flyback - Output Capacitor Co voltage waveforms in CCM, DCM and transition Mode.

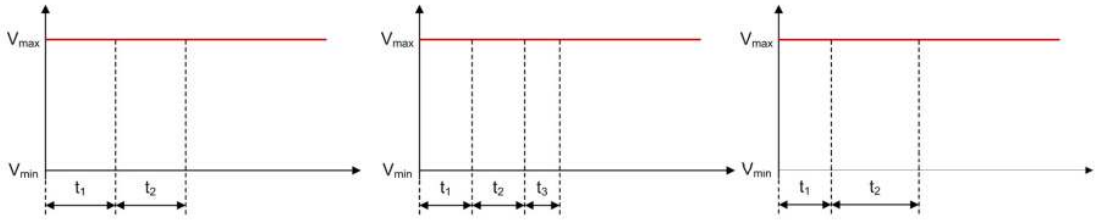


Figure 4.10 Flyback – output capacitor c_o voltage waveforms in CCM, DCM, and transition Mode

(Figure 4.11) shows the output capacitor C_o current waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and synchronous forced PWM.

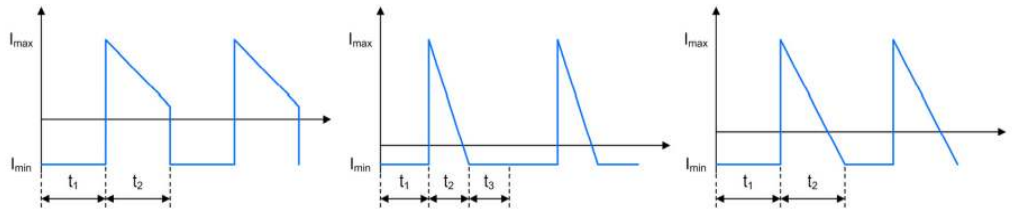


Figure 4.11 Flyback - output capacitor c_o current waveforms in CCM, DCM, and transition Mode

The output current of capacitor during time t_1 Equation (4.38)

$$I_{C_o,t_1} = -I_{out} \tag{4.38}$$

The minimum output current of capacitor during time interval t_2 to t_3 Equation (4.39)

$$I_{C_o,\min,t_{2/3}} = I_{\sec,\min} - I_{out} \tag{4.39}$$

The maximum output current of capacitor during time interval t_2 to t_3 Equation (4.40):

$$I_{C_o,\max,t_{2/3}} = I_{\sec,\max} - I_{out} \tag{4.40}$$

The average output current of capacitor Equation (4.41)

$$I_{C_o,avg} = 0A \tag{4.41}$$

The output capacitor voltage is Equation (4.42)

$$V_{C_o} = V_{out} \tag{4.42}$$

4.2 The Single Switch Forward Converter

A single-switch forward regulator converts an input voltage to a higher/lower, positive/negative output voltage. The energy is transferred to the output when the FET transistor is conducting. The turns ratio between Np and Nd is assumed to be 1:1.

- Advantages of a single-switch forward converter:

- Simple construction and operation.
- Low input capacitor ripple current.
- Lower current on the secondary diodes.

- Disadvantages:

- Requires a high transistor rating (twice the input voltage).
- Requirement for an active snubbers circuits for resetting the transformer core.
- Higher conduction losses.
- Bigger transformer.

Figure 4.12 shows the circuit of a single-switch forward converter

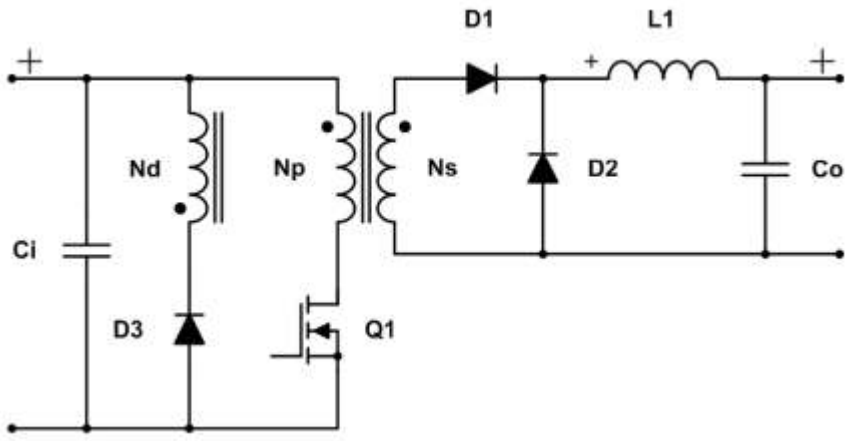


Figure 4.12 Circuit schematic of a single-switch forward converter

4.2.1 General single switch forward converter equation

The secondary side inductance Equation (4.43)

$$L_s = \frac{L_p}{(\frac{n_p}{n_s})^2} \tag{4.43}$$

The current ripple of inductor Equation (4.44)

$$I_{ripple} = \frac{1}{L_1}(V_{in}\frac{n_s}{n_p} - V_f - V_{out})t_1 \tag{4.44}$$

Continuous Conduction Mode (CCM)

When the FET transistor is on, then the increasing current time is Equation (4.45)

$$t_1 = \frac{1}{f_{switch}}\frac{(V_{out} + V_f)}{V_{in}\frac{n_p}{n_s}} \tag{4.45}$$

The demagnetization time $t_d = t_1$, when the FET transistor is off, then the decreasing current time is Equation (4.46)

$$t_2 = \frac{1}{f_{switch}} - t_1 \tag{4.46}$$

The magnetization current Equation (4.47)

$$I_{mag} = \frac{V_{in} t_1}{L_p} \tag{4.47}$$

The minimum primary current Equation (4.48)

$$I_{pre,\min} = I_{\sec,\min} \frac{n_s}{n_p} \tag{4.48}$$

The maximum primary current is given by Equation (4.49)

$$I_{pri,\max} = I_{\sec,\max} \frac{n_s}{n_p} + I_{mag} \tag{4.49}$$

The average input current Equation (4.50)

$$I_{in,avg} = I_{out} \frac{V_{out} + V_f}{V_{in}} \tag{4.50}$$

The minimum secondary current Equation (4.51)

$$I_{\sec,\min} = I_{out} - 0.5 * I_{ripple} \tag{4.51}$$

The maximum secondary current Equation (4.52)

$$I_{\sec,\max} = I_{out} + 0.5 * I_{ripple} \tag{4.52}$$

Discontinuous Conduction Mode (DCM)

When the FET transistor is on, then the increasing current time is Equation (4.53)

$$t_1 = \sqrt{2I_{out}L_1 \frac{V_{out}+V_f}{f_{switch}(V_{in}\frac{n_s}{n_p} - V_f - V_{out})V_{in}\frac{n_s}{n_p}}} \tag{4.53}$$

Demagnetization time is the same in the case of continuous conduction mode, when the FET transistor is off, then the decreasing current time is Equation (4.54)

$$t_2 = t_1(\frac{V_{in}\frac{n_p}{n_s}}{(V_{out}+V_f)} - 1) \tag{4.54}$$

In the case of the FET transistor is off, no current flows in the circuit and time t_3 in condition $t_2 > t_d$ Equation (4.55)

$$t_3 = \frac{1}{f_{switch}} - t_1 - t_2 \tag{4.55}$$

In the case of the FET transistor is off, no current flows in the circuit and time t_3 in condition $t_d \geq t_2$ Equation (4.56)

$$t_3 = \frac{1}{f_{switch}} - t_1 - t_d \tag{4.56}$$

The maximum primary current is given by Equation (4.57)

$$I_{pri,\max} = I_{\sec,\max}\frac{n_s}{n_p} + I_{mag} \tag{4.57}$$

Both the minimum secondary and currents are null.

The maximum secondary current Equation (4.58)

$$I_{\text{sec,max}} = I_{ripple} \tag{4.58}$$

The average input current Equation (4.59)

$$I_{in,avg} = \frac{(V_{out} + V_f)I_{out}}{V_{in}} \tag{4.59}$$

4.2.2 The basic components of a single-switch forward converter

- **Secondary side transformer winding Ns**

❖ Continuous and discontinuos conduction mode

Figure 4.13 shows the single switch forward - secondary side transformer winding N_s voltage waveforms in CCM and DCM.

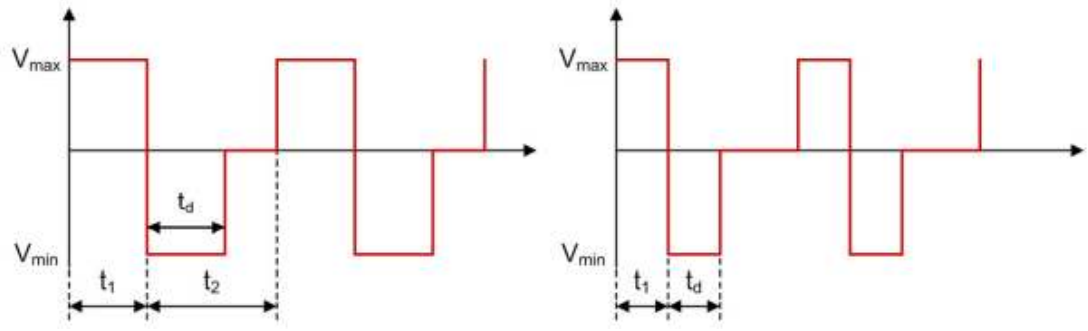


Figure 4.13 Single switch forward - secondary side transformer winding n_s voltage waveforms in CCM, and DCM

Figure 4.14 shows the single switch forward - secondary side transformer winding N_s current waveforms in CCM and DCM.

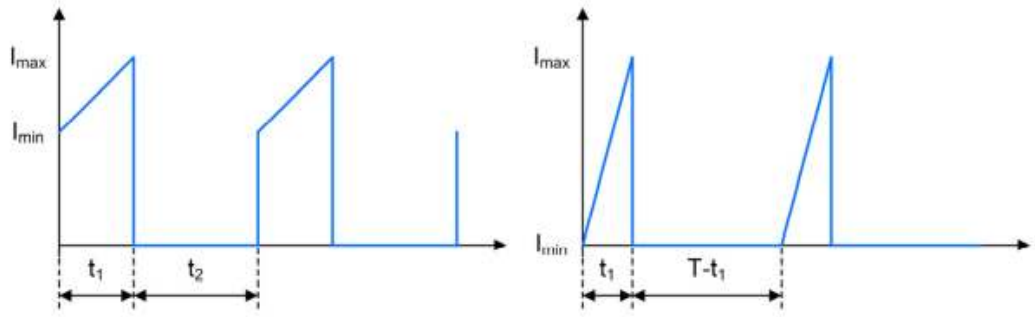


Figure 4.14 Single switch forward - secondary side transformer winding n_s current waveforms in CCM, and DCM

The average secondary current of transformer Equation (4.60)

$$I_{N_s,avg} = \frac{(I_{\text{sec,min}} + I_{\text{sec,max}})}{2} t_1 f_{switch} \tag{4.60}$$

The minimum secondary current of transformer Equation (4.61)

$$I_{N_s,\text{min}} = I_{\text{sec,min}} \tag{4.61}$$

The maximum secondary current of transformer Equation (4.62)

$$I_{N_s,\text{max}} = I_{\text{sec,max}} \tag{4.62}$$

The minimum secondary voltage of transformer Equation (4.63)

$$V_{N_s,\text{min}} = -V_{in} \frac{n_p}{n_s} - V_f \tag{4.63}$$

The maximum secondary voltage of transformer Equation (4.64)

$$V_{N_{\text{ثانوي}},\max} = V_{in}\frac{n_s}{n_p} \tag{4.64}$$

The secondary transformer voltage after t_d, and the secondary transformer voltage during t_3 are null.

- **FET transistor Q_1**

Figure 4.15 shows the Single Switch Forward - FET Q1 voltage waveforms in CCM, and DCM.

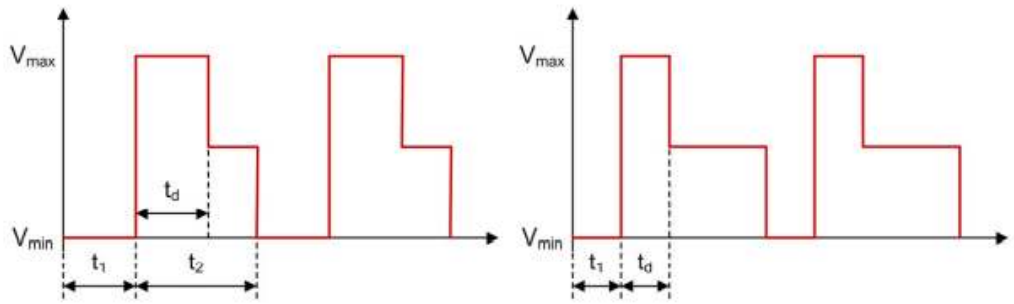


Figure 4.15 Single switch forward - fet q_1 voltage waveforms in CCM, and DCM

Figure 4.16 shows Single Switch Forward-FET Q1 current signals in CCM, and DCM.

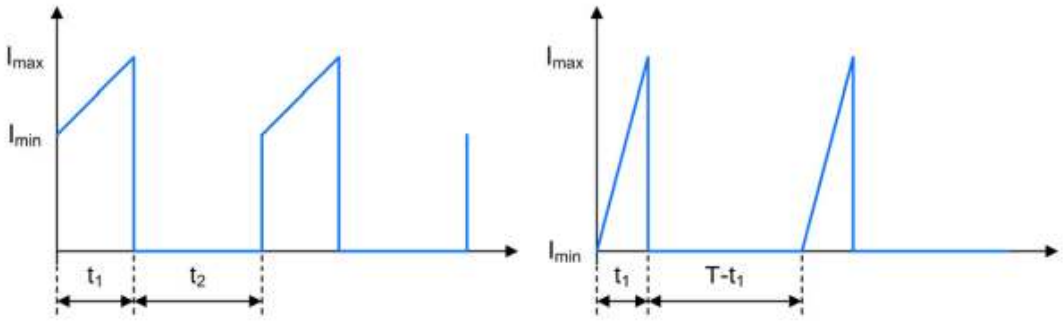


Figure 4.16 Single switch forward - fet q_1 current waveforms in CCM, and DCM

The average FET transistor current Equation (4.65)

$$I_{Q_1,avg} = I_{N_p,avg} \tag{4.65}$$

Minimum FET transistor current Equation (4.66)

$$I_{Q_1,\min} = I_{pri,\min} \tag{4.66}$$

The maximum FET transistor current Equation (4.67)

$$I_{Q_1,\max} = I_{pri,\max} \tag{4.67}$$

The minimum FET transistor voltage is null, but the maximum FET transistor voltage Equation (4.68)

$$V_{Q_1,\max} = 2*V_{in} + V_f \tag{4.68}$$

The FET transistor voltage during time t_3 Equation (4.69)

$$V_{Q_1,t_3} = V_{in} \tag{4.69}$$

- **Demagnetization Diode D_3**

Figure 4.17 shows the Single-Switch Forward-Demagnetization Diode D_3 voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

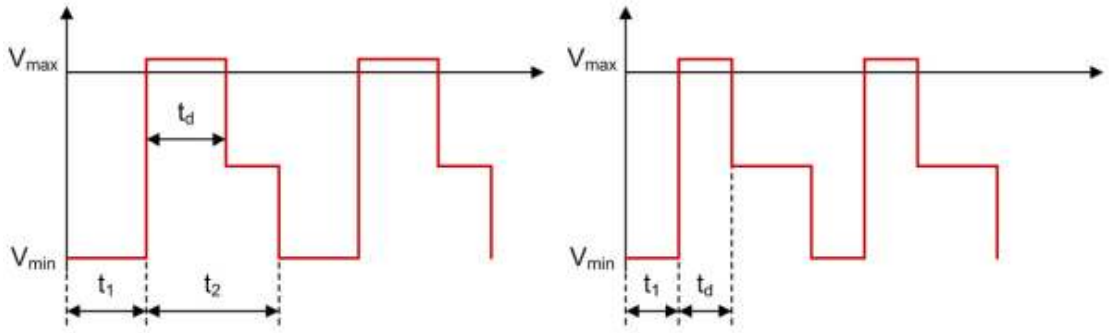


Figure 4.17 Single switch forward - demagnetization diode d_3 voltage waveforms in CCM, and DCM

Figure 4.18 shows the Single Switch Forward - Demagnetization Diode D_3 current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

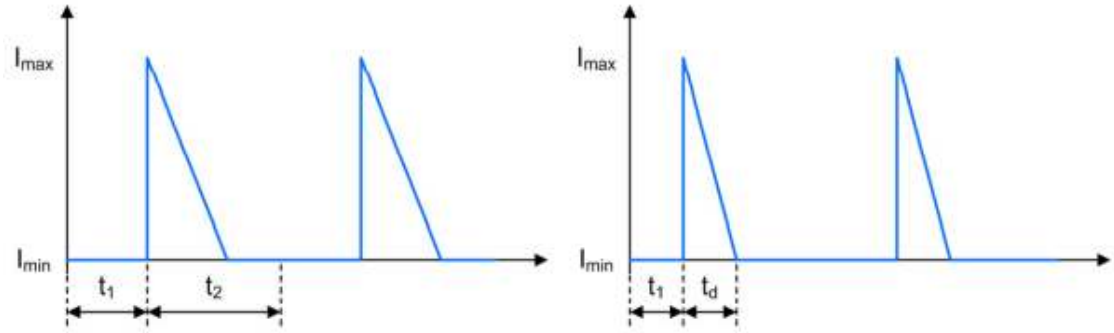


Figure 4.18 Single switch forward - demagnetization diode d_3 current waveforms in CCM, and DCM

The average current of demagnetization diode Equation (4.70)

$$I_{D_3,avg} = \frac{I_{mag}}{2} t_d f_{switch} \tag{4.70}$$

The minimum current of demagnetization diode is null, but maximum current of demagnetization diode Equation (4.71)

$$I_{D_3,\max} = I_{mag} \tag{4.71}$$

The minimum voltage of demagnetization diode Equation (4.72)

$$V_{D_3,\min} = -2V_{in} \tag{4.72}$$

The maximum voltage of demagnetization diode Equation (4.73)

$$V_{D_3,\max} = V_f \tag{4.73}$$

The voltage of demagnetization diode during t_d Equation (4.74)

$$V_{D_3,t_d} = -V_{in} \tag{4.74}$$

The voltage of demagnetization diode during t_3 Equation (4.75)

$$V_{D_3,t_3} = -V_{in} \tag{4.75}$$

- **Rectifier Diode D_1**

Figure 4.19 shows the Single-Switch Forward-Rectifier Diode D_1 voltage waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

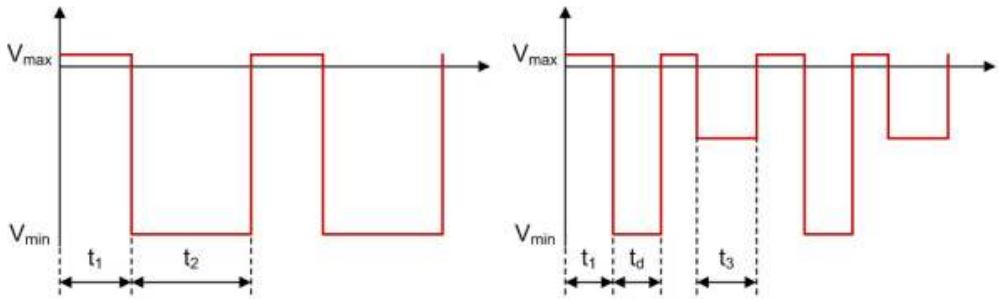


Figure 4.19 Single switch forward - rectifier diode d_1 voltage waveforms in CCM, and DCM

Figure 4.20 shows the Single Switch Forward - Rectifier Diode D_1 current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

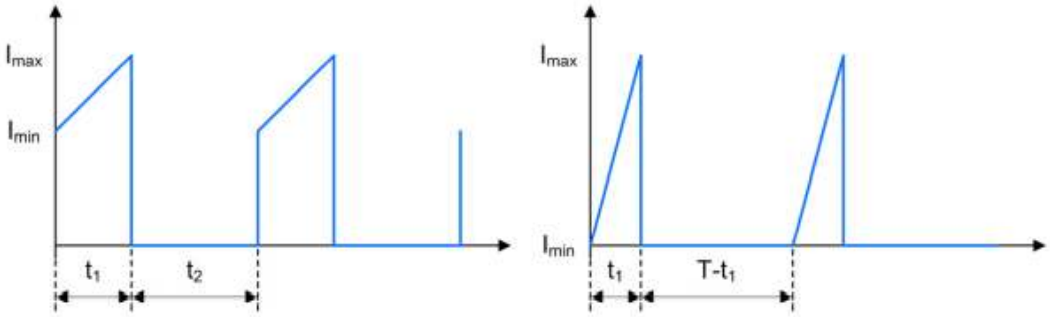


Figure 4.20 Single switch forward - rectifier diode d_1 current waveforms in CCM, and DCM

The average current of rectifier diode Equation (4.76)

$$I_{D_1,avg} = \frac{I_{\text{sec,min}} + I_{\text{sec,max}}}{2} t_2 f_{switch} \tag{4.76}$$

The minimum current of rectifier diode Equation (4.77)

$$I_{D_1,\text{min}} = I_{trans,\text{sec,min}} \tag{4.77}$$

The maximum current of rectifier diode Equation (4.78)

$$I_{D_1,\max} = I_{trans,\sec,\max} \tag{4.78}$$

The minimum voltage of rectifier diode Equation (4.79)

$$V_{D_1,\min} = -(V_{in} + V_f)\frac{n_s}{n_p} + V_f \tag{4.79}$$

The maximum voltage of rectifier Equation (4.80)

$$V_{D_1,\max} = V_f \tag{4.80}$$

The voltage of rectifier after t_d Equation (4.81)

$$V_{D_1,t_d} = V_f \tag{4.81}$$

The voltage of demagnetization diode during t_3 Equation (4.82)

$$V_{D_1,t_3} = -V_{out} \tag{4.82}$$

- **Input capacitor C_i**

Figure 4.21 shows the input capacitor C_i voltage waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and transition mode.

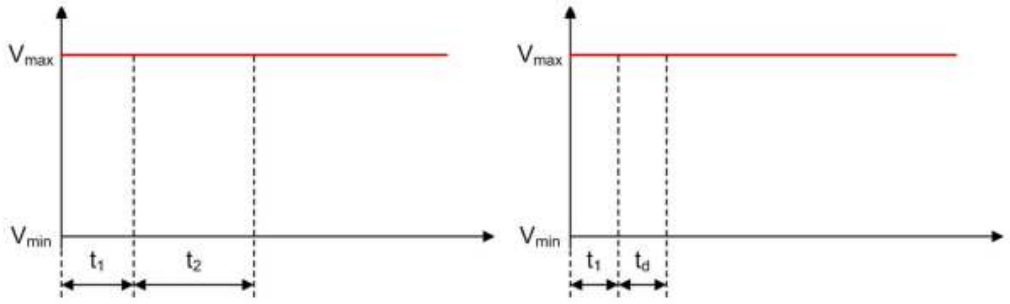


Figure 4.21 Single switch forward – input capacitor c_i voltage waveforms in CCM, DCM, and transition mode

Figure 4.22 shows the input capacitor C_i current waveforms in the continuous condition mode (CCM), discontinuous condition mode (DCM), and transition mode.

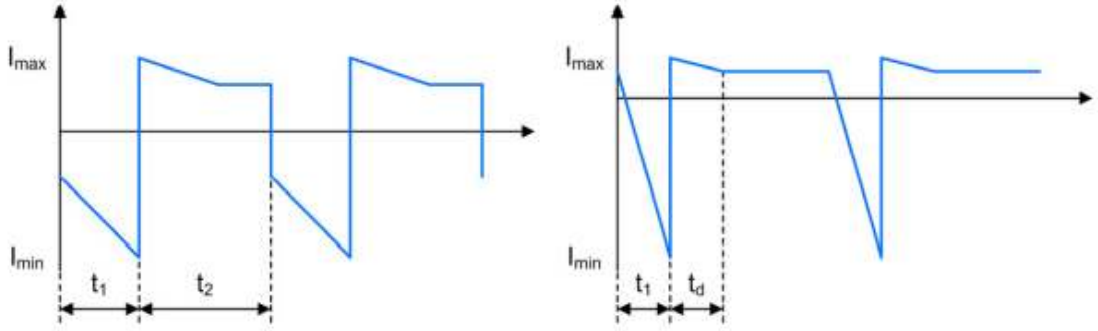


Figure 4.22 Single switch forward - input capacitor c_i current waveforms in CCM

The minimum input capacitor current during t_1 Equation (4.83)

$$I_{C_i,\min,t_1} = I_{N_p,avg} - I_{pri,\max} - I_{D_3,avg} \tag{4.83}$$

The maximum input capacitor current during t_1 Equation (4.84)

$$I_{C_i,\max,t_1} = I_{N_p,avg} - I_{pri,\min} - I_{D_3,avg} \tag{4.84}$$

The input capacitor current during t_3 Equation (4.85)

$$I_{C_i,\max,t_3} = I_{N_p,avg} - I_{D_3,avg} \tag{4.85}$$

The average input capacitor current is null, and input capacitor voltage is equal to input voltage.

- **Output capacitor C_0**

Figure 4.23 shows the single switch forward-Output Capacitor Co voltage waveforms in CCM, and DCM.

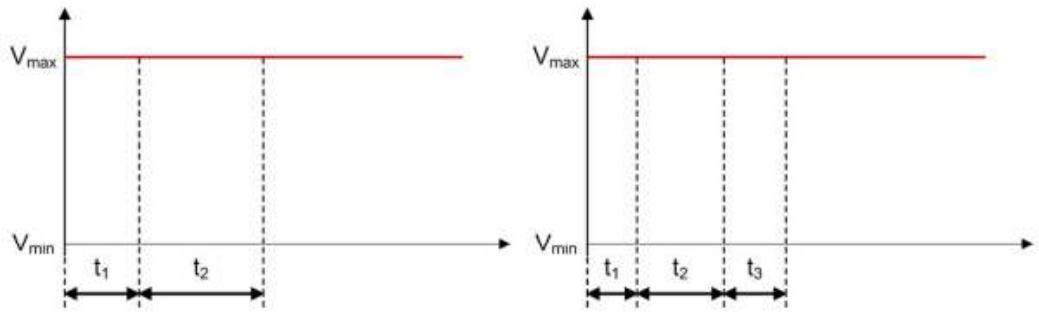


Figure 4.23 Single switch forward – Output capacitor C_o Voltage Waveforms in CCM, and DCM

Figure 4.24 shows the output capacitor C_o current waveforms in the continuous condition mode (CCM), and discontinuous condition mode (DCM).

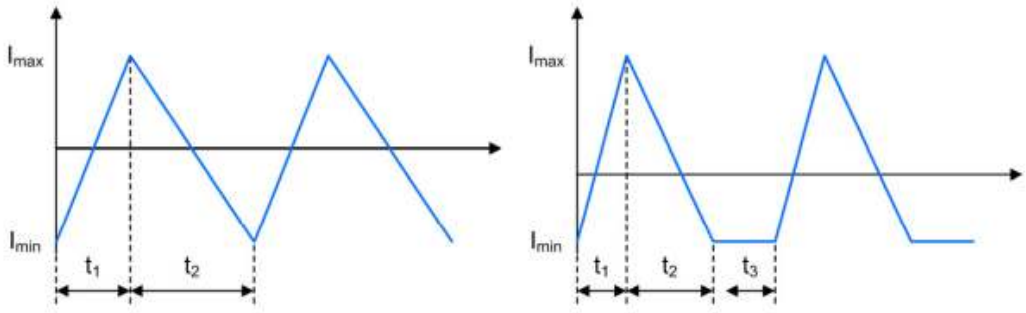


Figure 4.24 Single switch forward - output capacitor c_o current waveforms in CCM, and DCM

The minimum output current of capacitor Equation (4.86)

$$I_{C_o,\min} = I_{L_1,\min} - I_{out} \tag{4.86}$$

The maximum output current of capacitor Equation (4.87)

$$I_{C_o,\max} = I_{L_1,\max} - I_{out} \tag{4.87}$$

The average output current of capacitor Equation (4.88)

$$I_{C_o,avg} = 0A \tag{4.88}$$

The output capacitor voltage Equation (4.89)

$$V_{C_o} = V_{out} \tag{4.89}$$

In the single-switch forward power converter, the magnetizing energy that is stored in the primary inductance is restored to the input source by a demagnetization winding N_d. In general, the primary and the demagnetization windings have the same number of turns. That is why, when the switch is turned off, it has to bear twice the input voltage during the demagnetization time. Both the primary and demagnetization windings must be tightly coupled to reduce the voltage spike.

5. ISOLATED VS. NON-ISOLATED DC POWER SUPPLIES

It has become quite obvious that removing the transformer out of the design suddenly makes it a non-isolated power supply. Designing a power supply board without power isolation is common, however, the consideration of the end-user should be taken into account.

The advantages of non-isolated power supplies are numerous. First, it is more board space in comparison with an isolated power supply design due to the fact that designer needn't use a big transformer. Besides, the designer will also benefit from the increased efficiency with a non-isolated power supply.

Moreover, it is worth noting that it is common practice to place non-isolated supplies downstream of an isolated supply (generally being physically separated from each other). In this strategy, the isolated power supply is placed at the high power AC or DC source, which then drops the voltage down to a level that is safe enough for a standard DC regulator IC or voltage regulator circuit. This is a bit more complex, but it has the advantage of giving you the proper protection that checks off designer's safety requirements. An example of this may look like a standalone medical power supply (isolated) that feeds a handful of devices (non-isolated) downstream.

In summary, typically the power regulation circuit on your board will simply be a non-isolated power supply. These are built from small regulator circuits or chips that do not require isolation because they may not be generating much current or operating at very high voltage. Even if they do operate with high current, the user may not ever interact with the system in such a way as to be at risk of shock. Therefore, non-isolated supplies are just fine for the majority of smaller boards. This will usually just be a buck converter followed by an LDO to regulate power down to the required level. When you need to convert high-current AC to DC, or high current DC to DC, you'll generally use an isolated supply, and many times the power supply will be designed on its own board. What happens next depends on the particular characteristics of your power source (AC vs. DC, mains vs. battery, etc.), how your enclosure will be used,

and how ground is defined in any downstream circuits or systems connected to your power supply.

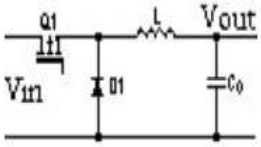
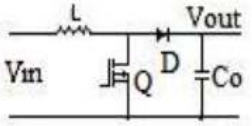
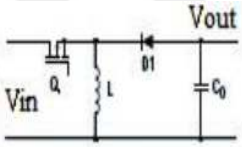
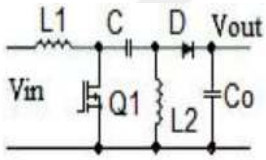
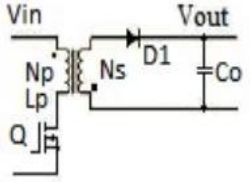
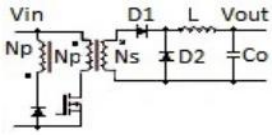
As previously stated, isolated power supplies are often required for regulated industries. Examples include the IEC 60601-1 safety standard for medical devices, IEC 62368-1 for IT and AV equipment (replaces IEC 60950-1 and IEC 60065), and IEC 61204-7:2016 for general switched-mode power supplies. Some regulations do not specify certain industry standards (for example, US FDA regulations on cardiovascular devices in 21CFR870.3605), but they do mandate safety and EMC testing to ensure these devices will be fully compatible with other electronics and basic safety standards in their intended environment.

If you've decided on an isolated vs. non-isolated power supply for your next system, Altium Designer has the circuit design and PCB layout tools you need to create your next product. Altium Designer delivers an unprecedented amount of integration to the electronics industry until now relegated to the world of software development, allowing designers to work from home and reach unprecedented levels of efficiency.

We have only scratched the surface of what is possible to do with Altium Designer.

The table below summarizes and compares electrical features and characteristics of the main single-stage switching regulator circuits (Table 5.1). This chart is followed by the DC to DC regulator selection guide

Table 5.1 Compares electrical features and characteristics of the main single-stage switching regulator circuits

Topology	$\frac{V_{out}}{V_{in}}$	$V_{switch,\max}$	$I_{switch,peak}$	$V_{rectifier,\max}$	$I_{rectifier,avg}$	Switch utilization ratio
NON-ISOLATING DC-DC CONVERTERS						
Buck 	$D \in]0,1[$	V_{in}	I_{out}	V_{in}	$I_{out}D$	$\frac{V_{out}}{V_{in}}$
Boost 	$\frac{1}{1-D}$ $D \in]0,1[$	V_{out}	$I_{out}\frac{V_{out}}{V_{in}}$	V_{out}	I_{out}	$\frac{V_{in}}{V_{out}}$
Inverting Buck-Boost 	$\frac{-D}{1-D}$ $D \in]0,1[$	$V_{in}+\lvert V_{out}\rvert$	$I_{out}(1+\frac{\lvert V_{out}\rvert}{V_{in}})$	$V_{in}+\lvert V_{out}\rvert$	I_{out}	$\frac{\lvert V_{out}\rvert}{V_{in}}$
SEPIC 	$\frac{-D}{1-D}$ $D \in]0,1[$	$V_{in}+V_{out}$	I_{out}	$V_{in}+V_{out}$	I_{out}	$\frac{V_{out}}{V_{in}+V_{out}}$
ISOLATING DC-DC CONVERTERS						
Flyback 	$\frac{(V_{in}D)^2}{2I_{out}L_pf}$ $D \in]0,1[$	V_{in}	$\frac{(V_{in}D)}{L_pf}$	$V_{out}+V_{in}\frac{n_s}{n_p}$	I_{out}	$\frac{D}{2(1+\frac{V_{out}n_p}{V_{in}n_s})}$
Single Switch Forward 	$D\frac{n_s}{n_p}$ $D \in]0,0.5[$	$2V_{in}$	$I_{out}\frac{n_s}{n_p}$	$V_{in}\frac{n_s}{n_p}$	$1: DI_{out}$ $2: (1-D)I_{out}$	$\frac{V_{out}n_s}{2V_{in}n_p}$

There is no single topology, which is best for all applications. The right switching power supply topology for a given application should be selected based on specific requirements for the power supply design including cost, size, time factors, and expected production volume. SMPS design handbook for example, for low-volume designs, the engineering expenses may be more important than BOM cost. In this case,

you may want to choose a straightforward "textbook-based" approach in which you are most experienced. Well executed trivial design is better than a poorly executed "fancy" one. Of course, while a basic design may be straightforward, meeting all of the safety and EMC regulatory specifications may still be a very time-consuming task. For high-volume production, you'll want to put extra engineering efforts into developing new solutions, minimizing component cost and assembly labor. When the functional requirements are pretty much conventional, the power level is usually the main factor that determines the topology selection. As an illustration, the table below shows the configurations I would normally prefer for a downstream DC-DC converter in an off-line switching power circuit depending on its output power level. This selector guide is given for the power sources with output voltages below 60V running off 120 to 400V DC-link (which are typical levels for rectified AC input line voltage or the output of a PFC boost). At power levels above 3000W, I would consider using multiple interleaved converters to spread heat dissipation. Note, all the information here, of course, is just general guidance based on the author's personal view.

5.1 Analysis by Python Power Electronics Programming

Python power electronics is a powerful and open-source circuit simulator for power electronics.

The following tutorial shows the tasks needed to install Python power electronics on a windows machine.

Install and run Anaconda on windows:

- Go to https://www.anaconda.com/products/distribution.
- Look for Anaconda Installers and download the installer (Figure 5.1).

Figure 5.1 Anaconda installers

- Run the downloaded file to install Anaconda on your operating system.
- Once installed you are ready for the next step.

1. Setting up Anaconda python on windows:

   in this task you will learn how to create environments in Anaconda and how to install packages within them.

- Run Anaconda prompt (Figure 5.2).

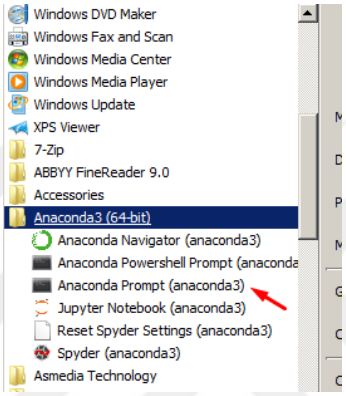


Figure 5.2 Run anaconda prompt

- Create new environment named (pythonpowerelectronics_env) by running the following command in the prompt window:

  conda create --name pythonpowerelectronics_env
- Activate the newly created environment by running the following command: conda activate pythonpowerelectronics_env
- Create a new folder for simulation in the desired drive on your machine and name it “pythonpowerelectronics_simulation”, for example let’s create it in the drive “C:”
- In the folder “C:\pythonpowerelectronics_simulation”, copy the zippid file “simulation.zip” and extract the contents of the file there (Figure 5.3).

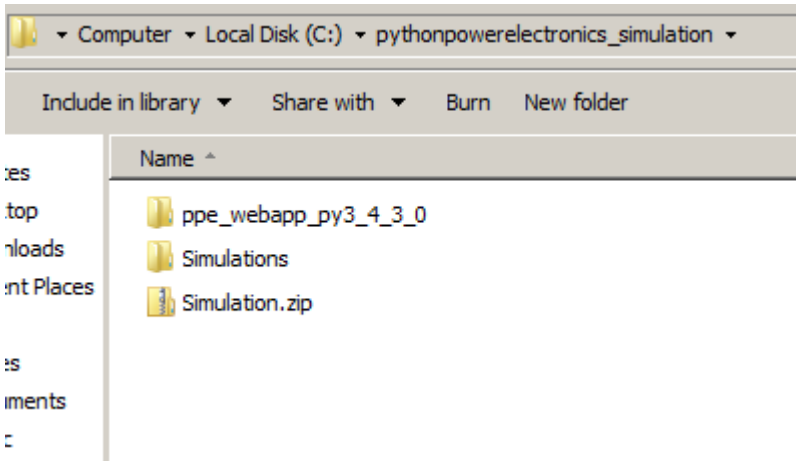


Figure 5.3 Choose the installation location

- Change the working directory to the created directory by running the following command:
  cd c:\pythonpowerelectronics_simulation\ppe_webapp_py3_4_3_0
- Install the required packages to run Pythonpowerelectronics by running the following command:
  conda install --file requirements.txt
- Change the working directory to "simulator interface" by running the following command:
  cd simulator_interface
- run the Pythonpowerelectronics web server by running the following command:
  python manage.py runserver (Figure 5.4).

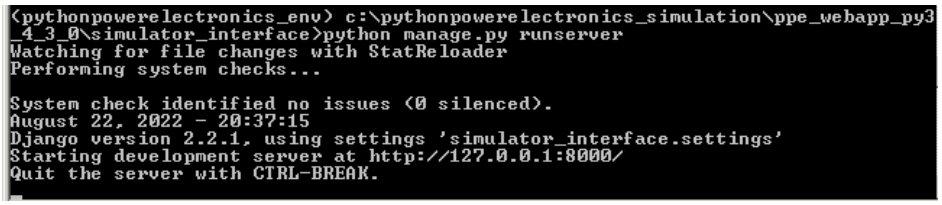


Figure 5.4 Installation of python power electronics

- Start the web server by going to the link http://127.0.0.1:8000 in your internet browser (Figure 5.5).

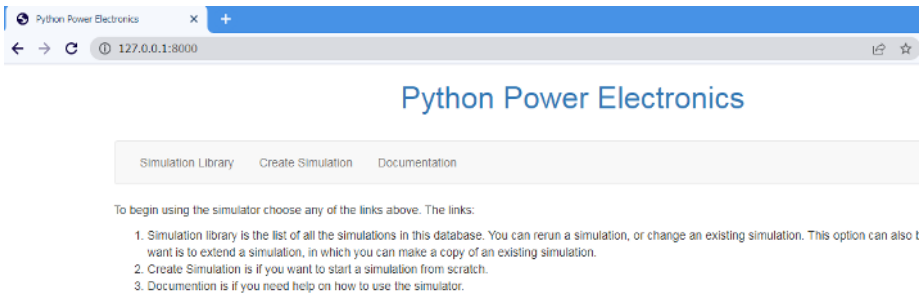


Figure 5.5 Start of python power electronics

- Now you are ready to use Pythonpowerelectronics to simulate electronic circuits on a windows machine.
  Change the working directory to "simulator interface" by running the following command:

  cd c:\pythonpowerelectronics_simulation\ppe_webapp_py3_4_3_0\simulator_interface

- run the Pythonpowerelectronics web server by running the following command:

  python manage.py runserver (Figure 5.6).

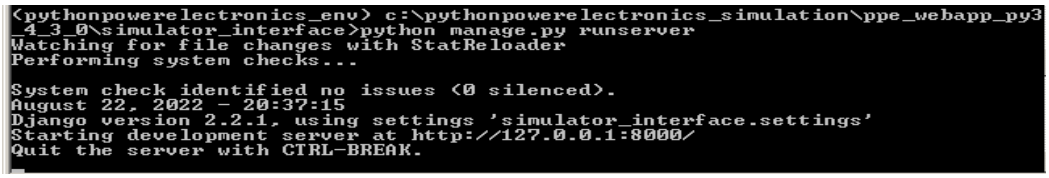


Figure 5.6 Python power electronics command

- Start the Python power electronics web server by going to the link http://127.0.0.1:8000 in your internet browser (Figure 5.7).

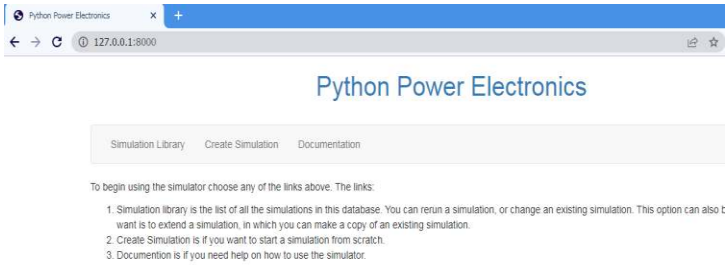


Figure 5.7 Starting to python power electronics

- Click on "Simulation Library" then load the buck converter simulation by clicking "Load Simulation" (Figure 5.8).

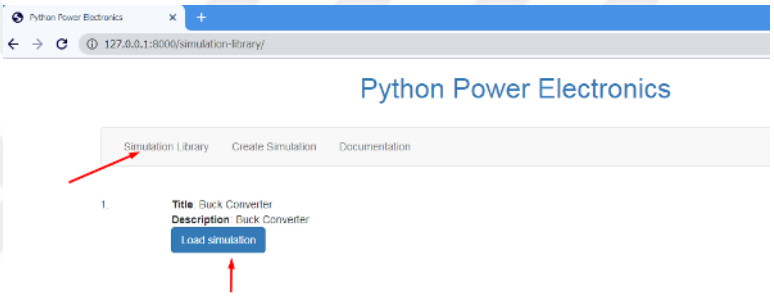


Figure 5.8 Loading simulation folder

- Then click on "Back to the main page" (Figure 5.9).

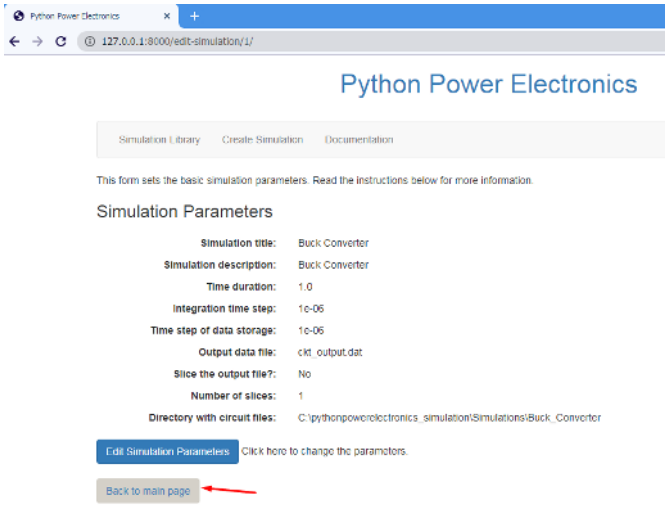


Figure 5.9 Simulation parameters

- This page is the main page for the simulation where you can “Edit circuit parameters”, “Edit control” or “View output” (Figure 5.10).

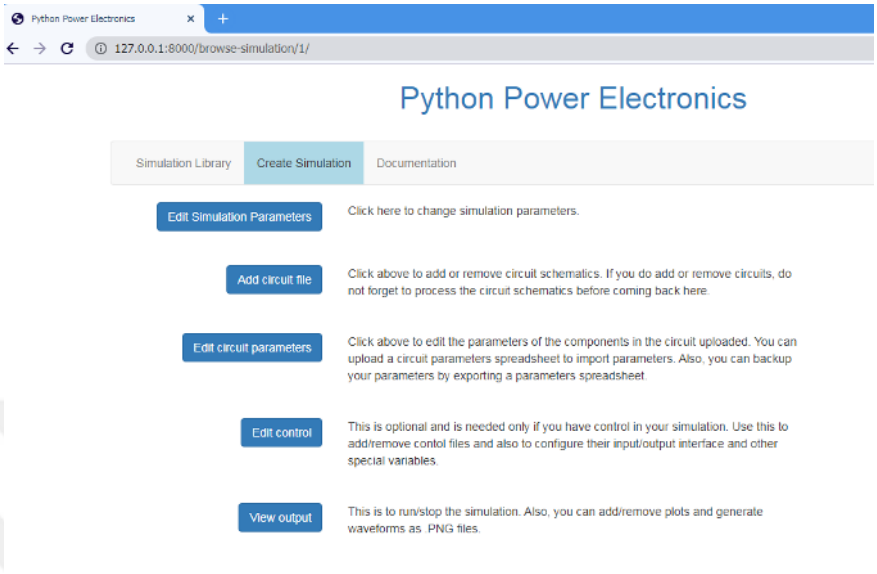


Figure 5.10 Create simulation

- To view the results of the simulation click on “View output”.
- To start the simulation click on “Run” (Figure 5.11).

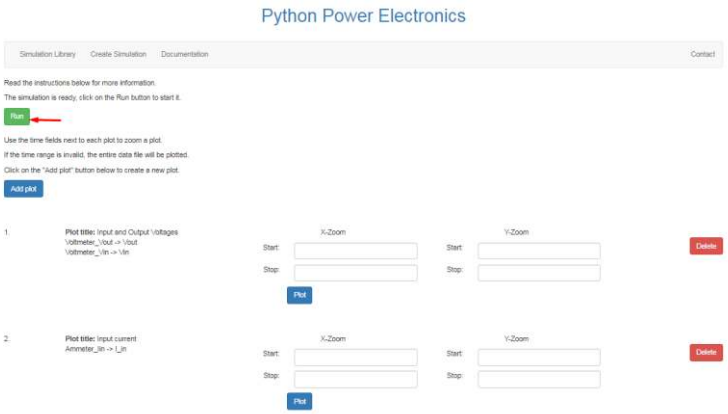


Figure 5.11 Run simulation

- To plot the input voltage versus the output voltage do as following
  - Input “start time = 0”
  - Input “stop time = 0.05”

- Click “plot” (Figure 5.12).

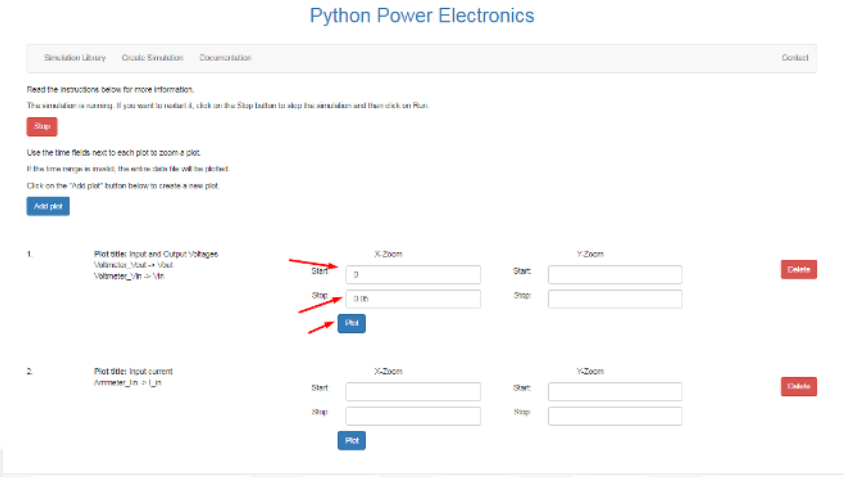


Figure 5.12 Select simulation plot

6. RESULTS AND DISCUSSION

In this section the simulation of some topologies (Buck, Buck-Boost, and the Flyback) will be presented and the result of simulation will be discussed.

6.1 Buck Converter Simulation Results

Using Python power electronics (Appendix A) to simulate the work of a buck converter as shown in Figure 6.1 with PWM = 30%:

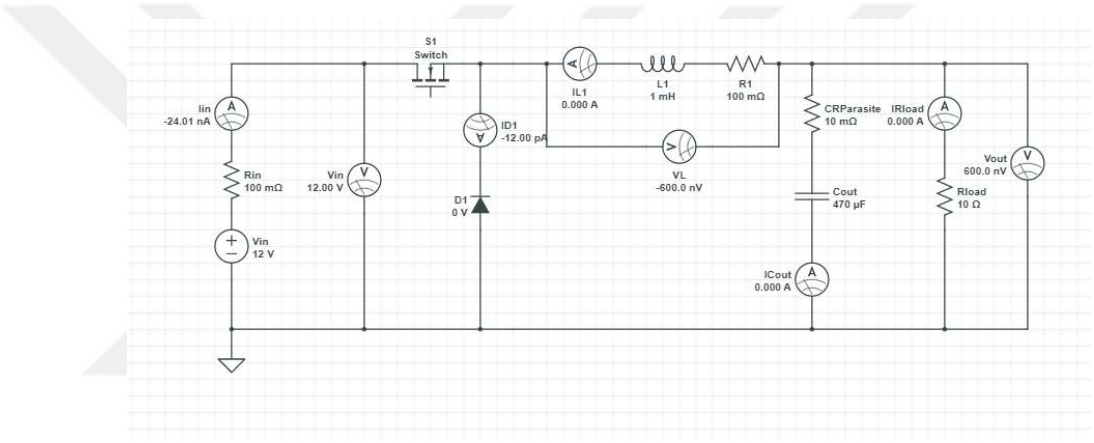


Figure 6.1 Buck converter circuit

After setup the simulation (Appendix B) the the simulation results would be in the folder "C:\pythonpowerelectronics_simulation\Simulations\Buck_Converter" and the name of the file is "InputandOutputVoltages.png". Figure 6.2 shows the output and input voltage for D=30%. The stability time 10ms with overshooting <55%.

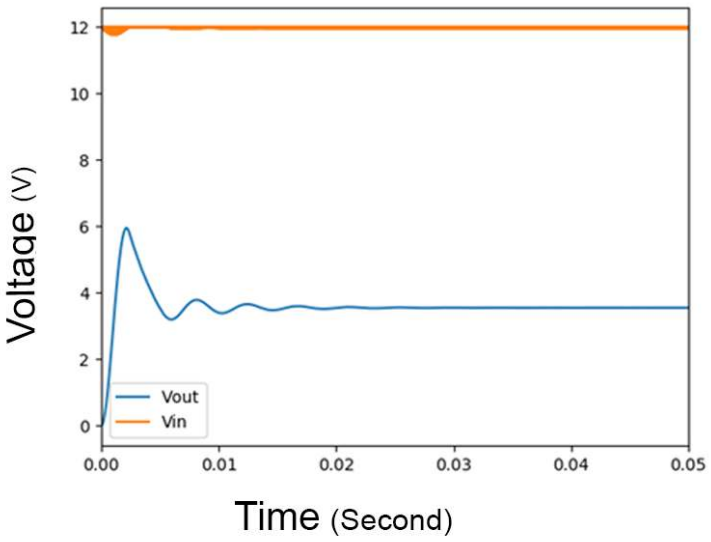


Figure 6.2 Buck converter simulated voltage

The simulation results for the input current are shown in Figure 6.3.

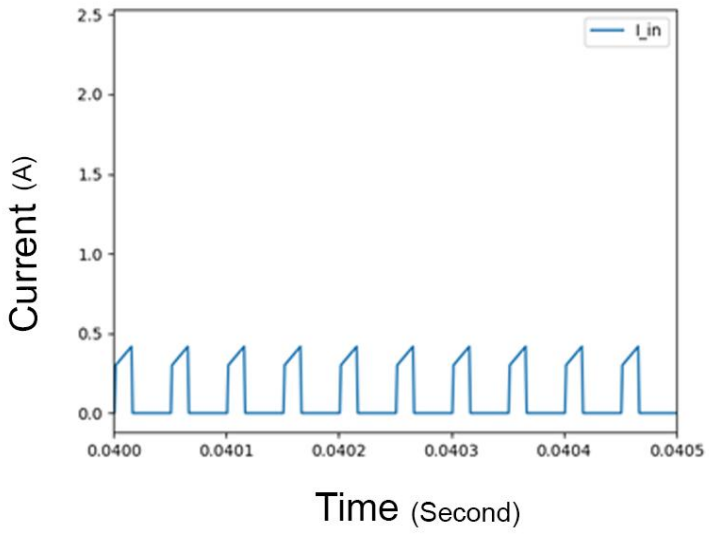


Figure 6.3 Buck converter simulated input current

The simulation results for the inductor current are shown in Figure 6.4.

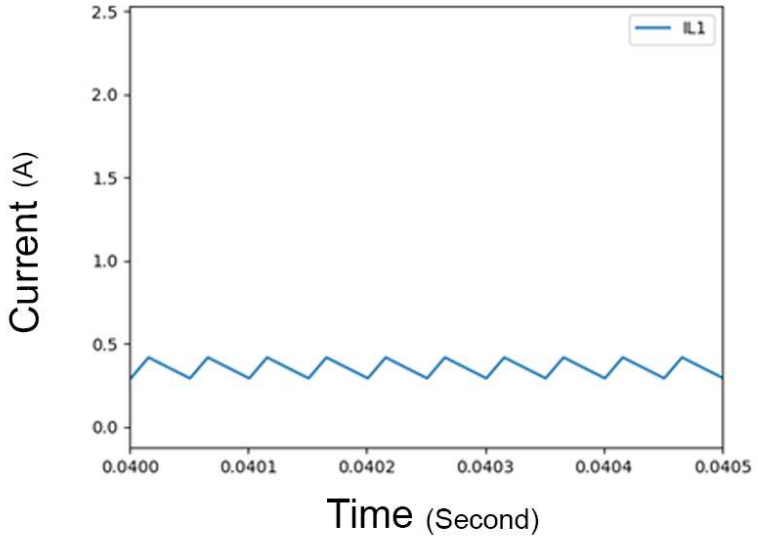


Figure 6.4 Buck converter simulated inductor current

The simulation results for the diode current are shown in Figure 6.5.

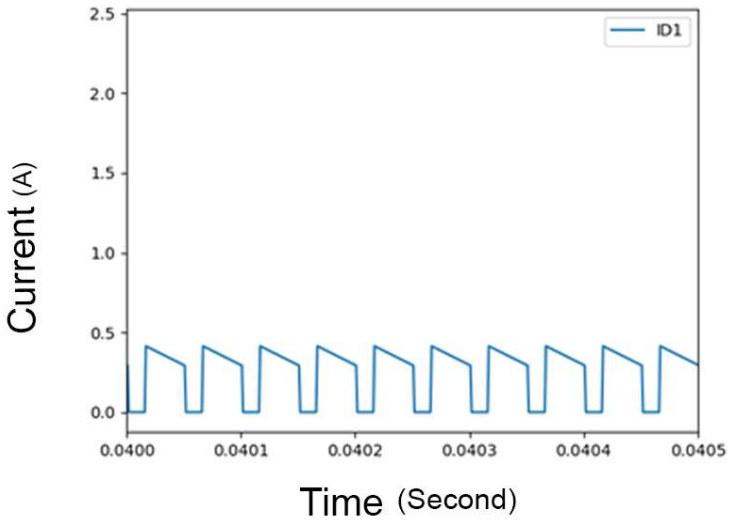


Figure 6.5 Buck converter simulated diode current

The results of the previous simulation correspond to the theoretical study in the third chapter. As we notice that practical voltage/current output signals curves in the buck DC-to-DC converter are identical with the simulation results and with the mathmatical equations presented in Chapter 3.

6.2 The Buck-Boost Converter Simulation Results

Figure 6.6 shows the schematic diagram of Buck-Boost converter.

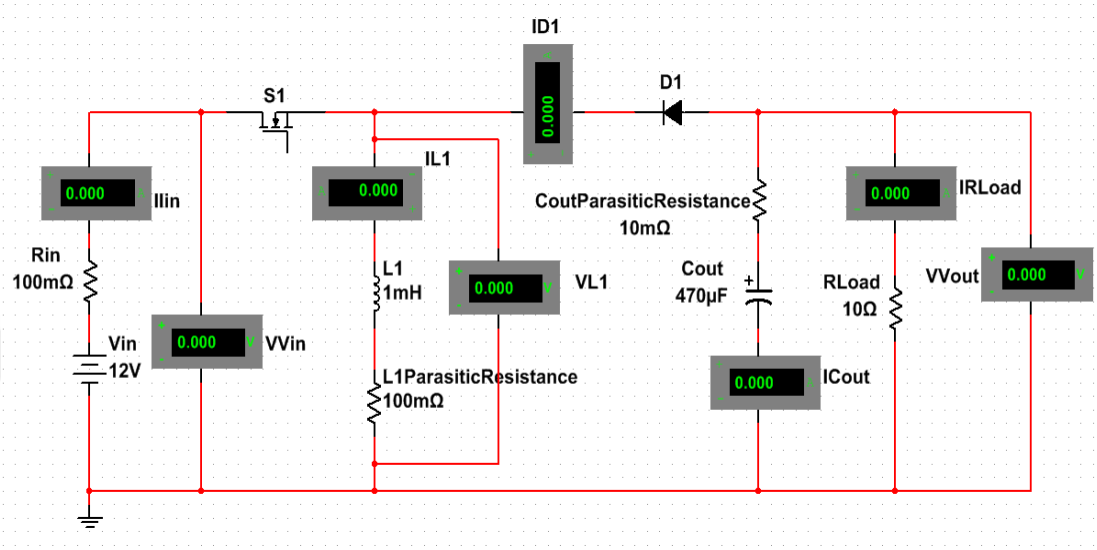


Figure 6.6 Buck-boost converter simulated circuit

The simulation results for continuous mode buck-boost converter with $PWM = 30\%$.

Simulation parameters are as following:

$RLoad = 10\Omega$.

$PWM = 30\%$.

$Switching\ frequency = 20kHz$.

Input and output voltage (transient waveform) is shown in Figure 6.7.

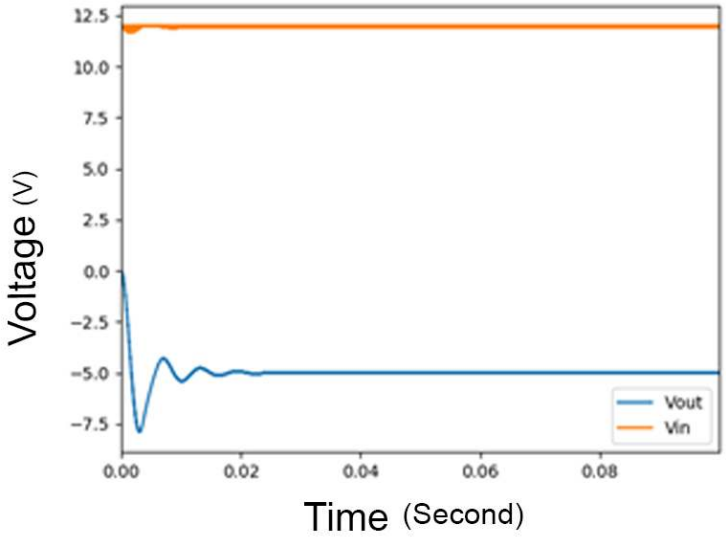


Figure 6.7 Buck-boost converter simulated Input and output voltage (Transient Waveform)

The Inductor voltage waveform is shown in Figure 6.8.

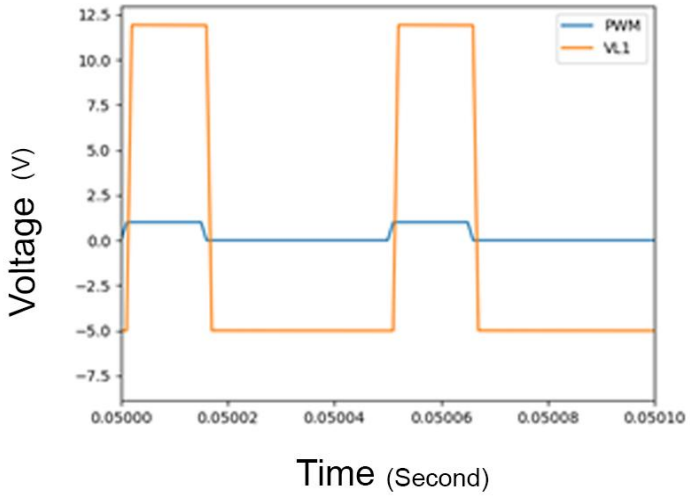


Figure 6.8 Buck-boost converter simulated Inductor voltage waveform

The Inductor current waveform is shown in Figure 6.9.

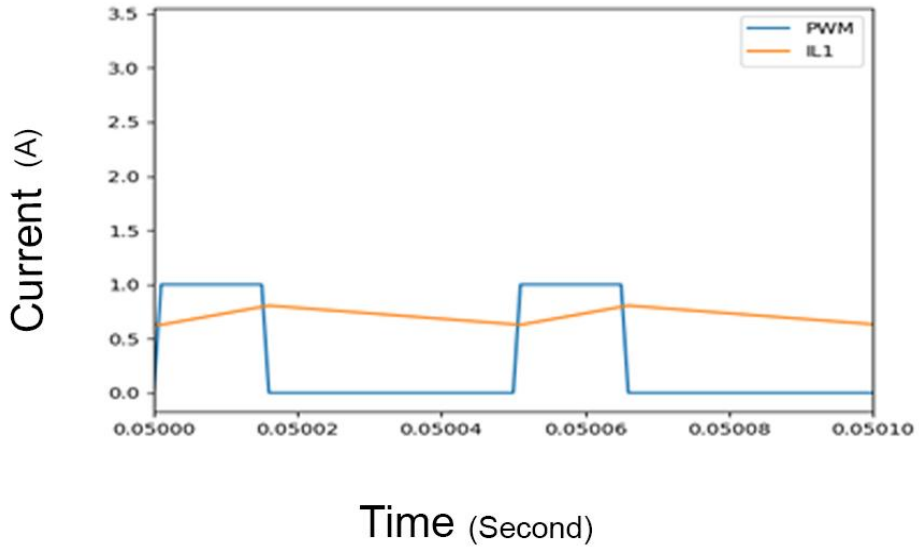


Figure 6.9 Buck-boost converter simulated pwm and Inductor current waveform

The diode current waveform is shown in Figure 6.10.

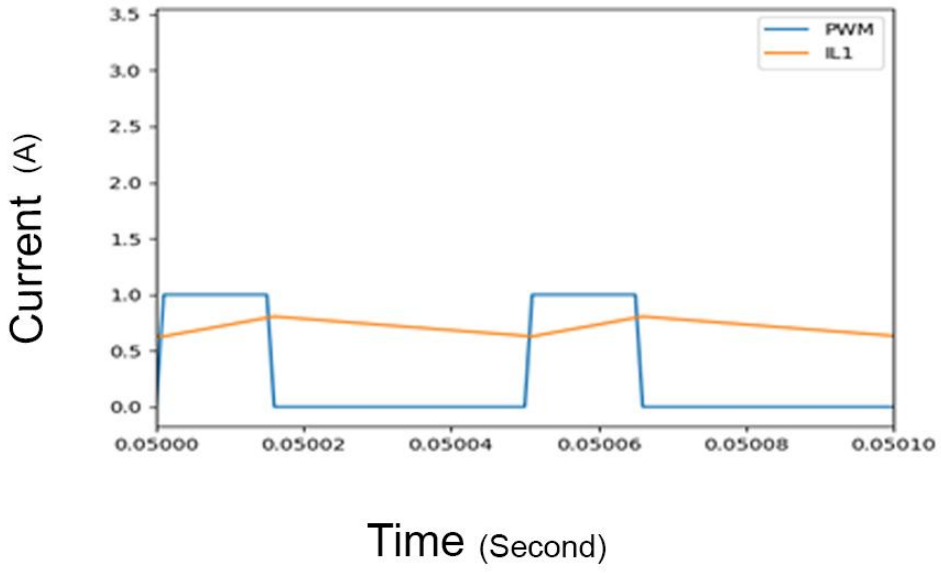


Figure 6.10 Buck-boost converter simulated pwm and diode current waveform

The Capacitor current waveform in Figure 6.11.

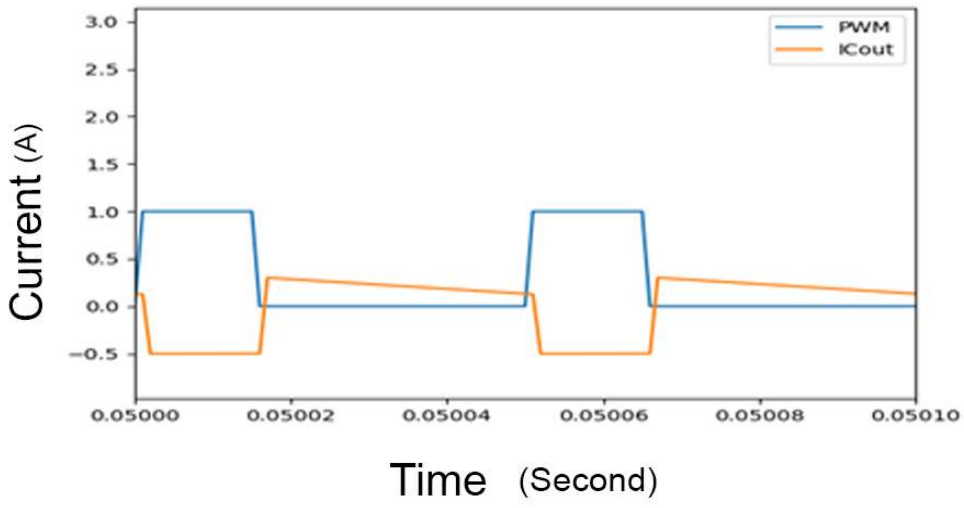


Figure 6.11 Buck-boost converter simulated capacitor current waveform

The simulation results for continuous mode buck-boost converter with$PWM = 70\%$.

Simulation parameters are as following:

$RLoad = 10\Omega$.

$PWM = 70\%$.

$Switching\ frequency = 20kHz$.

Input and output voltage (transient waveform) is shown in Figure 6.12.

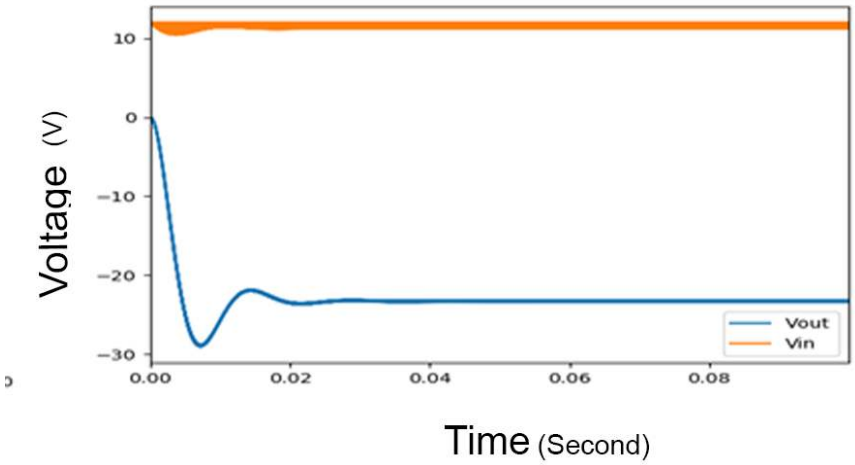


Figure 6.12 Buck-boost converter simulated Input and output voltage for d=70%

The Diode current waveform is shown in Figure 6.13.

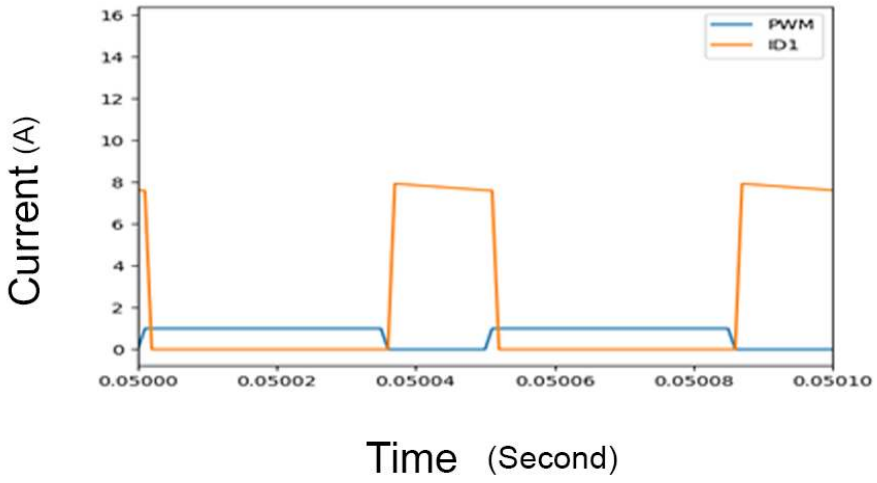


Figure 6.13 Buck-boost converter simulated diode current for d=70%

All currents waveform in Buck-Boost converter for D=70% are shown in Figure 6.14.

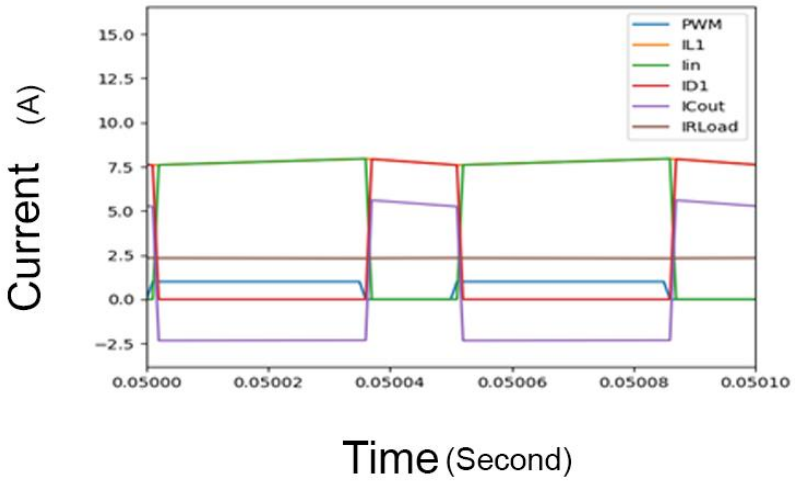


Figure 6.14 All currents waveform in buck-boost converter for d=70%

6.3 The Flyback Converter Simulation Results

Due to the slow simulation for isolated DC-DC converter, low switching frequency is used for the simulation ($Switching\ frequency = 1\ kHz$) (the typical switching frequency must be greater than 20 kHz but it takes too long time to simulate). Here is the simulation results for the flyback converter using Pythonpowerelectronics (schematic diagram is shown in Figure 6.15):

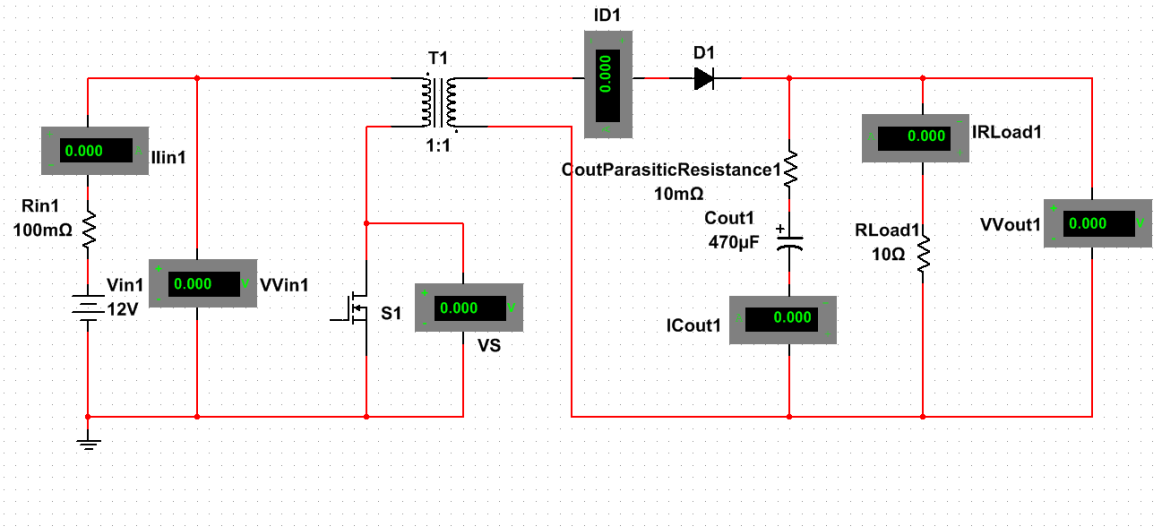


Figure 6.15 Flyback converter simulated circuit

1. The simulation results for flyback converter with $PWM = 30\%$.

Simulation parameters are as following:

$RLoad = 10\Omega$.
$PWM = 30\%$.
$Switching\ frequency = 1kHz$.
$Transformer\ turn\ ratio = 1$.

Input and output voltage (transient waveform) is shown in Figure 6.16.

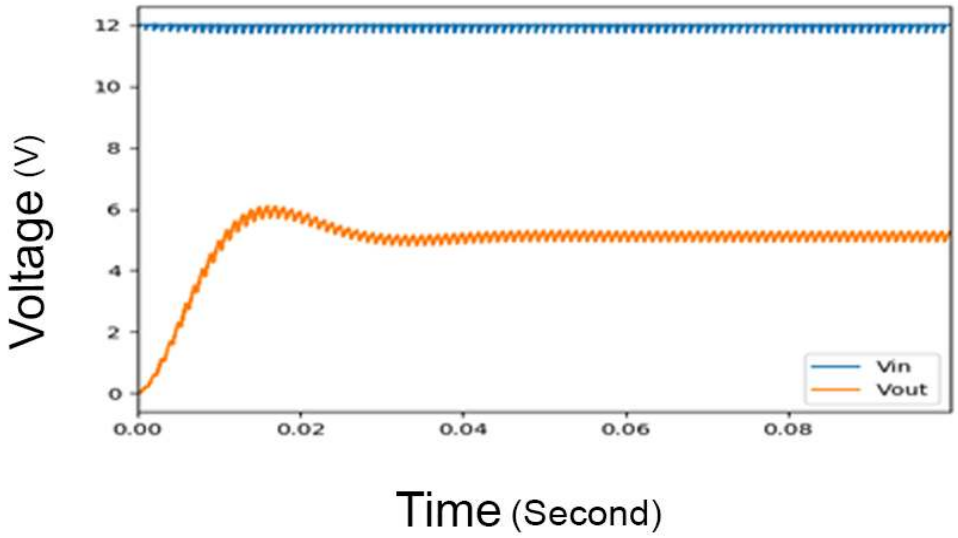


Figure 6.16 Flyback converter simulated Input and output voltage (Transient Waveform)

The Load resistance current waveform is shown in Figure 6.17.

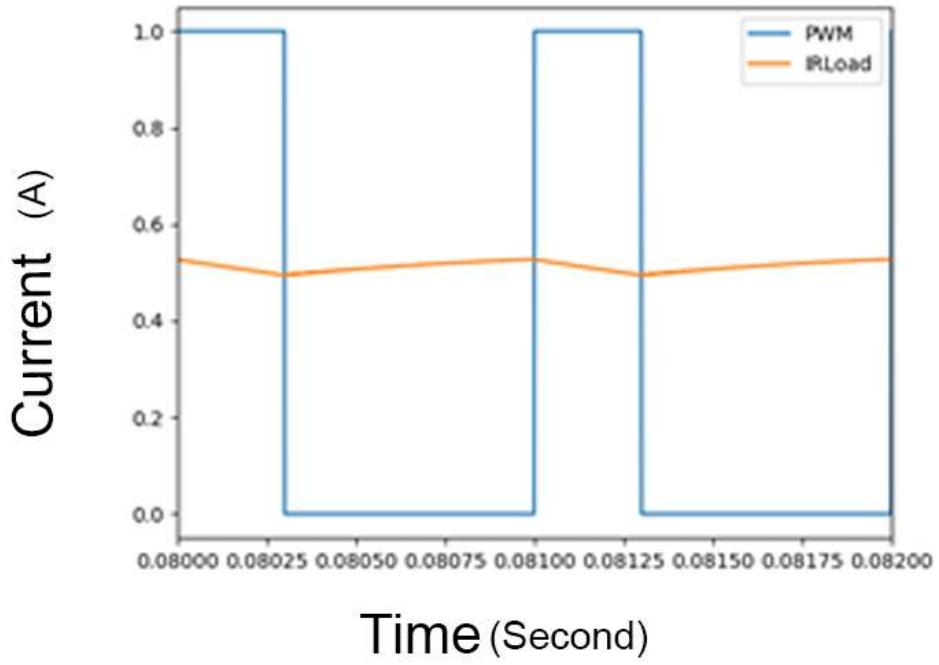


Figure 6.17 Flyback converter simulated load resistance current

The Transformer primary voltage waveform is shown in Figure 6.18.

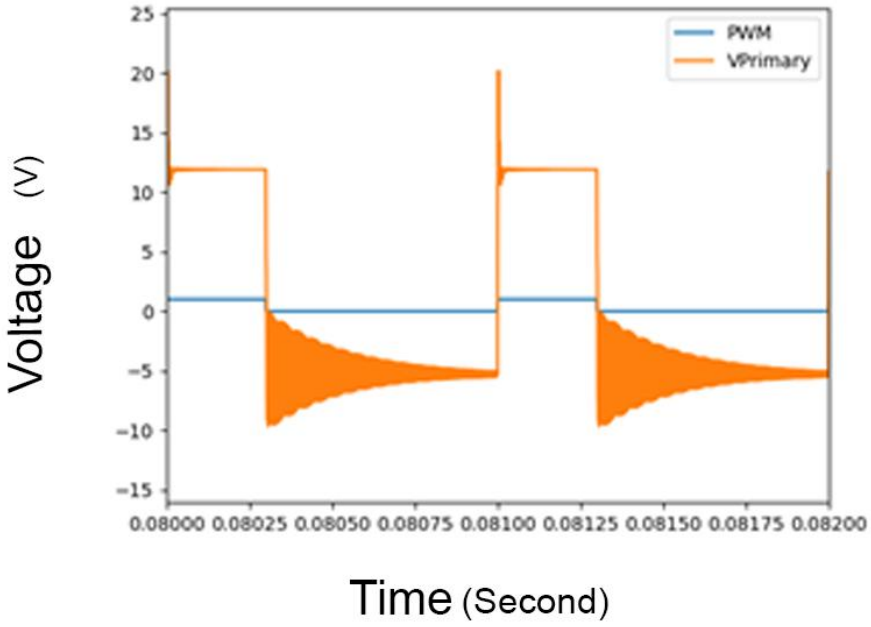


Figure 6.18 Flyback converter simulated transformer primary voltage waveform

The Transformer secondary voltage is shown in Figure 6.19.

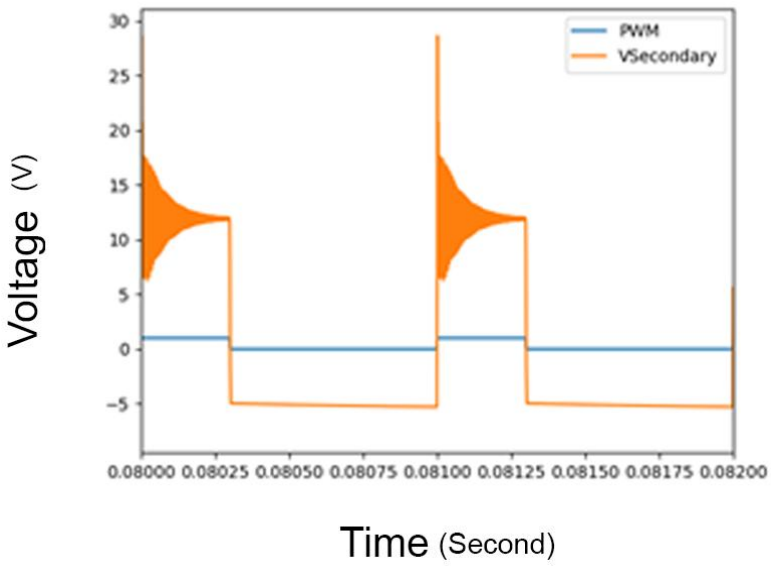


Figure 6.19 Flyback converter simulated transformer secondary voltage waveform

The Switch voltage waveform is shown in Figure 6.20.

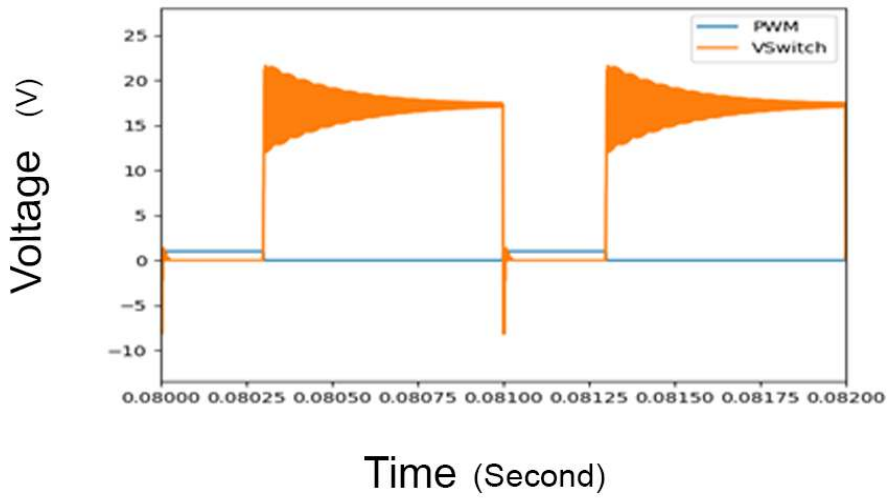


Figure 6.20 Flyback converter simulated switch voltage waveform

2. The simulation results for flyback converter with $PWM = 60\%$.

Simulation parameters are as following:

$RLoad = 10\Omega$.

$PWM = 60\%$.

$Switching\ frequency = 1kHz$.

$Transformer\ turn\ ratio = 1$.

Input and output voltage (transient waveform) is shown in Figure 6.21.

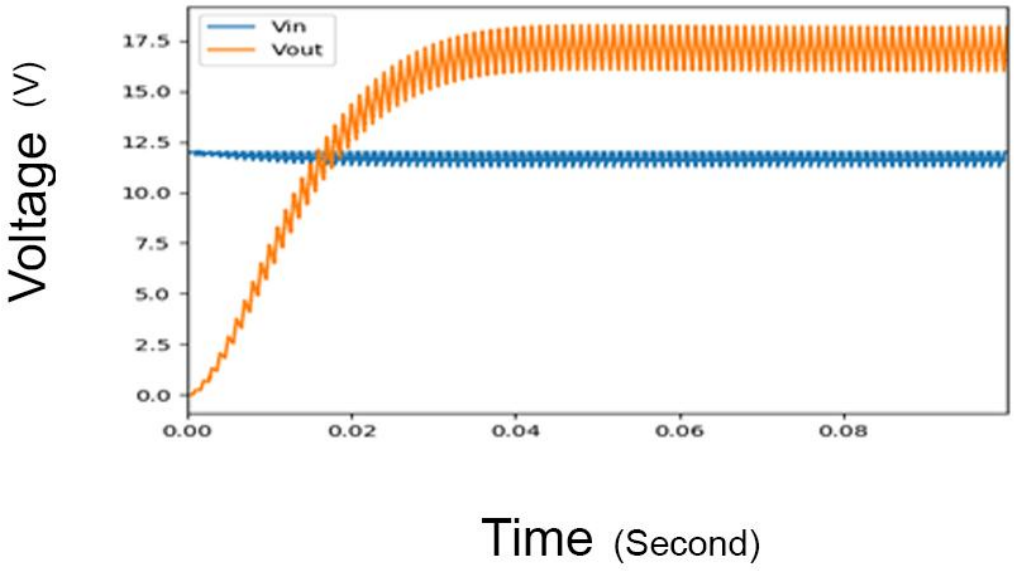


Figure 6.21 Flyback converter simulated Input and output voltage d=60%

The Load resistance current waveform is shown in Figure 6.22.

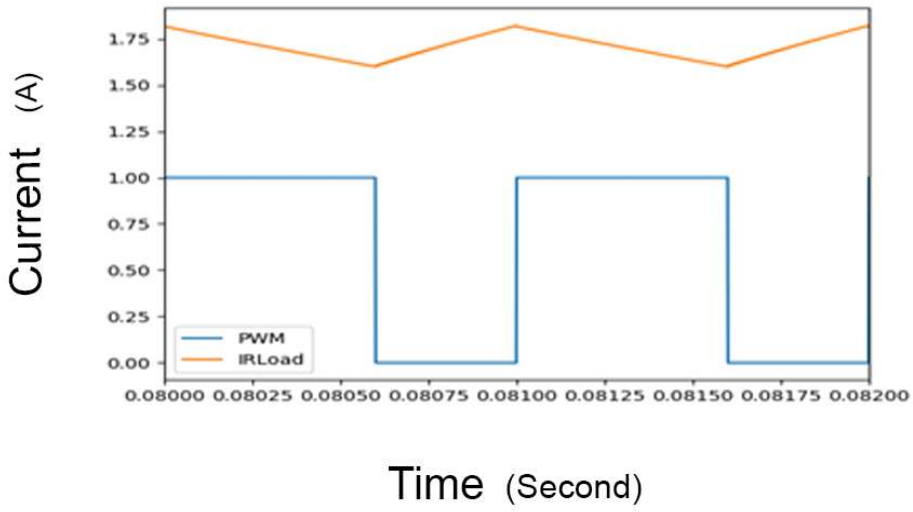


Figure 6.22 Flyback converter simulated load resistance current waveform

The Transformer primary voltage waveform is shown in Figure 6.23.

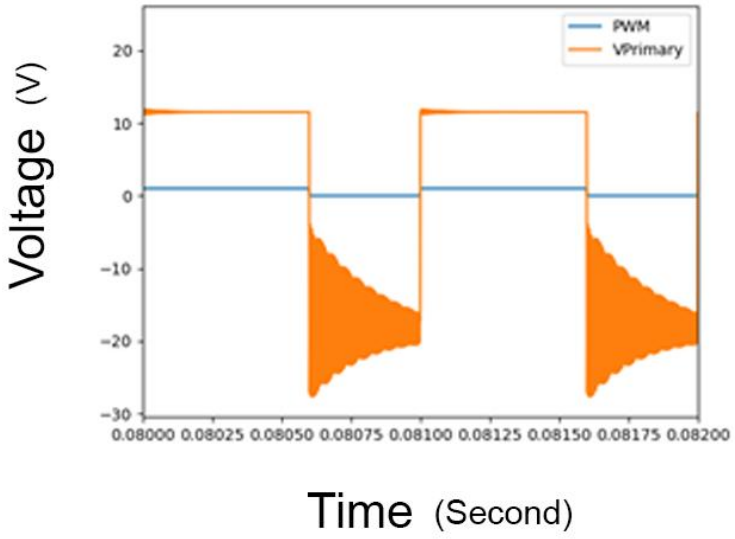


Figure 6.23 Flyback converter simulated transformer primary voltage waveform

7. CONCLUSION

Several significant technological changes in power supply design have lowered cost per watt while improving performance. Today, the latest technology is being used in SMPS in order to reduce both size and weight. Output voltage and load current are always application-dependent, and power supply designs are often designed for specific applications.

This paper provides an overview of the most commonly used topologies and lists the most important features of each one of them. A complete study of the most important types of isolated and non-isolated SMPS is presented and the mathematical relationships are presented that explain the form and nature of the circuit voltages and currents in full and each of its components. The studied topologies were simulated using the Python language after explaining the mechanism of work using this language. The simulation results showed a perfect match with the theoretical relationships that determine the behavior of each SMPS.

In the future, it is possible to work on developing SMPS so that the lost power is as little as possible through the use of elements that work on new technologies (silicon semiconductor).

Buck converter structure has output circuits that are more suitable for electric vehicle technologies among the circuit topologies examined. On the other hand, buck boost and flyback converter structures are not suitable for electric vehicles and electric charging stations because they contain too much noise as output value. It works in different ranges from 12 volts to 72 volts in the literature and is suitable for direct use for electric charging stations in the 12/36 volt range in buck converter structure.

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