ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES

PhD THESIS

Serhan YAMAÇLI

DEVELOPMENT OF AB INITIO BASED MODELS FOR CARBON NANOTUBE TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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ABSTRACT

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Carbon nanotube (CNT) circuit components are promising elements for the post silicon Very Large Scale Integration (VLSI) technology. Research on CNT components and circuits are advancing rapidly. Circuits produced in CNT technology are proven to provide high current density and ballistic transport in a small area. Despite the advancements in CNT circuit technology, accurate and versatile models for CNT interconnects and CNT field effect transistors (CNTFETs) are missing in the literature. This thesis is aimed to fill in this gap.

Firstly, electronic properties of CNTs are given as a basis in the introduction section. After section 2, in which related works in the literature are reviewed, material and methods for analysing CNT nanodevices are explained. The goals of this thesis are given in the results and discussions section.

The variation of CNT resistance with the applied voltage is obtained using self-consistent atomic simulations and then a polynomial model suitable for use in VLSI design and simulation tools is developed in the first subsection. Secondly, a neural network model for the nonlinear resistance-voltage variation of metallic CNTs is given. Utilization of the saturated current-voltage characteristics of metallic CNTs is then presented as a novel nanoscale design concept with example circuits and HSPICE simulations. Fourthly, a voltage-dependent capacitance extraction method for CNTs using self-consistent simulation results is provided with results. In the next subsection, metallic CNTs are modelled as transmission lines employing voltage-dependent resistance and voltage-dependent capacitance, then the delay through the CNT is calculated accurately with comparison to the delay calculation obtained by different methods. A CNTFET model utilizing self-consistent simulation method to calculate the channel charge accurately and suitable for use in SPICE is presented in the sixth subsection. Finally, example circuit simulations using the proposed CNTFET model are provided. The overall work is reviewed in the conclusions section.

Keywords: Carbon nanotubes, nanoelectronics, nanoscale device modelling.

ÖZ

DOKTORA TEZİ

KARBON NANOTÜP TEKNOLOJİSİ İÇİN AB INITIO MODELLERİN GELİŞTİRİLMESİ

Serhan YAMAÇLI

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Karbon nanotüp (CNT) devre elemanları, silikon sonrası çok geniş ölçekli tümleştirme (VLSI) teknolojisinde gelecek vaat eden elemanlardır. CNT elemanlar üzerindeki araştırmalar gittikçe yoğunlaşarak artmaktadır. CNT teknolojisiyle üretilen devrelerde, CNT'lerin yüksek akım yoğunluğu ve balistik elektron akımı küçük bir alanda gerçekleştirilebilmektedir. CNT teknolojisindeki gelişmelere rağmen, literatürdeki CNT arabağlaşım elemanları ve CNT alan etkili transistörler (CNTFET'ler) için yüksek doğruluklu ve kullanışlı model eksikliği vardır. Bu tezde, bu boşluğun doldurulması hedeflenmiştir.

Öncelikle, CNT'lerin elektronik özellikleri giriş bölümünde temel olması açısından verilmiştir. Literatürdeki ilgili çalışmaların gözden geçirildiği 2. bölümden sonra, CNT nano düzenleri incelemek için gereken materyal ve metotlar açıklanmıştır. Bu tezde elde edilen sonuçlar ise bulgular ve tartışmalar bölümündedir.

İlk altbölümde, CNT direncinin uygulanan gerilimle değişimi öz uyumlu atomik benzetimlerle elde edilmiş ve VLSI tasarım ve benzetim araçlarında kullanılabilecek bir polinom modeli geliştirilmiştir. İkinci olarak, metalik CNT'lerin doğrusal olmayan direnç-gerilim değişimleri yapay sinir ağları ile modellenmiştir. Üçüncü altbölümde ise, metalik CNT'lerin doymuş akım-gerilim karakteristiklerinden yararlanarak nano ölçekte yeni bir devre tasarım kavramı, örnek devreler ve bu devrelerin HSPICE benzetimleri verilmiştir. Dördüncü olarak, CNT'lerin gerilime bağlı kapasitanslarının öz uyumlu benzetim verilerinden elde edilmesi için önerilen bir yöntem verilmiştir. Sonraki altbölümde, CNT'ler için gerilime bağlı direnç ve gerilime bağlı kapasitans içeren bir iletim hattı modeli ile bu model kullanılarak yapılan yüksek doğruluklu gecikme hesaplamaları, literatürdeki diğer çalışmalardan elde edilen sonuçlar ile karşılaştırılarak açıklanmıştır. Öz uyumlu kanal yükü hesaplama yöntemi içeren ve SPICE uyumlu olan yüksek doğruluklu bir CNTFET modeli ise altıncı altbölümde önerilmiştir. Son altbölümde ise, önerilen CNTFET modeli kullanılarak yapılan VLSI temel yapı bloklarının benzetimleri ele alınmıştır. Sonuçlar bölümünde ise, yapılan çalışmalar gözden geçirilmiştir.

Anahtar Kelimeler: Karbon nanotüpler, nanoelektronik, nanoölçekli eleman modelleme.

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LIST OF ABBREVIATIONS AND NOTATIONS

q	**:** Elementary charge
h	**:** Planck's constant
$\mathbf{h}$	**:** Reduced Planck's constant
b	**:** Distance between carbon atoms
k_x	**:** Wave vector in x-direction
k_y	**:** Wave vector in y-direction
ε_0	: Dielectric constant of free space
g_0	**:** Bonding energy
d	**:** Carbon nanotube diameter
μ_i	**:** Electrochemical potential of the electrode *i*
E_g	**:** Energy gap
G	**:** Conductance
k_B	**:** Boltzmann constant
T	**:** Absolute temperature
E_F	**:** Fermi energy
U_{SCF}	**:** Self-consistent potential
C_G	**:** Gate capacitance
C_S	**:** Source capacitance
C_D	**:** Drain capacitance
C_{TOT}	**:** Total capacitance
N	**:** Number of electrons
V_{DS}	**:** Drain-source voltage
V_{GS}	**:** Gate-source voltage
$D(E)$	**:** Density of states function
$f(E)$	**:** Fermi-Dirac probability density function
N_0	**:** Initial electron density
U_p	**:** Potential of the p^{th} subband
A, B, C	: Fitting coefficients
L	: Carbon nanotube length

v_{sat} : Saturation velocity

C_e : Electrostatic capacitance

C_Q : Quantum capacitance

J_+ : Current density in +x direction

J_- : Current density in -x direction

m_e : Electron mass

J_{net} : Net current density

e : Shift coefficient

Δ : Broadening coefficient

I_1 : Current in +x direction

I_2 : Current in -x direction

γ : Flow rate

Ψ : Wavefunction

$\mathbf{H}$: Hamiltonian operator

R_T : Total resistance

μ_L : Electrochemical potential of the left electrode

μ_R : Electrochemical potential of the right electrode

V_{bias} : Bias voltage

CNT : Carbon nanotube

CNTFET : Carbon nanotube field effect transistor

U : Channel potential

L_{mfp_low} : Mean free path of electrons at low voltage levels

E_{ph} : Phonon energy

V_{mCNT} : Metallic CNT voltage

I_{mCNT} : Metallic CNT current

G_{mCNT} : Metallic CNT conductance

I_{sat} : Saturation current

V_{ES} : Electrostatic potential

SWCNT : Single walled carbon nanotube

MWCNT : Multi walled carbon nanotube

DFT	: Density functional theory
NEGF	: Non-equilibrium Green's function formalism
LDA	: Local density approximation
DZP	: Double zeta polarized
V_{XC}	: Exchange-correlation potential
R_L	: Load resistance
R_P	: Parallel resistance

1. INTRODUCTION

Since the conceptualization of integrated circuits (ICs) by Geoffrey Dummer in 1952 (Roberts, 1984) and the implementation of the first IC by Jack Kilby in 1958 (Kilby, 2000), the last five decades witnessed the amazing advancement of Silicon (Si) microelectronics. Developments in Si microelectronics are achieved by continuous scaling, in other words miniaturization, of the electronic components implemented on the ICs. Considering the modern complementary metal oxide (CMOS) technology, IC miniaturization methods sustained the scaling of metal oxide semiconductor field effect transistors (MOSFETs) and metallic interconnects; the conductors used to connect MOSFET terminals to supply voltage and to each other as required (Srivastava, 2005). Miniaturization in IC technology leads to denser circuits and faster switching to provide faster and improved ICs in all areas of life spanning from mobile phones to medical imaging equipment. According to Moore's law, the number of transistors on a standard IC is expected to double in every two years, which is also expressed as scaling the gate length of a contacted MOSFET on an IC to be 0.7 in every two years. This observation turned out to be true until today since 1970s as shown in Figure 1.1 (Mollick, 2006). The technology node was 45nm in 2010 and expected to be 38nm in 2011 by the International Technology Roadmap for Semiconductors (ITRS) committee (ITRS CMOS roadmap, 2011).

On the other hand, miniaturization of ICs are approaching its limit for several reasons including electron tunneling through short channels and thin insulator films, variations in device structure and doping, the effects of crystal misalignments and the increment of interface scatterings on the electron motion since the mean free path (MFP) of electrons become comparable to component dimensions. From a circuit point of view, the performance degredation due to miniaturization appears as the increment in the resistance of metallic on-chip interconnects and short channel effects in MOSFETs (Durkan, 2007), (Saraswat et al., 2008), (Naeemi et al., 2004), (Avouris et al., 2004).

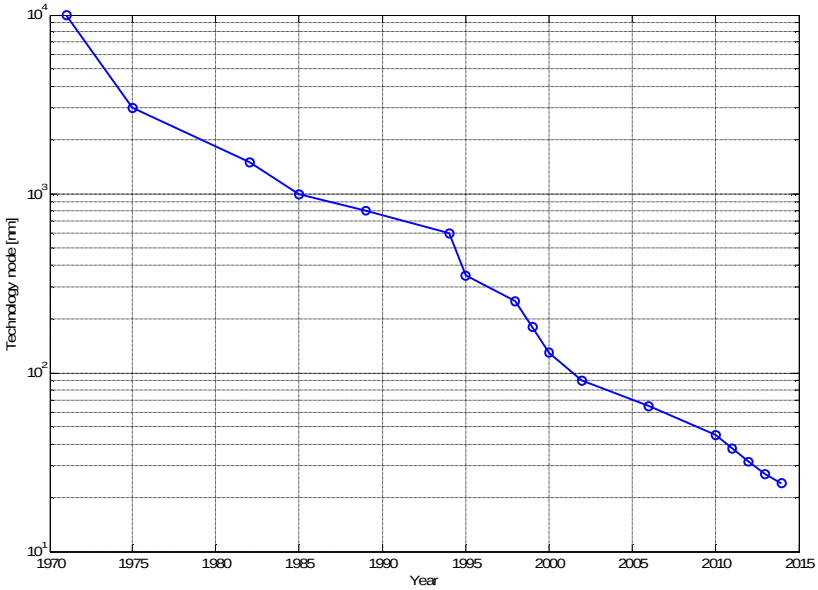

Figure 1.1. Decrement in technology node

There are two approaches to address the issues related to the scaling of silicon (Si) ICs. In long-term approaches, completely novel devices based on totally new concepts are proposed such as spintronic devices, single-molecule devices and quantum computing. These revolutionary devices are expected to be widely implemented in the far future. For the near future, devices that have current-voltage characterstics similar to current devices however with novel materials and nanoscale operating principles are explored (Avouris et al., 2004). These devices include graphene field effect transistors (FETs), silicon nanowire FETs and carbon nanotube (CNT) FETs, which are abbreviated as CNTFETs. Among these devices, CNTFETs take more attention due to its superior electrical transport properties. Furthermore, CNTs behave as either conductor or semiconductor depending on their crystal orientations which is also adventageous from IC viewpoint since the whole IC can be implemented using semiconductor CNTs in CNTFETs and conductor CNTs as interconnects (Liu et al, 2007), (Li et al., 2003), (Liu et al., 2009), (Sun et al, 2008), (Pesetski et al., 2008), (Amlani et al., 2006), (Harris, 2011), (Saito et al, 1998).

The objectives of this thesis are to model CNT interconnects and CNTFETs more accurately compared to the studies existing in the literature and to show sample circuit designs together with their simulations. Before advancing on the proposed

models, electronic properties of CNTs; required to understand the origins of superior performance of CNT interconnects and CNTFETs; are given in the following subsection. Then CNT interconnect and CNTFET structures are introduced in the next subsections which are followed by the thesis outline.

1.1. Electronic Properties of Carbon Nanotubes

The physical properties of CNTs are derived from those of graphene crystal therefore the properties of graphene structure are briefly explained and then the properties of CNTs are given.

Graphene is a 2-dimensional (2-D) honeycomb crystal structure made of carbon atoms as shown in Figure 1.2. The distance between atoms in graphene, expressed by *b*, is 0.142nm (Harris, 2011). The dispersion relationship, also called as *E–k* function, of graphene crystal is given as in Equation 1.1 (Hanson, 2008). Dispersion relation gives information on the energy of electrons dependent on their wave vectors in x- and y- directions. In Equation 1.1, γ_0 is the bonding energy, which has the value 3eV, $a = \sqrt{3}b$, k_x and k_y are electron wave vectors in x- and y- directions, respectively.

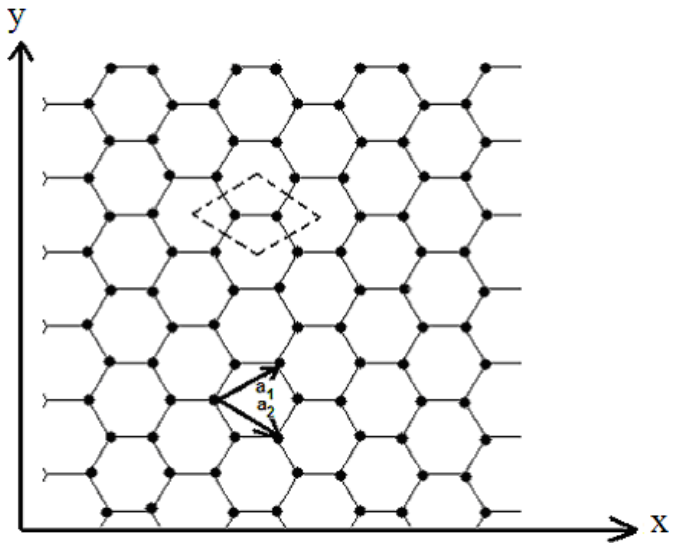

Figure 1.2. Graphene crystal lattice with basis vectors a_1 and a_2 and the unit cell shown by dashed lines

$$E(k_x,k_y)=\pm g_0\sqrt{1+4\cos\left(\frac{\sqrt{3}k_x a}{2}\right)\cos\left(\frac{k_y a}{2}\right)+4\cos^2\left(\frac{k_y a}{2}\right)} \quad (1.1)$$

The band structure of the graphene crystal is shown in Figure 1.3. *E–k* function around the Fermi level, shown inside circles, is approximated as in Equation 1.2 where v_F is the Fermi velocity of electrons, **h** is reduced Planck's constant and *k* is the wave vector (Hanson, 2008).

$$E=v_F\mathbf{h}k \quad (1.2)$$

The advantage of graphene and CNT based structures stems from the fact that, the form of the *E–k* function given in Equation 1.2 is in the form of the *E–k* function of photons. From this point, it is argued that the electrons in graphene based structures are expected to behave like massless particles, which makes their velocity faster than conventional Si or GaAs structures (Hanson, 2008). The ballistic transport and nearly massless behavior are also verified by experiments (Novoselov et al, 2005).

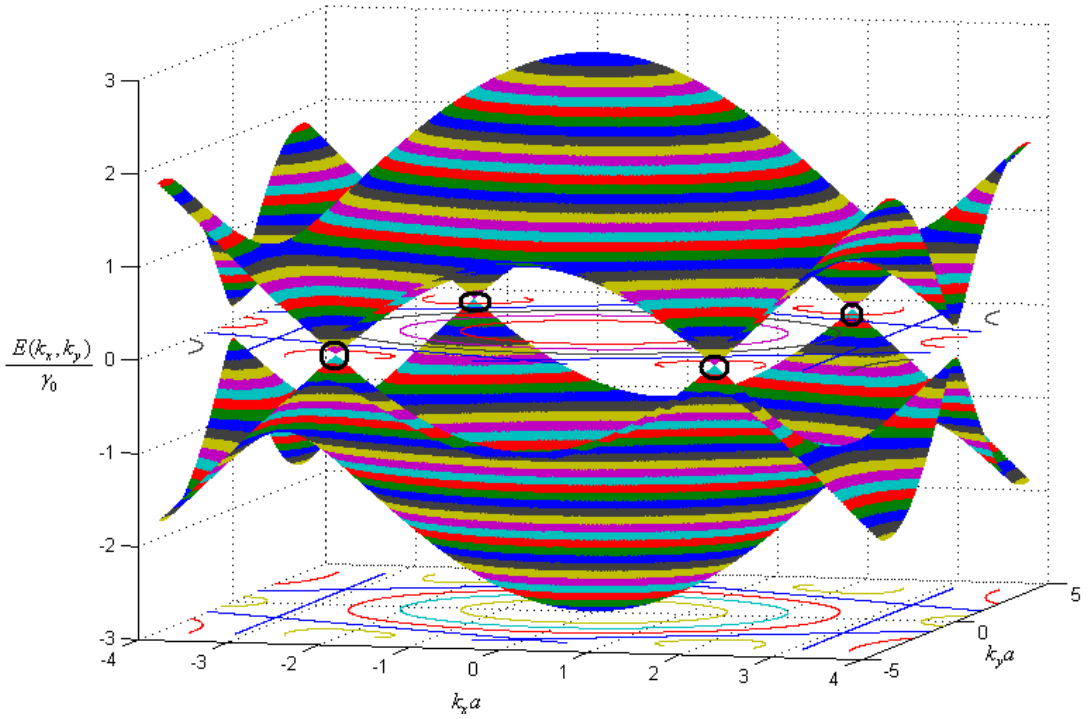

Figure 1.3. Band structure of graphene

CNTs are almost perfect hollow cylindrical crystals made of carbon atoms, which are discovered by Iijima in 1991 during an arc discharge experiment (Iijima, 1991). CNTs can be produced using various methods such as arc discharge or laser ablation (Harris, 2011). On the other hand, CNTs can be thought as rolled-up sheets of graphene to derive their electronic properties. The formation of various types of CNTs from 2–D graphene sheets are shown in Figure 1.4 where dashed lines show the rolling direction. Since any rolling direction can be expressed by a pair of integers in 2-D, CNTs are labeled according to these rolling direction with indices (n,m). In Figure 1.5, the vectors defining the geometry of CNTs namely the chiral vector *AA'* and translational vector *AB* are shown. If *A* and *A'* together with *B* and *B'* are connected, the chiral vector *AA'* can be written in terms of unit vectors as in Equation 1.3 which implies n=2 and m=1 hence a (2,1) CNT is formed. The vector *AB* is named as translational vector whose length is the length of the CNT unit cell (Saito et al., 1998).

$$AA' = 2a_1 + 1a_2 \tag{1.3}$$

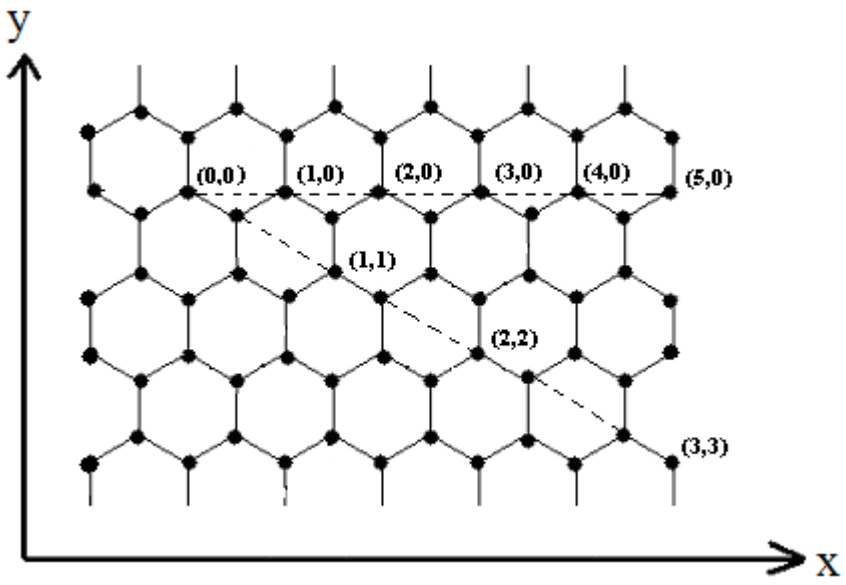

Figure 1.4. Formation of various CNTs from graphene layer

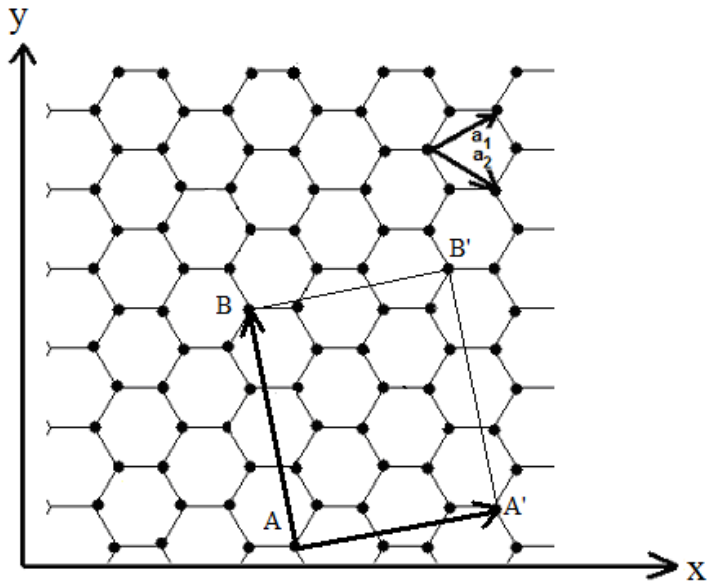

Figure 1.5. Unit vectors and indices of carbon nanotubes

Diameters of CNTs depend on their indices and the C-C bond length as given in Equation 1.4.

$$d = \frac{\sqrt{3}b\sqrt{n^2 + nm + m^2}}{p} \tag{1.4}$$

The period length of the carbon nanotube is the length of the translational vector. It is given in Equation 1.5 (Saito et al., 1998).

$$T = \frac{3b\sqrt{n^2 + m^2 + nm}}{gcd_T}$$
$$\gcd_T = \begin{cases} \gcd(n,m), & (n-m)\ is\ not\ multiple\ of\ 3 \\ 3\gcd(n,m), & (n-m)\ is\ a\ multiple\ of\ 3 \end{cases} \tag{1.5}$$

CNTs are classified into two groups according to their number of shells. If a CNT has a single shell, it is called as a single-walled CNT or if a CNT has more than one shell then it is named as a multi-walled CNT. Single-walled CNTs are reported to be more advantageous from electronics point of view (Massoud and Nieuwoudt,

2008). On the other hand, CNTs are also grouped into three groups according to their indices. If the indices of a CNT are equal as (n,n), then the CNT is called as an armchair CNT. If the indices are different and nonzero, then CNT is named as a chiral CNT while CNTs having m=0 are called as zigzag CNTs. The positions of carbon atoms in real space for (5,5) armchair and (12,0) zigzag CNTs are shown in Figure 1.6 and Figure 1.7, respectively. The vertical pattern of carbon atoms resemble armchair and zigzag patterns as can be seen from the figures which justify the classification namings (Yamacli and Avci, 2010a).

CNTs are classified also according to their electronic properties. CNTs exhibiting conductive behaviour are named as metallic CNTs while CNTs having semiconductor behaviour are called as semiconducting CNTs. All armchair CNTs show conductor behaviour hence they can be used as interconnects on ICs. On the other hand, zigzag and chiral carbon nanotubes are metallic if the difference between the indices; n-m; is an integer multiple of 3 otherwise they behave as semiconducting CNTs, which are utilized in CNTFETs (Hanson, 2008).

The dispersion relationships of CNTs can be obtained from Equation 1.1 by the quantization of the energy levels depending on the type of the CNT. Dispersion relations of zigzag and armchair carbon nanotubes are given respectively as in Equation 1.6 and Equation 1.7 (Hanson, 2008).

$$E_z(k) = \pm g_0 \sqrt{1 + 4\cos\left(\frac{\sqrt{3}k_x a}{2}\right)\cos\left(\frac{p\,c}{n}\right) + 4\cos^2\left(\frac{p\,c}{n}\right)} \tag{1.6}$$

$$E_a(k) = \pm g_0 \sqrt{1 + 4\cos\left(\frac{p\,d}{n}\right)\cos\left(\frac{k_y a}{2}\right) + 4\cos^2\left(\frac{k_y a}{2}\right)} \tag{1.7}$$

where c and d are nonzero integers. On the other hand, the energy gap of semiconductor carbon nanotubes can be given dependent on the tube diameter as in Equation 1.8.

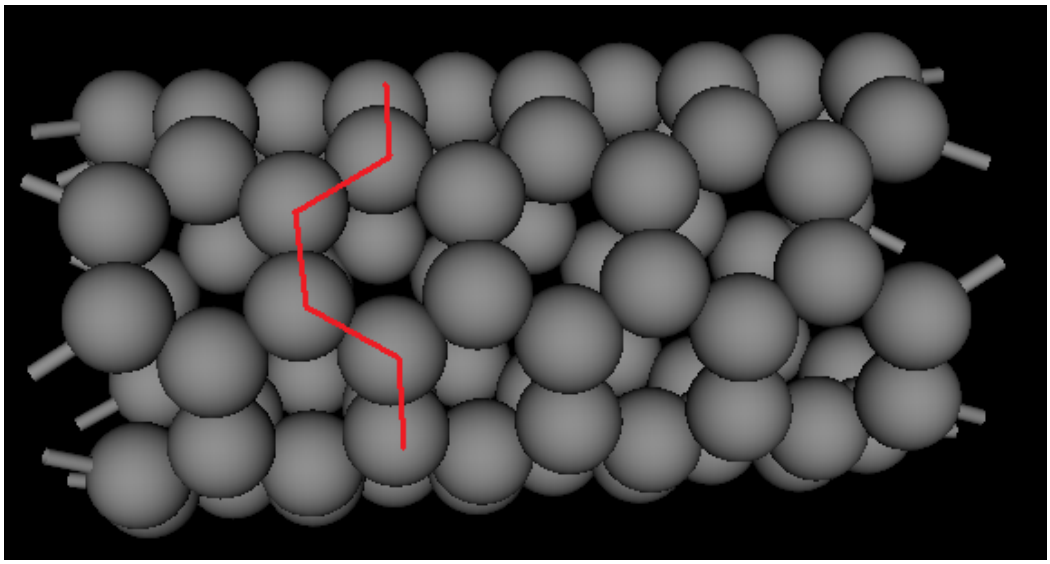

Figure 1.6. (5,5) armchair carbon nanotube

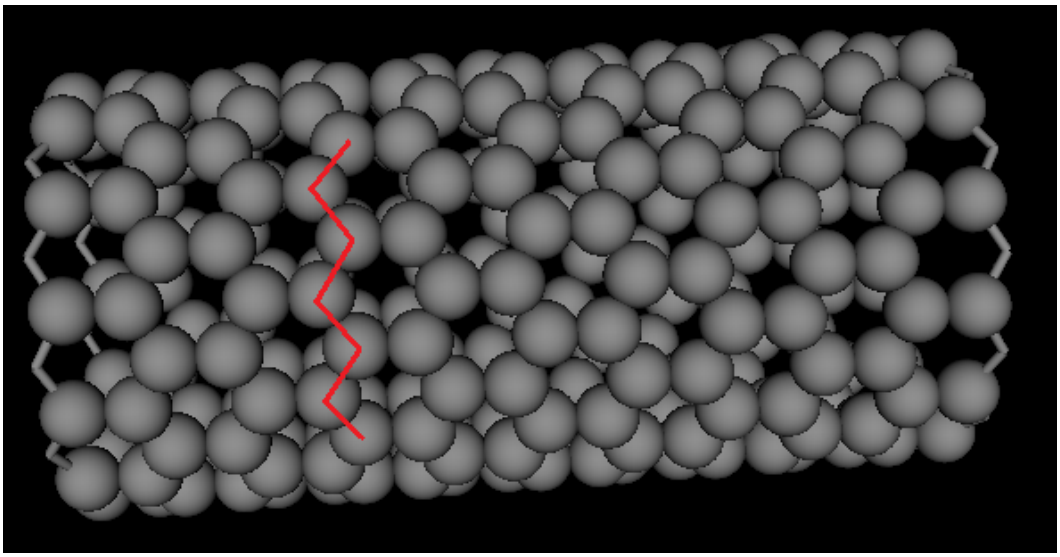

Figure 1.7. (12,0) zigzag carbon nanotube

$$E_g = \frac{0.766}{d} \tag{1.8}$$

where d is the diameter of the carbon nanotube in nm and E_g is the energy gap in eV (Hanson, 2008). Important electrical and physical characteristics of CNTs are summarized in Table 1.1 (Hoenlein et al., 2004).

Table 1.1. Electrical characteristics of CNTs

Electrical behaviour	Metallic or semiconducting
Electrical transport	Ballistic
Enegy gap	E_G [eV]=0.766/d [nm]
Maximum current density	10^{10} A/cm^2
Diameter	1-100nm
Length	Up to millimeters

1.2. Carbon Nanotube Interconnects

Clock pulse, other signals, power and ground lines in ICs are supplied among the circuit components via interconnects. In the current IC technology, copper (Cu) and aluminum (Al) are used as interconnects (May, 2006). However, according to ITRS interconnect roadmap, for the current interconnect technology, interconnect delays in 2010 was 2.1ps/mm and this value is expected to reach 3.2ps/mm in 2011 and 5.0ps/mm in 2012 (ITRS interconnect roadmap, 2010). The main reason of the increment in on-chip interconnect delays is the increment of the resistivities of interconnects. While the conductor resistivity for a Cu interconnect was 4.08μΩ .cm in 2010, it is supposed to be 4.48 μΩ.cm in 2011. The increase in the resistance of conventional bulk interconnects is caused from miniaturization, which increase electron surface scattering and grain-boundary scattering since the dimensions of interconnects become more comparable to the electron wavelength. On the other hand, the susceptibility of conventional interconnect materials to Joule heating and electromigration leads to the blockade of high current densities. The permissable current density for Cu interconnects is on the order of 10^6A/cm^2 which makes it difficult to use miniaturized interconnects to distribute power and ground around the IC. These drawbacks of the conventional interconnect technology leads to the investigations of various alternatives. One of these alternatives is metallic CNTs. The utilization of metallic CNTs as interconnects are feasible since the crystal structure of CNTs are almost ideal which enables ballistic electron transport with high current densities up to 10^{10}A/cm^2 (Kreupl et al., 2002), (Wei et al., 2001), (Choi et al., 2006),

(Massoud and Nieuwoudt, 2008). High thermal conductivity of CNTs, which is 1700-3000 W/mK together with the high current density and nanoscale dimensions make metallic CNTs ideal alternatives for the current interconnect technology. From electronics engineering point of view, accurate modelling of metallic CNTs are vital for the design and analysis of ICs containing CNT interconnects. This problem is also addressed in this thesis.

1.3. Carbon Nanotube Field Effect Transistors (CNTFETs)

Considering the disadvantages of bulk MOSFET miniaturization such as short channel effects, boundary scattering and leakage currents, CNTFETs are proposed as the alternatives of the current bulk MOSFETs. Semiconducting CNTs are utilized as channels in CNTFETs with a planar or cylindirical gate around the CNT channel. The advantages of CNTFETs over conventional MOSFETs stems mainly from the almost perfect crystal structure of semiconducting CNTs which provides high electron mobility and increased independence from fabrication variations. Ballistic transport in CNTFETs leads to lower loss, delay and heating which are crucial from IC engineering viewpoint (Lin et al, 2005a), (Javey et al, 2003). Another important advantage of CNTFETs is obviously their nanoscale dimensions.

CNTFETs operate by the modulation of the channel potential by the gate voltage. As in conventional Si MOSFETs, p-type and n-type CNTFETs can be obtained by doping. Intrinsically, CNT channel behaves as ambipolar, in other words permitting both electron and hole transport depending on the polarity of the gate voltage. However, in order to obtain unipolar current-voltage characteristics, doping is applied (Lin et al., 2005b), (Deng and Wong, 2006).

Utilization of CNTs as the main component of field effect transistors was realized in 1998 by Dekker's team as a back gated structure shown in Figure 1.8 (Tans et al., 1998).

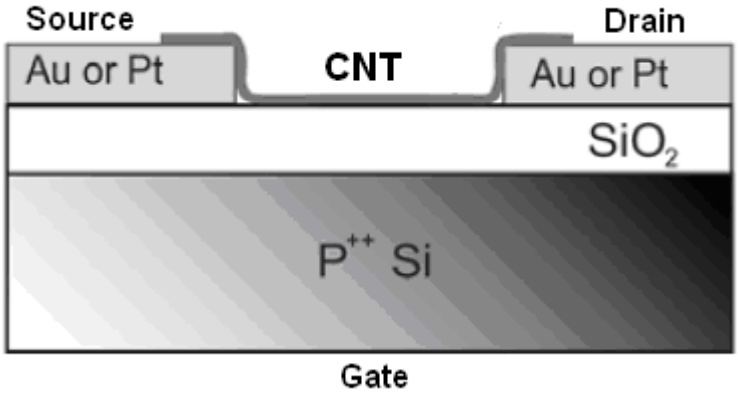

Figure 1.8. First implementation of CNTFET using a back gate (Tans et al., 1998)

Although the CNTFET structure shown in Figure 1.8 demonstrates the utilization of semiconducting CNTFETs, the practicality of this structure is not the best since the control of the back gate on the energy bands of the CNT channel is low due to the thickness of the gate oxide which has a value of 100nm resulting in low transconductance around 1nS. Moreover, since semiconducting CNT lays on the metal contacts, this causes high contact resistance which is around 1MΩ due to the weak bonds between semiconducting CNT and the metal (Avouris et al., 2004). These disadvantages of the first back-gated CNTFET structure directed researchers to develop CNTFET geometries with circuit parameters suitable for use in ICs. A better CNTFET sturucture employs the method that patterns source and drain contacts on the top of CNT channel as shown in Figure 1.9 (Martel et al., 2001). Thermal annealing is also used to improve CNT-metal interface to decrease contact resistance. The contact resistance of these type of devices are around 30kΩ, the saturation current is 1μA and the transconductance is around 0.3μS (Avouris et al., 2004). However, the drawback of the back gated CNTFET structure is their turn-on voltage, the voltage needed to be applied on the gate to shift the energy levels of the CNT channel so that current starts to flow through the device, is around 10V. Since lower voltage is advantageous in IC technology from power consumption point, it is clear that back-gated CNTFETs are not feasible for use in ICs. Apart from the high voltage needs, all back-gated CNTFETs on the wafer have to be switched at the same time since their gates are all the same. Hence, back-gated CNTFETs are not feasible

for the implementation of circuits requiring CNTFETs with gates connected to different nodes.

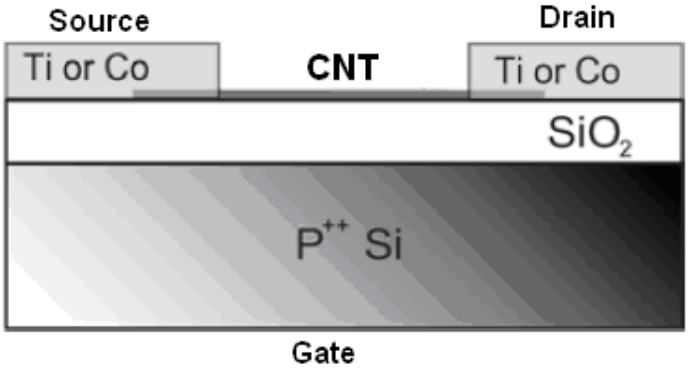

Figure 1.9. Back gated CNTFET with improved contacts (Martel et al., 2001)

It is obvious that, gate insulator thickness has to be small in order to achieve useable gate control. The top-gated CNTFET structure shown in Figure 1.10 provides threshold voltages as small as 0.2V and transconductance of 3.25μS (Wind et al., 2002). Subthreshold slope of top gated CNT is 2V/decade while back gated CNTFETs can only provide 130mV/decade.

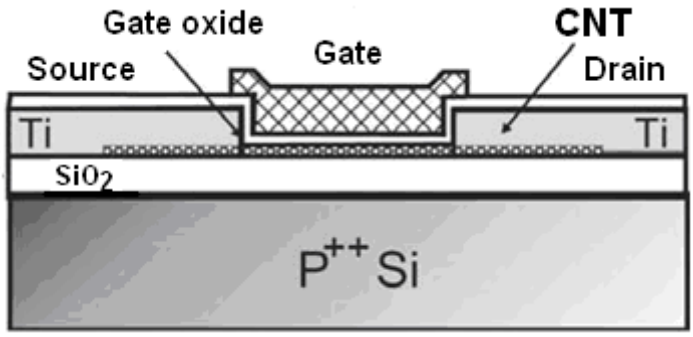

Figure 1.10. Top gated CNTFET structure (Wind, 2002)

In order to achieve better gate control, CNTFETs with cylindrical geometric shape, also named as gate all around (GAA) CNTFETs, are proposed. The geometry of a GAA CNTFET is shown in Figure 1.11 (Chen et al., 2008). Obtaining n-type or p-type devices in GAA CNTFET structures is easy since polarity can be set by doping the semiconducting CNTFET sections between gate insulator and source/drain contacts by n-type and p-type materials, respectively.

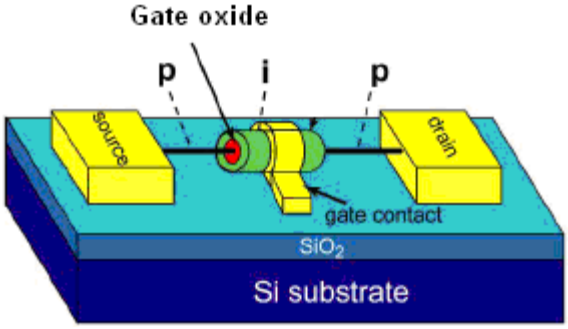

Figure 1.11. GAA CNTFET structure (Chen et al., 2008)

Since both planar and cylindrical top gate CNTFETs can be controlled by different gate signals on the IC, they are feasible for the implementation of versatile circuits in CNT technology. The comparison of conventional MOSFET prospects and CNTFETs is given in Table 2 (Hoenlein, 2003).

Table 1.2. Comparison of CNTFETs and MOSFET prospect of ITRS for 2016

Parameter	CNTFET	MOSFET prospect of ITRS for the year 2016
V_{dd} (V)	0.4	0.4
Drive current (μA/μm)	2500	1500
Transconductance (μS/μm)	15000	1000
Delay (ps)	0.08	0.15
Leakage current (μA/μm)	2.5	10
Effective oxide thickness (nm)	0.4	1

1.4. Summary of the Advantages of CNT Technology

The advantages of CNT technology over conventional IC technology can be summarized as follows.

1-) CNTs have very high mobility which provides high “on” current for CNTFETs over 1mA/μm.

2-) Chemical stability, strong chemical bonding and high thermal conductivity allow current densities up to 10^{10}A/cm^2.

3-) Gate insulators other than SiO_2 can be utilized in CNTFETs thanks to the absence of dangling bonds. This also helps to eliminate short channel effects.

4-) Complementary CNTFETs can be produced with better matching which is very important from IC point of view.

5-) Utilization of metallic and semiconducting CNTs on the same substrate is advantageous for integration.

1.5. Thesis Outline

This thesis covers accurate modeling of CNT interconnects and CNTFETs so that the developed models could easily be used in engineering tools by IC engineers. Previous studies are summarized together with their weak and strong points in Section 2. The tools used in the modelling of nanoscale devices are given in Section 3. Developed models for CNT interconnects and CNTFETs are presented in Section 4 and the overall study is concluded in Section 5.

2. RELATED WORKS

The literature on carbon nanotube technology in electronics engineering is reviewed in this section. Firstly, modelling and applications of CNT interconnects are given and then the studies regarding the modelling of CNTFETs are summarized. Section is concluded by explaining the missing parts in the previous studies; which are investigated in this thesis.

2.1. Studies Regarding Metallic CNT Interconnects

There are two modes in metallic CNTs in which the electron waves can travel. From the point of quantum conductance, there can be two electrons with opposite spins in these modes, hence the conductance of a single metallic CNT is given by the relation shown in Equation 2.1 (Avouris et al., 2004).

$$G = \frac{4q^2}{h} \tag{2.1}$$

In Equation 2.1, q is the charge of an electron and h is the Planck's constant (Naeemi et al., 2004). From a practical point of view, there are several studies on the feasibility of the utilization of metallic CNTs in integrated circuits. In (Wei et al., 2001), it is reported that CNT interconnect elements can stand to current densities more than 10^{10}A/cm^2 at 250^{o}C temperature without any measured change in its resistance. Hence, it is implied that the metallic CNTs can be used as interconnect elements in VLSI circuits. In another study, it is shown that metallic CNTs have ballistic transport property and can stand current densities of $5x10^9$A/cm^2 for 100 hours at 105^{o}C (Nihei et al., 2008). In (Naeemi et al., 2005), CNT interconnects are compared to copper interconnects and it is concluded that for 22nm technology, CNT interconnects has speed increments up to 80% compared to copper interconnects. CNT interconnects were reported to be produced in high densities and can be utilized as interconnect elements in VLSI circuits (Liu et al., 2007), (Li et al., 2003). The resistances of CNT-copper solder points are verified to have acceptable values,

which exist for outer world connections of VLSI integrated circuits (Sun et al., 2008). In (Close et al., 2007), it has been experimentally verified that the CNT elements can be used in VLSI circuits even if they are used with Al, Au, Ti and Pd contact elements. Methods to decrease the resistances by production processes are proposed and utilization of CNT interconnects as vias in VLSI circuits have been demonstrated in (Choi et al., 2006). In (Massoud et al., 2008), it is concluded that the delays of CNT interconnects can be decreased between 21% and 29% via the optimization of the CNT dimensions. CNT and gold interconnect components are compared and experimentally shown that CNT interconnects can be used with higher current densities in smaller areas in (Kreupl et al., 2002). In (Nihei et al., 2007), 0.05Ω resistance is reported for metallic CNTs when they are used as vias. Similarly, in another study, 2μm long CNT vias with 0.59Ω resistances are experimentally demonstrated (Sato et al., 2006). The studies until this point report that CNT interconnect components can be produced, they can be used in VLSI circuits and their delays and current densities are superior than the conventional interconnects.

There are also several studies regarding saturation current and the voltage dependent resistance variations of metallic CNTs. In one of these studies, the saturated current in a single metallic CNT is found to be 20μA using atomic simulations (Ouyang et al., 2007). Similarly, the saturation currents for very short metallic CNTs are obtained to have values up to 70μA in (Javey et al., 2004). In (Ahmadi et al., 2008a), the mechanisms that limit the electron velocity in CNTs are studied and it is concluded that the mean free path of an electron has to be greater than the length of the CNT in order to model the electron motion as ballistic. The voltage dependent resistances of metallic CNTs are modelled with a first order relationship using atomic calculations (Svizhenko et al., 2005). Similarly, the voltage dependent resistance variation in metallic CNTs are modelled using the data obtained from experiments in (Yao et al., 2000). The resistance dependency of metallic CNTs on the applied voltage level is measured and modelled in (Park et al., 2004).

It is obvious that, mathematical and circuit models for metallic CNTs are key in investigating the performances and speeding up the design process. There are several studies in the literature for this purpose. In one of these studies, electrons in

a CNT are considered with constant resistance and capacitance and a transmission line model is proposed (Maffuci et al., 2008). Another model, which is proposed in (Kordostami et al., 2008) considers the electrostatic capacitance modeling of metallic CNTs. Similarly, a circuit model for metallic CNTs is proposed by considering electrons in CNTs as Lüttinger liquid in (Burke, 2002) however the resistance is taken as lumped which is a drawback for the accuracy of the model.

There are also studies on the frequency dependent behaviour of metallic CNTs. Skin effect in CNTs and gold wires are compared and it is obtained that skin effect in metallic CNTs is less than the skin effect in gold wires in (Li et al., 2003). In (Tahvili et al., 2009) a high frequency distributed circuit model for CNTs is presented and the resistance and capacitance effects responsible for the high frequency behaviour is investigated. In another study regarding the transmission line characteristics of metallic CNTs, it is found out that short metallic CNTs exhibit lossless transmission line characteristics up to 1THz operating frequencies (Tahvili et al., 2009). Another high frequency model is developed in (Xu et al., 2009) and it is shown that for short CNTs (<1μm), the maximum operating frequency is 200GHz while for long CNTs (>1μm), the operating frequency is more than 10GHz.

In (Parkash et al., 2008), the parameters of CNT interconnect components are obtained using self-consistent calculations and then mathematically modelled. Equivalent circuit models for single walled CNT arrays are presented in (D'Amore et al., 2008) and then the signal delay is calculated. A CNT model is used in the simulations of a realistic microprocessor architecture and then performance variation using CNTs instead of copper are investigated in (Pasricha et al., 2009). Electronic properties of metallic CNT-copper junctions are obtained using simulations in (Sukirno et al., 2006). For IC applications, electrostatic capacitance calculations of CNTs are performed in (Wang et al., 2003).

2.2. Studies on the Modelling of CNTFETs

Modelling of electronic properties such as current-voltage variation and quantum capacitance of CNTFETs are critical for the analysis and design of ICs

utilizing CNTFETs. Thus, there are several studies in the literature for the modelling of CNTFETs. These studies are summarized in this subsection.

The current-voltage relationship of a CNTFET is explained from Equation 2.1 to Equation 2.7 in (Rahman et al., 2003).

$$I_{DS} = \frac{4qk_BT}{h}\left(\ln\left(1+e^{\frac{E_F-U_{SCF}}{k_BT}}\right)-\ln\left(1+e^{\frac{E_F-qV_{DS}-U_{SCF}}{k_BT}}\right)\right) \tag{2.2}$$

In Equation 2.2, q is the charge of an electron, k_B is Boltzmann's constant, T is absolute temperature, h is Planck's constant, E_F *is* the Fermi energy of the source electrode and V_{DS} is the drain-source voltage. U_{SCF} is the electrical potential of the CNT channel which is dependent on source, drain, gate voltages and source-channel, channel-drain and gate-channel capacitances as shown in Equation 2.3.

$$U_{SCF} = -q\left(V_G\frac{C_G}{C_{TOT}}+V_S\frac{C_S}{C_{TOT}}+V_D\frac{C_D}{C_{TOT}}\right)+q\left(\frac{qN_1(U_{SCF})+qN_2(U_{SCF})-qN_0(U_{SCF})}{C_{TOT}}\right) \tag{2.3}$$

In Equation 2.3, C_G is the gate-channel capacitance, C_D is the drain-channel capacitance and C_S is the source-channel capacitance. C_{TOT} is the total of these three capacitances. N_0, N_1 and N_2 are the electron densities of channel, source and drain that are functions of U_{SCF} as given in Equations 2.4, 2.5 and 2.6 respectively.

$$N_0 = \int_{-\infty}^{\infty} D(E)\,f(E-E_F)dE \tag{2.4}$$

$$N_1 = \frac{1}{2}\int_{-\infty}^{\infty} D(E)\,f(E+U_{SCF}-E_F)dE \tag{2.5}$$

$$N_2 = \frac{1}{2}\int_{-\infty}^{\infty} D(E)\,f(E+U_{SCF}+qV_{DS}-E_F)dE \tag{2.6}$$

where *D(E)* is the density of states function of the channel and *f(E)* is Fermi-Dirac probability density function as given in Equation 2.7 and Equation 2.8, respectively.

$$D(E) = \frac{8E}{3pg\,b\sqrt{E^2 - E_p{}^2}} \tag{2.7}$$

$$f(E) = \frac{1}{1 + e^{\frac{E - E_F}{k_B T}}} \tag{2.8}$$

where γ_0 is the carbon–carbon bond energy, b is the carbon-carbon bond length and E_p is the highest energy of the p^{th} subband (Raychowdhury et al., 2004).

The current-voltage variations can be obtained from these equations in a mathematical computing environment. However, electron density and channel potential have to be calculated in an iterative manner.

A CNTFET model suitable for use in SPICE is presented in (Raychowdhury et al., 2003) and (Raychowdhury et al., 2004) which is shown in Figure 2.1. In this model, C_{GD} and C_{GS} are the gate-drain and gate-source capacitances, respectively. This model utilizes fitted functions for the calculation of the channel potential in order to be able to use the model in circuit design environments. The electron density of the channel is given by the fitted function given in Equation 2.9.

$$N = \begin{cases} N_0 A e^x, & x < 0 \\ N_0 (Bx + C), & x \geq 0 \end{cases} \tag{2.9}$$

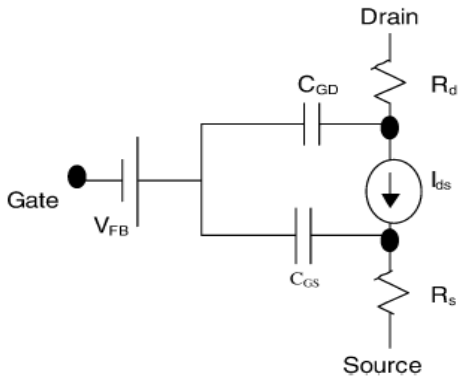

Figure 2.1. CNTFET model proposed in (Raychowdhury et al., 2004)

In Equation 2.9, *A*, *B* and *C* are fitting parameters which are given in Equation 2.10 and 2.11, respectively.

$$A = -5.3U_p^{\,2} + 10U_p + 1 \tag{2.10}$$

$$B = 0.34U_p + 1, \quad C = 0.12U_p \tag{2.11}$$

$$x_i = \left(\frac{m_i - U_p - U_{CNT}}{k_B T} \right) \tag{2.12}$$

Here U_p *is* p[th] subband potential, U_{CNT} is the channel potential, μ_i is the Fermi energy of the drain or source electrode. The channel potential is given in terms of V_{GS} and V_{DS} as Equation 2.13.

$$U_{CNT} = \begin{cases} V_{GS}, & V_{GS} < \Delta_1 \\ V_{GS} - a\,(V_{GS} - \Delta_1), & V_{GS} \geq \Delta_1 \end{cases} \tag{2.13}$$

$$a = a_0 + a_1 V_{DS} + a_2 V_{DS}^{\,2} \tag{2.14}$$

The values of α for some CNT dimensions are given in (Raychowdhury et al., 2004) however a general expression is not provided. The value of the current source is given as in Equation 2.15.

$$I_D = \frac{4qk_BT}{h} \sum_n \left[\ln\left(1 + e^{-x_S}\right) - \ln\left(1 + e^{-x_D}\right) \right] \tag{2.15}$$

The capacitances are given as in Equation 2.16 as fitted functions.

$$C_{Gi} = \begin{cases} qN_0 \dfrac{AL}{k_B T} e^{x_i}, & x_i < 0 \; ve \; V_{GS} \le E_{Ci} \\ qN_0 \dfrac{AL}{k_B T} e^{x_i} (1-a), & x_i < 0 \; ve \; V_{GS} \ge E_{Ci} \\ qN_0 \dfrac{BL}{k_B T}, & x_i \ge 0 \; ve \; V_{GS} \le E_{Ci} \\ qN_0 \dfrac{BL}{k_B T} (1-a), & x_i \ge 0 \; ve \; V_{GS} \ge E_{Ci} \end{cases} \quad (2.16)$$

where L is the channel length and E_{ci} is the conduction band minimum. The drawback of this model is providing fitting parameters for only limited CNTFET dimensions and the limited accuracy due to the usage of fitting functions.

There are also studies where CNTFET model parameters are calculated from measured characteristics. For instance, the CNTFET model of Figure 2.2 is proposed in (Bethoux et al., 2006) where equivalent circuit parameters are calculated from experimental values. The circuit parameters are calculated as R_{gs}=1.8kΩ, R_{gd}=1.4kΩ, C_{gs}=3.3fF, C_{gd}=1.3fF from the frequency dependent transconductance and output conductance are obtained as in Figure 2.3.

The drawback of the model of Figure 2.2 is that the parameters are calculated for only a few CNTFET geometries due to the utilization of experimental method to determine the model parameters.

In (Ahmadi et al., 2008b) a current–voltage equation for CNTFETs is given as shown in Equation 2.17.

$$I_D = \frac{mC_G}{2L} \frac{\left[2(V_{GS} - V_T)V_D - V_D{}^2\right]}{1 + \dfrac{V_D}{V_C}} \quad (2.17)$$

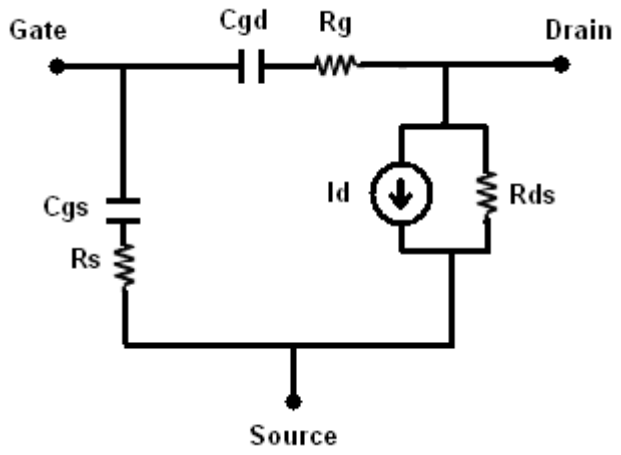

Figure 2.2. The high frequency CNTFET model (Bethoux et al., 2006)

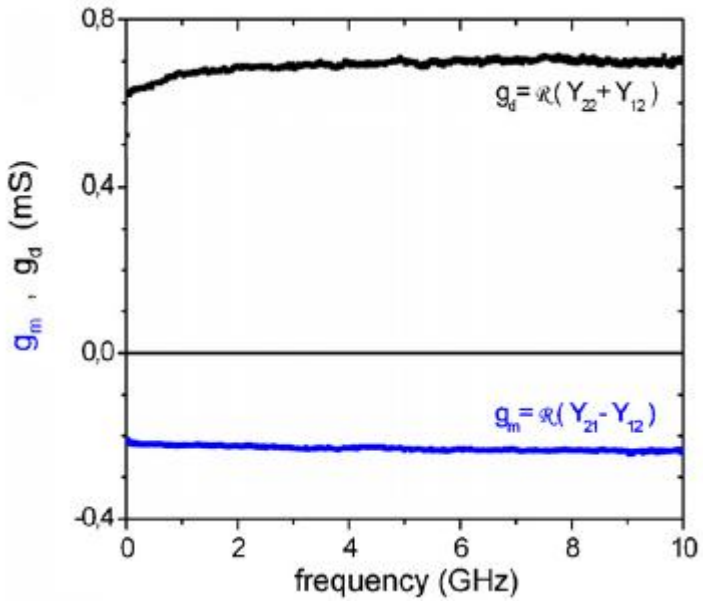

Figure 2.3. Frequency dependent variation of transconductance and output conductance (Bethoux et al., 2006)

In Equation 2.17, C_G is the unit length gate capacitance, V_C is the critical voltage and L is the channel length. C_G and V_C are given as in Equations 2.18 and 2.19, respectively.

$$C_G = \frac{C_e C_Q}{C_e + C_Q} \tag{2.18}$$

$$V_C = \frac{v_{sat} L}{m_e} \tag{2.19}$$

where C_e is the electrostatic capacitance of the gate while C_Q is the quantum capacitance of the gate, v_{sat} is the saturation velocity of the electrons, L is CNT length and μ_e is electron mobility. The current-voltage characteristics of the CNTFET can be obtained using these equations up to a limited accuracy since CNTFET is considered as a bulk structure to derive the model equations which is not accurate for nanoscale devices.

A model for coaxially gated; in other words gate all around; CNTFETs is given from the data obtained from atomic simulations in (Polash and Huq, 2008). However the model is not versatile for several types and dimensions of CNTFETs.

A mathematical model for the current–voltage relation of the CNTFET is given in (Akinwande et al., 2008a). In this model, drain current is given as in Equation 2.20.

$$I_D = \frac{k_B T}{q R_{eq}} \left[\ln\left(1 + e^{\frac{2qj_S - E_g}{2k_B T}}\right) - \ln\left(1 + e^{\frac{2qj_S - 2qa_A V_D - E_g}{2k_B T}}\right) \right] \tag{2.20}$$

where α_A is an emprical fitting parameter that is calculated from experimental data.

A couple of CNTFET models with different accuracies are proposed in (Deng et al., 2007a) and (Deng et al., 2007b) as shown in Figure 2.4. These models include the current-voltage calculation, quantum capacitance calculation and drain/source contact resistances. Furthermore, these models are implemented in Verilog-A hardware description language in order to provide utilization in circuit design and simulation environments. However, the CNT channel potential is again given with

fitting functions which limits the accuracy of the models in the whole input voltage range.

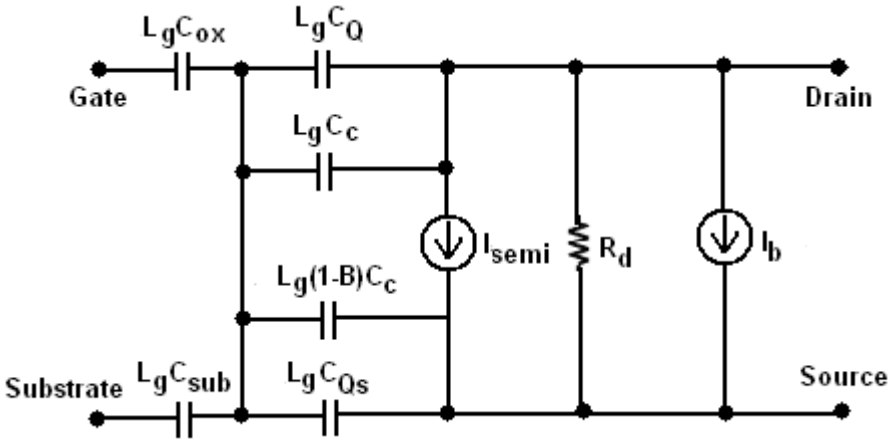

Figure 2.4. CNTFET model proposed in (Deng et al., 2007b)

A fitted DOS function is used in this model which is valid in the voltage range given in Equation 2.21.

$$V_i \leq \frac{g_0}{q} \tag{2.21}$$

where γ_0 is the C-C bonding energy. Hence, the main disadvantage of these models is that the utilization of fitted model parameters valid in an input voltage range.

2.3. Review of the Previous Studies

Considering the models of metallic CNT interconnects and CNTFETs existing in the literature, the following missing points are determined.

a) Most of the models take the resistance of metallic CNTs as having a constant value. However, resistance value depends on the electronic operating conditions namely the applied voltage and the current passing through the device.

The variation of the resistance of CNT interconnects are considered in three main studies. In one of these studies, voltage drop along the length of the CNT is computationally studied in order to model the voltage drop of CNT–metal electrode junctions (Svizhenko and Anantram, 2005). However, in this study, a voltage dependent qualitative resistance model is not given. In another study, the effects of inelastic phonon scattering and elastic electron–crystal scattering are considered (Yao et al., 2000). Combining these two scattering processes via Mattheissen's rule, a qualitative voltage dependent resistance model fitting to experimental values is given. Although, this approach is elegant, the model is questionable due to these reasons: usage of metallic electrical contacts whose junction with CNT introduces experimental errors such as contact scattering and the temperature of the experiment is 200K, which is below the realistic operating conditions of electronic circuits. Experimental I–V relationships up to 1.4V and 1.5V are given, respectively in (Javey et al., 2003) and (Park et al., 2004), for various CNT lengths and then the mean free paths of electrons are calculated. However, in these studies, CNTs are very long and voltage dependent resistances up to 3.3V or 5V voltages are not given. Moreover, the resistance variation due to the modulation of the transmission channels by the applied voltage is not considered in the previous studies, which affects the resistance of shorter CNT interconnects. Modelling of the resistance of short CNT interconnects is vital for IC engineers since there are high number of interconnects in an IC connecting near components. Furthermore, a mathematical model for the resistance variation suitable for integration into electronic design automation (EDA) tools is not given in these previous studies. Modelling the resistance variation in short CNT interconnects suitable for integration into EDA tools is one of the issues addressed in this thesis.

b) CNT interconnect models in the literature take constant values for the quantum capacitance, C_Q, independent of the applied voltage on the CNT (Srivastava and Banerjee, 2005), (Burke, 2002), (Xu and Srivastava, 2009). However, the value of the quantum capacitance changes when the applied voltage on the CNT is changed. This is due to the variation of the energy of traveling electrons (John et al.,

2004). Hence, in order to accurately model the CNTs, the quantum capacitance of CNTs has to be modelled dependent on the applied voltage. In a study, the variation of quantum capacitance is measured in experiments for a few CNTs however a general and convenient method to obtain the quantum capacitance of CNTs is not given (Ilani et al., 2006). A method for obtaining quantum capacitance of CNTs is presented in this thesis, which does not involve experimental measurements hence convenient for the CNT circuit designer.

c) The performance metrics of an interconnect element are its delay and current carrying capacity (Srivastava and Banerjee, 2005). However, delay is the most important parameter when interconnects carrying high speed signals are considered. There are several studies for estimating the delays of metallic CNT interconnects in the literature. In one of these studies, a transmission line model for CNT interconnects is given which employs constant contact resistance and quantum capacitance of 6.5k and 100aF/µm, respectively (Burke, 2002). In another study, although the resistance of carbon nanotubes is taken as voltage-dependent, the quantum capacitance is again considered having a constant value of 100aF/µm (Raychowdhury and Roy, 2006). The quantum capacitance is completely ignored in (Naeemi et al., 2007). Characterization of CNT interconnects is studied also in (Close and Wong, 2007) which models the resistance of CNTs as 6.8k and an equivalent capacitance of 1.5fF. In another study, the comparison of CNT interconnects and Cu alternatives are studied without considering voltage-dependent resistance and capacitance (Koo et al., 2007). Diameter-dependent parameters of CNT interconnects are investigated however the quantum capacitance is taken as constant having a value of 400aF/µm in (Maffuci et al., 2009) which leads to voltage-independent delay calculation. Resistances and capacitances of CNTs, hence the delay, are also taken as voltage-independent in (Nieuwoudt and Massound, 2006) and (Srivastava et al., 2009). An improved metallic CNT model is provided in (Xu and Srivastava, 2009), however, the quantum capacitance is considered to have a constant value of 90aF/µm. Considering these studies, it is seen that most of the previous studies on metallic CNT interconnect delays do not consider the voltage-

dependency of the resistance and none of them consider the voltage-dependency of the CNT capacitance. However, as it is pointed out, the resistance of metallic CNTs is dependent on the applied voltage and the quantum capacitance of CNT interconnects varies due to the additional subbands contributing the conduction as the applied voltage changes. Hence, it is obvious that the delays of CNT interconnects have to be calculated considering the voltage-dependencies of CNT resistance and capacitance. This type of delay calculation has not been studied in the literature before. The accurate calculation of CNT delay using voltage-dependent resistance and capacitance values is also addresses in this thesis.

d) Previous studies considering the nonlinear current-voltage characteristics of metallic CNTs regard the nonlinear resistance as a fact that has to be minimized as much as possible. This approach is valid when metallic CNTs are used as interconnects since the resistance of interconnect components are desired to have constant and low values in order to transmit the electrical signals as smooth as possible and without any distortion. In this study, it is also shown that the nonlinear behaviour in current-voltage characteristics of metallic CNTs can be utilized to design novel and compact nanoscale circuit architectures.

e) CNTFET models existing in the literature can be classified into two groups. The first group of studies utilize self-consistent simulations, in other words the calculation of CNT channel potential in an iterative manner using the applied voltages. These studies are available in various computation environments such as MATLAB and ViDES. Second group of studies include the calculation of the CNT channel potential by using fitted functions of the applied voltage and implemented in SPICE environment suitable for electronic engineers, which are less accurate. In conclusion, CNTFET models both utilizing accurate self-consistent method to calculate CNT channel potential and suitable for use in SPICE by electronic engineers do not exist in the literature. This is also completed in this thesis.

3. MATERIALS AND METHODS

The methods used to analyse nanoscale components and quantum mechanical simulation of nanodevices are given in this section which constitutes the basis for the modelling and simulation work in this thesis.

3.1. Landauer's Formulation

The current–voltage characteristics of nano-scaled devices are calculated using the transmission spectrum approach (Durkan, 2007). A general nanoscale electronic device can be sketched as in Figure 3.1.

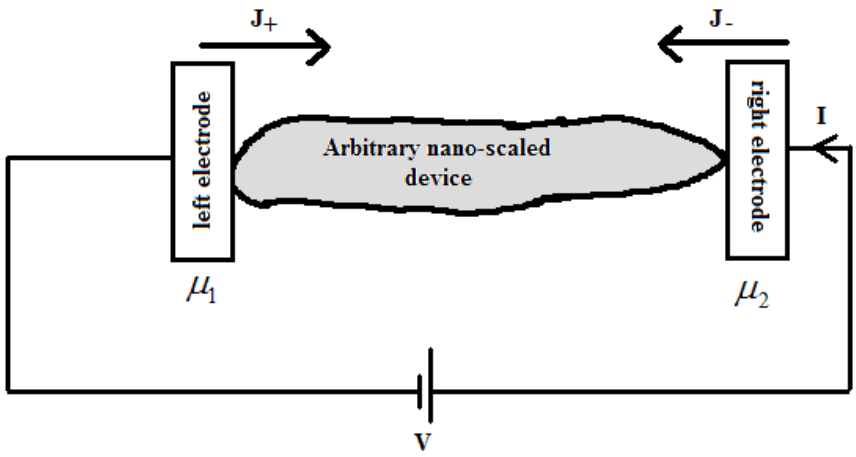

Figure 3.1. A general nanoscaled device with a voltage applied on it

In nanoscale electronic devices, the wavelength of the travelling electrons are on the order of the scale of the device, so the electronic motion has to be considered with reflection and transmission concepts. From this viewpoint, the electrons injected from the right hand side of the nanoscaled device of Figure 3.1 will be either transmitted into the device or reflected back towards the source. The probability of an electron having the energy *E* to transmit into the device is called as the transmission probability at energy *E* and expressed by *T(E)*. Transmission spectrum is the name given to the function *T(E)* over the whole energy range.

Moreover, the number of electrons flowing through the device is given using quantum mechanical treatments. Considering the nanoscale device model of Figure 3.1, the current density provided by the electrons injected into the nanoscale device from left hand side, J_+, is written as in Equation 3.1.

$$J_+(k) = 2qn(k)v_e(k)T(k)dk \tag{3.1}$$

where q is the charge of an electron, $n(k)$ is the number of electrons with wave vector k and flowing from left to right, $v_e(k)$ is the velocity of electrons having wave vector k and flowing from left to right and $T(k)$ is the transmission probability of electrons travelling from left hand side to the right hand side of nanoscaled device. On the other hand, the number of electrons having wave vector k can be written as the product of density of states function $D(k)$ and the Fermi–Dirac probability distribution function $f(k)$ as given in Equation 3.2.

$$n(k) = D(k)\,f(k) \tag{3.2}$$

The velocity of electrons having wave vector k can also be derived as in Equation 3.4 from the momentum expression of Equation 3.3.

$$mv_e(k) = \mathbf{h}k \tag{3.3}$$

$$v_e(k) = \frac{\mathbf{h}k}{m_e} \tag{3.4}$$

In Equation 3.4, m_e represents the mass of electrons inside the nanoscale device. Wave vector k can be given as a function of electron energy as in Equation 3.6 using Equation 3.5.

$$E = \frac{\mathbf{h}^2k^2}{2m_e} \tag{3.5}$$

Infitismall differential *dk* can be derived from Equation 3.5 as shown in Equation 3.6.

$$dk = \frac{m_e dE}{\mathbf{h}^2 k} \tag{3.6}$$

The total current in the $+x$ direction is the sum of all currents provided by the electrons having positive wave number, hence can be expressed as in Equation 3.7.

$$J_+ = \int_0^\infty 2qn(k)v_e(k)T(k)dk \tag{3.7}$$

Using Equations 3.1 to 3.7, the total current density flowing in the +x direction in terms of energy dependent functions can be given as in Equation 3.8.

$$J_+ = \frac{2q}{\mathbf{h}} \int_0^\infty D(E) f(E) T(E) dE \tag{3.8}$$

Equation 3.8 gives the current that will be formed by considering all the electrons that can have all the energies. However, the electrons injected from the left side can have energies from zero to the electrochemical potential of the left contact, μ_1, thus the limits of the integral of Equation 3.8 can be set as $[0, \mu_1]$. So, the current density formed by the electrons injected from left hand side contact can be rewritten as in Equation 3.9.

$$J_+ = \frac{2q}{\mathbf{h}} \int_0^{m_1} D(E) f_1(E) T(E) dE \tag{3.9}$$

Similarly, the electrons flowing from right to left provide the J_- current as given in Equation 3.10 where μ_2 is the electrochemical potential of the right electrode.

$$J_{-} = \frac{2q}{\mathbf{h}} \int_{0}^{m_2} D(E)\, f_2(E) T(E) dE \tag{3.10}$$

Hence, the net current density J_{net} can be expressed as the difference of two currents flowing in opposite directions which is shown in Equation 3.11 and Equation 3.12.

$$J_{net} = J_{+} - J_{-} = \frac{2q}{\mathbf{h}} \int_{0}^{m_1} D(E)\, f_1(E) T(E) dE - \frac{2q}{\mathbf{h}} \int_{0}^{m_2} D(E)\, f_2(E) T(E) dE \tag{3.11}$$

$$J_{net} = \frac{2q}{\mathbf{h}} \int_{m_1}^{m_2} D(E)\left[f_1(E) - f_2(E) \right] T(E) dE \tag{3.12}$$

Equation 3.12 is called as Landauer's formula (Durkan, 2007) and is used for the calculation of the current-voltage characteristics of nanoscale electronic devices. The accuracy of Landauer's formula is verified by various experiments (Datta, 2005).

3.2. Non-Equilibrium Green's Function Formalism (NEGF)

Density of states functions and transmission spectra of carbon nanotubes have to be calculated for obtaining the current-voltage relation of carbon nanotube devices as shown in the previous subsection.

If the density of states function of the channel region of Figure 3.1 is ***D(E)***, coupling to the contacts affects the density of states function as in Equation 3.13.

$$D(E,U) = \frac{g / 2p}{\left(E - e - \Delta - U\right)^2 + \left(g / 2\right)^2} \tag{3.13}$$

where γ and Δ are the shift and broadening of the energy levels and U is the potential created by the electrons inside the channel region due to the electrode potentials (Datta, 2005). The number of electrons in the channel region is then given

by Equation 3.14.

$$N = \int_{-\infty}^{\infty} \left(\frac{g_1}{g_1 + l_2} f_1(E) - \frac{g_2}{g_1 + g_2} f_2(E) \right) D(E,U)\, dE \tag{3.14}$$

where γ_1 and γ_2 are the coefficients describing the electron flow rate at the first and second electrode, respectively. Right hand and left hand currents are respectively given as in Equations 3.15 and 3.16.

$$I_1 = \frac{2qg_1}{\mathbf{h}} \int_{-\infty}^{\infty} D(E,U)\left(f_1(E) - N \right) dE \tag{3.15}$$

$$I_2 = \frac{2qg_2}{\mathbf{h}} \int_{-\infty}^{\infty} D(E,U)\left(f_2(E) - N \right) dE \tag{3.16}$$

The sum of I_1 and I_2 has to be zero at equilibrium state, for $f_1(E)$ is equal to $f_2(E)$, so obtaining N from Equation 3.14 and inserting into Equation 3.15 and Equation 3.16 gives the current through the nanodevice as in Equation 3.17 (Datta, 2002).

$$I_1 = -I_2 = I = \frac{2q}{\mathbf{h}} \frac{g_1 g_2}{g_1 + g_2} \int_{-\infty}^{\infty} \left(f_1(E) - f_2(E) \right) D(E,U)\, dE \tag{3.17}$$

Equation 3.17 can be written in Landauer's form as in Equations 3.18 and 3.19.

$$I = \frac{2q}{h} \int_{-\infty}^{\infty} \left(f_1(E) - f_2(E) \right) \underbrace{D(E,U) \frac{2pg_1 g_2}{g_1 + g_2}}_{T(E,U)} dE \tag{3.18}$$

$$I = \frac{2q}{h} \frac{g_1 g_2}{g_1 + g_2} \int_{-\infty}^{\infty} \left(f_1(E) - f_2(E) \right) T(E,U)\, dE \tag{3.19}$$

The potential created by the electrons, *U*, is a function of the number of electrons. However, the number of electrons is also related to the potential of the channel region as given in Equation 3.15. Hence, iterative methods have to be utilized to calculate the number of electrons and the potential created by the electrons in the channel region. After this calculation, the current flowing through the device can be obtained by Equation 3.18. This self–consistent method is shown in Figure 3.2.

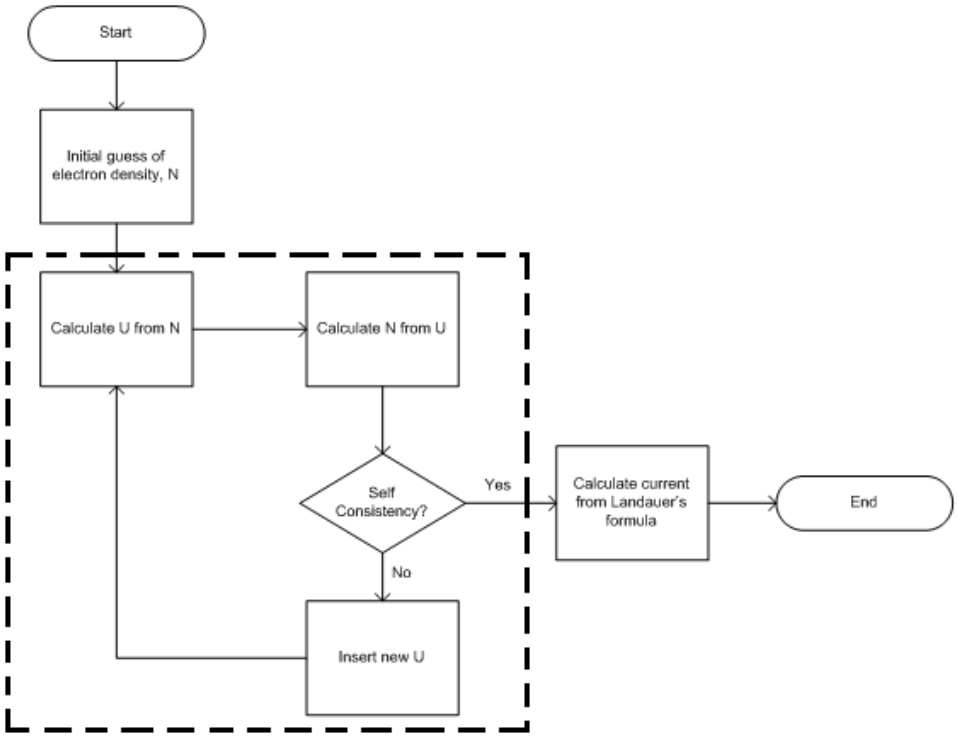

Figure 3.2. Current calculation procedure by self-consistent method

For a nanoscaled device, there will be many energy levels ε_n in which electrons can pass through the device. Number of electrons in the channel and the current of passing through the device can be expressed using matrices as in Equation 3.20 and Equation 3.21, respectively (Datta, 2002).

$$N = \frac{1}{2p}\int_{-\infty}^{\infty}\left[A_1(E,U)\,f_1(E) + A_2(E,U)\,f_2(E)\right]dE \tag{3.20}$$

$$I = \frac{q}{h}\int_{-\infty}^{\infty}\left(f_1(E) - f_2(E)\right)T\left(E,U\right)dE \tag{3.21}$$

where

$$G = [EI - H - \Sigma_1 - \Sigma_2]^{-1} \tag{3.22}$$

$$\Gamma_{1,2} = j\left[\Sigma_{1,2} - \Sigma_{1,2}{}^{+}\right] \tag{3.23}$$

$$A_{1,2} = G\Gamma_{1,2}G^{+} \tag{3.24}$$

$$T(E,U) = Tr\left[\Gamma_1 G \Gamma_2 G^{+}\right] \tag{3.25}$$

In Equations 3.22 to 3.25, Σ_1 and Σ_2 are the self energy matrices of the first and second contact and H is the Hamiltonian matrix whose eigenvalues give the allowed energy levels. Equations 3.20 to 3.25 are the known as equations of the non–equilibrium Green's function formalism (NEGF) since they consider systems at non–equilibrium, in other words, the electrons are not in equilibrium state where there is electron flow through the channel region, and the current is calculated using Green's function approach (Datta, 2005).

The transmission spectrum and the current of a realistic nanoscaled device can be calculated using Equations 3.20 to 3.25. However, the variation of the potential U inside the channel has to be calculated using number of electrons, N. Hence, NEGF is not enough to calculate the current–voltage characteristics, an accurate method to calculate the electron density and the potential of the channel region self-consistently is also necessary. This calculation can be performed using density functional theory which is explained in the following section.

3.3. Density Functional Theory (DFT)

In nanodevices, the solution to the many-body Schrödinger equation is required for the calculation of the electron density and the channel potential. The many-body Schrödinger equation is given in Equation 3.26 (Stokbro et al., 2005).

$$\hat{H}\Psi(\vec{r}_1, \vec{r}_2, ..., \vec{r}_N) = E_0\Psi(\vec{r}_1, \vec{r}_2, ..., \vec{r}_N) \tag{3.26}$$

$$\hat{H} = -\sum_{i=1}^{N}\frac{\hbar^2}{2m}\nabla_i^2 - \sum_{i=1}^{n}\sum_{m=1}^{N}\frac{Z_m q^2}{|\vec{r}_i - \vec{R}_m|} + \frac{1}{2}\sum_{i,j=1}^{n}\frac{q^2}{|\vec{r}_i - \vec{r}_j|} \tag{3.27}$$

In Equation 3.26, $\hat{H}$ is the Hamiltonian operator of the system, E_0 is an energy eigenvalue and $\Psi(\vec{r}_1, \vec{r}_2, ..., \vec{r}_N)$ is the joint electron wavefunction. The Hamiltonian operator of the system is given in Equation 3.27. In this equation, $\hbar$ is reduced Planck's constant, q is elementary charge, m_e is electron mass, Z_μ is the ion charge, $\vec{r}_i$ is ith electron position, $\vec{r}_j$ is jth electron position, $\vec{R}_m$ is μth ion position, N is the number of ions and n is the number of electrons. In this equation, the first term represents the kinetic energy, second term is the electrostatic electron-ion attraction term and the last term is electron-electron repulsion term. Since electron-electron repulsion term correlates different electrons, an exact solution is not possible. Hence, approximations are needed to reduce many body Schrödiner equation to a tractable model. One of these methods that is widely used in electronic simulations is density functional theory (DFT). Effective one-electron equations are obtained from many-body electron equation as shown in Equations 3.28 to Equation 3.30 using DFT (Stokbro et al., 2005). DFT considers the electrons as non-interacting particles in an effective potential denoted by $V^{eff}[n](\vec{r})$. The name DFT is given to this method since the potentials are expressed as functionals of the electron density (Brandbyge et al., 2002). The effective potential $V^{eff}[n](\vec{r})$ includes the potential of electron-electron interactions and the exchange-correlation potential. Selection of exchange-correlation functional is important for the accuracy of the solution (Abadir et al., 2009).

$$\hat{H}_{1el} = -\frac{\hbar^2}{2m_e}\nabla^2 + V^{eff}[n](\vec{r}) \tag{3.28}$$

$$\hat{H}_{1el}\psi_a(\vec{r}) = \varepsilon_a \psi_a(\vec{r}) \tag{3.29}$$

$$n(\vec{r}) = \sum_{\varepsilon_a < m} |\psi_a(\vec{r})|^2 \tag{3.30}$$

where $\hat{H}_{1el}$ is single-electron Hamiltonian and ψ_a is single electron wavefunction of the a^{th} electron. The above equations are called as Kohn-Sham equations (Kohn and Sham, 1965). In Kohn–Sham equations, since the effective potential is a functional of the electron density, Equations 3.28 and 3.30 have to be solved self–consistently to perform the required steps shown in dashed lines in Figure 3.2 (Brandbyge et al., 2002). Obtaining self–consistent solution of Kohn–Sham equations is tractable with today's computer technology.

In this thesis, a commercial DFT–NEGF simulation package, ATK from Quantumwise A/S, is utilized to obtain various electronics related parameters of carbon nanotubes (ATK, 2011). Current-voltage variation, charge-voltage variation and electron density variations in metallic CNT interconnects are also obtained using ATK. On the other hand, electrical characteristics of CNTFETs are obtained using an online self-consistent atomic simulator named cylindrical CNTFET simulator available on Nanohub (Nanohub, 2010). The results obtained using these simulators for CNT interconnects and CNTFETs and the models proposed in this thesis are given in the following section.

3.4. Proposed Methods

The methods for the modelling of voltage-dependent resistance, voltage-dependent capacitance, transmission line modelling of CNTs and the self-consistent modelling of CNTFETs are given in the following section.

4. RESULTS AND DISCUSSION

The results obtained in this thesis are given in this section which comprises 7 subsections given as follows.

a) Obtaining the voltage-dependent resistance of CNTs and modelling with polynomial functions,

b) Modelling the nonlinear CNT resistance with neural networks,

c) Utilization of the nonlinear CNT resistance as an advantage to design novel nanoscale circuits,

d) Modelling the voltage-dependent capacitance of CNTs,

e) Proposal of a voltage-dependent transmission line model for CNTs and accurate delay calculation,

f) Proposal of an accurate CNTFET model utilizing self-consistent calculation of the channel charge and suitable for use in SPICE environment,

g) Simulation of basic CNTFET circuit blocks using the proposed CNTFET model.

4.1. Voltage-Dependent Resistance of CNTs and Its Polynomial Model

4.1.1. Resistance of CNT Interconnects

There are voltage-dependent resistance expressions for long CNTs with electrical transports which is not ballistic in the literature (Hanson, 2008) however, there is not any voltage-dependent resistance model for short CNTs and this problem is addressed in this thesis (Yamacli and Avci, 2009). In (Naeemi et al., 2004), it is shown that the total resistance of a metallic CNT can be decomposed as a sum of fundamental resistance, the length dependent resistance and voltage dependent resistance as given in Equation 4.1.

$$R_T = R_{fundamental} + R_{length\_dependent} + R_{voltage\_dependent} \quad (4.1)$$

For short CNTs, the resulting equation for the total resistance can be written as in Equation 4.2 ($R_{lenght\_dependent} \approx 0$).

$$R_T(V) = R_{fundamental} + R_{voltage\_dependent}(V) \tag{4.2}$$

where $R_T(V)$ is the voltage dependent total resistance, which is considered and modeled in this study for the first time in the literature (Yamacli and Avci, 2009).

4.1.2. DFT-NEGF Simulations to Obtain CNT Resistance

In this work, (4,4) and (5,5) SWCNTs that exhibit metallic properties are considered and modelled as examples of CNT interconnects. (4,4) and (5,5) CNTs have 2.71Å and 3.39Å radii, respectively. Since the aim is the extraction of voltage dependent resistance of CNTs, electrodes through which the bias voltage is applied are also selected as the same type of CNT to eliminate contact scattering. Central regions, screening layers and the electrodes of the simulated sections are taken as 5 periods, 2 periods and 3 periods, respectively. Hence, the lengths of the central regions, screening regions and the electrodes respectively are 12.29Å , 4.91Å and 7.37Å for both (4,4) and (5,5) CNTs. The length values are selected as to eliminate the length–dependency of resistance, suitable for both eliminating the possible errors caused by the interactions of electrodes and reasonable simulation cost. The simulated geometries are shown in Figure 4.1 and Figure 4.2, for (4,4) and (5,5) CNTs, respectively. Electrodes are shown by (S1, S2, SC).

The DFT–NEGF simulation parameters are selected as the following: mesh cut–off energy is 400Ry, basis set is double zeta polarized with 0.001Bohr radial sampling, exchange correlation functional is local density approximation (LDA) type with double zeta polarized (DZP) basis set; these parameters are chosen to provide accurate results as pointed in (Abadir et al., 2009).

Brillouin zone integration parameters of electrodes are taken as (1,1,500), electronic temperature is 300K, Green's function infinitismall is 10^{-5}. The currents of

CNTs are calculated using the DFT-NEGF method and Landauer's formula in ATK as shown in Equations 4.3 and 4.4.

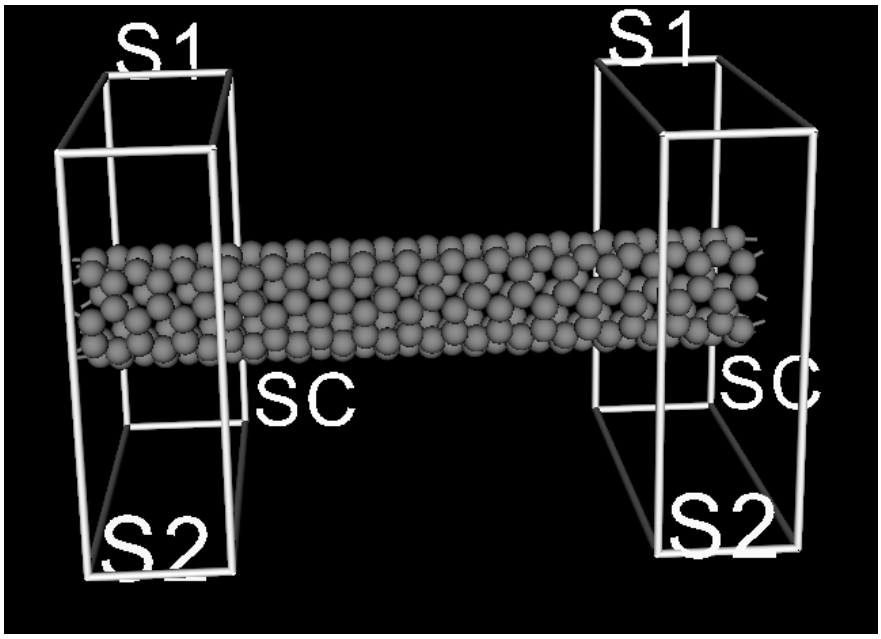

Figure 4.1. Simulated (4,4) CNT geometry

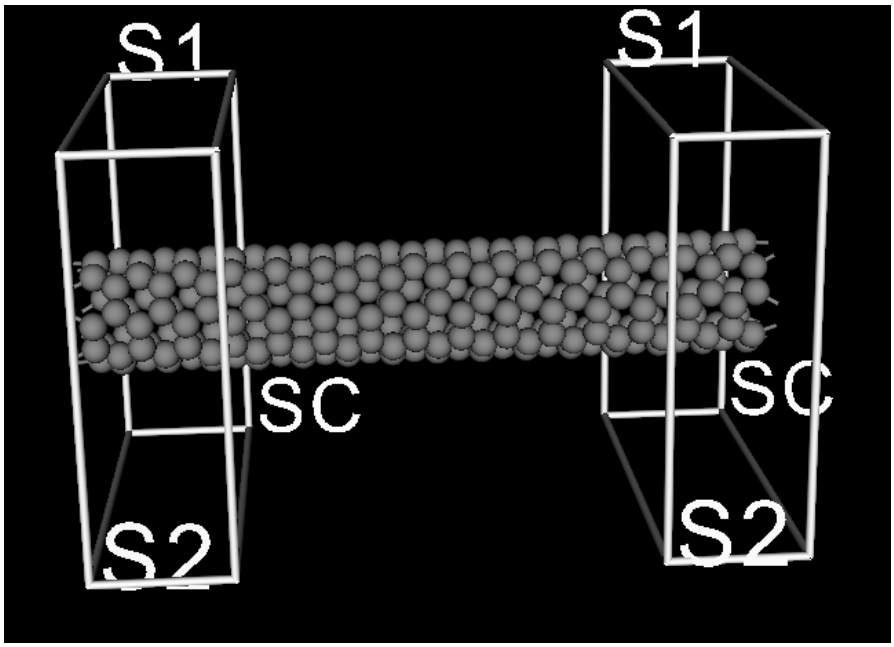

Figure 4.2. Simulated (5,5) CNT geometry

$$I = \frac{2q}{\mathbf{h}} \int_{-\infty}^{\infty} T(E)[f(E-m_L) - f(E-m_R)]dE \tag{4.3}$$

$$m_L - m_R = q.V_{bias} \tag{4.4}$$

where $T(E)$ is the transmission function of the CNT, $f_L(E)$ and $f_R(E)$ are the Fermi–Dirac distribution functions of left electrode and right electrode, respectively. The current calculation in ATK is performed using the electrochemical potentials, μ_L and μ_R of the left and right electrodes, respectively with the bias voltage, V_{bias} in Fermi-Dirac probability distribution functions. In the current calculations, the number of integration points of current calculation is taken as 1000 to ensure the accurate calculation of the current.

The current–voltage (I–V) values of the CNT interconnects are obtained for the voltage values in the range of (0V, 5V) with 0.1V steps. I–V characteristics of (4,4) and (5,5) CNTs are shown in Figures 4.3 and 4.4, respectively. Also, the variations of the total resistance with voltage are shown respectively in Figure 4.5 and Figure 4.6 for (4,4) CNT and (5,5) CNTs.

For low voltage values, the resistances have values of 6508kΩ and 6512kΩ for (4,4) and (5,5) CNT interconnects, respectively. These values are very close to the theoretical fundamental resistance associated with the CNTs which is given as in Equation 4.5 (Datta, 2005).

$$R_{fundamental} = \frac{h}{4q^2} = 6.4\ k\Omega \tag{4.5}$$

This fundamental resistance value is verified by various experiments in previous works (Yao et al., 2000), (Park et al., 2004). On the other hand, as it can be seen from Figures 4.3 and 4.4, the values of the CNT currents approach the order of 200μA. High values for the achieved currents are related to ballistic electron transport in short nanotubes as observed in previous experiments (Javey et al., 2004).

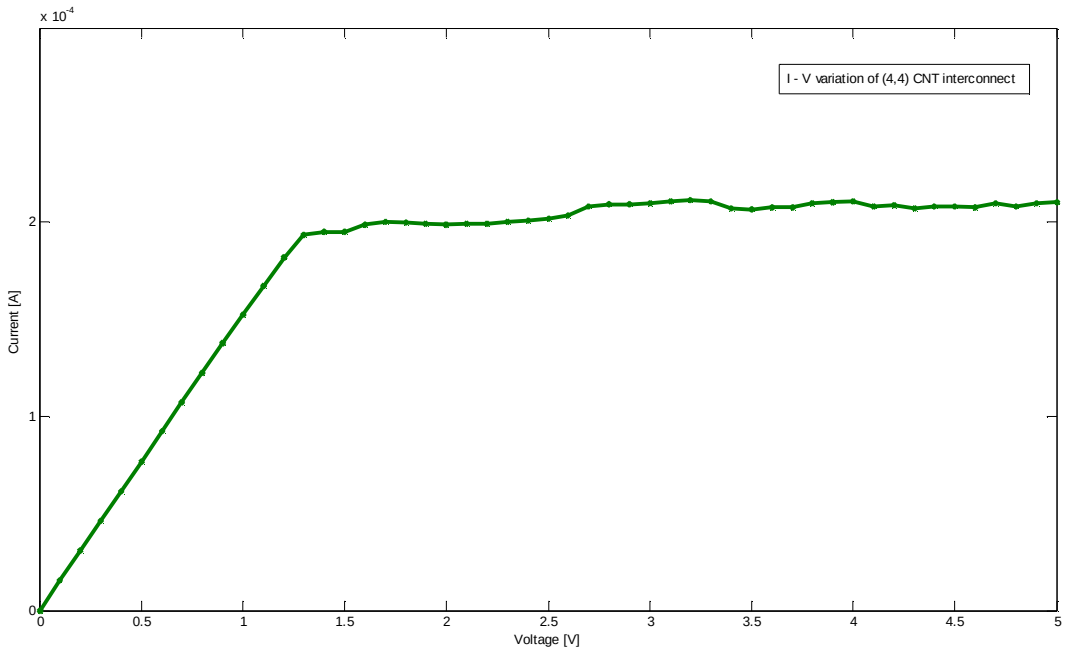

Figure 4.3. Current-voltage characteristics of (4,4) CNT

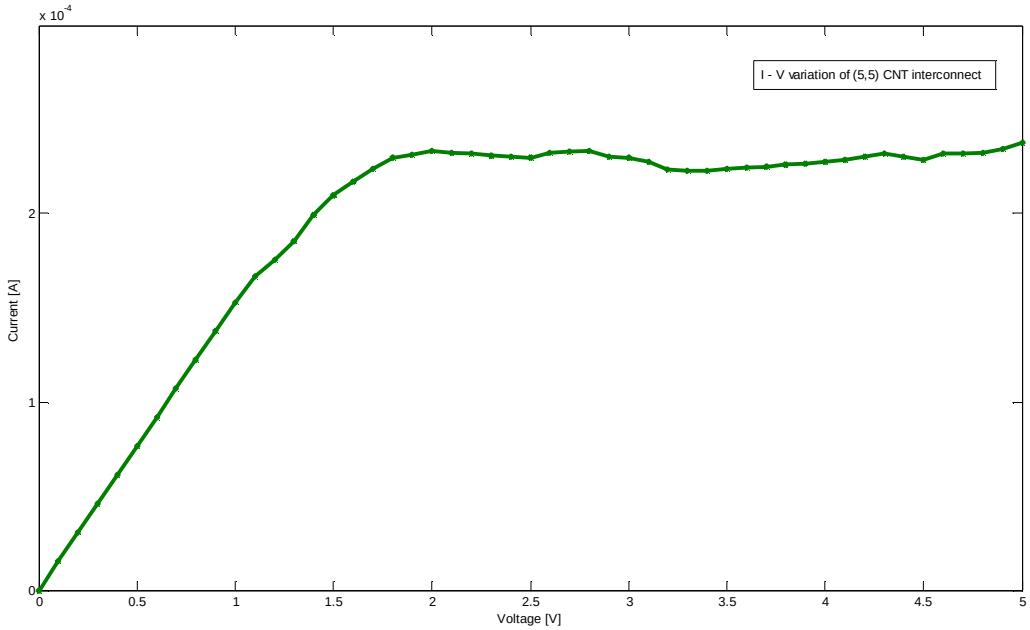

Figure 4.4. Current-voltage characteristics of (5,5) CNT

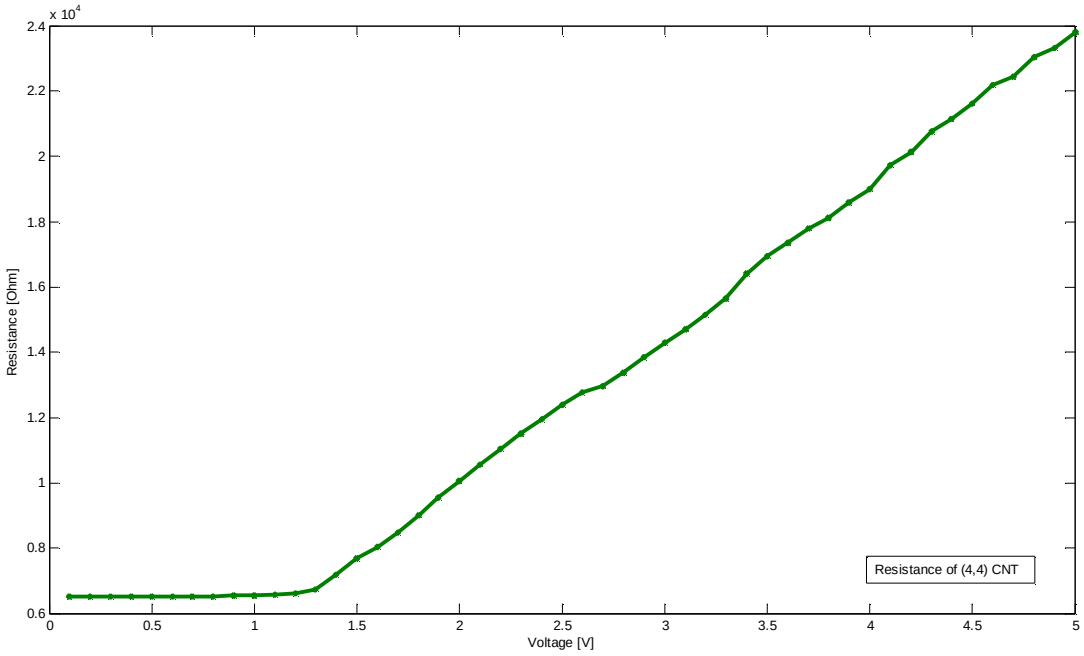

Figure 4.5. Resistance-voltage variation of (4,4) CNT

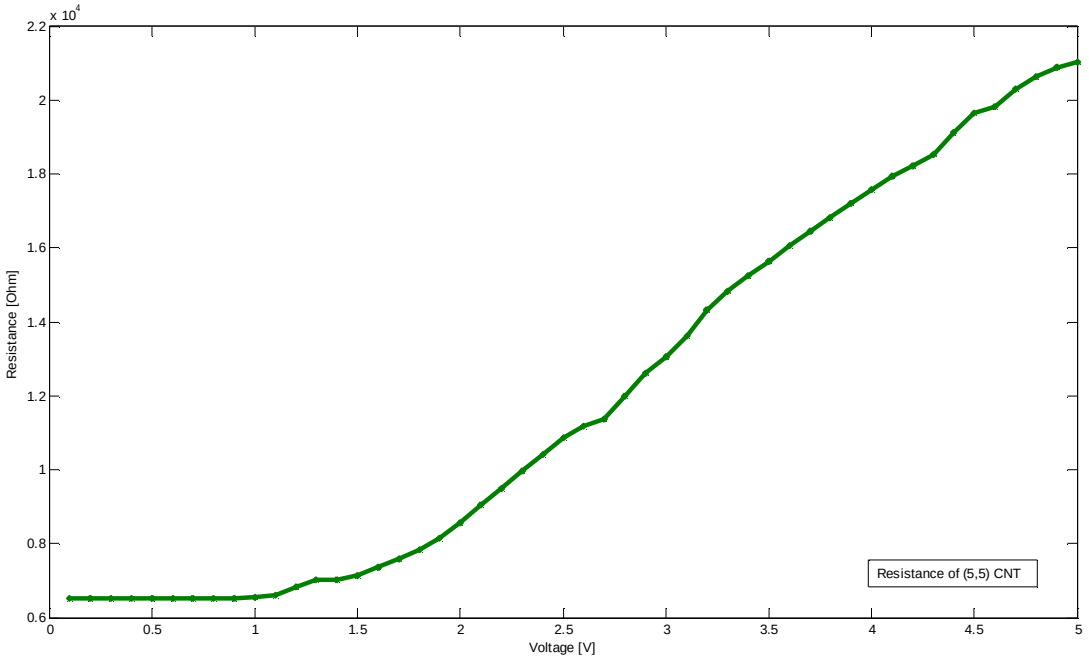

Figure 4.6. Resistance-voltage variation of (5,5) CNT

4.1.3. Interpretation of the Obtained Current-Voltage Characteristics

The obtained current-voltage characteristics of the carbon nanotube interconnects in this study are interpreted using the nanodevice model of (Datta, 2005). In general, the transmission spectrum of a nanodevice model as shown in Figure 4.7 can be given as in Equation 4.6.

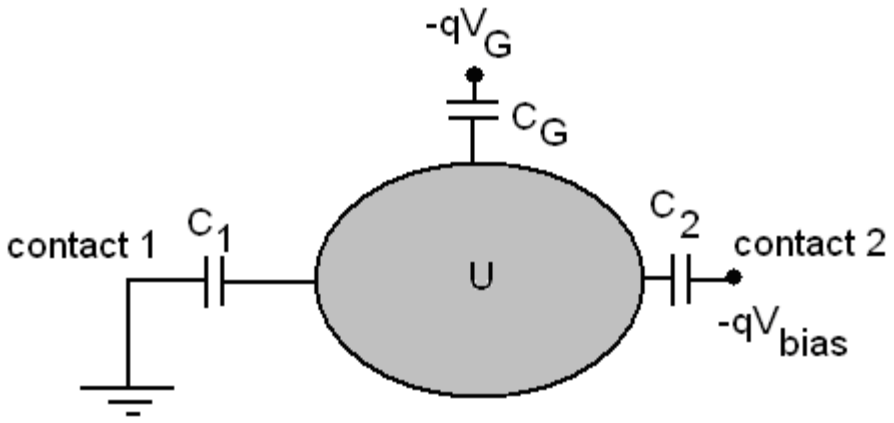

Figure 4.7. General nanodevice model

$$T(E) = D(E-U)\frac{2pg_1g_2}{g_1+g_2} \tag{4.6}$$

where *D(E-U)* is the density of states of the central region, γ_1 and γ_2 are the broadenings of contact$_1$ and contact$_2$, respectively. *U* is the potential of the central region dependent on: i) the bias voltage applied on the nanodevice, ii) the number of electrons in the central region, iii) the interaction of the electrons in the central region. The variation of the transmission spectra of the simulated carbon nanotubes by the bias voltages are due to the potential term *U* inside the density of states function, *D(E-U)*. The carbon nanotube interconnects of our study naturally do not employ a gate electrode hence C_G=0. Therefore, the potential of the central region, including the exchange-correlation potential, can be expressed as in Equation 4.7.

$$U = \underbrace{\frac{C_2}{C_T}(-qV_{bias}) + \frac{q^2}{C_T}(N - N_0)}_{part\ 1} + \underbrace{V_{xc}}_{part\ 2} \tag{4.7}$$

where $C_T=C_1+C_2$, N is the number of electrons in the channel in non-equilibrium state, N_0 is the number of electrons in the equilibrium state and q is the electron charge. Part 1 of Equation 4.7 represents the potential created by the electrode voltages and the travelling electrons while part 2 is the exchange-correlation term which represents the interaction between the central region electrons. Combining Equations 4.6 and 4.7 gives Equation 4.8.

$$T(E) = D\left(E + \frac{C_2}{C_1 + C_2} qV_{bias} - \frac{q^2}{C_1 + C_2} N + \frac{q^2}{C_1 + C_2} N_0 - V_{xc} \right) \frac{2pg_1g_2}{g_1 + g_2} \tag{4.8}$$

For the simulated geometries, the structure is symmetric therefore the coupling parameters are equal, $C_1=C_2$, then transmission spectrum function can be expressed as in Equation 4.9.

$$T(E) = D\left(E + \frac{qV_{bias}}{2} - \frac{q^2}{C_1 + C_2} N + \frac{q^2}{C_1 + C_2} N_0 - V_{xc} \right) \frac{2pg_1g_2}{g_1 + g_2} \tag{4.9}$$

The density of states function of quasi 1-D structures is given by Equation 4.10 (Hanson, 2008).

$$D(E) = \frac{\sqrt{2m_e}}{p\,\mathbf{h}} \sum_{n_x, n_y} \left(\frac{1}{\sqrt{E - E_{n_x, n_y}}} \right) H\left(E - E_{n_x, n_y} \right) \tag{4.10}$$

where m_e is the effective mass of electrons, $\mathbf{h}$ is the reduced Planck constant, $E_{nx,ny}$ are the energy eigenvalues of the 1-D structure and $H(x)$ is the Heaviside function.

Combining Equations 4.9 and 4.10 gives the transmission spectrum function as in Equation 4.11.

$$T(E)=\frac{2\sqrt{2m_e}g_1g_2}{\mathbf{h}(g_1+g_2)}\sum_{n_x,n_y}\left(\frac{1}{\sqrt{E+\frac{qV_{bias}}{2}-\frac{q^2}{C_1+C_2}N+\frac{q^2}{C_1+C_2}N_0-E_{n_x,n_y}-V_{xc}}}\right). \quad (4.11)$$
$$H\left(E+\frac{qV_{bias}}{2}-\frac{q^2}{C_1+C_2}N+\frac{q^2}{C_1+C_2}N_0-E_{n_x,n_y}-V_{xc}\right)$$

In Equation 4.11, the dependence of the transmission spectrum on the bias voltage, the number of electrons in the central region during the transport and the exchange-correlation potential is obtained analytically for the nanodevice model of Figure 4.7. As the bias voltage and the number of transported electrons increase, the transmission spectrum function is expected to shift to the right and the changes in the energy eigenvalues will occur. Hence, Equation 4.11 shows the reason behind the alteration of the transmission spectra of the carbon nanotubes with the applied voltages. The variation of the transmission spectrum of the general 1-D system of Figure 4.7 is plotted using Equation 4.11 as in Figure 4.8 for the applied voltages of V_{bias}=0V and V_{bias}=4V. Energy eigenvalues are $E_{nx,ny}$ = {0eV, 2eV,3eV} for V_{bias}=0V and $E_{nx,ny}$ = {0eV, 3eV,4.5eV} for V_{bias}=4V. Figure 4.8 shows the change of the shape of the transmission spectrum as the bias voltage increases. For this example, the contact broadenings are taken as γ_1= γ_2=0.05eV, $\mathbf{h}=1.054x10^{-34}$ J.s and m_e=1.2x10^{-31}kg. As it is seen from Figure 4.8, variation of the bias voltage and the corresponding change in energy eigenvalues affect the transmission spectrum significantly and as the bias voltage becomes greater, the eigenvalues shift to the right and the area under the transmission spectrum becomes smaller which means the current does not show a monotonous increasing regime but a saturation regime.

On the other hand, the bias voltage dependence of the transmission spectra of the (4,4) and (5,5) carbon nanotubes under consideration can not be obtained and plotted using Equations 4.11 since energy eigenvalues used in this calculation has to be found self-consistently for 240 atoms. However, the transmission spectra are

obtained using ATK as shown in Figures 4.9 and 4.10 for (4,4) and (5,5) CNTs, respectively.

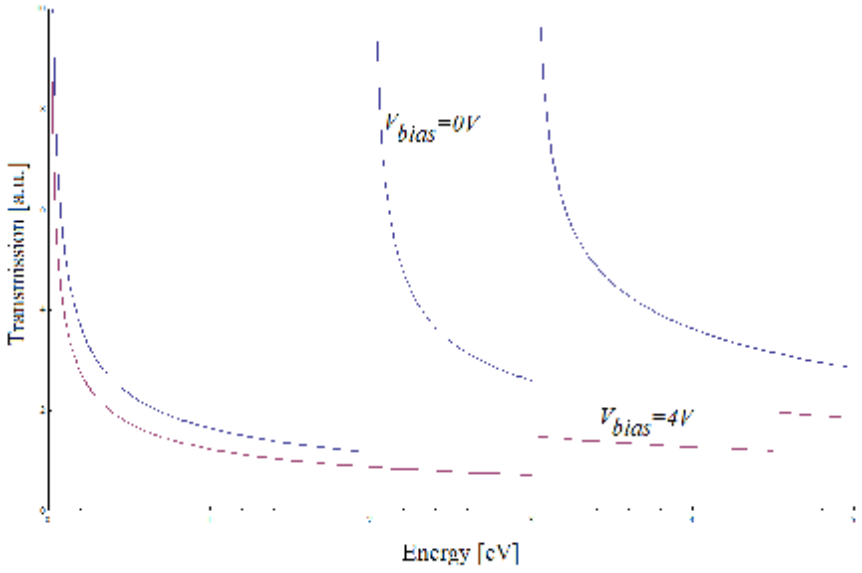

Figure 4.8. The variation of the transmission spectrum of an idealized 1-D system by the variation of the applied voltages and the energy eigenvalues

It can be seen from Figures 4.9 and 4.10 that, as the bias voltages increase, the transmission spectra are altered which causes the currents to be saturated even if the electron transport is ballistic for short nanotubes. As a result of this, the resistances of the CNTs appear to increase due to the lack of the increment in the current. Note that, the obtained transmission spectra of the (4,4) and (5,5) CNTs in Figures 4.9 and 4.10 are slightly different than the transmission spectra of the idealized 1-D system given in Figure 4.8 because in realistic structures, realistic electron interactions are taken into account.

In addition, as the applied voltages increase, the currents of the CNTs do not show the saturation regime exactly, however the currents slightly decrease and follow saturation regimes with small fluctuations. This situation is also related to the alteration of the transmission spectra of the CNTs by the electric fields created by applied bias voltages.

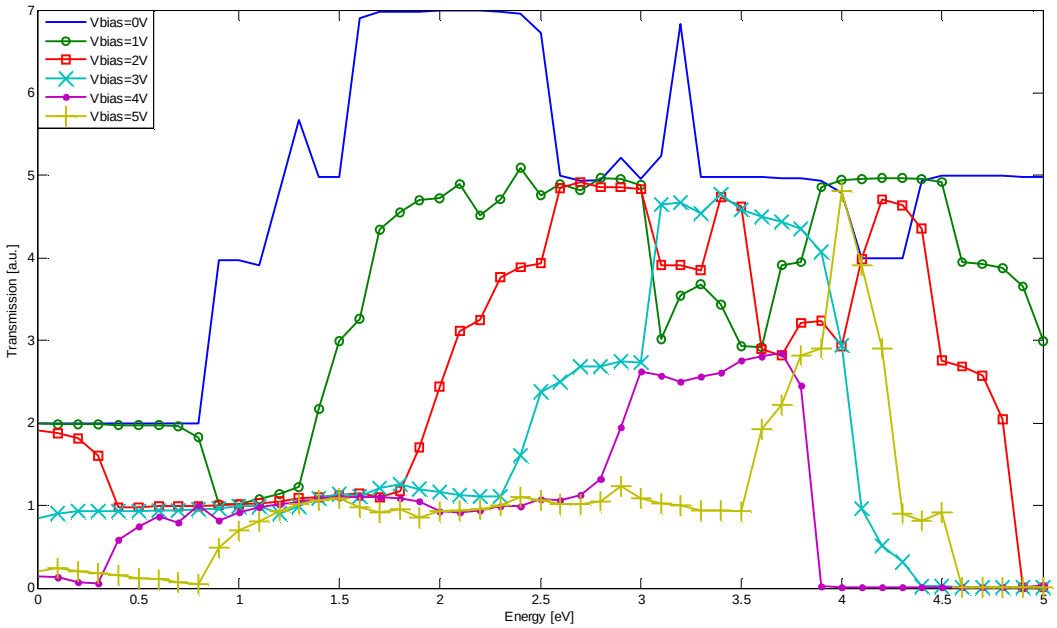

Figure 4.9. Transmission spectrum of (4,4) CNT

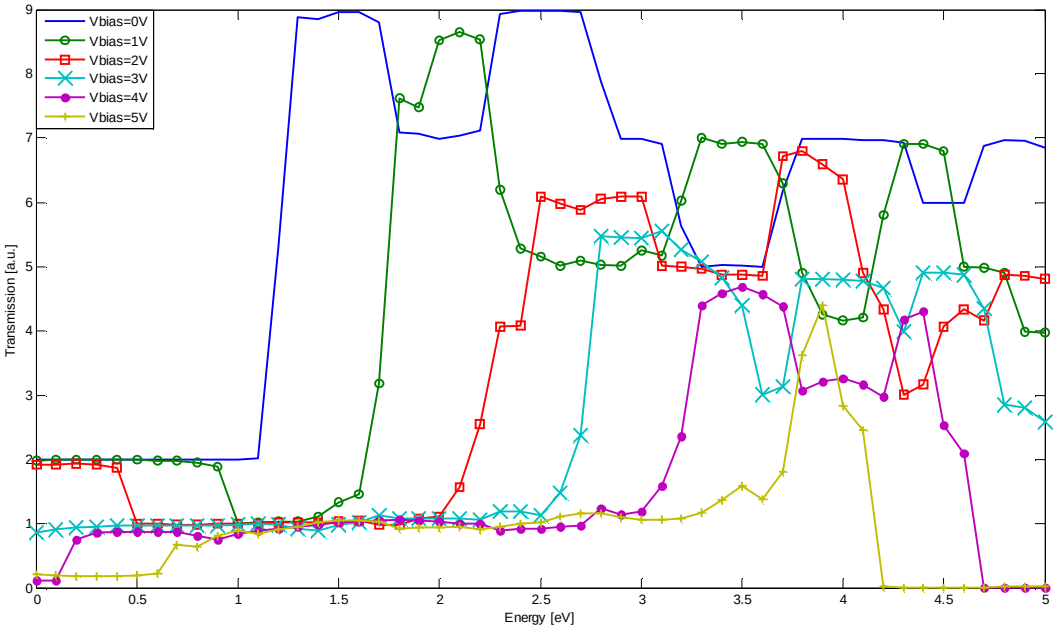

Figure 4.10. Transmission spectrum of (5,5) CNT

4.1.4. Polynomial Model for the Voltage Dependent Resistance of CNTs

The resistances of the CNTs increase by the applied bias voltage due to the saturation of the currents. This behavior is clearly seen in Figure 4.5 and Figure 4.6. The obtained resistance–voltage (R–V) characteristics of CNT interconnects are modeled with sixth order polynomial functions of the form shown in Equation 4.12 (Yamacli and Avci, 2009).

$$R_T(V) = a_6V^6 + a_5V^5 + a_4V^4 + a_3V^3 + a_2V^2 + a_1V + a_0 \tag{4.12}$$

The coefficients of Equation 4.12 for (4,4) and (5,5) CNTs are obtained respectively as in Equations 4.13 and 4.14 in MATLAB environment.

$$[a_6, a_5, a_4, a_3, a_2, a_1, a_0] = [-32.56, 499.2, -2861, 7309, -6775, 1984, 6400] \tag{4.13}$$

$$[a_6, a_5, a_4, a_3, a_2, a_1, a_0] = [-3.319, 89.37, -808.7, 3023, -3732, 1677, 6316] \tag{4.14}$$

The R–V characteristics of CNTs obtained from ab initio simulations and calculated with the developed polynomial R–V model are plotted on the same axes for (4,4) and (5,5) CNTs in Figure 4.11 and Figure 4.12, respectively. The developed model accurately represents the R–V characteristics of CNT interconnects as it is seen from these figures.

The current-voltage characteristics of CNTs and current saturation mechanism in short CNTs are obtained for the first time in the literature (Yamacli and Avci, 2009) in this thesis. Moreover, a polynomial model for the nonlinear resistance-voltage characteristics of CNTs is given and verified. The presented polynomial model for the resistance-voltage variation can easily be used for other types of CNTs and integrated into electronic design automation (EDA) tools as ready to use for the IC engineer. Modelling of the nonlinear resistance-voltage characteristics is especially important from the IC design viewpoint since the nonlinearity of the interconnects introduce distortion to the circuit.

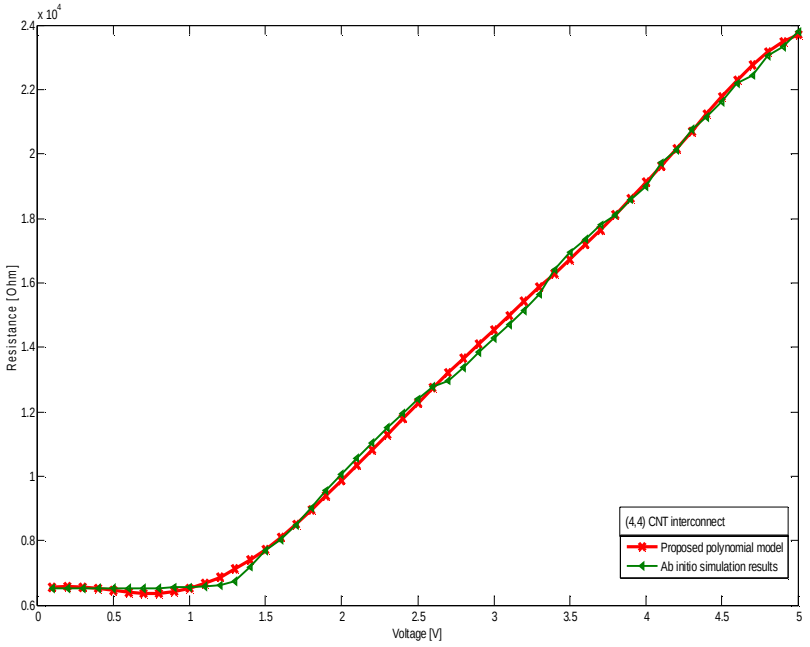

Figure 4.11. R–V characteristics of (4,4) CNT from ab initio simulations and the developed polynomial model

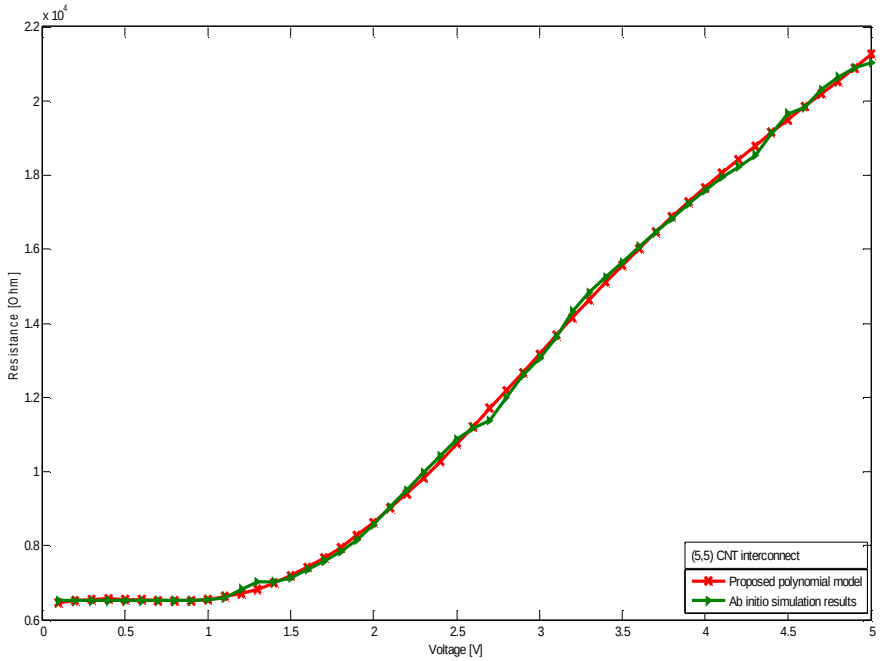

Figure 4.12. R–V characteristics of (5,5) CNT from ab initio simulations and the developed polynomial model

4.2. Neural Network Modelling of CNT Interconnect Resistance

In this subsection, a resistance model for metallic CNT interconnects is developed using neural networks. The proposed model is trained and tested with two types of metallic CNTs. The model can easily be generalized for other types of CNTs and is suitable for integration into EDA tools. First principles electronic transport simulations explained in the previous subsection are taken as bases to obtain electrical characteristics of CNTs.

4.2.1. Multilayer Perceptron Neural Networks as Modeling Tools

Multilayer perceptron (MLP) is the most common neural network (NN) model consisting of successive linear transformations followed by processing with non-linear activation functions. MLP represents a generalization of the single layer perceptron which is only capable of constructing linear decision boundaries and simple logic functions (Yamacli and Avci, 2010b).

In the general form of an MLP network, the x inputs are fed into the first layer of hidden units. The input units are simply `fan-out' units: no processing takes place in these units. The activation of a hidden unit (neuron j) is a function f of the weighted inputs plus a bias, as given in Equation 4.15 where w_{ji} is the weight of input i to neuron j where x_{pi} is input i. The outputs of the hidden units are distributed over the next layer until the last one where the outputs are fed into a layer of output units.

$$x_{pj} = f_i\left(\sum_i w_{ji}x_{pi} + l_i\right) = f_i(y_{pj}) \tag{4.15}$$

The multi layer perceptron neural network (NN) model used in this study is chosen to have 2 hidden layers and 1 output layer as shown in Figure 4.13.

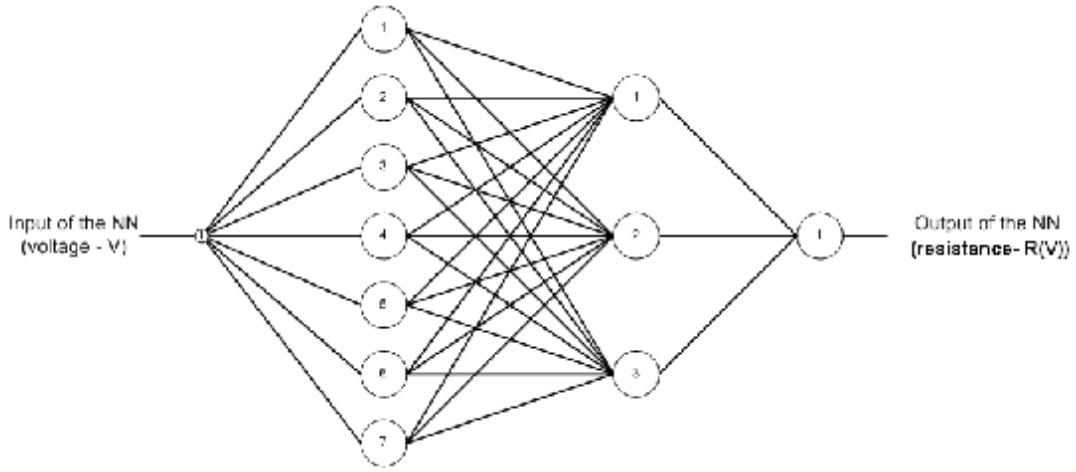

Figure 4.13. Multi layer perceptron NN model used for modeling of the nonlinear R-V relationship of the metallic CNTs

The defining equations of the utilized NN model are given in Equations 4.16, 4.17 and 4.19.

$$R(i) = \Theta_3\left(w_{32}u_2 + l_3\right) \tag{4.16}$$

$$u_2 = \Theta_2\left(w_{21}u_1 + l_2\right) \tag{4.17}$$

$$u_1 = \Theta_1\left(w_{11}V(i) + l_1\right) \tag{4.18}$$

where Θ_i is the activation function of layer *i*.

4.2.2. Neural Network Modelling Results

The activation functions of the first and second hidden layers and the output layer (Θ_1, Θ_2 and Θ_3) are chosen as tangential sigmoid, pure linear and pure linear functions, respectively. The NN training is performed in MATLAB.

Ab initio CNT R-V characteristics and the characteristics of the developed NN model are plotted on the same axes for (4,4) and (5,5) CNTs as shown in Figure 4.14 and Figure 4.15, respectively (Yamacli and Avci, 2010b). The developed NN model accurately fits the R-V characteristics of CNT interconnects as it is seen in these figures.

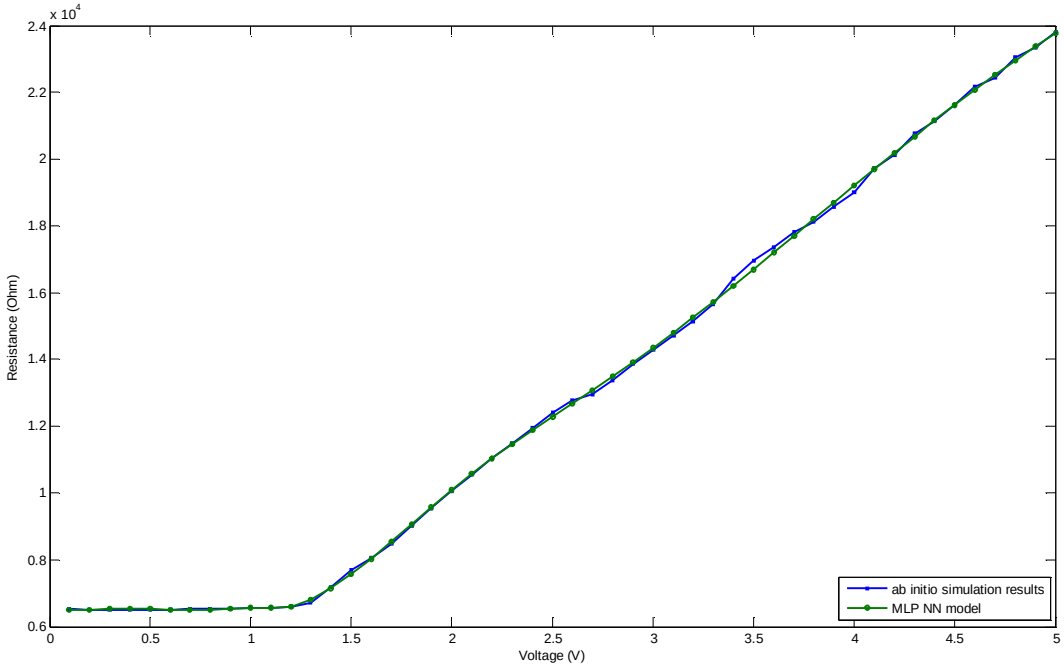

Figure 4.14. R-V characteristics of (4,4) CNT from ab initio simulations and the developed NN model

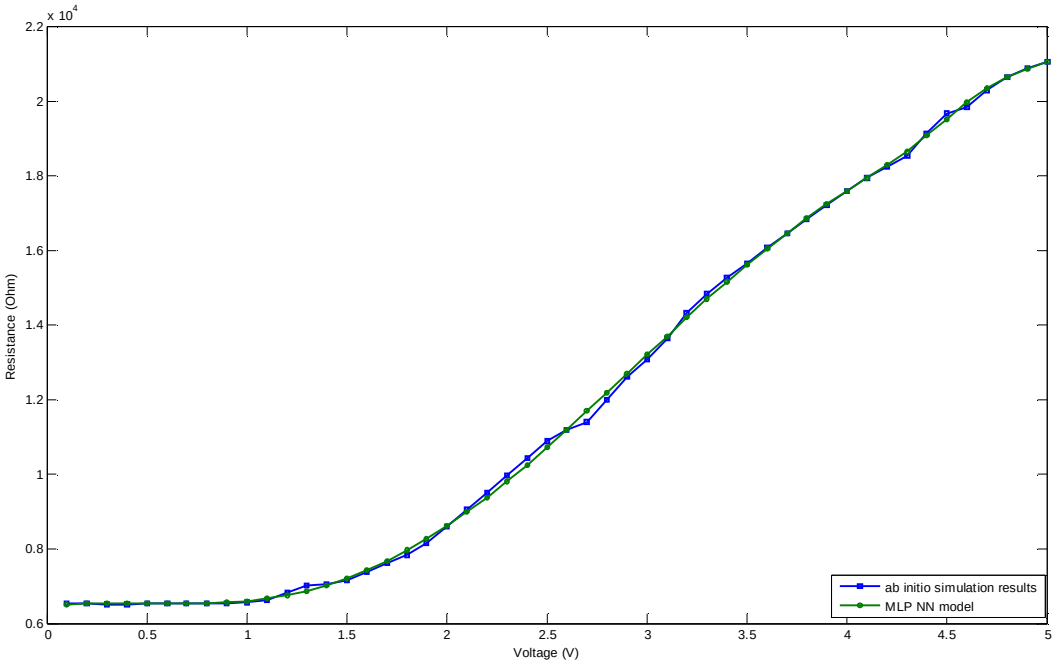

Figure 4.15. R-V characteristics of (5,5) CNT from ab initio simulations and the developed NN model

4.3. Utilization of Nonlinear Current-Voltage Characteristics of Metallic CNTs to Design Compact Nanoscale Circuits

It is experimentally shown that, metallic CNTs show current saturation characteristics as the applied voltage increases due to two reasons as given as follows.

a. For long metallic CNTs (having 50nm and longer length), current saturation occurs due to the lack of additional transmission channels above a threshold energy and growing electron-phonon scattering as the applied voltage increases (Hanson, 2008).
b. For short metallic CNTs, density of states functions of CNTs are altered by higher applied voltages hence causing current saturation (Yamacli and Avci, 2009).

As a result, the voltage-current characteristics of metallic carbon nanotubes show saturation trend with the permission of high current densities as high as 10^{10}A/cm^2 in nanoscale dimensions which cannot be achieved by conventional materials (Wei et al., 2001). Current saturation characteristics of metallic carbon nanotubes are analyzed in detail in the following subsection.

4.3.1. Current Saturation Characteristics of Metallic CNTs

For metallic CNTs having approximately 50nm and longer length, in which the transport is not ballistic, the I-V relationship is given Equation 4.19 (Hanson, 2008).

$$I_{mCNT} = \frac{V_{mCNT}}{\frac{h}{4q^2}\left(1+\frac{L}{L_{mfp\_low}}\right)+\frac{h}{4q}\frac{L\left|\vec{E}\right|}{E_{ph}}} \tag{4.19}$$

In Equation 4.19, V_{mCNT} and I_{mCNT} are voltage and current of the metallic CNT, respectively, h is Planck's constant, L is the length of metallic CNT, L_{mfp_low} is the mean free path of the electrons at low applied voltages, q is the electronic charge, $\vec{E}$ is the electric field inside the nanotube and E_{ph} is the phonon energy. Electric field and saturation current can be written as in Equations 4.20 and 4.21, respectively.

$$\left|\vec{E}\right| = \frac{V_{mCNT}}{L} \tag{4.20}$$

$$I_{sat} = \frac{4qE_{ph}}{h} \tag{4.21}$$

The current-voltage characteristics of a metallic CNT having the length 300nm is plotted in Figure 4.16 using the parameters of h=6.62x10^{-34}Js, q=1.609x10^{-19}C, E_{ph}=0.19eV and $L_{mfp\_low\_Vt}$ =1600nm. The saturation characteristics of metallic CNTs are verified by experiments (Yao et al., 2000), (Park et al., 2004). For metallic CNTs having 50nm or shorter length, using the results of the subsection 4.1, the I-V relationship is wirtten as in Equation 4.22.

$$I_{mCNT} = \frac{V_{mCNT}}{a_6 V_{mCNT}^{6} + a_5 V_{mCNT}^{5} + a_4 V_{mCNT}^{4} + a_3 V_{mCNT}^{3} + a_2 V_{mCNT}^{2} + a_1 V_{mCNT} + a_0} \tag{4.22}$$

where I_{mCNT} and V_{mCNT} are current and voltage of the metallic CNT, respectively and (a6,..,a0) are resistance coefficients dependent on the CNT (Yamacli and Avci, 2009). The I-V characteristics of a (5,5) metallic CNT having 10nm length is given in Figure 4.17 using the resistance coefficients of Equation 4.14. The following points can be determined from the characteristics of both short and long metallic CNTs.

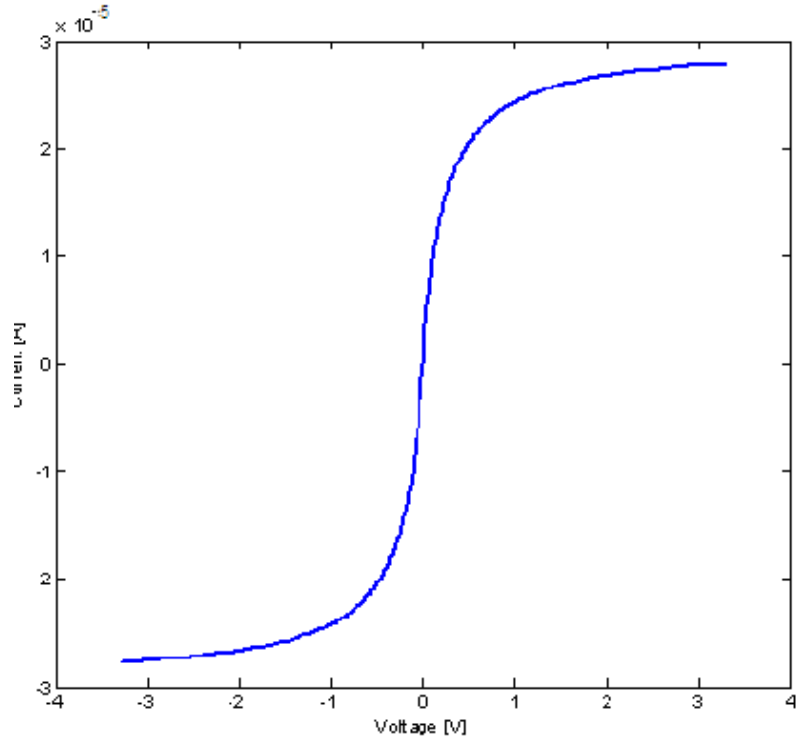

Figure 4.16. I-V characteristics of a 300nm metallic CNT

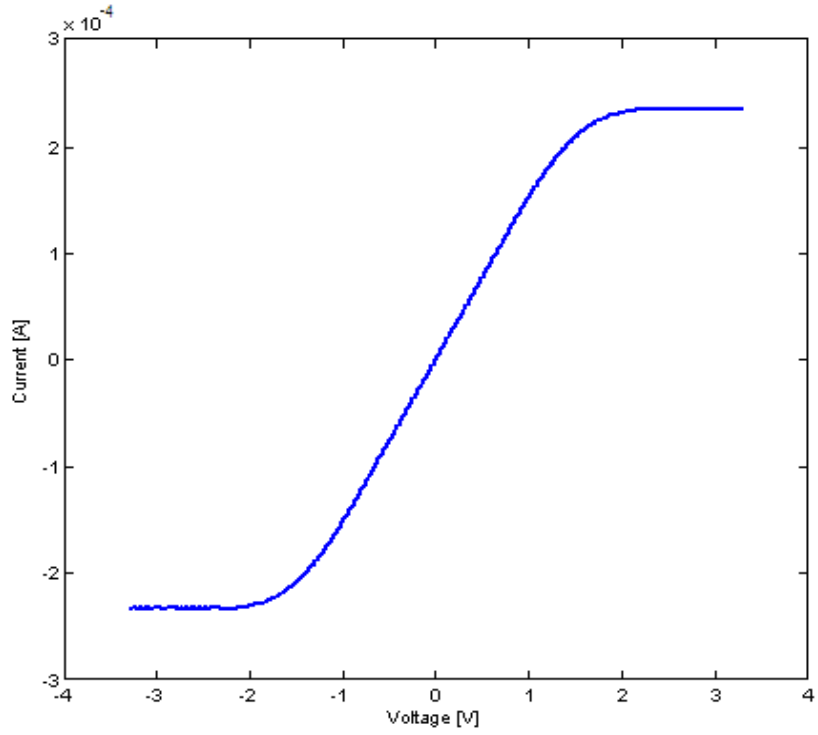

Figure 4.17. I-V characteristics of a 10nm metallic CNT

a. For relatively lower voltages, the current of the metallic CNT increases as the applied voltage increases, which can be named as 'resistive' region since CNT behaves as a resistance in this region. Metallic CNTs are used in this region when they are operated as interconnects.

b. As the applied voltage increases, the current of a metallic CNT approaches a saturation level and further increments in the applied voltage does not change the current passing through the CNT, which can be named as 'saturation' region. Saturation region is an unwanted region for interconnect applications (Javey et al., 2004) however utilization of saturation characteristics to design various circuits is the aim of this subsection.

Taking these facts into consideration, a piecewise linear function for the idealized I-V characteristics of a metallic CNT can be written as in Equation 4.23.

$$I_{mCNT} = \begin{cases} G_{mCNT} V_{mCNT}, & |V_{mCNT}| \le V_{th} \\ I_{sat}, & V_{mCNT} > V_{th} \\ -I_{sat}, & V_{mCNT} < -V_{th} \end{cases} \tag{4.23}$$

where I_{mCNT}, V_{mCNT} are current and voltage of the metallic CNT, respectively, G_{mCNT} is the conductance of the CNT in the resistive region and I_{sat} is the current of the CNT in the saturation region. V_{th} is the threshold voltage, which separates the resistive and saturation regions. I_{sat} and V_{th} can be determined from I-V characteristics obtained by either experiments (Javey et al., 2004) or by the given I-V equations (Yamacli and Avci, 2009). The plot of the idealized I-V characteristics of metallic CNTs with the key parameters and operating regions is shown in Figure 4.18.

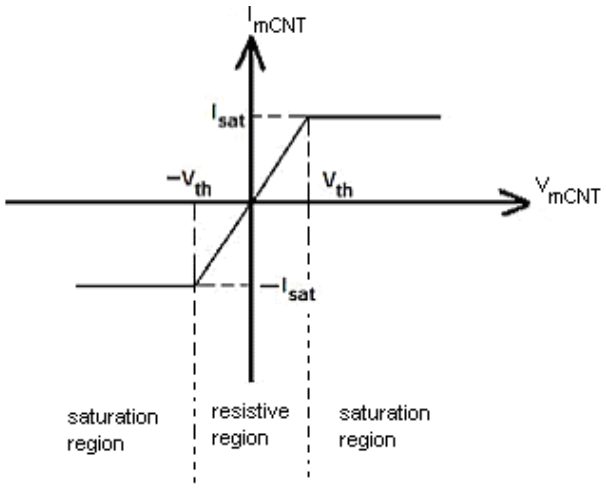

Figure 4.18. Idealized I-V characteristics of a metallic CNT

4.3.2. Comparison of the Current saturation Characteristics of Metallic Carbon Nanotubes and Silicon Devices

Silicon devices and even silicon wires also display current saturation characteristics, however, utilization of metallic CNTs as current saturation elements have the some advantages over conventional devices as listed in the following.

a. CNTs have smaller size, having diameter of a few nanometres and length of tens of nanometres making them suitable for nano-sized electronics technology. Metallic CNTs can be utilized easier than silicon devices in all-CNT nanocircuits where all components are made of CNTs (Sharifi and Ghasemi, 2010), (Lin et al., 2010).
b. Metallic CNTs permit current densities up to 10^{10}A/cm^2, which enables them to be used with high density saturated current continuously. However, silicon wires enable the current densities up to only 10^5A/cm^2 (Wurz et al., 2008). Continuous operation of high current density in silicon technology is problematic due to Joule heating and electromigration (Chen et al., 2010).
c. Metallic CNTs provide simplicity from the production point of view. For example, in order to obtain a current source using transistors, various steps have to be taken to produce the transistor on the integrated circuit, and then

the connections to achieve the saturated current are required. However, metallic CNT itself provides the saturation characteristics without any need for a specific connection or several production steps on the wafer.

d. The drift velocity saturation hence the current saturation in conventional bulk materials such as silicon, which is shown in Figure 4.19 is caused from the imperfectness of the bulk crystal periodicity (Hanson, 2008). This imperfectness results in electron-phonon scattering hence decrement in mobility and increment in self-heating of the structure limiting the permitted current density. However, in metallic carbon nanotubes, the crystal structure made of carbon atoms exhibits a nearly perfect periodicity (Srivastava et al., 2005), (Naeemi et al., 2004) and high thermal conductivity making them suitable for current saturation. The reason for current saturation in metallic CNTs is primarily due to the lack of transmission channels above the threshold voltage. In Figure 4.20, typical transmission spectrum of a metallic CNT is shown. Since the transmission function has no conducting channels for the energies above E_{max}, electrons having energies above E_{max}, cannot be injected into the structure hence causing the saturation of the current (Durkan, 2007). This mechanism in metallic CNTs provide current saturation with high current densities.

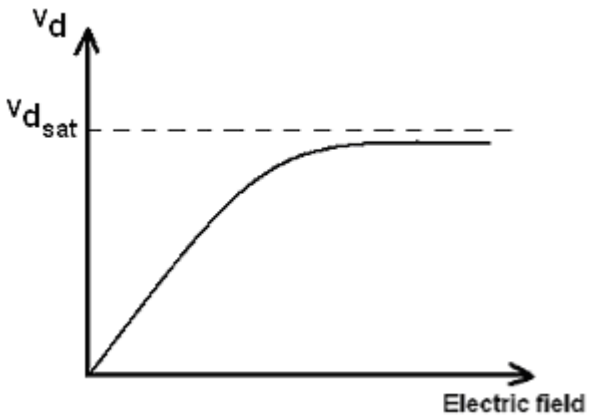

Figure 4.19. Drift velocity-electric field variation in bulk material

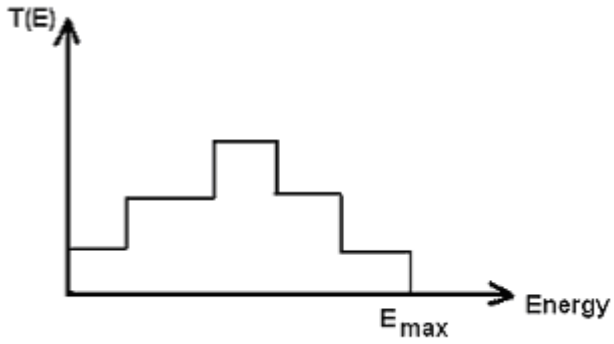

Figure 4.20. Typical transmission spectrum of a metallic CNT

4.3.3. Circuit Possibilities Using Metallic CNTs

Considering the advantages of metallic CNTs over bulk materials, current regulator, voltage regulator and sigmoidal function circuits are designed to show the versatility of utilizing the saturated *I-V* characteristics of metallic CNTs.

a. Current regulator circuit: Current regulator circuits utilizing metallic CNTs are shown in Figure 4.21 and Figure 4.22. For the circuit in Figure 4.21, the output current of current regulator circuit is CNT's saturation current and this current drives the load resistance R_L. In Figure 4.22, the current regulator circuit employing multiple CNTs is shown which can be used to obtain higher output currents.

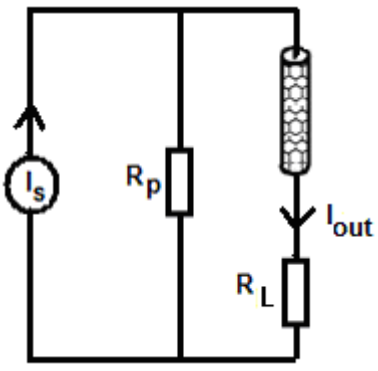

Figure 4.21. The current regulator circuit utilizing a metallic CNT

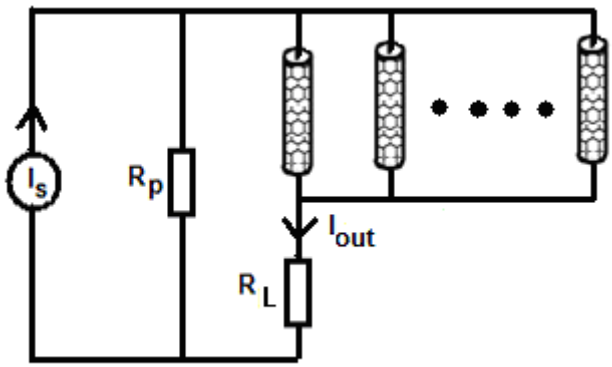

Figure 4.22. The current regulator circuit utilizing multiple metallic CNTs

Circuits in Figure 4.21 and Figure 4.22 operate as current regulator circuits with output currents I_{sat} and nI_{sat}, respectively, where n is the number of CNTs for multiple metallic CNT circuit. Metallic CNTs obviously have to be in saturation region in order to obtain current regulation characteristics, so the saturation condition given in Equation 4.24 has to be satisfied.

$$V_{mCNT} = I_{RP}.R_P - I_{mCNT}.R_L \geq V_{th} \tag{4.24}$$

$$V_{mCNT} = (I_S - I_{mCNT}).R_P - I_{mCNT}.R_L \geq V_{th} \tag{4.25}$$

where V_{th} is the threshold voltage of metallic CNT. Considering that $I_{CNT}=I_{sat}$ in the saturation region, the condition for the value of R_P can be written as in Equation 4.26.

$$R_P \geq \frac{V_{th} + I_{sat}R_L}{I_S - I_{sat}} \tag{4.26}$$

For the current regulator circuit employing n metallic CNTs, Equation 4.26 becomes Equation 4.27 using the same procedure.

$$R_P \geq \frac{V_{th} + nI_{sat}R_L}{I_S - nI_{sat}} \tag{4.27}$$

In order to verify the proper operation of the circuit of Figure 4.21, the *I-V* relationship is imported in Verilog-A language into HSPICE environment and then the current regulation circuit is simulated. Considering that I_{sat}=29.5µA and V_{th}=3V and taking the load resistance as R_L=100Ω, R_p is selected as 20k using Equation 4.26 to obtain current regulation for input currents of $I_S \geq$ 180µA.

The input-output current characteristics of the current regulator circuit of Figure 4.21 is obtained and plotted in Figure 4.23 using HSPICE. The output current has the fixed value of CNTs saturation current 29.5µA as seen from Figure 4.23. Transient simulation of the current regulator circuit is also performed and the waveforms of input and output currents are shown in Figure 4.24. The output current is regulated by the metallic CNT and has the fixed value as it is seen from Figure 4.24. There is a 20nA peak to peak ripple for 29.5µA regulated output.

b. Voltage regulator circuit: Second proposed application of metallic CNT characteristics is the voltage regulator circuits shown in Figure 4.25 and Figure 4.26. Output voltages of the circuits in Figure 4.25 and Figure 4.26 can be written as in Equation 4.28 and Equation 4.29, respectively where *n* is the number of CNTs in Figure 4.26 and I_{sat} is the saturation current of metallic CNTs.

$$V_o = I_{sat}(R_L // R_P) \tag{4.28}$$

$$V_o = nI_{sat}(R_L // R_P) \tag{4.29}$$

Metallic CNTs have to operate in saturation region in order to obtain voltage regulator characteristics, which can be written as in Equation 4.30 where V_{th} is the threshold voltage of CNTs. Considering $I_{CNT}=I_{sat}$ in the saturation region, Equation 4.31 can be obtained.

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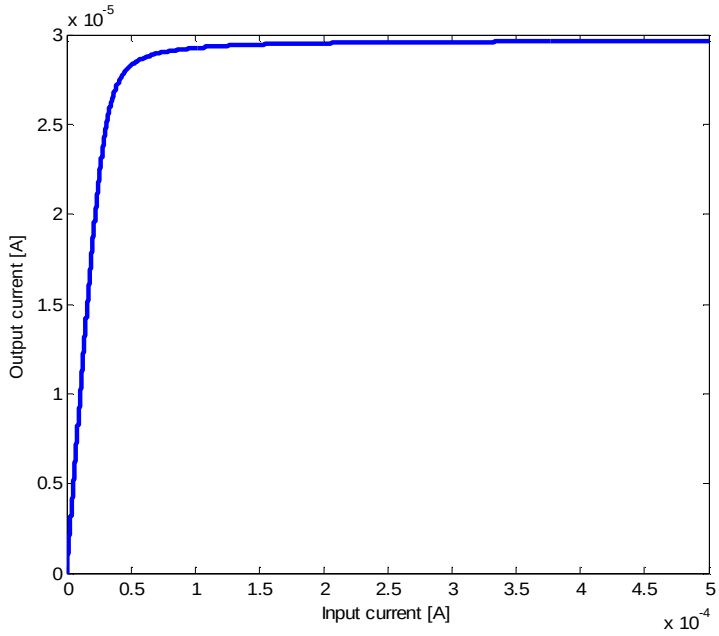

Figure 4.23. Simulated input-output characteristics of the current regulator employing metallic CNT as nonlinear element

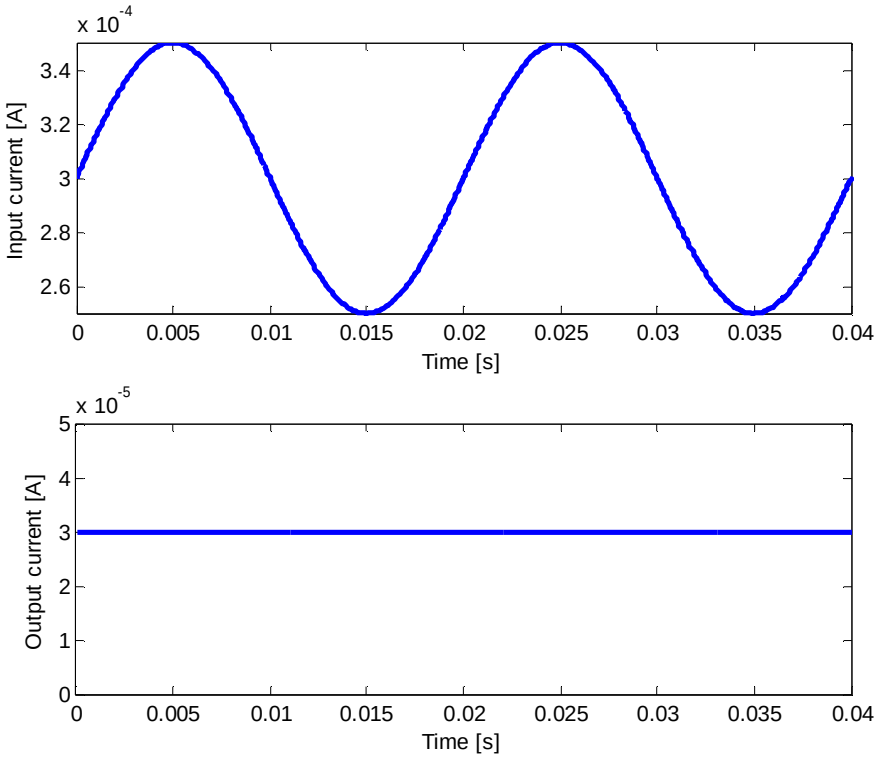

Figure 4.24. Input and output currents of the current regulator circuit in Figure 4.21

$$V_{CNT} = V_S - I_{CNT}\left(\frac{R_S R_L}{R_S + R_L}\right) \geq V_{th} \tag{4.30}$$

$$R_S \leq \frac{R_L(V_S - V_{th})}{I_{sat}R_L + V_{th} - V_s} \tag{4.31}$$

Similarly, the operating condition for the voltage regulator circuit employing *n* CNTs is written as in Equation 4.32.

$$R_S \leq \frac{R_L(V_S - V_{th})}{nI_{sat}R_L + V_{th} - V_s} \tag{4.32}$$

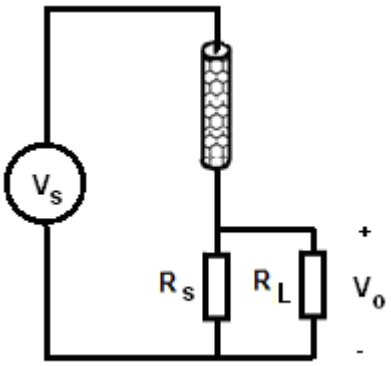

Figure 4.25. Voltage regulator circuit utilizing single metallic CNT

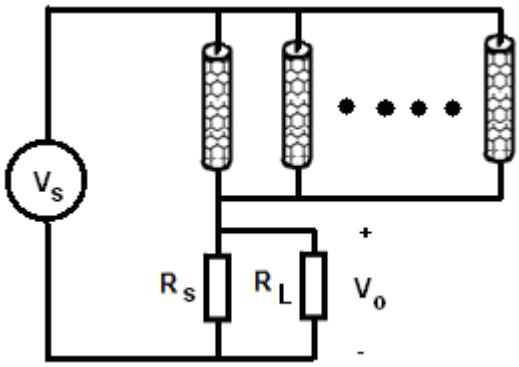

Figure 4.26. Voltage regulator circuit utilizing multiple metallic CNT

The operation of voltage regulator circuit is also verified by HSPICE simulations. The input-output voltage plot is given in Figure 4.27. Taking R_L=1M, I_{sat}=29.5µA and V_{th}=3V, the series resistor value is selected as R_s=20k using Equation 4.31. As can be seen from Figure 4.27, the output voltage of the circuit has the regulated value of 588mV which can also be verified using Equation 4.28 where I_{sat}=29.5µA. The transient response of the circuit is also tested by simulations and given in Figure 4.28. The ripple voltage is obtained as 1.1mV peak to peak for 588mV regulated output voltage. It can be seen from simulation results that output voltage of voltage regulator circuit using metallic CNT can be utilized to bias CNT field effect transistors (CNTFETs) since the output voltage is an appropriate voltage for CNTFET biasing (Amlani et al., 2006). Hence, utilization of metallic CNTs as nonlinear components is also a versatile solution for CNTFET biasing in all-CNT circuits.

c. Sigmoidal activation function characteristics for neural network circuits: Considering the symmetrical nonlinear I-V characteristics of metallic CNTs, it can be seen that metallic CNTs can be used to generate sigmoidal function characteristics which is extensively used in artificial neural network circuits (Haykin, 2008). Considering the simulated bipolar input-output characteristics of the circuit of Figure 4.25 which is shown in Figure 4.29, it is clearly seen that nonlinear I-V characteristics of metallic CNTs enable to build sigmoidal activation functions.

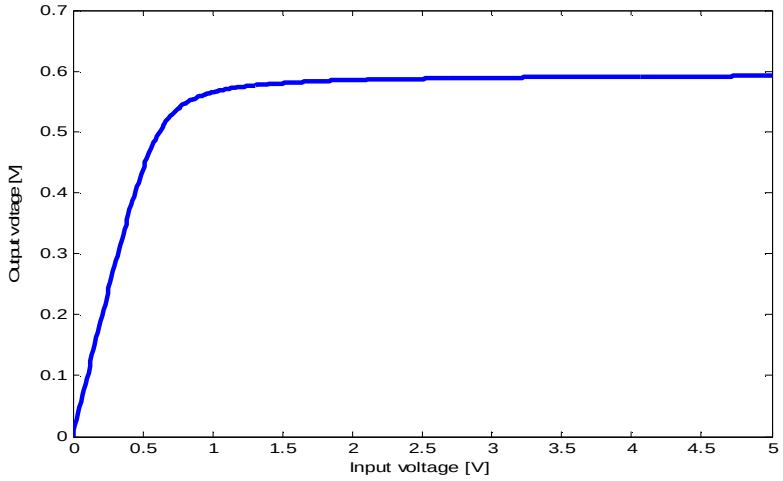

Figure 4.27. Input-output characteristics of the voltage regulator circuit utilizing metallic CNT

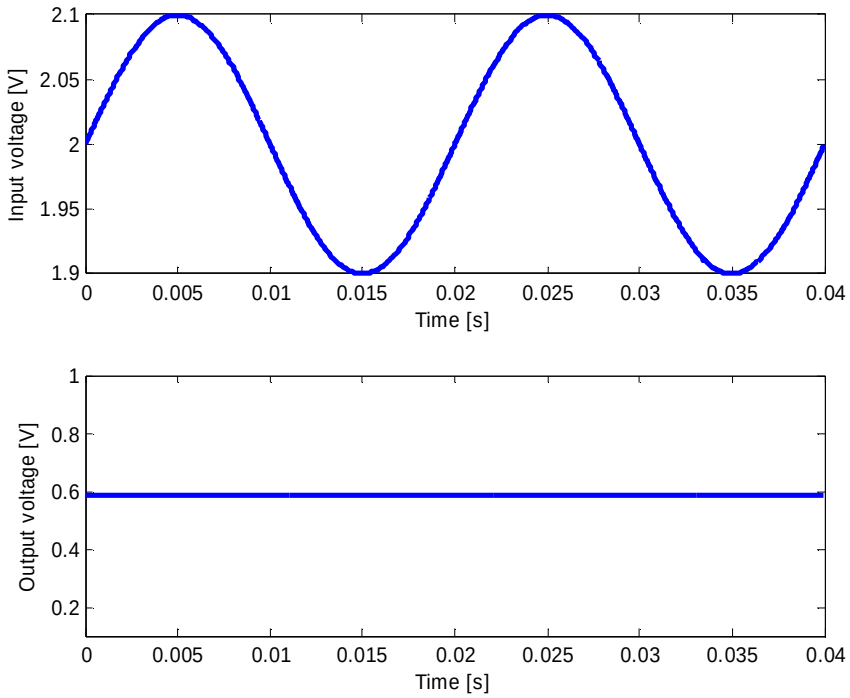

Figure 4.28. Transient simulation results of the voltage regulator circuit utilizing metallic CNT

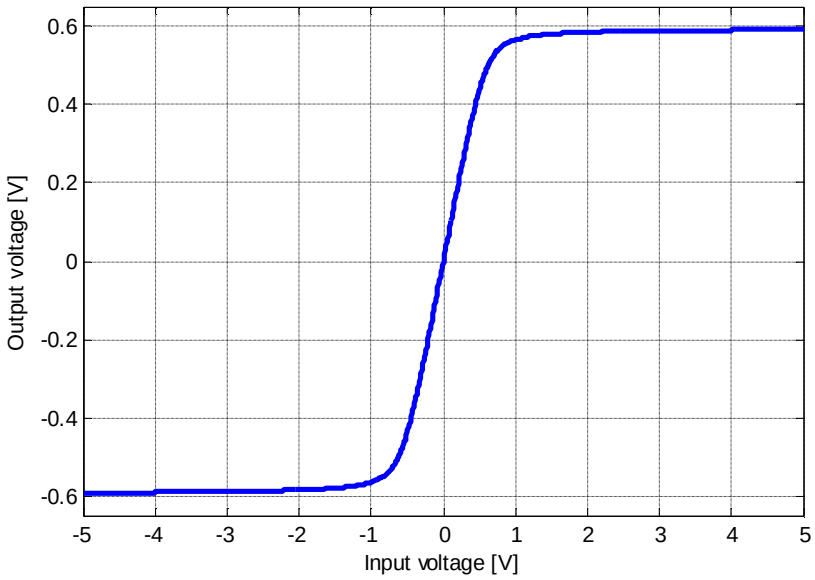

Figure 4.29. Sigmoidal activation function utilizing metallic CNT characteristics

Hence, the circuits given above show the versatility of the utilization of saturated metallic CNT characteristics to design compact nanoscale circuits.

4.4. A Method Developed for Voltage-Dependent Capacitance Extraction for CNTs

The transport properties of CNTs have to be investigated carefully in order to evaluate and increase their performances when they are used as transistor channels or interconnects in VLSI circuits. There are various circuit models concentrated on different parameters of CNTs such as delay, resistance and frequency response. However, complete models of CNTs must include quantum capacitances (C_Q) (John et al., 2004), (Burke, 2002).

CNT circuit models in the literature take constant values for C_Q, independent of the applied voltage on the CNT (Burke, 2002), (Srivastava and Banerjee, 2005). However, the value of the quantum capacitance changes when the applied voltage on the CNT is changed. This is due to the variation of the energy of traveling electrons (John et al., 2004), (Ilani et al., 2006). Hence, in order to accurately model CNTs, quantum capacitance has to be modelled dependent on the applied voltage which has not been considered yet in the literature.

In this subsection, a method to obtain the variation of the quantum capacitance with voltage applied on CNTs is presented (Yamacli and Avci, 2010c). As an application example, the quantum capacitance of a (6,6) metallic CNT is obtained using the proposed method for the voltages between 0V-2.5V. The calculated quantum capacitance values are compared to experimental quantum capacitance values existing in the literature (Ilani et al., 2006), (Donev, 2009).

4.4.1. Quantum Capacitance Concept

Quantum capacitance can be defined as the change in the electronic charge with respect to the change of electrostatic potential in an electron device as given in Equation 4.33 (John et al., 2004). Quantum capacitances in nanoscale devices are

important since as the devices become smaller, the effect of quantum capacitance increases and the quantum capacitances of nanoscaled devices must be taken into account.

$$C_Q = \frac{\partial Q}{\partial V_{ES}} \tag{4.33}$$

4.4.2. Proposed Method for the Extraction of the Quantum Capacitance

The electron charge density and electrostatic potential of a typical CNT at bias voltage V_1 is shown in Figure 4.30 which is composed of real space grids. Also shown in Figure 4.30 is the electronic charge density and the electrostatic potential at an arbitrary point having coordinates of (x_a, y_b, z_N). In Figure 4.31, the same CNT and the labels of the charge density and the electrostatic potential are shown under another applied bias voltage, V_2.

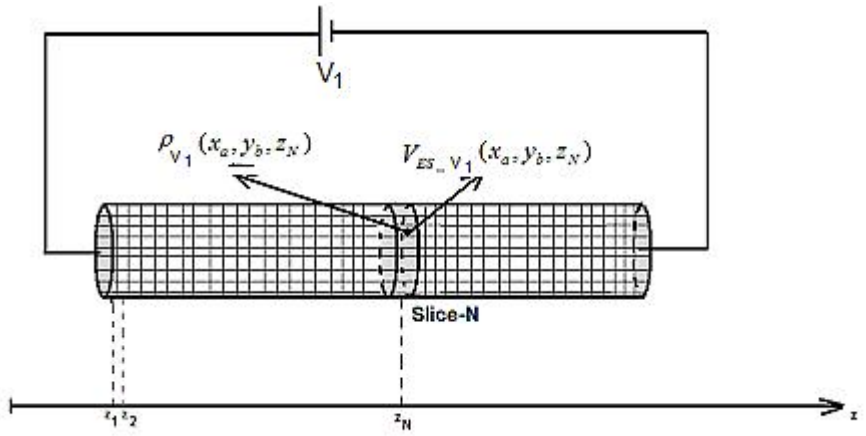

Figure 4.30. CNT interconnect as decomposed into real space grids in ATK for the calculation of the charge density and electrostatic potential at voltage V_1

When the applied voltage on the CNT is V_1, the total electron charge in the slice shown with slice *N* (grey 3-D region) is the sum of charge densities at the coordinate z_N, which can be expressed by Equation 4.34.

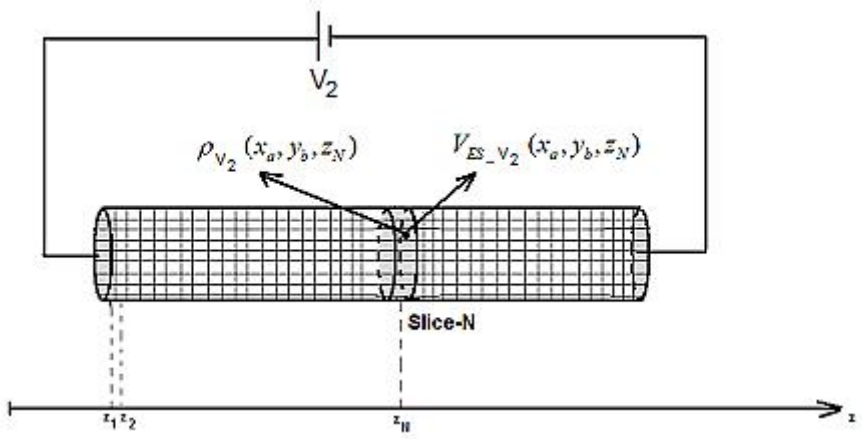

Figure 4.31. CNT interconnect as decomposed into real space grids in ATK for the calculation of the charge density and electrostatic potential at voltage V_2

$$Q_{N\_V_1}(z = z_N) = \sum_{x=x_{\min}, y=_{\min}}^{x=x_{\max}, y=y_{\max}} r_{V_1}(x, y, z = z_N) \tag{4.34}$$

Similarly, the average electrostatic potential of the slice at bias voltage V_1 is the average potential of all the points in slice *N*, which can be expressed in mathematical terms as in Equation 4.35 where avg() represents arithmetic mean.

$$V_{ESN\_V_1} = avg\left(V_{ES\_V_1}\left(x_{\min} < x < x_{\max}, y_{\min} < y < y_{\max}, z = z_N\right)\right) \tag{4.35}$$

When voltage V_2 is applied between the terminals of the CNT as shown in Figure 4.31, the total charge and the average electrostatic potential in the slice *N* change, which can be written in a similar manner as in Equations 4.36 and Equation 4.37, respectively.

$$Q_{N\_V_2}(z = z_N) = \sum_{x=x_{\min}, y=_{\min}}^{x=x_{\max}, y=y_{\max}} r_{V_2}(x, y, z = z_N) \tag{4.36}$$

$$V_{ESN\_V_2} = avg\left(V_{ES\_V_2}\left(x_{\min} < x < x_{\max}, y_{\min} < y < y_{\max}, z = z_N\right)\right) \tag{4.37}$$

On the other hand, from Equation 4.33, the quantum capacitance of slice N can be expressed, using a discrete approach, as the ratio of the change of total charge to the change in electrostatic potential of that slice as in Equation 4.38.

$$C_{Q_N} = \frac{\Delta Q_N}{\Delta V_{ES_N}} = \frac{Q_{N\_V_2} - Q_{N\_V_1}}{V_{ESN\_V_2} - V_{ESN\_V_1}} \tag{4.38}$$

where ΔQ_N and ΔV_{ESN} are the change of the total electronic charge and change of the electrostatic potential of slice N, respectively, when the applied voltage changes from V_1 to V_2. The quantum capacitance of the whole CNT is the sum of the quantum capacitances of all slices as in Equation 4.39.

$$C_Q = \sum_N C_{QN} \tag{4.39}$$

Practically, using the ab initio simulation results of CNTs, Equations 4.35 to 4.39 can be used to obtain the quantum capacitance. For this aim, using ATK and MATLAB, quantum capacitance of a CNT section for various applied voltages are obtained by the following steps.

a. Ab initio simulation of the CNT interconnect is performed for the applied voltage V_1.

b. The calculated electron charge density and electrostatic potential, which are the matrices of the real space position and the value, for the applied voltage V_1, are obtained.

c. The total charge of each slice is calculated by implementing Equation 4.34 and then Q_{N_V1} of all slices are obtained.

d. The electrostatic potential of each slice is calculated by implementing Equation 4.35. In this step, V_{ESN_V1} of all slices are calculated.

e. Ab initio simulation of the CNT interconnect is performed for a the applied voltage V_2.

f. The calculated electron charge density and electrostatic potential of the CNT interconnect, which are the matrices of the real space position and the value are obtained for applied voltage V_2.

g. The total charge of each slice for the applied voltage V_2 is calculated by implementing Equation 4.36. In this step Q_{N_V2} of all slices are obtained.

h. Similarly, the average of the electrostatic potential of each slice for the applied voltage V_2 is calculated by implementing Equation 4.37. In this step, V_{ESN_V2} of all slices are calculated.

i. The change of the total charge and the change of the electrostatic potential, when the applied voltage is raised from V_1 to V_2 are calculated using the quantities obtained in steps c, d, g and h for each slice.

j. The quantum capacitance of each slice is calculated by dividing the change of the total electron charge of that slice to the change of the electrostatic potential in each slice as the implementation of Equation 4.38.

k. The total quantum capacitance is calculated by summing quantum capacitances of all slices as shown in Equation 4.39.

l. Steps e-k are repeated for the desired voltage range.

By using the aforementioned steps, the quantum capacitance values of the CNT interconnect at various applied voltage values are extracted. The presented method is also summarized in the flowchart shown in Figure 4.32. Note that, the quantum capacitances of both metallic and semiconducting CNTs can be calculated using the proposed method since the quantum capacitance in Equation 4.32 is defined for all types of carbon nanotubes (Yamacli and Avci, 2010c).

4.4.3. Simulation of Sample CNTs for Capacitance Calculation

The quantum capacitance of a (6,6) metallic CNT is extracted as an application example of the presented method. The simulated CNT configuration is shown in Figure 4.33. (6,6) CNTs have 4.07Å radius. This type of CNT is chosen because of its versatility thanks to its realizability and small diameter. Electrodes through which the bias voltage is applied are also selected as the same type of CNT

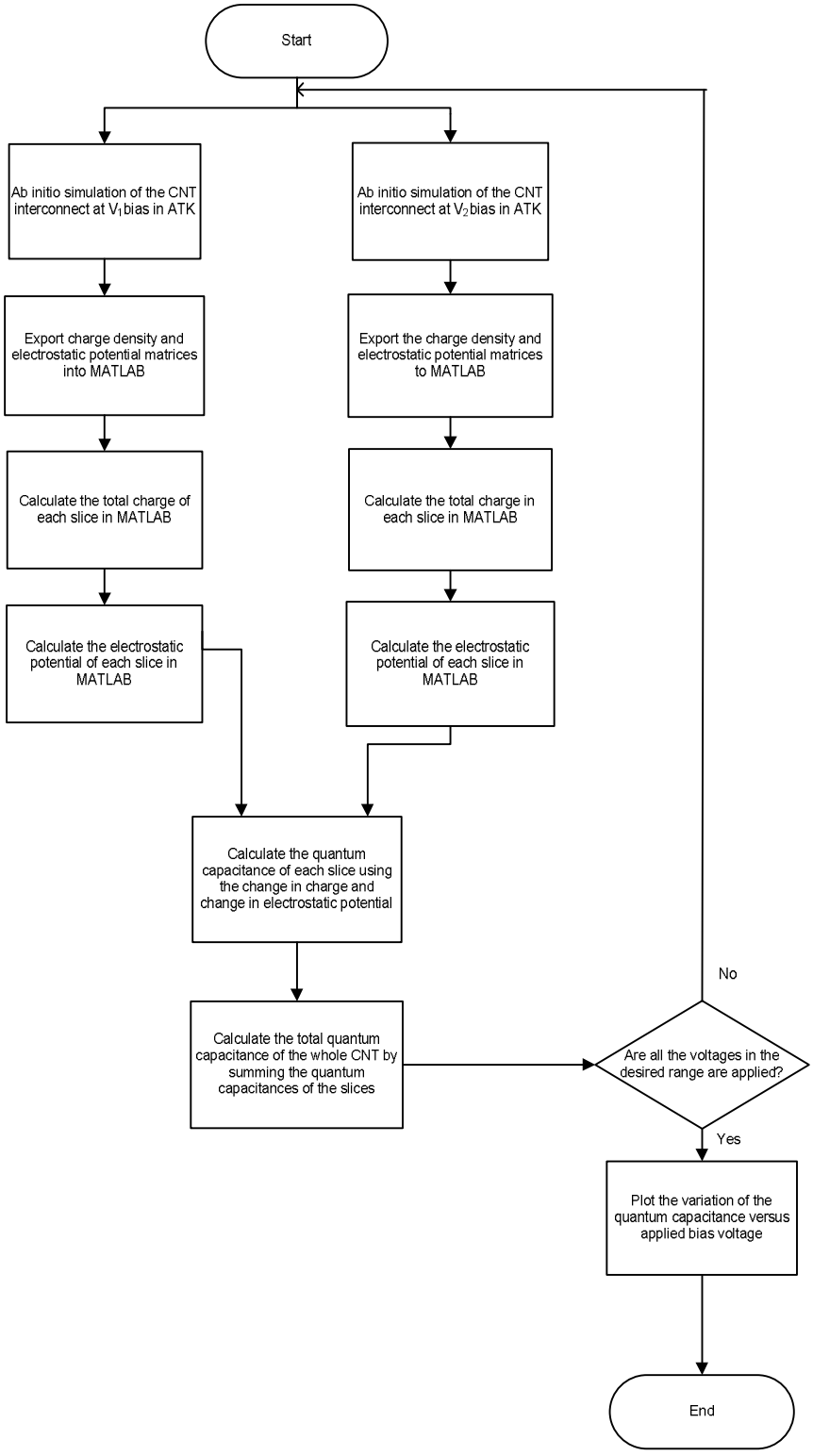

Figure 4.32. Flowchart of the presented method for finding voltage-dependent quantum capacitance

to eliminate contact scattering. Central region length of the simulated CNT is 49.26Å while the electrode lengths are 24.63Å. The lengths are selected by considering a reasonable simulation cost together with the elimination of the possible errors caused by the interactions of electrodes. Electrodes are shown by (S1, S2, SC) in Figure 4.33.

The DFT simulation parameters are selected as follows: mesh cut–off energy is 300Ry, basis set is double zeta polarized with 0.001Bohr radial sampling, exchange correlation functional is local density approximation (LDA). These parameters are selected by considering the results of (Abadir et al., 2009) in order to obtain accurate results at both low and high bias voltages. Brillouin zone integration parameters of electrodes are taken as (1,1,500) and electronic temperature is selected as 300K.

4.4.4. Voltage-Dependent Capacitance Calculation Results

The quantum capacitance-applied voltage (C_Q-V) values of the simulated CNT are obtained using the proposed method. The (6,6) CNT is decomposed into 326x326x326 real space grids in 3–D by ATK and the ab initio results of the charge density and electrostatic potential are exported to MATLAB to apply the proposed method. The quantum capacitance of the (6,6) CNT is calculated for the voltage values in the range of 0V-2.5V by 0.1V increments. Obtained C_Q-V variation of (6,6) CNT is shown in Figure 4.34. The plot in Figure 4.34 shows the quantum capacitance values dependent on the applied bias voltage for 49.26 Å length.

The values of quantum capacitance per unit length (aF/μm) are also calculated from obtained capacitance values and they are plotted in Figure 4.35.

The previously reported experimental values for the quantum capacitance per unit length of CNTs are also marked on Figure 4.35. As it can be seen from the figure, the reported experimental values and the values calculated using the method in this study are consistent.

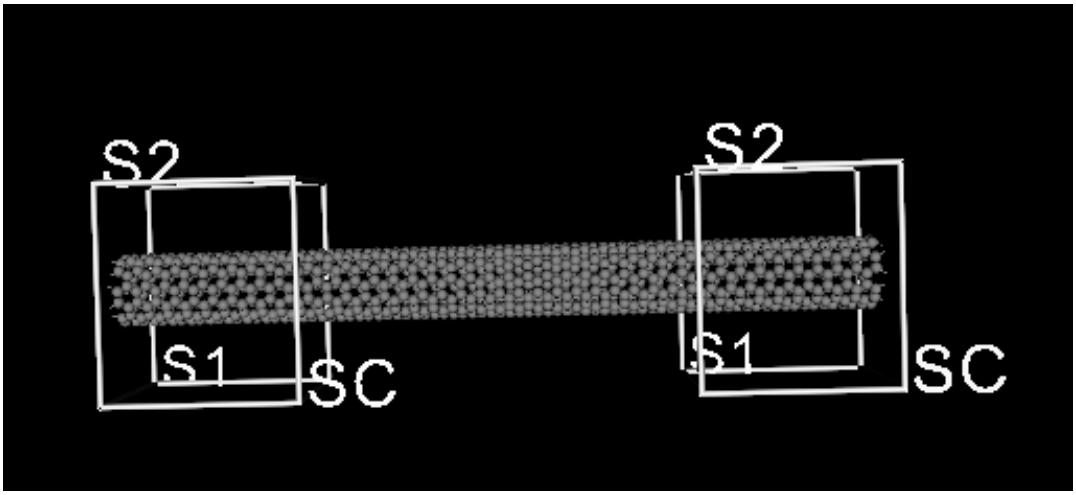

Figure 4.33. Simulated (6,6) metallic CNT section

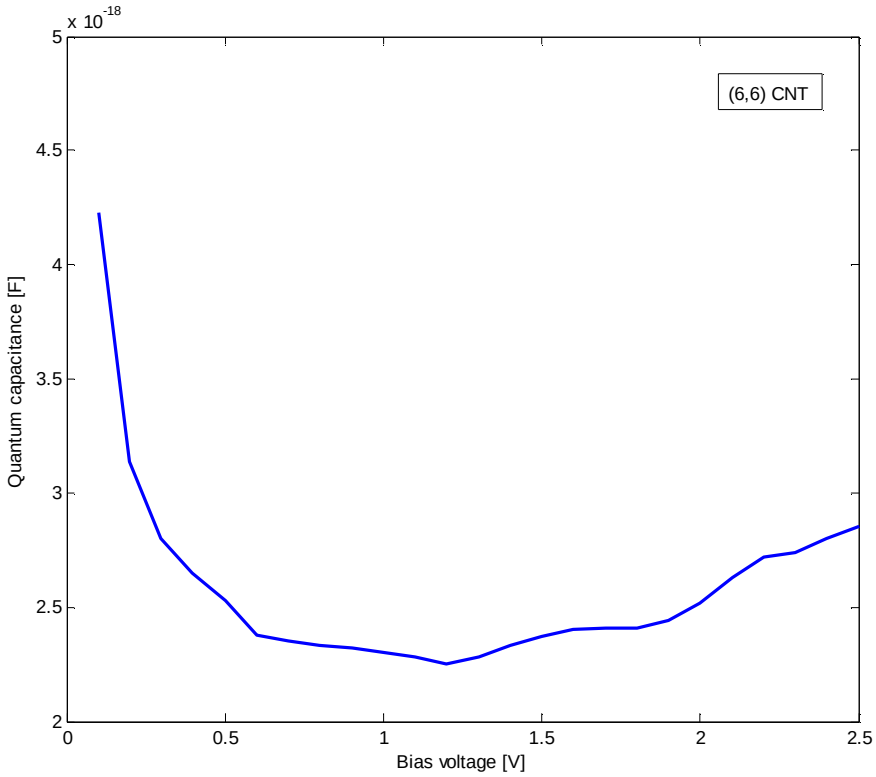

Figure 4.34. Variation of the quantum capacitance with the applied voltage for 49.26Å length

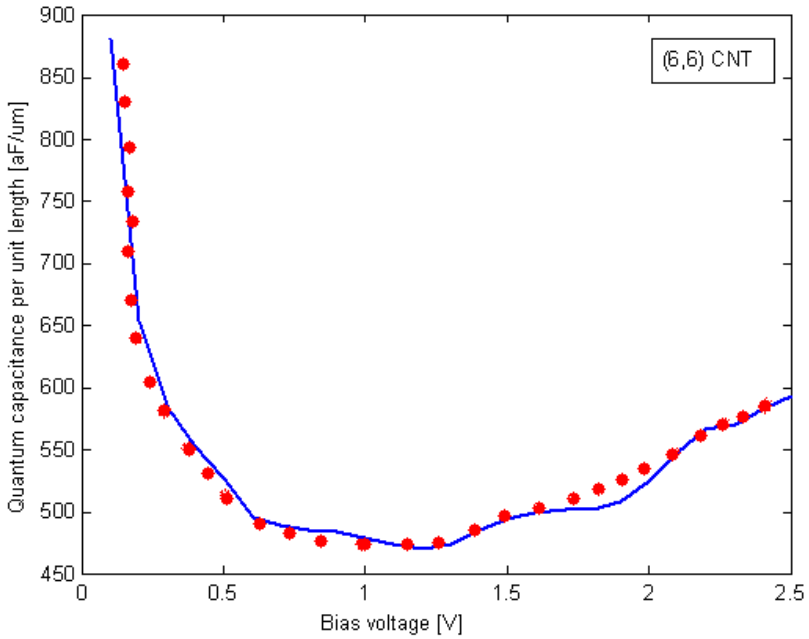

Figure 4.35. Variation of the quantum capacitance with the applied voltage for unit length (solid line: calculation, dots: experimental results)

4.5. Voltage-Dependent Transmission Line Model and Delay Calculation

In this subsection, a CNT interconnect model employing voltage-dependent resistance and capacitance is presented and then the delays of various CNTs are obtained using the given transmission model (Yamacli and Avci, 2011). Finally, delay values obtained from the previous models existing in the literature and the proposed model are compared.

4.5.1. Voltage-dependent Transmission Line Model

Metallic CNTs show current saturation characteristics due to electron-phonon scattering for long CNTs (Javey et al., 2004), (Park et al., 2004) and due to the variation of the channel potential for short CNTs (Yamacli and Avci, 2009). The voltage-dependent resistance of metallic CNTs is modelled as in Equation 4.19 (Hanson, 2008).

On the other hand, equivalent voltage-dependent capacitance of a CNT interconnect can be given as in Equation 4.40 (Burke, 2002).

$$C_{eq}(V_{CNT}) = (C_{ES}{}^{-1} + C_{Q}{}^{-1}(V_{CNT}))^{-1} \tag{4.40}$$

where C_{ES} is the electrostatic capacitance which is voltage independent and $C_Q(V_{CNT})$ is the voltage-dependent quantum capacitance of the CNT interconnect. The voltage-dependent quantum capacitance is given as in Equation 4.41.

$$C_Q(E) = q^2 D(E) \tag{4.41}$$

where q is the elementary charge and $D(E)$ is the density of states function of the CNT interconnect (Donev, 2009). Density of states functions of zigzag and armchair metallic CNTs are given as in Equations 4.42 and 4.43, respectively (Akinwande et al., 2008b).

$$D_{ZZ}(E) = \sum_{u=1}^{2n} g_{ZZ}(E,u) \tag{4.42}$$

$$D_{AC}(E) = \sum_{u=1}^{2n} g_{AC}(E,u) \tag{4.43}$$

where $g_{ZZ}(E, u)$ and $g_{AC}(E, u)$ are the DOS functions of subbands labeled with u as given in Equations 4.44 and 4.45, respectively. In Equations 4.44 and 4.45, E_{vHs1_u} and E_{vHs2_u} *are* van Hove singularity energies, A_{C1_u} and A_{C2_u} are the auxiliary energies, a is CNT's lattice constant and a is the zone degeneracy constant which is 1 if E is at the Brillouin zone center or 2 otherwise (Akinwande et al., 2008b).

$$g_{ZZ}(E,u) = \frac{4a}{\sqrt{3}ap} \frac{|E|}{\sqrt{(E^2 - E_{ZZ\_vHs1\_u}{}^2)(E_{ZZ\_vHs2\_u}{}^2 - E^2)}} \tag{4.44}$$

$$g_{AC}(E,u)=\frac{4a}{ap}\frac{|E|}{\sqrt{(E^2-E_{AC\_vHs1\_u}{}^2)}\sqrt{\left(\sqrt{(E^2-E_{AC\_vHs1\_u}{}^2)}-A_{C1\_u}\right)\cdot\left(-\sqrt{(E^2-E_{AC\_vHs1\_u})}+A_{C2\_u}\right)}} \quad (4.45)$$

Quantum capacitances of zigzag and armchair CNT interconnects can then be written respectively as in Equation 4.46 and Equation 4.47 dependent on the CNT voltage.

$$C_{Q\_zz}(V_{CNT})=q^2\sum_{u=1}^{2n}g_{ZZ}(qV_{CNT},u) \quad (4.46)$$

$$C_{Q\_AC}(V_{CNT})=q^2\sum_{u=1}^{2n}g_{AC}(qV_{CNT},u) \quad (4.47)$$

Voltage-dependent quantum capacitance of CNT interconnects is expressed as functions of the applied voltage in Equations 4.46 and 4.47 for the first time in the literature. The importance of presenting the voltage-dependent capacitance of metallic CNTs in this form stems from the possibility to use these voltage-dependent capacitance functions in VLSI design tools for calculating parameters associated with CNT interconnects such as delay and frequency response.

Taking the voltage-dependent resistance and capacitance into consideration, the transmission line model shown in Figure 4.36 is proposed for CNT interconnects.

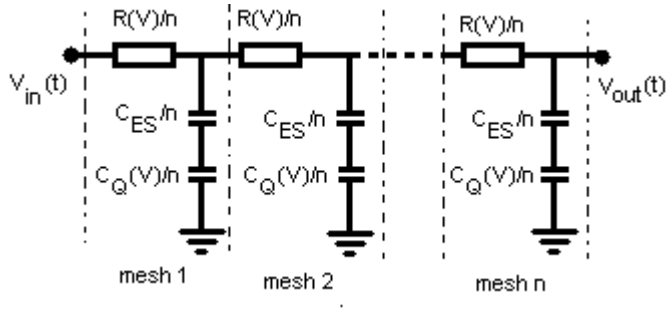

Figure 4.36. Distributed line model of CNT interconnects

The distributed transmission line model has *n* meshes as shown in Figure 4.36. Each lumped voltage-dependent component of CNT interconnect is divided into *n* parts in the distributed model.

4.5.2. Delay Calculation Using the Voltage-Dependent Model

The delay of the CNT interconnect, T_D, is the sum of the delays of each mesh shown in Figure 4.37 according to Elmore delay model, which is given in Equation 4.48 (Gupta et al., 1997), (Avci and Yamacli, 2010d).

$$T_D = \sum_{i=1}^{N} T_{Di} \tag{4.48}$$

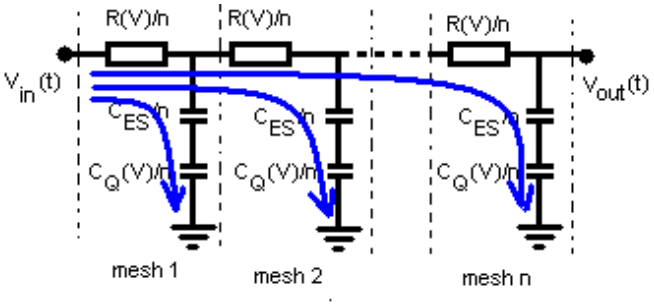

Figure 4.37. Loops used to calculate Elmore delay model

where T_{Di} is the delay of i^{th} loop. Hence, the delay of each loop has to be obtained to calculate the delay of the CNT interconnect.

For the delay calculation of i^{th} loop, Equation 4.49 has to be considered.

$$\underbrace{\frac{C_{eq}(V)}{N}}_{\substack{\text{capacitance} \\ \text{of } i^{th} \text{ mesh}}} \cdot \underbrace{\frac{i.R(V)}{N}}_{\substack{\text{resistance} \\ \text{of } i^{th} \text{ mesh}}} \cdot \frac{dV_{out}(t)}{dt} + V_{out}(t) = V_{in}(t) \tag{4.49}$$

Substituting voltage-dependent resistance and capacitance functions of Equation 4.19 and Equation 4.40, into the above equation gives Equation 4.50.

$$\left(C_{ES}{}^{-1} + \left(\underbrace{q^2 DOS(V_{out}(t) - V_{in}(t))}_{C_Q(V)} \right)^{-1} \right)^{-1} \left(i. \left(\underbrace{\frac{h}{4q^2} + \frac{h}{4q} \frac{V_{out}(t) - V_{in}(t)}{E_{ph}}}_{R_i(V)} \right) \frac{1}{N^2} \frac{dV_{out}(t)}{dt} \right) + V_{out}(t) = V_{in}(t) \tag{4.50}$$

For metallic zigzag and armchair CNT interconnects, Equation 4.52 can be written as Equations 4.51 and 4.52, respectively, considering voltage-dependent capacitance functions of Equations 4.46 and 4.47.

$$\left(C_{ES}{}^{-1} + \left(\underbrace{q^2 \left(\sum_{u=1}^{2n} g_{ZZ}(q(V_{out}(t) - V_{in}(t)), u) \right)}_{C_Q(V)} \right)^{-1} \right)^{-1} \cdot \left(\underbrace{\frac{h}{4q^2} + \frac{h}{4q} \frac{V_{out}(t) - V_{in}(t)}{E_{ph}}}_{R_i(V)} \right) \frac{i}{N^2} \frac{dV_{out}(t)}{dt} + V_{out}(t) = V_{in}(t) \tag{4.51}$$

$$\left(C_{ES}{}^{-1} + \left(\underbrace{q^2 \left(\sum_{u=1}^{2n} g_{AC}(q(V_{out}(t) - V_{in}(t)), u) \right)}_{C_Q(V)} \right)^{-1} \right)^{-1} \cdot \left(\underbrace{\frac{h}{4q^2} + \frac{h}{4q} \frac{V_{out}(t) - V_{in}(t)}{E_{ph}}}_{R_i(V)} \right) \frac{i}{N^2} \frac{dV_{out}(t)}{dt} + V_{out}(t) = V_{in}(t) \tag{4.52}$$

For the delay calculation, Equations 4.51 and 4.52 should be solved and then the 50% delay, T_{Di}, has to be calculated using Equation 4.53 when $V_{in}(t)$ is the unit step function.

$$V_{out}(T_{Di}) = 0.5V_{in} \tag{4.53}$$

Hence, in order to obtain an analytical expression for time delay T_{Di}, the analytical solutions to nonlinear differential equations of Equation 4.51 and Equation 4.52 are required. Unfortunately, analytical solutions for these equations do not exist. However, delay can be obtained for specific types of metallic CNTs by using voltage-dependent resistance and capacitance expressions given in Equation 4.19 and Equation 4.40 are imported as Verilog-A models in HSPICE. To demonstrate this, the delays of (9,0), (12,0) and (8,8) metallic CNTs are obtained in HSPICE for L=300nm, E_{ph}=0.2eV (Donev, 2009) and C_{ES}=53.73aF/μm (Hanson, 2008) using voltage-dependent model and then compared to the delay of existing voltage-independent CNT models.

Firstly, delays of (9,0), (12,0) and (8,8) CNT interconnects are obtained from HSPICE simulations using the voltage-independent resistance and capacitance. The resistance of the CNT is taken as 6.512kΩ, the electrostatic and quantum capacitances are taken as 53.73aF/μm and 400aF/μm, respectively (Burke, 2002), (Hanson, 2008) with 100 distributed components and L=300nm. The obtained input and output voltages are plotted in Figure 4.38. The obtained 50% delay using voltage-independent model is 4.17fs for all types of CNTs. Note that, since previous voltage-independent models take the same constant value for the resistances and capacitances of different types of metallic CNTs, the obtained delays for different types of CNTs are the same.

Secondly, simulations using voltage-dependent resistance and capacitance models proposed in this study are performed. The van Hove singularity energies needed in the formulation of the quantum capacitance are calculated for (9,0), (12,0) and (8,8) CNTs and then the voltage-dependent resistance and quantum capacitances are imported into HSPICE using Verilog-A language. The number of distributed elements is again taken as 100 with L=300nm. The simulated transient characteristics are plotted in Figure 4.39. For (8,8), (9,0) and (12,0) CNTs, obtained delays are 18.44fs, 18.82fs and 19.18fs, respectively. As it can be seen from Figure 4.39, the

output waveforms and delays of different types of CNTs are slightly different since quantum capacitances change according to the DOS function for different chiralities. 10%-90% rise time delays for (8,8), (9,0) and (12,0) CNTs obtained from simulations are also given in Table 4.1.

The voltage-dependency of the resistance and the capacitance utilized in the proposed voltage-dependent model are verified by experiments given in (Javey et al., 2004) and (Donev, 2009), respectively.

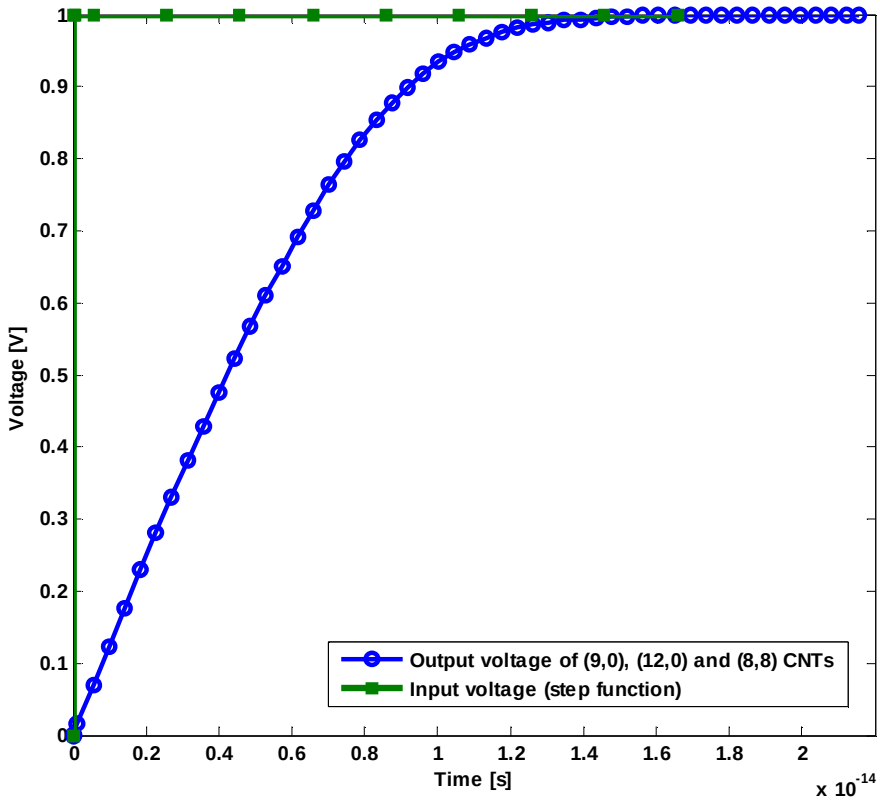

Figure 4.38. The waveforms of input and output voltages for the distributed CNT model using constant resistance and capacitance

On the other hand, the propagation velocity for metallic CNTs given in (Hanson, 2006) can also be used to verify the results of the voltage-dependent CNT model. In (Hanson, 2006), the propagation velocity for metallic CNTs is obtained as $v_p=0.025c$ using electromagnetics, where c is the speed of light having the value 3.10^8m/s. Since the length of the simulated CNTs in this study is 300nm, the total

delay using the propagation velocity given in (Hanson, 2006) can be obtained as in Equation 4.54

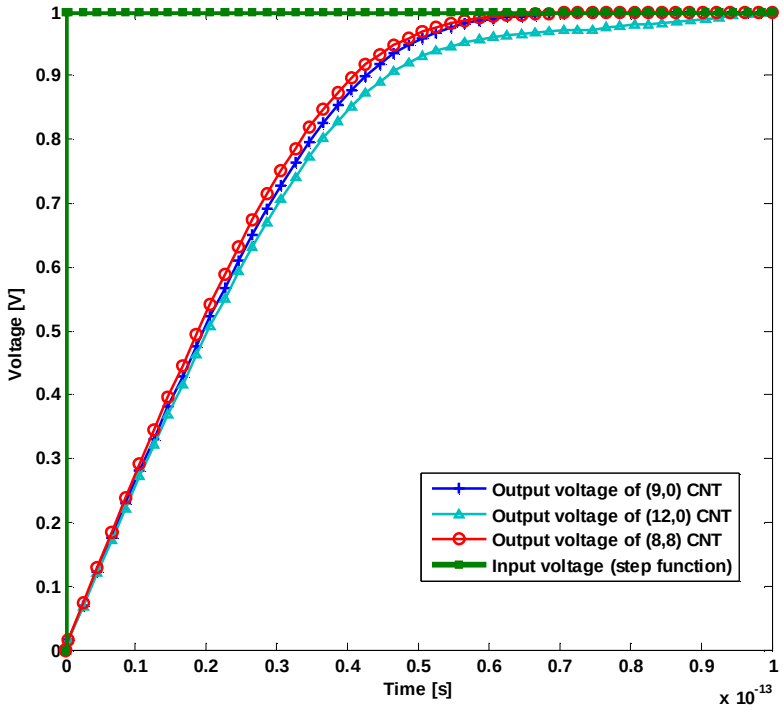

Figure 4.39. The waveforms of input and output voltages for the distributed CNT model using voltage-dependent resistance and capacitance models for (9,0), (12,0) and (8,8) CNTs

Table 4.1. 10%-90% rise time delays of (8,8), (9,0) and (12,0) CNTs obtained with voltage-independent and voltage-dependent models

CNT type / Model	(8,8)	(9,0)	(12,0)
Delay obtained using voltage-independent model	8.29fs	8.29fs	8.29fs
Delay obtained using voltage-dependent model	37.67fs	40.02fs	42.67fs

$$t_d = \frac{300nm}{0.025c} = \frac{300.10^{-9}m}{75.10^5 m/s} = 4.10^{-14}s = 40\,fs \qquad (4.54)$$

Hence, comparing the numerical values given in Table 4.1 to the calculation of Equation 4.54, it can be seen that, the delay calculated using the propagation velocity obtained from electromagnetics is close to the delay obtained using the voltage-dependent circuit model proposed in this study.

As it is clearly seen from the simulation results, utilization of voltage-dependent models for resistance and quantum capacitance significantly affects the calculated delay of CNT interconnects. This shows that the voltage-independent approximation of metallic CNT resistances and capacitances causes nonignorable errors hence voltage-dependent model for metallic CNTs has to be used. Moreover, the utilization of the proposed voltage-dependent model is not cumbersome since the voltage-dependent model can be expressed in Verilog-A language that can be used in many engineering tools (Yamacli and Avci, 2011).

4.6. SPICE Compatible CNTFET Model Employing Self-Consistent Charge Calculation

From electronics engineering point of view, CNTFETs have to be modelled as accurately as possible in order to use these models in circuit tools to design and analyse CNTFET circuits. There are various CNTFET models in the literature that permit IC design engineer to utilize these models in the nanoscale design process. For instance, in (Deng and Wong, 2007a), a circuit compatible compact model for CNTFETs is presented which provides intrinsic channel behaviour. A more detailed modeling is shown in (Deng and Wong, 2007b) where practical device nonidealities such as source and drain region resistance and various capacitances are included. A physics based CNTFET model utilizing approximate analytical expressions for channel charge is given in (Fregonése et al., 2008). This model also includes device non-idealities with a channel potential calculation method based on piecewise function approximation. A curve fitting is performed for the variation of channel charge with gate and drain voltages in (Raychowdhury et al., 2004). A fitted function is obtained for the channel charge which is then used to calculate electrical properties such as drain current and the quantum capacitance. Predictive CNTFET models are

also proposed (Goguet et al., 2008), (Belijepalli et al., 2007) that can be used in circuit design and simulation. In another study, a model based on local channel approximations is developed (O'Connor et al., 2007). The common approach of the studies existing in the literature is that they utilize an approximate channel charge equation or calculation method instead of calculating the channel charge self-consistently dependent on the channel potential. The approximate calculation of the channel charge is acceptable for a range of gate and drain voltages however not for the whole gate and drain voltage range and not suitable for all possible diameters of the semiconducting CNT used as the channel region.

A SPICE compatible circuit model for CNTFETs which uses self-consistent approach to obtain the channel charge hence providing a more accurate representation of CNTFET behaviour is presented in this subsection. The proposed model also includes device non-idealities such as parasitic capacitance and resistance of source and drain contacts. Moreover, the self-consistent calculation of channel charge and channel potential does not only enable to calculate the drain current of the CNTFET more accurately, however it also provides the accurate calculation of quantum capacitance.

4.6.1. Schematics of the Model

The proposed model is shown in Figure 4.40.

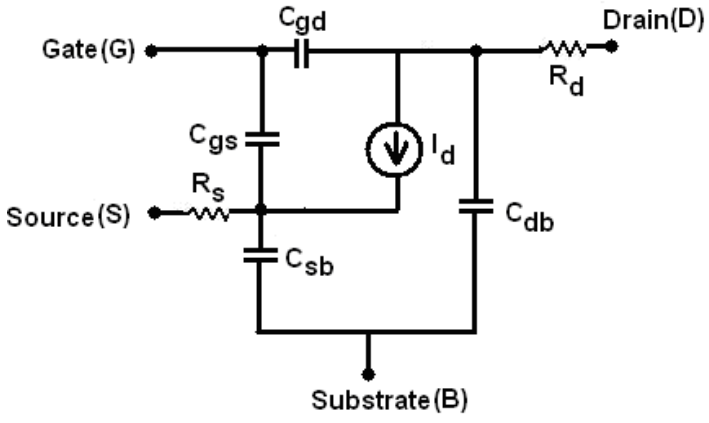

Figure 4.40. Proposed SPICE compatible CNTFET model

The proposed model is suitable for both planar and cylindrical gate CNTFETs. In the proposed model, the main element is the controlled current source depicited by I_d. The value of this current is calculated using quantum mechanical treatment as explained in detail in the following subsection. Capacitors C_{sb} and C_{db} are source-substrate and drain-substrate capacitors which are independent of source and drain voltages however dependent on the physical parameters such as source and drain area and the bulk permittivity. R_s and R_d model the parasitic resistance of source and drain contacts which are also independent of the applied voltages. On the other hand, C_{gs} and C_{gd}, which are gate-source and gate-drain capacitances, respectively, are highly dependent on the source and drain voltages due to the variation of the quantum capacitance with the applied voltage (Yamacli and Avci, 2010c).

4.6.2. Mathematical Expressions of the Model Parameters

4.6.2.1 Static Parameters

Source and drain parasitic resistances can be expressed as in Equation 4.55 and Equation 4.56, respectively.

$$R_s = r_s \frac{L_s}{W_s H_s} \tag{4.55}$$

$$R_D = r_D \frac{L_D}{W_D H_D} \tag{4.56}$$

where L_D, W_D, H_D, L_S, W_S, H_S are the length, width and height of the drain and source contacts, respectively. ρ_s ρ_d are the resistivities of the source and drain region, respectively. Source-bulk and drain-bulk capacitances are respectively given as in Equation 4.57 and Equation 4.58.

$$C_{sb} = e_{subs} e_0 \frac{W_s L_s}{W_{subs}} \tag{4.57}$$

$$C_{db} = e_{subs} e_0 \frac{W_d L_d}{W_{subs}} \tag{4.58}$$

where ε_{subs} and W_{subs} are the relative dielectric constant and width of the substrate and ε_0 is the permittivity of the free space. Electrostatic gate capacitance per unit length of the CNTFET is given as in Equation 4.59 and Equation 4.60.

$$C_{g\_static\_gaa} = \frac{2pe_g e_0}{\ln\left(\frac{t + d/2}{d/2}\right)} \tag{4.59}$$

$$C_{g\_static\_p} = \frac{2pe_g e_0}{\cosh^{-1}\left(\frac{t}{d}\right)} \tag{4.60}$$

for gate all around (cylindrical) and plane gate CNTFETs, respectively, where ε_g is the relative dielectric constant of the gate insulator material, t is the gate oxide thickness and d is the CNT diameter (Raychowdhury et al., 2004)

4.6.2.2. Dynamical Parameters

The drain current of a CNTFET can be expressed as in Equation 4.61 (Raychowdhury et al., 2004).

$$I_D = \frac{4qk_B T}{h} \sum_p \left[\ln\left(1 + \exp(x_S)\right) - \ln\left(1 + \exp(x_D)\right) \right] \tag{4.61}$$

where k_B is Boltzmann's constant, T is the absolute temperature, h is Planck's constant, p is the number of subbands contributing to the conduction. In Equation

4.61, ξ_S and ξ_D are given respectively as in Equation 4.62 and Equation 4.63 (Frégonese et al., 2008).

$$x_S = \frac{m_S - U_{CNT} - U_{\min\_p}}{k_B T} \tag{4.62}$$

$$x_D = \frac{m_D - U_{CNT} - U_{\min\_p}}{k_B T} \tag{4.63}$$

In Equation 4.62 and Equation 4.63, μ_S and μ_D are the electrochemical potentials of the source and drain contacts; U_{CNT} is the potential of the semiconducting CNT channel and U_{min_p} is the minimum of the p^{th} subband. μ_S and μ_D can be expressed in electrical terms as shown in Equations 4.64 and 4.65 (Frégonese et al., 2008).

$$m_S = qV_S \tag{4.64}$$

$$m_D = qV_D \tag{4.65}$$

where q is the elementary charge, V_S is the voltage of the source contact and V_D is the voltage of thee drain contact.

The channel potential, U_{CNT}, can be given as in Equation 4.66 (Rahman et al., 2003).

$$U_{CNT} = U_L + U_P \tag{4.66}$$

In Equation 4.66, U_L is the potential representing the influence of contacts on the channel potential and U_P is the charging potential. Charging potential depends on the number of charges in the CNT channel. These potentials can be expressed as in Equation 4.67 and Equation 4.68, respectively.

$$U_L = -q(a_G V_G + a_D V_D) \tag{4.67}$$

$$U_P = \frac{q^2}{C_{G\_static}} \Delta Q_c \tag{4.68}$$

In Equation 4.67, parameters α_G and α_D are the coefficients which model the influence of gate and drain voltages over the channel potential. ΔQ_C is the change in the channel charge. ΔQ_C can be expressed as in Equation 4.69.

$$\Delta Q_C = Q_1 + Q_2 - Q_0 \tag{4.69}$$

where Q_1, Q_2 and Q_0 are charges induced by source contact, drain contact and the equilibrium charge, respectively. These quantities can be written as in Equation 4.70, Equation 4.71 and Equation 4.72, respectively (Rahman et al., 2003).

$$Q_0 = \int_{-\infty}^{\infty} D(E) f(E - E_F) dE \tag{4.70}$$

$$Q_1 = \frac{q}{2} \int_{-\infty}^{\infty} D(E - U_{CNT}) f(E - E_{F1}) dE \tag{4.71}$$

$$Q_2 = \frac{q}{2} \int_{-\infty}^{\infty} D(E - U_{CNT}) f(E - E_{F2}) dE \tag{4.72}$$

where E_F is the equilibrium Fermi level of the CNTFET, E_{F1} and E_{F2} are the Fermi levels of the source and drain contacts and $D(E)$ is the density of states function of the CNT channel (Rahman et al., 2003). $D(E)$ can be taken as in Equation 4.73 (Koswatta et al., 2005).

$$D(E) = D_0 \frac{E}{\sqrt{E^2 - E_p^{\ 2}}} \tag{4.73}$$

In Equation 4.73, E_p is the minimum energy of the p^{th} subband and D_0 is the fundamental density of states given in Equation 4.74.

$$D_0 = \frac{8}{3pg_0 b} \tag{4.74}$$

where γ_0 and b are the carbon-carbon (C-C) bond energy and C-C bond distance of the CNT channel, respectively.

On the other hand, source-gate and drain-gate capacitances can be written as in Equation 4.75 and Equation 4.76 respectively.

$$C_{gs} = 0.5\left(\frac{C_{g\_static} C_Q(V_{GS}, V_{DS})}{C_{g\_static} + C_Q(V_{GS}, V_{DS})}\right) \tag{4.75}$$

$$C_{gd} = 0.5\left(\frac{C_{g\_static} C_Q(V_{GS}, V_{DS})}{C_{g\_static} + C_Q(V_{GS}, V_{DS})}\right) \tag{4.76}$$

where quantum capacitance of the CNT channel can be expressed as in Equation 4.77 (John et al., 2004).

$$C_Q(V_{GS}, V_{DS}) = \left.\frac{dQ_C}{dU_{CNT}}\right|_{V_{GS}, V_{DS}} \tag{4.77}$$

Taking Equation 4.67 to Equation 4.74 into consideration, it can be observed that the potential and the charge of the CNTFET channel are functions of each other thus they have to be solved iteratively. There are various quantum mechanical simulators for CNTFETs in different environments such as MATLAB and ViDES (Rahman et al., 2003), (Fiori et al., 2006). However, there is not any study to utilize this type of accurate self-consistent calculation in a SPICE compatible model. This improvement is accomplished in this thesis. Once the channel charge and potential is obtained, drain currennt and voltage dependent dynamic capacitances can be obtained using Equations 4.61 to 4.77 hence providing an accurate description of the dynamic behaviour of the CNTFET in the SPICE compatible model.

4.6.3. Implementation of the Model in Verilog-A Language

The circuit of Figure 4.40 is implemented in Verilog-A hardware description language (HDL) using the static and dynamic component equations given in Equation 4.55 to Equation 4.77. The flowchart of the Verilog-A model is shown in Figure 4.41. Self-consistent calculation of the channel charge and channel potential is implemented in Verilog-A for the first time in the literature.

The calculation of self-consistent channel charge and potential is achieved by a "for" loop in the Verilog-A model. Firstly, an arbitrary initial channel potential is set and then the corresponding channel charge is calculated using Equation 4.69 to Equation 4.74. Then, for the calculated channel charge, a new channel potential is obtained using Equation 4.71 to Equation 4.73 If the new potential is greater than the old potential value, then the old potential value is incremented by one potential unit. In this manner, calculated CNT channel potential converges to the actual value by a maximum error of $1/N_{itr}$ (V) when the potential unit is given the value of Equation 4.78.

$$\Delta U_{CNT} = 1 / N_{itr} \tag{4.78}$$

where N_{itr} is the number representing the number of cycles in the calculation loop.

On the other hand, the integrations of Equation 4.70 to Equation 4.72 are performed as numerical integration where the variable of integration is divided into 1000 equal parts which also provides accurate integration.

In the quantum capacitance calculation of Equation 4.77, the infinitesimal variation of the channel potential is implemented as $0.01V_T$. The channel potential is varied in this range and then the change in channel charge is calculated. Quantum capacitance is obtained as the ratio of the change in charge to the change in the potential (John et al., 2004).

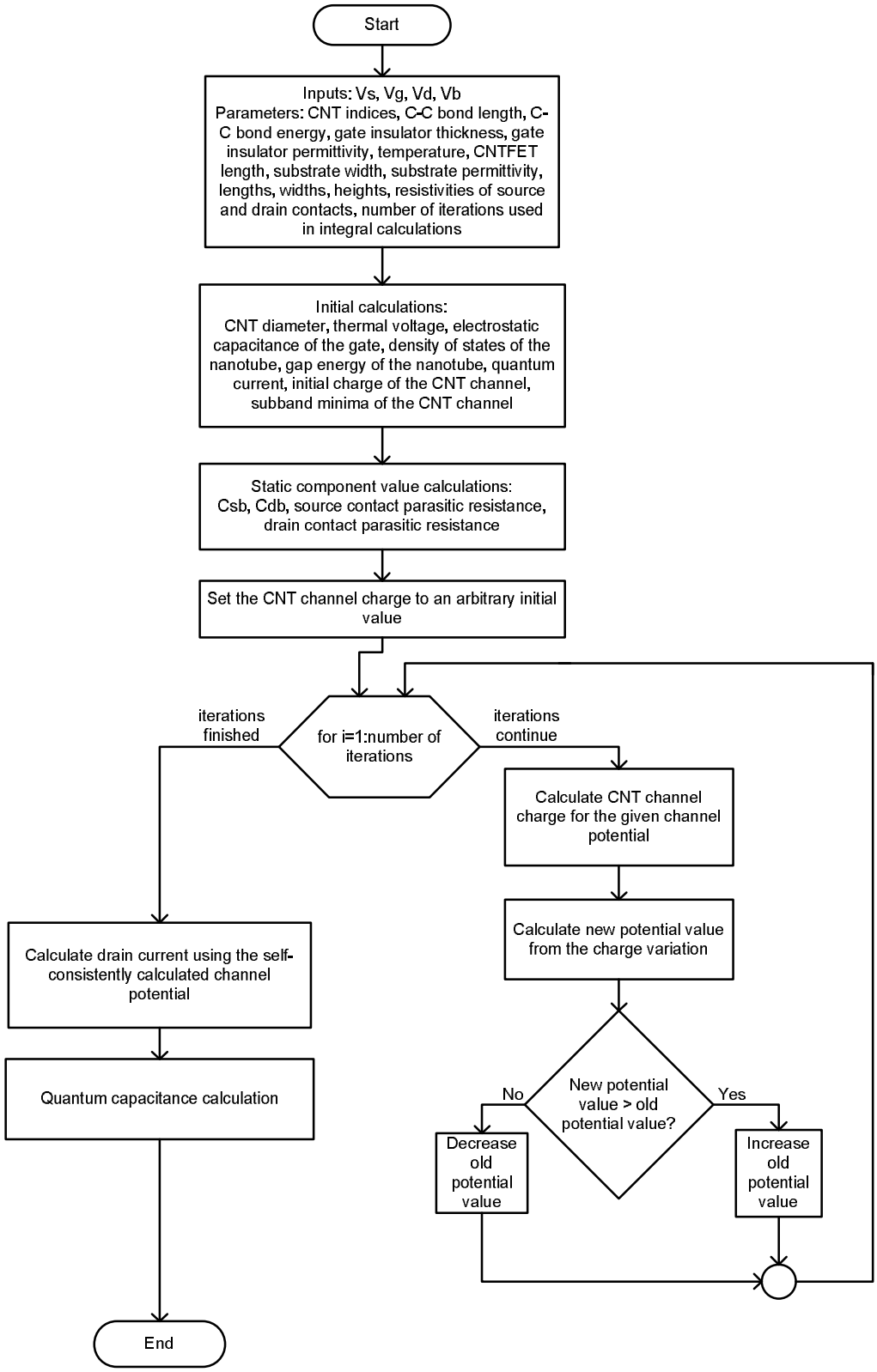

Figure 4.41. Detailed flowchart of the procedure for calculating the parameters of the presented model

4.6.4. Test Results Of The Presented CNTFET Model

I_D-V_{GS}, I_D-V_{DS} and C_Q-V_{GS} characteristics of an n-type GAA-CNTFET employing (11,0) semiconducting CNT as its channel is obtained in HSPICE using our model as an example and the results are compared to the characteristics obtained from the quantum mechanical cylindrical CNTFET simulator of Nanohub which implements the models given in (Koswatta et al., 2005a), (Koswatta et al., 2005b), (Guo et al., 2004). Obtained results for drain current vs. gate-source voltage, drain current vs. drain-source voltage and quantum capacitance vs. gate-source voltage are given in Figure 4.42, Figure 4.43 and Figure 4.44, respectively.

As it can be seen from these figures, the results of the quantum mechanical simulator and the presented SPICE compatible Verilog-A model are very close. This shows the accuracy of the proposed model.

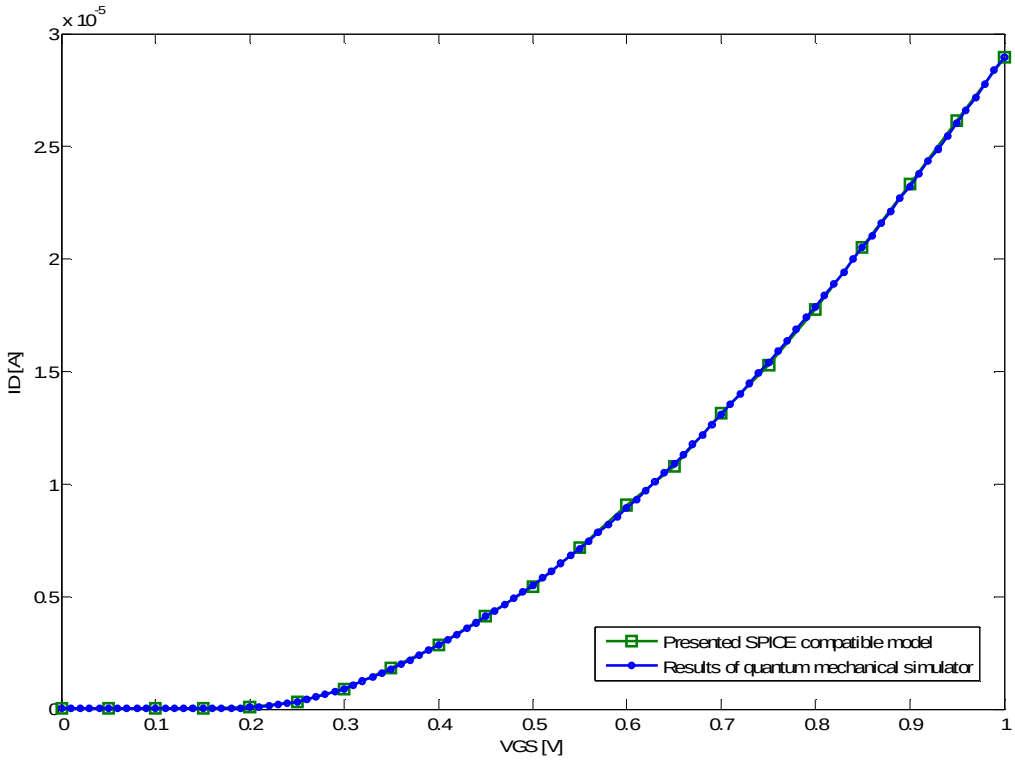

Figure 4.42. I_D-V_{GS} variation obtained in HSPICE using the presented model and obtained from the quantum mechanical simulator for V_{DS}=1V

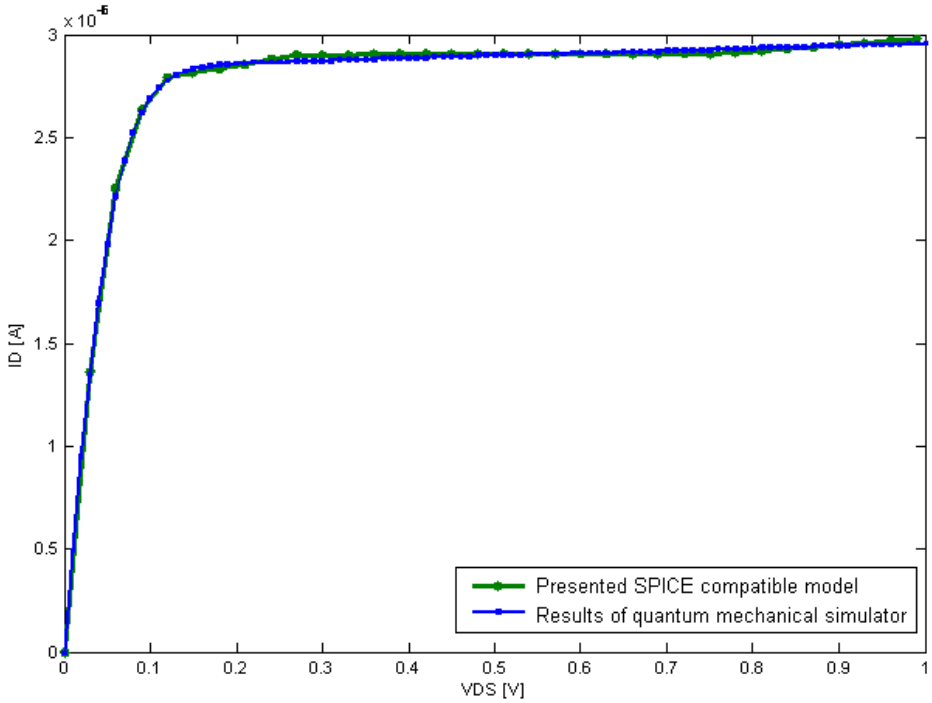

Figure 4.43. I_D-V_{DS} variation obtained in HSPICE using the presented model and obtained from the quantum mechanical simulator for V_{GS}=0.4V

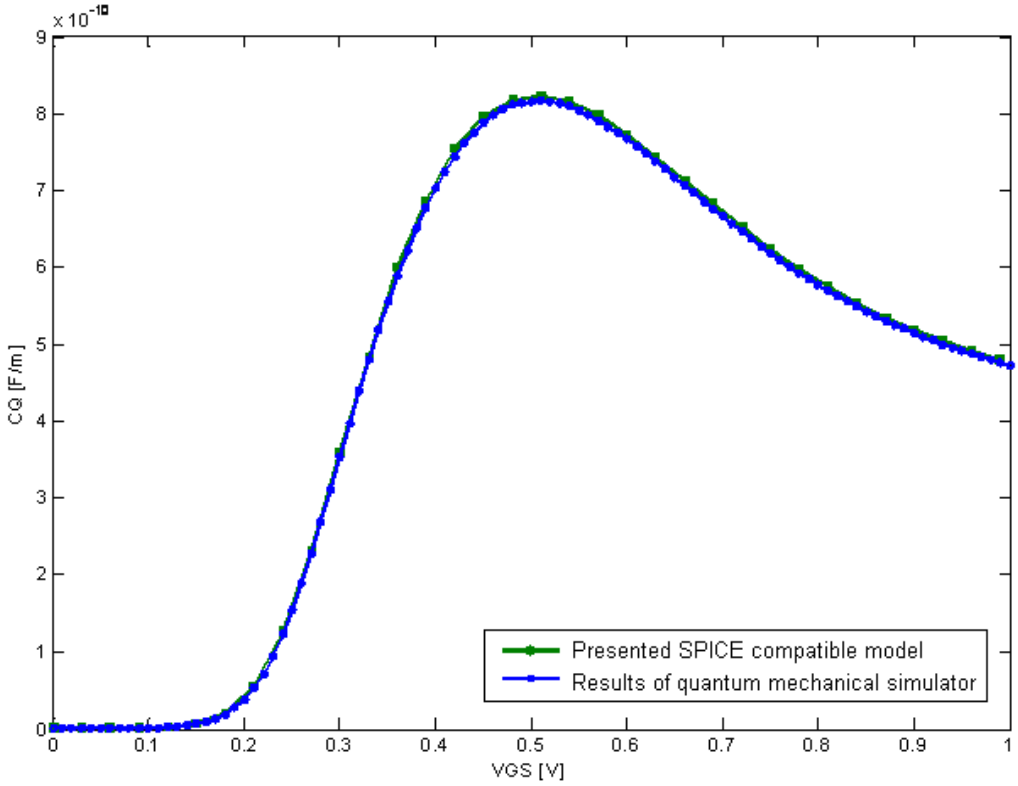

Figure 4.44. C_Q-V_{GS} variation obtained in HSPICE using the presented model and obtained from the quantum mechanical simulator for V_{DS}=1V

4.7. Sample Circuit Simulations Using the Proposed Model

Sample circuit blocks are simulated using the presented SPICE compatible model in HSPICE to show the useability of the model. GAA-CNTFETs are selected as (11,0) with 10nm length in all simulations.

4.7.1. Inverter Circuit Utilizing CNTFETs

The inverter circuit of Figure 4.45 is simulated in HSPICE using the presented SPICE compatible model. The channels CNTFETs are of (11,0) CNT and the supply voltage is V_{dd}=1V. Obtained characteristics is given in Figure 4.46.

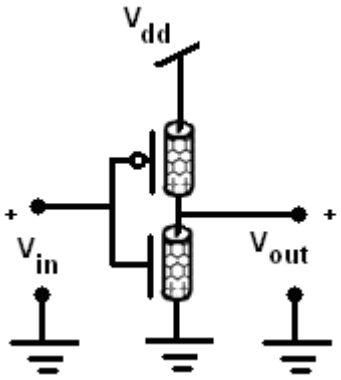

Figure 4.45. Inverter circuit utilizing CNTFETs

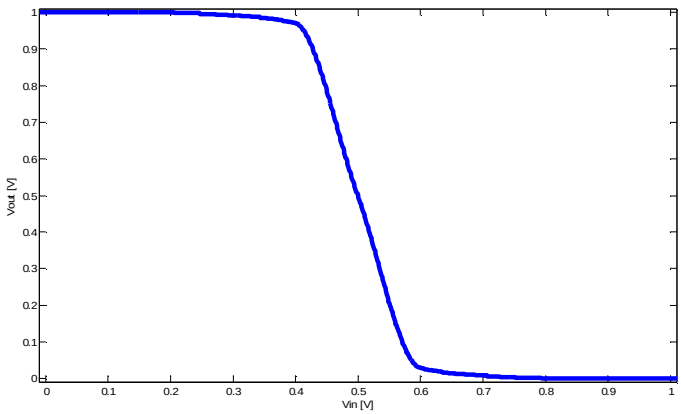

Figure 4.46. Input-output characteristics of the CNTFET inverter circuit

4.7.2. Ring Oscillator Using CNTFETs

A ring oscillator is simulated which consists of 31 stages of the inverter as shown in Figure 4.47 to show the dynamic response of the inverter. The output voltage is shown in Figure 4.48. Obtained oscillation frequency is 491 MHz which with 1V supply voltage and 10nm CNT channel lengths. Hence, the delay of each inverter is 65ps.

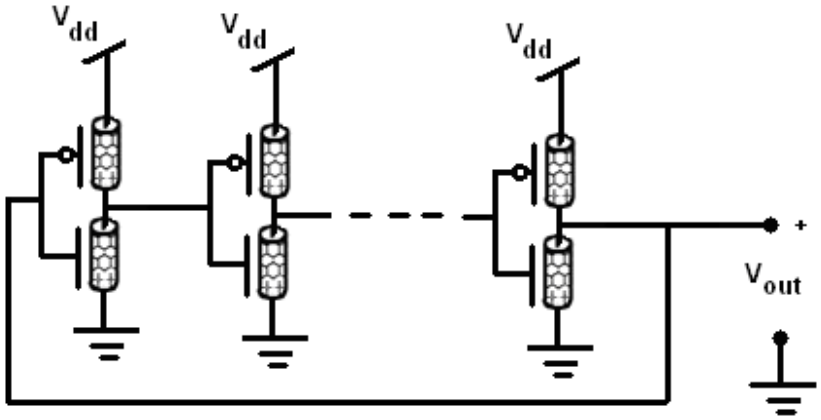

Figure 4.47. Ring oscillator circuit employing CNTFETs

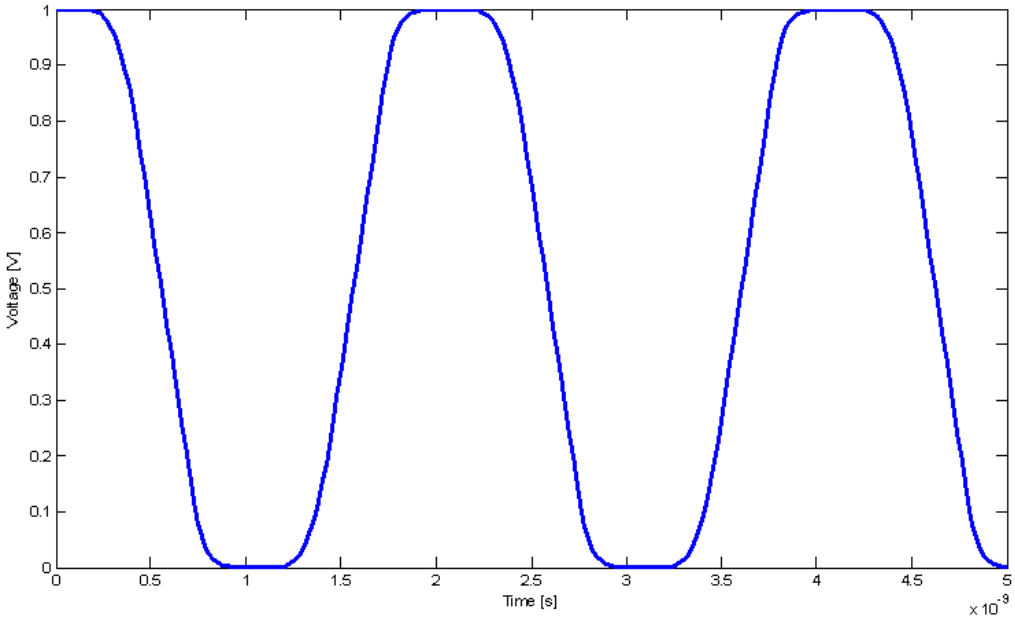

Figure 4.48. Output voltage of the ring oscillator

4.7.3. Operational Amplifier Using CNTFETs

The operational amplifier circuit of Figure 4.49 is simulated in HSPICE with supply voltages of V_{DD}=0.5V, V_{SS}=–0.5V and I_{B1}=I_{B2}=100μA. DC and AC transfer characteristics are given in Figure 4.50 and Figure 4.51, respectively. The gain of the operational amplifier circuit is 167.2dB with an output resistance of 259Ω in the open loop. Offset voltage is determined as 0.87mV with the accurate matching of p-type and n-type CNTFETs.

4.7.4. Operational Transconductance Amplifier (OTA) Using CNTFETs

The simple OTA structure employing CNTFETs as shown in Figure 4.52 is simulated with V_{DD}=–V_{SS}=0.5V and R_L=100Ω. DC and AC characteristics of the OTA are shown in Figure 4.53 and Figure 4.54, respectively.

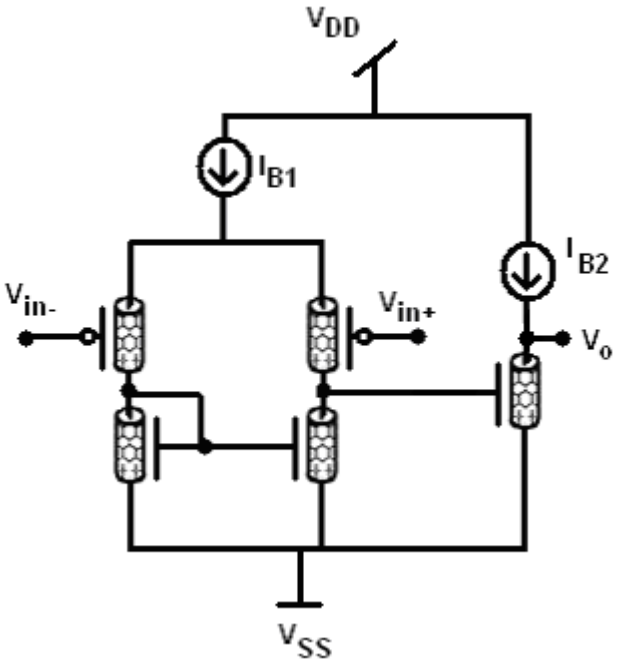

Figure 4.49. Operational amplifier circuit utilizing CNTFETs

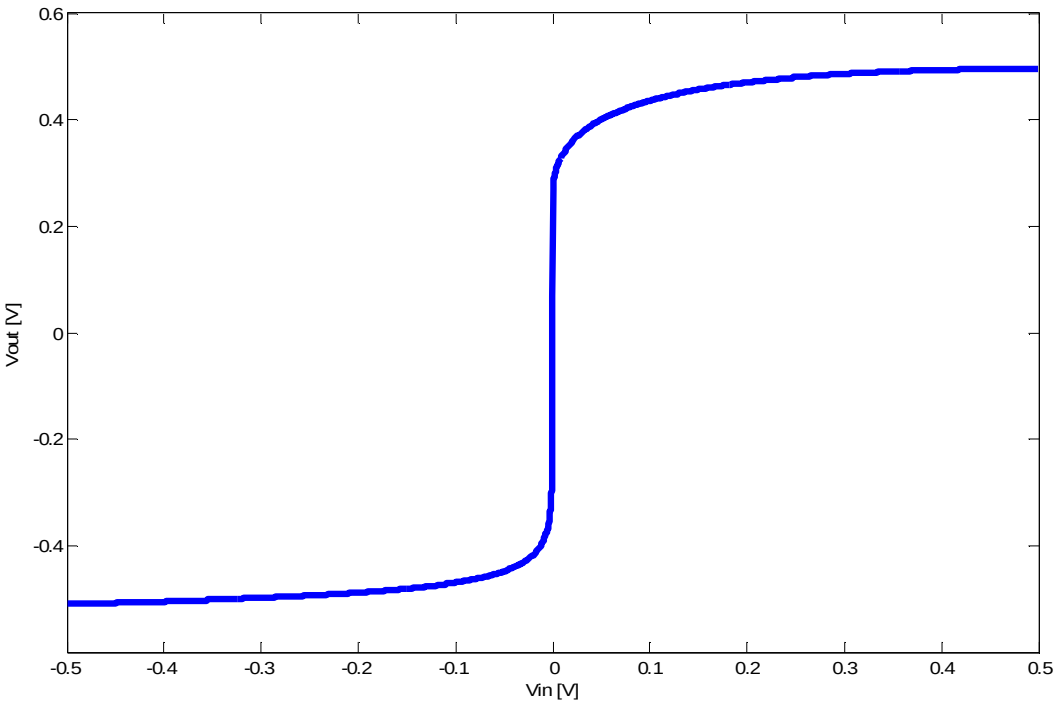

Figure 4.50. DC response of the operational amplifier

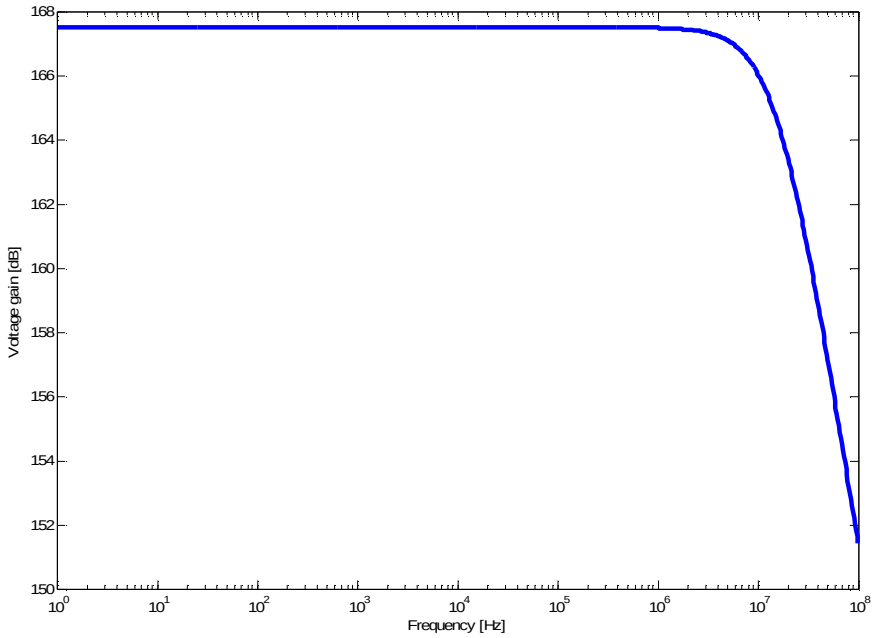

Figure 4.51. AC characteristics of the operational amplifier

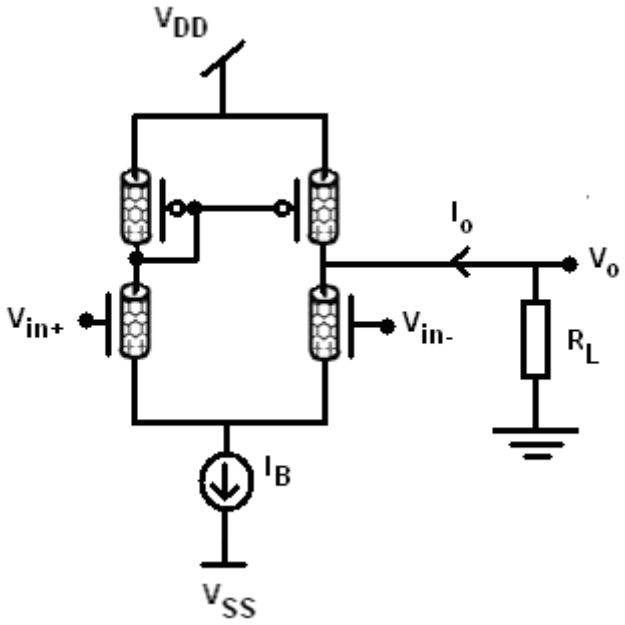

Figure 4.52. OTA circuit utilizing CNTFETs

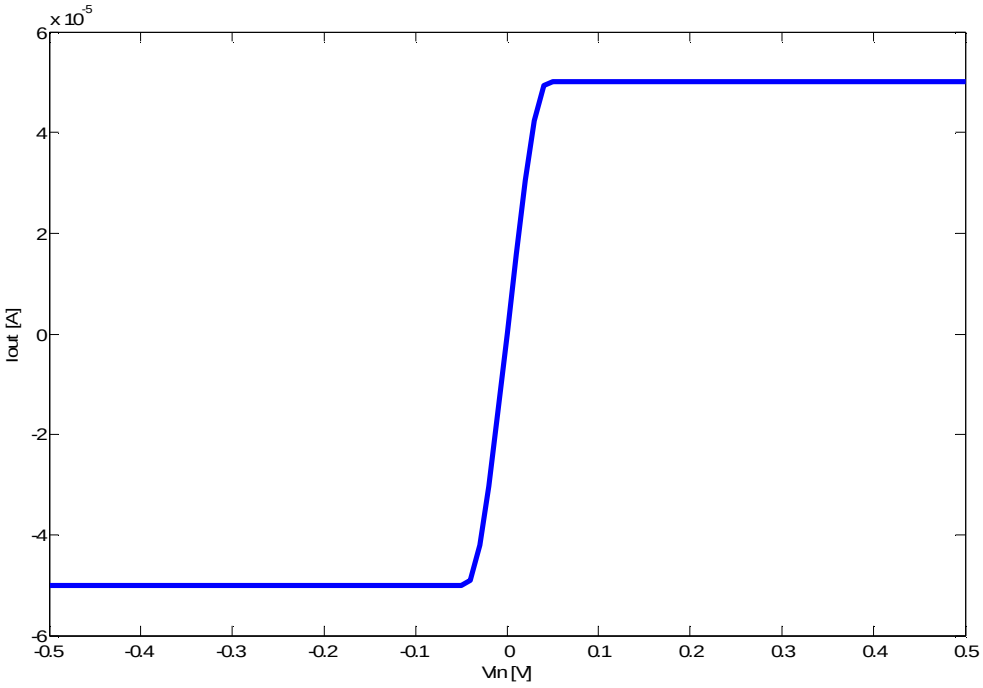

Figure 4.53. DC response of the OTA circuit using CNTFETs

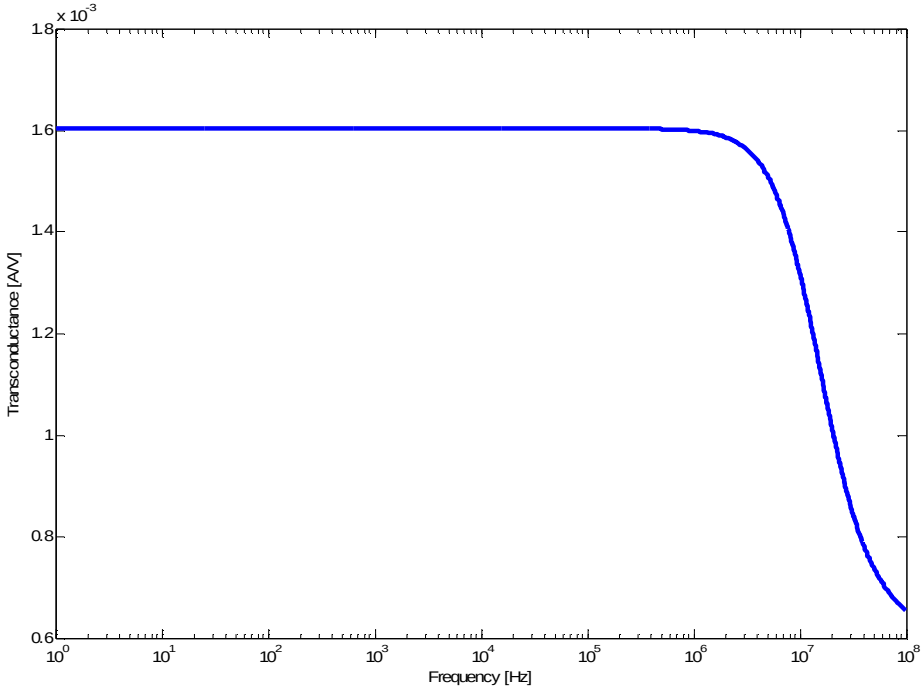

Figure 4.54. AC response of the OTA circuit using CNTFETs

DC transconductance of the OTA is found to be 1.63mA/V and the cut-off frequency is 21.2MHz. Output resistance is obtained as 808kΩ. Note that these sample circuits show the utilizability of the CNTFETs and the possibility of the simulation of the circuits using the presented self-consistent SPICE model.

4.7.5. Second Generation Current Conveyor Circuit Using CNTFETs

A basic CCII structure shown in Figure 4.55 is simulated using the presented CNTFET model. Voltage transfer and current transfer characteristics of the CCII are obtained in HSPICE and plotted in Figure 4.56 and Figure 4.57, respectively.

Supply voltages are taken as VDD=–VSS=0.5V and bias currents are $I_{B1}=I_{B2}=I_{B3}=100\mu A$. The output resistance of the Z-terminal is found to be 602kΩ while X terminal resistance is obtained as 736Ω. Frequency response of the CCII is also plotted in Figure 4.58.

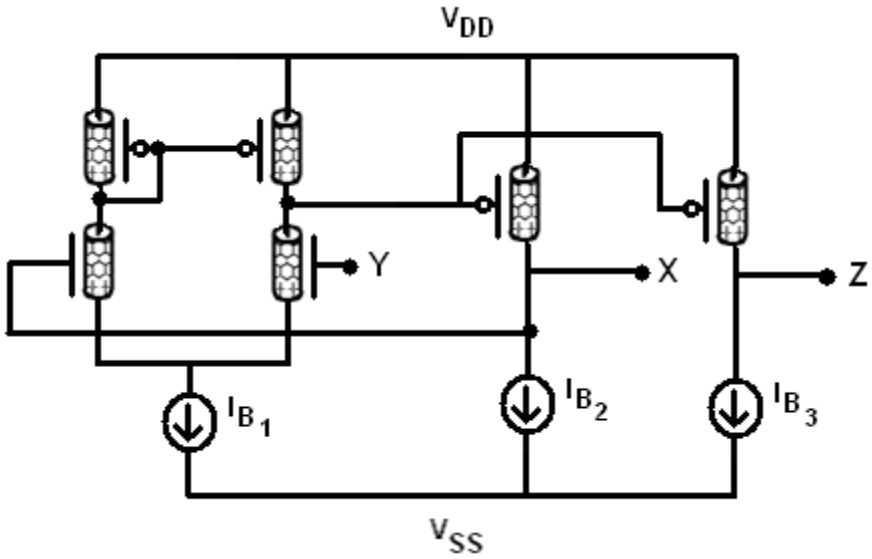

Figure 4.55. CCII+ circuit employing CNTFETs

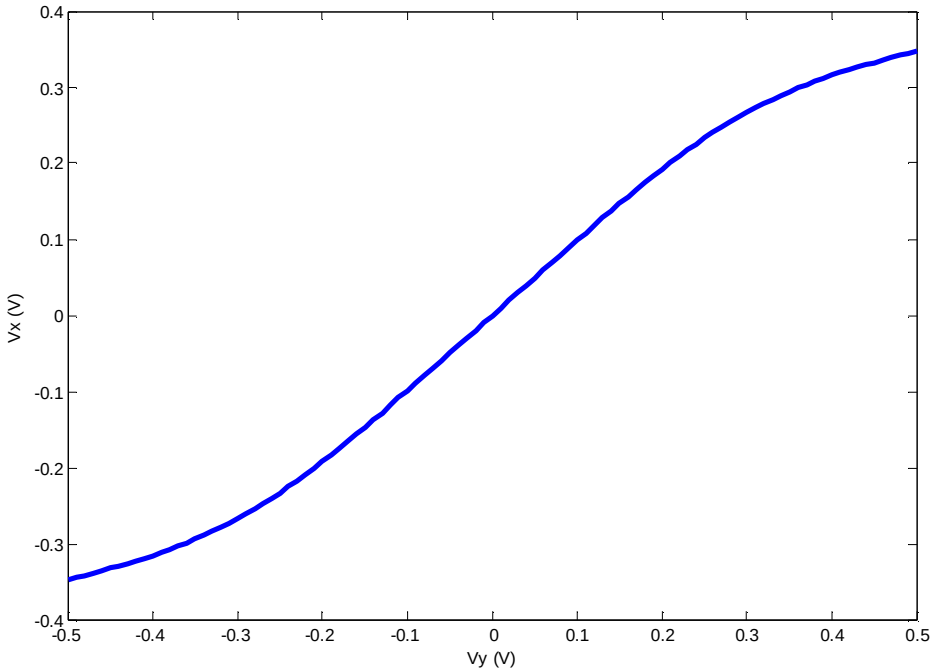

Figure 4.56. V_X-V_Y variation of the CCII using CNTFETs

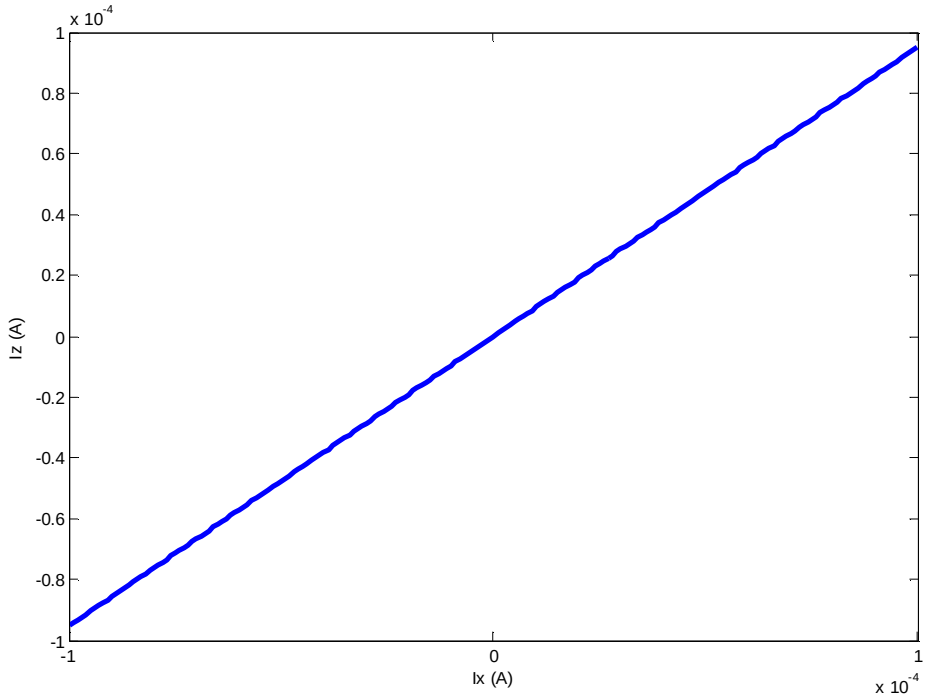

Figure 4.57. I_X-I_Z variation of the CCII using CNTFETs

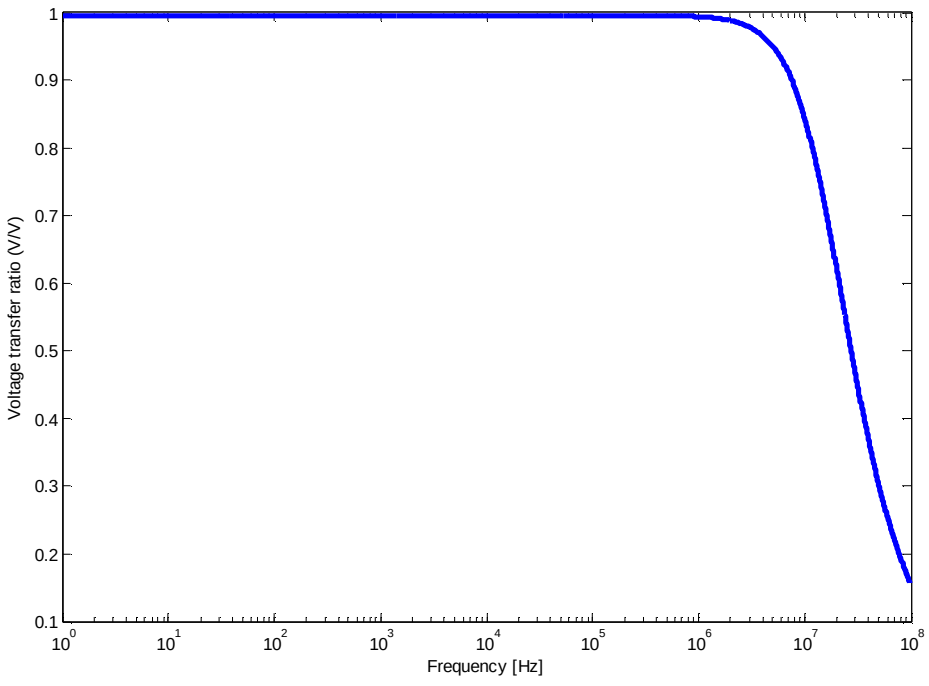

Figure 4.58. Frequency response of the voltage transfer ratio of the CCII circuit using CNTFETs

4.7.6. NOR Gate Using CNTFETs

The NOR gate shown in Figure 4.59 is simulated using the presented CNTFET model. V_{DD} is taken as 1V and the lengths of the CNTFETs are 10nm. Obtained transient characteristics is given in Figure 4.60. The delay of the gate is found to be 104ps.

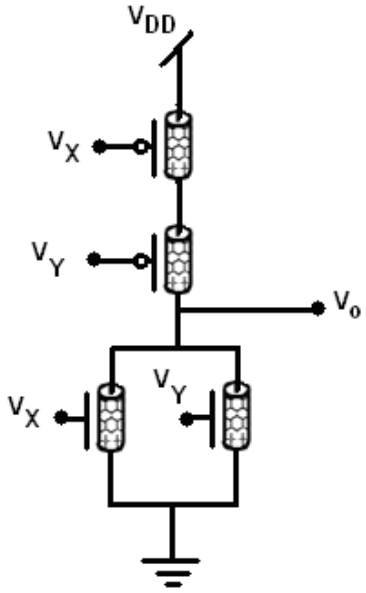

Figure 4.59. NOR gate using CNTFETs

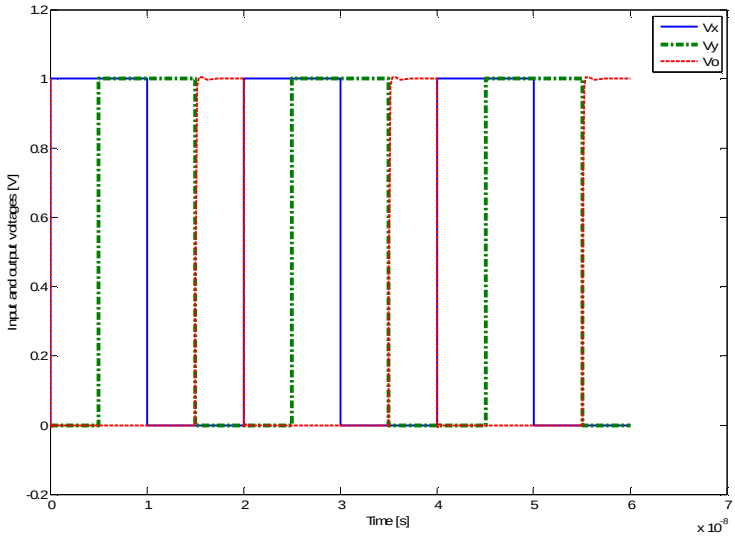

Figure 4.60. Transient simulation results of the NOR gate

4.7.7. NAND Gate Using CNTFETs

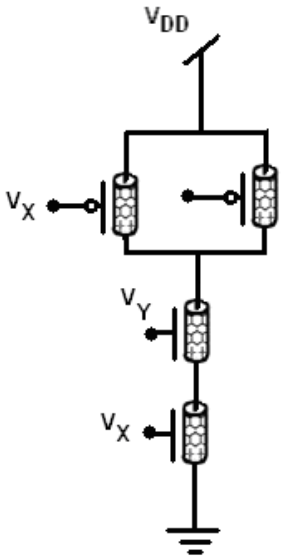

Figure 4.61. NAND gate with CNTFETs

The NAND gate shown in Figure 4.61 is also simulated in HSPICE Obtained transient characteristics is given in Figure 4.62. Gate delay is found as 112ps.

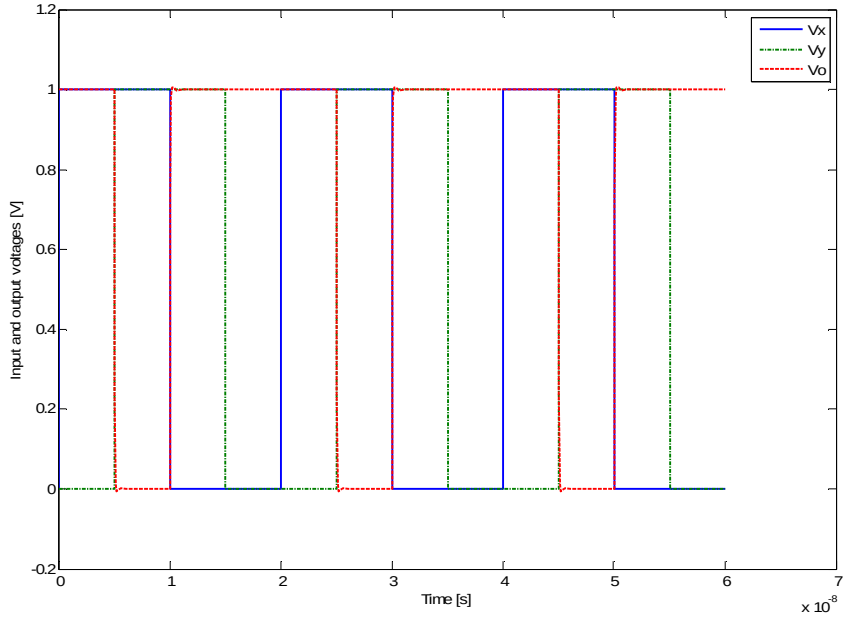

Figure 4.62. Transient response of the NAND gate

5. CONCLUSIONS

In this thesis, CNT interconnects and CNTFETs are accurately modelled and models suitable for use in circuit design and simulation tools are presented. The results can be summarized as follows.

a. Current saturation occurs in short metallic CNTs and this saturation is due to the lack of transmission channels above a certain applied voltage.
b. The nonlinear voltage-dependent resistance of metallic CNTs can be modelled by polynomial fitting functions which is suitable for use in circuit tools.
c. Artificial neural networks can also accurately model the nonlinear resistance of CNTs.
d. Current-voltage saturation of metallic CNTs are disadvantageous while used as interconnects. However, utilization of current saturation characteristics of metallic CNTs makes it possible to design novel compact nanoscale circuits.
e. A new method for the calculation of voltage-dependent capacitance of CNTs from DFT-NEGF simulation results is presented and applied on sample CNT sections.
f. An accurate transmission line model for CNT interconnects is proposed. The presented model includes voltage-dependent resistance and voltage-dependent capacitance. Delay of a sample CNT section is computed using the presented transmission line model and compared to the results in the literature. Comparison to the results obtained from electromagnetic approach verifies the accuracy of the calculated delay.
g. A CNTFET model suitable for use in SPICE environment is presented. The novelty of the proposed CNTFET model is the utilization of self-consistent channel charge calculation in SPICE. The comparison of the characteristics of the proposed model and the quantum mechanical simulator verifies the accuracy of the model.
h. Sample circuit simulations using the proposed CNTFET model are given in HSPICE to show the SPICE compatibility of the presented model

The contributions of this work to the literature are as follows.

i. Yamacli, S. and Avci, M., 2009. Simple and Accurate Model for Voltage-dependent Resistance of Metallic Carbon Nanotube Interconnects: An Ab Initio Study. Physics Letters A, 374, 297-304. (SCI journal paper)

ii. Yamacli, S. and Avci, M., 2010. Neural Network Modeling of Voltage-dependent Resistance of Metallic Carbon Nanotube Interconnects: An Ab Initio Study. Expert Systems with Applications, 37, 8014-8018. (SCI journal paper)

iii. Yamacli, S. and Avci, M., 2010. A Method for the Extraction of the Voltage-dependent Quantum Capacitance of Carbon Nanotubes Using Ab Initio Simulations. Physica Scripta, 82, 1-6. (SCI journal paper)

iv. Avci, M., Yamacli, S., 2010 An Improved Elmore Delay Model for VLSI Interconnects. Mathematical and Computer Modelling, 51, 908-914. (SCI journal paper)

v. Yamacli, S. and Avci, M., 2011. Accurate Voltage-Dependent Transmission Line Model for Metallic Carbon Nanotube Interconnects and the Delay Calculation. Journal of Electromagnetic Waves and Applications, 25, 553-563. (SCI journal paper)

vi. Yamacli, S. and Avci, M., 2010. Electronic Properties and Self Consistent Simulations of Carbon Nanotubes in Transistor Technology. In Transistors: Types, Materials and Applications, editor: Benjamin Fitzgerald, Nova Science Publishers, ISBN : 978-1-61668-908-7, USA. (Book chapter)

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