# OPTIMIZING DOHERTY POWER AMPLIFIER OUTPUT NETWORKS FOR MAXIMIZED BANDWIDTH

A DISSERTATION SUBMITTED TO
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ELECTRICAL AND ELECTRONICS ENGINEERING

By
Sinan Alemdar
June 2022

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We certify that we have read this dissertation and that in our opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

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# ABSTRACT

## OPTIMIZING DOHERTY POWER AMPLIFIER OUTPUT NETWORKS FOR MAXIMIZED BANDWIDTH

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A method is presented to optimize the combining network and the post matching network of a Doherty power amplifier for maximizing the bandwidth. For widely applicable results, RF power transistors are approximated in the large-signal regime using a simple analytical model with a few parameters. A definition of bandwidth of Doherty power amplifier is given, which involves gain and efficiency at full-power and 6 dB backoff. Different combining network topologies are compared in terms of this bandwidth definition. The element values are optimized using two factors, one to scale the combining node impedance and the other to scale the impedance seen by the transistors. For each optimized topology, explicit formulas are given resulting in the element values in terms of the optimized values and a few transistor parameters. The method presented also leads to a proper selection of the post-matching network.

*Keywords:* Doherty power amplifier, Doherty combining network, Doherty output network.

# ÖZET

# DOHERTY GÜÇ YÜKSELTECİ ÇIKIŞ BİRLEŞTİRME DEVRESİ OPTİMİZASYONU

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Doherty güç yükselteçlerinin bant genişliğini arttırmak için çıkış birleştirme devresi ve çıkış empedans eşleme devresi için bir optimizasyon metodu anlatılmaktadır. Önerilen metodun genel geçer olabilmesi için RF güç transistörünün yüksek güç bölgesi için parametrik analitik bir model kullanılmıştır. Optimizasyon, Doherty güç yükselteçleri için en yüksek çıkış gücünde ve 6 dB daha az çıkış gücünde kazanca ve verimliliğe dayanan bir bant genişliği tanımı kullanılarak yapılmıştır. Farklı çıkış birleştirme devre topolojileri birbirleri ile karşılaştırılmış ve bant genişlikleri bulunmuştur. Çıkış ve birleştirme devrelerindeki elemanlar iki ölçeklendirme parametresi ile optimize edilebilmektedir. Birinci ölçeklendirme parametresi çıkış birleştirme noktasındaki empedansı, ikinci ölçeklendirme parametresi transistörlerin gördüğü empedansı değiştirmektedir. Her optimize birleştirme topolojisi için devre elemanlarının formülleri ve transistör parametreleri paylaşılmıştır. Ayrıca çıkış empedans eşleme devresi için topoloji seçimi ve devre elemanlarının formülleri paylaşılmıştır.

*Anahtar sözcükler*: Doherty güç yükselteci, Doherty birleştirme devresi, Doherty çıkış devresi.

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I would like to extend my thanks to the members of my thesis monitoring committee, Prof. Fatih Ömer İlday and Prof. Barış Bayram for their support and Prof. Şimşek Demir and Asst. Prof. Erdinç Tatar for taking part in my thesis jury.

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# Chapter 1

# Introduction

Next-generation wireless networks impose tight requirements on transceiver front ends. Higher data rates and larger capacities introduce new modulation schemes using wider bandwidths. The power amplifiers employed on the transmitters should work with complex modulation schemes using a high peak-to-average power ratio (PAPR) and wide bandwidth while maintaining high efficiency [1, 2]. Such signals cause power amplifiers to operate with a reduced efficiency [3].

There are several power amplifier architectures aimed at providing high efficiency under large PAPR signals, mainly envelope tracking, outphasing, and the Doherty Power Amplifier (DPA). Doherty power amplifiers (DPA), first proposed by Doherty [4] and well discussed in [5] provide an efficient amplification for signals having high PAPR. The DPA features high efficiency across a large power range allowing high efficiency with large PAPR signals. The basic principle behind the DPA depends on two power amplifiers actively modulating each other while their outputs are combined and delivered to the load.

Although Doherty power amplifiers address the efficiency challenge of large PAPR signals, the classic approach suffers from intrinsic bandwidth limitations. There has been a lot of work on increasing the efficiency of the DPA or increasing the frequency range where the DPA is efficient. Efficiency optimizations can be

achieved in narrowband applications, but in broadband applications, it is not trivial to achieve similar performance. When it comes to building a wide-band DPA, several limitation factors are summarized and categorized in [1]. Frequency analysis of DPA is extensively investigated in [6] exploiting the bottleneck in the limitation of the impedance inverter's frequency response. By modifying the impedance transformation ratio of the transmission lines, the impedance seen by the carrier amplifier has less variation with frequency and the efficiency bandwidth increases to an octave [7]. There exist notable studies in the literature targeting the compensation of transistor parasitics or the impedance inverter [8, 9, 10]. Alternatively, digitally controlled dual-RF input DPAs are also another approach to increase efficiency bandwidth compared to single input DPAs [11].

In this thesis, we determine the topology and element values of the optimized output network of a DPA, to maximize the bandwidth. Instead of using specific and complex vendor models of transistors, we use a simple generic and robust transistor model to make the results more general. In Section 2, we analyze the Doherty Power Amplifier analytically and also introduce our analytical transistor model that is used in approximating the large signal behavior of any RF power amplifier including DPA. Afterward, we present the frequency analysis of a conventional DPA using our large signal transistor model. In Section 3, we divide the output network into two parts: a combining network and a post-matching network. We present different combining network topologies and introduce two factors for bandwidth optimization. We introduce the definition of bandwidth of the DPA dependent both on gain and efficiency at full-power and 6 dB backoff. There, we provide explicit formulas for the bandwidth maximized values of combining network element values that are dependent on the optimized factors and the transistor parameters [12]. The post-matching network that does not cause a bandwidth reduction can be selected subsequently. We also share examples to demonstrate the use of the method where all element values are calculated using the presented formulas. The resultant output networks are also analyzed using a harmonic balance simulator using vendor models of transistors to show that the results are close enough. The values can be used as a good starting point for further optimization in a harmonic balance simulation with more accurate

transistor models. Lastly, we present experimental results verifying the validity of the method.

# Chapter 2

# Analysis of Doherty Power Amplifier

Doherty power amplifiers (DPA) offer improved efficiency when the output power is backed off from its maximum level. They are typically used for communications applications where complex signals not having a constant amplitude need to be transmitted. These signals have a power distribution and are usually denoted by a metric called the peak-to-average power ratio (PAPR). As mobile services evolve, more complex modulation schemes are introduced to support increased data ratings, which requires higher bandwidth and higher peak-to-average power ratios shown in Fig. 2.1 [13].

Doherty power amplifiers consist of two (and recently more) amplifiers. One of the amplifiers is called the "carrier" amplifier and the second or others are called the "peaking" or "auxiliary" amplifier. Carrier and peaking amplifiers are biased differently in many different designs. The carrier amplifier is usually a class-AB or class-B biased amplifier because it is designed to conduct the input signal at all times. On the contrary, the peaking amplifier is usually biased class-C where it is normally turned off most of the time and only conducts when the signal level is higher for a small amount of time which are called peaks as shown in Fig. 2.2.[14]

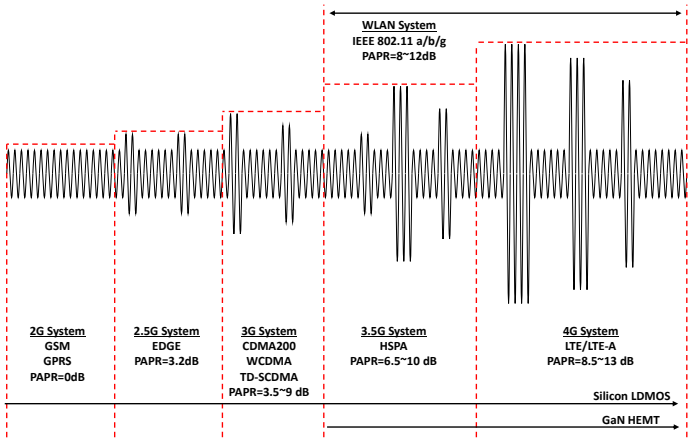


Figure 2.1: The technology development of the RF PAs with the increased PAPR of signal for wireless communication standards evolution.

Up to a certain power level which is usually 6 dB less than the maximum achievable power, only the carrier amplifier conducts the signal to the output while the peaking amplifier is off because the signal power is not enough to turn on the class-C biased transistor. This region is called the back-off region. In the conventional DPA and many DPA designs, a 6 dB back-off from the maximum power is chosen before the peaking amplifier starts to conduct. Compared to conventional amplifiers, Doherty Power Amplifiers offer improved efficiency at backed-off power levels[15].

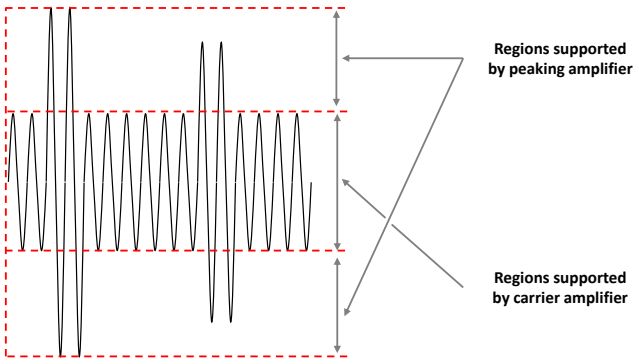


Figure 2.2: Modulated signal example and how it is handled through the Doherty Power Amplifier

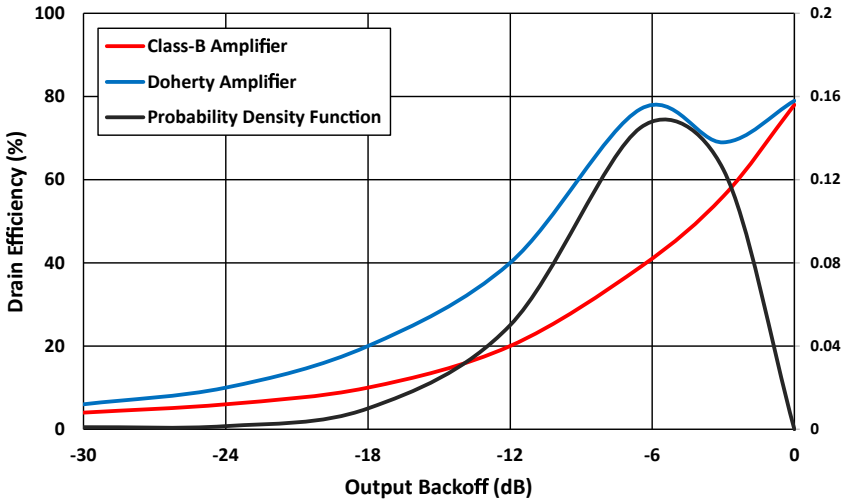


Figure 2.3: Efficiency of class B Amplifier and Doherty Power Amplifier versus output power backoff imposed over a typical power distribution of a 6 dB PAPR modulated signal.

The Doherty power amplifier offers improved efficiency at lower power levels thanks to the concept called active load modulation. Until the 6 dB backoff point, the carrier amplifier sees an impedance of $2R_{opt}$ where $Ropt$ is the optimum impedance for the maximum output power meanwhile the peaking amplifier is off. Between the 6 dB backoff point and the maximum output power, both amplifiers conduct and actively modulate each other so that the load seen by the two amplifiers is $R_{opt}$. The class-C biased peaking amplifier starts to conduct current and actively modulates the output combining node, thus changing the impedances seen by both carrier and peaking amplifiers. The load modulation concept is a complex operation and will be analyzed in detail.

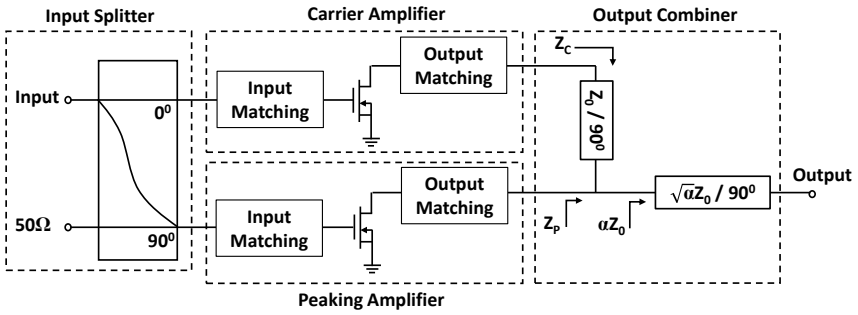


Figure 2.4: Doherty Power Amplifier Schematic

The Doherty output combiner consists of a quarter-wave impedance inverter between the carrier amplifier to the combining node and the post-matching network to convert the impedance to the output termination impedance. The Doherty combining node's impedance is adjusted to $R_{opt}/2$ by the post-matching network. The quarter-wave inverter of a characteristic impedance *Ropt* transforms this impedance into $2Ropt$ in the back-off region. When the input signal is enough to turn on the peaking amplifier, both amplifiers conduct current and each branch sees $R_{opt}$.

The additional phase at the output of the carrier amplifier needs to be compensated at the input so that when both amplifiers conduct, signals are combined in phase. At the input of the DPA, a Wilkinson power divider followed by a quarter-wave transmission line or a branch-line coupler is usually preferred. Due to the $90^o$ phase difference at the input, reflections from two amplifiers cancel out and a better return loss is achieved, similar to the case of balanced amplifiers.

## 2.1 Doherty Power Amplifier Solution using ABCD Parameters

The conventional DPA can be considered as shown in Fig.2.5. To complete an accurate analysis; we model drain-to-source capacitance, package inductance, and bias line inductance. After these components matching circuits or quarter-wave impedance transformers may also be used.

For analysis, the structures at the output of the transistors could be analyzed as 2-port networks. We have selected ABCD parameters because it is easy to cascade series or shunt elements, and the combined network could be calculated with standard matrix multiplication.

Referring to Fig. 2.5, the output loads of transistors including their parasitic capacitances and matching networks can be represented as a function of $\omega$ with ABCD parameters that have complex entries. The combining node is terminated

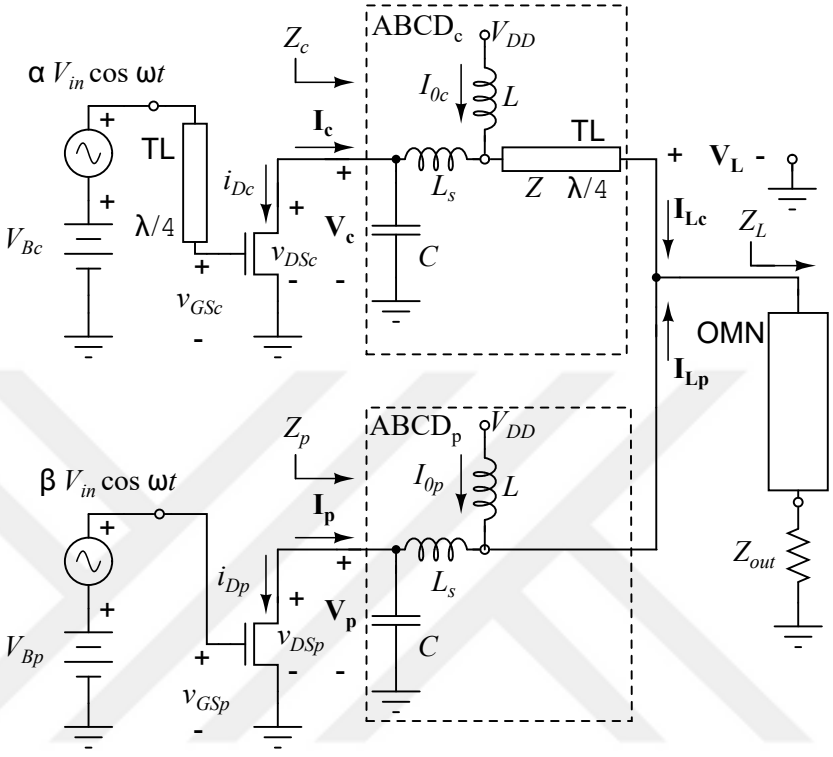


Figure 2.5: Conventional Doherty Power Amplifier Schematic

with the impedance $Z_L$ having a voltage phasor of $\mathbf{V_L}$ at $\omega$.

Let the voltage and current phasors of the carrier and peak transistors at $\omega$ be denoted by $\mathbf{V_c}$, $\mathbf{I_c}$, $\mathbf{V_p}$ and $\mathbf{I_p}$, respectively. From ABCD matrices shown in Fig. 2.5, we have:

$$\mathbf{V_c} = A_c\mathbf{V_L} + B_c\mathbf{I_{Lm}} \tag{2.1}$$

$$\mathbf{I_c} = C_c\mathbf{V_L} + D_c\mathbf{I_{Lm}} \tag{2.2}$$

$$\mathbf{V_p} = A_p\mathbf{V_L} + B_p\mathbf{I_{Lp}} \tag{2.3}$$

$$\mathbf{I_p} = C_p\mathbf{V_L} + D_p\mathbf{I_{Lp}} \tag{2.4}$$

The voltage at the combining node is given by

$$\mathbf{V_L} = (\mathbf{I_{Lc}} + \mathbf{I_{Lp}})Z_L \tag{2.5}$$

Substituting Eq. 2.5 in Eqs. 2.2, 2.4 and solving for $\mathbf{I_{Lm}}$ and $\mathbf{I_{Lp}}$, we rewrite Eq. 2.5 as

$$\mathbf{V_L} = Z_L \frac{D_p \mathbf{I_c} + D_c \mathbf{I_p}}{D_c D_p + (C_c D_p + C_p D_c) Z_L} \tag{2.6}$$

Substituting $\mathbf{I_{Lc}}$, $\mathbf{I_{Lp}}$ and Eq. 2.6 into Eqs. 2.1 and 2.3, we get

$$\mathbf{V_c} = \frac{B_c D_p + (A_c D_p + B_c C_p) Z_L}{D_c D_p + (C_c D_p + C_p D_c) Z_L} \mathbf{I_c} + \frac{(A_c D_c - B_c C_c) Z_L}{D_c D_p + (C_c D_p + C_p D_c) Z_L} \mathbf{I_p} \triangleq Z_c \mathbf{I_c} \tag{2.7}$$

$$\mathbf{V_p} = \frac{B_p D_c + (A_p D_c + B_p C_c) Z_L}{D_c D_p + (C_c D_p + C_p D_c) Z_L} \mathbf{I_p} + \frac{(A_p D_p - B_p C_p) Z_L}{D_c D_p + (C_c D_p + C_p D_c) Z_L} \mathbf{I_c} \triangleq Z_p \mathbf{I_p} \tag{2.8}$$

where $Z_c$ and $Z_p$ are defined as the impedances seen by each transistor.

Although transistors could be simply modeled as current sources in a small signal, large signal behavior requires special attention. Like any other power amplifier, Doherty power amplifiers also depend on transistors operating close to their power rating. The voltage and current behavior of the transistors close to their compression regime need to be modeled and included in the analysis as well.

## 2.2 Large-signal intrinsic RF transistor model

The drain current of the RF transistor depends linearly on the gate voltage, $v_{GS}$, minus the threshold voltage, $V_T$, through the transconductance of $G_m$. We write the instantaneous intrinsic drain current, $i_D$, in terms of the drain-to-source

voltage, $v_{DS}$, as

$$i_D = \begin{cases} G_m(v_{GS} - V_T)\, f(v_{DS}) & \text{if } v_{GS} \geq V_T \\ 0 & \text{otherwise} \end{cases} \tag{2.9}$$

with

$$f(v_{DS}) = 1 - \frac{1}{2}\left(1 - \frac{v_{DS}}{V_{DD}}\right)^{N_e} - \frac{1}{2}\left(1 - \frac{v_{DS}}{V_{DD}}\right)^{N_e+1} \tag{2.10}$$

where $f()$ is continuous function for all $v_{DS}$ values and $N_e$ is an even integer showing the order of knee function approximation. The resultant $I-V$ characteristics of our model is shown in Fig. 2.6 for $N_e$=14. For GaN transistors, $8 \leq N_e \leq 16$ is a good representation, while $N_e \geq 40$ would be accurate for GaAs transistors.

The knee voltage, $V_K$, is defined as the point where the slope of $f(v_{DS})$ with respect to $v_{DS}/V_{DD}$ is unity. For a given $V_K$ and $V_{DD}$, the most appropriate even integer, $N_e$, can be determined from the solution of

$$N_e\left(1 - \frac{V_K}{V_{DD}}\right)^{N_e-1} + (N_e+1)\left(1 - \frac{V_K}{V_{DD}}\right)^{N_e} = 2 \tag{2.11}$$

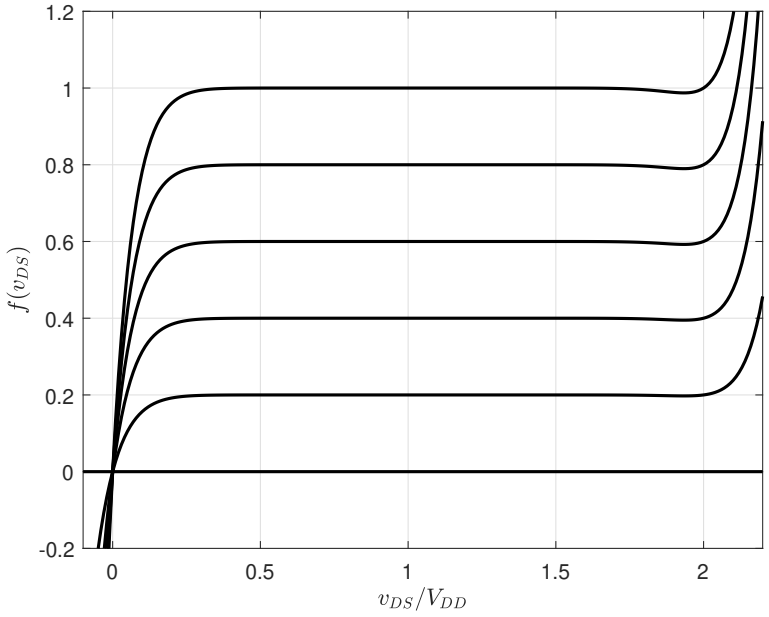


Figure 2.6: $I$-$V$ characteristics of our model with $N_e$=14.

This function is an improved version of that introduced recently [16]. Unlike the model there, our transistor characteristics are never in the fourth quadrant and hence it always remains a passive device. Therefore, the proposed model in this study is usable for transistors under any class of operation that experiences complex or negative real-part loads. This is especially important for DPA analysis since the individual transistors of a DPA may experience very high Q or even negative real-part loads under certain conditions. It is found that harmonic balance simulation of DPA using vendor models of transistors causes convergence problems under certain combining network combinations making an optimization very difficult.

Fig. 2.7 shows intrinsic drain current comparison of for this transistor with different transistor models for a negative-real part capacitive load. Our improved model is a better approximation than the existing [16] analytic model.

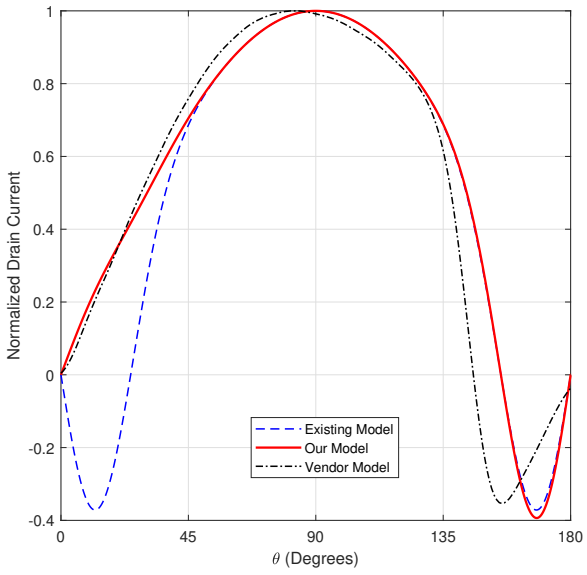


Figure 2.7: Intrinsic current waveforms of the existing and improved models in comparison to complex vendor model of Cree CGH40010 transistor for operation in Class-B with a load of $-8 - j35\ \Omega$. ($N_e$=14).

### 2.2.1 Analysis of a simple RF power amplifier using the model

The analysis method can be explained using an RF power amplifier shown in Fig. 2.8. The transistor is assumed to have a voltage-independent drain capacitance of $C$ and a series package inductance of $L_s$. The amplifier operates with a supply voltage of $V_{DD}$.

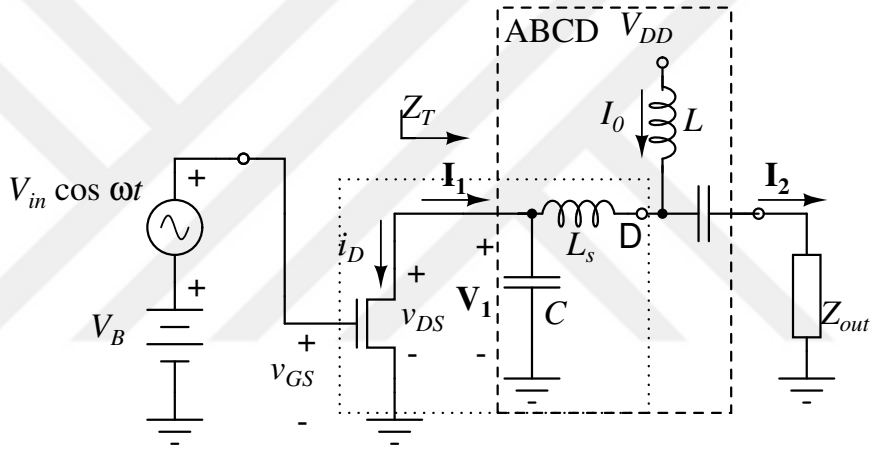


Figure 2.8: Schematic of an RF power amplifier

The transistor input is excited with a sinusoidal signal at $\omega$ shifted with a bias voltage $V_B$. To simplify the analysis, we assume that all harmonic voltages are shorted at the intrinsic transistor drain. This is a good approximation if the package inductance $L_s$ is small and the inductance, $L$, forms a resonant circuit at the fundamental frequency that shortens the harmonics. Therefore, it is assumed that the drain voltage is purely sinusoidal, and we can write $v_{DS}$ as:

$$v_{DS}(\theta) = V_{DD} + V_1 \cos(\theta + \phi) \tag{2.12}$$

An input voltage of $v_{GS} = V_B + V_{in} \cos\theta$ results in a drain current of

$$i_D = A(\theta) \left[ 1 - \frac{1}{2} \left( \frac{V_1}{V_{DD}} \right)^{N_e} \cos^{N_e}(\theta + \phi) + \frac{1}{2} \left( \frac{V_1}{V_{DD}} \right)^{N_e+1} \cos^{N_e+1}(\theta + \phi) \right] \tag{2.13}$$

with

$$A(\theta) = \begin{cases} G_m(V_{in}\cos\theta + V_B - V_T) & \text{if } \cos\theta > -\frac{V_B - V_T}{V_{in}} \\ 0 & \text{otherwise} \end{cases} \tag{2.14}$$

Following the approach of [16], we expand (2.13) as the product of an infinite series with a finite series. Hence one can obtain the DC current, $I_0$, and the fundamental current, $\mathbf{I_1}$ (in the phasor form), both as a finite series. Note that $I_0$ and $\mathbf{I_1}$ depend on $N_e$, $V_{in}$, $V_B - V_T$ and the phasor $\mathbf{V_1} = V_1 e^{j\phi}$, nonlinearly through the functions $f_1$ and $f_2$ defined as

$$I_0 = f_1(N, V_{in}, V_B - V_T, \mathbf{V_1}) = A_0 k_0 + \frac{1}{2}\sum_{n=1}^{N_e+1} A_n k_{n,R} \tag{2.15}$$

$$\mathbf{I_1} = f_2(N, V_{in}, V_B - V_T, \mathbf{V_1}) = A_1 k_0 + \frac{1}{2}A_0 k_{1,R} + \frac{1}{2}\sum_{n=1}^{N_e+1}[(A_{n-1} + A_{n+1})k_{n,R} + j(A_{n-1} - A_{n+1})k_{n,Q})] \tag{2.16}$$

where $A_n$, $k_{n,R}$ and $k_{n,Q}$ are defined in Appendix A. We should also satisfy $\mathbf{V_1} = Z_T\mathbf{I_1}$ or

$$\mathbf{V_1} = Z_T f_2(N, V_{in}, V_B - V_T, \mathbf{V_1}) \tag{2.17}$$

where $Z_T = \mathbf{V_1}/\mathbf{I_1}$ is the drain impedance seen by the transistor. This value is easily found as a function of $\omega$ in terms of $Z_{out}$ and ABDC parameters of the network composed of $C$, $L_s$ and $L$.

$$Z_T = \frac{AZ_{out} + B}{CZ_{out} + D} \tag{2.18}$$

With a given $\omega$, $N$, $V_{DD}$, $V_{in}$ and $V_B - V_T$, we solve[1] the nonlinear equation of (2.17) to find $\mathbf{V_1}$. Once the complex valued quantity, $\mathbf{V_1}$, is found, we can determine $I_0$ from (2.15), and the output RF power, $P_{out}$, using

$$P_{out} = \frac{1}{2}\mathcal{R}e\{Z_{out}\}|\mathbf{I_2}|^2 \text{ with } \mathbf{I_2} = \frac{\mathbf{V_1}}{AZ_{out} + B} \tag{2.19}$$

The efficiency is determined from

$$\eta = \frac{P_{out}}{I_0 V_{DD}} \tag{2.20}$$

[1]We use *fsolve* function of MATLAB. All MATLAB codes used in this thesis are available in the Appendix C.

As the active device we choose Cree CGH40010 GaN transistor to build a power amplifier with $V_{DD}$=28 V. We model the transistor using the parameters $G_m$=0.66 A/V, $V_T$=−3.3 V, $C$=1.84 pF and $L_s$=0.26 nH, and $N_e$=14. Here, $G_m$ and $V_T$ are determined from the transistor's $I$-$V$ characteristics. $C$ and $L_s$ are estimated from the vendor specified optimal load impedance. $N_e$ is found from the knee voltage using (2.11).

We first bias the transistor in Class-B ($V_B$=$V_T$) and choose $L$=$\infty$. Fig. 2.9 shows the calculated power and efficiency load-pull contours using our model at 2.5 GHz as $Z_{out}$ is varied. The full-power load-pull contours are generated with an input drive level to reach the rated power at the corresponding optimum load. At the same load, we reduce the input power to reach a 6 dB lower output power to define the 6 dB back-off (BO) level. Then the load-pull contours are regenerated at this BO level.

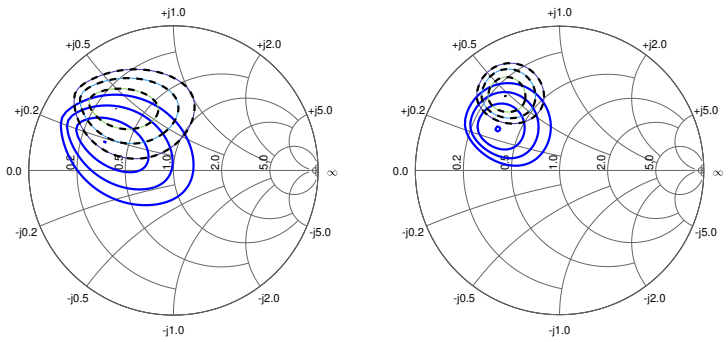


Figure 2.9: Power (left, in 1 dB steps) and efficiency (right, in 5% steps) load-pull contours of Class-B transistor at 2.5 GHz on 50 Ω Smith charts at two-input levels: full-power (solid) and 6 dB BO (dashed).

We repeated the load-pull simulation (Fig. 2.10) for the same amplifier with transistor biased as Class-C. It is excited with twice the input RF voltage to obtain the same output power with a properly selected gate bias voltage.

The maximum power is achieved nearly at the same impedance value as the Class-B amplifier. As BO is increased the optimal values move towards higher impedances more rapidly compared to Class-B amplifier.

To verify the accuracy of our model, we present a comparison of our results

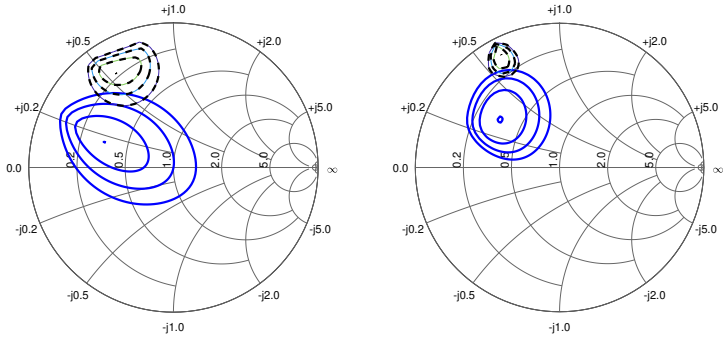


Figure 2.10: Fig. 2.9 repeated for Class C transistor at full-power (solid) and at 5 dB BO (dashed) rather than at 6 dB BO.

for Class-B and Class-C amplifiers with harmonic balance simulation[2] at 2.5 GHz using vendor supplied nonlinear model in Table 2.1. The results of our model are reasonably close to the results of a more accurate vendor model.

| | Harmonic Balance | | | Our Model | | |
|---|---|---|---|---|---|---|
| | $Z_{out}$ ($\Omega$) | $P_{out}$ (dBm) | $\eta$ | $Z_{out}$ ($\Omega$) | $P_{out}$ (dBm) | $\eta$ |
| CGH40010 Class-B at 2.5 GHz ($V_{Bc}$=−3.3 V) | | | | | | |
| Maximum Power | | | | | | |
| Full Power | 16 + j12 | 40.8 | 66 | 16.9+j8.9 | 40.6 | 67 |
| 6 dB Back-off | 16 + j19 | 36.8 | 61 | 15.9+j20.2 | 37.6 | 68 |
| Maximum Efficiency | | | | | | |
| Full Power | 16 + j18 | 40.2 | 71 | 17.3+j14 | 40.1 | 72 |
| 6 dB Back-off | 14 + j22 | 36.1 | 64 | 13.6+j23.4 | 37.2 | 72 |
| CGH40010 Class-C at 2.5 GHz ($V_{Bp}$=−5.6 V) | | | | | | |
| Maximum Power | | | | | | |
| Full Power | 14 + j13 | 41 | 72 | 16.8+j7.9 | 40.6 | 76 |
| Maximum Efficiency | | | | | | |
| Full Power | 16 + j19 | 40.4 | 80 | 16.9+j15.3 | 39.7 | 81 |

Table 2.1: Comparison of harmonic balance and our model for Class-B and Class-C amplifiers at full-power (FP) and 6 dB output BO.

Table 2.2 lists our model's optimal load impedance, $Z_{opt}$, defined at the drain pin (D in Fig. 2) of the transistor package for different frequencies. With a suitable value of shunt inductance ($L$ of Fig. 2.8), it is possible to move the center of the

[2]ADS, https://www.keysight.com

load-pull contours to the real axis to find the optimal load resistance, $R_{opt}$, which is also defined at the drain pin of the transistor. At low frequencies, $R_{opt}$ is equal to the optimal load resistance (26.6 Ω) of the intrinsic transistor, since the effects of the drain capacitance, $C$ and the package inductance, $L_s$, are negligible.

| $f_0$ (GHz) | $Z_{opt}$ (Ω) | $L$ (nH) | $R_{opt}$ (Ω) |
|---|---|---|---|
| $\ll 1.0$ | 26.6 | $\gg$15 | 26.6 |
| 1.0 | 24.5+j5.75 | 15 | 25.9 |
| 1.5 | 21.8+j6.52 | 6.0 | 24.5 |
| 2.0 | 18.9+j8.47 | 3.3 | 23.0 |
| 2.5 | 16.9+j8.87 | 2.05 | 21.1 |
| 3.0 | 14.3+j7.86 | 1.35 | 18.7 |
| 3.5 | 12.3+j6.95 | 0.935 | 16.4 |

Table 2.2: Optimal load impedance ($Z_{opt}$), and load resistance ($R_{opt}$, used with a shunt tuning inductor, $L$) for CGH40010 GaN transistor at full-power.

Note that this simple transistor model can be scaled by a factor $\xi$ to wider gate width transistors of the same family: For a transistor with $\xi$ times gate width[3], the parameters above become $\xi G_m$, $\xi C$, $L_s/\xi$, $L/\xi$, $R_{opt}/\xi$, $Z_{out}/\xi$, while $V_T$ and $\eta$ remain unchanged. Therefore, the load-pull contours of Fig. 3 and 4 are applicable if the reference impedance of the Smith chart is set to $(50/\xi)$ Ω. For example, for CGH40025 and CGH40045 power transistors, we need to set $\xi = 2.5$ and 4.5, respectively.

## 2.3 DPA Analysis with Large Signal RF transistor model

In the case of Doherty power amplifier, we can write individual currents and voltages of each amplifier $\mathbf{I_c}$ and $\mathbf{I_p}$ as the fundamental component of clipped cosine waves:

$$\mathbf{I_c} = f_2(N, \alpha V_{in}, V_{Bc} - V_T, \mathbf{V_c}) \tag{2.21}$$

[3]The number of drain bond wires and the drain capacitance is nearly proportional to the gate width.

$$\mathbf{I_p} = f_2(N, \beta V_{in}, V_{Bp} - V_T, \mathbf{V_p}) \tag{2.22}$$

Substituting Eqs. 2.21 and 2.22 into Eqs. 2.7 and 2.8, we get two nonlinear equations with two unknowns: $\mathbf{V_c}$ and $\mathbf{V_p}$. These equations can be solved simultaneously to find the unknown values.

We can then proceed to find the supply currents of the carrier ($I_{0c}$) and peaking ($I_{0p}$) amplifiers from

$$I_{0c} = f_1(N, \alpha V_{in}, V_{Bc} - V_T, \mathbf{V_c}) \tag{2.23}$$

$$I_{0p} = f_1(N, \beta V_{in}, V_{Bp} - V_T, \mathbf{V_p}) \tag{2.24}$$

At the center frequency, the carrier and the peaking amplifiers' ABCD matrices would look like Eqs. 2.25 and 2.26 since the transistor parasitics $C, L_s$ and the bias feed $L$ cancel out.

$$ABCD_c = \begin{bmatrix} A_c & B_c \\ C_c & D_c \end{bmatrix} = ABCD_{TL} = \begin{bmatrix} cos90^o & jZsin90^o \\ j/Zsin90^o & cos90^o \end{bmatrix} = \begin{bmatrix} 0 & jZ \\ j/Z & 0 \end{bmatrix} \tag{2.25}$$

$$ABCD_p = \begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{2.26}$$

On the other hand, the input drive levels for the carrier and the peaking transistors need to be adjusted as well. The main reason is the gain difference between the class-B or class-AB biased carrier amplifier would have 6 dB more gain than the class-C biased peaking amplifier. Due to this, the real implementation would require an unequal power division at the input. Referring to the simplified schematic Fig. 2.4, we have defined two coefficients $\alpha = 1/\sqrt{(}5)$ and $\beta = 2/\sqrt{(}5)$ to distribute the input voltage into the carrier and the peaking amplifier.

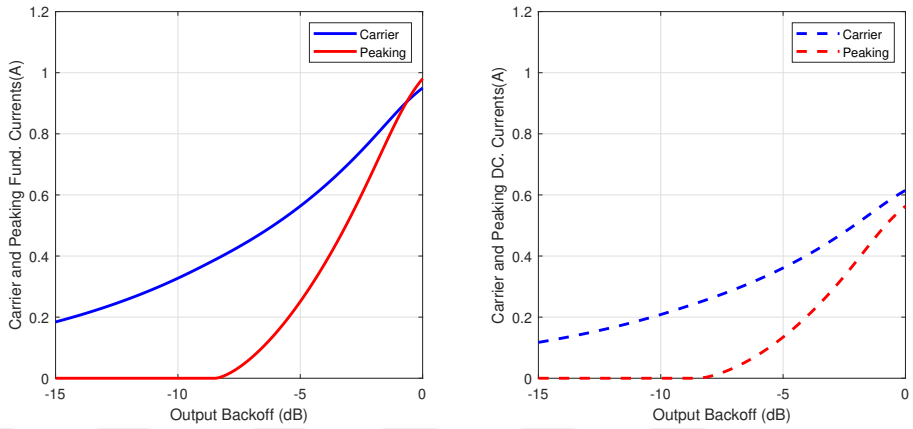


Figure 2.11: Currents generated for CGH40010 10W GaN transistor at the fundamental RF frequency (left) and at the DC (right) for the carrier(blue) and peaking(red) amplifiers as a function of back off from the full power

Fig. 2.11 shows how the fundamental RF currents and DC currents would scale using CGH40100 transistor parameters, a typical 10W GaN transistor. Similarly, it is possible to derive the impedances seen from the carrier and the peaking transistors $Z_c$ and $Z_p$ as stated in Eqs. 2.7 and 2.8 as shown in Fig. 2.12.

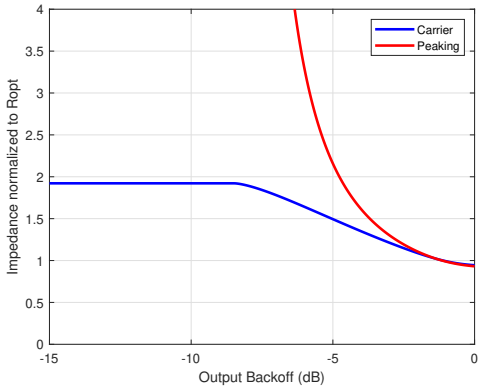


Figure 2.12: The impedance seen at the fundamental RF frequency for the carrier transistor(blue) and the peaking transistor(red) generated for CGH40010 10W GaN transistor as a function of back off from the full power

The phasor at the combining node, $\mathbf{V_L}$, is found using Eqs. 2.6, 2.21 and 2.22. Hence, the output power is written as

$$P_{out} = \frac{1}{2}\mathcal{R}e\left\{\frac{|\mathbf{V_L}|^2}{Z_L}\right\} \tag{2.27}$$

and the efficiency can be found from

$$\eta = \frac{P_{out}}{V_{DD}(I_{0c} + I_{0p})} \tag{2.28}$$

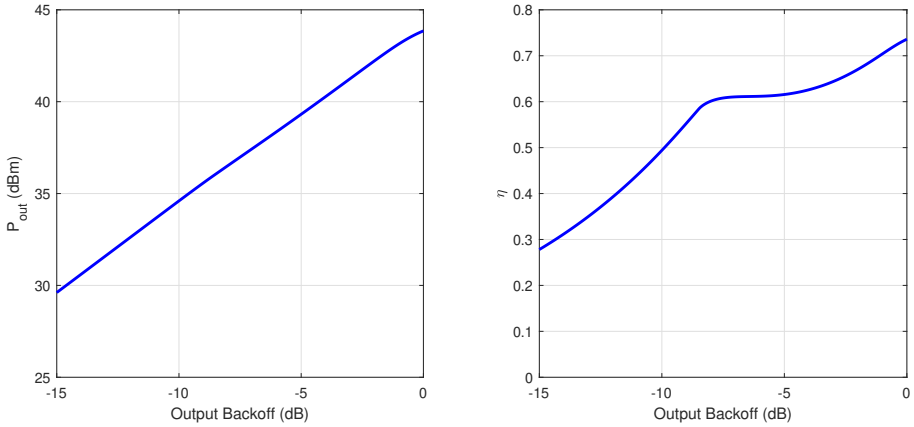


Figure 2.13: Output Power(left) and Efficiency(right) generated for CGH40010 10W GaN transistor as a function of back off from the full power

## 2.4 Conventional DPA Bandwidth Performance

Over the frequency band, drain to source capacitance $C$, package inductance $L_s$ and the bias feed inductance $L$ will have their effects as well. Thus, the ABCD matrices should be written down as a function of $\omega$ where $\omega_0$ is the center design frequency.

$$\begin{bmatrix} A_c & B_c \\ C_c & D_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L_s \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/j\omega L & 1 \end{bmatrix} \begin{bmatrix} cos\frac{w}{w_0}90^o & jZsin\frac{w}{w_0}90^o \\ \frac{j}{Z}sin\frac{w}{w_0}90^o & cos\frac{w}{w_0}90^o \end{bmatrix} \tag{2.29}$$

$$\begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L_s \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/j\omega L & 1 \end{bmatrix} \tag{2.30}$$

The frequency limitation mainly comes from the transistor's drain to source capacitance $C$ and the quarter-wave transmission line at the output of the carrier

amplifier, transforming the impedance. To compare and quantify the frequency limitation from the transistor, we define a quality factor with the definition shown in Eq. 2.31. As the parasitic drain to source capacitance increases, the transistor's inherent bandwidth reduces, which affects the overall Doherty power amplifier frequency response.

$$Q = \omega_0 C R_{opt} \tag{2.31}$$

Fig. 2.14 shows the output power and efficiency at two different drive levels, full power, and 6 dB backoff power. At 6 dB backoff, the output power and efficiency change significantly with respect to frequency. If 50% efficiency is chosen for a design target, $0.84f_0$ to $1.16f_0$ becomes the usable bandwidth, where $f_0$ is the center design frequency.

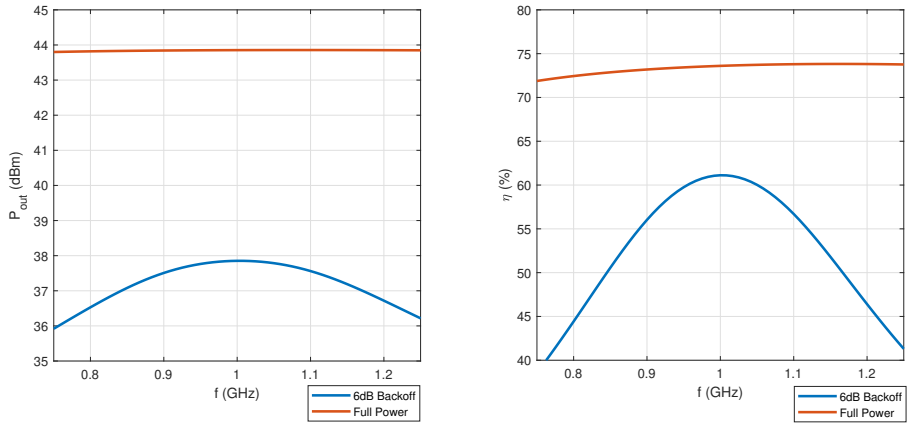


Figure 2.14: Power output (left) and efficiency (right) of the conventional Doherty Power Amplifier as a function of frequency for full-power (orange) and for 6 dB BO (blue).

For a given transistor, with a known quality factor $Q$, it is possible to optimize the combining network and the impedance transformation ratios to reduce efficiency variation over frequency. The next chapter will focus on the output combiner networks to achieve higher bandwidth for Doherty power amplifiers.

# Chapter 3

# Bandwidth Performance of Output Networks

The output network plays a crucial role in the performance of the DPA [6]. We divide the output network into two parts: A combining network (CN) which combines the outputs of both amplifiers and a post-matching network (PMN), which transforms the combining node impedance to the load impedance. In this section, we present different CN and PMN topologies.

A generic Doherty power amplifier could be represented as in Fig. 3.1. In this representation, there are 2-port networks inside the carrier and peaking amplifier networks, where we will define different combining networks. After the combining node, there is another impedance transformation called the "post-matching network" that transforms the impedance to the output termination, which is usually 50Ω. Since this study focuses on the limitations coming from the output network, the input of the amplifier is simplified. Wideband power division and transistor input impedance matching should also be wideband but these challenges are already addressed in various studies in the literature.

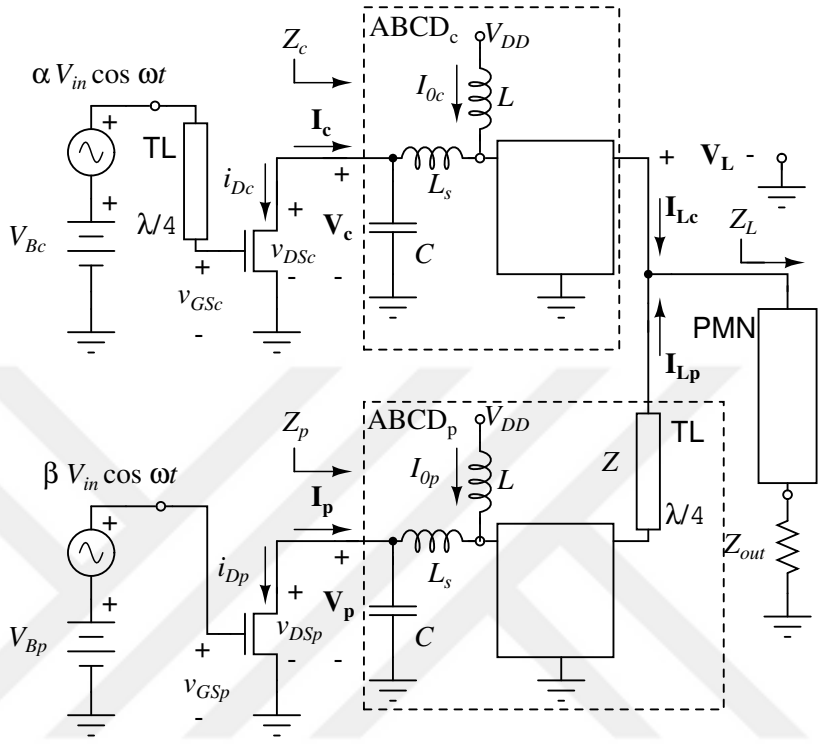


Figure 3.1: Generic Representation of Doherty Power Amplifier Schematic

## 3.1 Combining Network (CN)

We introduce two factors for the purpose of bandwidth optimization. Using the first factor, $\zeta$, we set the combining node impedance at the center frequency, $\omega_0$, as

$$Z_L(\omega_0) = \zeta \frac{R_{opt}}{2} \tag{3.1}$$

Using the second factor, $\kappa$, we set $Z_c$ and $Z_p$ at full-drive as

$$Z_c(\omega_0) = Z_p(\omega_0) = \kappa R_{opt} \tag{3.2}$$

and at 6 dB BO ($Z_{cBO}$) as

$$Z_{cBO}(\omega_0) = 2\kappa R_{opt} \tag{3.3}$$

At the center frequency and full power, the impedance transformation circuits at the output of both transistors should transform $Z_c(\omega_0) = Z_p(\omega_0) = \kappa R_{opt}$ to

$2Z_L$ so that when they are connected in parallel at the combining node it becomes $Z_L$. This corresponds to a transformation ratio of $\zeta/\kappa$. At 6 dB BO, the carrier amplifier's impedance transformation circuit should transform $Z_{cBO}(\omega_0) = 2\kappa R_{opt}$ to $Z_L$, corresponding to a transformation ratio of $\zeta/4\kappa$.

With a selection of $\kappa < 1$, the small-signal gain and maximum power are reduced at the center frequency, while increasing the performance at band edges, contributing to the bandwidth enhancement. However, we will keep $0.84 < \kappa < 1.2$ to prevent a gain reduction of more than 1.5 dB and to preserve the linearity within acceptable limits.

### 3.1.1 Conventional Combining Network

The conventional combining network is shown in Fig. 3.2.

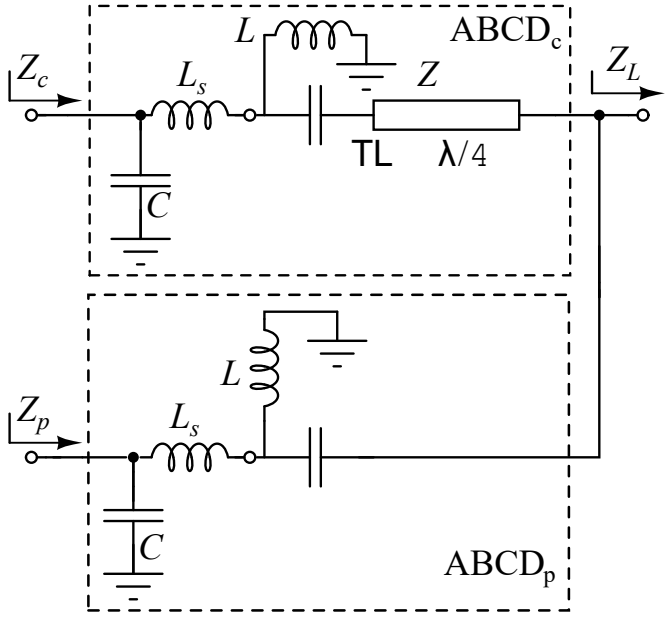


Figure 3.2: Conventional combining network.

The output capacitance, $C$, of each transistor is tuned out at the center frequency with a suitable shunt inductance, $L$, as given in Table 2.2, acting also like

the drain bias RFC. If $L$ turns out to be too small for practical realization, it can be replaced by a high impedance ($Z_H$) transmission line with a length $x$ (in $\lambda_0$ units) with a slight degradation in bandwidth performance.

$$x = \frac{1}{2\pi} \tan^{-1}\left(\frac{\omega_0 L}{Z_H}\right) \tag{3.4}$$

Since the peaking transistor is connected directly to the combining node, it is not possible to optimize $\zeta$ and $\kappa$ independently. To maintain the equal contribution of power at full-drive we must set

$$\zeta = \kappa \text{ and } Z = \zeta R_{opt} \tag{3.5}$$

Obviously, the delay compensation at the input side depicted in Fig. 3.1 must be swapped between transistors for proper operation.

### 3.1.2 Type I Combining Network - Two Section Peaking

The CN [17],[18],[19] shown in Fig. 3.3 achieves the desired characteristics using three quarter-wave transmission lines, which allows easy implementation, especially at high frequencies. $Z_1$ should transform $2Z_L$=$\zeta R_{opt}$ to $\kappa R_{opt}$ at full power and $Z_L$=$\zeta R_{opt}/2$ to $2\kappa R_{opt}$ at 6 dB BO. Similarly, $Z_2$ and $Z_3$ should transform $\zeta R_{opt}$ to $\kappa R_{opt}$ at the full-drive level. When the peaking transistor is off, no loading is presented at the combining node at the center frequency since there is a shunt inductance, $L$, to tune out the drain capacitance, $C$, at that frequency. Since $C$ is tuned out only at the center frequency, it's loading at other frequencies is one of the bandwidth limiting factors.

The transmission line impedances are given by

$$Z_1 = \sqrt{\kappa\zeta} R_{opt} \tag{3.6}$$

$$Z_2 = \kappa^{3/4}\zeta^{1/4} R_{opt} \quad Z_3 = \kappa^{1/4}\zeta^{3/4} R_{opt} \tag{3.7}$$

Note that both $Z_2$ and $Z_3$ contribute to transformation for a wider band operation.

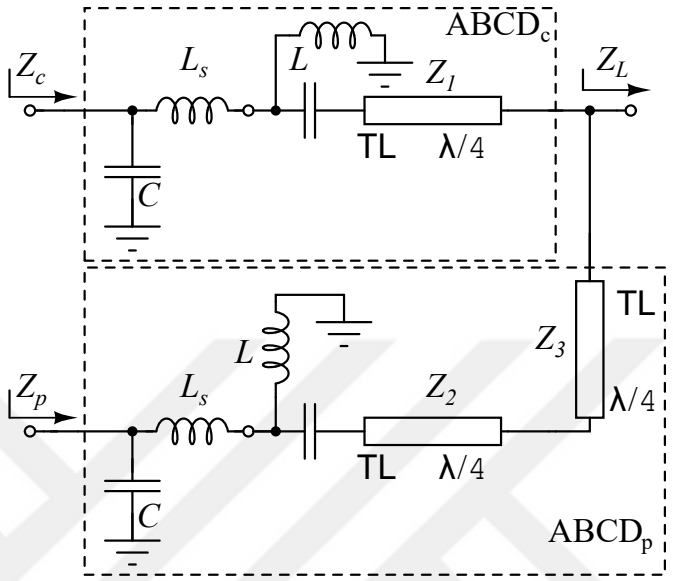


Figure 3.3: Type I Combining Network

### 3.1.3 Type II Combining Network - Parasitic Compensation with Lumped Inverter

A wide-band combining network using lumped elements [20],[21] is shown in Fig. 3.4. The inverters connected to the drain of the transistors have the possibility of absorbing the drain capacitance, $C$, and the package inductance, $L_s$, as part of the inverter, resulting in a higher bandwidth.

For the carrier amplifier, we need an inverter that transforms $\zeta R_{opt}$ to $\kappa R_{opt}$ under full-power. The same inverter will transform $\zeta R_{opt}/2$ to $2\kappa R_{opt}$ with 6 dB BO.

The peaking amplifier needs an identical inverter. Since the drain capacitor of the transistor is already present, depending on the value of the inverter ratio, adding a shunt capacitance or inductance on the drain side may be necessary. The component values can be calculated as:

$$C_1 = \frac{1}{\omega_0 R_{opt}\sqrt{\zeta\kappa}} \quad L_1 = \frac{R_{opt}\sqrt{\zeta\kappa}}{\omega_0} - L_s \tag{3.8}$$

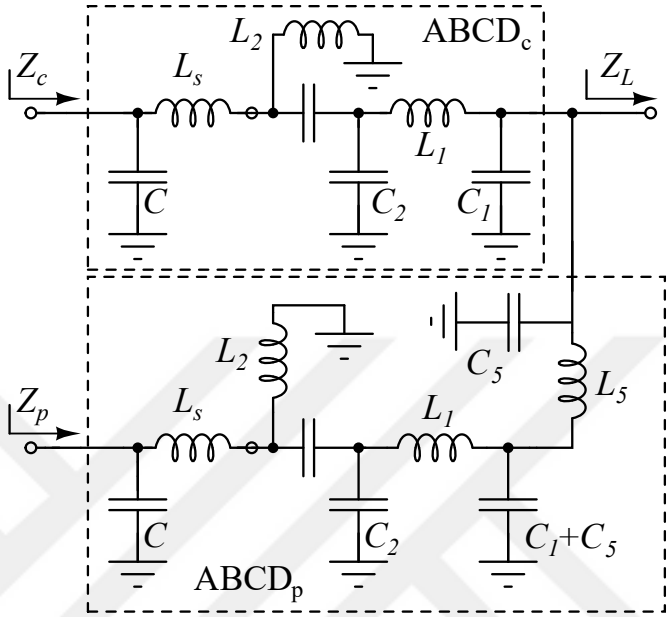


Figure 3.4: Type II Combining Network

$$C_5 = \frac{1}{\omega_0 R_{opt} \zeta} \quad L_5 = \frac{R_{opt}\zeta}{\omega_0} \tag{3.9}$$

where $L_s$ is the series package inductance at the drain.

$$C_2 = \begin{cases} C_1 - C & \text{if } C_1 > C \\ 0 & \text{otherwise} \end{cases} \tag{3.10}$$

$$L_2 = \begin{cases} 1/[(C - C_1)\omega_0^2] & \text{if } C_1 < C \\ \infty & \text{otherwise} \end{cases} \tag{3.11}$$

For a good bandwidth performance, it is important to choose $\zeta$ and $\kappa$ so that $C_1$ is nearly equal to the drain capacitance, $C$, if possible. In that case, there is no need for $C_2$ while a large value of $L_2$ can be kept to bias the device.

### 3.1.4 Type III Combining Network - Parasitic Compensation with TL Inverter

The inductor, $L_1$, of the inverter of CN type II, can be replaced by a transmission line [10], making the circuits easily realizable at microwave frequencies (see Fig. 3.5). It can be approximated using a transmission line of impedance $Z_H$ and length $x_3$ (in $\lambda_0$ units) as seen in Fig. 3.5.

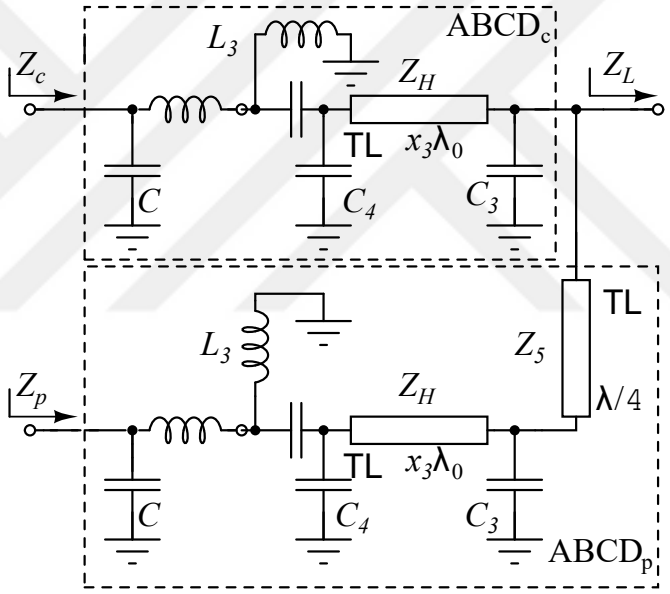


Figure 3.5: Type III Combining Network

We choose $Z_H$ to be 40% higher than the higher impedance value to shorten its length, but not too high to avoid fabrication problems. The two unknown values, $x_3$ and $C_3$, can be found by equating the input impedance of the inverter to the required impedance at the center frequency.

The required values are determined by solving a number of cases and fitting a polynomial to the results. For an inverter that inverts $R_0{=}\zeta R_{opt}$ to $rR_0$ with $r{=}\kappa/\zeta$ <1, we have

$$\omega_0 C_3 = \frac{-171.67r^3 + 466.58r^2 - 505.32r + 279.58}{100R_0} \tag{3.12}$$

$$x_3 = \frac{25.15p^3 - 67.43p^2 + 141.99p + 26.97}{1000}$$

$$\text{with } Z_H = 1.4R_0 \quad (3.13)$$

where

$$p = \left(\sqrt{r} - \frac{\omega_0 L_s}{R_0}\right)^2 \quad (3.14)$$

If the $Z_H$ value of Eq. 3.13 is too high for implementation, Eqs. B.2 and B.1 of Appendix B can be used for a smaller $Z_H$. If the required shunt capacitance is smaller than the drain capacitance of the transistor, a shunt inductance ($L_3$) can be added, which can also act as the DC power feed for the transistor. The remaining component values can be determined from

$$C_4 = \begin{cases} C_3 - C & \text{if } C_3 > C \\ 0 & \text{otherwise} \end{cases} \quad (3.15)$$

$$L_3 = \begin{cases} 1/[(C - C_3)\omega_0^2] & \text{if } C_3 < C \\ \infty & \text{otherwise} \end{cases} \quad (3.16)$$

$$Z_5 = \zeta R_{opt} \quad (3.17)$$

## 3.2 Post Matching Network

A post matching network(PMN) providing the desired combining node impedance can be chosen depending on the bandwidth requirement and the ratio of $Z_{out}$ to $Z_L$. A number of possibilities are shown in Fig. 3.6.

In (a), a single quarter-wave transmission line is used to transform $Z_L$ to $Z_{out}$ with

$$Z_A = \sqrt{Z_L Z_{out}} \quad (3.18)$$

If $\zeta R_{optc}/2$ is close to $Z_{out}$, one section is enough even in a wide band. For a larger transformation ratio, two $\lambda/4$ transmission lines may be used as shown in (b) with values

$$Z_B = Z_L^{3/4} Z_{out}^{1/4} \text{ and } Z_C = Z_L^{1/4} Z_{out}^{3/4} \quad (3.19)$$

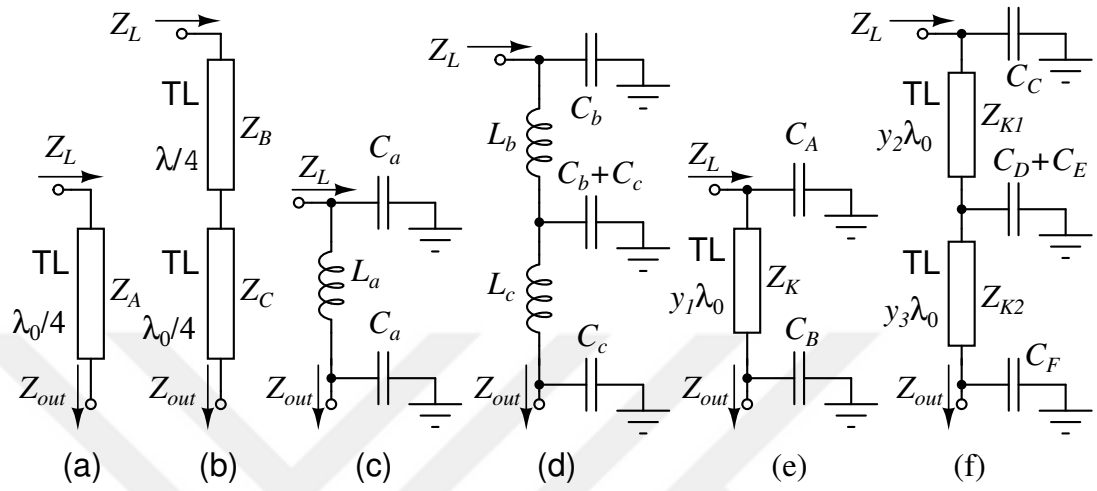


Figure 3.6: Different Post Matching Networks.

The impedance transformation can also be achieved with a small size lumped element inverter shown in (c). In this case, we should choose

$$L_a = \frac{\sqrt{Z_L Z_{out}}}{\omega_0} \quad \text{and} \quad C_a = \frac{1}{\omega_0^2 L_a} \tag{3.20}$$

For a wider bandwidth or when the transformation ratio is high, two inverters can be used as shown in (d) with

$$L_b = \frac{Z_L^{3/4} Z_{out}^{1/4}}{\omega_0} \quad \text{and} \quad C_b = \frac{1}{\omega_0^2 L_a} \tag{3.21}$$

$$L_c = \frac{Z_L^{1/4} Z_{out}^{3/4}}{\omega_0} \quad \text{and} \quad C_c = \frac{1}{\omega_0^2 L_a} \tag{3.22}$$

When a lumped inductance is not desirable or practical, PMN shown in (e) can be utilized: a high impedance ($Z_K$) transmission line and two shunt capacitors, $C_A$ and $C_B$. Since we do not need an inverter, the shunt capacitances do not have to be equal in value, hence providing higher bandwidth. The electrical length, $y_1$, of the transmission line (in $\lambda_0$ units) can be found from the solution of the nonlinear equation

$$\frac{Z_A}{Z_K} - \frac{2\pi y_1}{\cos^2(2\pi y_1)} = 0 \tag{3.23}$$

We equate the real part of $Z_{L1}$ to $Z_L(\omega_0)$ and the imaginary part of $Z_{L1}$ to 0, both at $\omega_0$. We find $C_A$ and $C_B$, by solving the resulting nonlinear equations numerically. For an impedance transformer that transforms $rR_0$ to $R_0$ with $0.4 < r < 1$ we have

$$\omega_0 C_A = \frac{27.06r^3 - 76.17r^2 + 83.14r - 11.76}{100R_0} \tag{3.24}$$

$$\omega_0 C_B = \frac{-181.59r^3 + 503.13r^2 - 568.26r + 268.09}{100R_0} \tag{3.25}$$

$$y_1 = \frac{25.37r^3 - 78.17r^2 + 108.17r + 29.24}{1000} \text{ and } Z_K = 1.4R_0 \tag{3.26}$$

Since the combining networks are of low-pass type, the band center is smaller than $\omega_0$.

For a wider band or when the transformation ratio from $Z_L$ to $Z_{out}$ is high, one may repeat the transformation operation in two steps and use two sections of the circuit of (e) as shown in (f).

| PMN | $Z_{out}/Z_L$ | 1.5 | 1.7 | 2 | 3 | 5 |
|---|---|---|---|---|---|---|
| (a) | $f_1/f_0$ | 0.3 | 0.53 | 0.67 | 0.80 | 0.87 |
| | $f_2/f_0$ | 1.7 | 1.47 | 1.33 | 1.2 | 1.13 |
| (b) | $f_1/f_0$ | 0.25 | 0.4 | 0.5 | 0.63 | 0.70 |
| | $f_2/f_0$ | 1.8 | 1.6 | 1.5 | 1.37 | 1.3 |
| (c) | $f_1/f_0$ | 0.77 | 0.79 | 0.81 | 0.86 | 0.90 |
| | $f_2/f_0$ | 1.13 | 1.13 | 1.12 | 1.11 | 1.08 |
| (d) | $f_1/f_0$ | 0.71 | 0.72 | 0.73 | 0.75 | 0.78 |
| | $f_2/f_0$ | 1.18 | 1.18 | 1.17 | 1.17 | 1.16 |
| (e) | $f_1/f_0$ | 0.34 | 0.57 | 0.69 | 0.83 | 0.95 |
| | $f_2/f_0$ | 1.37 | 1.30 | 1.22 | 1.16 | 1.14 |
| (f) | $f_1/f_0$ | 0.39 | 0.51 | 0.62 | 0.75 | 0.83 |
| | $f_2/f_0$ | 2.05 | 1.97 | 1.91 | 1.73 | 1.58 |

Table 3.1: Bandwidth performance of different PMNs.

The performances of different PMNs as a function of transformation ratio, $Z_{out}/Z_L$, are given in Table 3 for the condition that the transformed impedance

has a return loss higher than 15 dB. Note that the networks can also be used with the inverted transformation ratio.

An inspection of the table indicates that lumped element networks (PMN types (c) or (d)) can be used only when the transformation ratio and/or the bandwidth is small. For wider bandwidths or when the transformation ratio is high, for example, with high power transistors with large $\xi$ values, PMN type (b) gives the best performance. PMN types (e) and (f) give a good performance despite their smaller size. The center frequency of the PMN may have to be shifted since the band limits are not always symmetrical.

## 3.3 Optimized Combining Networks

For the purpose of optimization, we define the bandwidth of a DPA in which all of the following constraints are satisfied:

- The efficiency at 6 dB output BO is higher than 50%
- The efficiency at full-power is higher than 60%
- The power at 6-dB output BO is at most 1.5 dB less than the normal value.
- The power at full-power is at most 1.5 dB less than the normal value.

Here, "full-power" is defined as the 1 dB gain compression point at the center frequency with the optimal load. We should also consider the linearity of the DPA and keep it within acceptable limits. 1.5 dB value above is chosen as a compromise between linearity and bandwidth. A higher value will result in a higher bandwidth with more nonlinearity.

For bandwidth optimization of the conventional CN, the combining node impedance, $Z_L$=$\zeta R_{opt}/2$ should be as high as possible to minimize the quality

factor of the drain capacitance tuning network. We can increase $\zeta$ only up to 1.2, since $\zeta$=$\kappa > 1.2$ results in an unacceptable level of nonlinearity.

For other types of CN, we can increase $\zeta$ to higher values, while keeping $\kappa$ less than unity for a large band.

As an example, we consider CN type I and PMN type (a) with $\zeta$=4.8, $\kappa$=0.84 at $f_0$=3.5 GHz. We show the power and efficiency contours defined by the constraints above on the Smith charts of Fig. 3.7 for both carrier and peaking amplifiers. In the same charts, we also show the impedances experienced by the carrier ($Z_c$) and peaking ($Z_p$) amplifiers as a function of frequency at two drive levels, which should stay inside the relevant contours.

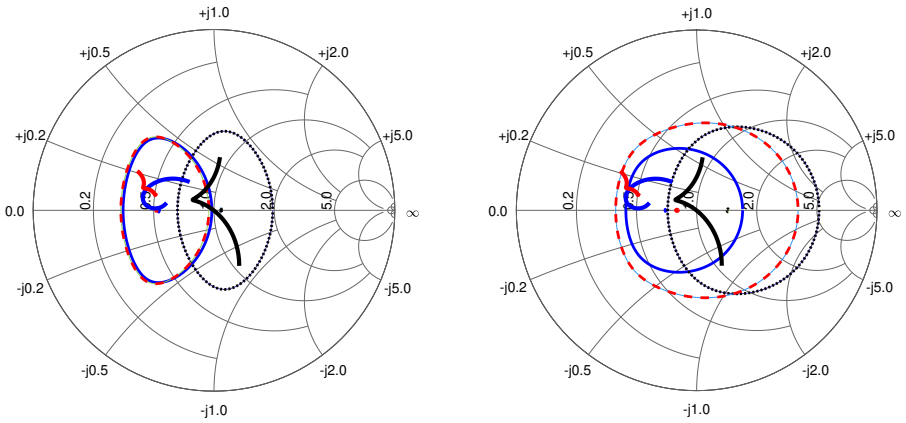


Figure 3.7: Limiting power (left) and efficiency (right) contours on Smith charts, for carrier amplifier at full-power (solid) and 6 dB backoff (dotted), and for peaking amplifier at full-power (dashed). Impedances seen by the amplifiers as a function of frequency ($0.79f_0$ to $1.20f_0$) are also shown.

These Smith charts can be used to observe the variation of impedances as the values of $\zeta$ and $\kappa$ are varied. The values are then optimized to reach the widest bandwidth. Those factors should be chosen to keep the impedance values within the power and efficiency contours for as wide frequency range as possible. We note that decreasing the value of $\kappa$ moves the impedance curves toward the left, reducing the power and efficiency at the center frequency while boosting power and efficiency at the band edges. On the other hand, a higher $\zeta$ improves the bandwidth at the backoff level resulting in a reduction of the bandwidth at

full-power.

| CN | $f_0$ (GHz) | $\zeta$ | $\kappa$ | $f_1/f_0$ | $f_2/f_0$ | $\frac{Z_{out}}{\xi Z_L}$ |
|---|---|---|---|---|---|---|
| Conv. | 1.0 | 1.2 | 1.2 | 0.793 | 1.200 | 3.21 |
| | 1.5 | 1.2 | 1.2 | 0.834 | 1.185 | 3.40 |
| | 2.0 | 1.2 | 1.2 | 0.852 | 1.165 | 3.62 |
| | 2.5 | 1.2 | 1.2 | 0.865 | 1.147 | 3.95 |
| | 3.0 | 1.2 | 1.2 | 0.878 | 1.134 | 4.45 |
| | 3.5 | 1.2 | 1.2 | 0.885 | 1.121 | 5.08 |
| I | 1.0 | 4.8 | 0.84 | 0.685 | 1.315 | 0.80 |
| | 1.5 | 4.8 | 0.84 | 0.720 | 1.295 | 0.85 |
| | 2.0 | 4.8 | 0.84 | 0.745 | 1.265 | 0.91 |
| | 2.5 | 4.8 | 0.84 | 0.776 | 1.231 | 0.98 |
| | 3.0 | 4.8 | 0.84 | 0.785 | 1.210 | 1.11 |
| | 3.5 | 4.8 | 0.84 | 0.798 | 1.188 | 1.27 |
| II | 1.0 | 2.6 | 0.94 | 0.605 | 1.195 | 1.44 |
| | 1.5 | 2.8 | 0.93 | 0.597 | 1.190 | 1.34 |
| | 2.0 | 2.9 | 0.91 | 0.593 | 1.187 | 1.30 |
| | 2.5 | 3.1 | 0.87 | 0.64 | 1.18 | 1.21 |
| | 3.0 | 3.3 | 0.84 | 0.67 | 1.170 | 1.14 |
| | 3.5 | 3.5 | 0.84 | 0.695 | 1.150 | 1.07 |
| III | 1.0 | 2.1 | 1.14 | 0.560 | 1.21 | 1.79 |
| | 1.5 | 2.2 | 1.02 | 0.555 | 1.220 | 1.71 |
| | 2.0 | 2.2 | 0.99 | 0.565 | 1.230 | 1.71 |
| | 2.5 | 2.2 | 0.91 | 0.626 | 1.230 | 1.71 |
| | 3.0 | 2.2 | 0.84 | 0.66 | 1.213 | 1.71 |
| | 3.5 | 2.4 | 0.84 | 0.68 | 1.162 | 1.56 |

Table 3.2: Normalized band limits of DPA with optimized $\zeta$ and $\kappa$ for CGH400XX family transistors at different frequencies. The input matching network and PMN are assumed to be properly chosen not causing a band limitation.

Table 3.2 gives the optimized results for CGH400XX series transistors at different center frequencies assuming that PMN matches $Z_L$ to $Z_{out}$ perfectly at all frequencies. The values of $\zeta$ and $\kappa$, as well as the normalized band limits, are given in the same table for different types of combining networks. [1] This table is applicable for transistors scaled with factor $\xi$ since an increase in the transistor

[1]Using the provided MATLAB code, it is possible to determine the optimal $\zeta$ and $\kappa$ values and the corresponding band limits for other technologies, when the transistor is approximated by three parameters.

gate width simply causes a reduction of the combining node impedance to $Z_L/\xi$.

| CN | $Q$ | $\zeta$ | $\kappa$ | $f_1/f_0$ | $f_2/f_0$ | $\frac{Z_{out}}{\xi Z_L}$ |
|---|---|---|---|---|---|---|
| Conv. | 0.3 | 1.2 | 1.2 | 0.805 | 1.210 | 3.75 |
| | 0.5 | 1.2 | 1.2 | 0.840 | 1.175 | 3.75 |
| | 0.7 | 1.2 | 1.2 | 0.858 | 1.145 | 3.75 |
| | 1.0 | 1.2 | 1.2 | 0.886 | 1.123 | 3.75 |
| | 1.5 | 1.2 | 1.2 | 0.912 | 1.094 | 3.75 |
| | 2.0 | 1.2 | 1.2 | 0.929 | 1.075 | 3.75 |
| I | 0.3 | 5.0 | 0.84 | 0.684 | 1.342 | 0.75 |
| | 0.5 | 5.0 | 0.84 | 0.733 | 1.297 | 0.75 |
| | 0.7 | 5.0 | 0.84 | 0.768 | 1.261 | 0.75 |
| | 1.0 | 5.0 | 0.84 | 0.807 | 1.218 | 0.75 |
| | 1.5 | 5.0 | 0.84 | 0.855 | 1.165 | 0.75 |
| | 2.0 | 5.4 | 0.84 | 0.890 | 1.125 | 0.75 |
| II | 0.3 | 2.9 | 0.98 | 0.520 | 1.200 | 1.30 |
| | 0.5 | 2.9 | 0.98 | 0.520 | 1.200 | 1.30 |
| | 0.7 | 3.0 | 0.93 | 0.570 | 1.200 | 1.25 |
| | 1.0 | 3.2 | 0.89 | 0.685 | 1.200 | 1.17 |
| | 1.5 | 3.5 | 0.87 | 0.790 | 1.160 | 1.07 |
| | 2.0 | 4.5 | 0.86 | 0.860 | 1.130 | 0.84 |
| III | 0.15 | 3.0 | 0.94 | 0.530 | 1.267 | 1.25 |
| | 0.3 | 3.0 | 0.94 | 0.530 | 1.267 | 1.25 |
| | 0.5 | 3.1 | 0.94 | 0.530 | 1.267 | 1.25 |
| | 0.7 | 3.1 | 0.85 | 0.615 | 1.240 | 1.21 |
| | 1.0 | 3.6 | 0.84 | 0.725 | 1.230 | 1.04 |
| | 1.5 | 4.0 | 0.84 | 0.815 | 1.177 | 0.94 |
| | 2.0 | 4.2 | 0.84 | 0.865 | 1.140 | 0.89 |

Table 3.3: Normalized band limits of DPA with optimized $\zeta$ and $\kappa$ for a transistor with $L_s$=0 and different combining networks. The input matching network and PMN are assumed not to cause a band limitation.

The effect of series drain inductance, $L_s$, is negligible at lower frequencies or in MMIC circuits where the transistors are integrated with the rest of the combining circuit. In such cases, it is possible to list more general results in terms of the drain quality factor, $Q$, rather than frequency. Quality factor results are presented in Table 3.3. Since all values in the table are normalized, they are applicable for the design of a DPA at any frequency band with any transistor, if $C$ and $R_{opt}$ of the transistor are known.

Inspection of Tables 3.2 and 3.3 indicates that the widest bandwidth is obtained with CN type II or III since $C$ and $L_s$ can be absorbed as part of the combining network. In Fig. 3.8 we present a comparison of different CN types for CGH400XX transistors with $f_0$=2.5 GHz, showing the power and efficiency at full-power and 6-dB BO. CN type III gives the widest bandwidth, while type II is slightly worse. CN type I may still be preferred for its ease of implementation even though it has the smallest bandwidth.

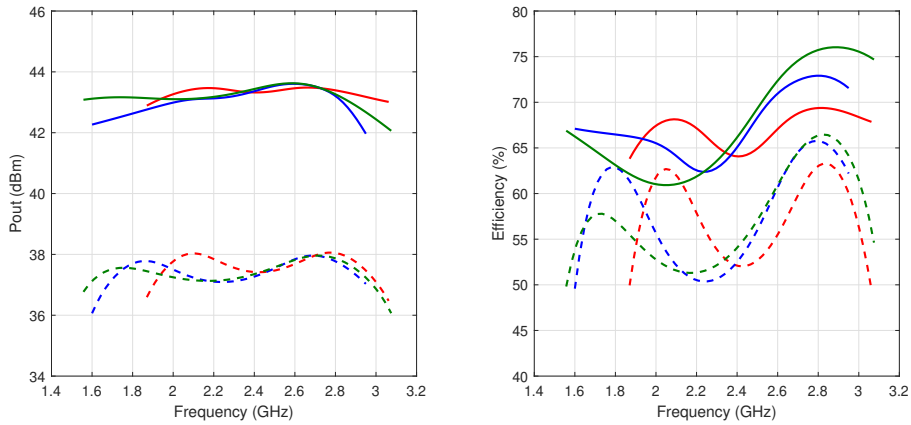


Figure 3.8: Comparison of power outputs (left) and efficiencies (right) of CN types I (red), II (blue), and III (green), all using transistors with $Q$=0.77. Solid lines represent full power and dashed lines represent 6 dB BO.

Tables are given for our specific bandwidth definition given above. If the limiting values in that definition are relaxed, it is possible to obtain DPAs with a wider bandwidth but with a lower performance.

## 3.4 Example designs

To demonstrate the use of our method, we give a number of example DPA designs.

### 3.4.1 Example I

As the first example, we use a CN type I with CGH40010 ($\xi$=1) at $f_0$=3.5 GHz. At this frequency we have $R_{opt}$=16.4 Ω and $L$=0.935 nH from Table 2.2. From Table 3.2, we set $\zeta = 4.8$ and $\kappa = 0.84$ to obtain a band from $f_1$=2.8 GHz to $f_2$=4.16 GHz. With $Z_{out}/Z_L$=1.27, it is sufficient to use PMN type (a), (c), or (e) without limiting the bandwidth. The values of components in the output network calculated from the relevant equations are given in Table 3.4 for PMN type (a).

| Comp. | Eq. | Value | Comp. | Eq. | Value |
|---|---|---|---|---|---|
| $Z_1$ | 3.6 | 32.9 Ω | $Z_2$ | 3.7 | 21.3 Ω |
| $Z_3$ | 3.7 | 50.9 Ω | $Z_A$ | 3.18 | 44.3 Ω |

Table 3.4: Component values for the CN type I and PMN type (a) with $f_0$=3.5 GHz.

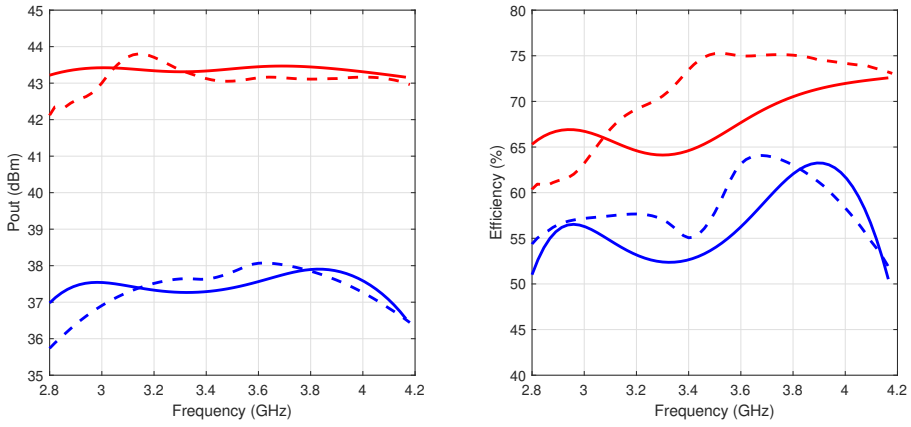


Figure 3.9: Power output (left) and efficiency (right) of the first example as a function of frequency for full-power (red) and for 6 dB BO (blue). Harmonic balance simulations (dashed) are also drawn.

Note that the inductance $L$ can be replaced with a high impedance transmission line of length determined by Eq. 3.4. The results from both our model and harmonic balance simulation using vendor supplied nonlinear model of the transistors are shown in Fig. 3.9. Since we ignore the bandwidth limitation of the input matching networks, for a fair comparison we connect voltage sources with zero source impedance as the input driving sources in the harmonic balance simulations. The similarity between the curves is a verification of our simple model.

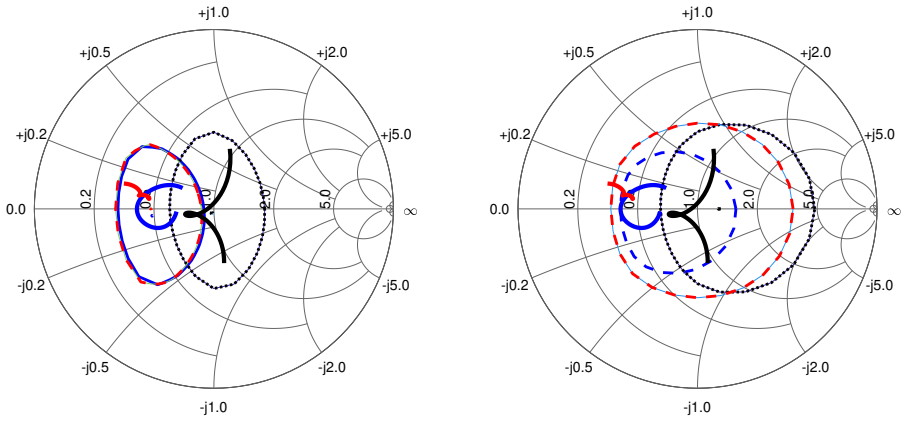


Figure 3.10: Limiting power (left) and efficiency (right) contours on Smith charts, for carrier amplifier at full-power (solid) and 6 dB backoff (dotted), and for peaking amplifier at full-power (dashed). Impedances seen by the amplifiers as a function of frequency (2.8GHz to 4.16GHz) are also shown.

In Fig. 3.11 we present the calculated AM-AM and AM-PM distortions of this example at different frequencies. The phase distortion becomes significant when the peaking transistor begins to conduct. As it is previously shown [22],[23],[24],[25], frequency dependent AM/PM nonlinearity is an undesired attribute of Doherty amplifiers, which may be reduced by analog or digital predistortion methods or by modifying the input power split ratio.

If we had used the transistor CGH40045 with $\xi$=4.5, $L$, $Z_1$, $Z_2$, and $Z_3$ would have been scaled down by 4.5 and $Z_{out}/Z_L$=1.27$\xi$=5.71 would have required PMN type (b) or (f). For such a large transistor, however, the assumption of the input

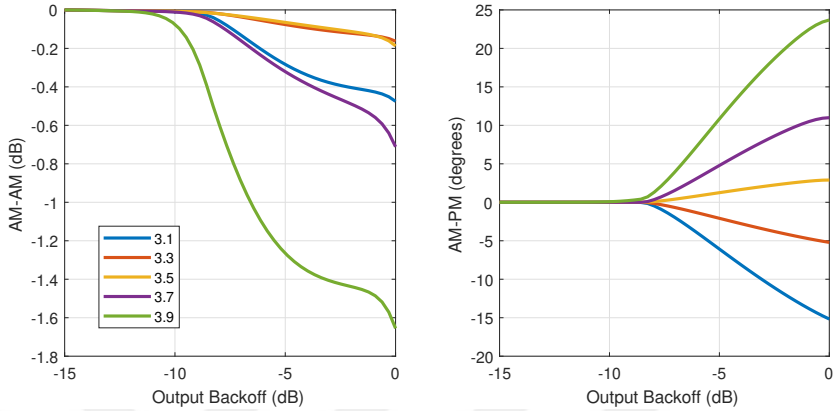


Figure 3.11: AM-AM (left) and AM-PM (right) characteristics of the first example at 3.1, 3.3, 3.5, 3.7, and 3.9 GHz.

matching network not limiting the bandwidth may be optimistic.

### 3.4.2 Example II

As the second example, we use CN type II with CGH40025 ($\xi$=2.5) for $f_0$=2.5 GHz. We use $R_{opt}$=26.6/$\xi$=10.6 Ω from Table 2.2 since the effect of $L_s$ is eliminated with CN type II. From Table 3.2, we set $\zeta$=3.1 and $\kappa$=0.87 and get a band from $f_1$=1.60 GHz to $f_2$=2.95 GHz. With $Z_{out}/Z_L$=1.30$\xi$=3.03, we should use PMN type (b) or type (f) not to reduce bandwidth. The component values are given in Table 3.5 for PMN type (b).

| Comp. | Eq. | Value | Comp. | Eq. | Value |
|---|---|---|---|---|---|
| $L_1$ | 3.8 | 0.99 nH | $L_2$ | 3.11 | 4.52 nH |
| $C_1$ | 3.9 | 3.70 pF | $C_2$ | 3.9 | 0 |
| $L_5$ | 3.17 | 2.10 nH | $C_5$ | 3.18 | 1.93 pF |
| $Z_B$ | 3.19 | 21.8 Ω | $Z_C$ | 3.19 | 37.9 Ω |

Table 3.5: Component values of the second example of CN type II and PMN type (b) at $f_0$=2.5 GHz.

We plot the results in Fig. 3.12 along with the harmonic balance simulation of the same circuit.

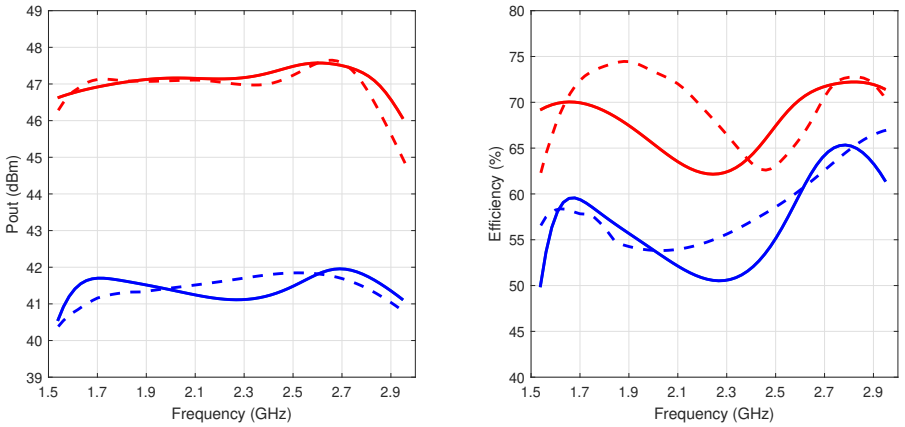


Figure 3.12: Power output (left) and efficiency (right) of the second example as a function of frequency for full-power (red) and for 6 dB BO (blue). Harmonic balance simulations are also shown (dashed).

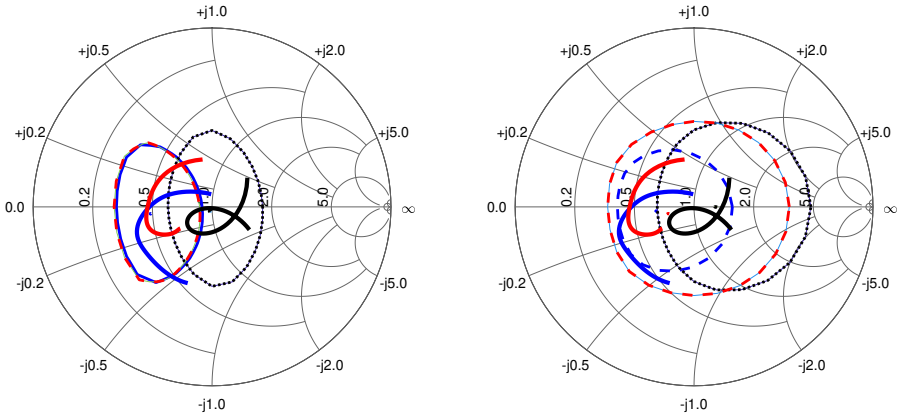


Figure 3.13: Limiting power (left) and efficiency (right) contours on $Z_0 = \frac{50\Omega}{\xi} = 20\Omega$ Smith charts, for carrier amplifier at full-power (solid) and 6 dB backoff (dotted), and for peaking amplifier at full-power (dashed). Impedances seen by the amplifiers as a function of frequency (1.60GHz to 2.95GHz) are also shown.

### 3.4.3 Example III

As the third example, we use the CN type III at $f_0$=1.5 GHz with $\xi$=1. From Table 3.2 with $\zeta$=2.2 and $\kappa$=1.02 we expect to get a band from $f_1$=820 MHZ to $f_2$=1.80 GHz. With $Z_{out}/Z_L$=1.70, we can use PMN type (f). The values of components in the output network as calculated from relevant equations are given in Table 3.6.

| Comp. | Eq. | Value | Comp. | Eq. | Value |
|---|---|---|---|---|---|
| $x_3$ | 3.13 | 0.0793 | $Z_H$ | 3.13 | 82.2 Ω |
| $C_3$ | 3.12 | 2.20 pF | $C_4$ | 3.15 | 0.360 pF |
| $Z_5$ | 3.17 | 58.7 Ω | | | |
| $y_2$ | 3.26 | 0.0777 | $Z_{K1}$ | 3.26 | 53.6 Ω |
| $y_3$ | 3.26 | 0.0777 | $Z_{K2}$ | 3.26 | 70.0 Ω |
| $C_C$ | 3.24 | 0.535 pF | $C_D$ | 3.25 | 1.28 pF |
| $C_E$ | 3.24 | 0.410 pF | $C_F$ | 3.25 | 0.981 pF |

Table 3.6: Component values of the second example of CN type III and PMN type (f) at $f_0$=1.50 GHz.

The comparison between our model and harmonic balance is depicted in Fig. 3.15.

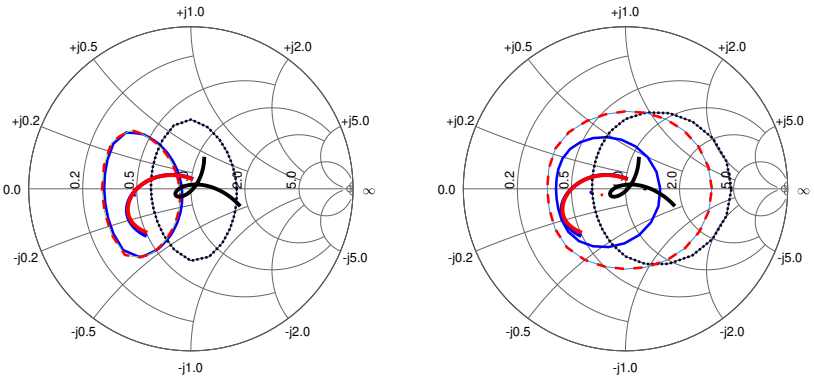


Figure 3.14: Limiting power (left) and efficiency (right) contours on Smith charts, for carrier amplifier at full-power (solid) and 6 dB backoff (dotted), and for peaking amplifier at full-power (dashed). Impedances seen by the amplifiers as a function of frequency (0.82GHz to 1.80GHz) are also shown.

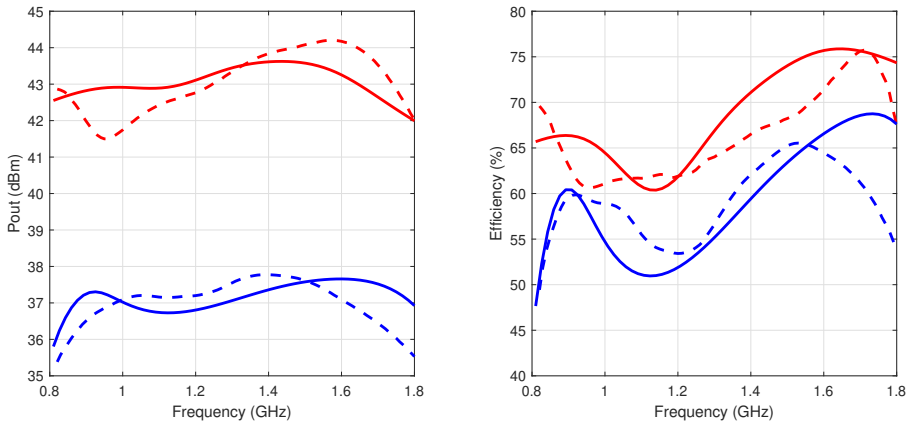


Figure 3.15: Power output (left) and efficiency (right) of the third example as a function of frequency for full-power (red) and for 6 dB backoff (blue). Harmonics balance simulations using vendor supplied transistor model are also shown x(dashed).

### 3.4.4 Example IV

At the last example, we use a relatively low center frequency ($f_0$=0.5 GHz) to demonstrate the use of Table 3.3. At this frequency the effect of $L_s$ is negligible. With $R_{opt}$=26.6 Ω and $C$=1.84 pF, we have $Q$=0.15. We use CN type III. From the table we set $\zeta$=3.0 and $\kappa$=0.97 to get a band from $f_1$=0.26 to $f_2$=0.61 GHz. With $Z_{out}/Z_L = 1.25$, a PMN type (e) is sufficient. The component values are given in Table. 3.7.

| Comp. | Eq. | Value | Comp. | Eq. | Value |
|---|---|---|---|---|---|
| $x_3$ | B.2 | 0.098 | $Z_H$ | B.2 | 79.8 Ω |
| $C_3$ | B.1 | 5.75 pF | $C_4$ | 3.15 | 3.91 pF |
| $Z_5$ | 3.17 | 79.8 Ω | | | |
| $y_1$ | 3.26 | 0.078 | $Z_K$ | 3.26 | 70 Ω |
| $C_A$ | 3.24 | 1.26 pF | $C_B$ | 3.25 | 2.69 pF |

Table 3.7: Component values of the example III at $f_0$=0.50 GHz.

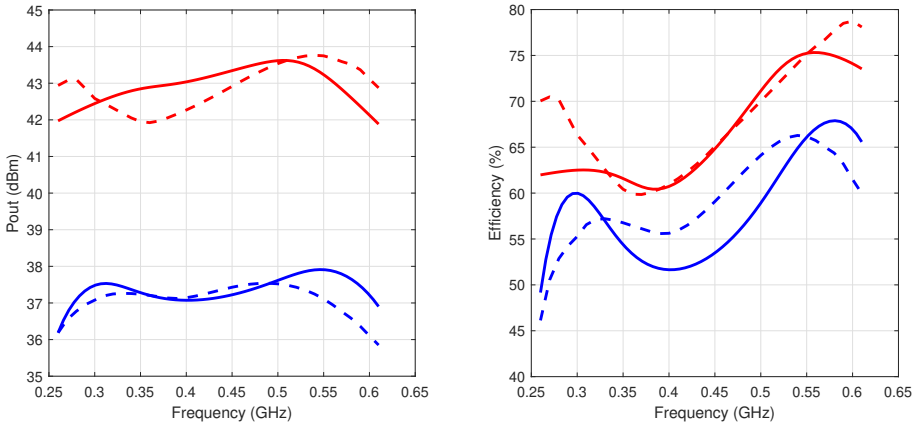


Figure 3.16: Power output (left) and efficiency (right) of the last example as a function of frequency for full-power (red) and for 6 dB backoff (blue). Harmonic balance simulations using the vendor supplied transistor model are also shown (dashed).

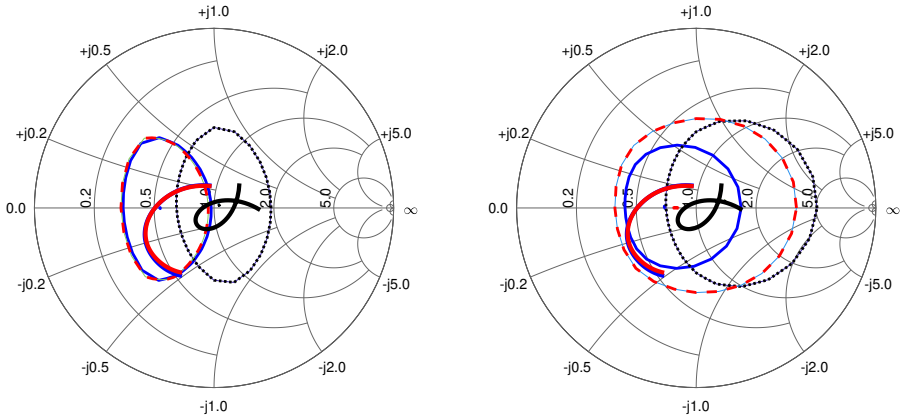


Figure 3.17: Limiting power (left) and efficiency (right) contours on Smith charts, for carrier amplifier at full-power (solid) and 6 dB backoff (dotted), and for peaking amplifier at full-power (dashed). Impedances seen by the amplifiers as a function of frequency (0.26GHz to 0.61GHz) are also shown.

### 3.4.5 Experimental Results

For the purpose of comparing our results with experimental results, we relax the efficiency limits in our bandwidth definition to take care of losses in the output combining network: 46% for 6 dB BO and 56% for full-power.

| Comp. | Eq. | Calculated Value | HB Optimized Value |
|---|---|---|---|
| $Z_1$ | 3.6 | 50.2 Ω | 53.9 Ω |
| $Z_2$ | 3.7 | 33.6Ω | 40.1 Ω |
| $Z_3$ | 3.7 | 80.4 Ω | 85.1 Ω |
| $Z_L$ | 3.18 | 62.2 Ω | 65.6 Ω |

Table 3.8: Component values for CN type I and OMN type (a) at $f_0$=1.0 GHz.

We built a DPA using type I, CN with $\zeta$=4.8 and $\kappa$=0.84 centered at 1.0 GHz. The schematic of the amplifier using two CGH40010 transistors is given in Fig. 3.18. Since $Z_{out}/Z_L$=0.80, a simple PMN of a tapered line of 0.35$\lambda$ at 1.0 GHz is sufficient. Optimized element values along with calculated values are given in Table 3.8.

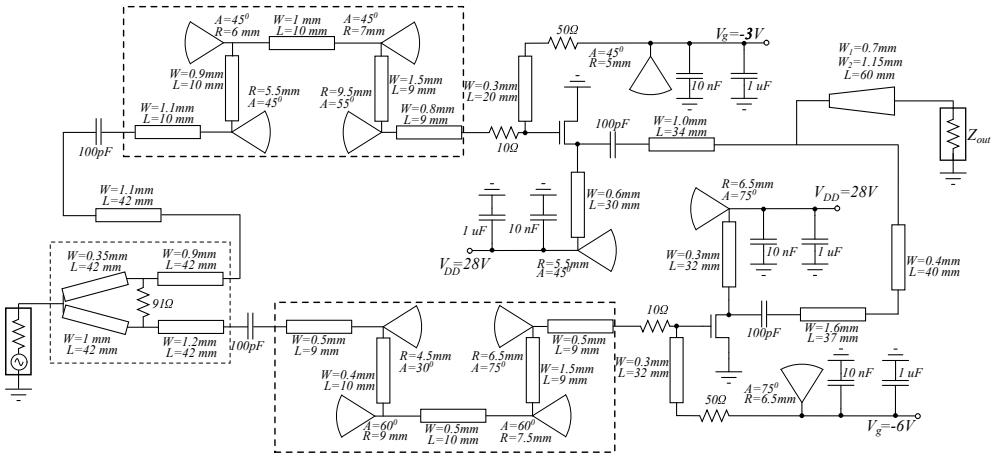


Figure 3.18: The circuit schematic of the fabricated wideband Doherty Power Amplifier

The DPA is implemented on Rogers 4003C[2] substrate with 0.508 mm thickness. The photo of the implementation can be seen in Fig.3.20. The performance of the

[2]Rogers Corp, www.rogerscorp.com

amplifier is depicted in Fig. 3.19 where the efficiency is better than 56% at full power and 46% at 6 dB BO. We achieved a bandwidth from 0.67 to 1.35 GHz, while the predicted bandwidth from Table 3.2 is 0.69 to 1.30 GHz, verifying our method.

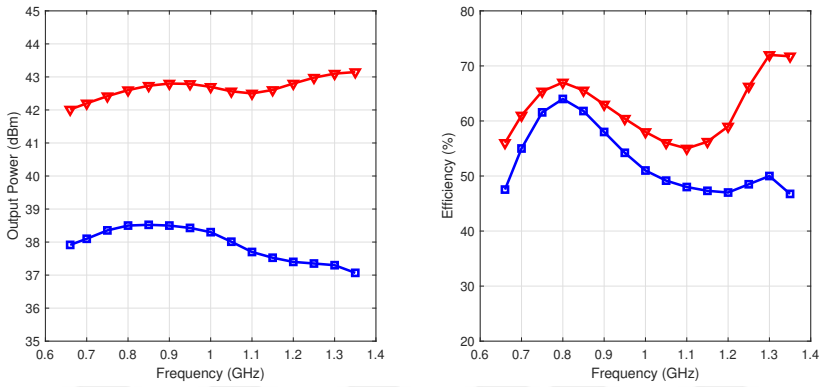


Figure 3.19: Measurements of fabricated DPA: Power output (left) and efficiency (right) as a function of frequency for full-power (red) and for 6 dB BO (blue).

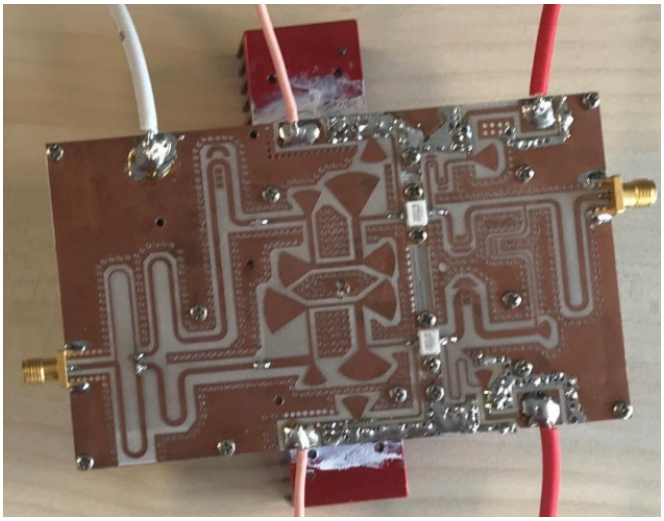

Figure 3.20: Photograph of the fabricated wideband DPA. The dimensions are 20×10 cm.

### 3.4.6 Examples from Previous Works

We chose three experimental studies from the literature whose limiting values are within or close to those in our bandwidth definition. Table 3.9 lists those studies for the estimated $\zeta$ and $\kappa$ values to the best of our understanding, as well as the predicted and measured band limits. Comparison of $\zeta$ and $\kappa$ values to those in the Table 3.2 indicates that they are close to optimum values. The measured band limits are also consistent with our expectations. It is possible to find other examples in the literature with a wider bandwidth, but they have lower performance for efficiency within the band.

| | T.W. | [17] | [21] | [26] |
|---|---|---|---|---|
| CN | I | I | II | III |
| OMN | (a) | N/A | N/A | (b) |
| $\zeta$ | 4.8 | 4 | 2 | 2.1 |
| $\kappa$ | 0.84 | 1 | 1.2 | 1.1 |
| $f_0$ (GHz) | 1.0 | 2.35 | 2.5 | 2.3 |
| $Q$ | 0.29 | 0.66 | 0.7 | 0.64 |
| $f_1/f_0$ (theo) | 0.69 | 0.78 | 0.83 | 0.60 |
| $f_2/f_0$ (theo) | 1.30 | 1.22 | 1.14 | 1.18 |
| $f_1/f_0$ (mea) | 0.67 | 0.9 | 0.8 | 0.69 |
| $f_2/f_0$ (mea) | 1.35 | 1.13 | 1.08 | 1.17 |
| $\eta_{BO}(\%)$ | 46-64 | 39-67 | 48-63 | 46-63 |
| $P_{BO}$ (dBm) | 37-38.5 | 35-39 | 34-35.5 | 37-38.5 |
| $\eta_{FP}(\%)$ | 56-71 | 57-84 | 46-60 | 56-75 |
| $P_{FP}$ (dBm) | 42-43.1 | 41-45 | 40-41 | 43.8-45.2 |

Table 3.9: Summary of this work (T.W.) and three studies from the literature at full-power (FP) and at 6 dB BO.

o

# Chapter 4

# Conclusion

In this thesis, we presented a method to design the output combining network of a wideband DPA maximizing the bandwidth of operation. We used a simple analytical model of the RF transistor with a few parameters ($V_T$, $G_m$, $N_e$, $C$, and $L_s$), and showed that the results are very similar to those obtained from harmonic balance simulation with a much more complex model of transistor.

We first presented a bandwidth definition for the DPA with strict limits on efficiency and power output performance. To optimize the bandwidth performance, we introduced two factors, $\zeta$ and $\kappa$. They are the multiplying factors for the impedance at the combining node and the impedance seen by transistors, both defined at the center frequency. For the given three parameters of a transistor and the type of the combining network, an optimal pair of $\zeta$ and $\kappa$ can be determined. We presented a table that lists those values as a function of frequency. We also gave explicit formulas for all element values of the combining network. We showed that the higher power transistors of the same family can be used by a proper scaling of the combining network element values. We also presented a method to choose the post-matching network in order not to degrade the bandwidth performance.

If the package inductance, $L_s$, of the transistor is negligible, then it is possible

to list the optimal values only in terms of transistor output quality factor, $Q$, making this second table more general for applications in lower frequencies or in MMICs.

The tables can be used to determine the potential bandwidth performance of a DPA using transistors with a quality factor, $Q$. Alternatively, they can be used in choosing a proper transistor for a DPA with a given bandwidth goal. We gave example designs to demonstrate the use of both tables to find all element values.

Among the three different CN topologies studied, type II gives a good bandwidth performance in applications where the distributed components are not preferred because of their size. CN type III can be implemented easily at higher frequencies and with a slightly better performance compared to type II. CN type I should be preferred for its robustness if a wide bandwidth is not required and the size is not a problem.

A higher power version of the DPA with the same bandwidth can be implemented by scaling the transistors and the combining network element values, provided that a sufficiently wideband post-matching network is utilized to take care of the reduced combining node impedance.

Obviously, for the complete DPA design input matching, stabilization, and input unequal dividing network must be added. Due to the bandwidth limitation of the input side, the resulting bandwidth of the DPA will be somewhat smaller than predicted here.

Even though our transistor model is extremely simple, the results obtained from our model are very close to harmonic balance simulations using the complex nonlinear models of transistors. Hence our method is very useful if there is no available nonlinear model of the transistors in an MMIC application. One can easily extract $R_{opt}$, $C$ and $L_s$ from the measured load-pull data of the transistor. Those parameters are sufficient to design the output combining networks.

If the transistor has a vendor supplied model, the proposed circuit topology and calculated values from our method can be used as a good starting point for

further optimization in a harmonic balance simulator.

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# Appendix A

# Cosine Series Expansion of Eq. 2.13

We can expand Eq. 2.13 in a cosine series as

$$i_D = \left( A_0 + \sum_{n=1}^{\infty} A_n \cos(n\theta) \right) \cdot \left( k_0 + \sum_{n=1}^{N_e+1} [k_{n,R} \cos(n\theta) + k_{n,Q} \sin(n\theta)] \right) \quad \text{(A.1)}$$

where

$$A_0 = \frac{G_m(V_B - V_T)}{\pi} \left( \alpha_2 - \frac{\sin \alpha_2}{\cos \alpha_2} \right) \quad \text{(A.2)}$$

$$A_n = \frac{2G_m(V_B - V_T)}{\pi} \left[ \frac{\sin(n\alpha_2)}{n} - \frac{1}{\cos \alpha_2} \left( \frac{\sin((n-1)\alpha_2)}{2(n-1)} + \frac{\sin((n+1)\alpha_2)}{2(n+1)} \right) \right] \quad \text{(A.3)}$$

$$\alpha_2 = \cos^{-1} \left( \frac{-(V_B - V_T)}{V_{in}} \right) \quad \text{(A.4)}$$

and with $\mathbf{V_1}$=$V_1 e^{j\phi}$ [16]

$$k_0 = 1 - \frac{1}{2} \left( \frac{V_1}{2V_{DD}} \right)^{N_e} \binom{N_e}{N_e/2} \quad \text{(A.5)}$$

$$k_{2n,R} = -\left(\frac{V_1}{2V_{DD}}\right)^{N_e}\binom{N_e}{N_e/2-n}\cos(2n\phi) \tag{A.6}$$

$$k_{2n-1,R} = \left(\frac{V_1}{2V_{DD}}\right)^{N_e+1}\binom{N_e+1}{N_e/2+1-n} \cos((2n-1)\phi) \tag{A.7}$$

$$k_{2n,Q} = \left(\frac{V_1}{2V_{DD}}\right)^{N_e}\binom{N_e}{N_e/2-n}\sin(2n\phi) \tag{A.8}$$

$$k_{2n-1,Q} = -\left(\frac{V_1}{2V_{DD}}\right)^{N_e+1}\binom{N_e+1}{N_e/2+1-n} \sin((2n-1)\phi) \tag{A.9}$$

# Appendix B

# Smaller $Z_H$ Solution

If $Z_H$ value found in Eq. 3.13 is too high for implementation, one can use the following formulas giving a longer transmission line with a lower $Z_H$ value. For an inverter that inverts $rR_0$ to $R_0$ with $r < 1$, we have

$$\omega_0 C_i = \frac{-337.13r^3 + 725.94r^2 - 674.74r + 297.9}{100R_0} \tag{B.1}$$

$$x_i = \frac{300.95p^3 - 497.42p^2 + 427.76p - 1.718}{1000} \quad \text{with } Z_H = R_0 \tag{B.2}$$

where $p$ is given by Eq. 3.14.

# Appendix C

# Matlab Codes

The following codes are used to generate the results shown in this thesis:

## C.1 Doherty Power Amplifier Synthesis and Analysis

### C.1.1 Design and Center Frequency Analysis

```
% Program using the formulas of Alemdar & Atalar paper to ...
    calculate:
%  * The necessary input levels for desired power output ...
    backoff of a Doherty Amplifier
%  * Center Frequency Performance such as Efficiency, Pout, ...
    Currents
% The result is a file BOn.mat that will be used by ...
    DohertyFreqResp_m2.m calculating:
%  * Frequency Response Performance
% Please make sure 6 mat files are on the same directory:
%  * DohertyInit_m2.m
%  * DohertyFreqResp_m2.m
```

```
%  * DrainCurrent1.m
%  * DrainCurrent1m.m
%  * DrainCurrent3.m
%  * DrainCurrent3m.m
clear;close all;

% COMBINING NETWORK SELECTION...
    -----------------------------------------
ConvDo=0;
% 1 if conventional Doherty amplifier (Conv)
% 0 if two section TL (type I in paper)
% 8 if C-L-C inverter (type II in paper)
% 5 if C-TL-C inverter (type III in paper)
% 6 if C-TL(longer)-C inverter (type III in paper)

% OUTPUT MATCHING NETWORK SELECTION...
    ---------------------------------------
OMNNo=2;
% 1 if one section lambda/4 line (a) in paper
% 2 if two section lambda/4 lines (b) in paper
% 3 if one section CA-TL-CB (e) in paper
% 4 if two section CA-TL-CB (f) in paper
% 6 if one section C-L-C (c) in paper
% 7 if two section C-L-C (d) in paper

fN=1; % Center frequency in GHz
zeta=3; % First scaling parameter
kappa=1; % Second scaling parameter
% -------------------------------------------------
% TRANSISTOR PARAMETERS

No=15; % order of knee function approximation (odd)
for n=1:(No+1)/2
     nchko(n)=nchoosek(No,(No+1)/2-n);
end

Ne=14; % order of knee function approximation (even)
for n=0:Ne/2
    nchke(n+1)=nchoosek(Ne,Ne/2-n);
end
```

```
47
48 VT=-3;         % threshold voltage of RF transistor
49 VDD=28;        % VDD voltage of RF transistor
50 Gm=0.6;        % transconductance of RF transistor
51 Ropt=26.68;    % optimal drain impedance of main amp
52 Roptp=25.75;   % optimal drain resistance of peaking amp
53 Ipmax=4.427;   %4.427
54 VBm=VT+0.001; % bias voltage of carrier amplifier (note: a ...
       small shift value is needed for Class B)
55 VBp=-5.6;      % bias voltage of peaking amplifier (Class-C)
56 C=1.84e-12;    % drain capacitance 1.84e-12;
57 Ls=0.26e-9;    % serial package inductance  0.26e-9;
58 Lsh=14e-9;     % shunt inductance for tuning;
59 Ropt=26.6;     % to be used with types II and III in paper
60 Roptp=25.75;   % to be used with types II and III in paper
61 % use Ropt given in Table in paper for type I
62 Ropt=26;
63 Roptp=Ropt;    %For simplicity
64
65 w0=2*pi*fN*1e9;
66 Q=Ropt/(w0*Lsh);
67 ZOUT=50; % Load impedance at the output of amp
68
69 alpha=1/sqrt(5); % input divider multiplier for main amplifier
70 beta=sqrt(4)/sqrt(5); % input divider multiplier for peaking ...
       amplifier
71
72 % END OF TRANSISTOR PARAMETERS
73 % ------------------------------------------------
74
75 %------------------CALCULTIONS BEGIN...
       ---------------------------------------
76
77 nw=300; % number of input steps of input excitation for ...
       interpolation
78 BOmin=-15; % Minimum output level in dBs
79 BOmax=0; % Maximum output level in dBs
80 NoOfSteps=2; % number of  backoff steps
81 BackOffSmall=0; % defines the largest power (smallest backoff ...
       in dB)
```

```
82 StepSize=6; % backoff step size in dB
83
84 w=w0; % frequency of evaluation
85 Zh=100; % maximum TL impedance
86
87 % Variables Defined
88 L=1000;
89 L1=0;L2=0;L3=0;
90 C1=0;C2=0;C3=0;C4=0;C_offset=0;L_offset=0;
91 CA=0;CB=0;CC=0;CD=0;LA=0;LB=0;
92 x=0;x1=0;y1=0;y2=0;
93 y=0.25; % by default lambda/4
94 ZSh=100000;
95 ySh=0.25;
96
97 Z5=ZOUT;
98 Z6=ZOUT;
99
100 %---COMBINING NETWORK CALCULATIONS BEGIN...
    ------------------------------------
101
102 switch ConvDo
103     case 1 % conventional Doherty amplifier (Conv)
104         ConvDoh=1;
105         Zcomb=zeta/2*Ropt;
106         kappa=zeta*Ropt/Roptp;
107         Z2=sqrt(zeta*kappa)*Ropt;
108         Z3=0;
109         Z4=0;
110
111     case 0 % if two section TL (type I in paper)
112         ConvDoh=0;
113         Zcomb=zeta/2*Ropt;
114         Z2=sqrt(zeta*kappa)*Ropt;
115         Z3=kappa^0.75*zeta^0.25*Roptp^0.75*Ropt^0.25;
116         Z4=kappa^0.25*zeta^0.75*Roptp^0.25*Ropt^0.75;
117
118     case 5 % if C-TL-C inverter (type III in paper)
119         ConvDoh=0;
120         Zcomb=zeta/2*Ropt;
```

```
121         r=kappa/zeta;
122         Z2=1.4*zeta*Ropt;
123         C1=(-53*r^3+207*r^2-324*r+240)/(100*zeta*Ropt*w0);
124         p=(sqrt(r)-w0*Ls/(zeta*Ropt))^2;
125         x=(18.0*p^3-52.8*p^2+132*p+28.8)/(1000);
126         if(C1>C)
127             C2=C1-C; % extra cap needed in parallel with C
128             L1=100; % no shunt inductance needed
129         else
130             C2=0; % no extra cap needed\
131             L1=1/(w0^2*C-w0^2*C1); % L1 is the shunt ...
                    inductance to partially cancel CC
132         end
133         Z4=zeta*Ropt;
134         r=kappa*Roptp/Z4;
135         Z3=Z2;
136         C3=(-53*r^3+207*r^2-324*r+240)/(100*zeta*Ropt*w0);
137         p=(sqrt(r)-w0*Ls/(zeta*Ropt))^2;
138         x1=(18.0*p^3-52.8*p^2+132*p+28.8)/(1000);
139         if(C3>C)
140             C4=C3-C; % extra cap in parallel
141             L3=100000;
142         else
143             C4=0;% no extra cap
144             L3=1/(w0^2*C-w0^2*C3);
145         end
146         Lsh=1;
147
148     case 6 % if C-TL(longer)-C inverter (type III in paper)
149         ConvDoh=0;
150         Zcomb=zeta/2*Ropt;
151         r=kappa/zeta;
152         x=(300.95*r^3-497.42*r^2+427.76*r-1.718)/(1000);
153         Z2=zeta*Ropt;
154         C1=(-337.13*r^3+725.94*r^2-674.74*r+297.9)/(100*zeta*...
                Ropt*w0);
155         if(C1>C)
156             C2=C1-C; % extra cap needed in parallel with C
157             L1=100000; % no shunt inductance needed
158         else
```

```
159             C2=0; % no extra cap needed\
160             L1=1/(w0^2*C-w0^2*C1); % L1 is the shunt ...
                    inductance to partially cancel CC
161         end
162         Z4=zeta*Ropt;
163         r=kappa*Roptp/Z4;
164         x1=(300.95*r^3-497.42*r^2+427.76*r-1.718)/(1000);
165         Z3=Z2;
166         C3=(-337.13*r^3+725.94*r^2-674.74*r+297.9)/(100*zeta*...
                Ropt*w0);
167         if(C3>C)
168             C4=C3-C; % extra cap in parallel
169             L3=100000;
170         else
171             C4=0;% no extra cap
172             L3=1/(w0^2*C-w0^2*C3);
173         end
174         Lsh=1;
175
176     case 8 %  if C-L-C inverter (type II in paper)
177         ConvDoh=0;
178         % zeta=3;
179         Zcomb=zeta/2*Ropt;
180         Z2=0;
181         L=sqrt(zeta*kappa)*Ropt/w0;
182         C1=1/(w0^2*L);
183         L=L-Ls; % since Ls is already there
184         if(C1>C)
185             C2=C1-C; % extra cap needed in parallel with C
186             L1=100000; % no shunt inductance needed
187         else
188             C2=0; % no extra cap needed\
189             L1=1/(w0^2*C-w0^2*C1); % L1 is the shunt ...
                    inductance to partially cancel CC
190         end
191         Z3=0;
192         Z4=zeta*Ropt;
193         L2=sqrt(zeta*kappa*Ropt*Roptp)/w0;
194         C3=1/(w0^2*L2);
195         L2=L2-Ls;
```

```
196         if(C3>C)
197             C4=C3-C; % extra cap in parallel
198             L3=100000;
199         else
200             C4=0;% no extra cap
201             L3=1/(w0^2*C-w0^2*C3);
202         end
203         %Offset line replacement CLC inverter
204         L_offset = Roptp*zeta/w0;
205         C_offset = 1/(w0*Roptp*zeta);
206         Lsh=1; % to eliminate
207 end
208
209 %---COMBINING NETWORK CALCULATIONS END...
        ------------------------------------
210
211 %---OUTPUT COMBINING NETWORK CALCULATIONS BEGIN...
    ----------------------------
212 switch OMNNo
213     case 1
214         Z5=sqrt(Zcomb*ZOUT);
215         Z6=ZOUT;
216         y1=0.25;
217         y2=0;
218
219     case 2
220         Z5=Zcomb^0.75*ZOUT^0.25;
221         Z6=Zcomb^0.25*ZOUT^0.75;
222         y1=0.25;
223         y2=0.25;
224
225     case 3
226         ZLBar=Zcomb/ZOUT; % normalized combining resistance
227         y1=(9.56*ZLBar^3-43.2*ZLBar^2+83.6*ZLBar+34.7)/(1000);
228         %y1=Z5/(2*pi*Zh);
229         CA=(1.7*ZLBar^3-7.08*ZLBar^2+10.9*ZLBar-1.09)/(w0...
                *1000);
230         CD=0;
231         CB=(-10.7*ZLBar^3+44.4*ZLBar^2-74.4*ZLBar+45)/(w0...
                *1000);
```

```
232         CC=0;
233         y2=0;
234         Z5=70;
235         Z6=ZOUT;
236
237     case 4
238         Z5=Zcomb^0.75*ZOUT^0.25;
239         Zmid=Z5^2/Zcomb;
240         ZLBar=Zmid/ZOUT;
241         Z6=70;
242         y2=(9.56*ZLBar^3-43.2*ZLBar^2+83.6*ZLBar+34.7)/(1000);
243         CC=(1.7*ZLBar^3-7.08*ZLBar^2+10.9*ZLBar-1.09)/(w0...
                *1000);
244         CD=(-10.7*ZLBar^3+44.4*ZLBar^2-74.4*ZLBar+45)/(w0...
                *1000);
245         y1=y2;
246         Z5=Zmid/ZOUT*70;
247         CA=CC*50/Zmid;
248         CB=CD*50/Zmid;
249
250     case 6
251         LA=sqrt(ZOUT*Zcomb)/w0;
252         CA=1/(LA*w0^2);
253         CB=CA;
254
255     case 7
256         LA=(ZOUT^0.25 * Zcomb^0.75)/w0;
257         LB=(ZOUT^0.75 * Zcomb^0.25)/w0;
258         CA=1/(LA*w0^2);
259         CB=CA;
260         CC=1/(LB*w0^2);
261         CD=CC;
262 end
263 %---OUTPUT COMBINING NETWORK CALCULATIONS END...
        ------------------------------
264
265
266 % initialize matrices to reserve space
267 POUT=zeros(1,nw);
```

```
GAIN=POUT;VDSm=POUT;VDSp=POUT;IDSm=POUT;IDSp=POUT;I0m=POUT;I0p...
    =POUT;BO=POUT;

myfun=@sA1;
options = optimoptions('fsolve','Display','none','...
    OptimalityTolerance',1e-7);


switch ConvDo
    case 1  %if conventional Doherty amplifier (Conv)

    Ap=[1 0; 1i*w*C 1]*[1 1i*w*Ls; 0 1]*[1 0; 1/(1i*w*Lsh) 1];
    Am=[1 0; 1i*w*C 1]*[1 1i*w*Ls; 0 1]*[1 0; 1/(1i*w*Lsh) ...
        1]*[cos(2*y*pi*w/w0) 1i*Z2*sin(2*y*pi*w/w0); 1i/Z2*sin...
        (2*y*pi*w/w0) cos(2*y*pi*w/w0)];
    case 0  %if two section TL (type I in paper)

    Am=[1 0; 1i*w*C 1]*[1 1i*w*Ls; 0 1]*[1 0; 1/(1i*w*Lsh) ...
        1]*[cos(pi/2*w/w0) 1i*Z2*sin(pi/2*w/w0); 1i/Z2*sin(pi...
        /2*w/w0) cos(pi/2*w/w0)];
    Ap=[1 0; 1i*w*C 1]*[1 1i*w*Ls; 0 1]*[1 0; 1/(1i*w*Lsh) ...
        1]*[cos(pi/2*w/w0) 1i*Z3*sin(pi/2*w/w0); 1i/Z3*sin(pi...
        /2*w/w0) cos(pi/2*w/w0)]*[cos(2*y*pi*w/w0) 1i*Z4*sin(2*...
        y*pi*w/w0); 1i/Z4*sin(2*y*pi*w/w0) cos(2*y*pi*w/w0)];
     case 8 %if C-L-C inverter (type II in paper)

    Ap=[1 0; 1i*w*C 1]*[1 1i*w*Ls; 0 1]*[1 0; 1/(1i*w*Lsh) ...
        1]*[1 0; 1i*w*C4 1]*[1 0; -1i/(w*L3) 1]*[1 1i*w*L2; 0 ...
        1]*[1 0; 1i*w*C3 1]*[1 0; 1i*w*C_offset 1]*[1 1i*w*...
        L_offset; 0 1]*[1 0; 1i*w*C_offset 1];
    Am=[1 0; 1i*w*C 1]*[1 1i*w*Ls; 0 1]*[1 0; 1/(1i*w*Lsh) ...
        1]*[1 0; 1i*w*C2 1]*[1 0; -1i/(w*L1) 1]*[1 1i*w*L; 0 ...
        1]*[1 0; 1i*w*C1 1];
    case {5,6} %if C-TL-C inverter (type III in paper)

```

```
289     Ap=[1 0; 1i*w*C 1]*[1 1i*w*Ls; 0 1]*[1 0; 1/(1i*w*Lsh) ...
            1]*[1 0; 1i*w*C4 1]*[1 0; -1i/(w*L3) 1]*[cos(x1*2*pi*w/...
            w0) 1i*Z3*sin(x1*2*pi*w/w0); 1i/Z3*sin(x1*2*pi*w/w0) ...
            cos(x1*2*pi*w/w0)]*[1 0; 1i*w*C3 1]*[cos(2*y*pi*w/w0) 1...
            i*Z4*sin(2*y*pi*w/w0);1i/Z4*sin(2*y*pi*w/w0) cos(2*y*pi...
            *w/w0)];
290     Am=[1 0; 1i*w*C 1]*[1 1i*w*Ls; 0 1]*[1 0; 1/(1i*w*Lsh) ...
            1]*[1 0; 1i*w*C2 1]*[1 0; -1i/(w*L1) 1]*[cos(x*2*pi*w/...
            w0) 1i*Z2*sin(x*2*pi*w/w0); 1i/Z2*sin(x*2*pi*w/w0) cos(...
            x*2*pi*w/w0)]*[1 0; 1i*w*C1 1];
291
292 end
293 Zout=ZOUT; % corresponding normalized load impedance of ...
        Doherty
294
295
296 AOMN=...
297     ...%shunt component 1
298     [1 0; 1i*w*CA 1]*...
299     ...%series component 1
300     [cos(y1*2*pi*w/w0) 1i*Z5*sin(y1*2*pi*w/w0); 1i/Z5*sin(y1...
            *2*pi*w/w0) cos(y1*2*pi*w/w0)]*...
301     [1 1i*w*LA; 0 1]*...
302     ...%shunt component 2
303     [1 0; 1i*w*(CB+CC) 1]*...
304     ...%series component 2
305     [cos(y2*2*pi*w/w0) 1i*Z6*sin(y2*2*pi*w/w0); 1i/Z6*sin(y2...
            *2*pi*w/w0) cos(y2*2*pi*w/w0)]*...
306     [1 1i*w*LB; 0 1]*...
307     ...%shunt component 3
308     [1 0; 1i*w*CD 1];
309 ZL=(AOMN(1,1)*ZOUT+AOMN(1,2))/(AOMN(2,1)*ZOUT+AOMN(2,2));
310
311
312 % find the coefficients to be used later for all ZL values
313 Den=Am(2,2)*Ap(2,2)+(Am(2,1)*Ap(2,2)+Am(2,2)*Ap(2,1))*ZL;
314 A11=(Am(1,2)*Ap(2,2)+(Am(1,1)*Ap(2,2)+Am(1,2)*Ap(2,1))*ZL)/Den...
        ;
315 A12=((Am(1,1)*Am(2,2)-Am(1,2)*Am(2,1))*ZL)/Den;
```

```
316 A22=(Ap(1,2)*Am(2,2)+(Ap(1,1)*Am(2,2)+Ap(1,2)*Am(2,1))*ZL)/Den...
        ;
317 A21=((Ap(1,1)*Ap(2,2)-Ap(1,2)*Ap(2,1))*ZL)/Den;
318 B11=ZL*Ap(2,2)/Den;
319 B12=ZL*Am(2,2)/Den;
320
321
322 IDQm=Gm*(VBm-VT);
323 IDQp=Gm*(VBp-VT);
324
325 il=BOmin;
326 ilstep=(BOmax-BOmin)/(nw-1);
327 % initial estimate of solution
328 VDSi=[(1-ConvDoh+ConvDoh*1i)*0.5;((1-ConvDoh)*1i+ConvDoh)*0.5...
        ];
329
330 for iw=1:nw
331     Vin=Ipmax/Gm*10^(il/20);
332     BO(iw)=il;
333     il=il+ilstep;
334     Vinm=Vin*alpha;
335     Vinp=Vin*beta;
336
337     Ipm=Gm*(Vinm+VBm-VT);
338     Ipp=Gm*(Vinp+VBp-VT);
339
340
341
342     AT=[A11 A12;A21 A22];
343     fun=@(VDS) myfun(Ipm,Ipp,IDQm,IDQp,VDS,No,nchko,Ne,nchke,...
            AT,VDD,ConvDoh,y);
344     [VDS,FVAL,EXITFLAG]=fsolve(fun,VDSi,options); % find the ...
            VDS value for these conditions
345     if max(abs(FVAL))<1e-4
346     VDSm(1,iw)=VDS(1);
347     VDSp(1,iw)=VDS(2);
348     VDSi=VDS;
349     else
350     VDSm(1,iw)=VDSi(1);
351     VDSp(1,iw)=VDSi(2);
```

```
352      end
353
354  I0m(1,iw)=DrainCurrent1m(Ipm,IDQm,((1-ConvDoh)*1i+ConvDoh)*VDS...
         (1),No,nchko);     % phase shift needed if ConvDoh=0
355  I0m(1,iw)=(I0m(1,iw)+DrainCurrent1(Ipm,IDQm,((1-ConvDoh)*1i+...
         ConvDoh)*VDS(1),Ne))/2;     % phase shift needed if ConvDoh...
         =0
356
357  I0p(1,iw)=DrainCurrent1m(Ipp,IDQp,(1-ConvDoh+ConvDoh*1i)*VDS...
         (2),No,nchko); % no phase shift needed
358  I0p(1,iw)=(I0p(1,iw)+DrainCurrent1(Ipp,IDQp,(1-ConvDoh+ConvDoh...
         *1i)*VDS(2),Ne))/2; % no phase shift needed
359
360  IDSm(1,iw)=(ConvDoh-(1-ConvDoh)*1i)*DrainCurrent3m(Ipm,IDQm...
         ,((1-ConvDoh)*1i+ConvDoh)*VDS(1),No,nchko); % current of ...
         main trans.
361  IDSm(1,iw)=(IDSm(1,iw)+(ConvDoh-(1-ConvDoh)*1i)*DrainCurrent3(...
         Ipm,IDQm,((1-ConvDoh)*1i+ConvDoh)*VDS(1),Ne,nchke))/2; % ...
         current of main trans.
362
363  IDSp(1,iw)=(-ConvDoh*1i+1-ConvDoh)*DrainCurrent3m(Ipp,IDQp,(1-...
         ConvDoh+ConvDoh*1i)*VDS(2),No,nchko); % current of peaking ...
         trans.
364  IDSp(1,iw)=(IDSp(1,iw)+(-ConvDoh*1i+1-ConvDoh)*DrainCurrent3(...
         Ipp,IDQp,(1-ConvDoh+ConvDoh*1i)*VDS(2),No,nchko))/2; % ...
         current of peaking trans.
365
366
367  end
368
369  VL=B11*IDSm+B12*IDSp; % voltage at the combining node
370  POUT=1/2*real((VL).*conj(VL./ZL)); % output power in W
371  EFF=POUT./((I0m+I0p)*VDD); % efficiency
372
373  PDB=10*log10(POUT)+30; % output power in dBm
374
375  figure(2)
376  subplot(2,2,1)
377  hold off
378  plot(BO,PDB,'-','LineWidth',2,'Color','blue')
```

```
379 hold on
380 grid on
381 xlabel('Output Backoff (dB)')
382 ylabel('P_{out} (dBm)')
383 axis([BOmin,BOmax,25,45]);
384
385 subplot(2,2,2)
386 hold off
387 plot(BO,EFF,'-','LineWidth',2,'Color','blue')
388 hold on
389 grid on
390 ylabel('\eta')
391 xlabel('Output Backoff (dB)')
392 axis([BOmin,BOmax,0.,0.8]);
393
394 subplot(2,2,3)
395 hold off
396 plot(BO,I0m)
397 hold on
398 plot(BO,I0p)
399 grid on
400 ylabel('Main and Peak. Currents')
401 xlabel('Output Backoff (dB)')
402
403 axis([BOmin,BOmax,0.,0.7]);
404
405 for ii=1:NoOfSteps
406     BOn(ii)=interp1(PDB,BO,PDB(nw)-BackOffSmall-StepSize*(...
        NoOfSteps-1)+StepSize*(ii-1)); % 2dB steps
407 end
408 % save the results in BOn.mat file for use later
409 save('BOn.mat','BOn','NoOfSteps','zeta','kappa','nchko','nchke...
    ','C','L','Ls','Lsh','Z2','Z3','ZSh','x','x1','y','y1','y2'...
    ,'ySh','CA','CB','CC','CD','Z4','Z5','Z6','C1','C2','C3','...
    C4','L1','L2','L3','VT','VDD','Gm','Q','Ropt','Roptp','ZOUT...
    ','No','Ne','VBm','VBp','alpha','beta','Ipmax','ConvDo','...
    ConvDoh','fN','C_offset','L_offset','CA','LA','LB');
410 DohertyFreqResp_m2
411
412 % Nonlinear function to be solved (find the zero)
```

```
413 function f=sA1(Ipm,Ipp,IDQm,IDQp,VDS,No,nchko,Ne,nchke,AT,VDD,...
        ConvDoh,y)
414
415 IDSm=(ConvDoh+(1-ConvDoh)*exp(-1i*2*y*pi))*DrainCurrent3m(Ipm,...
        IDQm,((1-ConvDoh)*exp(1i*2*y*pi)+ConvDoh)*VDS(1),No,nchko);
416 IDSm=(IDSm+(ConvDoh+(1-ConvDoh)*exp(-1i*2*y*pi))*DrainCurrent3...
        (Ipm,IDQm,((1-ConvDoh)*exp(1i*2*y*pi)+ConvDoh)*VDS(1),Ne,...
        nchke))/2;
417
418 IDSp=(-ConvDoh*1i+1-ConvDoh)*DrainCurrent3m(Ipp,IDQp,(1-...
        ConvDoh+ConvDoh*1i)*VDS(2),No,nchko);
419 IDSp=(IDSp+(-ConvDoh*1i+1-ConvDoh)*DrainCurrent3(Ipp,IDQp,(1-...
        ConvDoh+ConvDoh*1i)*VDS(2),Ne,nchke))/2;
420
421
422 f=VDD*VDS-AT*[IDSm;IDSp]; % vector to be zeroed
423 end
```

### C.1.2 Frequency Response Analysis

```
% program to find  the frequency response of a Doherty ...
    amplifier
% with predetermined output backoff levels
% Enter the parameters in DohertyInit.m and run that program ...
    first to
% generate BOn.mat, which will be used as input to this ...
    program
% Using the notation of Alemdar & Atalar paper
% Using the new odd+even model
clear


tic
load('BOn.mat')
wN=fN*2*pi*1e9;

% ------------------------------------------
% Select Start Stop Frequency
wmax=1.2*wN; %Stop Frequency
wmin=0.8*wN; %Start Frequency

nw=61; % number of frequency steps of input excitation
% end of input parameters
% ------------------------------------------

w=wmin:(wmax-wmin)/(nw-1):wmax;
fn=w/(2*pi*1e9); % the actual frequencies in GHz

% initialize matrices to reserve space
POUT=zeros(1,nw);
GAIN=POUT;VDSm=POUT;VDSp=POUT;IDSm=POUT;IDSp=POUT;
I0m=POUT;I0p=POUT;Zm=POUT;Zp=POUT;ZL=POUT;
PDB=zeros(NoOfSteps,nw);
EFF=POUT;
Am=zeros(2,2,nw);
Ap=Am;
AOMN=Ap;
```

```
ZL1=zeros(1,1,nw);

myfun=@sA1;
% options for nonlinear solver
options = optimoptions('fsolve','Display','none','...
    OptimalityTolerance',1e-7);
ig=1;
IDQm=Gm*(VBm-VT);
IDQp=Gm*(VBp-VT);
figure(4)
subplot(1,2,1)
hold off
subplot(1,2,2)
hold off
TotPow=0;
TotEff=0;

stepNo=0;
for ii=1:NoOfSteps
    Vin=Ipmax/Gm*10^(BOn(ii)/20);
    Vinm=Vin*alpha;
    Vinp=Vin*beta;

    Ipm=Gm*(Vinm+VBm-VT);
    Ipp=Gm*(Vinp+VBp-VT);

    mFVAL=0;
    % find the ABCD matrices
    % ABCDm for main
    % ABCDp for peaking
    for iw=1:nw
    switch ConvDo
    case 1  %if conventional Doherty amplifier (Conv)
            Ap(:,:,iw)=[1 0; 1i*w(iw)*C 1]*[1 1i*w(iw)*Ls; 0 ...
                1]*[1 0;1/(1i*w(iw)*Lsh) 1];
            Am(:,:,iw)=[1 0; 1i*w(iw)*C 1]*[1 1i*w(iw)*Ls; 0 ...
                1]*[1 0;1/(1i*w(iw)*Lsh) 1]*[cos(pi/2*w(iw)/wN)...
                 1i*Z2*sin(pi/2*w(iw)/wN);1i/Z2*sin(pi/2*w(iw)/...
                wN) cos(pi/2*w(iw)/wN)];
    case 0  %if two section TL (type I in paper)
```

```
70              Am(:,:,iw)=[1 0; 1i*w(iw)*C 1]*[1 1i*w(iw)*Ls; 0 ...
                    1]*[1 0;1/(1i*w(iw)*Lsh) 1]*[cos(pi/2*w(iw)/wN)...
                     1i*Z2*sin(pi/2*w(iw)/wN);1i/Z2*sin(pi/2*w(iw)/...
                    wN) cos(pi/2*w(iw)/wN)];
71              Ap(:,:,iw)=[1 0; 1i*w(iw)*C 1]*[1 1i*w(iw)*Ls; 0 ...
                    1]*[1 0;1/(1i*w(iw)*Lsh) 1]*[cos(pi/2*w(iw)/wN)...
                     1i*Z3*sin(pi/2*w(iw)/wN);1i/Z3*sin(pi/2*w(iw)/...
                    wN) cos(pi/2*w(iw)/wN)]*[cos(pi/2*w(iw)/wN) 1i*...
                    Z4*sin(pi/2*w(iw)/wN);1i/Z4*sin(pi/2*w(iw)/wN) ...
                    cos(pi/2*w(iw)/wN)];
72      case 8  %if C-L-C inverter (type II in paper)
73              Ap(:,:,iw)=[1 0; 1i*w(iw)*C 1]*[1 1i*w(iw)*Ls; 0 ...
                    1]*[1 0;1/(1i*w(iw)*Lsh) 1]*[1 0; 1i*w(iw)*C4 ...
                    1]*[1 0; -1i/(w(iw)*L3) 1]*[1 1i*w(iw)*L2; 0 ...
                    1]*[1 0; 1i*w(iw)*C3 1]*[1 0; 1i*w(iw)*C_offset...
                     1]*[1 1i*w(iw)*L_offset; 0 1]*[1 0; 1i*w(iw)*...
                    C_offset 1];
74              Am(:,:,iw)=[1 0; 1i*w(iw)*C 1]*[1 1i*w(iw)*Ls; 0 ...
                    1]*[1 0;1/(1i*w(iw)*Lsh) 1]*[1 0; 1i*w(iw)*C2 ...
                    1]*[1 0; -1i/(w(iw)*L1) 1]*[1 1i*w(iw)*L; 0 ...
                    1]*[1 0; 1i*w(iw)*C1 1];
75      case {5,6} %if C-TL-C inverter (type III in paper)
76              Ap(:,:,iw)=[1 0; 1i*w(iw)*C 1]*[1 1i*w(iw)*Ls; 0 ...
                    1]*[1 0;1/(1i*w(iw)*Lsh) 1]*[1 0; 1i*w(iw)*C4 ...
                    1]*[1 0; -1i/(w(iw)*L3) 1]*[cos(x1*2*pi*w(iw)/...
                    wN) 1i*Z3*sin(x1*2*pi*w(iw)/wN); 1i/Z3*sin(x1...
                    *2*pi*w(iw)/wN) cos(x1*2*pi*w(iw)/wN)]*[1 0; 1i...
                    *w(iw)*C3 1]*[cos(2*y*pi*w(iw)/wN) 1i*Z4*sin(2*...
                    y*pi*w(iw)/wN);1i/Z4*sin(2*y*pi*w(iw)/wN) cos...
                    (2*y*pi*w(iw)/wN)];
77              Am(:,:,iw)=[1 0; 1i*w(iw)*C 1]*[1 1i*w(iw)*Ls; 0 ...
                    1]*[1 0;1/(1i*w(iw)*Lsh) 1]*[1 0; 1i*w(iw)*C2 ...
                    1]*[1 0; -1i/(w(iw)*L1) 1]*[cos(x*2*pi*w(iw)/wN...
                    ) 1i*Z2*sin(x*2*pi*w(iw)/wN); 1i/Z2*sin(x*2*pi*...
                    w(iw)/wN) cos(x*2*pi*w(iw)/wN)]*[1 0; 1i*w(iw)*...
                    C1 1];
78      end
79
80
81
```

```
82
83      Zout=ZOUT; % corresponding normalized load impedance of ...
            Doherty
84
85      AOMN(:,:,iw)=...
86          ...%shunt component 1
87          [1 0; 1i*w(iw)*CA 1]*...
88          ...%series component 1
89          [cos(y1*2*pi*w(iw)/wN) 1i*Z5*sin(y1*2*pi*w(iw)/wN); 1i...
                /Z5*sin(y1*2*pi*w(iw)/wN) cos(y1*2*pi*w(iw)/wN)]*...
                ...
90          [1 1i*w(iw)*LA; 0 1]*...
91          ...%shunt component 2
92          [1 0; 1i*w(iw)*(CB+CC) 1]*...
93          ...%series component 2
94          [cos(y2*2*pi*w(iw)/wN) 1i*Z6*sin(y2*2*pi*w(iw)/wN); 1i...
                /Z6*sin(y2*2*pi*w(iw)/wN) cos(y2*2*pi*w(iw)/wN)]*...
                ...
95          [1 1i*w(iw)*LB; 0 1]*...
96          ...%shunt component 3
97          [1 0; 1i*w(iw)*CD 1];
98
99      ZL1(1,1,iw)=(AOMN(1,1,iw)*ZOUT+AOMN(1,2,iw))/(AOMN(2,1,iw)...
            *ZOUT+AOMN(2,2,iw));
100     end
101     ZL(1,:)=ZL1(1,1,:);
102
103
104 % find the coefficients to be used later for all ZL values
105     Den=Am(2,1,:).*Ap(2,2,:)+Am(2,2,:).*Ap(2,1,:);
106     Den(1,1,:)=Am(2,2,:).*Ap(2,2,:)+Den(1,1,:).*ZL1(1,1,:);
107     A11=(Am(1,2,:).*Ap(2,2,:)+(Am(1,1,:).*Ap(2,2,:)+Am(1,2,:)....
            *Ap(2,1,:)).*ZL1(1,1,:)./Den(1,1,:);
108     A12=((Am(1,1,:).*Am(2,2,:)-Am(1,2,:).*Am(2,1,:)).*ZL1...
            (1,1,:))./Den(1,1,:);
109     A22=(Ap(1,2,:).*Am(2,2,:)+(Ap(1,1,:).*Am(2,2,:)+Ap(1,2,:)....
            *Am(2,1,:)).*ZL1(1,1,:))./Den(1,1,:);
110     A21=((Ap(1,1,:).*Ap(2,2,:)-Ap(1,2,:).*Ap(2,1,:)).*ZL1...
            (1,1,:))./Den(1,1,:);
111     B11=ZL1(1,1,:).*Ap(2,2,:)./Den(1,1,:);
```

```
112     B12=ZL1(1,1,:).*Am(2,2,:)./Den(1,1,:);
113     B11a(1,:)=B11(1,1,:);
114     B12a(1,:)=B12(1,1,:);
115
116
117     VDSi=[0.2177-1i*0.9535;0.6511-1i*0.1119];
118     options=optimoptions('fsolve','Display','off','...
            MaxIterations',9000,'Algorithm','levenberg-marquardt','...
            StepTolerance',1e-9,'MaxFunctionEvaluations',90000,'...
            FunctionTolerance',1e-7);
119
120     for ip=1:nw
121         AT=[A11(1,1,ip) A12(1,1,ip);A21(1,1,ip) A22(1,1,ip)];
122         wp=w(ip)/wN;
123
124         itercnt=1;
125         COND=true;
126         while COND
127         fun=@(VDS) myfun(Ipm,Ipp,IDQm,IDQp,VDS,No,nchko,Ne,...
                nchke,AT,wp,VDD,ConvDoh,y);
128         [VDS,FVAL,EXITFLAG]=fsolve(fun,VDSi,options); % find ...
                the VDS value for these conditions
129
130         COND=(EXITFLAG<1);
131             if(EXITFLAG>0)
132         % if max(abs(FVAL))<1e-6
133                 VDSm(1,ip)=VDS(1);
134                 VDSp(1,ip)=VDS(2);
135                 VDSi=VDS;
136             else
137                 VDSi(1,1)=VDSi(1,1)+0.2*(rand(1,1)*2-1+1i*(...
                        rand(1,1)*2-1));
138                 VDSi(2,1)=VDSi(2,1)+0.2*(rand(1,1)*2-1+1i*(...
                        rand(1,1)*2-1));
139                 itercnt=itercnt+1;
140                 if(itercnt>1000)
141                     itercnt=1;
142                 end
143             end
144         end
```

```
145
146         % DC currents of main and peaking amplilfiers
147         I0m(1,ip)=DrainCurrent1m(Ipm,IDQm,((1-ConvDoh)*exp(1i*...
                pi/2*w(ip)/wN)+ConvDoh)*VDS(1),No,nchko);     % no ...
                phase shift needed
148         I0m(1,ip)=(I0m(1,ip)+DrainCurrent1(Ipm,IDQm,((1-...
                ConvDoh)*exp(1i*pi/2*w(ip)/wN)+ConvDoh)*VDS(1),Ne))...
                /2;     % no phase shift needed
149
150         I0p(1,ip)=DrainCurrent1m(Ipp,IDQp,(1-ConvDoh+ConvDoh*...
                exp(1i*pi/2*w(ip)/wN))*VDS(2),No,nchko); % phase ...
                shift VDS(2) as if it is cosine excited
151         I0p(1,ip)=(I0p(1,ip)+DrainCurrent1(Ipp,IDQp,(1-ConvDoh...
                +ConvDoh*exp(1i*pi/2*w(ip)/wN))*VDS(2),Ne))/2; % ...
                phase shift VDS(2) as if it is cosine excited
152
153         % fundamental currents of main and peaking amplifiers
154         IDSm(1,ip)=(ConvDoh+(1-ConvDoh)*exp(-1i*pi/2*w(ip)/wN)...
                )*DrainCurrent3m(Ipm,IDQm,((1-ConvDoh)*exp(1i*pi/2*...
                w(ip)/wN)+ConvDoh)*VDS(1),No,nchko); % current of ...
                main trans.
155         IDSm(1,ip)=(IDSm(1,ip)+(ConvDoh+(1-ConvDoh)*exp(-1i*pi...
                /2*w(ip)/wN))*DrainCurrent3(Ipm,IDQm,((1-ConvDoh)*...
                exp(1i*pi/2*w(ip)/wN)+ConvDoh)*VDS(1),Ne,nchke))/2;...
                 % current of main trans.
156
157         IDSp(1,ip)=(ConvDoh*exp(-1i*pi/2*w(ip)/wN)+1-ConvDoh)*...
                DrainCurrent3m(Ipp,IDQp,(1-ConvDoh+ConvDoh*exp(1i*...
                pi/2*w(ip)/wN))*VDS(2),No,nchko); % current of ...
                peaking trans.
158         IDSp(1,ip)=(IDSp(1,ip)+(ConvDoh*exp(-1i*pi/2*w(ip)/wN)...
                +1-ConvDoh)*DrainCurrent3(Ipp,IDQp,(1-ConvDoh+...
                ConvDoh*exp(1i*pi/2*w(ip)/wN))*VDS(2),Ne,nchke))/2;...
                 % current of peaking trans.
159
160
161         Zm(1,ip)=VDD*VDSm(1,ip)/IDSm(1,ip);
162         Zp(1,ip)=VDD*VDSp(1,ip)/IDSp(1,ip);
163
164     end
```

```
165
166     VL=B11a.*IDSm+B12a.*IDSp;
167     POUT=1/2*real((VL).*conj(VL./ZL));
168     EFF(ii,:)=POUT./((I0m+I0p)*VDD);
169
170
171     PDB(ii,:)=10*log10(POUT)+30;
172     toc
173     stepNo=stepNo+1;
174     figure(4)
175
176     subplot(1,2,1)
177     h=plot(fn,PDB,'LineWidth',2);
178     %hold on
179
180      grid on
181      xlabel('f (GHz)')
182      ylabel('P_{out} (dBm)')
183     if(wmin<wmax)
184         axis([wmin/(2*pi*1e9),wmax/(2*pi*1e9),35,45]);
185     else
186         axis([wmax/(2*pi*1e9),wmin/(2*pi*1e9),35,45]);
187     end
188
189     subplot(1,2,2)
190     h1=plot(fn,100*EFF,'LineWidth',2);
191
192     grid on
193     ylabel('\eta (%)')
194     xlabel('f (GHz)')
195     if(wmin<wmax)
196         axis([wmin/(2*pi*1e9),wmax/(2*pi*1e9),40,80]);
197     else
198         axis([wmax/(2*pi*1e9),wmin/(2*pi*1e9),40,80]);
199     end
200
201     figure(1)
202     subplot(1,2,1)
203
204
```

```
205
206     thick=3;
207
208     gamma = z2gamma(Zm(1:nw));
209     [line,hsm]=smithchart(gamma);
210     hold on
211     if(ii==1)
212         set(line,'LineWidth',thick,'Color','black','LineStyle'...
                ,'-');
213     else
214         set(line,'LineWidth',thick,'Color','blue','LineStyle',...
                '-');
215     end
216
217     if(ii>1)
218         gamma= z2gamma(Zp(1:nw));
219         [line,hsm]=smithchart(gamma);
220         set(line,'LineWidth',thick,'Color','red','LineStyle','...
                -');
221     end
222
223     subplot(1,2,2)
224
225     hold on
226
227     thick=3;
228
229     gamma = z2gamma(Zm(1:nw));
230     hold on
231     [line,hsm]=smithchart(gamma);
232
233     if(ii==1)
234         set(line,'LineWidth',thick,'Color','black','LineStyle'...
                ,'-');
235     else
236         set(line,'LineWidth',thick,'Color','blue','LineStyle',...
                '-');
237     end
238
239
```

```
240
241     if(ii>1)
242         gamma= z2gamma(Zp(1:nw));
243         [line,hsm]=smithchart(gamma);
244         set(line,'LineWidth',thick,'Color','red','LineStyle','...
                -');
245     end
246
247
248 end
249
250 function f=sA1(Ipm,Ipp,IDQm,IDQp,VDS,No,nchko,Ne,nchke,AT,wp,...
        VDD,ConvDoh,y)
251 %
252     IDSm=(ConvDoh+(1-ConvDoh)*exp(-1i*2*y*pi*wp))*...
            DrainCurrent3m(Ipm,IDQm,((1-ConvDoh)*exp(1i*2*y*pi*wp)+...
            ConvDoh)*VDS(1),No,nchko);
253     IDSm=(IDSm+(ConvDoh+(1-ConvDoh)*exp(-1i*2*y*pi*wp))*...
            DrainCurrent3(Ipm,IDQm,((1-ConvDoh)*exp(1i*2*y*pi*wp)+...
            ConvDoh)*VDS(1),Ne,nchke))/2;
254
255     IDSp=(ConvDoh*exp(-1i*2*y*pi*wp)+1-ConvDoh)*DrainCurrent3m...
            (Ipp,IDQp,(1-ConvDoh+ConvDoh*exp(1i*2*y*pi*wp))*VDS(2),...
            No,nchko);
256     IDSp=(IDSp+(ConvDoh*exp(-1i*2*y*pi*wp)+1-ConvDoh)*...
            DrainCurrent3(Ipp,IDQp,(1-ConvDoh+ConvDoh*exp(1i*2*y*pi...
            *wp))*VDS(2),Ne,nchke))/2;
257
258 f=VDD*VDS-AT*[IDSm;IDSp]; % vector to be zeroed
259 end
```

## C.2 Large Signal Transistor Model

### C.2.1 DC Current Solutions

```
function I0=DrainCurrent1(Ip,IDQ,VDS,N)
% this function finds the DC current
V=abs(VDS);
phi=pi-angle(VDS);
alpha2=acos(-IDQ/(Ip-IDQ));
k0=1-(V/2).^N*nchoosek(N,N/2);
k2R=-2*(V/2).^N*nchoosek(N,N/2-1).*cos(2*phi);
if and((2*IDQ<Ip),(Ip>0))
    j=2:N+1;
    A0=IDQ/pi*(alpha2-sin(alpha2)/cos(alpha2));
    A1=2/pi*(IDQ*sin(alpha2) - ((IDQ*alpha2)/2 + (IDQ*sin(2*...
       alpha2))/4)/cos(alpha2));
    Aj=2/pi*((IDQ*sin(j*alpha2))./j - ((IDQ*sin((j-1)*alpha2))...
       ./((j-1)*2)+(IDQ*sin((j+1)*alpha2))./((j+1)*2))/cos(...
       alpha2));
    Aj=[A1 Aj];
    for n=2:N/2-1
        k2Rn=-2*(V/2).^N*nchoosek(N,N/2-n).*cos(2*n*phi);
        k2R=[k2R k2Rn];
    end
    k2R=[k2R -2*(V/2).^N.*cos(2*N/2*phi)];
    I0=A0*k0+1/2*Aj(2:2:N)*k2R';
else
    if Ip<0
        I0=0;
    else
        A0=IDQ;

        I0=A0*k0;
    end
end
end
```

```
function I0=DrainCurrent1m(Ip,IDQ,VDS,N,nchk)
% this function finds the DC current

V=abs(VDS);
phi=pi-angle(VDS);
alpha2=acos(-IDQ/(Ip-IDQ));
n=1:(N+1)/2;
k0=1;
k1R=2*(V/2)^N*nchk(n).*cos((2*n-1)*phi);

if and((2*IDQ<Ip),(Ip>0))
    j=2:N+1;
    A0=IDQ/pi*(alpha2-sin(alpha2)/cos(alpha2));
    A1=2/pi*(IDQ*sin(alpha2) - ((IDQ*alpha2)/2 + (IDQ*sin(2*...
       alpha2))/4)/cos(alpha2));
    Aj=2/pi*((IDQ*sin(j*alpha2))./j - ((IDQ*sin((j-1)*alpha2))...
       ./((j-1)*2)+(IDQ*sin((j+1)*alpha2))./((j+1)*2))/cos(...
       alpha2));
    Aj=[A1 Aj];
    I0=k0*A0+1/2*Aj(1:2:N)*k1R';
else
    if Ip<0
        I0=0;
    else
        A0=IDQ;
        I0=k0*A0+A1*k1R(1);
    end
end
end
```

### C.2.2 Fundamental RF Current Solutions

```
function IDS=DrainCurrent3(Ip,IDQ,VDS,N,nchk)

V=abs(VDS);
phi=pi-angle(VDS);
alpha2=acos(-IDQ/(Ip-IDQ));
k0=1-(V/2)^N*nchk(1);
n=1:N/2;
k2R=-2*(V/2)^N*nchk(n+1).*cos(2*n*phi);
k2Q=2*(V/2)^N*nchk(n+1).*sin(2*n*phi);

if and(2*IDQ<Ip,Ip>0)
    j=2:N+1;

    A1=2/pi*(IDQ*sin(alpha2) - ((IDQ*alpha2)/2 + (IDQ*sin(2*...
        alpha2))/4)/cos(alpha2));
    Aj=[A1 2/pi*((IDQ*sin(j*alpha2))./j - ((IDQ*sin((j-1)*...
        alpha2))./((j-1)*2)+(IDQ*sin((j+1)*alpha2))./((j+1)*2))...
        /cos(alpha2))];

    IDS=A1*k0+1/2*(Aj(1:2:N-1)+Aj(3:2:N+1))*k2R'+1i/2*(Aj(1:2:...
        N-1)-Aj(3:2:N+1))*k2Q';
else
    if Ip<0
        IDS=0;
    else
    A1=Ip-IDQ;
    IDS=A1*k0+1/2*A1*k2R(1)+1i/2*A1*k2Q(1);
    end
end
end
```

```
function IDS=DrainCurrent3m(Ip,IDQ,VDS,N,nchk)

V=abs(VDS);
phi=pi-angle(VDS);
alpha2=acos(-IDQ/(Ip-IDQ));
n=1:(N+1)/2;
k0=1;
k1R=2*(V/2)^N*nchk(n).*cos((2*n-1)*phi);
k1Q=-2*(V/2)^N*nchk(n).*sin((2*n-1)*phi);

if and(2*IDQ<Ip,Ip>0)
    j=2:N+1;
    A0=IDQ/pi*(alpha2-sin(alpha2)/cos(alpha2));
    A1=2/pi*(IDQ*sin(alpha2) - ((IDQ*alpha2)/2 + (IDQ*sin(2*...
       alpha2))/4)/cos(alpha2));
    Aj=[A0 A1 2/pi*((IDQ*sin(j*alpha2))./j - ((IDQ*sin((j-1)*...
       alpha2))./((j-1)*2)+(IDQ*sin((j+1)*alpha2))./((j+1)*2))...
       /cos(alpha2))];
    IDS=k0*A1+A0/2*k1R(1)+1/2*(Aj(1:2:N)+Aj(3:2:N+2))*k1R'+1i...
       /2*(Aj(1:2:N)-Aj(3:2:N+2))*k1Q';
else
    if Ip<0
        IDS=0;
    else
    A1=Ip-IDQ;
    IDS=A1*k0+1/2*A1*k2R(1)+1i/2*A1*k2Q(1);
    end
end
end
```