

**BATCH-COMPATIBLE
MICROFABRICATION OF CMUT ARRAY
CHIPS FOR PHOTOACOUSTIC IMAGING
OF TISSUE-LIKE PHANTOMS (PART-II)**

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR
THE DEGREE OF
MASTER OF SCIENCE
IN
MATERIALS SCIENCE AND NANOTECHNOLOGY

By
Muhammad Rashid Mahmood
January 2024

BATCH-COMPATIBLE MICROFABRICATION OF CMUT ARRAY
CHIPS FOR PHOTOACOUSTIC IMAGING OF TISSUE-LIKE
PHANTOMS (PART-II)

By Muhammad Rashid Mahmood

January 2024

We certify that we have read this thesis and that in our opinion it is fully adequate,
in scope and in quality, as a thesis for the degree of Master of Science.

Mehmet Yilmaz (Advisor)

Mehmet Selim Hanay

Burhanettin Erdem Alaca

Approved for the Graduate School of Engineering and Science:

Orhan Arikan
Director of the Graduate School

ABSTRACT

BATCH-COMPATIBLE MICROFABRICATION OF CMUT ARRAY CHIPS FOR PHOTOACOUSTIC IMAGING OF TISSUE-LIKE PHANTOMS (PART-II)

Muhammad Rashid Mahmood

M.S. in Materials Science and Nanotechnology

Advisor: Mehmet Yilmaz

January 2024

In this thesis study, Capacitive Micromachined Ultrasound Transducer (CMUT) array chips are microfabricated with wafer-scale batch-compatible approaches as sensors for photoacoustic imaging (PAI) applications. Photoacoustic imaging (PAI) is a non-invasive medical imaging technology, free from X-ray radiation, that utilizes contrast data resulting from acoustic detection of optical stimulation to construct images. CMUT array devices are microelectromechanical systems (MEMS) devices that generate or detect acoustic or pressure waves within the ultrasonic frequency range. The CMUT devices function on the principle of vibrating parallel plate variable capacitors. Capacitance variations due to vibrating plate electrode create electrical current signals in CMUT cells, which are further processed to obtain meaningful results. In PAI, pulsed laser light is transmitted and absorbed by naturally occurring photo-absorber compounds or contrast agents in selective body-tissue or tissue-like materials. The laser pulses are converted into heat, resulting in thermoelastic expansion vibrations of the tissue or tissue-like materials (i.e., phantom material). These vibrations travel as pressure or acoustic waves through the tissue or tissue-like materials that may be detected by CMUT sensors. For the production of the CMUT array devices, borosilicate glass (Pyrex-7740) wafers were selected as transparent substrates. The bottom electrode and electrical insulation layer above the bottom electrode of the CMUT sensors are processed on the Pyrex substrates. Anodic wafer bonding is selected as one of the suitable CMUT gap formation and top electrode integration technologies. Clean and unprocessed SOI (silicon-on-insulator) wafers are used for the formation of the top electrode of the CMUT sensors. The silicon handle layer and buried oxide (SiO_2) layer of the SOI wafer are removed in order to reveal the silicon device layer that is used as the vibrating top electrode for the CMUT sensors. Metallization stacks on the Silicon device layer have been deposited

for electrical conductivity enhancement and wire bonding connections between CMUT top electrodes and printed circuit boards (PCBs). After the patterning of the vibrating top electrode layer, dicing saw processing is done to singulate the CMUT chips from 4-inch diameter wafers. Chip-scale sealing of the CMUT chips is done by conformal Parylene C deposition using UV-sensitive dicing tape as a manual mask to prevent the deposition of Parylene C on the electrical pad regions of the CMUT chips. After Parylene C deposition, UV-sensitive dicing tape is removed from chips to reveal the electrical connection pads. CMUT array devices are characterized by inspecting their capacitive gap height, measuring their resonance frequencies, and determining the integration process yield. The resonance frequency results obtained from impedance analyzer measurements of individual CMUT cells are around 5.7 MHz. Furthermore, change in the resonance frequency is clearly detectable when the applied DC bias voltage is increased during the small AC plus incremental DC excitation of CMUT cell membranes.

Keywords: Microelectromechanical Systems (MEMS), Capacitive Micromachined Ultrasound Transducer (CMUT), Microfabrication, Wafer-scale Batch-Compatible Microfabrication, Dicing Saw, Fully Automated Dicing Saw Processing, Anodic Wafer Bonding, Photoacoustic Imaging (PAI).

ÖZET

DOKU BENZERİ FANTOMLARIN FOTOAKUSTİK GÖRÜNTÜLENMESİ İÇİN CMUT DİZİN YONGALARIN ÖLÇEKLENEBİLİR MİKRO ÜRETİMİ (2. BÖLÜM)

Muhammad Rashid Mahmood

Malzeme Bilimi ve Nanoteknoloji Mühendisliği, Yüksek Lisans

Tez Danışmanı: Mehmet Yılmaz

Ocak 2024

Bu tez çalışmasında, Kapasitif Mikroışlenmiş Ultrason Dönüştürücü (CMUT) çipler, fotoakustik görüntüleme (PAI) uygulamaları için sensörler olarak kullanılmak üzere seri üretime uyarlanabilir bir şekilde üretilmişlerdir. Fotoakustik görüntüleme (PAI), görüntüleri oluşturmak için optik uyarının akustik algılamasından kaynaklanan kontrast verilerini kullanan, X-ışını radyasyonu içermeyen, invazif olmayan bir tıbbi görüntüleme teknolojisidir. CMUT sensörler, ultrasonik frekans aralığında akustik veya basınç dalgaları üreten veya tespit eden mikroeletromekanik sistem (MEMS) cihazlarıdır. CMUT cihazları paralel plakalı değişken kapasitörlerin titreşmesi prensibiyle çalışır. Titreşimli plaka elektrodundan kaynaklanan kapasitans değişimleri, CMUT hücrelerinde elektrik akımı sinyalleri oluşturur ve bunlar, anlamlı görüntüler oluşturmak üzere işlenir. Fotoakustik görüntülemede, darbeli lazer ışığı, seçici vücut dokusu veya doku benzeri malzemelerde doğal olarak oluşan foto soğurucu bileşikler veya kontrast maddeler tarafından iletilir ve emilir. Lazer darbeleri ısıya dönüştürülür, bu da doku veya doku benzeri malzemelerde termoelastik genleşme titreşimlerine neden olur. Bu titreşimler, CMUT sensörleri tarafından tespit edilebilecek doku veya doku benzeri materyaller boyunca basınç veya akustik dalgalar halinde hareket eder. CMUT sensörlerin üretimi için şeffaf alttaşlar olarak borosilikat cam (Pyrex-7740) alttaşlar seçilmiştir. CMUT sensörlerinin alt elektrotu ve alt elektrotunun üzerindeki elektrik yalıtım katmanını Pyrex alt katmanları üzerinde işlenmiştir. Anodik alttaş birleştirme, CMUT boşluk oluşturulması ve üst elektrot entegrasyon teknolojilerinden biri olarak seçilmiştir. CMUT sensörlerinin

üst elektrotunun oluşturulması için temiz ve işlenmemiş SOI alttaşlar kullanılmıştır. CMUT sensörleri için titreşimli üst elektrot olarak kullanılan silikon cihaz katmanını ortaya çıkarmak için SOI alttaşın silikon tutma katmanı ve gömülü oksit (SiO_2) katmanı aşındırılmıştır. Silikon cihaz katmanındaki metalizasyon katmanları, elektriksel iletkenliğin arttırılması ve CMUT üst elektrotları ile baskılı devre kartları (PCB'ler) arasındaki tel bağlama bağlantıları için biriktirilmiştir. Titreşimli üst elektrot katmanının şekillendirilmesinden sonra, CMUT çiplerini 4 inç çapındaki alttaşlardan ayırarak tekilleştirmek için yonga testeresi işlemi yapılmıştır. CMUT çiplerinin sızdırmazlığı Parylene C biriktirme yoluyla yapılmıştır. Parylene C biriktirilmesinden sonra UV ışığa duyarlı dilimleme bandı, elektriksel bağlantı pedlerini ortaya çıkarmak için yongalardan ayrılmıştır. CMUT dizi cihazları, kapasitif boşluklarının gözlemlenmesi, rezonans frekanslarının ölçülmesi, ve üretim adımlarının bütününe üretim verimliliği incelenerek karakterize edilmiştir. Tekli CMUT hücrelerinin empedans analizörü ölçümlerinden elde edilen rezonans frekansı sonuçları 5,7 MHz civarındadır. Ayrıca, CMUT hücre zarlarının küçük alternatif akım ve artımlı doğru akım uyarımı sırasında uygulanan doğru akım gerilim voltajı arttığında rezonans frekansındaki değişiklik açıkça tespit edilebilmiştir.

Anahtar sözcükler: Mikroelektromekanik Sistemler (MEMS), Kapasitif Mikroişlenmiş Ultrason Dönüştürücü (CMUT), mikrofabrikasyon, Seri üretime uygun ve ölçeklenebilir çip veya yonga üretimi, Yonga doğrama testeresi, Yonga doğrama testeresi ile tam otomatik dilimleme işlemi, Anodik alttaş birleştirme, Fotoakustik Görüntüleme.

Acknowledgement

First of all, I would like to express my deepest gratitude towards my advisor, Dr. Mehmet Yilmaz, for his invaluable mentorship, constructive feedback, and unconditional support throughout the pursuit of my master's degree studies at Bilkent University, Ankara. I was privileged to have the opportunity to work under his guidance in the xfrontiers Research Labs Group. His profound academic and research expertise significantly influenced my present accomplishments as a researcher. His guidance and support beyond academia played a crucial role in shaping my intellectual and personal growth.

I express my profound gratitude to Assoc. Prof. Dr. Fikret Yildiz for his mentorship and invaluable counsel throughout my research. I would also like to thank to Prof. Dr. Abdullah Atalar for his critical feedback on device characterization and generous permission to use his lab facilities.

I'm deeply thankful to my family for their never-ending love, support, and understanding while pursuing my master's degree. My mother, Sakina, and my father, Hanif, were always a source of motivation, and I'm really proud to be their son. I am grateful to my brothers, Tayyab, Tahir, and Qasim, for their support during the rough patches of my academic life. I am very appreciative of the trust and emotional support provided by my sisters, Tahira, Aamina, Sidra, and Rabia; this journey would have been extremely challenging without them. I extend my affection to my nephews Abdul Hadi, Saad, and Hassan, as well as my nieces Anaya, Asma, Sara, and Aizal; they have brought so much happiness into my life, and talking to them even over video calls always serves as an antidote to my stress.

Furthermore, I would like to thank the present and former members of the xfrontiers Research Labs Group, including Doğu Kaan, Halit Öztürk, Habibe Keleş, Merve Mintaş, and Ahmad Elshenety, for fostering a collaborative and cooperative research environment within the team. I'm grateful for your priceless

counseling and friendships.

Special thanks to my dear friends and colleagues —Salahuddin, Ali Sheraz, Imran Nawaz, Najeeb Ullah, Badar Munir, Zayn Siddiqui, Sobia Farooq, Momil Baig, Amir Parsi, Yusuf Aslan, Yunus Altintop, and Emin Aliyev—for all the support, camaraderie, and for making my experience wonderful at Bilkent University. A heartfelt acknowledgment to my hometown buddies – Faizan Ullah, Usman Afzal, and Asad Iqbal (Late) – your friendship has been my anchor from thousands of miles away. Your late-night pep talks, virtual cheers, and enduring support have turned this academic adventure into a shared triumph. You guys will always have a special place in my heart.

I would like to express our gratitude to TÜBİTAK, and TÜBİTAK Project No. 118S041 for providing all the necessary resources (money and time) for the realization of the studies presented in this thesis. Furthermore, additional time provided by TÜBİTAK during the most difficult times of the COVID-19 pandemic, was very critical for the completion of the entire microfabrication process of the CMUT chips, characterization of two CMUT chips, hence the completion of my thesis project. In addition, I would like to also express our gratitude to the National Nanotechnology Research Center (UNAM) at Bilkent University, and Institute of Materials Science & Nanotechnology at Bilkent University for providing us with the other necessary technical resources and financial assistance during my master’s program.

We appreciate the detailed technical support of Günther Weidlinger, Robert Eichinger-Heue, and Tobias Wernicke from EVG Austria throughout the process development phase of anodic wafer bonding process which was completed during the thesis studies of Doğu Kaan Buğra Özyiğit, and was vital development for the continuation and completion of the remaining parts of the CMUT chip microfabrication during my thesis studies.

We acknowledge the continuous and invaluable support from Jens Griesmann and DISCO HI-TEC EUROPE GmbH during the dicing saw process development

studies, and alignment-teaching assisted fully automated dicing saw process development studies.

We also acknowledge the technical consulting support of Spark Ölçüm Teknolojileri A.Ş., and ODTÜ Merkez Lab while we were trying to learn how to safely operate the impedance analyzer (HP 4194A).



Contents

1	Introduction	1
2	Microfabrication	12
2.1	Design of CMUT Array Sensor Chips	12
2.2	Mask Design and Fabrication	15
2.3	Fabrication of CMUT Cavity and Bottom Electrode	17
2.3.1	CMUT Cavity Formation	17
2.3.2	Metallization of the CMUT Gap	17
2.3.3	Photoresist Lift-off Process	18
2.3.4	Insulation Layer Deposition	19
2.3.5	Insulation Layer Patterning	20
2.4	Anodic Wafer Bonding	22
2.5	Top Electrode Fabrication	24
2.5.1	Removal of Handle Layer	24

2.5.2	Removal of Buried Oxide Layer	27
2.5.3	Deposition of Blanket Layers	31
2.5.4	Deposition with Shadow Mask (Stencil)	35
2.5.5	Patterning of Device Layer Silicon	37
2.6	Singulation of Chips	52
2.6.1	Removal of Dicing Tape	58
2.6.2	Removal of Dicing Tape using Oxygen Plasma Processing .	59
2.7	Oxygen Plasma Cleaning	62
2.8	Manual Masking and Parylene-C Coating	63
2.9	Microfabrication Process Flow for the CMUT Devices (2D View) .	64
3	Characterization	75
3.1	Inspection of Cavities of the CMUT Devices	75
3.2	Resonance Frequency Measurements	78
4	Fully Automated Dicing Saw Processing	84
4.1	Wafer-Scale Microfabrication of Pseudo MEMS Devices	84
4.1.1	Device Design	84
4.1.2	Photomask Manufacturing	85
4.1.3	Microfabrication of Wafers with Photoresist Features . . .	86

4.1.4	Microfabrication of Wafers with Copper Features	87
4.2	Selection of Appropriate Targets for Alignment Teaching	88
4.2.1	Macro Target Selection	88
4.2.2	Micro Target Selection	92
4.2.3	Limitations on the Target Dimensions	93
4.3	Alignment Teaching Procedure	95
4.3.1	Sample Preparation	95
4.3.2	Device Data Preparation	96
4.3.3	Alignment-Data Preparation	96
4.3.4	Workpiece Loading	98
4.3.5	Low Magnification (0.75X) Rough Theta Alignment	98
4.3.6	Channel 1 Macro Target Teaching	99
4.3.7	High Magnification (7.5X) Fine Theta Alignment	100
4.3.8	Channel 1 Micro Target Teaching	101
4.3.9	Channel 1 Street Adjustment	102
4.3.10	Channel 2 Micro Target Teaching and Street Adjustment	103
4.3.11	Teaching Data Writing	104
4.4	Potential Errors in Alignment Teaching and Their Troubleshooting	105
4.4.1	Wrong Target Selection	105

4.4.2	Index-Check Error	105
4.4.3	Error due to Fabrication Defects	106
4.5	Fully Automated Dicing Operation	107
4.5.1	Potential Applications of Alignment Teaching Assisted Automated Dicing	107
4.6	Dicing Saw Processing Time	108
4.6.1	Cutting Time (T_1)	108
4.6.2	Chuck Table Return Time in Multi-Step Cutting (T_2) . . .	111
4.6.3	Line Switching Time (T_3)	112
4.6.4	Channel Switching Time (T_4)	115
4.6.5	Blade Ascending and Descending Time (T_5)	115
4.6.6	Formulation of Total Dicing Saw Processing Time	116
4.6.7	Experimental and Theoretical Time Comparison	117
5	Conclusion and Future Work	119
5.1	Conclusion	119
5.2	Future Work	121

List of Figures

1.1	Schematic illustrating the structure of a single CMUT cell.	2
1.2	Schematic of the sacrificial release method for the CMUTs micro-fabrication.	5
1.3	Schematic of the wafer bonding process for the CMUTs microfab-rication.	6
1.4	Schematic representation of CMUTs operation: (a) Conventional Mode, (b) Collapse Mode.	7
1.5	Schematic illustrating the working principle of Photoacoustic Imaging (PAI).	8
1.6	Frequency versus Impedance plot displaying a mechanical reso-nance frequency of 77.6 kHz for a CMUT device.	9
1.7	Process flow of Diamond Blade Mechanical Dicing from the wafer to the die or chip level.	10
2.1	Chip-size drawing of CMUT Array Sensor showcasing CMUT cells, laser fiber area, and the connection wires.	13

2.2	Chip-size drawing of CMUT Array Sensor displaying main ASIC pad arrays, supplementary ASIC pad arrays, and the PCB pad arrays.	15
2.3	Chip-size drawings of microfabrication masks for the CMUT Devices: (a) Mask 1 (cavity formation and metallization), (b) Mask 2 (insulation layer patterning), (c) Mask 3 (metal pads deposition for wire bonding connections of device layer), (d) Mask 4 (device layer patterning), (e) All 4 masks aligned on top of each other. . .	16
2.4	CMUT Cavity Formation: (a) Chip size drawing of the fabrication Mask 1, (b) Schematic of a CMUT cell showing its cross-sectional view after cavity formation.	18
2.5	Metallization of the CMUT Gap: (a) Chip size drawing of the fabrication Mask 1, (b) Schematic of a CMUT cell displaying its cross-sectional view after the metals were deposited.	19
2.6	Conformal deposition of insulation layer: (a) Chip size drawing of the fabrication Mask 1, (b) Schematic of a CMUT cell displaying its cross-sectional view after the insulation layer (Al_2O_3) has been deposited.	20
2.7	Chip-size drawing of the insulation layer patterning mask (Mask 2).	21
2.8	Schematic of anodic wafer bonding process between Silicon and Glass wafers.	22
2.9	The wafer pair of Pyrex-7740 and SOI after anodic wafer bonding. Image is taken from the silicon handle layer side of the SOI wafer, while the Pyrex wafer is below the SOI wafer in this view.	25
2.10	Pyrex-SOI wafer pair with partially removed handle layer.	26
2.11	Pyrex-SOI wafer pair after complete removal of the handle layer.	27

2.12 Pyrex-SOI wafer pair with partially removed BOX layer.	28
2.13 Pyrex-SOI wafer pair after complete the removal of BOX layer (with Si-device layer on top).	29
2.14 Pyrex-SOI wafer pair with stagnant water on its surface (because of the un-etched the BOX layer) during water-slip test.	30
2.15 Pyrex-SOI wafer pair after masking its alignment marks with the Kapton tape.	31
2.16 Pyrex-SOI wafer pair after blanket deposition of Cr-Au-Cr layers.	32
2.17 Film thicknesses of Chrome and Gold layers measured by the laser scanning confocal microscope (Keyence VK-X100).	33
2.18 Optical microscope images of the alignment marks of the Pyrex- SOI wafer pair revealed by the mechanical scribing.	35
2.19 Optical microscope images of alignment marks after the Pyrex-SOI wafer pair was aligned with the stencil mask (Mask 3).	36
2.20 Pyrex-SOI wafer pair after depositing the electrical pads using shadow mask (Mask 3).	36
2.21 Bond 3 Pyrex-SOI wafer pair that was broken during spin-coating.	38
2.22 Pyrex-SOI wafer pair coated with a layer of AZ 5214E photoresist.	38
2.23 Silicon test wafer along with optical microscope images of well- defined (or sharp) photoresist features showing successful develop- ment.	39
2.24 Photoresist feature on the Silicon test wafer underwent the Scratch Test after photoresist development.	40

2.25	A photograph the device layer patterning photomask (Mask 4). . .	41
2.26	Screenshot of mask aligner after the back side crosshair alignment was completed: the green cross-hairs were aligned with the alignment marks on left and right side of the Pyrex-SOI wafer pair. . .	42
2.27	Pyrex-SOI wafer pair with patterned photoresist mask (Mask 4). .	42
2.28	Optical microscope images displaying alignment accuracy measurements of the photoresist mask (Mask 4) on corner CMUT chips of the Pyrex-SOI wafer pair. Note: These optical images are taken from the back side of the Pyrex wafer, after Si device layer was also etched. Although not shown here, similar alignment accuracy inspection has been done on the corner chips from the front side of the Pyrex wafers before all the wet etching and Bosch process Si etching steps were performed, because all these etch processes are irreversible patterning processes.	43
2.29	Pyrex-SOI wafer pair after etching the blanket-coated top chrome layer.	44
2.30	Schematic of the Cr-Au-Cr stack after etching the top chrome layer of the Pyrex-SOI wafer pair.	45
2.31	Pyrex-SOI wafer pair after etching of the blanket-coated gold layer.	46
2.32	Schematic of the Cr-Au-Cr stack after etching the gold layer of the Pyrex-SOI wafer pair.	47
2.33	Pyrex-SOI wafer pair after etching of the blanket-coated bottom chrome layer.	48
2.34	Undercuts formed in the Cr-Au-Cr layers of the Pyrex-SOI wafer pair after etching the bottom chrome layer: (a) Optical microscope image, (b) Schematic of Cr-Au-Cr stack.	49

2.35	Schematic of the Bosch Process.	50
2.36	Pyrex-SOI wafer pair after patterning the Silicon device layer using DRIE process.	52
2.37	Image of a dressing board specified for DISCO-R07 dicing blades.	53
2.38	Optical microscope images of the test Pyrex wafer displaying Chipping around edges of the dicing streets after cutting: (a) Front-Side, (b) Back-Side.	55
2.39	Chipping lengths on the Front and Back sides of test Pyrex wafer measured by Image-J software: (a) 15K RPM, (b) 20K RPM.	55
2.40	Image of a real wafer mounted on the dicing frame.	56
2.41	Junction of two dicing streets on the Pyrex wafer: (a) Before manual stiction of the dicing tape, (b) After manual stiction of the dicing tape.	57
2.42	Print-screen of Device Data of Dicing Saw (DISCO DAD-3220).	57
2.43	CMUT chips singulated from the real wafer using manual mechanical dicing process.	58
2.44	CMUT Sensor chips obtained after peeling off the dicing tape following the UV exposure.	59
2.45	CMUT chip (along with its schematic) covered with the D-841 dicing tape.	60
2.46	SEM image showing residues of the dicing tape on ASIC pads region of the CMUT chip.	61

2.47 Optical microscope image displaying the ASIC pads region of the CMUT chip after removing the dicing tape using oxygen plasma processing.	61
2.48 CMUT chip and optical microscope images of its ASIC pads after it was cleaned with oxygen plasma processing (Descum Process). .	62
2.49 CMUT chip covered with a layer of Parylene-C. The region that is inside the green colored square is the region that is coated with permanent layer of Parylene C, while the outer sides of the green square are protected with dicing tape (D-841) before Parylene C deposition. Hence, the Parylene C at the outer sides of the green colored square is removed while peeling the dicing tape to reveal the electrical pads.	63
2.50 Blank Pyrex-7740 wafer.	64
2.51 Chrome deposition as hard mask on Pyrex wafer.	64
2.52 Photolithography with Mask 1 for cavity formation on Pyrex wafer.	64
2.53 Argon Reactive Ion Etching (RIE) for etching chrome hard mask.	65
2.54 SF ₆ Reactive Ion Etching (RIE) for etching Pyrex wafer.	65
2.55 Buffered Oxide Etch (BOE) wet-etching process for Pyrex. Note that the undercut below the photoresist is increased, and depth of the gap is also increased.	65
2.56 Metallization (Ti-Pt-Au) as the bottom electrode.	66
2.57 Photoresist Lift-off with Prinha solution.	66
2.58 Chrome wet-etching using chrome etchant.	66
2.59 Alumina deposition using Atomic Layer Deposition (ALD).	67

2.60	Chrome hard mask deposition on the insulation layer.	67
2.61	Photolithography with Mask 2 for etching alumina layer from electrical pad regions.	67
2.62	Chrome wet-etching from electrical pad regions.	68
2.63	Alumina layer etching from electrical pad regions using diluted AZ 400K Developer.	68
2.64	Photoresist removal using acetone and Prinha.	68
2.65	Chrome hard mask removal using chrome etch.	69
2.66	Anodic Wafer Bonding of Pyrex and Silicon-on-Insulator (SOI) wafers.	69
2.67	SF ₆ Reactive Ion Etching for handle layer removal of the SOI wafer.	69
2.68	BOE wet-etching for removing buried silicon oxide layer of the SOI wafer.	70
2.69	Blanket layer deposition (Cr-Au-Cr) on Si-device layer of the SOI wafer.	70
2.70	Deposition of wire-bonding pads for top electrode using Stencil Shadow Mask 3.	70
2.71	Photolithography with Mask 4 to pattern the Si-device layer.	71
2.72	Wet-etching of blanket coated Cr-Au-Cr metal stack.	71
2.73	Deep Reactive Ion Etching (DRIE) of Si-device layer using Bosch Process.	71
2.74	Dicing saw processing for the chip singulation.	72

2.75	Photoresist removal using Descum Process (O_2 will also remove top chrome layer).	72
2.76	Parylene-C coating to seal the CMUT cavities.	72
2.77	ASIC to CMUT integration using flip-chip bonding process. . . .	73
2.78	Underfilling with non-conductive epoxy after ASIC to CMUT integration to enhance the integrity of the structure.	73
2.79	CMUT to PCB integration using flip-chip bonding.	73
2.80	Underfilling with non-conductive epoxy after CMUT to PCB integration to enhance the integrity of the structure.	74
3.1	Optical microscope image displaying 3 CMUT membranes after removing these silicon membranes from the Pyrex substrate.	76
3.2	SEM images displaying cavities and bottom electrodes of 2 CMUT devices.	76
3.3	SEM images displaying the FIB cross-section of a CMUT cell: (a) 8000 x magnification, (b) 25000 x magnification.	77
3.4	An image showing location of Chip-05 and Chip-06 on the Bond-8 wafer.	78
3.5	Impedance analyzer connected to a computer system and a probe station.	79
3.6	CMUT sensor chip connected with the impedance analyzer using 2 probes of the probe station.	80
3.7	Resonance frequency plot of an individual CMUT cell (B08-CH06-CL020) at 25V DC Bias.	81

3.8	Shift in the resonance frequency of the CMUT Cell B08-CH05-CL114.	82
3.9	Images of pin holes in alumina layer captured by the SEM imaging capability of the FIB/SEM dual beam instrument: (a) 2500 x Magnification, (b) 35000 x Magnification.	83
4.1	Chip-scale drawing of a pseudo MEMS device chip (16.75 mm by 16.75 mm) with 23 potential targets.	85
4.2	Photomask for wafer-scale manufacturing of pseudo MEMS device chips: (a) Photomask design, (b) Manufactured photomask. . . .	86
4.3	Four-inch diameter wafers with pseudo MEMS devices having photoresist features: (a) Pyrex-7740 wafer, (b) Silicon wafer.	86
4.4	Four-inch diameter wafers with pseudo MEMS devices having copper features: (a) Pyrex-7740 wafer, (b) Silicon wafer.	87
4.5	Q-value outcomes of the 4 approved macro targets.	91
4.6	Q-values of the approved micro targets.	94
4.7	Four-inch diameter Silicon wafer mounted on a dicing frame to prepare the sample for the alignment teaching and fully automated dicing.	95
4.8	Device data screen of dicing saw displaying workpiece dimensions and cutting parameters.	96
4.9	Print screen of dicing saw displaying the alignment data.	97
4.10	Silicon wafer positioned on the chuck table of the dicing saw. . . .	98

4.11	Print screen of the dicing saw after the target window was aligned horizontally with the dicing street edge on the wafer at low magnification (0.75X).	99
4.12	Q-value results of a good CH1 Macro target.	100
4.13	Print screen of the dicing saw after the target window was aligned horizontally with the dicing street edge on the wafer at high magnification (7.5X).	101
4.14	Q-value outcomes of a good CH1 Micro target.	102
4.15	Hairline of dicing saw aligned with the dicing street on the wafer in CH1.	103
4.16	Q-value outcomes of a good CH2 Micro target.	104
4.17	Print screen of the dicing saw displaying 1 Macro and 2 Micro targets recorded during alignment teaching operation.	104
4.18	Print screen of the dicing saw displaying a rejected target pattern due to the presence of similar features nearby on the pseudo-MEMS chip of the wafer.	105
4.19	Microfabrication defects on the pseudo-MEMS chips of the wafer: (a) Undeveloped photoresist feature, (b) A cluster of unwanted particles.	106
4.20	A 4-inch diameter Silicon wafer diced into 16 pseudo-MEMS chips using fully automated dicing saw processing.	107
4.21	Schematic of the wafer for cutting length calculations (not drawn to scale).	109
4.22	Schematic of the wafer for calculating line switching distance (not drawn to scale).	113

4.23 Comparison between the experimental and theoretical dicing saw processing times for a single-step cutting with 16.75×16.75 mm pseudo-MEMS devices of a 4-inch diameter wafer. 118

4.24 Comparison between the experimental and theoretical dicing saw processing times for a multi-step cutting of with 3×3 mm chips of a 4-inch diameter wafer. 118



List of Tables

2.1	Given design input parameters for the CMUT Arrays Chips to be manufactured.	15
2.2	Handle layer etching time for the 8 CMUT wafers.	26
2.3	BOX layer etching time for the 8 CMUT wafers.	29
2.4	E-beam Evaporator tooling factors calculated for Chrome and Gold metals.	34
2.5	Recipe parameters of the mask aligner for UV exposing Pyrex-SOI wafer pair covered with AZ 5214E photoresist layer.	41
2.6	Wet-Etching time for top chrome layer of the Pyrex-SOI wafer pairs.	45
2.7	Wet-Etching time for gold layer of the Pyrex-SOI wafer pairs.	47
2.8	Wet-Etching time for the bottom chrome layer of Pyrex-SOI wafer pairs.	49
2.9	DRIE etching time of Silicon device layer of Pyrex-SOI wafer pairs.	51
3.1	Yield data for the CMUT devices of Chip-05 and Chip-06.	80
4.1	Design Specifications for the Macro and Micro Alignment Targets.	85

4.2	Q-value results of the 15 potential Macro Targets having different geometries and dimensions.	89
4.3	Q-value results of the 8 potential micro targets having different geometries and dimensions.	92



Chapter 1

Introduction

Microelectromechanical systems (MEMS) are an integration technology that couples miniaturized mechanical and electrical components such as sensors and actuators using microfabrication processes [1]. The capacitive micromachined ultrasonic transducers (CMUTs) are electrostatic MEMS devices [2].

Capacitive micromachined ultrasonic transducers (CMUTs) are parallel plate capacitors that consist of two conducting plates separated by a vacuum-sealed cavity. In addition to the vacuum-sealed cavity, there may be a thin layer of insulating material deposited to one of the electrodes to prevent direct electrical connection between electrodes. Furthermore, instead of vacuum-sealed cavity, the CMUT cavity may be filled with air at atmospheric pressure. One of the capacitor plates is moveable with respect to the other, and the movement is caused by electrostatic force or mechanical pressure. The mobile plate may be seen as being clamped by a spring that opposes the electrostatic force of attraction. The capacitive transduction in CMUTs occurs as a result of the electrostatic force of attraction, also known as Coulomb's force, between the charged plates of the capacitor [3]. In order to ensure the effectiveness of competing electrostatic transducers, it is necessary to maintain an electric field of 10^8 V.cm^{-2} or higher in the gap [4]. Figure 1.1 displays the schematic of a CMUT device [5].

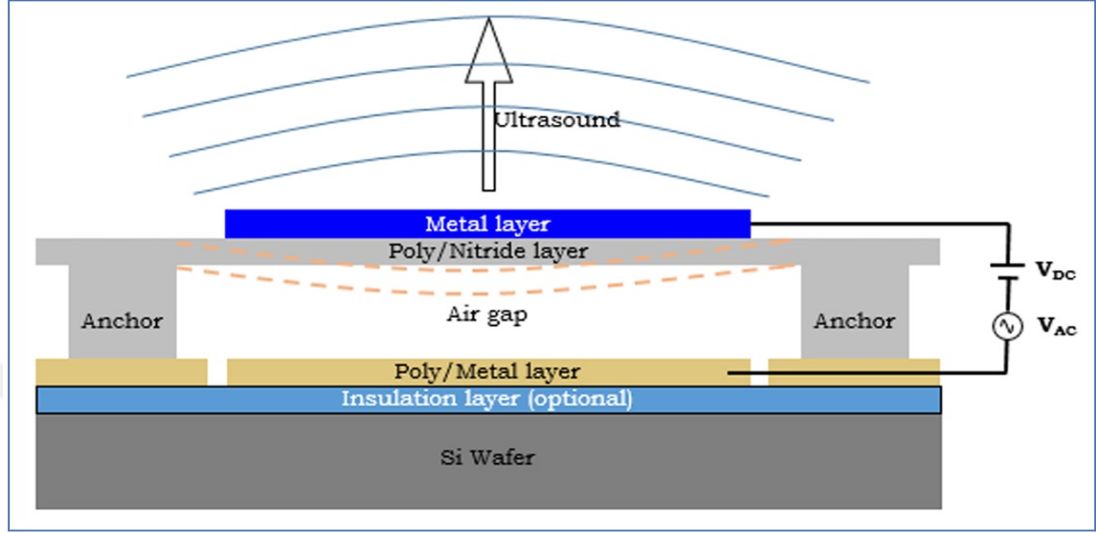


Figure 1.1: Schematic illustrating the structure of a single CMUT cell.

The CMUT devices may function as transmitters or receivers. In the transmission mode of CMUTs, the given alternating current (AC) signal of defined amplitude causes vibrations in the movable plate to generate ultrasonic waves. The output ultrasonic waves induce ultrasonic vibrations in the target medium. During the receive mode of the CMUTs, the incoming ultrasonic waves impinge against the flexible plate, resulting in displacements in the plate. The variations in displacement alter the capacitance [6], facilitating the measurement of the incoming signal [7]. The variation in capacitance generates an electric current signal under constant DC bias voltage, whose magnitude depends on the frequency of the ultrasonic wave, the bias voltage, and the capacitance of the CMUT device [4].

The first capacitive ultrasound transducer was constructed using traditional machining equipment, where a mylar membrane served as a top flexible plate against a rough metal surface as a fixed bottom electrode [8]. Later models of these capacitive ultrasonic transducers were manufactured using micromachining techniques to create cavities on a silicon substrate, as opposed to conventional machining processes [9]. However, the first iteration of a completely micromachined ultrasonic transducer (CMUT) was unveiled in 1994 by a research team at Stanford University [10].

The capacitive micromachined ultrasonic transducer devices are constructed according to the desired resonance frequency. The mechanical resonance frequency of the membrane of a CMUT cell is influenced by many factors, including its thickness (t_m), radius (a), Young's modulus (E), density (ρ), and Poisson's ratio (σ). The resonance frequency may be approximated using the analytical formula in Equation 1.1. Usually, finite element analysis (FEA) is conducted to determine the resonance frequency more accurately. FEA models consider several aspects, including constraints (i.e. boundary conditions) on the membrane and substrate material, atmospheric pressure, and stress in the membrane [11]. The resonance frequency (and bandwidth) of CMUTs is also influenced by the fill factor of the transducer, which is the ratio of the active area of the transducer to its total area [12].

$$\text{Resonance Frequency } (f_r) = \frac{0.47t_m}{a^2} \sqrt{\frac{E}{\rho(1 - \sigma^2)}} \quad (1.1)$$

Another crucial factor in the design of CMUTs is to identify their collapse (a.k.a. pull-in) voltage, which is used to establish their operating voltage. The applied DC voltage generates an electrostatic force between the electrodes of a CMUT cell that opposes the mechanical force or stiffness of the membrane. At a certain DC voltage, the electrostatic forces overpower the mechanical forces acting on the membrane, causing it to collapse over the bottom electrode [13]. The pull-in voltage is the lowest DC voltage at which the equilibrium between the mechanical and electrostatic forces of the membrane does not exist anymore due to imbalance between the electrostatic force and the restoring mechanical force. The force imbalance between mechanical and electrostatic forces due to applied voltage, known as the pull-in voltage, happens when the membrane moves approximately one-third of the original gap between the two electrodes. The pull-in voltage depends on the spring stiffness of membrane (k), the effective gap height (g), the permittivity of free space (ϵ), and the actuation area of two conductive parallel plates (A). Equation 1.2 provides an analytical formulation that approximates the pull-in voltage. However, accurate calculation and modelling requires finite element analysis, which considers fixing the membrane along the CMUT

cell's perimeter and other material and acoustic parameters [14].

$$V_{pi} = \sqrt{\frac{8kg^3}{27\epsilon A}} \quad (1.2)$$

The dielectric strength refers to the highest level of electric field intensity that a material can endure without experiencing breakdown or transitioning into a conductive state. It is crucial to determine the dielectric breakdown voltage in CMUT in order to safely operate them with a DC bias voltage, since dielectric breakdown is an irreversible process. It is quantified in terms of volts per unit thickness [15]. It is determined by ramping the voltage and then measuring the electric field at which a rapid rise in electric current is detected through the insulating layer. This rapid current rise leads to dielectric shorting between electrodes of the CMUT device due to localized heating, melting, or melt-filament creation [16].

The microfabrication techniques of CMUTs can be classified broadly into two main types: the sacrificial release method and the wafer bonding. In the sacrificial release method, the vibrating membrane or plate of the CMUT device is released by etching a sacrificial layer beneath its surface. The etchant reaches the sacrificial layer by penetrating via the etching vias or holes in the membrane or at a region close to the membrane. The process starts with a substrate covered with an insulating material, such as silicon dioxide or silicon nitride. A sacrificial material with a certain thickness is deposited since it determines the height of the CMUT cavities. The mobile plate material is deposited onto the sacrificial layer. Then, the sacrificial layer is isotropically etched from a patterned hole. Finally, an appropriate metal is coated and patterned on the plate and substrate for electrical contact (deposited metals are also part of the electrode, and metals also help with wire bonding connections). The sacrificial release method provides manufacturing simplicity, reliability, and higher yield compared to wafer bonding. Notable drawbacks include limitations on plate thickness and cavity height, concerns about membrane stresses, and issues with its stiction [17]. Figure 1.2 presents a schematic of the sacrificial release method [17].

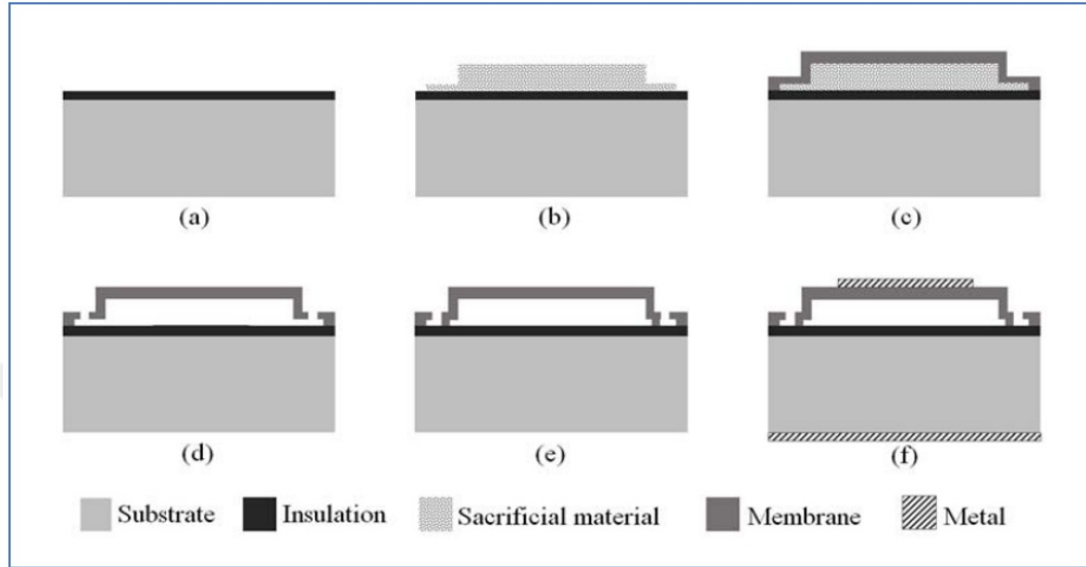


Figure 1.2: Schematic of the sacrificial release method for the CMUTs microfabrication.

Various wafer bonding techniques are used in the fabrication of CMUTs, with fusion bonding, anodic bonding, adhesive bonding, and thermo-compression bonding being the most significant methods. The wafer bonding approaches generate suspended membranes over the CMUT cavities; however, they vary according to the underlying physics and their implementation. The substrate wafer containing CMUT cavities is bonded with a second wafer, primarily a silicon-on-insulator (SOI) wafer. During the bonding process, the device side of the SOI wafer is oriented towards the substrate wafer. Dry and wet-etching procedures remove the handle and buried oxide layers of the SOI wafer, respectively. A metal electrode is deposited onto the surface of the device layer. Since the SOI wafer may be manufactured with a range of device layer thicknesses, CMUTs with different membrane thicknesses can be fabricated via wafer bonding. The yield of wafer bonding depends on the cleanliness and smoothness of the wafer surface [17]. The wafer bonding is shown schematically in Figure 1.3 [17].

The CMUTs can operate in three modes: conventional, collapse, and collapse-snapback. During conventional mode operation, the CMUTs are biased at a voltage near the collapse voltage. However, the total DC bias and AC excitation voltages are carefully controlled to ensure the membrane does not come into

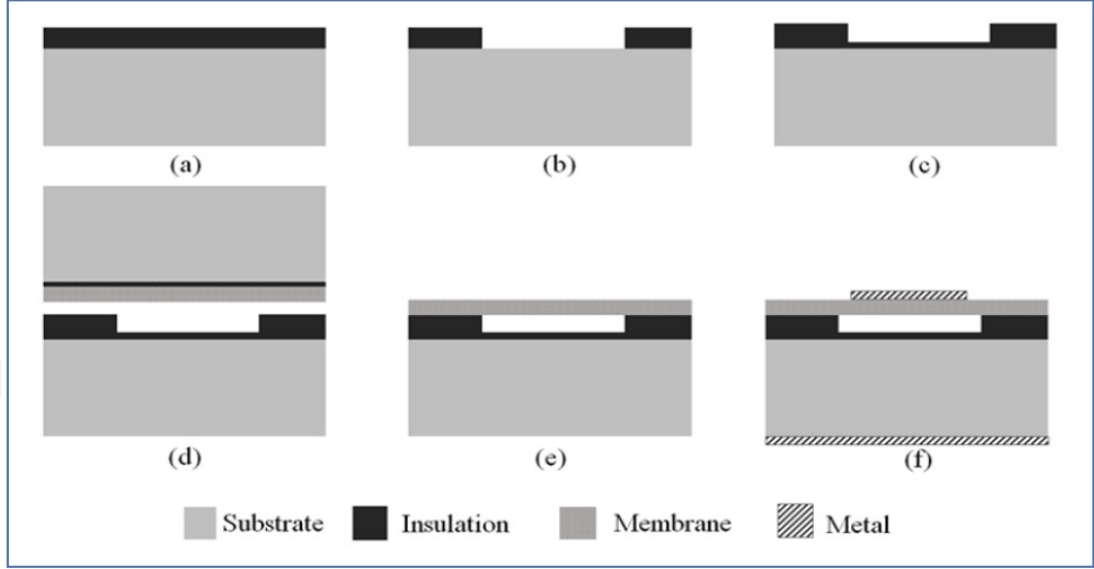


Figure 1.3: Schematic of the wafer bonding process for the CMUTs microfabrication.

contact with the substrate. In this mode, the highest displacement occurs at the membrane center. In collapse mode, the DC bias voltage applied to CMUTs is raised to a level where the electrostatic force gradient surpasses the mechanical force gradient, causing the membrane to collapse over the bottom electrode permanently. When CMUTs are subjected to AC voltage, the membrane exhibits the greatest displacement around the circular area located between its center and the edges. A schematic of conventional and collapse mode operations is shown in Figure 1.4 [18]. The membrane collapses into the bottom electrode and recovers its shape and position in the same AC cycle during the collapse-snapback mode, generating a displacement that exceeds the total gap height of the CMUT's cavity. The bias voltage applied in collapse-snapback mode is lower than the one used in the collapse mode [18].

CMUTs have many applications, such as medical imaging, minimally invasive and non-invasive treatment, biosensing, physical sensing, and airborne applications [17]. Photoacoustic imaging (PAI) is a non-invasive technique for medical imaging. The PAI utilizes a hybrid modality (optics plus acoustics) that offers excellent optical contrast and spatial resolution. In PAI, short pulses of laser light are transmitted and absorbed by naturally occurring photo-absorber compounds

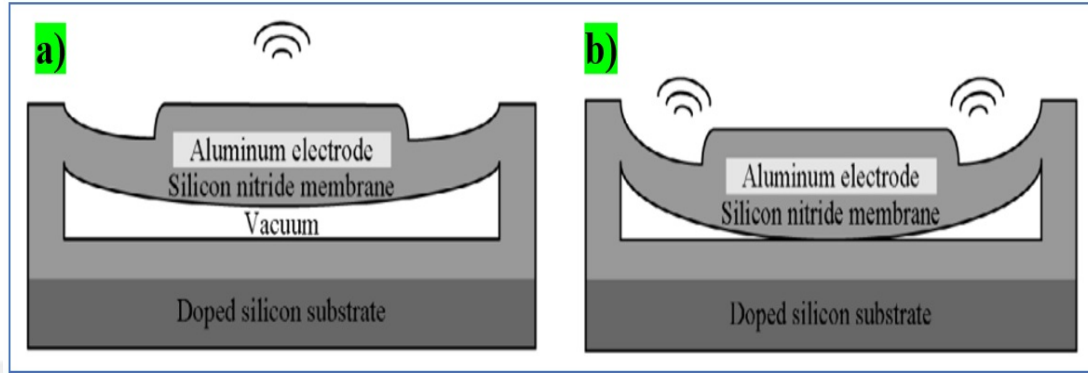


Figure 1.4: Schematic representation of CMUTs operation: (a) Conventional Mode, (b) Collapse Mode.

or contrast agents in selective body-tissue or tissue-like materials and converted into heat. The pulses of laser light are converted into heat, causing thermoelastic expansion vibrations of the tissue or tissue-like materials (i.e., phantom material), which travels as pressure waves or acoustic waves through the tissue or tissue-like materials. These heat-generated and traveling acoustic waves can be detected by the ultrasound sensing transducers[19]. Figure 1.5 displays a schematic of the working principle of photoacoustic imaging [19]. The CMUT sensor chip manufactured in this project can be used for photoacoustic imaging of phantom material that can mimic the acoustic and optical properties of human tissues under the skin.

The capacitive micromachined ultrasonic transducers (CMUT) provide several advantages compared to traditional piezoelectric transducers. CMUTs possess a wider bandwidth compared to piezoelectric transducers, resulting in the ability to provide high axial resolutions in imaging. The CMUT devices operate at reduced voltage and over a wide range of frequencies from 2 MHz to 17 MHz. Fabrication of CMUTs can be realized by surface micromachining and/or wafer bonding methods, resulting in a higher yield and lower cost than piezoelectric transducers. Photolithography and etching processes eliminate the need for subtractive dicing for electric and acoustic isolation of the array elements. In addition to allowing for the activation of certain array elements, transmit and receiver CMUT cells can be constructed on the array probe. The CMUTs may be integrated easily

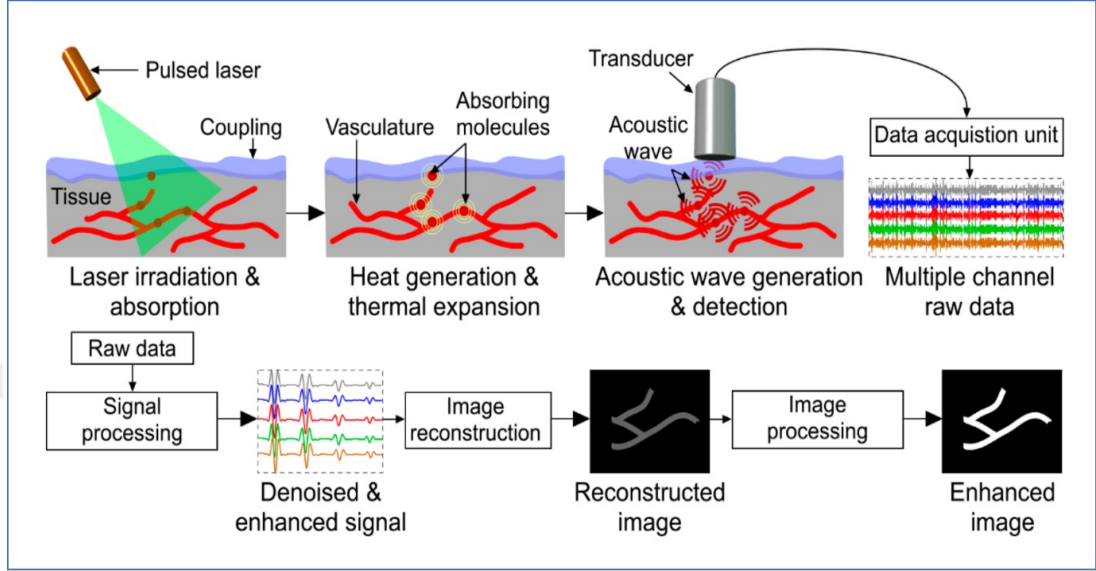


Figure 1.5: Schematic illustrating the working principle of Photoacoustic Imaging (PAI).

with the ASICs, reducing the need for conventional assembly procedures. The acoustic impedance of CMUTs matches closely the acoustic impedance of skin and tissues, eliminating the need for complicated acoustic matching layers often used in piezoelectric transducers. However, the CMUT devices suffer from inherent non-linearity, less dielectric breakdown strength, dielectric charging issues, limited penetration depth [20] and residual stress in the membrane generated during the microfabrication process [21]. The electric charges diffuse through the membrane or the bottom electrode under high electric fields, affecting the reliability of the CMUT devices [22].

Conventional piezoelectric transducer array components are bulk resonators with strong dielectric breakdown strength and environmental toughness. Piezoelectric transducers outperform CMUT devices in terms of greater signal-to-noise ratio and higher penetration depth [20]. Thermal instability, requirement of matching layer, difficulty in manufacturing arrays with high frequencies, and difficulty in miniaturization are some serious drawbacks of piezoelectric transducers [23].

Each dielectric material between the electrodes of a CMUT cell impacts its capacitance. The total capacitance of a CMUT cell may be calculated by considering it as a composite capacitor where the parallel plate capacitors are connected in series [24]. The static capacitance of CMUT devices is determined by measuring it with an LCR meter operating at a low frequency, i.e., 100 kHz. The measured capacitance values may be compared with values derived from the mathematical formula to identify discrepancies, if there are any. The variation in the capacitance may be attributed to the parasitic capacitance of the device [25].

The characterization of electrical impedance in the produced CMUT devices is essential as it offers valuable insights into the electrical and mechanical behavior of the devices. An impedance analyzer, coupled to a probe system, is used to measure the input impedance of the device. The bias voltage of CMUTs is swept systematically during measurements using an appropriate voltage increment. Electrical impedance data is collected for each biasing voltage value within the frequency range where mechanical resonance is expected [26]. Lastly, the resonance frequency is visualized by plotting the frequency versus impedance (or admittance) graphs, as shown in Figure 1.6 [27].

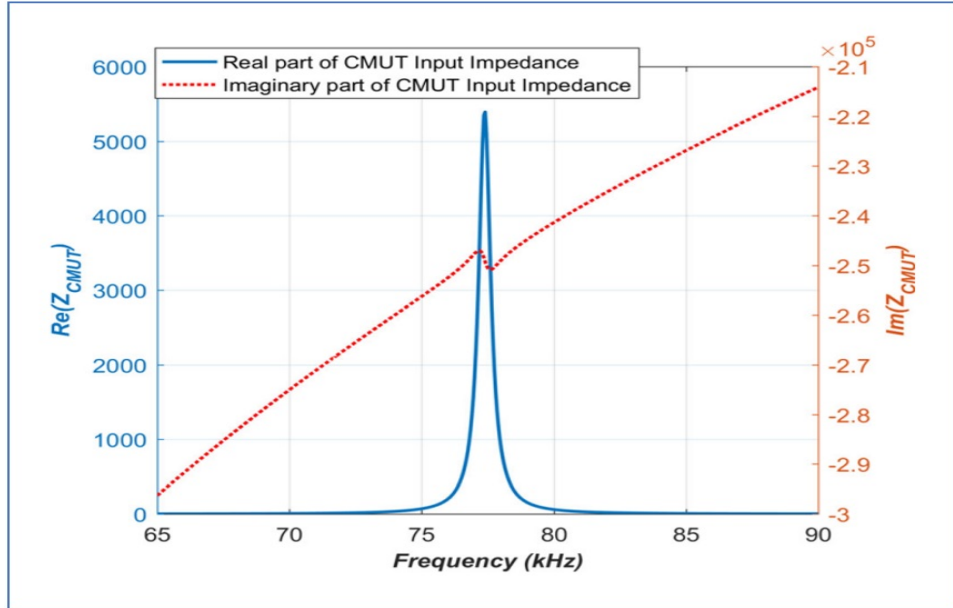


Figure 1.6: Frequency versus Impedance plot displaying a mechanical resonance frequency of 77.6 kHz for a CMUT device.

The safe transition from wafer-level (i.e., an array of multiple MEMS devices) to die-level (i.e., single MEMS device) chips is a crucial step, given the delicate nature of their structures [28]. Diamond blade dicing is the primary method used for singulating MEMS devices. In order to cut linear channels through the wafer's thickness, the circular dicing blade spins at high revolutions per minute (RPM) ranging from 20K to 80K [29]. Figure 1.7 shows the dicing process flow from the wafer to the die or chip level [29]. The functionality of MEMS devices may be compromised by particle contamination, water pressure, and rapid electrostatic energy discharge, which are common issues in traditional dicing procedures [29]. In order to prevent any potential damage to MEMS devices, a concave protective glass cap is mounted on the wafer before dicing. The protective glass cover is affixed on the wafer using thermoplastic adhesive, which is then detached by heating after the dicing process [30].

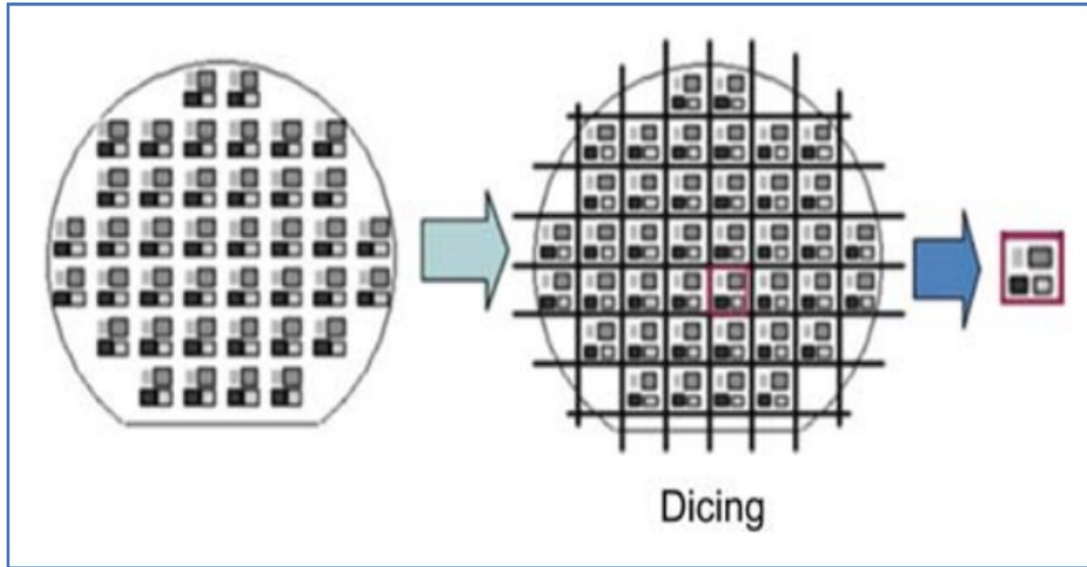


Figure 1.7: Process flow of Diamond Blade Mechanical Dicing from the wafer to the die or chip level.

This thesis project completed the remaining second part of the batch-compatible microfabrication of capacitive micromachined ultrasonic transducers (CMUTs). The first phase of the manufacturing process was conducted by another M.S. degree student (Doğu Kaan Buğra Özyiğit) from our research group. This included the formation of the bottom electrode of CMUTs and the anodic

wafer bonding of Pyrex and silicon-on-insulator (SOI) wafers [31]. In order to acquire the CMUT sensor chips from 4-inch wafers, I finished the remaining microfabrication steps, which included removing the handle layer of the SOI wafers, removing the BOX layer of SOI wafers, fabricating the top electrode by patterning the device layers, dicing the wafers into CMUT array chips, and Parylene C sealing of CMUT cell gaps in individual CMUT chips. Subsequently, the CMUT array devices were subjected to electrical characterization with an impedance analyzer, specifically in terms of measuring the resonance frequency of the vibrating individual membranes of individual cells of CMUT array chips. Another M.S. degree student (Mehmet Halit Öztürk) from our research group prepared a handheld imaging device by integrating ASIC (application-specific integrated circuit) chips with a CMUT sensor chip, the CMUT chip and ASIC pair with a printed circuit board (PCB), and the PCB with the imaging probe [32]. Integrated portable probe is planned to be used for photoacoustic imaging (PAI) of phantoms that mimic human body tissues.

This thesis is organized as follows: Chapter 1 contains a literature review on several aspects of CMUT devices, including their design, working principle, microfabrication processes, modes of operation, applications, especially photoacoustic imaging, comparison with traditional ultrasonic transducers, characterization, and singulation. Chapter 2 covers the entire microfabrication process used for manufacturing wafer-scale CMUT devices. Chapter 3 presents the electrical characterization of the manufactured CMUT devices. Chapter 4 provides details on the process development of alignment teaching, fully automated dicing, and analytical formulation for determining the total dicing time of MEMS devices. Finally, Chapter 5 provides a conclusion and future directions to the work that has been completed.

Chapter 2

Microfabrication

2.1 Design of CMUT Array Sensor Chips

The capacitive micromachined ultrasound transducers (CMUTs) array sensor chips were designed based on the required resonance frequency, operating voltage, previous studies, and microfabrication capabilities of the cleanroom at the National Nanotechnology Research Center at Bilkent University (Bilkent University UNAM). A 4-inch diameter borosilicate glass wafer (Pyrex 7740) was chosen as a substrate for CMUT microfabrication for several reasons itemized below: 1. Pyrex 7740 wafer has a comparable coefficient of thermal expansion to silicon (in the range of 20 to 440 °C) [33], making the anodic wafer bonding process between silicon and Pyrex 7740 feasible, 2. Because Pyrex 7740 wafer is an insulator, Pyrex 7740 substrate eliminates the need for a passivation layer between the substrate and bottom electrode, 3. The Pyrex 7740 wafer has high light transmission capability [34], which offers integration with a pulsed laser actuator without drilling a hole through the thickness of the Pyrex 7740 wafer.

An area for 20 by 20 array of the circular CMUT cells was chosen; however, the area equivalent to 12 by 12 cells was removed from the central region of the 20 by 20 array, leaving the CMUT array with 256 circular CMUT cells. The motivation

for designing circular CMUT devices stems from their superior flexibility and ability to deflect under lower applied voltage than square and hexagonal devices. Furthermore, circular CMUTs exhibit a uniform distribution of stress and strain along their perimeter, minimizing the risk of membrane breakage or fatigue during the operation [14]. The removed 12 by 12 array area was reserved for integrating the laser fiber light source, which serves as a light actuator. The connection wires were drawn to transmit and receive electrical signals from all 256 CMUT cells. The edge-to-edge distance between two CMUT cells, the width of wires, and the distance between two connection wires were carefully considered while designing for safe manufacturability of the chips. Figure 2.1 shows the designed CMUT cells, the reserved area for the laser fiber, and the connection wires.

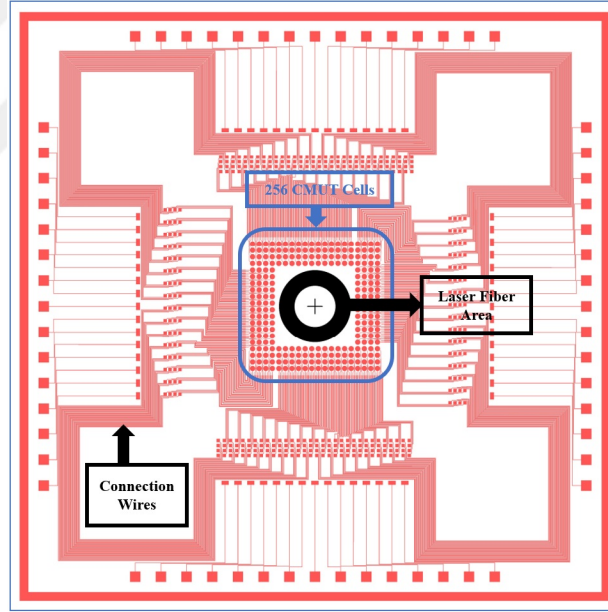


Figure 2.1: Chip-size drawing of CMUT Array Sensor showcasing CMUT cells, laser fiber area, and the connection wires.

The pads of an application specific integrated circuit (ASIC) chip were also drawn on the CMUT chip for the integration between ASIC and individual CMUT cells. Here it is important to emphasize that this thesis study is not related to the design or manufacturing of the ASIC chips. The function of the ASIC chip is to amplify the current signal received from CMUT cells, and is called a transimpedance amplifier (TIA) [35].

Two main ASIC pad arrays were included in the CMUT array chip to integrate two ASIC chips into a single CMUT. Each ASIC TIA is responsible for receiving 128 input current signals from 128 CMUT cells, and each ASIC TIA also has 15 pads that connect the ASIC TIA to the printed circuit board (PCB) pads.

Because at the time of the CMUT array chip design in 2019, our research group team was not sure if the flip-chip bonding integration process of an ASIC with 128 pads would be functional due to the limitation of the maximum applicable force of the flip-chip bonder (Finetech Fine Placer Matrix Ma) in our cleanroom [31] [32], two supplementary pad array sets for supplementary two ASIC chips were also designed, each with 64 input CMUT connections and 15 output connection pads.

The maximum force the flip-chip bonder can apply during thermosonic flip-chip bonding is 19 N. Therefore, two supplementary ASIC pad arrays for two supplementary ASICs were also designed, each to accommodate 64 input current signals from 64 CMUT cells. The transmission of the amplified signal from the ASIC TIA chip to the PCB is facilitated by the PCB connection pads located on the edge of the CMUT chip. Two potential ways for integrating ASIC TIA chips with a CMUT chip using flip-chip bonding were considered to get signals from 256 CMUT cells: using two ASICs with 128 connections per chip or employing four ASICs with 64 connections per chip. Figure 2.2 highlights the main ASIC pad arrays, the supplementary ASIC pad arrays, and the PCB pad arrays.

The dimensions of each CMUT chip were determined to be 16.75 mm by 16.75 mm (excluding the widths of the dicing streets), resulting in a 4 by 4 array of sensor chips on a 4-inch wafer. The wafer scale masks were designed with a consistent width of 250 microns for the dicing streets. The wafer bonding fabrication methodology was selected for this project, so the single-crystal silicon device layer of a silicon-on-insulator (SOI) wafer was deemed suitable as vibrating membrane material for the CMUT cells. The given design input parameters, such as cell shape, number of cells, membrane thickness, membrane radius, gap height, edge-to-edge distance between the cells, and insulator thickness, are given in Table 2.1.

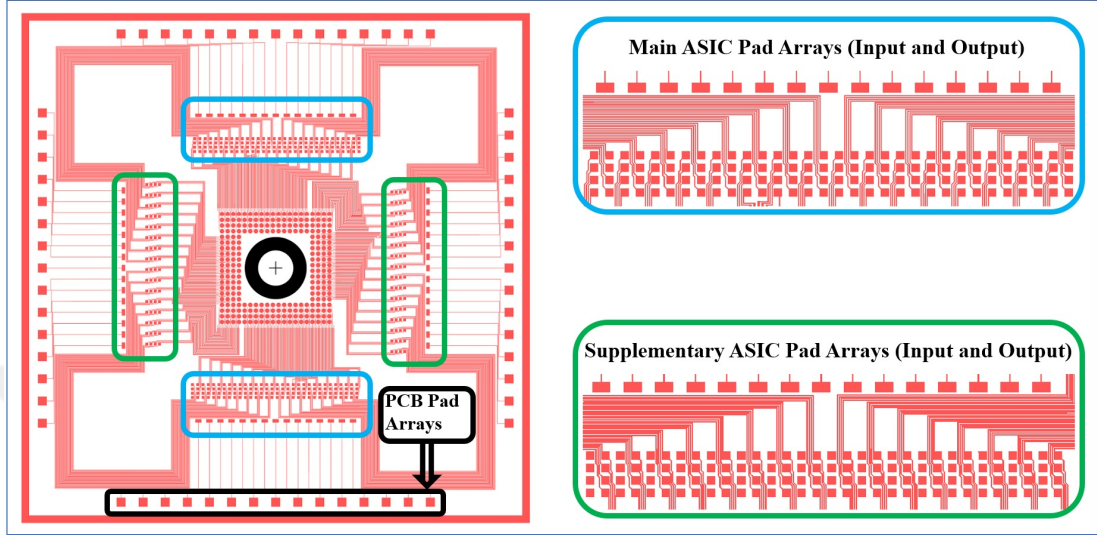


Figure 2.2: Chip-size drawing of CMUT Array Sensor displaying main ASIC pad arrays, supplementary ASIC pad arrays, and the PCB pad arrays.

Resonance Frequency	5.75 MHz
Cell Shape	Circular
Number of Total CMUT Cells	256
Membrane Thickness	12 microns
Membrane Radius	75 microns
Gap Height	150 nanometers
Insulator Layer Thickness	150 nanometers

Table 2.1: Given design input parameters for the CMUT Arrays Chips to be manufactured.

2.2 Mask Design and Fabrication

The batch-compatible microfabrication of CMUT array MEMS chips were completed using 4 masks. The 3 photomasks were created using a layout editor software and then manufactured by a laser mask writer (Heidelberg DWL 66FS) in our cleanroom. 1 shadow mask (stencil mask) was produced by PCBWay China. Subsequently, the photomasks were used to pattern the photoresist masks on the substrate utilizing the photolithography technique, while the shadow mask was directly used to deposit the needed materials (Cr-Au stack).

The first mask was used to form the CMUT gap and metallization of the bottom electrodes and wirings for CMUTs. The second mask was used for the purpose of etching the previously blanket deposited ALD (atomic layer deposition) alumina insulating layer from the designated electrical pad locations. The use of the third mask (stencil shadow mask) facilitated the deposition of metal pads for wire bonding connections on the device layer silicon. The stencil mask was used to simplify the microfabrication process flow by eliminating one photolithography step. The fourth and last mask was used to pattern the silicon device layer of the silicon-on-insulator (SOI) wafer. The chip-scale drawings of all four masks are shown in Figure 2.3.

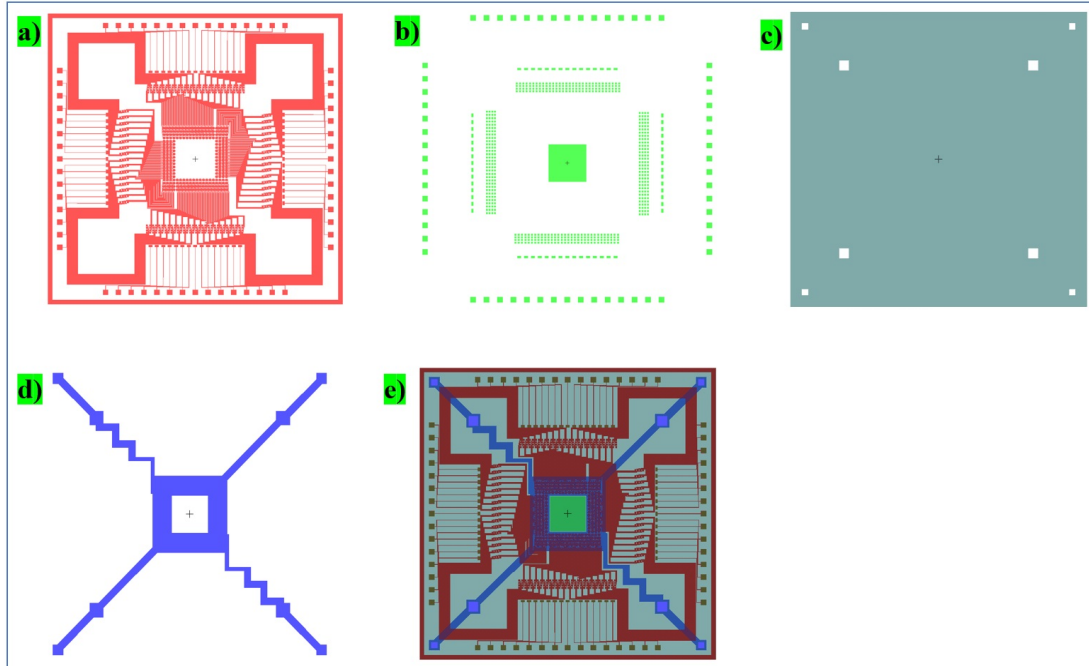


Figure 2.3: Chip-size drawings of microfabrication masks for the CMUT Devices: (a) Mask 1 (cavity formation and metallization), (b) Mask 2 (insulation layer patterning), (c) Mask 3 (metal pads deposition for wire bonding connections of device layer), (d) Mask 4 (device layer patterning), (e) All 4 masks aligned on top of each other.

2.3 Fabrication of CMUT Cavity and Bottom Electrode

Studies related to the microfabrication of the CMUT cavities and bottom electrodes were completed by Doğu Kaan Buğra Özyiğit, a former graduate student from our research group [31]. The information under section 2.3 is given to have brief information about the previously done microfabrication work related to these CMUTs.

2.3.1 CMUT Cavity Formation

The fabrication procedure started using a clean borosilicate wafer, named Pyrex 7740. The wafer was subjected to a thorough cleaning process using acetone, isopropyl alcohol, and deionized water. Lithography was done using a photomask to pattern the photoresist mask (Mask 1) to form a cavity on the Pyrex wafer. A chromium layer, with a thickness of about 50 nm, was used as both a hard mask and an adhesive layer for the photoresist mask. The argon plasma reactive ion etching was done for anisotropic etching of the chrome hard mask using an inductively coupled plasma (ICP) instrument. The approximately 850 nm deep cavities inside the Pyrex substrate were successfully formed using argon and SF_6 plasma based anisotropic reactive ion etching in the ICP and wet isotropic buffer oxide etching (BOE 7-1), respectively. The chip size drawing of the bottom electrode fabrication mask and the cross-sectional view of the CMUT cell are shown in Figure 2.4.

2.3.2 Metallization of the CMUT Gap

The CMUT cell cavities were partially filled with electron beam (e-beam) deposited approximately 100 nm thick layer of titanium (Ti) metal as the adhesion

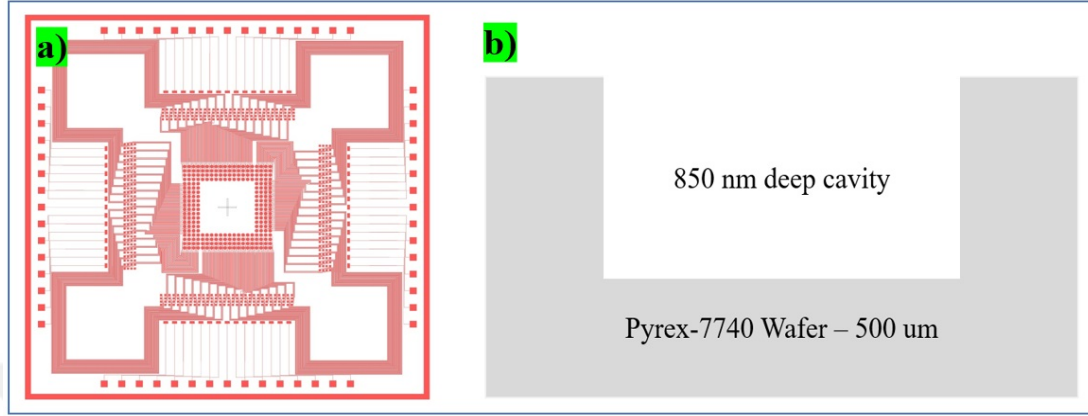


Figure 2.4: CMUT Cavity Formation: (a) Chip size drawing of the fabrication Mask 1, (b) Schematic of a CMUT cell showing its cross-sectional view after cavity formation.

and getter layer, followed by approximately 100 nm of platinum (Pt) as the barrier layer, and approximately 500 nm of gold (Au) as the bottom electrode with low electrical resistance. The 500 nm thick Au layer was deposited to enhance the reliability of the integration processes, such as wire bonding, ball bumping, and flip chip bonding for studies after the completion of the microfabrication of the CMUT array chips. A final gap height of approximately 150 nm was attained for CMUT cells by depositing a stack of three metals (Ti-Pt-Au) with a total thickness of approximately 700 nm inside an approximately 850 nm deep cavity. The metals were deposited using physical vapor deposition utilizing the electron-beam evaporator (Vaksis MiDAS Ankara, Turkey). Figure 2.5 shows the chip size drawing of the bottom electrode fabrication mask and the cross-sectional view of the CMUT cell after metallization.

2.3.3 Photoresist Lift-off Process

Following the deposition of metals in CMUT cavities and above the photoresist mask, the sacrificial layer of photoresist mask was removed using a process called lift-off. The piranha wet etching was carried out for the lift-off procedure because the photoresist mask was hard-baked before e-beam evaporation to retain its dimensions during metal deposition, so only acetone treatment was insufficient to

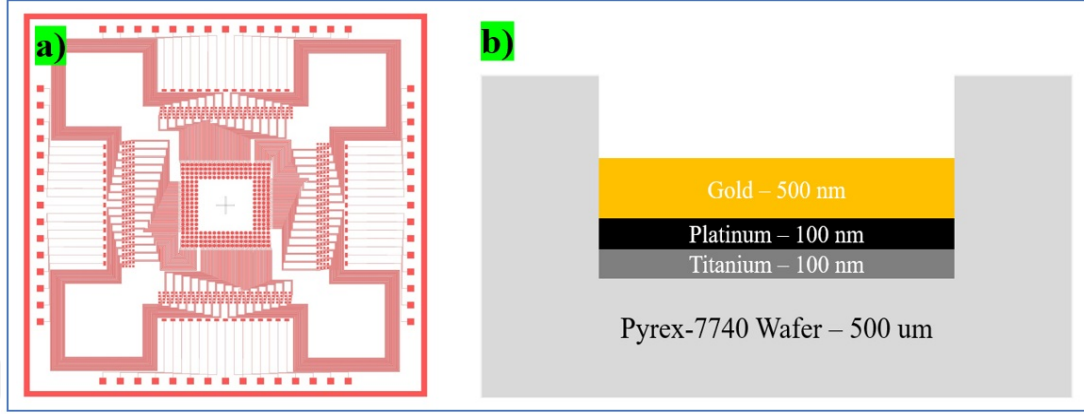


Figure 2.5: Metallization of the CMUT Gap: (a) Chip size drawing of the fabrication Mask 1, (b) Schematic of a CMUT cell displaying its cross-sectional view after the metals were deposited.

remove the hard baked photoresist. The piranha etching chemistry was prepared by adding 1 unit of hydrogen peroxide (H_2O_2) in 3 units of sulfuric acid (H_2SO_4) [36]. The piranha etch takes a long time, and there is a risk that piranha etchant may penetrate and etch titanium beneath the layers of gold and platinum, damaging the bottom electrode. Therefore, the acetone treatment was carried out before the piranha etch to assist in the lift-off process and lessen the burden on Ti layer from the piranha solution. The chrome hard mask was also removed after photoresist lift-off using wet chrome etchant (MicroChemicals, TechniEtch-Cr01).

2.3.4 Insulation Layer Deposition

Atomic layer deposition (ALD) is a special chemical vapor deposition (CVD) process. In ALD, a monolayer of one precursor gas is attached to the surface of the substrate with the help of chemisorption until the saturation point is reached. After saturation point, the left-over gas is pumped away from the process chamber, and the same process is repeated with another gas precursor to deposit a second monolayer on top of the initially deposited monolayer. The deposition cycles of both precursor gases are repeated until the desired coating thickness is achieved. Conformal coating and strong coating adhesion because of covalent bonding are two important advantages of ALD in the semiconductor industry [37].

A thin layer of alumina (Al_2O_3), 150 nm, was deposited on the surface of the whole wafer using atomic layer deposition (ALD) process and ALD equipment (Veeco-Savannah) to avoid the possibility of short-circuits between the top and bottom electrode that may happen during the operation of CMUT devices. The alumina was deposited using the conformal thermal atomic layer deposition method; therefore, the gap height of 150 nm for the CMUT cell cavities was maintained. The chip size drawing of the bottom electrode fabrication mask and the cross-sectional view of a CMUT cell after depositing the insulation layer can be seen in Figure 2.6.

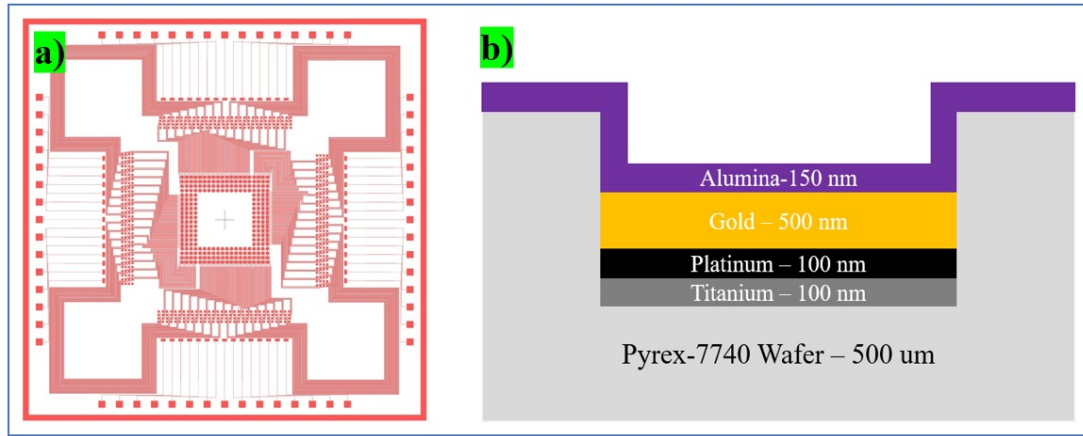


Figure 2.6: Conformal deposition of insulation layer: (a) Chip size drawing of the fabrication Mask 1, (b) Schematic of a CMUT cell displaying its cross-sectional view after the insulation layer (Al_2O_3) has been deposited.

2.3.5 Insulation Layer Patterning

As explained in the previous section 2.3.4, the device side of the wafer was covered with a conformal layer of alumina insulation. It is necessary to remove the insulating layer from the electrical pad areas, such as ASIC pads and PCB pads, since these pads will be used to make electrical connections between pads of ASIC chips and pads of PCB (printed circuit board) using flip-chip bonding, and wire bonding approached [32]. The alumina from the central region of the CMUT chip, where the central region of the CMUT chips is reserved for light transfer via a laser-fiber, is also removed. Furthermore, the non-uniformly deposited ALD

alumina at the back side of the wafer is also removed from the back side of the wafer, because there was no mask at the back side of the wafer.

The diluted AZ 400K developer solution was used to slowly etch alumina from the designated areas, as highlighted by the Mask 2 design in Figure 2.7. A combination of e-beam evaporated chrome hard mask, and hardened photoresist mask patterned the ALD alumina insulator layer. Because of low etch rates (i.e. approximately 1.25 nm/min. [31]), ALD alumina etching takes a few hours. During this long etching process, the hardened photoresist mask gradually degrades and should not be relied on for etching the ALD alumina. So, the Cr hard mask under the hardened photoresist protects the potential alumina etching from other regions. Following the ALD alumina etching, the chrome mask and remaining photoresist were removed from the surface of the wafer using AZ 100K remover and chrome etch (CR-7) in the given order. Etching the alumina layer from electrical pad regions prepared the wafers for the anodic wafer bonding process.

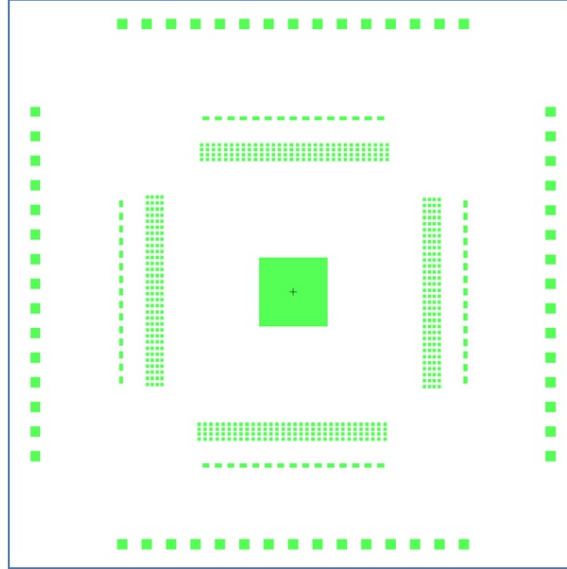


Figure 2.7: Chip-size drawing of the insulation layer patterning mask (Mask 2).

2.4 Anodic Wafer Bonding

Studies related to anodic wafer bonding were completed in collaboration with EVG from Austria during the studies of Doğu Kaan Buğra Özyiğit, a former graduate student from our research group [31]. The information under section 2.4 is given to have brief information about the previously done microfabrication work.

Anodic wafer bonding is a process where silicon and glass wafers are bonded together by applying a voltage between 200 and 1000 volts and heating the wafers to a temperature range of 200°C to 450°C. The glass wafer is connected to the negative terminal, while the silicon wafer is connected to the positive terminal of the power source. The sodium ions from the glass wafer are attracted toward the cathode, creating the depletion region for the positive charges that enhance electrostatic attraction between glass and silicon wafers. Consequently, oxygen ions from the glass substrate migrate to the interface and form Si-O-Si bonds by converting Si to SiO₂ [38]. The schematic in Figure 2.8 highlights the reaction occurring at the depletion layer [38].

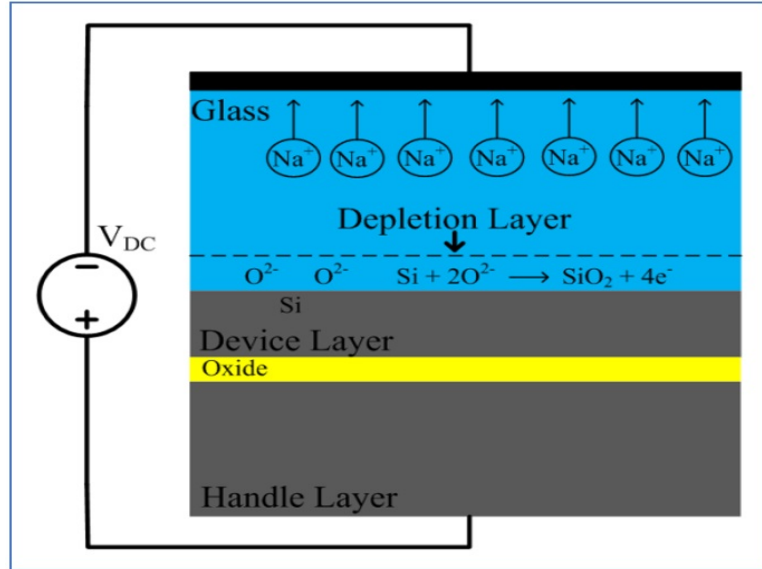


Figure 2.8: Schematic of anodic wafer bonding process between Silicon and Glass wafers.

The process development for anodic wafer bonding between Pyrex-7740 and silicon-on-insulator (SOI) wafers took place at the cleanroom facilities of EVG in Austria, with significant assistance from the technical team at EVG. A total of 8 pairs of Pyrex and SOI wafers were utilized for the process development and optimization. The wafer bonding quality of Bond 7 and Bond 8 wafer pairs were superior compared to the other 6 wafer pairs [31]. During the optimization of anodic wafer bonding, the process temperature was reduced significantly from 450°C to 350°C [31].

2.5 Top Electrode Fabrication

A total of 8 pairs of wafers were obtained after the anodic wafer bonding procedure was completed. The wafers underwent further microfabrication procedures to obtain the CMUT sensor chips. The following microfabrication steps include the removal of the handle layer, removal of the buried oxide layer, deposition of blanket layers, deposition with shadow mask (stencil), and patterning of the device layer.

2.5.1 Removal of Handle Layer

The inductively coupled plasma (ICP) reactive ion etcher is used for plasma etching of silicon to micro-manufacture micro and nanoelectronic devices. It uses gas plasma created by the magnetic field of a current-carrying coil and provides high etching rates with high selectivity. The ICP machines have a significant capability for both anisotropic silicon structures with high aspect ratios or isotropic silicon etching [39].

The wafer pairs received from EVG after anodic wafer bonding were cleaned with deionized water, acetone, isopropyl alcohol (IPA), and finally with deionized water again to remove the dust and other potential impurity particles. The appearance of the device side of the wafer pair after the wafer bonding can be seen in Figure 2.9. Maskless reactive ion etching was utilized for isotropic etching of 350 ± 25 microns thick silicon handle layer of the silicon-on-insulator (SOI) wafer, and SF_6 was used as the primary gas plasma in ICP tool. Prior to etching the actual wafer, the ICP chamber was conditioned with SF_6 plasma gas for about 10 minutes using a test Pyrex wafer.

The wafer was transferred to the reaction chamber of the ICP after the chamber was conditioned with SF_6 gas plasma. The silicon handle layer had a significant thickness of 350 microns, which took 4 to 5 hours of processing time to etch the handle layer completely from each wafer. The etching time slightly differs

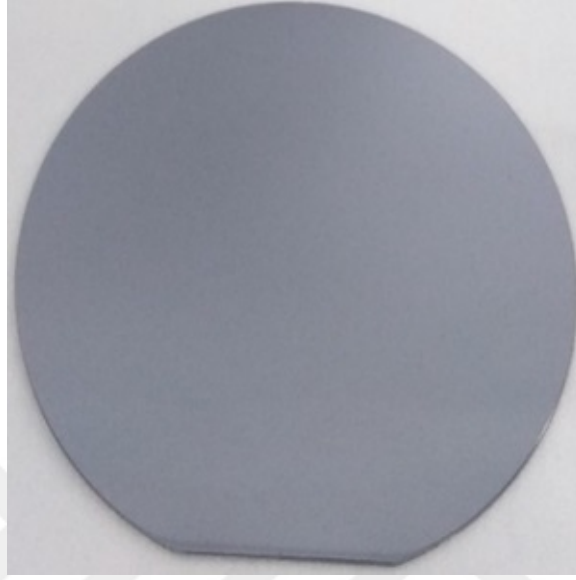


Figure 2.9: The wafer pair of Pyrex-7740 and SOI after anodic wafer bonding. Image is taken from the silicon handle layer side of the SOI wafer, while the Pyrex wafer is below the SOI wafer in this view.

from wafer to wafer due to the thickness variations on the handle layers of the SOI wafers. The etching time of all wafers is shown in Table 2.2. The clamp fingers securely grip the wafer inside the ICP chamber during the etching process. However, part of the silicon handle layer below the clamp fingers remains unetched due to the lack of exposure to the etching plasma. Therefore, the wafer was rotated every 10 minutes in order to etch the unexposed portion of the silicon handle layer.

During the removal of the handle layer, the buried oxide layer beneath the handle layer started appearing, and the process was stopped after the Si handle layer was removed entirely. Figure 2.10 displays an image of the wafer with a partially removed handle layer. An over-etching of one to two minutes was done in order to guarantee the thorough elimination of the silicon handle layer.

Figure 2.11 shows the wafer after the complete removal of the handle layer. Edges of the wafer pair were transparent after the removal of the handle layer because handle layer removal was a long process, and etching (i.e., etch rate) is significantly faster at the edges, so at the edges of the bonded wafer pair, the

Wafer no.	Total Etching Time (in minutes)
Bond 1	It was not recorded.
Bond 2	280
Bond 3	280
Bond 4	290
Bond 5	290
Bond 6	320
Bond 7	320
Bond 8	310

Table 2.2: Handle layer etching time for the 8 CMUT wafers.

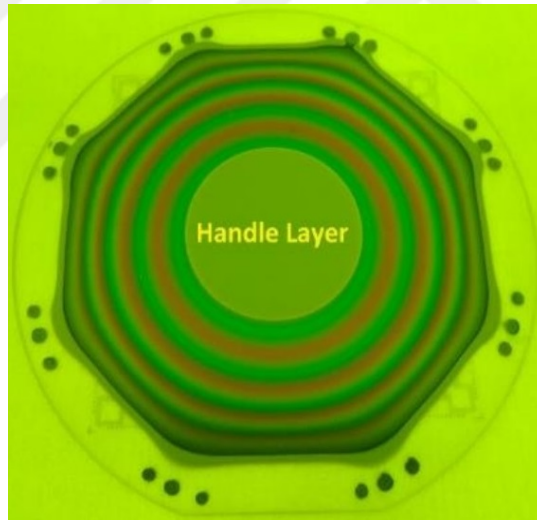


Figure 2.10: Pyrex-SOI wafer pair with partially removed handle layer.

buried oxide layer and silicon device layer of the SOI wafer are fully etched. This significant etch rate difference related issue is known for such ICP tools. Hence, we were aware that the edges of the wafer will not be suitable to obtain functional CMUT chips. The transparent wafer edges can be seen clearly in Figure 2.11.

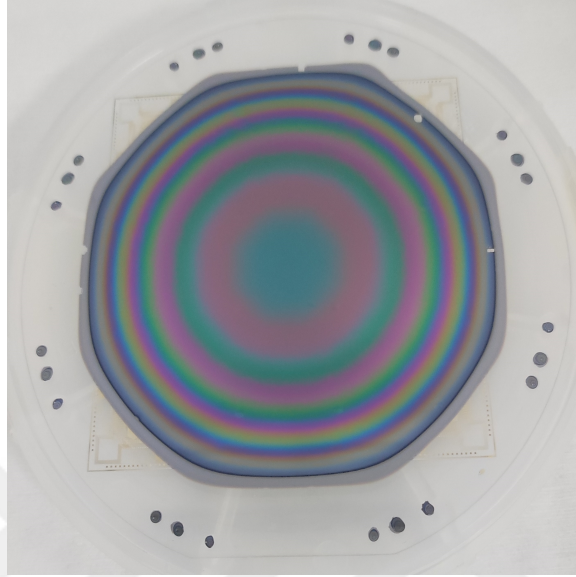


Figure 2.11: Pyrex-SOI wafer pair after complete removal of the handle layer.

2.5.2 Removal of Buried Oxide Layer

The buried oxide (SiO_2) layer in the SOI wafer is to electrically isolate the bulk handle layer from the thin silicon device layer. The reason behind the circular ring shaped brownish and greenish colors of the buried oxide (BOX) layer in Figure 2.11 is the variations in the thickness of the BOX layer across the diameter of the wafer due to plasma etch rate differences from the handle layer removal process. This variation in the thickness of the BOX layer occurred as a result of its exposure to the SF_6 plasma during handle layer etching. In order to access the silicon device layer of the bonded wafer-pair, it is essential to remove the BOX layer, the second layer of the silicon-on-insulator (SOI) wafer.

Buffer oxide etch (BOE) is a liquid etchant that selectively removes thin layers of insulating materials, including oxides and nitrides, often used in microfabrication processes [40]. BOE is a mixture of ammonium fluoride (NH_4F) and hydrofluoric acid (HF) and is available in different concentrations. The ammonium fluoride functions as a buffer, effectively regulating the etching rate of the process [41].

An isotropic wet-etching process using a buffered oxide etching solution (BOE 7-1) was performed on the wafer to eliminate approximately 1-micron thick BOX layer. The wafer pair was immersed in the pure BOE solution until the circular ring-shaped brownish and greenish-colored buried oxide layer disappeared (i.e., etched). Because the BOX is thinner towards the edges of the wafer and thicker at the center of the wafer and due to the naked eye observable effects of BOE, the etching of BOX layer started from the edges and slowly moved toward the center of the wafer pair, as seen in Figure 2.12.

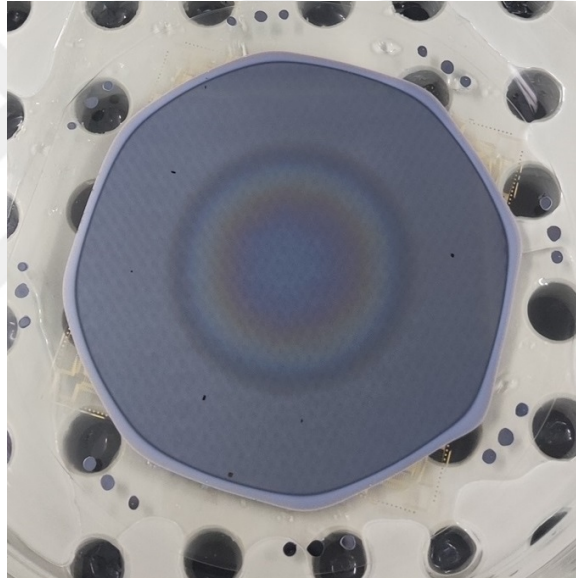


Figure 2.12: Pyrex-SOI wafer pair with partially removed BOX layer.

Following the complete removal of the BOX layer, the underlying grey colored silicon device layer of the wafer became visible. The wafer was immersed in fresh deionized (DI) water to remove the residues of BOE etchant from the surface of the silicon device layer and the exposed interface of the device layer silicon and ALD alumina coated Pyrex wafer. Since the poorly bonded parts of the silicon device layer of the wafer pair had a risk of peeling, extra care was taken while wet-etching and nitrogen-blowing to minimize damage to the silicon device layer. The image of the wafer after BOX layer removal is shown in Figure 2.13.



Figure 2.13: Pyrex-SOI wafer pair after complete the removal of BOX layer (with Si-device layer on top).

The wet-etching process for the 1-micron thick BOX layer typically requires around 15 to 20 minutes of etching time. The etching time for each wafer is shown in Table 2.3. The variation in etching time across all the wafers may be attributed to BOX thickness variations from wafer to wafer and other possible non-controlled parameters of the cleanroom, such as room temperature and temperature of the BOE wet etchant.

Wafer no.	Total Etching Time (in minutes)
Bond 1	It was not recorded.
Bond 2	17
Bond 3	16
Bond 4	14
Bond 5	22
Bond 6	20
Bond 7	18
Bond 8	17

Table 2.3: BOX layer etching time for the 8 CMUT wafers.

Given the hydrophobic nature of the silicon device layer (revealed after the etching of BOX layer), a "water slip test" was conducted to verify the thorough elimination of the BOX layer. Figure 2.14 depicts a water slip test in which the water stays on the center of the wafer due to an un-etched BOX layer. Silicon is vulnerable to forming very thin oxide layers of about 2 nm at ambient conditions [42]. Therefore, it is crucial to immediately process the wafer for the next micro-fabrication step to avoid forming native oxide (SiO_2) on the silicon device layer that is exposed to ambient conditions.

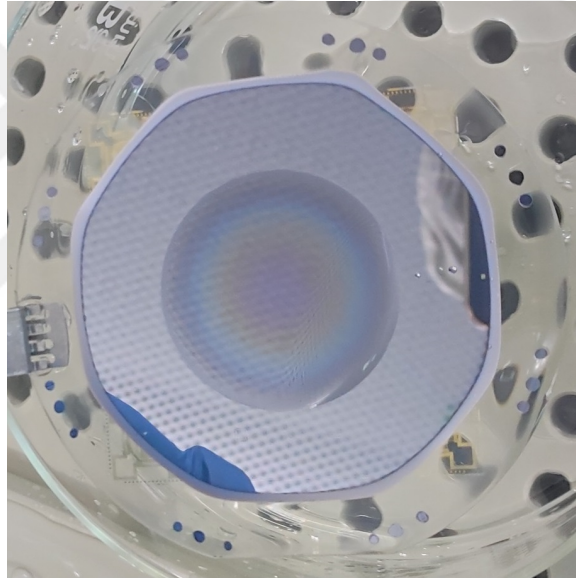


Figure 2.14: Pyrex-SOI wafer pair with stagnant water on its surface (because of the un-etched the BOX layer) during water-slip test.

2.5.3 Deposition of Blanket Layers

The silicon device layer of the wafer pair is accessed after removing the buried oxide layer. Following that, the wafer was blanket-deposited with a stack of chrome (Cr), gold (Au), and chrome (Cr) layers in the respective order. A thermally stable tape (Kapton) was used to cover the alignment marks on the wafer to prevent them from being coated because the alignment marks will be used in subsequent microfabrication processes. Figure 2.15 shows the wafer after masking its alignment marks with the Kapton tape.



Figure 2.15: Pyrex-SOI wafer pair after masking its alignment marks with the Kapton tape.

The wafer was fixed on the wafer holder using Kapton tape to prevent any damage that may occur from possible falls inside the chamber during the e-beam evaporation process. The chamber pressure of $3\text{E}-6$ Torr was attained inside the electron beam (e-beam) evaporator in order to begin the deposition. The deposition rate in the e-beam evaporator was maintained at $0.1 - 0.3 \text{ \AA/s}$ during the first 5 nm to 10 nm of coating for less residual stress on the deposited material. The deposition rate was increased to $1 \text{ \AA/s}$ until the required thickness of the coating was attained.

A layer of chromium with a thickness of 35 nm was applied onto the silicon device layer of the wafer using physical vapor deposition in an e-beam evaporator. This layer serves as an adhesion layer for the subsequent gold layer. Following that, 50 nm gold was deposited to enhance the electrical conductivity of the silicon device layer. A 35 nm chromium layer was deposited on top of the gold layer to function as an adhesive layer for the photoresist. The top (second) chrome layer also functions as an indicator for photoresist removal during the oxygen plasma process because oxygen plasma also etches the chrome. All three layers were deposited simultaneously during a single deposition cycle using the e-beam evaporation. Figure 2.16 displays the wafer after depositing the Cr-Au-Cr metal stack.



Figure 2.16: Pyrex-SOI wafer pair after blanket deposition of Cr-Au-Cr layers.

A brand-new quartz microbalance with more than 90% life was used to monitor the real-time coating rates. A test chip was coated with thin layers of chrome and gold, and the thickness of the film was examined using a Keyence VK-X100 laser scanning confocal microscope. However, Figure 2.17 illustrates that the coating thickness measured by the confocal microscope was different from the one computed by quartz microbalance.

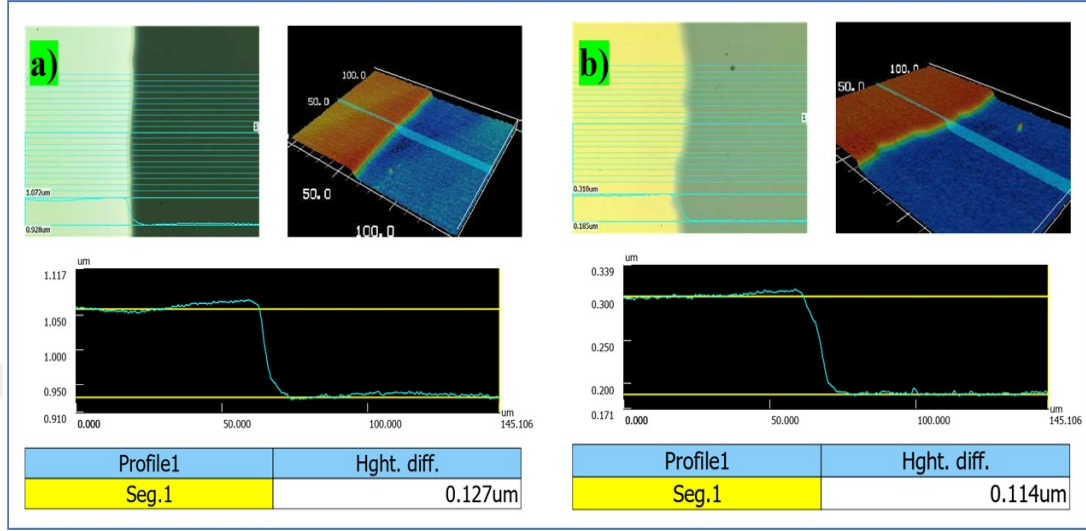


Figure 2.17: Film thicknesses of Chrome and Gold layers measured by the laser scanning confocal microscope (Keyence VK-X100).

The quartz microbalance did not receive the same deposited mass as the wafer because the position microbalance was different from that of the wafer during evaporation. The relationship between the mass and resonance frequency of the microbalance is not direct anymore, demanding optimization of the tooling factor. Furthermore, the density of the thin film differs from the density of the bulk metal used to calculate the thickness of the film [43]. The percentage tooling factor was computed using Equation 2.1 to identify the discrepancy between the film thickness and the thickness calculated by the microbalance. A tooling factor below 100% indicates that the thickness of the deposited layer is lower than what is displayed on the thickness monitor and vice versa [44]. The calculated tooling factor, as shown in Table 2.4, was recorded in the thickness monitor in order to achieve the desired film thickness on the actual wafer.

$$\text{Tooling Factor Percentage} = \left(\frac{\text{Thickness}_{\text{measured}}}{\text{Thickness}_{\text{calculated}}} \right) * 100 \quad (2.1)$$

Note: The etching combination of Cr-Au-Cr presents significant challenges during chrome wet-etching process due to the very high etch rates of chrome etchant (MicroChemicals, TechniEtch-Cr01), resulting in the formation of large

Material	Calculated Thickness	Measured Thickness	Tooling Factor (in %)
Chrome	100 nm	127 nm	127
Gold	100 nm	114 nm	114

Table 2.4: E-beam Evaporator tooling factors calculated for Chrome and Gold metals.

undercuts under the photoresist mask when Au thin-film is above or below the Cr layer. Depositing a titanium, gold, and titanium (Ti-Au-Ti) metal stack may be a good alternative to the challenging Cr-Au-Cr stack.

2.5.4 Deposition with Shadow Mask (Stencil)

The Kapton tape was removed from both alignment mark sides of the wafer after the deposition of the blanket layers. The majority of wafers have alignment marks visible on one side but are partly covered by the silicon device layer on the other side. Alignment marks under the device layer were exposed by scratching the device layer with a mechanical scribe, and then any remaining residues were removed using Kapton tape. Figure 2.18 displays the optical microscope images of the alignment marks on the left and right sides of the wafer after they were revealed.

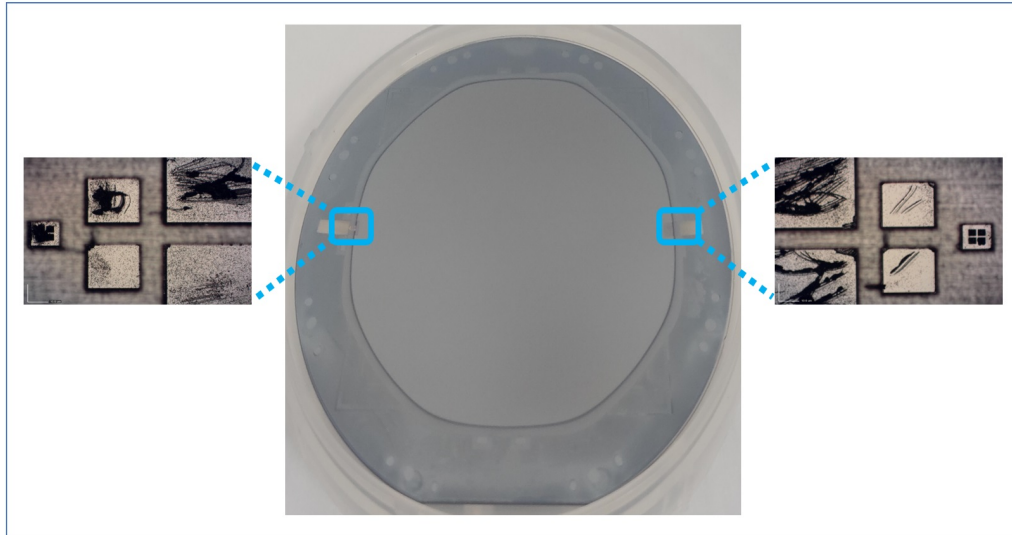


Figure 2.18: Optical microscope images of the alignment marks of the Pyrex-SOI wafer pair revealed by the mechanical scribing.

Under the optical microscope, the stencil shadow mask (Mask 3) was then manually aligned with the wafer using the alignment marks. The Kapton tape was used to attach the stencil mask to the wafer. Figure 2.19 shows optical microscope images of alignment marks after the stencil mask was aligned with the wafer.

An adhesion layer of 30 nm chromium was deposited on the wafer using e-beam evaporation in preparation for the gold deposition. Subsequently, a layer of gold with a thickness of 500 nm was applied to construct electrical pads for wire

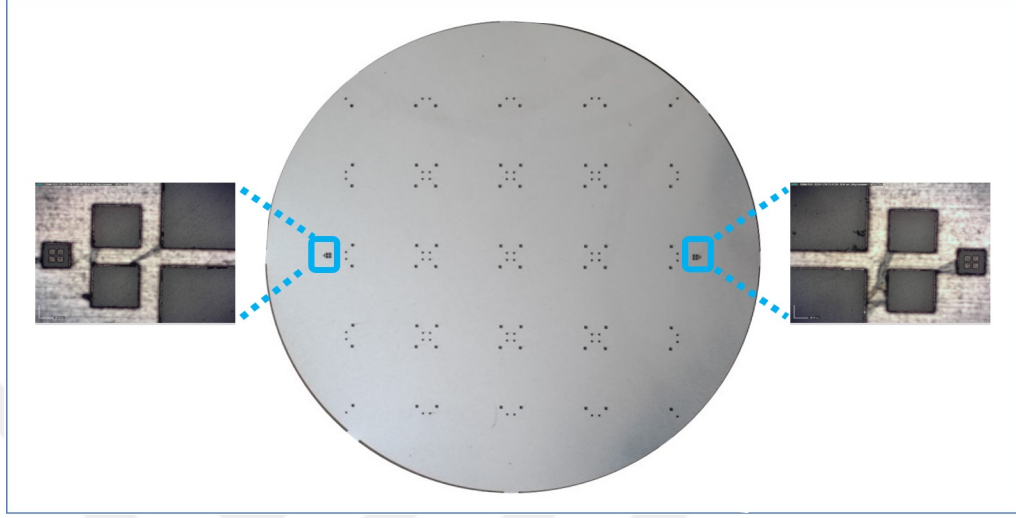


Figure 2.19: Optical microscope images of alignment marks after the Pyrex-SOI wafer pair was aligned with the stencil mask (Mask 3).

bonding the silicon device layer to the printed circuit board (PCB). The purpose of the deposited gold pads is to facilitate the transmission of the electrical signal from the CMUT sensor chip to the signal processing system via the PCB. The deposition was initiated once a chamber pressure of $3\text{E}-6$ Torr was attained inside the e-beam evaporator. The updated tooling factor was used for depositing both metals. The images of the wafer after the deposition of the electrical pads can be seen in Figure 2.20.

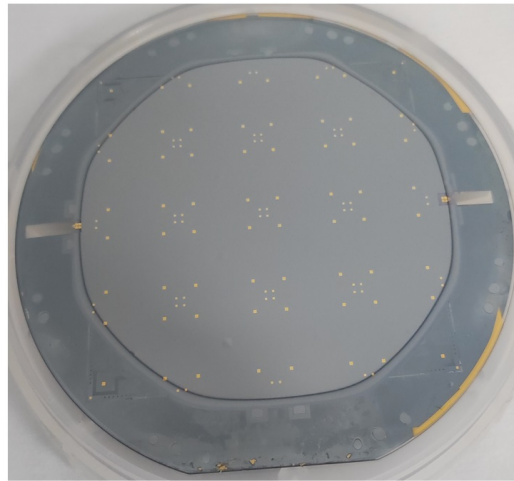


Figure 2.20: Pyrex-SOI wafer pair after depositing the electrical pads using shadow mask (Mask 3).

2.5.5 Patterning of Device Layer Silicon

The silicon device layer of the wafer was patterned with photolithography, a sequence of wet etching steps to etch the Cr-Au-Cr stack, and deep reactive ion etching (Bosch process) processes in the respective order. The channel gaps (where the wires between the CMUT bottom electrodes and ASIC connection pads are located) that provide access to the CMUT cell cavities will be opened after the device layer is patterned with the deep reactive ion etching (Bosch process).

2.5.5.1 Photolithography

A photoresist mask was required for the wet etching and deep reactive ion etching of the silicon device layer. Initially, the spin coater was cleaned from impurities using a pure acetone solution. The spin coater was conditioned by spinning hexamethyldisilazane (HMDS) using a clean silicon test wafer. The real wafer was then spin-coated for a minute with a thin layer of HMDS on the blanket Cr-Au-Cr coated silicon device layer using 2000 RPM and 1000 acceleration values. The HMDS was used as an adhesion promoter for the subsequent photoresist mask. The wafer was then heated at 150°C on a hot plate for 30 minutes to remove excess solvent from the HMDS layer. The Bond 3 wafer suffered breakage during the HMDS spinning process; an image of the broken wafer is shown in Figure 2.21. In order to avoid any further possible wafer breakages resulting from the vacuum created by the substrate holder part of the spin coater, the wafer was securely attached to a Pyrex support wafer.

The spin coater underwent a second cleaning process using acetone after the application of HMDS coating. The spin coater was conditioned with the AZ 5214E image reversal photoresist using a clean silicon test wafer. The photoresist was spin-coated on the real wafer for 60 seconds at an RPM of 2000 and acceleration of 1000 to get approximately 1.98-micron thick layer of photoresist according to the data sheet of the photoresist. A thick photoresist bead formed along the edge

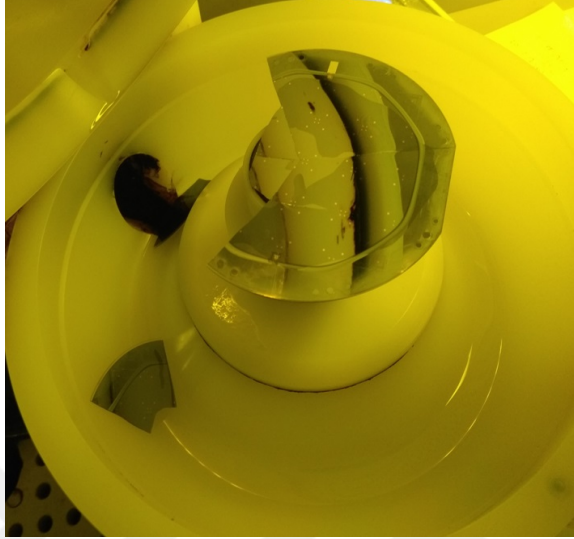


Figure 2.21: Bond 3 Pyrex-SOI wafer pair that was broken during spin-coating.

of the wafer was manually removed with a Q-tip. The wafer was placed on a hot plate at 110°C for 50 seconds to pre-bake the photoresist. No reversal baking was done since the AZ 5214E photoresist was utilized in positive mode. Figure 2.22 displays the real wafer after spin coating the photoresist.

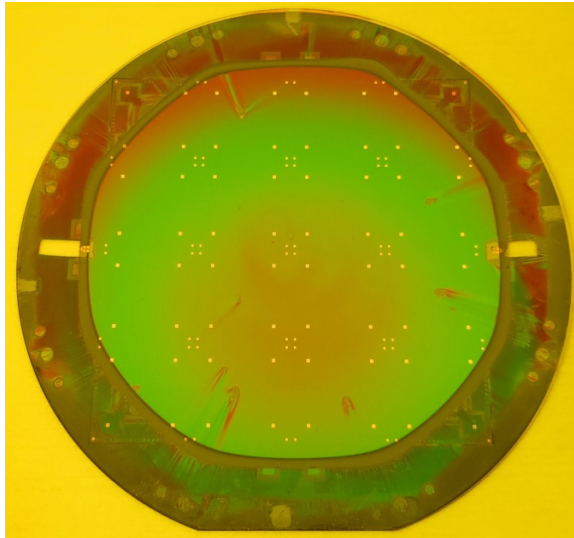


Figure 2.22: Pyrex-SOI wafer pair coated with a layer of AZ 5214E photoresist.

The ultraviolet (UV) light dose and the photoresist development time were optimized using a contact aligner system (EVG 620) before working with the real wafer. Three silicon test wafers were spin-coated with a 1.98-micron thick layer

of AZ 5214E positive photoresist. Subsequently, the test wafers were subjected to varying UV exposure levels: 20 mJ.cm^{-2} , 30 mJ.cm^{-2} , and 40 mJ.cm^{-2} . The test wafer exposed to 30 mJ.cm^{-2} of UV dose and underwent photoresist development with AZ 400K for 2 minutes gave the best results. Sharp photoresist features upon development were verified by optical microscope examination, and no evidence of underdeveloped photoresists was found in any other areas. The silicon test wafer following successful photoresist development is shown in Figure 2.23. The scratch test was also performed on the test wafer to confirm the photoresist development, as seen in Figure 2.24.

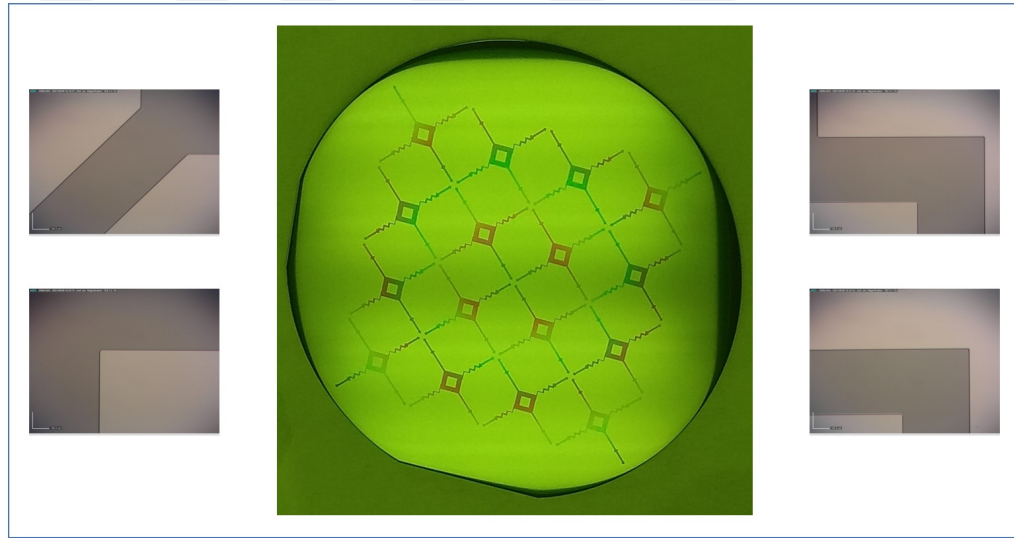


Figure 2.23: Silicon test wafer along with optical microscope images of well-defined (or sharp) photoresist features showing successful development.

In the event of overexposure of the photoresist, the removal of the device layer from only the specific desired areas may be challenging, perhaps leading to the loss of delicate details. Conversely, if the photoresist is underexposed, it might result in incomplete development and insufficient pattern definition. Likewise, in the case of an undeveloped photoresist, there will be a significant amount of photoresist residues on the surface of the wafer. The photoresist overdevelopment results in the removal of excess photoresist, the loss of sharp details, and changes in the size of the features. Therefore, achieving the best outcomes requires finding a trade-off between the amount of UV exposure and development time for the photoresist.



Figure 2.24: Photoresist feature on the Silicon test wafer underwent the Scratch Test after photoresist development.

The photomask, Mask 4, shown in Figure 2.25, was securely positioned inside the mask aligner to facilitate the photoresist patterning. The recipe for the mask aligner was created using the optimized parameters, including contact mode, separation, photomask thickness, wafer thickness, photoresist thickness, and exposure dosage. The recipe parameter values for the mask aligner are shown in Table 2.5. The proximity method was selected because the lateral dimensions of the smallest feature on Mask 4 were over 200 microns, making them non-critical. Moreover, the wafer surface could not be flat anymore because the wafer had undergone several microfabrication processes (i.e., ALD alumina deposition, anodic wafer bonding, SOI handle layer removal) that may induce stress and warpage on the wafer. Therefore, to compensate for the wafer warpage, contact mode lithography was avoided (i.e., proximity mode exposure was used) during UV exposure on the mask aligner to have an easier alignment procedure between the wafer and glass photomask. From the other side, working with proximity mode of the mask aligner limits the critical dimension that can be obtained with the mask aligner. Fortunately, the dimensions of this mask were large enough so that proximity mode exposure was acceptable.

Front-side alignment lenses may be used for alignment when alignment marks on the device side of the wafer are fully visible. However, removing the device

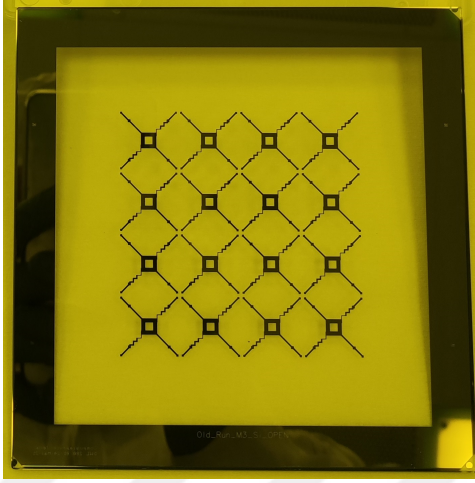


Figure 2.25: A photograph the device layer patterning photomask (Mask 4).

Process	Manual Bottom Side
Process Mode	Crosshair
Contact Mode	Proximity
Proximity Distance	40 microns
Separation	30 microns
Photomask Thickness	2.30 microns
Substrate Thickness	0.5 millimeters
Photoresist Thickness	1.98 microns
Exposure dose	30 mJ.cm ⁻²

Table 2.5: Recipe parameters of the mask aligner for UV exposing Pyrex-SOI wafer pair covered with AZ 5214E photoresist layer.

layer from the top of the alignment marks on the wafer with a mechanical scribe was a difficult task that may damage the device layer. The alignment markings on the Pyrex wafer were visible from the rear side because Pyrex is transparent. The wafer was precisely aligned with the photomask using the crosshair technique through the back-side alignment lenses of the mask aligner. Figure 2.26 displays the small alignment marks on the wafer after they were aligned with the cross-hair after the completion of the alignment operation. Once the wafer was properly aligned with the photomask, it underwent exposure to an optimum UV dose of 30 mJ.cm⁻² using the mask aligner.

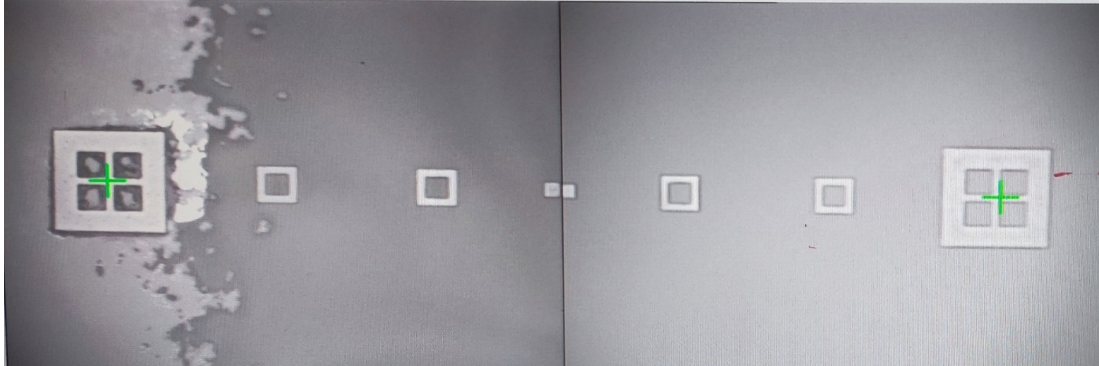


Figure 2.26: Screenshot of mask aligner after the back side crosshair alignment was completed: the green cross-hairs were aligned with the alignment marks on left and right side of the Pyrex-SOI wafer pair.

The photoresist was developed using diluted AZ 400K developer. The developer solution was prepared by combining 1 part of pure AZ 400K solution with 4 parts of deionized water. The wafer was agitated gently with a tweezer in order to assist the development of the photoresist. The positive photoresist regions exposed to the UV light were removed during development, resulting in the retention of the Mask 4 pattern on the wafer. The wafer was immersed in fresh deionized water to remove residues of diluted AZ 400K developer. The wafer was placed into a vacuum desiccator for about 10 minutes to eliminate the potential moisture at the interface. The wafer with the patterned photoresist mask can be seen in Figure 2.27.

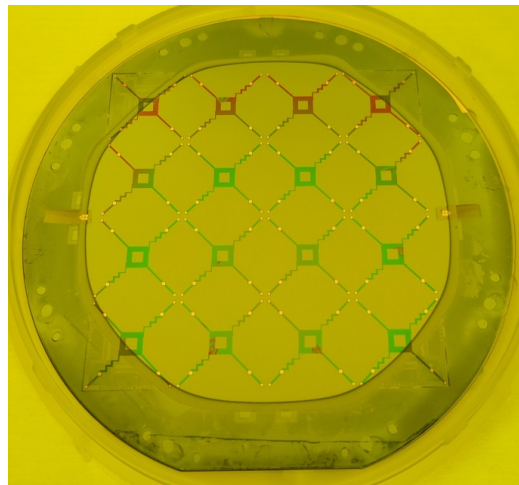


Figure 2.27: Pyrex-SOI wafer pair with patterned photoresist mask (Mask 4).

The alignment accuracy of the photoresist mask (Mask 4) after photolithography and development was verified using an optical microscope because it is crucial for the permanent patterning of the device layer in the coming process steps. The measurement was conducted on the corner devices of the wafer since they have the highest likelihood of misalignment, and the Si device layer at 4 corner chips were already etched during the handle layer removal step. The optical microscope measurements in Figure 2.28 indicate that the misalignment of Mask 4 falls within the given tolerance. Moreover, the CMUT cells of the corner chips are well aligned under the photoresist mask.



Figure 2.28: Optical microscope images displaying alignment accuracy measurements of the photoresist mask (Mask 4) on corner CMUT chips of the Pyrex-SOI wafer pair. Note: These optical images are taken from the back side of the Pyrex wafer, after Si device layer was also etched. Although not shown here, similar alignment accuracy inspection has been done on the corner chips from the front side of the Pyrex wafers before all the wet etching and Bosch process Si etching steps were performed, because all these etch processes are irreversible patterning processes.

Finally, the photoresist mask was hard-baked (after photolithography and development) at 110°C on the hot plate for about 1 minute to retain its profile for upcoming wet etching and dry etching processes.

2.5.5.2 Etching of Top Chrome layer

The chrome etching solution was prepared by diluting 1 unit of chrome etchant (MicroChemicals, TechniEtch-Cr01) with six units of deionized water. The top blanket-coated chrome layer of the wafer was selectively etched using a photoresist mask to expose the underlying gold layer. The wafer was dipped in the etching solution until the yellow-colored gold layer became visible, and the wafer was gently agitated with a metallic tweezer to assist the wet etching process. The wet etching process for removing a 35 nm chrome layer typically takes 3 to 5 minutes, which includes a further 10 to 20 seconds of over-etching to ensure the complete removal of chrome. It is crucial to be aware of the progress of the etch process by observing color changes. Figure 2.29 shows the wafer after the etching of the chromium layer. The etching time may vary between wafers owing to variations in the thickness of the chromium layer. Table 2.6 displays the etching duration for each wafer.

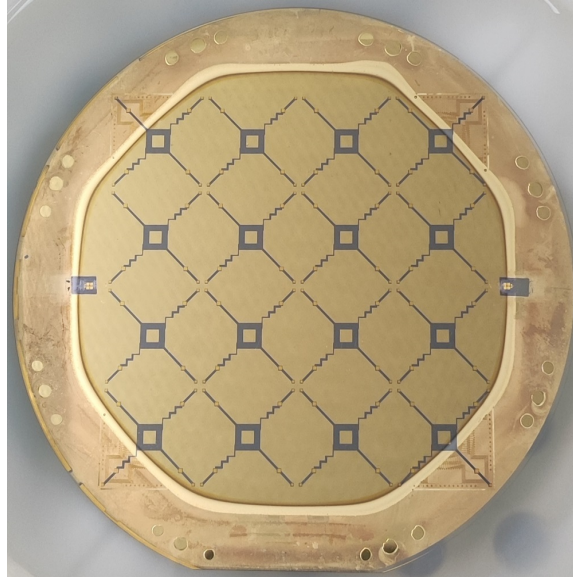


Figure 2.29: Pyrex-SOI wafer pair after etching the blanket-coated top chrome layer.

Etch rate of chrome etchant is relatively high, causing the formation of undercuts in the chrome layer above the gold layer and underneath the photoresist

Wafer no.	Etching Time (in minutes)
Bond 1	It was not recorded.
Bond 2	2.2
Bond 3	Not done because the wafer was broken.
Bond 4	3
Bond 5	5.5
Bond 6	2.2
Bond 7	2.8
Bond 8	2.5

Table 2.6: Wet-Etching time for top chrome layer of the Pyrex-SOI wafer pairs.

mask. Therefore, the wafer was removed from the etching solution immediately after the wet etching process was finished to prevent large undercuts in the chrome layer. Figure 2.30 displays a schematic of the undercut formed in the upper chromium layer. In order to eliminate the etch chemistry, the wafer was washed with fresh deionized water. Following that, the wafer was introduced into a vacuum desiccator for a duration of 10 to 20 minutes in order to eliminate moisture from the interface.

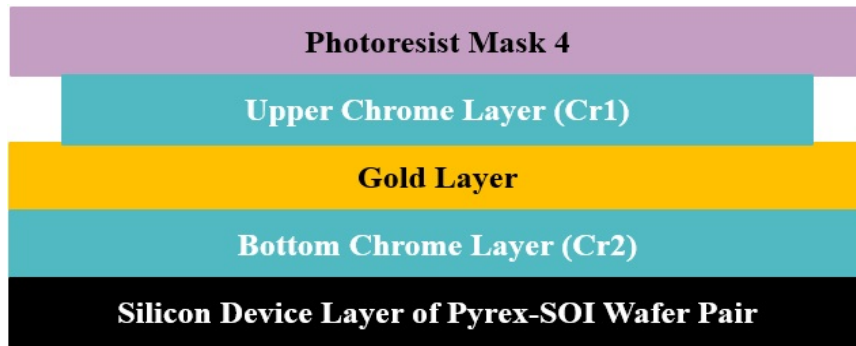


Figure 2.30: Schematic of the Cr-Au-Cr stack after etching the top chrome layer of the Pyrex-SOI wafer pair.

2.5.5.3 Etching of Gold Layer

The gold layer having a thickness of approximately 50 nm was removed by etching with Aqua Regia. The Aqua Regia solution was prepared by mixing 3 units of hydrochloric acid with 1 unit of nitric acid [45]. The etching solution was diluted by adding 2 units of deionized water since the gold layer that needed to be etched was quite thin (≈ 50 nm). The wafer was immersed in the prepared etching solution to etch the gold layer until the underlying grey-colored chromium layer became visible. The wafer after the gold layer etching can be seen in Figure 2.31. The wet etching process for the gold layer lasted around 30 to 40 seconds, which included an additional 10 seconds of over-etching to guarantee the thorough elimination of the gold. The etching time of each wafer is shown in Table 2.7.

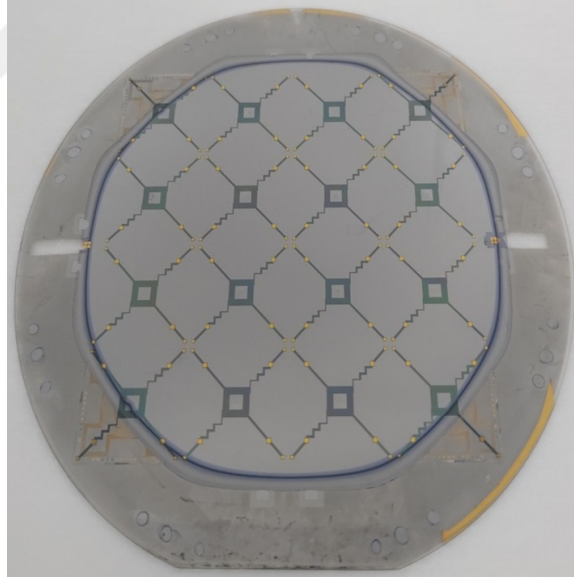


Figure 2.31: Pyrex-SOI wafer pair after etching of the blanket-coated gold layer.

Due to the formation of undercuts in the top chrome layer during the previous wet etching step, the chrome layer on top of the gold layer acted as a mask throughout the etching of the gold layer. Figure 2.32 presents a schematic representation of the undercut formed in the gold layer after etching. The undercut in the gold layer was not visible because it was positioned under the top chrome layer, which served as a mask during gold layer etching. After the wet etching,

Wafer no.	Etching Time (in seconds)
Bond 1	It was not recorded.
Bond 2	35
Bond 3	Not done because the wafer was broken.
Bond 4	40
Bond 5	30
Bond 6	30
Bond 7	35
Bond 8	40

Table 2.7: Wet-Etching time for gold layer of the Pyrex-SOI wafer pairs.

the wafer was washed with fresh deionized water to remove the aqua regia solution. The wafer was placed in a vacuum desiccator for about 10 minutes in order to eliminate moisture from the interface.

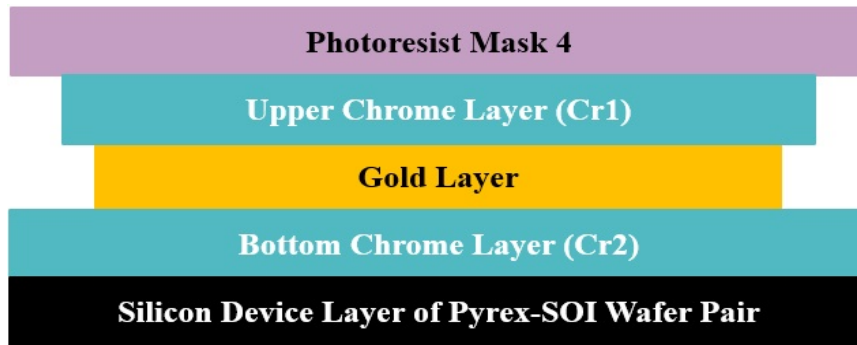


Figure 2.32: Schematic of the Cr-Au-Cr stack after etching the gold layer of the Pyrex-SOI wafer pair.

2.5.5.4 Etching of Bottom Chrome Layer

The last layer of the Cr-Au-Cr stack was removed using a chemistry of diluted chrome etchant prepared by adding 6 units of water to 1 unit of pure chrome etchant. The wafer was immersed in the etching solution until the chrome layer was completely dissolved, revealing the underlying silicon device layer. Due to the similarity in appearance between the gray colored silicon and gray colored chrome layers, the color changes were not obvious during this etching process. Therefore, the wafer was examined under the optical microscope to conclude whether or not the chrome layer was etched entirely. The wafer, after etching the bottom chrome layer, is shown in Figure 2.33. The etching of the bottom chrome layer took about 3 to 5 minutes, including 10 to 20 seconds of over-etching. Table 2.8 displays the bottom chrome layer etching time for all wafers.

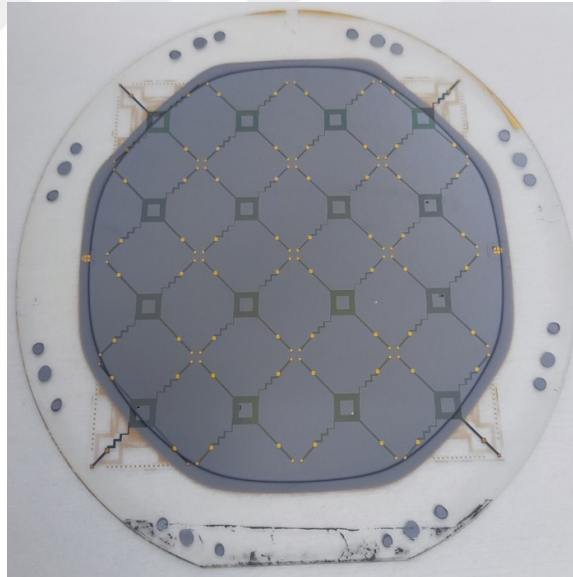


Figure 2.33: Pyrex-SOI wafer pair after etching of the blanket-coated bottom chrome layer.

The bottom chrome layer was etched using the gold layer as a mask due to the formation of the undercuts underneath the photoresist mask. The undercut of the top chrome layer increased because it was etched a second time while etching the bottom chrome layer. An optical microscope image and a schematic of the undercut in the top and bottom chrome layers are shown in Figure 2.34. The

Wafer no.	Etching Time (in minutes)
Bond 1	It was not recorded.
Bond 2	2.5
Bond 3	Not done because the wafer was broken.
Bond 4	3
Bond 5	5.7
Bond 6	3
Bond 7	3
Bond 8	2.5

Table 2.8: Wet-Etching time for the bottom chrome layer of Pyrex-SOI wafer pairs.

bottom chrome layer in Figure 2.34 is not visible because it is lying under the gold layer. Following the wet etching process, the wafer pair was dipped in fresh deionized water to remove residues of the chrome etchant. The vacuum desiccator was used to remove the moisture from the wafer's interface.

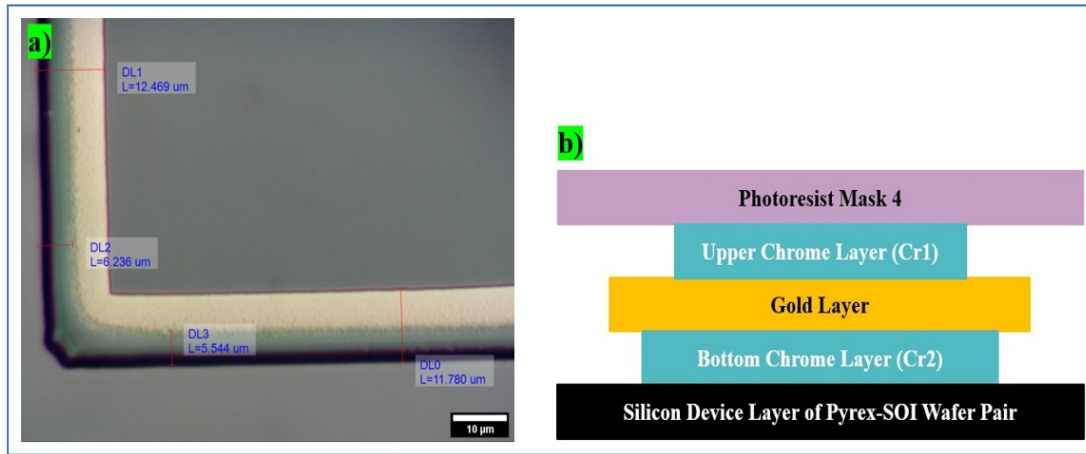


Figure 2.34: Undercuts formed in the Cr-Au-Cr layers of the Pyrex-SOI wafer pair after etching the bottom chrome layer: (a) Optical microscope image, (b) Schematic of Cr-Au-Cr stack.

2.5.5.5 Deep Reactive Ion Etching of the Silicon Device Layer

The silicon device layer of the wafer was patterned with a reactive ion etching plasma in an inductively coupled plasma (ICP) tool. The anisotropic deep reactive ion etching (DRIE) of the silicon device layer was done using a recipe of the Bosch Process having C_4F_8 and SF_6 gases for plasma processing. During the deposition stage of the Bosch process, C_4F_8 gas is deposited under specific plasma conditions to protect the vertical surfaces of the structure from the effects of mild ion bombardment. Conversely, during the etching process, the silicon is vertically etched by SF_6 plasma due to the passivation of the trench side walls by the C_4F_8 Teflon-like polymer layer [46]. Figure 2.35 displays a schematic representation of the Bosch Process [46]. The silicon undergoes etching by reacting with fluorine radicals generated by SF_6 plasma gas, as shown in Equations 2.2 and 2.3 [46].

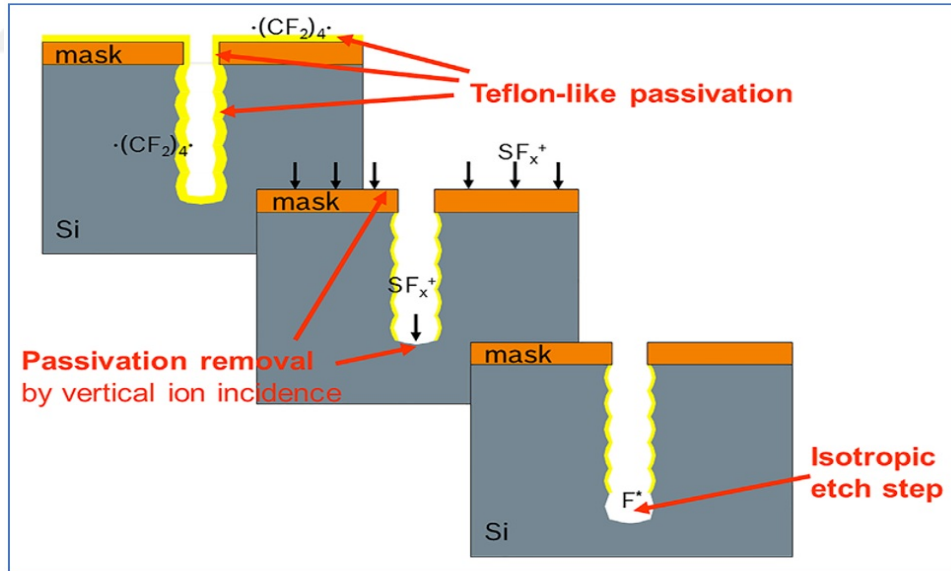
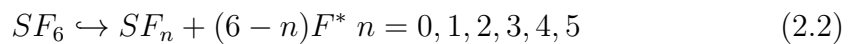


Figure 2.35: Schematic of the Bosch Process.



To prevent the wafer from being broken by mechanical clamping fingers inside the ICP chamber, it was connected to a 1 mm thick Pyrex support wafer using tiny pieces of Kapton tape. Prior to the actual etching procedure, the chamber of the ICP tool was prepared by conditioning it with the Bosch Process using a test wafer. The 12.5 microns thick silicon device of the wafer was etched with the photoresist mask on top. The etching process for the silicon device layer lasted around 30 to 60 minutes, and the duration was potentially influenced by variations in the thickness of the device layers on the SOI wafers and instabilities in the plasma etching process due to the old age of the process equipment. An over-etching was carried out to guarantee the thorough etching of the silicon device layer. Backside helium cooling is performed because silicon etching with Bosch Process is a highly exothermic reaction [46]. The duration required for the etching process of the device layer for all the wafers is shown in Table 2.9.

Wafer no.	Etching Time (in minutes)
Bond 1	30
Bond 2	40
Bond 3	Not done because the wafer was broken.
Bond 4	27
Bond 5	36
Bond 6	40
Bond 7	45
Bond 8	60

Table 2.9: DRIE etching time of Silicon device layer of Pyrex-SOI wafer pairs.

The process was stopped at the end of the etching cycle instead of the deposition cycle to prevent the formation of a C_4F_8 polymer layer on the surface of the wafer. Figure 2.36 depicts the wafer after the patterning of the device layer, revealing the insulation layer.

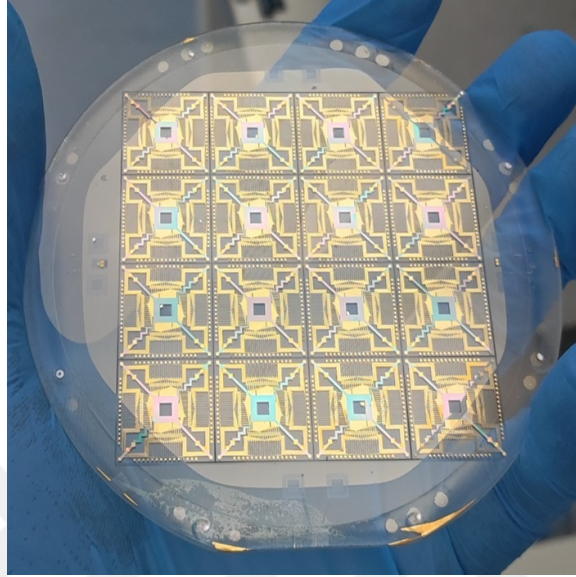


Figure 2.36: Pyrex-SOI wafer pair after patterning the Silicon device layer using DRIE process.

2.6 Singulation of Chips

The closest features (PCB Pads) between two neighboring chips are separated by a distance of 300 microns (i.e. the dicing streets). Therefore, it is crucial to dice the chips with minimum chipping around their edges in order to avoid damaging the features located along the edges of the chip. The damaged features around the chip edge not only affect the chip's functionality but may also cause problems during device integration processes. The cutting quality of the diced chips depends upon multiple parameters such as dicing blade type, proper blade dressing, dicing tape, the revolutions per minute (RPM) of the blade, and the feed rate of the dicing saw machine [47]. Prior to dicing the real wafer, the dicing saw processing was optimized to get the minimum possible front and back side chipping for the CMUT chips.

Dicing blade type and width are selected based on the mechanical properties of the substrate material to be diced. Dicing blades use diamond particles or other abrasive particles as cutting edges, which are embedded in a bond matrix on the dicing blade; for hard and brittle materials, dicing blades with the softer bond

material are used, while hard bond matrix blades are used to cut soft materials. The borosilicate glass wafer (Pyrex-7740) is brittle; therefore, the dicing process required a blade with a softer bond, the DISCO-R07. Dicing blades with a thickness of 150 microns were selected to keep chipping restricted to the 250-micron wide dicing street zone.

The dressing of the dicing blade was done by cutting the dressing boards to expose, sharpen, and bring the diamond particles in a self-sharpening regime. Dressing the dicing blade also helps to reduce its eccentricity to 10 microns or less. Stable spindle currents in the dicing machine were observed when the blade had less eccentricity and was in a self-sharpening regime. Stable spindle currents are crucial for achieving high-quality cutting since they indicate that the blade is operating in a self-sharpening state. An image of the dressing board is shown in Figure 2.37.

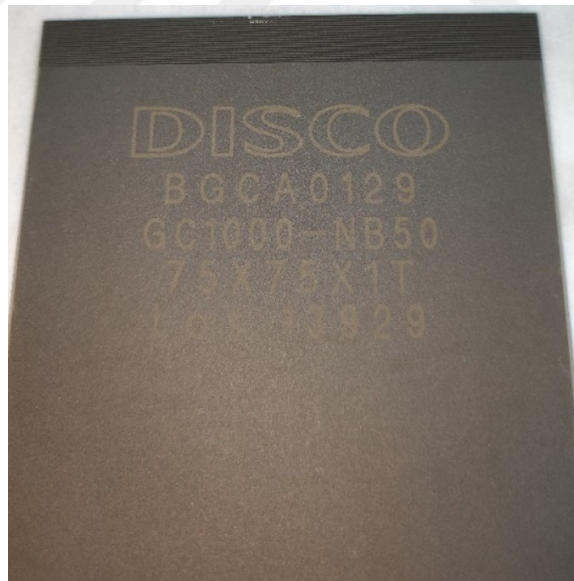


Figure 2.37: Image of a dressing board specified for DISCO-R07 dicing blades.

A dicing tape with a thickness of 150 microns (D-841, LINTEC Corporation) was used for dicing operations due to its strong adhesion capability, which effectively hold the wafer on the chuck table of a dicing saw. When used appropriately, this tape also prevents water penetration from the CMUT channels into the CMUT cavities in the sensor chips during dicing saw processing. Dicing tape

made of hard base film (polyolefins) was used because tapes with soft bases tend to produce more chipping [47].

The through-cut cutting approach was considered in which the dicing blade also penetrates approximately half of the thickness of the dicing tape, resulting in 90-degree vertical walls of the diced chips. The chips were diced utilizing a two-step cutting technique, in which about 450 microns of the 500-micron thick wafer were sliced during the first phase, while the remaining 50 microns thickness was cut during the second step to isolate the chips. The two-step dicing process assists in minimizing chipping and prevents chips from possible fractures. Moreover, the dicing of square chips using the four-channel cutting method enhances the flatness of their vertical walls and removes any excess burr or debris produced by the dicing blade and the substrate material.

The dicing blade's revolutions per minute (RPM) and the feed rate of the substrate material were optimized to improve the cutting process by reducing chipping on both the front and back sides of the diced chips. The diamond particles attached to the dicing blade may break at high spindle speeds or pull out at very low spindle speeds, which affects the quality as the feed rate does. Because of the brittle nature of the Pyrex wafer, low spindle RPM values of 15K and 20K were used. During the first set of trials, the feed rate of the wafer ranged from 1 to 10 mm.s⁻¹ while maintaining a constant RPM of 15K. In the second series of trials, the feed rate of the wafer was altered from 1 to 10 mm.s⁻¹ by keeping the RPM at 20K. Images around the front and back sides edges of the diced chips were captured by the optical microscope, shown in Figure 2.38. Using Image-J software, we measured the range of chipping length from the captured pictures.

Figure 2.39 shows that at constant spindle RPM, increasing feed speed reduced front-side chipping length while increasing feed speed increased back-side chipping size. So, it is a trade-off between the front and back side chipping length of the chips for the required cutting quality. The cutting quality on both the front and back sides of the chip was improved significantly using a feed rate of 5 mm.s⁻¹ and an RPM of 20K, yielding 52 and 55 microns, respectively. The overall increasing

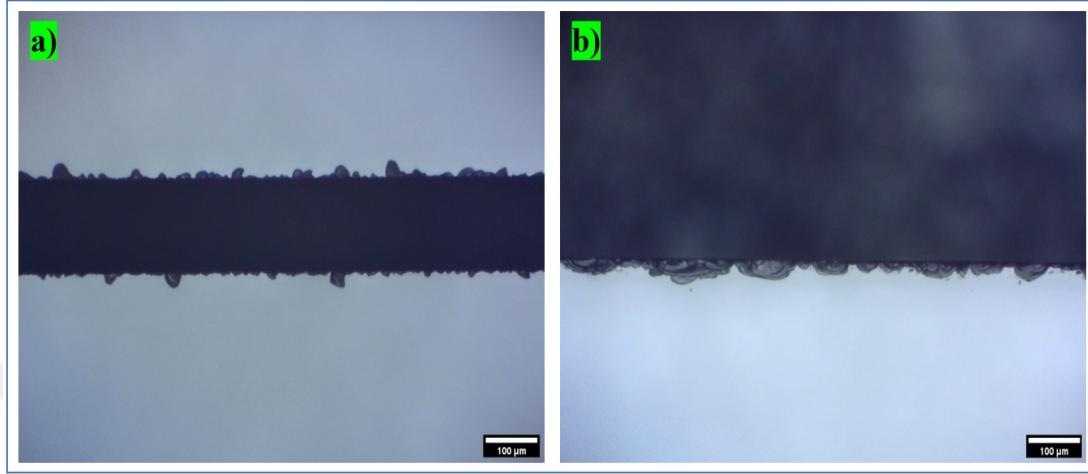


Figure 2.38: Optical microscope images of the test Pyrex wafer displaying Chipping around edges of the dicing streets after cutting: (a) Front-Side, (b) Back-Side.

or decreasing trend in Figure 2.39 had a few abnormalities. Possible causes of these irregularities include the diamond-cutting particles being pulled or broken out of the blade matrix and the high friction between the blade and substrate, which results in abrupt chipping loss around the edges of the chip.

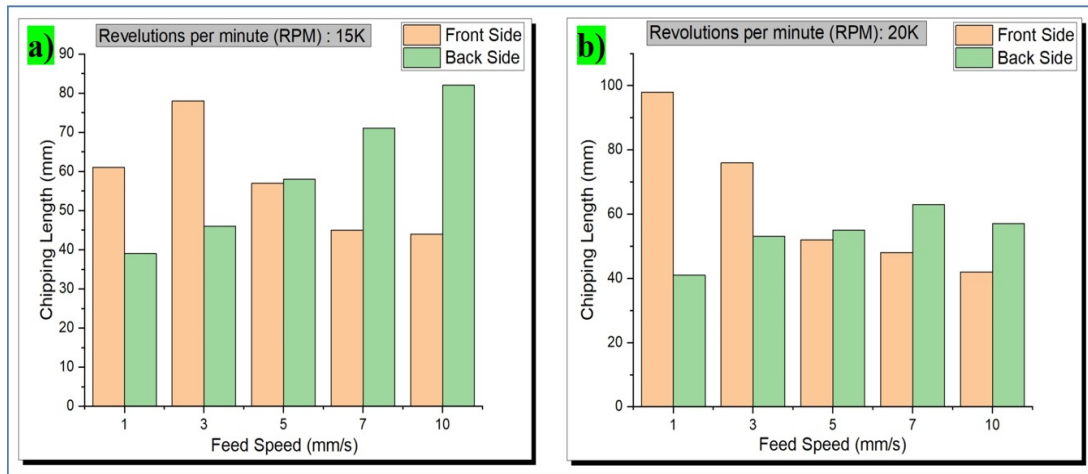


Figure 2.39: Chipping lengths on the Front and Back sides of test Pyrex wafer measured by Image-J software: (a) 15K RPM, (b) 20K RPM.

The wafer was fixed in the dicing frame with the help of the D-841 dicing tape to prepare the wafer for the cutting process. The dicing saw uses a constant water supply to cool the dicing blade and the substrate during the process. The wafer

was sensitive to wet processing after CMUT wiring channels going to the CMUT gaps were opened during the deep reactive ion etching (DRIE) of the device layer. The dicing sample was prepared by attaching the device side of the wafer to the sticky side of the tape to prevent the possibility of damage on the CMUT plates, and to prevent the water penetration into the CMUT gaps. The dicing frame was positioned on the chuck table of the dicing machine for about 15 to 20 minutes in order to eliminate the air that was trapped between the dicing tape and the wafer by applying vacuum from the chuck table to the dicing tape. Removing the trapped air is possible, because the dicing tape is porous, allowing trapped air to be sucked by the vacuum from the chuck table. Figure 2.40 shows the wafer mounted on a dicing frame.

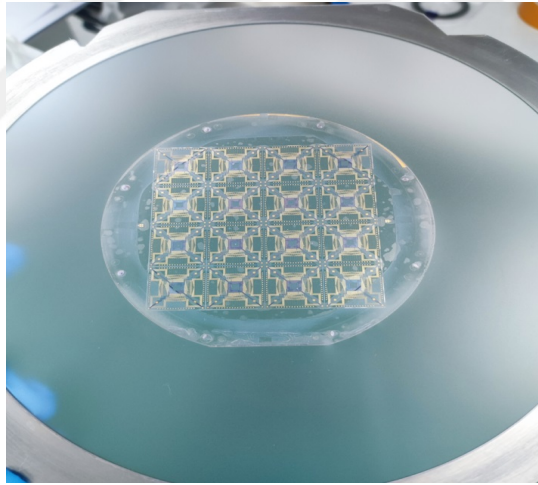


Figure 2.40: Image of a real wafer mounted on the dicing frame.

To prevent the undesired penetration of water (due to the water jet) between the wafer and the dicing tape interface (and into the CMUT gaps through the wiring channels), the manual stiction process was performed using a tweezer tip in the regions of the dicing streets due to a gap between the dicing tape and the trenches of the dicing streets on the wafer. The pictures of the dicing streets before and after the manual stiction are shown in Figure 2.41.

The device data recipe was prepared after placing the prepared wafer sample on the chuck table of the dicing machine, including the wafer's diameter and thickness, the dicing tape thickness, the channel angle, the blade height, spindle

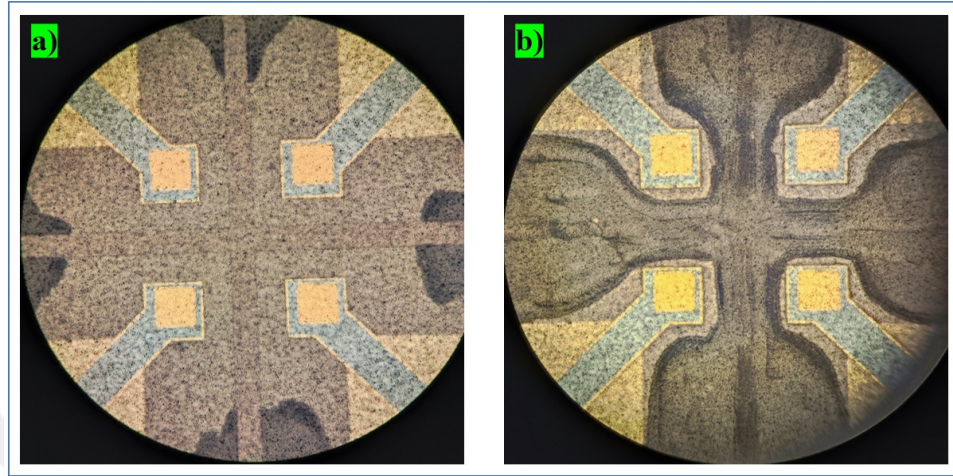


Figure 2.41: Junction of two dicing streets on the Pyrex wafer: (a) Before manual stiction of the dicing tape, (b) After manual stiction of the dicing tape.

RPM, and the feed rate of the chuck table. Figure 2.42 shows the optimized recipe parameters for the dicing process. The wafer was diced in two cutting channels to singulate the square shaped CMUT sensor chips. The chips were then isolated using a portable sharp cutting blade. The chips obtained after dicing the wafer are shown in Figure 2.43.

Work shape and size ☒ Round 101.600 mm ☐ Square Ch1 0.000 mm Ch2 0.000 mm				Spindle rev. 20000 /min Precut process No. 0 Cutting ch seq. 12																																					
Work Thickness 0.500 mm Tape Thickness 0.150 mm																																									
	Ch 1	Ch 2																																							
θ Deg.	0.000°	90.000°	Blade height	0.075	0.000	0.000																																			
Cut mode	A	A	Feed speed	5.000	0.000	0.000																																			
Cut dir.	FRONT	REAR	Y-index	17.0000	0.0000	0.0000																																			
Cut	0 lines	0 lines	Repeat times	0	0	0																																			
Offset Y	0.0000	0.0000																																							
Noncut F	0.000	0.000																																							
Noncut R	0.000	0.000																																							
			<table border="1"> <thead> <tr> <th colspan="3">Ch 1</th> <th colspan="3">Ch 2</th> </tr> <tr> <th>SEQ1</th> <th>SEQ2</th> <th>SEQ3</th> <th>SEQ1</th> <th>SEQ2</th> <th>SEQ3</th> </tr> </thead> <tbody> <tr> <td>0.075</td> <td>0.000</td> <td>0.000</td> <td>0.075</td> <td>0.000</td> <td>0.000</td> </tr> <tr> <td>5.000</td> <td>0.000</td> <td>0.000</td> <td>5.000</td> <td>0.000</td> <td>0.000</td> </tr> <tr> <td>17.0000</td> <td>0.0000</td> <td>0.0000</td> <td>17.0000</td> <td>0.0000</td> <td>0.0000</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table>			Ch 1			Ch 2			SEQ1	SEQ2	SEQ3	SEQ1	SEQ2	SEQ3	0.075	0.000	0.000	0.075	0.000	0.000	5.000	0.000	0.000	5.000	0.000	0.000	17.0000	0.0000	0.0000	17.0000	0.0000	0.0000	0	0	0	0	0	0
Ch 1			Ch 2																																						
SEQ1	SEQ2	SEQ3	SEQ1	SEQ2	SEQ3																																				
0.075	0.000	0.000	0.075	0.000	0.000																																				
5.000	0.000	0.000	5.000	0.000	0.000																																				
17.0000	0.0000	0.0000	17.0000	0.0000	0.0000																																				
0	0	0	0	0	0																																				

Figure 2.42: Print-screen of Device Data of Dicing Saw (DISCO DAD-3220).

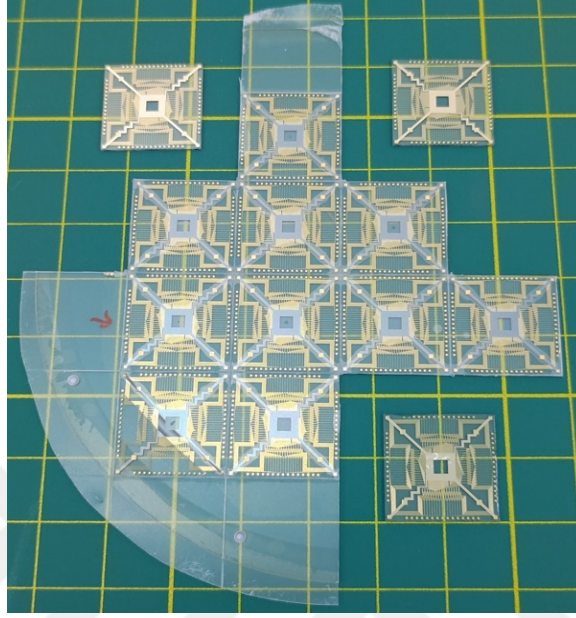


Figure 2.43: CMUT chips singulated from the real wafer using manual mechanical dicing process.

2.6.1 Removal of Dicing Tape

The D-841 dicing tape used to singulate chips from the wafer using the dicing saw processing is sensitive to ultraviolet (UV) light. The optimal UV dosage was discovered via experiments in which test Pyrex chips, covered with dicing tape, were exposed to UV light using the mask aligner. The test chips underwent exposure to various UV dosages, ranging from 300 to 2000 mJ.cm^{-2} , with an increment of 100 mJ.cm^{-2} . It was concluded that exposing the test chips to UV radiation between 900 to 1200 mJ.cm^{-2} made it much easier to remove the dicing tape, with fewer residues left behind. There was no significant shift in the adhesion when exposing the dicing tape to higher doses of UV radiation ranging from 1200 to 2000 mJ.cm^{-2} .

The motivation for optimizing the UV dosage was to reduce the risk of peeling off structures from the CMUT chips. The CMUT chips underwent UV exposure within the process window of 900 to 1200 mJ.cm^{-2} using the mask aligner. The dicing tape was peeled off from the chip using a tweezer, ensuring a 180-degree angle with the chip's surface to minimize residues from the tape. Since it was

noticed that the dicing tape left more residue in the areas where it was removed initially, we intentionally started removing regions not critical for flip-chip bonding. Figure 2.44 displays the chips obtained subsequent to the removal of the dicing tape.

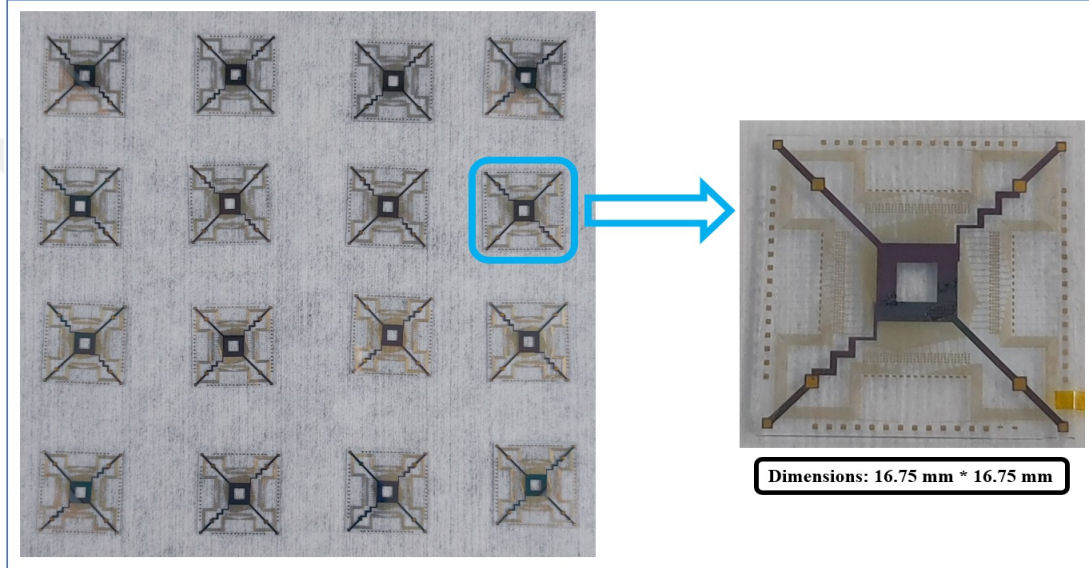


Figure 2.44: CMUT Sensor chips obtained after peeling off the dicing tape following the UV exposure.

2.6.2 Removal of Dicing Tape using Oxygen Plasma Processing

The stiction behavior of the dicing tape to the surface of the substrate varies depending on the surface quality (i.e., roughness) and material of the substrate. Experimental trials were conducted on a limited number of test chips made of Pyrex and Silicon before working with real CMUT chips. The test chips accurately represented the real CMUT chips since they had gold, alumina, and photoresist features on their surface. The results from the experiments confirmed that the D-841 dicing tape exhibits exceptional stiction with the test chips before UV exposure, and the tape shows a notable reduction in adhesion, resulting in easy removal from the chips after UV exposure.

However, we were not able to remove the dicing tape (D-841) from the real CMUT chips around the wafer's edge because the stiction of the dicing tape adhesives remained unchanged even after UV exposure. Capacitive MEMS devices might face damage to the structures on their surface if the dicing tape is peeled off with excessive force. The absence of the alumina layer and high surface roughness around the edges of the Pyrex wafer are the possible causes for the high stiction of the dicing tape. The damage to the alumina layer and Pyrex wafer happened during the microfabrication process steps, especially during the long silicon handle layer removal process step. Figure 2.45 displays the CMUT chip and its schematic prior to the oxygen plasma removal of the dicing tape.

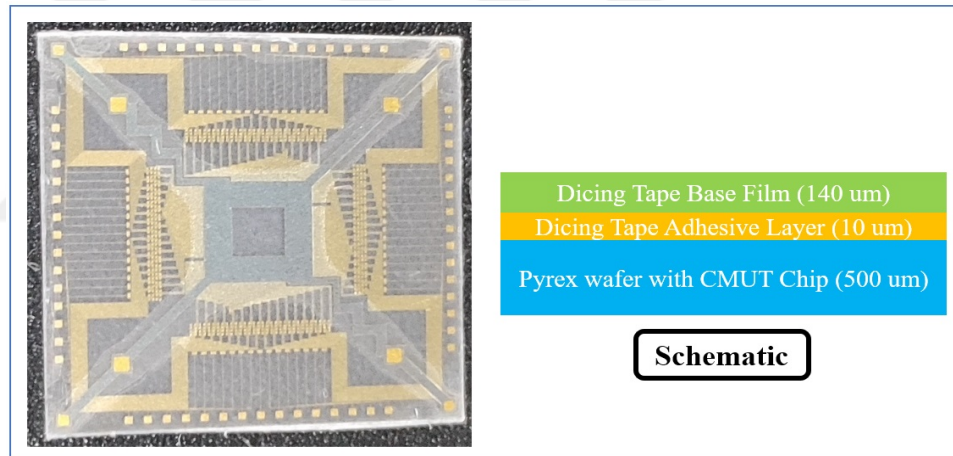


Figure 2.45: CMUT chip (along with its schematic) covered with the D-841 dicing tape.

A dry technique was used to remove a 150-micron-thick dicing tape composed of polyolefins (base film) and UV-curable acrylic (adhesive layer). The reason behind using the dry technique is that our CMUT chips were susceptible to damage from wet processing when the channels (reaching to the CMUT cavities) were opened during the patterning of the silicon device layer. The 150-micron-thick dicing tape was successfully removed with oxygen plasma using inductively coupled plasma (ICP) equipment. This method has been used for years to remove organic residues in the micro and nanofabrication industry. However, to the best of our knowledge, this removal technique was not used for complete removal of dicing tapes. It took around 3 hours to etch the full thickness of the dicing tape completely. The oxygen plasma processing of the dicing tape left some residues

on the surface of the CMUT chips, as shown in Figure 2.46.

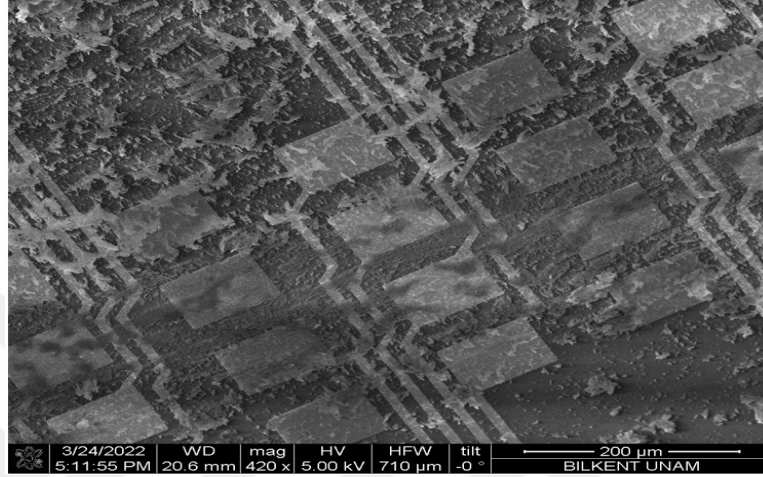


Figure 2.46: SEM image showing residues of the dicing tape on ASIC pads region of the CMUT chip.

The burned residues were peeled off with the help of a less sticky (compared to D-841) pressure-sensitive dicing tape (T-80HW-23A). Finally, a small amount of residues on the surface of the CMUT chip from pressure-sensitive dicing tape (T-80HW-23A) were removed by doing another oxygen plasma processing for a relatively shorter time (about 3 to 5 minutes). Figure 2.47 displays ASIC pads region of the CMUT chip after the complete removal of the dicing tape and its residues.

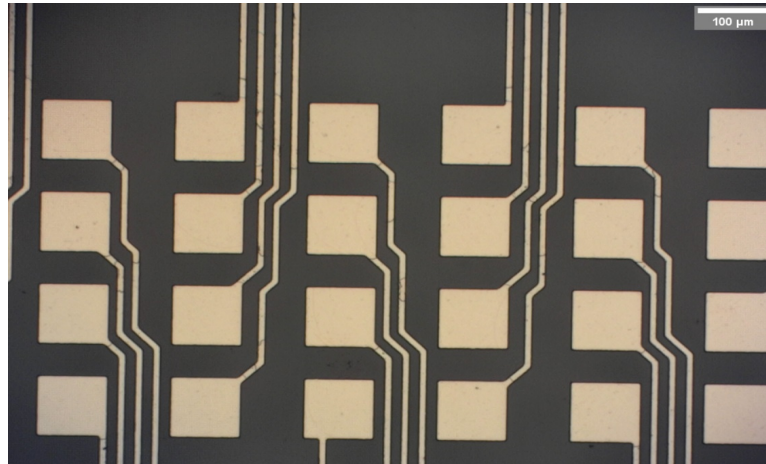


Figure 2.47: Optical microscope image displaying the ASIC pads region of the CMUT chip after removing the dicing tape using oxygen plasma processing.

2.7 Oxygen Plasma Cleaning

The photoresist Mask 4 and dicing tape residues were removed by subjecting the chip to an oxygen plasma process in an inductively coupled plasma (ICP) instrument. The descum process recipe was used for the purpose of conducting dry cleaning. Initially, the ICP chamber underwent oxygen plasma conditioning using a clean Pyrex wafer.

The photoresist, which had a thickness of approximately 1.98 microns, was fully removed in 2 to 3 minutes by etching during the descum process. The duration of the cleaning procedure may be extended by an additional 5 to 10 minutes, depending upon the quantity of dicing tape residues present on the surface of the chip. Removing the residues of dicing tape, especially from bonding pads, is critical since they might affect the flip-chip bonding process between a CMUT chip and ASIC chip. Furthermore, the oxygen plasma also etched the chrome layer beneath the photoresist mask. The etching of the chrome layer revealed the underlying gold layer, indicating that the photoresist mask had been removed. Figure 2.48 depicts the CMUT chip after its cleaning by the descum process.

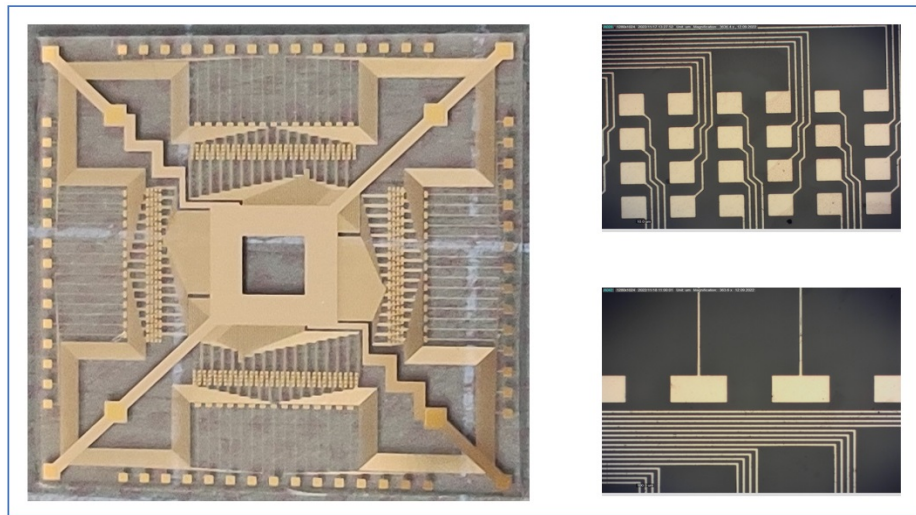


Figure 2.48: CMUT chip and optical microscope images of its ASIC pads after it was cleaned with oxygen plasma processing (Descum Process).

2.8 Manual Masking and Parylene-C Coating

The dicing tape with high adhesive stiction (D-841) was manually applied as a mask on the ASIC and PCB pad regions on the CMUT chip to protect from coating since these pads would be utilized in the forthcoming flip-chip and wire bonding procedures. In order to vacuum and seal the CMUT cavities, approximately 2-micron thick Parylene-C layer was deposited on the chips [48]. The Parylene-C coating was done at the METU-MEMS research facilities in Ankara. Figure 2.49 displays a picture of the chip subsequent to the application of Parylene-C coating.

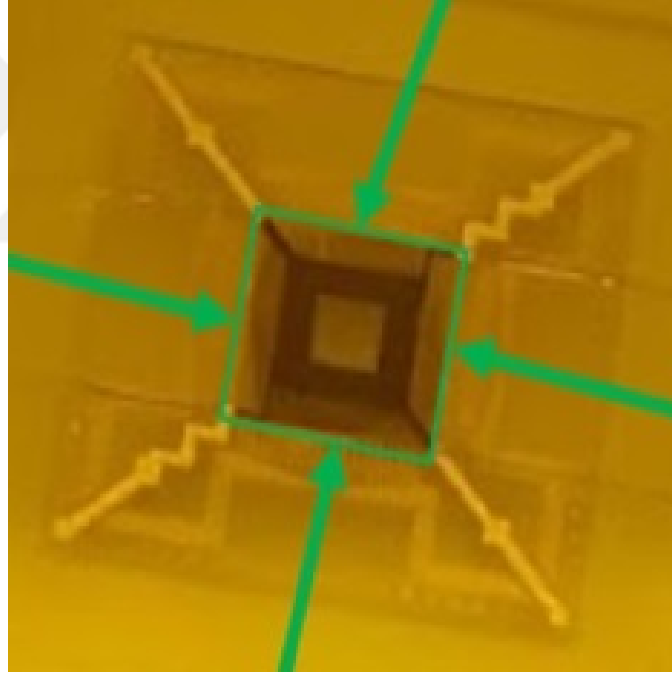


Figure 2.49: CMUT chip covered with a layer of Parylene-C. The region that is inside the green colored square is the region that is coated with permanent layer of Parylene C, while the outer sides of the green square are protected with dicing tape (D-841) before Parylene C deposition. Hence, the Parylene C at the outer sides of the green colored square is removed while peeling the dicing tape to reveal the electrical pads.

2.9 Microfabrication Process Flow for the CMUT Devices (2D View)

STEP 1: See Figure 2.50 for reference.

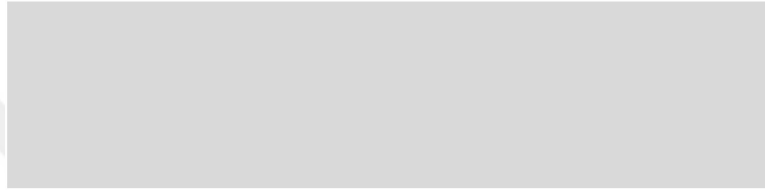


Figure 2.50: Blank Pyrex-7740 wafer.

STEP 2: See Figure 2.51 for reference.



Figure 2.51: Chrome deposition as hard mask on Pyrex wafer.

Step 3: See Figure 2.52 for reference.



Figure 2.52: Photolithography with Mask 1 for cavity formation on Pyrex wafer.

STEP 4: See Figure 2.53 for reference.



Figure 2.53: Argon Reactive Ion Etching (RIE) for etching chrome hard mask.

STEP 5: See Figure 2.54 for reference.



Figure 2.54: SF_6 Reactive Ion Etching (RIE) for etching Pyrex wafer.

STEP 6: See Figure 2.55 for reference.



Figure 2.55: Buffered Oxide Etch (BOE) wet-etching process for Pyrex. Note that the undercut below the photoresis is increased, and depth of the gap is also increased.

STEP 7: See Figure 2.56 for reference.



Figure 2.56: Metallization (Ti-Pt-Au) as the bottom electrode.

STEP 8: See Figure 2.57 for reference.



Figure 2.57: Photoresist Lift-off with Prinha solution.

STEP 9: See Figure 2.58 for reference.



Figure 2.58: Chrome wet-etching using chrome etchant.

STEP 10: See Figure 2.59 for reference.

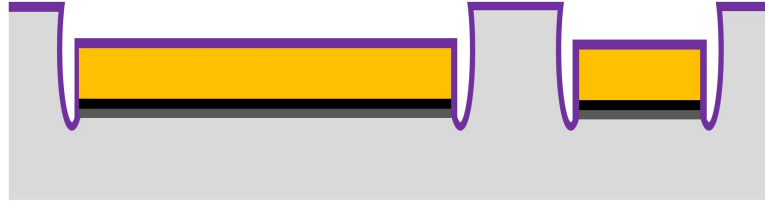


Figure 2.59: Alumina deposition using Atomic Layer Deposition (ALD).

STEP 11: See Figure 2.60 for reference.

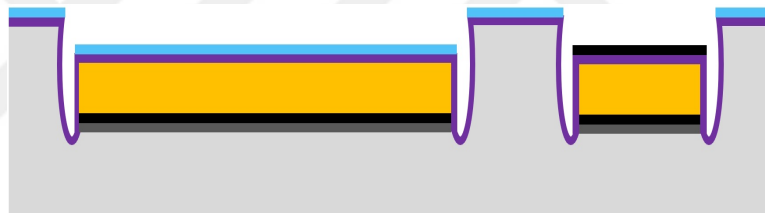


Figure 2.60: Chrome hard mask deposition on the insulation layer.

STEP 12: See Figure 2.61 for reference.

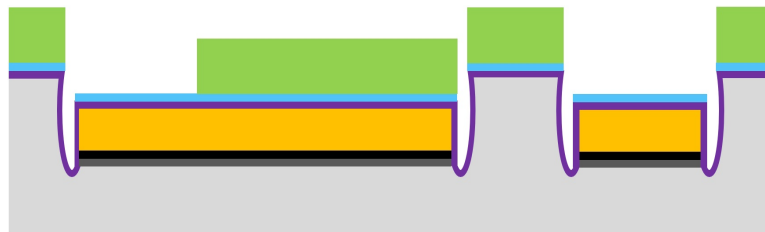


Figure 2.61: Photolithography with Mask 2 for etching alumina layer from electrical pad regions.

STEP 13: See Figure 2.62 for reference.

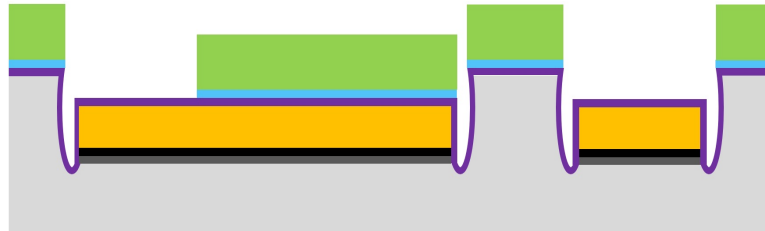


Figure 2.62: Chrome wet-etching from electrical pad regions.

STEP 14: See Figure 2.63 for reference.

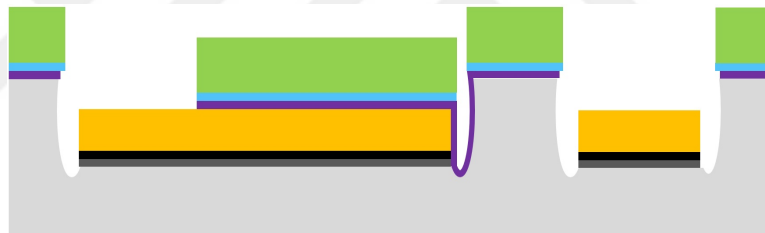


Figure 2.63: Alumina layer etching from electrical pad regions using diluted AZ 400K Developer.

STEP 15: See Figure 2.64 for reference.

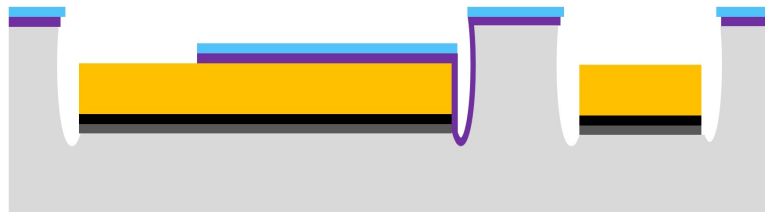


Figure 2.64: Photoresist removal using acetone and Prinha.

STEP 16: See Figure 2.65 for reference.

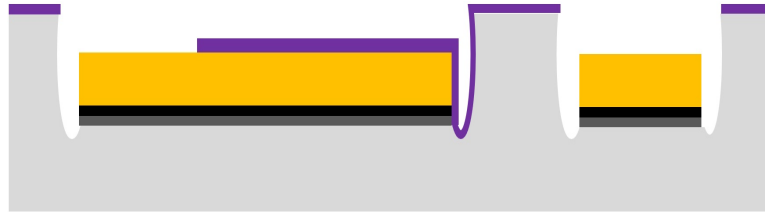


Figure 2.65: Chrome hard mask removal using chrome etch.

STEP 17: See Figure 2.66 for reference.



Figure 2.66: Anodic Wafer Bonding of Pyrex and Silicon-on-Insulator (SOI) wafers.

STEP 18: See Figure 2.67 for reference.

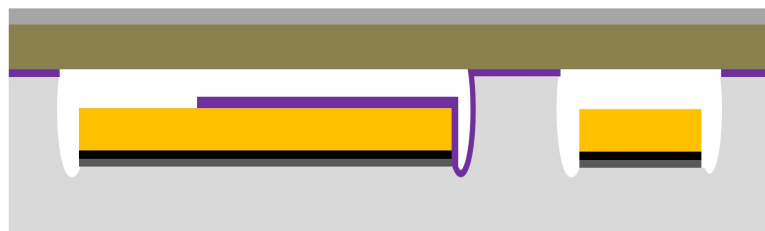


Figure 2.67: SF_6 Reactive Ion Etching for handle layer removal of the SOI wafer.

STEP 19: See Figure 2.68 for reference.

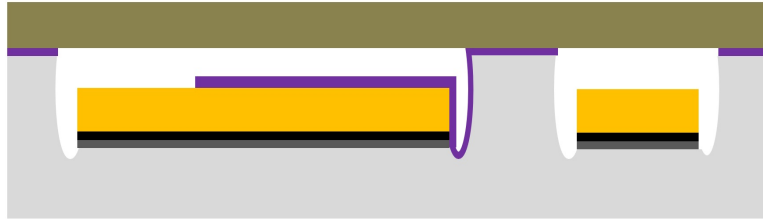


Figure 2.68: BOE wet-etching for removing buried silicon oxide layer of the SOI wafer.

STEP 20: See Figure 2.69 for reference.

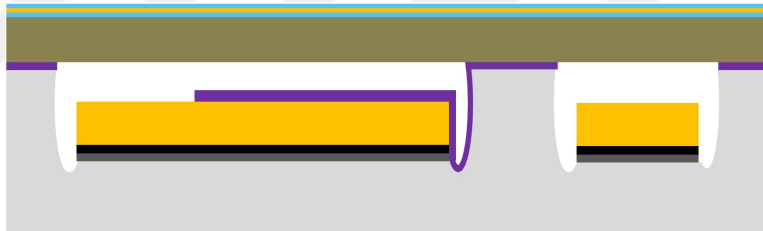


Figure 2.69: Blanket layer deposition (Cr-Au-Cr) on Si-device layer of the SOI wafer.

STEP 21: See Figure 2.70 for reference.

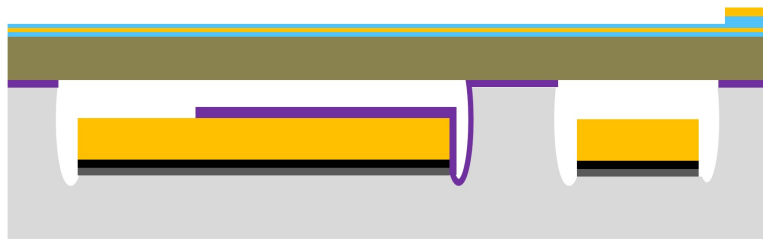


Figure 2.70: Deposition of wire-bonding pads for top electrode using Stencil Shadow Mask 3.

STEP 22: See Figure 2.71 for reference.

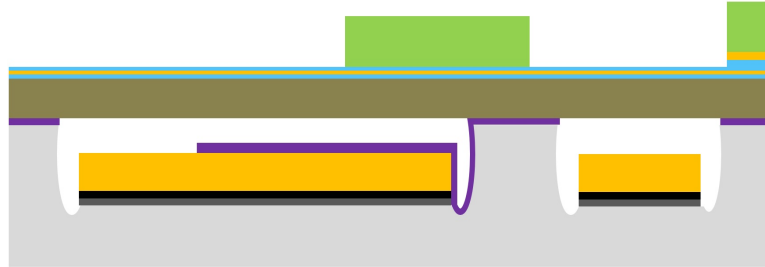


Figure 2.71: Photolithography with Mask 4 to pattern the Si-device layer.

STEP 23: See Figure 2.72 for reference.

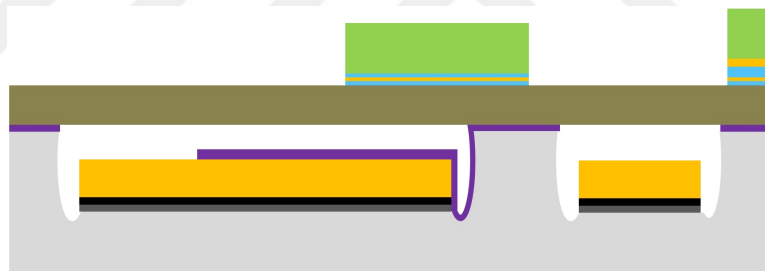


Figure 2.72: Wet-etching of blanket coated Cr-Au-Cr metal stack.

STEP 24: See Figure 2.73 for reference.

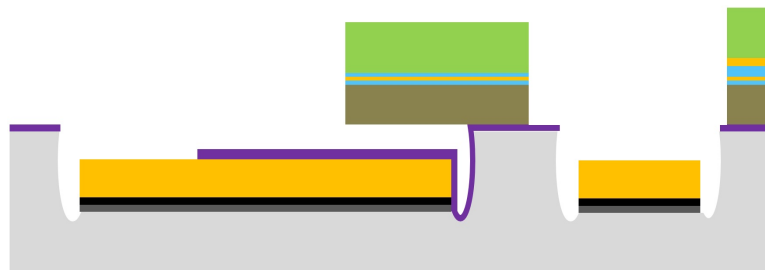


Figure 2.73: Deep Reactive Ion Etching (DRIE) of Si-device layer using Bosch Process.

STEP 25: See Figure 2.74 for reference.

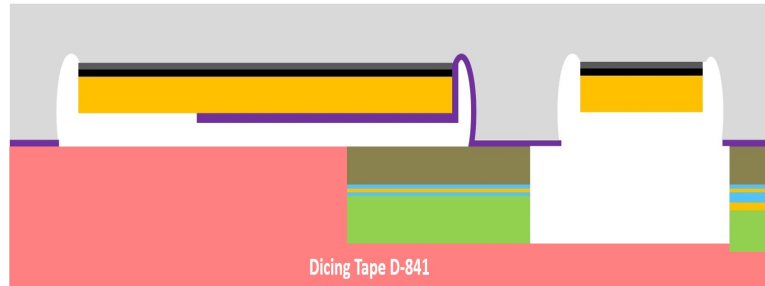


Figure 2.74: Dicing saw processing for the chip singulation.

STEP 26: See Figure 2.75 for reference.

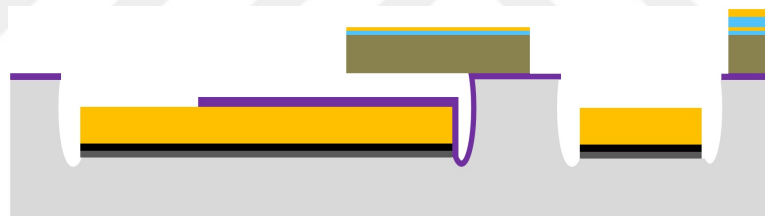


Figure 2.75: Photoresist removal using Descum Process (O_2 will also remove top chrome layer).

STEP 27: See Figure 2.76 for reference.

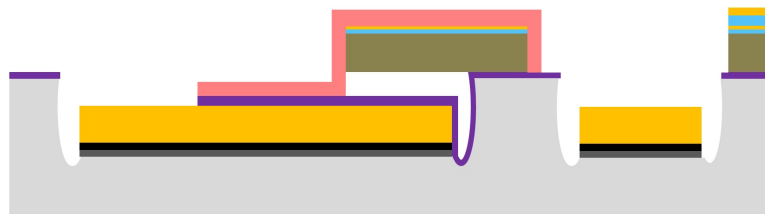


Figure 2.76: Parylene-C coating to seal the CMUT cavities.

STEP 28: See Figure 2.77 for reference.

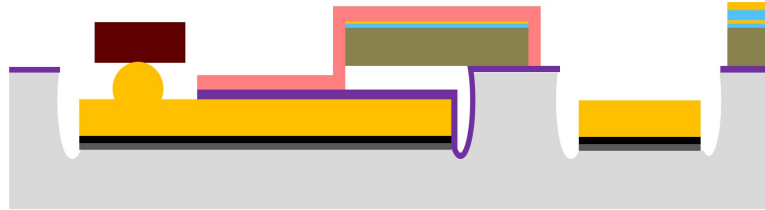


Figure 2.77: ASIC to CMUT integration using flip-chip bonding process.

STEP 29: See Figure 2.78 for reference.

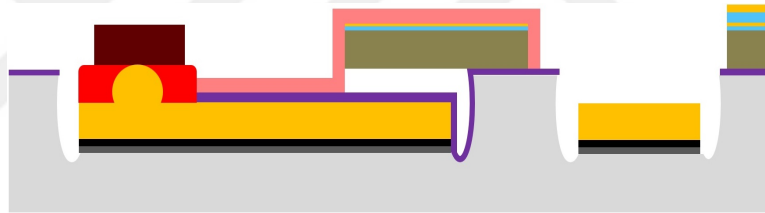


Figure 2.78: Underfilling with non-conductive epoxy after ASIC to CMUT integration to enhance the integrity of the structure.

STEP 30: See Figure 2.79 for reference.

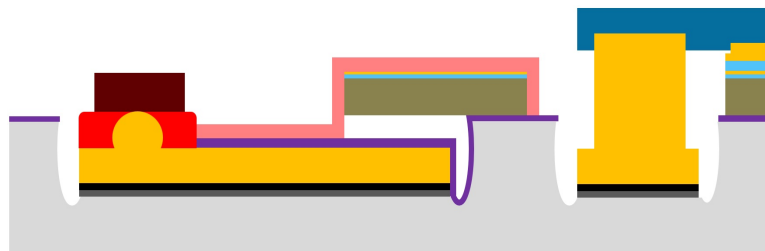


Figure 2.79: CMUT to PCB integration using flip-chip bonding.

STEP 31: See Figure 2.80 for reference.

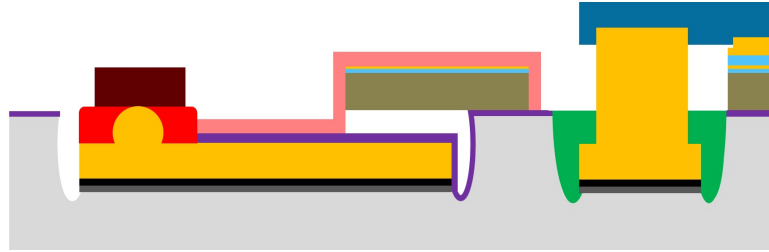


Figure 2.80: Underfilling with non-conductive epoxy after CMUT to PCB integration to enhance the integrity of the structure.

Chapter 3

Characterization

3.1 Inspection of Cavities of the CMUT Devices

In order to function as a variable capacitor, a capacitive micromachined ultrasonic transducer (CMUT) device must maintain a variable gap between its electrodes. CMUT devices operate based on the concept of capacitance variation, which occurs as a result of changes in the height of the CMUT cavity (gap). Therefore, the CMUT devices underwent destructive testing to examine their cavities.

The silicon membrane from the CMUT cells was peeled off using Kapton tape, or high-stiction dicing tape (D-841), or carbon tape. Here, it is important to emphasize that, the peeling force was hardly sufficient to separate the Si membranes from above the CMUT gaps, and we had to try the destructive peeling process for multiple times before the membranes were separable from the Pyrex substrate. The Si membrane was removed to visually observe and investigate the CMUT cavities located underneath the Si membrane. The CMUT cavities can be seen clearly in the optical microscope image shown in Figure 3.1 after successfully removing the Si membranes.

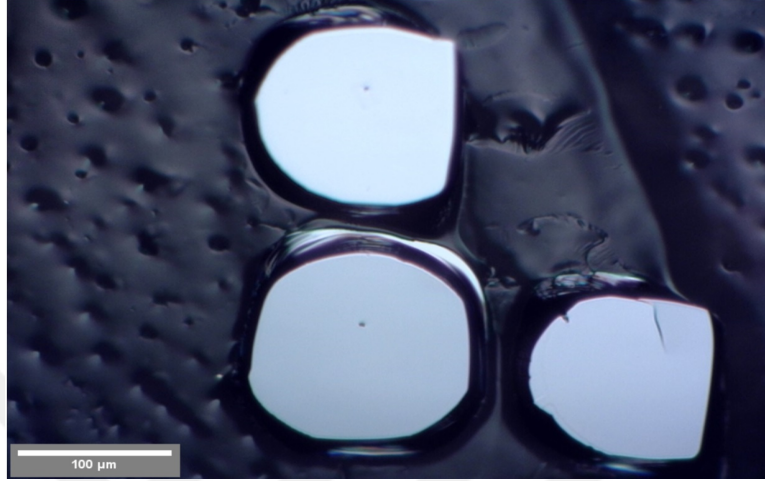


Figure 3.1: Optical microscope image displaying 3 CMUT membranes after removing these silicon membranes from the Pyrex substrate.

The CMUT cavities patterned into the Pyrex wafers were also examined using SEM after the Si membrane was removed. The SEM images in Figure 3.2 shows a well-defined gap between the membrane and the lower electrode of the CMUT device.

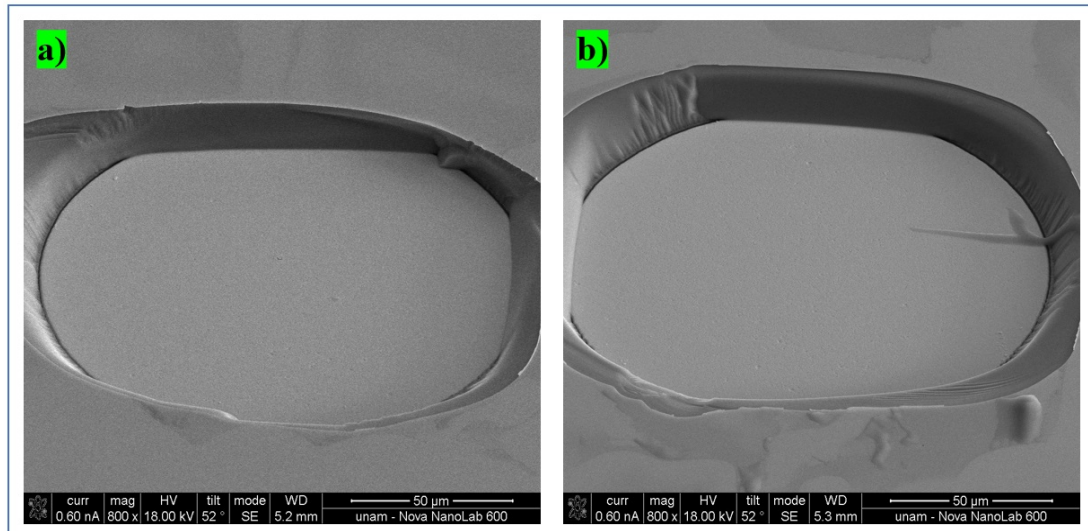


Figure 3.2: SEM images displaying cavities and bottom electrodes of 2 CMUT devices.

A CMUT cell was cut cross-sectionally from the cavity area utilizing FIB milling to examine the cavity height. The measured height of the cavity was 139 nm, which closely approximates the given value of 150 nm. The change in cavity height may be attributed to the bending of the membrane towards the bottom electrode or variations in the thickness of the insulation layer or variations in the thickness of the deposited metal stack. The bottom electrode metal stack, alumina layer, and anodic wafer bonding interface are distinguishable. The FIB/SEM pictures of a CMUT cavity cross-section are shown in Figure 3.3.

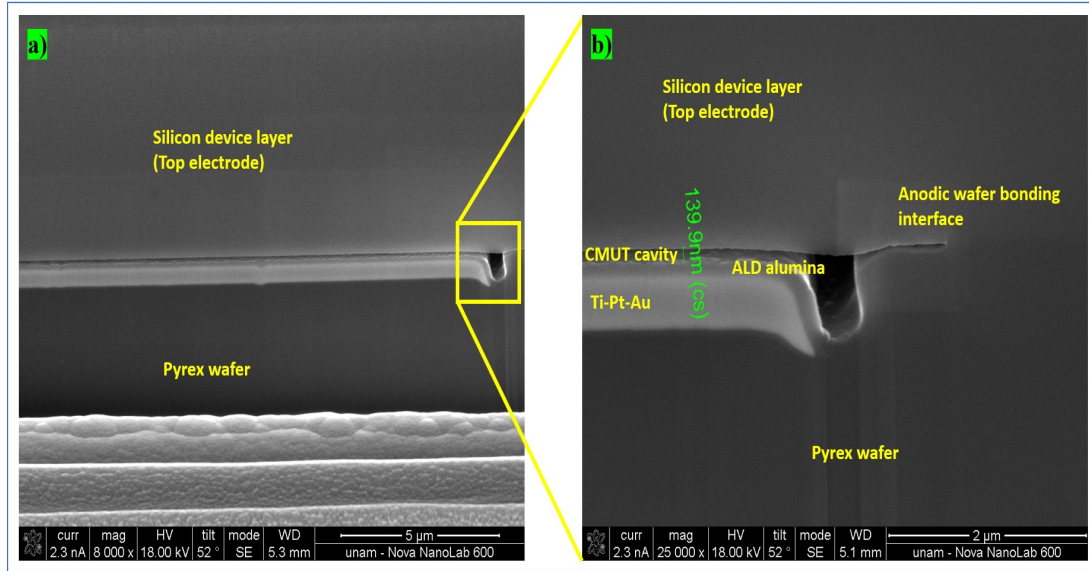


Figure 3.3: SEM images displaying the FIB cross-section of a CMUT cell: (a) 8000 x magnification, (b) 25000 x magnification.

3.2 Resonance Frequency Measurements

The entire microfabrication integration process on the Bond-8 wafer was of relatively higher quality compared to the other seven wafer pairs. Therefore, manufactured and singulated CMUT array chips from the Bond-8 wafer were selected for electrical characterization. Two chips were selected: chip-05 from the wafer's edge and chip-06 from the middle of the wafer, in case the position of the chips might have affected the yield of the entire microfabrication process. The corner chips from a wafer are not preferred for measurements because they partially lost their device layer during the fabrication processes (specifically, during the handle layer removal of the SOI wafer). Figure 3.4 displays the location of chip-05 and chip-06 on the wafer. Each CMUT sensor chip has a total of 256 CMUT cells. The resonance frequency of 64 individual cells in an array of 128 individual cells was attempted to be measured.

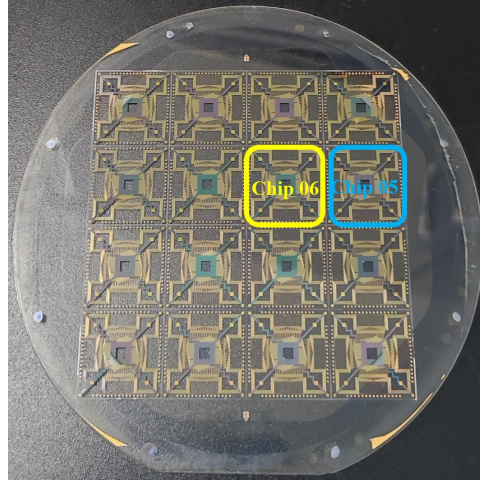


Figure 3.4: An image showing location of Chip-05 and Chip-06 on the Bond-8 wafer.

Impedance/Gain-Phase Analyzer (HP 4194A, Japan) and a probe station (Cascade M 150) were used to measure the conductance (the real part of admittance) of individual CMUT cells in air (while the CMUT gaps were vacuum sealed with Parylene C) to determine the resonance frequency of individual CMUT cells. Figure 3.5 showcases the computer system equipped with LabVIEW software, the impedance analyzer, and the probe station.

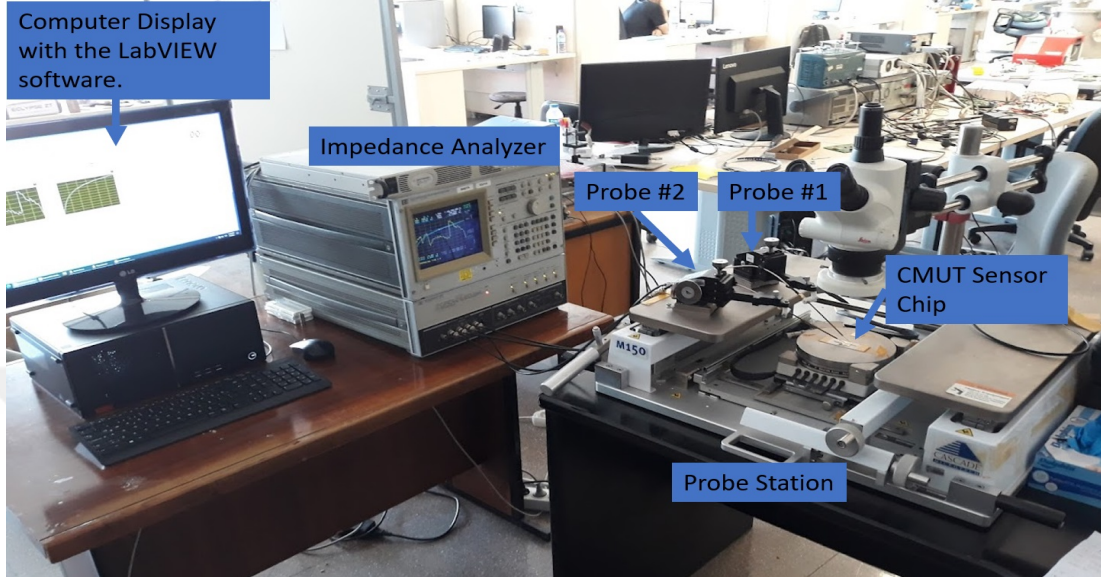


Figure 3.5: Impedance analyzer connected to a computer system and a probe station.

The bottom electrodes of individual CMUT cells were DC plus small AC biased, while the top common electrode (Silicon membrane with Cr-Au and Parylene C on top of them) was connected to a common ground terminal of the impedance analyzer using two probes of the probe station. The stencil-deposited metallic pads were used to establish a connection with the top electrode (Silicon membrane) of the CMUT device, while the supplementary pads for ASIC connections were utilized to access the bottom electrodes of individual CMUT cells using probes on the probe station. Figure 3.6 displays the chip after connecting to the impedance analyzer via a probe station.

The conductance of 64 individual cells from chip-05 and 64 individual cells from chip-06 were measured in air with 1 V AC bias plus DC bias. The 1 V AC bias was kept constant for all the measurements while the frequency was swept between 1 MHz and 10 MHz. The DC bias was applied starting from 1 V DC with a step of 1 V DC increments until the CMUT cell failed with a "DC current overload" warning by the impedance analyzer. The resonance frequency measurements were done up to 25 V DC under a constant AC voltage of 1 V. A small number of cells were already in poor condition and failed at 1 V. However, the majority of cells began to fail at or after 15 V. A sudden surge in

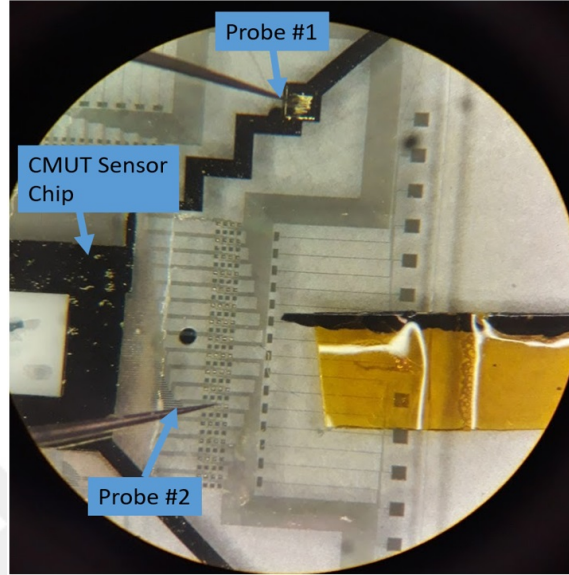


Figure 3.6: CMUT sensor chip connected with the impedance analyzer using 2 probes of the probe station.

the current served as an indicator in the impedance analyzer upon a cell failure. The capacitor begins to behave as a conductor when a CMUT device fails due to dielectric breakdown, an irreversible process. Hence, we opted not to proceed with the measurements above 25 volts to save the CMUT cells for future studies. The statistical data about the yield of CMUT devices from Chip-05 and Chip-06 was collected and presented in Table 3.1. The data explains the yield behavior of the entire microfabrication process. It has been observed that when the applied DC voltage increased from 10 V to 25 V, the yield or the number of functional devices per chip began to decrease.

DC Bias Voltage (in volts)	Chip-05 Yield (in %)	Chip-06 Yield (in %)
10	98.4	89.1
15	76.6	84.4
20	71.9	75
25	46.9	57.8

Table 3.1: Yield data for the CMUT devices of Chip-05 and Chip-06.

Impedance analysis provided the raw frequency and impedance data for all DC bias voltages of individual CMUT cells. The resonance frequency of CMUT cells was visualized by plotting a frequency vs. conductance (the real part of admittance) graph for a certain DC voltage, as displayed in Figure 3.7. The resonance frequency of a CMUT cell that was measured experimentally by the impedance analyzer was in the range of 5.7 – 5.8 MHz, which is close to the resonant frequency of a CMUT cell calculated (5.75 MHz) by a finite element analysis software (OnScale) model developed by another graduate student (Ahmad Elshenety) in our research group based on the realistic experimental conditions. The small peak next to the resonance peak in Figure 3.7 could be related to parasitic effects arising from the packaging and switching components on the PCB used for resonance frequency measurements [49].

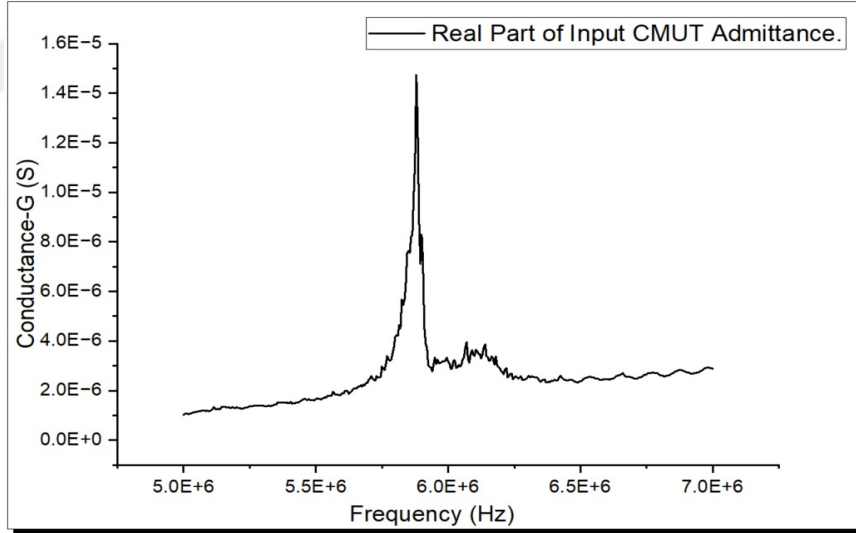


Figure 3.7: Resonance frequency plot of an individual CMUT cell (B08-CH06-CL020) at 25V DC Bias.

The CMUT cells in these CMUT chips were designed to operate at the maximum applied direct current (DC) voltage of 90 V, obtained by ADS (Advanced Design System) software simulations. This maximum DC operating voltage (which is related to the dielectric breakdown voltage of the CMUT gap composed of ALD alumina and vacuum) was a given input for this study. In other words, this thesis study is not about designing the operation DC voltage of the CMUT cells but about microfabricating these CMUT chips to a degree as close

as possible to these calculated and given design parameters.

The Cell-041 and Cell-114 from chip-05 survived until an applied DC voltage of 25 V. Next, we continued measuring their resonance frequency to find out at what voltage they would fail with “DC current overload” warning from the impedance analyzer. Both cells survived and maintained functionality up to the maximum applicable DC voltage of 40 V from the used impedance analyzer. In other words, these two CMUT cells keep their functionality for future studies where higher DC bias voltages may be explored. Based on our experience and observations from these measurements, any CMUT cell that fails with the “DC current overload” warning is not functional anymore. Therefore, we decided not to continue the resonance frequency measurements after 25 V to save these CMUT chips for future studies, such as optoacoustic imaging probe integration.

The resonance frequency was shifted to a lower frequency as the DC bias voltage increased from 15 V to 40 V. This shift in resonance frequency happens due to a phenomenon known as the “spring softening effect” because the effective spring constant of the CMUT cell membrane decreases with the increased voltage [5]. Figure 3.8 displays the frequency versus conductance (the real part of admittance) graph at six different DC bias voltages, clearly showing a shift in the resonance frequency of Cell-114.

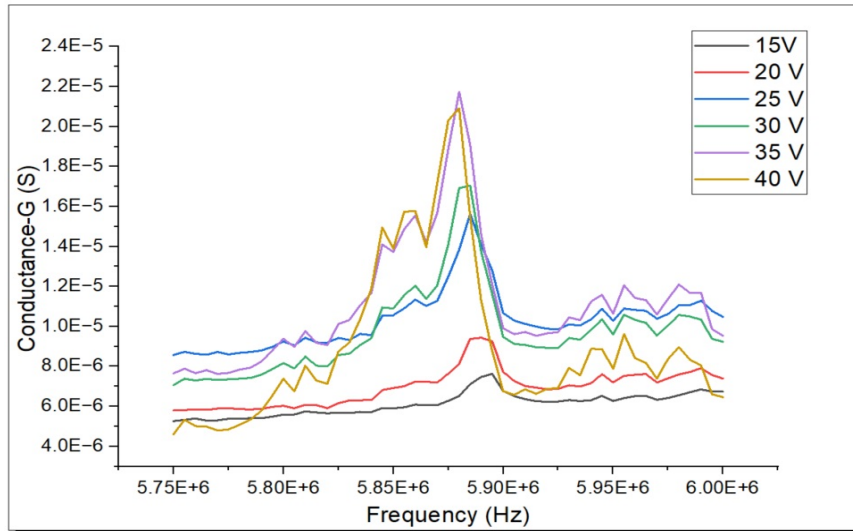


Figure 3.8: Shift in the resonance frequency of the CMUT Cell B08-CH05-CL114.

The possible reasons for the failure of the CMUT cells (before 90 V) could be directly related to the quality of the insulation layer (Al_2O_3), which was deposited using the atomic layer deposition (ALD) technique in our cleanroom facility. There could be two possible scenarios that may affect the quality of the ALD alumina. Firstly, we initially deposited good-quality alumina, which degraded in the subsequent fabrication and integration process steps. Secondly, the deposited alumina was not in good condition from the beginning, and it also deteriorated in the upcoming microfabrication process. Therefore, depositing a high-quality insulating layer and maintaining its integrity throughout the entire microfabrication process is equally important.

Pin holes in the alumina insulation layer were observed after removing the alumina (with AZ 400K etchant) from the electrical pad regions of the CMUT array chips. The presence of pin holes in the insulating layer further strengthens our claim about the poor quality of the alumina layer. Figure 3.9 displays images of the alumina layer captured using the SEM capability of the FIB/SEM dual beam instrument.

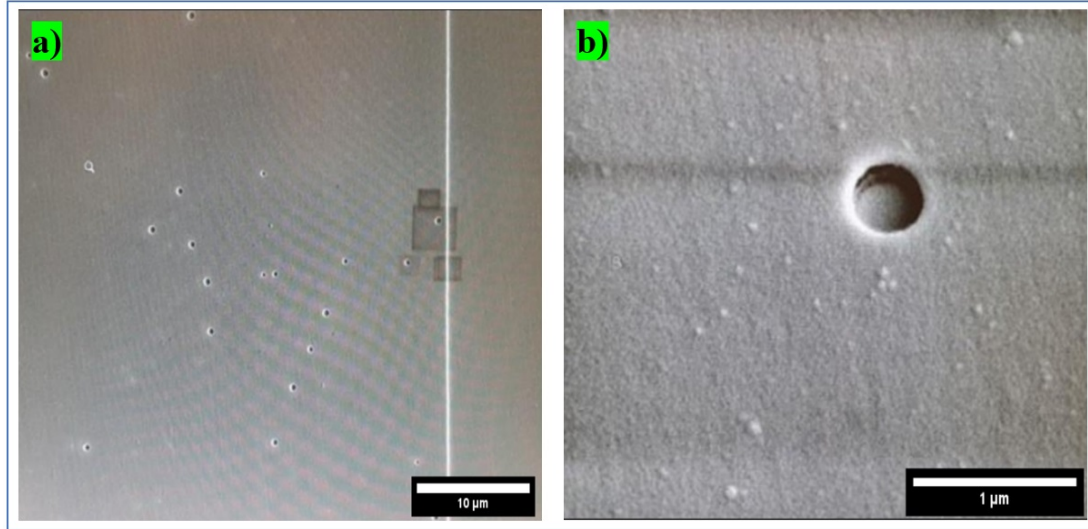


Figure 3.9: Images of pin holes in alumina layer captured by the SEM imaging capability of the FIB/SEM dual beam instrument: (a) 2500 x Magnification, (b) 35000 x Magnification.

Chapter 4

Fully Automated Dicing Saw Processing

4.1 Wafer-Scale Microfabrication of Pseudo MEMS Devices

4.1.1 Device Design

The Microfabrication Mask 1, originally used in the production of capacitive micromachined ultrasonic transducers (CMUTs), is repurposed for the fabrication of pseudo micro-electromechanical system (MEMS) devices for automated dicing saw processing studies. In total, 23 potential target patterns (or the alignment marks) were drawn using a layout editor software on the vacant area of a 16.75 mm by 16.75 mm MEMS device. The target patterns of various geometries and dimensions were created with careful consideration of their design criteria, as shown in Table 4.1 [50]. The circular, square, and rectangular features were created as macro targets, whilst the addition sign, the hash sign, and the rectangle-pair as micro targets. A 4x4 array of MEMS devices was designed on a 4-inch wafer. The MEMS device chip with potential target patterns is shown in Figure 4.1.

Macro Target	Micro Target
It should be a simple figure, less affected by ± 5 degree theta (θ) turning.	It must contain multiple straight lines in the Y-direction and at least one straight line in the X-direction.
Both targets should have high contrast compared to their background.	
Both targets should bear no similar target in the same die, i.e., it should be a unique shape.	

Table 4.1: Design Specifications for the Macro and Micro Alignment Targets.

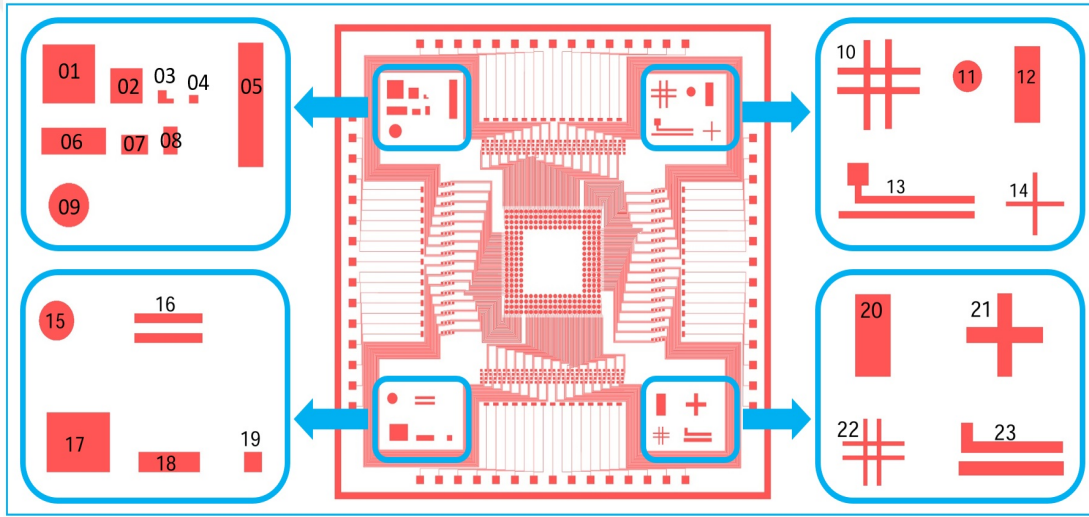


Figure 4.1: Chip-scale drawing of a pseudo MEMS device chip (16.75 mm by 16.75 mm) with 23 potential targets.

4.1.2 Photomask Manufacturing

A 5-inch by 5-inch soda lime glass mask covered with photoresist was first exposed using a laser mask writer (DWL-66FS, Heidelberg). The laser beam exposed photoresist underwent development, followed by wet-etching process of the chrome layer on the glass mask in order to get the desired pattern. Finally, the patterned mask photoresist was removed from the photomask. The photomask created for the photolithography process is shown in Figure 4.2.

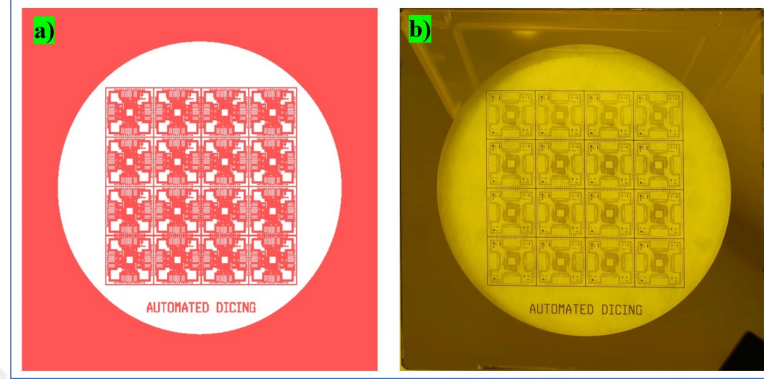


Figure 4.2: Photomask for wafer-scale manufacturing of pseudo MEMS device chips: (a) Photomask design, (b) Manufactured photomask.

4.1.3 Microfabrication of Wafers with Photoresist Features

Both borosilicate glass (Pyrex-7740) and silicon wafers underwent the lithography procedure alone to achieve pseudo-MEMS devices with photoresist features on their surfaces. Both wafers were spin-coated with 1.98-micron thick layer of positive tone photoresist AZ 5214E. The photoresist was pre-baked by putting the wafers on a hot plate for about 50 seconds. The wafers underwent exposure with the ultraviolet dosage of 30 mJ.cm^{-2} after positioning the photomask to the mask aligner. Finally, the photoresist on the wafers was developed with a diluted solution of AZ 400K developer. Figure 4.3 shows the fabricated wafers.

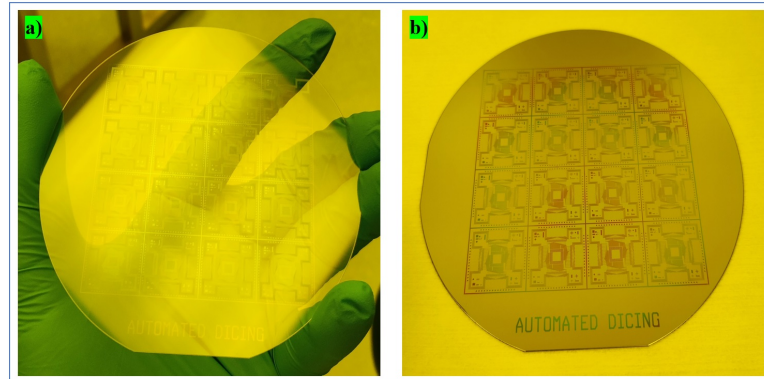


Figure 4.3: Four-inch diameter wafers with pseudo MEMS devices having photoresist features: (a) Pyrex-7740 wafer, (b) Silicon wafer.

4.1.4 Microfabrication of Wafers with Copper Features

Pyrex and silicon wafers underwent a series of processes, including photolithography, metal deposition, and lift-off, to create copper structures on the surface of pseudo-MEMS devices. 1.98-micron thick AZ 5214E photoresist was spin-coated onto the wafers first. It is a negative tone photoresist with image reversal and was used for improved lift-off processing. The photoresist was subjected to soft-baking on a hot plate for about 50 seconds.

Following that, the wafers were exposed (1st exposure) to an ultraviolet dosage of 30 mJ.cm^{-2} after positioning the photomask to the mask aligner. The photoresist was subjected to post-exposure reversal baking by putting the wafers on a hot plate set at a temperature of 120°C for 2 minutes. Next, the wafers covered with photoresist were flood-exposed to ultraviolet light with a dosage of 300 mJ.cm^{-2} (2nd exposure). The photoresist was developed using a diluted solution of AZ 400K developer. The e-beam evaporator was used to produce a copper layer on wafers that was 50 nm thick. Lastly, the wafers were submerged in pure acetone until the photoresist was lifted off. The wafers with copper features are displayed in Figure 4.4.

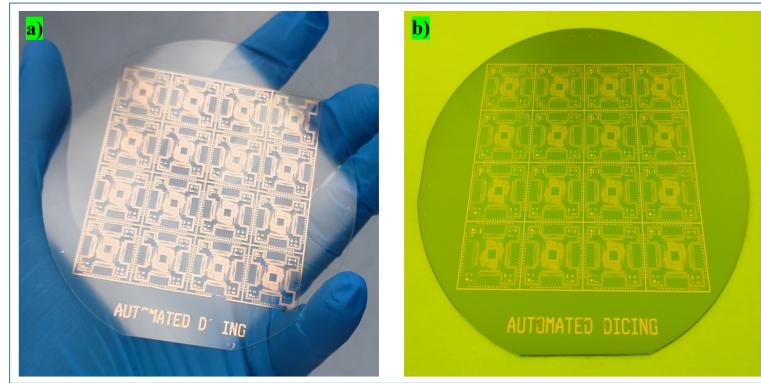


Figure 4.4: Four-inch diameter wafers with pseudo MEMS devices having copper features: (a) Pyrex-7740 wafer, (b) Silicon wafer.

4.2 Selection of Appropriate Targets for Alignment Teaching

Choosing a unique target pattern is essential for an effective teaching alignment procedure. This pattern should have little resemblance to neighboring features on the device or, ideally, no similarity. Suitable target patterns are a prerequisite for a successful alignment teaching operation. In auto-alignment, the macro targets are responsible for the first rough alignment, whilst the micro targets are responsible for the more precise fine alignment. An alignment teaching was conducted for each prospective target pattern to determine the most suitable one. The wafers (Silicon and Pyrex) with pseudo-MEMS devices having photoresist and copper features were used for these studies.

4.2.1 Macro Target Selection

In order to find the right macro target, 15 different targets with square, rectangular, and circular shapes were drawn on each chip of the wafer, as shown in Figure 4.1. Each macro target was taught individually during the teaching process due to its distinct shape and dimensions. The dicing saw subsequently conducted three verification checks to assess the suitability of the target, depending on the Q-values obtained from the verification process.

4.2.1.1 Spiral Check

Once the potential macro target was chosen, the dicing saw did a spiral check to verify the uniqueness of the selected macro target and to confirm that there were no similar targets (or features) present in the same chip. The microscope of the dicing saw scanned the chip in a spiral pattern, starting at the macro target's position. An acceptable macro target should possess a Q-value below 60%, the difference between Q-level and spiral check Q-margin.

The mean Q-values for the 11 macro targets were below 60%, suggesting they are suitable for alignment teaching work. Nevertheless, the dicing machine rejected macro targets with identification numbers 04, 07, 12, and 19 due to their resemblance to adjacent features on the MEMS chip. Please refer to Table 4.2 for the outcomes of the spiral check.

Target Details			Mean Q-Values (in percentage)		
ID no.	Shape	Dimensions (in microns)	Spiral Check	Angle Check	Index Check
01	Rectangle	Length * width = 650 * 675	40.4	51.5	99
02	Square	Length * width = 400 * 400	37.5	74	99
04	Rectangle	Length * width = 110 * 90	Resembles other features on the chip.		
05	Rectangle	Length * width = 308 * 1420	37.4	40	99
06	Rectangle	Length * width = 800 * 300	34.8	56	99
07	Rectangle	Length * width = 325 * 215	Resembles other features on the chip.		
08	Rectangle	Length * width = 170 * 312	45.7	86.5	99
09	Circle	Radius = 250	32.8	97	99
11	Circle	Radius = 175	47.9	96.5	99
12	Rectangle	Length * width = 305 * 850	Resembles other features on the chip.		
15	Circle	Radius = 200	33.4	96.5	99
17	Rectangle	Length * width = 720 * 600	40.4	63	99
18	Rectangle	Length * width = 700 * 200	36.8	55	99
19	Square	Length * width = 200 * 200	Resembles other features on the chip.		
20	Rectangle	Length * width = 365 * 790	38.6	62	98

Table 4.2: Q-value results of the 15 potential Macro Targets having different geometries and dimensions.

4.2.1.2 Angle Check

The purpose of this verification check is to rectify any considerable tilt of the wafer during auto-alignment, which may occur during sample preparation. The dicing saw purposely tilted the workpiece by up to $\pm 5^\circ$ and attempted to identify the same target pattern inside the same die after rotating. An acceptable macro target must maintain a Q-value above the Q-level threshold (80%), meaning the identified and recorded targets should exhibit maximum similarity.

The macro targets 01, 02, 05, 06, 17, 18, and 20 showed average Q-values of 51.5%, 74%, 40%, 56%, 63%, 55%, and 62% after the angle check. These results indicate that these targets are not appropriate for the alignment teaching. Conversely, the dicing machine recognized targets 08, 09, 11, and 15 as suitable macro targets due to their Q-values above 80%. The Q-value outcomes of the angle verification are shown in Table 4.2.

4.2.1.3 Index Check

In order to determine whether the neighboring chip has the same macro target, the dicing saw moved one index to the right on the wafer and performed an index check. The Q-value must be above the Q-level requirement of 80% for the macro target to be acceptable.

Based on the statistical data shown in Table 4.2, it was observed that 11 out of 15 potential macro targets achieved Q-values over 98%. This indicates that these targets are suitable for alignment teaching.

4.2.1.4 Macro Target Selection Results

The dicing saw rejected 11 potential macro target patterns that were not suitable for alignment teaching work based on the outcomes of the three verification checks. Figure 4.5 illustrates that 3 circular targets and 1 rectangular target had

the greatest Q-values in angle and index checks, whereas they had the lowest values in spiral checks compared to the other targets.

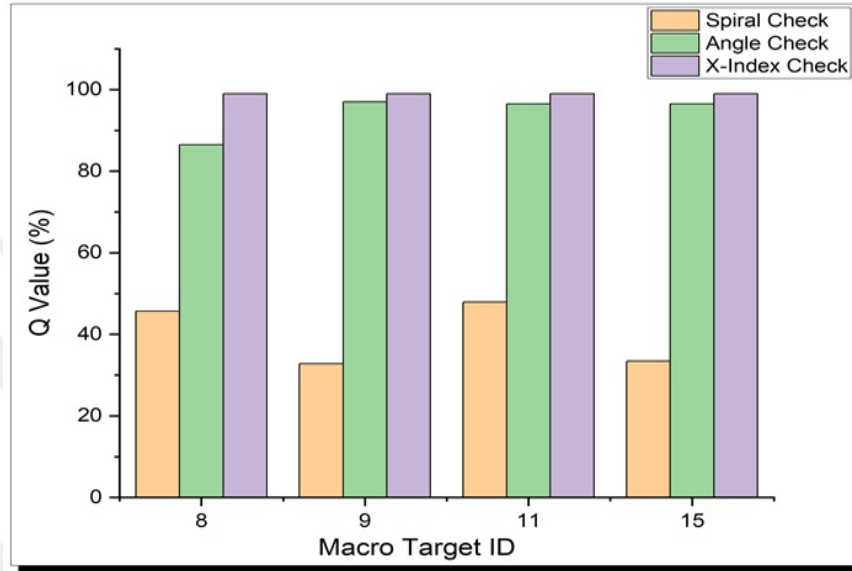


Figure 4.5: Q-value outcomes of the 4 approved macro targets.

The idea behind the suitability of a macro target is that it should be a simple figure less affected by the angle or rotational movement. The circle remained unaffected as a macro target, allowing the dicing machine to locate it during auto-alignment despite significant shifts in its position while prepping the workpiece. Circles with different radii were found to be the most appropriate macro target as they successfully passed all three verification checks during the alignment teaching trials. However, the dicing machine identified just one rectangular target as acceptable out of 12 rectangular and square features. Thus, this research suggests using circular features as suitable macro targets.

4.2.2 Micro Target Selection

Alignment teaching was conducted on 8 potential micro targets in sequential order to choose the optimal target. The dicing saw performed two verification tests to determine the suitability of the selected target pattern.

4.2.2.1 Spiral Check

The dicing saw performed a spiral check in 9 separate view fields at a high magnification of 7.5X to verify the absence of any identical micro targets. The microscope camera provides a high-magnification view field of 640 microns by 640 microns. A micro-target with a Q-value below 60% is considered acceptable since it has less resemblance with other chip features.

Each of the 8 potential micro targets had Q-values lower than the 60% threshold, with target 23 boasting the highest Q value at 56%. The results of the spiral check's Q-values are shown in Table 4.3.

Target Details			Mean Q-values (in percentage)	
ID no.	Shape	Dimensions (in microns)	Spiral Check	Angle Check
03	Polygon	Edge lengths = 148*190*47*90	34.25	98.5
10	Hash symbol	Arm thickness = 75	43.57	98.5
13	Rectangle-pair	Width of one bar = 80	30	99
14	Addition symbol	Arm thickness = 50	41.75	99
16	Rectangle-pair	Width of one bar = 95	45.75	97.25
21	Addition symbol	Arm thickness = 150	29.5	98.75
22	Hash symbol	Arm thickness = 40	46	98.5
23	Rectangle-pair	Width of one bar = 130	56	97.25

Table 4.3: Q-value results of the 8 potential micro targets having different geometries and dimensions.

4.2.2.2 Index Check

The microscope of the dicing saw moved along the Y-axis and X-axis to detect the chosen micro target on 8 additional dies or chips. The tool used the index values (or the chip dimensions) included in the device data to move to the other chips. The Q-value must be above the 80% threshold to be considered an acceptable micro target.

In this verification test, all 8 micro targets exhibited Q-values over 97%, indicating their suitability for alignment teaching. Table 4.3 displays the Q-values for the index check of the micro targets.

4.2.2.3 Micro Target Selection Results

The potential targets, including the hash sign, addition symbol, and rectangle-pair, all showed promising results in alignment teaching trials, as seen in Figure 4.6. These targets qualify as appropriate micro targets because they include many straight lines in the X-direction and at least one straight line in the Y-direction. The presence of straight lines is essential for achieving precise auto-alignment, and their absence negatively impacts the alignment accuracy. Therefore, this research proposes using the addition sign, rectangle-pair, and hash symbol as suitable micro targets for the alignment teaching operation.

4.2.3 Limitations on the Target Dimensions

The maximum size of the target window—2.52 mm by 2.52 mm in low magnification mode and 0.332 mm by 0.332 mm in high magnification mode—limits the size of the macro and micro targets, respectively. In addition, it is crucial to ensure that the straight lines on a target are spaced appropriately: the minimum distance between two lines should be 160 microns when the microscope is set to high magnification and 16 microns when the microscope is set to low

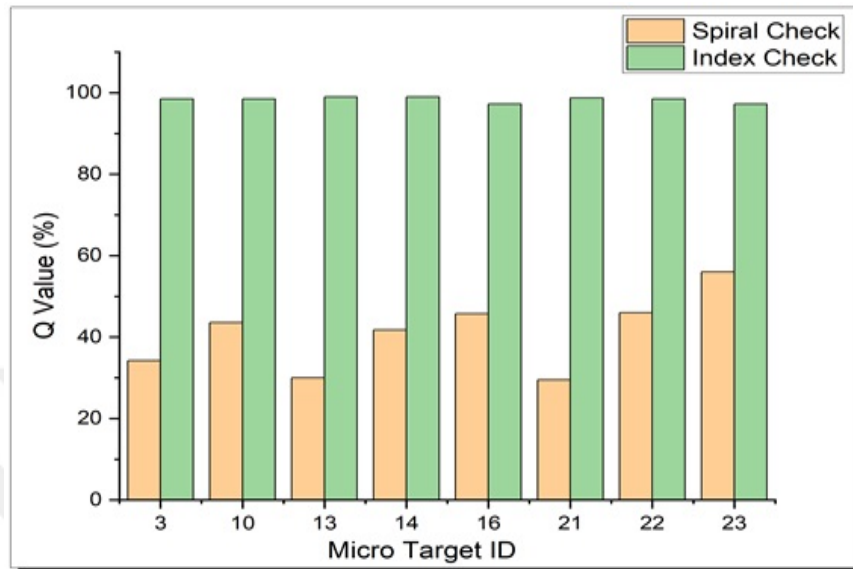


Figure 4.6: Q-values of the approved micro targets.

magnification.

4.3 Alignment Teaching Procedure

4.3.1 Sample Preparation

Establishing a reliable alignment-teaching procedure begins with properly preparing the samples. The dicing frame was first attached to the adhesive side of the dicing tape, with the monogram of the dicing frame (DISCO) positioned towards the user and facing upwards. The 4-inch wafer was attached to the frame by aligning their midpoints manually. The air trapped between the dicing tape and the wafers was removed by positioning it on the chuck table of the dicing saw for roughly 30 minutes. The vacuuming feature of the chuck table and the dicing tape's permeable material assisted in extracting the air. Figure 4.7 displays a prepared sample.

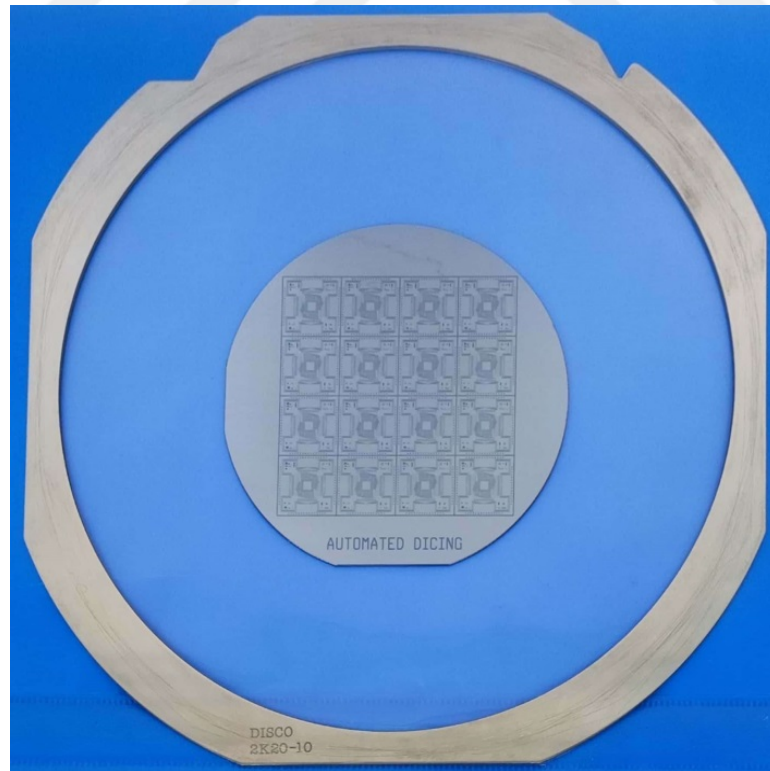


Figure 4.7: Four-inch diameter Silicon wafer mounted on a dicing frame to prepare the sample for the alignment teaching and fully automated dicing.

4.3.2 Device Data Preparation

The dimensions of the workpiece and the dicing tape were recorded on the Device Data screen, including their size, shape, and thickness. The Y-index, the workpiece's feed rate, the blade height (from the chuck table), and the blade RPMs were also entered as cutting parameters. The Measure feature on the device data screen enables the finding of real-time index values. The angle between channel CH1 and channel CH2 was kept at 90 degrees because of the square MEMS chips. Figure 4.8 displays a print screen displaying the device data.

The screenshot displays the 'Device Data' screen with various input fields and tables. The 'Work shape and size' section includes radio buttons for 'Round' (selected) and 'Square', with a diameter of 101.600 mm. Channel dimensions (Ch1, Ch2) are 0.000 mm. Work Thickness is 0.500 mm and Tape Thickness is 0.150 mm. Spindle rev. is 20000 /min, Precut process No. is 0, and Cutting ch seq. is 12. A table shows parameters for Ch 1 and Ch 2, including Blade height, Feed speed, Y-index, Repeat times, and Cut mode. Navigation arrows are at the bottom.

Work shape and size		Ch 1		Ch 2		Ch 1			Ch 2		
☒ Round	101.600 mm	Ch1	0.000 mm	Ch2	0.000 mm	SEQ1	SEQ2	SEQ3	SEQ1	SEQ2	SEQ3
☐ Square						0.075	0.000	0.0	0.075	0.000	0.0
Work Thickness	0.500 mm					5.000	0.000	0.0	5.000	0.000	0.0
Tape Thickness	0.150 mm					17.0000	0.0000	0.00	17.0000	0.0000	0.00
Blade height						0	0		0	0	
Feed speed											
Y-index											
Repeat times											
θ Deg.	0.000°										
Cut mode	A										
Cut dir.	FRONT										
Cut	0 lines										
Offset Y	0.0000										
Noncut F	0.000										
Noncut R	0.000										

Figure 4.8: Device data screen of dicing saw displaying workpiece dimensions and cutting parameters.

4.3.3 Alignment-Data Preparation

The Q-Value: The dicing saw determines whether the recorded and detected targets are similar by comparing their images during the alignment teaching and auto-alignment operations. The Q value, with an overall magnitude of 100, indicates the degree of similarity between images of a detected target pattern and a recorded target pattern.

The Q-Level: The minimum threshold Q-value (or the Q-level) for an acceptable target pattern for angle and index verification checks was set to 80% in the alignment data. The 20% tolerance was added to the Q-value due to the microfabrication limitations of the MEMS devices.

Theta Adjust Stroke: The value of the theta adjust stroke was input as 70%, indicating that during theta alignment, the microscope of the dicing saw travels horizontally from left to right or vice versa over a distance equal to 70% of the wafer's diameter.

The Spiral Check Q-Margin: The spiral check Q-margin was set to 20% in the alignment data function screen; it provides a tolerance of 20% to the Q-level for spiral check verification during alignment teaching operation. The resultant Q-value of an appropriate target pattern should be less than the difference between the numerical values of the Q-level and the spiral check Q-margin.

In addition, the alignment teaching operation will automatically record the window size X, window size Y, direct light level, oblique light level, street adjustment, and hairline width. Figure 4.9 displays a screenshot of alignment data.

Alignment Data (3.1.3)

Alignment mode: NORMAL
 Alignment pattern: A
 Time out: 30 s
 Retry count: 3
 Permissible Y adjust: 0.0020 mm
 Permissible θ adjust: 0.0020 mm
 Index check: θ adjust stroke: 70 %
 X position: 0 die
 Y position: 0 die
 Permission: 0.010 mm
 Escape data auto adjust: ☐

Focus data
 Focus timing: MIC
 Focus mode: WORK
 Focus stroke: 0.100 mm
 Focus step: 0.050 mm
 By point distance: 0.0 mm
 Focus pos.: 0.000 mm
 (- for upper)

	Macro	Ch1	Ch2	Ch3	Ch4	
Q-level	80	80	80	80	80	%
Window size X	52	254	254	254	254	pixel
Window size Y	48	254	254	254	254	pixel
Light level dir	30	28	27	28	27	%
Light level obl	0	0	0	0	0	%
Street adjust		3.3388	2.8299	13.2540	2.2098	mm
Hairline width		186	184	186	184	pixel

Target Display

Figure 4.9: Print screen of dicing saw displaying the alignment data.

4.3.4 Workpiece Loading

The dicing frame with a wafer was first set up on the chuck table of the dicing saw machine, as shown in Figure 4.10. Due to the manual preparation of the wafer sample, the dicing streets (or cutting lines) were not aligned parallel to the dicing blade. Therefore, the tilt of the dicing streets will also be adjusted during the alignment teaching.

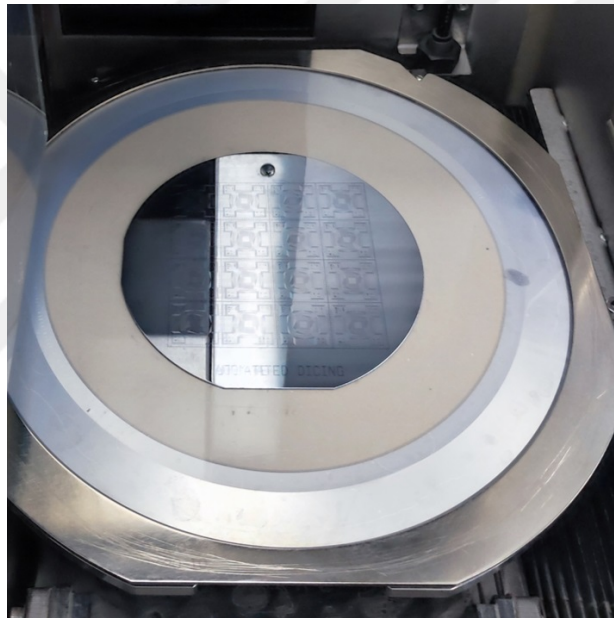


Figure 4.10: Silicon wafer positioned on the chuck table of the dicing saw.

4.3.5 Low Magnification (0.75X) Rough Theta Alignment

The macro target window was opened using the F1-Teach option from the manual operations menu after the dicing saw was initialized. Optimal contrast between the features on the wafer was achieved by manipulating the intensity of direct and oblique lighting from the microscope. The light information was then saved by clicking the Enter button. The focus of the microscope was then adjusted to the surface of the wafer using the Focus button. The Exit button was hit in order to return to the macro target window.

The center of the green target window was first aligned with the edge of the dicing street on the left-hand side of the wafer, as displayed in Figure 4.11. Upon clicking the Align- θ button, the microscope traveled to the right side of the wafer, covering a distance equivalent to 70% of the wafer diameter. Next, the center of the green target window was aligned parallel to the edge of the dicing street on the right side of the wafer. It is advised to repeat this operation many times until the center of the green target window aligns parallel to the edge of the dicing street.

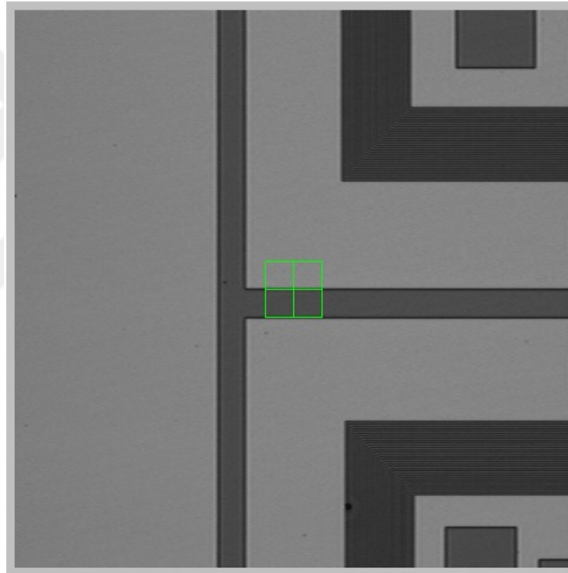


Figure 4.11: Print screen of the dicing saw after the target window was aligned horizontally with the dicing street edge on the wafer at low magnification (0.75X).

4.3.6 Channel 1 Macro Target Teaching

The microscope was again adjusted for illumination and focus to provide optimum contrast for the features on the wafer, as explained in the preceding section. The circle was enclosed inside the green target window as a macro target since only the window interior is considered a target. The dimensions of the target window concerning the size of the circle were adjusted using the ADJ-Window function. The dicing saw machine performed spiral, angle, and index verification

checks after pressing Enter to determine whether the chosen macro target was appropriate. The dicing machine indicated in the information bar that the "Target is good" based on the Q-value results of all three verification tests. Figure 4.12 shows the Q-values of an acceptable macro target. The macro target information was recorded by pressing the Enter key. The macro target has to be taught again if the dicing machine determines that the selected target is incorrect.

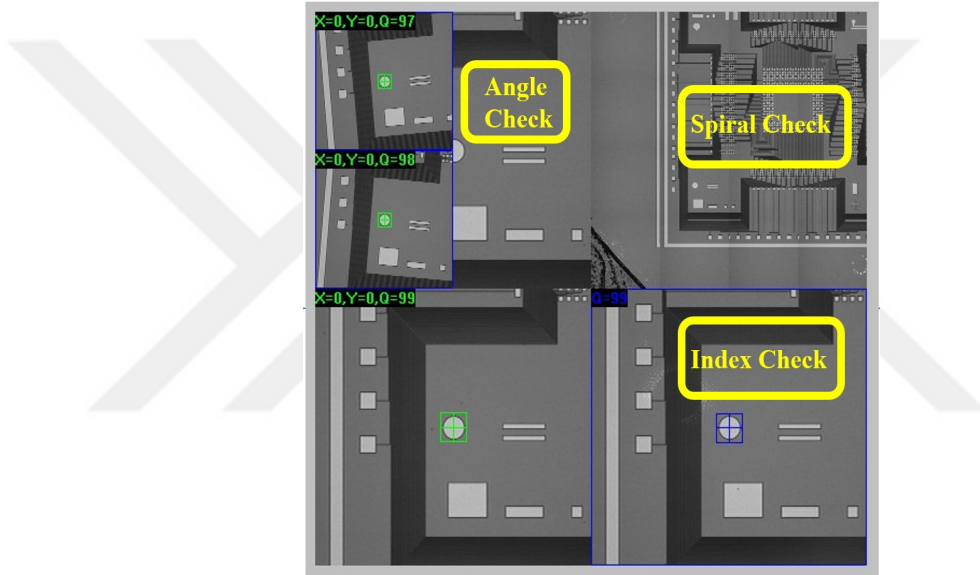


Figure 4.12: Q-value results of a good CH1 Macro target.

4.3.7 High Magnification (7.5X) Fine Theta Alignment

The microscope's magnification automatically switches to higher magnification (7.5X) after entering the micro-target teaching screen. For precise tilt correction in the wafer, the fine theta alignment was repeated at high magnification, identical to the one done at low magnification in section 4.3.5. Figure 4.13 displays the green target window once its center is horizontally aligned with the edge of the dicing street.

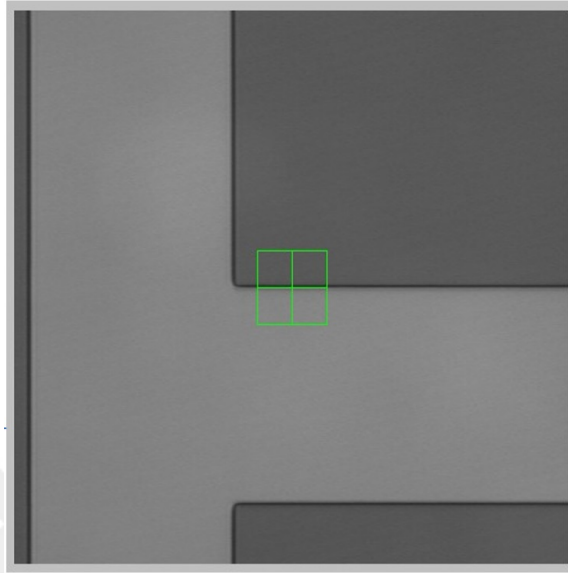


Figure 4.13: Print screen of the dicing saw after the target window was aligned horizontally with the dicing street edge on the wafer at high magnification (7.5X).

4.3.8 Channel 1 Micro Target Teaching

Once the fine theta alignment had been completed, the microscope's illumination and focus were adjusted for the optimum contrast of the features on the wafer. The addition symbol (+) from one of the MEMS device chips was enclosed inside the green target window as a micro-target. The ADJ-Window function on the user interface was used to adjust the height and width of the target window according to the dimensions of the micro-target. The Enter key was pressed after the selection of the micro-target to check whether the selected target was appropriate. The dicing saw conducted spiral and index verification checks and displayed the result in the information bar as "Target is good." If the dicing saw determines that the micro-target is inaccurate, it is advisable to repeat the teaching process with another appropriate target. Figure 4.14 displays the Q-value outcomes of a good micro-target.

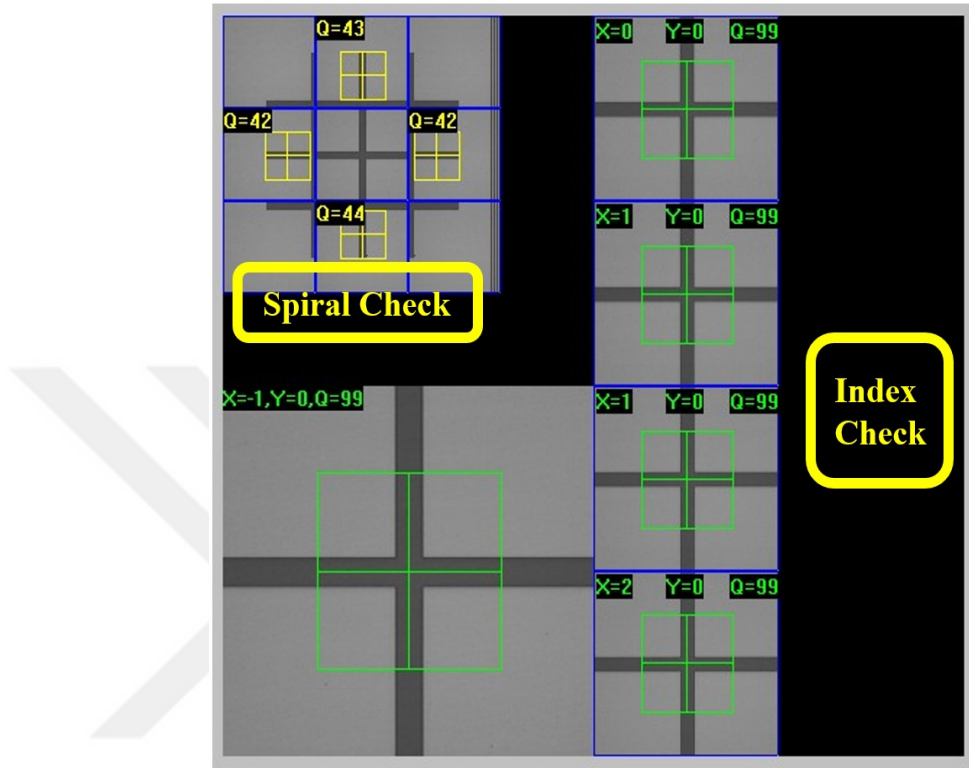


Figure 4.14: Q-value outcomes of a good CH1 Micro target.

4.3.9 Channel 1 Street Adjustment

The Micro Street Adjust display appears automatically after recording the micro-target in channel 1. The hairline's dotted borders were aligned parallel with the edges of the dicing street to accurately measure the distance between the micro-target and the cutting line. The distance from the micro-target to the street was measured and used as the first reference for the cutting process. It is recommended to conduct street adjustments at the intersection of two dicing streets. To avoid the dicing saw from misidentifying other features as kerf during kerf check, ensure that there are no identical patterns by moving in the x-direction. Figure 4.15 exemplifies a well-executed street adjustment.

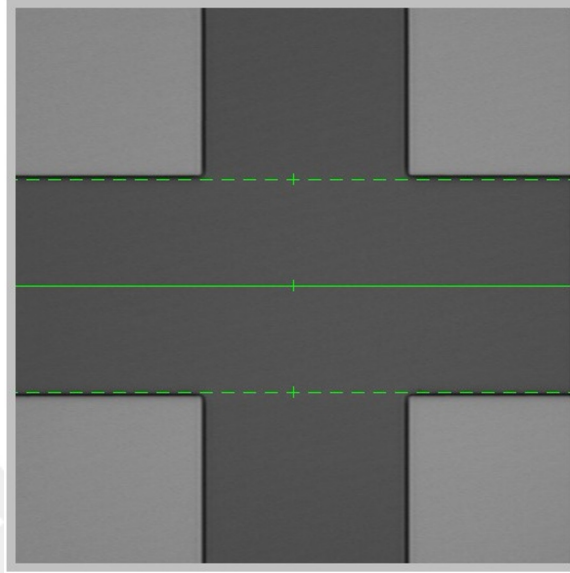


Figure 4.15: Hairline of dicing saw aligned with the dicing street on the wafer in CH1.

4.3.10 Channel 2 Micro Target Teaching and Street Adjustment

The wafer was rotated at an angle of 90 degrees (as recorded in device data) by the automated movement of the chuck table to reach the micro-target teaching window in channel 2. The hash symbol feature (#) was selected as a second unique micro-target for teaching operation. In CH2, the street adjustment and micro-target teaching followed the same steps as in CH1's teaching procedure. Please see Sections 4.3.8 and 4.3.9 for reference. Figure 4.16 presents the Q-values of an acceptable micro-target.

Note: The alignment teaching in channels 1 and 2 is sufficient for square or rectangular MEMS devices. However, it is possible to teach alignment in channels 3 and 4 for hexagonal or octagonal devices.

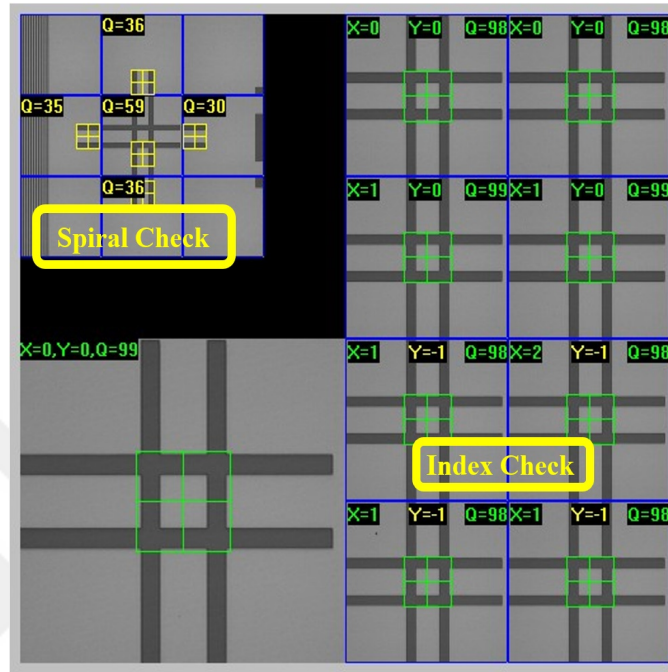


Figure 4.16: Q-value outcomes of a good CH2 Micro target.

4.3.11 Teaching Data Writing

When the teaching procedure on macro and micro-target patterns was finished, the data was saved in the dicing saw by pressing the Enter key. Figure 4.17 displays the recorded macro and micro targets.

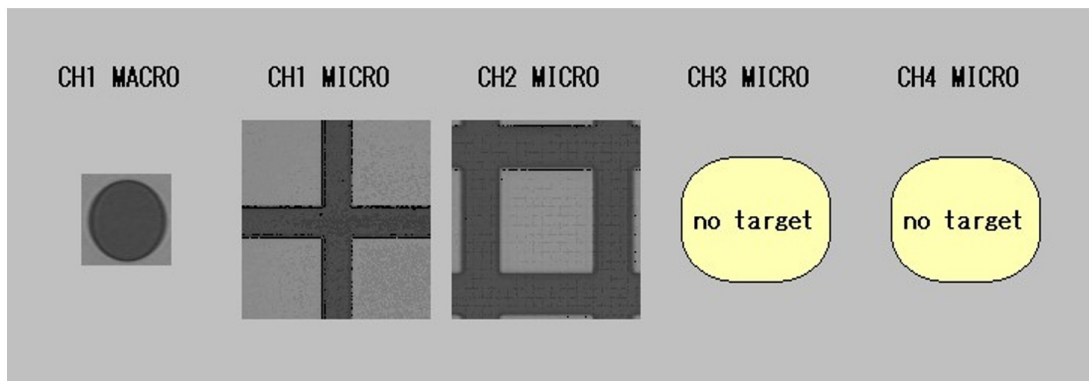


Figure 4.17: Print screen of the dicing saw displaying 1 Macro and 2 Micro targets recorded during alignment teaching operation.

4.4 Potential Errors in Alignment Teaching and Their Troubleshooting

4.4.1 Wrong Target Selection

If the target verification procedure detects a comparable target (or feature) near the chosen target, the dicing saw will show an error message stating, "Target is not good." The chosen target in Figure 4.18 had a 99% similarity to a neighboring feature. This error may occur if the selection window does not have a target.

Solution: Selecting a unique target pattern that does not resemble any structure on the chip can fix this issue.

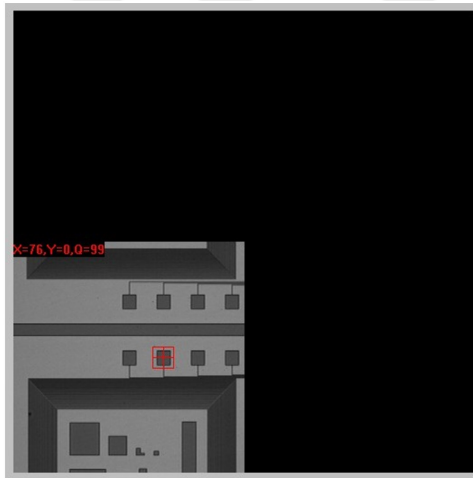


Figure 4.18: Print screen of the dicing saw displaying a rejected target pattern due to the presence of similar features nearby on the pseudo-MEMS chip of the wafer.

4.4.2 Index-Check Error

Index error occurs when the index value recorded in the dicing saw — the distance between the centers of two successive dicing streets — does not match the actual index value on the wafer. Consequently, the dicing saw terminates the alignment

teaching operation with the error message “Index check is not good.”

Solution: The Measure function can determine the real-time and precise index values on the wafer. The revised index values will rectify the index error.

4.4.3 Error due to Fabrication Defects

Fabrication flaws are mostly inevitable in a multi-user cleanroom facility, and these inaccuracies may be in the form of missing features or unwanted particles in different locations of the wafer. If the manufacturing defects are located on or near the target patterns, alignment errors might occur as a result of target misrecognition by the dicing saw. In Figure 4.19, the manufacturing defects can be seen around the features.

Solution: To prevent the misrecognition of targets during dicing, it is advisable to use a combination of direct and oblique illumination to achieve the optimal contrast of the features on the substrate. Selecting a defect-free target is an alternative approach to address this problem.

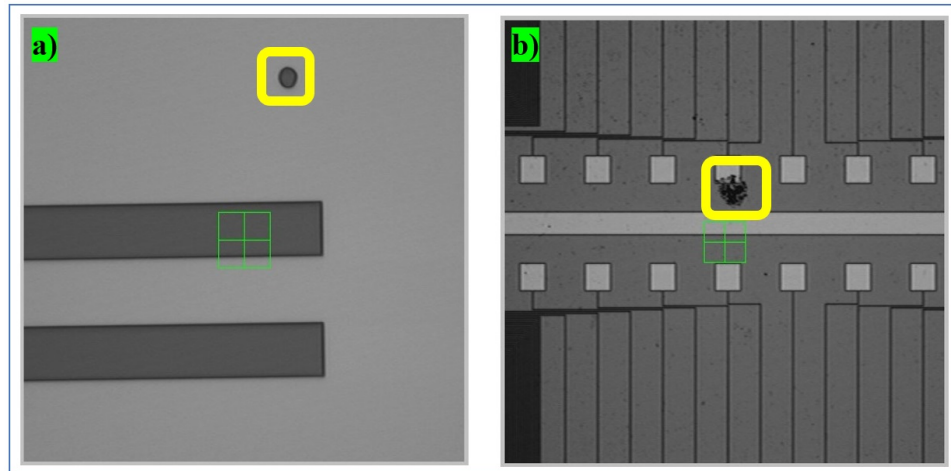


Figure 4.19: Microfabrication defects on the pseudo-MEMS chips of the wafer: (a) Undeveloped photoresist feature, (b) A cluster of unwanted particles.

4.5 Fully Automated Dicing Operation

Alignment teaching is a pre-requisite for the complete automation of the dicing saw operation. Following the successful alignment teaching, the dicing saw tool readies itself for the automated dicing. A single touch of the Start button in the Full-Automation user interface initiated a two-channel automated dicing process. No further support was needed for the dicing after this stage. The dicing saw performed an automatic alignment and then diced the workpiece into square pseudo-MEMS device chips. Figure 4.20 depicts a 4-inch silicon wafer successfully diced into chips utilizing a completely automated dicing process.

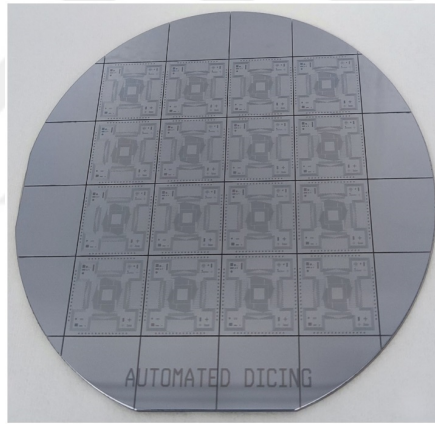


Figure 4.20: A 4-inch diameter Silicon wafer diced into 16 pseudo-MEMS chips using fully automated dicing saw processing.

4.5.1 Potential Applications of Alignment Teaching Assisted Automated Dicing

A fully automated dicing process was developed and implemented for the pseudo MEMS devices produced on Pyrex and Silicon wafers, which possess photoresist and copper features on their surface. Hence, the alignment teaching assisted fully automated dicing operations can be developed for other MEMS devices, irrespective of the substrate material and the material of their features. The primary difference is that the Q-values will vary based on the contrast of the features according to the materials used for the substrate and device structures.

4.6 Dicing Saw Processing Time

The overall time duration of the dicing saw operation has the components explained below: the cutting time for the dicing blade (T_1), the time used for the chuck table to return during multiple-step cutting (T_2), the time required for the chuck table for line switching (T_3), the time needed for the chuck table for channel switching (T_4), and the time taken for the blade to ascend and descend before and after completing a cut (T_5).

$$T_{total} = T_1 + T_2 + T_3 + T_4 + T_5 \quad (4.1)$$

4.6.1 Cutting Time (T_1)

Cutting time is defined as the time when the dicing blade touches the substrate and cutting is being performed. Equation 4.2 is the general expression to calculate the time of basic machining processes, such as drilling, turning, and milling [51].

$$T = \frac{L}{F} \quad (4.2)$$

where T is the cutting time in seconds, L is the total cutting length in millimeters, and F is the feed rate in millimeters per second.

The blade holder remains stationary while the blade rotates at a specified RPM during the dicing process. Moreover, the chuck table travels towards the blade holder while carrying a substrate that is mounted and is meant to be cut into chips. Equation 4.2 could also calculate the cutting time of a dicing experiment by introducing another parameter, step cutting (S), which specifies whether the wafer was cut across its thickness in a single step or multiple steps. Equation 4.3 is used for calculating the time of the cutting process performed by the dicing saw.

$$T_1 = S * \left(\frac{L_{total}}{F} \right) \quad (4.3)$$

Total Cutting Length (L_{total}): It is defined as the distance between the centers of the dicing blade at the beginning and end of a cut line. In order to simplify the computations, we assumed that the wafer is symmetrical, meaning that there are equal numbers of chips or cutting lines on each side of its diameter. In the given case, the semicircle was diced by three cut lines starting from the center. The schematic of the wafer with a diameter equal to the cutting length line L_1 and a center C is shown in Figure 4.21. The L_2 and L_3 cutting lengths were determined using the Pythagorean theorem for triangle ABC and triangle CDE, respectively, as shown in Equations 4.7 and 4.11. Equations 4.7 and 4.11 were used to produce a general formula for the length of a single cut line on a wafer, given in Equation 4.12. The cutting length of a semicircle was first calculated and then doubled to estimate the overall cutting length of the wafer inside a single channel. Equation 4.13 displays the mathematical expression for the entire cutting length of the wafer.

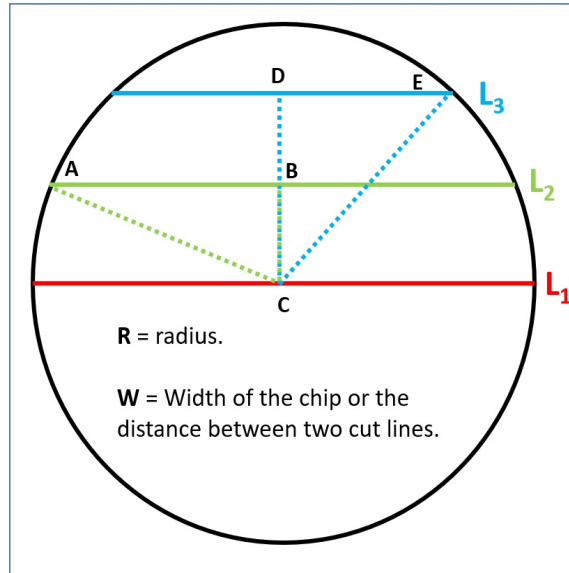


Figure 4.21: Schematic of the wafer for cutting length calculations (not drawn to scale).

$$(R)^2 = (1 \times W)^2 + \left(\frac{L_2}{2}\right)^2 = W^2 + \frac{L_2^2}{4} = \frac{(4W^2 + L_2^2)}{4} \quad (4.4)$$

$$4R^2 = 4W^2 + L_2^2 \quad (4.5)$$

$$L_2^2 = 4(R^2 - W^2) \quad (4.6)$$

$$L_2 = 2\sqrt{R^2 - W^2} \quad (4.7)$$

Similarly,

$$(R)^2 = (2 \times W)^2 + \left(\frac{L_3}{2}\right)^2 = 4W^2 + \frac{L_3^2}{4} = \frac{(16W^2 + L_3^2)}{4} \quad (4.8)$$

$$4R^2 = 16W^2 + L_3^2 \quad (4.9)$$

$$L_3^2 = 4(R^2 - 4W^2) \quad (4.10)$$

$$L_3 = 2\sqrt{R^2 - 4W^2} \quad (4.11)$$

Hence, the general formula for the length of a cut line on the wafer:

$$L_n = 2\sqrt{R^2 - (n-1)^2W^2} \quad (4.12)$$

The total cutting length of the wafer in a single cutting channel:

$$L_{total} = 4 \left(\sum_{n=1}^n \sqrt{R^2 - (n-1)^2 W^2} \right) \quad (4.13)$$

Equation 4.14 provides the revised equation for the cutting time with the addition of the cutting length formulation.

$$T_1 = S * \left(\frac{4 \left(\sum_{n=1}^n \sqrt{R^2 - (n-1)^2 W^2} \right)}{F} \right) \quad (4.14)$$

where S represents the number of depth steps taken during the dicing process, R represents the radius of the wafer, n represents the position of the cut line from the center, W represents the width of the chip along with the dicing street width, and F represents the feed rate.

4.6.2 Chuck Table Return Time in Multi-Step Cutting (T_2)

The thickness and mechanical properties of the wafer determine whether it can be diced in a single step or whether the cutting process has to be done in multiple repetitive depth steps. In multi-step cutting, the chuck table returns to its original position on the same cut line after the 1st step without performing any cutting. Once the first cutting phase is finished, the 2nd cutting step follows the same line at a given cut depth. The chuck table returns horizontally (along X-axis) at a speed different from the feed rate by covering the distance equivalent to the length of the line it diced during the previous step. The cutting is not performed while the chuck table returns to its starting position. However, this prolongs the overall processing time for the dicing operation. The time required for the return of the dicing blade in multi-step cutting can be determined using Equation 4.15.

$$T_2 = (S - 1) * \left(\frac{L_{total}}{C_s} \right) \quad (4.15)$$

The total distance travelled by the chuck table (equivalent to L_{total}) was calculated in the section 4.6.1; therefore, the equation 4.15 is developed as follows:

$$T_2 = (S - 1) * \left(\frac{4 \left(\sum_{n=1}^n \sqrt{R^2 - (n - 1)^2 W^2} \right)}{C_s} \right) \quad (4.16)$$

where S represents the number of depth steps taken during the dicing process, R represents the radius of the wafer, n represents the position of the cut line from the center, W represents the width of the chip along with the dicing street width, and C_s represents the chuck table speed along X-axis.

4.6.3 Line Switching Time (T_3)

The dicing saw consumes additional time when the chuck table positions the dicing blade from one cutting line to an adjacent cutting line. The line switching time may be calculated by dividing the travel distance (D_{total}) of the chuck table by its speed, as shown in Equation 4.17.

$$T_3 = \left(\frac{D_{total}}{C_s} \right) \quad (4.17)$$

Total Line Switching Distance (D_{total}): The chuck table moved diagonally, traversing the distances D_2 and D_3 , facilitating the positioning of the blade from line L_1 to L_2 and from line L_2 to L_3 , respectively. Figure 4.22 provides the schematic of the wafer. The Pythagorean theorem was used in triangle ABC to calculate the distance D_2 covered by the dicing blade as it switched from line L_1 to line L_2 . Similarly, the distance D_3 covered by the chuck table while traveling from line L_2 to L_3 was estimated by finding the diagonal of the EFG triangle. The

mathematical expressions for distance D_2 and D_3 are provided in Equations 4.21 and 4.25. Equation 4.26 is the generic formulation for the distance covered by the chuck table when switching from one line to another. The total line switching distance during a dicing process can be calculated using the analytical expression given in Equation 4.27.

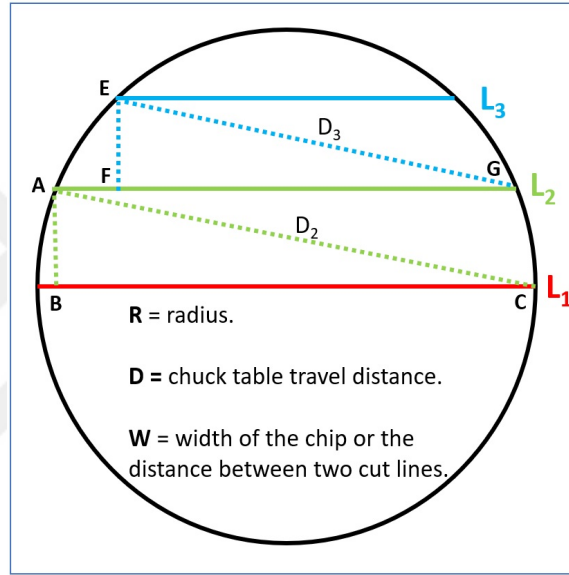


Figure 4.22: Schematic of the wafer for calculating line switching distance (not drawn to scale).

$$D_2^2 = W^2 + \left(\frac{L_1}{2} + \frac{L_2}{2} \right)^2 \quad (4.18)$$

$$D_2^2 = W^2 + \frac{(L_1 + L_2)^2}{4} \quad (4.19)$$

$$D_2^2 = \frac{4W^2 + (L_1 + L_2)^2}{4} \quad (4.20)$$

$$D_2 = \frac{\sqrt{4W^2 + (L_1 + L_2)^2}}{2} \quad (4.21)$$

Similarly,

$$D_3^2 = W^2 + \left(\frac{L_2}{2} + \frac{L_3}{2} \right)^2 \quad (4.22)$$

$$D_3^2 = W^2 + \frac{(L_2 + L_3)^2}{4} \quad (4.23)$$

$$D_3^2 = \frac{4W^2 + (L_2 + L_3)^2}{4} \quad (4.24)$$

$$D_3 = \frac{\sqrt{4W^2 + (L_2 + L_3)^2}}{2} \quad (4.25)$$

The generic formulation for the line switching distance:

$$D_n = \frac{\sqrt{4W^2 + (L_{(n-1)} + L_n)^2}}{2} \quad (4.26)$$

Total line switching distance of the semi-circle in a single channel:

$$D_{total} = \sum_{n=2}^n \frac{\sqrt{4W^2 + (L_{(n-1)} + L_n)^2}}{2} \quad (4.27)$$

Equation 4.29 give the line switching time of chuck table for a wafer in a single channel.

$$T_3 = 2 \left(\frac{\sum_{n=2}^n \frac{\sqrt{4W^2 + (L_{(n-1)} + L_n)^2}}{2}}{C_s} \right) \quad (4.28)$$

$$T_3 = \left(\frac{\sum_{n=2}^n \sqrt{4W^2 + (L_{(n-1)} + L_n)^2}}{C_s} \right) \quad (4.29)$$

where W represents the width of the chip along with the dicing street width, L is a cut length, n represents the position of the cut line from the center, and C_s represents speed of the chuck table along X-axis.

4.6.4 Channel Switching Time (T_4)

The chuck table of the dicing saw rotates in order to transition between different cutting channels, depending on the geometry of the chips to be diced. The dicing saw consumes very little time (in comparison to T_1 , T_2 , and T_3) when switching channels. The channel switching time may be calculated by dividing the angular distance (A) traveled by the chuck table by its angular speed (S_a), as shown in Equation 4.30.

$$T_4 = \left(\frac{A}{S_a} \right) \quad (4.30)$$

4.6.5 Blade Ascending and Descending Time (T_5)

The dicing blade descends from a certain height to the required depth on the substrate to start cutting, and it ascends to the same height after the cutting is completed. This time consumption during blade ascending and descending movements is too little, but it may become significant during multi-step cutting when it happens several times for each cut line. The time duration of the blade's vertical motions (along Z-axis) may be calculated by dividing the distance it traveled (Z) by its speed (S_z). The Z value for the multi-step dicing would enlarge in each subsequent cutting step due to the corresponding increase in blade penetration depth into the substrate. Equation 4.32 provides the analytical expression for the time T_5 .

$$T_5 = (N * S) * \left(2 * \frac{Z}{S_z} \right) \quad (4.31)$$

$$T_5 = \left(\frac{2 * N * S * Z}{S_z} \right) \quad (4.32)$$

where S represents the number of depth steps in multi-step cutting, and N represents the total number of cutting lines.

4.6.6 Formulation of Total Dicing Saw Processing Time

Equation 4.34 provides the final mathematical formulation for the overall processing time of the mechanical dicing saw.

$$T_{total} = T_1 + T_2 + T_3 + T_4 + T_5 \quad (4.33)$$

$$\begin{aligned} T_{total} = & S * \left(\frac{4 \left(\sum_{n=1}^n \sqrt{R^2 - (n-1)^2 W^2} \right)}{F} \right) + \\ & (S-1) * \left(\frac{4 \left(\sum_{n=1}^n \sqrt{R^2 - (n-1)^2 W^2} \right)}{C_s} \right) + \\ & \left(\frac{\sum_{n=2}^n \sqrt{4W^2 + (L_{(n-1)} + L_n)^2}}{C_s} \right) + \\ & \left(\frac{A}{S_a} \right) + \left(\frac{2 * N * S * Z}{S_z} \right) \end{aligned} \quad (4.34)$$

where S represents the number of depth steps in multi-step cutting, R represents the radius of the wafer, n represents the position of the cut line from the center, W represents the width of the chip (including dicing street width), F represents the feed rate during dicing, C_s represents speed of the chuck table along X-axis, L represents the length of a cutting line, A is the angular distance covered by the chuck table while transitioning from one cutting channel to another, (S_a) represents the angular or rotational speed of the chuck table, N represents the

total number of cutting lines, Z is the vertical distance traveled by the dicing blade before and after completing a cut, and (S_z) is the travelling speed of the dicing blade along the Z -axis.

The DISCO DAD3220 dicing saw machine has a chuck table X-axis speed (C_s) of 500 mm/s, an angular chuck table speed (S_a) of 180 degrees/s, and a dicing blade Z-axis speed (S_z) of 50 mm/s. It is important to note that the speed values may vary depending on the specific version of the tool.

4.6.7 Experimental and Theoretical Time Comparison

A MATLAB code was developed using Equation 4.34 to simulate the time for the one-step cutting process of a 4-inch wafer containing a 4 by 4 array of pseudo-MEMS device chips (16.75 mm $\times$ 16.75 mm). The theoretical processing time for the dicing saw was determined using MATLAB, while the experimental time was measured using a stopwatch. Figure 4.23 shows that the experimental and theoretical values were almost identical, validating the formulated mathematical expression for the dicing saw processing time. The time required for auto-alignment is influenced by the tool focus configurations, as well as the size of the wafer and chip. However, it was not considered for this comparison of cutting time.

Small samples (3 mm $\times$ 3 mm) were also diced in multiple depth steps to ensure the formulation created for the dicing saw processing time was accurate. Figure 4.24 displays that the experimental cutting time exceeds the theoretical time by 15 to 20 seconds. One possible explanation might be the difference between the actual and input speeds of the dicing blade and chuck table. This variation could become more noticeable when cutting small samples with many depth increments. Speed calibration of the dicing saw's blade and chuck table can fix this time error. Human error is another possible factor since the stopwatch was manually started and stopped while recording the experimental time.

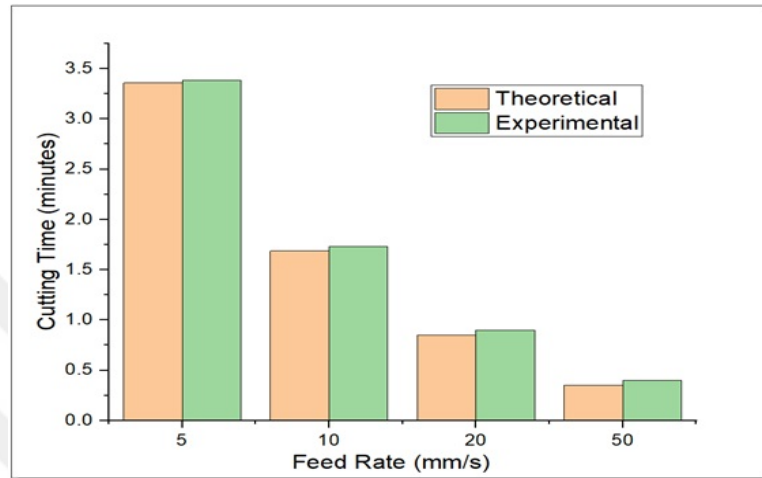


Figure 4.23: Comparison between the experimental and theoretical dicing saw processing times for a single-step cutting with 16.75×16.75 mm pseudo-MEMS devices of a 4-inch diameter wafer.

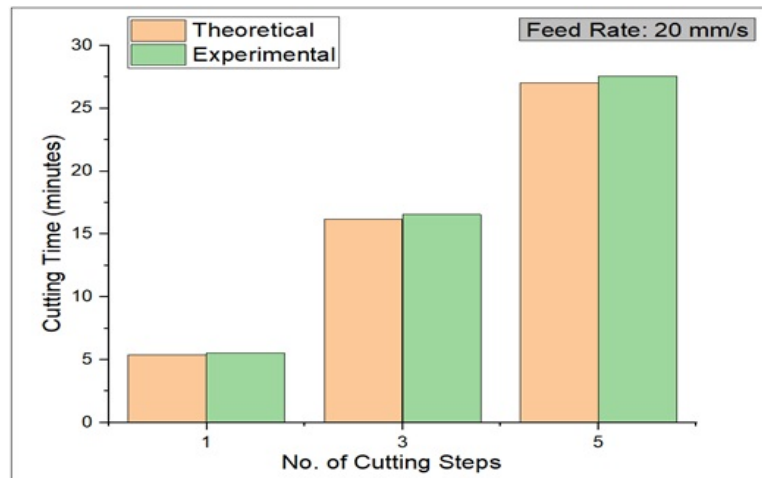


Figure 4.24: Comparison between the experimental and theoretical dicing saw processing times for a multi-step cutting of with 3×3 mm chips of a 4-inch diameter wafer.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

Wafer-scale and batch-compatible microfabrication of 7 pairs of wafers (out of 8 pairs of wafers) and chip-scale characterization of 2 CMUT array chips were completed in this study. The wafer-scale microfabrication was done at the cleanroom facilities of UNAM at Bilkent University, except the anodic wafer bonding process. A former M.S. degree graduate student (Dogu Kaan Bugra Ozyigit) from our research group completed the first phase of the manufacturing processes, including the processes related to the bottom electrode formation, bottom electrode isolation on Pyrex substrates, and the anodic wafer bonding between SOI wafers and Pyrex wafers. The research studies done during the timeline of this M.S. thesis covers processes related to fabricating the top electrode, chip singulation, and the characterization of the manufactured CMUT array devices at individual cell level.

The top electrode was fabricated in a series of processes, including metal deposition, photolithography, and wet and dry etching. Following anodic wafer bonding of Pyrex-SOI wafers, the 350-micron thick handle layer of the SOI wafer was removed using an isotropic RIE process. The wet-etching approach was used

to etch the 1-micron thick layer of silicon-buried oxide that was sandwiched between the device layer and the handle layer of the SOI wafer. In order to enhance the electrical conductivity of the device layer silicon, a 50 nm layer of gold was deposited on the silicon device layer using the physical vapor deposition (PVD) method. Subsequently, gold pads with a thickness of 500 nm were deposited using the stencil shadow mask (Mask 3) as an alternative to photolithography to decrease the process time, process challenges, and process costs. The gold pads were utilized to make the electrical connections between the top electrode (Si-device layer) and the printed circuit board (PCB) via wire bonding for system integration. The last photoresist mask, namely Mask 4, was created on the wafer using the photolithography process to pattern the silicon device layer. In order to reach the device layer silicon, the metal layers (Cr-Au-Cr) that had been blanket-deposited were wet-etched using the photoresist mask. Next, the silicon device layer with a thickness of approximately 12 microns was patterned with the same photoresist mask in anisotropic etching process.

The chips were singulated from the Pyrex substrate using the dicing saw processing optimized for minimized chipping at the front and back sides of the chips. Overall, 112 CMUT chips were obtained from 7 pairs of SOI-Pyrex wafers, with 16 chips per wafer. The chips underwent oxygen plasma etching to remove the photoresist mask and any residues from the dicing tape. Prior to characterization, the gaps of the CMUT devices were vacuumed and sealed with a conformal coating of about 2 microns thick Parylene C. Here it is important to emphasize that vacuum sealing with Parylene C is not a permanent vacuum seal due to the gas permeability properties of Parylene C. In the future, better sealing alternatives for permanent sealing of the CMUT gaps must be considered. Although the Parylene C is not a permanent vacuum sealing process, using Parylene C was very important for the demonstration of vacuum sealing of the CMUT gaps for characterization and demonstration purposes.

The capacitive gap between the upper and lower electrodes of CMUT cells were examined using an optical microscope, scanning electron microscope (SEM), and focused ion beam (FIB) equipment. The FIB-measured gap height was 139 nm, close to the given design value of 150 nm. The individual CMUT cells showed

a resonance frequency in the 5.7 – 5.8 MHz range, measured by an impedance analyzer. This resonance frequency value is comparable with the one calculated by finite element analysis (FEA) simulations that are done by another graduate student in our research group (Ahmad Elshenety). The yield of the operational CMUTs per chip was determined to be between approximately 47 and 58% when a direct current (DC) voltage of 25 volts was applied with 1 volts AC.

Lastly, an alignment teaching-assisted, fully automated dicing saw processing was developed for future studies related to MEMS chips singulation. The most appropriate macro and micro alignment target features were identified, followed by the optimized alignment teaching operation.

5.2 Future Work

Resonance frequency measurements will be conducted on the remaining CMUT sensor chips from the Bond-7 and Bond-8 wafers. Device failure prior to the dielectric breakdown voltage will also be investigated.

Photoacoustic imaging of phantom tissues will be carried out after a suitable CMUT sensor chip is integrated into a handheld probe device.

Future CMUT devices could be made more reliable with efficient electrical connections (shorter wire lengths) and smaller metallization area (on membrane) on the chip and increased dielectric strength. In addition, reducing the CMUT chip dimensions with an optimized singulation process may result in miniaturization and lower fabrication costs per chip.

Bibliography

- [1] Y. Huang, A. S. S. Vasan, R. Doraiswami, M. Osterman, and M. Pecht, “MEMS reliability review,” *IEEE Transactions on Device and Materials Reliability*, vol. 12, no. 2, pp. 482–493, 2012.
- [2] V. Oliveira, R. Ibrahim, E. Barros, L. Mendonça, B. Lima, H. Piazzeta, and A. Gobbi, “MEMS-based ultrasound transducer: CMUT modeling and fabrication process,” *ECS Transactions*, vol. 49, no. 1, p. 431, 2012.
- [3] A. S. Ergun, X. Zhuang, Y. Huang, O. Oralkan, G. G. Yaralioglu, and B. T. Khuri-Yakub, “Capacitive micromachined ultrasonic transducer technology for medical ultrasound imaging,” in *Medical Imaging 2005: Ultrasonic Imaging and Signal Processing*, vol. 5750, pp. 58–68, SPIE, 2005.
- [4] B. T. Khuri-Yakub and Ö. Oralkan, “Capacitive micromachined ultrasonic transducers for medical imaging and therapy,” *Journal of micromechanics and microengineering*, vol. 21, no. 5, p. 054004, 2011.
- [5] M. B. Thacker and D. A. Buchanan, “Design and characterization of low frequency capacitive micromachined ultrasonic transducer (CMUT),” in *2020 IEEE International Conference on Systems, Man, and Cybernetics (SMC)*, pp. 2876–2881, IEEE, 2020.
- [6] J. Bartlett, *Electronics for Beginners*. Apress Springer, Page 446, 2020.
- [7] J. Hernandez, T. Zure, and S. Chowdhury, “Capacitance measurements of an SOI based CMUT,” in *2013 IEEE 4th Latin American Symposium on Circuits and Systems (LASCAS)*, pp. 1–4, IEEE, 2013.

- [8] M. Rafiq and C. Wykes, “The performance of capacitive ultrasonic transducers using v-grooved backplates,” *Measurement Science and Technology*, vol. 2, no. 2, p. 168, 1991.
- [9] A. Erguri, Y. Huang, X. Zhuang, O. Oralkan, G. G. Yarahoglu, and B. T. Khuri-Yakub, “Capacitive micromachined ultrasonic transducers: Fabrication technology,” *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 52, no. 12, pp. 2242–2258, 2005.
- [10] M. I. Haller and B. T. Khuri-Yakub, “A surface micromachined electrostatic ultrasonic air transducer,” *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 43, no. 1, pp. 1–6, 1996.
- [11] Z. Wang, C. He, W. Zhang, Y. Li, P. Gao, Y. Meng, G. Zhang, Y. Yang, R. Wang, J. Cui, *et al.*, “Fabrication of 2-d capacitive micromachined ultrasonic transducer (CMUT) array through silicon wafer bonding,” *Micromachines*, vol. 13, no. 1, p. 99, 2022.
- [12] O. Oralkan, S. T. Hansen, B. Bayram, G. G. Yaralioglu, A. S. Ergun, and B. T. Khuri-Yakub, “High-frequency CMUT arrays for high-resolution medical imaging,” in *IEEE Ultrasonics Symposium, 2004*, vol. 1, pp. 399–402, IEEE, 2004.
- [13] B. Ma, C. Chang, H. K. Oğuz, K. Firouzi, B. T. Khuri-Yakub, and E. L. G. Lab, “Multi-parameter optimization of vented CMUTs for airborne applications,” in *2017 IEEE International Ultrasonics Symposium (IUS)*, pp. 1–4, IEEE, 2017.
- [14] K. Howard, L. Ramirez, B. H. You, and I.-H. Song, “Design analysis of capacitive micromachined ultrasonic transducers,” in *2022 IEEE 17th International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*, pp. 296–300, IEEE, 2022.
- [15] T.-I. Chiu, S.-B. Luo, and T.-C. Hsiao, “Electromechanical modeling and characterization of the electrical breakdown for the capacitive microarrayed ultrasonic transducers,” in *SENSORS, 2010 IEEE*, pp. 188–192, IEEE, 2010.

- [16] J. W. McPherson, J. Kim, A. Shanware, H. Mogul, and J. Rodriguez, “Trends in the ultimate breakdown strength of high dielectric-constant materials,” *IEEE transactions on electron devices*, vol. 50, no. 8, pp. 1771–1778, 2003.
- [17] J. Joseph, B. Ma, and B. Khuri-Yakub, “Applications of capacitive micro-machined ultrasonic transducers: A comprehensive review,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 69, no. 2, pp. 456–467, 2021.
- [18] O. Oralkan, B. Bayram, G. G. Yaralioglu, A. S. Ergun, M. Kupnik, D. T. Yeh, I. O. Wygant, and B. T. Khuri-Yakub, “Experimental characterization of collapse-mode CMUT operation,” *ieee transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 53, no. 8, pp. 1513–1523, 2006.
- [19] R. Manwar, M. Zafar, and Q. Xu, “Signal and image processing in biomedical photoacoustic imaging: a review,” *Optics*, vol. 2, no. 1, pp. 1–24, 2020.
- [20] C. D. Herickhoff and R. van Schaijk, “CMUT technology developments,” *Zeitschrift für Medizinische Physik*, vol. 33, no. 3, pp. 256–266, 2023.
- [21] G. G. Yaralioglu, A. S. Ergun, B. Bayram, T. Marentis, and B. Khuri-Yakub, “Residual stress and young’s modulus measurement of capacitive micromachined ultrasonic transducer membranes,” in *2001 IEEE Ultrasonics Symposium. Proceedings. An International Symposium (Cat. No. 01CH37263)*, vol. 2, pp. 953–956, IEEE, 2001.
- [22] H. Martinussen, A. Aksnes, and H. E. Engan, “Investigation of charge diffusion in CMUTs using optical interferometry,” in *2008 IEEE Ultrasonics Symposium*, pp. 1218–1221, IEEE, 2008.
- [23] R. Manwar, K. Kratkiewicz, and K. Avanaki, “Overview of ultrasound detection technologies for photoacoustic imaging,” *Micromachines*, vol. 11, no. 7, p. 692, 2020.
- [24] J. Wang, Y. Yu, S. H. Pun, Y. Gao, U. K. Che, and P. U. Mak, “An accurate design to calculate and measure the capacitance of CMUT for pressure

- sensors,” in *2016 IEEE International Conference on Consumer Electronics-China (ICCE-China)*, pp. 1–4, IEEE, 2016.
- [25] R. Manwar, T. Simpson, A. Bakhtazad, and S. Chowdhury, “Fabrication and characterization of a high frequency and high coupling coefficient CMUT array,” *Microsystem Technologies*, vol. 23, pp. 4965–4977, 2017.
- [26] P. Shanmugam, L. Iglesias, J. Michaud, D. Alquier, L. Colin, I. Dufour, and D. Certon, “Broad bandwidth air-coupled micromachined ultrasonic transducers for gas sensing,” *Ultrasonics*, vol. 114, p. 106410, 2021.
- [27] M. Khan and T. M. Khan, “Tunable q matching networks for capacitive ultrasound transmitters,” *Analog Integrated Circuits and Signal Processing*, vol. 111, no. 3, pp. 301–312, 2022.
- [28] C. Chang, A. Moini, A. Nikoozadeh, A. F. Sarioglu, N. Apte, X. Zhuang, and B. T. Khuri-Yakub, “Singulation for imaging ring arrays of capacitive micromachined ultrasonic transducers,” *Journal of Micromechanics and Microengineering*, vol. 24, no. 10, p. 107002, 2014.
- [29] M. Tilli, M. Paulasto-Kröckel, M. Petzold, H. Theuss, T. Motooka, and V. Lindroos, *Handbook of silicon based MEMS materials and technologies*. Elsevier, 2020.
- [30] Y. Awatani, Y. Matsumoto, and K. Kato, “Damage free dicing method for MEMS devices,” in *IEEE/LEOS International Conference on Optical MEMS*, pp. 137–138, IEEE, 2002.
- [31] D. K. B. Özyiğit, “Batch-compatible micromanufacturing of a CMUT array for optoacoustic imaging of tissue-like phantoms,” Master Thesis, Bilkent University Turkey, 2021.
- [32] M. H. Öztürk, “Integration of chips by flip-chip bonding techniques,” Master Thesis, Bilkent University Turkey, 2023.
- [33] B. Moğulkoç, H. V. Jansen, J. W. Berenschot, H. J. ter Brake, K. Knowles, and M. C. Elwenspoek, “Characterization of MEMS-on-tube assembly: re-flow bonding of borosilicate glass (duran®) tubes to silicon substrates,”

Journal of micromechanics and microengineering, vol. 19, no. 8, p. 085027, 2009.

- [34] L. Que, C. G. Wilson, and Y. B. Gianchandani, “Microfluidic electrodischarge devices with integrated dispersion optics for spectral analysis of water impurities,” *Journal of microelectromechanical systems*, vol. 14, no. 2, pp. 185–191, 2005.
- [35] V. Kaajakari, “Practical MEMS,” *Small Gear Publishing*, pp. 126–127, 2009.
- [36] K. R. Williams, K. Gupta, and M. Wasilik, “Etch rates for micromachining processing-part ii,” *Journal of microelectromechanical systems*, vol. 12, no. 6, pp. 761–778, 2003.
- [37] C. Bishop, “19—atomic layer deposition,” *Vacuum Deposition onto Webs, Films and Foils (Second Edition)*; Bishop, CA, Ed, pp. 331–336, 2011.
- [38] E. Tatar, M. Torunbalci, S. Alper, and T. Akin, “A method and electrical model for the anodic bonding of soi and glass wafers,” in *2012 IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 68–71, IEEE, 2012.
- [39] A. B. Kaul, *Microelectronics to Nanoelectronics: Materials, Devices & Manufacturability*. CRC Press, Pages 129-130, 2013.
- [40] N. Burham, G. Sugandi, M. M. Nor, and B. Y. Majlis, “Effect of temperature on the etching rate of nitride and oxide layer using buffered oxide etch,” in *2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES)*, pp. 516–519, IEEE, 2016.
- [41] W. Kern, “Cleaning solution based on hydrogen peroxide for use in silicon semiconductor technology,” *RCA review*, vol. 31, no. 2, pp. 187–206, 1970.
- [42] C. Bohling and W. Sigmund, “Self-limitation of native oxides explained,” *Silicon*, vol. 8, pp. 339–343, 2016.
- [43] J. Jaworski, M. Marszalek, J. Prokop, Z. Stachura, O. Boelling, and B. Sulkio-Cleff, “Performance of the evaporation system for thin film deposition in ultrahigh vacuum,” tech. rep., 2000.

- [44] M. Campione, M. Cartotti, E. Pinotti, A. Sassella, and A. Borghesi, “Thickness measurements by quartz microbalance during thin-film growth by organic-molecular-beam deposition,” *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 22, no. 3, pp. 482–486, 2004.
- [45] P. Walker and W. H. Tarn, *CRC handbook of metal etchants*. CRC press, Page 278, 1990.
- [46] F. Laermer and A. Urban, “MEMS at bosch—si plasma etch success story, history, applications, and products,” *Plasma Processes and Polymers*, vol. 16, no. 9, p. 1800207, 2019.
- [47] K. W. Shi, K. Yow, and R. Khoo, “Investigations of the effects of blade type, dicing tape, blade preparation and process parameters on 55nm node low-k wafer,” in *2010 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT)*, pp. 1–6, IEEE, 2010.
- [48] L. Wen, K. Wouters, F. Ceyssens, A. Witvrouw, and R. Puer, “A parylene temporary packaging technique for MEMS wafer handling,” *Sensors and Actuators A: Physical*, vol. 186, pp. 289–297, 2012.
- [49] J. L. Sanders, X. Wu, O. J. Adelegan, M. M. Mahmud, F. Y. Yamaner, C. M. Gallippi, and Ö. Oralkan, “A row-column (rc) addressed 2d capacitive micromachined ultrasonic transducer (CMUT) array on a glass substrate: Preliminary results,” in *2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pp. 1–4, IEEE, 2018.
- [50] DISCO Corporation Japan, *Alignment Tips and Tricks*, 2016-3.
- [51] R. Creese and M. Adithan, *Estimating and costing for the metal manufacturing industries*. CRC Press, Page-118, 1992.