BUFFER AMPLIFIERS FOR AN ELECTRICALLY SMALL BROADBAND ANTENNA

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By
Burak Şahinbaş
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Buffer amplifiers for an electrically small broadband antenna
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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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Professional direction finding applications cover broad bandwidth of one to two decades and performance of the radiative element is of fundamental importance for such receiver oriented applications. It is important to optimize radiative element, i.e, antenna, for the bandwidth of interest. However, portability and weight concerns for the system limits radiator dimensions and eventually restricts the antenna design. Such antennas with their limitations are referred as electrically small antennas. For the application, utilization of a single electrically small monopole antenna that is capable of recovering the electromagnetic signal within a bandwith more than a decade is considered. Due to electrically small radiator, the antenna has a large reactance and small resistance as its input impedance, making it strictly narrowband. For wideband applications, presence of highly reactive impedance of the antenna implies significant reflection loss.

This work is based on buffering an electrically small monopole receiver antenna that is to be used by a compact direction finding system. In the bandwidth of operation (20MHz–1GHz), the antenna is not suitable for passive matching, therefore a buffer amplifier is considered. Transferring the power directly to the receiver is not possible due to input impedance of the antenna. Alternatively, the approach is to probe the antenna output voltage by the active circuit with a high input impedance. This implies antenna voltage is taken without any reduction, then reference voltage is buffered to the output while providing a constant output impedance. Two types of buffer amplifiers for the monopole are designed, simulated and tested combined with the antenna.

Keywords: Active Impedance Matching, Buffer Amplifier, High Input Impedance Buffer Amplifier, Electrically Small Antenna.

ÖZET

ELEKTRİKSEL UZUNLUĞU KISA ANTEN İÇİN TAMPON AMFİLERİ

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Ağustos, 2015

Profesyonel yön bulma uygulamaları, bir veya iki onluk bant genişliğini kapsar ve anten performansı, bu gibi alıcıya yönelik uygulamalarda temel öneme sahiptir. İlgi odağındaki frekans aralığında, anten unsurunun en uygun seviyeye getirilmesi önemlidir. Bununla birlikte, sistemin taşınılabilirliği ve ağırlığı, anten boyutlarını sınırlandırmaktadır. Beraberinde getirdikleri sınırlandırmalarla birlikte bu tip antenler, elektriksel uzunluğu kısa antenler olarak nitelendirilmektedirler. Bu uygulama için, bir onluktan daha fazla bir bant genişliğinde elektromanyetik sinyalleri alabilen bir kısa tekkutup antenin kullanımı söz konusudur. Antenin elektriksel uzunluğu kısa olduğu için, giriş empedansı küçük bir reel dirence ve yüksek bir sanal dirence sahiptir. Bu durum anteni kesin suretle dar bantlı yapmaktadır. Geniş bantlı uygulamalarda, yüksek sanal dirence sahip anten giriş empedansı, dikkate değer bir yansıma kaybı olacağını belirtmektedir.

Bu çalışma, küçük yer kaplayan bir yön bulma sistemi tarafından kullanılacak olan elektriksel olarak kısa tekkutup alıcı antenin tamponlanmasına dayanmaktadır. Anten empedansı, çalıştırılacağı bant genişliğinde (20MHz–1GHz), pasif olarak eşlenememektedir, dolayısıyla bir tampon amfisi düşünülmüştür. Gücün doğrudan alıcıya aktarılması, anten giriş empedansı nedeniyle olanaklı değildir. Bunun yerine seçilen yöntem, anten çıkış voltajının yüksek giriş empedanslı aktif bir devre ile algılanması ve sabit bir çıkış empedansı ile alıcı tarafına gerekli akım sağlanarak tamponlanmasıdır. Tekkutup anten için iki çeşit tampon amfi tasarlanmış, benzetimi yapılmış ve uygulamalı olarak denenmiştir.

Anahtar sözcükler: Aktif Empedans Eşleme, Tampon Amfi, Yüksek Giriş Empedanslı Tampon Amfi, Elektriksel Mesafesi Kısa Anten.

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Chapter 1

Introduction

Professional direction finding applications cover broad bandwidth of one to two decades and performance of the radiative element is of fundamental importance for such receiver oriented applications. It is important to characterize the radiative element, i.e, antenna, for the bandwidth of interest. However, portability and weight concerns for the system limits radiator dimensions and eventually restricts the length and the number of the antennas that are to be used. As a result, an antenna that is reduced in size while capable of recovering the electromagnetic signal within a bandwidth of more than a decade should be considered for such an application. Within the bandwidth of interest, such antennas are electrically small as they are much smaller than the wavelength of the signals.

Electrically small antennas (ESAs), on the other side, have their fundamental limitations as explained in detail by H.A.Wheeler [1].

1.1 Motivation

For a compact system bounded to the utilization of ESAs, there exists two fundamental problems regarding the signal flow from the antenna to the load. The first issue is that the induced voltage at the antenna would be small as the ESA

would be operated well below its resonant frequency. The second issue is that the antenna is mismatched. Combination of these two problems implies that the signal power cannot be transfered to the load of the antenna efficiently, which in turn causes poor sensitivity yielding that weak signals cannot be traced for direction finding.

The input impedance of the ESA at the feed point consists of a large reactance and a small resistance which can be modeled as shown in Figure 1.1. The large

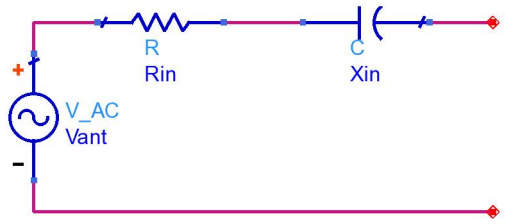


Figure 1.1: Circuit Model of an Electrically Small Monopole Antenna

reactance implies the voltage that is induced on the antenna would lead to a large mismatch when terminated by a typical 50 ohms receiver impedance. Thus the high quality factor implies that if the bandwidth is large, a passive matching cannot be adopted [2, 3]. As a result, a buffer amplifier becomes a candidate solution that utilizes the ESA for large bandwidth.

The maximal possible power transfer implies transferring half of the induced antenna voltage to the load, which is practically not possible. The buffering approach, transferring the induced voltage to the possible extent within the wide bandwidth, will be our preferred method. Necessary current will be provided by the active circuitry, thus with the combination of the current and the voltage, the antenna is capable of delivering the signal power well below the resonant frequency at a sufficiently large magnitude at the expense of increased noise.

1.2 Thesis Contribution

A buffer amplifier has been designed in the range 20–1000MHz for an ES monopole antenna designed and provided by Fraunhofer IIS Erlangen, Germany. Single and double stage amplifiers have been characterized, simulated and implemented. Measurements for these amplifiers have been done. Eventually, the buffered antenna is tested for performance evaluation.

Chapter 2

Background

2.1 Electrically Small Antennas

A modern direction finding application targets proper utilization of spacing of the antenna array within a limited area, for which a wide bandwidth is to be considered as a specification. Due to limited spacing, electrically small antenna (ESA) finds specific interest for the antenna array of a direction finding system, by virtue of their compact physical size. On the other side, ESA has a narrow band.

Definition of ESA was made by Wheeler's work in 1947 which addresses fundamental limitations [1]. It is stated that an antenna whose dimensions are much less than wavelength is an ESA. Mathematically speaking, it is defined that antenna whose physical dimensions can be completely enclosed by a sphere with radius a, for which the following equation holds:

$$2\pi a < \lambda \tag{2.1}$$

where λ is the free space wavelength in meters, is an ESA.

High quality factor of ESA results in a large reactance while radiation resistance is very small. Most of the power is stored in the reactive near field of the antenna

and little is radiated to the far field where imaginary part of the power density vector dominates [4, 5]. An ESA can be modeled as a voltage source that has a highly reactive input impedance with a small resistance as shown in Figure 1.1. ESA is narrowband, due to the presence of gain bandwidth constraint [2, 3].

The bandwidth of the element is inversely proportional with its quality factor (Q), therefore to emphasize why ESA cannot be designed for large bandwidths, it will be adequate to state that there is a theoretical lower bound of Q of an ESA no matter which type of a design is practiced. The theoretical lower bound of the ESA is given by the statement [4, 6, 7]:

$$Q = \frac{1 + 2(ka)^2}{(ka)^3[1 + (ka)^2]} \approx \frac{1}{(ka)^3} \tag{2.2}$$

for $(ka) \ll 1$ where $k = \frac{2\pi}{\lambda}$.

$$\frac{1}{Q} \approx (ka)^3 \tag{2.3}$$

$$BW \propto (\frac{2\pi a}{\lambda})^3 \tag{2.4}$$

2.2 Impedance Matching Problem of ESA

Impedance matching targets maximum power transfer to the load. An ESA is significantly problematic at this point, since its source impedance consists of a large reactive part. Eliminating the reactive part of the ESA impedance would recover most of the power that is available from the source on the load for dissipation. The source resistance is the deterministic element of available power.

Impedance matching concept mostly has to do with eliminating the source reactance. Matching the load resistance to the source resistance would contribute further to the maximal power transfer, however this is not trivial for an ESA for a wideband application, since source resistance is variable with respect to the frequency. This further contribution is valuable since the induced voltage of the ESA is small and the signal power should be delivered to the receiver efficiently.

At this point, there exists proposed solutions in the literature for impedance matching problem of the ESA. The topic could be divided into passive and active applications.

2.2.1 Passive Matching Limitations

Passive matching is based on driving the circuit with reactive components at the resonant frequency, where reactive components cancel each other's impedances, reflecting the intended resistance to the source for maximal power transfer.

Achievable level of impedance matching of a resistance and capacitance connected in series over a specified bandwidth with a passive network is governed by Bode-Fano Equation [3, 8, 9]:

$$\int_0^\infty \frac{1}{w_0^2} \ln \frac{1}{|\Gamma(\omega)|} dw \leq \pi RC \tag{2.5}$$

where ω is the passband, $\Gamma(\omega)$ is the intended reflection coefficient profile. This equation gives us the upper limit of matching. If RC is small, the frequency range where $|\Gamma|$ is less than a certain value is rather small. For example, if $|\Gamma| = 0.3$ within the band of matching and $|\Gamma| = 1$ outside the band, we have

$$\frac{1}{w_0^2} 1.2\Delta w = \pi RC \tag{2.6}$$

or the fractional bandwidth is given by

$$FBW = \frac{\Delta f}{f_o} = \frac{\pi}{1.2} RC f_o \tag{2.7}$$

The fractional bandwidth is proportional to the unitless quantitiy RCf_o. For instance, the ESA that is used in this work has $C = 11.3$pF and $R = 15\Omega$ at $f_0 = 500$MHz. As a result, for the intended reflection coefficient, $FBW = 0.21$ is found, which is insufficient. The problem of ESA is that the resistance would be even less as the frequency decreases and the reflection coefficient cannot be kept small within any large bandwidth, such as 1.7 decades considered in this work. Higher reflection coefficient implies higher reflection losses, thus power cannot be delivered to the load efficiently.

2.2.2 Active Matching Literature

Significant effort on eliminating large reactance of an ESA has been made in the literature. As mentioned previously, passive components could only eliminate the reactive part at a single frequency, as they are bounded to Foster's reactance theorem [10]. Conversely, non-Foster circuits found particular interest for having capability of attaining negative reactance versus frequency slope. This is an equivalent statement for realization of negative capacitance or inductance.

In previous research, realization progress of negative capacitance and inductance has been demonstrated. These devices are called negative impedance converters (NICs) which have been introduced by Linvill [11]. NIC circuits have been further categorized in [12]. Research on using NIC's for matching the ESA has been conducted by Sussman-Fort [7].

2.2.3 Buffering

Apart from using NICs for matching, there exists the concept of buffering the antenna from the receiver with transistor amplifier. An analysis of using such circuits is given in [13], where the bandwidth of operation is limited to FM frequencies. Along with separate applications, there exists combination of non-Foster circuits followed by a buffer stage. It is suggested that the combined topology has a tendency to improve ESA power transfer characteristics, therefore it is referred as enhanced non-Foster matching [14].

2.3 Amplifier Concepts

A buffer amplifier is to be designed within the considered bandwidth of 1.7 decades. The flexibility of the buffer amplifier comes from simple characterization of port impedances. It will constitute buffering to the induced voltage of the antenna and supplementary current will be provided to the receiver, yielding

a better power transfer characteristics. There exist two important concepts for amplifier characterization, which are the power gain and the noise figure.

There are three power gain definitions for amplifiers. The first one is the operational power gain which does not account for power that is available from the source. The second one is the available power gain G_A which accounts for source mismatches only. The third one is the transducer power gain G_T which accounts for source and load mismatches. Therefore among these definitions, G_T is a good measure for our application. It is given by:

$$G = \frac{P_L}{P_{av}} \tag{2.8}$$

where P_L is the power that is actually delivered to load and P_{av} is the power available from the source.

Existence of an antenna implies that external noise is inserted to the receiving system. Additionally, the active part will introduce its own noise which is added on the recovered signal. Being the first stage of the cascade, the noise figure of the system will be dominated by the amplifier, hence the noise figure of the amplifier that is driven by the antenna should be small.

Chapter 3

Buffer Amplifier Design

Design stage of the active element in the antenna system requires proper treatment of operational requirements. The objective of the buffer amplifier is transferring the antenna power to the receiver while having a low noise contribution within 20–1000MHz frequency range providing a uniform source impedance to the receiver.

To be specific, the output of the active part is planned to be nearly equal to 50Ω, as a generic receiver would be optimized for this source impedance. Additionally, the circuit should be stable and has a small noise figure.

3.1 Design Approach and System Definition

Modelling the active part as a two port element whose input and output are characterized by impedances as represented in Figure 3.1, is the first step of system oriented design.

An ESA with a variable, highly reactive input impedance would drive the buffer amplifier. There is a voltage division between the antenna and the load impedances. According to Figure 3.2, the voltage V_L and the average power P_L

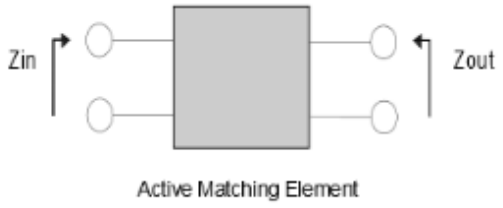


Figure 3.1: Two Port Representation of the Active Matching Circuit

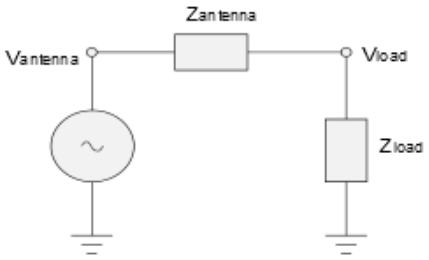


Figure 3.2: Representation of a generic load that is driven by ESA. Induced antenna voltage is represented by $V_{antenna}$.

that is delivered to the load is simply:

$$V_L = \frac{(V_{antenna})(Z_{load})}{(Z_{load} + Z_{antenna})} \tag{3.1}$$

$$P_L = \left[\frac{\mid V_{antenna} \mid^2 R_{load}}{(R_{load} + R_{antenna})^2 + (X_{load} + X_{antenna})^2} \right] \tag{3.2}$$

Equation 3.2 demonstrates that presence of a large reactance would mean power delivered to the load is very small. If there is a conjugate matching, then the power that is delivered to the load would be:

$$P_{av} = \left[\frac{\mid V_{antenna} \mid^2}{4R_{antenna}} \right] \tag{3.3}$$

In order to examine the delivered power for an ESA, the drive point impedance characteristics should be evaluated. For a short antenna having length l, radiation

resistance R_{rad} is proportional to $(l/\lambda)^2$. For the same electric field strength, induced open circuit voltage of the antenna (V_{oc}) is proportional to l. Substitution into Equation 3.3 yields:

$$P_{av} \propto \frac{(l)^2}{(\frac{l}{\lambda})^2} \tag{3.4}$$

It is observed that both nominator and denominator are proportional to l^2 cancelling effect of l from the available power identity, which indicates that receiving the antenna available power is independent from electrical size of the antenna. However, the presence of a dominating reactive part of the antenna impedance which is variable with respect to frequency prevents transferring the available power.

The small antenna reactance is analyzed and a formulation is proposed in [1]. Specifically, disk loaded monopole is investigated with modified formulations in [15]. Accordingly, the capacitance of the small antenna is given by:

$$C = \epsilon_0 \frac{A_e}{h_e} \tag{3.5}$$

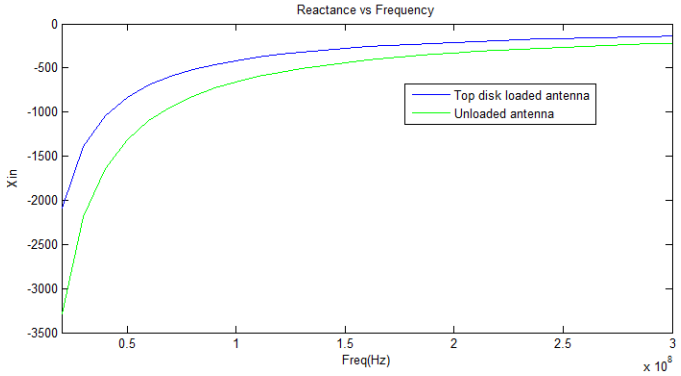
where A_e is top disk that loads the antenna and h_e is the effective monopole height. h_e is defined as the ratio of the moment of vertical charge to total charge over radiator, since the current on the radiator is not uniform as the antenna is operated well below it's resonant point. Thus, h_e will be less than physical length of the radiator. If the top disk is not placed, C is given by:

$$C = 2\pi\epsilon \frac{L}{\ln(L/a) - 1} \tag{3.6}$$

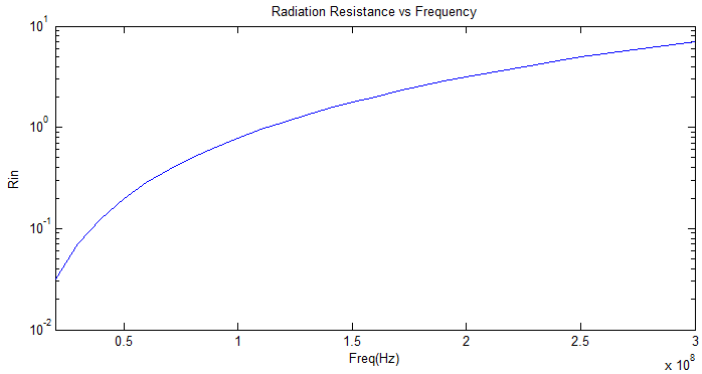
for $\frac{l}{\lambda} < 0.1$. Moreover, the radiation resistance R_{rad} is given by:

$$R_{rad} = 160\pi^2 (\frac{h_e}{\lambda})^2 \tag{3.7}$$

Regarding these formulas, the antenna impedance could be compared for loaded and unloaded cases. ESA that is used here has a radiator having $l = 0.1$m and accordingly, the comparison is valid for $f < 300$MHz as $\frac{l}{\lambda} < 0.1$. The loading capacitor has radius of 3.7cm and the resultant antenna impedance parameters



(a) Calculated reactance of the antenna for top disk loaded and unloaded cases.



(b) Calculated resistance of the antenna having 10cm radiator length.

Figure 3.3: Calculated resistance and reactance of the antenna having 10cm radiator length and 3.7cm top disk included and excluded for reactance.

are demonstrated in Figure 3.3, for which $h_e = 0.1$cm approximately obtained from moment of current simulations demonstrated in next section.

It is observed that loading the antenna decreases reactance significantly by increasing the effective length, however due to small sizes of the antenna, radiation resistance is very small and still suppressed by the reactance. Delivering the available power would therefore be possible either by providing a very good lossless matching, which is possible at a single frequency or within a narrowband, or by terminating the antenna with a very high loading and buffering the voltage using a buffer amplifier within a wide bandwidth.

Simply from Equation 3.1, recovering the voltage from antenna impedance could

be provided by loading the antenna with a magnitude-wise larger impedance, Z_{in}.

Z_{in} being very large indicates that $|\Gamma_{in}|$ should be very close to 1. Γ_{in} would be equal to S_{11} as the active device would be unilateral, so $S_{11} \approx 1$ is expected.

For the output reflection coefficient Γ_{out}, due to unilateral characteristics again, S_{22} would be equal to Γ_{out}. For providing near 50Ω impedance to the receiver, the constraint is $|S_{22}| \leq -10$dB throughout the bandwidth.

Recovering the voltage from the antenna requires a well characterization of S_{21}. Voltage gain would be derived for S_{21} characterization, thus port voltages are:

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \approx S_{11}V_1^+ \tag{3.8}$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \approx S_{21}V_1^+ \tag{3.9}$$

since S_{12} is negligible due to unilateral design and since the output of the active element would be matched, S_{22} would be negligible as well.

Input port voltage is given by $V_1 = V_1^+ + V_1^-$ and since there would be no reflection from 50Ω receiver impedance, output port voltage would be $V_2 = V_2^-$. Using Equations 3.8 and 3.9 in port voltage statements would imply:

$$V_1 = 1 + S_{11}V_1^+ \tag{3.10}$$

$$V_2 = S_{21}V_1^+ \tag{3.11}$$

Hence, voltage gain would be simply stated as:

$$A_v = \frac{S_{21}}{1 + S_{11}} \tag{3.12}$$

The result implies that for eliminating the effect of antenna's variable impedance, $S_{21} = 1 + S_{11}$ would be required for buffering whole antenna induced voltage.

The power transfer characteristics of the amplifier would be evaluated in terms of transducer gain G_T, which is dependent to the source impedance thus it will provide the extent of the delivered power to the receiver when the amplifier is driven by the antenna.

Parameter	Magnitude	Phase
S_{11}	≈ 1	$\approx 0^{\circ}$
S_{12}	≈ 0	-
S_{21}	≥ 1	-
S_{22}	$< -10dB$	-

Table 3.1: S-parameter specifications for the design approach.

The output of the amplifier is designed to be matched and the system is unilateral, thus the identity for the transducer gain is:

$$G_T = \frac{\mid S_{21} \mid^2 (1- \mid \Gamma_s \mid^2)}{\mid 1 - S_{11}\Gamma_s \mid^2} \tag{3.13}$$

where Γ_s is source reflection coefficient. The available power from the antenna is given by:

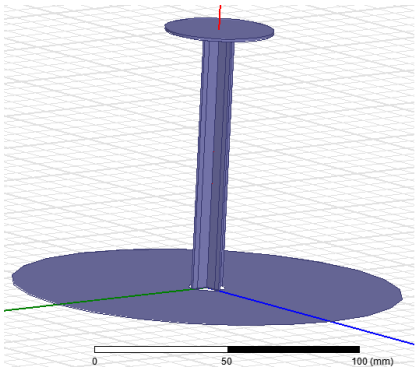
$$P_{av} = \frac{\mid V_{antenna} \mid^2}{8Z_0} \frac{\mid S_{21} \mid^2 \mid 1 - \Gamma_s \mid^2}{(1- \mid \Gamma_s \mid^2)} \tag{3.14}$$

A system definition with respect to S-parameters has been made for the design as shown in Table 3.1. Prior to realization part, antenna that is utilized should be introduced.

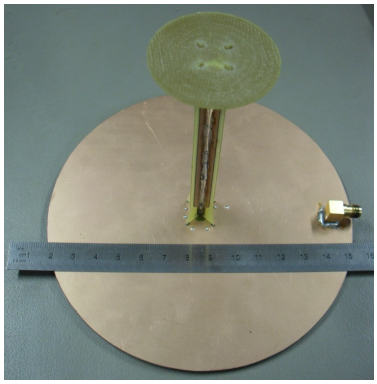
3.2 Analysis of the Antenna

The antenna is designed and implemented by Fraunhofer IIS. It is a monopole with eight symmetric transmission line patches at each side of the crossing FR4 substrates, directing perpendicularly outwards of a large ground plane. The height of the antenna is 10cm and the monopole is terminated with a capacitive hat for increasing current density. All the patches are connected at the driving point located at the center of the ground plane and at the termination hat. HFSS model is demonstrated in Figure 3.4a and a photo of the antenna is shown in 3.4b.

The antenna is a resonant monopole around $\lambda/4$ distance. The radiative surface



(a) HFSS model of the antenna that is considered for the application.



(b) Photo of the fabricated antenna.

length is 10cm. Initially, the top hat is not considered and the antenna geommetry will be explained regarding equivalent circular cylinder monopole model [16].

Circular cylinder monopole is used for a bandwidth extension. For each crossing conductors on the radiator, there exists one equivalent circular cylindric monopole, whose effective radius is $a_e = 0.4w$ where w is the width of radiator conductor slots. As a result, there exists four close cylindrical monopoles. Thus each has width of 4.7mm and in total, an approximation of one large cylindrical monopole whose height is 100mm and $a_e = 2 * 0.4 * 4.7\text{mm}$, leading to an effective radius of $a_e = 3.76\text{mm}$.

There exists empirical formulation of resonant frequencies for cylindrical monopoles in [16]. For this antenna, the resonant points could be calculated using a coefficient, which is given by:

$$F = \frac{\frac{l}{2a_e}}{1 + \frac{l}{2a_e}} s \tag{3.15}$$

In this case, $l = 100\text{mm}$ and $F = 0.93$ is found. Accordingly, the first resonance is expected at

$$\lambda_1 = \frac{100\text{mm}}{0.24F} \tag{3.16}$$

and the secondary is expected at

$$\lambda_2 = \frac{100\text{mm}}{0.72F} \tag{3.17}$$

The approximate resonant points of the antenna is therefore $\lambda_1 = 448$mm and $\lambda_2 = 149$mm thus corresponding $f_1 = 670$MHz and $f_2 = 2.01$GHz. For lower frequencies, this estimation is more accurate since the primary approximation is antenna's being electrically small.

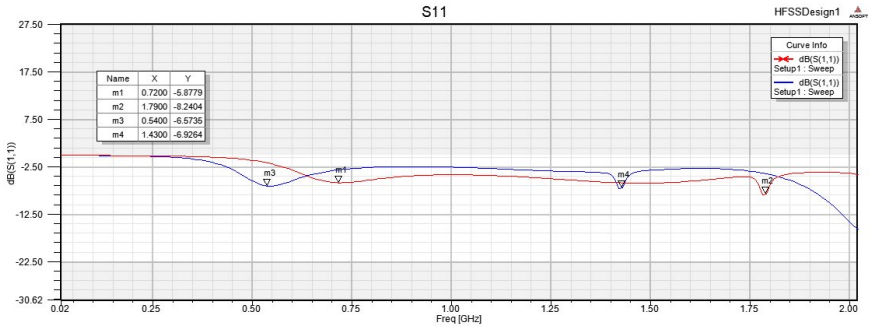
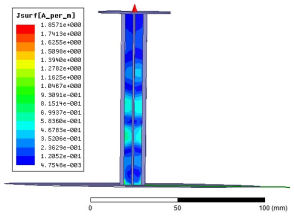
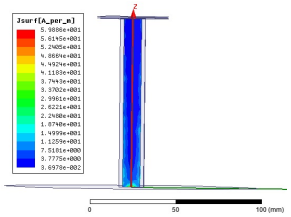


Figure 3.5: Simulated reflection coefficient of the antenna without top hat.

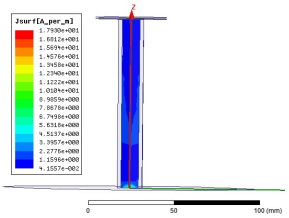
HFSS simulation of antenna reflection coefficient demonstrates this fact. The antenna impedance is demonstrated in Figure 3.5 with and without top loading.



(a) Current density of the radiative element at 20MHz.



(b) Current density of the radiative element at first resonance.



(c) Current density of the radiative element at 1000MHz.

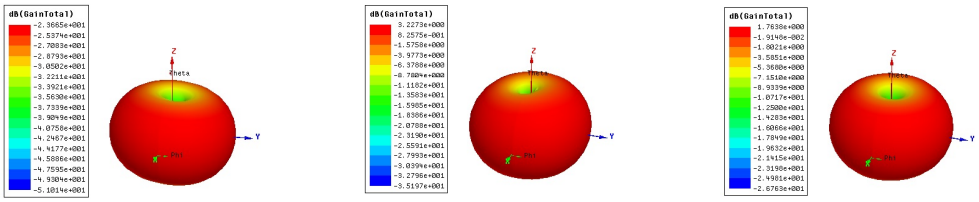
Figure 3.6: Current densities induced on the antenna at beginning and end of the band and at the resonant point of the antenna.

The first resonant frequency is at 720MHz while the second resonance is at 1790MHz. As expected, the approximation is more accurate in the electrically

small portion. From these reflection coefficient values, it is seen that the antenna occupies a large 3dB bandwidth after first resonance, however the level of reflection is larger than -10dB.

Addition of the top hat increases current density of the radiative part and the effective length of the antenna. Therefore, $\lambda/4$ resonance occurs at 540MHz, improving the characteristics of the antenna bandwidth significantly.

Resulting induced current density on the antenna is presented in Figure 3.6. Current density values indicate that at 20MHz the magnitude is small as the antenna is electrically short. At resonance point, the magnitude reaches its maximal value and it is not decreasing significantly till 1GHz.



(a) Gain pattern at 20MHz.

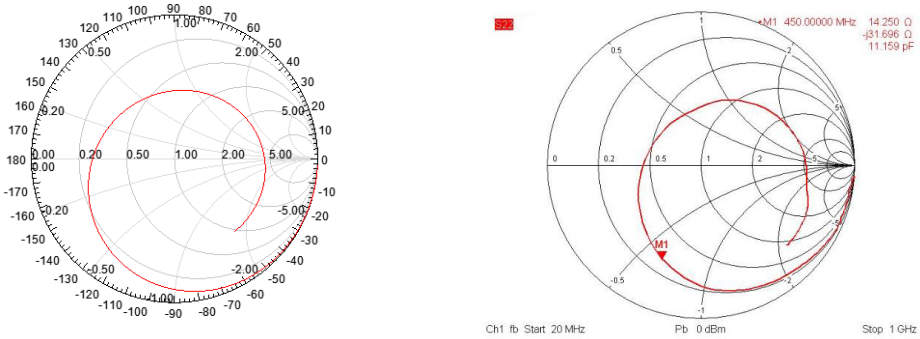
(b) Gain pattern at first resonance.

(c) Gain pattern at 1000MHz.

Figure 3.7: Gain patterns of the antenna at beginning and end of the band and at the resonant point of the antenna.

The radiation pattern of the antenna is another important aspect. It is omnidirectional and the gain patterns at three different frequencies are demonstrated in Figure 3.7. In addition, the drive point impedance of the antenna is going to be demonstrated. This will be used for verification of the simulation of the antenna, as shown in Figure 3.8.

It appears that the simulation and the measurement agrees in a satisfactory manner.



(a) Simulated reflection coefficient of the antenna represented on smith chart between 20MHz-1000MHz.

(b) Measured S_{11} parameter of the electrically short monopole antenna in the range from 20 MHz to 1000 MHz.

Figure 3.8: Comparison of the simulated and the measured S_{11} of the antenna drive point.

3.3 High Input Impedance Buffer Amplifier Design

Realization of the design aspects is a mutual concept of transistor operation principles, therefore an analysis of transistor topologies shall be presented. This section will first introduce topology behavioural regarding the port impedances and the gain, then required stages will be determined. Finally in this section, transistor selection aspects will be mentioned.

3.3.1 Transistor Topology Analysis

The analysis would be divided into three subjects; input impedance, output impedance and gain analysis.

3.3.1.1 Input Impedance Analysis

Primary objective of the design is to achieve a high input impedance which would dominate antenna impedance at any frequency. Considering common emitter initially, it could be stated that r_π approximates the input impedance. Equation of r_π could be given as:

$$r_\pi = \frac{V_{thermal}}{I_{Base}} \tag{3.18}$$

where I_{Base} is the DC base bias current and $V_{thermal}$ is approximately equal to 26mV at room temperature. As a result, r_π is strongly dependent to biasing. For achieving a high input impedance, base current would be very small and impractical, hence common emitter would not yield required high input impedance.

For the case of common collector, input impedance characteristics of the BJT changes. Ignoring parasitic effects, R_{in} can simply be stated as:

$$R_{in} = r_\pi + (\beta + 1)R_{emitter} \tag{3.19}$$

Presence of a high emitter resistance allows intended high input impedance which is multiplied by forward current gain β. On the other side, when the circuit is loaded, emitter node bias resistance is parallelled with R_{load}, hence for achieving high input impedance, the topology should be terminated with a high load.

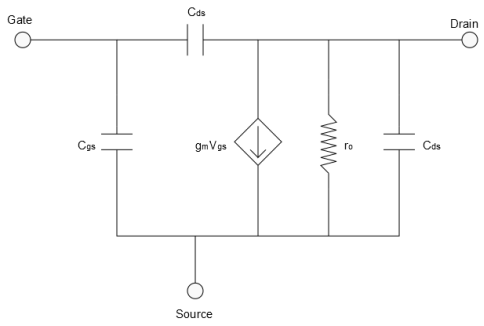


Figure 3.9: High frequency circuit model of FET.

As observed from BJT, physical connections inside the device has a significant degenerative effect on the input impedance performance. For the case of FET, parasitic capacitances inside the transistor are problematic. High frequency FET model including parasitic effects are shown in Figure 3.9.

For simplification, r_0 can be neglected as it is large as well as C_{ds}. Starting the

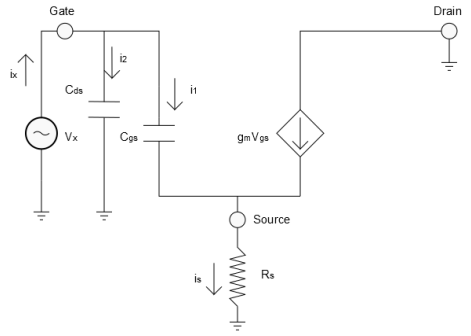


Figure 3.10: Test source connected to FET with source resistance for calculation of the input impedance of the common drain.

analysis from the common drain, the input impedance can be found by connecting a test source V_x to the input of the circuit and similarly investigating $\frac{V_x}{i_x}$, as shown in Figure 3.10. Making use of the phasor notation, KCL and KVL equations could be written as follows:

$$i_x = i_1 + i_2 \tag{3.20}$$

$$i_1 = \frac{V_x - V_s}{Z_{gs}} \tag{3.21}$$

$$i_2 = \frac{V_x}{Z_{ds}} \tag{3.22}$$

where the voltage at source node is given by V_s and impedance of C_{gs} is Z_{gs}. Using Equations 3.21 and 3.22 in Equation 3.20 yields:

$$i_x = V_x \left[\frac{1}{Z_{ds}} + \frac{1}{Z_{gs}} \right] - \frac{V_s}{Z_{gs}} \tag{3.23}$$

The source voltage is given by:

$$V_s = [i_1 + g_m V_{gs}] R_s \tag{3.24}$$

V_{gs} can be expanded as $V_g - V_s$ and $V_g = V_x$, hence:

$$V_s = [i_1 R_s + g_m R_s V_x - g_m R_s V_s] \tag{3.25}$$

Here, substitution of i_1 in Equation 3.21 results in:

$$V_s[1 + g_m R_s] = \left[\frac{V_x - V_s}{Z_{gs}}\right] R_s + g_m R_s V_x \tag{3.26}$$

$$V_s\left[1 + g_m R_s + \frac{R_s}{Z_{gs}}\right] = V_x\left[\frac{R_s}{Z_{gs}} + g_m R_s\right] \tag{3.27}$$

Simple manipulation of Equation 3.23 enables obtaining V_s in terms of i_x as:

$$V_s = V_x\left[\frac{Z_{gs}}{Z_{ds}} + 1\right] - i_x Z_{gs} \tag{3.28}$$

Substitution of Equation 3.28 into Equation 3.27 would give:

$$V_x\left[\left(1 + g_m R_s + \frac{R_s}{Z_{gs}}\right)\left(\frac{Z_{gs}}{Z_{ds}} + 1\right) - \left(\frac{R_s}{Z_{gs}} + g_m R_s\right)\right] = i_x\left[Z_{gs} + g_m R_s Z_{gs} + R_s\right] \tag{3.29}$$

The input resistance of the common drain, Z_{in}, is given by:

$$Z_{in} = \frac{V_x}{i_x} = \frac{\left[Z_{gs} + g_m R_s Z_{gs} + R_s\right]}{\left[1 + \frac{Z_{gs}}{Z_{ds}} + \frac{g_m Z_{gs} R_s}{Z_{ds}} + \frac{R_s}{Z_{ds}}\right]} \tag{3.30}$$

The outcome of the analysis for the common drain is that C_{ds} is critical and should be small in any case in order to provide high input impedance. Additionally, C_{gs} should be small. Good parasitic performance of the transistor boosts the input impedance and the topology becomes suitable for the application.

Similar analysis has been carried out for the common source topology and the input impedance appears as follows:

$$Z_{in} = Z_{gs} // \left[\frac{R_d}{1 + g_m R_d} + \frac{Z_{ds}}{1 + g_m R_d}\right] \tag{3.31}$$

and stating that $Z_{ds} = [jwC_{ds}]^{-1}$, the equation becomes:

$$Z_{in} = Z_{gs}//\left[\frac{R_d}{1+g_mR_d} + \frac{1}{jwC_{ds}(1+g_mR_d)}\right] \tag{3.32}$$

suggesting a modification in C_{ds} in a way that equivalently, $C_m = C_{ds}(1+g_mR_d)$ is reflected to the input. C_m is called Miller capacitance.

The analysis demonstrated that C_{gs} and C_m are the critical elements, thus presence of Miller effect will decrease the input impedance of the topology making it inappropriate for buffering applications. Therefore, common source is not a candidate at the buffering stage.

The result of the discussion for high input impedance favors utilization of common drain topology.

3.3.1.2 Output Impedance Analysis

The output of the active circuit is intended to provide near 50Ω impedance to the receiver which would yield an output reflection coefficient less than −10dB.

Initially, the output impedance of the common source and the common drain will be investigated regarding the high frequency FET model, then the analysis will be evaluated for the common emitter and the common collector. The test circuit for the common source output impedance is shown in Figure 3.11. Starting from the set of equations for current and voltage at the particular nodes:

$$i_1 = \frac{V_x}{r_0//R_d} \tag{3.33}$$

Noting that V_{gs} is equal to V_g:

$$i_2 = i_x - i_1 - g_mV_g \tag{3.34}$$

$$i_2 = \frac{V_x - V_g}{Z_{gs}} \tag{3.35}$$

Thus Equation 3.33 and 3.35 can be substituted into 3.34 as follows:

$$\frac{V_x - V_g}{Z_{gs}} = i_x - \frac{V_x}{(r_0//R_d)} - g_mV_g \tag{3.36}$$

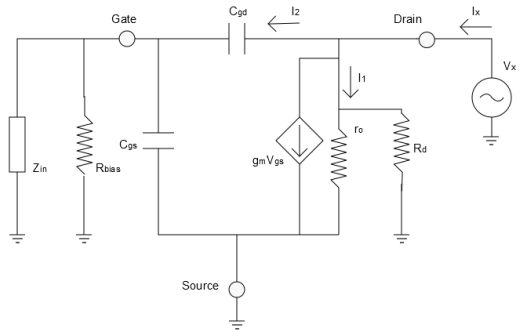


Figure 3.11: Common source topology output impedance analysis test circuit.

At this point, the only remaining part is to derive V_g:

$$V_g = V_x \left[\frac{(Z_{in}//R_{bias}//Z_{gs})}{Z_{gd} + (Z_{in}//R_{bias}//Z_{gs})} \right] \tag{3.37}$$

Substitution of Equation 3.37 into Equation 3.36 and organizing the result leads:

$$i_x = V_x \left[\frac{1}{Z_{gs}} + \frac{1}{(r_0//R_d)} + \left(g_m - \frac{1}{Z_{gs}} \right) \left(\frac{(Z_{in}//R_{bias}//Z_{gs})}{Z_{gd} + (Z_{in}//R_{bias}//Z_{gs})} \right) \right] \tag{3.38}$$

Hence, the output impedance of the common source topology that is given by V_x/i_x is found as:

$$Z_{out} = \left[\frac{1}{Z_{gs}} + \frac{1}{(r_0//R_d)} + \left(g_m - \frac{1}{Z_{gs}} \right) \left(\frac{(Z_{in}//R_{bias}//Z_{gs})}{Z_{gd} + (Z_{in}//R_{bias}//Z_{gs})} \right) \right]^{-1} \tag{3.39}$$

Here, Z_{gd} and Z_{gs} would eliminate the first and the third terms, as they are large. If the transistor provides good output isolation, i.e, S_{12} is small, the Equation 3.39 becomes:

$$Z_{out} \approx \left[\frac{1}{(r_0//R_d)} \right]^{-1} \tag{3.40}$$

Accurate characterization of the output impedance is possible by selecting R_d accordingly.

For the case of BJT, Z_{gs} becomes Z_{be} and R_d becomes R_c. Corresponding approximation then becomes:

$$Z_{out} \approx \left[\frac{1}{Z_{be}} + \frac{1}{(r_0//R_c)} \right]^{-1} \tag{3.41}$$

Thus, the common emitter output impedance is dependent to r_π significantly, which is unintended since it could change with respect to thermal effects.

In this subsection, the common drain and the common collector topologies are evaluated. Similar analysis is conducted and the resulting common drain output impedance is as follows:

$$Z_{out} = \left[\frac{1}{Z_{gs}} + \frac{1}{r_0} + \frac{1}{R_s} + g_m + \left(g_m - \frac{1}{Z_{gs}}\right)\left(\frac{(Z_{in}//R_{bias}//Z_{ds})}{Z_{gs} + (Z_{in}//R_{bias}//Z_{ds})}\right)\right]^{-1} \tag{3.42}$$

The equation can be accurately approximated by neglecting the first and the last terms which are small. Hence:

$$Z_{out} \approx \left[r_0//R_s//\frac{1}{g_m}\right] \tag{3.43}$$

It appears that g_m is the deterministic element for the output impedance thus it should be chosen accordingly. For BJT, the approximation becomes the following:

$$Z_{out} \approx \left[r_\pi//r_0//R_e//\frac{r_\pi}{\beta}\right] \tag{3.44}$$

As a result, BJT output impedance is dominated by r_π/β since it is the smallest term.

3.3.1.3 Gain Analysis

The voltage gain of the active element is important for transferring the antenna voltage to the receiver. For common source, there is a significant voltage gain given by the following equation:

$$A_v = \left[\frac{\frac{R_d}{Z_{gs}} - g_m R_d}{1 + \frac{R_d}{Z_{gd}}}\right] \tag{3.45}$$

The gain is arranged by the drain resistance while the Miller capacitance has a negligible effect. For BJT equivalent, the equation is identical when Z_{gs} becomes Z_μ.

For the common drain, the voltage gain appears as:

$$A_v = \frac{\left[\frac{R_s}{Z_{gs}} + g_m R_s\right]}{\left[1 + \frac{R_s}{Z_{gs}} + g_m R_s\right]} \tag{3.46}$$

where the terms including Z_{gs} in the denominator are negligible as it is much larger than R_s. Hence, the voltage gain of the common source is approximately:

$$A_v \approx \frac{g_m R_s}{1 + g_m R_s} \tag{3.47}$$

This identity is valid for the BJT as well. In order to provide the voltage buffer to the maximal extent, $g_m R_s$ should be kept large.

3.3.2 Required Amplifier Stages

Discussions above are summarized briefly in Table 3.2 for determining required stages. Immediately, it could be deduced that the first stage should be common drain, as it yields the highest input impedance among others.

In this case, it appears that g_m is dominating both the output impedance and the gain. Increasing it is preferred for higher voltage gain while output impedance limits parameter g_m to be at most 25mS for matching. Considering $g_m = 25$mS, Equation 3.47 states a voltage gain of 0.52, which is small as there would be an additional voltage drop between the antenna and the input of the amplifier.

To overcome this limitation and having a better gain, two alternatives appear. The first one is a single stage amplifier which has a moderate g_m while keeping the voltage gain at a good level besides having a smaller output impedance than 50Ω. A block diagram is presented in Figure 3.12.

The second alternative is to place an additional amplifier stage, which would provide a high loading to the first stage, hence the voltage gain governed by the Equation 3.47 is increased. In the second stage, the voltage is further amplified

Topology	Constraint	
Common Source	Input Impedance	Parasitic capacitance dependent only. Cannot be further increased.
	Output Matching	Enables matching without external resistances. Dependent on drain resistance.
	Voltage Gain	Larger than unity. Dependent on drain resistance and g_m.
Common Emitter	Input Impedance	Due to presence of r_π, it is not possible to achieve sufficient high values.
	Output Matching	Dependent on r_π and collector resistance.
	Voltage Gain	Larger than unity. Collector resistance and g_m dependent.
Common Drain	Input Impedance	Parasitic capacitance dependent. Could be boosted by increasing effective source resistance.
	Output Matching	Primarily dependent on g_m. Additional series resistance could be used.
	Voltage Gain	Less than one. Effective source resistance and g_m dependent.
Common Collector	Input Impedance	Could be boosted by emitter resistance, however r_π decreases isolation leading poor performance compared to common drain FET.
	Output Matching	Dependent on r_π.
	Voltage Gain	Less than one. Effective source resistance and g_m dependent.

Table 3.2: Summary of the transistor topology behavioural. Effective resistance implies AC resistance.

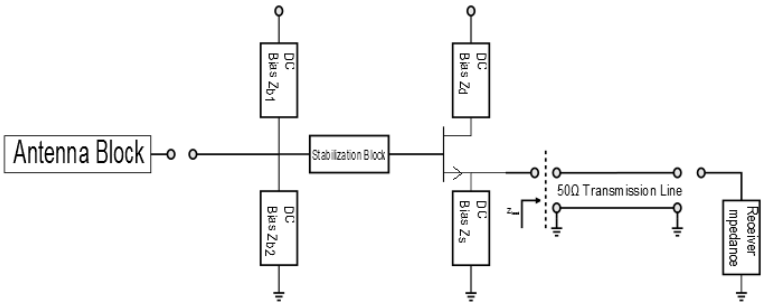


Figure 3.12: Single stage amplifier block diagram.

with a common source and it is to be delivered to the receiver with a near 50Ω output impedance. A block diagram is demonstrated in Figure 3.13.

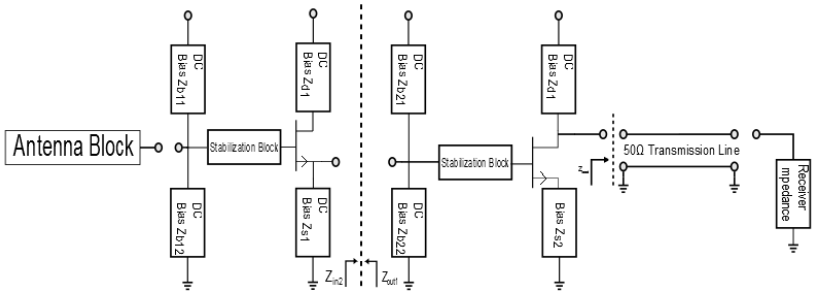


Figure 3.13: Double stage amplifier block diagram.

For the second stage, using FET is preferable for the noise performance. Due to the presence of the gain, it is a promising approach while it costs more circuit space and DC power consumption compared to single stage.

3.3.3 Transistor Selection

For practical purposes, the noise figure of the active device is important. Currently, the industry presents alternatives of ultra low noise FETs. As a result, devices such as H-JFETs (Hetero-Junction Field Effect Transistor) and HEMTs (High Electron Mobility Transistor) are suitable for this application. It is also important that the sensitivity of the noise figure, R_n, of the device with respect to changes in its source impedance should be small.

Another consideration is that the parasitic capacitances should be very small. In that sense, as the designed operational frequency of the transistor increases, the parasitic capacitance values decreases. On the contrary, the noise parameters are usually optimized in the specified frequency of the transistor. Choosing a transistor for which the designed operational frequencies are close to the application's frequency range is appropriate.

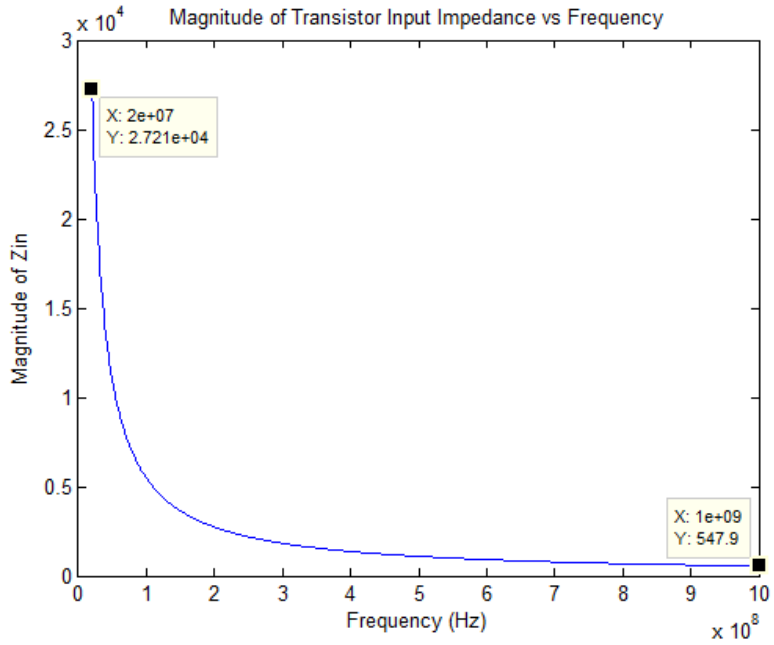


Figure 3.14: Calculated input impedance of ATF35143 within 20MHz-1000MHz.

Considering these facts, it is decided that Avago Technologies ATF-35143 pseudomorphic HEMT is a good choice for generic design requirements for both stages. It has a moderate g_m value of 100mS while $C_{gs} = 0.4$pF and $C_{gd} = 0.23$pF for the device. Additionally, R_n is small. The relevant portion of the datasheet is provided in the Appendix.

The input impedance of the transistor is calculated as in Figure 3.14 by using the Equation 3.30. It is especially superior to antenna impedance in the location of band where the antenna impedance has very large reactance. In the overall sense, the device appears to be suitable for the application.

3.4 Deployment and Simulations

Simulations have been made on Agilent ADS for comparison purposes with the measurements. Accordingly, the amplifier is simulated in a 50Ω source and load impedance framework for verification purposes with the measurements done by devices having 50Ω terminations. Later in the next chapter, antenna impedance is used as source impedance of the amplifier for calculation of the overall antenna performance.

3.4.1 Single Stage Amplifier

Single stage amplifier occupying ATF35143 transistor is initially biased. For

freq	DC.Vs	DC.Vd	DC.Vg	DC.I_drain.i
0.0000 Hz	2.379 V	4.312 V	1.731 V	10.12 mA

keeping the noise small, drain bias current (I_D) is selected as 10mA with drain to source voltage (V_{gs}) of 2V with respect to noise parameters of the transistor.

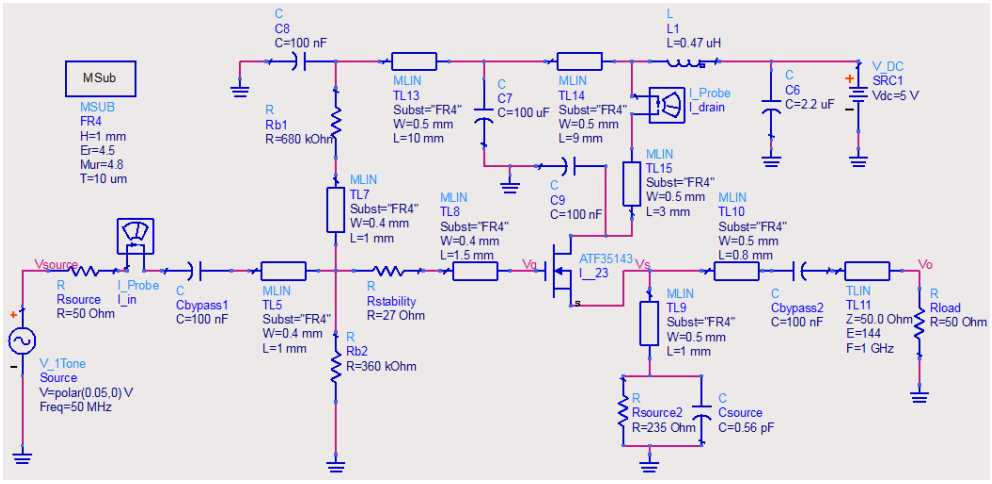
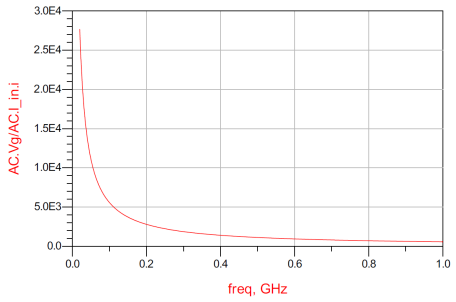


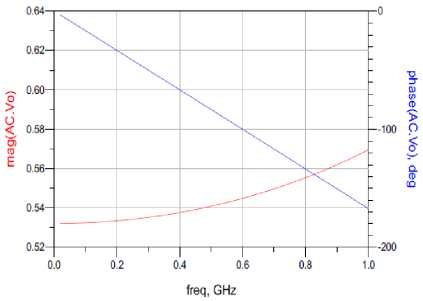
Figure 3.15: The schematic of single stage amplifier.

The schematic of the single stage amplifier is demonstrated in Figure 3.15. The

transmission lines represent connections of the individual components in the circuit. There is a compensation capacitor at the source and a stabilization resistance is added to the gate for damping the oscillations triggered by the circuit at high frequencies.



(a) Simulated input impedance of the single stage amplifier.



(b) Simulated voltage gain of the amplifier.

Figure 3.16: Simulated input impedance and gain of the single stage amplifier.

The input impedance pattern of the circuit is as demonstrated in Figure 3.16a, which is almost identical to the calculated pattern in Figure 3.14. The voltage gain of the amplifier is demonstrated in Figure 3.16b, thus half of the probed voltage would be transferred to the output.

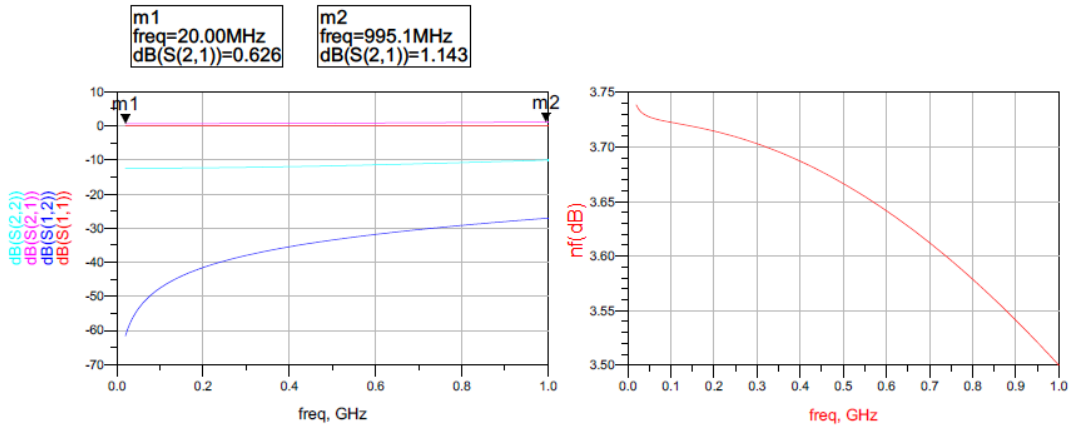


Figure 3.17: S-parameter and noise figure measurements schematic of the single stage amplifier.

S-parameters together with the amplifier noise figure have been simulated as shown in Figure 3.17. The port impedances are 50Ω.

The device is unilateral as S_{12} and the gain are small, which implies that S_{11} is the input reflection coefficient and S_{22} is the output reflection coefficient. Here, S_{11} demonstrates presence of high input impedance. For S_{21}, the value is starting from 0.63dB and slightly increasing till 1.14dB.

noisefreq	NFmin	Sopt	Rn
20.00 MHz	0.154	0.974 / 0.227	68.210
128.9 MHz	0.195	0.967 / 1.435	67.697
237.8 MHz	0.257	0.957 / 2.637	67.376
346.7 MHz	0.326	0.944 / 3.837	66.899
455.6 MHz	0.399	0.932 / 5.036	66.254
564.4 MHz	0.473	0.918 / 6.235	65.445
673.3 MHz	0.547	0.904 / 7.434	64.477
782.2 MHz	0.621	0.889 / 8.633	63.358
891.1 MHz	0.695	0.874 / 9.831	62.099
1.000 GHz	0.768	0.858 / 11.026	60.709

Figure 3.18: Noise parameters extracted from the simulation for single stage amplifier.

The noise figure appears less than 3.75dB when the source impedance is 50Ω. This data will be compared to the measurement since noise source for the measurement has 50Ω impedance. For determining actual noise figure of the amplifier when antenna is connected, noise parameters of the configuration that are demonstrated in Figure 3.18 are to be used in the next chapter.

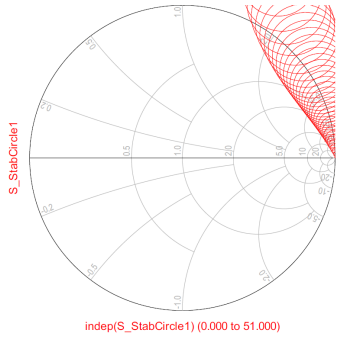
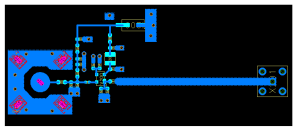


Figure 3.19: Stability circles from 20MHz to 1000MHz for which centre point in the Smith chart is stable as $\mid S_{11} \mid < 1$.

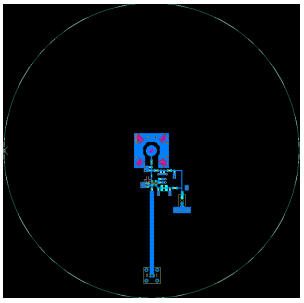
Stability of the amplifier is another important consideration. Together with the stabilization resistor and the compensation capacitor, the stability circles of the amplifier are as shown in Figure 3.19. The amplifier is stable when the antenna is connected, for which Γ_s is given in Figure 3.8a.

3.4.1.1 PCB Layout

PCB design is done by "MENTOR Graphics". The substrate is made of 1mm thick FR4 material. Surface mounted components are used. The design is as shown in Figure 3.20.



(a) PCB design mounted on back side of the ground plate of the antenna where antenna drive point is in the proximity of amplifier input.



(b) Location of the amplifier on the back side of circular ground plane of the antenna.

Figure 3.20: PCB of the single stage amplifier attached on the antenna drive point.

The antenna is extending on the opposite side of the circuit plane. Mounting framework is the large blue copper square and inside it, there exists the antenna drive point. The output port of the circuit is extended through the edge of the circuit plane for receiver connection.

3.4.2 Double Stage Amplifier

Similar to the single stage amplifier, the first stage is identical except for the compensation resistance and stabilization components. The second and the first stage biasing are demonstrated here.

freq	DC.Vs21	DC.Vd2	DC.Vg2	DC.I_drain2.i
0.0000 Hz	2.138 V	3.678 V	1.633 V	19.44 mA
freq	DC.Vs11	DC.Vd1	DC.Vg1	DC.I_drain1.i
0.0000 Hz	2.408 V	4.303 V	1.762 V	10.25 mA

The schematic of double stage amplifier is as in Figure 3.21. Regarding the

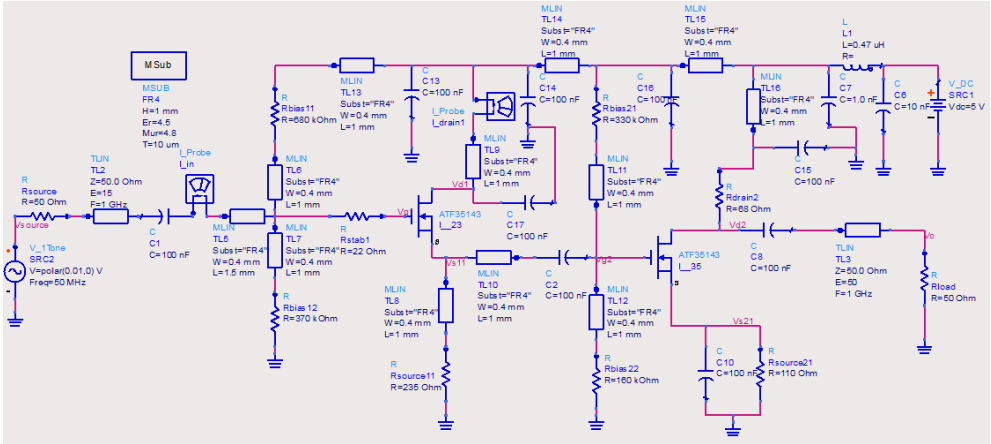


Figure 3.21: Schematic of double stage amplifier. Both transistors are ATF35143.

simulation of input impedance, there is no significant difference from the single stage therefore it is not repeated. Here, the gate resistor of the first stage is for stability. The second stage drain resistance determines primarily the output impedance and the gain. As a result, gain could not be further improved as output impedance has a constraint.

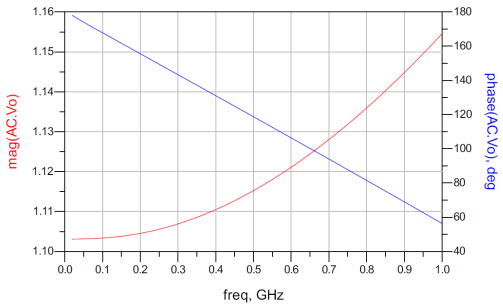


Figure 3.22: Simulated voltage gain of the double stage amplifier.

The voltage gain of the amplifier is demonstrated in Figure 3.22. There is a voltage gain this time for compensation of voltage drop at the buffering of antenna voltage.

S-parameters together with the noise figure of the amplifier when the source resistance is 50Ω are simulated as demonstrated in Figure 3.23. The output isolation is increased here significantly due to presence of the second stage. Again,

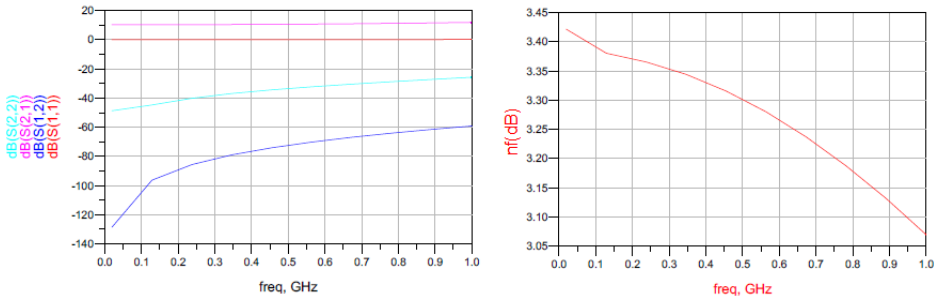


Figure 3.23: S-parameter and noise figure measurements schematic of the double stage amplifier.

S_{11} indicates presence of a high input impedance. The noise figure of the amplifier is less than 3.45dB for 50Ω source impedance which is less than single stage due to smaller stabilization resistors. For the actual noise figure of the amplifier when

freq	NFmin	Sopt	Rn
20.00 MHz	0.142	0.973 / 0.850	59.895
128.9 MHz	0.173	0.967 / 5.448	58.720
237.8 MHz	0.218	0.958 / 10.042	58.006
346.7 MHz	0.270	0.947 / 14.638	56.960
455.6 MHz	0.324	0.935 / 19.240	55.566
564.4 MHz	0.380	0.923 / 23.850	53.842
673.3 MHz	0.436	0.910 / 28.470	51.819
782.2 MHz	0.492	0.896 / 33.103	49.530
891.1 MHz	0.547	0.882 / 37.751	47.015
1.000 GHz	0.602	0.867 / 42.415	44.317

Figure 3.24: Noise parameters extracted from the simulation for double stage amplifier.

the antenna is connected, the noise parameters of the circuit that are given in Figure 3.24 are to be used in the next chapter.

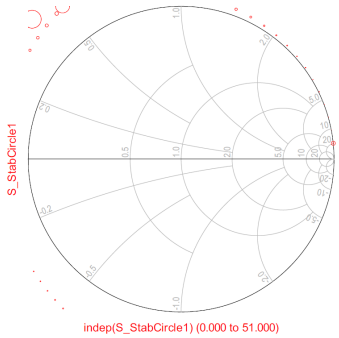
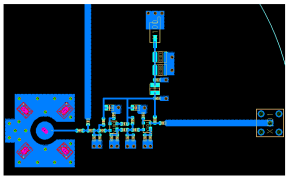


Figure 3.25: Stability circles from 20MHz to 1000MHz for which center point in the Smith chart is stable as $\mid S_{11} \mid < 1$.

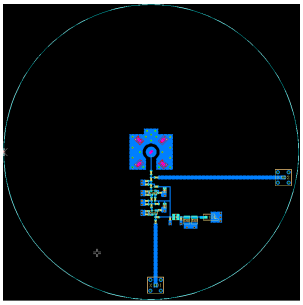
For the stability, the presence of resistance at the gate of the first stage provides stability which is demonstrated in Figure 3.25.

3.4.2.1 PCB Layout

Here, everything is identical with the case of single stage amplifier, except for presence of an aditional stage. The layout of the double stage amplifier attached on the antenna is demonstrated in Figure 3.26.



(a) PCB design mounted on back side of the ground plate of the antenna where antenna drive point is in the proximity of amplifier input.



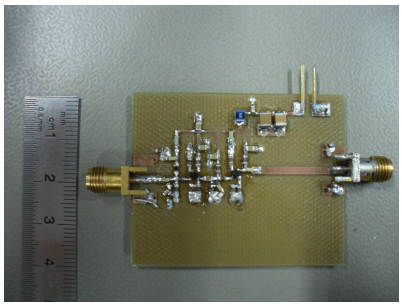
(b) Location of the amplifier on the back side of circular ground plane of the antenna.

Figure 3.26: PCB of the double stage amplifier attached on the antenna drive point.

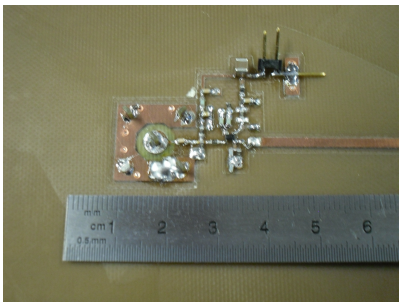
Chapter 4

Measurement Results

Initially, S-parameters of the amplifiers are measured with the network analyzer. The test board for two stage amplifier and single stage mounted on the antenna are as in Figure 4.1, for representing two test schemes with different configurations.



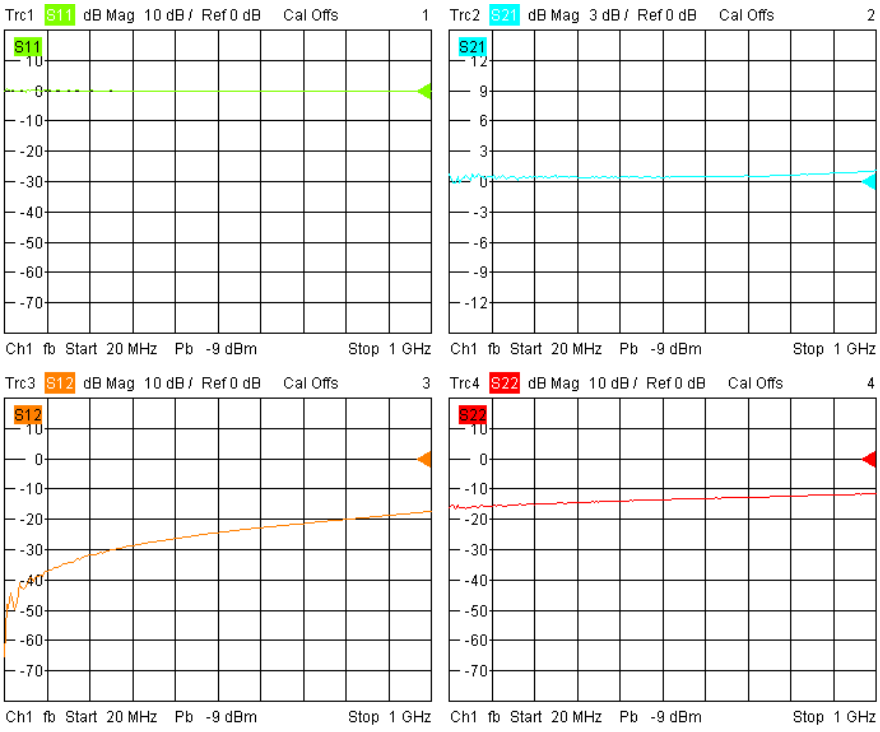
(a) Test board of two stage amplifier.



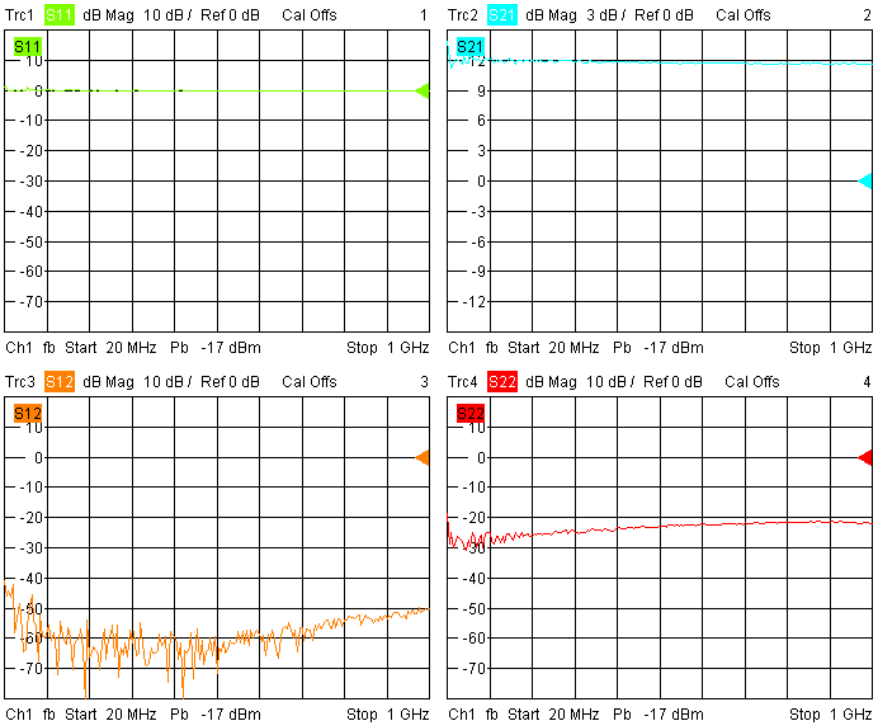
(b) Single stage just after antenna drive point.

Figure 4.1: Layouts of the amplifiers on the test board and antenna.

In Figure 4.2a and 4.2b, the measured S-parameters of the single and the double stage amplifiers are demonstrated. It appears that for both of the amplifiers, measured and simulated S-parameters are consistent. This implies that noise parameters that are obtained from ADS model provided by the transistor vendor would yield accurate noise parameters.



(a) Single stage measured S-parameters.



(b) Double stage measured S-parameters.

In order to evaluate performance of the antenna combined with the amplifier, single port S-parameter measurement of the antenna should be conducted. In the previous chapter, the measurement was compared to the simulation of the antenna and it appeared to be consistent. For completeness, Figure 4.3 demonstrates the antenna reflection coefficient data in detail. Measurement of the antenna is

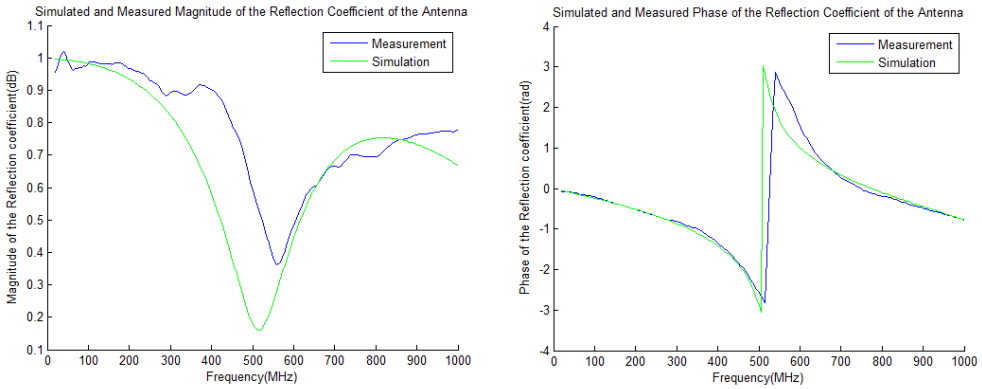


Figure 4.3: Measured and simulated antenna reflection coefficient.

sensitive to the external environment, thus it could be observed from fluctuations in the measured antenna reflection coefficient. Nevertheless, the measured data is adequately represented by the simulation. Hence, while determining transducer gain and noise performance of the amplifier, simulation data is preferable since it provides smooth data in an accurate manner.

Performance of the active antenna could be demonstrated by determining the amplifier transducer gain and noise figure when it is driven by the antenna. Initially, noise figure would be considered.

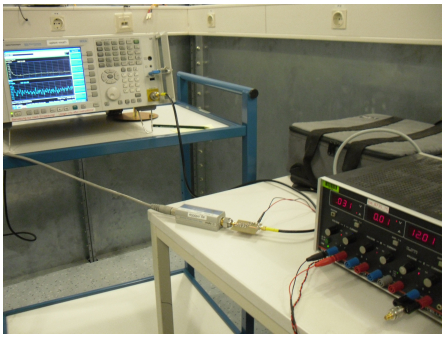
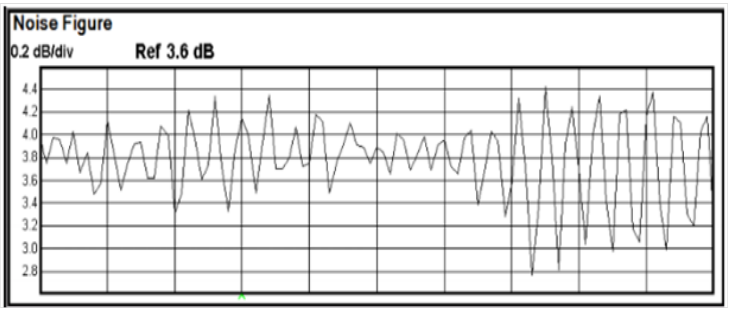


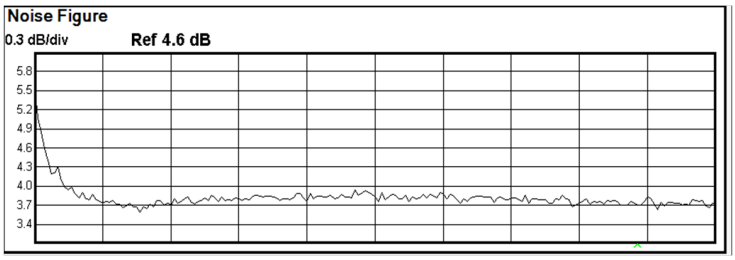
Figure 4.4: Shielded room and noise figure measurement environment.

Measurement environment consists of a shielded room with a noise source having 50Ω impedance and a signal analyzer, which is calibrated prior to the measurement. The setup is demonstrated in Figure 4.4. The data obtained here can only be used for determining accuracy of the noise parameters that are provided by the simulation, since during operation of the active antenna, noise performance of the amplifier would be determined by the antenna impedance.

Figure 4.5a shows the measured noise figure of the single stage amplifier and Figure 4.5b demonstrates the measured noise figure of the double stage amplifier when the source impedance for both cases is 50Ω.



(a) Noise figure measurement of the single stage amplifier from $20MHz$ to $1000MHz$.



(b) Noise figure measurement of the double stage amplifier from 20MHz to 1000MHz.

Figure 4.5: Noise figure measurement results for respective designs.

The noise performance of the devices are similar to the simulation results. For the single stage amplifier, the noise figure is aproximately 3.7dB in the overall. For the double stage amplifier, the noise figure is around 3.75dB at frequencies higher than 80MHz and at most 5.2dB at the lower portion of frequency range. The measured noise values are slightly higher than circuit simulation values.

Operational noise figure of the amplifiers when the antenna is connected could be determined by:

$$NF = NF_{min} + \frac{4R_n}{50} \frac{\mid \Gamma_s - \Gamma_{optimal} \mid^2}{(1- \mid \Gamma_s \mid^2) \mid 1 + \Gamma_{optimal} \mid^2} \tag{4.1}$$

where R_n, $\Gamma_{optimal}$ and NF_{min} are noise parameters of the amplifiers introduced in Figures 3.18 and 3.24. Resultant operational noise figure of the amplifiers are

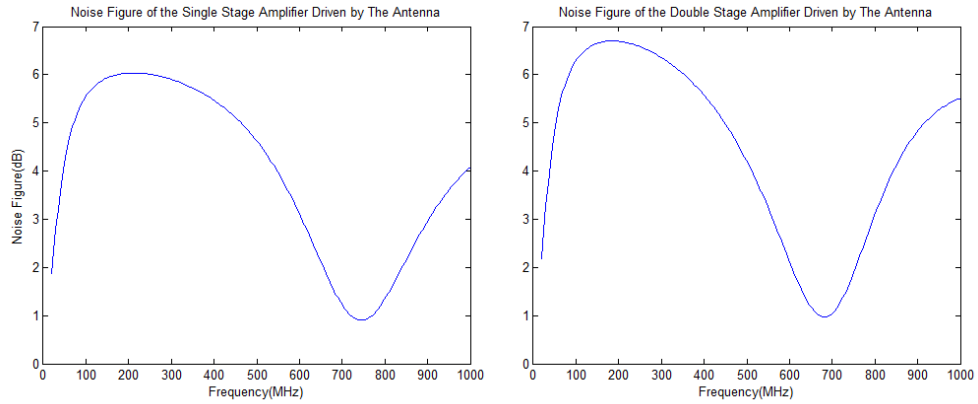


Figure 4.6: Noise figure of the single and the double stage amplifiers driven by the antenna.

demonstrated in Figure 4.6. The values of the single stage noise figure is 6.6dB and the double stage noise figure is 7.2dB at their worst cases.

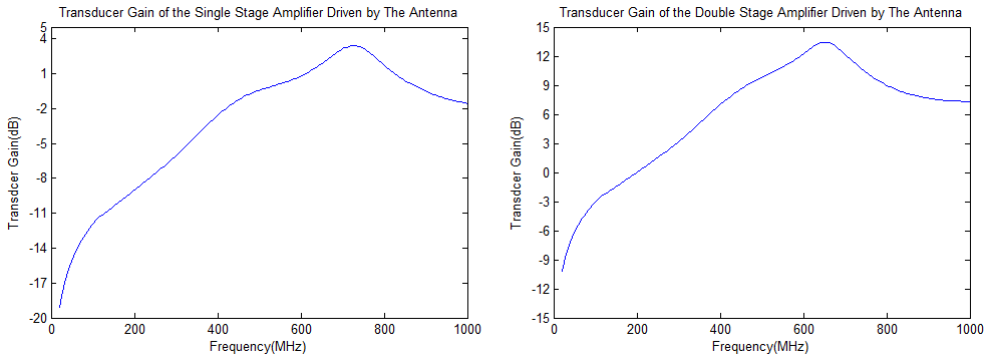


Figure 4.7: The transducer gain of the single and the double stage amplifiers driven by the antenna.

The transducer gain of the amplifiers should be determined. The measured data is used in Equation 3.13 and the transducer gain is shown in Figure 4.7.

The statement suggests the extent of delivered power to the load with respect to available power from the antenna. For lower frequencies, around 9dB less of the available power is delivered to the receiver for the single stage amplifier when compared with the double stage amplifier. For the lower frequency band, the available power from the antenna is very large due to the small antenna resistance. As a result, the transducer gain is very small in this location, however, the antenna resistance is so small that even if there exists passive matching, loss resistance of the passive matching network dominates the antenna resistance and delivered power will be less than available power. This fact could be demonstrated by matching the antenna passively and comparing the performance with the amplifier performance.

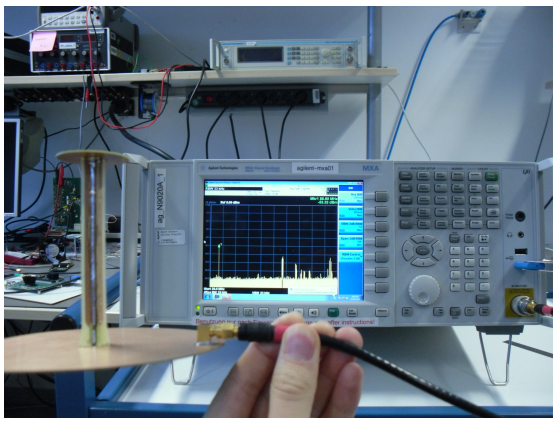
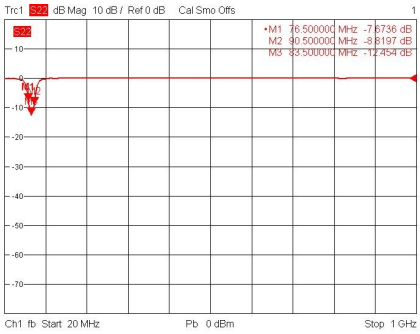


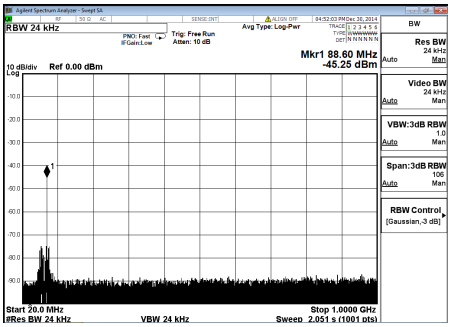
Figure 4.8: Antenna connected to the signal analyzer.

To demonstrate power that is delivered to the receiver, signals on the air are tracked for fixed positioning of the antennas for which one is passively matched and the other two are antennas consisting of respective amplifiers attached. The signal analyzer that is used for this purpose is demonstrated in Figure 4.8, which is optimized for 50Ω source impedance. Therefore, for performance evaluation, the antenna is initially passively matched to the receiver impedance, then compared with the active antenna performance.

The test frequency is selected as 88.6MHz, which is transmitted from nearby place having good signal strength. In Figure 4.9, the passively matched antenna and delivered power is demonstrated, which would be taken as reference. Here, LC section is used for matching, for which there is losses due to components.

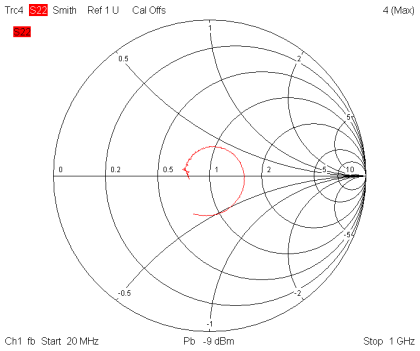


(a) Reflection coefficient of passively matched antetenna at 88.6MHz.

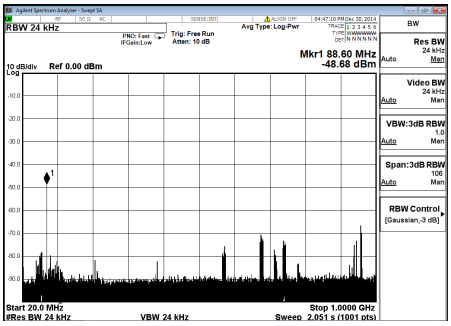


(b) Field test of passively matched antenna.

Figure 4.9: Passively matched antenna measurements.



(a) Reflection coefficient of single stage amplifier when antenna is connected.



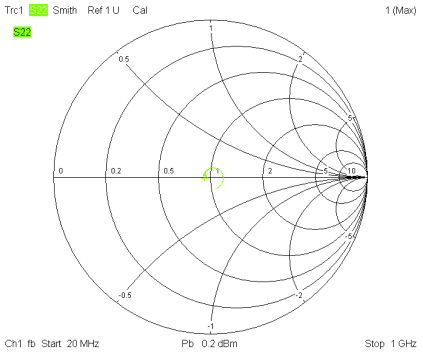
(b) Test of single stage active antenna.

Figure 4.10: Single stage active antenna test.

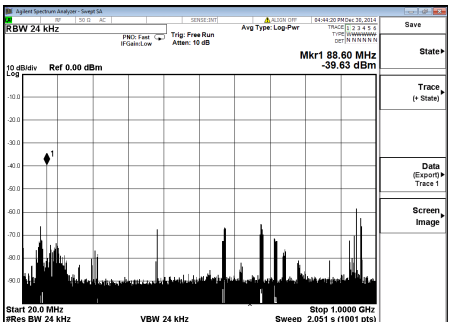
The signal strength is around -45.2dBm. Regarding this result, single stage active antenna performance which appears to be as in Figure 4.10, could be compared. For the reference frequency, the signal power appears around -48.7dB. The difference between passive matching and this is around 3.5dB. It is less than the value which transducer gain suggests, since antenna resistance is very small at this frequency and the matching losses dominates as mentioned. Therefore, a comparison with the passive matching will provide insight about the extent of improvement in the power gain which is provided by the amplifiers. It can be deduced that for the frequency less than 300MHz where loss resistance dominates the antenna resistance, practically the single stage amplifier provides 3.5dB less power gain when compared with the LC passive matching that has component losses. Thus, comparison with the double stage would be made for justification

of the transducer gain.

For the case of output impedance, the single stage active antenna provides a source impedance that is near 50Ω to the receiver, as demonstrated on the Smith chart. Reflection coefficient of single stage active antenna is at most −10dB.



(a) Reflection coefficient of double stage amplifier when antenna is connected.



(b) Test of double stage active antenna.

Figure 4.11: Double stage active antenna test.

The performance of the double stage active antenna is shown in Figure 4.11. When compared to the single stage amplifier, the increase in the delivered power appears as 9dB as expected from the comparison of the transducer gain of the amplifiers. For the lower portion of the bandwidth where the loss resistance dominates the antenna resistance, the double stage amplifier provides a 6dB power gain improvement when compared with the lossy LC matching. For the higher frequencies where the antenna resistance dominates the loss resistance, the transducer gain represents the improvement of the delivered power from the antenna.

For the case of the output impedance, the double stage buffer amplifier provides an impedance to the receiver having a very close value to 50Ω.

Chapter 5

Conclusion

In this thesis, an electrically small antenna (ESA) is utilized for an ultra wideband direction finding system. The antenna performance is bounded with theoretical limitations which indicates that the antenna itself is strictly narrowband and not possible to be used within $20 - 1000$MHz. Addition of a buffer amplifier to the drive point of the antenna provided the flexibility of ultra wideband utilization of the ESA.

Two different buffer amplifiers have been designed and analyzed. Both designs have the potential to probe the antenna induced voltage effectively due to their high input impedance, on the other side, the single stage buffer amplifier provided a poor transducer gain with 3.5dB more loss when compared with the passive matching as its worst case while the double stage buffer amplifier yields good performance having transducer gain of 9dB better than the single stage and 5.5dB better than the passive matching at its worst case, within the whole bandwidth of operation.

The single stage amplifier demonstrates smaller noise contribution, having a worst case noise figure of 6.6dB and costs less DC power as well as less space. The double stage buffer amplifier has a better isolation while having a better output impedance compared to the single stage, however the DC power consumption is

larger and the noise figure performance is 7.1dB at its worst case.

The achieved performance demonstrates that the antenna became wideband and signal delivery capabilities are improved significantly. Compared to the passive matching, the double stage buffer amplifier is better while the single stage amplifier appears to be deficient in terms of power gain. Justification of the choice between respective designs should be made according to the operational requirements and the SNR of the considered signal.

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Appendix A

ATF35143 Datasheet

ATF-35143
Low Noise Pseudomorphic HEMT
in a Surface Mount Plastic Package

Data Sheet

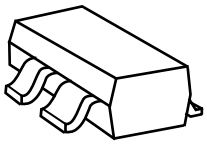
Description

Avago's ATF-35143 is a high dynamic range, low noise, PHEMT housed in a 4-lead SC-70 (SOT-343) surface mount plastic package.

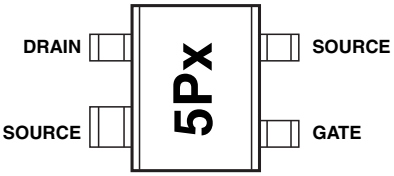
Based on its featured performance, ATF-35143 is suitable for applications in cellular and PCS base stations, LEO systems, MMDS, and other systems requiring super low noise figure with good intercept in the 450 MHz to 10 GHz frequency range.

Other PHEMT devices in this family are the ATF-34143 and the ATF-33143. The typical specifications for these devices at 2 GHz are shown in the table below:

Surface Mount Package
SOT-343



Pin Connections and Package Marking



Note: Top View. Package marking provides orientation and identification.
"5P" = Device code
"x" = Date code character. A new character is assigned for each month, year.

Features

- Lead-free Option Available
- Low Noise Figure
- Excellent Uniformity in Product Specifications
- Low Cost Surface Mount Small Plastic Package SOT-343 (4 lead SC-70)
- Tape-and-Reel Packaging Option Available

Specifications

1.9 GHz; 2 V, 15 mA (Typ.)

- 0.4 dB Noise Figure
- 18 dB Associated Gain
- 11 dBm Output Power at 1 dB Gain Compression
- 21 dBm Output 3rd Order Intercept

Applications

- Low Noise Amplifier for Cellular/PCS Handsets
- LNA for WLAN, WLL/RLL, LEO, and MMDS Applications
- General Purpose Discrete PHEMT for Other Ultra Low Noise Applications

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 0)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

Part No.	Gate Width	Bias Point	NF (dB)	Ga (dB)	OIP3 (dBm)
ATF-33143	1600 µ	4 V, 80 mA	0.5	15.0	33.5
ATF-34143	800 µ	4 V, 60 mA	0.5	17.5	31.5
ATF-35143	400 µ	2 V, 15 mA	0.4	18.0	21.0

ATF-35143 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain - Source Voltage[2]	V	5.5
V_{GS}	Gate - Source Voltage[2]	V	-5
V_{GD}	Gate Drain Voltage[2]	V	-5
I_{DS}	Drain Current[2]	mA	I_{dss}[3]
P_{diss}	Total Power Dissipation[4]	mW	300
$P_{in\ max}$	RF Input Power	dBm	14
T_{CH}	Channel Temperature	°C	160
T_{STG}	Storage Temperature	°C	-65 to 160
θ_{jc}	Thermal Resistance[5]	°C/W	150

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Assumes DC quiesent conditions.
3. V_{GS} = 0 V
4. Source lead temperature is 25°C. Derate 3.2 mW/°C for T_L > 67°C.
5. Thermal resistance measured using QFI Measurement method.

Product Consistency Distribution Charts [7, 8]

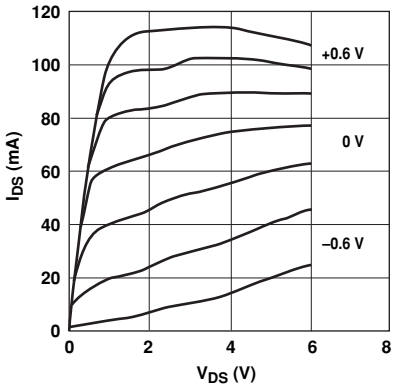


Figure 1. Typical Pulsed I-V Curves[6]. (V_{GS} = -0.2 V per step)

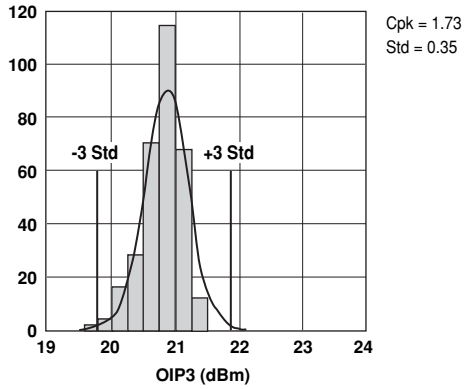


Figure 2. OIP3 @ 2 GHz, 2 V, 15 mA. LSL=19.0, Nominal=20.9, USL=23.0

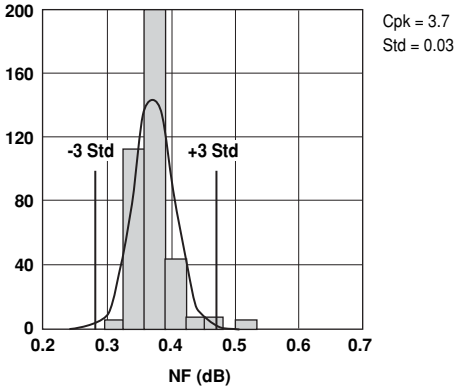


Figure 3. NF @ 2 GHz, 2 V, 15 mA. LSL=0.2, Nominal=0.37, USL=0.7

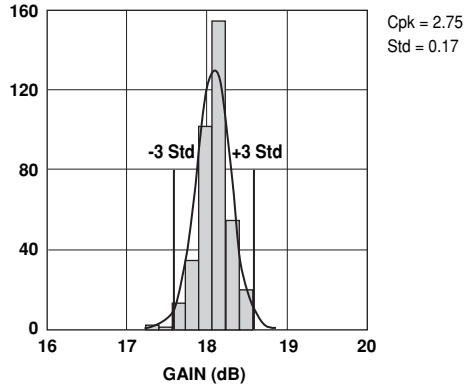


Figure 4. Gain @ 2 GHz, 2 V, 15 mA. LSL=16.5, Nominal=18.0, USL=19.5

Notes:
6. Under large signal conditions, VGS may swing positive and the drain current may exceed Idss. These conditions are acceptable as long as the maximum Pdiss and Pin max ratings are not exceeded.
7. Distribution data sample size is 450 samples taken from 9 different wafers. Future wafers allocated to this product may have nominal values anywhere within the upper and lower spec limits.
8. Measurements made on production test board. This circuit represents a trade-off between an optimal noise match and a realizeable match based on production test requirements. Circuit losses have been de-embedded from actual measurements.

ATF-35143 Electrical Specifications

T_A = 25°C, RF parameters measured in a test circuit for a typical device

Symbol	Parameters and Test Conditions			Units	Min.	Typ.[2]	Max.
I_{dss}[1]	Saturated Drain Current		V_{DS} = 1.5 V, V_{GS} = 0 V	mA	40	65	80
V_P[1]	Pinchoff Voltage		V_{DS} = 1.5 V, I_{DS} = 10% of I_{dss}	V	-0.65	-0.5	-0.35
I_d	Quiescent Bias Current		V_{GS} = 0.45 V, V_{DS} = 2 V	mA	—	15	—
g_m[1]	Transconductance		V_{DS} = 1.5 V, $g_m = I_{dss}/V_P$	mmho	90	120	—
I_{GDO}	Gate to Drain Leakage Current		V_{GD} = 5 V	µA			250
I_{gss}	Gate Leakage Current		$V_{GD} = V_{GS}$ = -4 V	µA	—	10	150
NF	Noise Figure[3]	f = 2 GHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB		0.4	0.7
			V_{DS} = 2 V, I_{DS} = 5 mA			0.5	0.9
		f = 900 MHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB		0.3	
			V_{DS} = 2 V, I_{DS} = 5 mA			0.4	
G_a	Associated Gain[3]	f = 2 GHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB	16.5	18	19.5
			V_{DS} = 2 V, I_{DS} = 5 mA		14	16	18
		f = 900 MHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB		20	
			V_{DS} = 2 V, I_{DS} = 5 mA			18	
OIP3	Output 3rd Order Intercept Point[4, 5]	f = 2 GHz	V_{DS} = 2 V, I_{DS} = 15 mA	dBm	19	21	
			V_{DS} = 2 V, I_{DS} = 5 mA			14	
		f = 900 MHz	V_{DS} = 2 V, I_{DS} = 15 mA	dBm		19	
			V_{DS} = 2 V, I_{DS} = 5 mA			14	
P_{1dB}	1 dB Compressed Intercept Point[4]	f = 2 GHz	V_{DS} = 2 V, I_{DSQ} = 15 mA	dBm		10	
			V_{DS} = 2 V, I_{DSQ} = 5 mA			8	
		f = 900 MHz	V_{DS} = 2 V, I_{DSQ} = 15 mA	dBm		9	
			V_{DS} = 2 V, I_{DSQ} = 5 mA			9	

Notes:
1. Guaranteed at wafer probe level
2. Typical value determined from a sample size of 450 parts from 9 wafers.
3. 2V 5 mA min/max data guaranteed via the 2V 15 mA production test.
4. Measurements obtained using production test board described in Figure 5.
5. P_{out} = -10 dBm per tone

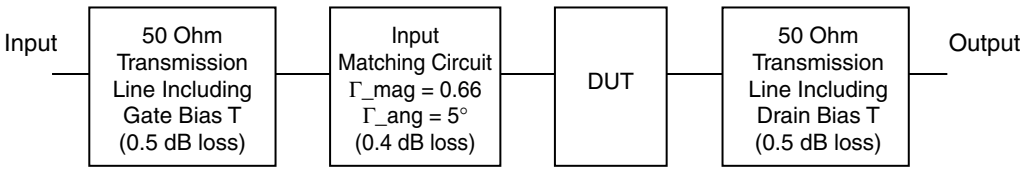


Figure 5. Block diagram of 2 GHz production test board used for Noise Figure, Associated Gain, P_{1dB}, and OIP3 measurements. This circuit represents a trade-off between an optimal noise match and a realizable match based on production test requirements. Circuit losses have been de-embedded from actual measurements.

ATF-35143 Typical Scattering Parameters, V_{DS} = 2 V, I_{DS} = 10 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.50	0.99	-18.75	15.89	6.23	164.76	-32.40	0.024	77.63	0.63	-14.09	24.14
0.75	0.97	-29.11	15.79	6.16	155.98	-28.87	0.036	70.58	0.61	-19.69	22.30
1.00	0.95	-38.28	15.61	6.03	148.42	-26.56	0.047	64.88	0.60	-26.10	21.08
1.50	0.91	-55.52	15.17	5.73	133.92	-23.61	0.066	54.16	0.57	-38.73	19.39
1.75	0.89	-63.78	14.92	5.57	127.01	-22.62	0.074	49.11	0.56	-44.79	18.75
2.00	0.86	-71.82	14.65	5.40	120.27	-21.72	0.082	44.08	0.54	-50.70	18.19
2.50	0.81	-87.59	14.11	5.08	107.36	-20.35	0.096	34.60	0.51	-61.95	17.23
3.00	0.76	-103.22	13.54	4.76	95.04	-19.41	0.107	25.71	0.47	-72.47	16.48
4.00	0.66	-134.81	12.40	4.17	71.95	-18.27	0.122	9.04	0.41	-91.47	15.34
5.00	0.61	-165.34	11.29	3.67	50.43	-17.65	0.131	-5.97	0.34	-110.05	14.47
6.00	0.58	165.88	10.27	3.26	30.28	-17.33	0.136	-20.15	0.27	-129.24	13.80
7.00	0.57	137.00	9.27	2.91	10.68	-17.14	0.139	-33.84	0.21	-150.49	13.21
8.00	0.58	110.78	8.33	2.61	-8.09	-17.14	0.139	-45.60	0.17	-174.77	12.73
9.00	0.61	86.75	7.32	2.32	-26.38	-17.20	0.138	-57.65	0.13	154.01	10.69
10.00	0.65	66.25	6.44	2.10	-43.90	-17.20	0.138	-68.22	0.11	118.18	9.85
11.00	0.69	46.88	5.54	1.89	-61.97	-17.27	0.137	-79.30	0.14	78.36	9.16
12.00	0.72	27.76	4.56	1.69	-79.90	-17.39	0.135	-90.87	0.19	49.57	8.34
13.00	0.74	8.62	3.45	1.49	-97.18	-17.79	0.129	-102.19	0.26	29.95	7.35
14.00	0.77	-5.28	2.33	1.31	-112.92	-18.20	0.123	-110.80	0.33	9.45	6.51
15.00	0.82	-16.03	1.29	1.16	-128.66	-18.56	0.118	-120.09	0.39	-7.98	6.51
16.00	0.82	-28.32	0.19	1.02	-144.87	-18.79	0.115	-129.92	0.45	-22.30	5.48
17.00	0.84	-40.43	-0.87	0.91	-159.49	-18.79	0.115	-139.60	0.51	-32.23	5.24
18.00	0.86	-56.14	-1.99	0.80	-175.19	-19.33	0.108	-149.17	0.57	-44.43	4.72

ATF-35143 Typical Noise Parameters

V_{DS} = 2 V, I_{DS} = 10 mA

Freq.	F_{min}	Γ_{opt}		$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.	-	dB
0.5	0.10	0.88	5.0	0.15	20.5
0.9	0.11	0.84	14.0	0.15	19.0
1.0	0.12	0.83	16.0	0.15	18.6
1.5	0.17	0.77	26.0	0.15	17.5
1.8	0.20	0.74	31.9	0.15	16.9
2.0	0.23	0.71	37.3	0.14	16.4
2.5	0.29	0.66	48.6	0.14	15.7
3.0	0.34	0.60	60.6	0.12	15.0
4.0	0.46	0.52	86.8	0.12	13.6
5.0	0.58	0.45	115.3	0.08	12.4
6.0	0.69	0.40	145.8	0.05	11.3
7.0	0.81	0.37	177.7	0.05	10.3
8.0	0.92	0.35	-149.3	0.07	9.5
9.0	1.04	0.35	-115.6	0.12	8.8
10.0	1.16	0.37	-81.8	0.22	8.3

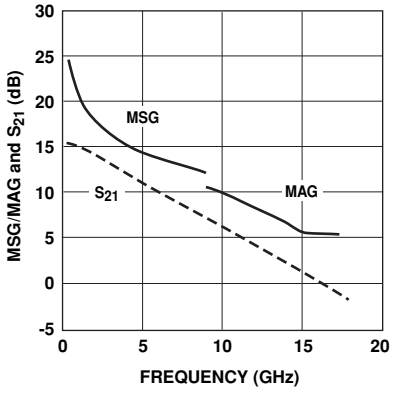


Figure 19. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 2 V, 10 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at sixteen different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead. The parameters include the effect of four plated through via holes connecting source landing pads on top of the test carrier to the microstrip ground plane on the bottom side of the carrier. Two 0.020 inch diameter via holes are placed within 0.010 inch from each source lead contact point, one via on each side of that point.

ATF-35143 Typical Scattering Parameters, V_{DS} = 2 V, I_{DS} = 30 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.50	0.99	-20.95	18.17	8.10	163.18	-33.56	0.021	77.39	0.49	-15.99	25.87
0.75	0.96	-32.34	18.02	7.96	153.79	-30.17	0.031	70.55	0.47	-22.00	24.10
1.00	0.94	-42.36	17.77	7.73	145.67	-27.96	0.040	65.08	0.46	-29.03	22.86
1.50	0.88	-61.09	17.18	7.22	130.36	-25.04	0.056	54.79	0.43	-42.64	21.11
1.75	0.85	-69.98	16.85	6.96	123.20	-24.01	0.063	50.12	0.41	-48.96	20.42
2.00	0.82	-78.53	16.50	6.69	116.28	-23.22	0.069	45.58	0.39	-55.19	19.86
2.50	0.76	-95.14	15.81	6.17	103.17	-21.94	0.080	37.15	0.36	-66.91	18.87
3.00	0.70	-111.48	15.11	5.69	90.88	-21.01	0.089	29.29	0.34	-77.74	18.06
4.00	0.61	-143.89	13.73	4.86	68.24	-19.83	0.102	14.76	0.28	-97.29	16.78
5.00	0.56	-174.55	12.46	4.20	47.48	-19.02	0.112	1.63	0.23	-117.24	15.74
6.00	0.55	157.19	11.31	3.68	28.10	-18.49	0.119	-10.98	0.17	-139.78	14.90
7.00	0.55	129.18	10.22	3.24	9.28	-18.13	0.124	-23.67	0.13	-169.09	14.17
8.00	0.56	104.19	9.20	2.88	-8.75	-17.79	0.129	-34.72	0.11	155.22	11.98
9.00	0.60	81.48	8.15	2.56	-26.37	-17.59	0.132	-46.33	0.11	112.23	10.82
10.00	0.64	62.07	7.24	2.30	-43.37	-17.33	0.136	-57.43	0.13	77.30	10.15
11.00	0.68	43.83	6.29	2.06	-60.90	-17.20	0.138	-68.78	0.18	51.74	9.51
12.00	0.72	25.46	5.27	1.84	-78.22	-17.14	0.139	-81.32	0.24	32.67	8.77
13.00	0.74	6.81	4.14	1.61	-94.88	-17.33	0.136	-93.11	0.31	17.81	7.87
14.00	0.77	-6.74	3.01	1.41	-110.07	-17.65	0.131	-103.06	0.38	0.45	7.08
15.00	0.82	-17.21	1.94	1.25	-125.15	-17.86	0.128	-112.88	0.43	-15.44	7.06
16.00	0.83	-29.31	0.87	1.11	-140.80	-18.06	0.125	-123.55	0.49	-29.37	6.13
17.00	0.85	-41.30	-0.15	0.98	-154.83	-18.13	0.124	-134.43	0.54	-38.55	5.89
18.00	0.87	-56.87	-1.24	0.87	-170.03	-18.56	0.118	-144.88	0.60	-49.70	5.39

ATF-35143 Typical Noise Parameters

V_{DS} = 2 V, I_{DS} = 30 mA

Freq.	F_{min}	Γ_{opt}		$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.	-	dB
0.5	0.11	0.87	2.7	0.18	21.6
0.9	0.15	0.81	12.1	0.17	20.2
1.0	0.16	0.80	14.5	0.16	19.9
1.5	0.22	0.73	26.3	0.15	18.7
1.8	0.25	0.69	33.4	0.15	18.0
2.0	0.27	0.66	38.1	0.14	17.7
2.5	0.33	0.60	50.6	0.13	17.0
3.0	0.39	0.54	64.2	0.12	16.2
4.0	0.52	0.45	94.0	0.10	14.8
5.0	0.64	0.39	126.5	0.07	13.5
6.0	0.77	0.34	160.6	0.05	12.4
7.0	0.90	0.33	-164.7	0.06	11.4
8.0	1.02	0.33	-130.3	0.10	10.5
9.0	1.15	0.36	-97.5	0.18	9.7
10.0	1.28	0.40	-67.0	0.30	9.1

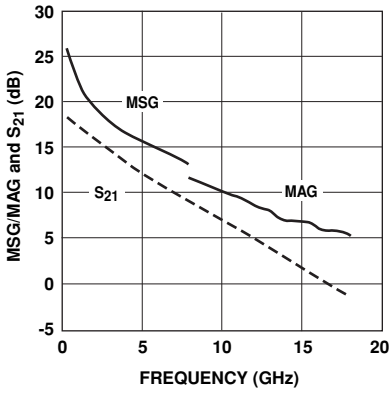


Figure 21. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 2 V, 30 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATF NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead. The parameters include the effect of four plated through via holes connecting source landing pads on top of the test carrier to the microstrip ground plane on the bottom side of the carrier. Two 0.020 inch diameter via holes are placed within 0.010 inch from each source lead contact point, one via on each side of that point.