GaN-on-SiC BROADBAND DRIVER AMPLIFIER DESIGN FOR C– AND X–BAND APPLICATIONS USING EM-BASED EXTRINSIC PARASITIC EXTRACTED HEMT MODELS

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By

Abdullah Hannan

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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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April 2025

Gallium Nitride (GaN) high electron mobility transistor (HEMT) technology is known for its high-power applications due to its wide band-gap and high electron mobility characteristics, which allow the use of larger voltages and currents in the circuit. This enables the design to output a higher RF power for the same gate periphery when compared to other technologies. Broadband driver amplifiers (DAs) operating in the C– and X–bands are commonly used for satellite communications, phased-array radar systems, and, signal generators. Designing an amplifier that achieves both, good small-signal and large-signal performance for such fractional bandwidths remains a challenge today. In this thesis, we present a GaN-on-SiC-based broadband DA monolithic microwave integrated circuit (MMIC) operating at 5-12 GHz. The 3-stage MMIC exhibits a typical small signal gain of 29.7 dB with a ± 1.4 dB gain ripple and input and output reflection losses better than 10.5 dB and 8.5 dB, respectively. The average saturated output power is 2.65 W, with an average power density of 3.31 W/mm. The DA occupies a chip area of 2.7 x 3.2 mm^2.

EM-based cold-FET technique is used to extract the extrinsic parasitic parameters (EPPs) for a typical $6 \times 100\ \mu m$ HEMT. Various HEMT structures are EM simulated discretely to obtain the scalability rules of the EPPs used for the HEMT model. The DA design is verified using the Process Design Kit (PDK) HEMT models, and the two sets of simulations are compared with the measurement results.

Keywords: Gallium Nitride, Broadband, Driver Amplifier, MMIC, Parasitic Extraction.

ÖZET

EM-TABANLI EKSTRİNSİC PARAZİTİKLERİ ÇIKARILMIŞ HEMT MODELİ KULLANARAK C- VE X-BANDI UYGULAMALARI İÇİN GaN-on-SiC GENİŞ BANT SÜRÜCÜ YÜKSELTECİ TASARIMI

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Elektrik vs Elektronic Mühendisliği, Yüksek Lisans
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Galyum Nitrür (GaN) yüksek elektron hareketlilik transistör (HEMT) teknolojisi, devrede daha büyük voltaj ve akımların kullanılmasına izin veren geniş bant aralığı özellikleri nedeniyle yüksek güç uygulamalarıyla bilinir. Bu, tasarımın diğer teknolojilerle karşılaştırıldığında aynı kapı çevresi için daha yüksek bir RF güç çıkışı sağlar. C- ve X- bantlarında çalışan geniş bant sürücü amplifikatörleri (DA'lar) genellikle uydu iletişimleri, faz dizili radar sistemleri ve sinyal jeneratörleri için kullanılır. Bu tür kesirli bant genişlikleri için hem küçük sinyal hem de büyük sinyal koşulunda iyi performans sunan bir amplifikatör tasarlamak günümüzde hala bir zorluktur. Bu tezde, 5-12 GHz'de çalışan GaN-on-SiC tabanlı geniş bant DA monolitik mikrodalga entegre devresi (MMIC) sunuyoruz. Tasarlanan 3 aşamalı MMIC, ± 1,4 dB kazanç dalgalanması ile 29,7 dB'lik tipik küçük sinyal kazancı sergilerken, giriş ve çıkış yansıma kayıpları sırasıyla 10,5 dB ve 8,5 dB'den daha iyidir. Ortalama saturasyon çıkış gücü 2,65 W iken ortalama güç yoğunluğu 3,31 W/mm'dir. DA çip alanı 2.7 x 3.2 mm^2.

EM tabanlı soğuk FET tekniği, tipik bir $6\times100\ \mu m$ HEMT'e ait dışsal parazitik parametrelerini (DPP) çıkarmak için kullanıldı. Çeşitli HEMT yapıları, HEMT modeli için kullanılan DPP'lerin ölçeklenebilirlik kurallarını elde etmek için ayrı ayrı EM simüle edildi. DA tasarımı, proses tasarım kiti (PDK) HEMT modelleri kullanılarak doğrulanır ve iki simülasyon seti ölçüm sonuçlarıyla karşılaştırıldı.

Anahtar sözcükler: Galyum Nitrür, Geniş Bant, Sürücü Amplifikatörü, MMIC, Parazitik Çıkarma..

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I am truly blessed to have my wife, Sara, as my partner. Her unwavering support and belief in me motivates me to push further every day. Her constant help and comfort provided me with the resilience to make this possible.

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Chapter 1

Introduction

1.1 Motivation & Problem Definition

In the past, Gallium Nitride (GaN) technology has been used for many high-power and advanced military applications such as in radar systems and satellite communications. The technology is now also being recognized in the commercial world as it is now considered a fundamental part of the ongoing and upcoming 5G/6G communication networks [3]. To make GaN suitable for high-frequency operations, GaN-based High Electron Mobility Transistors (HEMTs) are widely used because of their superior material properties. Monolithic Microwave Integrated Circuits (MMICs) allow consistent reproduction of GaN-based high-frequency circuits, such as RF power amplifiers [4, 5, 6], RF switches [7, 8], LNAs [9, 10, 11], phase-shifters and attenuators. An MMIC process can produce many compact chips in a single batch which helps to reduce the cost per chip.

More recently, broadband driver amplifiers using GaN technology are being used for multiple applications. The C– and the X–bands in particular are useful for satellite communications and are commonly used in electronic warfare applications. An important application of driver amplifiers (DAs) in these bands

is their use in-phased-array radar systems which are based on active electronically scanned arrays [12]. Another application of broadband amplifiers in these frequency bands includes signal generators where combining different bands in a single device is beneficial in reducing the total number of components used in the system [13]. In recent literature, there have been some medium output powered (< 3 W) broadband driver amplifiers reported. However, some of these have less output power densities [12, 13, 14]. Other reported DAs, although, have a very broadband design thanks to distributed or feedback-based matching networks [15], with fractional bandwidths greater than 100 %, they either compromise on the output reflection loss [14, 16, 17] or have a high output power ripple [12, 14]. Some DAs with good output return losses and output power densities [18, 19] lack enough fractional bandwidths. Moreover, there are reported amplifier designs that either focus only on the C-band [20, 21] or on the X-band [22]. Although these have good performances and can be used together for broadband applications using switches and triplexers, the extra circuitry causes losses and adds to the total cost of the system [23].

1.2 GaN HEMT Technology

The most widely used Silicon (Si) transistors are not very useful for high-power applications because of their limited band-gap energies. Recently, much research has been done in the field of wide-band semiconductors to cater to high-power, high-temperature, and high-frequency applications. Some of the other known wide band-gap semiconductors include Gallium Arsenide (GaAs), Silicon Carbide (SiC), and Indium Phosphide (InP). These semiconductors have been known to use MESFET, HBT, MOSFETs, and pHEMT-type transistors. However, over time, HEMTs turned out to be the preferred choice of transistors for high-power and high-frequency applications because of a naturally occurring highly dense two-dimensional electron gas (2DEG). A 2DEG is formed due to the piezo-electric effects at the heterojunction between Aluminum Gallium Nitride (AlGaN) and GaN. Such a heterojunction, with unequal band gaps, results in a confined quantum well consisting of high mobility free electron carriers. Since the free electrons

are separated from the donor atoms, there is less impurity scattering along the channel resulting in high drift and saturation velocities [24].

	Si	**GaAs**	**SiC**	**GaN**	**InP**
Band-gap energy eV	1.1	1.4	2.9	3.4	1.35
Electric break-down field 10^6 V/cm	0.3	0.4	2.5	3.3	0.5
Thermal Conductivity $W/(K\ cm)$	1.5	0.46	4.9	1.3	0.7
Electron Mobility cm^2/s	1300	5000	260	2000	5400
Saturation velocity $10^7 cm/s$	1.0	1.0	2.0	2.5	1.0

Table 1.1: Comparison of various semiconductor material properties [2].

Because of its wide band gap, the breakdown voltage of GaN HEMT is high. This allows the use of high voltages and currents and subsequently obtain high RF output powers. GaN HEMTs have higher electron mobility and saturation velocity making them ideal candidates for mm-wave purposes. A high maximum operation temperature is necessary to sustain the significant power dissipation across the transistors. However, since GaN does not have high thermal conductivity and is expensive to produce in bulk, it is not preferred as the main substrate carrier. GaN-on-Si can be used but it has a significant lattice mismatch and poor thermal properties. Silicon Carbide (SiC) is the best choice as the main substrate carrier because it has small lattice and thermal mismatches. The thermal conductivity of SiC is sufficiently high [3, 2].

1.3 Thesis Outline

In this thesis, NANOTAM's 250 nm AlGaN/GaN-on-SiC HEMT technology is used to fabricate a broadband DA MMIC focusing on the C– and X– bands (5–12 GHz). The presented DA achieves a good combination of small signal and

large signal performance. The DA has good reflection losses, high gain, and a low gain ripple. At the same time, it has a high output power density with a small output power ripple and reasonably good power added efficiency (PAE) for a broadband design.

The GaN-on-SiC fabrication technology that is used to fabricate this MMIC, together with the direct current (DC), small-signal, and large signal transistor characterization techniques, are discussed in Chapter 2. The HEMT models' extrinsic parasitic parameters were extracted and scaled using EM simulations as illustrated in Chapter 3. In Chapter 4, the detailed design steps of a three-stage DA and its respective small signal and large signal simulation results have been discussed. The design is done using the HEMT measurements but the simulations were also verified using the scalable HEMT models developed. In Chapter 5, the fabricated DA MMIC's measurement results have been compared with both sets of simulations. Finally, a discussion followed by a conclusion is presented in Chapter 6.

Chapter 2

Fabrication Process & Transistor Characterization

Before starting a design, it is important to understand the fabrication process and to characterize the active devices. The fabrication process can reveal critical parameters such as the resistivity of the metal layers, capacitance density between any two metal layers, and the use of application-specific structures like the air bridge. On the other hand, HEMT characterization gives a reasonably good estimate of how the device will perform under certain environmental and physical conditions. The HEMTs DC characterization is performed first to extract some fundamental characteristics like the transconductance (g_m), the threshold voltage (V_{th}), the maximum saturated drain current (I_{dss}), and the knee voltage of a transistor. Then the small-signal RF characterization is performed to evaluate the performance of the device as a function of frequency using the scattering parameters (S-parameters). Finally, the large-signal characterization helps identify the optimum impedance points under device gain compression. Important parameters like saturated output power and power-added efficiency (PAE) are characterized.

2.1 Fabrication Process

AlGaN/GaN HEMT on SiC process of Bilkent University Nanotechnology Research Center (NANOTAM) was used to fabricate the DA MMIC. The MMIC is fabricated on a 3-inch SiC wafer.

First, a controlled epitaxial growth on the SiC substrate is performed using the metal-organic chemical vapor deposition (MOCVD) technique. Then, mesa-etching is performed with an inductively coupled plasma reactive ion etching system by using a plasma-based dry etch to define the active regions. The passivation of the wafer takes place with Si_3N_4 using plasma enhanced chemical vapor deposition technique. Ohmic contact formation is done using an electron beam evaporator with Ti/Al/Ni/Au metal stacks. The passivation helps to produce T-shaped gates of 250 nm foot length.

The thin film resistors (TFRs) are realized with the sputtering of TaN. This results in a resistance equal to about 30 $\Omega/\square$. Metal-insulator-metal (MIM) capacitors are implemented with two metal layers of the process with Si_3N_4 as the dielectric material. The capacitors have a capacitance density equal to approximately 270 pF/mm^2. Air-bridge structures are used to prevent any parasitic capacitance at metal layer cross-overs and for the implementation of spiral inductors. During the back-side process, the SiC is thinned down to 100 μm, and the via-holes are coated with Au to provide a path to the ground plane. A sketch of the cross-section representing the fabrication process of the active devices and of the various passive components used in this design are shown in Figure 2.1 [25].

2.2 DC Measurement

The DC measurement set-up is used to perform a set of measurements in order to extract important device parameters. The three measurements that are typically performed include $I_d - V_d$, $I_{ds} - V_{gs}$, and the drain/gate leakage or breakdown measurements.

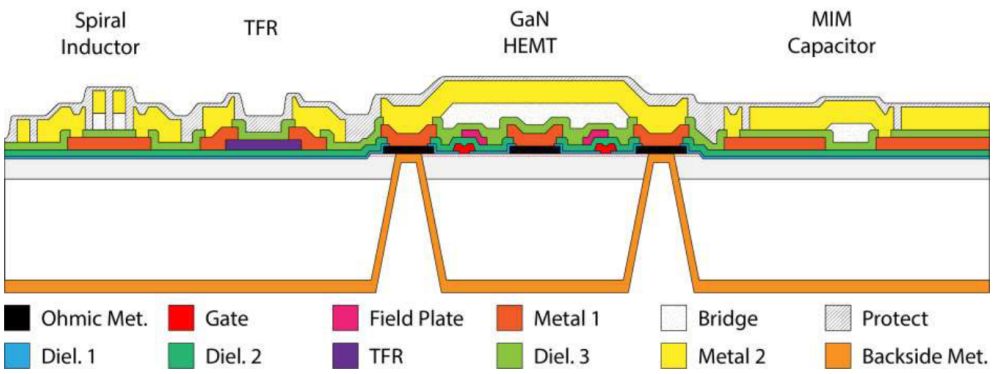


Figure 2.1: Cross-section sketch of NANOTAM's 250 nm fabrication process.

The DC measurements are performed on-wafer using a probe station and a high current handling probe to provide contact to the active devices. A power device analyzer, B1505 from Keysight, is used to visualize and save the data. The setup is shown in Figure 2.2.

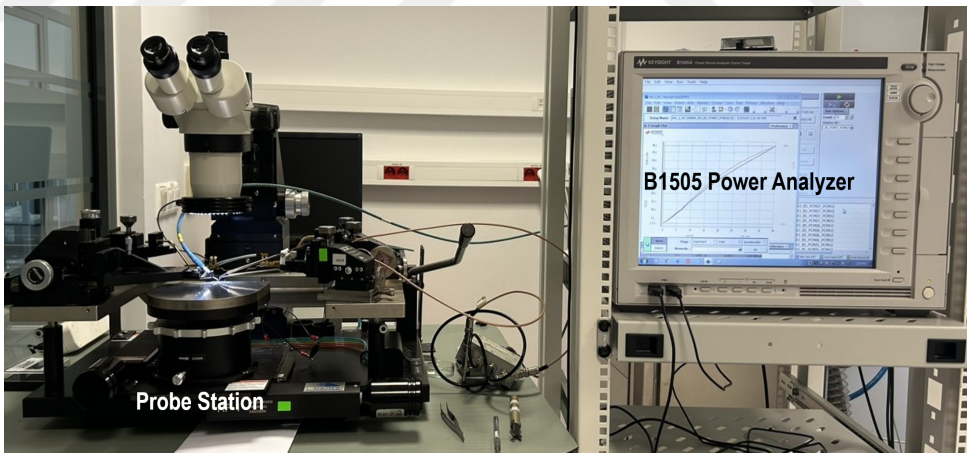


Figure 2.2: DC HEMT characterization set-up with the B1505 power analyzer.

The $I_d - V_d$ curves of an active device are important because they give a good idea of the optimum Q-point of the device for the specific application. The measurement is performed by fixing the gate voltage and sweeping the drain voltage from 0 V to 10 V. The measurement is repeated as the gate voltage is changed from -4 V to $+2$ V in steps of 1 V to obtain the $I_d - V_d$ plots. For a high-power design, the device may be biased at a higher drain current, while for a high-efficiency design, it may be biased at a lower drain current. The knee voltage, which differentiates the current saturation region from the triode region,

is an important parameter for power amplifier designs because it indicates the lower end of the voltage swing. This measurement also indicates the maximum current handling of the device, quantified by saturated drain current, I_{dss}. The $I_d - V_d$ curves for a typical 4×75 μm device are given in Figure 2.3. The maximum drain current at 2 V gate-to-source voltage is about 312 mA, which, when normalized by the periphery, corresponds to about 1040 mA/mm. The knee voltage is determined as 3.7 V.

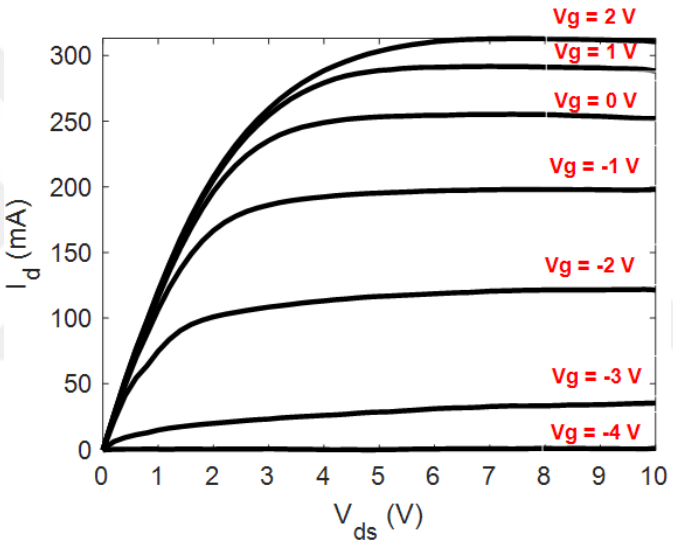


Figure 2.3: $I_{ds} - V_{ds}$ curves of a typical 4×75 μm device. The gate voltages are swept from -4 V (lower) to +2 V (upper) in steps of 1 V.

The $I_d - V_{gs}$ curve for the same HEMT is plotted in Figure 2.4. This time, the drain voltage is fixed at 10 V and the gate voltage is swept from -6 V to 1 V. The increase in the drain current can help identify the threshold voltage. The transconductance or the g_m of the device can also be determined using this measurement. The g_m of a device is defined as [26]:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{2.1}$$

Therefore, the slope of the $I_d - V_{gs}$ is the g_m of the device. The transconductance peak is measured as 88 mS at about -2.5 V_{gs}. The normalized transconductance is approximately 293 mS/mm.

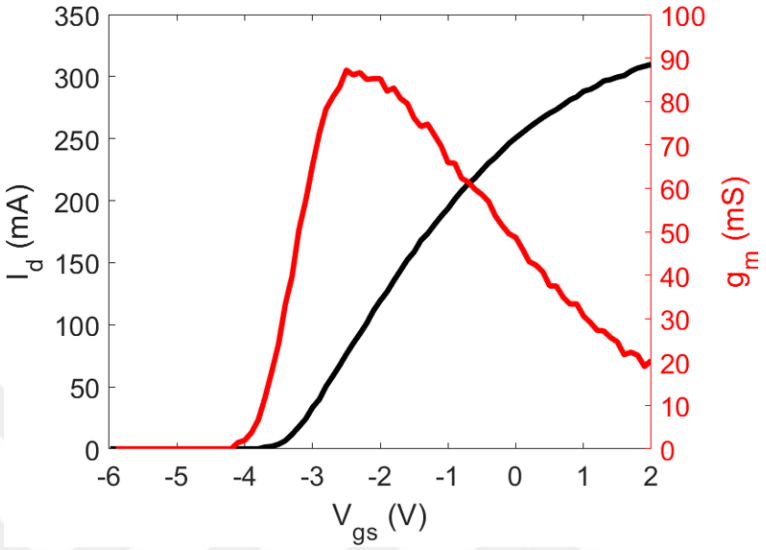


Figure 2.4: $I_{ds} - V_{gs}$ (black) measurement for a typical 4×75 μm device. The transconductance (g_m) is plotted in red.

The drain and gate leakage currents are determined using the break-down voltage measurements. The device is held under pinch off, at -8 V V_{gs} as the drain voltage is swept from 0 V to 40 V. The leakage currents tend to increase with the increase in drain voltage as shown in Figure 2.5. The maximum gate leakage observed was 1.55 μA and the maximum drain leakage observed was 1.40 μA.

2.3 Small Signal Measurements

The small-signal measurements are performed using a network analyzer, ZVA-40 from Rhode & Schwarz. A pair of high-quality RF probes and RF cables are used. DC cables are connected with the help of bias tees to bias the device. The HEMT measurements are performed on-wafer which is placed on a chuck whose temperature can be controlled. Figure 2.6 shows the setup used to measure the HEMTs.

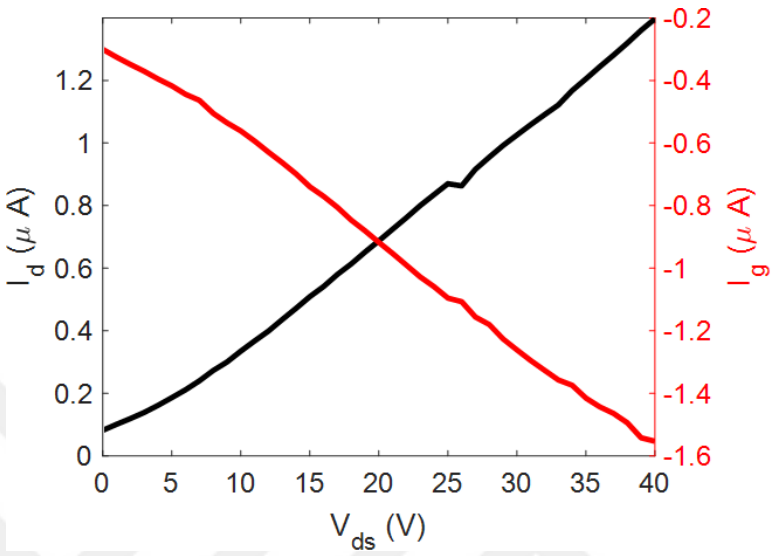


Figure 2.5: Sub-threshold gate (red) and drain (black) current leakages.

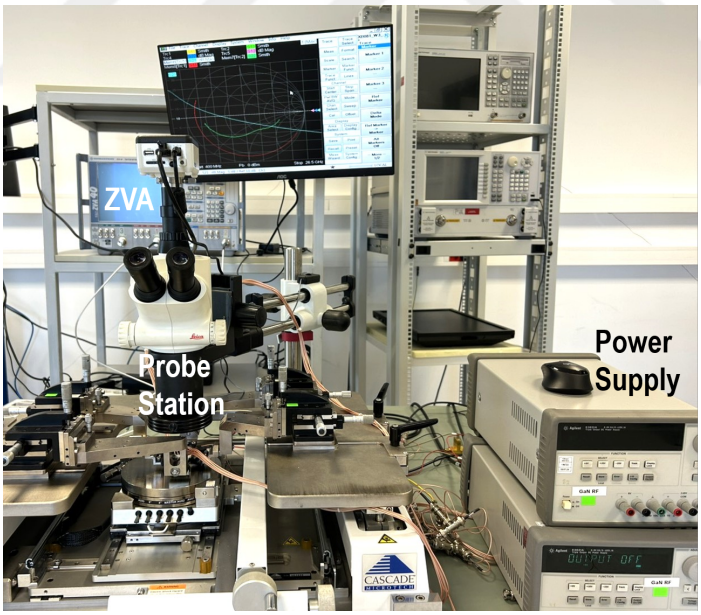


Figure 2.6: Small-signal measurement set up with ZVA-40.

After performing the calibration using a calibration standard, the wafer is placed on the chuck with an air vacuum pump underneath. The HEMTs are biased at 100 mA/mm and 28 V drain voltage under continuous wave (CW) conditions using external power supplies. A low-power signal is applied to ensure that the device is operating under a small-signal regime. The frequency of the

applied power is swept across the frequency range of interest. The ZVA is capable of measuring the resulting S-parameters of the device under that Q-point.

In high-frequency circuits, it is important to understand the measurements using ideas of reflected and transmitted waves instead of measuring the equivalent voltages and currents. Moreover, the measurement of Z– or Y– parameters of active devices are more difficult because an active device may be unstable when one of the ports is open- or short-circuited. For this purpose, the S-parameters are used, which relate the power of the incident waves to the power of the reflected waves at all ports of a network.

The incident and reflected waves for a two-port network can be represented using a set of variables a_1, b_1, a_2, and b_2 as shown in Figure 2.7.

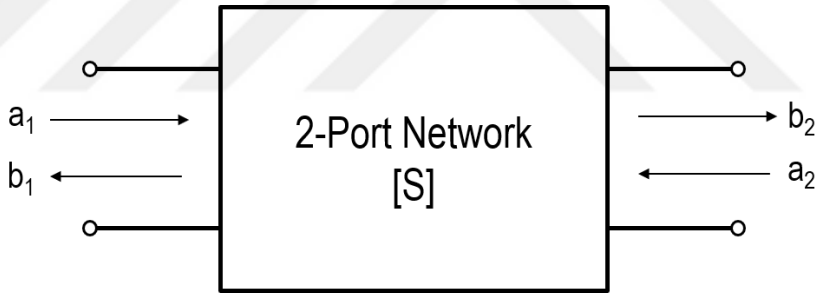


Figure 2.7: 2-port network and respective incident and reflective waves.

The incident and the reflected waves are defined as follows [27]:

$$a \triangleq \frac{1}{2}\left(\frac{V}{\sqrt{Z_0}} + I\sqrt{Z_0}\right) \tag{2.2}$$

$$b \triangleq \frac{1}{2}\left(\frac{V}{\sqrt{Z_0}} - I\sqrt{Z_0}\right) \tag{2.3}$$

Where Z_0 is the characteristic impedance of the system.

The scattering parameters are defined as functions of these incident and reflective waves and are given by the following expressions:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \quad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \quad S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \quad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{2.4}$$

Where S_{11} and S_{22} are the reflection coefficients seen at port 1 and at port 2, respectively, when all other ports are terminated in matched load. S_{12} and S_{21} are the transmission coefficients from port 2 to port 1 and from port 1 to port 2, respectively, when all other ports are terminated in matched loads. Therefore, to perform such S-parameter measurements, it is essential to ensure that all ports are terminated in matched loads [27]. The S-parameters can be visualized graphically using a Smith Chart. The S-parameter characterization of a typical 8×100 μm device is shown in Figure 2.8.

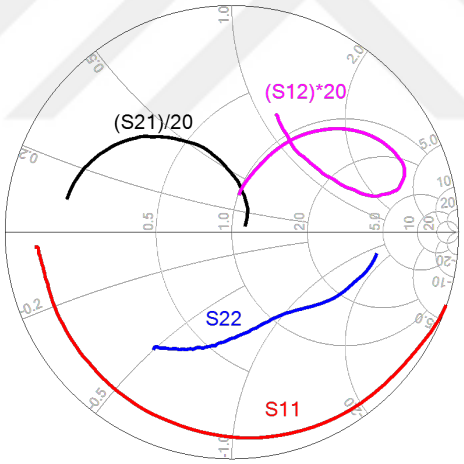


Figure 2.8: Measured S-parameters of a typical 8×100 μm device for a frequency range of 0.4 GHz to 20.0 GHz.

Since the S_{21} can be thought of as the inherent gain of the transistor when it is terminated with the characteristic impedance, it is worthwhile to observe it in dB scale as well. This is shown in Figure 2.9

Any two-port network can be characterized using the S-parameters by terminating the network with the characteristic impedances. This gives us 4 parameters for a two-port network: S_{11}, S_{12}, S_{21}, and, S_{22}. The S-parameters of active two-port networks can be used to derive some important design parameters. When the second port is terminated with any impedance other than the characteristic

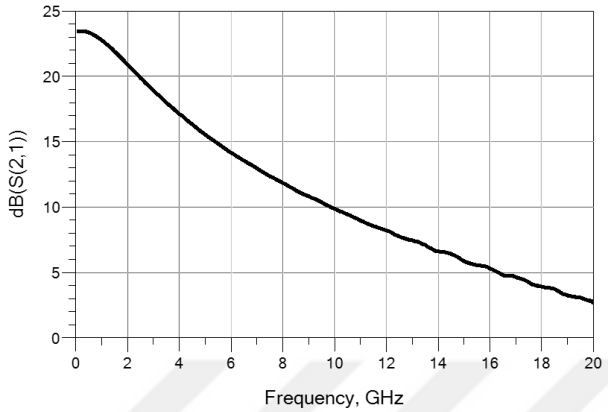


Figure 2.9: Measured S_{21} of a typical $8 \times 100\ \mu m$ device in dB scale or a frequency range of 0.4 GHz to 20.0 GHz.

impedance, the input reflection coefficient is modified as follows [27]:

$$\Gamma_{in} = S'_{11} = S_{11} + \frac{S_{21}\Gamma_L S_{12}}{1 - S_{22}\Gamma_L} \tag{2.5}$$

where Γ_L is the normalized load impedance

Oscillations may occur if $|\Gamma_{in}| > 1$. The load stability circles show which load impedances or Γ_L causes $|\Gamma_{in}|$ to be greater than 1. For unconditional stability, it must be certain that there are no load stability circles inside the Smith chart. Another indicator of unconditional stability is the stability factor (K) which is defined as [27]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{21}|} \tag{2.6}$$

where $|\Delta|$ is given as:

$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| \tag{2.7}$$

If the K factor is greater than 1, it is certain that the device is unconditionally stable. This means that it can be terminated with any impedance without the risk of oscillations.

The maximum available gain (MAG) represents the small signal gain that can be attained if the device is perfectly matched to the conjugates of its input and

output impedance at the gate and drain sides, respectively. The MAG is defined as shown in equation 2.8 [27].

$$MAG = \begin{cases} \frac{|S21|}{|S12|}(K - \sqrt{K^2 - 1}), & \text{if } K > 1 \\ \frac{|S21|}{|S12|}, & \text{if } K \leq 1 \end{cases} \tag{2.8}$$

The MAG and the stability factor for a typical $8 \times 100\ \mu m$ device are shown together in Figure 2.10. Smaller periphery devices tend to have a higher MAG compared to larger periphery devices. This is because larger periphery transistors have more parasitic capacitance, which limits their gain, and hence the operation frequency.

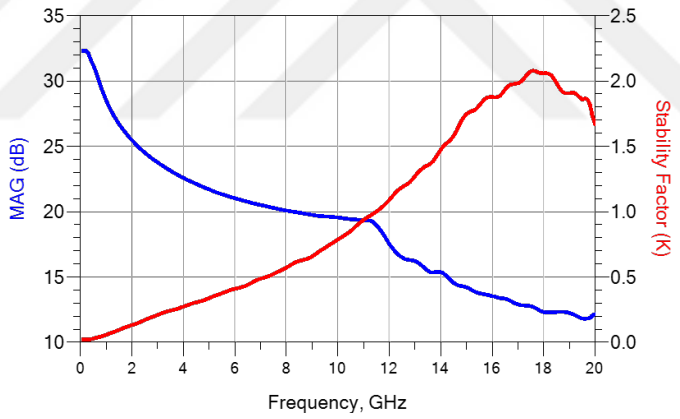


Figure 2.10: MAG (blue) and K-factor (red) for a typical $8 \times 100\ \mu m$ device

The MAG plot has a distinguishable notch that is an indicator of unconditional stability. With close inspection, it can be observed that this notch occurs when the stability factor transitions to a value greater than 1. In fact, before the notch the MAG is determined by assuming that the stability factor is equal to 1. This means that it actually represents the maximum stable gain (MSG) at those frequencies.

2.4 Large Signal Measurements

Under high-power operation, the active devices' gain compresses, and the input and output impedance of the device change. For this reason, the maximum output power (P_{out}) impedance is different from that of the transducer gain (G_T) or the operating gain (G_P). The impedance for maximum power-added efficiency (PAE) also deviates. The G_T, G_P, and PAE are defined as follows:

$$G_T = \frac{\text{Power delivered to the load}}{\text{Power available from source}} \tag{2.9}$$

$$G_P = \frac{\text{Power delivered to the load}}{\text{Power input to the network}} \tag{2.10}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \times 100 \tag{2.11}$$

Since the amplifier will operate in the non-linear region with relatively high input powers, the large-signal characterization of HEMTs is important. For this purpose, a passive vector-based load-pull set-up is done. The set-up sketch is shown in Figure 2.11 and the actual set-up photograph used to perform these measurements is shown in Figure 2.12. The setup is used with AMCAD Engineering's IVCAD software to perform the measurements.

A power amplifier is used to drive the device-under-test (DUT) because the PNA-X itself is not capable of generating such large input powers. The measurement is performed under pulsed conditions with a duty cycle of 10 %. For this reason, a pulser connected to the PNA-X is used to bias the DUT. A mechanical load tuner is used to change the load impedance every time a measurement is performed. A source tuner is used to present a fixed source impedance, preferably closer to the conjugate of the input impedance. The measurement is performed by sweeping the input power starting from powers as low as small-signal and increasing them until the device's gain compresses by about 6 dB. The pulser records the

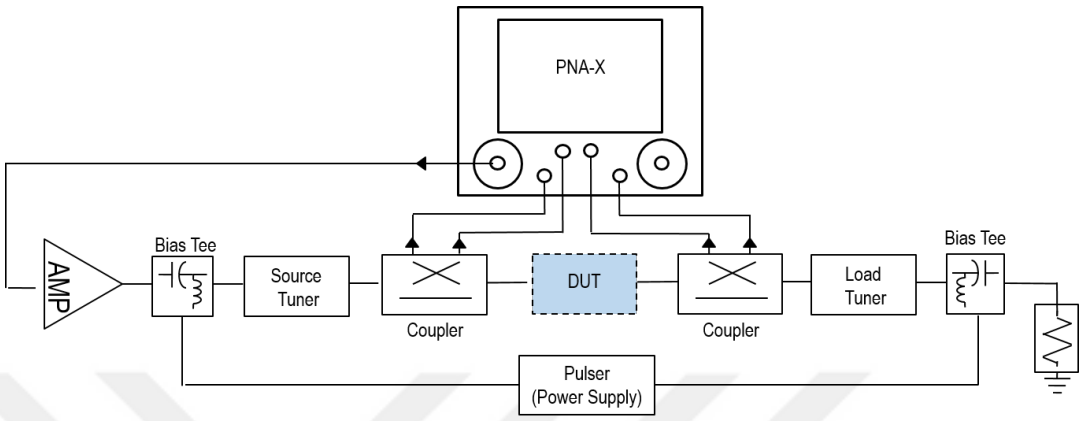


Figure 2.11: Passive VNA-based load pull set up sketch

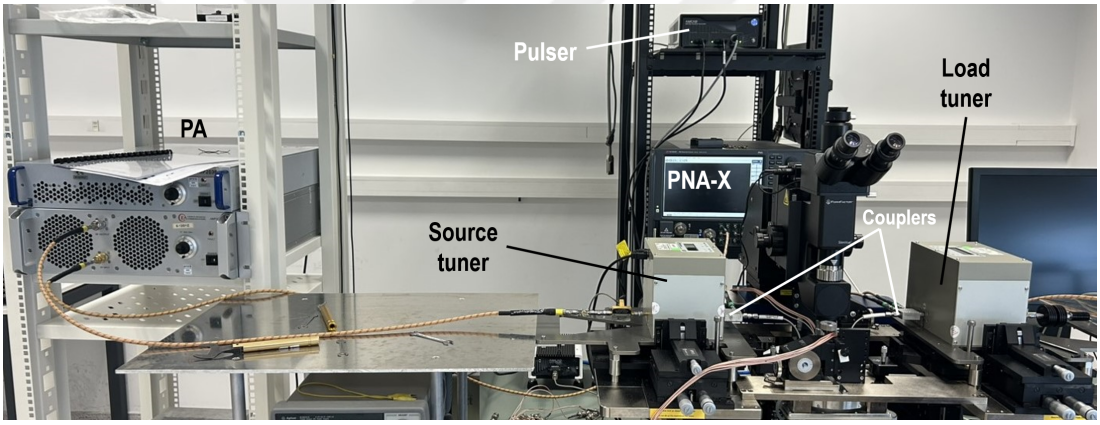
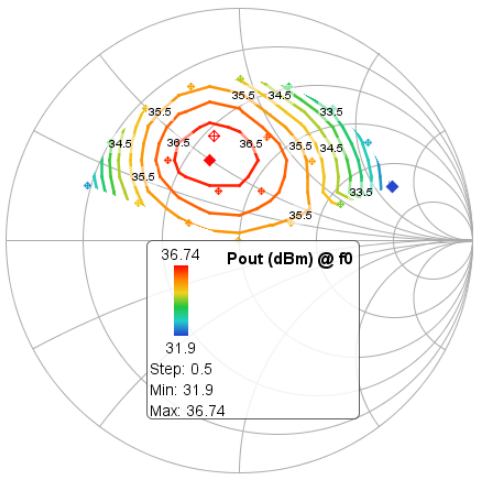


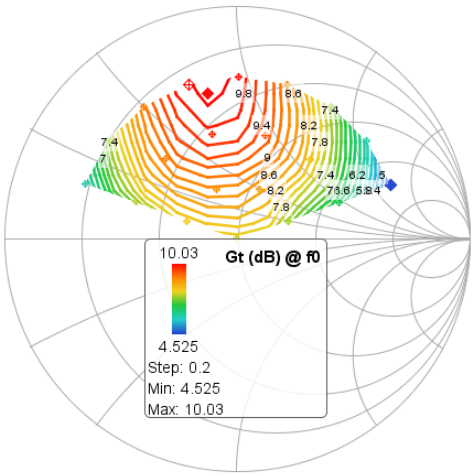
Figure 2.12: Actual load-pull set up with tuners for large-signal HEMT characterization.

drain and gate currents simultaneously to determine PAE and other parameters. This is repeated for a set of load impedance points to obtain the load-pull contours. The load-pull contours for a typical $8 \times 100\ \mu m$ device are shown in Figure 2.13. These contours give the designer insight related to the maximum achievable performance and also about the trade-offs between the large-signal parameters.

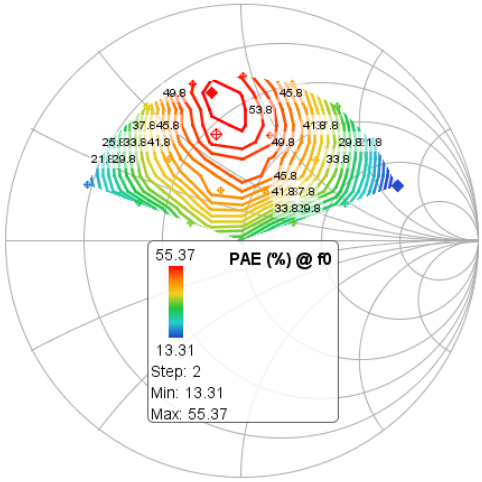
The source-pull was not performed because AMCAD's IVCAD software has a built-in source-pull utility program.



(a) P_{out} contours.



(b) G_T contours.



(c) PAE contours.

Figure 2.13: Load-pull contours of a typical 8×100 μm um device at 10 GHz and 6 dB gain compression. The measurements were performed at 80 °C with a 10 % Duty cycle.

Chapter 3

HEMT Model Development

HEMT measurement-based design has been the traditional method for developing an MMIC. This means that HEMT small-signal and large-signal characterizations are performed at the desired bias point before starting a design. Among these measurements, the most suitable HEMTs, according to the design specification are selected. For a small-signal design, an s2p file containing the HEMT small signal measurement data is imported into the design environment. The passive matching networks are then designed around this measurement-based file. The large signal measurements are used to identify the optimum power, gain, or PAE impedance points, and manual examination is required to estimate the non-linear performance of the HEMT.

Although these conventional techniques are very accurate, they limit the range of options available to a designer in terms of HEMT peripheries that can be used. The designer can only use the HEMTs for which the measurement is available. Moreover, this method is time-consuming because a complete fabrication cycle is required and the characterization is a lengthy procedure. Therefore, to improve a PDK's flexibility and to reduce the time and cost of a design cycle, it is desired to have scalable active device models.

3.1 Cold-FET Extrinsic Parasitic Extraction Technique

There are various equivalent circuit transistor models available in the literature [28, 29, 30]. The accuracy of a model increases with its complexity. A robust and well-established FET model is shown in Figure 3.1 which represents the lumped components of which the model is comprised of [1]. The components enclosed inside the dashed box represent the intrinsic device components which are bias-dependent i.e. their values are subject to change as the gate or drain voltage of a device changes. Other components: L_g, R_g, L_d, R_d, L_s, R_s, C_{pg} and C_{pd} are the extrinsic parasitic components. These extrinsic parasitic parameters (EPP) are bias-independent and mainly depend on the physical structure of the device [31].

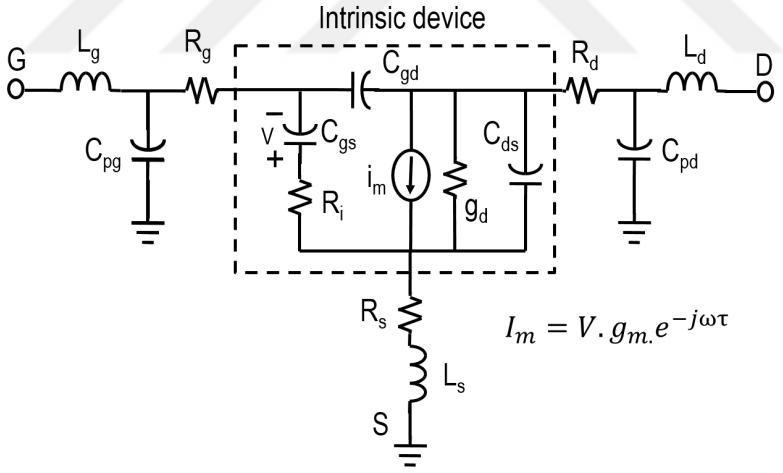


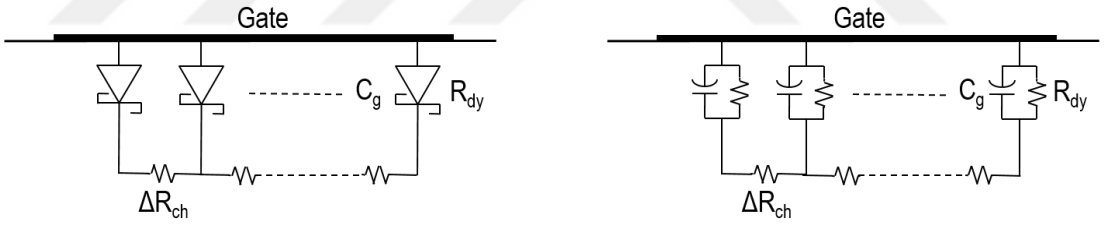
Figure 3.1: Small signal equivalent circuit proposed by Dambrine et al [1].

Conventionally, the model parameters are determined by optimizing the parameter values until a good S-parameter match is achieved between the model and the actual device measurement [32]. However, such an approach can lead to non-physical model parameters and can also converge to a local minimum with a significantly high error. Therefore, in order to obtain accurate and realistic values, a direct extraction method is preferred. If a good realistic value is extracted directly, it can be used as a starting value for optimization and eventually obtaining accurate models.

The EPPs are preferred to be extracted under cold-FET bias conditions where the drain-to-source voltage is kept at zero. This significantly simplifies the intrinsic circuitry and helps easily extract the extrinsic parameters using a few measurements [33]. Under the cold-FET condition, the intrinsic part beneath the gate can be modeled by the given equivalent circuit in Figure 3.2. Due to a metal-semiconductor (MS) contact region at the gate, the gate can be modeled as distributed MS Schottky diodes comprising parallel RC networks. The channel underneath can also be modeled using a distributed channel resistance R_{ch} [34]. The R_{dy} for an MS Schottky contact is given by [1]:

$$R_{dy} = \frac{nkT}{qI_g}$$

where n is the ideality factor, k the Boltzmann constant, T the temperature, and I_g the gate current.



(a) Distributed Schottky diodes. (b) Schottky diode equivalent circuit.

Figure 3.2: Equivalent open-channel intrinsic circuit under cold-FET bias conditions.

If the gate is not forward-biased, there is negligible current, and R_{dy} is very high. Therefore, the region under the gate can be modeled using a distributed network of gate capacitance only. From the literature, in the channel on-state, the resistance due to the channel when looking from the gate is $R_{ch}/3$ [35]. It is also assumed that C_{gd} and C_{ds} are negligible in comparison to C_{gs} and that the C_{pg} is interchangeable with L_g. Therefore, the simplified small-signal model under cold-FET conditions used is shown in Figure 3.3.

The equivalent input circuit is as shown in Figure 3.4. The C_{gs} is the combination of different parasitic capacitance sources. These are due to the fringing

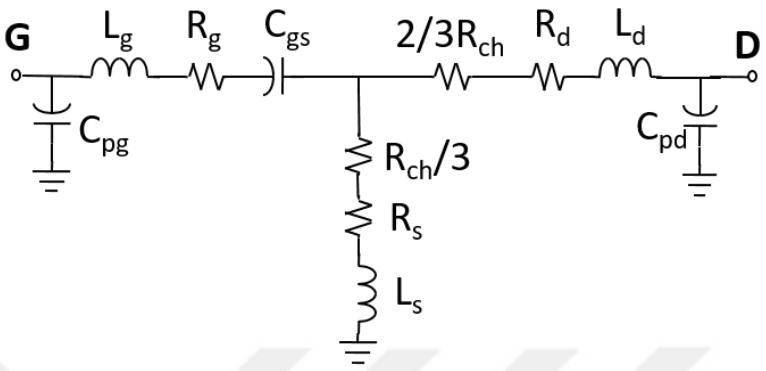


Figure 3.3: Simplified small signal model under cold-FET bias conditions.

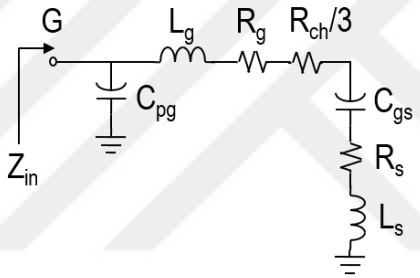


Figure 3.4: Small signal equivalent input circuit under cold-FET bias conditions

capacitance between the gate finger and the source electrodes, the parallel capacitance between the gate and the 2DEG underneath, and the capacitance due to the close proximity of the gate structure to the source-connected field plates.

The equivalent output impedance circuit is shown in Figure 3.5. Here, the fringing capacitance between the gate and the drain structures is considered negligible.

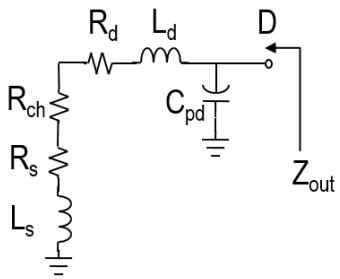


Figure 3.5: Small signal equivalent output circuit under cold-FET bias conditions

Thus, using the Cold FET technique and some reasonable assumptions, the

equivalent circuits become relatively simple. With the help of some EM simulations and some circuit analysis the EPPs can be extracted.

3.2 Custom EM-Substrate Development

ADS from Keysight was used to perform momentum simulations to extract the EPPs. Even though the momentum simulations are meant for simulating passive components only, a detailed and custom EM substrate is needed to EM simulate the different structures of an active device. A reference HEMT with a gate periphery of 6x100 μm is used for these simulations. The layout of the device is broken down into smaller and simpler pieces to easily associate a specific EPP to an EM response.

Since direct EPPs will be extracted, a very detailed EM-stack is sought after so as to obtain accurate and meaningful values. For this reason, a more detailed epitaxial structure is defined in comparison to the one used for design purposes. A 98 μm SiC carrier substrate is defined. The Fe-doped GaN buffer layer and the transition GaN layer are defined together by a single GaN substrate layer of 1.9 μm. A mesa GaN layer of 77 nm and an AlGaN layer of 23 nm is then defined to correctly mimic the actual epitaxial structure. The 2DEG is defined using the "Channel" layer whose material properties are defined as a 3 nm conductor with known conductivity. All of the substrate layers that are defined on top of the AlGaN substrate layers are defined as SiN. More than 3 SiN layers had to be defined to cater to the extruding conductor layers of varying thicknesses. The defined EM-substrate's epitaxial structure is shown in Figure 3.6.

Since the maximum thickness of a conductor is limited by the thickness of the respective defined substrate layer in ADS, some conductors had to be distributed across multiple substrate layers. A connection between these layers was facilitated with the help of a conductor via which is defined with the same material properties as the conductor itself. The gate foot, gate head, MET1, MET2, and field plate layers are all defined using such a method. The derived layer option was used

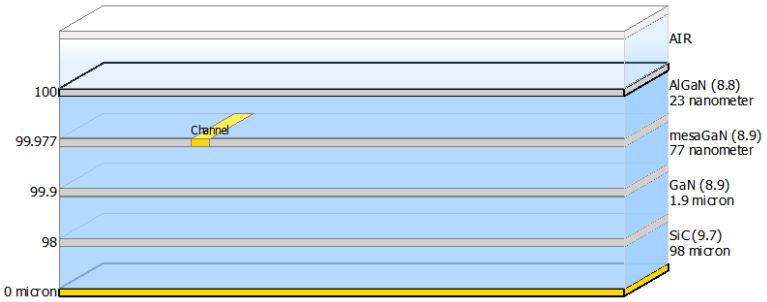


Figure 3.6: The epitaxial structure defined in the EM-Substrate

to keep the layout as simple as possible so that all of the defined layers in the substrate do not need to be drawn or assigned individually in the layout drawing. The definition of the conductors distributed among different layers is shown in Figure 3.7. The complete custom EM-substrate defined in ADS is shown in Figure 3.8.

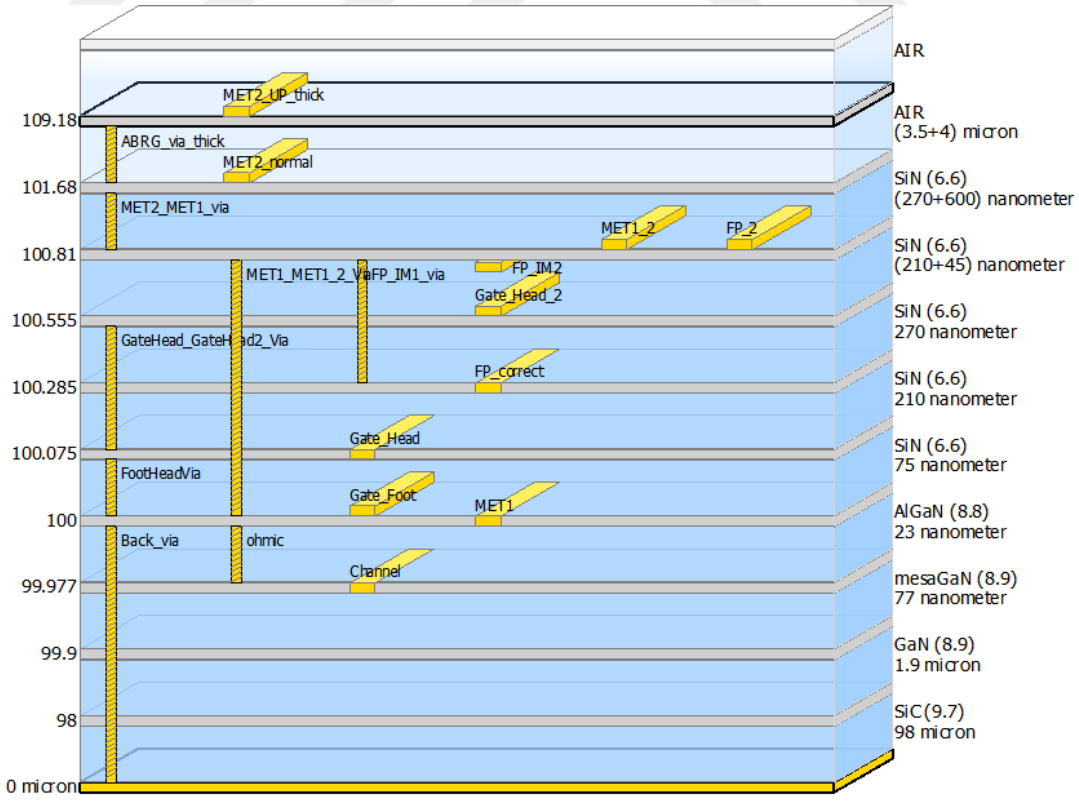
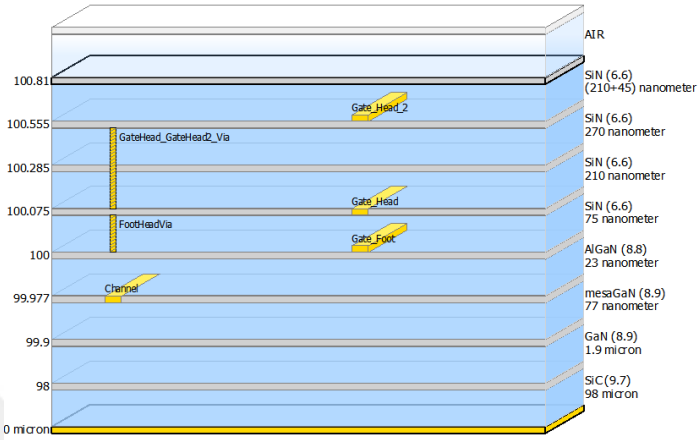
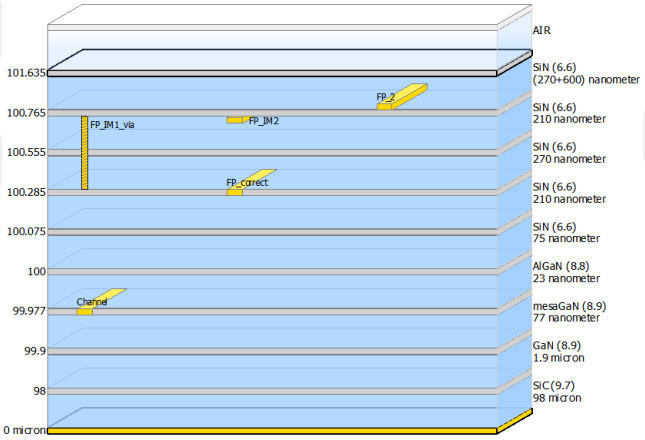


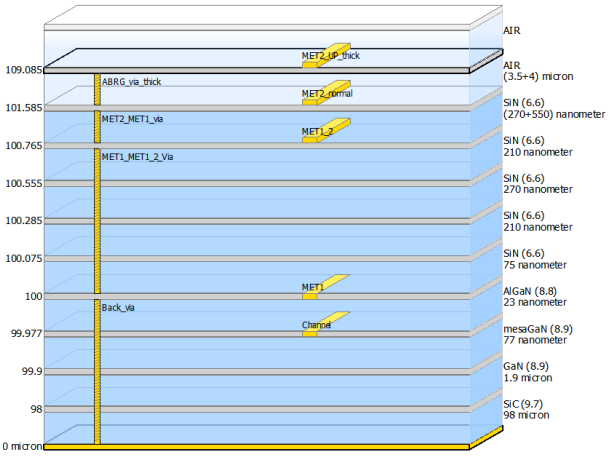
Figure 3.8: The complete custom EM-substrate defined in ADS used for EPP extractions.



(a) Gate foot and gate head



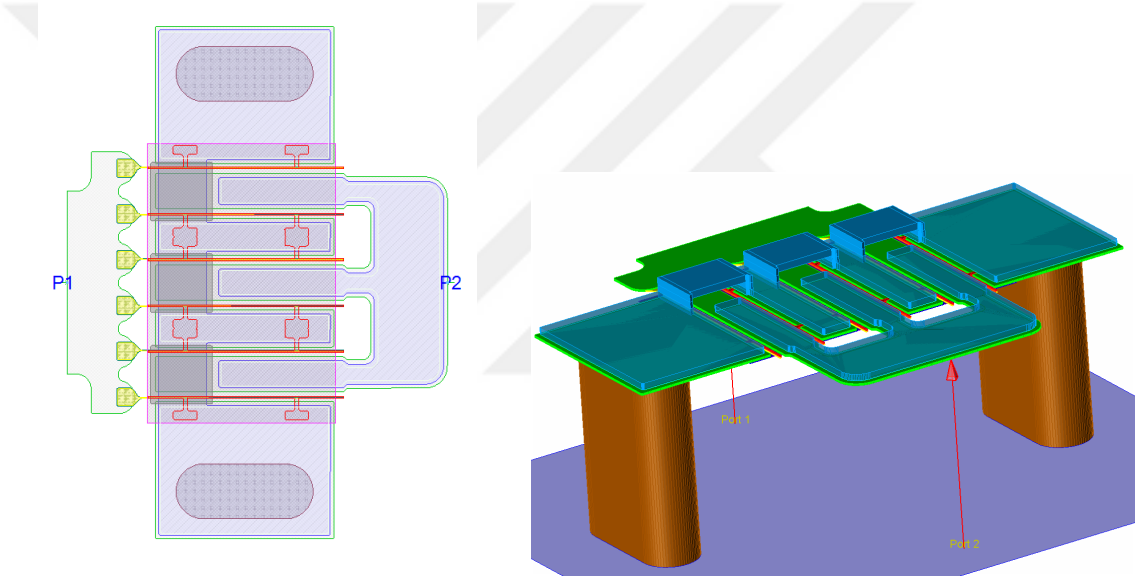
(b) Source-connected field plates



(c) MET1, MET2, air bridge and back-via

Figure 3.7: Substrate definition of various conducting structures.

A $6 \times 100\ \mu m$ HEMT structure was drawn in the layout and the defined layers were assigned to the drawings accordingly. The layer definition file automatically draws the derived layers depending on the source layers and their respective boolean functions. The layout drawing and its corresponding 3D EM preview structure generated by the EM set-up pre-processing are shown in Figure 3.9. The 3D preview is important for verifying the correct structure of the device. All of the dimensions of the structure can be measured in all 3 axes.

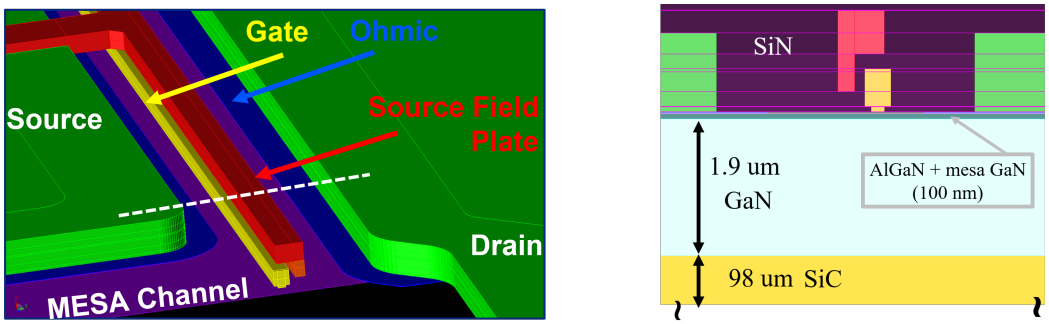


(a) Layout drawing. (b) Corresponding 3D preview.

Figure 3.9: Layout drawing and its correspondin 3D EM preview of a standard $6 \times 100\ \mu m$ HEMT using the substrate in Figure 3.8.

A close-up 3D preview of one of the fingers of the HEMT and its corresponding cross-section is shown in Figure 3.10. Some of the layers e.g. MET2 have been intentionally deleted for easier viewing. From this Figure, the gate structure can be seen clearly. The cross-section view allows us to observe the substrate dielectric thicknesses. The dimensions of the field plate, which is placed near the gate, can also be checked. The dimensions and separations are ensured that they correctly represent the real structure of a HEMT as closely as possible.

In order to validate the EM-stack, EM simulations of the reference HEMT were performed at 2 frequencies: 0.4 GHz and 10 GHz, in 2 different states: with the channel and without the channel. The EM-simulations were only performed



(a) (b)

Figure 3.10: Zoomed-in 3D preview of a single finger of a $6 \times 100\ \mu m$ HEMT (a) and its corresponding cross-section (b).

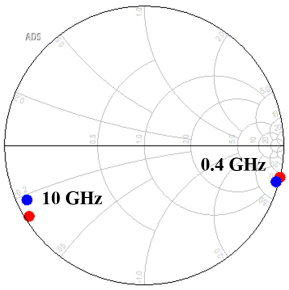
at 2 frequency points because of the long simulation durations due to the complex substrate structure. 2 HEMTs were fabricated, one with the MESA i.e. 2DEG present, and the other without the MESA layer i.e. without the 2DEG. The HEMTs were measured under cold-FET bias conditions and were compared with the response of the simulations. This comparison is shown in Figure 3.11.

3.3 Extrinsic Parasitic Parameter Extraction

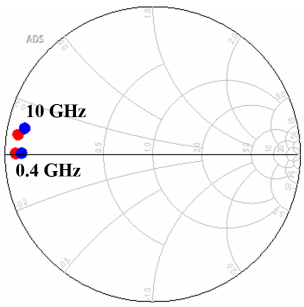
Using the simple equivalent circuits derived under cold-FET conditions in section 3.1 and with the help of EM simulations using the substrate developed in section 3.2, the EPPs can be extracted directly.

Since the C_{pg} and C_{pd} defined in Figure 3.1, are due to the gate and drain manifold capacitance to the ground respectively, one-port EM simulations of just the drain and gate manifolds in separate layouts can be performed to extract them. The gate and drain manifolds that were EM-simulated to extract C_{pg} and C_{pd} are shown in Figure 3.12. From these simulations C_{pg} was determined as 18 fF and C_{pd} as 27 fF.

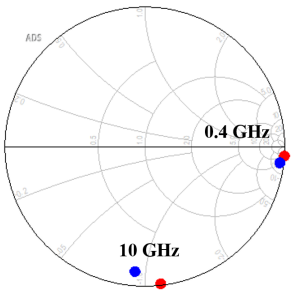
By de-embedding the response of C_{pg} and C_{pd} from Figure 3.4 and Figure 3.5, respectively, these circuits are modified as shown in Figure 3.13. From these



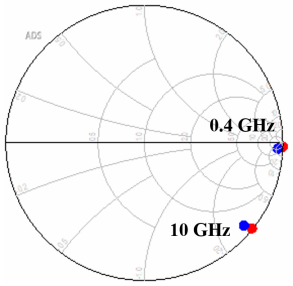
(a) Z_{11} with the channel



(b) Z_{22} with the channel



(c) Z_{11} without the channel



(d) Z_{22} without the channel

Figure 3.11: EM substrate validations performed at with the channel ((a) and (b)) and without the channel ((c) and (d)). Red are simulations while blue are measurements.

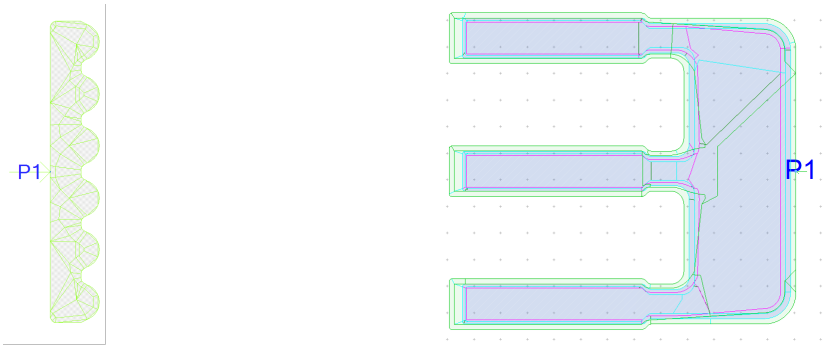
equivalent circuits, the following simple relations can be determined:

$$Z'_{in} = Z'_{11} = R_g + \frac{R_{ch}}{3} + R_s + j\omega(L_g + L_s - \frac{1}{\omega^2 C_{gs}}) \tag{3.1}$$

$$Z'_{out} = Z'_{22} = R_d + R_{ch} + R_s + j\omega(L_d + L_s) \tag{3.2}$$

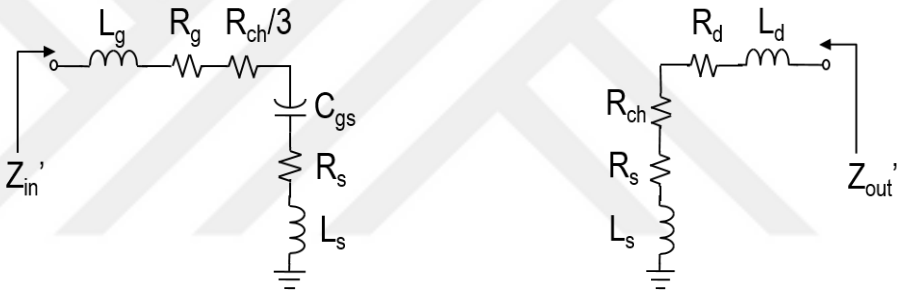
$$Z'_{21} = Z'_{12} = R_s + \frac{R_{ch}}{3} + j\omega L_s \tag{3.3}$$

At sufficiently low frequencies, the effect of the reactance due to L_g and L_s is negligible compared to the reactance due to C_{gs}. Hence, C_{gs} can be extracted from the imaginary part of Z'_{in} at low frequency. The equivalent circuit at low frequency is shown in Figure 3.14. Performing the EM-Simulation at 300 MHz, the value of C_{gs}, extracted from the imaginary part of Z'_{11} is 907 fF. This value for C_{gs} is then used in equation 3.1 to extract $L_g + L_s$ at 10 GHz when the effect of the inductance due to $L_g + L_s$ is significant. The sum $L_g + L_s$ was found as



(a) Gate manifold layout. (b) Drain manifold layout.

Figure 3.12: Gate (a) and Drain (b) manifold layouts of the reference device.



(a) Equivalent input circuit. (b) Equivalent output circuit

Figure 3.13: Equivalent input (a) and output (b) circuits with C_{pg} and C_{pd} de-embedded respectively

58.13 pH. The real part of Z'_{11} is used to identify the sum $R_g + R_s + R_{ch}/3$ which is equal to 0.90 Ω.

Similarly, using equation 3.2, the sum $L_d + L_s$ is found as 74.27 pH and the sum of $R_d + R_{ch} + R_s$ is 1.72 Ω. Equation 3.3 is used to find R_s equal to 0.07 Ω and L_s equal to 31.88 pH. There are now 3 equations but 4 unknown resistances. Since the material properties of the channel are known, the channel resistance can be calculated easily. The MESA layer has a resistance of 320 Ω/□. For a device with a gate width of 100 μm and a drain-to-source distance of 3 μm, this is equivalent to 9.6 Ω. Since we have 6 such resistances in parallel, R_{ch} is determined equal to 1.6 Ω. With R_{ch} known, simple algebra can be used to determine all of the EPPs. Figure 3.15 shows the extracted EPPs for a standard 6×100 μm device.

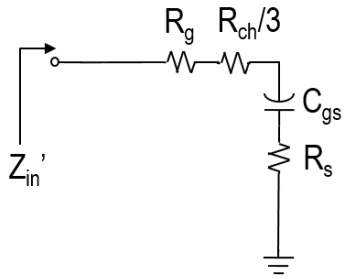


Figure 3.14: Equivalent input circuit with C_{pg} de-embedded at low frequency.

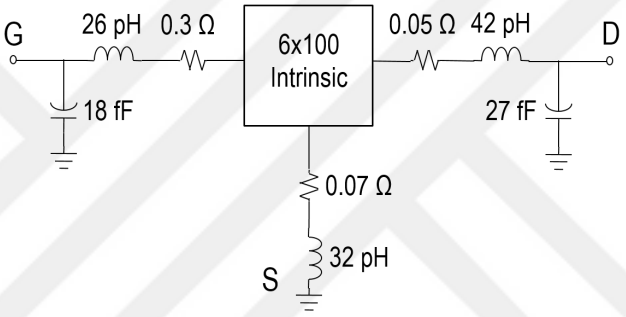


Figure 3.15: Extracted EPPs for a typical 6×100 μm device.

3.4 Extrinsic Parasitic Parameter Scaling

A model is more useful when it can be accurately scaled up or down. This provides the designer with a large number of usable active device options, and eventually, the HEMT periphery can also be used as a tuning parameter of the circuit. Since the EPPs depend solely on the device geometry, any changes in the layout can make the EPPs susceptible to change. Two main parameters define the change in layout, namely: Number of Fingers (NoF), and the Gate Width (W_g). The total periphery is the product of these two parameters. Increasing W_g scales up the device in the x-axis, while increasing the NoF scales up the device in the y-axis.

Since C_{pg} and C_{pd} are pad capacitances to the bulk ground, they must scale with the change of area of the pads. The gate pad area is not a function of W_g but increases linearly with the increase in the NoF. After performing several one-port EM simulations of the gate manifold, a fitting equation in terms of NoF was developed to model C_{pg}. The equation is given as follows:

$$C_{pg} = (\alpha_0 H_0 + \alpha_1 H_n(\frac{NoF}{2} - 1)) \times L \times C \tag{3.4}$$

Where H_0 is the height of the gate manifold of a base 2-finger device, H_n is the change in the height of the gate manifold with increasing NoF, L is the fixed length of the gate manifold and C is the capacitance density between the metal layer and the bulk. α_0 and α_1 are correction factors catering to the fringing capacitance effects. The simulated gate pad capacitance and the modeled capacitance are shown in Figure 3.16.

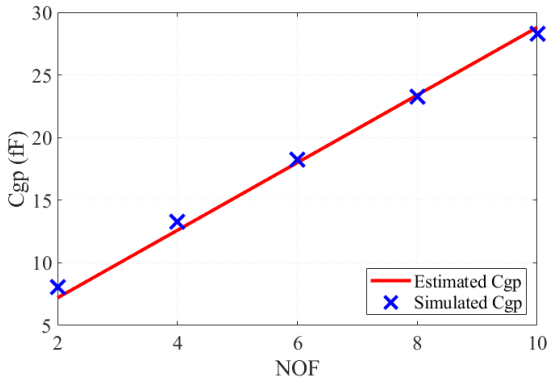


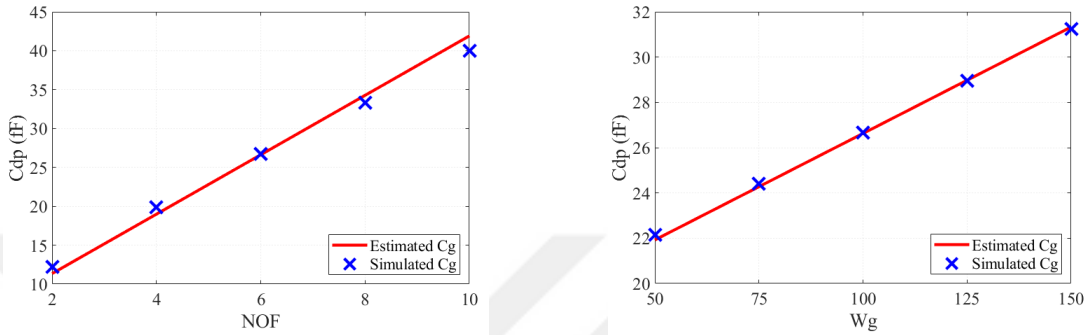
Figure 3.16: EM simulated (blue cross) and modeled (red line) gate parasitic capacitance for fixed W_g of 100 um.

Similarly, the drain parasitic capacitance was modeled. The drain capacitance, in addition to NoF, is also a function of W_g. The equation governing the scalability of the drain parasitic capacitance is given as:

$$C_{pd} = \left[\left(\alpha_0 H_{0m} + \alpha_1 H_n(\frac{NoF}{2} - 1) \times L_m\right) + \left(\alpha_F \frac{NoF}{2} \frac{W_g}{2} \times H_F\right)\right] \times C \tag{3.5}$$

Where H_F is the height of one of the drain fingers, H_{0m} is the height of the drain manifold of a base 2-finger device, H_n is the change in the height of the drain manifold, L_m is the fixed length of the power combining part of the drain manifold and C is the capacitance density. α_0, α_1 and α_F are correction factors

to accommodate the fringing effects. The simulated drain and modeled drain parasitic capacitance as a function of NoF and W_g are shown in Figure 3.17.



(a) Against NoF for 100 um W_g. (b) Against W_g for 6 NoF.

Figure 3.17: EM simulated (blue cross) and modeled (red line) gate parasitic capacitance.

The scalability for all in-between combinations of NoF and W_g is represented in Figure 3.18. It can be seen that C_{dp} is a stronger function of NoF as compared to W_g. Larger W_g although increases the size of the drain pad, the coupling among the fingers limits its effect on the overall drain-to-bulk capacitance.

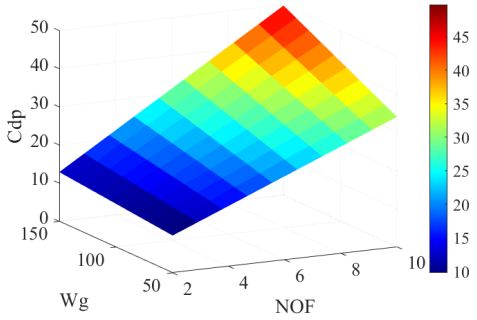


Figure 3.18: Modeled scalability of C_{pd} as a function of W_g and NoF.

The drain inductance and resistance were modeled using an equivalent circuit. The series parameters of the equivalent circuit were extracted using EM simulations at 40 GHz. To explain the equivalent circuit, a 6-finger reference device is used. As shown in Figure 3.19, the inductance (and resistance) is distributed along the drain pad fingers and the drain manifold. L_1 (and R_1) are functions of

W_g, while L_2 (and R_2) are constants independent of any layout scaling parameters.

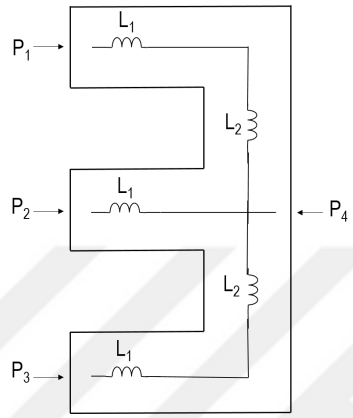


Figure 3.19: Distributed drain inductance model of a 6-finger drain pad.

When ports 2, 3, and 4 are shorted, the two-port network has an equivalent inductance and resistance given by:

$$L_{eq} = \frac{L_1^2 + L_1 L_2}{3(L_1) + L_2} \tag{3.6}$$

$$R_{eq} = \frac{R_1^2 + R_1 R_2}{3(R_1) + R_2} \tag{3.7}$$

For a generalized scalable model, the equations are modified as follows:

$$L_{eq} = \frac{L_1^2 + L_1 L_2}{\frac{NoF}{2}(L_1) + L_2} \tag{3.8}$$

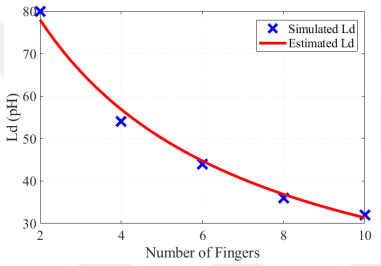
$$R_{eq} = \frac{R_1^2 + R_1 R_2}{\frac{NoF}{2}(R_1) + R_2} \tag{3.9}$$

Where L_1, and R_1 are given by:

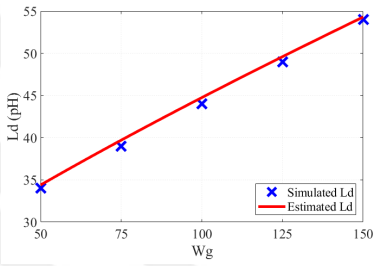
$$L_1 = \alpha_{L1} + \beta_{L1} W_g \tag{3.10}$$

$$R_1 = \alpha_{R1} + \beta_{R1} W_g \tag{3.11}$$

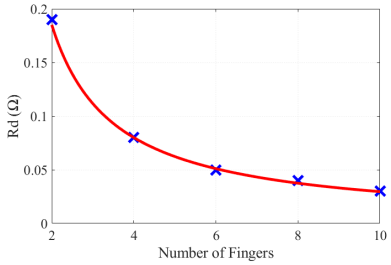
α_{L1}, β_{L1}, α_{R1}, and β_{R1} are constants aiding in fitting the model to the simulated data. The validity of the scalability of L_d and R_d for varying NoF and W_g are shown in Figure 3.20. The scalability of L_d and R_d for all of the in-between combinations of NoF and W_g are represented using 3D plots in Figure 3.21.



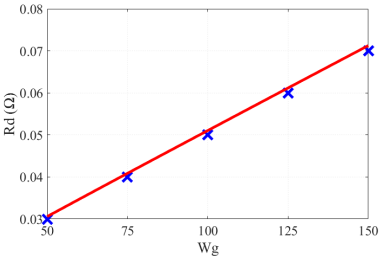
(a) L_d against NoF for 100 um W_g.



(b) L_d against W_g for 6 NoF.

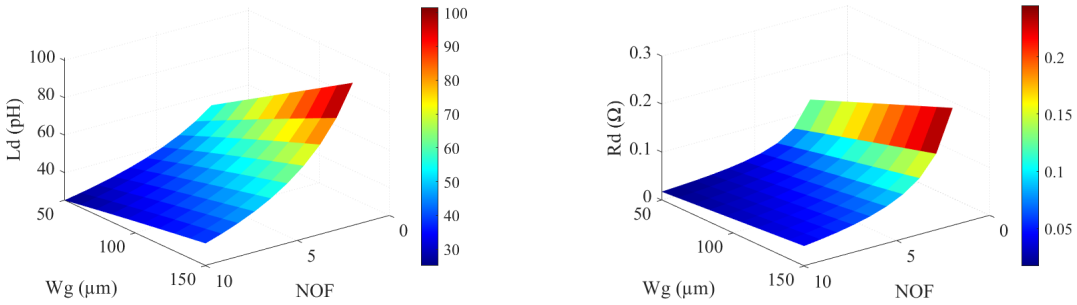


(c) R_d against NoF for 100 um W_g.



(d) R_d against W_g for 6 NOF.

Figure 3.20: EM simulated (blue cross) and modeled (red line) drain parasitic inductance and resistance.

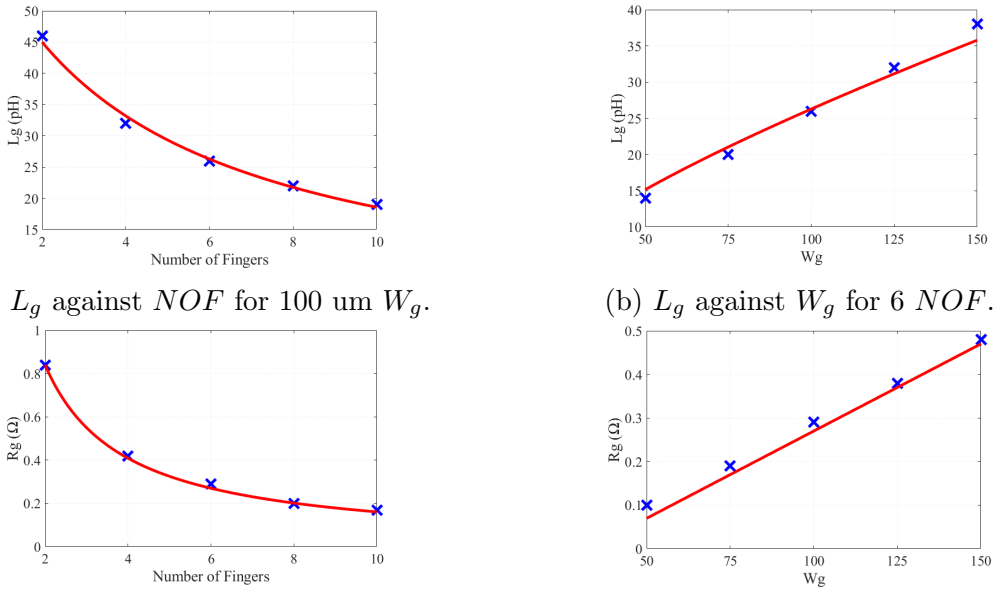


(a) Scalability of L_d.

(b) Scalability of R_d.

Figure 3.21: Modeled scalability of L_d (a) and R_d (b) as a function of W_g and NoF.

Since the gate structure is similar to that of the drain, it is also modeled using equations similar to 3.6 and 3.7. The constants α_{L1}, α_{R1}, β_{L1} and β_{R1}, are adjusted to fit the EM-simulated extracted parameter values. The scalability of the model of the gate series parasitic is shown in Figure 3.22.



(a) L_g against NOF for 100 um W_g.

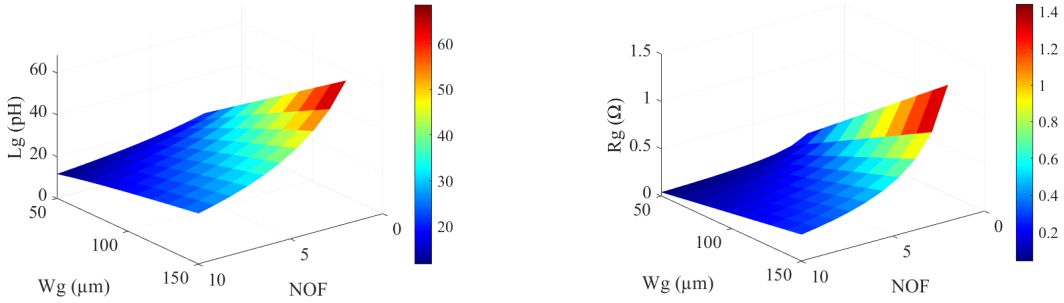
(b) L_g against W_g for 6 NOF.

(c) R_g against NOF for 100 um W_g.

(d) R_g against W_g for 6 NOF.

Figure 3.22: EM simulated (blue cross) and modeled (red line) gate parasitic inductance and resistance

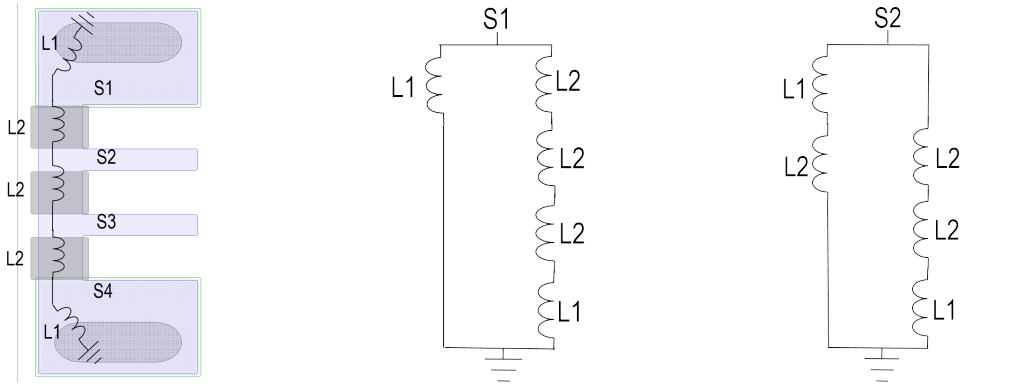
The scalability of L_g and R_g for all of the in-between combinations of NoF and W_g are represented using 3D plots in Figure 3.23.



(a) Scalability of L_g. (b) Scalability of R_g.

Figure 3.23: Modeled scalability of L_g (a) and R_g (b) as a function of W_g and NoF.

The scalability of source parasitic is done differently compared to the series components of the drain or the gate. This is because all of the source pads are connected in series via the air-bridge structures, each of them contributing additional inductance. Since the position of some of the source pads is closer to the back-via as compared to the others, they see less parasitic inductance or resistance compared to the ones that are closer to the center of the device. To better explain, this is illustrated with the help of equivalent circuits for a standard 6-finger device in Figure 3.24.



(a) Scalability of L_s. (b) S1 equivalent circuit. (c) S2 equivalent circuit.

Figure 3.24: Representation of L_s contribution due to the device layout (a). Equivalent circuits for source node 1 (b) and source node 2 (c).

There are two major sources of inductance (and resistance) inherent to the source structure. L1 is the inductance due to the back-via while L2 is the inductance due to the air-bridge connections. The inductance due to an air bridge

is more than the inductance of a transmission line with equal dimensions. This is because as shown in Figure 3.25, it is important to consider the additional distance that a transmission line travels vertically upwards and then downwards. Equivalent circuits are developed at each source node and the equivalent inductance (or resistance) is determined by EM-simulating the corresponding structure at relatively high frequencies and modeling the response using a single series LR network. The overall L_s (and R_s) are determined by taking the average of the determined inductance (or resistance) at each source node.

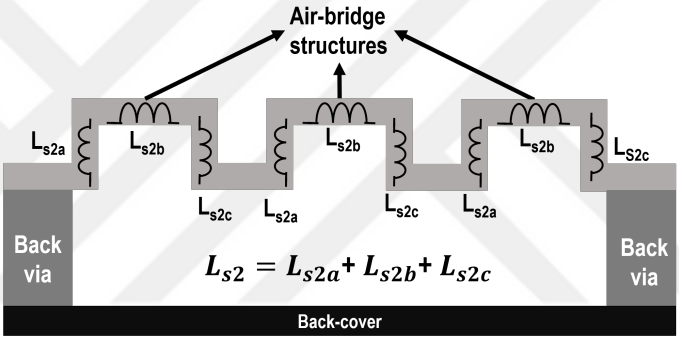


Figure 3.25: Cross-section of the source structures of a standard 6×100 μm device.

This method was applied to varying HEMT peripheries to determine the scalability of L_s and R_s. It was observed that L_s and R_s do not scale with changing W_g. The scalability of L_s and R_s as a function of NoF was modeled using the following equation:

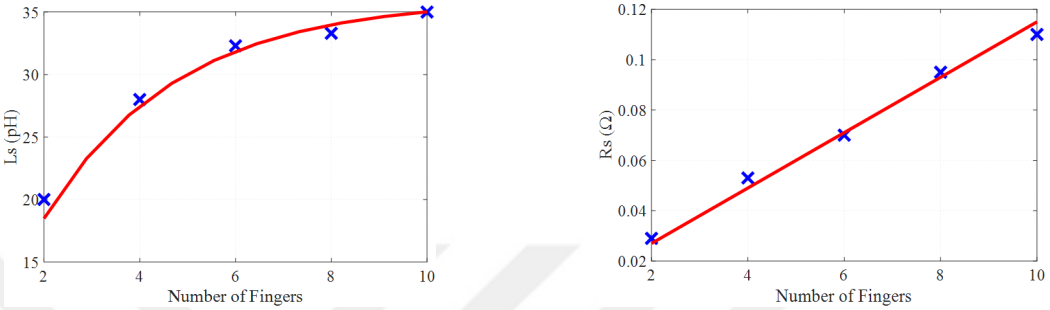
$$L_s = A(1 - e^{-B \times NoF}) \tag{3.12}$$

Similarly, R_s was fitted to the EM-based extractions using the following equation:

$$R_s = \alpha_0 NoF + \alpha_1 \tag{3.13}$$

Where A, B, α_0 and α_1 are constants used for fitting.

The L_s and R_s values determined using EM-simulations (blue cross) and using the model (red solid) for varying NoF are plotted in Figure 3.26:



(a) Scalability of L_s. (b) Scalability of R_s.

Figure 3.26: Modeled scalability of L_s (a) and R_s (b) as a function of NoF.

3.5 Intrinsic Parameter Extraction

Once the EPPs are known, they can be de-embedded from the S-parameter measurement data. If the EPPs are determined accurately, the de-embedded measurement closely represents the intrinsic part of the device. These de-embedded measurements, along with some assumptions can be safely used to extract the intrinsic parameters.

The S-parameter measurements are taken at the operating bias conditions of 28 V and 100 mA/mm. They can also be taken at other bias conditions to obtain a multi-bias HEMT model. The S-parameters can be converted to Z-parameters to easily de-embed the series extrinsic parasitics while they can be converted to Y-parameters to de-embed the shunt connect parasitic. From Figure 3.1, we have 2 series and 1 shunt extrinsic component at the gate and drain sides, and 2 series components connected to the source. The S-parameters are first converted to Z-parameters and the series parasitic inductance at the gate and the drain are de-embedded. The resulting 2-port network is then converted to Y-parameters so that the shunt pad capacitance at the drain and the gate C_{pd}, and C_{gd} can be easily de-embedded. Next, it is changed back to its updated Z-parameters so that the remaining series resistances and the source parasitics can be removed.

This procedure is summarized in Figure 3.27 [1].

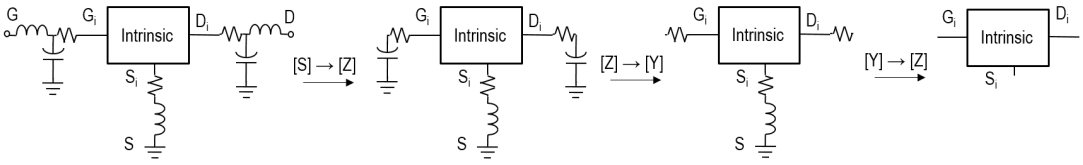


Figure 3.27: Extracted EPPs for a 6x100 μm device.

The remaining intrinsic part's Y-parameters can be represented using the following equations [36]:

$$Y_{11} = \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega(\frac{C_{gs}}{D} + C_{gd}) \tag{3.14}$$

$$Y_{12} = -j\omega C_{gd} \tag{3.15}$$

$$Y_{21} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} - j\omega C_{gd} \tag{3.16}$$

$$Y_{22} = g_{ds} + j\omega(C_{ds} + C_{gd}) \tag{3.17}$$

where $D = 1 + \omega^2 C_{gs}^2 R_1^2$.

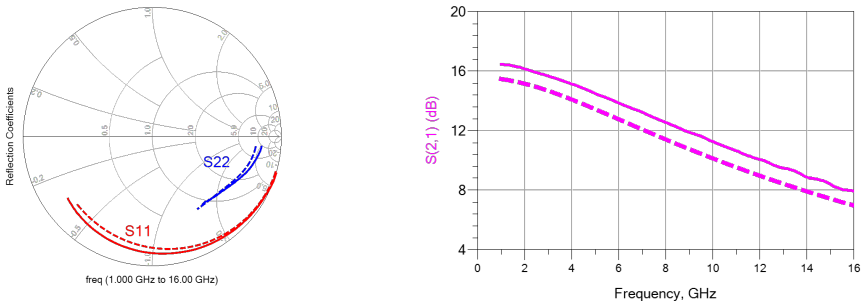
By separating the imaginary and real parts, all of the intrinsic parameter values can be determined. At this point, the complete initial HEMT model has been derived. However, significant intrinsic parameter tuning is required to fit the model response to the measured response of varying HEMT peripheries. Also, such a model is only valid for a single bias point and base temperature. For this reason, state-of-the-art ASM-HEMT models are used to refine the accuracy of the models further and to model the effect of the change of the bias conditions and the base temperature on the overall performance. These physics-based models are capable of obtaining powerful multi-bias, non-linear, scalable intrinsic parameters of a model.

3.6 Model Validation

The extrinsic extraction method was validated by performing schematic simulations using the complete HEMT model and comparing them with the measurements of HEMTs with varying gate peripheries. The small-signal response of the model was validated against measured frequency sweep from 1 GHz up to 16 GHz and the large-signal response at 10 GHz against non-linear measurement power contours at fixed input power levels.

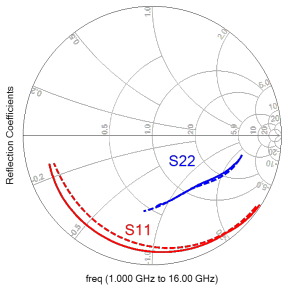
3.6.1 Small-Signal Validation

To verify the small-signal scalability of the model, measurement comparisons were performed using $4 \times 75\ \mu m$, $6 \times 100\ \mu m$, and $8 \times 125\ \mu m$ devices. The comparisons are shown in Figures 3.28, 3.29 and 3.30 respectively below. From these validation plots. It can be observed that the small-signal response of the model scales well when NoF or W_g is varied. The model slightly underestimates the gain of the transistors.

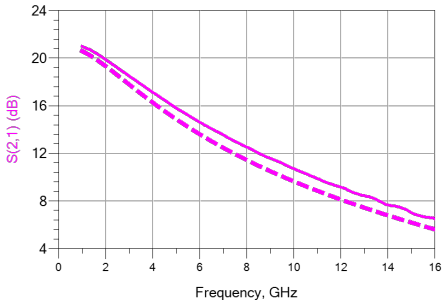


(a) S_{11} and S_{22}. (b) S_{21}.

Figure 3.28: Small-signal response of $4 \times 75\ \mu m$ HEMT model (dashed line) and measurement (solid line).

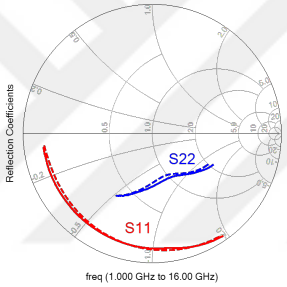


(a) S_{11} and S_{22}.

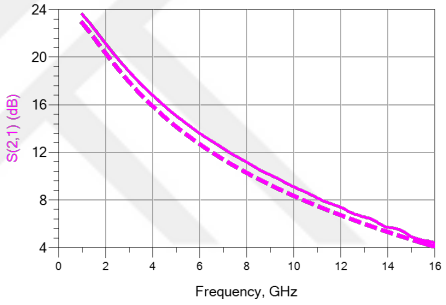


(b) S_{21}.

Figure 3.29: Small-signal response of $6 \times 100\ \mu m$ HEMT model (dashed line) and measurement (solid line)



(a) S_{11} and S_{22}.



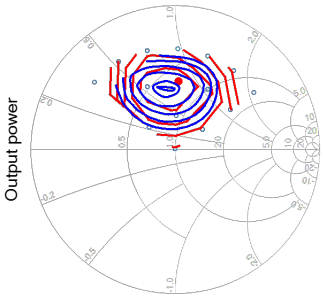
(b) S_{21}.

Figure 3.30: Small-signal response of $8 \times 125\ \mu m$ HEMT model (dashed line) and measurement (solid line

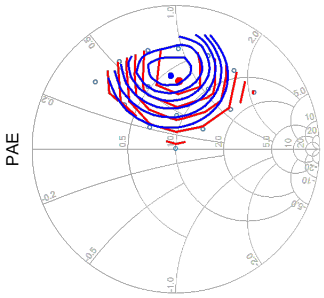
3.6.2 Large-Signal Validation

The large-signal validation was performed against measured load-pull HEMT data. The measurements were imported into ADS from Keysight using a load-pull GUI tool. Harmonic balance simulations were performed using the HEMT models to develop output power and PAE contours at fixed available input power levels. The input power levels were kept relatively high to keep the device under high (approximately 3-4 dB) gain compression. It was ensured that the source impedance in the simulation was the same as in the load-pull measurement.

The large-signal validation was performed using $6 \times 100\ \mu m$, $8 \times 125\ \mu m$ and $10 \times 100\ \mu m$ devices. The output power and PAE contours of these HEMTs are shown in Figures 3.31, 3.32 and 3.33

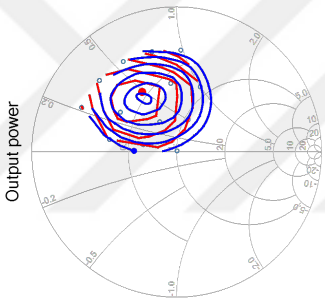


(a) Output power.

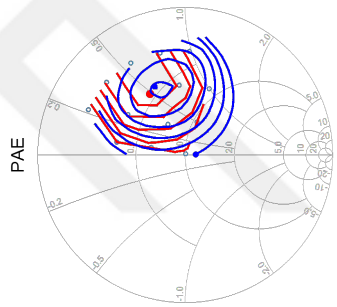


(b) PAE.

Figure 3.31: Large-signal response of 6×100 μm HEMT model (blue) and measurement (red) at 22 dBm available input power. Comparison performed at 80°C base temperature.

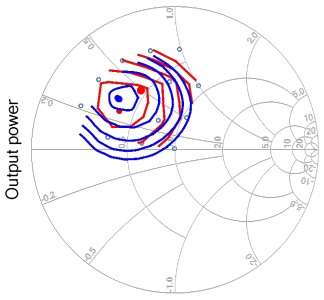


(a) Output power.

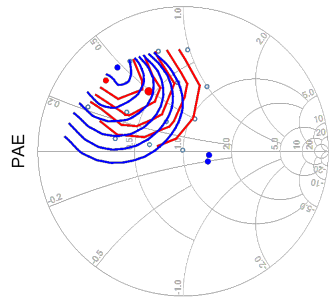


(b) PAE.

Figure 3.32: Large-signal response of 8×125 μm HEMT model (blue) and measurement (red) at 24 dBm available input power. Comparison performed at 80°C base temperature.



(a) Output power.



(b) PAE.

Figure 3.33: Large-signal response of 10×125 μm HEMT model (blue) and measurement (red) at 24 dBm available input power. Comparison performed at 80°C base temperature.

The large-signal performance of the model can be verified by observing the difference in the optimum impedance for output power and PAE, and by observing the difference in their corresponding values. Overlapping contours represent a good optimum impedance agreement. For an input available power of 22 dBm, the maximum output power and PAE values from the measurement of the $6 \times 100\ \mu m$ are 34.9 dBm and 56.2 %, respectively. The model exhibited 35.1 dBm and 59.6 % output power and PAE, respectively.

For an input available power of 24 dBm, the maximum output power and PAE values from the measurement of the $8 \times 125\ \mu m$ are 35.8 dBm and 52.5 %, respectively. The model exhibited 36.2 dBm and 50.6 % output power and PAE, respectively.

For an input available power of 24 dBm, the maximum output power and PAE values from the measurement of the $10 \times 125\ \mu m$ are 36.1 dBm and 56.9 %, respectively. The model exhibited 36.2 dBm and 53.4 % output power and PAE, respectively.

The large signal validation is summarized in Table 3.1. The large-signal validation confirms the good scalability of the model in terms of W_g and NoF.

HEMT	$\mathbf{P_{in,avs}}$	$\mathbf{P_{out,\ sim}}$	$\mathbf{P_{out,\ meas}}$	$\mathbf{PAE_{sim}}$	$\mathbf{PAE_{meas}}$
$\mathbf{6 \times 100\ \mu m}$	22 dBm	35.1 dBm	34.9 dBm	59.6 %	56.2 %
$\mathbf{8 \times 125\ \mu m}$	24 dBm	36.2 dBm	35.8 dBm	50.6 %	52.5 %
$\mathbf{10 \times 125\ \mu m}$	24 dBm	36.2 dBm	36.1 dBm	53.4 %	56.9 %

Table 3.1: Summary of OSV model large-signal validation.

The slight difference is due to the distinct harmonic impedances in the simulations and the measurements.

Chapter 4

Design of a 3 Stage Driver Amplifier MMIC

This chapter discusses the in-detail design procedure of the 3-stage driver amplifier MMIC. The transistor sizes and the number of stages are decided after considering the target specifications. Both, the small signal and the large signal measurements, using the set-ups explained in Chapter 2 are carefully analyzed. The small signal measurements are analyzed using ADS from Keysight, while the large signal measurements are examined using AMCAD Engineering's IVCAD.

NANOTAM's 250 nm PDK in ADS is used as the main design tool for this MMIC. An EM substrate is carefully tuned to closely match the EM simulations to the measurements. Shunt RC or series LR networks are used to unconditionally stabilize the transistors. A combination of lumped and distributed elements is used to design the matching networks. The output matching network is designed considering the optimum output impedance and the output reflection loss. The interstage matching networks are designed to control the gain ripple while the input matching network aims to achieve the maximum gain. DC bias lines with sufficient DC-RF isolation are also incorporated into the matching networks.

The complete MMIC was also simulated using the transistor models discussed

in Chapter 3. A comparison between the HEMT measurement-based simulations and the model-based simulations is done.

4.1 Topology Selection

The MMIC was designed to achieve more than 28 dB of small signal gain and output power of greater than 2 W. The periphery of the output stage indicates the achievable output power, while the sum of the maximum available gains (MAGs) of all the stages indicates the greatest possible attainable small signal gain.

The load-pull contours using the measurement set-up described in Chapter 2.4 were used to select a suitable device. The output power contours at 4 dB gain compression and 12 GHz for a typical 8×100 μm device are shown in Figure 4.1.

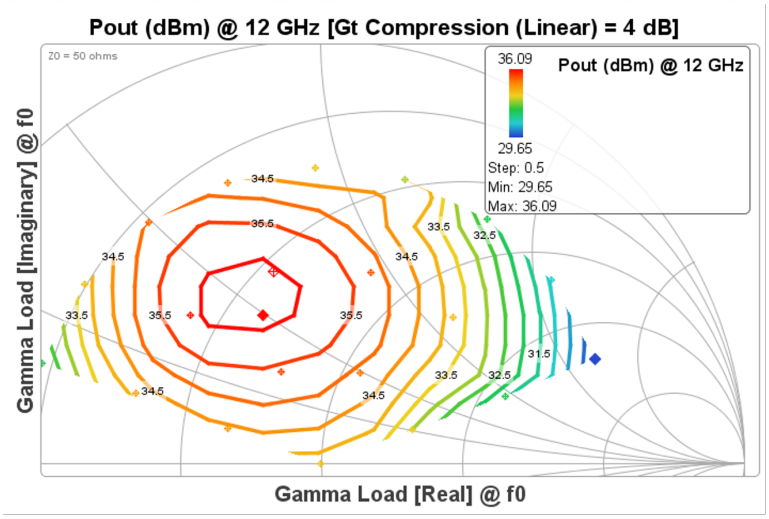


Figure 4.1: LP contours of a typical 8×100 μm device at 12 GHz and at 4 dB gain compression. Measurement performed on copper with 10% duty cycle at 28 V and 80 mA.

Since the GaN-On-SiC has an output power density of about 5 W/mm, an 8×100 μm device can easily output 4 W of saturated power. Using this estimate, and by observing the contours shown in Figure 4.1, it can be deduced that a 0.8 mm device is sufficient to fulfill the required output power specifications. A

margin for output power is maintained for the load impedance mismatch to ensure that a good output reflection loss and output power ripple are achieved as well.

The MAG for typical 4×75 μm, 6×125 μm, and 8×100 μm devices are plotted when they are biased at 28 V drain voltage and 100 mA/mm drain current in Figure 4.2.

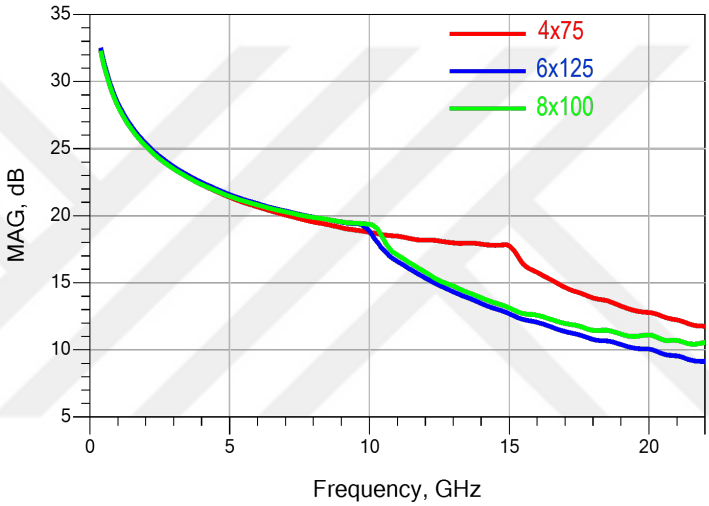


Figure 4.2: Measured MAG for typical 4×75 μm (red), 6×125 μm (blue), and 8×100 μm (green) devices. Measurement performed on-wafer at 28 V and 100 mA/mm.

Considering the inevitable substrate and conduction losses and the intentional resistive losses to be introduced in the matching networks, a three-stage design is necessary. To finalize the topology, a power budget estimate was performed using the large signal HEMT measurements. This is shown in Figure 4.3.

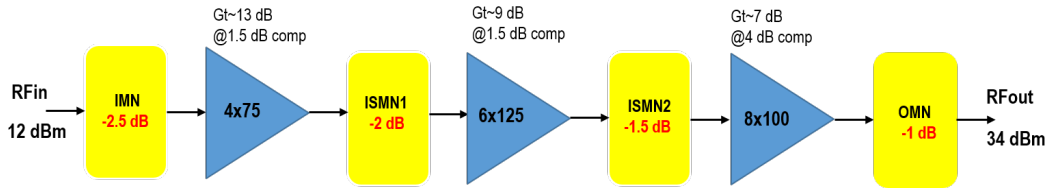


Figure 4.3: Power budget estimate for the driver amplifier. The gain and compression levels are estimated from the load pull measurements.

Apart from the small signal gain requirement, which can be easily verified from the MAG plots, it was ensured that the preceding stages' peripheries were large

enough to readily drive the subsequent stages. A large signal gain requirement of 20 dB dictates the maximum gain compression for the amplifier. For this reason, the total allowed compression is also carefully budgeted among the stages.

4.2 Stability Circuits

Designing the stability circuits is an important step in amplifier design. These lossy filter-like networks help achieve unconditional stability, which means that the HEMT can be safely terminated with any impedance without the risk of undesired oscillations.

The stability of the device is checked using its small signal measurements. The measurements include the drain and the gate manifold patterns and the HEMT core to obtain a connection to the outside world. However, in an actual MMIC, only the HEMT cores are utilized. Therefore, it is necessary to de-embed the effect of the gate and drain manifolds so that the reference plane is shifted to the core active device as shown in Figure 4.1 The de-embedding is performed using the manifold pattern's EM simulations and the de-embed tool available in ADS library.

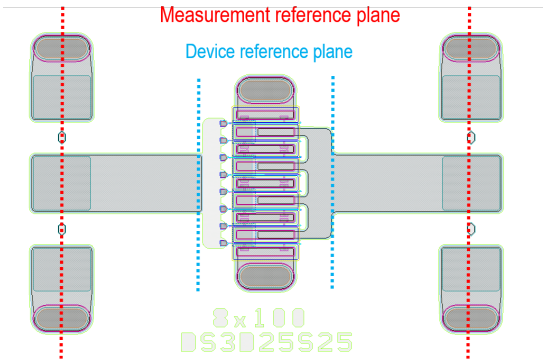


Figure 4.4: HEMT measurement reference plane (red) and device reference plane (blue).

To make a device stable, resistive components need to be introduced. For this reason, stability networks are preferred at the gain side rather than the drain in

high-power applications. Introducing lossy networks can improve the stability but can also reduce the gain of the device. Therefore, it is important to monitor the MAG when designing the stability circuits. As an example, the stability factor and the MAG of a typical $6 \times 125\ \mu m$ device are plotted in Figure 4.5

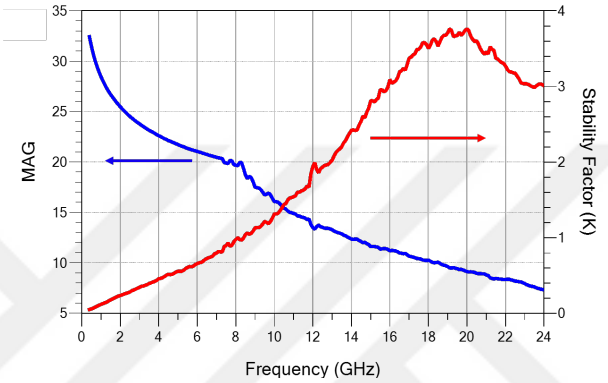


Figure 4.5: MAG (blue) and stability factor (red) of a typical $6 \times 125\ \mu m$ device

From Figure 4.5, it can be seen that the K-factor is typically less than 1 for relatively lower frequencies. This means that the device is conditionally stable for the frequency range where the K factor is less than 1. A high-pass filter in the shape of a parallel RC circuit, connected in series to the gate of the transistor, is implemented to preserve the gain at frequencies higher than 8 GHz but to introduce losses at frequencies less than 8 GHz to make them unconditionally stable. Figure 4.6 shows the network used for this purpose. The K-factor and MAG after implementing this stability network are shown in Figure 4.7. The K-factor and MAG before introducing the stability network are also shown in this figure for comparison.

With the help of the stability network, the HEMT is now stable down to 2 GHz. Thanks to the high-pass network, the decrease in MAG at higher frequencies is minimal. The conditional stability below 2 GHz is expected to be catered with the losses introduced in the gate bias line. This is equivalent to a series LR network connected in shunt configuration, at the gate of the transistor. The resistor will dampen the low-frequency signals. An example of such a bias line implemented at the gate of stage 1 is shown in Figure 4.8

Verifying the stability of an active device using the μ and μ' parameters can be

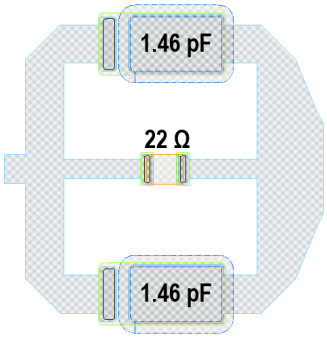


Figure 4.6: Stability RC network used at the gate of stage 2

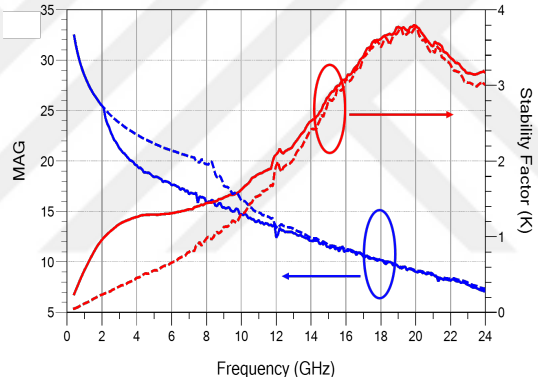


Figure 4.7: MAG (blue) and stability factor (red) of a typical $6 \times 125\ \mu m$ device. The dotted plots represent the parameters after the stability networks while the solid lines represent the parameters before the stability networks.

more useful than the K-factor. This is because the K-factor only tells us whether the device is unconditionally stable. μ and μ' however, give information about 'how much' the device is unconditionally stable. These are a measure of the distance from the center of the Smith Chart to the nearest unstable impedance point at the gate and at the drain, respectively. μ and μ' are defined as follows:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta(S_{11}^*)| + |S_{21}S_{12}|} \tag{4.1}$$

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta(S_{22}^*)| + |S_{21}S_{12}|} \tag{4.2}$$

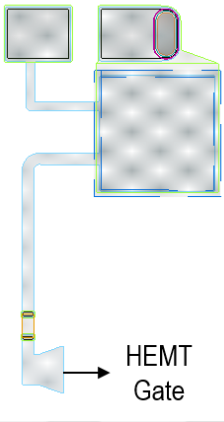


Figure 4.8: Gate bias line for Stage 1 HEMT.

The μ and μ' parameters for a typical $6 \times 125\ \mu m$ device after including the stability networks are shown in Figure 4.9.

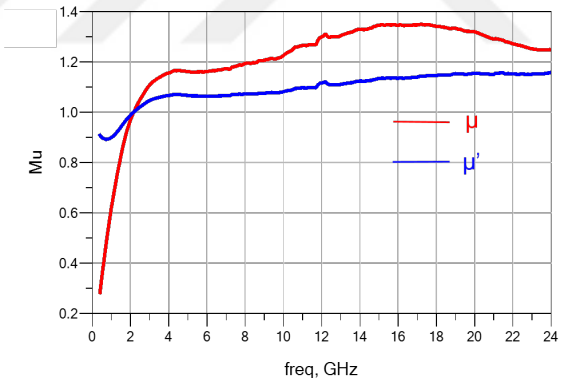
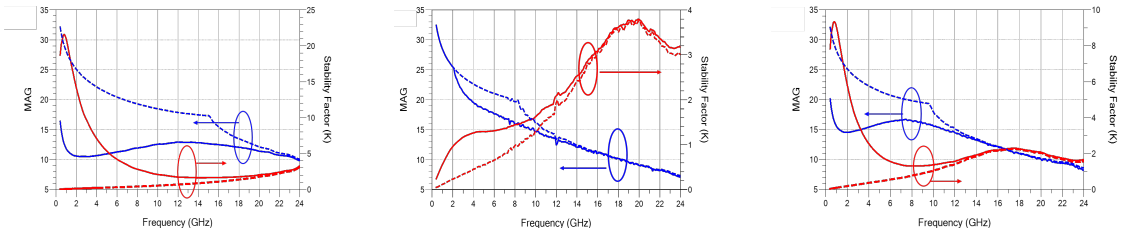


Figure 4.9: μ and μ' for the $6 \times 125\ \mu m$ device after including the stability network.

Similar techniques were used to unconditionally stabilize other HEMTs in the design to avoid undesired oscillations. The MAG and the stability factor for each device, before and after the implementation of the stability networks, are shown in Figure 4.10



(a) MAG and K factor for $4 \times 75\ \mu m$ HEMT.

(b) MAG and K factor for $6 \times 125\ \mu m$ HEMT.

(c) MAG and K factor for $6 \times 100\ \mu m$ HEMT.

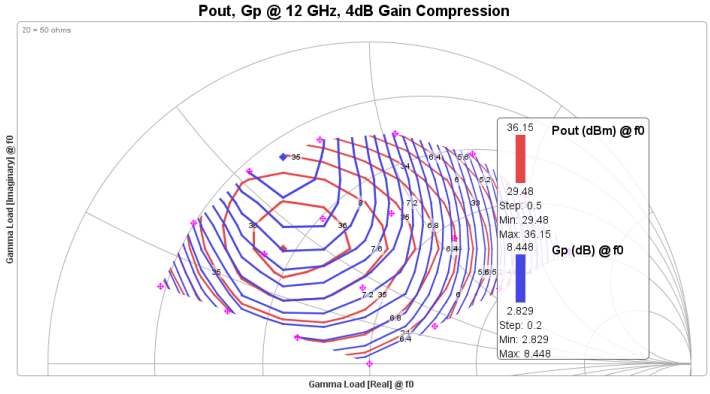
Figure 4.10: MAG (blue) and stability factor (red) of all 3 HEMTs, before (dotted lines) and after (solid lines) adding the stability networks.

4.3 Output Matching Network

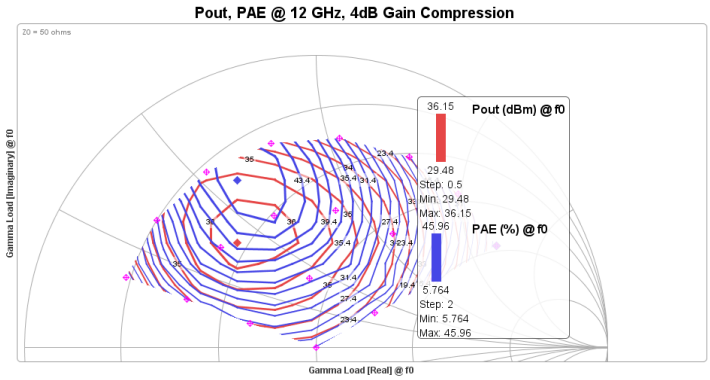
The purpose of the output matching network (OMN) is to present a good load impedance to the drain of the third stage HEMT in terms of output power and S_{22}. Since most of the output power contributions come from the third stage, it is also the most crucial stage in determining the PAE. Load pull measurements were performed using the methods explained in Chapter 2.4 in identifying the optimum target impedances. The output power contours are compared to the operating power gain (G_p) contours, and the PAE contours for a typical $8 \times 100\ \mu m$ device, at 4 dB gain compression, in Figure 4.11

From this figure, it can be noted that the optimum impedance for output power is $(23 + 20.5i)\ \Omega$, while it is $(12.7 + 31.8i)\ \Omega$ for G_p. This is because under higher powers i.e. in the non-linear regime the small signal impedances of a transistor tend to change. Since this transistor will be used in the final stage, it will certainly be operating deep in the non-linear region. Therefore, it is important to select the optimum impedances by analyzing the large-signal measurements. The optimum impedance for PAE is $(15.5+29.5i)\ \Omega$ which is also different. It is clear from these measurements that there is a trade-off between output power, Gp (or S22), and PAE. This is one of the reasons why an output periphery larger than necessary was used. As a result, the optimum target impedances were chosen in between to obtain a good trade-off between gain, output power, and PAE.

Since this is a broadband design, such an analysis was done at more than one



(a) Output power and G_p.



(b) Output power and PAE.

Figure 4.11: Load pull contours of a typical 8×100 μm device at 12 GHz and 4 dB Gain compression under CW, 70 °C base temperature conditions.

frequency. The optimum target impedances were chosen accordingly at various frequencies between 5 GHz and 12 GHz.

Finally, the matching network is designed. The matching networks are optimized at 3 different frequencies simultaneously: 5 GHz, 8 GHz, and 12 GHz. A relatively higher order matching network was used to achieve a wide-band match. The necessary drain bias line and the DC block capacitor were integrated into the matching network. The schematic of the OMN is shown in Figure 4.12

The resulting load impedance seen by the third stage HEMT evaluated using the EM simulation of the layout corresponding to the schematic of the OMN is shown in Figure 4.13. Achieving a perfect match is difficult for a broadband

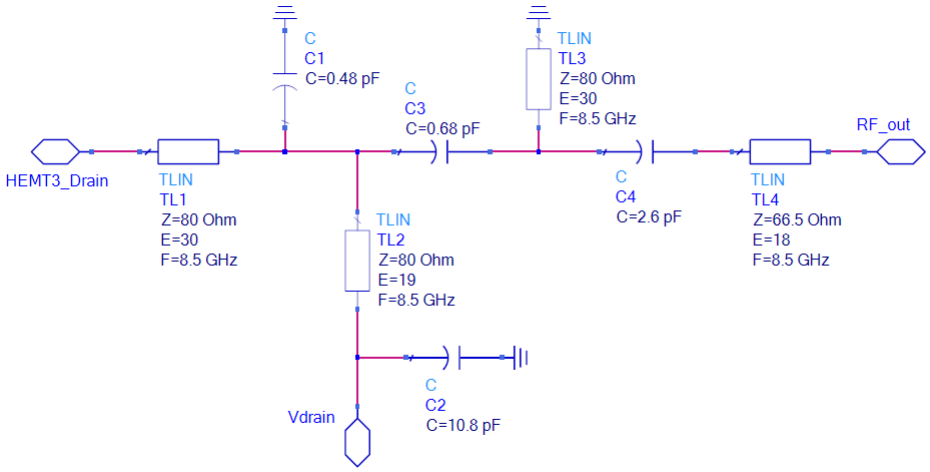


Figure 4.12: DA MMIC OMN schematic design.

design using conventional reactive matching techniques. The matching was optimized such that the impedance at all frequencies of interest is sufficiently close to their respective targets simultaneously. Moreover, since the device is capable of delivering more output power than needed, there is room for slight mismatch.

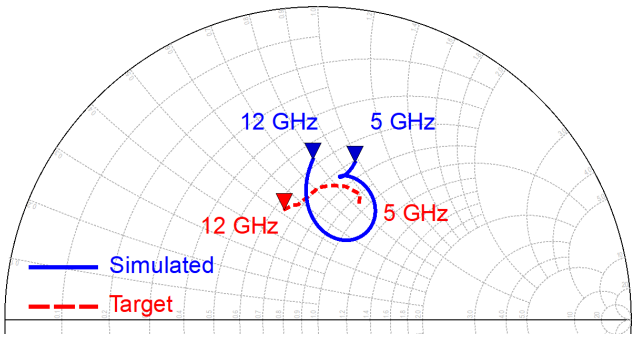


Figure 4.13: Target (red dotted line) and EM-simulated (solid blue line) impedance for the third stage HEMT.

Since output power is mostly dependent on the last stage, the forthcoming OMN must have as little loss as possible to conserve the output power. The loss is checked using the MAG component available in ADS. This method assumes perfect conjugate matching and hence ignores the mismatch losses. The loss of the OMN is plotted in Figure 4.14. Despite the high-order matching network, the loss of the OMN in the frequency range of interest is limited to 0.9 dB.

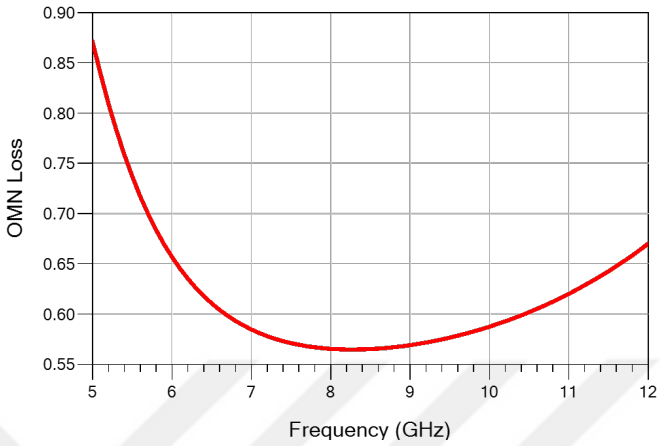


Figure 4.14: DA MMIC OMN EM-simulated loss.

The layout of the OMN is shown in Figure 4.15. EM simulations were performed to obtain the results shown in the figures above. The layout was optimized as a whole so that the coupling effects could also be considered in the simulations.

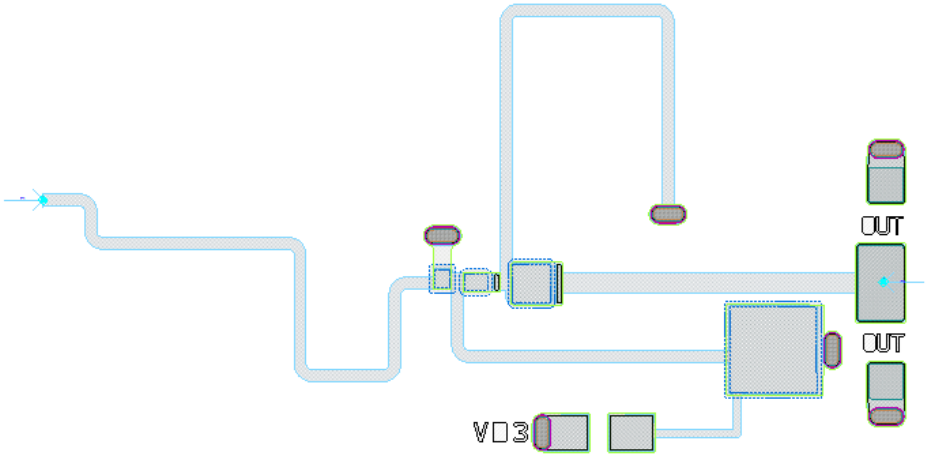


Figure 4.15: DA MMIC OMN layout design.

4.4 Interstage Matching Networks

Since this is a 3 stage design, there are two inter-stage matching networks: The first inter-stage matching network (ISMN1) and; the second inter-stage matching

network (ISMN2).

ISMN2 is in between the second and third-stage transistors. It is responsible for presenting the optimum source impedance to the third-stage HEMT for achieving a good gain and also showing the correct impedance at the load of the second-stage HEMT. It is also responsible for controlling the small-signal gain ripple to some extent.

The gain ripple in ISMN2 is mostly controlled by introducing intentional conjugate mismatches at the load and source of the second and third stages, respectively. The small-signal gain of a transistor is dependent on how well it is conjugately matched at its drain and source and also on its inherent $|S_{21}|$. The MAG plots that were obtained in section 4.1 suggest that the gain of an active device tends to decrease with increasing frequency because of the dominant effect of the parasitic capacitances inherent to these frequencies. Therefore, obtaining a better conjugate impedance match at higher frequencies and intentionally obtaining relatively poor conjugate impedance at lower frequencies can help reduce the gain at lower frequencies.

After choosing the optimum load impedance for stage 3 while designing the OMN, a magic source-pull was performed using AMCAD Engineering's IVCAD measurement software. Even though the source impedance was fixed as the load impedance was swept during the load-pull measurements, the software is capable of developing source-pull contours for a fixed load impedance. The power gain source-pull contours for the 8×100 μm device for a load impedance of $(26+30i)$ Ω are shown in Figure 4.16.

To obtain the maximum power gain from the third stage at 12 GHz, the source impedance should be $(6 + 0i)$ Ω. Similar analyses were performed to obtain the optimum source impedance at 8 GHz and 5 GHz.

The output load impedance is analyzed using the load-pull contours of the 6×125 μm HEMT. The second stage must be able to output enough power so that it can drive the third stage. This means that the second stage should not

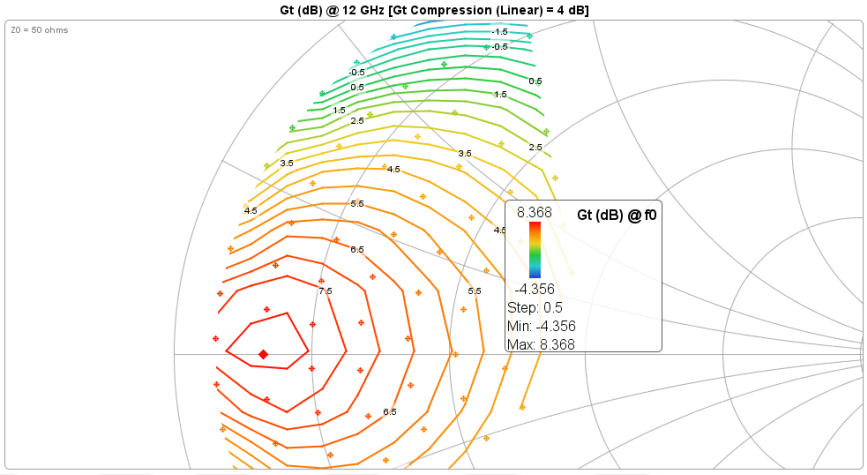


Figure 4.16: Power gain source-pull contours of an 8×100 μm device at 12 GHz and 4 dB gain compression. $Z_L = (26 + 30i)\ \Omega$

compress as much as the third stage. However, it is known that in order to tune the small-signal response of the full MMIC, there will be significant mismatches in terms of output power and large signal gain. This can cause the second stage to compress more at some frequencies. The load-pull contours of a typical 6×125 μm are shown in Figure 4.17.

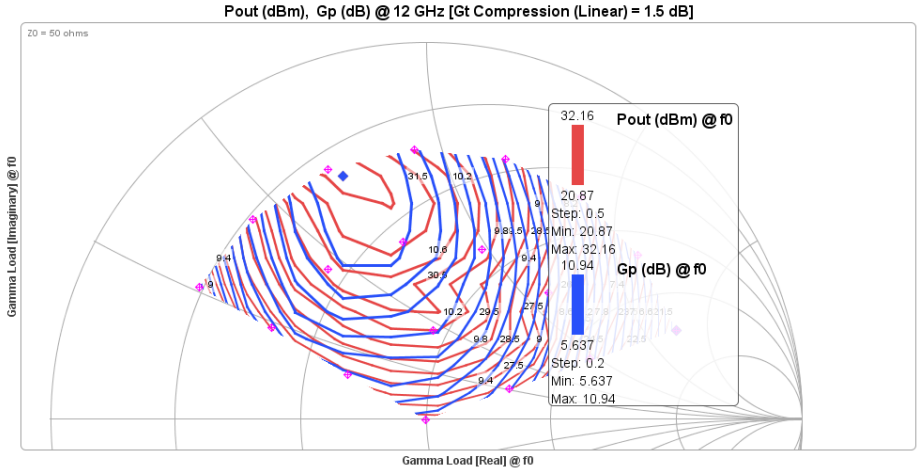


Figure 4.17: Output power (red) and available gain (G_p) Load pull contours for a typical 6×125 μm device at 12 GHz at 1.5 dB gain compression.

In a similar manner, both, the optimum load impedance for output power, and, the optimum load impedance for gain are selected at 8 GHz and at 5 GHz. However, since a transistor has inherently a higher gain at a lower frequency,

the low-frequency response should be intentionally mismatched with regard to the optimum impedance for gain at that particular frequency. The third stage's source pull and the second stage's load pull provide a good starting point for developing the matching networks. However, as the design matures, the full MMIC's tuned response strongly influences the impedance.

The tuned stage 3 source impedance together with the optimum impedance points for power gain at 5 GHz, 8 GHz, and 12 GHz are shown in Figure 4.18.

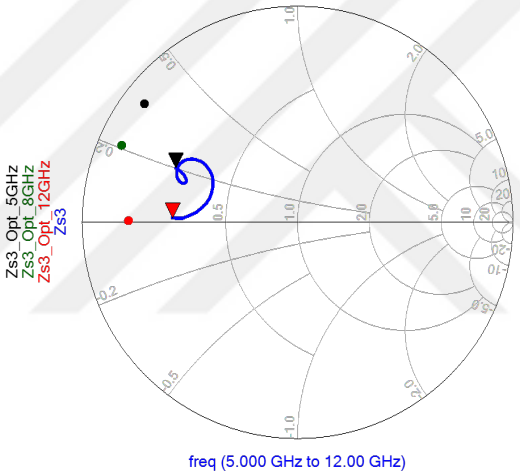
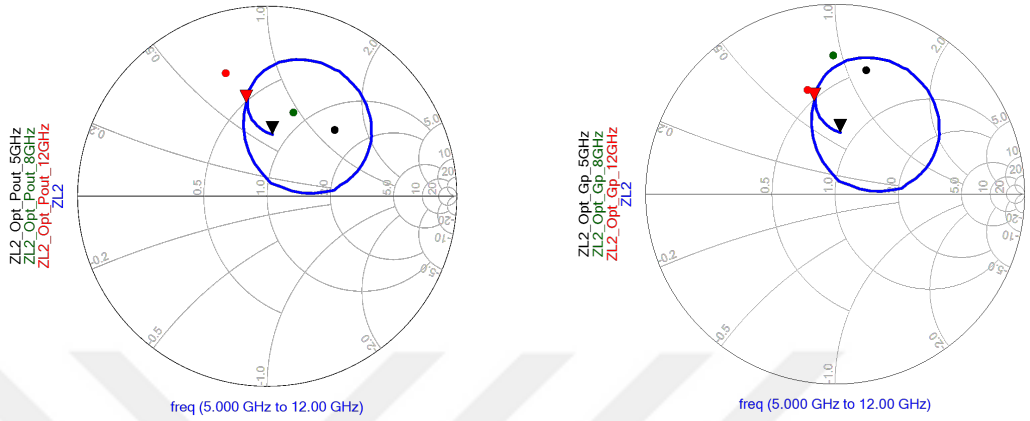


Figure 4.18: DA MMIC stage 3 source impedance (blue) and optimum impedance for power gain at 5 GHz (black), 8 GHz (green), and at 12 GHz (red).

The tuned stage 2 load impedance with optimum points for power gain and output power is plotted in Figure 4.19. It can be seen that the source impedance of stage 3 and load impedance of stage 2 are intentionally better matched at higher frequencies than at lower frequencies in terms of gain. Stage 2 has a decent load impedance match in terms of output power.



(a) (b)

Figure 4.19: DA MMIC stage 2 load impedance (blue) with optimum impedance for output power (a) and with optimum impedance for G_p (b) at 5 GHz (black), 8 GHz (green) and at 12 GHz (red).

The loss of ISMN2 is shown in Figure 4.20. The loss in ISMN2 was also carefully monitored so that the power available from the second stage HEMT could easily drive the third stage.

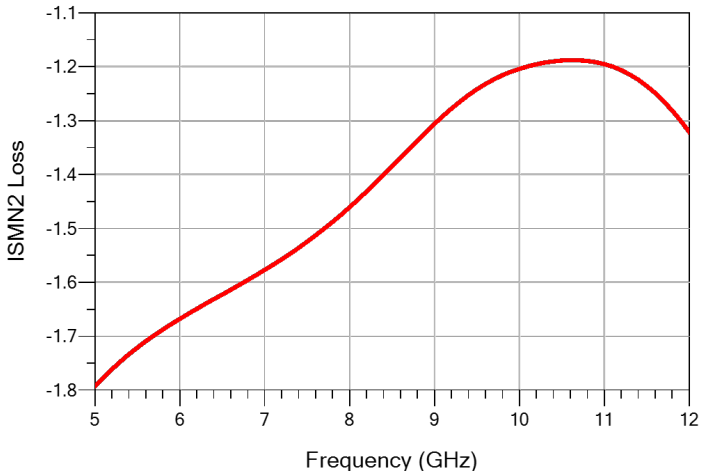
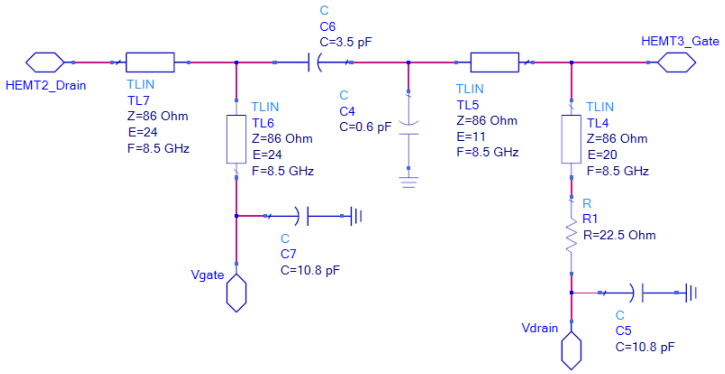
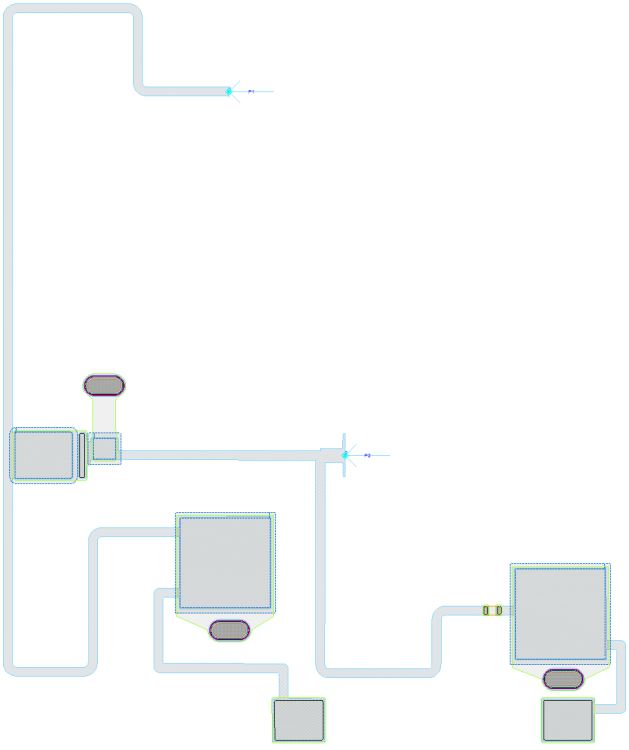


Figure 4.20: DA MMIC EM-simulated ISMN2 loss.

The schematic and the corresponding tuned layout are shown below in Figure 4.21.



(a) Schematic.



(b) Layout.

Figure 4.21: DA MMIS ISMN2 schematic (a) and layout (b) design.

ISMN1 is between the first stage HEMT and the second stage HEMT. It is mainly responsible for the gain ripple control. The optimum impedance for output power is not as important as the latter stages because the first stage only needs to compress the second stage slightly. As done with ISMN2, the large signal HEMT measurements are used as a starting point. As the design proceeds, the need to make changes to adjust the gain ripple becomes much more significant. Moreover, other resistive components were incorporated in addition to the stability network to increase the loss at lower frequencies. The introduction of the extra resistive components is the main facilitator of gain ripple control in ISMN1. This is evident from the insertion loss of this matching network shown in Figure 4.22. The loss at 5 GHz is about 7.4 dB compared to only 2.2 dB at 12 GHz.

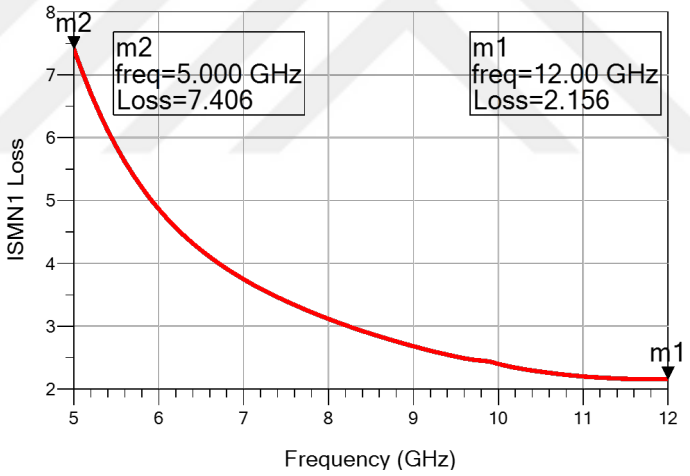
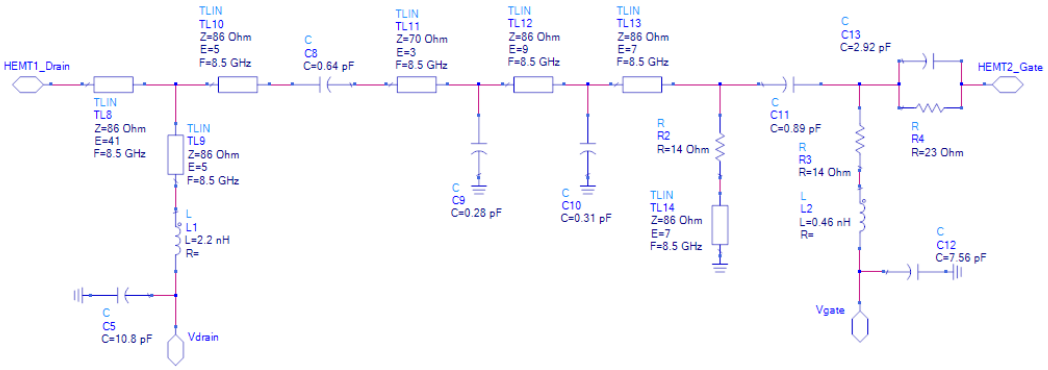


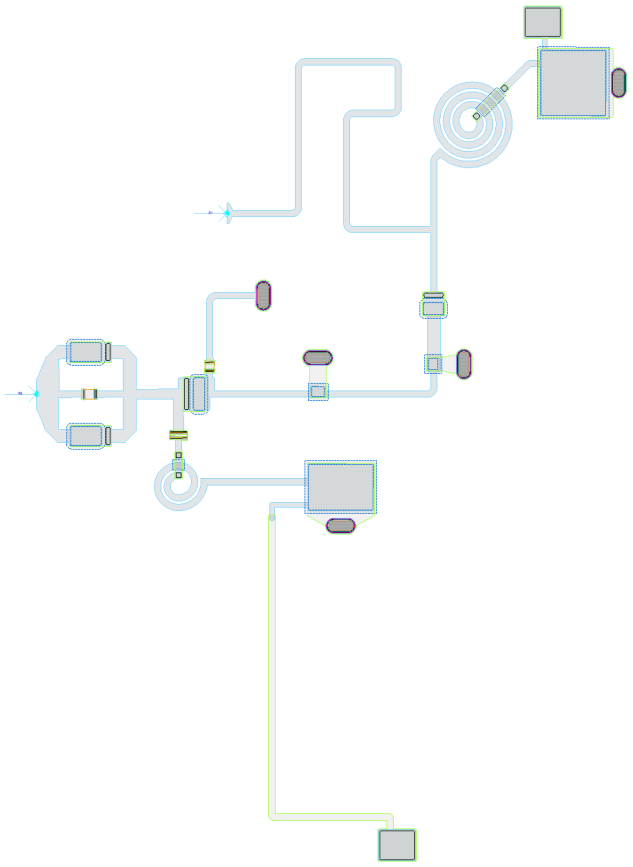
Figure 4.22: DA MMIC's EM-simulated ISMN1 loss.

The schematic and the corresponding layout are shown in Figure 4.23. An even higher order matching network is used to obtain the desired gain ripple and impedance matching. The obtained load impedance of stage 1 and the source impedance of stage 2 are shown in Figure 4.24.

The DC-RF isolation is checked for each bias line in the design to ensure that the impedance of the DC probes does not affect the RF response. The layout used to EM-simulate the bias lines to check the DC-RF isolation for the ISMN1 is shown in Figure 4.25. The isolation of ports 1 and 2 to port 3 is more than 25 dB. Another method of checking the isolation is to connect an arbitrary impedance

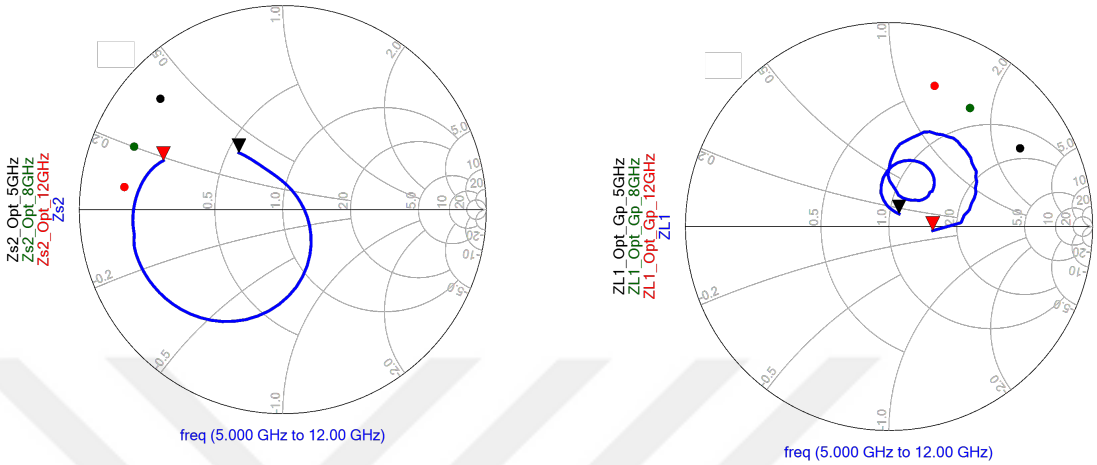


(a) Schematic



(b) Layout

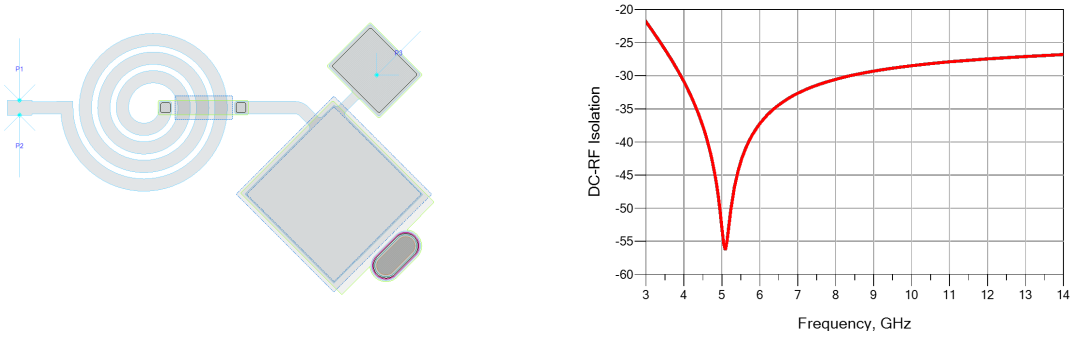
Figure 4.23: DA MMIC ISMN1 schematic (a) and layout (b) design.



(a) (b)

Figure 4.24: ISMN1 EM-simulated stage 2 source (a) and stage 1 load (b) impedances.

termination to the DC pad, sweep both the real and imaginary parts for all practical values, and check whether the impedance response of the matching network changes.



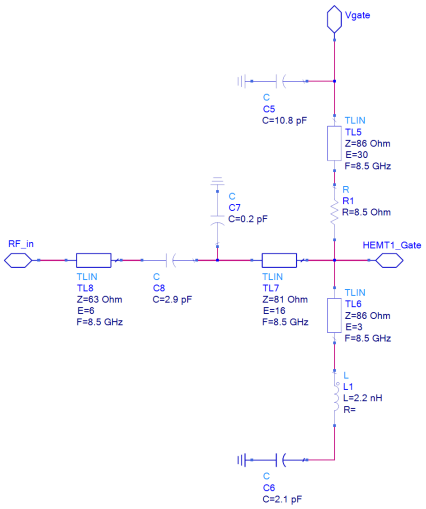
(a) (b)

Figure 4.25: ISMN1 drain bias line layout (a) and its corresponding EM-simulated DC-RF isolation

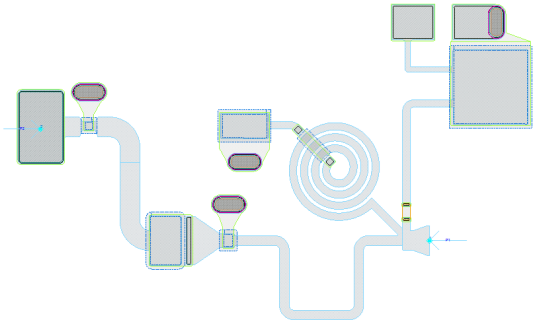
4.5 Input Matching Network

The IMN is important for achieving a good input return loss and a high gain from the MMIC. A conjugate match is intended at the gate of the first stage

HEMT. This not only boosts the small signal gain but also provides a good input reflection coefficient (IRC). Again, the bias lines were kept as a part of the matching network. The designed IMN schematic and its corresponding tuned layout are shown in Figure 4.26. The loss of the matching network is plotted in Figure 4.27 and the impedance seen at the gate of stage 1 HEMT is shown in Figure 4.28



(a) Schematic.



(b) Layout.

Figure 4.26: DA MMIC IMN schematic (a) and layout (b) design.

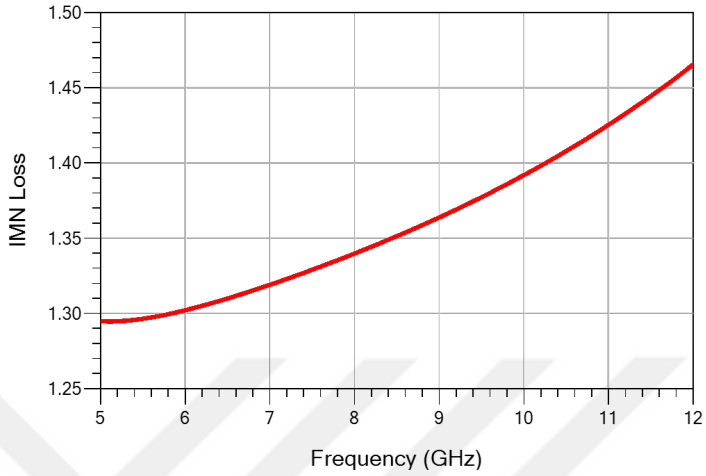


Figure 4.27: DA IMN EM-simulated loss.

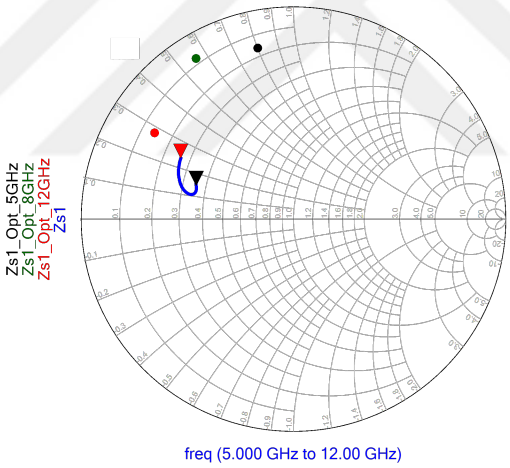


Figure 4.28: DA IMN EM-simulated stage 1 source impedance.

4.6 Full MMIC Simulation Results

4.6.1 Small Signal Simulation Results

4.6.1.1 Stability Analysis

Before finalizing the MMIC, it is most important to check the stability of the completed MMIC. Even slight oscillations in a design can cause signal distortion and lead to output power loss. Oscillations can be caused either by parasitic

intrinsic and extrinsic feedback components in an active device or due to poorly isolated DC bias lines. Another reason could be reflections greater than unity i.e. the reflected signal has a magnitude greater than the feed signal. Such a back-and-forth signal can grow in magnitude and greatly disrupt the working of an amplifier. Therefore, it is very important to perform a stability analysis.

Using the RC and LR stability networks, the transistor was kept unconditionally stable down to 2 GHz. Frequencies less than this must be stabilized using either the bias lines or due to the inherent loss of the matching networks.

To perform the even-mode stability check, the MMIC was divided into three parts as shown in Figure 4.29.

The μ and μ' parameters are checked for these three sub-circuits to check the stability for each stage together with the matching networks. The μ and μ' are plotted in Figure 4.30. It can be observed that these are greater than 1 for the full frequency range.

Another way of checking the even-mode stability is by checking the oscillation condition. It is certain that there will be an oscillation at the node where all three of the following conditions are satisfied at any frequency:

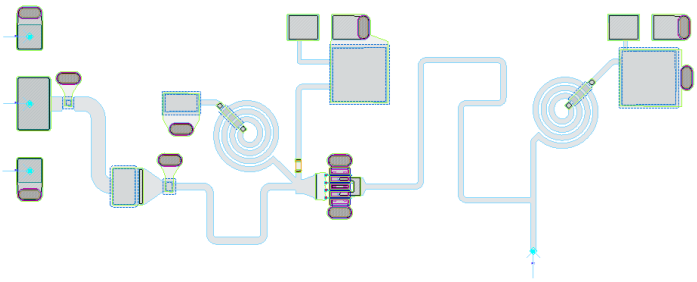
1. The real part of the sum of impedance looking to the left and looking to the right of the node must be negative:

$$Re(Z_L + Z_R) < 0 \tag{4.3}$$

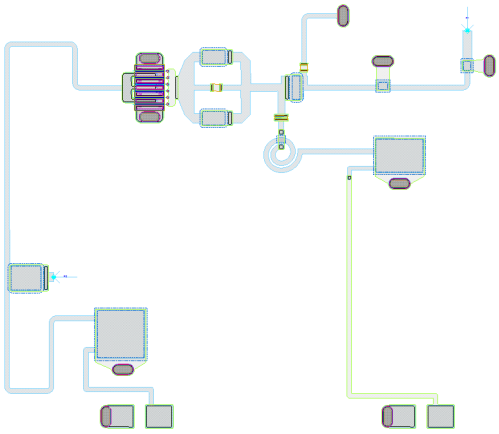
2. The imaginary part of the sum of the impedance looking to the left and to the looking to the right of the node must be zero:

$$Im(Z_L + Z_R) = 0 \tag{4.4}$$

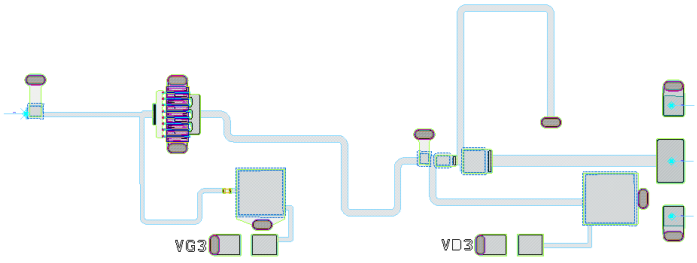
3. The partial derivative with respect to the frequency of the imaginary part



(a) Part 1

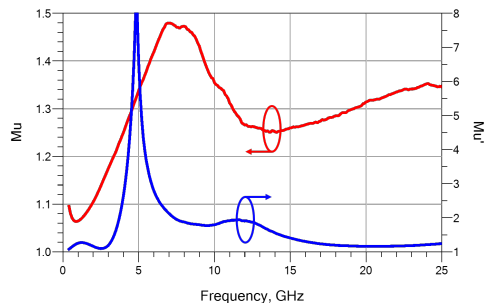


(b) Part 2

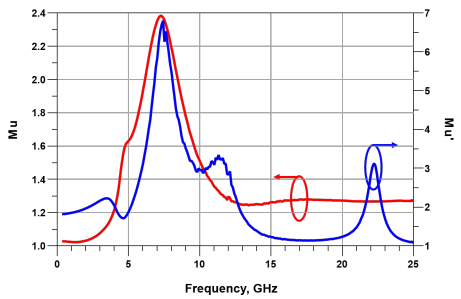


(c) Part 3

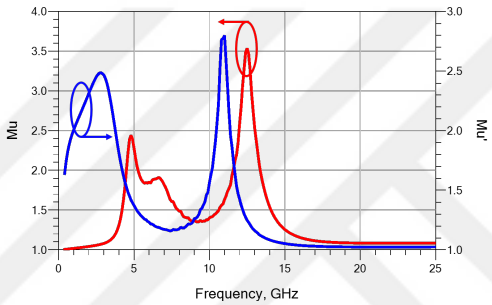
Figure 4.29: DA MMIC layout partitioning for even-mode stability test.



(a) Part 1.



(b) Part 2.



(c) Part 3.

Figure 4.30: EM-simulated μ(red) and μ'(blue) plots for the three sub-circuits shown in Figure 4.29.

of the sum of the impedance looking to the left and looking to the right of the node must be positive:

$$\frac{\partial Im(Z_L + Z_R)}{\partial f} > 0 \tag{4.5}$$

The oscillation conditions can be checked using the S-probe component available in ADS. It can check the impedance to its left and right while remaining transparent to the circuit. If any of the above-mentioned conditions are not satisfied at any frequency, there will be no oscillations. Although the check must be performed at every node, the condition mentioned in equation 4.3 is most likely to be true closest to the active devices. Hence, the test is performed at the gate and at the drain of each device as shown in Figure 4.31.

The resulting plots corresponding to the oscillation conditions are plotted in Figure 4.32.

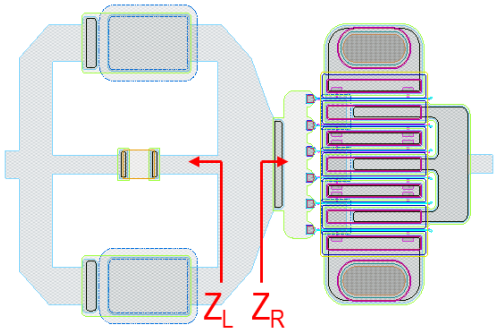


Figure 4.31: Stability test example showing impedance looking to the right Z_R and impedance looking to the left Z_L at the gate of stage 2 HEMT.

The first condition of oscillation, Equation 4.3, is only satisfied for the gate sides of stage 1 and stage 3 HEMTs for some frequencies. However, the sum of the imaginary parts (second oscillation condition in Equation 4.4) does not cross the x-axis at these frequencies. Hence, the DA MMIC passes the even-mode stability test.

The same test was successfully performed again, this time for the admittance. The oscillation conditions for admittance are similar to that of impedance:

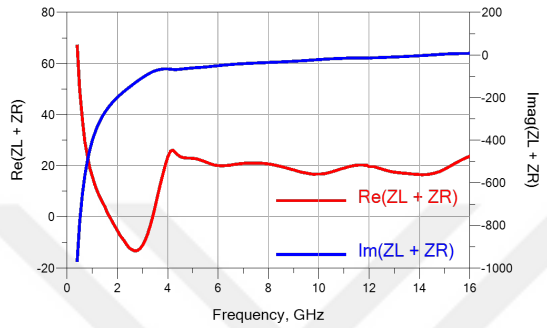
$$Re(Y_L + Y_R) < 0, \tag{4.6}$$

$$Im(Y_L + Y_R) = 0 \text{ and}, \tag{4.7}$$

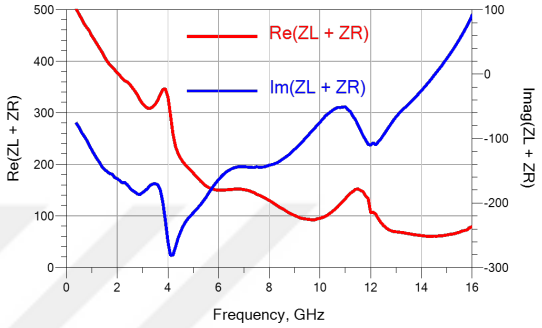
$$\frac{\partial Im(Y_L + Y_R)}{\partial f} > 0 \tag{4.8}$$

4.6.1.2 S-parameter Simulation

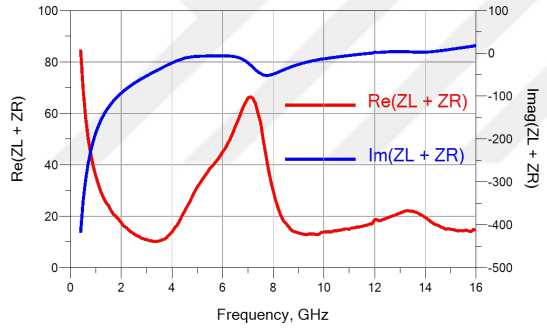
The full MMIC was EM-simulated and the EM response was tuned when all of the matching networks were placed in the same layout. This allows the designer to observe any changes due to the coupling effects between the different matching networks. The full completed layout is shown in Figure 4.33. Air bridges were used wherever a cross-over of MET1 and MET2 was required. A meandered layout was preferred to fit the MMIC in a relatively small area of 2.7 x 3.2 mm^2. This resulted in significant coupling effects, especially between ISMN1 and OMN,



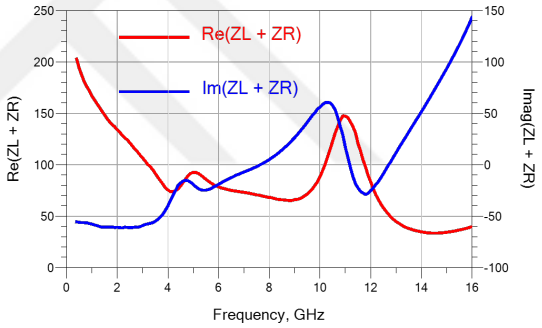
(a) At the gate of stage 1 HEMT.



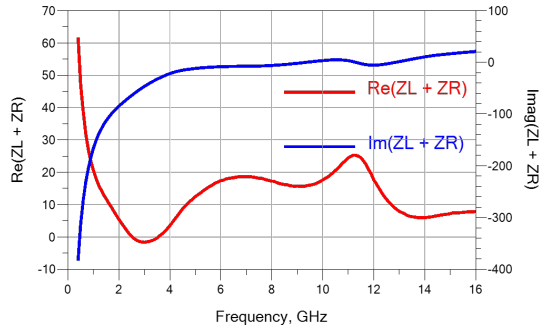
(b) At drain of stage 1 HEMT.



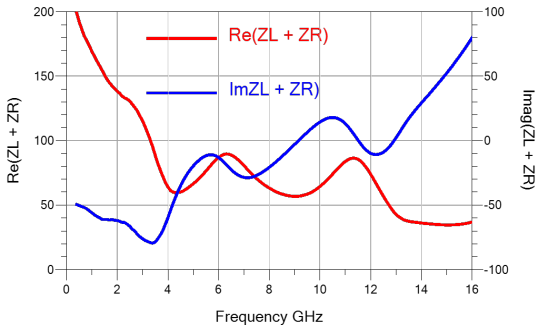
(c) At the gate of stage 2 HEMT.



(d) At drain of stage 2 HEMT.



(e) At the gate of stage 3 HEMT.



(f) At drain of stage 3 HEMT.

Figure 4.32: Sums of real (red) and imaginary (blue) parts of the impedances looking towards right and towards left at the gate and drain of each stage of the DA MMIC.

which were later absorbed as part of the matching networks. The origin of the coupling effects was located by breaking the full layout into smaller portions and observing which two components, when simulated separately, got rid of the undesired changes in the EM response. The identified components were then tuned so that the effect of coupling was minimized. Some space, in the top right corner, has been left intentionally for future integration with other circuitry like an RF switch. The full schematic is shown in Figure 4.34.

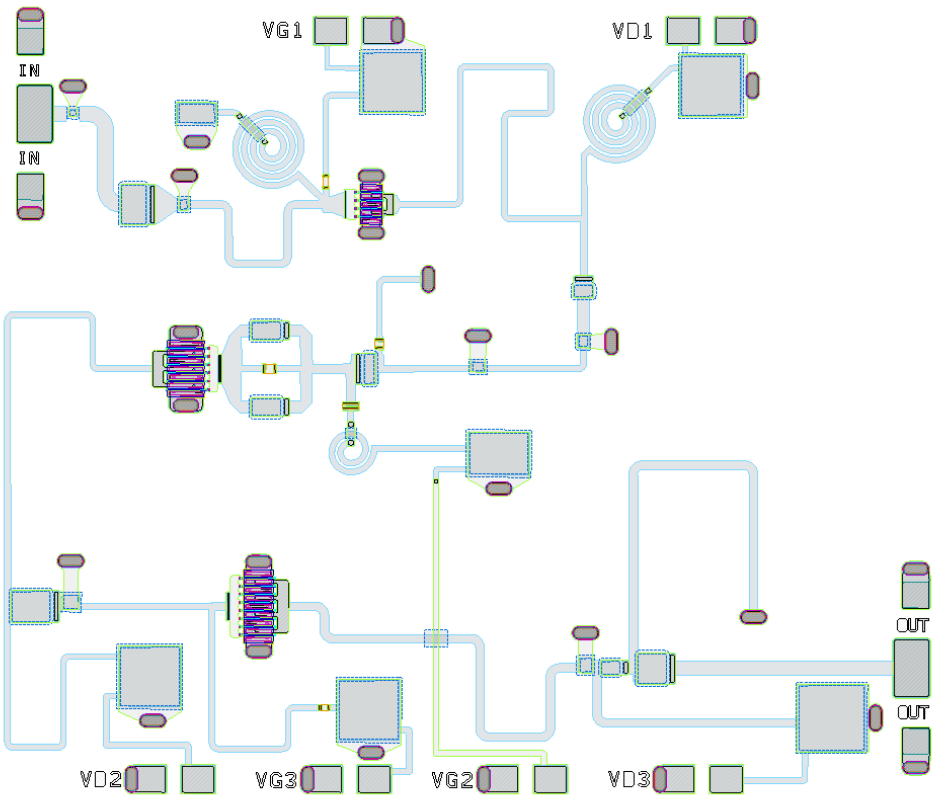


Figure 4.33: Full DA MMIC layout.

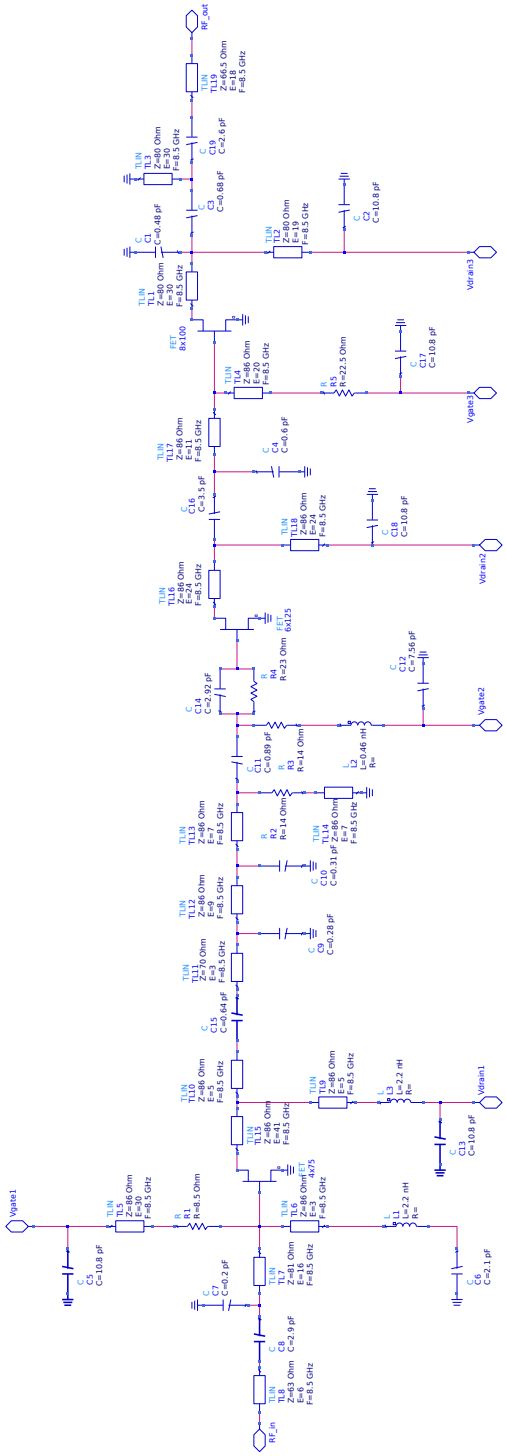


Figure 4.34: Full DA MMIC schematic.

The small signal simulation results using the HEMT measurement data and using the PDK HEMT models are shown in Figure 4.35. The simulation results using the HEMT models are sufficiently close to the simulations using the HEMT measurements. When using HEMT measurement data, the simulation results exhibit a typical small signal gain of 31.2 dB with a gain ripple of ± 0.95 dB. The worst IRL and ORL were -11.7 dB and -11.5 dB, respectively. For the S-parameter simulations using the PDK HEMT models, the typical small signal gain was 28.8 dB with a gain ripple of ± 1.10 dB. The worst IRL and ORL in this case were -11.6 dB and -11.3 dB, respectively. The small signal gain using the measured HEMT data is higher because the HEMTs were measured on a copper carrier, while the models were fitted to HEMT measurements made on-wafer from a different fabrication process. The on-copper measurement provides better heat dissipation and a better ground connection. This is why on-copper measurements have higher gain than on-wafer measurements. The comparison between the simulation responses of the two sets of simulations is summarized in Table 4.1.

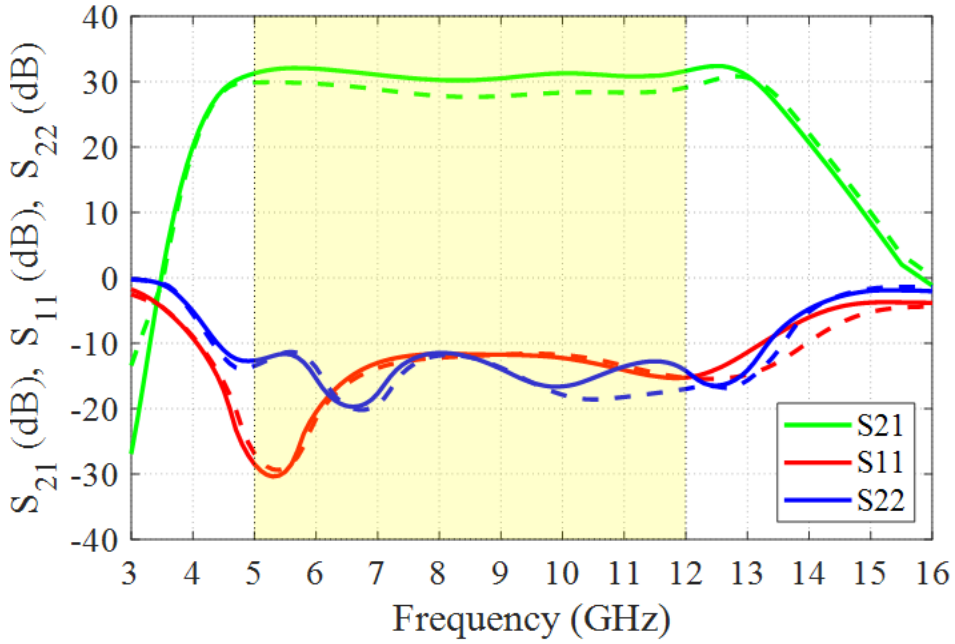


Figure 4.35: DA MMIC S-parameter EM simulation response using the HEMT measurement data (solid lines) and using the PDK HEMT models (dashed lines).

Parameter	Simulation (PDK HEMT model)	Simulation (HEMT measurements)
$\mathbf{S_{11}}$	-11.6 dB	-11.7 dB
$\mathbf{S_{22}}$	-11.3 dB	-11.5 dB
$\mathbf{S_{21}}$	28.8 dB	31.2 dB
$\mathbf{\Delta S_{21}}$	$\pm$ 1.10 dB	$\pm$ 0.95 dB

Table 4.1: Small signal response comparison of the two sets of simulations (using the PDK HEMT models and using the HEMT measurements). Worst-case IRL and ORL quoted. Typical gain quoted.

4.6.2 Large Signal Simulation Results

Large signal simulations were performed using the PDK's HEMT models. The harmonic balance simulator was used to perform these non-linear simulations. A single fundamental tone is applied to simulate the output power, PAE, and large signal gain as a function of input power. 2-tone measurements were performed to characterize the linearity of the MMIC. Since the large signal measurements were to be performed with a 10% duty cycle, the thermal resistance, R_{th}, parameter of the HEMT model was adjusted until the output power of the HEMTs was similar to that observed from the measurements. The harmonic balance simulation responses for a fixed input power of 10 dBm and a frequency step-size of 0.5 GHz are plotted in 4.36. The minimum output power achieved is 34.3 dBm at 6.5 GHz, while the large signal transducer gain, G_T, varies between 24.2 dB (at 11.5 GHz) and 25.4 dB (at 8.0 GHz). The minimum PAE is 22.3 %.

The input power was swept from -20 dBm to 16 dBm to observe the transition from linear to non-linear region and to determine the saturated output power, gain, and efficiency as functions of available input power. These simulations were performed at 3 frequencies: 5 GHz, 9 GHz, and at 12 GHz. The transducer gain, output power, and PAE as a function of input power are shown in Figure 4.37. The output power saturates at 35.8 dBm when the input power to the MMIC is about 14 dBm at 9 GHz. The transducer gain at this input power is

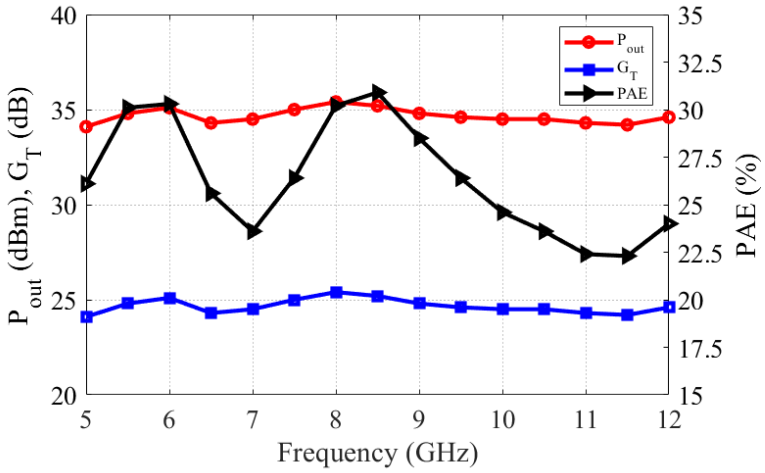
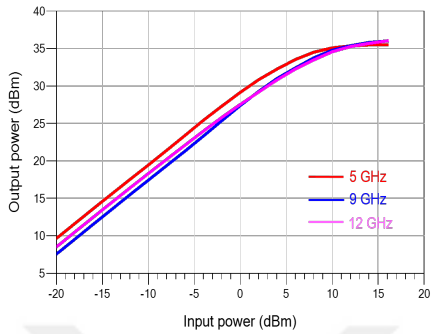


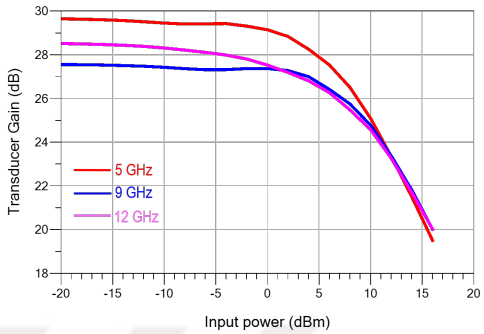
Figure 4.36: DA MMIC Harmonic Balance simulation response with an input available power of 10 dBm.

approximately 21.7 dBm, while the PAE is 30.7 %.

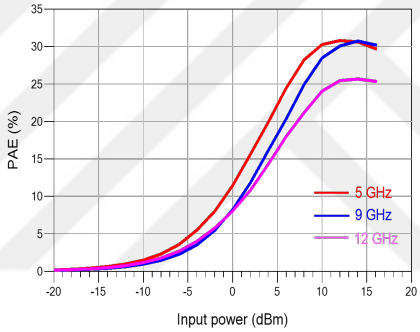
To characterize the linearity of the MMIC, 2-tone harmonic balance simulations were performed. Two closely separated fundamental tones are applied to the amplifier. This gives rise to intermodulation products at the output of the amplifier due to its non-linear characteristics. Third intermodulation products can adversely interfere with the DA's operation because these are generated very close to the fundamental tones and cannot easily be filtered out. Two fundamental tones with -20 dBm input power at 7.995 GHz and at 8.005 GHz are applied to the MMIC. A low input power is applied to ensure that the simulation is performed under linear conditions. The output spectrum is shown in Figure 4.38. The power of the fundamental tones is 7.7 dB The third-order inter-modulation products are generated at 7.985 GHz and 8.015 GHz, and have an output power of -43.7 dBm. The fifth-order intermodulation products can also be observed at 7.975 GHz and 8.025 GHz with an output power of -83.4 dBm. The simulated OIP3 (the extrapolated output power at which the fundamental tone and third-order intermodulation products will be equal) of the DA is 33.4 dBm.



(a) Output power vs input power.



(b) Transducer gain vs input power.



(c) PAE vs input power.

Figure 4.37: Harmonic balance simulation results for an input power sweep at 5 GHz (red), 9 GHz (blue), and at 12 GHz (pink).

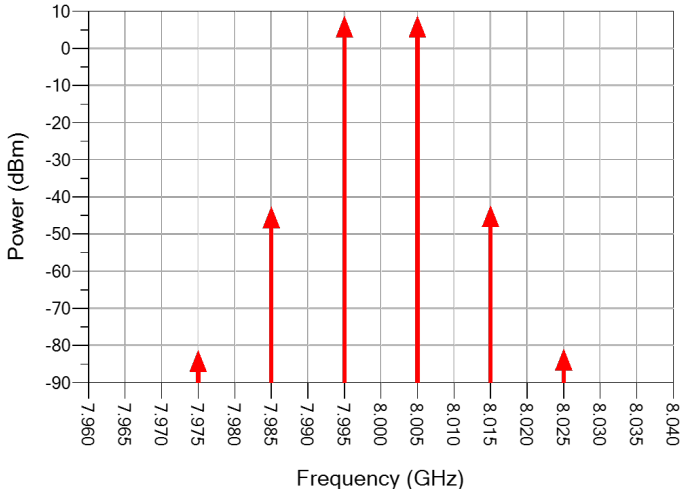


Figure 4.38: DA output spectrum for a two-tone harmonic balance simulation.

Chapter 5

MMIC Measurements

The finalized MMIC design was fabricated using NANOTAM's 250 nm process. A total of 9 MMICs were fabricated across different regions of the wafer. The MMIC's microphotograph image is shown in Figure 5.1.

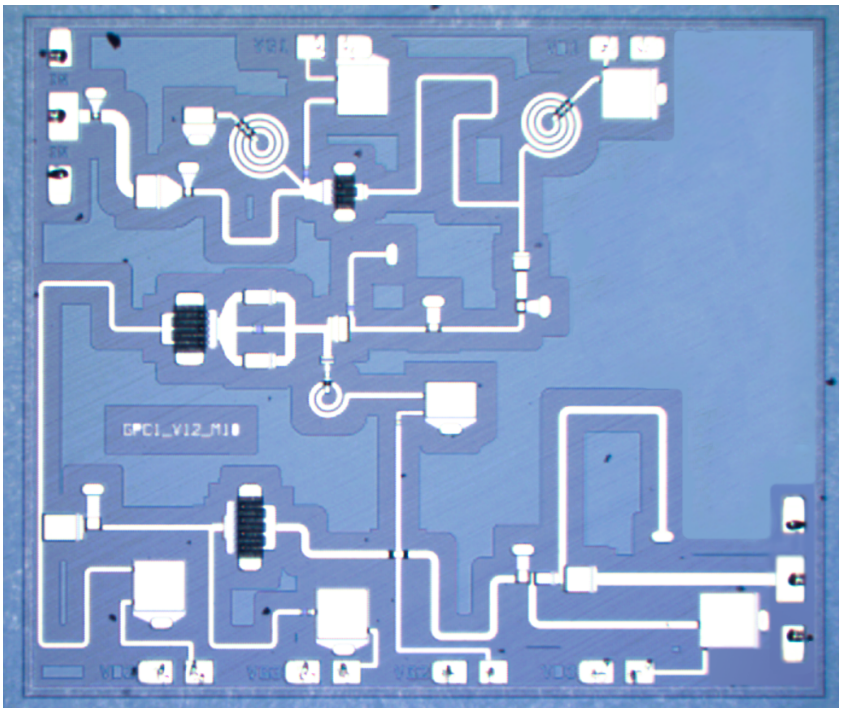


Figure 5.1: Fabricated DA MMIC using NANOTAM's 250 nm process.

The design was done using the HEMT measurement data but the simulations were also performed using the HEMT models. Since at this time the models are not very mature, the measurements are expected to be closer to the simulations using the HEMT measurement data rather than the HEMT models.

5.1 MMIC Small-Signal Measurements

The small-signal measurements were performed on-wafer under CW conditions and the chuck temperature was raised to 70°C. The MMIC was biased at 28 V drain voltage and 100 mA/mm drain current and two-port measurements were performed. The small signal measurements together with the HEMT measurement-based simulation are shown in Figure 5.2. Across the 9 measurements, the gain fluctuated between 28.1 dB and 33.1 dB. However, the gain ripple for any one MMIC does not exceed ± 1.35 dB. The measured gain was slightly less than the simulated gain due to the minor fabrication differences. For most of the MMICs, IRL was better than -10 dB. The worst ORL measured was -8.6 dB. Overall, there is a good match between the S-parameter measurements and the HEMT measurement-based simulations. The consistency in the measurement response is an indication of a uniform and mature process.

The PDK HEMT model simulations are plotted on top of the measurements in Figure 5.3. The simulation slightly deviated from the measurements at the higher frequency because of the difference in the response of the model HEMTs and the actual fabricated HEMTs. The model was fitted to an older process and the minor difference from one process to another may be responsible for this change. In comparison to the measurements, the simulation slightly underestimates the gain and the gain ripple. There is a decent match between the measurements and the simulation but there is some room for improvement, especially at higher temperatures. Another reason could be that the current model does not consider the change in intrinsic or extrinsic parasitics with the change in the drain or source pad pitches. Varying source and drain pad sizes were used for the HEMTs in this design. The small-signal results are summarized in Table 5.1.

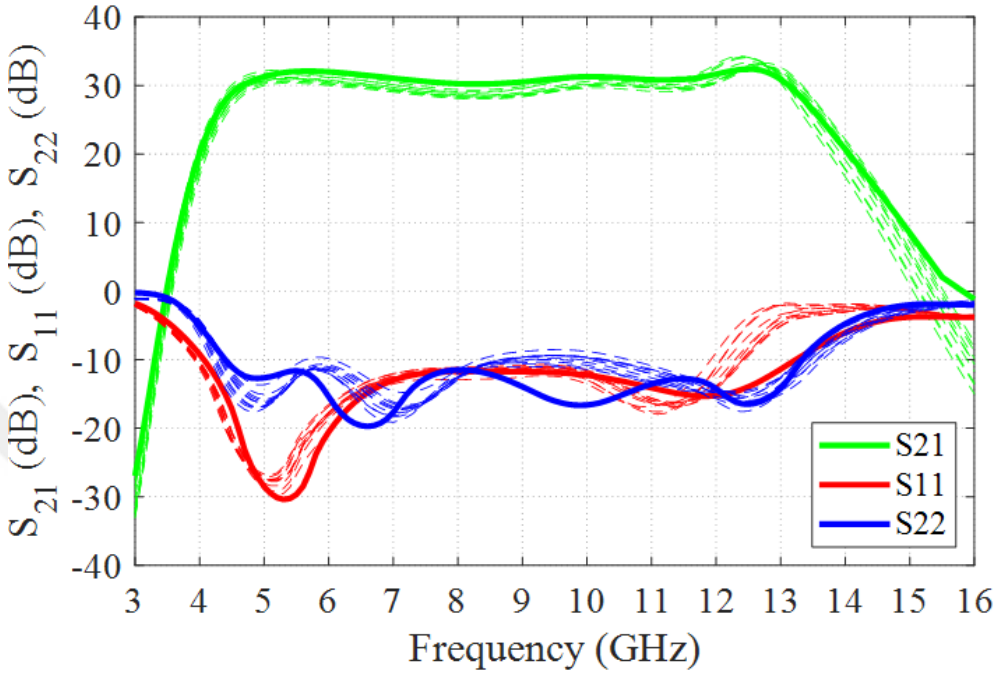


Figure 5.2: DA MMIC small signal measurements (dashed lines) and simulations (solid) using HEMT measurement-based data.

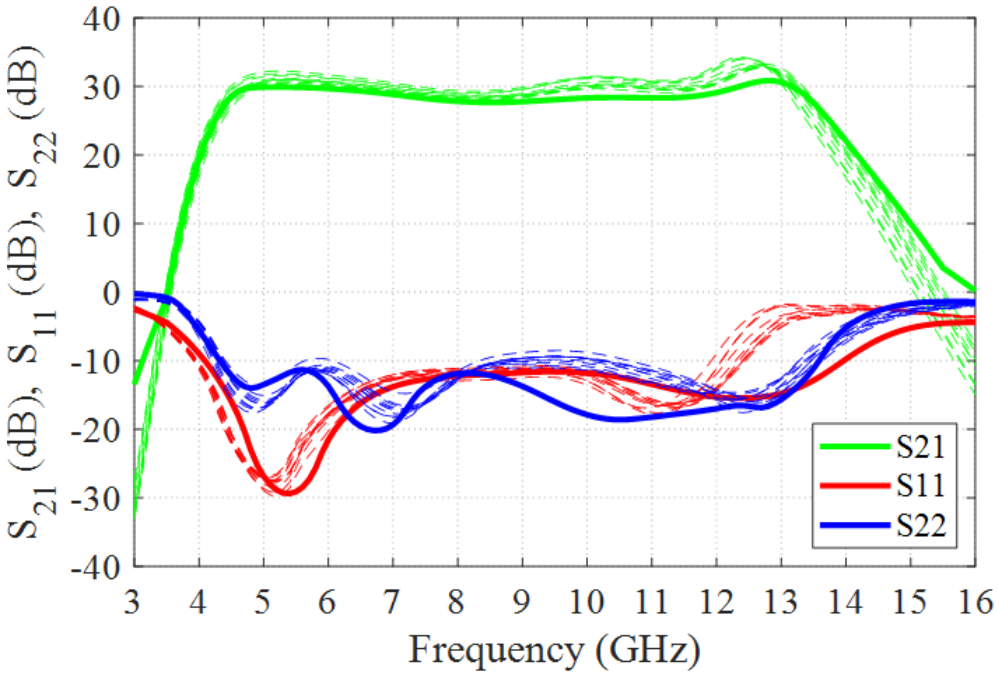


Figure 5.3: DA MMIC small signal measurements (dashed lines) and simulations (solid) using HEMT models.

Parameter	Simulation (PDK HEMT model)	Simulation (HEMT measurements)	Measurement
$\mathbf{S_{11}}$	-11.6 dB	-11.7 dB	-10.0 dB
$\mathbf{S_{22}}$	-11.3 dB	-11.5 dB	-8.6 dB
$\mathbf{S_{21}}$	28.8 dB	31.2 dB	29.1 dB
$\mathbf{\Delta S_{21}}$	$\pm$ 1.10 dB	$\pm$ 0.95 dB	$\pm$ 1.35 dB

Table 5.1: Small signal response comparison between measurements and the two sets of simulations (using the PDK HEMT models and using the HEMT measurements). Worst-case IRL and ORL quoted. Typical gain quoted.

5.2 MMIC Large-Signal Measurements

The large-signal MMIC measurements were performed on a copper carrier at 70°C. A copper carrier provides better heat dissipation and a more robust ground connection as compared to on-wafer measurements. The drain and gate bias voltages were pulsed with a 10 % duty cycle with a period of 25 μs. The supply voltages were applied using pulsers, which are capable of keeping a record of the gate and the drain currents as the input power is swept. These currents are used by the Maury software to internally calculate the PAE of the MMIC.

The measurements were performed in frequency steps of 0.5 GHz from 5 GHz to 12 GHz. Since the MMIC is matched to 50 Ω, there is no need to use load tuners because the Power Network Analyzer (PNA) itself is matched to 50 Ω. The MMIC is biased with a 28 V drain voltage and 185 mA (i.e. 100 mA/mm). The measured response for a fixed input power of 10 dBm, together with the simulated response is shown in Figure 5.4. The output power varies between 34.4 dBm and 33.3 dBm for frequencies between 5 GHz and 12 GHz. This means that for an output periphery of 8×100 μm, the minimum output power density is an impressive 2.68 W/mm. The large signal gain fluctuates between 23.2 dB and 24.4 dB while the minimum and maximum measured PAE are 18.2% and

30.2%, respectively. The output power and power gain at 10 dBm input power have ripples of only ± 0.65 dB and ± 0.60 dB, respectively. This means that the driver amplifier is consistent across different frequency bands, allowing uniform amplification and preservation of signal integrity. Moreover, for a system-level design, it is desirable to have a constant output power for the same input power level because it is challenging to control input power levels precisely.

When compared with the simulations, the HEMT models overestimate the large-signal performance of the MMIC. Typically, the simulated output power was 1.2 dB greater than the measured output power. The gain was also overestimated by almost 1.1 dB. The measured PAE, although matches the simulated PAE until 7 GHz, the model overestimates the PAE for the rest of the frequencies. Nevertheless, the model's large-signal performance is sufficiently accurate.

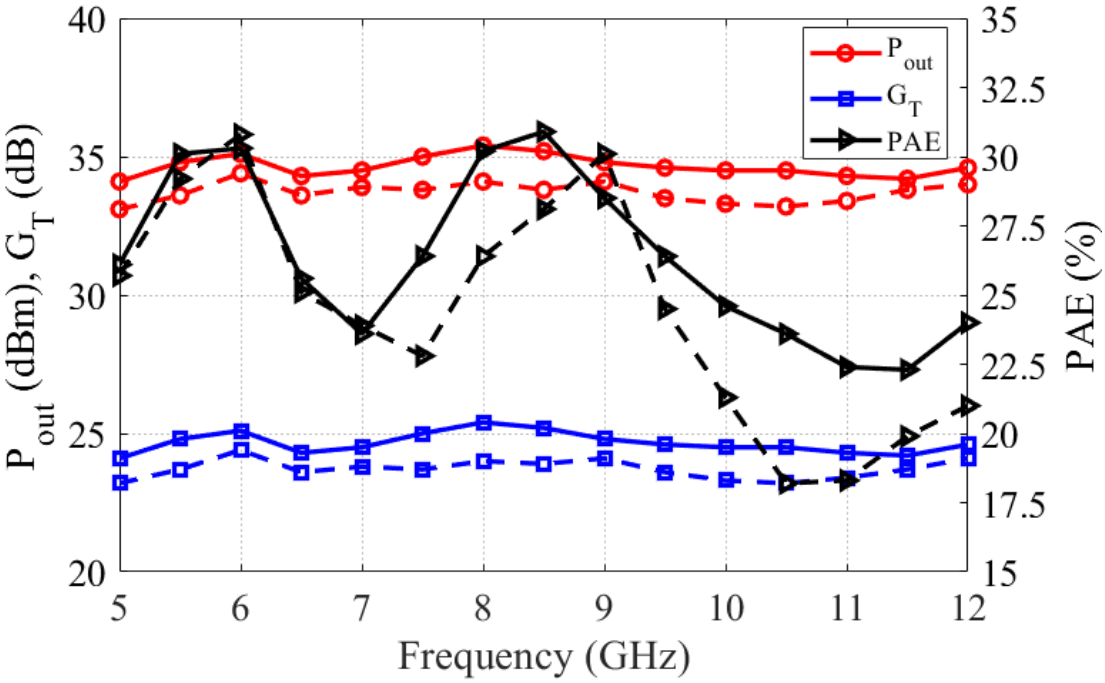


Figure 5.4: DA MMIC large-signal measurement (dashed lines) at 10 dBm available input. Model-based simulation (solid) is also plotted.

The input power was swept from -15 dBm to 13 dBm and the large-signal parameters: Output power, transducer gain, and PAE were measured. The measurement stop condition was set at a gain compression of 9 dB. This means that

the input power continued to increase until the amplifier's small-signal transducer gain was compressed by 9 dB. The input power sweep covers both, the small signal as well as the non-linear operation mode of the amplifier. The large-signal measurement as a function of input power for a single MMIC at 12 GHz is shown in Figure 5.5. It can be seen from this curve that as the input power increases, the gain starts to compress as the amplifier goes into the non-linear operating region. As the gain compresses, the power continues to increase. At a certain input level (approximately 11 dBm in this case), the output power saturates. As the input power is further increased, the PAE starts to decrease. This is because the output power has saturated but the HEMTs continue to draw more drain current. This drain current increases the DC power consumption, leading to a decrease in PAE. Therefore, an optimum operating input power of 10 dBm was chosen at which all specifications were satisfied for the frequency range of interest.

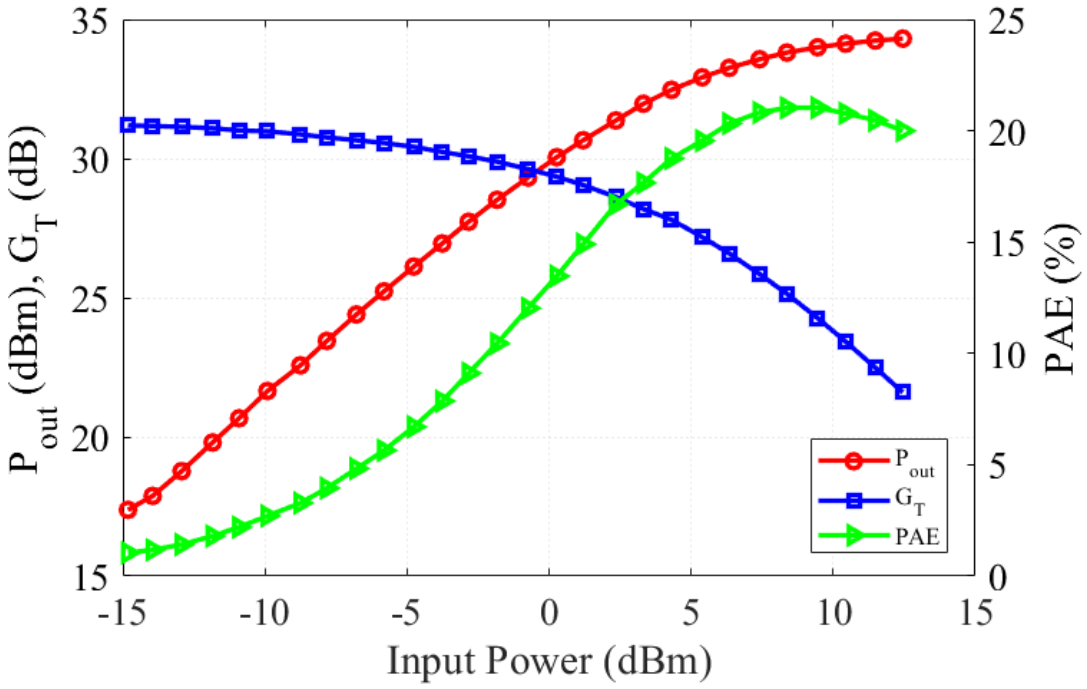


Figure 5.5: DA MMIC large-signal measurements performed on-carrier at 70°C as a function of input delivered power.

5.3 MMIC Linearity Measurements

The linearity of the DA was characterized by performing 2-tone measurements and observing the output power using a spectrum analyzer. The results are plotted in Figure 5.6. The input signals were generated using a signal generator at a separation of 10 MHz: at 7.995 GHz and 8.005 GHz. From the large-signal input power sweep measurements, the input power until which the device is operating in the linear region was determined. Since the OIP3 must be measured under small-signal conditions, the input powers were swept from -20 dBm to -15 dBm. To verify that the measurements were performed under linear operating conditions, it was ensured that the slope of the fundamental tone with respect to the change in input power was 1, while for the third-order intermodulation products, the slope was 3.

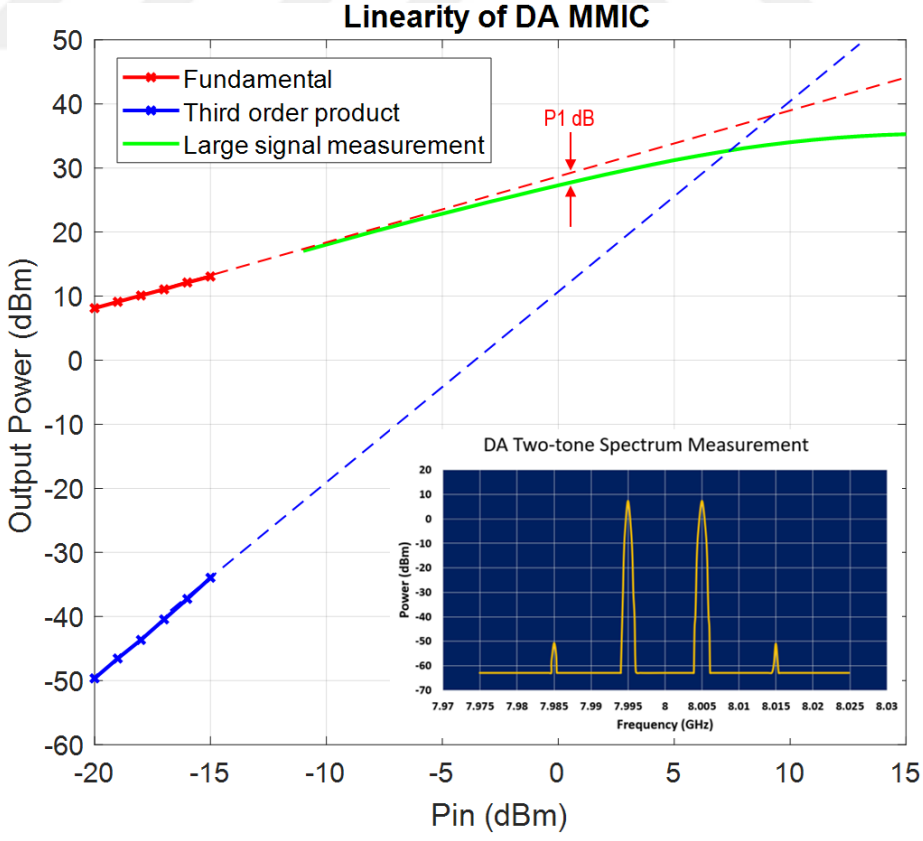


Figure 5.6: DA MMIC two-tone measurements for linearity characterization.

The fundamental output power for an input available power of -20 dBm was

8.3 dBm, while for the third order interm-modulation products generated at 7.985 GHz and at 8.015 GHz, was almost -50 dBm. The fifth-order intermodulation products could not be observed because of the low input power and high noise level of the spectrum analyzer. The extrapolated interception point of the fundamental and the third-order intermodulation products, which defines the OIP3 level, was determined as 37.7 dBm. The P1dB, which is the input power at which the DUT transducer gain is compressed by 1 dB was observed at an input power of 1 dBm. Table 5.2 summarizes the comparison between the simulated and the measured large-signal performance of the DA MMIC.

Parameter	**Simulation**	**Measurement**
$\mathbf{P_{out}}$	35.0 dBm	33.8 dBm
$\mathbf{G_T}$	24.9 dB	23.8 dBm
PAE	29.2%	24.2 %
OIP3	33.4 dBm	37.7 dBm

Table 5.2: DA MMIC Large signal response comparison between the simulation and the measurement. Typical values at 10 dBm input available power have been quoted for P_{out}, G_T and PAE.

Chapter 6

Conclusion & Discussions

For almost all communication systems, RF amplifiers are necessary. DAs can either be used in the transmitter chains to drive the high-power amplifiers feeding the antenna or in receive chains to further amplify the low-power signals from low-noise amplifiers. Broadband driver amplifiers provide the user with the flexibility to choose the most convenient frequency band or to switch from one band to another. MMICs are used because of their reliable reproducibility, low cost, compactness, and low weight. Accurate scalable HEMT models are important tools to help implement new MMIC designs quickly without the need to fabricate and characterize HEMTs beforehand. Powerful ASM HEMT models coupled with EM-simulation techniques can help extract reasonably good HEMT models.

Focusing on the C– and X– bands, a medium powered DA MMIC is designed using NANOTAM's GaN-On-SiC 250 nm technology. The MMIC achieves both, good small signal as well as large signal responses. Attaining an output power density of 2.68 W/mm, while having good reflection losses and small-signal gain ripple for such a bandwidth, using only conventional matching techniques is promising. Furthermore, such a low ripple for output power and large signal gain is among the lowest reported for MMICs in this frequency range of interest.

To the best of my knowledge, there are no reported GaN-based medium-powered (less than 3 W) DAs in the frequency band 5–12 GHz. Thus, a comparison with other state-of-the-art DAs that have comparable fractional bandwidths and output powers is made in Table 6.1. For a fractional bandwidth greater than 82 %, this MMIC has a typical small signal gain of 29.7 dB with a gain ripple of ± 1.4 dB, an IRL of 10.5 dB and an ORL 8.5 dB. It has a minimum saturated output power of 2.14 W corresponding to an output power density of 2.68 W/mm and an output power ripple of only ± 1.1 dB. The PAE is also greater than 18.4% which is reasonably high for a broadband design. When compared to other works, this DA presents the highest small signal gain and power density and also a very competitive ORL, small signal gain ripple, and saturated output power ripple. Only [18] has a better ORL and power ripple gain, but its fractional bandwidth is less than the proposed DAs.

Ref.	Specification							
	Freq. (GHz)	S21 (min) (dB)	IRL (dB)	ORL (dB)	Psat (W)	ΔS21 (dB)	ΔPsat (dB)	Power Density (W/mm)
[12]	6-18	-	7.5	-	0.5	-	±7.0	0.31
[13]	2-10	7	5	8	1.4	±2.5	±1.4	0.88
[14]	2-18	18	13	6	0.8	±2.5	±2.5	0.33
[17]	6-20	12.5	14	8	0.4	±2.5	±1.1	1.25
[18]	6-12	21	9	11	2.0	±2.0	±0.4	-
[19]	8-13	14.5	11	5	0.9	±0.6	±2.0	0.94
This work	5-12	28.3	10.5	8.5	2.12	±1.4	±1.1	2.68

Table 6.1: Comparison of broadband driver amplifiers having comparable fractional bandwidths and similar output powers.
Quoted values have been estimated from respective graphs and figures if they are not explicitly mentioned. Minimum values of PAE and P_{sat} have been reflected in this table.

As part of future works, the HEMT model's response and its scalability will be further improved. The model must be capable of estimating the HEMT response up to relatively higher frequencies and down to DC. The HEMT will be made scalable as a function of the drain and source pad pitches. In addition to EM simulations, other powerful tools like Silvaco TCAD and COMSOL will be used to improve the accuracy of the extracted scalable extrinsic parasitic parameters. With the help of broadband matching techniques like feedback matching and distributed matching, the response of the DA will be further improved. Such non-conventional techniques will also help to design a more area-efficient design.

Bibliography

[1] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151–1159, 1988.

[2] D. W. Runton, B. Trabert, J. B. Shealy, and R. Vetury, "History of GaN: High-power RF gallium nitride (GaN) from infancy to manufacturable process and beyond," *IEEE Microwave Magazine*, vol. 14, no. 3, pp. 82–93, 2013.

[3] M. Rudolph, "GaN HEMTs for low-noise amplification — status and challenges," in *2017 Integrated Nonlinear Microwave and Millimetre-wave Circuits Workshop (INMMiC)*, pp. 1–4, 2017.

[4] B. C. Akoglu, B. Sutbas, O. Cengiz, and E. Ozbay, "GaN based driver and power amplifier MMICs for X-Band transceiver modules," in *2019 IEEE 19th Mediterranean Microwave Symposium (MMS)*, pp. 1–4, 2019.

[5] U. Ozipek, A. Gurdal, B. Sutbas, B. C. Akoglu, and E. Ozbay, "Design and topology considerations for a family of X-Band GaN Power Amplifier MMICs," in *2019 IEEE 19th Mediterranean Microwave Symposium (MMS)*, pp. 1–4, 2019.

[6] A. Gurdal, U. Ozipek, B. Sutbas, and E. Ozbay, "A high gain and high efficiency 15 W X-band GaN power amplifier MMIC," in *2019 European Microwave Conference in Central Europe (EuMCE)*, pp. 10–13, 2019.

[7] V. Erturk, A. Gurdal, B. C. Akoglu, and E. Ozbay, "60W stacked-HEMT based asymmetric X-band GaN SPDT switch for single chip T/R modules,"

in *2023 18th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 265–268, 2023.

[8] V. Erturk, A. Gurdal, and E. Ozbay, "A high-power and broadband GaN SPDT MMIC switch using gate-optimized HEMTs," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 8, pp. 1207–1210, 2023.

[9] M. I. Nawaz, S. Zafar, B. C. Akoglu, G. T. Caglar, A. Hannan, E. Urfali, E. Aras, and E. Ozbay, "A highly survivable X-band low noise amplifier based on GaN HEMT technology and impact of pulse width on recovery time," *Microwave and Optical Technology Letters*, vol. 66, no. 9, p. e34330, 2024.

[10] M. Imran Nawaz, S. Zafar, A. Gurdal, B. Cankaya Akoglu, and E. Ozbay, "Robustness of GaN on SiC low-noise amplifiers in common source and cascode configurations for X-band applications," *International Journal of Circuit Theory and Applications*, vol. 52, no. 8, pp. 4148–4163, 2024.

[11] M. I. Nawaz, S. Zafar, B. C. Akoglu, E. Aras, and E. Ozbay, "GaN-based low noise flat gain amplifier for X-Band applications," in *2024 21st International Bhurban Conference on Applied Sciences and Technology (IBCAST)*, pp. 1–4, 2024.

[12] U. Schmid *et al.*, "Ultra-wideband GaN MMIC chip set and high power amplifier module for multi-function defense AESA applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, pp. 3043–3051, Aug. 2013.

[13] C. Meliani, R. Behtash, J. Wurfl, W. Heinrich, and G. Trankle, "A broadband GaN-MMIC power amplifier for L to X bands," in *2007 European Microwave Integrated Circuit Conference*, pp. 147–150, 2007.

[14] R. Santhakumar *et al.*, "Two-stage high-gain high-power distributed amplifier using dual-gate GaN HEMTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, pp. 2059–2063, Aug. 2011.

[15] *Broadband Amplifier Techniques*, ch. 11, pp. 297–300. John Wiley & Sons, Ltd, 2009.

[16] "QPA2213D." https://www.qorvo.com/products/p/QPA2213D.

[17] S. Zhang, J. Wan, J. Zhao, Z. Yang, Y. Yan, and X. Liang, "Design of a broadband MMIC driver amplifier with enhanced feedback and temperature compensation technique," *Electronics*, vol. 11, no. 3, p. 498, 2022.

[18] "TGA2598." https://www.qorvo.com/products/p/TGA2598.

[19] Y. Fan, J. Wan, Z. Yang, S. Zhang, J. Zhao, G. Gao, X. Zhang, H. Shen, N. Xiao, and Y. Zhang, "Coplanar asymmetry transformer distributed modeling for X-band drive power amplifier design on GaN process," *Electronics*, vol. 11, no. 16, p. 2478, 2022.

[20] R. Giofrè, P. Colantonio, F. Giannini, A. Pantellini, A. Nanni, C. Lanzieri, and D. Pistoia, "1–7 GHz single-ended power amplifier based on GaN HEMT grown on Si-substrate," in *2012 7th European Microwave Integrated Circuit Conference*, pp. 425–428, 2012.

[21] Z. Cheng, D. Zhu, G. Yan, G. Liu, and S. Gao, "A 3–7 GHz GaN HEMT power amplifier," *Microwave and Optical Technology Letters*, vol. 58, no. 4, pp. 901–904, 2016.

[22] R. Giofre, P. Colantonio, and F. Giannini, "X-band MMIC GaN power amplifier for SAR systems," *Microwave and Optical Technology Letters*, vol. 55, no. 11, pp. 2611–2616, 2013.

[23] K. Harrouche and F. Medjdoub, *GaN-Based HEMTs for Millimeter-wave Applications*, ch. 3, pp. 99–135. John Wiley & Sons, Ltd, 2020.

[24] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 85, pp. 3222–3233, 03 1999.

[25] U. Ozipek, "Design of an X-band GAN based microstrip MMIC power amplifier," Fubruary 2019.

[26] D. A. Neamen, *Microelectronics: circuit analysis and design*, vol. 43. McGraw-Hill New York, 2007.

[27] D. M. Pozar, *Microwave engineering: theory and techniques*. John wiley & sons, 2021.

[28] G. Chen, V. Kumar, R. Schwindt, and I. Adesida, "A low gate bias model extraction technique for AlGaN/GaN HEMTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 7, pp. 2949–2953, 2006.

[29] G. Crupi, D. Xiao, D.-P. Schreurs, E. Limiti, A. Caddemi, W. De Raedt, and M. Germain, "Accurate Multibias Equivalent-Circuit Extraction for GaN HEMTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 10, pp. 3616–3622, 2006.

[30] D. Resca, A. Raffo, A. Santarelli, G. Vannini, and F. Filicori, "Extraction of an extrinsic parasitic network for accurate mm-Wave FET scalable modeling on the basis of Full-Wave EM simulation," in *2008 IEEE MTT-S International Microwave Symposium Digest*, pp. 1405–1408, 2008.

[31] R. S. Pengelly, "Microwave field-effect transistors - Theory, design and applications," *NASA STI/Recon Technical Report A*, vol. 83, p. 10876, Jan. 1982.

[32] A. Jarndal and G. Kompa, "A new small-signal modeling approach applied to GaN devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3440–3448, 2005.

[33] F. Diamand and M. Laviron, "Measurement of the extrinsic series elements of a microwave mesfet under zero current conditions," in *1982 12th European Microwave Conference*, pp. 451–456, 1982.

[34] R. G. Brady, C. H. Oxley, and T. J. Brazil, "An improved small-signal parameter-extraction algorithm for GaN HEMT devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 7, pp. 1535–1544, 2008.

[35] K. Lee, K. Lee, M. Shur, T. T. Vu, P. Roberts, and M. Helix, "Source, drain, and gate series resistances and electron saturation velocity in ion-implanted GaAs FET's," *IEEE Transactions on Electron Devices*, vol. 32, no. 5, pp. 987–992, 1985.

[36] R. A. Minasian, "Simplified GaAs MESFET model to 10 GHz," *Electron. Lett.*, vol. 13, no. 8, pp. 549–541, 1911.