T.R.
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INSTITUTE OF GRADUATE STUDIES
DEPARTMENT OF PHYSICS

COMPREHENSIVE INVESTIGATION ON THE ELECTRICAL CHARACTERISTIC AND IRRADIATION RESPONSE OF SIC MOS CAPACITORS WITH EU_2O_3 DIELECTRICS

DOCTOR OF PHILOSOPHY, PHYSICS

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TO MY FAMILY

ABSTRACT

COMPREHENSIVE INVESTIGATION ON THE ELECTRICAL CHARACTERISTIC AND IRRADIATION RESPONSE OF SIC MOS CAPACITORS WITH EU_2O_3 DIELECTRICS
PHD THESIS
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This study provides an in-depth analysis of Al/Eu_2O_3/SiO_2/4H-SiC MOS capacitors, employing a dual gate dielectric stack of Eu_2O_3 and SiO_2 on 4H-SiC to enhance device performance. The transition in film structure due to heat treatment was confirmed through X-ray diffraction and atomic force microscopy, revealing optimal crystallization and reduced stress at 800 °C. Electrical measurements show that moderate temperature annealing enhances capacitance stability and decreases interface state density, leading to adjustments in flat band voltage. The device characteristics were notably affected by series resistance. The presence of thermally grown SiO_2 was found to enhance the electrical properties of the devices even at higher annealing temperatures. However, a significant degradation in barrier height was observed, likely attributed to carbon migration and the formation of parasitic silicates at temperatures above 600 °C. On the other hand, the effect of X-rays on the structural and electrical properties of Eu_2O_3 dielectric thin films was studied. The films were exposed to different periods of radiation, and their structural modifications were evaluated using X-ray diffraction (XRD). Meanwhile, the electrical properties were measured by capacitance-voltage (C-V) and conductance-voltage (G/ω-V) techniques. The results indicated that longer exposure to radiation resulted in a decrease in lattice strain and an increase in crystal volume, which can be attributed to the local heating and rearrangement of atoms induced by radiation. Electrical analysis revealed slight shifts in the flat voltage and mid-gap due to defects induced by radiation, affecting the charge-trapping behavior. Despite these defects, the dielectric material showed stable electrical performance under the tested radiation conditions, indicating its potential for use in radiation-resistant electronic devices. These results confirm the potential application of Eu_2O_3 films as a highly efficient dielectric material in such technologies. It can be said that this research demonstrates a promising insulating structure on 4H-SiC that balances crystallinity and defect control, which makes MOS devices a suitable candidate for future applications.

KEYWORDS: 4H–SiC, MOS Capacitor, Eu_2O_3, MOS Irradiation, High-k

ÖZET

Eu_2O_3 DİELEKTRİKLİ SİC MOS KAPASİTÖRLERİNİN ELEKTRİKSEL ÖZELLİKLERİ VE RADYASYON CEVAPLARININ DETAYLI İNCELENMESİ
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Bu çalışma, cihaz performansını artırmak için 4H-SiC üzerinde Eu_2O_3 ve SiO_2'den oluşan çift kapılı bir dielektrik yığını kullanan Al/Eu_2O_3/SiO_2/4H-SiC MOS kapasitörlerinin derinlemesine bir analizini sunmaktadır. Isıl işlem nedeniyle film yapısındaki geçiş, X-ışını kırınımı ve atomik kuvvet mikroskobu ile doğrulanmış ve 800 °C'de optimum kristalleşme ve azaltılmış stres ortaya çıkarılmıştır. Elektriksel ölçümler, orta sıcaklıkta tavlamanın kapasitans kararlılığını artırdığını ve arayüz durum yoğunluğunu azalttığını, bunun da düz bant voltajında ayarlamalara yol açtığını göstermektedir. Cihaz özellikleri, seri dirençten önemli ölçüde etkilenmiştir. Termal olarak büyütülmüş SiO_2'nin varlığının, daha yüksek tavlama sıcaklıklarında bile cihazların elektriksel özelliklerini iyileştirdiği bulunmuştur. Ancak, muhtemelen karbon göçüne ve 600 °C'nin üzerindeki sıcaklıklarda parazitik silikatların oluşumuna atfedilen bariyer yüksekliğinde önemli bir bozulma gözlemlenmiştir. Öte yandan, X-ışınlarının Eu_2O_3 dielektrik ince filmlerin yapısal ve elektriksel özellikleri üzerindeki etkisi incelenmiştir. Filmler farklı radyasyon maruziyet sürelerine bırakılmış ve yapısal modifikasyonları X-ışını kırınımı (XRD) kullanılarak değerlendirilmiştir. Bu arada, elektriksel özellikler kapasitans-voltaj (C-V) ve iletkenlik-voltaj (G/ω-V) teknikleriyle ölçülmüştür. Sonuçlar, radyasyona daha uzun süre maruz kalmanın kafes gerginliğinde bir azalmaya ve radyasyonla indüklenen atomların yerel ısınmasına ve yeniden düzenlenmesine atfedilebilen kristal hacminde bir artışa yol açtığını göstermiştir. Elektriksel analiz, radyasyonla indüklenen kusurlar nedeniyle düz voltajda ve orta boşlukta hafif kaymalar olduğunu ve yük tutma davranışını etkilediğini ortaya koymuştur. Bu kusurlara rağmen, dielektrik malzeme test edilen radyasyon koşulları altında kararlı bir elektriksel performans göstermiştir ve bu da radyasyona dayanıklı elektronik cihazlarda kullanım potansiyelini göstermektedir. Bu sonuçlar, Eu_2O_3 filmlerinin bu tür teknolojilerde oldukça verimli bir dielektrik malzeme olarak potansiyel uygulamasını doğrulamaktadır. Bu araştırmanın, kristalinite ve kusur kontrolünü dengeleyen 4H-SiC üzerinde umut verici bir yalıtım yapısı ortaya koyduğu ve bu nedenle MOS aygıtlarını gelecekteki uygulamalar için uygun bir aday haline getirdiği söylenebilir.

ANAHAR KELİMELER: 4H–SiC, MOS Kapasitör, Eu_2O_3, MOS Işınlama, Yüksek-k

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LIST OF ABBREVIATIONS AND SYMBOLS

AFM : Atomic Force Microscopy
A : Area of Gate Electrode
C_{ox} : Dielectric Capacitance
D_{it} : Interface Trap Density per Energy Level
Eu_2O_3 : Eubium Oxide
E_g : Band Gap Energy
E_c : Energy Level of Conduction Band
E_v : Energy Level of Valance Band
eV : Electron Volt
e : Electron
Gy : Gray
HfO_2 : Hafnium Oxide
h : Hole
MOS : Metal Oxide Semiconductor
MOSFETs : Metal Oxide Semiconductor Field Effect Transistor
N_{it} : Interface Trap Density
n_i : Intirinsic Carrier Concentration
Q_m : Mobile Ionic Charges
Q_f : Fixed Charge Density in Dielectric Layer
Q_{ox} : Trapped Charge Density in Dielectric Layer
Q_{it} : Trapped Charge Density at Interface
Q_{eff} : Effective Charge Density in Device Structure
q : Electrical Charge
RMS : Averarge Surface Rougness
SiO_2 : Silicon Dioxide
Si : Silicon
T : Temperature in Kelvin
μp : Mobility of Hole
μs : Effective Surface Mobility
V_{th} : Threshold Voltage
V_{ox} : Voltage Drops in Dielectric
V_{FB} : Flat band voltage
V_G : Gate voltage
V_d : Drain Voltage
XRD : X-ray Diffractometer
χi : Electron Affinity of Dielectric layer

χ : Electron Affinity of Semiconductor

ψ_B : Fermi Potential Respect to Midgap Edge

ϕ : Fermi Poteltial Respect to Conduction/Valance Band Edge

ϕ_S : Surface Potential

ϕ_m : Work Function of Metal

ϕ_S : Work Function of Semiconductor

ε_S : Dielectric Constant of Semicondutor

ε_i : Dielectric Constant of Insulator

ε_0 : Permitivity of Free Speace

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1. INTRODUCTION

1.1 An Overview of Metal-Oxide-Semiconductor (MOS) Devices

Metal-oxide-semiconductor devices have played a crucial role in the development of modern electronics. From their humble beginnings to becoming a cornerstone of technology, their evolution has transformed industries and enabled a range of devices that power our daily lives. MOS devices have become the foundation for a myriad of applications in modern electronics. They are essential components in smartphones, computers, digital cameras, and many other digital devices. MOS devices consist of a semiconductor material, usually silicon, covered with a thin layer of insulating oxide and integrated with metal gates, allowing for efficient control of electrical currents. The two main types of MOS devices - NMOS (n-channel MOS) and PMOS (p-channel MOS) - have unique properties that cater to a variety of electronic applications. Thanks to their versatility, MOS technology has found wide-ranging applications such as MOSFET (metal-oxide-semiconductor field-effect transistor) (Kahng, 1976). This is the most common type of MOS device used to amplify or switch electrical signals and MOS capacitors. This is the simplest type of MOS device used to store electrical charge. Although MOS devices offer significant advantages, such as low power consumption and small size, they also exhibit disadvantages, including susceptibility to voltage fluctuations, hot carrier degradation, and radiation exposure. The history of metal-oxide semiconductor devices (MOS) constitutes a pivotal chapter in the development of modern electronics technology, profoundly influencing both the design and functionality of integrated circuits. Metal-oxide semiconductor devices, characterized by their unique structure and operating mechanisms, have facilitated the miniaturization of electronic components, enabling their ubiquity in a variety of electronic devices. The origins of semiconductor technology can be traced back to the early 20th century when scientists began exploring the properties of semiconductor materials. The foundation for semiconductor devices was laid with the development of semiconductor theory in the 1930s and 1940s. Key discoveries included the understanding of p-n junctions and the behavior of P-type and N-type charge carriers in semiconductors. However, the turning point in the history of semiconductors came with the introduction of the first transistor in 1947 by

John Bardeen, Walter Brattain, and William Shockley at Bell Labs. This invention marked the transition from vacuum tubes to solid-state devices, paving the way for future developments. In the late 1950s, the concept of the metal-oxide-semiconductor field-effect transistor began to emerge. The first successful transistor was demonstrated by Muhammad M. Atalla and Dawn Kang at Bell Labs in 1959 (Brinkman et al., 1997; Kahng, 1960). By using a thin layer of oxide as an insulator, their invention enabled the flow of current to be controlled using an electric field, greatly improving the performance and compactness of the device compared to previous technologies. The 1960s and 1970s saw rapid advances in MOSFET technology as researchers began to improve manufacturing techniques, leading to the integration of multiple MOSFET transistors on a single chip. This period produced the first commercially viable MOS devices that were used in calculators and early computers. In 1971, Intel released the first microprocessor, the 4004, which used MOS technology. This product demonstrated the potential of MOS devices, revolutionizing the electronics industry. Complementary metal oxide semiconductor (CMOS) technology also emerged as an effective alternative to traditional MOSFET transistors. CMOS uses both N-type and P-type MOSFET transistors to reduce power consumption. In 1980, the first commercially successful CMOS chip was manufactured. This enhanced the potential of MOS technology in various applications, including microprocessors, memory devices, and digital logic circuits (Bhuyan, 2017). The 1980s and 1990s saw rapid progress in CMOS technology driven by the continuous miniaturization of transistors, which enabled the production of MOS devices with dimensions approaching nanometers, known as Moore's Law (the shrinking of integrated circuits). This stimulated research and development efforts around the world. As the twenty-first century entered, the challenges brought by the shrinking size of transistors became clear. Issues such as short-channel effects, increased leakage currents and power dissipation have been major obstacles to further scaling down MOS technology. In response, researchers have begun exploring alternative materials and structures, including high-efficiency k-isolators and FinFETs, which maintain efficient performance at smaller scales. These innovations are giving new life to Moore’s Law. Today, MOS devices are small in size, low power consumption and high reliability, but challenges remain. These major challenges and limitations facing MOS devices,

as the semiconductor industry moves towards smaller dimensions in modern electronic systems, stem from the management of power dissipation, leakage currents and trapped charges in sub-micron devices. Future research may focus on overcoming these limitations to further improve device performance and integration. The future of MOS devices remains promising (Pearson and Brattain, 1955).

1.1.1 Silicon Carbide and its Technological Impact

Silicon carbide is a compound of silicon and carbon, known for its exceptional hardness. Its wide band gap of about 3.2 eV allows for greater power conversion efficiency, higher blocking voltage, and improved temperature stability compared to silicon-based semiconductors with a band gap of about 1.1 eV. The impact of SiC (silicon carbide) technology on electronic applications has been profound. Silicon carbide technology has revolutionized the electronics industry by developing high-performance devices with improved efficiency, reliability, and power handling capabilities, especially in high-power, high-frequency, and high-temperature applications. Silicon carbide is a semiconductor compound that has gained significant attention in recent years due to its unique properties and wide-ranging applications in modern technology. As industries strive for greater efficiency and sustainability, silicon carbide is emerging as a critical material that can enhance performance in various sectors, including powerful electronics, automotive, and telecommunications. Silicon Carbide offers a unique combination of physical and electrical properties that set it apart from traditional silicon-based semiconductors. The properties of silicon carbide are fundamental to its effectiveness as a semiconductor and its technological impact. Silicon carbide has a unique crystalline structure that allows for a high degree of hardness and thermal stability. This structure not only contributes to its durability but also allows silicon carbide to maintain performance under extreme conditions, making it an ideal choice for high-temperature applications. Some of the most notable properties of silicon carbide are its high thermal conductivity, which exceeds that of conventional silicon, allowing it to dissipate heat efficiently in electronic components (operating at higher temperatures than silicon) (Wutikuer, 2016). This property is critical in rugged electronics, where managing thermal performance is vital for reliability, longevity, and operating at

higher power levels without overheating. Additionally, silicon carbide exhibits electrical resistance, making it an excellent insulator under certain conditions. Silicon carbide has a wider band gap than silicon, resulting in a higher breakdown voltage, and better radiation resistance. Due to its higher breakdown voltage, silicon carbide can withstand higher electric fields, making it suitable for high-voltage applications. Silicon carbide is chemically inert (chemically stable), making it resistant to corrosion and oxidation, which extends the life of the device. Silicon carbide devices can turn on and off faster than their silicon counterparts, improving efficiency in switching applications. The low leakage currents of silicon carbide result in lower power consumption and improved device performance. Silicon carbide-based MOS capacitors can be used in radiation-hardened electronics for applications such as aerospace and nuclear power. The integration of silicon carbide into power electronics not only enhances energy efficiency but also significantly reduces power losses, which is critical in a world that seeks sustainability. One of the most important advantages of conventional silicon (Si) is its thermal oxidation, as the generated oxide (native oxide) acts as a stable insulator in MOS applications (Salinaro, 2016). Therefore, silicon-based MOS devices have performed well, and silicon carbide has this property because it supports the growth of thermal silicon oxide films. Despite its advantages, silicon carbide technology faces challenges, including the high cost of substrates and manufacturing processes. Silicon carbide-based devices can be more expensive to manufacture than silicon-based devices. However, as research advances and production techniques improve, these costs are expected to decrease. Silicon carbide semiconductor technology is used in various sectors, including:

Power electronics, where silicon carbide transistors and diodes are increasingly used in power conversion systems, including inverters for renewable energy systems and electric vehicles. Due to its thermal stability, silicon carbide is ideal for applications in harsh conditions (high-temperature environments), such as oil drilling equipment and aerospace components. Silicon carbide's ability to operate at high frequencies and withstand high voltages makes it suitable for radio frequency and microwave applications, such as radar systems and satellite communications. Silicon Carbide's broadband semiconductor

technology has had a significant impact on electronic applications. It has enabled the development of high-performance devices with improved efficiency, reliability, power handling capabilities, and reduced size and weight. The increasing use of silicon carbide technology in various industries has the potential to revolutionize the way we use and utilize electronic devices in the future (Pushpakaran et al., 2016; Chieh Kao, 2015).

1.1.2 High-k Dielectrics

Insulators are generally materials with high electrical resistance and low conductivity, which impede the flow of electrical current, protect users from electrical shock, and ensure the proper functioning of electrical devices. High-k dielectrics are materials with high relative permeability, which have become essential in modern electronics, especially as gate insulators in semiconductor devices. These materials are essential for improving the electrical performance of devices by allowing greater capacitance without increasing the physical thickness of the insulating layer. “k” stands for dielectric constant, which is a measure of a material’s ability to store electrical energy. The higher the dielectric constant, the more charge the material can hold without allowing it to leak out. Traditional insulators such as silicon dioxide have served well for decades. But with technological advances, and the demand for smaller, faster, and more efficient devices, these materials are reaching their limits. This is where high-k materials come in, offering a way to maintain or even improve their insulating properties while allowing for further shrinkage of device dimensions. Integrating high-k dielectrics into metal-oxide-semiconductor devices addresses many of the key challenges associated with shrinking device dimensions. With conventional silicon dioxide insulator layers ineffective at these scales, high-efficiency materials (e.g., hafnium oxide) provide a powerful alternative to better control the gate over the channel region and electric fields, leading to dramatically improved performance in metal-oxide-semiconductor transistors (Wilk et al.,2001). As researchers strive to make transistors smaller and more efficient, when silicon dioxide becomes too thin, it begins to leak excessive current, leading to increased power consumption and reduced device reliability. Due to the high gate leakage current due to the thin silicon dioxide gate insulator, inefficient devices are created. It has become necessary to replace the silicon dioxide insulator with

other suitable and good gate insulators such as high-k dielectrics, which have a high resistance to current flow due to the polarization of electric charges within the insulator in the presence of an applied field (Boukortt, 2016). Insulators can be made substantially thicker while maintaining the same electrical properties as the thin silicon dioxide layer. This also greatly reduces the leakage current and allows devices to operate more efficiently, extending their life. The electric field in an MOS device is generated by the voltage applied to the gate terminal, which affects the behavior of charge carriers in the channel. The strength of this electric field is determined by the gate voltage and the thickness of the insulating layer. In K-dielectrics, the movement of electric charges is primarily influenced by external factors such as electric fields. When an electric field is applied to a MOS device, it creates a potential difference that drives the movement of charge carriers (electrons and holes) within the insulating layer. This movement is critical to the overall performance of the device. The strength and composition of the electric field in MOS devices can significantly change how charges move within the k-dielectric. A stronger electric field can lead to a higher density of charge carriers, affecting the conductivity and operating speed of the device. Conversely, weaker electric fields can lead to lower charge mobility, leading to inefficiency. Understanding this relationship not only helps improve device performance but also encourages the development of new materials and designs for future electronic applications. Although high-k dielectrics have the advantages of reducing tunneling currents, reducing leakage, achieving the same capacitance with a thicker layer, and better charge storage, they are not without their drawbacks. One of the drawbacks of high-k dielectrics is that they can exhibit poorer interface quality with silicon, resulting in increased trap density and differences in electrical properties. Material selection: Selecting the right high-K material and optimizing process conditions is critical, as different materials can have varying effects on device performance. Potential applications for high-K dielectrics extend beyond transistors and capacitors to advanced integrated circuits, memory devices, and other critical electronic components as well. Dielectrics are essential for modern electronics technologies, enabling the continued miniaturization and performance of semiconductor devices. Their development and integration are key factors in advancing electronic materials science (Lavallée, 2013).

1.1.3 Aim and Scope of the Study

Rare oxides are an integral part of modern technology. They are materials of great importance in various scientific fields and play a prominent role in semiconductor technology. Oxides are compounds consisting of at least one oxygen atom and another element. "Rare oxides" refers to oxides of rare earth elements in general. These oxides are characterized by a high dielectric constant and a large energy band gap. It is necessary to be careful and careful in choosing suitable materials for manufacturing devices that have good specifications and are resistant to the processes that are performed on them. Among the rare oxides, (Eu2O3) is a good insulator, a basic component in many electronic applications, and a promising element in future device technology. It is characterized by a high dielectric constant (k = 14) compared to traditional silicon dioxide (3.9) and high thermal stability. It is a good conductor of heat and is characterized by its chemical stability and a large energy band gap (4.4 electron volts). It has many uses such as communications, microelectronics, and optical devices. Despite the advantages and applications of insulators (rare oxides) in general in all fields of electronic device technology (Petit et al.,2005; Singh and Shivashankar,2005), there are still obstacles for these devices such as interface states within the oxide layer, reliability of devices under radiation exposure, and manufacturing problems. Within the scope of this thesis, a MOS capacitor device was fabricated, and we used Europium oxide as a high-efficiency gate insulator instead of traditional silicon dioxide (Kumar et al., 2015). The device was studied and investigated in detail in terms of its use in normal conditions at room temperature without radiation exposure and the resistance of the device and the failure mechanism were also investigated after many times of radiation exposure and the radiation source used was X-rays. The fabrication and all scientific experiments were carried out in the Nurdam Laboratories at Abant Izzet Baysal University Bolu, Turkey.

1.2 Structure of Metal-Oxide-Semiconductor (MOS)

1.2.1 Ideal MOS Structures

The term MOS refers to three interconnected parts: metal - oxide - semiconductor. The MOS structure, as mentioned in the term, consists of a

semiconductor (Si or SiC) covered by an insulator (SiO_2 or another insulator) on which a conducting electrode is deposited as shown in Figure 1.1 (Wutikuer, 2016). The conditions that must be met in an ideal MOS structure are: 1) When the work function of the silicon Φ_S is equal to the work function of the metal Φ_m, when no voltage is applied to the structure. 2) The electric field is zero, meaning that there is no charge in the oxide or at the SiO_2/Si interface, when no voltage is applied to the structure. MOS capacitors play a prominent role in the field of microelectronics, especially in transistors, which are the basic building blocks of modern electronic devices. There are three important areas or regions when studying the properties of the device: accumulation, depletion, and inversion. The behavior of MOS capacitors in these three regions is affected by many factors such as local oxide thinning and surface chemical treatments. Understanding these factors is essential in the context of enhancing the performance of electronic devices to manufacture MOS capacitors with the best quality and high reliability. The behavior of charge carriers in a MOS capacitor is in equilibrium when the gate voltage is zero, meaning that there is no voltage applied to the gate. This equilibrium changes significantly when an external voltage is applied, affecting the charge distribution inside the MOS device and there is a relative shift of the Fermi level for the metal and semiconductor. Through the capacitance measurements of the MOS capacitor, we obtain a lot of information about the quality of the oxide. There are three different bias states for the MOS capacitor and to understand these states where three different bias voltages are applied which are (1) greater than the flat band voltage V_{FB} (2) the middle of the flat band voltage V_{FB} and the threshold voltage V_{th} (3) less than the threshold voltage V_{th}. Before going into explaining these biases, we would like to define the terms flat band voltage and threshold voltage to simplify the understanding (Morkoç, 2020).

Flat Band Voltage

It is the voltage difference between the accumulation layer and the depletion layer, if the semiconductor and the metal are isolated by an oxide layer between them, then in this isolated state all the energy bands are flat and this is the flat band. When the voltage is equal to the difference in work function (Φ_s - Φm) between the work function of the semiconductor and the work function of the metal, then the ideal flat band condition is achieved. If ($V_{FB} = \Phi_{sm}$), this is

called the flat band potential, the flat band potential is flat when there is no applied voltage ($V_G = 0$). Changing the applied voltage will change the flat band potential (the curvature of the energy bands changes after they are flat). Figure 1.2 shows the flat band potential،work function of a metal and a semiconductor at zero bias (Ytterdal et al., 2003).

Threshold Voltage

It is the voltage difference between the depletion and the inversion layer, and it is an important parameter that greatly affects the electrical properties of MOS based devices. In transistors, it affects their performance as the threshold voltage determines when the transistor is on or off. Changing the bias voltage of the device may modify the threshold voltage, which affects the input and output characteristics of some devices. It is symbolized in some sources by V_{TN} or V_T instead of V_{th} (Jaeger, 2016; Ytterdal et al., 2003).

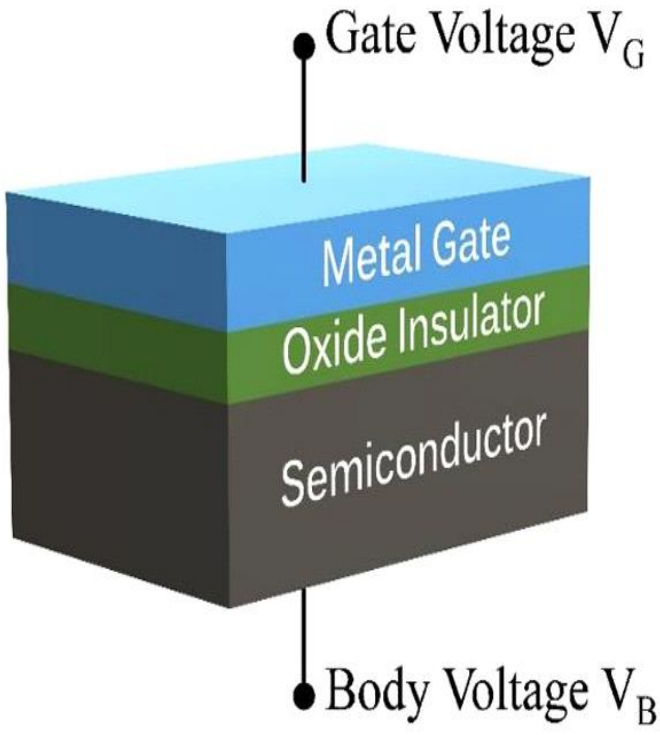

Figure 1.1. MOS Capacitor Structure (Wutikuer, 2016)

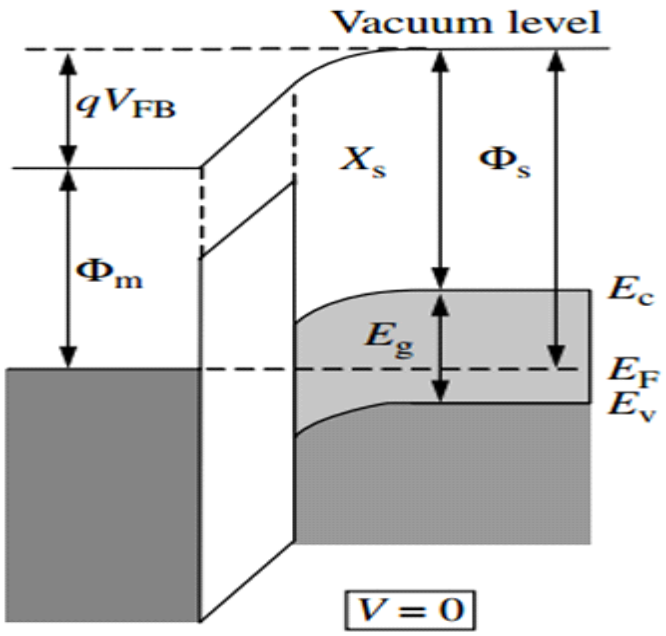

Figure 1.2. Band diagrams of MOS capacitor at zero bias (Ytterdal et al., 2003)

1.2.1.1 Accumulation

As shown in Figure 1.3a (Jaeger, 2016) when an external voltage (V_G) is applied to the MOS capacitor structure, i.e., a positive bias is applied to the gate, the electrons are attracted by the positive charges to form an accumulation layer. The accumulated electrons with high concentration represent the other pole of the two-plate capacitor parallel to the first pole at the gate. In other words, when the concentration of the dominant carrier in the silicon is less than the concentration of the dominant carrier at the oxide/silicon interface, the majority carriers are drawn towards the interface, creating a multi-carrier region and the semiconductor surface becomes covered with majority carriers. This bias is known as accumulation. In this region, the energy band at the semiconductor surface bends upward when it is of the P-type and downward when it is of the N-type (as in Figure 1.4a) (Sze and LEE, 2010) and thus the majority carriers are on the semiconductor surface. The accumulation occurs at the positive gate voltage where the applied voltage is greater than the plate voltage ($V_{FB} < V_G$) and the capacitance is high. Here the capacitance of the Cox oxide is the capacitance of the parallel plate capacitor. The high capacitance of the accumulation layer is necessary for many electronic applications and the charge on the gate is opposite in sign to the charge in the semiconductor. The accumulation is used in the

MOSFET transistors in the on state to create a channel between the source and the drain (Bentarzi, 2011).

1.2.1.2 Depletion

After the formation of the accumulation layer, i.e., the formation of the capacitor, with the increase in the gate voltage, the separation distance between the capacitor plates increases and the capacitance decreases. Silicon is neutral in all its aspects when the electrons leave the accumulation layer after removing the positive charges from the gate. In this case, the gate bias is called the flat band voltage. A region is formed on the surface that is depleted of carriers and is then called the depletion region. In other words, when the gate bias increases, the holes move towards the interface of the oxide and the substrate. This leads to the formation of a layer in which the concentration of electrons decreases, and thus the electrons are depleted from the oxide/silicon interface (the majority carriers are repelled from the interface, which creates a region depleted of carriers and the surface of the semiconductor becomes free of majority carriers). The energy band at the surface of the semiconductor bends upward when it is of the P- type and downward when it is of the N- type (Figure 1.4b) (Sze and LEE, 2010). This is in the form of a barrier that prevents the majority carriers from reaching the interface. The conditions for the occurrence of the depletion state are when the gate voltage (V_G) is between the flat band voltage (V_{FB}) and the threshold voltage (V_{th}). [(V_{th}) > (V_G) > (V_{FB})] as shown in Figure 1.3b (Jaeger, 2016; Bentarzi, 2011).

1.2.1.3 Inversion

When the voltage applied to the gate increases, the electrons are attracted upwards, and the electron density exceeds the hole density. Then the polarity of the interface reverses from P-type (substrate polarity) to N-type polarity. This high electron density arises from the generation of electrons and holes in the depletion layer. The inversion layer is formed, which is a very thin layer and is completely separated from the silicon layer by the depletion layer. It is possible that the charge density in this layer is able or unable to follow the alternating change in the applied gate voltage. There are two cases for the applied frequency, high frequency and low frequency. The voltage at which the inversion layer is

formed is called the threshold voltage V_{th}. When V_G exceeds the threshold voltage V_{th}, this layer is formed, and the capacitance increases again. In this case, the energy band at the semiconductor surface is clearly bent upward for P-type semiconductors and downward for N-type semiconductors (as shown in Figure 1.4c) (Sze and LEE, 2010). This leads to the trapping of the majority carriers at the interface. The reflection occurs when $V_G >> V_{th}$. One of its uses is that it is used as a conducting channel between the source and drain in MOSFET transistors as shown in Figure 1.3c (Jaeger, 2016; Bentarzi, 2011).

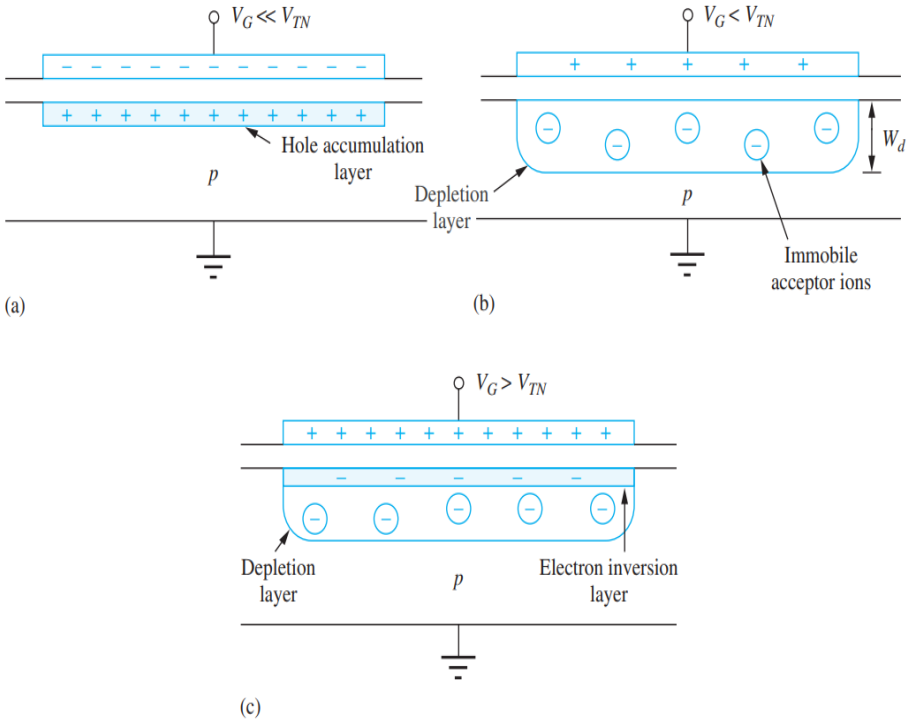

Figure 1.3. MOS capacitor (a) accumulation (b) depletion (c) inversion (Jaeger, 2016)

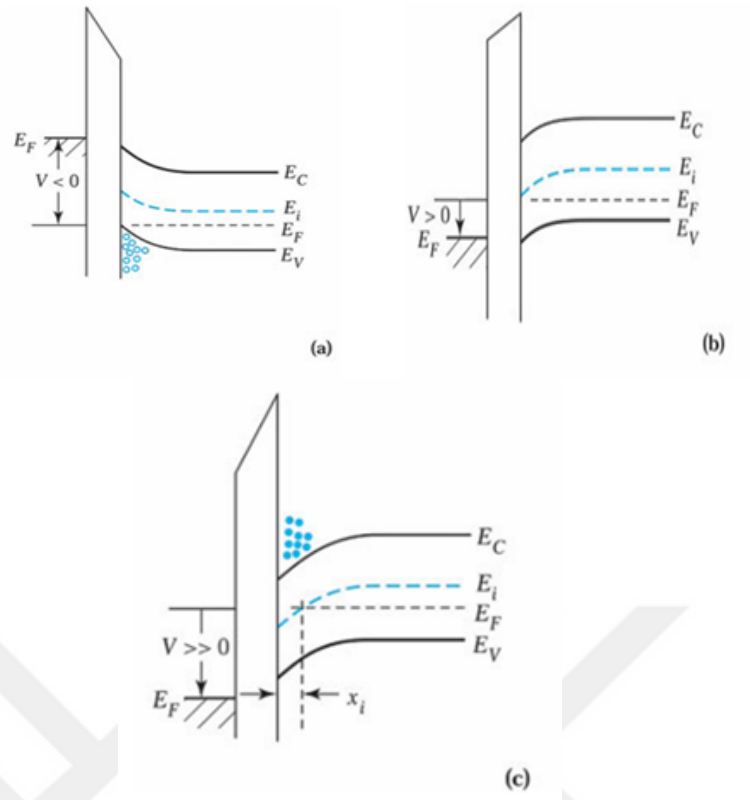

Figure 1.4. (a) Accumulation (b) depletion and (c) inversion of a p-MOS capacitor (Sze and LEE, 2010)

1.2.2 Non-Ideal MOS Structure

By comparing the C–V characteristics measured in the ideal case of a MOS capacitor and the non-ideal case, we find a clear difference between the two cases, as the C–V characteristics measured in the MOS capacitor actually deviate due to many reasons that have a prominent role in affecting the operation of the MOS capacitor and thus have an actual role in the poor performance of the device (device instability). The performance of manufactured MOS devices depends on these reasons, and among these reasons, for example, is the presence of (fixed charge - mobile Ionic charge - interface charge - oxide charge) inside the oxide layer and at the SiO_2/Si interface as shown in Figure 1.5 (Wutikuer, 2016; Morkoç,2020).

1.2.2.1 Mobile Ionic Charges

Mobile ionic charges are ionic impurities that can diffuse across the oxide layer of a MOS capacitor such as K^+, Na^+ and possibly negative ions that can be generated during the manufacturing process or from the environment, and

depending on the voltage applied to the gate, they affect the C-V curves and cause the C-V curve to shift towards negative bias. The presence of any charge in the oxide is caused by a neighboring charge in the substrate with opposite polarity, and the ions near the SiO_2/Si interface are opposite to the charges in the substrate. They can cause the threshold voltage to shift in devices because these charges create an electric field that opposes the gate voltage, thus changing the operating point of the device. Over time or due to temperature, the threshold voltage may vary, making the device operation difficult to control and reducing its reliability and instability. Because they are constantly moving mobile charges, they cause an increase in the leakage current through the oxide layer, which increases the energy loss of the devices and reduces their efficiency. Because of these effects, the performance of the devices in general decreases (Wutikuer, 2016; Salinaro, 2016).

1.2.2.2 Fixed Oxide Charges

These are fixed charges, as their name suggests, they do not move within the oxide layer. They are positive charges present at the SiO_2/Si interface, which arise due to oxidation, annealing, radiation damage, or impurities. There is no electrical contact with silicon (substrate). Temperature plays a major role in this charge. The higher the temperature, the lower the charge. Therefore, oxidation or annealing at high temperatures is not permissible. That is, there is a different relationship between the charge, oxidation, and annealing. These charges cause the C-V curve to shift towards negative bias. They may shift the threshold voltage of the device, but because they are fixed and immobile, the threshold voltage shift is more stable. When devices with a very thin gate oxide layer, fixed oxide charges play a role in the instability of the device and also play a role in increasing the leakage current, which increases the device's energy consumption. Using high-quality oxide materials with low impurity and defect rates reduces fixed oxide charges, and good control of the oxide growth process is also another factor in reducing these charges. For devices exposed to radiation, radiation-hardened oxide materials can be used to reduce the generation of static oxide charges (Estève, 2011; Salinaro, 2016).

1.2.2.3 Oxide Trapped Charges

Oxide trapping charges are electrically charged defects present in the insulating oxide layer of metal-oxide-semiconductor (MOS) devices away from the oxide-semiconductor interface. These charges can be either positive or negative, depending on the nature of the defect. They are produced when positive from holes and negative from electrons trapped in the oxide. They can be trapped by radiation, or they can be produced by processes that produce both electrons and holes or by other defects. Annealing processes can help redistribute trapped charges within the oxide layer, reducing their overall effect on the behavior of the device. The use of high-quality insulating materials and post-fabrication treatments can reduce the number of trapped charges. Oxide trapping charges because a shift in the C-V curve similar to fixed oxide charges (a shift in the flat-band voltage). The density of oxide trapping charges can be determined from the shift in the flat-band voltage. The effect of trapped oxide charges varies greatly depending on the type of MOS device and the specific application. For example, for NMOS and PMOS devices, the effect of trapped oxide charges on threshold voltage or mobility is lower in NMOS than in PMOS, but the mobility is lower in PMOS than in NMOS. The accumulation of trapped oxide charges over time can lead to reliability issues in MOS devices. These charges can lead to device instability, especially in devices exposed to radiation. These charges can act as recombination centers, reducing the life of semiconductor devices (Kahraman et al., 2020; Estève, 2011).

1.2.2.4 Interface Trapped Charges

They are positive or negative charges present at the SiO_2/Si interface arising due to defects in the MOS structure, oxidation defects, impurities or radiation. There is an electrical contact with silicon (substrate). They are also called interface states or surface states. There are two types of them, acceptor and donor. These charges are either positively or negatively charged depending on whether they are of the donor or acceptor type or at the Fermi level. These types of charges are more complex than their counterparts because they are distributed at different energy levels within the energy gap and influence the shift of the C-V curve. The charges trapped at the interface may generate noise in the devices and lead to device degradation. These charges can cause a shift in the threshold

voltage and increase the leakage current of the devices. The use of damping techniques such as hydrogenation helps to reduce them, micro processing techniques and the use of high-quality gate oxides with low density of interface states help to reduce the charges trapped at the interface (Kahraman et al., 2020; Fleetwood et al., 1993).

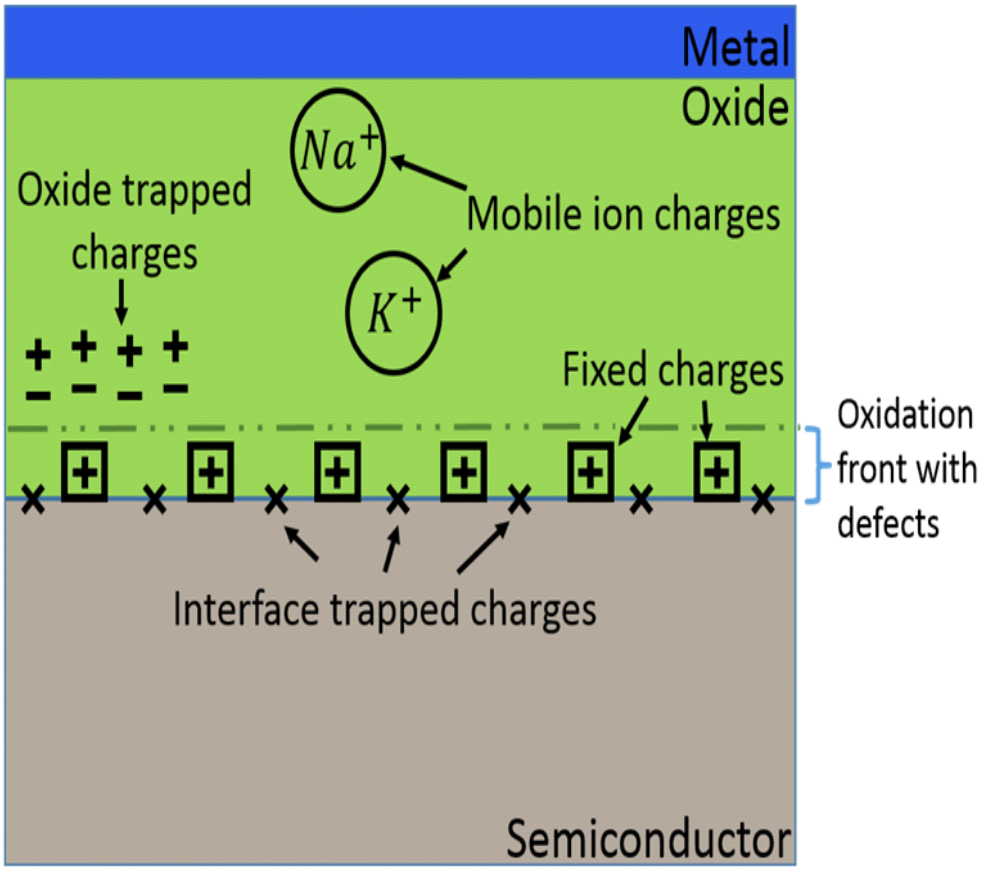

Figure 1.5. Oxide and interface charges in a MOS capacitor (Wutikuer, 2016)

1.2.3 Investigation of Interface and Oxide States Density at MOS Devices

In the ideal MOS capacitor structure, there are no oxides, impurities, or defects inside the structure, but in a real capacitor, we find a group of charges and defects that are formed after the completion of the fabrication of the structure. There are non-mobile charges inside the MOS structure, such as fixed charges in the oxide, charges trapped in the oxide and interface states, and mobile charges such as positive or negative ions. Studying these charges and defects is important for researchers because these charges present inside the oxide and at the SiO_2/Si

interface can pose a problem in determining the threshold voltage and dispersing carriers via the Coulomb scattering mechanism, thus affecting the movement of carriers. Among the defects present at the interface may cause the breakdown of the insulator when they are abundant in the insulator, and over time the number of charges may change, which also affects the properties of the device. Among these defects, such as dangling bonds and Si-Si bonds, they can capture and release electrons and holes and be electrically active, affecting the movement of the channel. The interface states or surface states are basically distributed energies as shown in Figure 1.6 (Chieh Kao, 2015) within the band gap and continuing to the conduction and valence bands of silicon. The density of interface states is symbolized by the symbol (D_{it}). There are two types of interface states, like donor states and like acceptor states. These donor and acceptor states are either neutral or charged. The donor states are neutral when occupied by an electron and positively charged when empty, while the acceptor states are the opposite, neutral when empty and negatively charged when occupied by an electron. At the SiO_2/Si interface, all states in the upper part of the band gap (above the middle gap) represent acceptor like and all states in the lower part of the band gap (below the middle gap) represent donor like with the intrinsic Fermi level of silicon (E_i is the intrinsic (fundamental) Fermi level located in the middle of the energy gap at absolute zero temperature) as shown in Figure 1.7. If the Fermi level is aligned with the intrinsic Fermi level ($V_G = V_{midgap}$), then the interface states are neutral. The interface states have an effect on the C–V curves, shifting them to the left if they are of the donor type, and when the shift is to the right, the interface states are of the acceptor type from the ideal direction (Wutikuer, 2016).

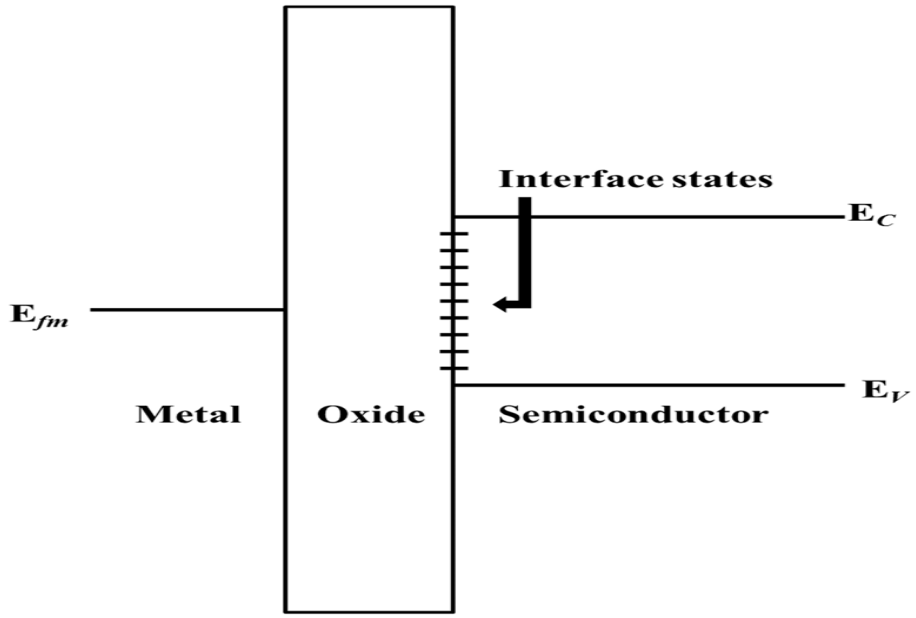

Figure 1.6. Energy-band diagram of a MOS structure (Chieh Kao, 2015)

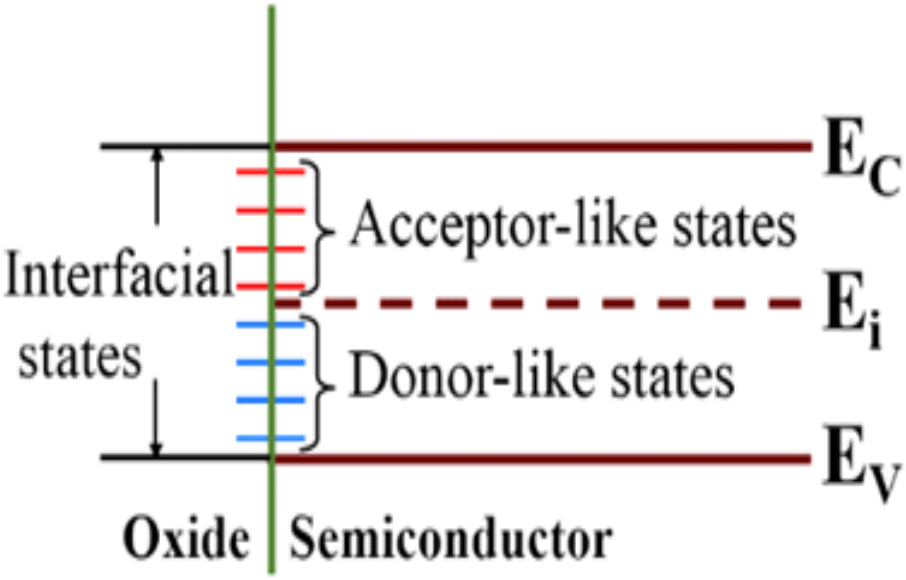

Figure 1.7. Interfacial states (Wutikuer, 2016)

1.2.3.1 Capacitance Methods

MOS capacitors differ from conventional capacitors, but there are basic concepts common between the two, such as capacitance, which is a physical quantity that expresses the storage capacity of the capacitor. A conventional capacitor consists of two homogeneous parallel plates insulated with a thin insulating layer used to store electrical charges, and the distribution of charges on

each plate is the same amount and opposite in sign, and the larger the capacitance of the capacitor, the larger the number of charges on each plate, and the capacitance can be expressed as follows:

$$C = \frac{Q}{V} \tag{1.1}$$

Where C is the capacitance of the capacitor and its unit is farad, Q is the charge on each plate and its unit is coulomb, and V is the voltage applied to the capacitor and its unit is volts. As for the MOS capacitor, it differs from the conventional capacitor because the capacitance changes with the applied voltage. The MOS capacitor also consists of two terminals with an insulator in the middle. The gate insulator, usually SiO_2 or another insulator, is sandwiched between the two electrodes, the gate electrode and the semiconductor electrode (substrate). The gate is biased (when voltage is applied) and the substrate is grounded. The gate voltage affects the distribution of charges inside the MOS capacitor. The MOS capacitor can be biased into three regions (accumulation - depletion - inversion). The capacitors can be connected in series or in parallel. The MOS capacitor is similar to the conventional capacitor in the accumulation region. The capacitance of the MOS capacitor is variable. When the gate voltage changes, the capacitance value changes. This is what distinguishes it from the conventional capacitor, where the capacitance is constant regardless of the applied voltage. There are many techniques to determine the interface state density and series resistance, including capacitance methods. There are three methods for capacitance: The first method was designed by Terman, which is the high-frequency capacitance (C_{HF}) (Chieh Kao, 2015). In this region, the signal frequency is greater than (105 Hz). At high frequencies the interface traps do not follow the AC signal superimposed on the DC signal applied to the gate and thus do not contribute to the total capacitance. The total capacitance of the MOS capacitor is given by:

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}} \tag{1.2}$$

Where C_{ox} oxide capacitance and C_{sc} space charge capacitance (Kahraman et al., 2020; Tataroglu and Altındal, 2008). The second method was designed by Bergland, this region is created when the signal frequency is very low (C_{LF}) (less

than 10 Hz) (Chieh Kao, 2015). In this method the interface traps follow the AC signal and thus contribute to the total capacitance of the device. In this case the capacitance of the structure is equal to or equivalent to the capacitance of the oxide layer as was the case in the accumulation region. The total capacitance of the MOS capacitor is given by:

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_{sc} + \left(\frac{C_{it}}{1+\omega^2\tau_{it}^2}\right)} \tag{1.3}$$

Where C_{it} interface trap capacitance τ_{it} relaxation time ω angular frequency (Kahraman et al., 2020). The third method was designed by Vapaille and Castagne, in this method the high frequency and low frequency methods are combined (Chieh Kao, 2015). Figure 1.8 shows high and low frequency.

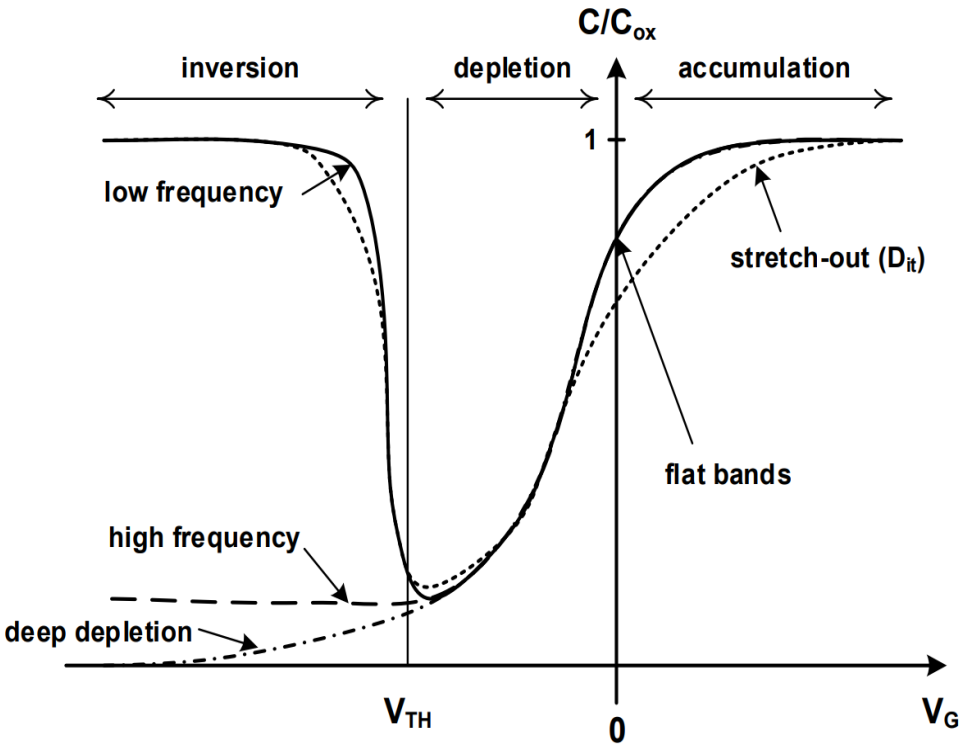

Figure 1.8. C-V measurements at high and low frequency (Salinaro, 2016)

1.2.3.2 Conductance Methods

The conduction method was first used by Nikulian and Gotzberger. The conduction technique is one of the most important methods to characterize the interface states so that we can get information about the traps such as their location in the band gap or their concentration and evaluate the interface trap

density. In this method, we get enough information as we can collect information about the channel in the upper or lower half of the silicon band gap using P-type or N-type capacitors, and by combining the results we get enough information. The conduction technique is based on the conduction losses resulting from the exchange of majority carriers between the interface states and the majority carrier band in semiconductors when a small AC signal is applied to the MOS structures. In this method, C-V and G/ω–V plots are required at different frequencies of the applied bias voltage. Conductance measurements are essential to characterize the electrical properties of MOS capacitors as they provide insights into the performance and behavior of the device. By analyzing the conduction curves, it is possible to extract useful information about the manufacturing process of MOS capacitors and identify defects resulting from the process and to evaluate the reliability and determine the failure mechanisms. This method is used in research and development in studying the physics of MOS devices and developing new device structures (Tataroglu and Altındal, 2008; Selcuk and Ocak, 2007; Dokme et al., 2008).

1.3 Radiation Effect on MOS Structure

1.3.1 Radiation Interaction with Matter

When radiation such as charged particles or uncharged objects (electromagnetic waves) encounters matter, a set of interactions occur between the radiation and the atoms or molecules that make up the matter. The extent and type of these interactions depend on the properties of both the radiation and the material targeted by the radiation. These interactions include scattering, where the radiation deviates from its original path due to the interaction of the radiation with the atoms and molecules of the material. There are two types of scattering: elastic (no energy transfer) and inelastic (energy transfer). Absorption, where energy is absorbed by the atoms or molecules, leading to the excitation or ionization of the target atoms. Transmittance, which indicates that the radiation passing through the material does not undergo scattering or absorption. There are interactions of electromagnetic radiation (uncharged particles) such as gamma rays and X-rays and charged particles such as electrons and alpha particles and the emission of electromagnetic radiation by charged particles due to deceleration

in matter (Bremsstrahlung radiation) and therefore the study and understanding of these interactions with matter is very necessary (Fabjan and Schopper, 2020; Cern, 2018; Sedl´aˇckov´a, 2014).

1.3.1.1 Charged Particle Irradiation Interaction with Matter

Charged particles (electrons, protons and alpha particles) interact with matter through several processes and change the physical and chemical properties of matter, so these interactions and changes are worthy of study and attention. Interactions such as inelastic collisions: In these collisions, the charged particle loses part of its energy, and this happens with electrons as follows: When charged particles transfer energy to an atomic electron, raising it from a lower energy state to a higher energy state, this process is called excitation, and can lead to the emission of light and the creation of stable states in matter. When charged particles transfer enough energy to remove an electron from an atom, this leads to the creation of electron-hole pairs, and this process is called ionization and can lead to the formation of defects in matter. When a charged particle passes through a medium at a speed greater than the speed of light in that medium, it emits electromagnetic radiation (Cherenkov radiation), and this is called (light emission), and here too it loses part of its energy in the form of light. The energy deposited by charged particles can heat the material, which is due to thermal expansion of the material or melting (loss of energy in the form of heat). Elastic collisions: In these collisions, the charged particle collides with the nuclei elastically, i.e. it does not lose energy when the charged particle deviates from the nucleus due to Coulomb repulsion (Rutherford scattering). At high energy levels, the particles can interact directly with the nucleus, leading to nuclear reactions. When slowed down by the electric field of the nucleus, it emits electromagnetic radiation (emitting a photon). Obviously, there are factors that affect these interactions, including the energy of the particle (affecting the extent of its interaction with the material) and the density and composition of the material. Charged particles are used in cancer treatment and studying the effect of radiation on matter (Fabjan and Schopper, 2020; Cern, 2018; Sedl´aˇckov´a, 2014).

1.3.1.2 Neutral Particles and Electromagnetic Irradiation Interaction with Matter

There are different mechanisms for the interaction of neutral particles and electromagnetic radiation with matter. The interactions of neutral particles and electromagnetic radiation with matter are an important element for understanding the study of physics. The properties of neutral particles and electromagnetic radiation greatly affect the scattering and absorption of radiation by matter. First, neutral particles such as Neutrons and Neutrinos are particles that do not carry an electrical charge (uncharged), so their interaction with matter is not like charged particles because they do not interact with matter through the Coulombic force but instead interact through nuclear forces and weak interactions. Second, photons (electromagnetic radiation) such as X-rays and gamma rays are neutral particles that have no mass or charge, so their interaction with matter is through electromagnetic interactions. The following is a list of the main interactions. Neutron interactions such as:

Elastic scattering: Neutrons collide elastically with nuclei and transfer some of their energy to the nucleus (energy loss). Inelastic scattering: Here the neutron is absorbed (energy absorption) and gamma radiation is emitted after the nucleus returns to its ground state after excitation. Absorption: The nucleus can absorb neutrons, leading to reactions such as fission or transformation. Neutrino's interactions (weak interactions): Neutrinos interact with matter through the weak nuclear force. Photon interactions (electromagnetic radiation) such as: The photoelectric effect: The photon is absorbed by the atom, causing the electron to be ejected from the atom (such as X-ray imaging). Compton scattering: The photon collides with the electron, losing some of its energy and transferring it to the electron. Pair production: When a photon with an energy greater than (1.022 MeV) passes near the nucleus, it can be converted into an electron-positron pair (the energy of the photon is greater than the energy of the electron). Rayleigh scattering: Low-energy photons can be scattered by atoms. The mechanisms of these interactions include ionization and excitation, whereby particles and photons can ionize atoms by removing electrons from their original orbits and exciting atoms and molecules and raising them to higher energies, which leads to the emission of radiation or light after the excited atoms return to their original

places. These interactions depend on several factors such as the energy of the particle, the atomic number of the substance, and the density of the medium. Understanding these interactions is essential for many applications such as particle physics research, radiotherapy of patients, and the design of radiation detection devices. These interactions and their effects are complex and remain an area for further research and development (Bonaldo, 2019; Sedl´aˇckov´a, 2014).

1.3.2 Radiation Degradation on MOS Structure

The interaction of radiation with the materials in the MOS structure leads to various types of radiation-induced degradation. MOS structures, which are the building blocks of modern electronic devices, are adversely affected by radiation. Radiation affects MOS oxides strongly and these effects come about through 1) Charge build-up in the oxide trap (charge trapping): Ionizing radiation such as X-rays or gamma rays, can create pairs of electrons and holes in the oxide layer. Electrons typically have higher mobility and are captured at the gate, while holes, due to their lower mobility, tend to be trapped in the oxide layer, leading to a build-up of positive oxide charge. 2) Charge build-up in the interface trap (interface trap build-up): Radiation can also create defects at the interface between a semiconductor (such as silicon) and the gate oxide. These interface traps can act as recombination centers, trapping and releasing charge carriers, affecting the mobility within the oxide. Figure 1.9 illustrates the main steps of radiation-induced charge generation within an oxide from the moment of radiation incident on the structure through pair generation, hole movement, electron re-bonding, hole trapping, and hole or electron trapping at interface states. The effects of radiation-induced degradation in MOS structures manifest themselves in several ways: Displacement and charge trapping mechanisms can lead to a shift in the threshold voltage, reducing the efficiency of the device. Or radiation can create defect states that facilitate current paths, increasing leakage current and leading to increased power consumption. Or the cumulative effects of radiation damage over time can significantly reduce the operational life of electronic components, especially in satellite applications where devices are exposed to high radiation. Various forms of radiation can affect MOS structures including ionizing radiation: This type includes gamma rays and X-rays as mentioned above. Non-ionizing radiation: Such as ultraviolet radiation, which is

less harmful than ionizing radiation, but exposure over long periods can also cause degradation of devices. Neutron radiation: Can produce secondary charged particles, which can damage the displacement and further degrade electrical performance. To mitigate the effects of radiation degradation on MOS structures, techniques such as the use of radiation-resistant materials and device design modifications are used. Understanding the mechanisms of radiation-induced degradation in MOS structures is critical to the development and reliability of electronic devices in radiation-intensive environments, such as space applications and high-energy physics experiments (Schwank, 2007; Oldham et al., 1989; Bee, 1997; Pejović, 2012).

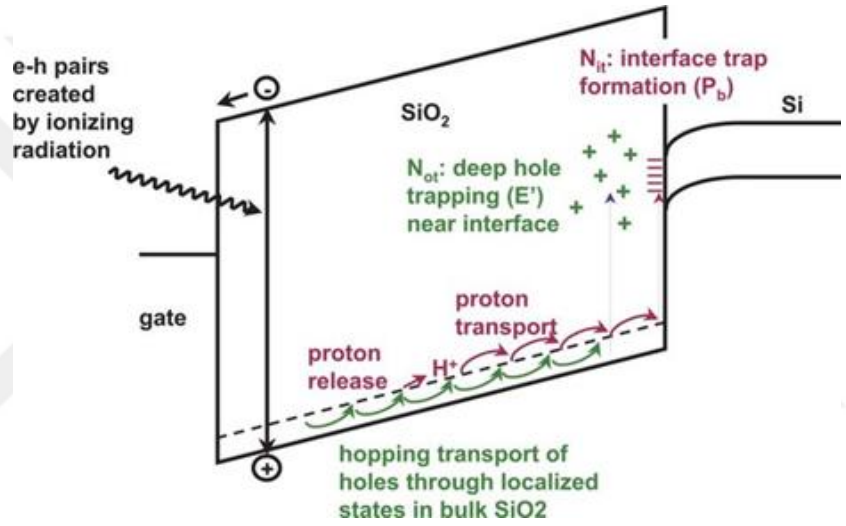

Figure 1.9. Band diagram of an MOS capacitator Illustrated are the main processes for radiation-induced charge generation (Schwank, 2007)

1.3.2.1 Initial Recombination/Initial Hole Yield

Understanding the fundamental mechanisms that govern the performance of capacitors under different conditions is crucial. One of these important issues is the interaction of ionizing radiation with these devices, which can induce primary recombination and affect hole production mechanisms. Primary recombination and primary hole yield in metal-oxide-semiconductor (MOS) capacitors due to radiation are fundamental concepts for understanding how radiation affects semiconductor devices. Primary recombination: This refers to the process by which electron-hole pairs generated by ionizing radiation recombine before they can contribute to current flow in a MOS capacitor. Upon exposure to radiation, the energy transferred to the semiconductor can create

electron-hole pairs in the semiconductor. Depending on the energy levels and trap states in the material, a portion of these charge carriers may recombine shortly after creation, resulting in a significant reduction in the effective charge that can be collected. Alternatively, the carriers may interact with impurities or defects in the semiconductor lattice, resulting in recombination. This recombination is a loss mechanism that reduces the overall hole yield. The recombination rate depends on factors such as the age and concentration of carriers and is affected by the presence of defects and impurities in the semiconductor material. Pairs are generated when an electron combines with a hole, transferring energy to a third charge carrier, which is then promoted to an excited state. This mechanism can lead to the generation of additional pairs of electrons and holes, contributing to the overall carrier gain. The density of these pairs depends on the type of radiation and energy, as well as the atomic structure of the material. Initial hole yield: This describes the number of holes created per unit energy deposited in the material during radiation. It is a critical parameter for determining how efficiently a semiconductor converts energy from radiation into usable charge carriers (Schwank, 2007). In a capacitor, the yield can be affected by factors such as Material properties: The band gap of a semiconductor material can affect recombination rates and hole yield. Electric field: The presence of an electric field in a capacitor can help remove charge carriers before they recombine, improving the initial hole yield. Interface states: The quality of the semiconductor-oxide interface plays an important role in determining hole production. Increased interface states can trap carriers, reducing the initial hole yield. Radiation type and dose: Different types of radiation and doses (fluxes) will generate different amounts of charge carriers. Carrier mobility: The greater the mobility, the greater the initial hole yield. The resulting holes may become trapped in defects within the oxide or at the oxide-semiconductor interface, which not only affects the effective hole yield but also the stability of the capacitance over time. Increased thermal energy can facilitate carrier mobility and enhance recombination, affecting hole yield. Excessive radiation exposure may increase recombination and trapping states but may ultimately degrade device performance. Investigating the initial recombination and hole yield provides insights into the extent of radiation effects on MOS capacitors (Oldham, 1989; Oldham, and McLean, 2003; Bee, 1997).

1.3.2.2 Hole Transport/ Short Time Recovery

Radiation significantly affects the hole transport properties of MOS capacitors through mechanisms such as trapping of charge carriers and modification of their transport properties. Studies indicate that ionizing radiation leads to the formation of localized states in the SiO_2 layer, which affects the kinetics of hole transport. While radiation generally degrades hole transport properties due to trapping and scattering, hole transport in MOS capacitors exposed to radiation is affected by various factors including temperature, electric field, and the nature of the defects induced by radiation. When radiation interacts with the oxide layer, the energy levels within the band gap of the semiconductor correspond to shallow and deep traps caused by these defects. The presence of these traps can either aid or hinder hole transport. Figure 1.10 shows the polaron jumps (the term polaron refers to the interaction that occurs between the hole and the medium through which it passes and during its passage creates a distortion in the lattice) for holes as it is clear that the holes are free of holes and after the hole is captured the energy decreases and after a period of time the hole shifts to the other position and the hole is in position number 2.Short-time recovery refers to the ability of MOS capacitors exposed to radiation to restore the charge movement and stability shortly after the radiation exposure stops. After the initial exposure to radiation, the effects caused by radiation may partially recover within a short period of time. The interaction between the removal and localization of holes makes it possible for carriers to neutralize some of the traps, which leads to reducing the trapped charge and improving the performance of the sound and thus enhancing the recovery rates. Short-time recovery is a dynamic process that can be affected by the temperature and energy levels created by the defects. The trapped holes can be redistributed back into the conduction band or recombine with electrons, which may restore the original capacitor properties to some extent. However, although short-term recovery techniques are effective, they may not fully restore all electrical properties to pre-radiation exposure levels (Milanowski, 1999; Bersuker et al., 2003; Pejović, 2012).

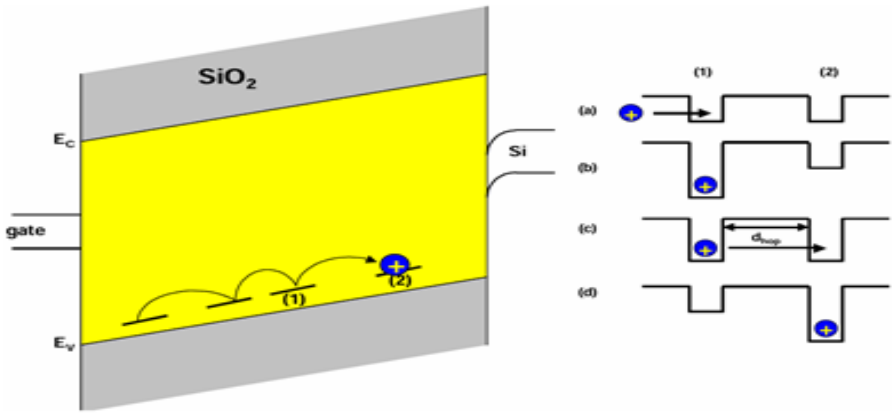

Figure 1.10. Illustration of the polaron hopping of the holes (a) Positions (1) and (2) are empty; (b) At position (1) a hole is taken(c) Stop for a period of time (d) Hole at position 2. (Milanowski, 1999)

1.3.2.3 Dose rate effects

In radiation environments, the effect of dose rate on devices (MOS capacitors) means that the performance and reliability of these devices are affected by the rate of exposure to ionizing radiation. The dose rate can be defined as the amount of ionizing radiation energy absorbed per unit time and is usually measured in grays per hour (Gy/h). Radiation-induced effects, such as the accumulation of positive oxide charge and the creation of interface traps, appear depending on the dose rate. Higher dose rates can lead to a faster accumulation of these radiation-induced effects, which can lead to a faster degradation of device performance. Conversely, lower dose rates can lead to a slower accumulation of radiation-induced effects, allowing device performance to be restored. The dose rate can affect the dynamics of charge transfer and trapping processes within the gate oxide. At higher dose rates, the rate of charge generation may exceed the rate at which charges can be transferred or neutralized, resulting in a greater accumulation of positive oxide charge. The dose rate can also affect the generation of interface traps, which can contribute to the overall degradation of performance caused by radiation. Radiation causes changes in the threshold voltage of MOS capacitors. The amount of shifts can depend greatly on the dose rate, for example at high dose rates there may be a larger and more immediate shift in the threshold voltage towards negative bias than at low dose rates. Degradation mechanisms such as displacement damage, ionization effects and defect generation within the dielectric material, the rate of these processes varies

widely with dose rate. Higher rates generally cause more degradation of devices exposed to radiation (Oldham and McLean, 2003; Barnaby and Marinella, 2013).

1.3.3 Theory of the Radiation Induced Traps

There are many defects that occur in devices due to exposure to ionizing radiation. Understanding the mechanisms of trap formation and their effects allows for improved device designs, which ultimately contributes to the advancement of electronics in all fields. The theory of radiation-induced traps in a capacitor (metal oxide and semiconductor) includes defects that arise in the oxide layer or at the interface between the oxide and the semiconductor due to exposure to ionizing radiation. These traps can capture and release charge carriers, resulting in shifts in the threshold voltage. The traps can facilitate tunneling currents, leading to increased leakage and decreased device reliability. Radiation-induced traps significantly affect the electrical properties of capacitors by changing the charge distribution and interface properties. The accumulation of traps either in the oxide or at the interface leads to shifts in the capacitance and voltage (C-V) characteristics and can lead to deterioration of device performance. The use of high-quality, radiation-hardened materials can reduce the susceptibility to trap formation (Oldham, and McLean, 2003; Bonaldo, 2019).

1.3.3.1 Defect Generated by Secondary Electrons in Impact Ionization Process

An important mechanism that contributes to defect formation is the ionization process caused by high-energy radiation, such as X-rays or gamma rays, when energetic photons collide with atoms in the silicon structure. An important result of these collisions is Compton scattering (a process in which a photon transfers some of its energy to the material). Compton scattering can eject electrons from the semiconductor. These high-energy secondary electrons can have enough energy to cross the SiO_2/Si interface, further contributing to the generation of electron-hole pairs within the silicon substrate or insulator. In a semiconductor, the energy absorbed from the radiation can excite electrons from their bound states in the atoms to higher energy states or release them completely, leading to ionization and the creation of electron-hole pairs that contribute to electrical conduction, where the resulting electron-hole pairs contribute to charge

transfer. In insulators, this process may require much more energy due to the larger band gaps, resulting in limited conduction. Figure 1.11 shows that the incident beam can overcome the binding energy between the atoms and thus generates a chain of secondary electrons capable of displacing the orbital electrons of the atom. As a result of this process, free electrons and holes are produced. Some of the free electrons may combine with the positively charged holes left by the ionization process. This recombination can lead to the emission of energy, often in the form of light (photons) as they move to lower energy states. The high-energy electrons generated may, in turn, cause further ionizations by colliding with other atoms, leading to a chain of electron generation. The free electrons may initially have high energy after the reaction. They can lose energy through collisions with other electrons or lattice atoms, eventually leading to thermal equilibrium with the material. The reaction can also create defects such as oxygen vacancies and suspended bonds between silicon and silicon oxide at the SiO_2/Si interface. These defects act as traps in the lattice structures. These defects can capture some of the generated electrons, effectively trapping them and creating localized charge carriers that can affect the electrical properties of the material. In general, the fate of the generated electrons depends on their initial energy, the properties of the material, and the presence of any traps or recombination centers (Brillson, 2023; Schwank, 2007).

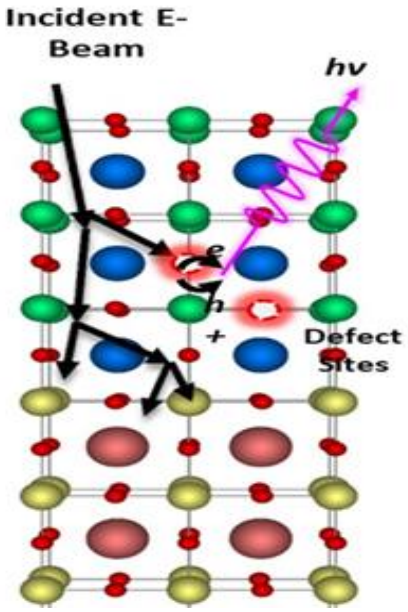

Figure 1.11. Consists of an incident beam generating a series of secondary electrons, and light (Brillson, 2023)

1.3.3.2 Defect Generated by Hole

Holes refer to the absence of electrons in the valence band of a semiconductor, which can act as positive charge carriers. Holes can be created during the manufacturing process (oxidation, heat treatment, or incorporation of impurities) or arise from external factors, such as ionizing radiation or thermal stress. Their presence can lead to several types of defects that can negatively affect device performance. When holes are present, they can create localized states at the interface between the oxide and the semiconductor. These interface states can trap charge carriers, resulting in increased dispersion and decreased mobility in the channel region. For example, in a MOSFET, the presence of these states contributes to threshold voltage shifts and can hamper the overall efficiency of the device. Holes can also interact with the insulating oxide layer, forming oxide traps. These traps can capture and release charge carriers, resulting in slower capacitance-voltage (C-V) characteristics of the MOS capacitor, changes in the oxide capacitance, and increased response time. The movement of holes within the SiO_2/Si interface generates defects. During its passage, it encounters unstable (stressed) Si–O bonds due to structural defects (lattice mismatch between the SiO2/Si interface and silicon) or due to external stress, which leads to their breakage and the formation of a defect or changes in the properties of the material (Bonaldo,2019). We notice from Figure 1.12a that the stressed Si–O bond is unstable, so it is natural to break this stressed bond (recombination process with the electron) by rearranging a new weak bond in place of the old broken bond, thus acting as an interface trap, as shown in Figure 1.12b. The density of defects resulting from holes in the interface or in the oxide layer can vary according to the processing conditions and the quality of the materials used, or due to an external influence. Over time, the accumulation of defects resulting from holes can lead to reliability problems such as oxide breakdown or insulator breakdown, which can lead to catastrophic failure of the device (Al-kofahi et al., 1997; Oldham, and McLean, 2003; Pejović, 2012).

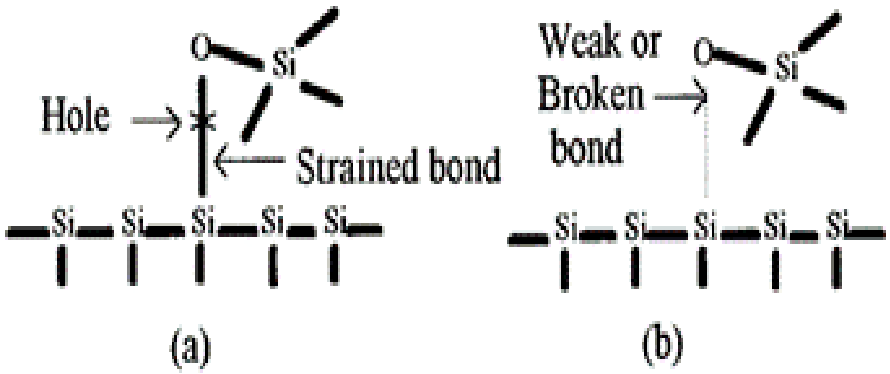

Figure 1.12. (a) Strained bond (b) new bond (Al-kofahi et al., 1997)

1.3.3.3 Defect Generation at Gate Oxide/ Semiconductor Interface

The silicon dioxide layer acts as an electrical insulator in various electronic applications. Among the various factors that can negatively affect the performance of electronic devices, defects at the interface between different materials stand out, especially phenomena such as interface traps. Interface traps are defects located at the boundaries between two different materials, such as between a semiconductor and an oxide layer or at heterojunctions where different semiconductors meet. Fast-switching traps (FST) represent a particular class of interface traps that have time constants in the order of nanoseconds or faster. This fast response time makes them particularly problematic in high-speed digital circuits. They can lead to a delay in the response of the transistor. Fast-switching traps are generated by electron-hole recombination at the SiO_2/Si interface. How to form interface traps: First, the holes trapped in the oxide react with the oxide mass (oxide defects containing hydrogen) and trap some of them and produce positive hydrogen ions +H, these positive ions move towards the SiO_2/Si interface under the positive applied voltage and from the silicon substrate, they pick up an electron that makes Ho active, where Ho react with the Si-H bond to form the H_2 molecule and the dangling Si∗ bonds (interface traps). As shown in the relationship: $SiH + Ho \rightarrow Si^{*} + H_2$

In other words, by hydrogen, the dangling bonds are passivated (electrically inactive) through the annealing process. During exposure to radiation by reacting with hydrogen, these bonds are stripped (bonds are broken) and as a

result a new defect appears at the SiO_2/Si interface called the lead center P_b (where Si∗ is the P_b center in the above relationship), from the lead centers that are abundantly present at the interface are the defects P_{b0} and P_{b1} as shown in Figure 1.13 (Poindexter et al., 1981; Barnaby and Marinella, 2013; Pejović,2012).

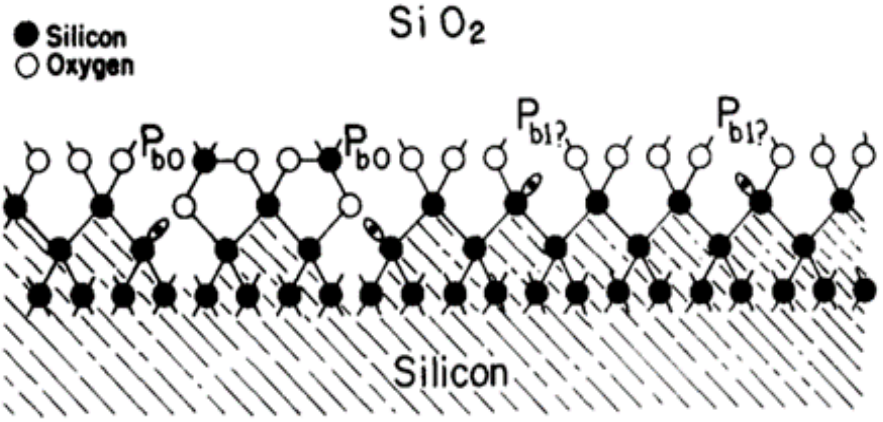

Figure 1.13. Illustration of the P_{b0} and P_{b1} interface trap defect (Poindexter et al., 1981)

During irradiation and when the electric field is low, the creation or formation of interface traps is greater. The disadvantages of interface traps are that they impede the movement of carriers, which leads to a change in the threshold voltage, as the threshold voltage decreases if the channel is of the P-type and increases if the channel is of the N- type (for transistors). Defects at this interface profoundly affect charge retention, leakage currents, and overall device reliability. The causes of defect generation at the gate oxide/semiconductor interface in general are: Radiation, mechanical effects, or changes in the crystal structure of semiconductors can lead to the formation of defects at the interface, High temperature changes during manufacturing processes can lead to the formation of defects such as impurities or heterogeneous regions, The difference in thermal expansion between oxides and semiconductors can lead to mechanical stress, causing defect formation, and Contamination of the manufacturing environment (exposure to moisture or harmful gases) during manufacturing can enhance defect formation (Bersuker et al.,2003; Brower,1998; Cartier and Stathis,1996).

2. MATERIALS and METHOD

2.1 Fabrication of MOS Capacitor

The N-type 4H-SiC wafer underwent a thorough cleaning to remove impurities, following the standard Radio Corporation of America (RCA) cleaning procedure, to prepare the Al/(Eu_2O_3/SiO_2/n-SiC) MOS capacitors. After the RCA cleaning, the SiC substrate was dried with nitrogen of 8N (%0.00000099) purity. The dried substrate was then placed in a diffusion oven, where SiO_2 was grown using the dry oxidation method at a furnace temperature of 900 °C. Pure oxygen gas was subsequently introduced to create a SiO_2 layer approximately 5 nm thick. After the deposition of the interfacial transition layer, a 120 nm thick Eu_2O_3 layer was applied to the substrates using an electron beam evaporation system. The resulting thin films were divided into five sections and subjected to nitrogen annealing for 120 minutes at five different temperatures: 200 °C (T-200), 400 °C (T-400), 600 °C (T-600), 800 °C (T-800), and 1000 °C (T-1000). The structural analysis of the films was performed using a Rigaku X-ray diffraction (XRD) instrument, utilizing CuKα characteristic X-rays with a wavelength of 1.5 Å, over a 2Θ range of 10° to 70°. The surface morphology of the Eu_2O_3 thin films was assessed through Atomic Force Microscopy (AFM), while the chemical changes in the surface films due to annealing were analyzed using Fourier-transform infrared (FTIR) spectroscopy. Subsequently, aluminum (Al) metal with a purity of 99.99% was deposited onto the front surface of all samples using a sputtering system equipped with a 1 mm diameter circular shadow mask. The entire backside was coated with silver to facilitate signal collection.

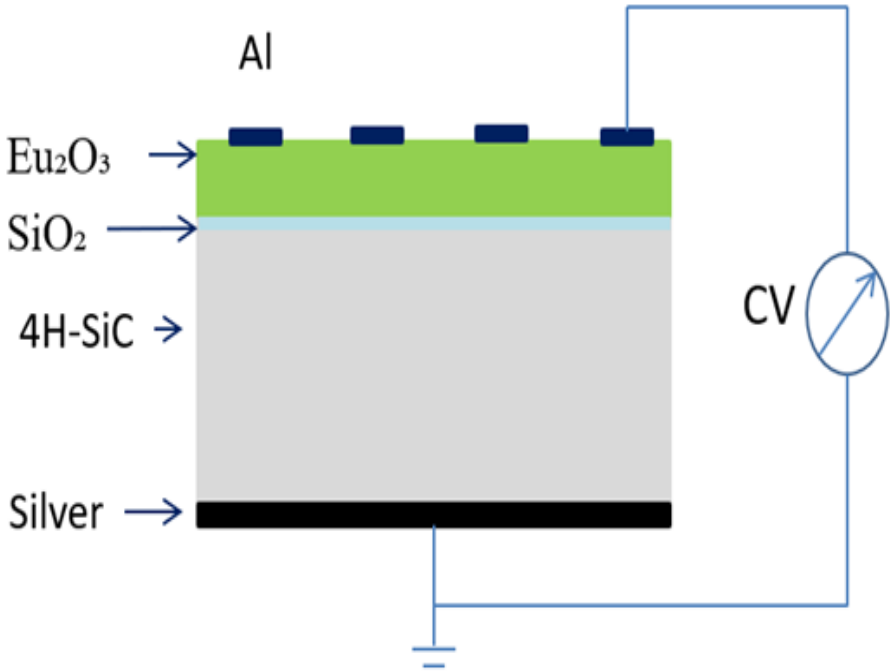

Figure 2.1. Schematic structures of the fabricated MOS capacitors

Electrical measurements, including capacitance-voltage (C–V) and conductance-voltage (G/ω–V) characteristics, were conducted using the Keithley 4200-SCS Parameter Analyzer at a frequency of 100 kHz and at room temperature. The electrical characterizations were thoroughly investigated, taking into account the structural evolution. As shown in Figure 2.1.

2.1.1 2.1.1 Cleaning Process of Wafers

The RCA wafer cleaning process is a standard method used in the semiconductor industry, involving a series of chemical treatments that effectively remove various types of contaminants. Especially in the context of metal oxide semiconductor devices (MOS), it is essential for the quality of the deposited layers that grow on the wafer and to ensure the quality and performance of the final semiconductor products, as the cleanliness of the wafer surface directly affects the performance of the devices manufactured on it. The RCA cleaning process is one of the most widely used methods for cleaning silicon wafers, and it was named after the Radio Corporation of America, which developed the procedure. Each step in the RCA cleaning process is designed to address specific types of contamination. Here is an overview of the RCA cleaning process:

Step 1: Removal of organic residues and some particles.

The chemicals used are Deionized water (DI-H_2O), Hydrogen peroxide (H_2O_2), and Ammonium hydroxide (NH_4OH).

The solution is in the ratio: 5:1:1 (DI-H2O:H_2O_2: NH_4OH).

Step 2: Remove inorganic contaminants, such as metal ions and salts.

The chemicals used are Deionized water (DI-H2O), Hydrogen peroxide (H_2O_2), and Hydrochloric acid (HCl).

The solution is in the ratio: 6:1:1 (DI-H2O:H_2O_2: HCl).

Step 3: Clean the original oxide (SiO2)

The chemicals used are Deionized water (DI-H2O) and hydrofluoric acid (HF).

The solution is in a ratio: 100:1 (DI-H2O: HF).

After the RCA cleaning process, the chips are dried with pure nitrogen. It ensures the removal of contaminants could otherwise degrade the performance of the device. By providing a clean and defect-free surface, which is critical to preparing the wafer surface for subsequent processing steps.

2.2 Measurement Materials and Irradiation of Fabricated Devices

2.2.1 X-Ray diffractometer (XRD)

X-ray diffraction is a powerful analytical technique used to identify and characterize materials at the atomic or molecular level. It provides critical insights that can enhance research and analysis across a variety of fields. One of the most important benefits of X-ray diffraction readings is its ability to identify the crystalline phases present in a sample, by analyzing the diffraction pattern, which is vital to understanding the properties of materials. X-ray diffraction provides detailed information about the crystal structure, researchers can gain fundamental information about a sample without changing its chemical or physical state. In our study, we used the Rigaku X-ray diffraction device, which is based on the constructive interference of X-rays with a wavelength of (1.5418 Å) with Cu Kα radiation, where the angle range 2Θ is between 10-70 degrees and a speed of scanning 3.5 degrees/min. Measurements were taken of the crystal structure of the manufactured films. The XRD spectra obtained from the device

measurements were tabulated through the database of the International Center for Diffraction Data (ICDD). The crystallization stages and phase changes were identified by analyzing the results by studying the indexed diffraction peaks obtained from the XRD spectra. These procedures were done before radiation exposure. After radiation exposure, the effects of radiation on the manufactured films were determined. The results were analyzed through the changes obtained after exposure to radiation, such as peak shifts, their amplitudes, and changes in their intensity.

2.2.2 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a pioneering technique that has changed the field of nanoimaging. It is a type of scanning microscope that provides high-resolution imaging by scanning a sharp tip (a small probe) attached to an arm over the surface. The interaction between the probe and the atom on the surface generates a force (due to the up-and-down movement of the arm, AFM images are generated, and this movement is due to the attractive force between the probe and the surface). This creates detailed 3D topographic maps of semiconductor surfaces, which helps in assessing roughness, defects, and other structural properties that affect electrical and optical properties. The rough surface of thin films is the cause of charge carrier scattering and thus leads to poor electrical conductivity. Thanks to this innovative imaging technique, significant progress has been made in research in various fields. In our study, we used an AFM device and investigated the morphological properties of thin films. The measurements were performed in contact mode under normal indoor conditions. The AFM images were analyzed, and the mean surface roughness (R_q) values were calculated.

2.2.3 C-V and G/ω–V Characteristics

The capacitance-voltage characteristics are fundamental to understanding and developing semiconductor technology. Capacitance-voltage characteristics are graphs that represent the relationship between capacitance and voltage in semiconductor devices. These characteristics are typically measured across a p-n junction or metal-oxide-semiconductor (MOS) and can indicate how capacitance changes with applied voltage. The shape and nature of the capacitance-voltage

curve provides critical information about the properties of the semiconductor, including charge carrier concentration, interface states, flat voltage, threshold voltage, etc., from capacitance and voltage data which are essential for understanding the behavior of materials and improving manufacturing processes. Our study used a Keithley 4200-SCS Parameter Analyzer under normal conditions at room temperature in the dark mode. Measurements were taken from the device, the voltage-capacitance curves and flat band voltage shift were investigated, and the series resistance and the interface charge density (D_{it}) were obtained using the conduction method at a frequency of 100 kHz. This procedure was done before the films were exposed to radiation. After the radiation exposure, the voltage-capacitance curves were also investigated, radiation's effects on the films were studied, and radiation-induced defects were explored.

2.2.4 Irradiation Experiment

Metal-oxide semiconductor (MOS) capacitors are fundamental components in semiconductor electronics. Understanding their behavior under radiation exposure is crucial for designing devices intended for radiation-dominated environments. When MOS capacitors are exposed to radiation, several physical processes can occur. The most important effects arise from high-energy particles, which can cause defects at the interface between the semiconductor and the oxide, and within the oxide layer. The effect of radiation on MOS capacitors can be evaluated by testing in controlled environments where specific radiation doses are applied, followed by electrical characterization to evaluate changes in relevant parameters. All samples were exposed to radiation doses (X) of 50 kV, and the samples were placed vertically and directly, 5 mm away from the radiation source, and the current through the device was 80 μA. Capacitance-voltage measurements were performed immediately after each radiation dose, XRD measurements were performed for the samples and the exposure time for each sample was different. The effect of radiation on the structural, morphological, and chemical properties of thin films was investigated.

3. RESULTS

3.1 Before Irradiation

3.1.1 XRD Results

Figure 3.1 illustrates the X-ray diffraction (XRD) patterns of the deposited and annealed thin films**.**

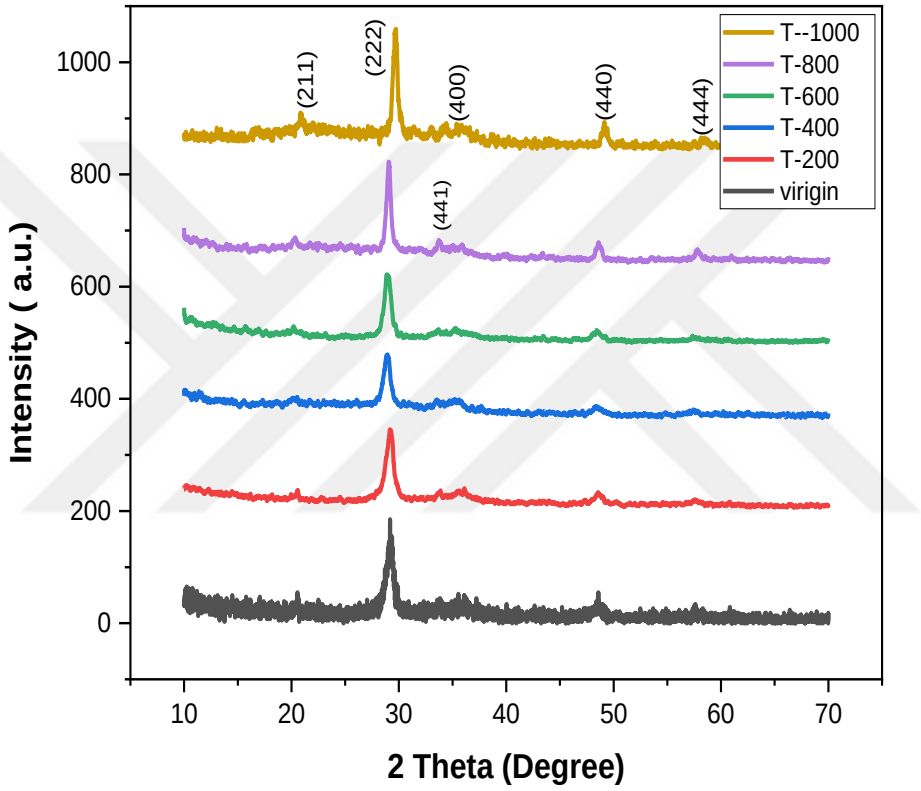

Figure 3.1. XRD patterns of Eu_2O_3/SiO_2 thin films annealed at various temperatures

3.1.2 AFM Results

The surface morphology of the films was analyzed using atomic force microscopy (AFM), and surface roughness values were recorded. Figures 3.2 a-d present 3D-AFM images of representative post-annealed films.

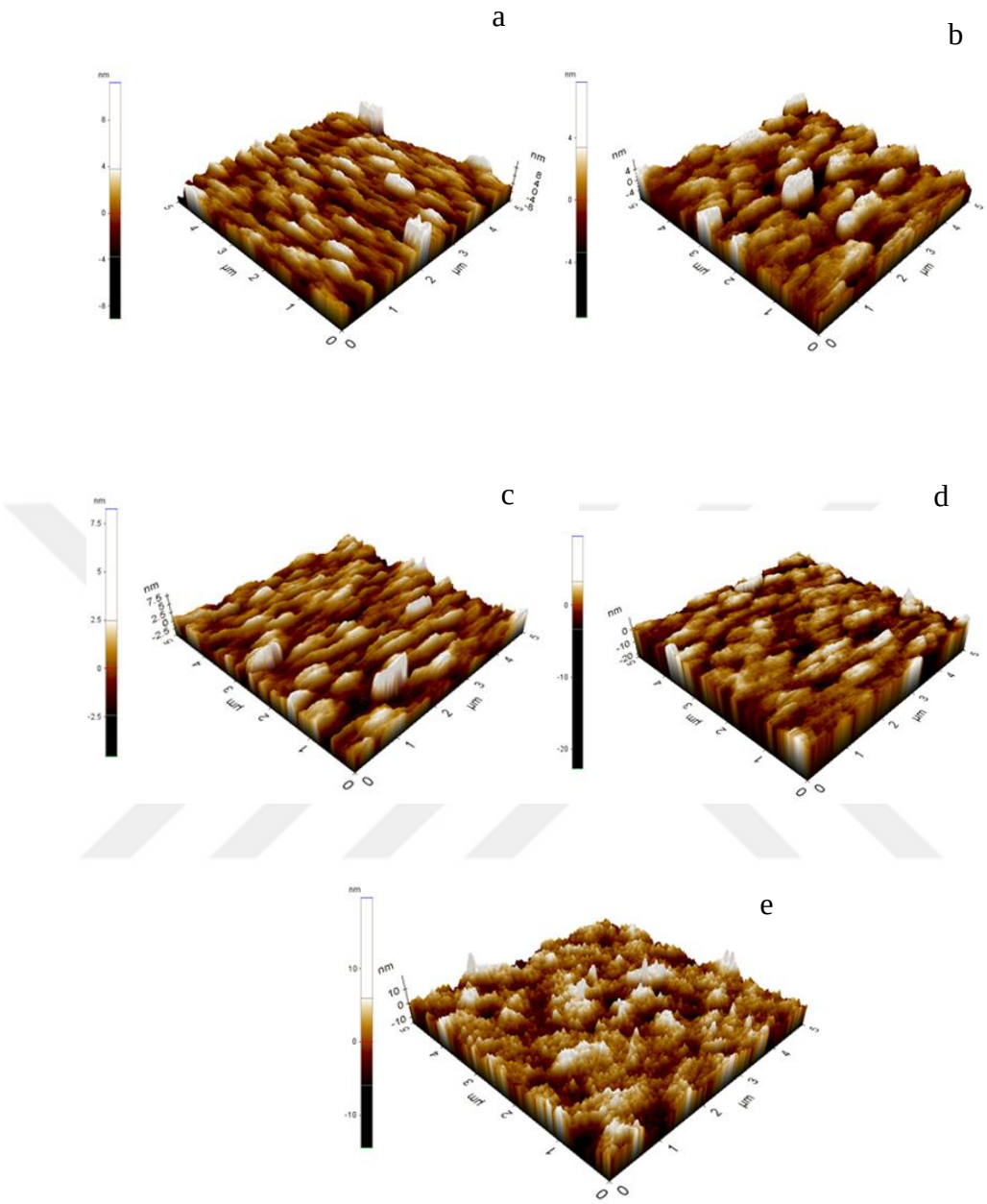

Figure 3.2. The AFM measurements of a-) T-200, b-) T-400, c-) T-600, d-) T-800, e-) T-1000 samples.

3.1.3 ATR-FTIR Results

ATR-FTIR analysis was performed to investigate how annealing temperature influences the lattice vibration modes in $Eu_2O_3/SiO_2/SiC$ thin film samples. All spectra were recorded using SiC as the background, and the resulting ATR-FTIR spectra are presented in the range of 400 to 2000 cm-1 in Figure 3.3.

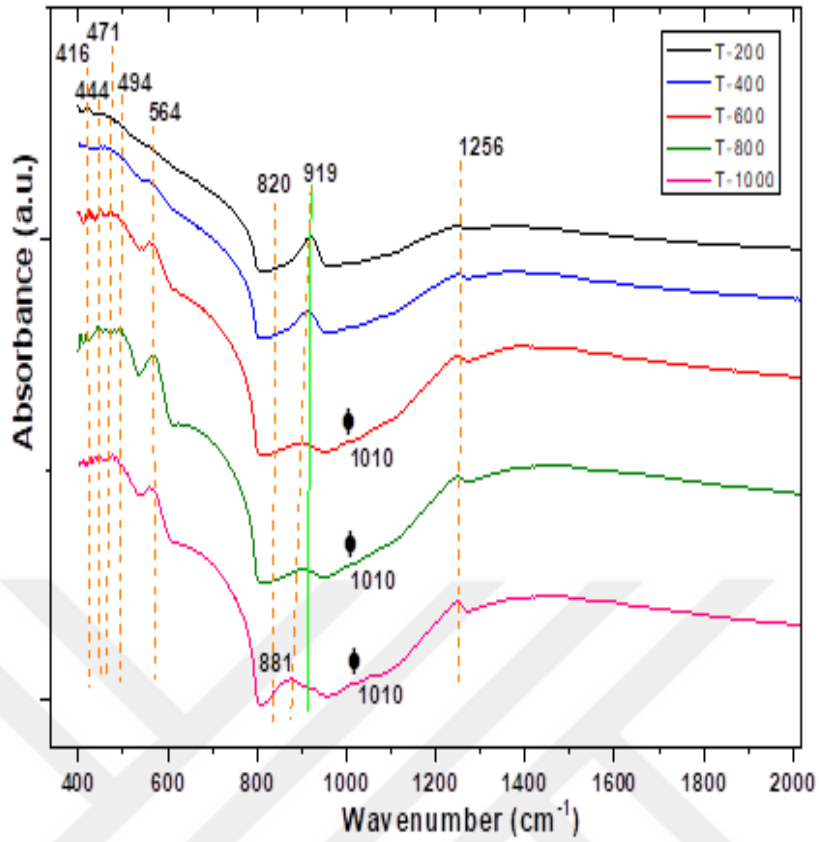

Figure 3.3. ATR-FTIR spectra of $Eu_2O_3/SiO_2/SiC$ thin films annealed at various temperatures.

3.1.4 Electrical measurements Results

The impact of heat treatment on the electrical properties of the samples was analyzed through the Capacitance-Voltage (C-V) and Conductance-Voltage (G-V) characteristics, as shown in Figure 3.4 (a) and (b).

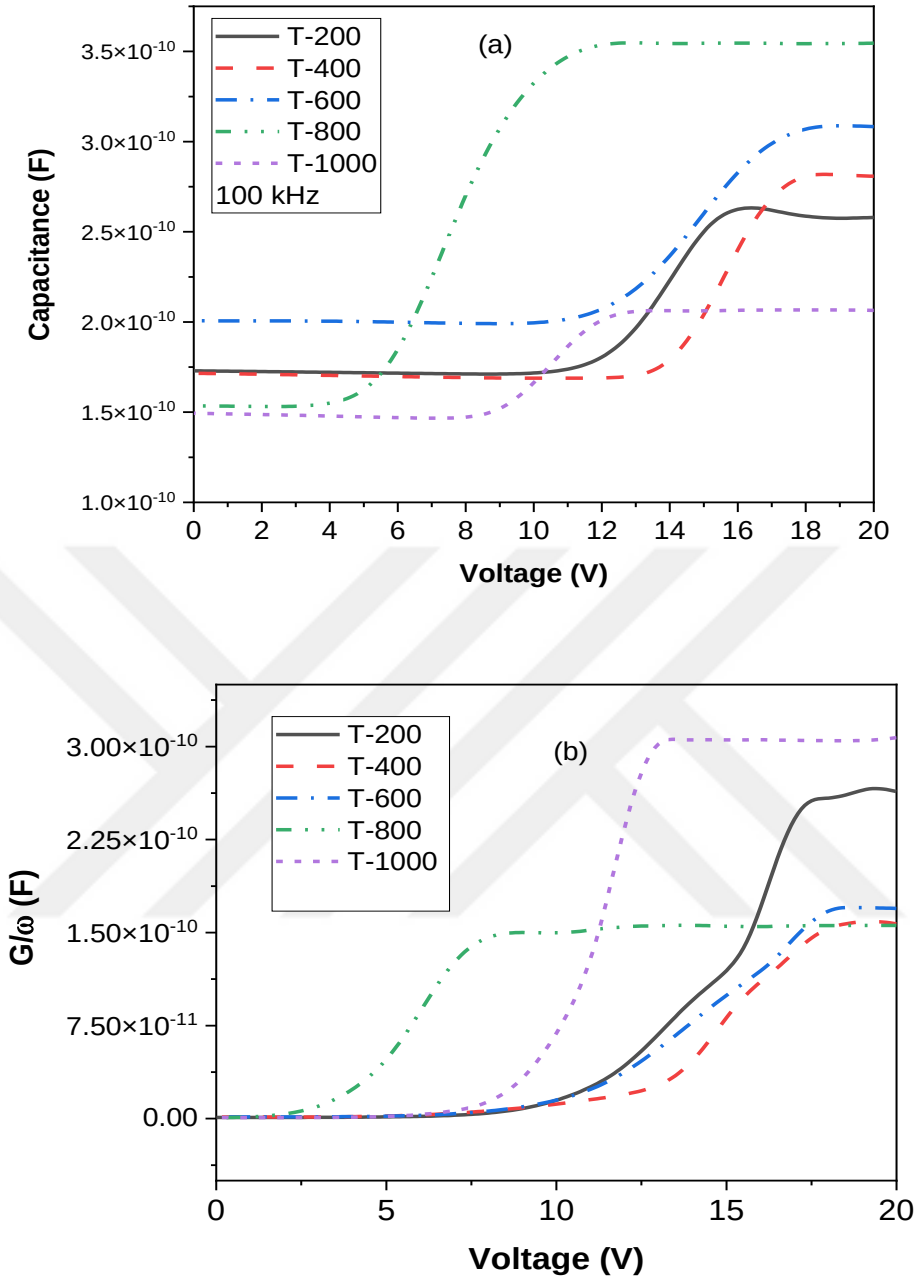

Figure 3.4. Measurement of a- Capacitance-Voltage and b- Conductance-Voltage characteristics of MOS capacitors

3.2 After Irradiation

3.2.1 XRD Results

Figure 3.5 illustrates the XRD patterns of Eu_2O_3 thin films both prior to and following exposure to X-rays. The impact of X-ray irradiation on the crystalline structure of the Eu_2O_3 films was examined through the analysis of

these XRD patterns. The peaks were indexed using the International Centre for Diffraction Data (ICDD) database, revealing a strong alignment with ICDD card number 65-3182, which corresponds to the cubic phase of Eu_2O_3 exhibiting a (222) preferred orientation.

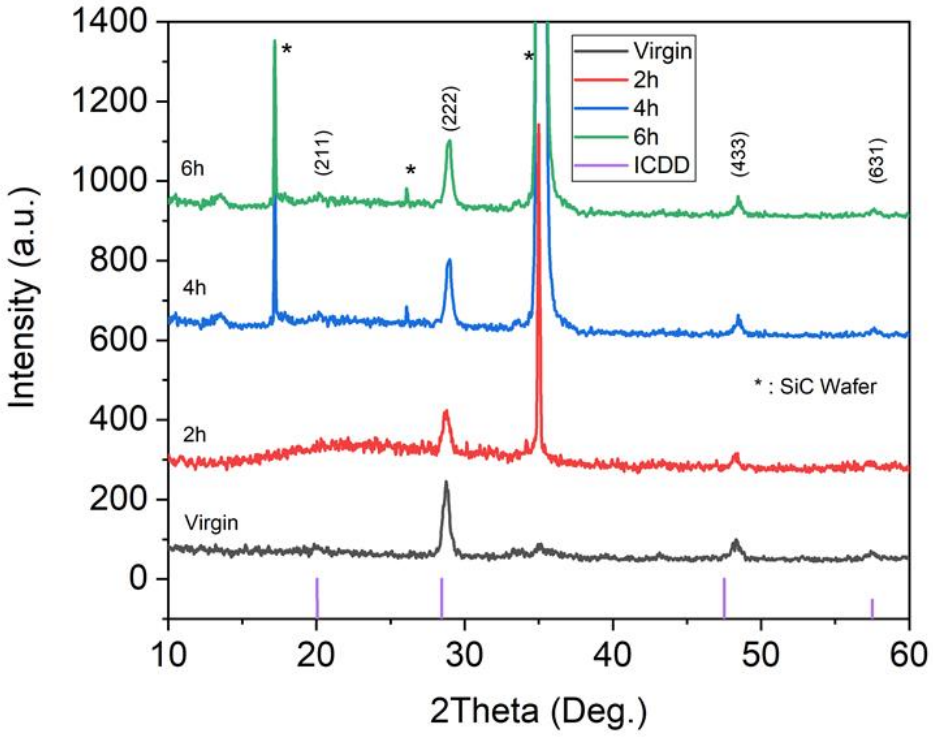

Figure 3.5. X-ray diffraction patterns of irradiated and unirradiated Eu_2O_3 dielectric thin film annealed at 800°C

3.2.2 Electrical Measurement Results

To investigate the impact of radiation on the electrical properties of Eu_2O_3 films, capacitance-voltage (C-V) and conductance-voltage (G/ω–V) measurements were performed on both unirradiated and irradiated samples. An x-ray radiation source with an energy of 50 kV was used for various exposure durations: 300 s, 600 s, 900 s, 2100 s, 2700 s, and 3100 s. The C-V characteristics obtained are illustrated in Figure 3.6.

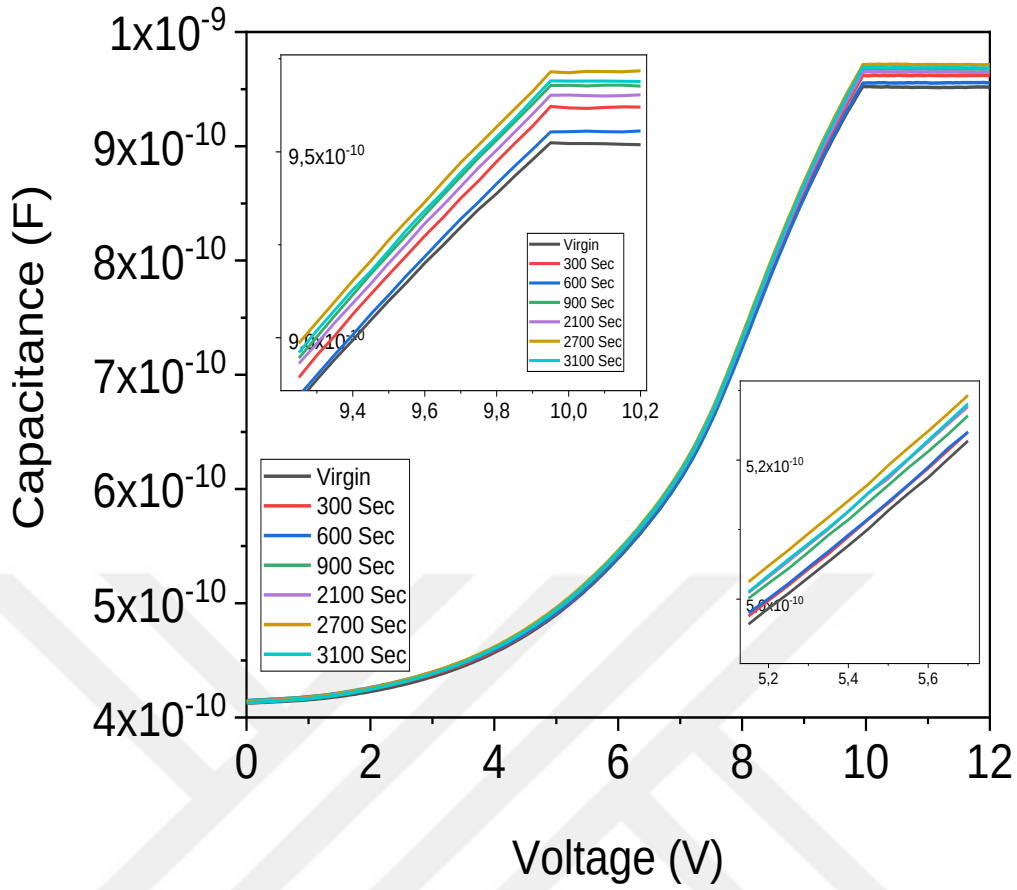

Figure 3. 6. C-V curves showing the radiation response of a Eu_2O_3 dielectric thin film at 100 kHz

In order to determine the behavior of the interface states in response to radiation, conductivity measurements were performed. After correcting for series resistance, the results are presented in Figure 3.7.

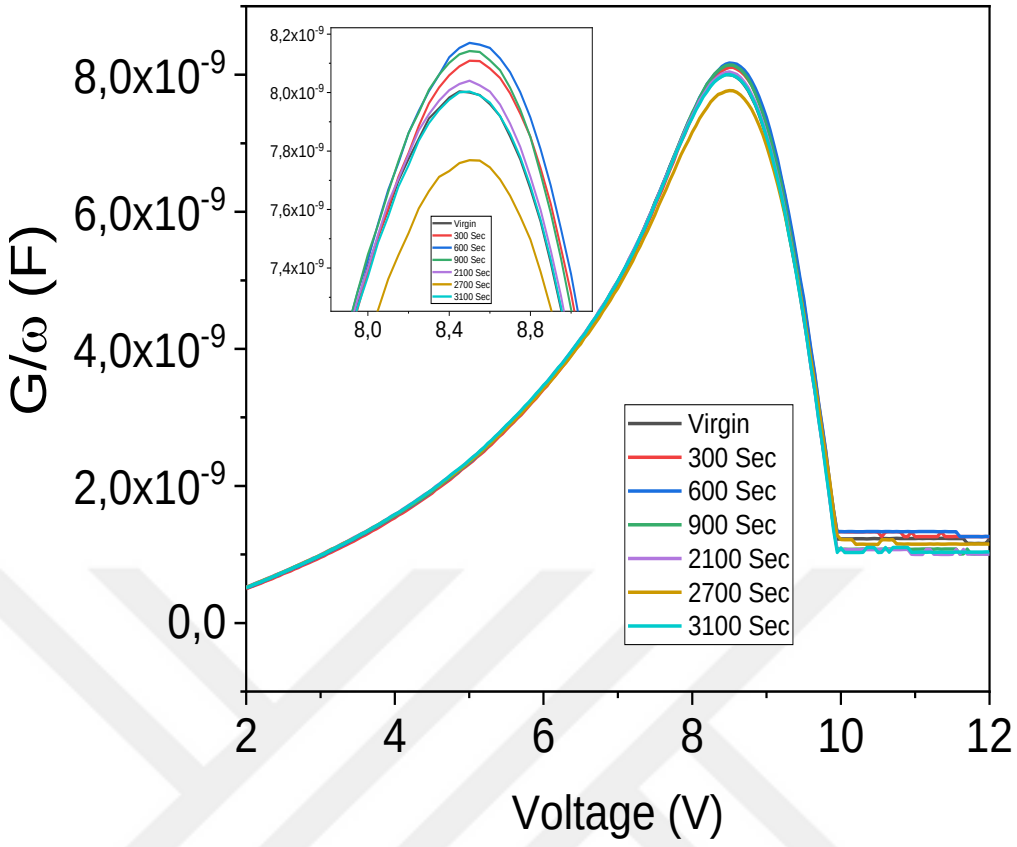

Figure 3.7. G/ω -V curves showing the radiation response of a Eu_2O_3 dielectric thin film

4. DISCUSSION

4.1 Before Irradiation

4.1.1 XRD Analyses

The intensity of the peaks, as well as the presence of minor peaks, varied with different annealing temperatures as can be seen in Figure 3.1. Notably, the films annealed at 800 °C exhibited peaks that were indexed using the International Centre for Diffraction Data (ICDD) database, showing a strong alignment with ICDD card number 65-3182, which corresponds to the cubic phase of Eu_2O_3 with a preferred orientation of (222). The indexed peaks were also in agreement with findings in the literature (Dakhel, 2003; Mo et al., 2012). Depending on the base layer, multiple phases of Eu_2O_3 can be observed (Mariscal, 2016) however; a pure cubic phase was achieved specifically for the T-800 films deposited on Silicon Carbide. The distribution of the (222) peaks, influenced by annealing, allowed for the calculation of the crystalline size and tangent stress of the films, as detailed in Table 4.1. For films annealed at lower temperatures, the lack of certain minor peaks can be linked to insufficient crystallization of Eu_2O_3, as demonstrated by the T-200 sample. As the annealing temperature rises, these minor peaks become more distinct. Their appearance is associated with an increase in stress within the film, which leads to a decrease in crystalline size in the T-400 sample, likely due to heightened compressive stress. At 800 °C, there is a significant increase in the visibility of minor peaks, along with improvements in both crystalline size and stress values. Higher temperatures provide enough energy for micro grains to merge into larger clusters, resulting in reduced stress. However, at an annealing temperature of 1000 °C, there is a rise in peak intensity and a shift to higher angles, accompanied by a decrease in crystalline size and the formation of a parasitic phase. This change may be attributed to chemical variations and/or the diffusion of Eu ions in the film composition at temperatures exceeding 950 °C (Ferrier et al., 2020). Additionally, the formation of the monoclinic phase is observed when the annealing temperature surpasses 900 °C (Dakhel, 2003). The crystalline size for the T-800 samples was calculated to be 178.41 Å, accompanied by a low-stress value. This measurement aligns with the properties of Eu_2O_3 dielectrics deposited

on silicon substrates that were annealed at similar temperatures (Dakhel, 2003; Castro et al., 2007), and it is superior to those of other gate dielectrics grown on the same 4H-SiC substrate (Odesanya et al.,2023; Tanner et al.,2007).

Table 4.1. Some structural and morphological parameters

ID	2Theta (degree)	Crystalline Size(Å)	Lattice Strain $x10^{-3}$	R_q (nm)
T-200	29.18	106.61	5.7	2.07
T-400	29.02	107.97	5.6	3.13
T-600	29.05	115.58	5. 3	1.90
T-800	29.09	178.41	3.4	2.23
T-1000	29.66	161.13	3.7	4.25

Yilmaz et al. (Yilmaz et al., 2020) studied the X-ray diffraction patterns of Eu_2O_3 films deposited on silicon at different annealing temperatures, where at 500 °C they obtained a grain size of 24.28 nm and at 700 °C the grain size was 26.45 nm. Wang et al. (Wang et al., 2000) studied the crystal structure of Eu_2O_3 films deposited on silicon using XRD at an annealing temperature of 800 °C and obtained a grain size of 12 nm. Dakhel (Dakhel, 2003) studied the XRD patterns of Eu_2O_3 films deposited on silicon and treated at 800 °C and obtained a grain size of 35 nm. Kumar et al. (Kumar et al., 2016) also studied the XRD patterns of Eu_2O_3 films deposited on silicon and obtained a grain size of 37 nm at an annealing temperature of 750 °C. When comparing our results with previous studies, we find similar or close results and better results. We can say that our results are of average quality, but there is a difference in terms of the materials used, as we used SiC as a substrate (semiconductor) instead of silicon used by researchers, because SiC contains carbon, and when it spreads at high temperatures, it causes defects within the crystal structure, which may be the reason behind this result.

4.1.2 AFM Analyses

The surface roughness (R_q) values, which provide a description of the surfaces, are detailed in Table 4.1. The T-200 samples exhibit a homogeneous surface at the nanoscale, with a roughness of 2.07 nm, and no significant defects such as pinholes or cracks were observed. The surface topology remains consistent for films annealed at temperatures up to 1000 °C, with the primary

change being the variation in surface height distribution. The increase in R_q values for the T-400 sample may be attributed to the heightened film stress discussed in the XRD analysis. Reducing stress and strain on the film helps to minimize swelling effects caused by the microscopic migration of surface atoms to the substrate (Kaya, 2019). Following heat treatment, the film surface becomes denser and smoother. As the annealing temperature rises to 1000°C, the distribution of individual columnar grains becomes wider, leading to an increased R_q distribution. The roughness values of the films are similar to those of previously published Eu_2O_3 films (Castro et al., 2007; Kumar et al., 2018), suggesting that high-quality films have been deposited on the new SiC substrate.

4.1.3 ATR-FTIR Analyses

Upon initial observation, faint IR bands were identified at approximately 471, 820, and 1010 cm^{-1}, particularly at temperatures above 400 °C. These bands correspond to Si-O rocking, Si-O bending, and Si-O-Si asymmetric stretching vibrations associated with the silicates formed during the annealing process (Loganathan et al.,2013; Li et al.,2014; Herth et al.,2016). Additionally, specific absorption bands observed at around 413, 444, 494, 564, and 919 (881) cm^{-1} were attributed to the characteristic bending or stretching vibration modes of the Eu-O and Eu-O-Eu bonds in Eu_2O_3 (Mo et al., 2012; Ahlawat et al.,2018; Ahmed et al., 2022). At temperatures exceeding 400 °C, the bands, particularly the peak at 564 cm^{-1}, became more pronounced and sharper, as illustrated in the figure. Upon reaching an annealing temperature of 800 °C, the peak exhibited maximum intensity and sharpness, indicating an improved lattice structure of Eu_2O_3 due to enhanced phase formation. However, beyond 800 °C, the ATR-FTIR results showed a decrease in both the sharpness and intensity of this peak, accompanied by broadening. This observation serves as experimental evidence that the lattice structures of Eu_2O_3 deteriorate at elevated temperatures, leading to the formation of crystal defects. Additionally, the ATR-FTIR spectra revealed that a small absorption band at 919 cm^{-1} became broader and shifted while decreasing in intensity as the temperature increased. This infrared (IR) mode was likely associated with the bending vibration of O-H bonds resulting from moisture absorption on the surface of the metal oxide (Sheikh et al., 2023). As the temperature increased, the surface activity of Eu_2O_3 decreased, leading to a

reduction in the amount of moisture absorbed on the metal oxide surface, which in turn caused a decrease in the intensity of this peak (Azad and Maqsood, 2014). Consequently, the specific IR band corresponding to Eu_2O_3 became more pronounced in the spectra. Additionally, a small absorption band around 1256 cm^{-1} was attributed to the Si-O-Eu bonds formed between the layers. As anticipated, this peak became more prominent with higher annealing temperatures due to improved chemical interactions (Gao et al., 2022).

4.1.4 Electrical Measuremenets Analyses

It was noted that the C-V curves varied significantly based on the annealing process. Each C-V curve, however, displayed three distinct regimes: accumulation, depletion, and inversion. Additionally, the C-V curves exhibited a shift along the positive voltage axis, which can be attributed to the presence of surface states. Similar trends were observed in the G-V curves of the samples. Conductance reflects the losses due to the exchange of majority carriers between the interface states and the majority carrier band of the semiconductor (Kaya et al.,2015; Nicollian and Brews,2003), typically showing a peak at the depletion edge. The non-ideal behavior observed may be attributed to factors such as oxide defects, interface states, and series resistance (Kaya et al.,2014). To investigate the impact of series resistance (Rs) and eliminate parasitic effects from the measurements, a correction was applied. The Rs values were calculated using the Nicollian and Goetzberger method, as outlined in Eq. 4.1(Kaya and Yilmaz,2015).

$$R_s = \frac{G_{ma}}{(G_{ma})^2 + (\omega C_{ma})^2} \tag{4.1}$$

where $\omega = 2\pi f$ represents the angular frequency, and C_{ma} and G_{ma} denote the measured capacitance and conductance in the strong accumulation region, respectively. The calculated Rs values for the Eu_2O_3 MOS capacitors are presented in Table 4.2. This table indicates that the series resistance values range from 2105 Ω to 3572 Ω. The variations in Rs values may be due to reordering and restructuring effects induced by the applied voltages at different frequencies (Reddy et al.,2013). The capacitance and conductance characteristics can be corrected by (Nicollian and Brews,1982):

$$C_C = \frac{\left[(G_m)^2 + (\omega C_m)^2\right] C_m}{a^2 + (\omega C_m)^2} \tag{4.2}$$

$$G_C = \frac{\left[(G_m)^2 + (\omega C_m)^2\right] a}{a^2 + (\omega C_m)^2} \tag{4.3}$$

where $a = (G_m) - \left[(G_m)^2 + (\omega C_m)^2\right] R_s$, ω represents the angular frequency, C_m denotes the measured capacitance, and G_m indicates the measured conductance. The corrected capacitance-voltage (C-V) and conductance-to-angular frequency (G/ω) versus voltage curves are illustrated in Figures 4.1 (a) and (b), respectively. When comparing C_c with C_m, no significant differences were noted, except in the T-1000 samples. Notably, the capacitance characteristics of the T-1000 samples exhibited a substantial increase following series resistance correction. This unusual behavior has been corroborated by capacitance measurements taken from various locations (not shown here) on the T-1000 samples. The unexpected rise in the C_c curve for the T-1000 sample may be linked to the formation of Eu-Si-O bonds, which arise carbon-related defects during high-temperature annealing. Furthermore, the conductance displays a peak at the depletion edge, a behavior typically observed in MOS devices after applying series resistance corrections. The impact of Rs on the capacitance and conductance curves has been thoroughly examined for silicon-based MOS devices, but there is limited understanding regarding silicon carbide-based MOS devices. In this context, it is observed that Rs also significantly affects the capacitance and conductance characteristics of silicon carbide-based MOS devices. This influence should be especially considered following high-temperature annealing when analyzing the capacitance curves.

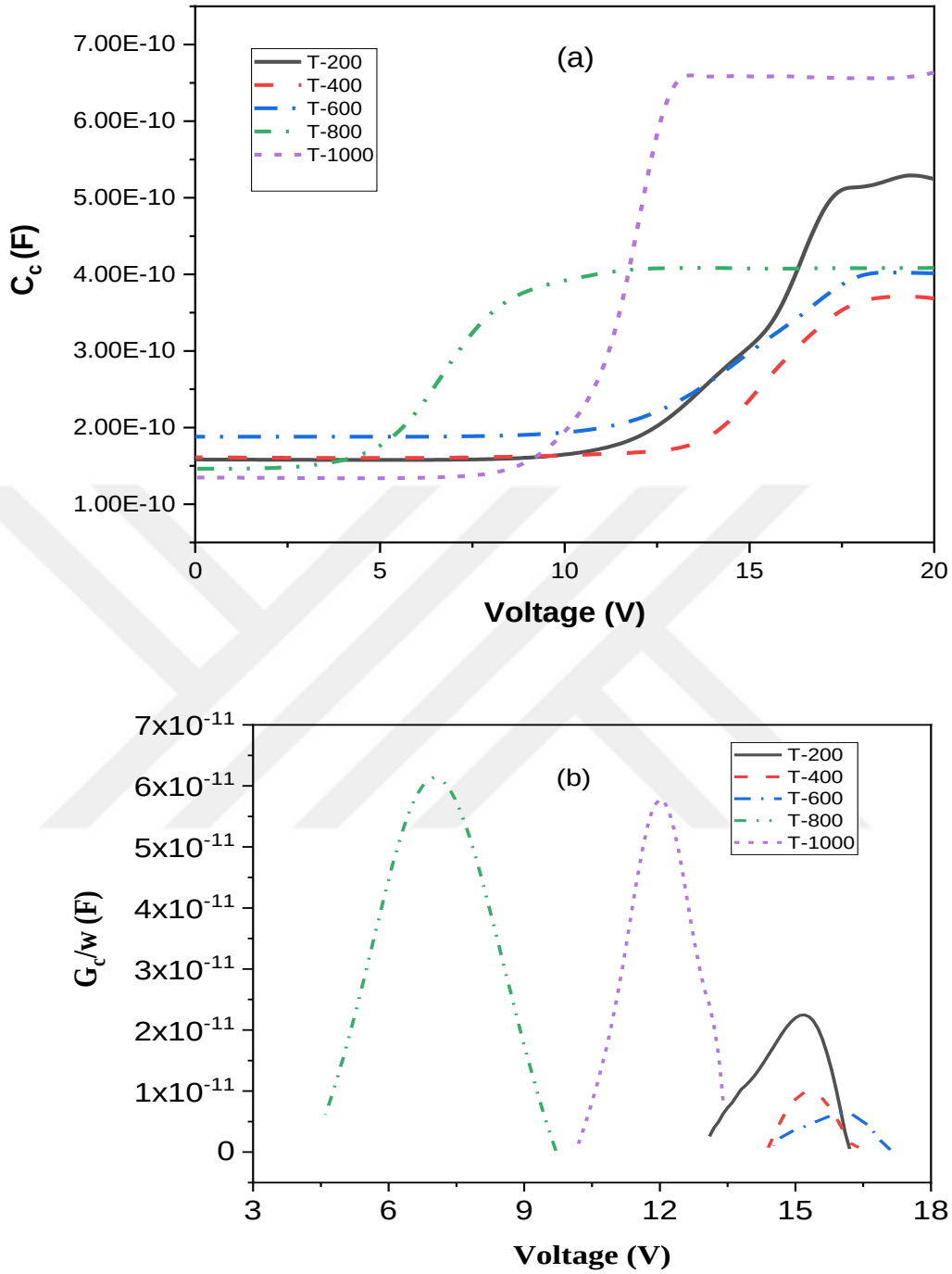

Figure 4.1. Characteristics of a- Corrected Capacitance-Voltage and b- Corrected Conductance-Voltage of MOS capacitors

The flat band voltage (V_{fb}) values can be derived from the curves presented in Figure 4.1 (a). A variation in V_{fb} was noted for the annealed samples, attributed to the oxide state density (N_{eff}) present in the thin films (Quah

and Cheong,2012). By applying Eq. 4.4 (Kaya et al.,2015), we can determine the effective oxide state densities (N_{eff}) using the Cc curves.

$$V_{fb} = \Phi_{ms} - \frac{Q_{eff}}{C_{ox}} \quad (4.4)$$

In this context, Φ_{ms} represents the work function difference between SiC and Al, C_{ox} denotes the oxide capacitance, and Q_{eff} is the effective charge, defined as $Q_{eff} = qAN_{eff}$, where q is the electrical charge and A is the contact area of the capacitor. Up to 800°C, the annealing process improved the oxide defects in the thin film, likely due to the healing of oxygen vacancies and a reorganization of the film's structure. However, at an annealing temperature of 1000°C, an increase in oxide traps was noted. This increase may be linked to the beginning of thermal degradation of the oxide material, which can lead to heightened stress and defects at the oxide-substrate interface. Furthermore, elevated temperatures may trigger undesirable reactions or the diffusion of carbon or silicon impurities from the SiC wafer, potentially creating additional trap sites and compromising the film's electrical properties.

Table 4.2. Some electric characteristics of Al/Eu_2O_3/SiO_2/SiC MOS capacitor

ID	R_s (ohm)	N_{eff}x10^{12} (cm^{-2})	D_{it}x10^{11} ($eV^{-1}cm^{-2}$)	V_d (eV)	N_dx10^{16} (cm^{-3})	E_F (eV)	$\Delta\Phi_B$ (meV)	Φ_B (eV)
T-200	2849	9.09	0.969	12.80	3.34	0.175	77.02	1.473
T-400	2434	10.05	0.348	14.70	2.35	0.184	73.01	1.221
T-600	2105	9.73	0.307	13.30	5.78	0.161	89.23	2.540
T-800	2365	5.27	2.411	5.85	2.24	0.186	57.36	0.548
T-1000	3572	6.55	5.487	10.30	1.40	0.198	58.62	0.599

Interface states in a MOS capacitor refer to energy levels at the semiconductor-oxide boundary that arise from defects, which can capture charge carriers and affect the device's electrical performance. Consequently, the density of interface states (D_{it}) was determined using Eq. 4.5, applying the Hill-Coleman method (Hill and Coleman,1980).

$$D_{it} = \frac{2}{Aq} \frac{G_{c,\max} / \omega}{\left(G_{c,\max} / \omega C_{ox}\right)^2 + \left(1 - C_c / C_{ox}\right)^2} \quad (4.5)$$

In this context, $G_{c,max}/\omega$ represents the peak values of the corrected G_c/ω–V curve, while Cc denotes the corrected capacitance of the MOS capacitor associated with $G_{c,max}/\omega$. The calculated D_{it} values are presented in Table 4.2. Initially, as the annealing temperature rises, the density of interface states decreases, indicating that the heat treatment effectively repairs crystal defects, reduces surface traps, and enhances the oxide-semiconductor interface by facilitating bond rearrangement or the elimination of contaminants. This is supported by ATR-FTIR analysis of the $Eu_2O_3/SiO_2/SiC$ layers, which shows that at moderate temperatures (~400 °C), there is a presence of Si-O rocking, bending, and Si-O-Si stretching modes that may help passivate the interface traps. However, when the temperature reaches 800 °C, the density of interface states begins to increase due to thermal degradation, which introduces new defects at the oxide-semiconductor interface, such as dislocations and vacancies. At temperatures exceeding 800 °C, the FTIR spectra indicate a broadening and reduced intensity of the silicon-containing bonds, which suggests crystal degradation and defect formation resulting from the diffusion of elements such as europium (Eu), carbon (C), or silicon (Si). This diffusion likely leads to the introduction of dislocations and oxygen vacancies, thereby increasing the density of interface states. Furthermore, the Si-O-Eu bond band at 1256 cm^{-1} becomes more pronounced at higher temperatures, indicating enhanced interlayer interactions that facilitate the development of a parasitic interfacial silicate layer. It has also been observed that at elevated temperatures—typically between 1000 and 1200 °C— a significant number of carbon bonds break, releasing carbon monoxide from the surface and generating new crystal defects. Meanwhile, the remaining carbon on the surface becomes increasingly unstable due to this dissociation. Consequently (Ventra and Pantelides,1999), the rise in both N_{eff} and D_{it} values may also be linked to carbon-related defect sites within the film structure, especially at annealing temperatures around 1000 °C.

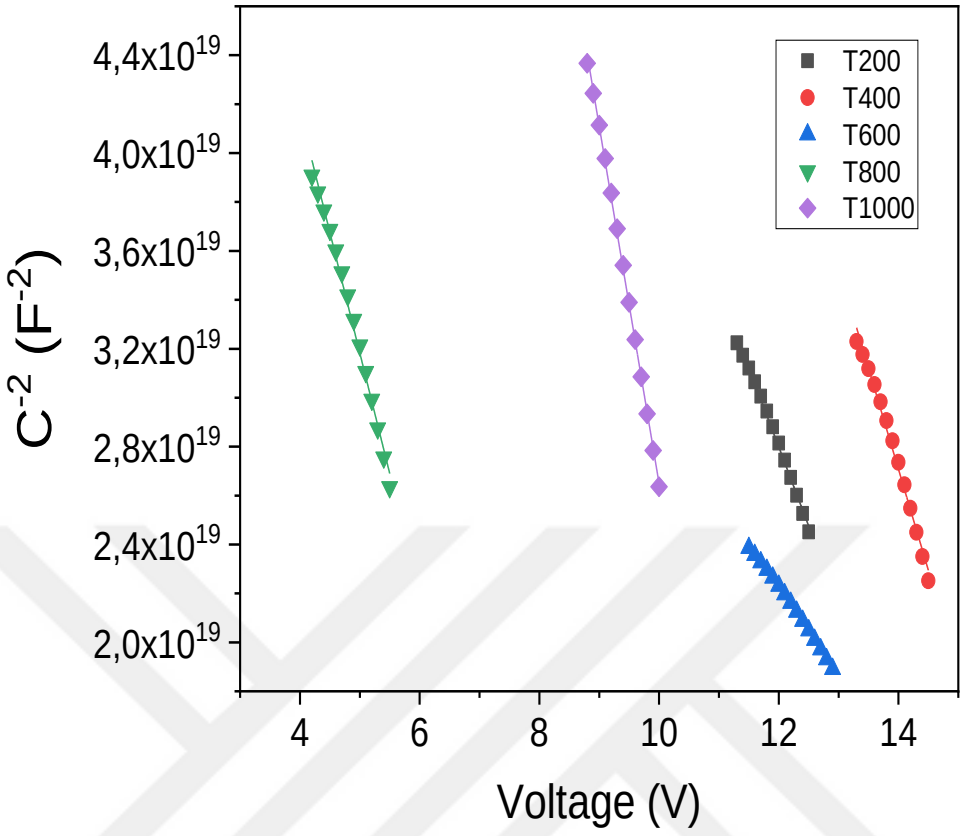

Figure 4.2. The Cc^{-2} –V characteristics of MOS capacitors

The doping concentration (N_d), Fermi energy level (E_F), diffusion potential (V_d), and barrier height (Φ_B) are obtained from the inverse of the squared corrected capacitance-voltage (Cc^{-2}-V) characteristics. The relationship between capacitance (C) and voltage (V) can be expressed as follows (Kaya and Yilmaz,2020):

$$C_c{}^{-2} = \frac{2(V_0+V)}{\varepsilon_s \varepsilon_0 q A^2 N_d} \tag{4.6}$$

Here, V represents the applied bias, and V_0 (= V_d-kT/q) is the point where the Cc^{-2} versus V plot intersects the voltage axis. In this context, ε_s denotes the relative permittivity of SiC, while ε_o refers to the permittivity of free space. The doping concentration N_d is determined from the slope of the Cc^{-2} versus V graph. The barrier height Φ_B can be calculated from the Cc^{-2}-V curve using the following equation (Kaya and Yilmaz,2015; Kaya and Yilmaz,2020):

$$\Phi_B = V_0 + \frac{kT}{q} + E_F - \Delta\Phi_B = V_d + \frac{kT}{q} ln\left(\frac{N_c}{N_d}\right) - \Delta\Phi_B \quad (4.7)$$

In this equation, E_F signifies the energy difference between the bulk Fermi level and the valence band edge, Nc represents the effective density of states in the conduction band, and $\Delta_{\Phi B}$ accounts for the image force barrier lowering, which can be determined from (Kaya and Yilmaz,2015; Kaya and Yilmaz,2020)

$$\Delta\Phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}} \quad (4.8)$$

The maximum electric field is given by $E_m = \sqrt{}$ ($2qV_D$ Na/ ε_0 ε_s). These electrical properties are detailed in Table 4.2. As shown in Table 4.2, the V_d values are positive, indicating that negative charges are trapped within the MOS structure. Additionally, the concentration of N_d changes with annealing temperatures, which corresponds to the variations in slope observed in the Cc^{-2} versus V plot. The reported barrier height ranges from 2.30 eV to 2.65 eV for between 4H-SiC and SiO_2 (Wang et al.,2024; Fiorenza et al.,2018; Wan et al.,2022), with lower values noted for different material/4H-SiC interfaces (Jia et al.,2015; Karadavut et al.,2023). The structure under investigation consists of a thermally grown SiO_2 layer, approximately 5 nm thick, situated between Eu_2O_3 and SiC, forming the Eu_2O_3/SiO_2/4H-SiC configuration. Consequently, the barrier potential of the T-600 sample aligns well with the SiO_2/4H-SiC stack. The schematic representation of the band model, which illustrates the changes in barrier height resulting from various annealing treatments for the T-600 sample, is presented in Figure. 4.3 (a)a. Additionally, the distribution of barrier height is affected by traps at the metal-semiconductor interface, leading to inhomogeneities. Wang et al. have noted that traps in SiC-based devices alter the barrier height by capturing and releasing carriers, resulting in both permanent and transient shifts in barrier height under bias conditions (Nicholls, 2021). As the temperature approaches 1000 °C, the barrier properties of SiO_2 begin to degrade. At this high temperature, carbon migration from the SiC wafer, along with the diffusion of silicon into SiO_2 and the movement of Eu, likely contributes to the development of a defect-rich silicate layer within the device structure. This layer,

which is abundant in defects, promotes the capture and emission of carriers, resulting in a decrease in barrier height, as illustrated in Figure 4.3b.

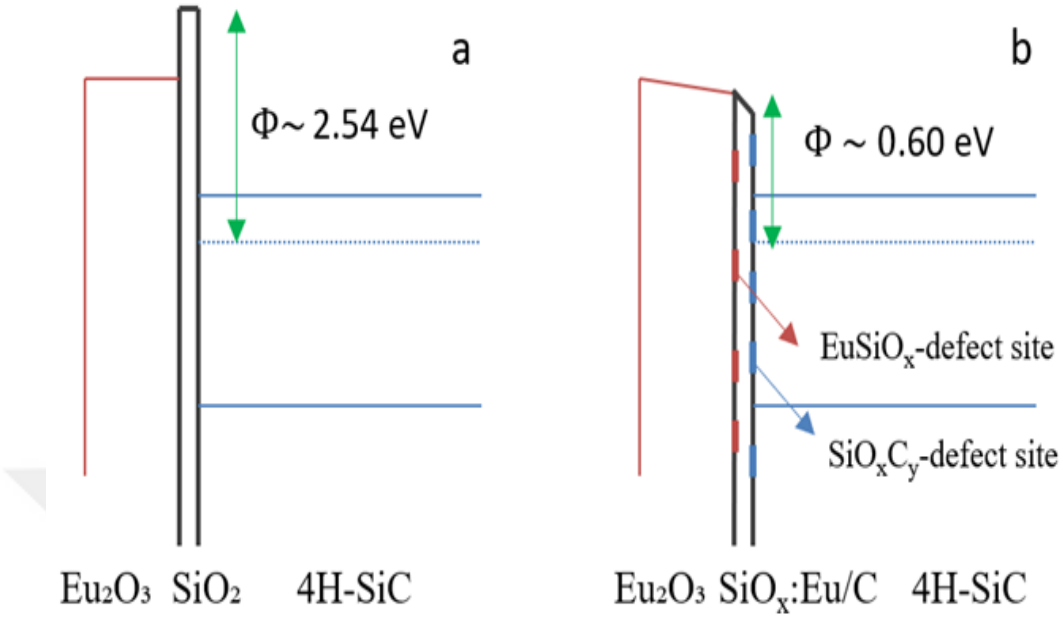

Figure 4.3. Schematic band structure for a-) T-600 sample and b-) T-1000 sample

4.2 After Irradiation

4.2.1 XRD Analyses

It was noted that the intensity of the (222) peak increased with longer exposure times, while the peak shifted towards higher angles. In an ideal crystal, where no internal strain affects the d-spacing, the atomic arrangement is regular and aligns with the theoretically predicted d_0 plane spacing. However, when homogeneous strain is present in the crystal structure, the distances between atoms increase, resulting in a greater separation between the reflecting planes than d0.In this scenario, the diffraction lines in the XRD pattern shift to lower angles due to the larger d-spacing being linked to a reduced diffraction angle. When non-uniform strain is present, the atoms within the crystal may compress at different rates, resulting in a broadening of the XRD peaks, as various regions of the crystal display differing levels of strain. Conversely, an increase in peak intensity was noted alongside a shift to higher angles, indicating an increase in crystalline size. The calculated lattice strain values were 3.44, 3.25, 3.53, and 3.52 x 10^{-3} for the unirradiated sample and those irradiated for 2, 4, and 6 hours, respectively. These lattice strain values decreased with longer exposure times, as

illustrated in Table 4.3. The radiation energy can shift the individual atoms of the material from their positions by imparting kinetic energy to them. This process leads to Compton scattering, the creation of oxygen vacancies (resulting from bond breakage), the formation of interstitial defects, and the development of a granular structure. These changes significantly impact the structural alterations in the device, and the shifts in the XRD peaks are associated with variations in crystalline size (Subramanian and Wang,2012; Kaleji et al.,2012; Mazzolini et al.,2016; Zhanga et al.,2021; Liu et al.,2021; Kozlovskiy al.,2022; Baydogan et al.,2013; Doyle,2014; Tracy et al.,2014).

Table 4.3. Some structure parameters of Eu_2O_3 MOS at different times of dose radiation

Exposure Time	**2θ (degrees)**	**Crystalline Size (Å)**	**Lattice Strain x10^{-3}**
Virgin	29.09	178.41	3.44
2 hours	29.40	186.66	3. 25
4 hours	29.55	171.16	3.53
6 hours	29.59	171.18	3.52

Furthermore, the crystalline sizes were determined using the Scherer equation based on the (222) peak, as shown in Table 4.3. The calculated crystalline sizes were 178.41 Å, 186.66 Å, 171.16 Å, and 171.18 Å for the unirradiated sample and those irradiated for 2, 4, and 6 hours, respectively (Moziaa et al.,2009; Mozia, 2008). In addition to ionization and atomic displacement caused by radiation, the process also induces lattice vibrations as kinetic energy is transferred to the lattice points, resulting in localized heating. This heating effect causes atoms to displace and aggregate into larger masses. The observed increase in crystalline size can be attributed to this localized heating of the atoms (Laha et al.,2012; Kaya et al.,2019). As the exposure time increased, the crystalline size grew while the lattice strain decreased, which is an expected outcome.

4.2.2 Electrical Measuremets Analyses

A review of the overall C-V curve revealed that there was no significant degradation in the structure. Ionizing radiation, such as gamma rays and X-ray, can induce defects, as well as interface and oxide trap charges in MOS capacitors (Ma and Dressendorfer, 1989). The interface states may behave like additional capacitance, depending on their ability to respond to the applied voltages (Kaya and Yilmaz, 2015). The interface states created by irradiation could contribute to the observed capacitance, leading to an increase in the total capacitance values. Changes in capacitance may result from the voltage signal tracking these trap sites. Additionally, upon magnifying the curves, it was noted that the flat band voltage (V_{fb}) and midgap voltage (V_{mg}) values shifted in both directions as a result of radiation exposure. Prolonged exposure times contributed to the breaking of bonds within the structure, leading to the emergence of new defects or trap centers. This, in turn, resulted in a greater number of charges being confined to these centers, causing an increase in the shift of flat band voltage (Kaya and Yilmaz, 2018). However, in certain instances, the broken or non-stoichiometric bonds may be neutralized by radiation exposure (Kaya et al., 2018). Shifts towards zero volts in V_{fb} and V_{mg} suggest that positive charges are primarily being trapped within the structure. Conversely, shifts towards higher voltage values at specific dose levels may indicate that the trapped positive charges have been neutralized or that some radiation-induced trap regions are now capturing negative charges. The data indicates that the peak conductivity value fluctuated in response to the radiation dose. Given that conductivity measurements are affected by the interaction of interface traps, it can be inferred that trap densities vary with radiation exposure. The density of interface states (D_{it}) was calculated using the well-known Hill-Coleman method (Hill and Coleman, 1980). The calculations revealed the interface trap densities before and after radiation exposure to be $1.506x10^{12}$, $1.490x10^{12}$, $1.481x10^{12}$, $1.486x10^{12}$, $1.501x10^{12}$, $1.558x10^{12}$, and $1.507x10^{12}$ $(eV.cm^2)^{-1}$ for exposure times of virgin, 300 s, 600 s, 900 s, 2100 s, 2700 s, and 3100 s, respectively. Like the charge density of radiation-induced oxide traps in capacitance, the densities of interface traps can either be neutralized or generated based on the exposure doses. For dielectric materials to be effective

in radiation detection, a one-way voltage shift behavior is anticipated as the radiation dose increases. The behavior observed at the applied radiation doses indicates that the material has low dosimetric properties. However, it is crucial to recognize that this behavior may manifest at higher dose levels. The measurements revealed that the structure being studied demonstrated electrically stable characteristics when subjected to the radiation field. This stability underscores its potential for developing reliable electronic devices in demanding radiation environments.

5. CONCLUSIONS

This study explored the complex relationships between structural and electrochemical changes and the electrical properties of a dual gate dielectric stack consisting of Eu_2O_3 and SiO_2 on 4H-SiC, with the goal of enhancing the performance of Al/Eu_2O_3/SiO_2/4H-SiC MOS capacitors. The findings underscored the significant impact of annealing on optimizing film characteristics. At an annealing temperature of 800 °C, XRD and AFM analyses revealed improved crystallinity and reduced stress, with a notable crystalline size of 178.41 Å and minimal lattice strain. However, the oxide state density was at its lowest for samples treated at 800 °C, while the best interface state density was observed in samples annealed at 600 °C. The passivation of broken bonds in the bulk Eu_2O_3 layer occurs at higher temperatures, but at 800 °C and above, there may be carbon migration or silicon diffusion from the wafer to the oxide/semiconductor interface. The elemental diffusion can undermine the electrochemical stability of the interface structure, leading to an increase in interface states. ATR-FTIR data corroborated this degradation, revealing a broadening of specific IR bands and a decrease in intensity, indicating a rise in crystal defects. Similar degradation effects were observed in the barrier height of the devices, suggesting that interface states significantly influence the barrier height of SiC-based devices. This influence arises from the formation of localized centers that enhance the capture and emission of carriers, thereby degrading the barrier function of thermally grown SiO_2 at the interface. The study also addressed how X-rays affect the structural and electrical properties of Eu_2O_3 insulating films. The results indicated changes in crystalline size, lattice strain, and electrical characteristics based on the duration of radiation exposure. Structural analysis using X-ray diffraction showed that longer radiation exposure led to a reduction in lattice strain and an increase in crystalline size. These alterations were linked to local heating and structural rearrangements caused by the radiation, highlighting its influence on the structural integrity of Eu_2O_3 films. Electrical characterization through capacitance-voltage (C-V) and conductance-voltage (G/ω-V) measurements revealed that defects induced by radiation resulted in minor changes to the interface states and charge-trapping behavior. Changes in flat band and mid-gap voltages were noted, which corresponded with

the development of traps and the redistribution of charges due to radiation exposure. Even with the introduction of defects, the Eu_2O_3 dielectric maintained stable electrical properties, showcasing its robustness under radiation conditions. Additionally, the material's response indicated limited dosimetric capability within the tested dose range. Nevertheless, its structural and electrical stability in the presence of radiation emphasizes its suitability for use in radiation-tolerant devices. These results highlight the significance of Eu_2O_3 as a high-K dielectric material for advanced electronic applications. Further investigations at higher radiation doses could yield valuable insights into its potential for radiation detection and its wider application in demanding environments.

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