T.R.
BOLU ABANT İZZET BAYSAL UNIVERSITY
INSTITUTE OF GRADUATE STUDIES

FABRICATION AND CHARACTERIZATION OF THE STACKED NUCLEAR RADIATION SENSING FIELD EFFECT TRANSISTORS (NürFETs) WITH HIGH-K

DOCTOR OF PHILOSOPHY

SALEH ABUBAKAR

BOLU, MAY 2021

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ACADEMIC SUPERVISOR
PROF. DR. ERCAN YILMAZ

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APPROVAL OF THE THESIS

FABRICATION AND CHARACTERIZATION OF THE STACKED NUCLEAR RADIATION SENSING FIELD EFFECT TRANSISTORS (NürFETs) WITH HIGH-K submitted by **Saleh ABUBAKAR** and defended before the Examining Committee Members listed below in partial fulfillment of the requirements for the degree of **Doctor of Philosophy** in **Department of Physics, Institute of Graduate Studies of Bolu Abant İzzet Baysal University on 18.05.2021** by

Examining Committee Members	**Signature**
Supervisor Prof. Dr. Ercan YILMAZ Bolu Abant İzzet Baysal University	.....
Member Assoc. Prof. Dr. Aliekber AKTAĞ Bolu Abant İzzet Baysal University	.....
Member Dr. Erhan BUDAK Bolu Abant İzzet Baysal University	.....
Member Assoc. Prof. Dr. Ayşegül KAHRAMAN Bursa Uludağ University	.....
Member Prof. Dr. Kadir GÖKŞEN Düzce University	.....

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Saleh ABUBAKAR

ABSTRACT

FABRICATION AND CHARACTERIZATION OF THE STACKED NUCLEAR RADIATION SENSING FIELD EFFECT TRANSISTORS (NürFETs) WITH HIGH-K
PHD THESIS
SALEH ABUBAKAR
INSTITUTE OF GRADUATE STUDIES
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NürFETs are integrated ionizing radiation sensors that operate on the principle of converting radiation-induced threshold voltages into absorbed doses, which are commonly used to measure absorbed doses in spacecraft, military, high energy physics laboratories, and radiotherapy. However, one of the major drawbacks of the conventional NürFETs is the inability to sense and detect very low radiation doses at the mGy range, which are needed for personal dosimeter and low radiation environments. In this study, the NürFETs with a stacked structure, a design method, where NürFETs are coupled in a stacked structure (stacked-NürFETs) were fabricated. The stacked-NürFETs structure approach was designed to improve the sensitivity of single NürFETs and the performance of the stacked-NürFETs as radiation sensors were investigated and discussed. The pre-irradiation electrical characteristics of the device were evaluated, and the initial threshold voltages (V_{th}) have shifted to larger negative voltage values, which are proportional to the number of the NürFETs increased in the stacked-NürFETs structure. The post-irradiation electrical characteristics of the device were obtained, and their responses to irradiation and possible usages in radiation dosimetry have been investigated and discussed. The results demonstrate that the sensitivities of the stacked-NürFETs are directly proportional to the number of sensors used in the stacked-NürFETs structure.

KEYWORDS: Stacked-NürFETs, NürFETs, Radiation Effects, Radiation Sensors, Dosimeters.

ÖZET

YÜKSEK-K'LI NÜKLEER RADYASYONA DUYARLI ALAN ETKİLİ TRANSİSTÖRLERİN (NürFETs) YIĞIN YAPIDA ÜRETİMİ VE KARAKTERİZASYONU
DOKTORA TEZİ
SALEH ABUBAKAR
BOLU ABANT İZZET BAYSAL ÜNİVERSİTESİ
LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ
FİZİK ANABİLİM DALI

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NürFET'ler, nükleer radyasyona duyarlı alan etkili transistörler uzay araçlarında, askeri alanda, yüksek enerji fiziği laboratuvarlarında ve radyoterapide yaygın olarak soğrulan dozu ölçmek amacıyla kullanılırlar. Bu radyasyon sensörlerinin en büyük dezavantajı bazı medikal uygulamalar ve kişisel dozimetre olarak kullanım için gerekli olan birkaç mGy'den daha düşük radyasyon dozlarını okuyamamalarıdır. Bu çalışmada, yığın yapıya sahip NürFET üretilmiştir. NürFET'lerin yığın bir yapıda birleştirerek bir tasarım yöntemi ile yığın-NürFET'ler elde edilmiştir. Tekli NürFET'lerin radyasyon duyarlığını geliştirmek için yığın yapı yaklaşımı tasarlanmış ve yığın-NürFET'lerin radyasyon sensörü olarak performansı incelenmiş ve değerlendirilmiştir. Aygıtların, ışınlama öncesi elektriksel karakterizasyonu değerlendirilmiş ve başlangıç eşik gerilimleri (V_{th}) yığın-NürFET'lerin yapısında artan NürFET sayısı ile orantılı olan daha büyük negatif gerilim değerlerine kaydığı gözlenmiştir. Yığın-NürFET'lerin ışınlanma sonrası elektriksel karakterizasyonu elde edilerek yığın-NürFET yapılarının radyasyon cevapları ve duyarlılıkları detaylı olarak incelenmiş ve elde edilen veri analizlerine göre yığın-NürFET'lerin olası radyasyon dozimetre olarak kullanımı değerlendirilmiştir. Sonuçlar incelendiğinde yığın-NürFET'lerin hassasiyetlerinin yapıda bulunan artan NürFET sensör sayısı ile doğru orantılı olduğu görülmüştür.

ANAHTAR KELİMELER: NürFET'ler, Yığın-NürFET'ler, Radyasyon Etkileri, Radyasyon Sensörleri, Dozimetreler.

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LIST OF ABBREVIATIONS AND SYMBOLS

A	: Area of Gate Electrode
AFM	: Atomic Force Microscopy
Al	: Aluminum
Ar	: Argon
B	: Boron
BE	: Binding Energy
C	: Capacitance
C_d	: Depletion Capacitance
C_{ox}	: Oxide Capacitance
CP	: Charge Pumping
D_{it}	: Interface State Density
e	: Electron
E_c	: Energy Level of Conduction Band
E_g	: Energy Band-gap
Er_2O_3	: Erbium Oxide
eV	: Electron Volt
E_v	: Energy Level of Valance Band
F	: Force
G	: Conductance
g_m	: Transconductance
Gy	: Gray
h	: Hole
H_2	: Hydrogen Gas
ICs	: Integrated Circuits
I_d	: Drain Current
k	: Dielectric Constant
L	: Length
Mg	: Mid-gap
MOS	: Metal Oxide Semiconductor
MOSFET	: Metal Oxide Semiconductor Field Effect Transisto
N_2	: Nitrogen Gas
N_a	: Acceptor State Density

$\mathbf{N_{fs}}$: Surface State Density

$\mathbf{n_i}$: Instricsic Carrier Concentration

$\mathbf{N_{it}}$: Interface Trap Density

NürFET : Nuclear Radiation Field Effect Transistor

O_2 : Oxygen Gas

P : Phosphorus

Pa : Pascal

$\mathbf{P_s}$: Hole Concentration

Q : Charge

$\mathbf{Q_{acc}}$: Accumulation Charge

$\mathbf{Q_{dep}}$: Depletion Charge

$\mathbf{Q_{eff}}$: Effective Charge

$\mathbf{Q_f}$: Fixed Charge

$\mathbf{Q_{in}}$: Inversion Charge

$\mathbf{Q_{it}}$: Interface Trap Charge

$\mathbf{Q_m}$: Mobile Charge

$\mathbf{Q_{ox}}$: Oxide Charge

RadFET : Radiation Field Effect Transistor

Si : Silicon

$\mathbf{SiO_2}$: Silicon Oxide

$\mathbf{S_R}$: Surface Roughness

T : Temperature

V : Voltage

$\mathbf{V_d}$: Drain Voltage

$\mathbf{V_{FB}}$: Voltage of the Flat – band

$\mathbf{V_G}$: Applied Volatge to the Gate

$\mathbf{V_{ox}}$: Oxide Volatge

W : Width

XRD : X-ray Diffraction

ΔE : Sweep of Surface Potential

$\mathbf{\Delta N_{it}}$: Radiation Induced Interface Trap Density

$\mathbf{\Delta N_{ox}}$: Radiation Induced Oxide Trap Density

ε_0 : Dielectric Constant of Free-Space

ε_i : Dielectric Constant of Insulator

ε_s : Dielectric Constant of Semiconductor

μ_c : Mobility of Coulomb Scattering

μ_p : Mobility of Hole

μ_{ph} : Mobility of Phonon Scattering

μ_{rs} : Mobility of Surface Roughness Scattering

μ_s : Mobility of Effective Surface

ϕ : Potential

χ_i : Electron Affinity of Dielectric

χ_s : Electron Affinity of Semiconductor

ψ_B : Potential of Fermi Level

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1. INTRODUCTION

Nuclear Radiation Field Effect Transistors (NürFETs) or in another name Radiation Field Effect Transistors (RadFETs) are widely used to measure absorbed radiation doses in radiation environments such as spacecraft, military, high energy physics laboratories, and radiotherapy (1–43). The main advantage of the NürFETs sensors is that they are very small in size and provides an instant readout of the irradiated total doses. The dose ranges for various applications are as follows; nuclear application: approximately 10 to 10^5 Gy, space applications: approximately 0.1 Gy to 5000 Gy, medical applications: approximately 10 mGy to 500 Gy, and for personnel dosimetry ranges from 10 μGy to 10 Gy (9,30,44). However, the application and reliability of these devices strongly depend on their sensitivity and stability (4,5,7–9,24,39).

The major disadvantage of these radiation sensors is that they have not been able to read radiation doses lower than a few mGy required for uses in some medical applications and personal dosimeters, due to the low sensitivity of the devices (5,7–9,11,12,19,20,22,23,25,27–29,41). In this study, the stack structure (stacked-NürFETs) approach was designed to improve the sensitivity of single NürFETs and the performance of the stacked-NürFETs as a radiation sensor.

Nearly all of today's technology involves the use of semiconductors, which attracted attention for being a circuit; integrated circuit (IC) (45–49). Almost all of today's radiation sensors are semiconductor-based devices (5,7,10,12,13,16,18,19,24,35,39,40,50–53). To produce reliable semiconducting devices, purification is necessary such as chemical purification. All kinds of impurities can cause significant effects no matter how small it is. Any small inadequacy can distract from how the semiconducting device behaves or perform. Crystalline solids semiconducting materials are the well-known semiconducting materials, but also non-crystalline solids semiconductor exists, such as amorphous and liquid. And these are the combination of different proportions, such as hydro-generated amorphous silicon and arsenic mixtures, tellurium, and selenium. These semiconducting materials share better-known semiconductors the properties of intermediate conductivity and a rapid variation of conductivity with temperature, as well as occasional negative resistance. Such disordered materials lack the rigid crystalline structure of conventional semiconductors such as silicon (54). They are

generally used in thin-film structures, which do not require material of higher electronic quality, being relatively insensitive to impurities and radiation damage (55). A Semiconductor (silicon) is the mother of modern electronics that set the foundation of today's technologies. For the semiconductors, the bandgap is so small between that of conduction bands and valence bands, which excitation of those thermals can overlap or bridge the gaps between. Having such a small gap between, small amounts of doping materials can change the electrical conductivity that can increase conductivity intensely. For an advanced understanding of semiconductors and their properties, electrons-hole movements in the crystal lattice are explained in Quantum Physics (46,49,54,55). The unique arrangement of the crystal lattice makes silicon the most commonly used element in the preparation of semiconducting materials. Increased knowledge of semiconductor materials and fabrication processes has made possible continuing increases in the complexity and speed of microprocessors and memory devices (45,48,55).

In recent years, in many countries, the field of health proton accelerator to produce diagnostic radioisotope, the establishment of new radiation unit for cancer treatment (radiotherapy) and nuclear power plants to meet its energy needs, satellite designs for space exploration are taking important steps in their fields (3,9–13,24,35,39,40,42). These advancements made by researchers in the field of nuclear technologies increase the need for devices that can read the radiation dose with high sensitivity, accuracy, ability, and the capability to measure exposed radiation. It is very important to measure the dose of the environment to determine the dose to which the personnel working in the areas at risk of radiation and to determine the possible radiation damages that may occur in critical electronic components.

The developments of today's technologies have increased the importance of these MOS-based radiation sensors, which are needed for medical and personnel applications. For this reason, the improvement of the sensitivity of the single NürFET via stacked-NürFET fabrication and investigation has been planned. Stacked field effects transistor (stacked-NürFETs/RadFETs), is a new design approach, whereby more than one single NürFETs/RadFETs are connected serially on the same chip to increase the radiation sensitivity of the single field effects transistor sensors (15,44,56–58). The main advantage of these stack structures is

that the sensitivity of the MOS-based field effects transistor sensor is increased depending on the number of NürFETs in the stacked-NürFETs structure (37). Furthermore, for the radiation sensor to be able to measure exposed radiation dose in the lower range the sensitive gate dielectric layer thickness should have to be thicker than 1 µm. The usage of stacked-NürFETs instead of a thicker dielectric gate layer will be a solution to the tunneling effects caused by thicker gate oxides. Using a stack structure will keep the same capacitance and decreases the leakage current (1,37,44,57,58). Therefore, in the scope of this thesis, the MOSFET having SiO_2 and Er_2O_3 gate dielectrics have been fabricated and the possible device usage and device failure mechanism under radiation environment has been investigated comprehensively. Moreover, the variations on the Er_2O_3 characteristics have also been compared to SiO_2 gate dielectric stacked-NürFETs.

The radiation sensors/dosimeters that undertake these tasks are divided into two types, which provide active and passive measurements (46,48,54). With dosimeters that allow passive measurement such as Thermo-Luminescence Dosimeters (TLD) and Optical-Stimulated Luminescence (OST), the dose taken by the user can be measured after a certain period. The TLD is smaller in size and well-characterized. The Optical-Stimulated Luminescence devices such as gas-based sensors require voltage consumption during the measurements. Precisely, the calibration procedures of the TLD, which are widely used in personal dose measurements, are quite multifaceted and the large changes in sensitivity can be seen as important disadvantages of these devices. Another important disadvantage of passive dosimeters is that they cannot measure the dose instantly and cannot act as an alarm in case of any emergency (55,59).

2. GENERAL OUTLOOK

One of the significant advantages of NürFETs is that they can provide both active and passive measurements of the absorbed radiation doses (5,8,41). Radiation dosimeters are devices that measure ionizing radiation doses. Generally, these devices are a combination of electronic components and one or more sensors, which are integrated for measuring devices. Radiation dosimeters can be classified as devices that display dose values directly (active dosimeters) or devices that cannot display dose values directly, thus record a signal that can be measure and converted into doses (passive dosimeters) (45,55):

Active dosimeters: Active dosimeters produce a radiation-dependent signal that displays a direct reading of the radiation sensor dose in real-time. Active dosimeters are electronic dosimeters that can provide real-time information, not only as an integrated dose of radiation environments, but also the dose rate is a very important parameter to be known in case of accidental radiation. They can be equipped with alarms set at different thresholds as required (45,55).

Electronic semiconductor-based active dosimeters are modern sensors that give an instant and continuous reading of cumulative doses and current-applied doses. They are also used as an alarm, which alerts the wearer in case of emergency. Active dosimeters can be used in both high and low radiation environments (45).

Active dosimeters are powered by a battery system and the most commonly active dosimeters are metal-oxide-semiconductor filed effects transistors in which ionizing radiation generate charges resulting in measurable electric currents. Also, a sensing elements tube is used to detect radiation, which indicates the result and processing electronic components, these dosimeters are commonly applicable in portable instrumentations due to their high sensitivity, but they lack reliability. Any ionizing radiation can cause a high avalanche, which can bring about long-time recovery between the pulses in the sensing elements tube. Consequently, these dosimeters have difficulties in measuring high radiation because of the dead time of the tube (5,13).

MOS-based dosimeters are based on ionization in solid such as silicon that has three terminals; source, drain, and gate (MOSFETs). MOSFETs are silicon-based transistors with discharge gate-source structures in which the gate layer is sensitive to ionizing radiation, particularly gamma rays and X-rays. The structure of MOS-based dosimeters includes a MOS structure with a doped source and drain regions. In development mode (V_{GS} ~ 0), p-channel MOSFET dosimeters have an n-type semiconductor as substrate and p + source and discharge regions created by the doping process. When a voltage lower than a threshold voltage ($V_{GS} < V_{th}$) is applied to the gate, there is no current flow between the drain and the source zone, even if there is a drain voltage (V_{DS}). In this mode, the NürFETs act as two front-to-front p-n connections. However, when $V_{GS} > V_{th}$, the semiconductor layer is reversed and a transmission channel is created below the gate dielectric. In this mode, current can flow from the source to the drain in the presence of V_{DS}. Increases in gate voltage increase the number of carriers in the inverted channels and allow more current flow (8,9,13,39).

Passive dosimeters: Solid state devices (dosimeters) such as Thermo-Luminescent, optically induced luminescence, and film (including radio chromic film) that can be placed on personnel working in a radiation environment or inside cavities to measure skin or organ doses. Passive dosimeters are generally used in high radiation environments. The radiation dosimeters that undertake these tasks are passive dosimeters, which provide passive measurements. With dosimeters that allow passive measurement such as Thermo-Luminescence Dosimeters (TLD) and Optical-Stimulated Luminescence (OST), the dose taken by the user can be measured after a certain period (5).

TLD are passive dosimeters that measure exposed ionizing radiation by measuring the visible light intensity, which is emitted from the sensitive region of the crystal in the dosimeter when the crystal is heated. The emitted light intensity depends on the exposed radiation. The TLD is smaller in size and well-characterized. TLD devices were invented in 1954 by Professor Farrington Daniels of the Wisconsin-Madison University. These dosimeters are applicable in which real-time readout is not needed (45).

The Optical-Stimulated Luminescence devices such as gas-based sensors require voltage consumption during the measurements. Precisely, the calibration procedures of the TLD, which are widely used in personal dose measurements, are quite multifaceted and the large changes in sensitivity can be seen as important disadvantages of these devices (45,55).

Another important disadvantage of passive dosimeters is that they cannot measure the dose instantly and cannot act as an alarm in case of any emergency. TLD and film badges are the commonly used passive dosimeters. These passive dosimeters generate radiation-induced charges (signal), which are stored in the devices and the outputs are analyzed later.

2.1 NürFETs

NürFETs are discrete p-channel Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) with a gate oxide optimized for radiation sensitivity, which is also known as RadFET. The domestic production of these devices consisting of a single sensor was comprehended within the scope of the project titled TÜBİTAK 3001-114F066 "Production and Characterization of Silicon-Based Nuclear Radiation Field Effect Transistors (NürFETs), which was fabricated at Nuclear Radiation Detectors Applications and Research Centre (NÜRDAM) (5,8,14,41).

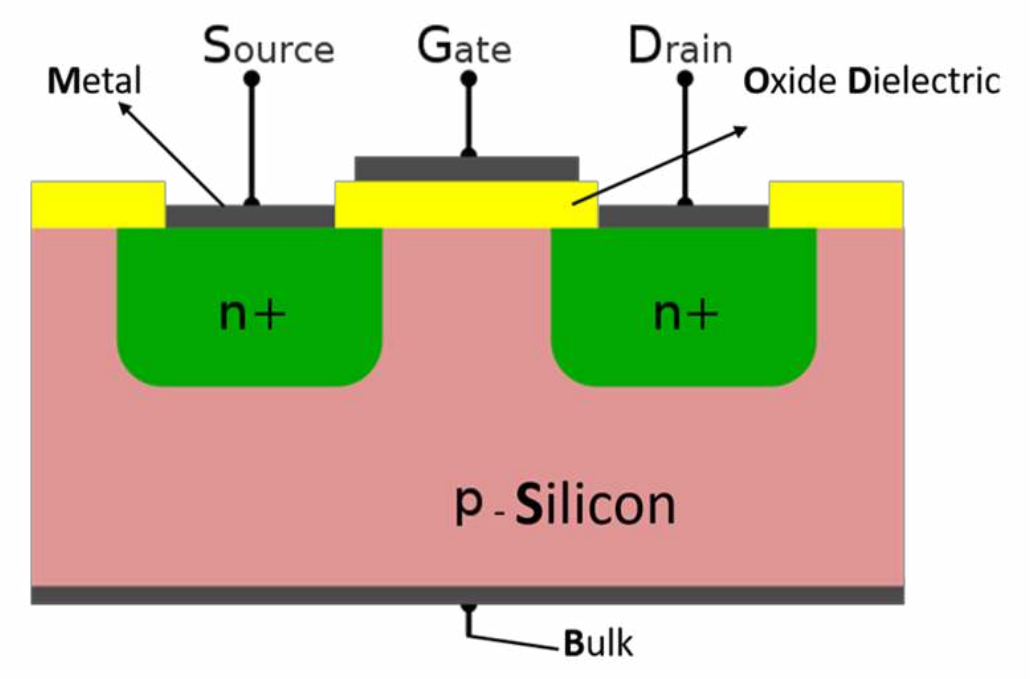


Figure 2.1. A schematic illustration of p- channel NürFETs.

The structure of NürFETs contains a MOS structure with a doped source and drain regions. At enhancement mode (V_{GS} ~ 0), a p-channel NürFET has an n-type semiconductor as substrate and p^+ source and drain regions formed by the doping process. A schematic illustration of p-channel NürFETs is shown in Figure 2.1. When a lower voltage than a threshold voltage ($V_{GS} < V_{th}$) is applied to the gate, no current flow occurs between the drain and source region even in the existence of drain voltage (V_{DS}). In this mode, NürFETs act like two front-to-front p-n junctions. However, when $V_{GS} > V_{th}$, the semiconductor layer is inverted and a conduction channel below the gate dielectric is formed. In this mode, the current can flow from source to drain in the presence of V_{DS}. The rises in the gate voltage enhance the number of carriers in the inverted channels and allow more current flow (5,7–9,24,39).

2.2 Fundamentals of NürFETs

2.2.1 Gate Dielectric Materials

The device gate insulator layer of these MOS-based transistor sensors produced on the n-type silicon substrate is made of dielectric materials. Dielectrics can be defined as materials where the electrostatic field could persist for a long time. The dielectrics do not have free electrons; hence exhibit very high resistance to conduct the electricity, but their behavior may be switched under an applied electric field. The dielectric phoneme comes from polarization characteristics which are electronic polarization, ionic polarization, orientation polarization, and space charge polarization, of the materials. Dielectrics have positive and negative charges which are bounded by an elastic force having a spring. Under the applied electric field, these coupled charge pairs cannot move inside the insulator; the positive and negative charges pull the spring to opposite directions resulting in a rise in the spring tension which is proportional to the applied electric field. After a critical point, a continuous increase in the applied electric field is going to breaks the imaginary spring, and the charge becomes free, which resulting in the insulating dielectric layer starting to conduct an electric current (5,8,9,11–14,20,25,39–41).

Depending on several parameters, such as polarization magnitude and bandgap of the materials, the dielectric constant exhibits variations between materials to materials. The SiO_2 has been a conventional dielectric layer with permittivity of 3.9, for years. For the MOS-based technology, the high- k materials can be defined as materials that have a dielectric constant value higher than silicon

nitrate (k = 7) (45,48,55). Some of the high-k dielectric materials are Titanium Oxide (TiO_2), Hafnium Oxide (HfO_2), Aluminum Oxide (Al_2O_3), Erbium Oxide (Er_2O_3), etc. These high-k dielectric materials have been used in several applications such as optoelectronics, MOS-based sensor technologies, depending on their material specifications (52,60–64). On both sides of the gate dielectric layer, there are p+ regions that are formed by boron doping as drain and source. With the applied electric field to the gate electrode, the minority charge carriers begin to advance into the channel region. If enough voltage is applied to the gate electrode (above the threshold voltage), a current will flow from source to drain (48,59,65,66).

Reducing the scaling of MOS transistors caused the high gate and channel leakage current when the SiO_2 was used as gate dielectrics. This means that devices become unreliable. Hence, conventional SiO_2 had to be replaced with suitable new gate dielectrics. Due to high resistance to the passage of electric current characteristics, the high- k dielectrics can be introduced as new gate dielectric materials to replace conventional SiO_2 layer for the future device approach. A MOS-based transistor electrical source-drain current is strictly connected to a capacitance of the gate dielectric which can be expressed as $C = \varepsilon_0 kA/t$ where ε_0 is the permittivity of free space, k is the relative dielectric constant, A is the area of the gate contact, and t is the thickness of the dielectric layer. Leakage currents decrease almost exponentially with enhancing dielectric thickness. However, the usage of the high-k dielectric layer instead of the physically thicker SiO_2 dielectric layer may be a solution to the tunneling effects. The use of the high-k materials is going to keep the same capacitance while it decreases the leakage current. In a general view, the electrical thickness of a novel high-k dielectrics in terms of equivalent SiO_2 thickness or 'equivalent oxide thickness' can be expressed as $EOT= d(3.9)/k$ where 3.9 is the dielectric constant of SiO_2 (46,48,54,67–69).

As mentioned above, the high-k dielectrics are promising for MOS-based electronic applications, but not all high-k materials are convenient for MOSFET applications. Some issues have to be solved for the process integration of high-k dielectrics to be used in the device applications; Permittivity, thermodynamic stability with silicon, bandgap and band-offset values, kinetic stability, interface quality, and the gate electrode (50,52,60,62–64,70–79):

Permittivity: The static dielectric constant of selected materials should be higher than that of SiO_2. The convenient dielectric constant for the gate dielectric applications should be in the range of 10 to 40. The general trend of the high-k value of dielectrics is inversely proportional to the bandgap. Hence, dielectric having a large k value, causes a strong fading field which degrading the channel performance (80–82).

Thermodynamically stable with silicon: The deposited dielectric materials must not react with underlying Si to form parasitic suboxide (SiO_x) and silicide. The presence of any form of the SiO_x is going to decrease the equivalent oxide thickness and metallic silicate (MSi_x) formation may increase the tunneling effects. The selection of a dielectric layer that has large Gibbs free energy of formation to prevent reaction with Si is a suitable way to eliminate the parasitic phase formation (55,68).

Bandgap and band-offset values: The dielectric materials have to be insulators; the expected bandgap level for the microelectronics must be higher than 5 eV. Besides, barrier potentials for electron and hole conduction should be at least 1 eV to prevent Schottky emission from dielectric material bands (55,59,66,68).

Kinetic stability: Dielectrics should resist the dopant activation anneal for at least 5 seconds at 1000 ^{0}C. The problem arises for some gate dielectrics having lower crystallization temperatures. Crystallized dielectrics that have grain boundaries acted as dopant diffusion path, location of the trap center lead to increase in the leakage current. Also, the thickness of the gate oxide can have the same dimensions as crystalline-grain size at low scales. Hence, the uses of amorphous materials are more common for MOS transistors. On the other hand, it is also reported that crystallization of the dielectric layer sometimes enhances the dielectric constant of the film (61,63,64,71–73,76,83–87).

Interface quality: The conventional SiO_2/Si interface exhibits excellent interface quality for the MOS technologies. Interface defects are important due to the following reasons; the threshold voltages may shift to higher values due to trapped charges, the number of trapped charges may change with time, causing devices operating characteristics, the carriers can be scattered by defect site in channels, leading to lower carrier motilities, and the higher number of traps may cause a dielectric breakdown. The interface quality of the film can be generally

controlled by the fabrication process. To obtain good electrical performance, the deposited dielectric layer must have good uniformity, low roughness, and a high-quality interface. The interface trap density must be in the order of 10^{10} cm^{-2} for high interface quality; however, it is acceptable up to 10^{12} cm^{-2} in microelectronics (60).

Gate electrode: The interface structure between gate contact and the dielectric layer is one of the significant criteria for the specifications of the MOS-based device. The selection of the gate electrode can be changed depending on the device structure. For n-channel MOSFETs gate electrodes having a low work function which is close to the conduction edge of silicon (4.06 eV) are suitable. However, the p-channel MOSFETS gate electrodes having a high work function, which is close to the valance edge of Si (5.10 eV), are more useful (46,54,55,59,65–67). Suitable gate electrodes deplete the Si layer and the conduction band edge bends to Fermi Level. Hence only a small applied voltage is required for saturation. Such gate is necessary for low threshold voltage and sub-threshold slope for MOSFETs (5,12,19,80,86,88,89).

2.3 Impurities in the MOS Structure of NürFETs

In the ideal MOS structure, no impurity charges exist at the dielectric layer and dielectric/semiconductor interface (48,90–93). Though, in the non-ideal device structure, one cannot eliminate the presence of parasitic charges even in SiO_2/Si interface in which a perfect interface structure is expected. In the previous studies, the MOS devices have revealed that the presence of the parasitic charges strongly influences the electrical performance of MOS-based transistors including the threshold voltage, leakage characteristics, mobility of carriers, etc. The charges in device structures are mobile ionic charges, fixed oxide charges, oxide trapped charges, and interface trapped charges (60,63,71,74,77,79,85,94,95).

2.3.1 Mobile Charges

Mobile ionic charges are ionized alkali metals, such as sodium-ions and potassium-ions. These charges are relatively moveable in the dielectric layer even in low temperature and low gate voltages. Therefore, the higher density of these ionic charges causes significant ionic current and threshold voltage shift which degrade the performance instabilities. These impurities are due to the cleaning process and used chemicals during the fabrication steps. For few decades, great developments have been achieved to avoid impurities associated with mobile ions

by using clean rooms and a hands-free cleaning process. The orders of mobile ions are 10^{11} cm^{-2} for real MOS devices. The mobile ions are almost positively charged result in a net amount of these charges because of a negative voltage shift. The densities of these charges can be specified by bias-temperature stress techniques. In bias-temperature stress techniques, following the complete fabrication process, the capacitance curves of the device are measured. After that, devices are heated to certain temperatures and positive voltages are applied to the gate. Following the cooling of the device under negative gate voltage, the capacitance curves are measured and then the Q_m can be calculated using the following relation (46,54,65):

$$Q_m = C_{ox} [V_{FB} (-Voltage) - V_{FB} (+Voltage)] \quad (2.1)$$

This technique is useful for the detection of high mobile ionic concentration typically 10^{13} cm^{-2}. When the concentration of the mobile ion approaches 10^{11} cm^{-2}, the limitation occurs due to the electron/hole injection toward the gate layer. Especially, possible holes transport under gate voltage may create a new defect in the dielectric layer. The contribution of the created new defect to flat band voltage may deviate from the real mobile ion calculation (46,54,59,65,66,68).

2.3.2 Oxide Charges

Owing to the oxidation-induced defects, impurities, or generation of defects created by irradiation or similar bond-breaking processes of dielectric, the oxide charges can be generated. Roughly, these charges are fixed oxide charges (Q_f) and oxide trapped charges (Q_{ox}). The fixed oxide charges cover positive charges inside the dielectric layer which are close to the dielectric semiconductor interface, these charges are usually generated during the fabrication process. These charges are immobile under applied voltage and temperature stressing. Hence, the contribution of the fixed charges to the flat band or threshold voltage shift is fixed and stable. Oxide trapped charges cover almost all charges which are captured by defect site generated by irradiation or by the applied field and temperature stress. The trapped charges in the oxide layer can be positive or negative but they are generally positive charges, which are holes. The oxide trapped charges may move under the applied electric field by hopping or tunneling mechanism. The total contribution to flat band/threshold voltage can be positive or negative depending on the sign of the oxide trapped charges (20,51,80–82,96–112).

2.3.3 Interface Charges

The interface charges are charges that are trapped at the electronic energy level of the dielectric/semiconductor interface. These charges increase due to lattice mismatch between the dielectric/semiconductor interface, dangling bonds, etc. Interface traps create a kind of potential well at the interface where both electrons and holes can be trapped (55,59,65,66,92).

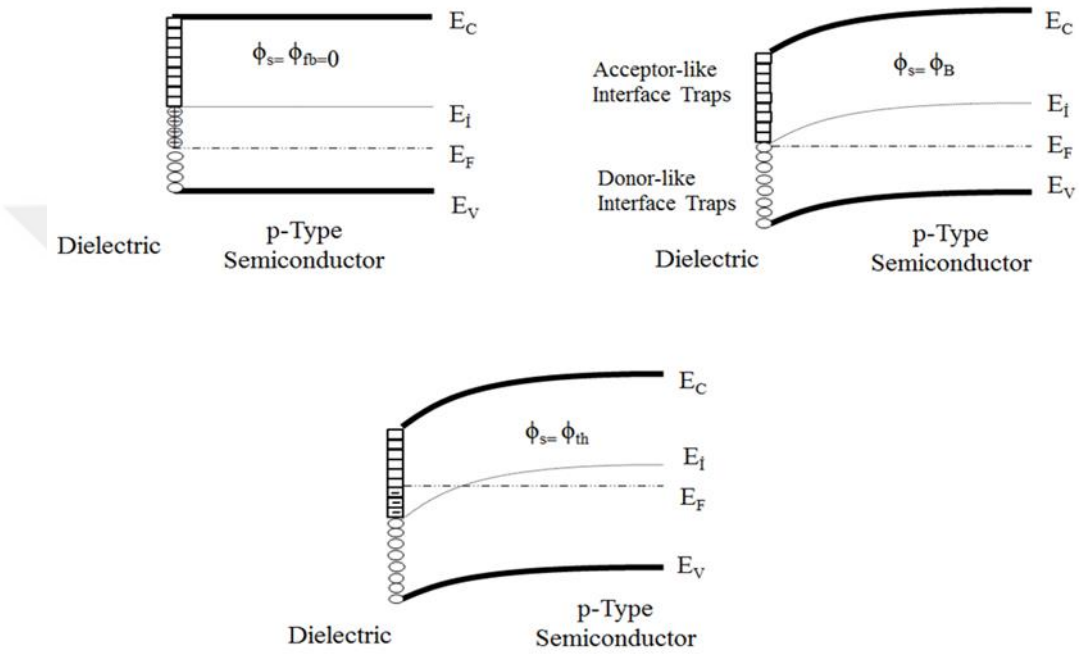


Figure 2.2. A physical illustration interface traps (45).

Due to the presence of additional field generated by interface trapped charges, the carrier mobility is degraded when the device operated in saturation. Besides, the presence of field causes the bending of the energy bands and shifts the flat band/threshold voltages. A localized trap site at the energy band can release mobile carriers depending on the applied voltage field. These behaviors decrease the device's reliability. Hence, the low interface trap density of the device is curial to reach expected device performance. Energy band diagram of dielectric/semiconductor interface incorporating the interface traps for the cases; $\phi_s = 0$, mid-gap level ($\phi_s = \phi_B$) and $\phi_s = \phi_{th}$ (55,66).

Two types of defects exist in the forbidden band of the semiconductor. The trap sites localized near the conduction band are called acceptor-like traps where an

electron can be trapped while the trap sites close to the valence band are called donor-like traps where holes can be trapped. The physical illustration of these interface traps is depicted in Figure 2. 2. Acceptor-like interface traps behave like acceptors and they are neutral when empty. When electrons are captured, their charges change to negative. On the other hand, donor-like interface traps behave like donors and they are positively charged while empty. The donor-like interface traps become neutral when they are filled with electrons. On the other hand, in the mid-gap level, the interface trap charge is zero for $\phi_s = \phi_B$. Therefore, no additional contribution from interface traps to the voltage shift is observed at the mid-gap level. This energy level also tends to pin the semiconductor Fermi level at the surface and also the presence of higher localized interface trap density influences the barrier height of the device. It means that at accumulation, almost all the donor-like trap charges are positive and the acceptor-like traps are neutral. Hence, the total charge due to interface states, Q_{it}, will be positive. When gate voltage increases, some of the acceptor-like traps moves below the Fermi level and capture electron. Since donor-like traps are neutral, the net charge due to interface states will be negative at inversion (48,55,59,66,69). The amount of these charges can be calculated by the following relations;

$$Q_{it} = \int_{E_F}^{E_{cb}+ q\emptyset_s} D_{it}\ (E)\ dE \tag{2.2a}$$

$$Q_{it} = -q \int_{E_{vb}+ q\emptyset_s}^{E_F+ q\emptyset_s} D_{it}\ (E)\ dE \tag{2.2b}$$

Where D_{it} represents the interface trap density per energy level. Eq. (2.2a) is valid assuming all interface traps are donor-like, whereas Eq. (2.2b) is valid assuming all interface traps are acceptor-like. The limits of integrals change with the modulation of Fermi level and the surface potentials of the semiconductor (50,60,73,76,78,79,83,85,86,94,113,114).

2.4 Electrical Characteristics of NürFETs

2.4.1 Threshold Voltage

The threshold voltages are crucial for the operation of the NürFETs because the current flow is almost zero below the threshold voltage (V_{th}) values. The MOS-based transistors behave like a two p-n junction, whereby the only current that exists

is the diffusion current and its value is almost zero. When the applied electric field to the gate is above the V_{th} ($V_{GS} > V_{th}$), the MOS-based transistor (NürFET) becomes a current source and it starts to conduct current in the presence of any small voltage applied (drain to source). The initial V_{th} should be close to the theoretical values typically less than 1 V depending on the capacitance of the gate dielectric. The larger values of V_{th} than ideal values indicate the presence of high parasitic charge densities. Large V_{th} requires a large power supply and this enhances the power consumption and heat generation during the operation of devices (3–5,8,9,11,12,19,22–24,39).

2.4.2 Drain Current in a Linear Region

Under sufficiently high gate voltages ($V_{GS} > V_{th}$), an inversion layer forms where the current would flow. The higher V_{GS} enables stronger inversion, i.e., larger mobile carrier, and higher conduction between source and drain (66,69). Under constant V_{GS} above the V_{th} value, the drain to source current is controlled by drain voltage. For a small V_{DS} value, carriers start to flow from source to drain and inverted channels act as a resistor; thus, the drain current (I_{DS}) is proportional to V_{DS}. These I_{DS} - V_{DS} relations continue linearly and this region is called a linear region. In the linear region, the V_{DS} is lower than the saturation value of $V_{DS,}$ and drain current is proportional to inversion charge times velocity of carriers expressed as follows (65,66);

$$I_{DS} = -WQ_{in}(y)\,V(y) \tag{2.3}$$

Where W is the channel width and velocity defined as mobility (μ_p) times electric field (E), therefore,

$$I_{DS} = -WQ_{in}(y)\,\mu_p E \tag{2.4}$$

Here charge density can be defined as $Q_{in} = C_{ox}$ ($V_{GS} - V(y) V_{th}$) and Eq. (2.4) becomes;

$$I_{DS} = -WC_{ox}\,[V_{GS} - V(y) - V_{th}]\mu_p E \tag{2.5}$$

The electric field is correlated with negative gradient of voltage along the channel, hence;

$$I_{DS} = WC_{ox}\,[V_{GS} - V(y) - V_{th}]\mu_p \frac{dV}{dy} \tag{2.6}$$

When we integrate Eq. (2.6) between the channel boundaries.

$$\int_0^L I_{DS}\,dy = \int_0^{V_{DS}} WC_{ox}\,[V_{GS} - V_{th}]\mu_p\,dV \tag{2.7}$$

The solution of Eq. (2.7) gives us the I_{DS} current as follows;

$$I_{DS} = \mu_p\, C_{ox}\, \frac{W}{L}\, [(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}] \tag{2.8}$$

This relation is valid for the linear region of I_{DS} - V_{DS} characteristics, i.e., relatively small values of V_{DS}. Therefore, in this region, the field effects transistors behave like voltage-controlled resistors (59,65,66,68,69).

2.4.3 Drain Current in a Saturation Region

Further increase in the V_{DS} beyond the linear region causes a reduction in the inverted layer width near the drain region. This region is called the pinch-off point. In this case, the channel current remains almost constant, regardless of further rises in the V_{DS}. At the pinch-off point, drain to source voltage is equal to the drain to source voltage in the saturation region, which is also equal to the $V_{GS} - V_{th}$ (55,66).

$$I_{DS,Sat} = \mu_p\, C_{ox}\, \frac{W}{2L}\, (V_{GS} - V_{th})^2 \tag{2.9}$$

Therefore, in the saturation, the drain to source current is directly correlated to square dependence of gate to source voltage and is independent of drain voltage.

2.4.4 Trans-Conductance Characteristics

Trans-conductance (g_m) is defined as the ratio of the change in drain current to the change in the gate voltage. The trans-conductance of a device can be obtained from the following relation;

$$g_m = \frac{\partial I_{DS}}{\partial I_{GS}} \tag{2.10}$$

The g_m is important for specifying voltage gain in liner mode. However, the g_m value should be zero for the ideal MOS-based transistors characteristics in saturation mode. For the non-ideal devices the g_m in saturation can be calculated using the following expression;

$$g_m = \frac{\partial I_{DS}}{\partial I_{GS}} = \frac{W}{L} \mu_p C_{ox} (V_{GS} - V_{th}) \tag{2.11}$$

Therefore, it can be concluded that g_m can be obtained by specifying the slope of the $I_{DS} - V_{GS}$ curve in saturation (66,69).

2.4.5 Sub-Threshold Current

The drift current conduction mechanism is dominant for the current flow when the transistor is operated in the saturation mode as mentioned before. However, the dominant conduction mechanism is the diffusion of carriers for the gate to source voltage below the threshold voltage. Therefore, two different carriers flow mechanisms exist for the drain current conduction (66,69).

The ideal value of the drain current should be zero when the gate voltage is below the V_{th}. However, carriers do not disappear when the gate voltage is lower than the V_{th}. The presence of minority carrier immigration occurs due to the presence of PNP and NPN regions when the p-channel/n-channel device is operating in the sub-threshold regions. The drain current is proportional to the exponential function in the sub-threshold regions. In the weak inversion region specification of the sub-threshold parameter, n is expressed as follows;

$$n = 1 + \frac{qN_{fs}}{C_{ox}} + \frac{C_b}{C_{ox}} \tag{2.12}$$

Where N_{fs} is voltage-dependent surface state density, C_b is the depletion capacitance per unit area. Here, the voltage-dependent surface state density is an important parameter for the sub-threshold regions. It typically varies between 2 – 4, but it also changes due to the fabrication process depending on the surface states (5,6,10,11).

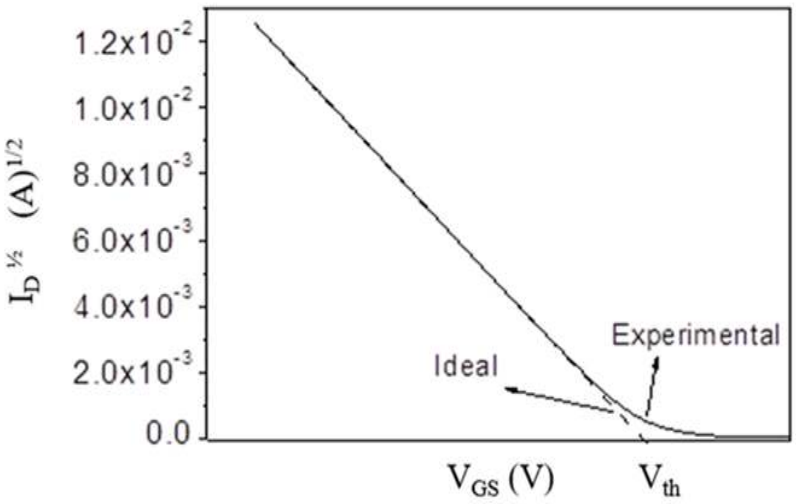


Figure 2.3. I_D curves for ideal and experimental measurements (45).

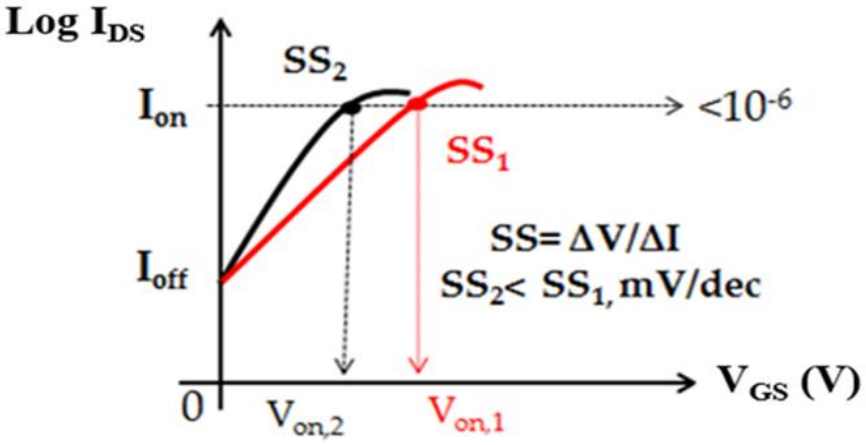


Figure 2.4. Sub-threshold regions current below the V_{th} for two slopes (115).

The n parameter is directly proportional to thermal voltage to express the gate to a source voltage value, which marks an arbitrary boundary between strong inversions; the current is proportional to the square of the gate to source voltage, and a weak inversion; the current is proportional to the exponential function of the gate to source voltage. And this boundary is called V_{on};

$$V_{on} = V_{th} + n\frac{kT}{q} \tag{2.13}$$

The drain current at V_{on} is called $I_{on.}$ This I_{on} current and V_{on} parameters are important because they are critical values to jump from the sub-threshold region to strong inversion regions (66,69). Because the drain current is proportional to the exponential function, the semi-log plot of I_D below the I_{on} linearly changes as seen in Figure 2.4. The inverse slope of log I_D - V_{GS} characteristics in the sub-threshold region is defined as sub-threshold swing (SS) which is the function of n (66,69);

$$SS = n\frac{kT}{q}\log(10) \tag{2.14}$$

In real devices, SS values are higher than 60 mV/dec typically 70-80 mV/dec is good for real devices. The small value of the SS is desirable for microelectronic systems, especially, for digital electronics. As seen in Figure 1.4, the current drops more slowly for the higher value of SS. Lower SS (mV/dec) is required for low power consumption and low leakage below the V_{th}. This consideration is important for the art-of-state scale area, where small leakage current in off devices degrades the total processor currents, for example; 10 pA sub-threshold current for MOS devices in one billion transistor causes 1A in off states (54,65,66,69).

2.4.6 Channel Mobility

Mobility is defined as the ability of the carriers' respond to an external electric field. The MOS-based transistor's performance is generally evaluated by I_D in saturation. The I_D in saturation is directly proportional to channel mobility of carriers denoted by μ_p for holes, μ_n for electrons as seen in Eq. 2.15. The bulk mobility of the Si is 480 cm^{-2}/V at $N_a = 10^{16}$ cm^{-3} doping density for hole carriers, and 1430 cm^{-2}/V at $N_d = 10^{16}$ cm^{-3} doping density for electron carriers. However, the mobility of the carriers near the interface is lower than the bulk due to several scattering mechanisms (54,65,66,69). The basic scattering effects to inversion carriers are given following:

Coulomb scattering (μ_c): Depending on the fabrication process, various charge impurities are localized close to the dielectric/semiconductor interface. These charge impurities such as ionized impurity (doping concentration amount) at

the substrate, interface states, fixed charges may scatter the carriers in the inversion layer via Coulomb force. This Coulomb force is proportional to the impurity concentration at the surface where the inversion layer occurs and it is the dominant mechanism when inversion carrier density is low or high depending on channel doping (66).

Phonon scattering (μ_{ph}): Presence of vibration in the lattice of a substrate at dielectric/semiconductor interface, bulk lattice vibration under external electric field and temperature causes lattice phonon scattering. This scattering mechanism becomes dominant in the intermediate transverse electric field (55).

Surface roughness scattering (μ_{sr}): Any discontinuity and deviation from an abrupt dielectric/semiconductor interface where inversion carriers are located cause extra quantum well. The value of dielectric/semiconductor interface and correlation length of oscillations in the surface should be small to decrease roughness scattering effects. Considering this scattering mechanism, the effective surface mobility, $\mu_{s,}$ can be calculated by Matthiessen's' rule expressed as follows (54,59,65,66);

$$\frac{1}{\mu_s} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{2.15}$$

2.5 Non-Idealities in the NürFETs Characteristics

Non-idealities in the NürFETs naturally degrade the device performance. The important non-ideals are the presence of trap sites and trapped charges in the dielectric and its interface underlying semiconductors. The non-idealities come from the design and operation of the MOS-based transistors which may also deviate from the ideal device characteristics. The important non-idealities are explained below;

Short channel effect: Due to the scaling of the device geometries, the influence of the applied electric field becomes important. Above the "pinch-off" voltage. Drain current in the saturation region, the inverted channel length reduces by a value ΔL. The variations on the ΔL can be attributed to a high electric field generated by V_{DS} Thus, the expression for drain current in Eq. (2.9) becomes;

$V_{D,\,Sat} < V_{DS}$;

$$I_{DS,Sat} = \mu_p C_{ox} \frac{W}{2(L-\Delta L)} (V_{GS} - V_{th})^2 \quad (2.16)$$

Now that ΔL is smaller than L, equation (2.16) becomes;

$$I_{DS,Sat} = \mu_p C_{ox} \frac{W}{2L} (V_{GS} - V_{th})^2 (1 + \frac{\Delta L}{L}) \quad (2.17)$$

Therefore, $\Delta L/L = WV_{DS}$ where w is the channel-length modulation parameter. Thus Eq. (2.17) becomes;

$$I_{DS,Sat} = \mu_p C_{ox} \frac{W}{2L} (V_{GS} - V_{th})^2 (1 + kV_{DS}) \quad (2.18)$$

Another short channel influence is the reduction of the threshold voltages. Overlapping source and drain depletion become the significant effect. This causes the depletion region under the inversion layer to increase. The wide depletion region enhances the surface potential, thus this decreases the required V_{th} value of the device to form saturation regions. This effect is also known as drain-induced barrier lowering. To reduce drain-induced barrier lowering under a high drain electric field, a lightly doped drain region is used in the state-of-the-art MOS devices (54,59,65,66).

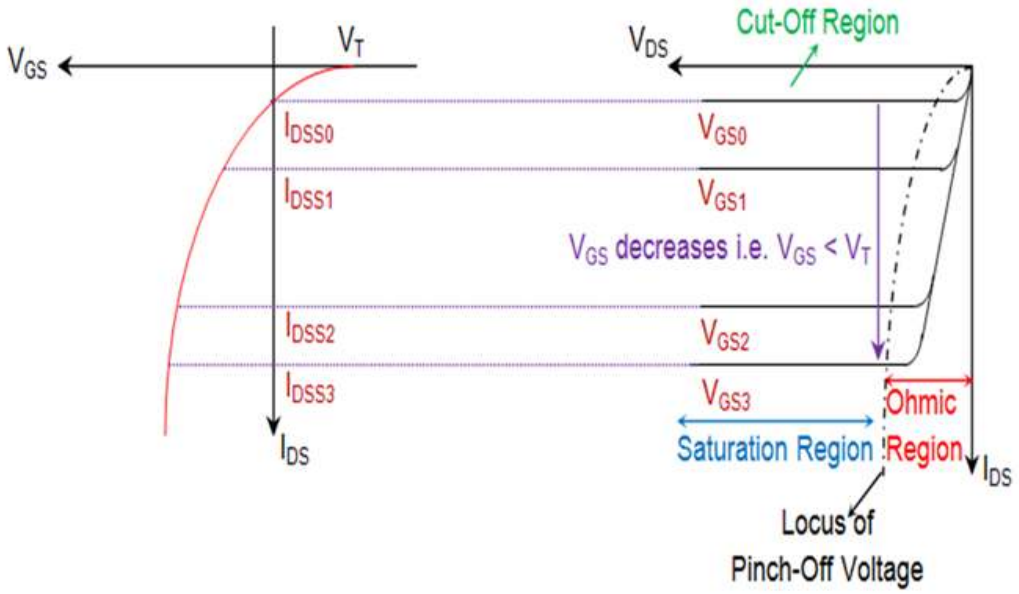


Figure 2.5. Effects of the short channel in the I_{DS} characteristics, and I_{DS} degradation due to saturation velocity in the short channel (59).

Substrate current: The dramatic increase near the drain region beyond the saturation V_{DS}, carriers gain high energy between scattering events to cause impact ionization upon following a collision which is especially observed for short channel

devices. These hot carriers generate additional electron-hole pairs. Generated electrons are gathered in the substrate, while holes contribute to the I_{DS} in p- channel MOS devices. This substrate current is proportional to V_{DS} beyond the strong inversion and contributes to the conductance term of the device. The highest influence of this additional conductance becomes a problem for one who requires minimum output conductance at high V_{DS} (54,59,65,66).

Gate current: This gate current is produced by hot carriers formed under a high electric field. The hot carriers may move along the gate dielectric either creating the new trap states or hoping mechanism. Hence, it degrades the electrical performance of devices. On the other hand, this movement is sometimes useful for devices used in non-volatile memories but reduces long-term reliability (55).

Bulk contact effect: The V_{th} value of the devices is also affected by the voltage applied from the bulk contact. The applied voltage difference between the source and the bulk, V_{BS}, changes the depletion layer width which causes a difference in the threshold voltages (54,55);

$$V_{th,bs} = V_{th} + \gamma(\sqrt{2\emptyset_b} + \sqrt{V_{bs}} - \sqrt{2\emptyset_b}) \tag{2.19}$$

$$\gamma = \frac{\sqrt{2qN_a\varepsilon_s}}{C_{ox}} \tag{2.20}$$

Where γ is the body effect parameter. As seen in Eq. (2.20), body effect can be controlled by doping concentration of semiconductor and dielectric layer capacitance. To control the bulk effect, generally, the bulk terminal is directly connected to the source during the device operations (5,7,8,24,41).

Temperature effect: The threshold voltage of the devices can be varied by temperature approximately from -1 to -3 mV/^{0}C. Besides, the mobility of the carriers decreases with increasing the operating temperature of the devices (66,69).

2.6 Radiation Interaction with Matter

Any electromagnetic waves or energetic particle that can have enough energy to create ion pairs by interaction with matter is called ionizing radiation. The ionizing radiation can interact with materials in several ways depending on their type, energy, charge, and density of the target material (45). Radiation interacts with materials in two ways. Charged particles, like gamma, beta, or alpha particles

having sufficient kinetic energy, directly interact with atoms and molecules to create electron-hole pairs. This process is known as direct ionization due to no intermediary step required. On the other hand, non-charged particles such as photons and neutrons interact with atoms, and molecules release charged particles and these charged particles cause ionization in the matter by a direct mechanism (49,65,66,69). This process is called indirect ionization. The details of the radiation interaction mechanism are explained below:

2.6.1 Charged Particles Interactions with Matter

The charged particle irradiation is a particle with an electric charge and has enough energy to cause ionization in the matter. These particles mainly transfer their energies with Coulomb attraction and repulsion with electrons of target materials (45). The interaction probability of these charged particles with matter and the traveling range inside the materials is directly connected with the magnification of its charge and energy. For the proton and non-relativistic nuclei, ionizing density is inversely correlated to their energy declining with range and is proportional to the square of their charge. These particles interact with Coulomb scattering which can induce ionization for a proton with energy less than 100 keV. Excitation or displacement can occur and collision with nuclei and nuclear reaction may also occur energies higher than 10 MeV (45,49). On the other hand, charged particles having lower mass such as electron and beta irradiation are much more freely than heavy-ion radiation. In addition to Coulomb interaction, when electrons decelerate in the target material, they also lose energy by emitting Bremsstrahlung in form of an X-ray (46,54,65,66,69).

2.6.2 Neutral Particles and Electromagnetic Radiation Interaction with Matter

Neutrons are an excellent example of uncharged particle radiation which has almost the same mass as protons. Thanks to their neutrality, neutrons cannot exhibit electrostatic interactions with materials; hence, they move in a straight line until they collide with a nucleus to be scattered into a new direction or absorbed. Neutron can interact with materials basically in three ways (45,47). The first interaction type is a nuclear reaction. When indecent neutrons are absorbed by the target, the secondary particles or electromagnetic radiation, e.g., protons, gamma rays can be

emitted. Elastic scattering is the second type of interaction with matter. When neutrons collide with the target nucleus, they transfer some amount of their energy and continue their path. If sufficient energy is transferred to the target atom, the nucleus of target materials may be displaced as ionization nuclear displacements. An inelastic collision is the third interaction type with the matter. In an inelastic collision, neutrons are captured by target material having a relatively high atomic number of the nucleus (Z) and re-emitted by target nuclease together with gamma radiation. Interaction types are correlated with the energy of neutrons. Generally, slow neutrons interact with the target materials via nuclear reactions or elastic collisions, fast neutrons interact via elastic collisions. Also, inelastic collisions dominate for extremely energetic neutrons. Another neutral radiation type is photon radiation which is an electromagnetic wave that is classified by its energy. The X-rays having energies from 100 eV to 100 keV and gamma-rays having energies from a few hundred keV to a few MeV are two important photon types for nuclear physics applications. The ionizing photon radiation interaction with target materials can be classified into three phenomena. The first interaction type is photoelectric effects. The incident photon emits or ejects electrons from the target materials by losing all their energies. The ejected electrons come back to their ground states by emitting low-energy photons that can also interact with target materials (45).

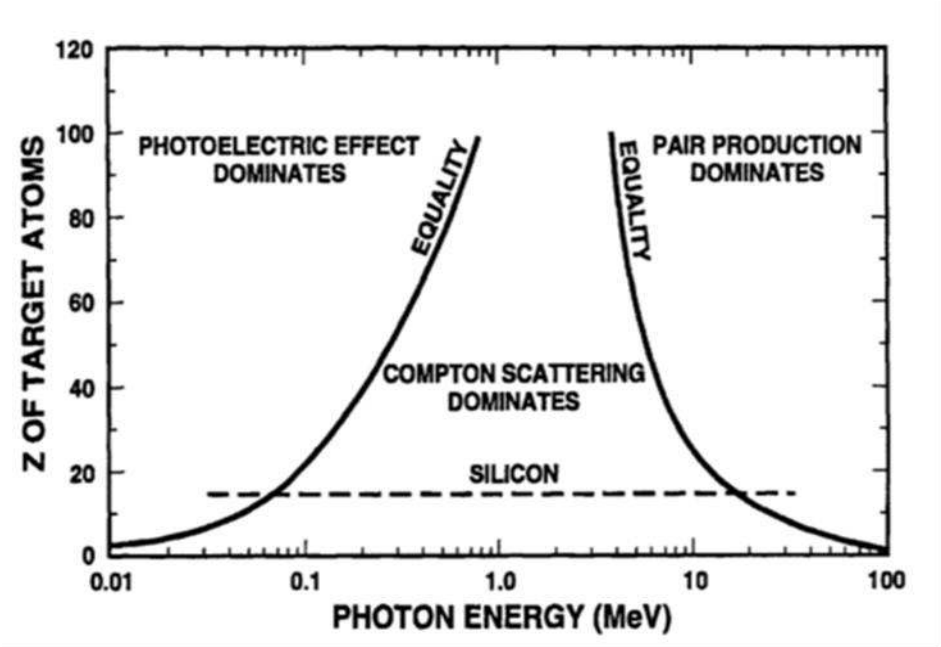


Figure 2.6. The dominant photon - matter interaction mechanism depending on incident photon energy and the atomic number of target materials (65).

Compton scattering is the second interaction phoneme. In this phoneme, the incident photon hits the target materials and loses its energy and it emits a free electron and energetic photon. The last interaction type is pair production. The incident photons completely lose their energy creating electron-positron pairs. The positron combines with an electron. Result of this annihilation of the positron two new photons is created. These photons may also interact with target materials. The pair production can occur when photons have energies higher than 1.024 MeV, but to be the dominant interaction mechanism the energy of the incident photon should be much higher than 1.024 MeV. All these types of interaction can be observed when materials are exposed to ionizing radiation, especially, for higher energies. However, depending on the incident photon energy one or two phonemes dominate the basic interaction phoneme that occurs inside the material under radiation exposure. The dominant interaction phoneme depending on the atomic number of the target material and incident photon energies can be seen in Figure 2.6 (45,49).

2.7 Radiation Effects on NürFETs

Ionizing radiation interactions with material via Compton scattering, Coulomb interaction, etc., cause ionization on the target material. An enormous number of electron-hole pairs and new trap centers were generated in the dielectric as a result of the ionization and its interface with the underlying semiconductor. Four major physical processes are observed in the radiation responses of the MOS structure (45,55). The physical effects under ionizing radiation and positive applied voltage to the gate are illustrated in Figure 1.7, and the degradation of these physical effects on the V_{th} is illustrated in Figure 1.8. This physical mechanism is developed for the MOS-based transistor having SiO_2 gate dielectric. The gate dielectric layer is known to be the most sensitive part of the MOS-based devices. The usability of the MOS-based devices in a radiation environment as a radiation sensor is determined by the responses of dielectric layers. When radiation passes through the dielectric layer, a large number of electron-hole pairs are generated depending on radiation energy and interaction mechanism. Holes are almost immobile compared to electrons, and electrons are easily swept out from the gate electrode in few picoseconds after generation by irradiation as seen in the first steps of Figure 2.7. However, a large amount of the generated electron-hole pairs recombine with each other in a picosecond. Initial generated electron-hole pairs cause a significant shift

to the V_{th} and are demonstrated in the first step of Figure 2.8. The numbers of holes that escape from initial recombination move closer to the interface between SiO_2/Si where deep traps are located by hopping between the shallow states seen in the second step of Figure 2.8. This mechanism is sensitive to the oxide processing, applied electric field, and ambient temperature. Typically this movement takes less than 1 second at room temperature. Also, some of the mobile charges can be recombined with electrons during their movement and this causes a short time recovery. The contribution of this short time recovery to the V_{th} can be seen in the second step of Figure 2.8. When the mobile holes approach the semiconductor interface, some fraction of them falls into deep traps, as seen in the third steps of Figure 1.8, where they can be trapped. These trapped holes cause remnant threshold voltage shifts which are illustrated in the third step of Figure 2.8. These trapped holes can be treated by high-temperature annealing. The last physical phoneme is the radiation-induced buildup of interface traps localized at the SiO_2/ Si interface as seen in the fourth step of Figure 2.8. The radiation-generated holes or electrons can be trapped in acceptor or donor-like interface states (45,49,55,59). The accumulation of the trapped charge at the interface also causes the positive or negative shift in V_{th} as seen in the fourth step of Figure 2.8.

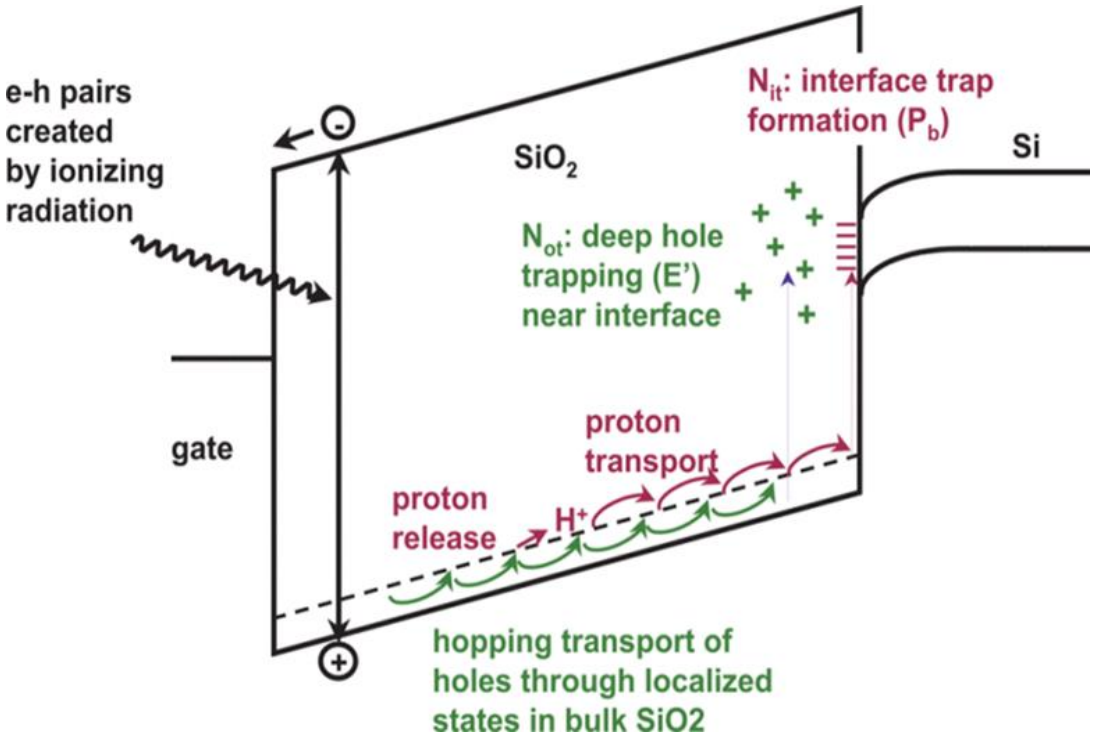


Figure 2.7. Schematic of the physical radiation interaction mechanism (45).

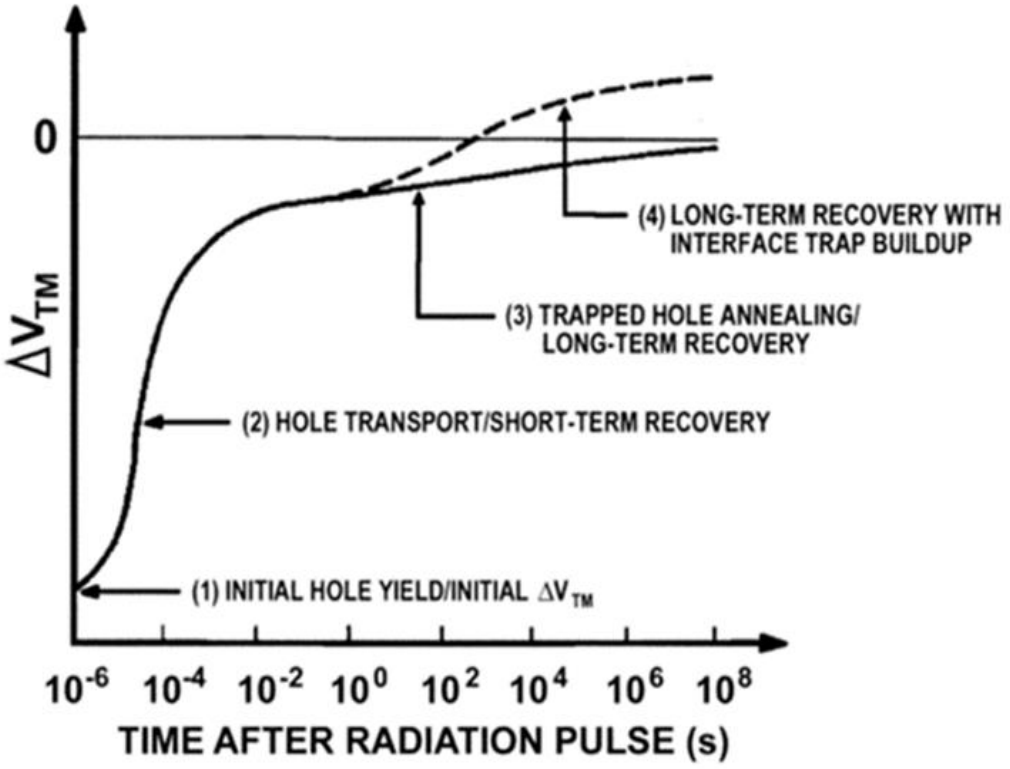


Figure 2.8. Radiation effects on the threshold voltages (115).

2.7.1 Initial Charge Recombination

The initial threshold voltage shift is directly related to the initially generated positive charge yields in the dielectric structure. The magnitude of the initial shift depends on the e-h pair generation energy and field-dependent holes escape from initial recombination. A large number of e-h pairs are created after radiation interaction with the dielectric layer, but this initial density is reduced by initial recombination just before the electrons are swept out from the gate in picoseconds. The number of the final holes yields that cause the V_{th} shift in a long time is proportional to the magnitude of the electric field in the dielectric and initial line density of e-h created by incident radiation. The pair line density can be determined by linear energy transfer (LET) and it is a function of incident particle type and energy but it is inversely proportional to the average separation distance between electron and hole. This means that the close average separation distance of the pair causes more recombination and this decreases the number of final hole yields (82,105,106).

In the germinate model, the separation distance, of isolated single charge pairs is higher than thermalization distance, where e-h pair easily recombine, thanks

to Coulomb interaction. On the other hand, if the average pair separation distance is less than thermalization distance columnar recombination can be observed. Here the e-h pairs lose their identity and recombination occurs between electrons and holes lying track under cylindrical distribution around a track. The recombination probability is much higher than germinate model due to recombination encounters between opposite charges. These two models work successfully depending on the pair separation distance. For instance, low-LET particles, like beta radiation or secondary electron come from Compton scattering, create discontinuous charge pairs in its path, e.g., average separation distance is 50 nm for 1 MeV electron radiation, hence germinate model is valid. On the other hand, for high- LET particles like proton and alpha particles, they create a high density of pair along their path, e.g., the average separation distance is 0.3 nm for 1 MeV proton radiation; henceforth, the columnar model gives more appropriative results. It should be noted that when electron-hole density enhances, columnar model behavior becomes more convenient. It is also important to note that a fraction of positive charge yields is associated with particle source. For example, the yield fraction varied from 90 percent for low- LET particles (12 MeV electron and Co-60 gamma radiation) to 6 percent for the high LET particles (2 MeV alpha radiation) at a constant applied electric field. Hence, different sources may cause variations in the radiation responses of MOS devices (45,46,68).

2.7.2 Charge Transportations

There are two types of charge transport mechanisms. The first transportation mechanism is described as carriers move in shallow trap states in the extended band. The localized states are distributed in the energy range and exhibit large fluctuations in the thermal release rates from trap states; thus, the fluctuations are temperature-dependent. The second transport mechanism is described as hopping transportation whereby carriers move directly between localized trap sites via phonon-assisted tunneling (45). In addition to hopping transportation, the mechanism is temperature dependent, the hopping distance is also important for the hopping holes transport. The transport models are schematically illustrated in Figure 1.9 (5,11,17,22,32,40);

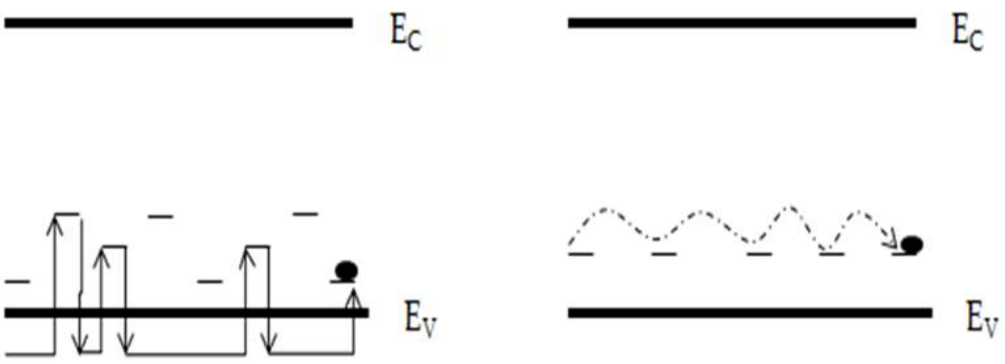


Figure 2.9. Trap modulated charge transportation, and hoping charge transportation between localized states via tunneling.

The small polaron hopping of the holes is given in Figure 2.9, between localized shallow trap states having a random spatial distribution is the more popular holes transport mechanism for the movement of the generated holes toward the interface. The transport of holes in the dielectric layer is responsible for the short time recovery. This recovery effect occurs due to carrier interaction with the surrounding medium, and the movement of holes also carries the lattice distortion with it. The holes transport mechanism and short-time recovery have also the following specifications; Holes movement is dispersive, it may take many decades just after radiation exposure. Any small temperature changes, applied field, dielectric thickness do not cause variations in the recovery curve. These variances only influence the time scale of the curve. The transport is field and strongly temperature-activated. Finally, the holes transport and recovery time have a strong linear power-law dependence on dielectric thickness.

2.7.3 Dose Rate Effects

The changes can be observed in the MOS device parameters with time after radiation exposures. Hence, non-linear dependencies in the total dose accumulated at different dose rates can be observed due to the long-term interface trap build-up and rebound effect. Researchers have reported that the device responses with different dose rates under the same total exposed doses exhibit different sensitivities. They have demonstrated that at a higher dose rate V_{th} shifts to negative, while it was positive at a lower dose rate (96,97,100,102,107,112). These differences are caused by the reduction of the trapped oxide charges at lower dose rates due to tunnel annealing and an increase in the interface trap charges due to the

long-term build-up of interface traps (45,55). At higher dose rates, the presence of an electric field due to generated holes may degrade the electric field of the dielectric layer. These generated charges may cause a reduction in the internal electric field resulting in enhancement of the recombination effect. Hence less radiation damage can be observed compared to low dose rates. As it can be understood, dose rate dependencies can be different for the devices, even in the same device (20,51,80–82,96–112). The parameter variations on the devices should be carefully considered to make an accurate analysis. Understanding the basic charge generation and trapping mechanism under irradiation influence on the dielectric and its interface with the underlying semiconductor is important for device reliability (45–48,54,55).

2.8 Stacked-Field Effects Transistors

Stacked field effects transistor (stacked-NürFETs/RadFETs), is a new design approach, whereby more than one single NürFETs/RadFETs are connected serially on the same chip to increase the radiation sensitivity of the single field effects transistor sensors (15,44,56–58). The main advantage of these stack structures is that the sensitivity of the MOS-based field effects transistor sensor is increased depending on the number of NürFETs in the stacked-NürFETs structure (37). Furthermore, for the radiation sensor to be able to measure exposed radiation dose in the μGy range the sensitive gate dielectric layer thickness should have to be thicker than 1 μm. As explained in the previous discussions, the improvement of the sensitivity can be achieved to some extent using a thicker gate dielectric layer. However, it is also clearly observed that thicker oxide layers alone cannot solve the problem. The usage of stacked-NürFETs instead of a thicker dielectric gate layer will be a solution to the tunneling effects caused by thicker gate oxides. Using a stack structure will keep the same capacitance and decreases the leakage current (1,37,44,57,58). To reveal the advantages and disadvantages of the stacked-NürFETs, the output voltages of the NürFETs should be examined. Figure 2.10 shows the reader circuit diagram of pMOS dosimeters; pMOS reader circuits for (a) a single NürFETs and (b) stacked-NürFETs (7,9,22,53,116).

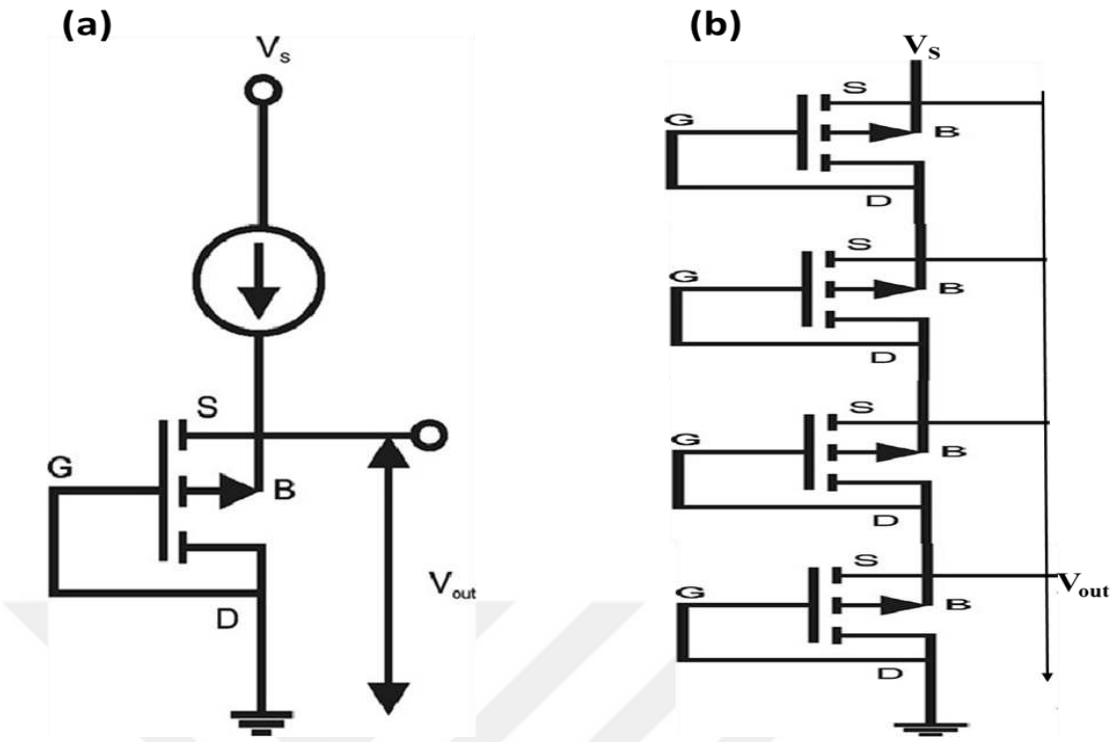


Figure 2.10. pMOS reader circuits for (a) a single NürFETs and (b) stacked-NürFETs.

As seen in Figure 2.10, the gate and drain electrodes of NürFETs are grounded. So the output voltage is expressed as:

$$V_{out} = V_{gs} = V_{Dsat} + V_{th} \tag{2.21}$$

Where V_{Dsat} is the value at which the voltage between source and drain reaches saturation as a result of feeding the circuit with a current source. Therefore, it can be concluded that the output voltage is dependent on the threshold voltage and this value affects the dose reading range of the radiation sensors. The threshold voltage can be determined from a specific current, which is between 5 to 100 microampere (5 µA – 100 µA). In this study, 10 µA constant current was used to determine the initial threshold voltage. To determine the threshold voltage, the NürFET reader circuit is fed by delivering a constant drain current (I_{DS}) at the saturation point. The drain current is expressed as follows:

$$I_{DSat} = -\frac{W}{L}\mu C_{ox}\frac{(V_o - V_{th})^2}{2(1+\delta)} \tag{2.22}$$

Here *W/L*, is the width per length of the NürFET, μ is mobility, C_{ox} is oxide capacitance, $V_o = V_{GS}$ is the reader circuit output voltage as given below:

$$\delta = \frac{\gamma}{2\sqrt{-V_{DS}-\emptyset_B}} \tag{2.23}$$

Where V_{DS} is the drain-source voltage, $\emptyset_B$ is the bulk potential:

$$\emptyset_B = \frac{2kT}{q} ln \frac{N_{SUB}}{n_i} + \frac{6kT}{q}, \gamma = \frac{\sqrt{2\varepsilon_s q N_{SUB}}}{C_{ox}} \tag{2.24}$$

Therefore, the output voltage of a single NürFET is expressed as:

$$V_o = V_{th} + \sqrt{\frac{-2I_{DS}(1+\delta)}{\mu C_{ox}\frac{W}{L}}} \tag{2.25}$$

The change that will occur as a result of irradiation of NürFET reflects the shift in the threshold voltage. The most frequently used method in the literature to determine the threshold voltage is to read the output voltage (V_{out}) by applying a current of 10 µA to the circuit. This value is accepted as the threshold voltage (V_{th}). However, irradiation reduces the mobility of NürFET. This indicates that the change in the output voltage of the reader circuit will be greater than the change in the threshold voltage. The reason for this is the current dependence as expressed in Equation 2.25. The bulk NürFET approach to be fed with a current source at the saturation point is important for the development of dosimeters with higher radiation sensitivity. Thus, the change in output voltage will be higher as a result of irradiation and the usage range of the dosimeter will expand. Output voltage to be obtained as a result of feeding four NürFETs with the same characteristics connected to each other with a current source is expressed as:

$$V_o = 4V_{th} + \sqrt{\frac{-2I_{DS}}{\mu C_{ox}\frac{W}{L}}} \left(\sqrt{1+\delta_1} + \sqrt{1+\delta_2} + \sqrt{1+\delta_3} + \sqrt{1+\delta_4}\right) \tag{2.26}$$

δ Parameter changes from one NürFET to another due to its different values. Therefore, for the structure consisting of four NürFETs, the change in output voltages will be at least four times ($4\times\Delta V_o$) more than the value obtained with a single NürFET.

A design of stacked-NürFETs for increased radiation sensitivity was reported in previous studies. Kelleher et al. (1995), reported a study that details developments in the design of stacked-NürFETs for increased radiation sensitivity. Two different gate dielectric layer thickness and width/length (W/L) were investigated. For the first category; the gate dielectric thickness is 50 nm and the W/L is 300/10 µm and the second category; the gate dielectric layer thickness is 800 nm and W/L is 300/50 µm. The stacked-RadFETs were fabricated by connected 3 RadFETs on one chip with 50 nm and 800 nm gate layer. For 800 nm gate layer stacked-RadFETs, the initial output voltage has exceeded the supply voltage. Because of this, reverse avalanche diffraction occurred in the device conduction of the 3rd stacked-RadFETs. The obtained results are as follows: The pre-irradiation initial threshold voltage for single RadFETs was found to be 16.83 V and obtained output voltage after irradiation is 27.26 V. The observed shifts ΔV is 10.53 V. For the stack structure, the initials output voltage before irradiation is 50.45 V. The measured output voltage after irradiation is 84.37 V, and the shift in the threshold voltage is 33.9 V. The result indicated that the value of stacked-RadFETs is 3.2 times higher than obtained the single structure value. It is observed in the study that the sensitivity of the single RadFET increases with the stack structure. However, a suitable structure for personal dosimetry and medical applications was not found in this study (44).

O'Connell et al. (1996), reported a study that details improvements in the design of stacked-RadFETs using 40 RadFETs, and the radiation sensitivity of the dosimeter was examined. The radiation sensitivity of the sensor is 220 times higher than a single RadFET. To use this structure in medical applications and personnel dosimetry, the device must be optimized. O'Connell et al. (1996), reported the minimum dose value was obtained as < 250 µGy with a voltage of 5 V applied to the system during irradiation with radiation, and < 100 µGy with a voltage of 10 V. To increase the efficiency of these devices, especially for their possible usage in radiotherapy units, it is necessary to improve their sensitivity. Therefore, the design of the sensor in the stacked structure, in other words, the use of more than one interconnected sensor in one chip, may result in improving the sensitivity of the single field effects transistor sensors (57,58).

3. AIM AND SCOPE OF THE STUDY

This study aims to fabricate and characterize the stacked Nuclear Radiation Field Effect Transistors (stacked-NürFETs) that will be used in all ionizing radiation environments such as military, nuclear industry, space, and medical applications. Highly sensitive stacked-NürFETs can be fabricated along with the study of different fabrication parameters such as gate dielectric materials. Furthermore, the fabrication parameters can be comprehensively investigated and analyzed. Two different stacked-NürFETs sensors are being fabricated with 100 nm SiO_2 and 100 nm Er_2O_3 gate dielectric layers. The p-channel MOSFETs optimized to be radiation-sensitive are called RadFET / NurFET / pMOS dosimeters. The sensor gate oxide layer of these transistor-shaped sensors produced on n-type Si substrate is made of dielectric materials, such as SiO_2 and Er_2O_3 to their excellent interface quality with silicon. On both sides of the gate oxide layer, there are p – channels that are formed by boron doping. With the negative stress applied to the metal contact (gate electrode) on the gate oxide layer, the minority charge carriers begin to advance into the channel region. If enough negative voltage is applied to the gate electrode above the threshold voltage, a current will flow through the channel bring about current conduction in the transistor.

Analyzing the electrical characterizations of the fabricated stacked-NürFETs before and after irradiation is also one of the main purposes of this work. The interaction of ionizing radiation with the oxide layer results in electron-decoupled pairs in the device. Negative charges with higher mobility compared to positive charges easily move to metal contacts, avoiding the recombination or trapping process. In contrast, most of the positive charges are trapped in the defect centers in the structure, usually in the centers known as the oxygen gap. This causes the threshold voltage to shift to larger negative voltage values. The magnitude of the change in threshold voltage is proportional to the applied radiation dose. Charge traps occur in the oxide layer, bring about oxide trap charges, in regions very close to the interface are also called boundary traps, and at the interface, we have interface trap charges.

Stacked-NürFETs sensors can measure absorbed radiation instantly to given radiation doses. Stacked-NürFETs are MOSFETs with a gate oxide optimized for radiation sensitivity. By simple measurement of the change of threshold voltage V_{th}, the user gets information on the radiation dose. They may operate compatibly with microprocessors. Therefore, the read-out systems of stacked-NürFETs are simple and the absorbed doses can be measured directly as an electrical signal without any signal converter.

The radiation responses of the stacked-NürFETs sensors deviate from the linearity due to the increased electric field shielding effect after a certain dose value, depending on the sensory region thickness, type, and energy of the radiation. Today, RadFETs which can detect the minimum dose range of 50 mGy are commercially available, but the sensitivity is low. The boron implantation applied to the channel region to bring the threshold voltage closer to zero has also improved the sensitivity of the sensor to some extent as new trapping centers are formed in the structure. Nevertheless, it is important to improve the sensitivity of these sensors to lower doses to increase their effectiveness in medical applications such as radiotherapy. There are two methods to improve the sensitivity of NürFETs to low doses: i) Alternative dielectric may be used instead of SiO_2 used as sensory material, ii) By increasing the number of sensors in the chip, stacked-structure (Stacked-NürFETs), which is the preeminent way. The prospect of radiation interfering with the structure can be increased.

3.1 Outline of the Thesis

This section presents a brief outline of the thesis scheme. Chapters 1 and 2 clarify the introduction and overview that outline the structure of the thesis, which prepares readers for the structure of the study. Chapter 3 briefs the aim and scope of the study. Chapters 4 and 5 provide a background of the study which discusses the fundamentals of semiconductor devices and technologies. Chapter 6 provides the experimental details of the study which covers an overview of high vacuum growth of different dielectric oxides layers, fabrications, and characterizations for MOS device and MOS-based transistors. Chapters 7 and 8 outline the results and discussions of the study which covers the characterizations of the fabricated stacked Nuclear Radiation Field Effects Transistors (Stacked-NürFETs) and the use of the outcomes of the characterizations in the MOS-based radiation sensors/detectors.

4. SEMICONDUCTOR DEVICES

For over one and half centuries, semiconductor devices have been studied. Up to now, there are over 20 most commonly used semiconductor devices, with more than hundreds of distinctions related to them. These semiconductor devices are fabricated from device building blocks as given in Figure 4.1 (55,66).

Figure 4.1a presents the semiconductor-metal interface that intimate contact between a semiconductor and a metal. The first-ever semiconductor device studied was this building block. The top metal is used as a rectifying contact, which allows electric current to flow in one direction easily, and also is used as an ohmic contact (bulk electrode); in this case, the device does not block any current passage, therefore, a current passes through the device in both directions without a significant voltage drop (55,66).

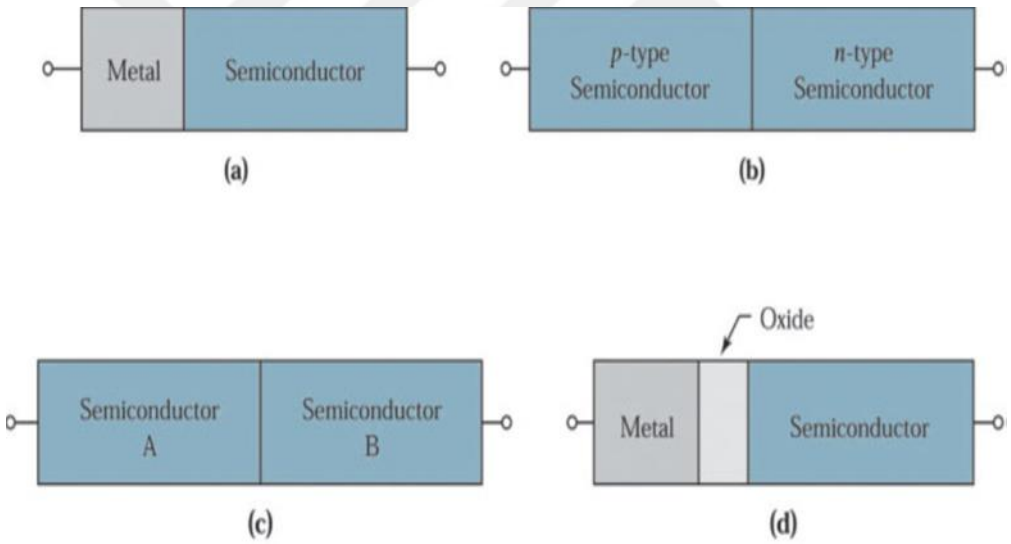


Figure 4.1. Device building blocks. (a) Semiconductor – Metal; (b) p-type – n-type Semiconductor Junction; (c) Semiconductor-Semiconductor Junction Hetero-Junction Interface; and (d) Metal Oxide Semiconductor Structure (55).

The second building block given in Figure 4.1b is the formation of an *n*-type semiconductor (negatively charged carriers) and *p*-type semiconductor (positively charged carriers), which is called a *p*-type – *n*-type semiconductor junction. These devices are the fundamental building blocks for some major semiconductor devices such as bipolar transistors (*p*-type – *n*-type – *p*-type) and thyristor (*p*-type – *n*-type – *p*-type – *n*-type) (45,49,55).

Figure 4.1c presents a building block that is formed between two different semiconductors, which formed a heterojunction interface. This building block is mostly used for the formation of photonic and high-speed devices.

Figure 4.1d illustrates the metal oxide semiconductor structure. This semiconductor device structure is the integration of two interfaces: A Semiconductor – Oxide interface and an Oxide – Metal interface. By adding two p – n junctions to the Metal Oxide Semiconductor (MOS) structure as the drain and source, we can obtain MOS field-effect transistors (MOSFETs), which are the most significant devices for advanced integrated circuits. Semiconductor devices are widely applicable in digital circuits such as microprocessors and transistors. And one of the advantages of semiconductor devices is no power is needed to excite them to bring about the electron's emission (55).

4.1 MOS Devices

Metal Oxide Semiconductor (MOS) is the fundamental of most used Micro-Nano electronic devices in our modern time. Examples of these devices are digital logic circuits, modern microprocessors, radiation detectors, radiation sensors, and storage memories. MOS diodes or capacitors are the main structures that integrated the most semiconductor device surfaces. These MOS devices are used as storage capacitors in integrated circuits and they are also the formation of the fundamental of the charge-coupled devices' building blocks. Moreover, MOSFETs are simply MOS devices with additional n-type – p-tape junctions, which act as source and drain as n-channel MOSFET and p-channel MOSFETs (70,71,73–75).

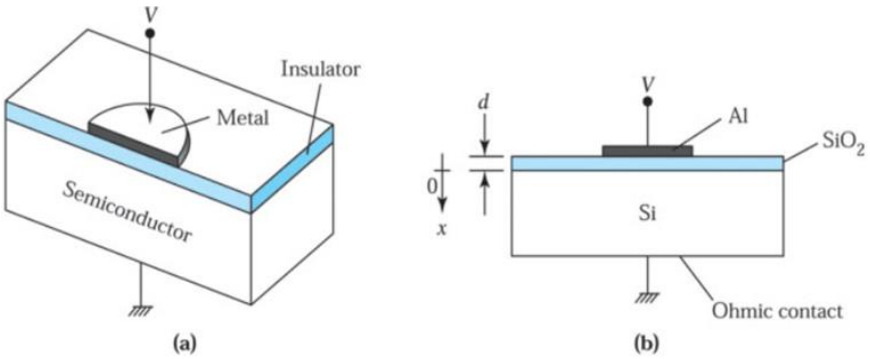


Figure 4.2. (a) Point View of Metal Oxide Semiconductor devices. (a) Cross-Section View of MOS devices (66).

Figure 4.2 illustrates the viewpoint of Metal-Insulator Semiconductor and the cross-section view of the MOS diodes and capacitors. As given in figure 3.2 V is the applied voltage to the metal contact gate and *d* is the thickness of the dielectric oxide. Furthermore, the applied gate voltage is positive when the metal contact gate is positively biased under the bulk contact (ohmic contact) and also the applied gate voltage is negative when the metal gate contact is negatively biased under the ohmic contact (117–120).

Figure 4.3 describes the energy-band diagram of a p-type semiconductor (silicon) MOS device with no applied gate voltage (V = 0), which is called the ideal MOS device. The energy differences between the Vacuum level and the Fermi level (E_F) is the work function of the device; ($q_{\phi m}$ is the work function of the metal and $q_{\phi s}$ is the work function of the silicon). The illustrated $q\chi$ is the electron affinity that is the gap between the Vacuum level and conduction band-edge in the semiconductor, $q\chi_i$ presents the electron affinity of the oxide, $q\phi_B$ presents the barrier energy between the oxide and the metal, and the gap between the intrinsic Fermi level E_i and Fermi level E_F is $q\psi_B$.

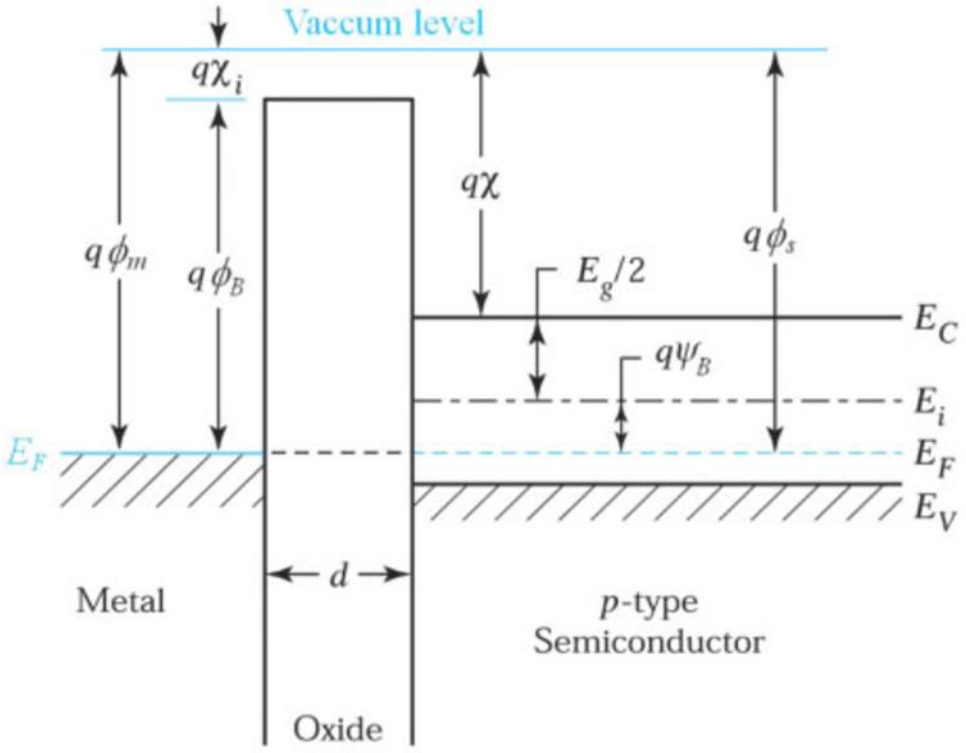


Figure 4.3. Band diagram of a MOS device with zero applied gate voltage (55).

An ideal MOS device can be easily described as at zero applied gate voltage (V = 0), there are no energy differences between the semiconductor and the metalwork functions that is the work function difference is zero. The only charges that exist in the MOS device under applied gate voltage conditions are gate metal surface charges and the charges in the semiconductor. Under the direct current condition, there is no transportation of carriers within the dielectric oxide, which is the resistivity of the dielectric oxide is infinite (46,54,55).

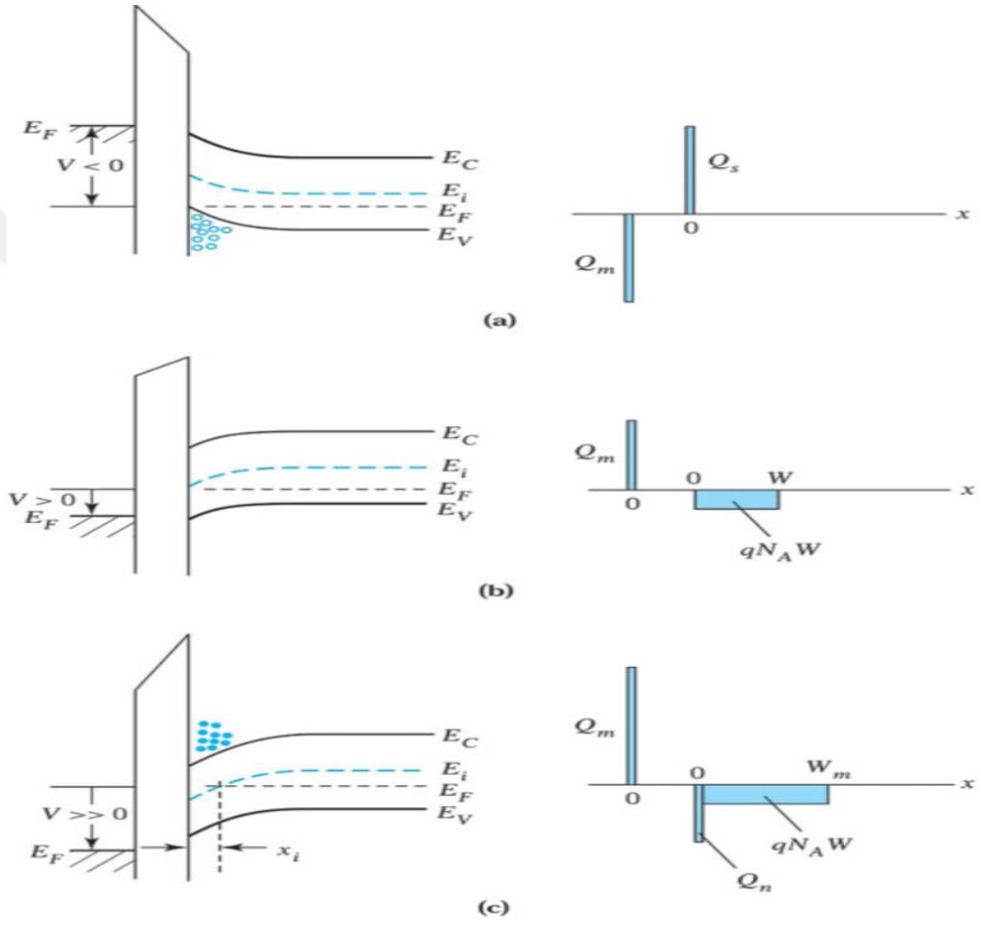


Figure 4.4. Energy band diagrams of a MOS device in three cases; (a) accumulation, (b) depletion, and (c) inversion (55).

An ideal MOS device possesses three characteristics under both two applied voltage conditions (positive and negative voltages). An example for a p-type silicon semiconductor, when a negative potential (V < 0) is applied to the p-MOS device metal gate, extra positive charge carriers (holes) will be generated at the Oxide – Silicon interface. Figure 4.4a illustrated the behavior of the (V < 0) case. In this

case, the bands bent upward, which cause an accumulation of positive charge carriers. This case is called an accumulation mode (46,54,55).

Figure 4.4b describes a case when the applied potential is positive (V > 0), the energy bands here are bent downward and holes are depleted. Due to the depletion of the majority carriers, this case is called the depletion mode. When the applied positive voltage keeps increasing to a larger voltage (V >> 0) the depletion mode switches to the inversion mode as shown in Figure 4.4c (119–121).

4.2 Metal Oxide Semiconductor Field Effects Transistors (MOSFETs)

MOSFETs have several identification names such as Insulating Gate Field Effects Transistors (IG-FETs), Metal Oxide Semiconductor Transistors (MOS-T), and Metal Insulating Semiconductor Field Effects Transistors (MISFETs). A cross-section view of a MOSFET is illustrated in Figure 4.5. This MOS-based device has consisted of four terminals; p-type silicon (semiconductor) substrate in which the source and drain regions are formed. The gate (metal plate) that is formed on the oxide dielectric in another insulator is the third terminal. The fourth terminal is the bulk (ohmic contact) contact to the semiconductor substrate (19,39–41).

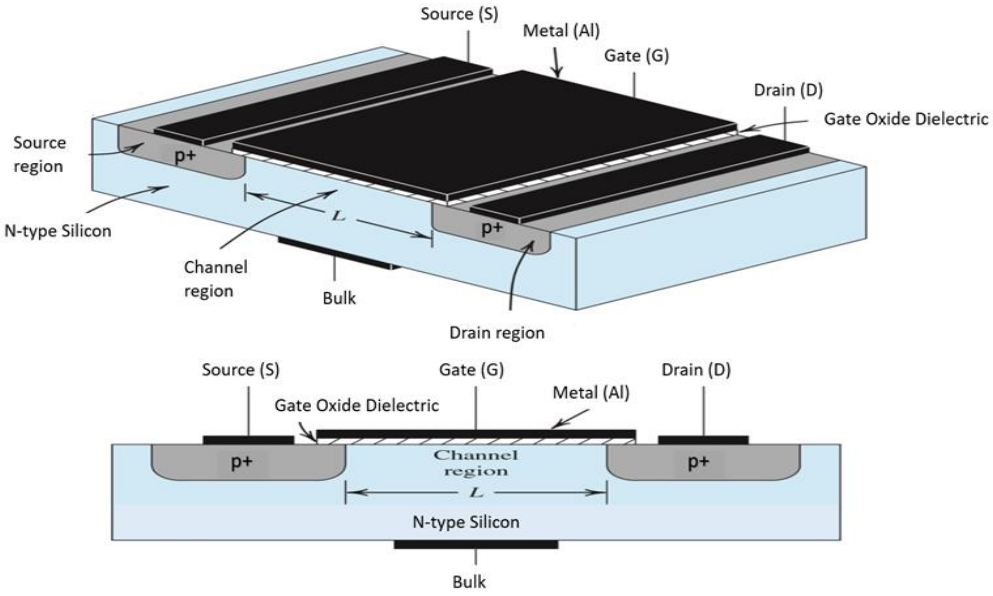


Figure 4.5. Cross-Section View of a Metal Oxide Semiconductor Field-Effects Transistor (MOSFET).

In most of the applications, the source contact is referred to as the referencing voltage. When the device is under the unbiased condition with zero voltage at the gate, there will be no current flow from the source to drain. However, when enough voltage is applied to the gate, the MOS region forms a channel, which is called the inversion layer is generated between two terminals (source and drain). This channel turns into a conducting layer by connecting the source and drain terminals with a large current flow. This behavior can be moderated by applying a gate voltage. The bulk (ohmic contact) can be at the source voltage, the channel conduction is always related to the semiconductor (substrate) potential (55).

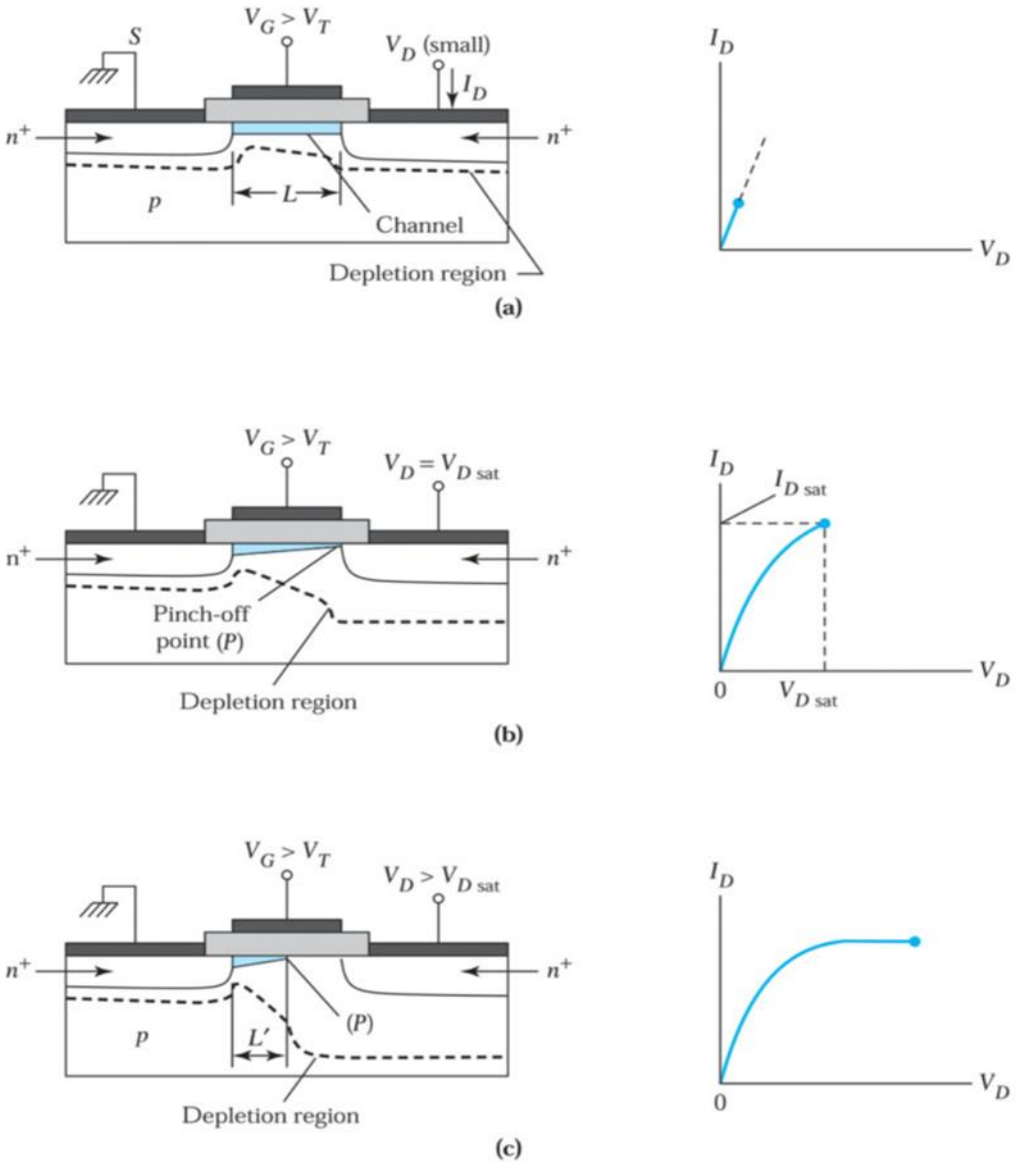


Figure 4.6. Functions and I – V Characteristics of the MOSFETs. (a) Small Drain Voltage. (b) At Saturation ($V_D = V_{D,Sat}$). (c) Over Saturation ($V_D > V_{D,Sat}$) (55).

The linear and saturation regions. When a MOSFET device is biased, which is a voltage is applied to the gate metal, an inversion layer is generated at the top of the silicon as shown in Figure 4.6. If the applied voltage to the drain is low, the direction of the electrons flow will be from the source to drain, while the equivalent current will flow in the opposite direction, which is from the drain to the source. Therefore, the inversion layer behaves like a resistor, and the drain current (I_d) increases with the increasing drain voltage (V_d) and vice versa. This region is called the linear region, as illustrated in figure 4.6a (49,55).

When the drain voltage keeps increasing, it reaches a saturation ($V_{d\ sat}$), at which the channel thickness reduces to zero. In this case, a pinch-off point is observed (Figure 4.6b). The drain current does not change above the pinch – point, it almost remains the same. At this point, $V_d > V_{d\ sat}$, and the $V_{d\ sat}$ remains constant. Therefore, the number of carriers coming from the source and the current flowing between the source and drain remains the same. This case indicates the saturation region as shown in Figure 4.6c. Under this circumstance, the drain current will remain constant no matter how the drain voltage increases. The significant factor is the channel length and the channel width under this condition and it was given in Figure 4.6c (65).

Now that we are familiar with the basic characteristics of the MOSFETs, discussions on the region of the subthreshold will be significant. If the applied gate voltage is less than the threshold voltage, this will cause weak inversion on the silicon surface, the drain current corresponding to this voltage is called the subthreshold current. This region is significant, especially, in low-power devices, such as logic digital switches and storage applications. MOSFET devices can be categorized into four types. The types of these devices depend on the structure of the inversion layer (channel). When the gate is at zero bias, the inversion layer conduction is very low, therefore, to form an n-channel positive voltage must be applied to the gate, and in this case, the device is off (enhancement) n-channel MOSFETs. If this channel exists with zero voltage at the gate, here additional negative voltage is needed to form a depletion in the channel to reduce the conduction, this device is depletion n-channel MOSFETs (45,55,65).

Likewise, there are p-channel normally off and depletion p-channel MOSFETs. A comprehensive description of the device type is illustrated in Figure 4.7 (55);

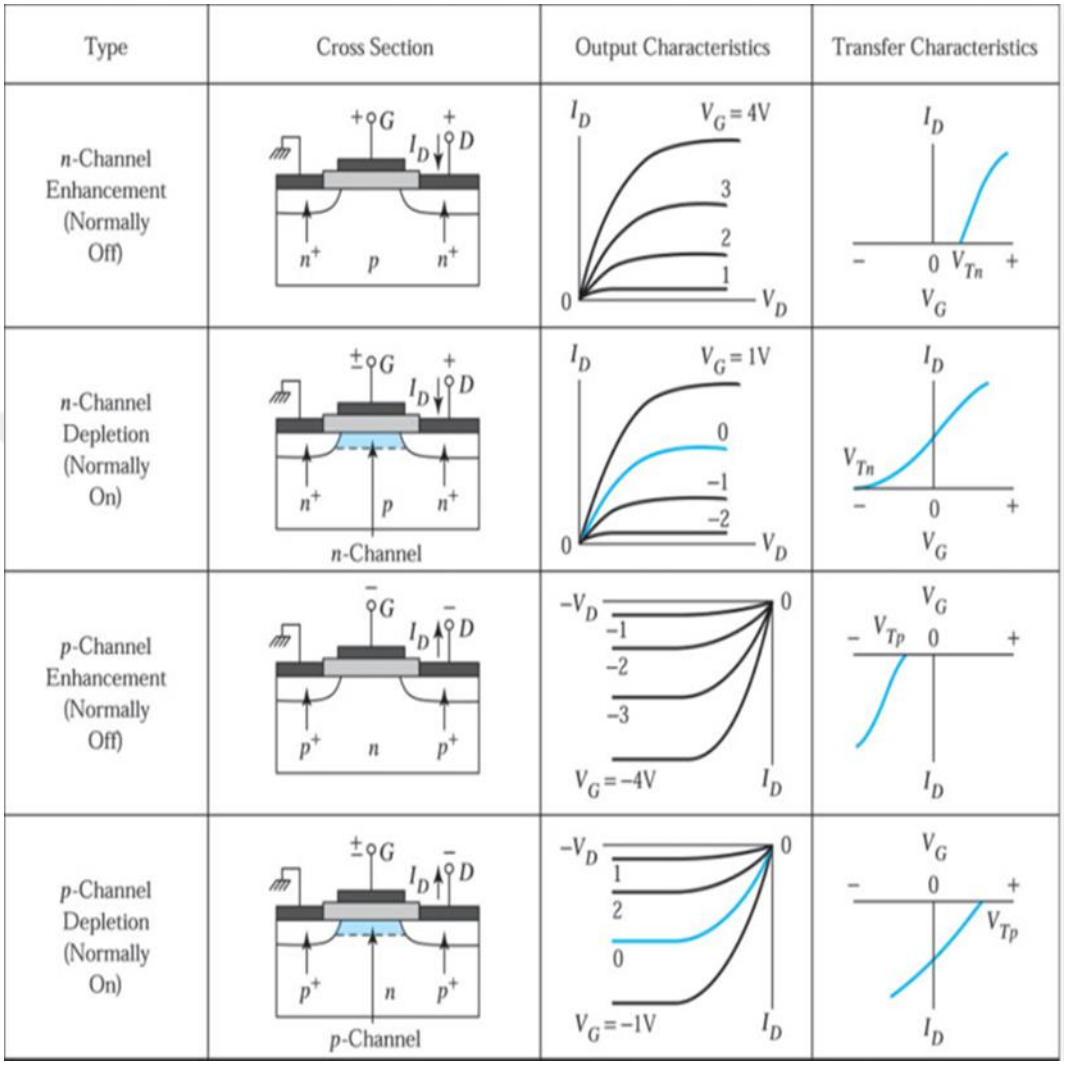


Figure 4.7. Schematic Structures and Electrical Characteristics of four Types of MOSFETs (55).

5. SEMICONDUCTOR TECHNOLOGY

The most common semiconductor technologies were invented over a century ago. Then, they were developed, and also the technologies were invented. Especially, the invention of lithographic photoresist in the nineteenth century was important for lithography in that it established the fundamental pattern transfer procedure for today's semiconductor devices. After this development, innovative invention and integration circuits caused rapid advancement of the microelectronic industries and Dynamic Random-Access Memories and Micro-processors, which make up the most significant and largest sections of the Micro-Nano electronic industries (46,54,55,65).

It can be easily said that silicon and gallium arsenide are the most significant semiconductors for integrated circuits and discrete components such as transistors, diodes, capacitors, resistors, and inductors. In this section, the well-known technologies and techniques for growing and fabricating a single crystal of these semiconductors are discussed. Silicon dioxide is the starting material for silicon (Si) wafer, while gallium (Ga) and arsenic (As) are the starting materials for a gallium arsenide (GaAs) semiconductor wafer (55). These materials are chemically processed to obtain a high purity polycrystalline silicon and gallium arsenide, from this single crystal are formed. Etching and polishing are performed on the wafers to get smooth and specular surfaces for device applications.

5.1 Thin Films Growth

Thin films dielectric oxides are paramount important for discrete devices and integrated circuits. For the fabrication of metal-dielectric semiconductors or in other words MOS based devices, different kinds of dielectric oxide thin films are used (4,8,12,13,24). Advancements in the growth of thin-film technology have made Micro-Nano electronic industries what is it today. These thin films can be categorized into four groups: Thermal oxidation, dielectric layers, polycrystalline-silicon, and metal thin films for rectifying and ohmic contacts. All these four thin-film groups can be used in semiconductor (silicon) n-MOS field effects transistors as shown in Figure 5.1. The gate oxide layer from the thermal oxidation, which under its channel is formed (inversion layer) between the source and drain. Thermal oxidation is used to grow both field oxide and gate oxide. Because thermal oxidation provides high-quality oxides with lower interface traps (2,10,19,26).

Dielectric layers (silicon dioxide and silicon nitride) are used between the gate metal and the semiconductor to prevent impurities and passivation. Polysilicon is used as a conduction material for multiple level metallization devices, and also is used as a contact material for inter-junction devices. Metal thin films such as gold, copper, and silicide are used as gate electrodes, bulk (ohmic contacts), and low resistance inter-connections (45,55).

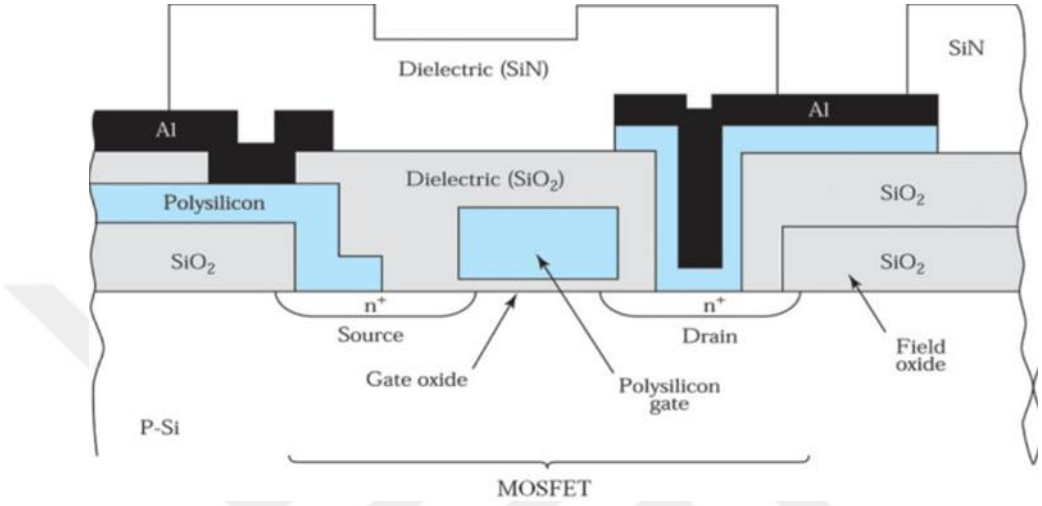


Figure 5.1. Schematic Structure of n-Channel MOS Field Effects Transistor (n-MOSFET) (55).

5.1.1 Thermal Oxidation

Thermal oxidation is one of the well-known and commonly used methods to oxidized semiconductors. Because thermal oxidation is the most significant for silicon-based devices (55).

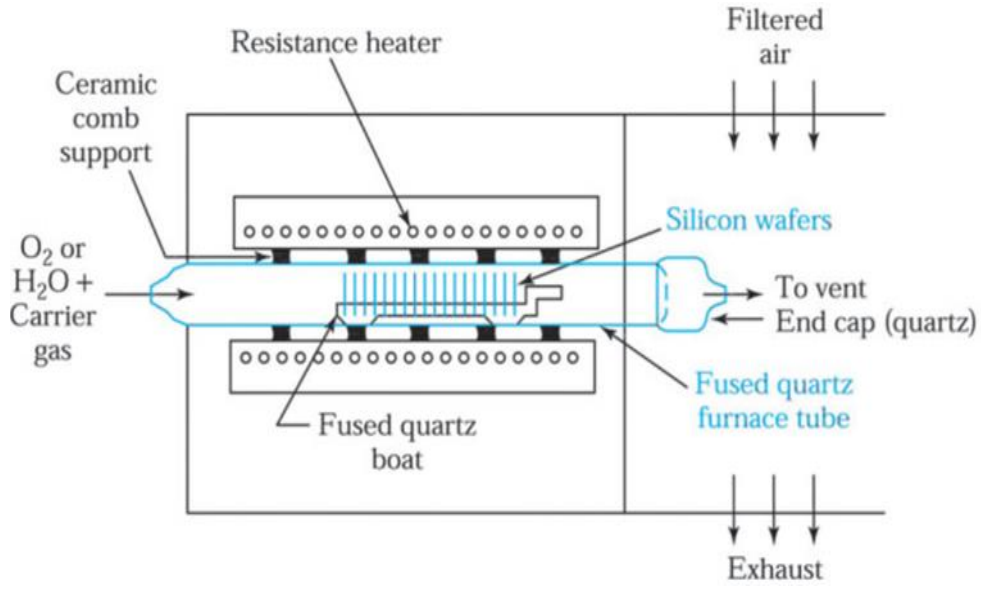


Figure 5.2. Schematic Structure of Oxidation Furnace (55).

The operational steps of thermal oxidation are illustrated in Figure 5.2. The system contains a heat resistance furnace, a fused quartz cylindrical tube, a quartz boat, a source of gases, and a source of distilled water vapor (45,55,65). The thermal oxidation system can resist up to 2000 °C. Gases flow regulations in the system are done by micro-processors. The following equations describe the chemical reactions of dry and wet oxidation:

$$Si_{(s)} + O_{2(g)} \rightarrow SiO_2 \quad (5.1)$$

$$Si_{(s)} + 2H_2O_{(g)} \rightarrow SiO_{2(s)} + 2H_{2(g)} \quad (5.2)$$

During the oxidation process, the interface of Si/SiO_2 moves into the Silicon, which creates a new interface layer due to the surface contamination on the silicon wafer that is an oxide layer (55).

5.1.2 Chemical Vapor Growth of Dielectrics

Dielectric oxides thin films are used essentially for insulating layers and passivation of semiconductor devices and integrated circuits. Some parameters such as the growth processing substrate temperature, growth rate, uniformity of the films, electrical characteristics, and the chemical properties of the dielectrics, need to be taken into consideration before deposition of the films (49,55).

Chemical vapor growth is the widely used technique for the growth of the film in semiconductor device processing. Chemical vapor growth is used to grow polysilicon for gate contact, silicon nitride dielectric oxides, emerging dielectrics oxide, and many more. The most used chemical vapor growth methods are atmospheric pressure chemical vapor growth, low-pressure chemical vapor growth, and plasma-enhanced chemical vapor growth.

The system of the atmospheric pressure chemical vapor growth is similar to the thermal oxidation system as described in Figure 5.2; the only difference is the addition of gases. Low-pressure chemical vapor growth is a system that operates at sub-atmospheric pressure. When the pressure is reduced the unwanted gas phase decreased, in this case, the uniformity of the films improves. However, the growth is very low, due to the low pressure. Plasma-enhanced chemical vapor growth is an energy-added chemical vapor growth system. In this method, additional plasma energy is added to the conventional chemical vapor growth, which causes plasma discharge between the electrodes (55,66).

Chemical vapor growth is the process by which solid thin films are formed on the target substrate by the chemical reactions in the system. Reactants are sent

into the system with the species gas, which activates and disconnects by plasma. From these chemical reactions, reactive agents are adsorbed onto the substrate, through this solid thin films are formed on the substrate (5,10,39).

5.1.3 Physical Vapor Growth

The main applications of the physical vapor growth in semiconductor technology are the growth of metals and compounds such as aluminum, titanium, copper, titanium nitride, and tantalum nitride, which are used to connect devices and junctions on the semiconductor substrate. However, this technique is also good for dielectric oxide growth. Metal evaporation, electron beam evaporation, plasma spray growth, and sputtering are the most widely used physical vapor growth methods. When the source material is heated to a very high temperature, which is above the melting temperature of the material, the source material evaporates. The evaporated material travels to the target materials in the form of atoms. Evaporation and electron beam evaporation are widely used due to their high growth rate and the compatibility to grow high-temperature materials (54,55).

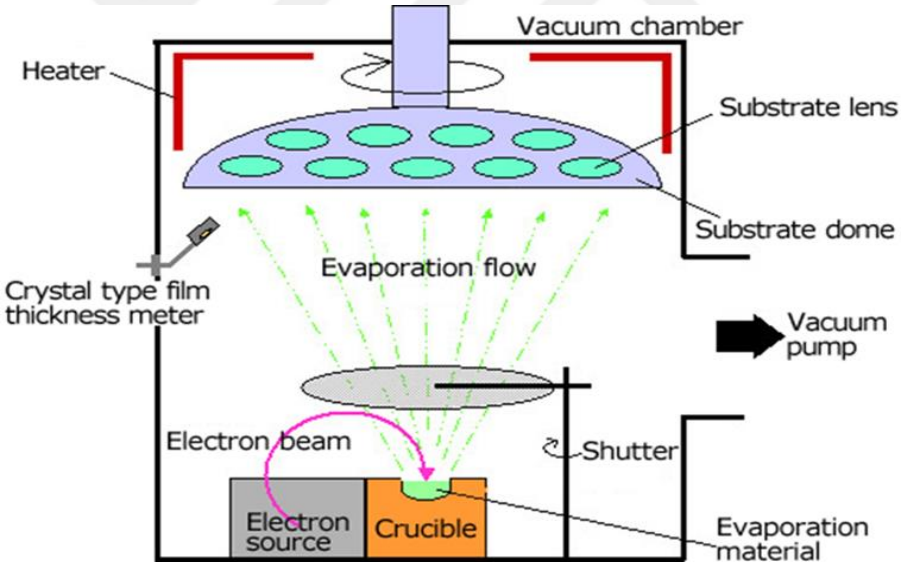


Figure 5.3. Electron Beam Evaporation System (65).

Electron beam evaporation is a technique by which a generated electron beam from the filament that is driven via electric and magnetic fields is ejected to strike the source material and evaporates it. During this process, the source material is heated up to its evaporation point, which causes atoms to leave the source surface to the target substrate. The processing mechanism of the electron beam evaporation is illustrated in Figure 5.3.

Sputtering is the transportation of materials from a target to the desired substrate. This process is achieved by bombarding the material target surface with ions gas, especially argon gas, however, gases such as oxygen and nitrogen are occasionally used. This deposition technology is gas generated plasma technique; the generated plasma is confined to a region containing the target materials to be grown. Particles in the form of atoms from the target material are ejected as the results of high-energy ions within the plasma to a substrate to obtain a thin film (55).

Direct Current (DC) and Radio Frequency (RF) sputtering are the main two types of sputtering systems. The DC sputtering is generally used to grow metal films. The RF sputtering is more commonly used than the DC sputtering, because is suitable for both conductive (metals) and nonconductive (dielectrics) materials, but is generally used for growing dielectrics. The advantage of this system is that it does not require the source materials to melt or evaporate, almost all materials can be grown regardless of their melting points (80,82,100,102,103).

5.1.4 Atomic Layer Deposition (ALD)

Atomic Layer Deposition is one of the significant chemical vapor deposition technology that can grow monolayer order ultra-thin dielectric oxide films. The atomic layer deposition technique is generally used to grow films thinner than 100 nm thickness due to its conformal growth structure. Because of this ALD becomes an important technology for Nano-devices fabrications (46,55,65,68).

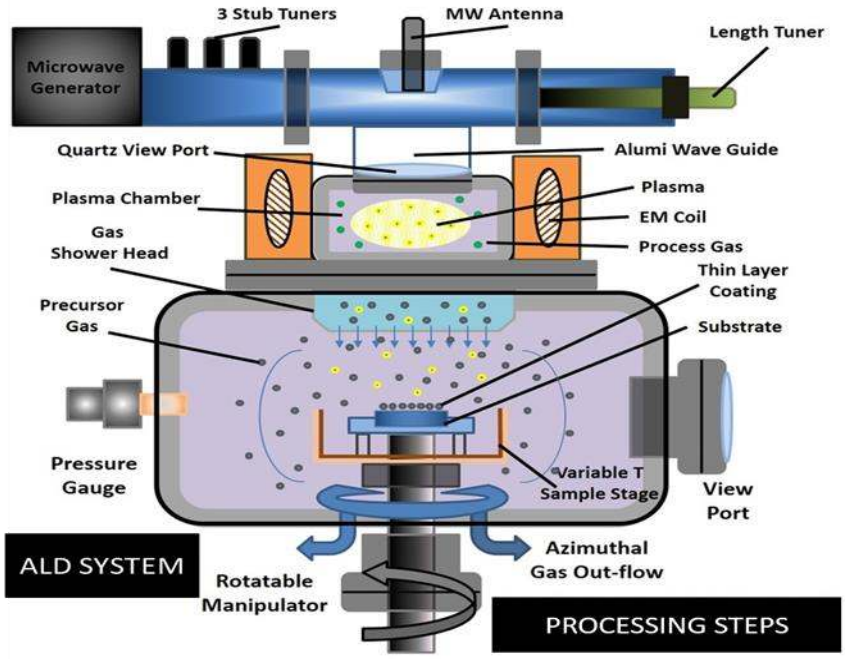


Figure 5.4. Schematic Structure of Atomic Layer Deposition Technique (59).

ALD system processing is different from conventional chemical vapor deposition, which processes chemical reactant supplies that are in the system. In the ALD system processing, serial exposures of chemical reaction agents that have the self-limitation time of deposition are used. In conventional chemical vapor deposition, chemical reactions take place within the gases phase or on the sample substrate, while in atomic layer deposition, these reactions take place on the sample substrate alone, which prevents gas-phase reactions. Processing steps of the atomic layer deposition system are illustrated in Figure 5.4. The cycle time that is the sum of exposures and the periods of removal, is the parameter, which determines the thickness of the films. This allows us to control the thickness and the accuracy is high (49,55).

5.2 Lithography

Lithography is the processing system that transfers patterns of different geometries on a mask to a thin layer resist (radiation-sensitive material), which is used to cover the surface semiconductors such as silicon wafers. These patterns are used to define the terminals and regions in integrated circuits. Semiconductor devises integration requires various terminals, which make them the backbone of our today's Micro-Nano electronics industries. The invention and development of lithography technology made this sophisticated device fabrication easier. The pattern transfer is achieved with the help of etching processes, which remove the unmasked regions selectively (55).

The environment is the most important basis of the lithography process, all steps must be performed in an ultra-clean environment, which is the cleanroom. To avoid contaminations and impurities, which affect semiconductor devices' performance and reliability, clean processing rooms are required. For example, the presence of dust particles on a silicon wafer surface can easily disrupt the formation of any single-crystal films by forming dislocations (4,5,12,96). The existence of dust particles in the gate oxide layer improved conductivity and causes voltage breakdown. This creates more damages in the lithography process. Because, presence of dust particles on a photomask, destroy the circuit patterns, by creating additional patterns on the mask. Lithography processing is given in Fig. 5.5;

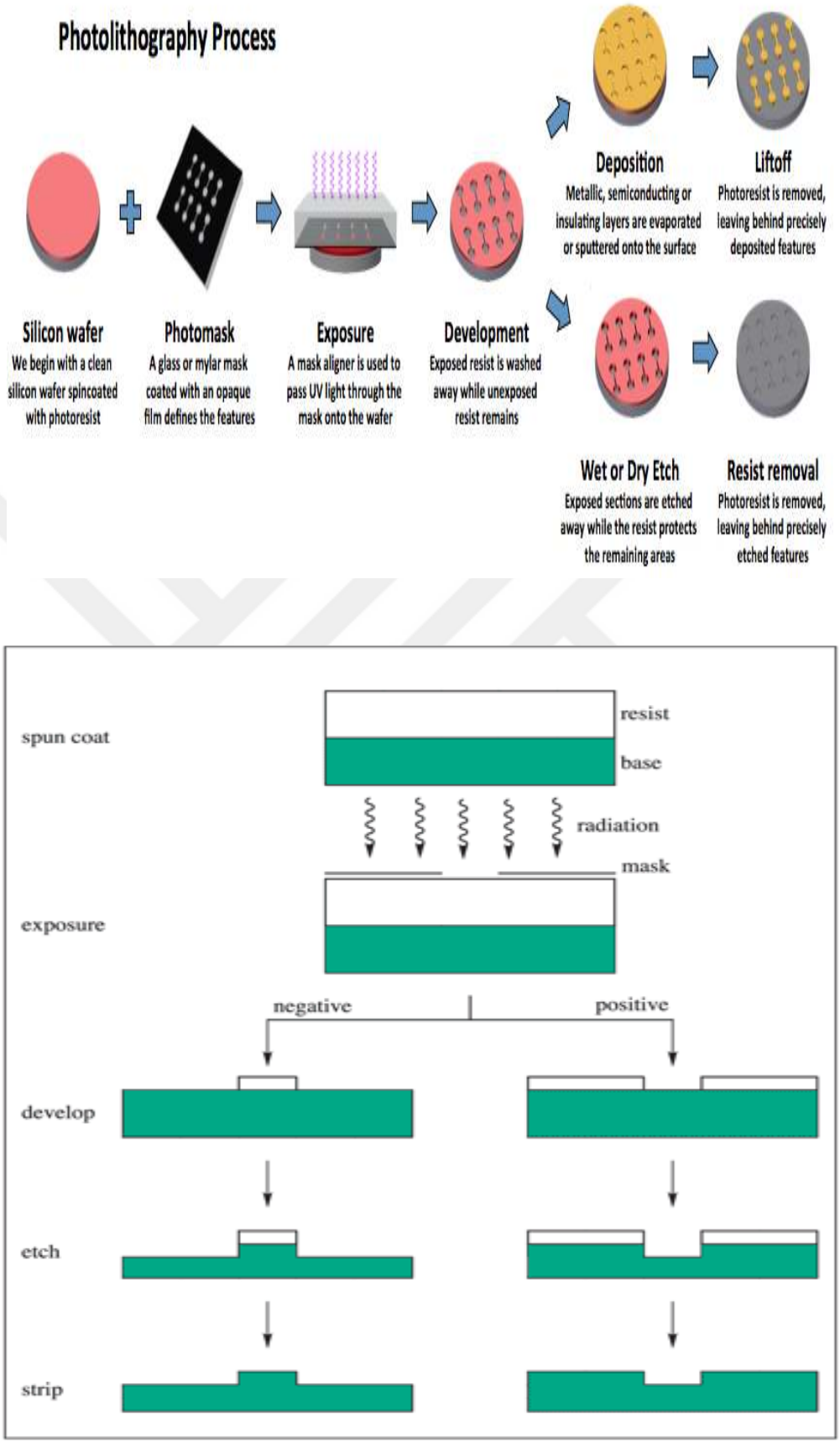


Figure 5.5. Lithography Process for Negative and Positive Photoresist (46).

5.3 Integrated Circuits

Microprocessors, photonic devices, sensors, detectors, and power application discrete devices. Almost all electronic devices are built on integrated circuits. Integration is the ensemble of transistors, which are active devices and resistors, capacitors, and inductors, which are passive devices within and on the single crystalline semiconductor substrate and interconnect them using a metallization process. Integrated circuits have many advantages over discrete devices such as reduction of interconnection parasites by metallization connections and the ability to use the whole semiconductor wafer, which reduces the production cost (45,49,65).

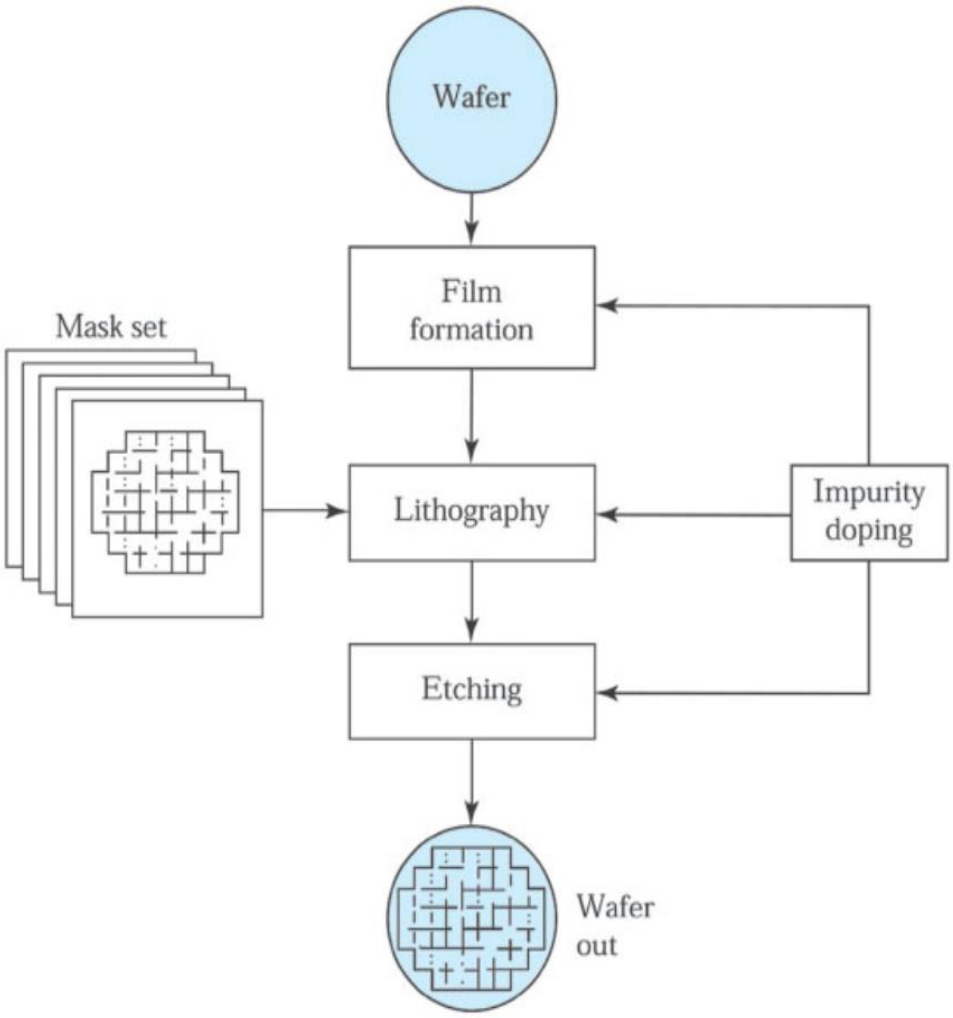


Figure 5.6. Schematic diagram of Integrated Circuits Fabrication (55).

The most common key devices of the integrated circuits are field effects transistors, particular systems are developed to improve their performance. Metal oxide semiconductor field effects transistors, bipolar transistors, and metal-semiconductor field effects transistors are the three major devices associated with

the integrated circuits technologies. Figure 5.6 describes mutual relations between the major processing steps used for integrated device fabrications. Polished silicon wafers with a desired resistivity and orientation are the starting materials. The formations of film steps consist; field oxides growth, gate dielectrics growth, and metal film formations for drain, source, gate, and bulk contacts. Field oxide formation is always followed by impurity doping for the formation of drain and source regions. Lithography is the heart of the processing, apart from field oxide growth, and every step is interrelated with lithography. Lithography processes are generally followed by etching steps. Each technique has interrelationships with another (45,55,59).

Finally, as illustrated in figure 5.6, integrated circuits are made by transferring each mask pattern in the sequence, step by step, onto the prepared silicon wafers. After every processing step is performed, on each wafer hundreds of identical chips are fabricated. These chips are separated by laser or sawing cutting. Separated chips are electrically tested, followed by packaging for desired electronic applications.

6. MATERIALS AND METHODS

6.1 Processing

The design and production of lithographic masks for the fabrication of the stacked Nuclear Radiation Field Effects Transistors (stacked-NürFETs) are the most important parts of this work. The masks were designed by Prof. Dr. Ercan YILMAZ. Six different masks were designed and produced.

6-inch n-type silicon wafers with 1-10 Ohm-centimeter (Ω-cm) resistivity are the starting materials. Silicon substrate purity has a significant impact on the production and fabrication of microelectronics and Nano electronics devices. The cleaning of the silicon substrates is very important because possible contaminations on the substrates can negatively affect the semiconductor device's performance and reliability. To remove impurities, the n-type silicon wafers were cleaned using the standard Radio Corporation of America (RCA) cleaning process; organic clean, oxide strip and ionic cleaning are the three steps for RCA procedures. The cleaning procedure steps are detailed below:

Organic cleaning: This process is used to remove organic contaminations with ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and deionized water (DI-H_2O) solution. The solution ratio is; 1:1:5 (NH_4OH + H_2O_2 + DI-H_2O), the solution was heated to 60 °C, and the wafers were put into the solution and waited for 10 minutes. Following this process, the wafers were immediately put into distilled water and rinsed for at least 4 cycles (69).

Oxide strip: This process is used to remove natural oxides such as silicon dioxide (SiO_2) from the silicon wafers surface. The author prepared Hydrofluoric acid (HF) and deionized water (DI-H_2O) solution with a ratio of 1:50. For the HF bath, the wafers were put into the solution and waited for 12 seconds, were then rinsed with deionized water for at least 4 cycles.

Ionic cleaning: This process is used to remove ionic contaminations such as sodium ions (Na^+) with hydrochloric acid (HCl), peroxide (H_2O_2), and deionized water (DI-H_2O) solution. The solution ratio is 1:1:6 (HCl + H_2O_2 + DI-H_2O), the solution was heated to 60 ^oC and then the wafers were put into the solution and waited for 10 minutes. Following this process, the wafers were immediately put into distilled water and rinsed for at least 4 cycles. Finally, the cleaned wafers were dried with ultra-pure nitrogen gas (N_2). The entire procedures and processes were

carried out in a cleanroom at NÜRDAM using the semi-automatic wet benches. All operations were handled without touching RCA cleaning process was applied to Si substrates and dried with 8 N purity nitrogen gas (N_2). Then, the cleaned wafers were taken to a vacuum environment quickly. Thus, the possible oxide layer which may occur again on the wafers was prevented.

6.1.1 Field Oxide Growth

The field oxide layer was grown on the RCA cleaning process applied Si wafers by the wet thermal oxidation method (5,12,41). Field oxide layer formation was carried out in a high temperature (1000 °C) diffusion furnace. 1 µm SiO_2 layer was grown on n-type silicon substrates.

Figure 6.1. 1 µm SiO_2 thick grown field oxide layer on the n-type silicon substrate.

6.1.2 Phosphorus Deposition for Bulk Contact

The purpose of this stage was to create a region where the back contact was taken. Firstly, the structures (silicon wafers with grown silicon dioxide Si + SiO_2) were covered with photoresist. Then, the exposed part of the structure covered with the mask was decomposed with UV light as given in Figure 6.2. To separate this part from the structure, the Silicon substrates were put into a developer solution for 50 seconds. Then, with the help of a hydrofluoric acid buffer (BHF) solution, the desired part of the oxide layer was abraded from the structure and the silicon substrates were reached. The photoresist was removed from the structure with the help of a piranha solution (a mixture of 300 ml H_2SO_4 + 100 ml H_2O_2). The schematic and under microscope view of the structure obtained after this process is shown in Figure 6.3.

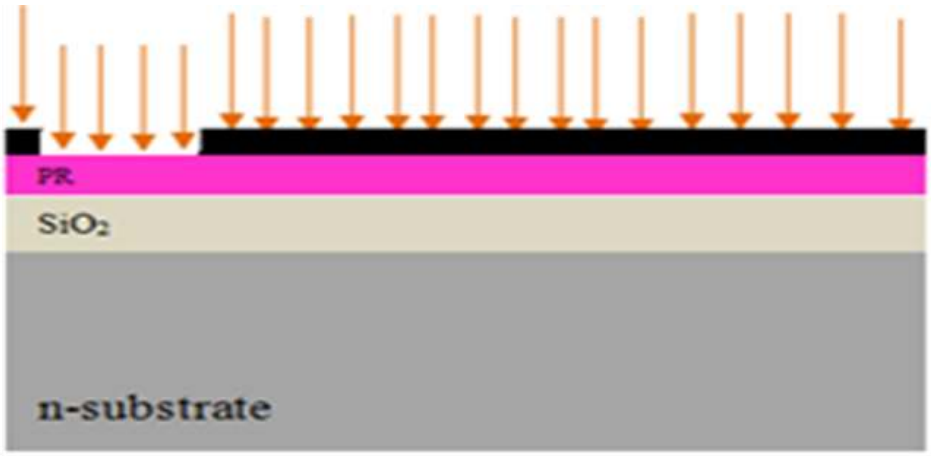


Figure 6.2. First lithography stage for phosphorus doping.

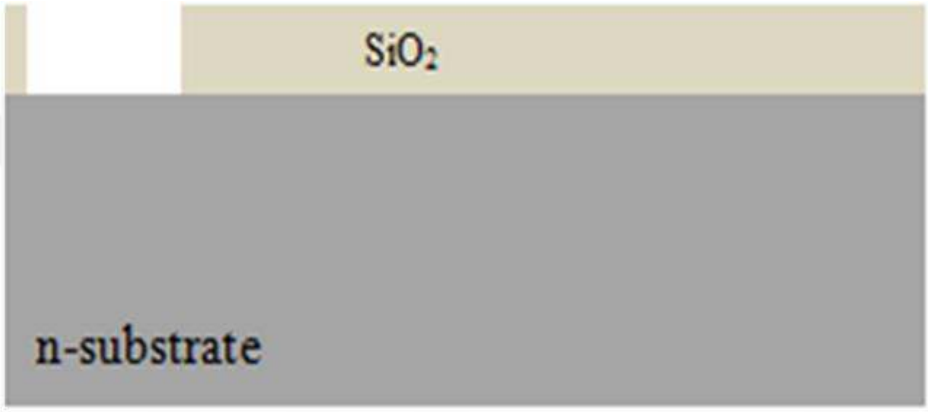


Figure 6.3. First lithography stage for phosphorus doping.

After the lithography process, the phosphorus doping process was performed, the fabrication steps were followed (4,12,24,39,41).

After the phosphorus doping, some oxide layer forms on the structures. To clean this oxide, silicon wafers were leached into an HF solution. Experimental steps were performed and processed for the added phosphorus to penetrate the silicon substrates. Since the electron density on the substrates will increase after phosphorus doping, the surface resistance will decrease. Surface resistance obtained values are in accordance with the expected values, and the surface resistance distribution is given in Figure 6.4. As a result of all these processes, phosphorus doping into Si wafers has been successfully achieved.

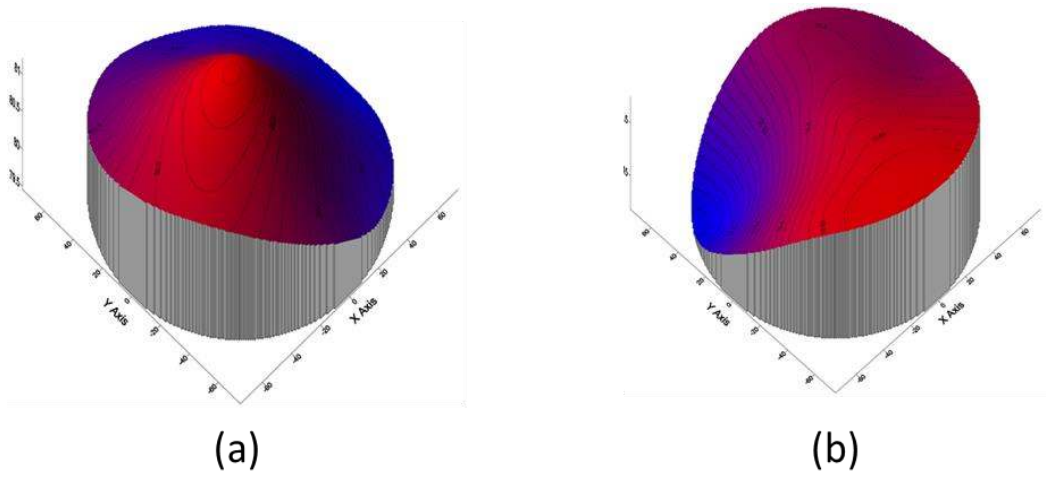


Figure 6.4. Surface resistance distribution a) Before phosphorus doping, b) After phosphorus doping.

6.1.3 Boron Doping for P-Channel

The purpose here is to create p + regions that will provide the current passage in stacked-NürFETs. By putting a mask on the structures covered with photoresist, it is ensured that the desired regions are illuminated with UV light. Figure 6.5 illustrates a schematic view of the process.

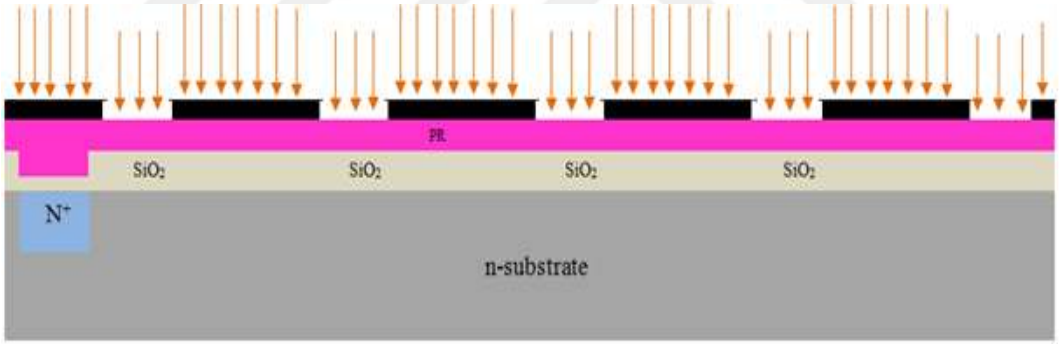


Figure 6.5. Second lithography stage to open regions for the boron doping.

Si substrates were placed in the developer for 50 seconds and the decayed parts (UV exposed parts) were separated from the main structures. Then, the oxide layer was abraded with a BHF solution and Si substrates were reached. The schematic view of the structure reached after this process is shown in Figure 6.6.

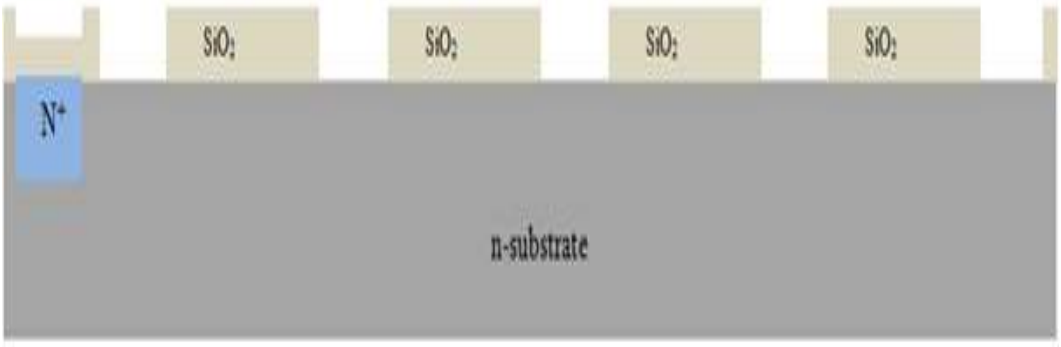


Figure 6.6. The schematic view of the structure reached after the lithography stages.

Boron doping rates significantly affect device performance. Our workgroup used the TCAD simulation program in their previous studies to examine the effect of boron doping on sensor performance and determined the necessary experimental parameters. A part of the structure used in the simulation is seen in Figure 6.7. The experimental steps followed in boron doping are taken from laboratory literature (5,8,12,14).

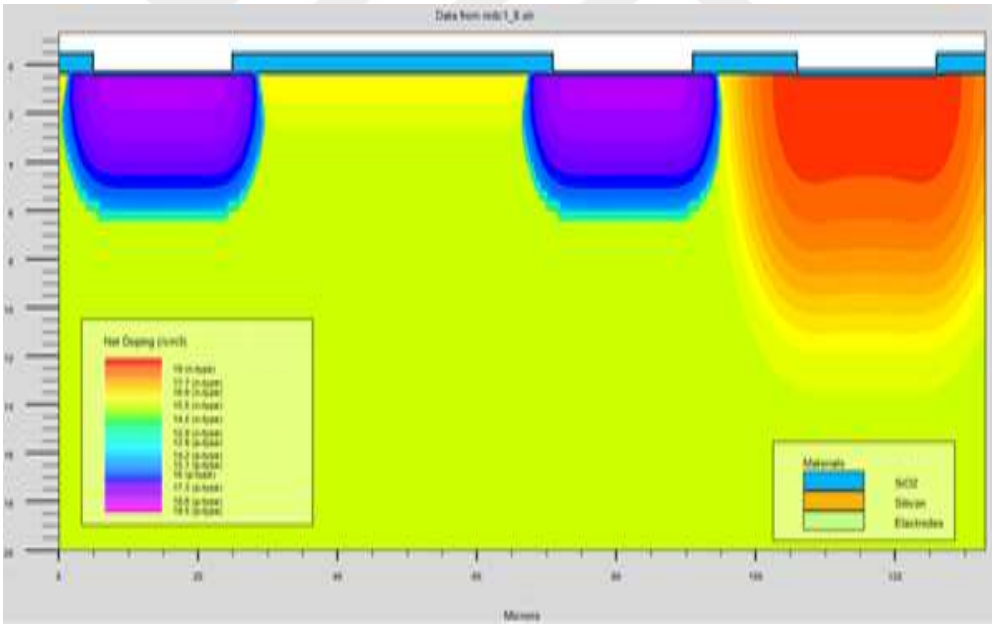


Figure 6.7. View of p + and n + regions in the TCAD simulation program (14).

The experimental steps for the drive-in were performed, for the added boron to penetrate deeper into the Si substrates, like the process performed in phosphorus doping. As a result of boron doping, the surface resistance will increase due to the increase in the density of the holes on the surface. This increase in resistance value was caused by the low mobility of the holes compared to the electrons. Measurements were taken for resistance control and an increase in values was

observed as expected. The schematic view of the structure obtained after this process is given in Figure 6.8.

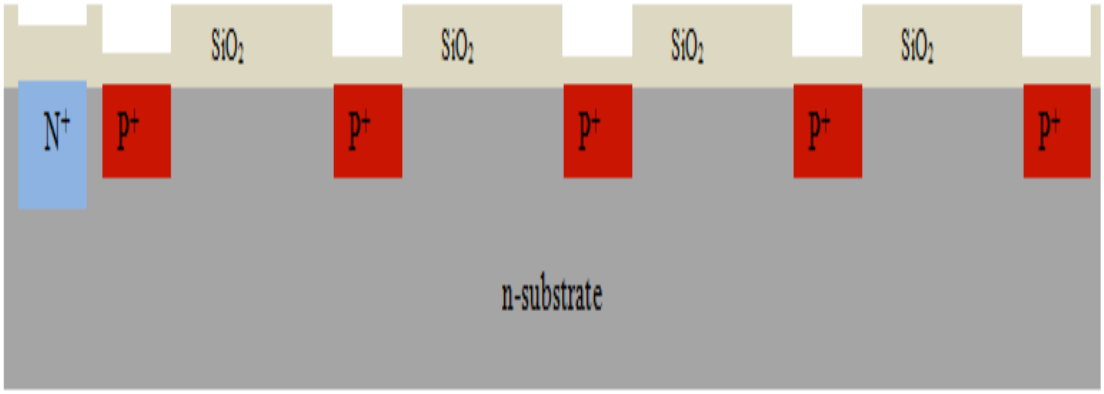


Figure 6.8. The obtained structure after the boron doping process.

6.2 Fabrication of Stacked-NürFETs with 100 nm SiO_2 Gate Dielectrics

Before starting fabrication of stacked-NürFETs, piranha solution cleaning was applied to remove any photoresist residue on the surface of processed silicon substrates. To perform the third lithography process for 100 nm SiO_2 gate oxide, the processed silicon wafers were covered with photoresist with the help of a pin coater. After that similar steps to the previous section's lithography steps were performed, to remove SiO_2 from the channels. The schematic view of this process is shown in Figure 6.9.

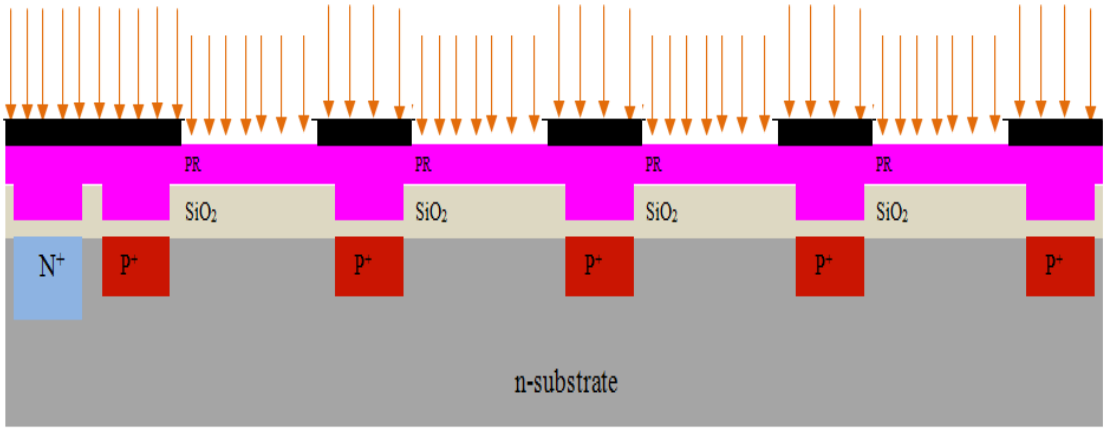


Figure 6.9. Schematic view of the third lithography stage.

The processed silicon wafers were put into a developer solution for 50 seconds to separate the exposed part from the Si substrates. After this step, the wafers were put into a BHF solution to remove the exposed oxide from the structures. Finally, the photoresist in the structures was cleaned with piranha

solution. The schematic view of the structure obtained after this process is given in Figure 6.10.

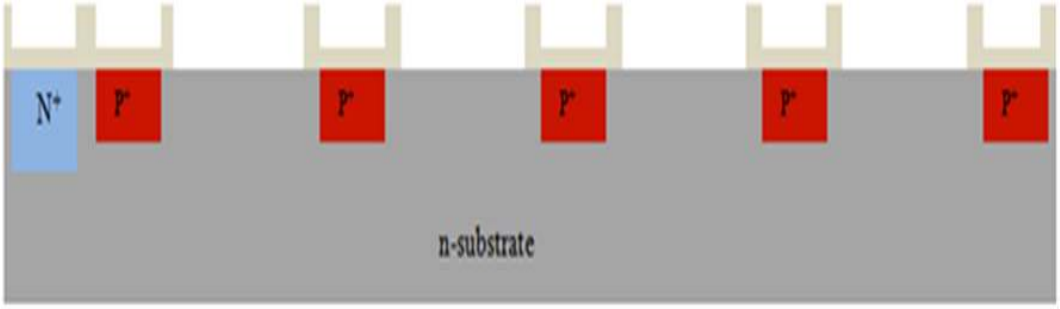


Figure 6.10. Schematic View of the Structure Obtained after the Third Lithography Process.

After the third lithography process, the radiation-sensitive gate oxide layer (100 nm SiO_2) was grown by using the thermal oxidation method.

The thickness of the fabricated 100 nm SiO_2 gate oxide layer was measured with the help of a spectroscopic reflectometer and the results obtained are given in Figure 6.11.

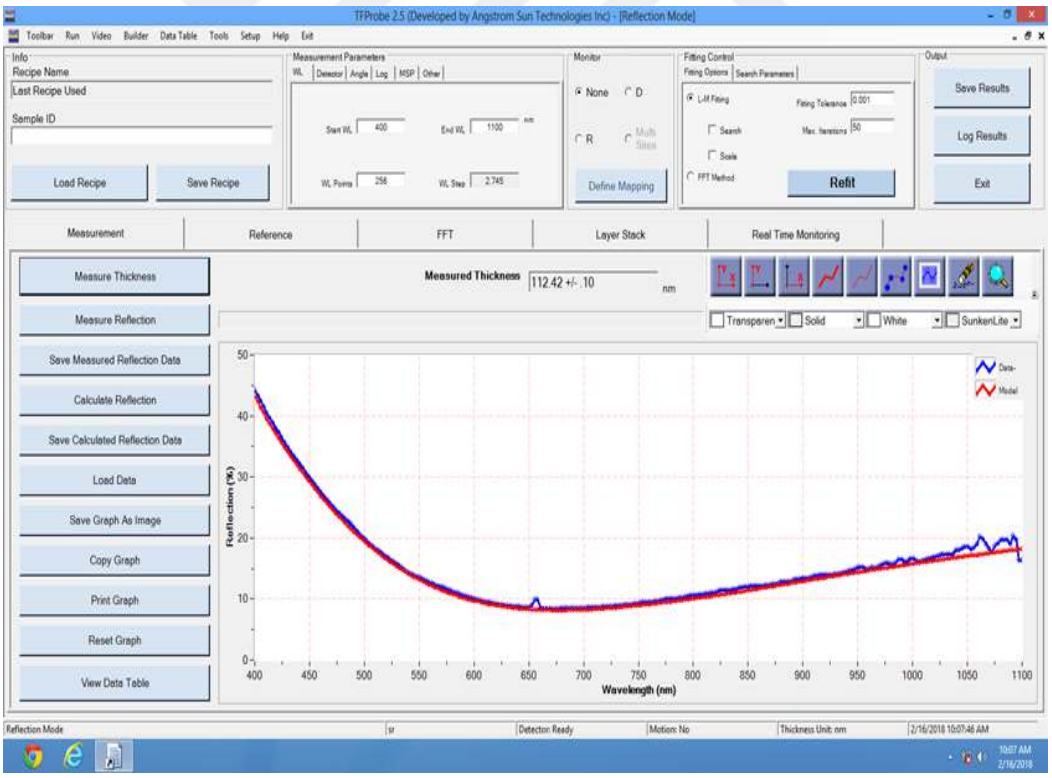


Figure 6.11. 100 nm SiO_2 Gate Oxide Layer Thickness of the Fabricated Stacked-NürFETs.

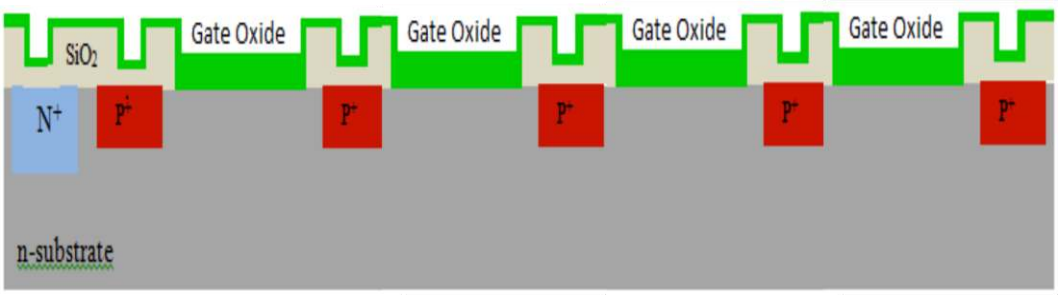


Figure 6.12. Processed Silicon Wafers after Gate Oxide Growth.

6.3 Fabrication of Stacked-NürFETs with 100 nm Er_2O_3 Gate Dielectrics

The substrates of the stacked-NürFETs structures are silicon wafers. Since the stacked-NürFETs to be produced will be in p-channel MOSFETs structures, n-type silicon wafers were used as substrates. The silicon wafers, where all processes will be were carried out were cleaned using various chemicals. For the cleaning process, the RCA cleaning procedure, which is commonly used in the literature, is preferred.

Immediately after the cleaning process was carried out, the field oxide layer was grown on the silicon wafers by wet and dry oxidation method. Field oxide layer formation was carried out in a high temperature (1000 °C) diffusion furnace. The purpose of growing the field oxide layer is to protect the surface smoothness and structure quality of the Si wafers, especially in the doping process and other production stages.

Similar to section 6.2 lithography steps (third lithography) were performed. After the third lithography stage, the radiation-sensitive 100 nm Er_2O_3 gate oxide layer was grown using an electron beam evaporation system. The experimental steps followed in this process are as follows; firstly, the processed silicon wafers were loaded into the electron beam evaporation chamber, then, the pressure of the chamber was set to 5×10^{-4} Pascal. When the process started a current is passed through a conducted filament, which causes heat up and electron emission. High voltage (8 kilovolts) was applied between the hearth and filament to speed up the emitted electrons in the direction of the Er_2O_3 granular target to be grown. A high magnetic field turned these electrons into beams and transferred them to the

deposition material, with high energy, then the material evaporated and grown onto the processed silicon substrates (80).

The thickness of the fabricated 100 nm Er_2O_3 gate oxide layer was measured with the help of a spectroscopic reflectometer and the desired thickness was obtained. The obtained thickness graph is given in Figure 6.13. At the end of the process Er_2O_3 gate oxide layer was grown on the processed silicon substrates. The structure is illustrated in Figure 6.14.

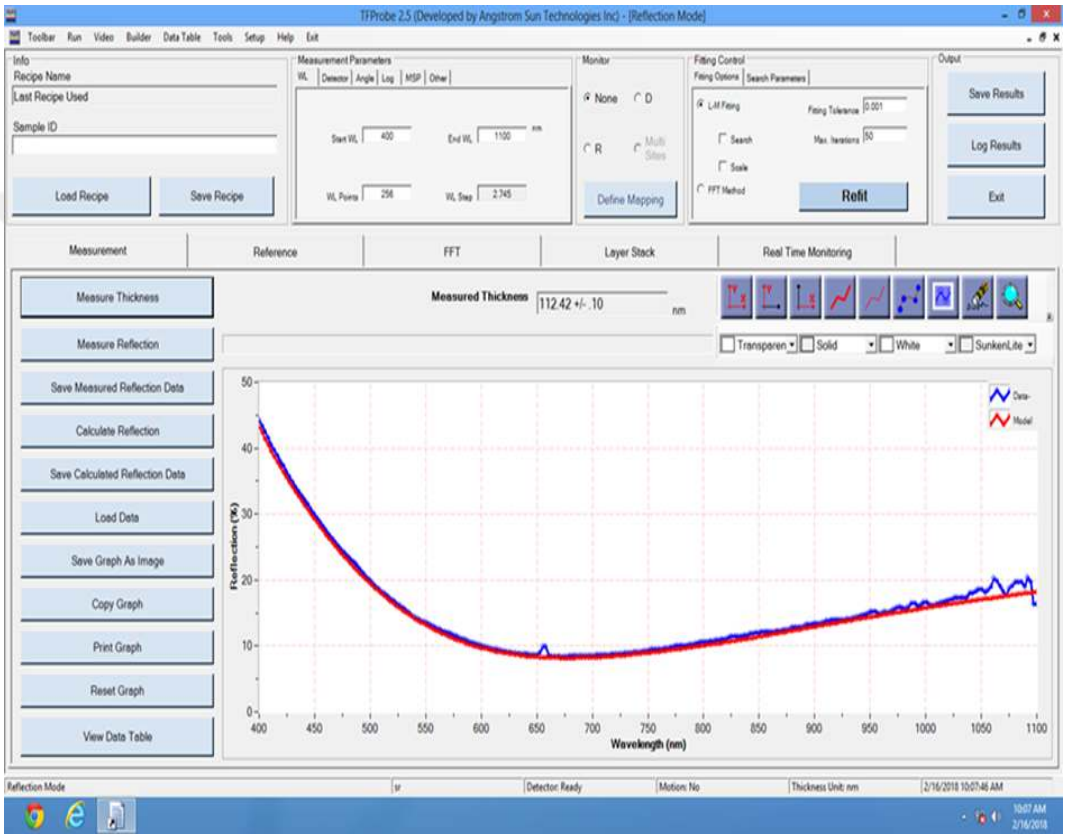


Figure 6.13. 100 nm Er_2O_3 Gate Oxide Layer Thickness of the Fabricated Stacked-NürFETs.

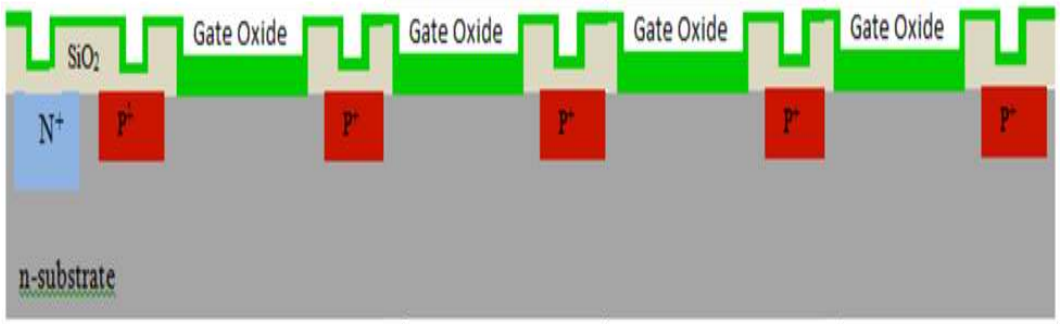


Figure 6.14. The Processed Wafers Structures after the Growth of Er_2O_3 Gate Oxide Dielectric Layer.

6.4 Metallization Process

This section aims to make metal contacts for bulk, source, gate, and drain terminals. To achieve this, the fourth and fifth lithography stages were performed. Therefore, the structures are primarily covered with photoresist with the help of a spin coater. Then, the fourth mask was applied using a mask aligner system, the exposed regions were decomposed with UV light and these regions were developed by putting the processed wafers into a developer solution for 50 seconds. The schematic view of this process is given in Figure 6.15.

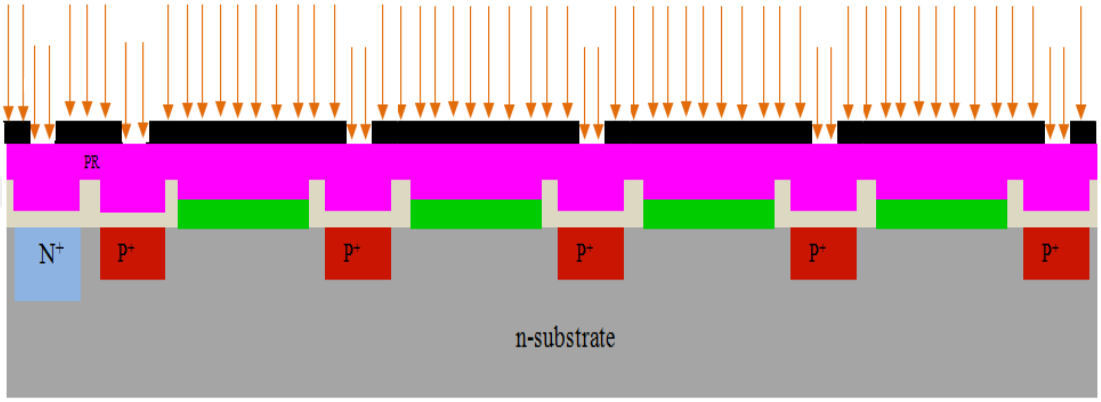


Figure 6.15. A Schematic View of the Lithography Stage Performed to Make Metal Contacts.

Then, the oxide layer was etched using BHF solution and Si substrate was reached. The photoresist was removed from the structure with a piranha solution. The schematic and under microscope view of the structure reached at the end of this process can be seen in Figures 6.16.

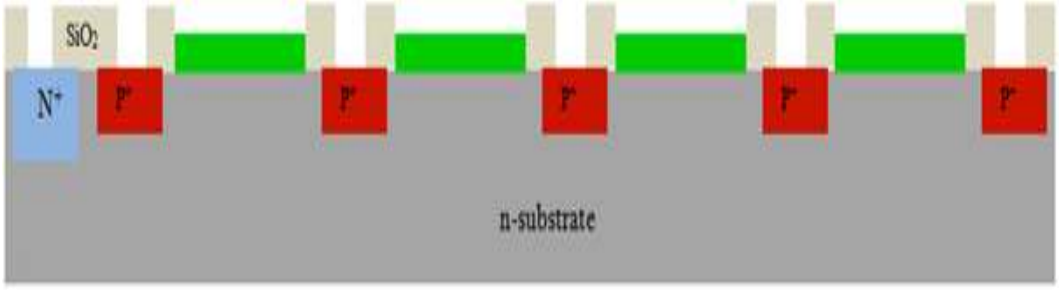


Figure 6.16. After the Fourth Lithography Process; Obtained Structure.

For forming metal contacts, the entire structures were covered with Aluminum (Al) using RF magnetron sputtering system. Firstly, the processed silicon wafers were loaded into the vacuum chamber of the sputtering system. The pressure of the system was adjusted to 6×10^{-4} Pa and the sputtering power was set to 150 W. Later, argon gas was sent into the chamber, and plasma was formed. Pre-

sputtering was performed for 15 minutes to remove possible contaminations on the 99.9% pure Aluminum (Al) target. Following this process, the covers on the Si substrate were opened and Al deposition was performed for 45 minutes.

After Al coating, the final lithography and etching process to separate the structure into source passage, gate, and drain regions were performed. After these two processes, the annealing process was finally performed to reduce the resistance coefficient between the metal and the fabricated layer. The annealing process was performed in forming gas (H_2 and N_2 mixture) environment for 30 minutes at 400 degrees.

6.5 Packaging of the Fabricated Devices

The fabricated stacked-NürFETs with 100 nm SiO_2 and 100 nm Er_2O_3 gate dielectrics oxide chips were diced with the help of a dicing machine. Following the cutting of the stacked-NürFETs, the obtained chips were placed into 8-Pin DIP electronic integrated packages and the terminals electrode were bonded to the packages pin using a wire-bonder.

The packing procedures of the stacked-NürFETs sensors are as follows: (a) completed stacked-NürFETs before cutting, (b) diced stacked-NürFETs chips, and (c) bonded and covered stacked-NürFETs sensors.

6.6 Irradiation of the Fabricated Stacked-NürFETs

The irradiation response of the stacked-NürFETs devices was investigated and evaluated. The stacked-NürFETs having 100 nm SiO_2 and 100 nm Er_2O_3 gate dielectric oxides were exposed to radiation doses at the same conditions. The irradiation experiments were performed under ^{60}Co radioactive source with GAMMACELL 220 irradiation source at the Turkish Atomic Energy Authority (TAEK), Ankara, the image of the source is given in Picture 6.1. The stacked-NürFETs were irradiated at dose ranges from 50 mGy to 48 Gy, with an approximate dose rate of 417 Gy/h. The devices were irradiated with zero gate bias all terminals were grounded. Dimensions of the irradiation chamber were 220 mm x 250 mm and the samples were placed at the center of the irradiation chamber. The samples were also placed perpendicular to irradiation sources to eliminate angle dependency on the irradiation response of the devices.

Picture 6.1. ^{60}Co radioactive source at the Turkish Atomic Energy Authority (TAEK), Ankara.

6.7 Stacked-NürFETs Characterizations and Their Radiation Responses

The required electrical I – V measurements were performed before and after irradiation. For the post-irradiation, I – V measurements; measurements were performed immediately after each exposed irradiation dose. Sensor to sensor variations and the irradiation effects on the sensors in the related measurements doses were plotted and discussed.

6.7.1 Determination of the Initial Threshold Voltages

The threshold voltages are crucial for the operation of the MOSFETs because the current flow almost zero below the V_{th} values. The threshold voltage can be determined using two methods; Extrapolation in Linear Region (ELR) method and the Constant Current (CC) method (5,24,39).

Extrapolation in Linear Region method; The extrapolated threshold voltages are determined from the intersection of linear curve fit of the square root saturation drain current curve as a function of voltage as given in Figure 6.17 (45,55);

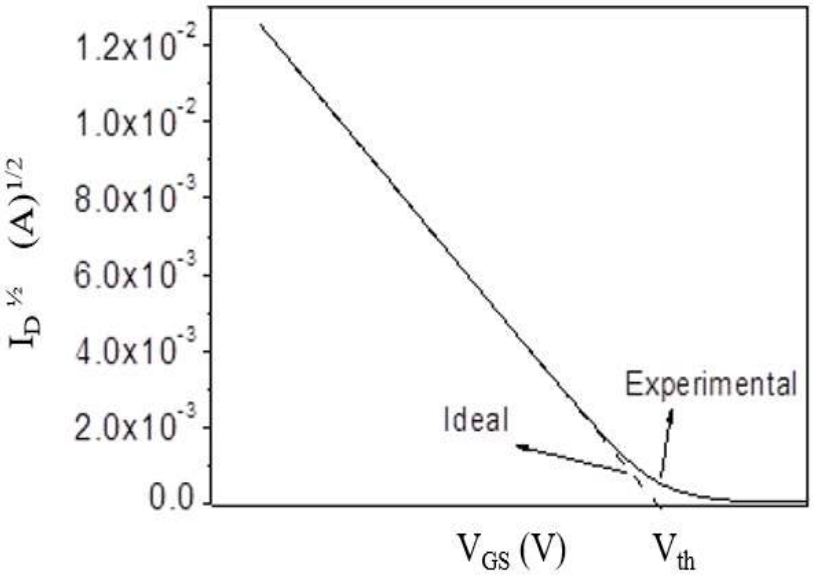


Figure 6.17. V_{th} extrapolation in linear region (ELR) method (45).

In the Constant Current (CC) method; the threshold voltage can be determined from a specific current, which is between 5 to 100 microampere (5 µA – 100 µA). In this study, 10 µA constant current was used to determine the initial threshold voltage. Figure 6.18 illustrates how the constant current method is applied (5,8,9,24,42);

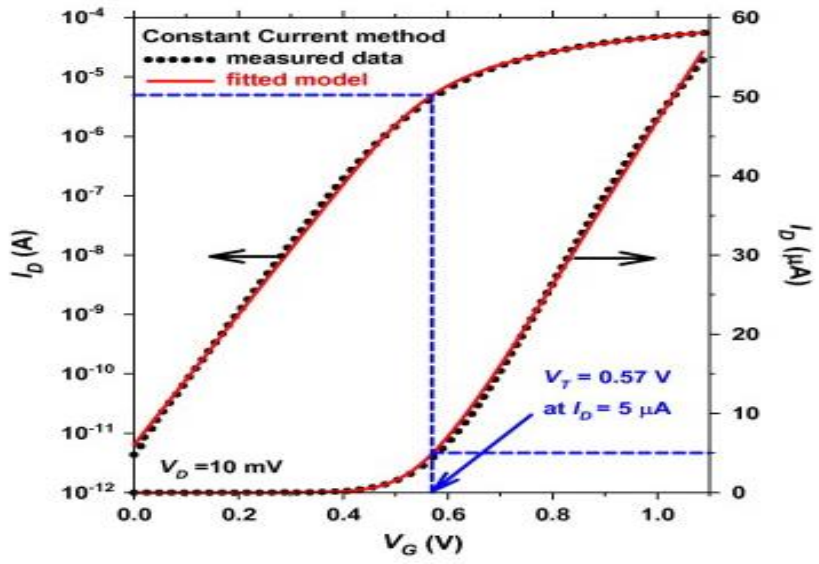


Figure 6.18. V_{th} determination using constant current (CC) method (45).

6.7.2 Mid-Gap Technique

The Mid-gap technique was used to analyze the electrical characteristics of the fabricated Stacked-NürFETs. This technique was used to determine and analyze the radiation-induced oxide trapped charge density (ΔV_{ot}) and interface trapped density (ΔV_{it}). The radiation-induced causes variations in electrical behaviors of the sensors like threshold voltage shifts which were determined and analyzed in detail.

The I – V, transfer characteristics measurements were carried out. Several parameters including the initial threshold voltages (V_{th}), interface state density (ΔN_{it}), and oxide trap density (ΔN_{ot}) were calculated using the measurements.

The stacked-NürFETs were irradiated under zero applied gate voltage (zero gate bias). Before the irradiation current versus voltage (I – V) measurements were obtained, and immediately after every irradiation process I – V measurements were taken again to observe the radiation responses to the stacked-NürFETs.

The radiations response of the stacked-NürFETs sensors was investigated by using the measurements of the I – V transfer characteristics measurements. Here the important specifications for radiation response of the sensors are radiation, threshold voltage shifts (ΔV_{th}), generated interface states (ΔN_{it}), generated oxide traps (ΔN_{ot}), devices sensitivity (S), and fading characteristics (F) of the Stacked-NürFETs sensors after irradiation exposure were investigated and analyzed. The threshold voltage of the devices can shift (ΔV_{th}) due to the contribution of the radiation-induced interface trap voltages (ΔV_{it}) and radiation-induced oxide trapped voltage (ΔV_{ot}), where the shift in the threshold voltages is; $\Delta V_{th} = \Delta V_{it} + \Delta V_{ot.}$ Threshold voltage (V_{th}) values were determined as voltage values at the specified current level (10 μA for SiO_2 stacked-NürFETs, and Er_2O_3 stacked-NürFETs). The values of radiation-induced ΔN_{it} and ΔN_{ot} can be calculated using the changes on the ΔV_{it} and $\Delta V_{ot.}$ As reported in the previous studies, the contribution of the interface traps to the voltage at the mid-gap level is almost zero, and just trapped oxide charges influence the mid-gap voltages (45,115). Hence, the V_{ot} values can be found from the mid-gap level; $V_{MG} = V_{ot}$. The determination of the V_{MG} can be found from the regression of the linear region of the sub-threshold current. The mid-gap current can be calculated by using the sub-threshold current in saturation (4,9,10,12,39).

$$I_D = \frac{\sqrt{2\beta\varepsilon_s}}{2C_{ox}L_d}\left(\frac{kTn_i}{qN_d}\right)^2\left(\frac{q}{kT}\emptyset_s\right)^{-1/2}\exp\left(\frac{q}{kT}\emptyset_s\right) \quad (6.1)$$

Where $\beta = W\mu C_{ox}/L_{eff}$ and $L_d=[(\varepsilon_s kT/(q^2N_d)]^{1/2}$ is the Debye length. It is well-known that in the mid-gap level the condition is $\phi_s = \phi_B$, as stated in the previous sections. Hence, using the straight line of the $\log(I_D) = aV_G + b$ which is obtained from the linear fit of the sub-threshold curve, the V_{MG} that corresponds to the $I_D = I_{MG}$, and can be obtained from; $V_{GM} = (\log(I_{MG}) - b)/a$. Using these processes, the different V_{MG} values were obtained after the irradiation stress and the $\Delta V_{MG} = \Delta V_{ot}$ can be calculated from;

$$\Delta V_{MG} = \Delta V_{ot} = V_{MG,1} - V_{MG,0} \tag{6.2}$$

Where $V_{MG,\,0,}$ and $V_{MG,\,1}$ are the mid-gap voltage values before and after gamma irradiation.

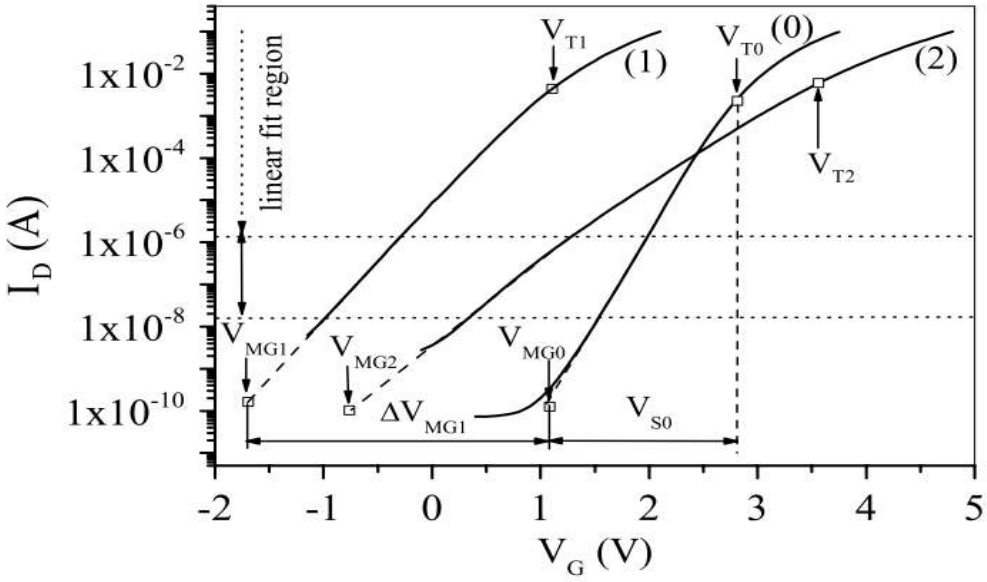


Figure 6.19. The relation between V_{th}, V_{MG}, and V_{so} (45).

The second important parameter is the determination of the stretch-out voltage, V_{so}. To calculate V_{so}, one needs to determine the threshold voltage value. The easiest way to obtain V_{th} is the above-threshold method. In this method, the extrapolated threshold voltages (V_{th}) can be found from the drain current curve in saturation. In other words, the extrapolated threshold voltages are determined from the intersection of linear curve fit of the square root saturation drain current curve as a function of voltage. The following determination of the V_{th} value, the V_{so} can be calculated from;

$$V_{so} = V_{th} - V_{MG} \tag{6.3}$$

Where $V_{MG,0,}$ and $V_{MG,1}$ are the mid-gap voltage values before and after gamma irradiation. Finally, the ΔN_{it} and ΔN_{ot} values can be calculated from;

The relation between V_{th}, $V_{MG,}$ and V_{so} can be seen in Figure 6.19. Using these procedures the different V_{so} values were obtained after the irradiation stress and its value is equal to ΔV_{it}, i.e., $\Delta V_{it} = \Delta V_{so}$ and they can be calculated employing the following:

$$\Delta V_{it} = \Delta V_{so} = V_{so,1} - V_{so,0} \tag{6.4}$$

Where $V_{MG,0,}$ and $V_{MG,1}$ are the mid-gap voltage values before and after gamma irradiation. Finally, the ΔN_{it} and ΔN_{ot} values can be calculated from;

$$\Delta N_{it} = \frac{\Delta V_{it} C_{ox}}{qA} \tag{6.5}$$

$$\Delta N_{ot} = \frac{\Delta V_{ot} C_{ox}}{qA} \tag{6.6}$$

Here the extracted values give the density of the radiation-induced in interface and oxide trapped charge.

7. RESULTS

7.1 Electrical Characteristics of the Stacked-NürFETs before Irradiation

7.1.1 The Electrical Characteristics Obtained for Stacked-NürFETs with 100 nm SiO_2 Gate Dielectric Oxide before Irradiation

Determining the initial threshold voltages. 10 µA constant current was used to determine the initial threshold voltage as explained in chapter 6. Figure 7.1 illustrates the electrical characteristics obtained for Stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide before irradiation, the initial threshold voltages were obtained for 1-NürFETs, 2-NürFETs, 4-NürFETs, 6-NürFETs, 8-NürFETs, 10-NürFETs, and 12-NürFETs stacked-NürFETs as illustrated in Figure 7.1. It is observed that the initial threshold voltage shifts towards higher negative voltage values with the increasing number of NürFET in the Stacked-NürFETs. As the number of NürFETs in the structure increases, the number of charges trapped at the interface and oxide layer increases. Therefore, larger values of negative gate voltage are required to allow current to flow between source and drain.

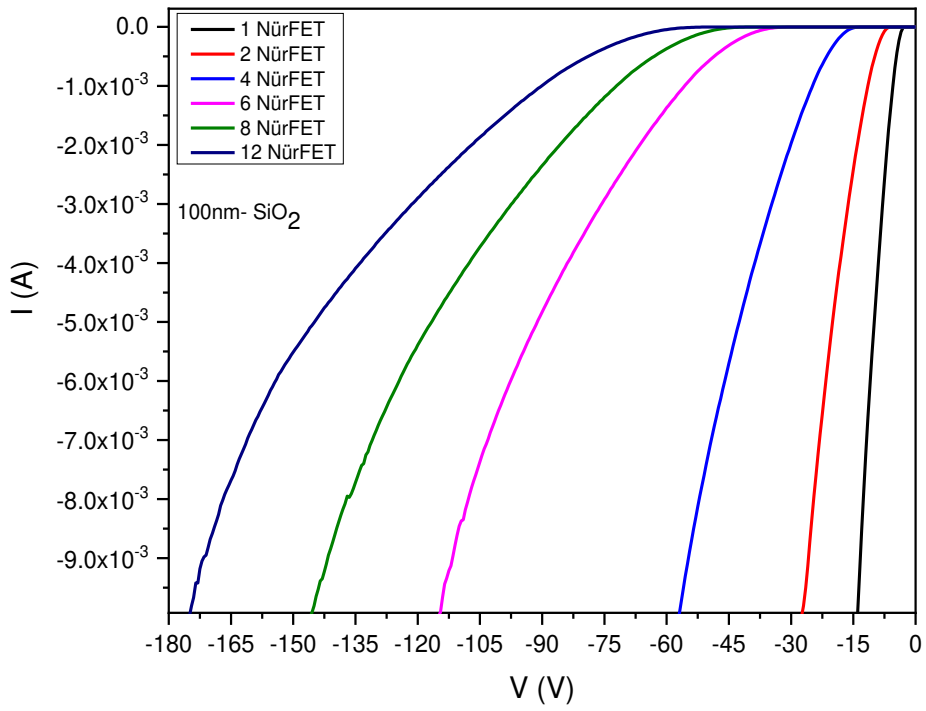


Figure 7.1. The obtained I – V plots for stacked-NürFETs with 100 nm SiO_2 Gate dielectric oxide.

Table 7.1 illustrates the initial threshold voltage values obtained for 1-NürFETs, 2-NürFETs, 4-NürFETs, 6-NürFETs, 8-NürFETs, 10-NürFETs, and 12-NürFETs stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide.

Table 7.1. The threshold voltages of stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide.

Number of Sensors in the Stack.	**Initial Threshold Voltage V_{th} (V)**
1	-3.02
2	-6.51
4	-14.53
6	-32.42
8	-43.44
12	-55.07

Figure 7.2 shows the variation of the initial threshold voltages of stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide depending on the number of NürFETs.

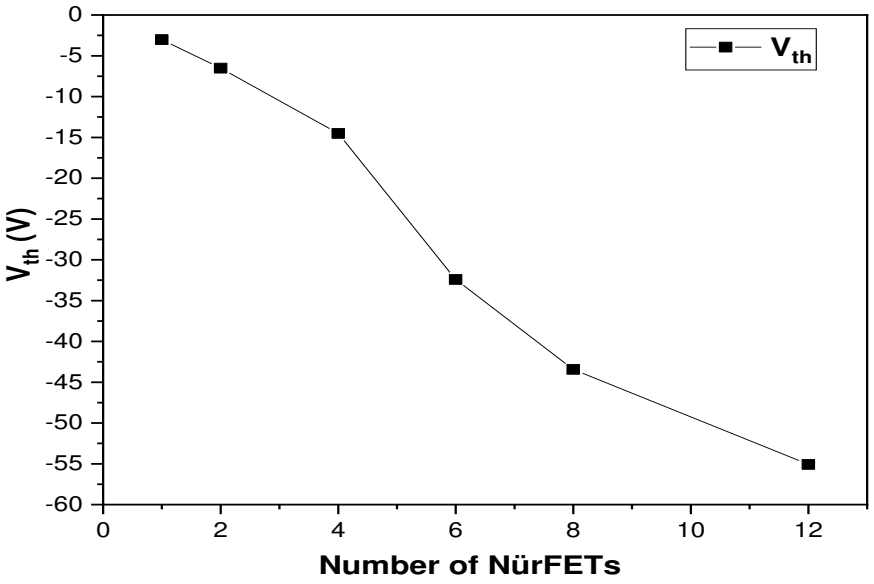


Figure 7.2. The variation of the initial threshold voltages of stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide depending on the number of NürFETs in the stacked structure.

7.1.2 The Electrical Characteristics Obtained for Stacked-NürFETs with 100 nm Er_2O_3 Gate Dielectric Oxide before Irradiation

Figure 7.3 shows the electrical characteristics obtained for stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide before irradiation, the initial threshold voltages were obtained for 1-NürFETs, 2-NürFETs, 4-NürFETs, 6-NürFETs, 8-NürFETs, 10-NürFETs, and 12-NürFETs stacked-NürFETs as illustrated in Figure 7.3.

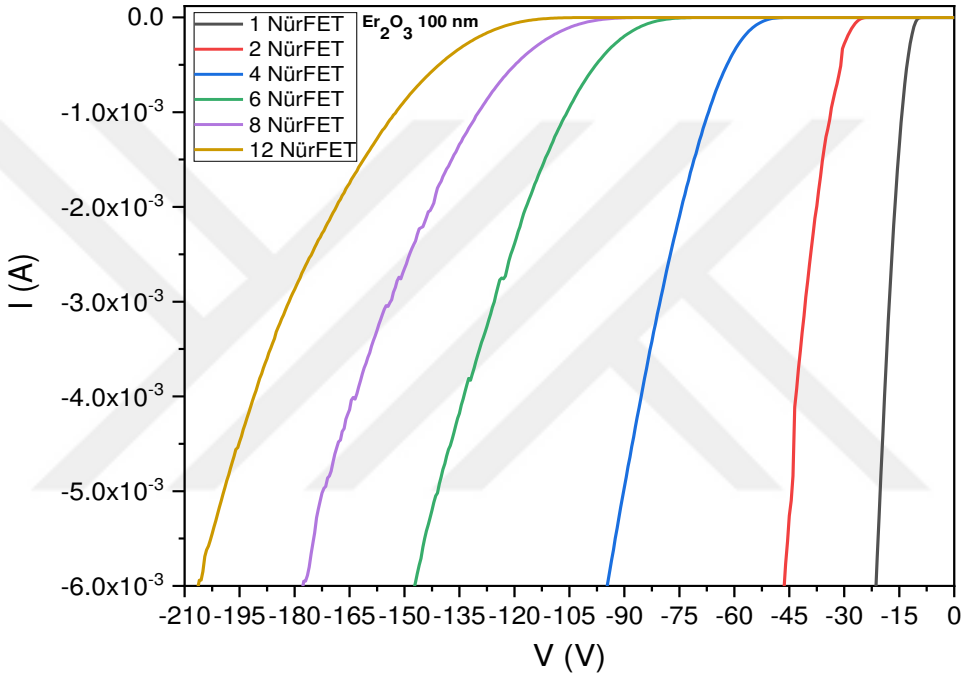


Figure 7.3. The obtained I – V plots for stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide.

As the number of NürFETs in the structure increases, the number of charges trapped at the interface and oxide layer increases. Therefore, higher values of negative gate voltage are essential to allow current conduction between the source and drain. As shown in Figure 7.3 it can be seen that when the number of NürFETs in the stacked-NürFETs increases the initial threshold voltage moves towards higher negative voltage values.

Table 7.2 illustrates the initial threshold voltage values obtained for stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide, and Figure 7.4 illustrates the

variation of the initial threshold voltages of stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide depending on the number of NürFETs in the stacked-NürFETs.

Table 7.2. The threshold voltages of stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide.

Number of Sensors in the Stack.	**Initial Threshold Voltage V_{th} (V)**
1	-9.99
2	-25.32
4	-49.69
6	-76.61
8	-93.85
12	-111.06

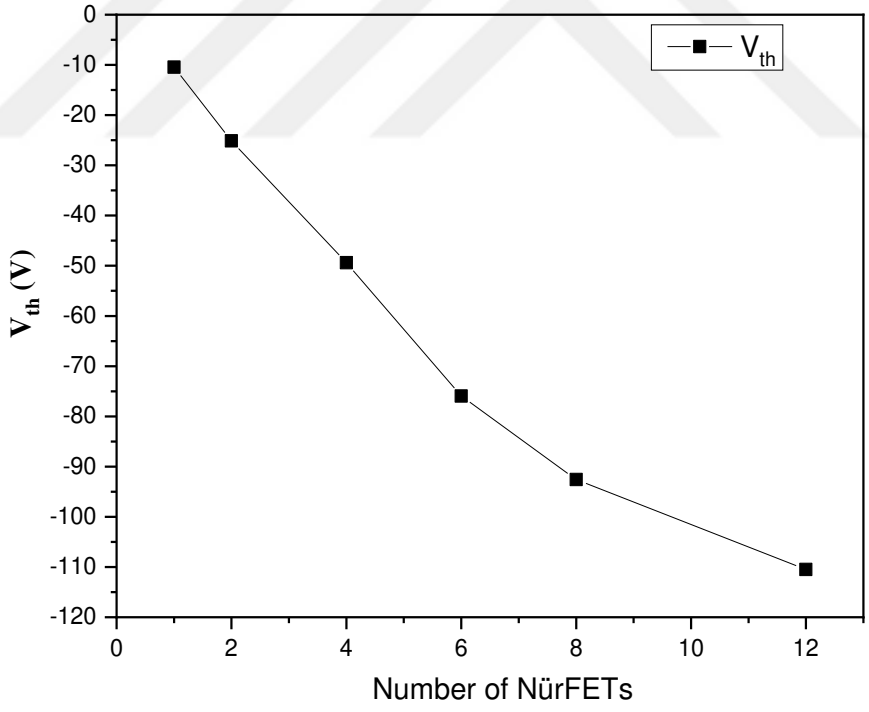


Figure 7.4. The variation of the initial threshold voltages of stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide depending on the number of NürFETs in the stacked structure.

7.2 Radiation Responses of the Stacked-NürFETs under ^{60}Co Radioactive Source

The irradiation response of the stacked-NürFETs devices was investigated and evaluated. The Stacked-NürFETs having 100 nm SiO_2 and 100 nm Er_2O_3 gate dielectric oxides were exposed to radiation doses at the same conditions. The irradiation experiments were performed under a ^{60}Co radioactive source with GAMMACELL 220 irradiation source. The stacked-NürFETs were irradiated at dose ranges from 50 mGy to 48 Gy, with an approximate dose rate of 417 Gy/h.

Under the effect of ionizing radiation, the threshold voltages shift to a negative direction for the fabricated p-channel stacked-NürFETs. The V_{th} shift (ΔV_{th}) is directly proportional to the absorbed radiation dose, D: $\Delta V_{th} = A \times D^n$, where A is a constant, and n is the degree of linearity, which depends on the dielectric thickness, electric field, and the absorbed dose. Ideally, n =1, and then A becomes the sensitivity of the MOS-based sensors, as given in Eq. (7.2) (5,11,23,34,39):

$$\Delta V_{th} = V_{th,\ 1} - V_{th,\ 0} \tag{7.1}$$

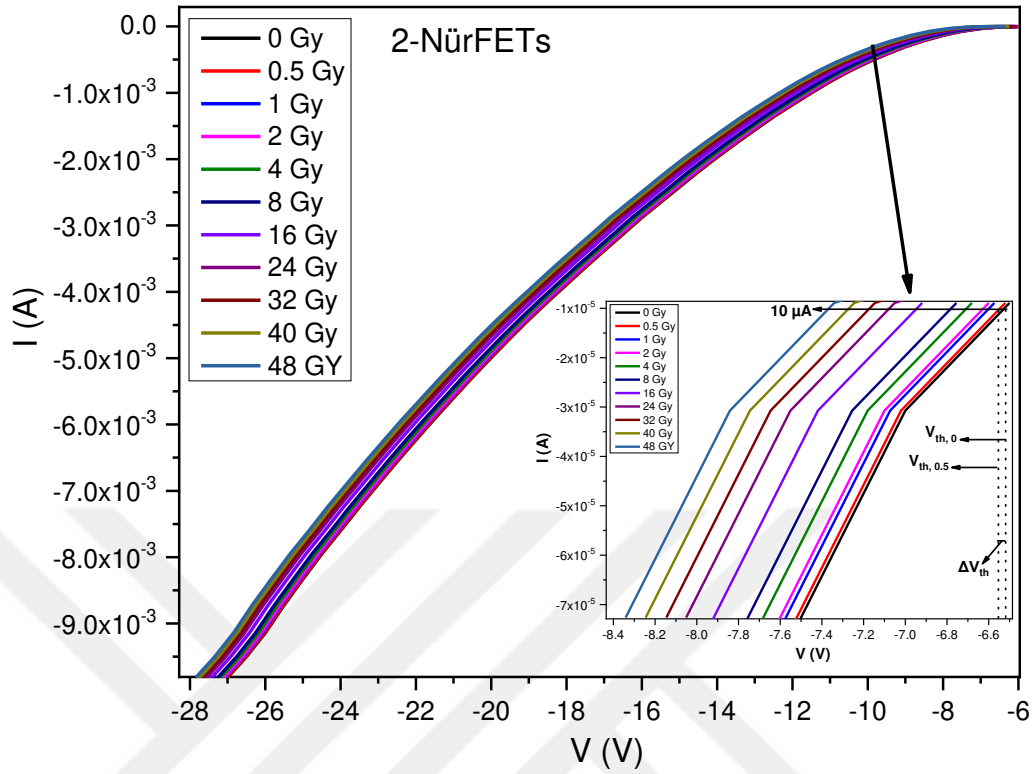
$$S = \frac{\Delta V_{th}}{D} \left(\frac{mV}{Gy}\right) \tag{7.2}$$

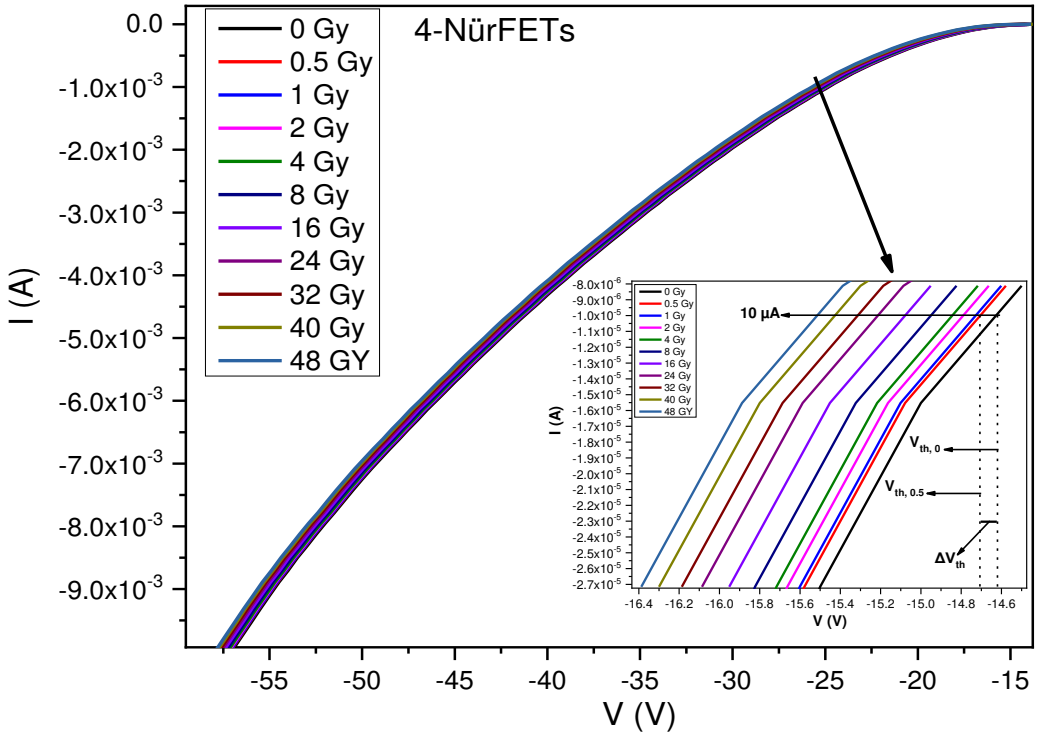
Where $V_{th,\,1}$ is the threshold voltage after irradiation, and $V_{th,\,0}$ is the initial threshold voltage (threshold voltage before irradiation).

The Mid-gap technique was used to analyze the electrical characteristics of the fabricated stacked-NürFETs. This technique was used to determine and analyze the radiation-induced oxide trapped charge density (N_{ot}) and interface trapped density (N_{it}). The radiation-induced causes variations in electrical behaviors of the sensors like threshold voltage shifts which are explained in detail in the previous sections.

7.2.1 Radiation Effects on the Electrical Characteristics of Stacked-NürFETs with 100 nm SiO_2 Gate Dielectric Oxide

The radiation responses on the electrical characteristics of Stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide are given in Figure 7.5 and 7.6, respectively. The threshold voltages shift depending on the applied radiation doses are illustrated in Figure 7.5.


2-NürFETs
0 Gy
0.5 Gy
1 Gy
2 Gy
4 Gy
8 Gy
16 Gy
24 Gy
32 Gy
40 Gy
48 GY
I (A)
V (V)
10 µA
$V_{th, 0}$
$V_{th, 0.5}$
ΔV_{th}


4-NürFETs
0 Gy
0.5 Gy
1 Gy
2 Gy
4 Gy
8 Gy
16 Gy
24 Gy
32 Gy
40 Gy
48 GY
I (A)
V (V)
10 µA
$V_{th, 0}$
$V_{th, 0.5}$
ΔV_{th}

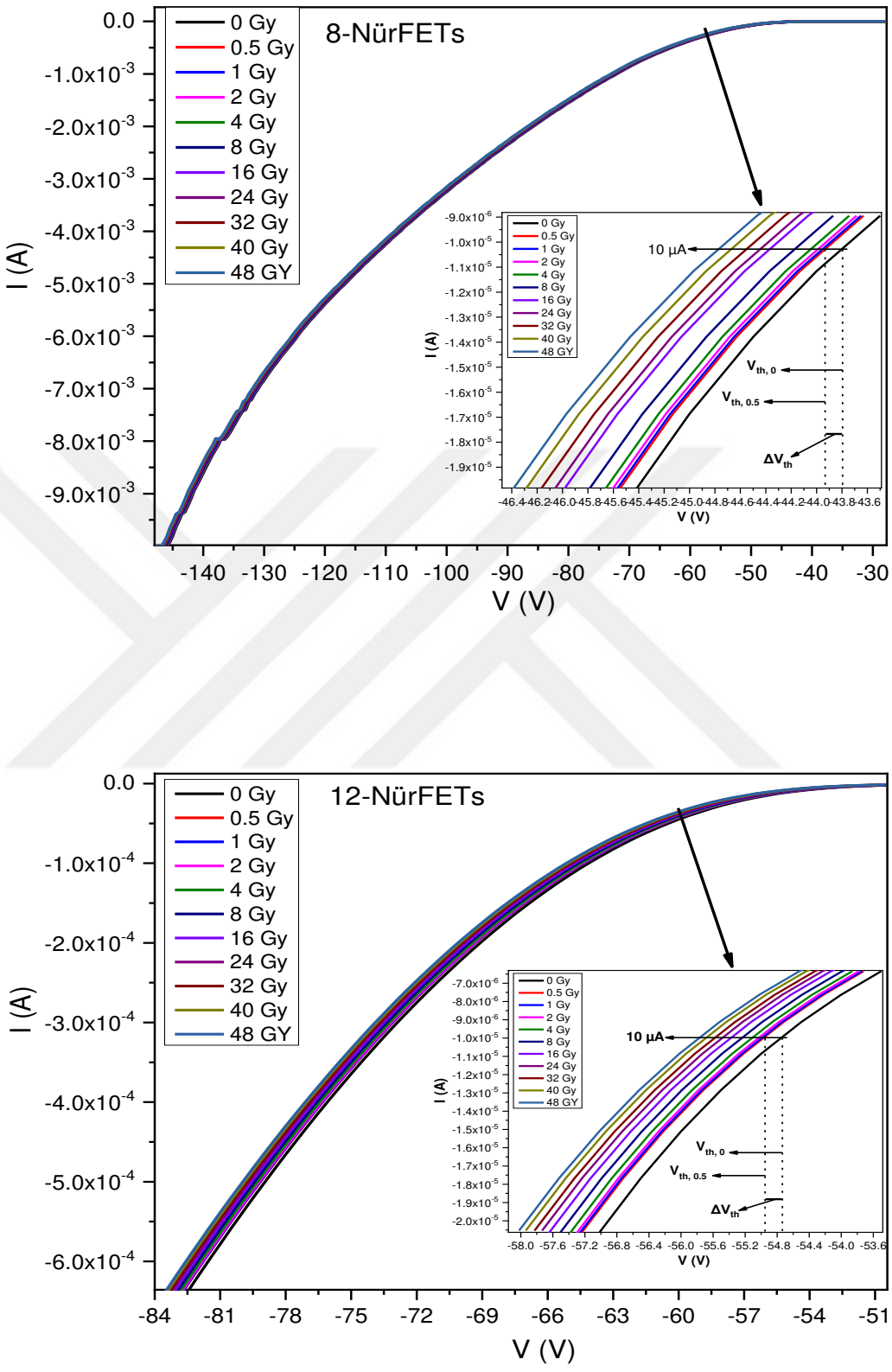


Figure 7.5. Threshold voltages shift depending on the applied radiation doses of stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide.

As seen in Figure 7.5 the radiation-induced causes variations in electrical behaviors of the stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide sensors. Under the effect of ionizing radiation, the threshold voltage shifted to higher negative values, which is directly proportional to the absorbed radiation dose.

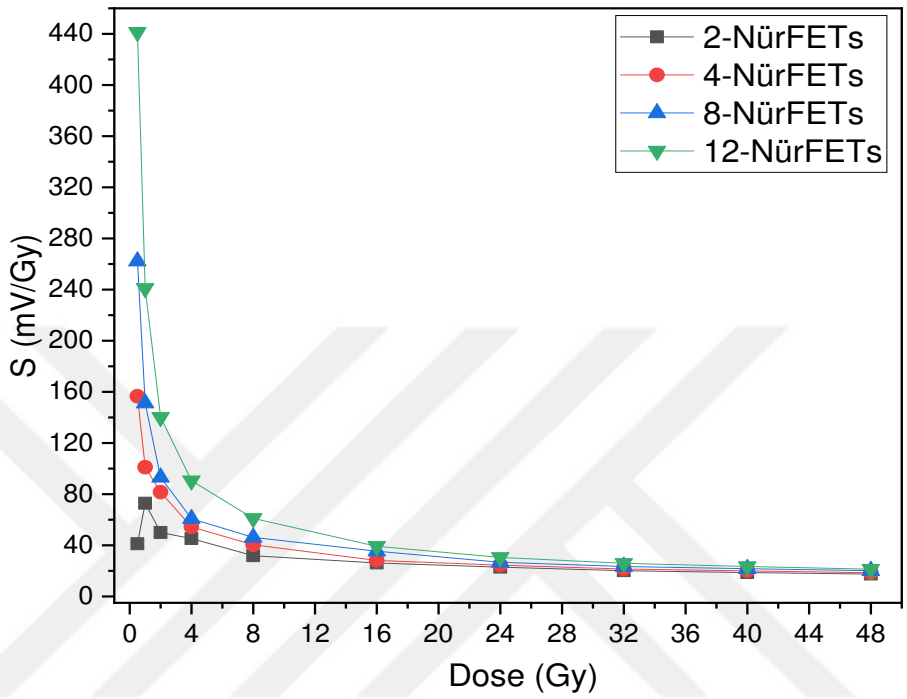


Figure 7.6. Sensitivity (S) of the stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide as a function of the applied radiation dose.

The sensitivities (S) of the stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide sensors for the applied doses are shown in Figure 7.6 and Table 7.3. As seen in the figures the sensitivities increase with the number of NürFETs in the sensor. However, the sensitivities decrease with the increase in radiation doses. Owing to the oxidation-induced defects and impurities created by irradiation. When the radiation interacts with the sensitive region (gate dielectric oxide), electron-hall pairs are formed in the structure. With the increasing radiation dose, more charges are trapped in the oxide layer and caused the internal electric field to increase in the device over time. Due to these electric field effects, sensitivity deviates from linearity as high doses are reached.

Table 7.3. Sensitivity (S) of the stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide as a function of the applied radiation dose.

Dose (Gy)	**2-NürFET S (mV/Gy)**	**4-NürFET S (mV/Gy)**	**8-NürFET S (mV/Gy)**	**12-NürFET S (mV/Gy)**
0.5	41.2	156.56	262.26	441.29
1	72.9	101.11	151.15	240.89
2	49.95	81.58	93.09	140.18
4	45.25	54.31	60.81	90.59
8	31.88	40.42	46.17	61.11
16	26.19	28.22	35.41	39.16
24	22.96	24.44	26.74	30.58
32	20.19	21.46	23.43	25.88
40	18.63	19.99	21.75	23.44
48	17.53	18.49	20.19	21.28

Table 7.4 shows the oxide trapped charge densities of the Stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide. It is observed that as the number of NürFETs in the Stacked-NürFETs increases, the number of charges trapped at the interface and oxide layer increases. Therefore, higher values of negative gate voltage, which are essential to allow current to drift between source and drain are observed. It is also observed that both the oxide trapped charge and interface trapped charge densities increase with the increasing radiation doses applied to the stacked-NürFETs. Furthermore, the oxide trapped charge densities increase in direct proportion to the number of sensors in the Stacked-NürFET.

Table 7.5 illustrates the variations of the interface trapped charge density of the Stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide. It is observed that as the number of NürFETs in the Stacked-NürFETs increases, the number of charges trapped at the interface layer increases. It is also observed that interface trapped charge densities increase with the increasing radiation doses applied to the stacked-NürFETs.

Table 7.4. Oxide Trapped Charge Densities of Stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide as a Function of the Applied Radiation Dose.

Dose (Gy)	**2-NürFET N_{ot} (cm^{-2})**	**4-NürFET N_{ot} (cm^{-2})**	**8-NürFET N_{ot} (cm^{-2})**	**12-NürFET N_{ot} (cm^{-2})**
0.5	5.10×10^{9}	1.59×10^{10}	2.64×10^{10}	4.72×10^{10}
1	1.53×10^{10}	2.19×10^{10}	3.52×10^{10}	5.19×10^{10}
2	2.17×10^{10}	3.38×10^{10}	3.96×10^{10}	5.97×10^{10}
4	3.95×10^{10}	4.77×10^{10}	5.28×10^{10}	7.70×10^{10}
8	5.48×10^{10}	6.95×10^{10}	7.91×10^{10}	1.06×10^{11}
16	9.05×10^{10}	9.74×10^{10}	1.19×10^{11}	1.34×10^{11}
24	1.20×10^{11}	1.28×10^{11}	1.37×10^{11}	1.58×10^{11}
32	1.39×10^{11}	1.47×10^{11}	1.59×10^{11}	1.78×10^{11}
40	1.56×10^{11}	1.71×10^{11}	1.85×10^{11}	2.02×10^{11}
48	1.74×10^{11}	1.91×10^{11}	2.07×10^{11}	2.19×10^{11}

Table 7.5. Interface Trapped Charge Densities of Stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide as a Function of the Applied Radiation Dose.

Dose (Gy)	2-NürFET N_{it} (cm^{-2})	4-NürFET N_{it} (cm^{-2})	8-NürFET N_{it} (cm^{-2})	12-NürET N_{it} (cm^{-2})
0.5	6.67×10^{8}	9.42×10^{8}	1.82×10^{9}	2.91×10^{8}
1	3.66×10^{8}	1.08×10^{8}	2.66×10^{9}	6.67×10^{7}
2	1.94×10^{8}	1.33×10^{9}	4.71×10^{8}	5.72×10^{8}
4	5.81×10^{8}	9.64×10^{8}	4.43×10^{8}	9.14×10^{8}
8	2.15×10^{7}	4.30×10^{6}	3.16×10^{8}	1.57×10^{8}
16	3.87×10^{8}	2.69×10^{8}	3.17×10^{9}	1.15×10^{9}
24	1.32×10^{9}	1.02×10^{9}	1.73×10^{9}	6.47×10^{8}
32	2.15×10^{7}	6.65×10^{8}	3.02×10^{9}	4.60×10^{8}
40	4.91×10^{9}	1.14×10^{9}	2.47×10^{9}	3.97×10^{8}
48	7.70×10^{9}	4.09×10^{9}	1.82×10^{9}	1.15×10^{9}

Fading characteristics of the Stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide are shown in Figure 7.7. The fading characteristics increase with the increasing number of NürFETs in the Stacked-NürFETs. The most important reason for this is that the trapped charge densities in the structure increase with the increasing sensitivity and consequently the number of charges that are released from the traps over time. On the other hand, the 5,37% fading value observed in 2-NürFETs indicates that the dose can be preserved by storing for a long time in these structures.

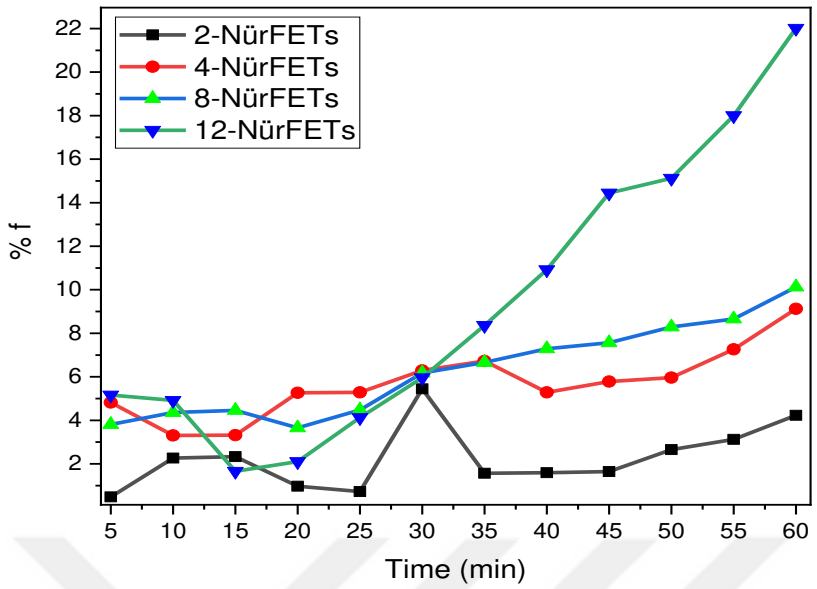
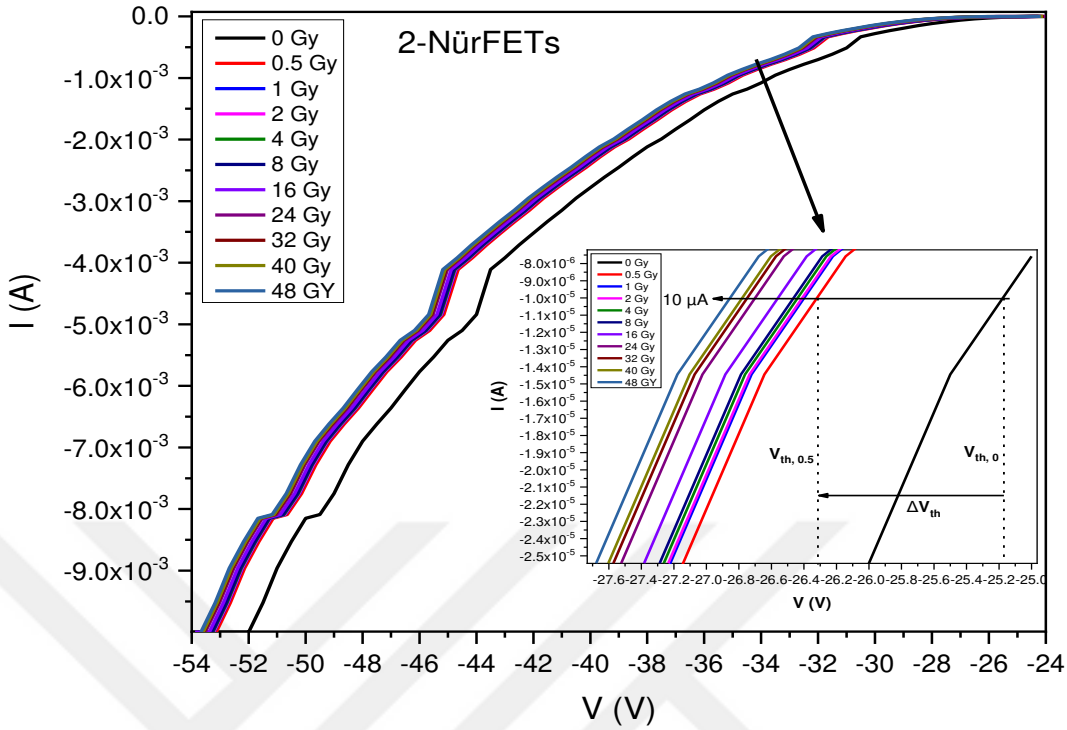


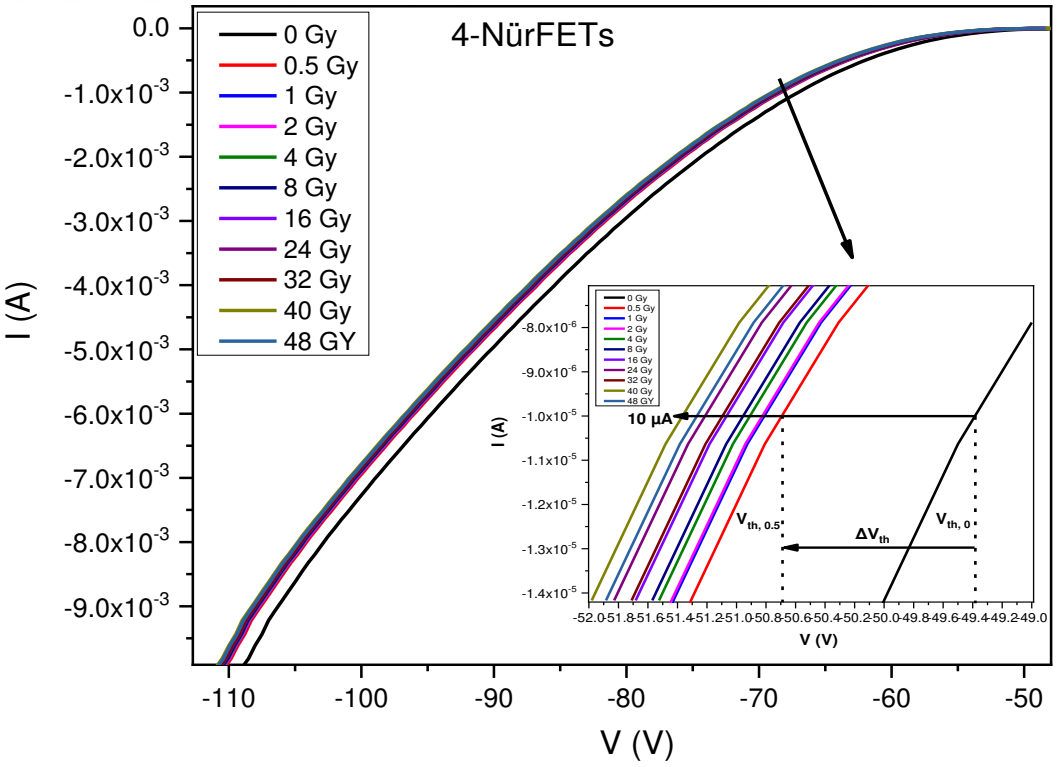
Figure 7.7. The Post-Irradiation Fading Values of Stacked-NürFETs with 100 nm SiO_2 gate dielectric oxide.

7.2.2 Radiation Effects on the Electrical Characteristics of Stacked-NürFETs with 100 nm Er_2O_3 Gate Dielectric Oxide

In Figure 7.8 the changes in threshold voltages after ^{60}Co irradiation of the stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide are illustrated depending on the applied radiation doses. The radiation responses on the electrical characteristics of Stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide are given in Figure 7.8 and 7.9, respectively. The threshold voltages shift (ΔV_{th}) depending on the applied radiation doses are illustrated in Figure 7.8. The sensitivities (S) of the Stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide depending on the applied radiation doses are shown in Figure 7.9 and Table 7.6. When the radiation interacts with the sensitive region (gate dielectric oxide), electron-hall pairs are formed in the structure. With the increasing radiation dose, more charge will be trapped in the oxide layer and the internal electric field will increase in the structure over time. Due to this electric field shielding effect, sensitivity deviates from linearity as doses increased.

These results show that the sensitivity increases with the increasing number of NürFET in the Stacked-NürFETs. On the other hand, the sensitivity did not increase in direct proportion to the number of sensors in the Stacked-NürFET. The most important reason for this is the electric field shielding effect.


2-NürFETs
0 Gy
0.5 Gy
1 Gy
2 Gy
4 Gy
8 Gy
16 Gy
24 Gy
32 Gy
40 Gy
48 GY
I (A)
V (V)
10 µA
$V_{th, 0.5}$
$V_{th, 0}$
ΔV_{th}


4-NürFETs
0 Gy
0.5 Gy
1 Gy
2 Gy
4 Gy
8 Gy
16 Gy
24 Gy
32 Gy
40 Gy
48 GY
I (A)
V (V)
10 µA
$V_{th, 0.5}$
$V_{th, 0}$
ΔV_{th}

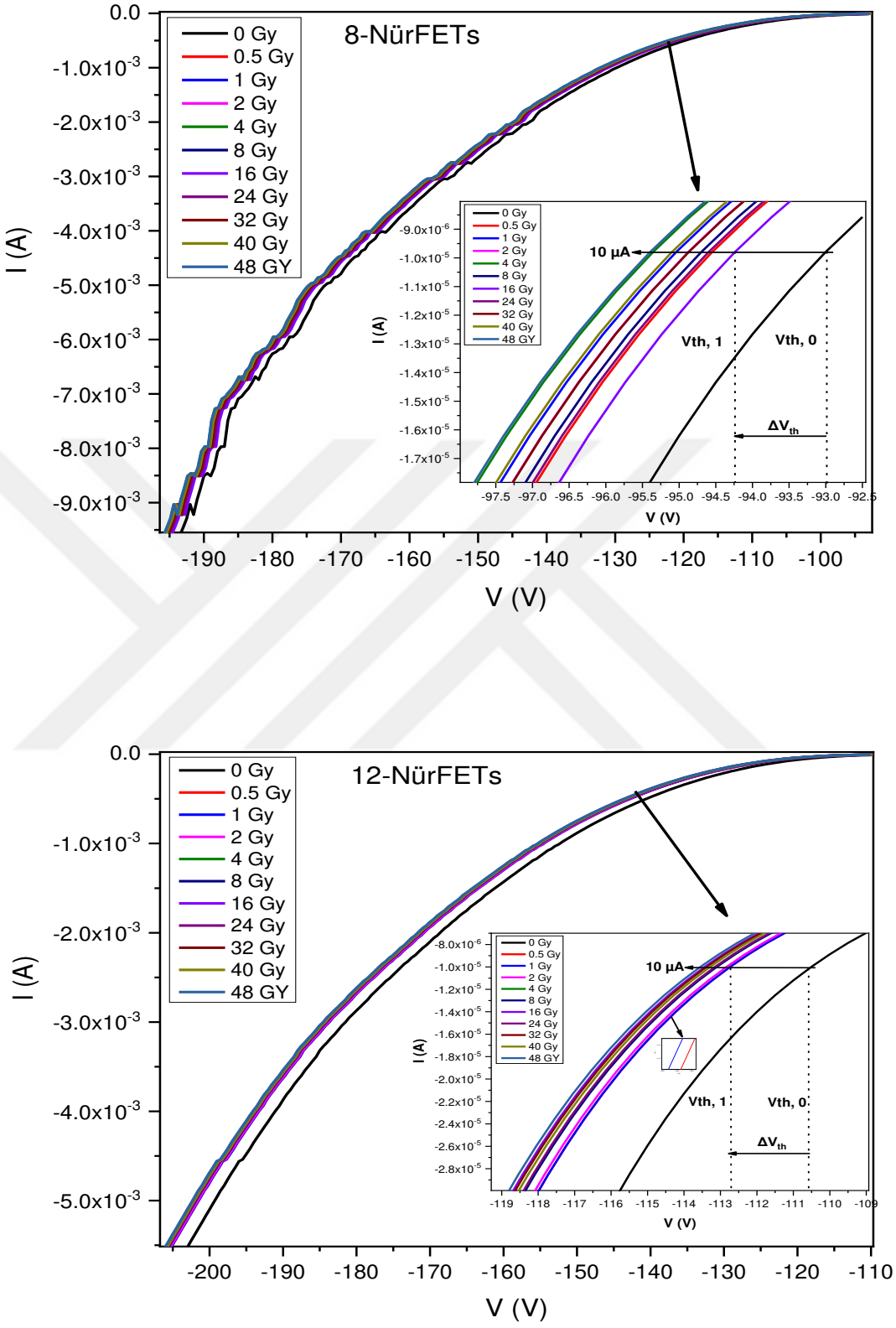


Figure 7.8. Threshold Voltages Shifts Depending on the Applied Radiation Doses of Stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide.

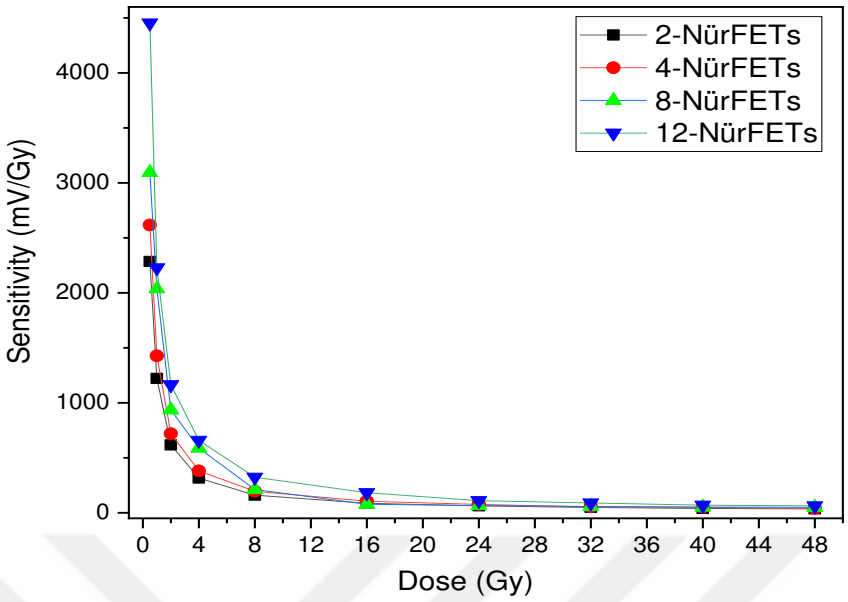


Figure 7.9. Sensitivity (S) of Stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide as a Function of the Applied Radiation Dose.

Table 7.6. Sensitivity (S) Values of Stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide as a Function of the Applied Radiation Dose.

Dose (Gy)	**2-NürFET S (mV/Gy)**	**4-NürFET S (mV/Gy)**	**8-NürFET S (mV/Gy)**	**12-NürFET S (mV/Gy)**
0.5	2286	2616.62	3095.09	4453.63
1	1222	1427.43	2037.04	2227.65
2	617	720.22	935.94	1164.29
4	315.50	381.13	588.34	658.59
8	160.87	196.32	211.96	324.17
16	86.44	105.17	77.27	183.07
24	63.50	76.20	66.45	110.11
32	49.13	53.46	58.37	89.82
40	40.08	49.53	52.39	69.43
48	34.96	39.25	49.84	63.41

Table 7.7 and 7.8 show the oxide trapped charge densities and interface trapped charge densities of the Stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide. It is observed that as the number of NürFETs in the stacked-NürFETs increases, the number of charges trapped at the oxide and interface layers increases. It is also observed that trapped charge densities increase with the increasing radiation doses applied to the stacked-NürFETs.

Table 7.7. Oxide Trapped Charge Densities of Stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide as a Function of the Applied Radiation Dose.

Dose (Gy)	**2-NürFET** N_{ot} **(cm^{-2})**	**4-NürFET** N_{ot} **(cm^{-2})**	**8-NürFET** N_{ot} **(cm^{-2})**	**12-NürFET** N_{ot} **(cm^{-2})**
0.5	8.84×10^{11}	1.01×10^{12}	9.25×10^{11}	1.74×10^{12}
1	9.43×10^{11}	1.11×10^{12}	9.55×10^{11}	1.76×10^{12}
2	9.54×10^{11}	1.12×10^{12}	1.19×10^{12}	1.82×10^{12}
4	9.79×10^{11}	1.18×10^{12}	1.23×10^{12}	2.02×10^{12}
8	9.93×10^{11}	1.22×10^{12}	1.31×10^{12}	2.07×10^{12}
16	1.07×10^{12}	1.31×10^{12}	1.44×10^{12}	2.17×10^{12}
24	1.18×10^{12}	1.33×10^{12}	1.57×10^{12}	2.23×10^{12}
32	1.22×10^{12}	1.42×10^{12}	1.62×10^{12}	2.29×10^{12}
40	1.24×10^{12}	1.46×10^{12}	1.82×10^{12}	2.33×10^{12}
48	1.30×10^{12}	1.53×10^{12}	1.86×10^{12}	2.39×10^{12}

Table 7.8. Interface Trapped Charge Densities of Stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide as a Function of the Applied Radiation Dose.

Dose (Gy)	2-NürFET N_{it} (cm^{-2})	4-NürFET N_{it} (cm^{-2})	8-NürFET N_{it} (cm^{-2})	12-NürET N_{it} (cm^{-2})
0.5	1.56×10^{9}	1.78×10^{9}	2.73×10^{11}	1.64×10^{10}
1	3.10×10^{9}	4.31×10^{9}	6.23×10^{11}	3.97×10^{10}
2	1.55×10^{9}	1.98×10^{9}	2.54×10^{11}	1.96×10^{10}
4	1.60×10^{9}	1.92×10^{9}	5.92×10^{11}	2.12×10^{10}
8	3.10×10^{9}	4.41×10^{8}	2.87×10^{9}	5.39×10^{10}
16	3.88×10^{9}	1.79×10^{9}	4.85×10^{11}	1.01×10^{11}
24	1.55×10^{9}	9.43×10^{10}	3.42×10^{11}	1.82×10^{11}
32	7.75×10^{8}	9.47×10^{10}	1.76×10^{11}	5.33×10^{10}
40	3.89×10^{9}	7.35×10^{10}	2.02×10^{11}	1.81×10^{11}
48	3.11×10^{9}	7.44×10^{10}	3.63×10^{9}	3.82×10^{10}

Fading characteristics of the Stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide are shown in Figure 7.10. It is observed that the fading values fluctuate, and the fading characteristics increase with the increasing number of NürFETs in the Stacked-NürFETs. The most important reason for this is that the trapped charge densities in the structure increase with the increasing sensitivity region and consequently the number of charges that are released from the traps over time. Furthermore, the observed highest fading value for 2-NürFETs is 6.18% and for the 12-NürFETs is 20.03% were observed fading value was observed Er_2O_3 Stacked-NürFETs, this indicates that the dose can be preserved by storing for a long time in these Stacked-NürFETs.

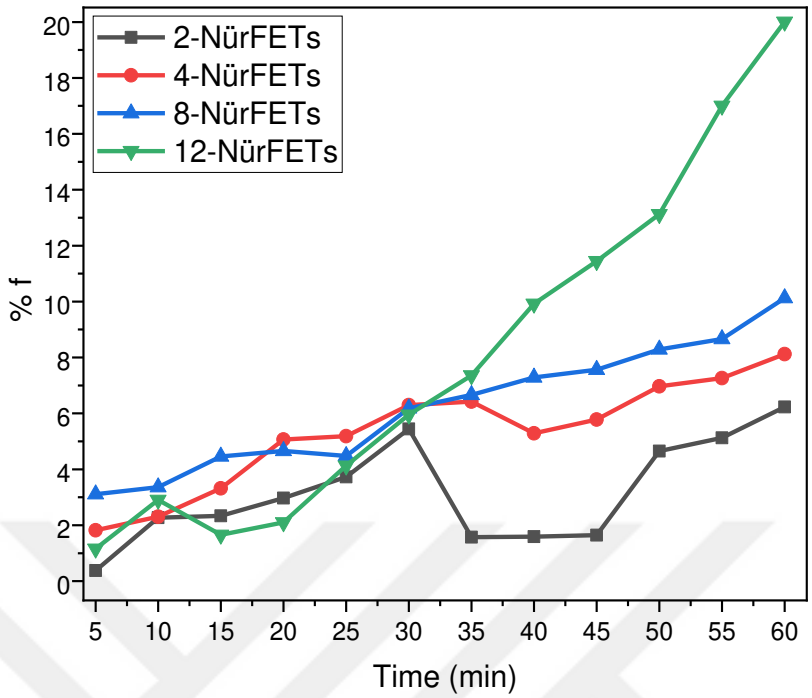


Figure 7.10. The Post-Irradiation Fading Values of Stacked-NürFETs with 100 nm Er_2O_3 gate dielectric oxide.

8. DISCUSSION

In this section, the author discusses and investigates the meaning, importance, and relevance of the obtained results. By explaining and evaluating what is obtained, which describes how they are related to the previous studies.

The electrical characteristics obtained for the fabricated stacked-NürFETs with 100 nm SiO_2, and 100 nm Er_2O_3 gate dielectrics oxide before irradiation were plotted and investigated. Furthermore, the obtained results have shown the expected values. When these devices are irradiated, it will be difficult to see the threshold voltage shifts, which will be higher than 200 volts. Therefore, initial threshold voltages of stacked-NürFETs with 100 nm SiO_2, and 100 nm Er_2O_3 gate dielectrics oxide were measured for 1, 2, 4, 6, 8, and 12-stacked-NürFETs. And for the irradiation 2, 4, 8, and 12-stacked-NürFETs were prepared and irradiated. This helped to easily bonded the NürFETs and determined the irradiation responses of the stacked-NürFETs. It is observed that the initial threshold voltages move towards higher negative voltage values with the increasing number of NürFET in the stacked-NürFETs. As the number of NürFETs in the structure increases, the number of charges trapped at the interface and oxide layer increases. Therefore, larger values of negative gate voltage are required to allow current to flow between source and drain (1,2,44,57,58).

Table 8.1. Compared threshold voltage values of the stacked-NürFETs.

Number of Sensors in the Stacked-NürFETs	**SiO_2 Initial Threshold Voltage V_{th} (V)**	**Er_2O_3 Initial Threshold Voltage V_{th} (V)**
1	-3.02	**-9.99**
2	-6.51	**-25.31**
4	-14.52	**-49.68**
6	-32.41	**-76.60**
8	-43.44	**-93.85**
12	-55.07	**-111.05**

Comparing the two stacked-NürFETs of 100 nm SiO_2 and 100 nm Er_2O_3 gate dielectrics to the single MOS-based sensors, it is observed that the initial threshold voltages and the irradiation sensitivities of the stacked-NürFETs are much higher than the single NürFETs (3–8,12,14,17,19,20,24,25,35,39,42,53,122). The reason for these values is the presence of high parasitic charge densities generated by the increasing number of NürFETs.

When the V_{th} obtained for the stacked-NürFETs of 100 nm SiO_2 is compared to the stacked-NürFETs of 100 nm Er_2O_3 as shown in Table 8.1. It is observed that the initial threshold voltages shifted with the increase in the number of NürFETs for both. However, the highest threshold voltage values were obtained in 100 nm Er_2O_3 gate oxide layer Stacked-NürFETs. Though the SiO_2/Si interface exhibits excellent interface quality for the MOS-based technologies, due to stack structure interface defects are significant, which bring about the threshold voltages shifted to the higher values. Moreover, changes occurred in the trapped charges with time, which caused the variations in the device characteristics. The charge carriers are scattered by the site of the defect in the device channel, causing lower carrier mobilities and the high number of traps that caused variation in the stacked-NürFETs (13,22,24,26,37,39,44,58).

As expected, the initial electrical characteristics of the fabricated stacked-NürFETs have improved with the increasing number of NürFETs in the device, however, larger shifts to higher negative voltages in the Er_2O_3 stacked-NürFETs have been observed compared to the SiO_2 stacked-NürFETs. As given in Table 8.1, the initial threshold values of Er_2O_3 stacked-NürFETs are higher than the initial threshold values of the SiO_2 stacked-NürFETs. The reason for this behavior is related to the generation of trapped charges in the Er_2O_3 device structure at the time of the fabrication processes (2,12,34,36,58). Moreover, this indicates that positive charges are trapped during the fabrication of the Er_2O_3, owing to these trapped positive charges; the initial threshold voltages of the Er_2O_3 stacked-NürFETs are higher than the SiO_2 stacked-NürFETs (5,24,25,34,38).

Under the effect of ionizing radiation, the stacked-NürFETs threshold voltages shifted to the higher negative voltages with the increasing doses. The V_{th} shift (ΔV_{th}) is directly proportional to the absorbed radiation dose. However, a

decrease in the ΔV_{th} with increasing radiation doses is observed, oxidation-induced defects can be produced due to the formation of impurities or defects created by radiation or similar bond-breaking processes of the dielectric (45,115). Approximately, these charges are fixed oxide charges and oxide trapped charges. These charges include positive charges closer to the gate dielectric/semicındcutor interface that is inside the gate dielectric layer. These charges are created due to the fabricating process of the stacked-NürFETs (34,37,38,44,58). The interaction of ionizing radiation with the dielectric oxide layer results in electron-decoupled pairs in the sensors, and negative charges with higher mobility related to positive charges simply transport to the gate terminal, avoiding the recombination or trapping process. In contrast, most of the positive charges are trapped in the defect centers in the device.

The sensitivities ($S = \Delta V_{th}$/applied dose) of the 100 nm SiO_2 Stacked-NürFETs are much higher than single SiO_2 NürFETs (5,8,9,12,14,20,25). The sensitivities values decreased with the increasing irradiation doses. An increase in the irradiation doses has caused an accumulation of oxide trapped charges, which leads to a decrement in the sensitivity (45,115). The obtained trapped charge densities increased with the increasing irradiation doses. This is due to a large number of the initial yield of holes and defects, whereby traps are generated.

The gamma irradiation effects on the electrical characteristics of 100 nm Er_2O_3 Stacked-NürFETs were obtained and investigated. The obtained threshold voltages shifted to the higher negative voltages with the increasing irradiation doses. The irradiation responses of the stacked-NürFETs sensors and the fundamental mechanisms of the irradiation-induced impacts depend on the generated number of defects and electrons – holes couples by irradiation. This arises due to the high mobility of electrons, which are easily depleted from the gate dielectric oxide layer, at the same time the holes present at the layer relocated to the oxide/semiconductor interface, where traps arose (45,115). These generated defects and traps due to the irradiation, bring about threshold voltages shifts as shown in Figures 7.5 and 7.8.

The interaction of ionizing radiation with the dielectric oxide layer results in electron-decoupled combinations in the devices, and negative charges with

higher mobility compared to positive charges easily transfer to the gate electrode, escaping the recombination or trapping progression. In contrast, most of the positive charges are trapped in the defect centers in the structure. As given in Table 8.2 the sensitivities (ΔV_{th}/applied dose) of the 100 Er_2O_3 nm Stacked-NürFETs are much higher than 100 nm SiO_2 NürFETs, this is due to the higher dielectric constant, thin films quality, and trapping efficiency of the Er_2O_3 dielectric oxide.

Table 8.2. Compared sensitivity (S) values of the stacked-NürFETs as a function of the applied radiation dose.

Dose (Gy)	SiO_2 2-NürFET S (mV/Gy)	Er_2O_3 2-NürFET S (mV/Gy)	SiO_2 4-NürFET S (mV/Gy)	Er_2O_3 4-NürFET S (mV/Gy)	SiO_2 8-NürFET S (mV/Gy)	Er_2O_3 8-NürFET S (mV/Gy)	SiO_2 12-NürFET S (mV/Gy)	Er_2O_3 12-NürFET S (mV/Gy)
0.5	41.20	**2286**	156.56	**2616.61**	262.26	**3095.09**	441.29	**4453.62**
1	72.90	**1222**	101.11	**1427.42**	151.15	**2037.04**	240.89	**2227.65**
2	49.95	**617**	81.58	**720.22**	93.09	**935.94**	140.18	**1164.29**
4	45.25	**315.50**	54.30	**381.13**	60.81	**588.34**	90.59	**658.59**
8	31.87	**160.87**	40.42	**196.32**	46.17	**211.96**	61.11	**324.17**
16	26.19	**86.44**	28.22	**105.17**	35.41	**77.27**	39.16	**183.07**
24	22.96	**63.50**	24.44	**76.20**	26.73	**66.45**	30.58	**110.11**
32	20.19	**49.13**	21.46	**53.46**	23.43	**58.37**	25.87	**89.82**
40	18.62	**40.08**	19.99	**49.53**	21.75	**52.38**	23.43	**69.43**
48	17.52	**34.96**	18.49	**39.25**	20.19	**49.84**	21.28	**63.41**

The radiation responses of the stacked-NürFETs sensors vary from the linearity on account of the increased electric field shielding effect after a certain dose value, depending on the oxide dielectric materials, dielectric thickness, type, and energy of the applied radiation dose. The sensitivities values decreased with the increasing irradiation doses. An increase in the irradiation doses has caused an accumulation of oxide trapped charges, which leads to a decrement in the sensitivity. The obtained trapped charge densities increased with the increasing irradiation doses. This is due to a large number of the initial generated holes and defects, whereby traps are generated.

The irradiation generated oxide trapped charge and interface trapped charge densities for both SiO_2 and Er_2O_3 stacked-NürFETs improved with increasing irradiation doses. It is observed that the obtained trapped charges are positive for both oxide and the interface layers. Furthermore, a large number of oxide trapped charges are observed compared to interface trapped as given in Tables 8.3 and 8.4. This shows that oxide trapped charges are dominants for the V_{th} shifts. Besides, obtained both types of trapped charges are higher in the Er_2O_3 stacked-NürFETs as seen in the compared oxide trapped charge densities of the stacked-NürFETs as a function of the applied radiation dose and compared interface trapped charge densities of the stacked-NürFETs as a function of the applied radiation dose.

These results have shown that the sensitivities increase with the increasing number of NürFET in the stacked-NürFETs sensors. However, the sensitivities did not increase in direct proportion to the applied radiation doses to the stacked-NürFETs sensors. This is due to the width and length of the current-conducting channels. Eventually, when the drain voltage keeps increasing, it reaches a saturation state, at which the channel thickness reduces to zero. In this case, the pinch-off point is observed. The drain current does not change above the pinch – point, it almost remains the same. The applied gate voltage is higher than the saturated voltage, and the saturated voltage remains constant. Therefore, the number of carriers coming from the source and the current flowing between the source and drain remains the same, which indicates the saturation region is reached in the device. Therefore, the drain current will remain constant no matter how the drain

voltage increases. Here the significant factor is the channel length and the channel width (2,44,58).

Table 8.3. Compared Oxide Trapped Charge Densities of the Stacked-NürFETs as a Function of the Applied Radiation Dose.

Dose (Gy)	SiO_2 2-NürFET N_{ot} (cm^{-2})	Er_2O_3 2-NürFET N_{ot} (cm^{-2})	SiO_2 4-NürFET N_{ot} (cm^{-2})	Er_2O_3 4-NürFET N_{ot} (cm^{-2})	SiO_2 8-NürFET N_{ot} (cm^{-2})	Er_2O_3 8-NürFET N_{ot} (cm^{-2})	SiO_2 12-NürET N_{ot} (cm^{-2})	Er_2O_3 12-NürET N_{ot} (cm^{-2})
0.5	5.10×10^{9}	**8.83×10^{11}**	1.59×10^{10}	**1.01×10^{12}**	2.64×10^{10}	**9.25×10^{11}**	4.71×10^{10}	**1.74×10^{12}**
1	1.53×10^{10}	**9.43×10^{11}**	2.19×10^{10}	**1.11×10^{12}**	3.52×10^{10}	**9.56×10^{11}**	5.18×10^{10}	**1.76×10^{12}**
2	2.17×10^{10}	**9.54×10^{11}**	3.38×10^{10}	**1.12×10^{12}**	3.96×10^{10}	**1.19×10^{12}**	5.97×10^{10}	**1.82×10^{12}**
4	3.95×10^{10}	**9.78×10^{11}**	4.77×10^{10}	**1.18×10^{12}**	5.27×10^{10}	**1.23×10^{12}**	7.70×10^{10}	**2.02×10^{12}**
8	5.48×10^{10}	**9.93×10^{11}**	6.95×10^{10}	**1.22×10^{12}**	7.91×10^{10}	**1.31×10^{12}**	1.06×10^{11}	**2.06×10^{12}**
16	9.05×10^{10}	**1.07×10^{12}**	9.73×10^{10}	**1.31×10^{12}**	1.19×10^{11}	**1.44×10^{12}**	1.34×10^{11}	**2.17×10^{12}**
24	1.19×10^{11}	**1.18×10^{12}**	1.27×10^{11}	**1.32×10^{12}**	1.36×10^{11}	**1.58×10^{12}**	1.57×10^{11}	**2.23×10^{12}**
32	1.39×10^{11}	**1.22×10^{12}**	1.47×10^{11}	**1.42×10^{12}**	1.58×10^{11}	**1.62×10^{12}**	1.78×10^{11}	**2.29×10^{12}**
40	1.55×10^{11}	**1.24×10^{12}**	1.71×10^{11}	**1.46×10^{12}**	1.85×10^{11}	**1.82×10^{12}**	2.01×10^{11}	**2.33×10^{12}**
48	1.73×10^{11}	**1.30×10^{12}**	1.91×10^{11}	**1.53×10^{12}**	2.07×10^{11}	**1.86×10^{12}**	2.19×10^{11}	**2.40×10^{12}**

Table 8.4. Compared Interface Trapped Charge Densities of the Stacked-NürFETs as a Function of the Applied Radiation Dose.

Dose (Gy)	SiO_2 2-NürFET N_{it} (cm^{-2})	Er_2O_3 2-NürFET N_{it} (cm^{-2})	SiO_2 4-NürFET N_{it} (cm^{-2})	Er_2O_3 4-NürFET N_{it} (cm^{-2})	SiO_2 8-NürFET N_{it} (cm^{-2})	Er_2O_3 8-NürFET N_{it} (cm^{-2})	SiO_2 12-NürET N_{it} (cm^{-2})	Er_2O_3 12-NürET N_{it} (cm^{-2})
0.5	6.66×10^{8}	$\mathbf{1.55 \times 10^{9}}$	9.42×10^{8}	$\mathbf{1.79 \times 10^{9}}$	1.81×10^{9}	$\mathbf{2.73 \times 10^{11}}$	2.90×10^{8}	$\mathbf{1.64 \times 10^{10}}$
1	3.65×10^{8}	$\mathbf{3.10 \times 10^{9}}$	1.07×10^{8}	$\mathbf{4.31 \times 10^{9}}$	2.65×10^{9}	$\mathbf{6.23 \times 10^{11}}$	6.66×10^{7}	$\mathbf{3.97 \times 10^{10}}$
2	1.93×10^{8}	$\mathbf{1.55 \times 10^{9}}$	1.33×10^{9}	$\mathbf{1.98 \times 10^{9}}$	4.70×10^{8}	$\mathbf{2.54 \times 10^{11}}$	5.72×10^{8}	$\mathbf{1.97 \times 10^{10}}$
4	5.80×10^{8}	$\mathbf{1.56 \times 10^{9}}$	9.63×10^{8}	$\mathbf{1.92 \times 10^{9}}$	4.43×10^{8}	$\mathbf{5.92 \times 10^{11}}$	9.14×10^{8}	$\mathbf{2.12 \times 10^{10}}$
8	2.15×10^{7}	$\mathbf{3.10 \times 10^{9}}$	4.30×10^{6}	$\mathbf{4.41 \times 10^{8}}$	3.16×10^{8}	$\mathbf{2.87 \times 10^{9}}$	1.57×10^{8}	$\mathbf{5.39 \times 10^{10}}$
16	3.87×10^{8}	$\mathbf{3.87 \times 10^{9}}$	2.69×10^{8}	$\mathbf{1.79 \times 10^{9}}$	3.17×10^{9}	$\mathbf{4.85 \times 10^{11}}$	1.14×10^{9}	$\mathbf{1.01 \times 10^{11}}$
24	1.31×10^{9}	$\mathbf{1.55 \times 10^{9}}$	1.01×10^{9}	$\mathbf{9.43 \times 10^{10}}$	1.73×10^{9}	$\mathbf{3.42 \times 10^{11}}$	6.47×10^{8}	$\mathbf{1.82 \times 10^{11}}$
32	2.15×10^{7}	$\mathbf{7.74 \times 10^{8}}$	6.64×10^{8}	$\mathbf{9.47 \times 10^{10}}$	3.02×10^{9}	$\mathbf{1.76 \times 10^{11}}$	4.60×10^{8}	$\mathbf{5.33 \times 10^{10}}$
40	4.90×10^{9}	$\mathbf{3.87 \times 10^{9}}$	1.14×10^{9}	$\mathbf{7.35 \times 10^{10}}$	2.47×10^{9}	$\mathbf{2.02 \times 10^{11}}$	3.98×10^{8}	$\mathbf{1.81 \times 10^{11}}$
48	7.69×10^{9}	$\mathbf{3.10 \times 10^{9}}$	4.08×10^{9}	$\mathbf{7.44 \times 10^{10}}$	1.82×10^{9}	$\mathbf{3.63 \times 10^{9}}$	1.15×10^{9}	$\mathbf{3.82 \times 10^{10}}$

The outcomes have shown that the fabricated Stacked-NürFETs can be future p-MOS-based radiation sensors. However, improvements in fabrication stages and comprehensive investigations need to be performed to develop and enhance the reliability of the devices. Further actions and additional scientific

studies should be done to address what this study could not achieve and explain: The gate channel length/width ratio can be used to reduce the external voltage electric field shielding effect to be applied to the sensor during irradiation. During irradiation, the terminals of the stacked-NürFETs were short-circuited, irradiation connection and read-out configuration will improve the performance of the device. And with external bias voltage, the linearity and the sensitivity of the stacked-NürFETs will be improved.

9. CONCLUSIONS AND RECOMMENDATIONS

The p-MOS sensors in the stacked structure (stacked-NürFETs) whereby multiple p-channel MOSFETs are interconnected in one chip were fabricated and characterized. The fabricated stacked-NürFETs are silicon-based NürFETs with 100 nm SiO_2 and 100 nm Er_2O_3 gate dielectrics oxides optimized for radiation sensitivity. Characterizations and relevant measurement analysis of the gate dielectric oxides were investigated. After the initial device assessment, the device performance and possible degradation mechanism in the radiation environment have been also discussed. The major conclusions and recommendations obtained from this study are listed below:

1. The obtained initial threshold voltages shifted to the higher negative voltages with the increasing number of NürFETs in the stacked-NürFETs. It is observed that the initial threshold voltage moves towards higher negative voltage values due to the increasing number of sensors in the 100 nm SiO_2 Stacked-NürFETs. It is observed that as the number of NürFETs in the Stacked-NüeFETs increases, the number of charges trapped at the interface and oxide layer increases. Therefore, larger values of negative gate voltage, which are required to allow current to flow between source and drain are observed.

2. The obtained threshold voltages shifted to the higher negative voltages with the increasing irradiation doses. The irradiation responses of the Stacked-NürFETs sensors and the fundamental mechanisms of the irradiation-induced impacts depend on the generated number of defects and electrons – holes pairs by irradiation. This occurs due to the high mobility of electrons, which are easily depleted from the gate dielectric oxide layer, at the same time the holes present at the layer moved to the oxide/semiconductor interface, where traps occurred. These generated defects and traps due to the irradiation bring about threshold voltages shifts as shown in the obtained I – V measurements.

3. The V_{th} values shifted toward more negative voltages for both Er_2O_3 and SiO_2 stacked-NürFETs, due to the accumulation of positive trapped charges.

The obtained sensitivities of Er_2O_3 stacked-NürFETs are significantly higher than SiO_2 stacked-NürFETs. The sensitivities of the 100 Er_2O_3 nm Stacked-NürFETs are much higher than 100 nm SiO_2 NürFETs, this is due to the higher dielectric constant, thin-film quality, and trapping efficiency of the Er_2O_3 gate dielectric oxide. The results showed that the sensitivities of the Stacked-NürFETs are directly proportional to the number of sensors used in the structures. Also, the higher positive charge trapped densities have been observed in the Er_2O_3 Er_2O_3 stacked-NürFETs compared to SiO_2 stacked-NürFETs as expected.

4. The sensitivities values for both Er_2O_3 and SiO_2 stacked-NürFETs decreased with the increasing irradiation doses. The obtained trapped charge densities increased with the increasing irradiation doses. This is due to a large number of the initial yield of holes and defects, whereby traps are generated.

5. These initial results are demanding for the possible usage of Er_2O_3 and SiO_2 stacked-NürFETs to be used in P-MOS dosimeters as new MOS-based radiation sensors. The observed remarkable rise in the sensitivities of the devices can be a milestone for the improvement of the p-MOS dosimeters, and the results have also shown that the fabricated Stacked-NürFETs can be future p-MOS radiation sensors. However, further actions and additional scientific studies should be done to address what this study could not achieve and explain; improvements in fabrication stages and comprehensive investigations need to be performed to develop and enhance the reliability of the devices.

10. REFERENCES

Vancouver citation system was used in this thesis.

1. Lane W, Microe N, Adams L. Performance of Stacked PMOS Dosimeters under Bulk Bias for Use in Realtime Radiation Dosimetry. :10–3.

2. Holmes-Siedle A, Adams L. RADFET: A review of the use of metal-oxide-silicon devices as integrating dosimeters. Int J Radiat Appl Instrumentation Part. 1986;28(2):235–44.

3. Ilić S, Jevtić A, Stanković S, Ristić G. Floating-gate MOS transistor with dynamic biasing as a radiation sensor. Sensors (Switzerland). 2020;20(11):1–28.

4. Pon A, Tulasi KSVP, Ramesh R. Effect of interface trap charges on the performance of asymmetric dielectric modulated dual short gate tunnel FET. Vol. 102, AEU - International Journal of Electronics and Communications. 2019. p. 1–8.

5. Kaya S, Jaksic A, Duane R, Vasovic N, Yilmaz E. FET-based radiation sensors with Er2O3 gate dielectric. Nucl Instruments Methods Phys Res Sect B Beam Interact with Mater Atoms [Internet]. 2018;430(June):36–41. Available from: https://doi.org/10.1016/j.nimb.2018.06.007

6. Mah SK, Ahmad I, Ker PJ, Tan KP, Faizah ZAN. Modeling, simulation and optimization of 14nm high-K/metal gate NMOS with taguchi method. IEEE Int Conf Semicond Electron Proceedings, ICSE. 2018;2018-Augus:275–8.

7. Wang J, Li B, Huang Y, Zhao K, Yu F, Zheng Q, et al. The total ionizing dose response of leading-edge FDSOI MOSFETs. Microelectron Reliab. 2018;88–90(July):979–83.

8. Kaya S, Jaksic A, Yilmaz E. Co-60 gamma irradiation effects on electrical characteristics of HfO2 MOSFETs and specification of basic radiation- induced degradation mechanism. Radiat Phys Chem. 2018;149(March):7–13.

9. Dubey A, Singh A, Narang R, Saxena M, Gupta M. Modeling and Simulation of Junctionless Double Gate Radiation Sensitive FET (RADFET) Dosimeter. IEEE Trans Nanotechnol. 2018;17(1):49–55.

10. Pejović MM, Pejović SM. VDMOSFET as a prospective dosimeter for radiotherapy. Appl Radiat Isot. 2018;132(October 2017):1–5.

11. Carvajal MA, Escobedo P, Jiménez-Melguizo M, Martínez-García MS, Martínez-Martí F, Martínez-Olmos A, et al. A compact dosimetric system for MOSFETs based on passive NFC tag and smartphone. Sensors Actuators, A Phys [Internet]. 2017;267:82–9. Available from: http://dx.doi.org/10.1016/j.sna.2017.10.015

12. Yilmaz E, Kahraman A, McGarrigle AM, Vasovic N, Yegen D, Jaksic A. Investigation of RadFET response to X-ray and electron beams. Appl Radiat Isot [Internet]. 2017;127(July 2016):156–60. Available from: http://dx.doi.org/10.1016/j.apradiso.2017.06.004

13. Egner B V., Holland DE, Burggraf LW, Bevins JE. Development of a modular mixed-radiation directional rotating scatter mask detection system. Nucl Instruments Methods Phys Res Sect A Accel Spectrometers, Detect Assoc Equip [Internet]. 2021;987(November 2020):164820. Available from: https://doi.org/10.1016/j.nima.2020.164820

14. KAHRAMAN A, YILMAZ E. Farklı kapı oksitli RadFET dozimetrelerinin ışınlama öncesi elektriksel karakterizasyonlarının TCAD simülasyon programı ile değerlendirilmesi. SAÜ Fen Bilim Enstitüsü Derg. 2017;21(6):1–1.

15. Martínez-García MS, del Río JT, Jaksic A, Banqueri J, Carvajal MA. Response to ionizing radiation of different biased and stacked pMOS structures. Sensors Actuators, A Phys [Internet]. 2016;252:67–75. Available from: http://dx.doi.org/10.1016/j.sna.2016.11.007

16. Falke P, Fischer HH, Seidensticker KJ, Thiel K, Fischer H, Hilchenbach M, et al. Cosmic ray dose monitoring using RadFET sensors of the Rosetta instruments SESAME and COSIMA. Acta Astronaut [Internet]. 2016;125:22–9. Available from: http://dx.doi.org/10.1016/j.actaastro.2016.03.001

17. Carvajal MA, Martínez-García MS, Guirado D, Banqueri J, Palma AJ. Dose verification system based on MOS transistor for real-time measurement. Sensors Actuators, A Phys [Internet]. 2016;247:269–76. Available from: http://dx.doi.org/10.1016/j.sna.2016.06.009

18. Pershenkov VS, Bakerenkov AS, Felitsyn VA, Rodin AS, Telets VA, Belyakov V V. ELDRS in SiGe transistors for room and low-temperature irradiation. Microelectron Reliab [Internet]. 2016;63:56–9. Available from: http://dx.doi.org/10.1016/j.microrel.2016.05.010

19. Zheng Y, Shi W, Wang M, Liu H. N-RADFET will able to replace P-RADFET. Int J Appl Res. 2016;2(5):958–60.

20. Kahraman A, Kaya S, Jaksic A, Yilmaz E. A comprehensive study on the photon energy response of RadFET dosimeters using the PENELOPE Monte Carlo code. Radiat Eff Defects Solids. 2015;170(5):367–76.

21. Wong H, Iwai H. On the scaling of subnanometer EOT gate dielectrics for ultimate nano CMOS technology. Microelectron Eng [Internet]. 2015;138:57–76. Available from: http://dx.doi.org/10.1016/j.mee.2015.02.023

22. Andjelković MS, Ristić GS, Jakšić AB. Using RADFET for the real-time measurement of gamma radiation dose rate. Meas Sci Technol. 2015;26(2).

23. Pejović MM. Dose response, radiation sensitivity and signal fading of p-channel MOSFETs (RADFETs) irradiated up to 50 Gy with 60Co. Appl Radiat Isot. 2015;104:100–5.

24. Jingar N, Khandelwal A, Pandya A. Design of programmable current source for MOSFET based gamma dosimetry system. Nucl Instruments Methods Phys Res Sect A Accel Spectrometers, Detect Assoc Equip [Internet]. 2021;990(November 2020):164944. Available from: https://doi.org/10.1016/j.nima.2020.164944

25. Kahraman A, Yilmaz E, Kaya S, Aktag A. Effects of packing materials on the sensitivity of RadFET with HfO2 gate dielectric for electron and photon sources. Radiat Eff Defects Solids [Internet]. 2015;170(10):832–44. Available from: https://doi.org/10.1080/10420150.2015.1118689

26. Martínez-García MS, Simancas F, Palma AJ, Lallena AM, Banqueri J, Carvajal MA. General purpose MOSFETs for the dosimetry of electron beams used in intra-operative radiotherapy. Sensors Actuators, A Phys [Internet]. 2014;210:175–81. Available from: http://dx.doi.org/10.1016/j.sna.2014.02.019

27. Pejovic MM, Pejovic MM, Jaksic AB. Contribution of fixed oxide traps to sensitivity of pMOS dosimeters during gamma ray irradiation and annealing at room and elevated temperature. Sensors Actuators, A Phys [Internet]. 2012;174(1):85–90. Available from: http://dx.doi.org/10.1016/j.sna.2011.12.011

28. Pejović MM, Pejović SM, Dolićanin EĆ, Lazarević D. Gamma-ray irradiation and post-irradiation at room and elevated temperature response of pMOS dosimeters with thick gate oxides. Nucl Technol Radiat Prot. 2011;26(3):261–5.

29. Ristić GS, Vasović ND, Kovačević M, Jakšić AB. The sensitivity of 100 nm RADFETs with zero gate bias up to dose of 230 Gy(Si). Nucl Instruments Methods Phys Res Sect B Beam Interact with Mater Atoms. 2011;269(23):2703–8.

30. Carvajal MA, Vilches M, Guirado D, Lallena AM, Banqueri J, Palma AJ. Readout techniques for linearity and resolution improvements in MOSFET dosimeters. Sensors Actuators, A Phys. 2010;157(2):178–84.

31. Manigandan D, Bharanidharan G, Aruna P, Devan K, Elangovan D, Patil V, et al. Dosimetric characteristics of a MOSFET dosimeter for clinical electron beams. Phys Medica [Internet]. 2009;25(3):141–7. Available from: http://dx.doi.org/10.1016/j.ejmp.2008.11.003

32. Gopiraj A, Billimagga RS, Ramasubramanian V. Performance characteristics and commissioning of MOSFET as an in-vivo dosimeter for high energy photon external beam radiation therapy. Reports Pract Oncol Radiother [Internet]. 2008;13(3):114–25. Available from: http://dx.doi.org/10.1016/S1507-1367(10)60001-6

33. Ravotti F, Glaser M, Moll M, Ilgner C, Camanzi B, Holmes-Siedle AG. Response of RadFET dosimeters to high fluences of fast neutrons. IEEE Nucl Sci Symp Conf Rec. 2004;1(August):335–9.

34. Jaksic A, Ristic G, Pejovic M, Mohammadzadeh A, Sudre C, Lane W. Gamma-ray irradiation and post-irradiation responses of high dose range RADFETs. Proc Eur Conf Radiat its Eff Components Syst RADECS. 2002;1(2):57–65.

35. Baader JE, Anderson SD. A custom high-stability pulse generator for the test of a novel in-situ magnetic sensor developed to detect radiation damage in undulators. Nucl Instruments Methods Phys Res Sect A Accel Spectrometers, Detect Assoc Equip [Internet]. 2021;985(August 2020):164633. Available from: https://doi.org/10.1016/j.nima.2020.164633

36. Jaksic A, Ristic G, Pejovic M, Mohammadzadeh A, Lane W. Characterisation of radiation response of 400 nm implanted gate oxide RADFETs. 2002 23rd Int Conf Microelectron MIEL 2002 - Proc. 2002;2(Miel):727–30.

37. Buehler M, Holmes-Siedle A, Caines C, Carmichael C, Martin D. Stacked p-FET dosimeter for the STRV-2 MWIR detector. IEEE Trans Nucl Sci. 1996;43(6 PART 1):2679–86.

38. Karlsson PR, Jeppson KO. An efficient method for determining threshold voltage, series resistance and effective geometry of MOS transistors. IEEE Trans Semicond Manuf. 1996;9(2):215–22.

39. Marzo M, Alia RG, Infantino A, Brucoli M, Danzeca S. Impact of neutrons on the RadFET dose response when exposed to mixed-fields. Radiat Phys Chem [Internet]. 2021;179(July 2017):108062. Available from: https://doi.org/10.1016/j.radphyschem.2018.11.016

40. Ge H, Zhang EX, Chen J, Xu L, Wang S, Chai Z, et al. Comparing the TID-induced RF performance degradation of floating body and body contacted 130 nm SOI NMOS transistors. Microelectron Reliab [Internet]. 2020;104(May 2019):113547. Available from: https://doi.org/10.1016/j.microrel.2019.113547

41. Kramberger G, Ambrožič K, Gürer U, Hiti B, Karacali H, Mandić I, et al. Development of MOS-FET dosimeters for use in high radiation fields. Nucl Instruments Methods Phys Res Sect A Accel Spectrometers, Detect Assoc Equip [Internet]. 2020;978(March):164283. Available from: https://doi.org/10.1016/j.nima.2020.164283

42. Tekin N, Sarimli F, Sezer ZA, Yilmaz E. Electronic Reader Design With Radfet (Pmosfet) Dosimeter Sensor. 2020;(February).

43. Express AP. Interface and electrical properties of buried InGaAs channel MOSFET with an InP barrier layer and Al2O3/HfO2/Al2O3 gate dielectrics. 2020;13.

44. Kelleher A, Lane W, Adams L, Member S. PMOS Dosimeters : The Stacked RADFET Approach. 1995;42(1):48–51.

45. Knoll GF, Kraner HW. Radiation Detection and Measurement. Vol. 69, Proceedings of the IEEE. 1981. 495 p.

46. Demkov AA, Posadas AB. Integration of Functional Oxides with Semiconductors. Integration of Functional Oxides with Semiconductors. 2014. 1–278 p.

47. Patil KC, Hegde MS, Rattan T, Aruna ST. Chemistry of Nanocrystalline Oxide Materials. Chemistry of Nanocrystalline Oxide Materials. 2008.

48. Oktyabrsky S, Ye PD. Fundamentals of III-V semiconductor MOSFETs. Fundamentals of III-V Semiconductor MOSFETs. 2010. 1–445 p.

49. Plieth W. Electrochemistry for Materials Science. Electrochemistry for Materials Science. 2008.

50. Gaur A, Agarwal T, Asselberghs I, Radu I, Heyns M, Lin D. A MOS capacitor model for ultra-thin 2D semiconductors: The impact of interface defects and channel resistance. 2D Mater. 2020;7(3).

51. Kong D, Nishio K, Kurosawa MK. Surface acoustic wave propulsion system with acoustic radiation force. Vol. 309, Sensors and Actuators, A: Physical. 2020.

52. Cao S rui, Ke X yu, Ming S ting, Wang D wei, Li T, Liu B yan, et al. Study of γ-ray radiation influence on SiO2/HfO2/Al2O3/HfO2/Al2O3 memory capacitor by C–V and DLTS. J Mater Sci Mater Electron. 2019;30(12):11079–85.

53. Pejović MM. Processes in radiation sensitive MOSFETs during irradiation and post irradiation annealing responsible for threshold voltage shift. Radiat Phys Chem. 2017;130:221–8.

54. WILLIAM D. CALLISTER J, DAVID G. RETHWISCH. Fundamentals Materials science and Engineering : An Integrated Approach. Fundam Mater Sci Eng AN Integr APPROACH [Internet]. 2015;(5th Edition):1–964. Available from: 9781119230403

55. Sze, S. M. and Lee MK. Semiconductor Devices Physics and Technology. Vol. 53, JOHN WILEY & SONS, INC. 2012. 578 p.

56. L. Wang, J. Tang, Q.A. Huang, Gamma and electron beam irradiation effects on the resistance of micromachined polycrystalline silicon beams, Sensors Actuators, A Phys. 177 (2012) 99–104. doi:10.1016/j.sna.2012.01.028.

57. Connell BO. optimized Stacked RADFETs for milli-rad Dose Measurement.

58. O'Connell B, Kellehei A, Lane W, Adams L. Stacked RADFETs for increased radiation sensitivity. IEEE Trans Nucl Sci. 1996;43(3 PART 1):985–90.

59. Zhuiykov S. Nanostructured Semiconductor Oxides for the Next Generation of Electronics and Functional Devices. Nanostructured Semiconductor Oxides for the Next Generation of Electronics and Functional Devices. 2013. 1–439 p.

60. Abubakar S, Yilmaz E. Effects of series resistance and interface state on electrical properties of Al/Er2O3/Eu2O3/SiO2/n-Si/Al MOS capacitors. Vol. 232, Microelectronic Engineering. 2020.

61. Gumrukcu AE, Kaplan H, Akin Sonmez N, Ozcelik S. Electrical, optical and structural properties of silver-based multilayer films deposited by magnetron sputtering. J Mater Sci Mater Electron. 2019;30(20):18519–23.

62. Scarafagio M, Tallaire A, Tielrooij KJ, Cano D, Grishin A, Chavanne MH, et al. Ultrathin Eu- and Er-Doped Y2O3 Films with Optimized Optical Properties for Quantum Technologies. J Phys Chem C. 2019;123(21):13354–64.

63. Abubakar S, Yilmaz E. Optical and electrical properties of E-Beam deposited TiO2/Si thin films. J Mater Sci Mater Electron. 2018;29(12):9879–85.

64. Kahraman A, Gurer U, Lok R, Kaya S, Yilmaz E. Impact of interfacial layer using ultra-thin SiO2 on electrical and structural characteristics of Gd2O3 MOS capacitor. J Mater Sci Mater Electron [Internet]. 2018;29(20):17473–82. Available from: http://dx.doi.org/10.1007/s10854-018-9847-9

65. Miura-Mattausch M, Mattausch H. The physics and modeling of MOSFETS: surface-potential model HiSIM [Internet]. Engineering. 2008. Available from: http://books.google.com/books?hl=en&lr=&id=q5vK3B0adloC&oi=fnd&pg=PR5&dq=The+Physics+and+Modeling+of+MOSFETs&ots=-oUhrzeRJq&sig=foHVRMNQsk0nk6jHEuoPBrnsATg

66. Sze SM, Ng KK. Physics of Semiconductor Devices: Third Edition. Physics of Semiconductor Devices: Third Edition. 2006. 1–815 p.

67. Jha AR. Rare earth materials: Properties and applications. Rare Earth Materials: Properties and Applications. 2014. 1–332 p.

68. Pergament A. Oxide electronics and functional properties of transition metal oxides. Oxide Electronics and Functional Properties of Transition Metal Oxides. 2014. 1–242 p.

69. Adamu-Lema F. Scaling and intrinsic parameter fluctuations in nano-CMOS devices. 2005;

70. Li S, Wu Y, Li G, Yu H, Fu K, Wu Y, et al. Ta-doped modified Gd2O3 film for a novel high k gate dielectric. Vol. 35, Journal of Materials Science and Technology. 2019. p. 2305–11.

71. Abubakar S, Kaya S, Aktag A, Yilmaz E. Yttrium oxide nanostructured thin films deposited by radio frequency sputtering: the annealing optimizations and correlations between structural, morphological, optical and electrical properties. J Mater Sci Mater Electron. 2017;28(18):13920–7.

72. Kahraman A, Yilmaz E, Kaya S, Aktag A. Effects of post deposition annealing, interface states and series resistance on electrical characteristics of HfO2 MOS capacitors. J Mater Sci Mater Electron. 2015;26(11):8277–84.

73. Robertson J, Wallace RM. High-K materials and metal gates for CMOS applications. Mater Sci Eng R Reports [Internet]. 2015;88:1–41. Available from: http://dx.doi.org/10.1016/j.mser.2014.11.001

74. Mudavakkat VH, Atuchin V V., Kruchinin VN, Kayani A, Ramana C V. Structure, morphology and optical properties of nanocrystalline yttrium oxide (Y2O3) thin films. Opt Mater (Amst) [Internet]. 2012;34(5):893–900. Available from: http://dx.doi.org/10.1016/j.optmat.2011.11.027

75. He G, Zhu L, Sun Z, Wan Q, Zhang L. Integrations and challenges of novel high-k gate stacks in advanced CMOS technology. Prog Mater Sci [Internet]. 2011;56(5):475–572. Available from: http://dx.doi.org/10.1016/j.pmatsci.2011.01.012

76. Oka R, Yamamoto K, Akamine H, Wang D, Nakashima H, Hishiki S, et al. High interfacial quality metal-oxide-semiconductor capacitor on (111) oriented 3C-SiC with Al2O3 interlayer and its internal charge analysis. Jpn J Appl Phys. 2020;59(SG).

77. Kang M, Yang HI, Choi W. Electrical properties of Al2O3/WSe2interface based on capacitance-voltage characteristics. J Phys D Appl Phys. 2020;53(32).

78. Lok R, Budak E, Yilmaz E. Structural characterization and electrical properties of Nd2O3 by sol–gel method. J Mater Sci Mater Electron [Internet]. 2020;31(4):3111–8. Available from: https://doi.org/10.1007/s10854-020-02857-2

79. Kahraman A, Karacali H, Yilmaz E. Impact and origin of the oxide-interface traps in Al/Yb2O3/n-Si/Al on the electrical characteristics. J Alloys Compd [Internet]. 2020;825:154171. Available from: https://doi.org/10.1016/j.jallcom.2020.154171

80. Kahraman A, Deevi SC, Yilmaz E. Influence of frequency and gamma irradiation on the electrical characteristics of Er2O3, Gd2O3, Yb2O3, and HfO2 MOS-based devices. Vol. 55, Journal of Materials Science. Springer US; 2020. p. 7999–8040.

81. Kahraman A, Yilmaz E. A comprehensive study on usage of Gd2O3 dielectric in MOS based radiation sensors considering frequency dependent radiation response. Radiat Phys Chem [Internet]. 2018;152(July):36–42. Available from: https://doi.org/10.1016/j.radphyschem.2018.07.017

82. Abubakar S, Kaya S, Karacali H, Yilmaz E. The gamma irradiation responses of yttrium oxide capacitors and first assessment usage in radiation sensors. Sensors Actuators, A Phys [Internet]. 2017;258:44–8. Available from: http://dx.doi.org/10.1016/j.sna.2017.02.022

83. Salomone LS, Lipovetzky J, Carbonetto SH, García Inza MA, Redin EG, Campabadal F, et al. Deep electron traps in HfO2-based metal-oxide-semiconductor capacitors. Thin Solid Films [Internet]. 2016;600:36–42. Available from: http://dx.doi.org/10.1016/j.tsf.2016.01.007

84. Mishra M, Kuppusami P, Ramya S, Ganesan V, Singh A, Thirumurugesan R, et al. Microstructure and optical properties of Gd2O3 thin films prepared by pulsed laser deposition. Surf Coatings Technol [Internet]. 2015;262:56–63. Available from: http://dx.doi.org/10.1016/j.surfcoat.2014.12.012

85. Kimbugwe NT, Yilmaz E. Impact of SiO2 interfacial layer on the electrical characteristics of Al/Al2O3/SiO2/n-Si metal–oxide–semiconductor capacitors. J Mater Sci Mater Electron [Internet]. 2020;(0123456789). Available from: https://doi.org/10.1007/s10854-020-03783-z

86. Fleetwood DM. Border traps and bias-temperature instabilities in MOS devices. Microelectron Reliab [Internet]. 2018;80(July):266–77. Available from: http://dx.doi.org/10.1016/j.microrel.2017.11.007

87. Purohit A, Chander S, Dhaka MS. Impact of annealing on physical properties of e-beam evaporated polycrystalline CdO thin films for optoelectronic applications. Vol. 66, Optical Materials. 2017. p. 512–8.

88. Kahraman A, Gurer U, Yilmaz E. The effect and nature of the radiation induced oxide-interface traps on the performance of the Yb2O3 MOS device. Radiat Phys Chem [Internet]. 2020;177(August):109135. Available from: https://doi.org/10.1016/j.radphyschem.2020.109135

89. Bera MK, Ahmet P, Kakushima K, Tsutsui K, Sugii N, Nishiyama A, et al. Electrical Properties of Yttrium-Titanium Oxide High-k Gate Dielectric on Ge. ECS Trans. 2019;33(6):275–84.

90. Jha AR. A.r. jha. 2012. 401 p.

91. Maiti CK, Armstrong GA. SOI MOSFETs. Technology Computer Aided Design for Si, SiGe and GaAs Integrated Circuits. 2011. 153–194 p.

92. Metal Oxides. Fine Particles. 2020. 21–144 p.

93. Publications B, A Jorio; G Dresselhaus; M S Dresselhaus. Topics in Applied Physics Volume 111. Vol. 111. 2008. 264 p.

94. Ang DS, Gu CJ, Tung ZY, Boo AA, Gao Y. Evolution of oxide charge trapping under bias temperature stressing. Microelectron Reliab. 2014;54(4):663–81.

95. Khairnar AG, Mahajan AM. Effect of post-deposition annealing temperature on RF-sputtered HfO 2 thin film for advanced CMOS technology. Solid State Sci [Internet]. 2013;15:24–8. Available from: http://dx.doi.org/10.1016/j.solidstatesciences.2012.09.010

96. Kaya S, Yilmaz E. Modifications of structural, chemical, and electrical characteristics of Er2O3/Si interface under Co-60 gamma irradiation. Nucl Instruments Methods Phys Res Sect B Beam Interact with Mater Atoms [Internet]. 2018;418(September 2017):74–9. Available from: https://doi.org/10.1016/j.nimb.2018.01.010

97. Kaya S, Yıldız I, Lok R, Yılmaz E. Co-60 gamma irradiation influences on physical, chemical and electrical characteristics of HfO2/Si thin films. Radiat Phys Chem. 2018;150(April):64–70.

98. Kahraman A, Yilmaz E. Irradiation response of radio-frequency sputtered Al/Gd2O3/p-Si MOS capacitors. Radiat Phys Chem [Internet]. 2017;139(April):114–9. Available from: http://dx.doi.org/10.1016/j.radphyschem.2017.04.003

99. Kahraman A, Yilmaz E, Aktag A, Kaya S. Evaluation of Radiation Sensor Aspects of Er2O3 MOS Capacitors under Zero Gate Bias. IEEE Trans Nucl Sci. 2016;63(2):1284–93.

100. Kaya S, Yilmaz E, Kahraman A, Karacali H. Frequency dependent gamma-ray irradiation response of Sm2O3 MOS capacitors. Nucl Instruments Methods Phys Res Sect B Beam Interact with Mater Atoms [Internet]. 2015;358:188–93. Available from: http://dx.doi.org/10.1016/j.nimb.2015.06.037

101. Kaya S, Yilmaz E. Influences of Co-60 gamma-ray irradiation on electrical characteristics of Al2O3 MOS capacitors. J Radioanal Nucl Chem. 2014;302(1):425–31.

102. Kaya S, Aktag A, Yilmaz E. Effects of gamma-ray irradiation on interface states and series-resistance characteristics of BiFeO3 MOS capacitors. Nucl Instruments Methods Phys Res Sect B Beam Interact with Mater Atoms [Internet]. 2014;319:44–7. Available from: http://dx.doi.org/10.1016/j.nimb.2013.11.006

103. Kaya S, Yilmaz E. Use of BiFeO3 layer as a dielectric in MOS based radiation sensors fabricated on a Si substrate. Nucl Instruments Methods Phys Res Sect B Beam Interact with Mater Atoms [Internet]. 2014;319:168–70. Available from: http://dx.doi.org/10.1016/j.nimb.2013.10.016

104. Cheng Y, Ding M, Wu X, Liu X, Wu K. Irradiation effect of HfO2 MOS structure under gamma-ray. Proc IEEE Int Conf Solid Dielectr ICSD. 2013;764–7.

105. Wang L, Tang J, Huang QA. Gamma and electron beam irradiation effects on the resistance of micromachined polycrystalline silicon beams. Vol. 177, Sensors and Actuators, A: Physical. 2012. p. 99–104.

106. Ta MT, Briand D, Boudart B, Guhel Y. 60Co gamma irradiation effects on electrical characteristics of Al/Y2O3/n-Si/Al capacitors. Microelectron Eng [Internet]. 2010;87(11):2158–62. Available from: http://dx.doi.org/10.1016/j.mee.2010.01.018

107. The Co-60 gamma-ray irradiation effects on the Al_HfSiO4_p-Si_Al MOS capacitors.pdf.

108. Lok R, Budak E, Yilmaz E. Radiation response of zirconium silicate P-MOS capacitor. Vol. 109, Microelectronics Reliability. 2020. p. 113663.

109. Gurer U, Yilmaz O, Karacali H, Kaya S, Yilmaz E. Co-60 gamma radiation influences on the electrochemical, physical and electrical characteristics rare-earth dysprosium oxide (Dy2O3). Vol. 171, Radiation Physics and Chemistry. 2020.

110. de Araújo EP, Arantes AN, Costa IM, Chiquito AJ. Reliable Tin dioxide based nanowire networks as ultraviolet solar radiation sensors. Vol. 302, Sensors and Actuators, A: Physical. 2020.

111. Vavasour OJ, Jefferies R, Walker M, Roberts JW, Meakin NR, Gammon PM, et al. Effect of HCl cleaning on InSb-Al 2 O 3 MOS capacitors. Semicond Sci Technol. 2019;34(3):1301–5.

112. Kaya S, Abubakar S, Yilmaz E. Co-60 gamma irradiation influences on device characteristics of n-SnO 2 /p-Si heterojunction diodes. Nucl Instruments Methods Phys Res Sect B Beam Interact with Mater Atoms. 2019;445(February):63–8.

113. Afzali M, Mostafavi A, Shamspur T. Performance enhancement of perovskite solar cells by

rhenium doping in nano-TiO2 compact layer. Org Electron [Internet]. 2020;86(May):105907. Available from: https://doi.org/10.1016/j.orgel.2020.105907

114. Cantas A, Aygun G, Turan R. Impact of incorporated oxygen quantity on optical, structural and dielectric properties of reactive magnetron sputter grown high-κ HfO 2 /Hf/Si thin film. Appl Surf Sci [Internet]. 2014;318:199–205. Available from: http://dx.doi.org/10.1016/j.apsusc.2014.03.077

115. Gerhard Lutz. Semiconductor Radiation Detectors [Internet]. Vol. 5, Springer-Verlag Berlin Heidelberg New York. 2007. 1–353 p. Available from: http://www.elsevier.com/locate/scp

116. Pejović MM, Pejović MM, Nešic NT. RADFET as a sensor and dosimeter of gamma-ray irradiation. MIPRO 2012 - 35th Int Conv Inf Commun Technol Electron Microelectron - Proc. 2012;31–5.

117. Kaya S, Yilmaz E. A detailed study on frequency dependent electrical characteristics of MOS capacitors with dysprosium oxide gate dielectrics. Semicond Sci Technol. 2020;35(2).

118. Yalameha S, Nourbakhsh Z. Coexistence of type-I and critical-type nodal line states in intermetallic compounds ScM (M = Cu, Ag, Au). Supercond Sci Technol. 2020;33(5).

119. Omar R, Mohamed BA, Adel M. Effects of series and parallel resistances on the C-V characteristics of silicon-based metal oxide semiconductor (MOS) devices. Eur Phys J Plus. 2015;130(4).

120. Xiao H, Huang S. Frequency and voltage dependency of interface states and series resistance in Al/SiO2/p-Si MOS structure. Vol. 13, Materials Science in Semiconductor Processing. 2010. p. 395–9.

121. Kaya S, Yilmaz E. A comprehensive study on the frequency-dependent electrical characteristics of Sm2O3 MOS capacitors. IEEE Trans Electron Devices. 2015;62(3):980–7.

122. Ristić GS, Andjelković M, Jakšić AB. The behavior of fixed and switching oxide traps of RADFETs during irradiation up to high absorbed doses. Appl Radiat Isot. 2015;102:29–34.