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DESIGN OF FPGA BASED PLC AND ITS USE IN REMOTELY CONTROLLED INDUCTION MOTOR DRIVE

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Master's Thesis

Supervisor

Asst. Prof. Dr. Sefer KURNAZ

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ABSTRACT

DESIGN OF FPGA BASED PLC AND ITS USE IN REMOTELY CONTROLLED INDUCTION MOTOR DRIVE

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As a result of continuous development, the importance of variable speed drive has risen dramatically in recent years. Over time, the demand for modular and more standardized drive has increased. Thyristor technology, high-speed digital switching systems, microprocessors, Programmable Logic Controller (PLC), microcomputers, and microcontrollers have all contributed to the popularity of drive technology. High-performance and reliable drives are already being used with advanced technology. Drives frameworks with low power utilization and little size are popular today to satisfy the needs of high voltage, minimal expense execution, and remote observing through information procurement frameworks. A significant initial phase in creating complex plan and control techniques for remote-found drives has been made with the present PLC framework. Enlistment engine boundaries will be digitalized with high exactness and speed utilizing the proposed framework's re-configurable programmable gadgets and Simple to Computerized Converters with sufficient transformation speed. FPGA will be utilized for LCD connect with the FPGA to show different engine boundaries utilizing the simultaneously working model that will be assembled. When it comes to implementing the VHDL-coded hardware modules, the FPGA will be employed by Xilinx.

Keywords: Programmable Logic Controller (PLC), AC Motor Drive, FPGA.

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ABBREVIATIONS

PMSM : Permanent Magnet Synchronous Motors

IM : Induction Motors

MIMO : Multiple-Input Multiple Output

PC : Personal Computer

XSG : Xilinx System Generator

FPGA : Field Programmable Gate Ar

1. INTRODUCTION

Acceptance Engines and Super durable magnet simultaneous engines have higher effectiveness and power/size proportions than customary DC engines, which were broadly utilized for delivering mechanical energy in the robotization business, transportation, and different ventures. Mechanical commutations are not required for AC motors. The absence of mechanical commutation results in a simple physical structure and reliable operation. As a result, AC motors require less maintenance and are more reliable.

The numerical demonstrating of AC engines, then again, is nonlinear Numerous Information Various Result. It makes control and advancement more troublesome. Besides, more computational execution is expected for the viable execution of control calculations. These difficulties arouse the curiosity of modern and scholastic exploration networks to examine groundbreaking thoughts and strategies to find arrangements that convey better execution while further developing unwavering quality while staying basic and simple to carry out.

The power control demand existed in the early development of drive and was continuously brought in. The interest for electric power control is for the still up in the air by the exchanging gadgets utilized in the particular control framework. With cutting edge gadgets, exchanging methods and taking care of have proactively gotten to the next level. The utilization of cutting edge control methods in power control has many applications, making it hard to characterize the power control application's limits. The latest thing in control drive improvement is moving away from conventional power gadgets and toward microchips, microcontrollers, and PCs. In light of its solidness and trustworthiness, power control innovation has overwhelmed the market. Power electronic gadgets are broadly utilized in drive innovation, which has filled in significance in the last quarter decade. Power control has filled consistently initially, yet has as of late experienced nonlinear development because of expanded interest for dependable control, adaptability, and intricacy

Superior execution, control, and checking procedures are broadly utilized in acceptance engine drives, which have acquired ubiquity because of their atomization. Quality execution is a central question that is perceived in numerous modern applications. The different control gadgets like the Programmable Rationale Regulator, Chip, PC (PC), and Microcontrollers assume a significant part in keeping up with the necessary degree of value and control.

AC drives are generally used to control the speed of electrical engines. An alternating gadget of this sort can be either an enlistment engine or a coordinated engine. There are a few kinds of AC drives, including variable recurrence, speed, and other variable boundary drives known as converters. AC drives, such as motors, are frequently used to power industrial machinery. The AC drives are also used in common appliances such as food blenders and drills. Although these drives are not limited to the applications mentioned, they play an important role in more complex and difficult environments in the majority of applications.

1.1 REVIEW OF LITERATURE

Before, a straightforward machine essentially affected human existence. The straightforward machine has a set number of tasks. In the beginning phases of the liver, pulleys were utilized in most of the activities. Nonetheless, the straightforward machine was subsequently moved as hand power drives that were driven by people. This is presently not valuable in current ventures and has been supplanted by torque driven by creatures, which is as of now not helpful in industry. The time of mechanical and electro-mechanical power driven drives keeps on existing as the underpinning, everything being equal, however with the development of electric drives, past drives were not generally broadly utilized in that frame of mind in a couple of fields.

Electric drives are significant in light of the fact that main players are typically significant in the power gain process. Bunch electric drives previously showed up during the 1920s, yet because of their low productivity, they were supplanted during the 1950s by modern electric drives, which tracked down broad use in most modern cycles. Afterward, the multi-engine drive idea was created and applied to complex cycles.

At the point when the modern insurgency started, DC engines [1] were unmistakably utilized for the control of different modern applications, and this training has proceeded right up 'til now. Notwithstanding, because of changes in the control of AC load applications, it has a few

drawbacks, so it has been replaced by induction motors over the last 50 to 70 years. These induction motors are powered by an alternating current supply, so no additional complex circuitry is required for control applications. Because the available supply was rotating current , enlistment engines became famous in modern cycles. With cutting edge computerized gadgets, giving exact control of the modern process is conceivable. The acceptance engine has demonstrated to be a significant control part in the present control component [2]. Since the improvement of drives, it is normal that it will be outfitted with various procedures with trend setting innovations [3, 4] and complex cycles [5] with staggered converters [6]. The interest for drive control was required. Indeed, even in remote and uncommon areas, enlistment engine drives assume a significant part in diminishing line music [7].

Using digital techniques with compact and micro-levels, induction motor drive control has changed the face of the world over the last two decades. To design sophisticated machines, significant reliable advanced devices are used. This computerized nature of drive control made ready for a huge achievement throughout the entire existence of drive framework improvement. The utilization of microcontrollers, FPGAs, PLCs, and other elite execution parts brought about the advancement of superior execution frameworks. Presently, the estimation of different boundaries and control plans [8] has put a superior on the plan of the information obtaining framework. Innovation has progressed to where it expands past changes. The time of equipment control plans is at this point not predominant in drive control innovation, yet half and half innovation, which controls equipment with programming, has acquired conspicuousness over the most recent twenty years. Demonstrating, reproduction, and man-made reasoning [9-11] have helped drive innovation and prompted the improvement of new control methodologies [12]. The computerized stockpiling nature of the gadget of enlistment engine drives is helped with programming that helps with putting the best answer for the drive. The ongoing examination addresses the plan of a basic single to three stage drive with not many parts and a little size, as well as its investigation [13].

PLCs are microprocessor/microcontroller-based systems that perform a variety of functions in industrial processes. Directions are decoded in the PC Unit (PU) to control different cycle tasks, and the important signs are given to control the suitable gadget. Assuming that the control succession is to be changed, the guidance code in the computer chip should be changed. Such data

sources are acknowledged by the PLC as a stepping stool chart of PC programming directions. The focal transfers, counters, clocks, and sequencers are supplanted by a computer processor in light of a chip. PLCs with word processors are utilized when mathematical information, estimations, measuring, controlling, and recording, as well as straightforward sign handling in double qualities, are required.

Three phase motors are the most commonly used motors for industrial motion control because they are tough and easy to operate. The three phase control algorithms are created in an open loop environment. Microprocessors and microcontrollers are less expensive and used in a wide range of applications, but their speed is very high and frequently causes problems with changes in control techniques, as opposed to PLCs, Programmable logic devices (PLD), FPGAs, and so on. The FPGA can be used to implement programming for any digital function. FPGA's principal benefits are its speed, the quantity of accessible entryways that decides limit, and extra usefulness [14] with insignificant extra equipment. On the off chance that the FPGA is customized, it will work freely subsequent to being separated from the PC. R. Tejaswini and R Sinduja introduced a way to deal with voltage/recurrence (V/F) control of enlistment engines in which they planned a three stage acceptance engine inverter drive with a heartbeat width balance (PWM) control approach.

The development of a FPGA-based speed control framework was chipped away at by B. Hariram and N. S. Marimuthu [15]. The completely planned space vector PWM V/F control plot is utilized in this article. This can likewise be executed utilizing computerized signal handling (DSP), which gives programming adaptability and high productivity. Power converters turned out to be more famous as exchanging procedures further developed utilizing strong state power gadgets. This empowers basic recurrence and extent voltage adjustment, taking into account higher productivity and execution with less commotion. The tweak technique utilizing space vector PWM (SVPWM) is useful, and the linearity is moved along. Much headway has been made in computerized hardware throughout the course of recent years. Due to its execution ability in planning and programming V/F control conveyed by Austere III FPGA, FPGA is upgrading telecom, DSP, implanted control frameworks, and electrical frameworks.

Ooi and colleagues [16] propose a field-oriented FPGA-based control scheme. The adaptability and honesty of SV Tweak and field-situated control are utilized on a solitary chip, which has restricted computational properties that are overwhelmed by numerous DSP. Altera's high level

application explicit incorporated circuit - based gadgets give an affordable arrangement and quick circuit reaction through equal execution instead of consecutive execution. These creators focused on the plan and improvement of an adaptable and financially savvy framework.

To effectively control power, software tools such as modeling and simulation, which can handle many functions in an integrated environment, play an important role. Because multiple operations can be handled concurrently in parallel in FPGA, the time required to execute the algorithm is much lower than in DSP. The simulation will aid in the efficient and effective design of hardware using electromagnetic pulse technology (EMPT) and MATLAB or Simulink.

J. G. Mailloux and colleagues[18] use Xilinx Framework Generator (XSG) in the execution of vector control for acceptance engine drive. The effective Xilinx framework generator device is utilized in a Simulink climate, and the graphical algorithmic methodology has been stretched out to FPGA improvement utilizing Simulink. New licensed innovation (IP) modules have been utilized for open circle vector control plan, however the XSG 8.1 control is intended for shut circle with electromechanical balanced drives.

Three-stage acceptance engines are generally utilized for uncompromising burdens. On the off chance that a three-stage power supply isn't accessible, the inverter module's single stage power supply can be switched over completely to a three-stage power supply. Indeed, even in exceptionally uncompromising applications, three stages are deficient and overburdened the engine, so S. S. Kumbhar and associates [25] presented the polyphase idea. In this review, six stage inverters with 60 degree each stage is utilized to supply convert the power. The drive's exhibition was tried, and the improved outcomes were found.

A, M, and Eltamaly [26] utilized a stator voltage controller with a FPGA to control the speed of an enlistment engine. The stator voltage is fluctuated to change the speed utilizing six two-way switches and a saw-tooth waveform with a twofold power supply recurrence as the control signal. The framework's result voltage is constrained by changing the sawtooth wave signal. At low balance record, a delicate beginning methodology in light of FPGA reproduction is likewise carried out. The FPGA gives equal capability in autonomous activity for different controls for this situation. The utilization of SPWM in the inverter has decreased sounds. The utilization of a PWM system works on engine execution as well as engine control.

1.2 STATEMENT OF PROBLEM

The proposed research issue will fixate on the improvement of a PLC control framework in view of a FPGA that can detect different boundaries from an enlistment engine and contrast them with the standard scope of the equivalent. The FPGA module will be responsible for information procurement. Assuming the set boundary of the acceptance engine drive contrasts from the standard one, the drive will take care to keep up with the expected boundaries.

FPGA will assume a basic part in playing out every one of the complicated tasks by driving the expected information procurement module, which will show different enlistment engine boundaries. The FPGA would drive the power driver circuit, which is expected to control the power. The previously mentioned FPGA-based module will work simultaneously, staying away from the framework's consecutive nature.

A three-stage enlistment engine drive is being examined, and its boundaries will be checked. A delicate beginning component will be utilized to begin the development of this engine. The engine will be driven utilizing the beat width regulation method. To speak with the PLC control framework and send orders to control the acceptance engine drive boundaries, the Double Tone Multi-Recurrence (DTMF) method will be utilized. On account of an excess drive, in the event that the principal PLC drive neglects to work appropriately, a backup PLC control framework will be enacted to keep the framework functional. PLC regulator in view of FPGA will enact the exchanging circuit.

1.3 METHODOLOGY

The proposed framework will be founded on re-configurable programmable gadgets, and Simple to Computerized Converters with sufficient change speed will be utilized for the high exactness and speed digitization of enlistment engine boundaries. The simultaneously working model that will be created in the FPGA itself will be utilized to deal with LCD connecting with the FPGA to show different engine boundaries. The Xilinx FPGA will be utilized to carry out the VHDL-coded equipment modules.

1.4 STEPS INVOLVED IN IMPLEMENTATION RESEARCH PROBLEM

The programmable rationale regulator is intended to work continuously outrageous circumstances in which the machine can't work and is probably going to be harmed. The PLC has countless ports for interfacing with information obtaining modules like sensors, engines, information converters, observing gadgets, etc. The framework will have undeniably a larger number of assumptions than a standard PLC or existing PLC control frameworks..

2. BACKGROUND

The previous chapter introduced the drive and its associated information survey. The evolution of the literature survey as well as chapter-by-chapter information from the research work has been highlighted. The final chapter also includes a brief summary and statement of the research problem. The ongoing part gives an outline of the fundamental drive and its different sorts. The electrical machine and its different assortments are examined. The hypothesis of the enlistment machine and its speed control methods are totally talked about. The ongoing part likewise incorporates a past filled with the drive and its transformative idea. In a similar section, the FPGA-based engineering and its itemized hypothesis, as well as the projects, are introduced.

2.1 DEVELOPMENT OF MACHINES AND ITS BACKGROUND

An electrical machine can change over electrical energy into mechanical energy. The generator is the most common way of changing over mechanical energy into electrical energy in switch. Regularly, motoring mode is utilized, in which the collaboration of attractive field and current produces power and couple, and the engine starts to turn. Engines in transportation can be worked in both motoring and breaking modes.

2.2 ELECTRICAL MACHINES

2.2.1 DC Machine

The field windings, armature windings, rotor, burden, brushes, stator, and field windings of a DC machine are provided to the dc hotspot for excitation. The sectional perspective on a DC machine is displayed in Figure 2.1. The attractive posts' not entirely set in stone by the course of the field current. The guides are embedded into the openings that convey the current. The two brushes between the armature can pivot. These brushes are opposite to the primary field hub. Accordingly, they can openly pivot between the two tomahawks. These brushes are fixed, while the rotor pivots. When the armature begins to rotate, electromotive force (EMF) is generated in the armature conductors.

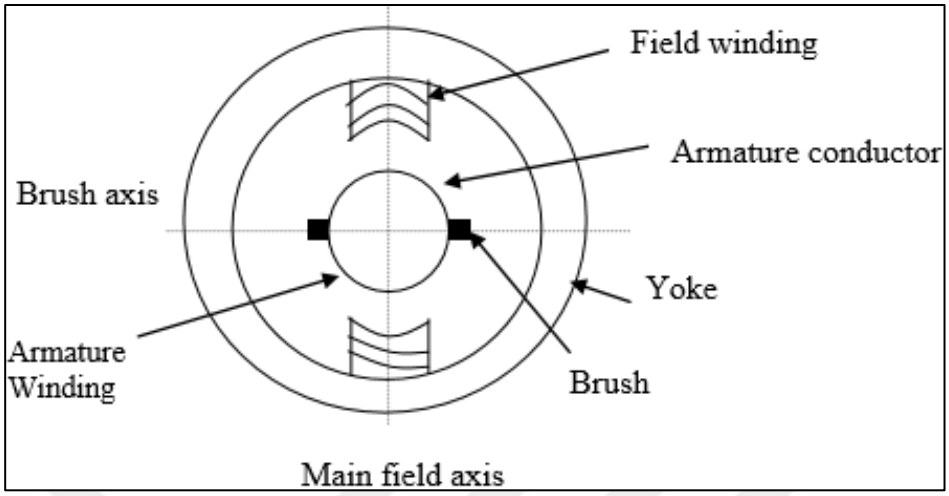

Figure 2.1: Cross sectional view of DC machine

Around the get together diversion curls are wound called burden which moves the armature into the movement.

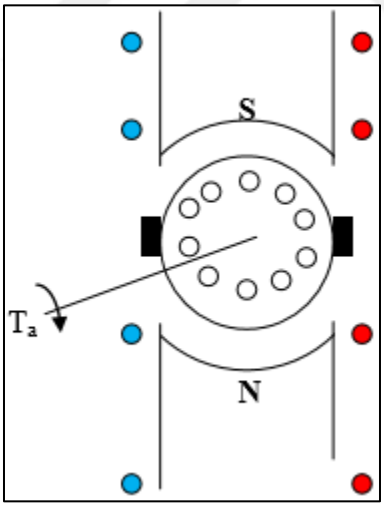

Figure 2.2: Electric torque developed in DC machine

Ta is the armature and electromagnetic force as displayed in Fig. 2.3. The created in an enemy of clockwise bearing as the field's fixed north and south poles pulled in the armature's south and north poles. The size of electromagnetic force and the shaft not set in stone by the ongoing moving through the field winding.

2.2.2 AC Machine

AC machines play an important role as prime movers in both domestic and industrial applications. Single phase and three phase AC machines are available. The single phase machine has a low work power and operates at a lower power level. Single phase motors are commonly used in domestic appliances. The alternating current machine is a type of electric machine that has a wide range of applications in industry as a prime motor drive and in several domestic applications in its single phase form. Over 90% of drives are rotating current and use enlistment engines. Three stage drives are utilized in rock solid and enormous modern applications. Single stage drives for homegrown use are favored [1]. Single stage engines are likewise utilized in studios and business settings Q[2].

2.3 CLASSIFICATION OF THREE PHASE MOTORS

Three phase motors are used in almost all heavy industries around the world. Three phase motors, with minor modifications to their structure and power, are well suited to a variety of applications.

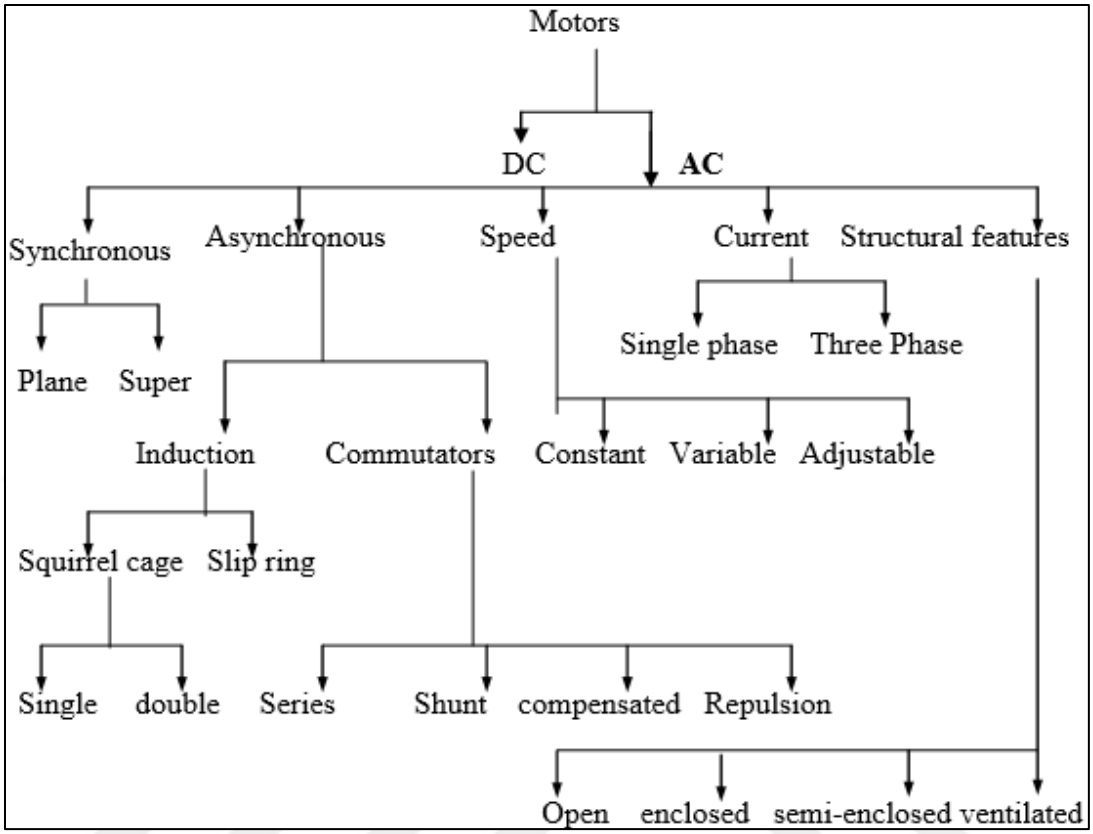

Figure 2.3: Tree diagram of classification of three phase motors

The above kinds are all three stage engines with a couple of kilowatts of limit, however for hard core engines, the limit of the engines referenced is being able to drive extremely enormous burdens, so the wattages increment. Engines are planned, fabricated, and utilized as per industry norms.

2.4 THREE -PHASE INDUCTION MOTORS

Each three-stage enlistment engine is worked to run on three-stage rotating current current provided straightforwardly to the stator winding and acceptance or transformer activity to the rotor winding [3,4]. In view of the enlistment activity, the rotor starts turning with extraordinary power, and stage helps with adding more solidarity to drive the rotor in pivoting movement. The pivoting transformer is one more name for an acceptance machine. The fixed twisting on the stator is associated with the line supply, while the other twisting on the rotor gets power from the transformer as it turns. Three-stage acceptance engines have preferred execution qualities over single-stage enlistment engines. Enlistment engine execution attributes are:

2.5 CONCEPT OF MACHINE DRIVE

Practically all advanced machines are comprised of three unmistakable parts that are expected for process activity: the main player, the transmission framework, and the functioning machine parts. The main player, related to the control part, helps with the development of machine parts during the work interaction, and the transmission framework comprises of a progression of shafts, pulleys, belts, gears [9-12], and different parts through which the central player can move machine parts. These two components worked together to keep the machine moving, which is commonly referred to as drive. [13].

2.5.1 Simple Drive Configuration

The drive is a basic design of the cycle's functioning machine. The drive can be open circle or shut circle, and it can carry out numerous roles. The source supplies the necessary power for engine load movement by means of the power regulator, which is constrained by the control unit, and input is acquired from power detecting, and the power is controlled and the activity is kept stable. This is a shut circle criticism drive framework in which restorative activity is taken right away and no criticism is accessible, rather than an open circle drive.

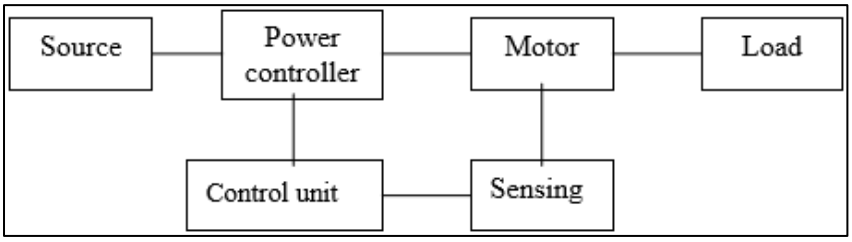

Figure 2.4: General representation of drive

The blocks are all connected together, and the signs stream in a particular request and heading. The power is provided to the engine through the regulator, which is overseen by its control unit. The input is shipped off the control unit, which then makes the fitting move to give the right sign. The engine can drive the heap detected by the different detecting game plans.

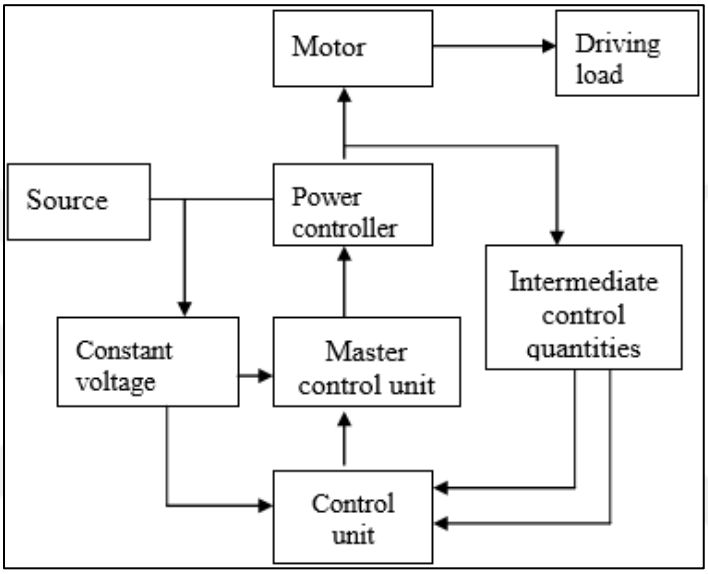

Figure 2.5: Representation of controlled drive

Drive is a mix of a few performing parts addressed by blocks and interconnected for the particular interaction. All a bunch of differential conditions depicting different conduct conditions can be utilized to address the drive framework and its parts. Each block has its own feedback and result relationship whenever it is addressed by a block chart. It gives significant knowledge into the framework's tendency. It is exceptionally easy to work on a framework utilizing the block chart decrease procedure. The cycle is mechanical, and it brings about a solitary by and large block that addresses the framework's exhibition. The unidirectional blocks are all associated toward signal stream. Beside addressing the framework with a numerical model, the block outline in Figure 2.5 portrays the progression of signs all things considered. It is a straightforward portrayal for getting data about unique way of behaving. It doesn't, in any case, give any data about the actual idea of the framework.

Each control interaction is an exceptional blend of sign and energy. The sign high priority an ideal worth, a genuine worth, and an estimation cycle that is conceivable with the drive framework

utilizing one of the different kinds of drives. There are right now four unique sorts of drive frameworks accessible.

2.6 PWM CONTROL OF INDUCTION MOTOR

The PWM method is utilized to control the power provided to the heap. The scaffold rectifier produces an immediate current inventory that is utilized as a contribution for inverter power control. There are a few PWM strategies accessible, however sinusoidal PWM is the most normally utilized. The result not entirely set in stone by the tweak list. Therefore, PWM control is fitting for consistent force and HP modes. Chosen consonant end works on the symphonious substance considerably more. Since the DC supply voltage is gotten by means of a controlled scaffold rectifier, it remains almost steady all through the speed control range. The power factor of the input is also high. Commutation is quite satisfactory due to the stable supply voltage, and no separate DC source is required for commutation. If continuous operation is required, floating batteries can be used.

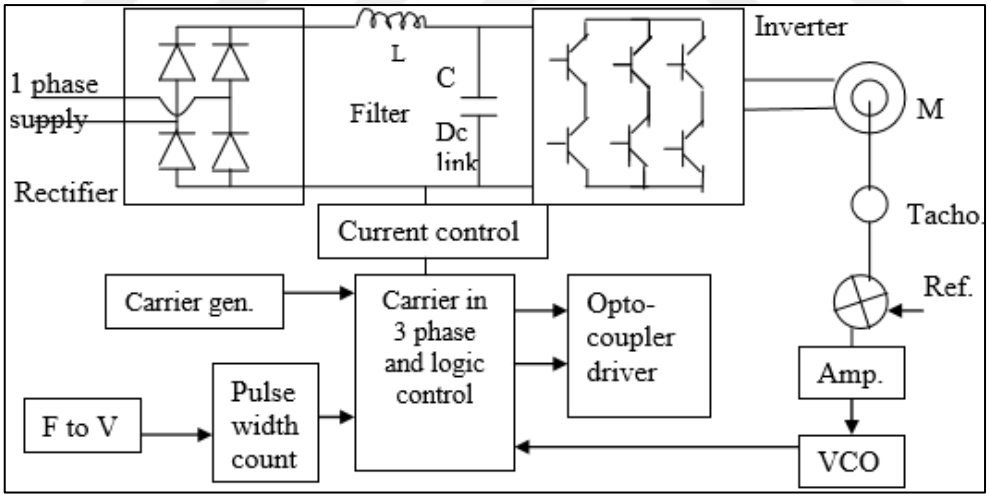

Figure 2.6: Microprocessor based PWM control of drive

At the point when the PWM framework is utilized, high flows are created during inverter exchanging. Therefore, fast exchanging frameworks with low power utilization are utilized. High recurrence exchanging creates high inrush flows, which require the utilization of snubber circuits in the plan. High flows likewise cause warming in the protection of the engine's windings, and there is a gamble of drive harm.

To get the best results from PWM, the frequency must be chosen carefully. This switching and required frequency is accomplished through the use of a microprocessor, which calculates the optimal number of pulses per cycle for each speed setting and generates coded output at all frequencies.

Figure 2.6 depicts the block diagram of a microprocessor-based PWM system [19,20]. The logic section is comprised of an Intel 8085 microprocessor. The rectifier and DC link capacitor banks convert the single phase line voltage to direct current. The bypass ripple contents are provided by the capacitor banks, and the inverter receives nearly pure DC. The microprocessor logic control program regulates the inverter firing. The inverter semiconductor gadget is picked so that it yields the ideal recurrence and greatness to the heap as an engine. The tachometer estimates the engine speed and thinks about it to the reference speed utilizing the VCO, giving criticism to the chip control. The slope generator utilizes the blunder voltage to decide the most extreme and least speed limits. The rationale plot utilized in chip is sine coded with twofold edged regulation. The microchip yield is steered to the inverter gadgets through the coupler driver. This setup produces an exceptionally close sine wave result to the engine load.

Without criticism to the engine, an open circle conspire is additionally conceivable. Where steady speed is a trait of the enlistment engine, the open-circle framework is very reasonable, and its speed guideline requires the steadiness of the voltage controlled oscillator.

2.7 MICROCOMPUTER CONTROL MOTOR DRIVE

The microcomputer control conspire [21, 22] is smaller and requires less wiring. The framework is exceptionally solid and performs well. The plan's product execution is monetarily accessible and versatile for changing the control procedure. This adds the additional component of evolving control. This framework incorporates various applications that go about as interaction managers. In case of a drive issue, a microcomputer control framework can likewise perform properly. At the same time, demonstrative and administrative controls for engine control are executed involving the PC in the drive.

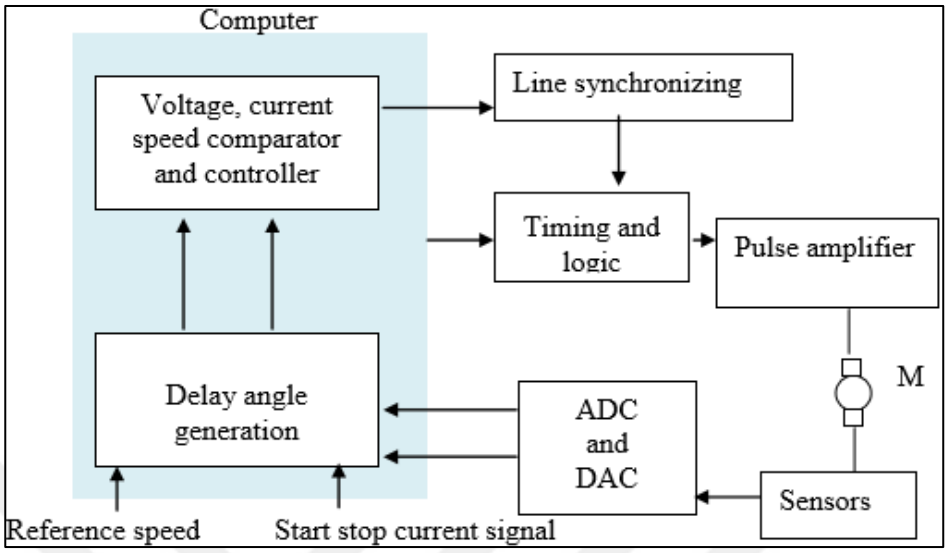

Figure 2.7: Block diagram of computer based induction drive

The block graph of a microcomputer control drive is displayed in Figure 2.7. ADC gives the expected control sign to the microcomputer. The defer point generator and control rationale empower the PC to produce the expected terminating beat for inverter terminating. Line recurrence synchronization is required and given to supply line voltage. Albeit the microcomputer can perform entryway beat generator and rationale circuit capabilities, they are displayed external the microcomputer. The beat speaker, as well as entryway beats with adequate levels, give the essential seclusion. The PC control procedure is proper for changing the speed for different applications. This is just conceivable by changing the product code.

2.8 PROGRAMMABLE LOGIC CONTROLLER

Automation and control techniques in industrial electronics play an important role. These techniques are usually tailored to specific requirements to achieve the most attractive and desired results. These are the custom designed systems using personal computers in industrial process control or other control systems. Study of automatic control has played a vital role in the field of advance engineering and science.

The control systems before 1960's were based on relay control. These systems faced the problem of flexibility in the expansion of process, occupied large space in the control room and taken longer duration of time during the changes and troubleshooting of control process. To overcome these difficulties Bedford Associates team Richard Morley, Mike Greenberg, Jonas Landau, George

Schwent and Tom Boissevain, introduced the first Programmable Logic Controller (PLC) in the year 1969 called as Modicon Modular Digital Controller (Modicon 084). The initial machine had 125 words of memory, occupied large space and there were no considerations for speed. Later this was modified with some changes in the control design by the engineers of AllenBradley, named as Odo Struger and Ernst Dummermuth. Current processors have the ability to scan a 100,000 steps program in one millisecond, small and light weight with a built-in Ethernet port [1-5].

Since 1970s, Programmable Logic Controllers (PLCs) were used in the industrial automation. They were often reprogrammed during the operation of the plant to adapt them to new requirements. Introduction of distributed control systems in 1980 revolutionized the use of PLCs in the control industry. In 1987, further improvements in the PLC technologies provided most responsive and processing power for the building automation applications due to centrally located controlling capability, millisecond or fast response time, simplified wiring, cost saving, improved maintenance, increased reliability, more flexibility, communication capabilities, easy of programming and trouble shooting, lower cost, higher level of performance, expandability, modularity and withstand against harsh environments [6-8].

The characteristics of a PLC include modular design, allowing easy replacement or addition of units and large number of peripherals (20 to 100 I/O s) in each PLC. Controlling both digital and analog signals, operated in the extreme temperature range (-30 oC to 85 oC), Programming with hand-held terminals or with a lap-top/computer, capable of communicating with other PLCs, computers and intelligent devices, economical for cost to usage systems, and easily understandable programming language.

Apart from the advantages mentioned above, PLCs have some disadvantages. PLC manufactures provide closed architecture for their products as compared to microcontroller systems which have open architecture. Software programs of the PLCs differ among the manufactures. Therefore they cannot be used from one manufacturer PLCs to the other manufacturer. Interface I/O modules of the PLC to the interface devices is not that easy. For any changes in the control design it requires skillful work and it is difficult to find errors if the problems occur in the design stage and may take long time to resolve. Sometimes it's hazardous to use in the case of potentially explosive chemical processes. Following sections discusses basic components, architecture, classifications,

programming languages, ladder diagram program, data acquisition and data communication with regard to PLC.

2.8.1 Basic components of PLC

The basic components of a PLC include power supply, Central Processing Unit (CPU), programming device, memory, input and output module as shown in Figure 2.8. The power supply voltage of 220V AC / 24V DC is required for operating PLC. CPU has microprocessor to store the program instructions in the memory and controls the output based on the input statuses and program instructions. Therefore CPU is said to be a brain of a programmable logic controller. Generally personal computer (PC) is used as a Programming unit of a PLC and is removed after software testing or execution of the program. Memories of a PLC are used to store the instructions and data. These are organized as program memory and data memory to store the logic program and variable data of the program respectively. The storage of information in these memories is tracked by an addressing system, to indicate the location of memory contents. The input module receives both digital and analog signals from the field devices and the output module sends the control signals to the devices to be controlled by the PLC based on the control program. Thus the inputs are the switches and/or sensors (both digital and analog) and the outputs are either discrete signals (ON/OFF signals) or analog control signals which provide the analog voltage/current proportional to the physical parameters to be controlled. A PLC can be used to send/receive the information over a communication network via local area network (LAN) or through Ethernet by using a communication interface ports [9, 10].

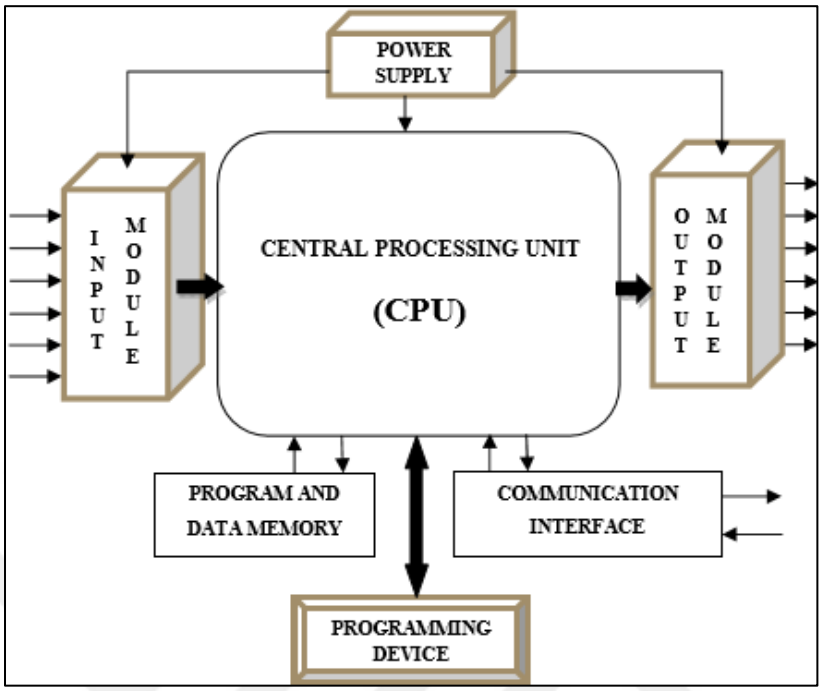

Figure 2.8: Basic components of PLC

2.8.2 Architecture of PLC

Internal architecture of a PLC shown in Figure 2.8 consists of CPU, buses, memory, input/output units and programming unit. CPU controls the whole operation of a PLC and is provided with the clock signal generator for the timing and synchronization of the control operations. This has an arithmetic and logic unit (ALU) to carry out the arithmetic operations such as addition, subtraction, multiplication, division etc. and logical operations of AND, OR, NOT, NOR etc. The executed results are retrieved in the memory. The whole operation is controlled by the control unit by providing the timing signals for these operations.

The paths which connect different parts of PLC are called as buses. These are tracks on Printed Circuit Boards (PCB) for controlling data flow between the control elements. The data bus is used to send the data, address bus is used to send the location of addresses and control bus is used to control these data and address bus information within the PLC for the internal operation. The data bus has 8 bit words and address bus has 8 address lines of 8 bit words. Thus the possible addresses are 28 = 256 address lines. Similarly 65,536 addresses can be used for 16 address lines. The data between memory devices .

Inputs devices supply a signal/data to an input module to perform control functions. Typical examples of inputs are push buttons, switches, and physical parameter measurement devices such as humidity sensor, temperature sensor, light sensor etc. The outputs execute the control operations based on the control signals from the output module. Switches, relays, solenoids and valves are the examples of output devices. Optoisolators or optocouplers made up of light emitting diode and photo transistor are used to provide electrical isolation. and input/output is controlled by the control bus signals.

2.8.3 Programming languages

PLC has its own design methods and programming languages and has been standardized by the International Electro technical Commission (IEC) as IEC standard 61131. These standards are instruction list (IL), function block diagram (FBD), structured text (ST), sequential function chart (SFC) and ladder diagram (LD) program.

IL is a European counterpart language, uses textual low-level assembler for programming PLC which is similar to programming a microprocessor in assembly level method. That is, it uses machine codes in mathematical form in instructions and is executed one after the other. The programs so written in this language can be moved easily between hardware platforms. Some limitations of this are i) It is difficult to find the errors in the complex mathematical operations. ii) It is not suitable for implementing large programs. iii) Also processing speed of operation and compactness are less as compared to other languages used in PLCs.

FBD is a very common to the process industry and uses the graphical blocks during the programming. These blocks are used to execute functional operations and require large screen space for programming. For large scale control applications, it is difficult to trace the error in the program because the program becomes clumsy to make any corrections.

ST and SFC are the graphical languages used for the control system and control process respectively. ST is the high level textual language and uses the instructions as similar to the instructions used in BASIC, PASCAL or C languages. SFC uses flowcharts to control the process in its program which simplifies the control logic programming and organizes functional specifications of a system. It is easier to read and add notes to clarify steps orcapture important

information for later use. The language utilizes reduced time to design and debug the program with faster and repeated execution of individual pieces of logic with simple screen display.

LD a graphical language has its roots in USA and is the most widely used programming language. It is based on the relay control logic. One can understand and troubleshoot a program with some basic ideas of Boolean logic operations [17, 18]. Following discusses the LD programme in detail since this one is used in our proposed systems.

2.8.4 Programmable Logic Controller Drive

In industrial control, a digital control device known as a programmable logic controller is preferred over an analog control device (PLC). The PLC can deal with countless boundaries for different temperature, current, and voltage ranges. Commotion, blunder, obstruction variety, and different boundaries are dependably controlled. Numerous I/O boundaries are dealt with simultaneously, speeding up the activity and the framework's reaction time. The PLC can store information in a capacity gadget known as memory. PLCs operate in real time, with tasks that are specific in nature. In a closed loop structure, PLC sequencing logic is used.

The early PLCs were not as powerful as those used today. Dick Morely, known as the "Father of PLC," provided the proper design structure. The first PLCs were hardware-based and used relays with ladder logic. Concerning experts, this assists with decreasing preparation and labor supply interest. Transfers are utilized in current PLCs, and programming is written in more elevated level programming dialects.

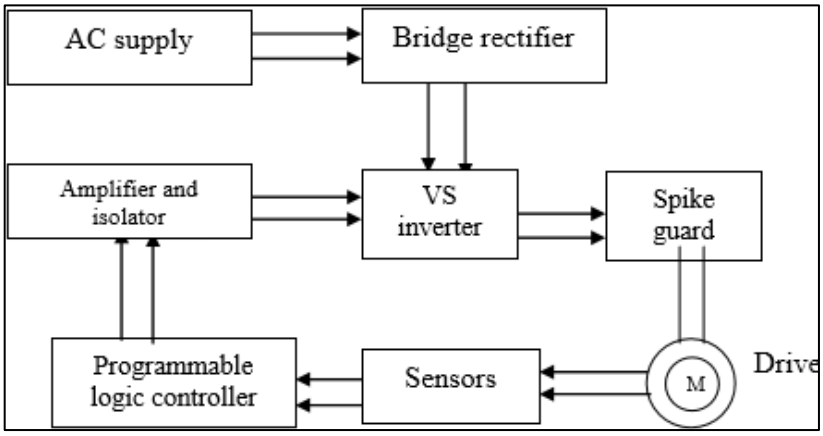

Figure 2.9: PLC based drive system.

The fundamental control part of the PLC is its 8-digit computer chip. The central processor is fit for taking care of correspondence between different equipment parts. The PLC handles the particular undertakings of handling and executing I/O gadgets. All control boundaries and orders are saved in a capacity gadget known as blaze memory.

The software program generates the control pulses. Because the control pulse strength is insufficient for firing the inverter MOSFETs, it must be amplified. The amplifier boosts the signal's strength. Isolation is used between the power and control circuits. The isolation circuit protects the control circuit from damage caused by uneven or false triggering and overvoltage. The power transistors were used in the design of the VSI [23, 24]. The necessary voltage is provided to the engine with 50 Hz steady recurrence and the ideal size because of the legitimate activity of the voltage source inverter. The capacity to the not entirely settled by the control signal. The more prominent the conduction, the more noteworthy the power provided to the drive, and hence the more prominent the speed, as well as the other way around. To control the drive, the framework is planned in a shut circle structure in which different engine boundaries are detected through sensors and the information is shipped off the PLC where standard information is put away in the ROM and the detected information is contrasted with the standard information in the memory and a criticism signal is produced. This input signal alters the terminating beat width and accordingly the drive's power. The framework might change the speed utilizing a current or voltage circle. The spike watch is utilized to stifle drifters created during inverter terminating. The PLC-based drive is particularly significant in light of the fact that it is little and can handle countless control factors, permitting the perplexing framework to be made due.

2.8.5 Microcontroller Based Drive System

On account of complicated processes in modern control frameworks, computerized control gadgets are more significant. The development of computerized gadgets like PLCs, PCs, and chip altogether affects drive innovation. Innovation is continuously advancing from the complex to the easier. The intricacy of the gadgets considers the improvement of new innovation for a superior control system. The microcontroller control gadget has satisfied the developing need for modern control.

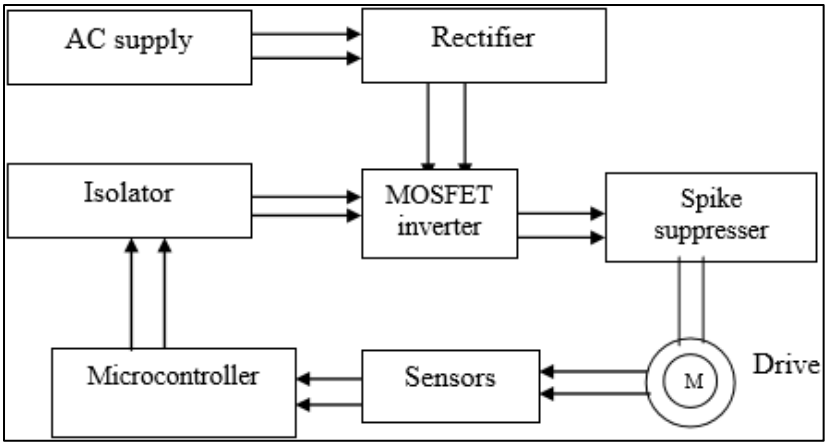

Figure 2.10: Microcontroller based drive system

The blocks inside the regulator are all interconnected, and the sign streams accurately. The redressed line supply is taken care of to the extension inverter. The inverter is terminated in the right grouping, and the microcontroller produces succession beats. The created beats can't drive the doors of the voltage source MOSFETs. Therefore, segregation and intensification are given. The Air conditioner signal across the voltage source inverter is created when the inverter is appropriately terminated. The Spike watch is utilized to smother drifters created during MOSFET terminating. This smoothes the sign and forestalls misleading setting off and drive overheating. The drive boundaries are recognized utilizing different sensors and took care of to the microcontroller. The framework is designed in a shut circle with the goal that it can make a remedial move on the off chance that any boundary upsets or disregards the reach.

2.9 FIELD PROGRAMMABLE GATE ARRAY

A field programmable door cluster is a coordinated circuit that can be arranged by a creator after it has been produced. The equipment depiction language indicates its arrangement (HDL). FPGA is a programmable semiconductor chip with different blocks for programming sources. These blocks are set up to imitate genuine equipment, and the functionalities are all connected without contacting the breadboard. The errands are created in computerized structure as programming and can be ordered to frame a record that contains data about wiring the circuit together. The FPGA can be reconfigured whenever and adds new character when recompiled. The progression of the FPGA has changed the guidelines of plan of the FPGA by engineers, which were already just utilized. Some significant level plan devices can alter designs, codes, and equipment circuits.

FPGAs can work in parallel, which means that different operations can be performed at the same time. FPGAs evolved from simple logic to application specific integrated circuits with the invention of Xilinx in 1984. (ASICs).

The advancement of digital systems has taken an architectural approach with traditional and logical blocks, as well as embedded systems on a single chip. Different components are assembled on a common platform to perform a specific function in an on-chip system. The system chip employs both the hardcore and softcore approaches. As a result, high-performance system functions are carried out in parallel.

To frame an on-chip programmable framework, the Xilinx framework incorporates a memory interface IP center framework, customs, fixed peripherals, gas pedals, and related parts. The blocks are all associated in the predefined way and play out the predetermined undertakings in view of the data gave. Different errands are registered simultaneously, and the cycle is finished at a quicker rate..

3. PROPOSED SYSTEM

The fourth chapter covers the hardware design and drive theory separately. The basic power circuit is described in detail, along with its specifications. The cushion Darlington pair is utilized for both intensification and impedance coordinating. The entryway drive, enhancer, and isolator are likewise completely talked about. The past section portrayed a three stage voltage source inverter plan and particulars. In this section, the planned equipment is introduced in a solitary unit called drive, which frames the fundamental portrayal of drive and is examined exhaustively in open and shut circle designs. Signal molding circuits, for example, AC voltage detecting, speed detecting, current detecting, etc are momentarily presented with their equipment. The product is written in Xilinx FPGA to create PWM terminating beats, decreasing equipment and cost. To work the engine productively, a delicate beginning component is required, which is shrouded in this part. Framework adjustment is additionally completed.

Using re-configurable programmable devices and Analog to Digital Converters with appropriate conversion speed, induction motor parameters will be digitized with high accuracy and speed. The LCD interface with the FPGA will be used to display various motor parameters using the concurrently working model that will be built. When it comes to implementing the VHDL-coded hardware modules, Xilinx will use the FPGA.

3.1 STEPS INVOLVED IN IMPLEMENTATION RESEARCH PROBLEM

Figure 4.1 depicts a general representation of the entire system. Feedback is absent in open loop configurations but present in closed loops. Controlled PWM is used to avoid current peaking losses during power on. There is immediate feedback current control. The feedback signal will aid in controlling the machine's various parameters.

The voltage source inverter receives power from a power rectifier. The rectifier is connected across the DC capacitor banks. The PWM beat created by the FPGA decides the control of the voltage source inverter. Since the created beat is deficient to drive the voltage source, impedance coordinating and enhancement are performed utilizing the Darlington semiconductor enhancer.

The programmable logic controller (PLC) is designed to perform in real-time harsh conditions in which the machine cannot be operated and may be susceptible to harm. Many of the PLC's

interface ports allow it to connect to various data acquisition modules, including sensor devices and motors as well as other types of monitoring devices and data converters. According to module wiz implementation procedures and specifics regions, the system will have a lot more demands than typical PLCs or existing PLC control systems.:

a) A standard door drive circuit will be utilized to control a three-stage enlistment engine.

b) A delicate IP Center will be created and executed in FPGA to control the inverter PLC.

c) For control, a Xilinx miniature burst based processor center will be defined and executed on a Xilinx Straightforward 3E FPGA.

d) The FPGA will be the focal module for executing PLC hardware.

e) A Heartbeat Width Adjustment (PWM) terminating method will be utilized to test the inverter in the PLC.

f) Following signal molding, the information values are recorded/showed, and a correlation with standard qualities is performed simultaneously.

g) FPGA and related hardware will be utilized to carry out the DTMF module. This strategy will be utilized to test remote exchanging of PLC control.

h) The drive's presentation will be tried in the wake of consolidating all of the executed.

i) I The exhibition of the fundamental PLC drive and the excess drive will be analyzed and archived.

3.2 SYSTEM DESIGN

For the drive, this paper discusses the design of a variety of hardware components necessary. The power inverter and snubber are also detailed in detail. We will also see different hardware circuits used to sense the various parameters. Power rectifier, gate driver, voltage source inverter, buffer and parameter sensor are just a few of the different pieces that make up the closed loop system.

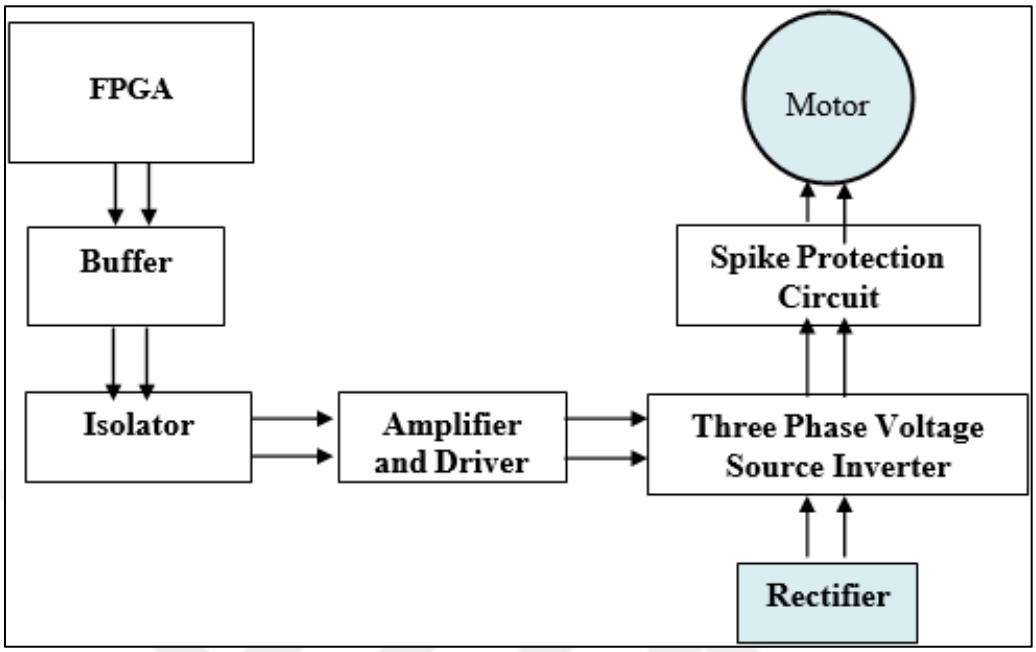

Figure 3.1: Representation of closed loop system design

A block-by-block outline of the current research endeavor is shown in Figure 3.1. The general system always works without any feedback from the user. There is no feedback in open loop, thus control is difficult. Changing parameter values do not have any effect on the motor speed, either. Closed-loop feedback is crucial for controlling motors. Controlling a motor in a close-loop setup involves a variety of control feedback loops. Utilizing FPGA and a data collecting system, a multiple pulse width modulation approach is used to control the motor's rotation speed. Buffer circuits, drivers, and amplifiers on the FPGA bus eliminate the loading effects. As long as the signal intensity can be amplified, the buffer will be used to do so. The driving skill has been improved.

Speaker and opto-isolator are remembered for the door drive circuit. Opto-isolator disconnects terminating circuit from power circuit, while driver intensifies the sign expected to work the power MOSFETs of voltage source inverters.

To power the inverter, a DC voltage is given after filtering through a capacitor bank. With each PWM pulse, the motor's power is modified. Due to this, motor speed can be adjusted by the pulse width of a pulse. The opto-interrupter gadget measures the motor's speed. There is a frequency (F)

to voltage converter (V) that converts the pulses into proportional voltage. Software converts this proportional voltage into the proper speed. One-by-one, the following part explains the design of several circuits that are employed in the system.

3.3 BASIC DESCRIPTION OF REMOTE CONTROLLED DRIVE

Figure 3.2 portrays a total framework graph of a solitary to three stage enlistment engine drive that can be controlled from a far-off area. Widespread Offbeat Collectors and Transmitters (UART), DTMF, FPGA, Show, receiving wire, ADC, DAC, and F to V converters, voltage sensors, momentum detecting, converter, support, isolator, inverter driver, three stage inverter, snubber, engine, and related little hardware parts involve the framework.

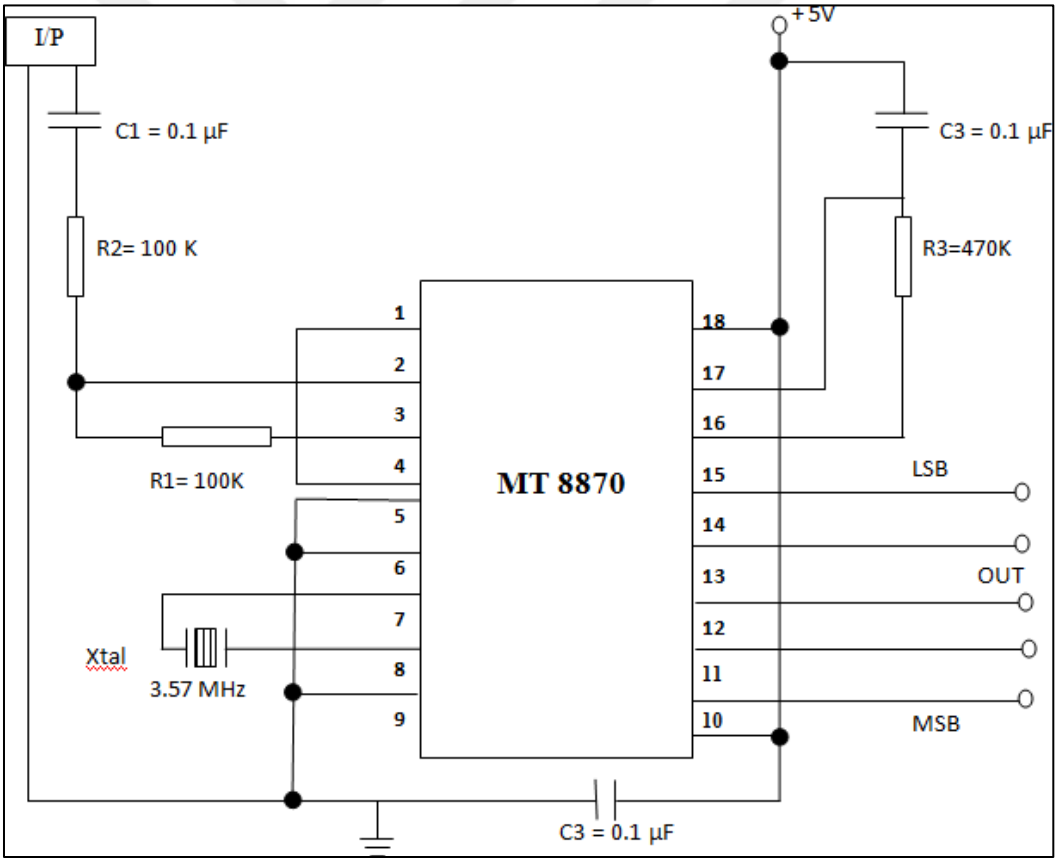

Figure 3.2: DTMF remote control drive

The framework is intended to give immediate current control criticism. Involving the ongoing circle criticism in the engine drive, the framework produces a result square heartbeat with the

necessary recurrence, current, and abundancy. A channel bank comprised of different high limit voltage capacitors is associated across the rectifier's dc yield. As flood beats are created during inverter terminating, this capacitor bank gives separating as well as a flood defender, and it effectively sidesteps to ground. The times the exchanging happens in PWM guarantees that flood beats are constantly created, and dispensing with or stifling the capacitor will serve somewhat. Six MOSFETs structure the inverter extension, and they will be terminated in a particular request to deliver three stage result to drive the engine.

3.4 BUFFER STAGE

To get control PWM beats, the FPGA and its related communicating part are utilized. At the point when the FPGA produces the control signal, it is lacking to drive the driver circuit opto-isolators, which are utilized to separate the control signal from a power circuit. The FPGA cannot be used to drive the motor directly, and if it is, it will cause problems with the inverter's firing, resulting in inaccurate power to the motor and poor speed control. There is a buffer circuit utilized for the FPGA and opto-isolator in order to avoid this problem. The buffer stage circuit diagram is shown in Figure 3.3.

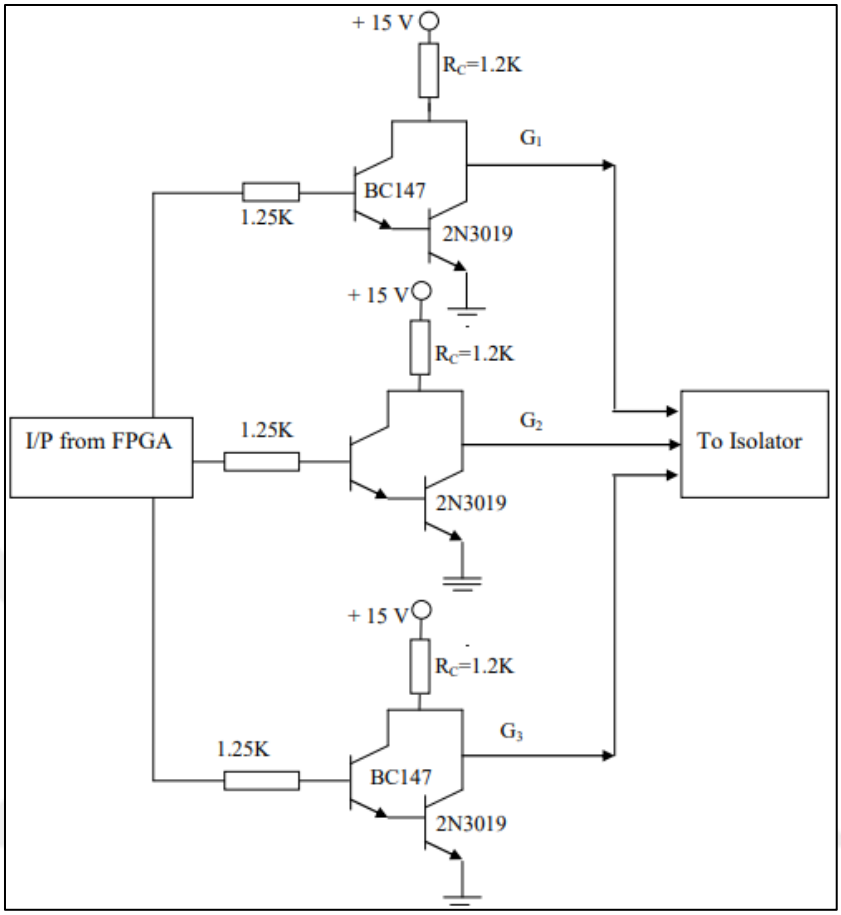

Figure 3.3: Buffer circuit

In order to create FPGA control signals, a basic design called a Darlington pair is used, which serves to provide the isolator with appropriate current capability. The Darlington transistor pair consists of a simple NPN transistor BC147 and a 2N3019, whose output is sent to the opt isolator. The buffer's design is indicated as a minus symbol. The transistor BC 147's base bias is controlled by the FPGA's output control signal.

3.5 GATE DRIVE STAGE

LED and phototransistor make comprise an opto-coupler. Whenever a photo transistor is used, it's always in reverse bias. Transistors have an extremely short growth and decay time. Due to the high frequency application's limited turn-on and turn-off time. Other than the control and power circuit,

an opto-coupler requires a separate power supply source to function properly. Because of this, the drive becomes more expensive and sophisticated, as well as more large. The internal structure of an opto-coupler is shown in Figure 3.4. (MCT2E);

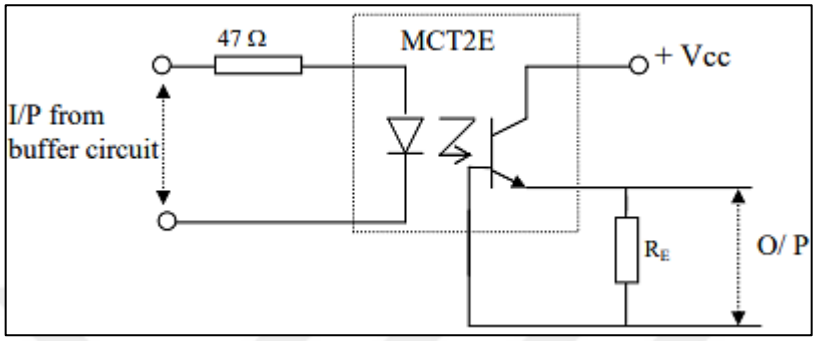

Figure 3.4: Circuit of opto-coupler

The input control signal from the buffer is supplied to the light emitting diode, as the light falls on the base, photo-register changes and the output changes with proportion of light. The purpose of isolator to isolates control and power circuit from one another. This is a requirement in any power application where the output power is controlled. This also eliminates the risk of shock in the control section.

3.6 SNUBBER MODULE

For the MOSFET switching circuit, the snubber is essential to reduce the transients. Since most semiconductor exchanging gadgets have unstructured frail elements like feeble holding, lopsided glasslike structure, resistivity, as well as conductivity [8], semiconductor materials are utilized in the plan of the gadgets. Conceptual design of the device does not account for these flaws. It's possible that the system's false triggering or partial activation is caused by the system's quick and repetitive application and currents in the process. For the MOSFET switching circuit, the snubber is essential to reduce the transients. Because most semiconductor switching devices have unstructured weak features like weak bonding, uneven crystalline structure, resistivity, and conductivity [8], semiconductor materials are used in the device's design. Conceptual design of the device does not account for these flaws. It's possible that the system's false triggering or partial activation is caused by the system's quick and repetitive application and currents in the process. The maximum (di/dt) rating of the gadget should not be exceeded in order to avoid harm. It is

easiest to use an inductive snubber circuit as shown in Figure 3.5. Fortunately, many loads have a significant inductive component, so separate protection may be required.

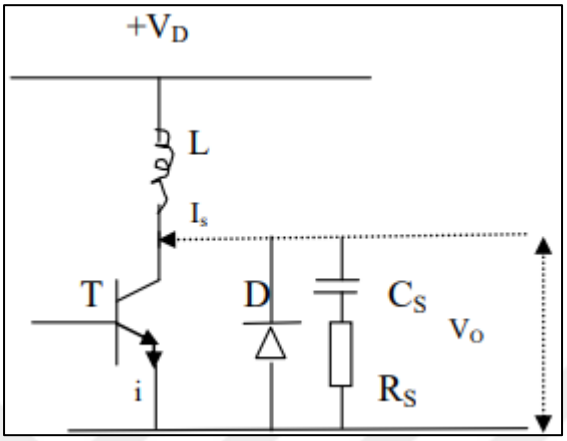

Figure 3.5: Transistor based snubber circuit

This occurs as the stored charge inside the transistor current decreases, increasing the diode's conduction. As a result, the load current remains constant and vice versa. Whole cycle appears across the snubber during the rise and fall of the current through transistor, during number of switching the heavy power loss takes place. LC combination will try to keep the transistor change in the certain limits.

3.7 SIGNAL CONDITIONING

Optical interrupters are used to measure speed. A photodetector and LED are coupled to sense light in the opt interrupter. For each revolution of the motor shaft, one pulse is created. For example, the opto-interrupter is made up of an opto-coupler, which contains both the light source and the light detector in one package. Over the motor's shaft, a thin, round disc is attached in a circular pattern. There is a hole in the center of the disk, which has been painted with a dark color pigment. Disk rotates in between LED and detector when opto-interrupter is mounted. This means that when a hole travels through a disc, its light is blocked and a pulse will be generated for every hole that passes through the arrangement. During each revolution, a pulse is produced. Speed of the motor is determined by the pulse duration generated by the motor's generator. A pulse will be repeated after a long period of time if its speed is less than that of the pulse generator because the wheel rotates slowly. Figure 3.6 shows a speed sensor block. The F to V converter receives the

generated pulses and converts them to voltage. The output is created based on the number of rounds per minute or the frequency. To display the correct speed, the output of the frequency to voltage converter is scaled between 0 and 5 V for speed range of 0.01 to 1300 rpm. A non-linear rotation of the disk causes the speed sensor in the system to respond non-linearly at the beginning, but linearity is restored subsequently. If you're driving slowly, you'll need to take corrective action. After a certain speed, the correction factor can be bypassed, allowing for the corrective action to be taken. On Figure 3.6, you can see a real-world setup of the speed sensing arrangement with opt interrupter device.

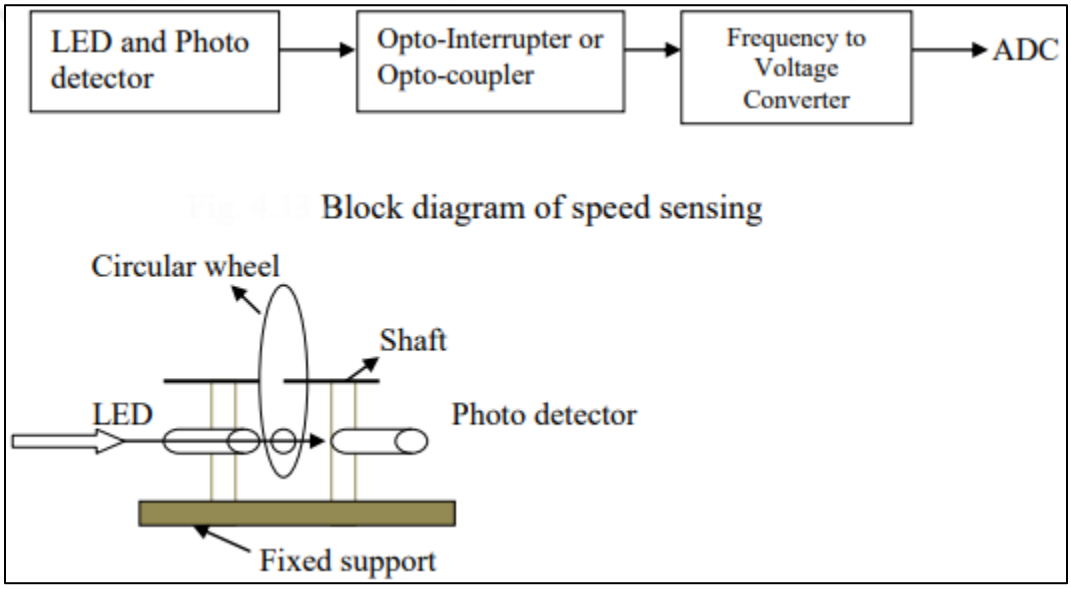

Figure 3.6: Speed sensing

4. RESULTS & DISCUSSION

In the previous section, the hardware design and theory of the drive were discussed in detail. The basic power circuit is described in detail, along with its specifications. Impedance matching as well as buffer Darlington pair amplification. There's also a lot of information on how the gate drive and the amplifier, as well as the isolator, work. Design and specifications of three phase voltage source inverters can be found in the preceding section. We'll look at open and closed loop configurations of the designed hardware in the following section. Circuits for AC voltage and current sensing are briefly described along with the hardware that they use. To generate PWM firing pulses, a Xilinx FPGA is used in the program, which reduces the hardware and cost requirements. We'll talk about soft start mechanisms in this section to make the motor more efficient. As well as that, the system is calibrated.

4.1 SOFTWARE DEVELOPMENT

IP Core based VHDL Programming is used to develop the software. As a result of the following criteria, the VHDL language was chosen for software development.

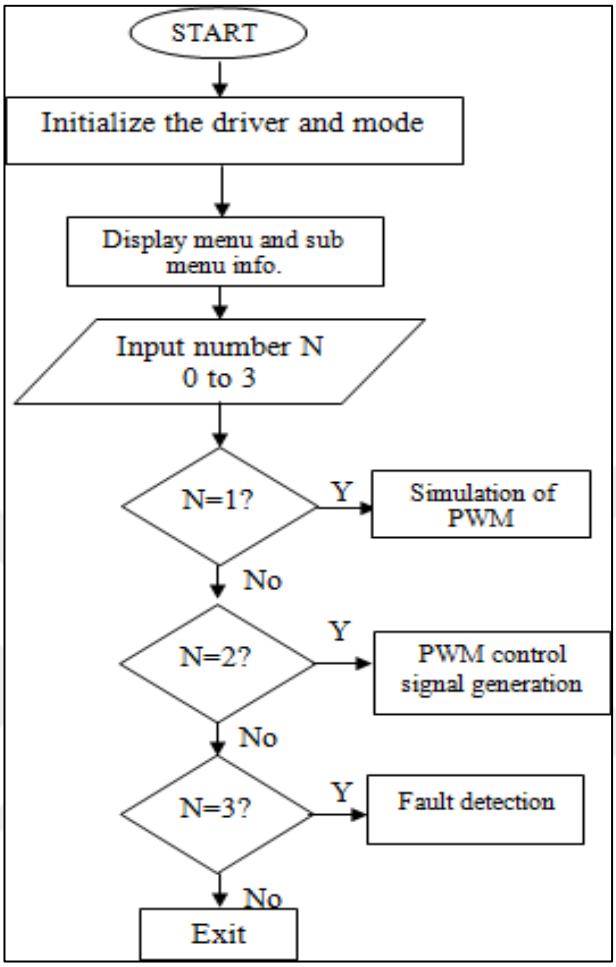

Figure 4.1: Flow chart of main program

4.1.1 Main Software Routine Flow Chart

The development of software is at the heart of this project. As a result, the system's basic flow sequence can be shown in this diagram. Figure 4.1 depicts the flowchart of the main program routine that was used to create the system software. It begins by configuring the drivers, menus, and modes of operation for displaying the information. When it gets to the second stage, it enters a number between 0 and 3 to wait for a task selection signal. The user must enter the number in order to proceed with the menu selection. According to the user's input, one of the menus is selected, such as modeling of the system or generation of control pulses or defect detection. It then enters sub-menus, where tasks are completed in accordance with the programmer's instructions.

4.1.2 PWM Generation Routine

The above flow chart is critical for simulation, PWM generation, and fault detection in the system. It's also at this stage that drivers are initialized, and I/O modes are selected for use. In order to simulate, generate PWM, and detect faults, you will need to provide a number in the range of 0 to 3. It will simulate programs written in Xilinx VHDL when the number 1 is entered. For example, if you enter number 2, the system will begin generating PWM signals for the voltage source inverter to fire. If the third button is pressed, the system will do a malfunction diagnosis. Another number would cause the program to exit its primary routine.

Because the software was built in Xilinx VHDL, it has the added advantage of being easier to modify and has greater flexibility with configurable approaches. The program will initialize the required drivers, and then the I/O modes and interrupts will be initialized after the controller driver initialization. For the drive to be operated slowly and gradually without jerks and sudden changes, the 5 Hz step input is used.

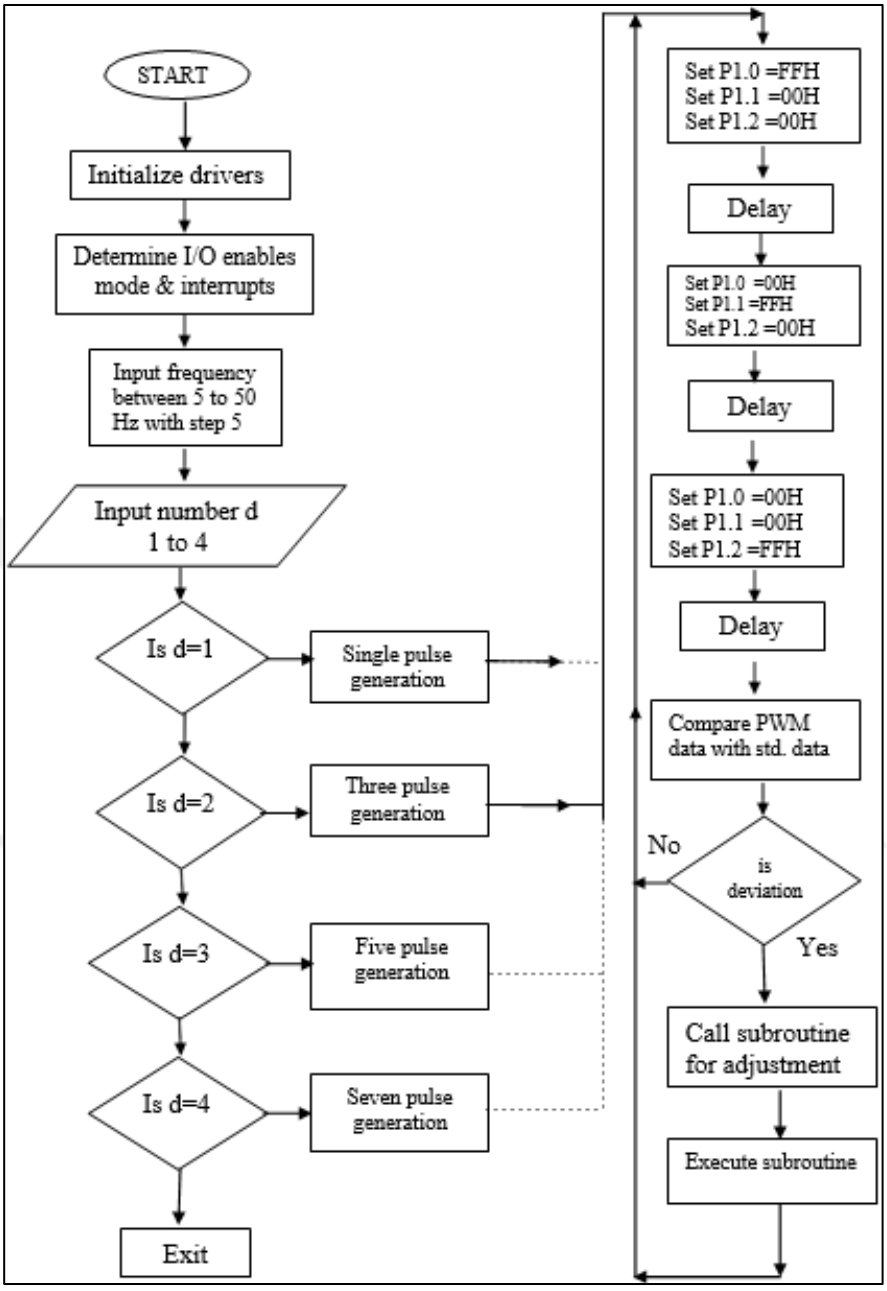

Figure 4.2: Flow chart of PWM pulse generation

When the frequency is increased by 5 Hz or even more, the stepping function is bypassed and the frequency is increased to 50 Hz. The drive will be able to vary its power in small increments with the help of the step function. PWM menu appears when the input value is received. It asks for how many pulses are in each third cycle. FPGA generates the PWM signal after selecting one of the options from 1 to 5. For three phases, a single PWM pulse is created every third cycle by selecting the first option. Before 1200 of a cycle's time period, P1.0's PWM signal is high compared to other

ports' (P1.1 and P1.2). From 1200 to 2400, P1.1's PWM signal is high compared to other ports' (P1.1 and P1.2). A pulse is created every third cycle, and the port signals are all generated simultaneously. It works in a similar fashion, generating pulses per third cycle by sequentially selecting any one option from 2 to 5. Upon finding a departure from the standard data stored in the random-access memory (RAM), the appropriate code will be called to rectify the parameter. Assembler is used to write all of the PWM generating subroutines.

4.2 SIMULATION OF THE SYSTEM ON AN FPGA WITH VHDL

This segment portrays the VHDL improvement process for Field-situated Control of a Three-Stage Engine. The objective of this segment of the task is to utilize the abilities of the VHDL language at the reproduction level to recreate and check the framework, as well as its signs and conduct. In view of the utilization of unsupported libraries and the utilization of another sort expected exclusively for reproduction, the code composed underneath isn't synthesizable.

Figure 4.3 shows how to describe the new reference frame in hardware using direct projections of the 3-phase vector. To try not to lose goal, the sign beta should be dealt with as genuine qualities until not long before simultaneous meeting, when it is changed over into a number worth.

```
entity clarke is
    port (  a, b: in integer;
            alpha, beta : out integer
            );
end clarke;

architecture behavioral of clarke is begin

alpha <= a;
beta <= integer(0.5774*real(a) + 1.1547*real(b));

end behavioral;
```

Figure 4.3: Transformation description in VHDL

Geometry is utilized as a Look-into Table to work out the transgression and cos upsides of a discrete theta esteem going from 0 to 359 degrees. To produce the cos esteem, an inward theta (theta 90) is made to get to memory 90 situations in front of the transgression signal.

Table 4.1: Trigonometry component description in VHDL

```
entity trigonometry is
    port (  clk, reset : in std_logic;
            address : in integer range 0 to 359;
            sin, cos : out real range -1.0000 to 1.0000
            );
end trigonometry;

architecture behavioral of trigonometry is

    type rom_type is array (0 to 359) of real range -1.0000 to 1.0000;
    constant rom : rom_type := (
    0.0000  ,
    0.0175    ,
    0.0349    ,
    0.0523    ,
    0.0698    ,
    -- . . .
    -0.0349    ,
    -0.0175
    );

    signal address_90 : integer range 0 to 359 := 89;

begin

process (clk) begin
    if(rising_edge(clk)) then
        sin <= rom(address);
        cos <= rom(address_90);
    end if;
end process;

process (clk) begin
    if(rising_edge(clk)) then
        if (address >= 269) then
            address_90 <= address - 269;
        else
            address_90 <= address + 90;
        end if;
    end if;
end process;

end behavioral;
```

The part that takes care of the three-stage inverter (s) with the (alpha, beta) signals from the Opposite Park change is Space Vector Heartbeat Width Balance.

Table 4.2: SVPWM description in VHDL (Architecture: state machine)

```
output_decode : process (state) begin
    case state is
        when s0 =>
            pwm_h <= "000";
            pwm_l <= "000";
        when s1 =>
            pwm_h <= "010";
            pwm_l <= "110";
        when s2 =>
            pwm_h <= "100";
            pwm_l <= "101";
        when s3 =>
            pwm_h <= "100";
            pwm_l <= "110";
        when s4 =>
            pwm_h <= "001";
            pwm_l <= "011";
        when s5 =>
            pwm_h <= "010";
            pwm_l <= "011";
        when s6 =>
            pwm_h <= "001";
            pwm_l <= "101";
        when s7 =>
            pwm_h <= "111";
            pwm_l <= "111";
    end case;
end process;

next_state_decode : with sector select
    next_state <=
        s0 when 0,
        s1 when 1,
        s2 when 2,
        s3 when 3,
        s4 when 4,
        s5 when 5,
        s6 when 6,
        s7 when 7;

state_decode : process (clk) begin
    if rising_edge(clk) then
        if reset = '1' then
            state <= s0;
        else
            state <= next_state;
        end if;
    end if;
end process;
```

Figure 4.4: SVPWM description in VHDL (Architecture: state machine)

The SVPWM's limited state machine shifts back and forth between eight potential states. Each state addresses an area (Figure 4.6). Every area is lined by two vectors that lead to a particular setup of IGBTs. The contrast between two neighboring vectors of a state is just a single piece, and this piece is weighted and driven on proc PWM exchanging at a decent recurrence (just for

reproduction purposes). The result signals are then directed to the 6-digit vectors that control the inverter.

```
sector_determination : process (clk) begin
    if rising_edge(clk) then
        if (reset = '1') then
            sector <= 0;
        elsif (v_beta >= 0) then
            if (v_alpha >= 50) then
                sector <= 3;
            elsif (v_alpha <= -50) then
                sector <= 5;
            else
                sector <= 1;
            end if;
        else
            if (v_alpha >= 50) then
                sector <= 2;
            elsif (v_alpha <= -50) then
                sector <= 4;
            else
                sector <= 6;
            end if;
        end if;
    end if;
end process;

proc_pwm_switching : process begin
    vector <= pwm_h; wait for 5us;
    vector <= pwm_l; wait for 5us;
end process;

s_buff(1) <= vector(0);
s_buff(3) <= vector(1);
s_buff(5) <= vector(2);
s_buff(4) <= not(s_buff(1));
s_buff(6) <= not(s_buff(3));
s_buff(2) <= not(s_buff(5));
s <= s_buff;
```

Figure 4.5: SVPWM description in VHDL (Architecture: behavioral)

Signal routing between code parts (functions, components, signals, ports) must be described in the top level file that collects all of them. To accomplish this, an instance of each of the FOC method's components must be instantiated (Figure 4.7). These modules run simultaneously, accomplishing one of the essential objectives of fostering a regulator in VHDL as opposed to programming.

```
inst_clarke : clarke
    port map (  a => i_a,
                b => i_b,
                alpha => i_alpha,
                beta => i_beta
                );

inst_park : park
    port map (  clk => clk,
                reset => reset,
                alpha => i_alpha,
                beta => i_beta,
                theta => theta,
                d => i_d,
                q => i_q
                );

inst_invpark : invpark
    port map (  clk => clk,
                reset => reset,
                d => v_d_ref,
                q => v_q_ref,
                theta => theta,
                alpha => v_alpha_ref,
                beta => v_beta_ref
                );

inst_svpwm : svpwm
    port map (  clk => clk,
                reset => reset,
                v_alpha => v_alpha_ref,
                v_beta => v_beta_ref,
                s => s
                );
```

Figure 4.6: Routing the components on the top level file

The stimulus signals are defined on the TestBench. Stimulus signals are used to test the Field-oriented Control as a whole in order to ensure that the system and all of its components are functioning properly. On (Figure 4.7), a three-phase generation is simulated, and a theta, which defines the period of the signals, is defined and calculated.

4.3 FLOW CHART OF MAIN SOFTWARE ROUTINE FOR STATUS OF THE DRIVE

In order to detect faults, the system follows the routine depicted in Figure 4.8. As well as initializing a driver, menus, and modes of operation, the program displays the program's title and relevant information. A message or audio message will be given to the user if there is no voltage present. Afterwards, it enters the corresponding even number between 0 and 8 into the task selection. The user must enter the number using the DTMF technique on the mobile receiver-transmitter. There are several options to choose from, such as simulation, pulse-generation, fault

detection and ON/OFF status of the motor. It then enters a specified menu and tasks are executed according to the program's directives.

The real software flow of the system is shown in Figure 4.8. The FPGA is initialized by declaring the input and output ports, as well as initializing the different drivers required for the FPGA's operation and operation. DTMF decoder receives the signal from the FPGA when a user makes a call to a mobile phone that is set to auto-answer mode and interfaced with the FPGA. There are several different key formats that are decoded by a decoder (see below). As soon as the user presses the key "1" on his phone, the DTMF decoder will identify the signal and send it to the FPGA. Single phasing voltage will be read into the FPGA. You'll receive an alert telling you that the motor cannot start because there is no phase voltage in the one or two-phase supply if there is a phase down. Next, we can retrieve information about the line voltage by hitting "2". If there is no line voltage, a voice message is sent to the mobile unit. As long as the line voltage is correct, the motor can be started by pressing the "4" button. It is possible to verify the status of the motor while the motor is running by pressing the "5" key.

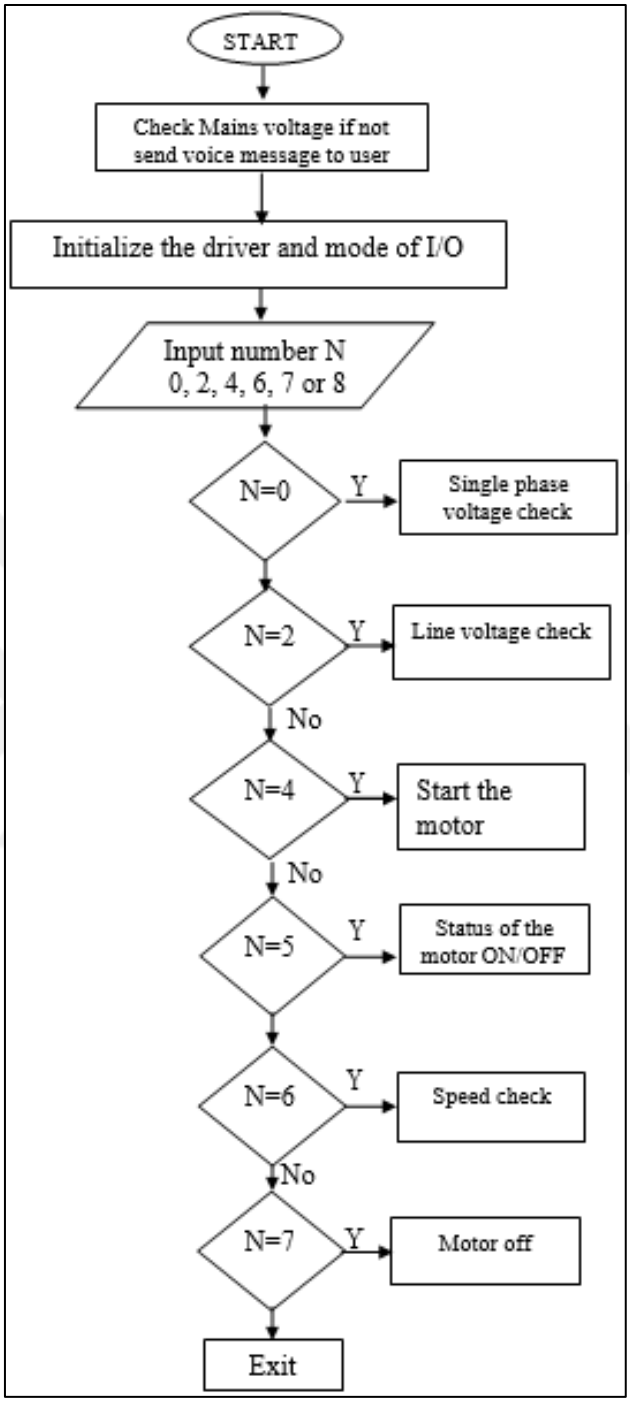

Figure 4.7: Flow chart of main program of status of drive

4.4 SOFT START CONCEPT WITH PWM

When any electrical machine is given sudden supply, it starts with jerk and some parts may get damage due to tearing and wearing effects. The temperature of the system may rise and damage of the system may lead to loss in the production of leading to failure of the machine. This may sometime lead to malfunction so rapid acceleration is dangerous for the machine or even the abrupt stopping. Changes in the starting currents may be up to 8 times the required current. The soft start mechanism provides the proper way of starting stopping of the machine. Surge currents are avoided. The soft start mechanism is used at the starting and after that it is bypassed.

As a result of this, practically all induction motors waste energy when they are first started up. Electric drives are likewise expected to consume the greater part of all power and 70% of all modern applications by 2050. Equipment and accompanying mechanisms can be damaged by overvoltage. The motor drive system's power consumption is reduced by using a soft start strategy. Improving the power factor helps to minimize the real demand for electricity in the early phases. Soft start reduces the peak current to 40 percent, preventing the need for large starting currents.. Graph of soft start versus hard start mechanism is shown in Figure 4.9.

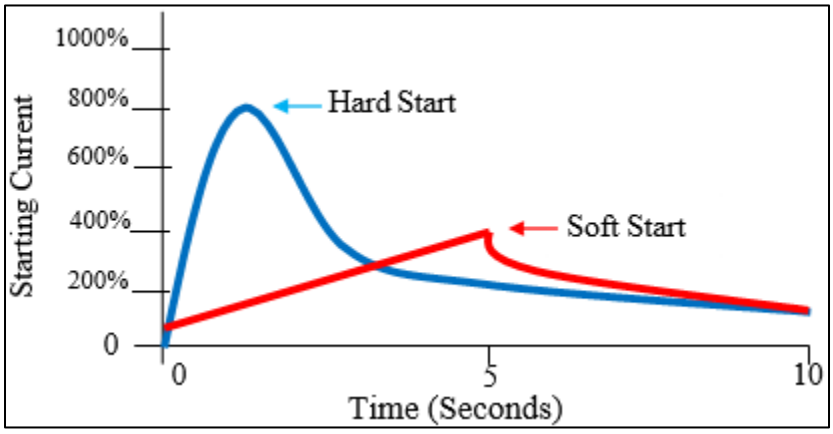

Figure 4.8: Performance of hard and soft start in two dimensions

In the current system, the voltage source inverter is started using a software-based soft start technique. A soft start mechanism has been bypassed when 90 percent power is reached in order to vary the pulse width progressively.

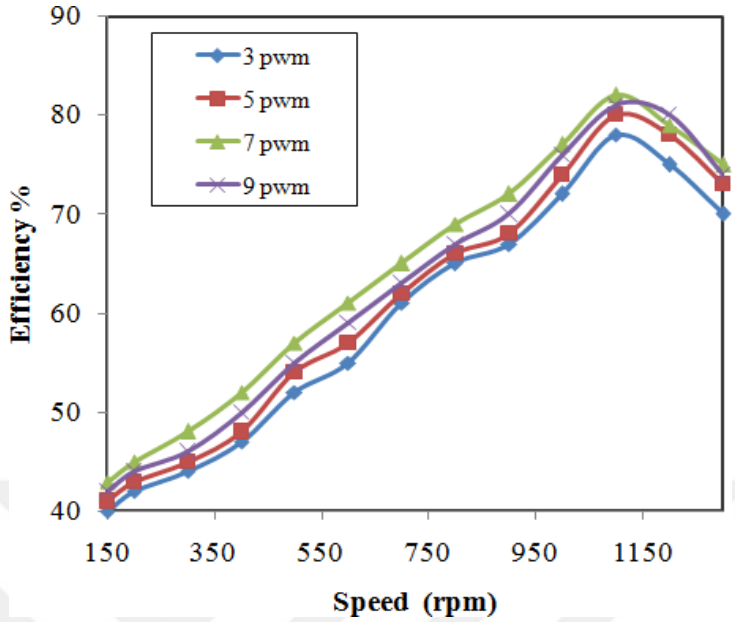

Figure 4.9: Speed efficiency characteristics of the drive

According to the graph in Figure 4.10, the efficiency of the machine increases with speed as a result of the motor's performance under different PWM approaches. Around 1100 rpm, it reaches its maximum and then begins to diminish as the speed increases. Up to 7 pulses in each half cycle, the total efficiency increases, but beyond that the efficiency declines. For the 11 PWM pulses, the efficiency was lower than the single PWM method. Since 7 PWM has a higher efficiency, this technique is the most ideal for firing the inverter and was employed to test this theory.

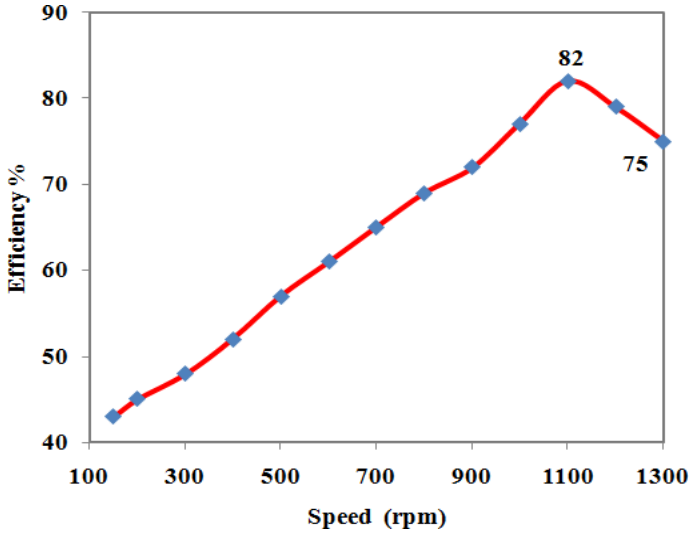

Figure 4.10: Speed efficiency characteristics of the developed drive

Its speed efficiency characteristics are shown in Figure 4.10. As can be seen from the graphs, efficiency increases linearly with speed. There is an upper limit to the efficiency at roughly 1100 revolutions per minute, but above that the efficiency starts to decline. It is owing to machine wear and tear and temperature fluctuations that the efficiency impact has changed, putting certain constraints on performance. Despite its efficiency, the drive is well-suited for the application.

4.5 CALIBRATION OF DEVELOPED SYSTEM

Due to instrument, human and environmental errors that may occur when observing data that may cause variation from the real value, calibration of the system is important to ensure accuracy of system. Because of this, it is vital to have a precision meter and a noise-free DC power source. The system may cause mistakes due to the aging of the components. For this reason, calibration is vital in order to avoid such inaccuracies.

4.5.1 Speed Calibration

Using an opto-coupler, which generates a pulse for every complete revolution, the real speed may be determined by counting the pulses for a certain time interval and then calculating the speed using software. Figure 4.12 displays the recorded voltage and felt speed characteristics. The non-linear information is obtained from the voltage variation at the beginning of the period. The software correction factor is used to make the features linear. The system is now suitable for experimentation once a second correction factor has been applied. On the graph, we can see the linear changes that have taken place. Figure 4.13: Speed voltage fluctuation characteristic.

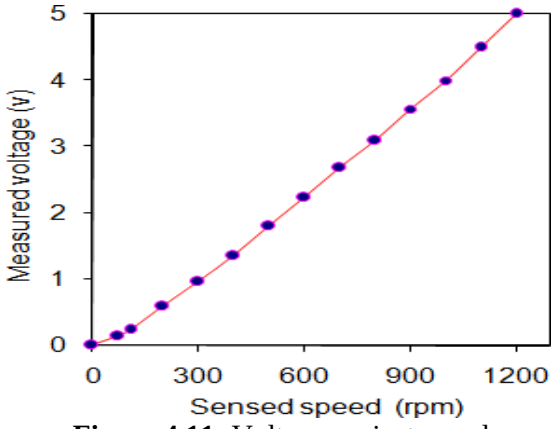

Figure 4.11: Voltage against speed

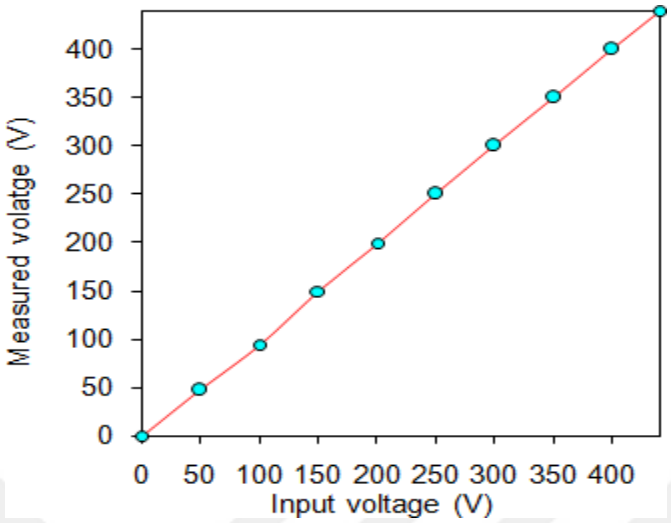

Figure 4.12: Calibrated speed characteristics

4.5.2 Voltage Calibration

Peak detector circuit measures the voltage of the system under examination, and the voltage is shown. Figure 4.14 shows the characteristics of the detected current and the input current, respectively. Linearity is evident in both input and output voltage variations. Observing the characteristic, the output voltage varies linearly in relation to a given voltage input. In spite of this, the initial output differs slightly from the input. This issue causes the input voltage to be read incorrectly. An input voltage correction factor is used in software programs in order to accurately depict actual value of the input voltage [1].

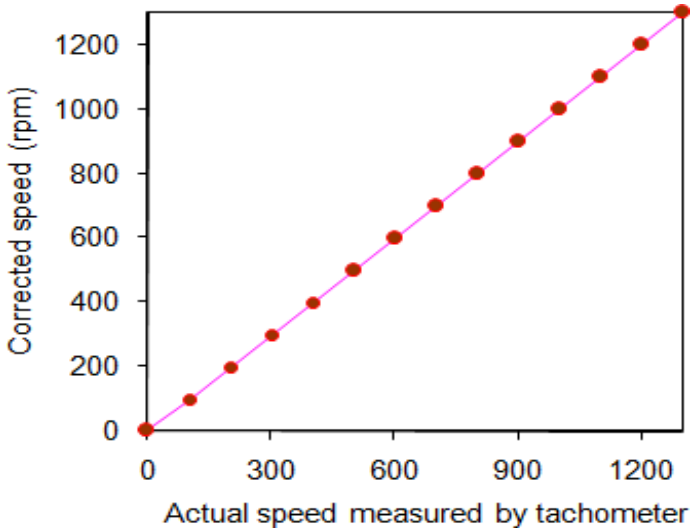

Figure 4.13: Measured (Sensed) voltage against input voltage

To conclude, from Figure 4.15 features, the FPGA's displayed correction fluctuates linearly with standard voltmeter-measured voltage.

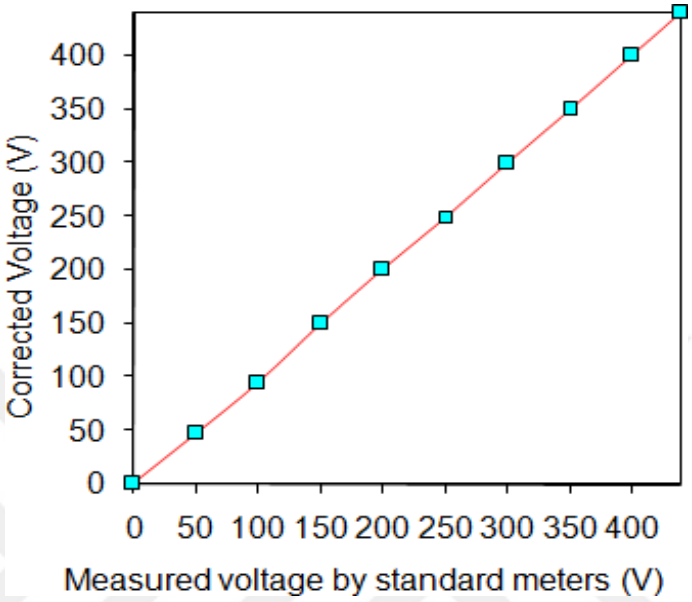

Figure 4.14: Calibrated voltage characteristics

4.6 CONCLUSION

In the early stages of the development of drive, there was a desire for power management, which led to a revolution in power control. The need for electric power control is mostly determined by the switching devices utilized in the particular control system in question. Techniques for switching and their handling have previously been refined with newer technology and gadgets. Many applications exist for advanced power control techniques, and it's difficult to define the bounds. Microprocessors, microcontrollers, PLCs, and personal computers are replacing traditional power devices in the development of control drives. Because of its stability and reliability, the power control technology alone has captured over 70 percent of the market. There has been a significant increase in the use of power electronic devices in drive technology. Initial power control growth was linear, but it has slowed down in recent years due to the rising demand for reliable power control, flexibility, and complexity

5. CONCLUSION AND FUTURE WORKS

5.1 CONCLUSION

The power control request existed in the early improvement of drive and persistently acquired the unrest power control. The interest for electric power control is for the not entirely set in stone by the exchanging gadgets utilized in the particular control framework. With cutting edge gadgets, exchanging strategies and taking care of have previously moved along. The use of cutting edge control strategies in power control has a large number of utilizations, making it hard to characterize the limits of force control applications. The latest thing in control drive advancement is moving away from customary power gadgets and toward chip, microcontrollers, PLCs, and PCs. As a result of its soundness and unwavering quality, power control innovation has caught almost 70% of the market. Power electronic gadgets are broadly utilized in drive innovation, which has filled in significance in the last quarter decade. Power control has filled consistently before all else, yet has as of late experienced nonlinear development because of expanded interest for solid control, adaptability, and intricacy.

Elite execution, control, and checking methods are broadly utilized in acceptance engine drives, which have acquired prominence because of their atomization. Quality execution is a central question that is perceived in numerous modern applications. The different control gadgets like the Programmable Rationale Regulator, Chip, PC (PC), and Microcontrollers assume a significant part in keeping up with the necessary degree of value and control.

AC drives are commonly used to regulate the speed of electrical motors. A rotating device of this type can be either an induction motor or a synchronous motor. AC drives, such as motors, are frequently used to power industrial machinery. The AC drives are also used in common appliances such as food blenders and drills. Despite the fact that these drives are not restricted to the previously mentioned applications, they assume a significant part in additional perplexing and troublesome conditions in most of uses.

Improving receptiveness in PLC frameworks can be achieved by consolidating the Double Tone Numerous Recurrence (DTMF) unit into the PLC, permitting admittance to the separate framework from anyplace on the planet. A controlling far off gadget speaks with the PLC used to

control the framework to perform remote observing of modern hardware. It turns into an essential necessity of framework improvement to persistently send orders to control the PLC-based control framework; in the event that orders are not gotten and executed by it, the framework will fall flat.

At the point when popular, it might require an elevated degree of soundness and trustworthiness. To guarantee that a framework disappointment doesn't create a setback for creation, the control framework is in many cases utilized couple with repetitive frameworks. When a system problem occurs, the working drive is automatically switched to the redundant drive. This switching makes use of both soft and hard redundancy. Soft redundancy is achieved by switching through PLC programming software.

Recently, the combination of an AC controller and an AC motor has emerged as the dominant drive system option. Traditional techniques are used to control the machines the majority of the time. Until now, most monitoring and control operations have been performed manually. Control gradually shifts from manual to mechanical, semiautomatic microprocessor, computer, and microcontroller-based systems. These systems evolved over time, laying the groundwork for remote control switching techniques. In view of their plan and speed control systems, AC drives are ruling the general commercial center all over the place. Notwithstanding, returning to the beginnings of the drive and related frameworks control and atomization advances in drives is entrancing and testing, and has gotten a ton of consideration. As the machine essentially affects day to day existence, it has been upset through various stages, including hand power drives, pull drives, mechanical drives, electromechanical drives, and electrical drives. Throughout the course of recent many years, there has been a critical change in science and innovation toward local area improvement using power drives. Be that as it may, electric drives are the most famous decision for all modern and vehicle drives, and they are broadly utilized in the movement business for different applications. Electric drive development patterns have been nonlinear previously. As per the patterns, electric drives are the most reasonable and promising drives in the movement business, with various benefits over traditional drives.

5.2 FUTURE WORKS

PWM reenactment is accomplished for a solitary heartbeat, three heartbeats for every third cycle, and five, seven, and nine heartbeats for each third cycle utilizing FPGA-based Xilinx natives

VHDL code. The reenactment thinks about consonant investigation and execution of different PWM procedures. Following examination, the best appropriate seven PWM strategy for inverter terminating was picked. Since the proficiency of the inverter diminishes as the quantity of switches increments past seven, for example for nine PWM. The seven heartbeat PWM proficiency and execution are prevalent, and the consonant items are fundamentally lower than in different techniques. Thus, the seven PWM conspire was picked for the MOSFET inverter terminating. The utilization of reproduction assists with diminishing the time and simplicity of building the expected equipment without genuine equipment testing, subsequently bringing down the expense. Recreation is fundamental for precisely planning the framework.

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