

**DEVELOPMENT OF A MULTI-CHANNEL
OPTICAL COMMUNICATION SYSTEM FOR
MRI GRADIENT, RF-TRANSMIT AND
RF-RECEIVE ARRAY CHAINS USING
FPGAs**

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE
OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR
THE DEGREE OF
MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

By
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August 2025

Development of a Multi-Channel Optical Communication System for
MRI Gradient, RF-Transmit and RF-Receive Array Chains using
FPGAs

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August 2025

We certify that we have read this thesis and that in our opinion it is fully adequate,
in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

DEVELOPMENT OF A MULTI-CHANNEL OPTICAL COMMUNICATION SYSTEM FOR MRI GRADIENT, RF-TRANSMIT AND RF-RECEIVE ARRAY CHAINS USING FPGAs

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M.S. in Electrical and Electronics Engineering

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August 2025

Modern Magnetic Resonance Imaging (MRI) systems are increasingly using array configurations for gradient, transmit, and receive chains due to their ability to improve imaging performance and spatial control. However, this introduces cabling complexity; array systems require multiple coaxial cables and dense on-coil electronics, leading to bulky cable assemblies and handling challenges. Long coaxial cables between the console and magnet rooms can heat up under high currents, change resistance, and be difficult to handle when placed near amplifiers or FPGAs. Moreover, RF chokes on coaxial help to reduce shield currents but increase the cable bulk, making handling difficult. Optical fibers, Small Form-factor Pluggable Plus (SFP+) or Plastic Optical Fiber (POF), are a good substitute as there are no conductive parts or currents traveling. Field-Programmable Gate Arrays (FPGAs) with built-in high-speed transceivers will be used to create an optical fiber communication network to facilitate the creation of the physical layer design. FPGAs built-in AXI 1G/2.5 Ethernet Subsystem library can also help create a data link layer design, which is proposed for the network layer. To reduce the cost of the system, a two-stage architecture is proposed with a spectrometer and distributor board communicating on SFP+ cables and the distributor and controller boards communicating on POF cables. This architecture can control multiple channels with reduced cost and cabling parameters. The SFP+ will work with the Ethernet Subsystem IP at 2.5 Gbps, and the network layer design will have decreased overhead. A simple Universal-Asynchronous Receiver Transmitter (UART) code will manage the POF part of the architecture, working at 20 Mbps or 100 Mbps. Simulation and Integrated Logic Analyzer (ILA) tests have been done to verify the design of each code block. Moreover, a complete working system showing Pulse-Width Modulation (PWM) waveforms for the gradient and

RF-Transmit chain and data storage and reconstruction on the console PC are demonstrated for the RF-Receive chain.



Keywords: FPGA, Optical Fiber, SFP+, POF, Gradient Amplifier, RF-Transmit Amplifier, RF-Receive Chain.

ÖZET

FPGA KULLANILARAK MRI GRADİENT, RF-İLETİCİ VE RF-ALICI DİZİ ZİNCİRLERİ İÇİN ÇOK KANALLI OPTİK İLETİŞİM SİSTEMİNİN GELİŞTİRİLMESİ

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Tez Danışmanı: Ergin Atalar

Ağustos 2025

Modern Manyetik Rezonans Görüntüleme (MRI) sistemleri, görüntüleme performansını ve mekânsal kontrolü artırma yeteneklerinden dolayı gradyan, iletim (transmit) ve alım (receive) zincirlerinde dizisel (array) yapılandırmalarını giderek daha fazla kullanmaktadır. Ancak bu yapı, kablolama karmaşıklığını artırmaktadır; dizi sistemleri çok sayıda koaksiyel kablo ve coil üzerinde yoğun elektronik bileşenler gerektirir; bu da hantal kablo montajları ve kullanım zorluklarına yol açar. Konsol ile mıknatıs (magnet) odaları arasındaki uzun koaksiyel kablolar, yüksek akımlar altında ısınabilir, dirençleri değişebilir ve amplifikatörler ya da FPGA'lara yakın yerleştirildiklerinde taşınmaları zor hale gelebilir. Ayrıca, koaksiyellerde kullanılan RF choke'ları (bobinler) zırh akımlarını azaltmaya yardımcı olur, ancak kablo hacmini artırarak kullanımını zorlaştırır. Optik fiberler — Küçük Form Faktörlü Takılabilir Plus (Small Form-factor Pluggable Plus, SFP+) veya Plastik Optik Fiber (Plastic Optical Fiber, POF) — iletken parça içermemeleri ve akım taşımamaları nedeniyle iyi bir alternatiftir. Fiziksel katman (physical layer) tasarımını kolaylaştırmak amacıyla, yerleşik yüksek hızlı transceiver'lara sahip FPGA'lar ile bir optik fiber iletişim ağı oluşturulacaktır. FPGA'ların dahili AXI 1G/2.5 Ethernet Alt Sistem (Ethernet Subsystem) kütüphanesi, veri bağlantı katmanı (data link layer) tasarımını destekleyebilir ve ağ katmanı (network layer) için bir tasarım önerilmektedir. Sistemin maliyetini düşürmek amacıyla iki aşamalı bir mimari önerilmektedir: spektrometre ile dağıtıcı (distributor) kartı arasında SFP+ kablolar; dağıtıcı ile kontrol kartları arasında ise POF kablolar kullanılacaktır. Bu mimari, daha düşük maliyet ve kablolama parametreleri ile birden çok kanalın kontrol edilmesini mümkün kılar. SFP+, 2,5 Gbps hızında Ethernet Alt Sistem IP'si ile çalışacak

ve ağ katmanı tasarımı daha düşük yük (decreased overhead) içerecektir. Basit bir Evrensel Eşzamanlı Olmayan Alıcı Verici (Universal-Asynchronous Receiver Transmitter, UART) kodu, mimarının POF bölümünü 20 Mbps veya 100 Mbps hızlarında yönetecektir. Her bir kod bloğunun tasarımını doğrulamak için simülasyon ve Entegre Mantık Analizörü (Integrated Logic Analyzer, ILA) testleri gerçekleştirilmiştir. Ayrıca, tam çalışan bir sistem sunulmuştur: gradyan ve RF-Transmit zinciri için Darbe Genişlik Modülasyonu (Pulse-Width Modulation, PWM) dalga form örnekleri; RF-Receive zinciri için ise konsol PC üzerinde veri depolama ve yeniden yapılandırma gösterilmiştir.

Anahtar sözcükler: FPGA, Optik Fiber, SFP+, POF, Gradient Amplifikatör, RF-Verici Amplifikatör, RF-Alıcı.

Acknowledgement

Firstly, I would like to thank Prof. Ergin Atalar for giving me the opportunity to complete my M.Sc. studies under his supervision. His continuous support, advice, knowledge, and experience helped me in this research and made me a better engineer than at the start of my studies. Moreover, I would like to thank my colleagues at UMRAM, especially Fatma Gul Uyar, Ege Aydin, Mehmet Emin Ozturk, Mehdi Ghasemzadeh, and Manouchehr Takrimi, who collaborated to support this thesis. I want to thank all the other group members of UMRAM who were always helpful. Furthermore, I would like to thank my parents and siblings, Baji, Umair, and Tayyaab, whose support and prayers were pivotal in my studies. I am grateful to them for believing in me and lovingly giving up whatever they had to for me to achieve this milestone. Lastly, I would like to thank all my friends, Abdullah Hannan, Haider Raheem, Mahnoor Aizad, Huzaifa bin Asad, and all the Brown Boys for being with me and supporting me throughout my time in Bilkent.

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Chapter 1

Introduction

Conventional Magnetic Resonance Imaging (MRI) employs whole-body coils for gradient, transmit, and receive chains to manipulate the spins of hydrogen protons to receive an MR signal, which can be reconstructed to get diagnostic images. To achieve more degrees of freedom, array coils for gradient have been the subject of research [2, 3], and RF-transmit arrays [4, 5] have also been introduced in recent years. RF-receive channels, supporting up to 128 channels [6, 7], have been commercially available for quite some time. However, integrating additional channels into the gradient, transmit, and receive chains introduces challenges, as bulky connectors and dense cabling complicate operation and handling.

To address these challenges, this thesis investigates the application of fiber-optic communication networks in MRI systems. Optical fibers offer an alternative to coaxial cables, capable of transferring multiple channels of information with fewer wires and eliminating the need for additional electronics to enhance the coupling between the controller boards and the cables. While efforts have been made to create a fiber optic channel for the receiver system [8], a comprehensive system for all three channels, gradient, RF-transmit, and RF-receive, has yet to be realized.

Therefore, this thesis aims to introduce a communication network to mitigate

the dense cabling issues inherent in current MRI systems. By utilizing the advantages of optical fibers, this work seeks to improve the efficiency and performance of MRI systems.

In conventional gradient systems, voltage and current requirements are astonishingly high, exceeding 2000 volts and 1000 amperes. Ultrahigh power amplifiers are placed away from the gradient coils, and power is carried using expensive cables. In the design currently under development by our research group, hundreds of small amplifiers are planned to be placed near the gradient coil. One of the design hurdles is handling cables leading to these amplifiers. The coaxial cables may pick up electromagnetic interference from fast-switching electronics, amplifiers, or FPGAs, affecting pulse-width modulation (PWM) waveforms.

Similarly, array configurations are introduced in RF-transmit systems to achieve spatial distribution of the RF field, providing greater degrees of freedom. Additionally, transmit arrays can generate implant-friendly modes and reduce the local and global SAR [9]. Studies have shown that to reduce the RF-induced heating, a series of chokes can be added to the coaxial cables to reduce cable shield currents [10] and minimize electric fields generated near the implant. These modifications increase cable bulk, making them difficult to handle in an array system as the number of channels increases.

Array configurations have been integral to RF-receive systems for quite some time. In the array configuration, the receive coils have on-coil electronics that sample the MR signal and send the digital data to the console PC for reconstruction. The inclusion of on-coil electronics increases coil density and bulkiness. These dense cables and electronics can shield the internal transmit array coils and interact with the gradient signals. Therefore, in addition to the aforementioned issues, the large number of cables with bulky connectors and baluns complicates handling of the array system cables.

Therefore, to handle the bulky cabling issues of the array configuration, this thesis proposes a method to control multiple channels with optical cables, and on-board smart amplifiers or FPGAs will convert the data to digital, and optical

fibers will be used to send the data between the console room and magnet room.

This thesis aims to develop an optical communication network for the MRI gradient, RF-transmit, and RF-receive array chains to mitigate challenges caused by bulky cabling. The proposed communication architecture employs a two-stage design. In the first stage, high-speed Small-Factor Pluggable Plus (SFP+) laser links serve as the primary optical backbone, while the second stage uses LED-driven POF or copper Ethernet connections to manage a larger number of channels and directly drive on-board amplifiers. FPGAs act as the digital interface between the MRI system and console electronics. They have built-in transceivers to accommodate high-speed communication, parallel processing capability, and built-in IPs, such as AXI 1G/2.5G Ethernet Subsystem IP, which will be used to directly control the transceivers for the first stage, and a protocol to control the data flow will be written. Custom UART code at a high baud rate will drive the second stage hardware. A generic code to control the flow and the addressing of the multiple channels is written to be adaptable for various numbers of output boards. Simulations and digital testing are done to verify the individual code blocks, and final verification is done by displaying the PWM waveforms on the oscilloscope for the gradient and RF-transmit array chains. For the RF-receive array chain, data reconstruction on the console PC was done.

The methods used to create this communication system and other hardware components, using the FPGAs and optical cables, will be discussed in Chapter 3. Moreover, the FPGA design components needed to make optical communication have also been described, and a complete working two-stage communication model is proposed. Chapter 4 verifies the working of the transceiver for the SFP+ part and the POF part individually using ILA. Moreover, simulations validate the working of the additional code blocks needed for effective communication within the FPGA. Finally, a complete working system for each MRI chain is validated using PWM waveforms for the gradient and RF-transmit chains. Data reconstruction on the PC for the RF-receive chain is shown to verify the working of the RF-receive chain. Furthermore, the discussion and conclusion of the whole thesis will be presented in Chapter 5.

Chapter 2

Background

This section provides the foundational background for this thesis. We begin by examining the fundamental principles of MRI and the essential hardware components of a conventional MRI system. Next, we explore recent advancements in array technologies across the MRI signal chain. Following this, we discuss the working principles of optical fibers. Finally, we discuss Field-Programmable Gate Arrays (FPGAs) and compare them with Central Processing Units (CPUs) and Application-Specific Integrated Circuits (ASICs).

2.1 Principles and Hardware of MRI

Magnetic Resonance Imaging (MRI) is one of the primary diagnostic procedures and has experienced rapid growth in clinical and research domains. It is a powerful non-invasive imaging system that can map and take images of nearly any internal structure throughout the body [11, 12]. MRI leverages the phenomenon of Nuclear Magnetic Resonance (NMR) to produce detailed images of the body. Conventional MRI imaging relies on the presence of hydrogen atoms for imaging, as it is the most abundant element in the human body. The hydrogen atom, the most abundant element in the human body, exhibits the MR phenomenon due

to its nuclear spin angular momentum [11]. In the presence of a strong external magnetic field, B_0 , along the z-axis (longitudinal direction), hydrogen spins align themselves parallel to the B_0 field [12]. An RF pulse, B_1 , is then applied in the xy-direction (transverse direction) at the Larmor frequency, at which the hydrogen atoms are resonating, causing the hydrogen spins to deviate from their alignment. This excitation results in the rotation of the net magnetization vector into the transverse plane [11, 12]. Once the B_1 field is removed, the net magnetization vector returns to the equilibrium state, emitting an RF signal, a process known as Free Induction Decay (FID). The NMR phenomenon is visualized in Figure 2.1.

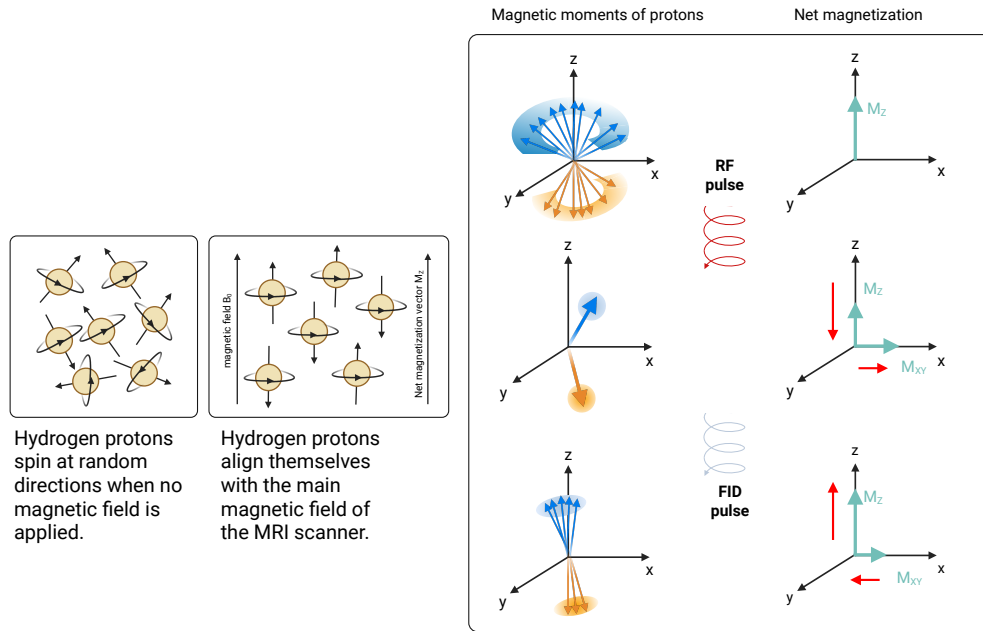


Figure 2.1: Step-by-step NMR process.

The detected signal represents a sum of all excited protons; however, this global signal cannot form an image without spatial encoding. Linear gradient magnetic fields, G , are added to achieve spatial localization, which makes the total field vary with position and time [11]. The equation describes the total magnetic field

at any point:

$$B(x, y, z; t) = B_0 + G_x(t) x + G_y(t) y + G_z(t) z \quad (2.1)$$

where B_0 is the main magnetic field, and G_x , G_y , and G_z are the gradient fields along the respective axes. The main static field is generated for clinical MRI using a superconducting magnet [11, 13, 14]. This strong, uniform magnetic field can provide high field strengths, 1.5 T–3.0 T and up to 7.0 T for clinical purposes [15] and up to 11.7 T for research purposes [16]. The RF system comprises an RF power amplifier and transmit/receive coils, to generate the RF fields and detect the NMR signal [14, 17]. Gradient coils generate three orthogonal gradient fields for slice selection, phase encoding, and frequency encoding gradients [18, 19]. These major components drive the MRI machine and help us get analytical images for diagnosis purposes. A conventional MRI system, other driving amplifiers, and electronic equipment are complete, as shown in Figure 2.2.

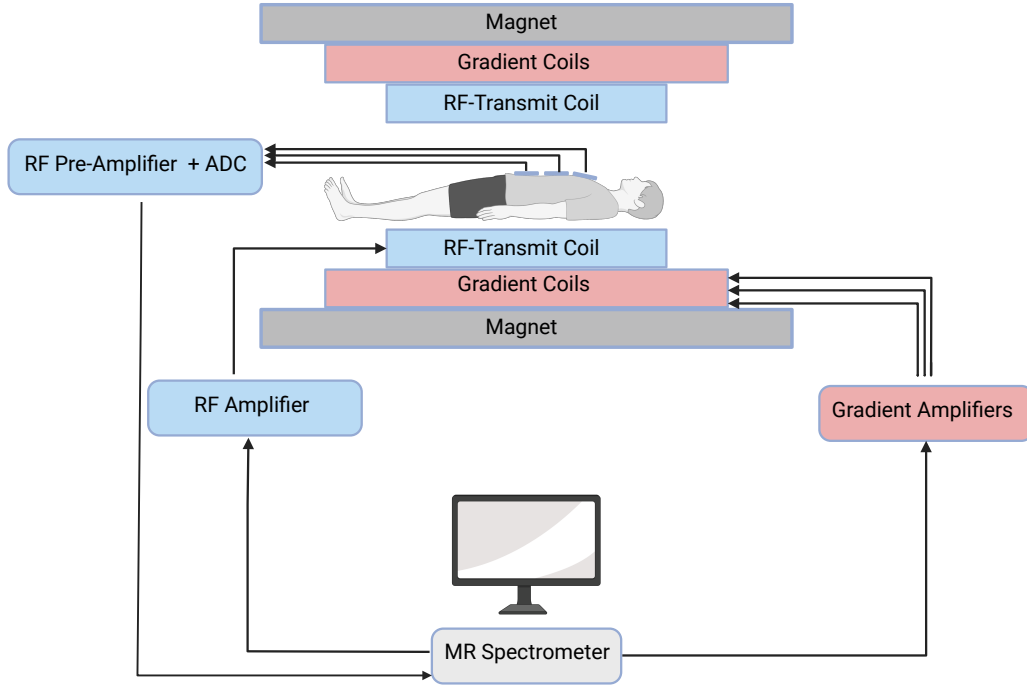


Figure 2.2: Conventional MRI hardware components block diagram.

Apart from the conventional techniques, significant advancements have been

made in gradient, Rf-transmit, and RF-receive chains. A key innovation is array technology, which replaces a single large coil with multiple smaller coil elements [3, 20]. This configuration enables more complex and flexible patterns. Conventional MRI hardware requires large amplifiers for the gradient and RF-transmit, capable of producing high current pulses for the whole body conventional coil. The RF-receive chain includes on-coil electronics and analog-to-digital converters (ADC) to sample MR signals and transmit them for image reconstruction. In the following subsections, we discuss array technologies for each component of the MRI chain. This thesis employs these array technologies in its experimental setup, and their communication frameworks will be detailed in later chapters.

2.2 Gradient Array Technology

Conventional gradient coils produce linear magnetic fields along the x, y, and z axes, creating spatial localization in the total magnetic field, and allowing specific slices to be selectively excited at the Larmor frequency. Although conventional coils produce linear gradient fields, gradient array coils allow for more complex gradients and customizable fields [21]. Gradient array coils comprise multiple small coil elements that can be individually controlled to produce complex spatial encoding schemes. They can also emulate conventional gradient coils by supplying uniform current to all elements, creating a linear gradient field. In this configuration, multiple coil elements are grouped in clusters and driven by compact amplifiers to achieve spatial localization at a specific region of interest (ROI). By adjusting the current in each element, this configuration supports linear and complex fields. The minimum current required to produce a specific field pattern is pre-calculated based on the number of array elements, along with their resistance and inductance. Another advantage is the ability to excite multiple slices simultaneously to allow for parallel imaging [22].

Each coil element is powered by its own Gradient Power Amplifier (GPA) with H-bridge topology [23, 22] or by modifying an audio amplifier [24]. These GPAs receive Pulse-Width-Modulated (PWM) control signals, which an FPGA

can send from the console room. Figure 2.3 shows an example of a simple H-bridge topology [20].

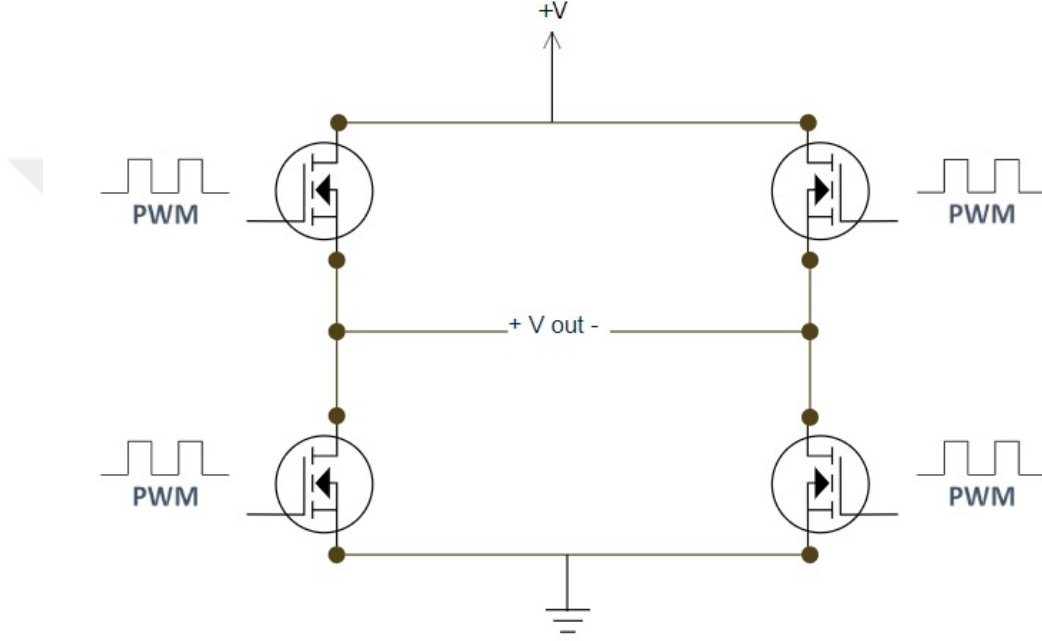


Figure 2.3: Simple schematic of an H-bridge amplifier for gradient applications.

The H-bridge output drives each coil element, which can be approximated as a first-order resistor-inductor (RL) circuit. However, real-world dynamics are more complex, requiring a trapezoidal current waveform to drive the coils accurately. The PWM waveforms act as inputs to the transistors, turning them on and off to create the required waveform. The PWM parameters, duty cycle, period, and dead time, are pre-determined based on the target B_0 field in the ROI, as well as the coils' resistance and mutual inductance [25]. The PC/console computes the necessary current profiles and generates PWM control signals for each channel of the gradient array. These PWM signals are transmitted from the console room to the gradient power amplifiers situated near the magnet.

2.3 RF-Transmit Array Technology

The RF transmit coil generates the B_1 fields at Larmor frequency, which tips the net magnetization vector onto the transverse plane. For this purpose, volume coils such as the birdcage resonator are commonly used [5]. These coils are tuned to the Larmor frequency of the hydrogen atoms, ensuring efficient excitation through resonance. While conventional coils only control RF phase and amplitude, multi-channel transmit arrays enable dynamic control over the spatial distribution of the B_1 fields [5]. This configuration improves RF excitation efficiency, reduces the specific absorption ratio (SAR), and introduces additional spatial degrees of freedom [26, 27]. Each independent coil element requires its own RF amplifier to control phase and amplitude precisely. The literature documents various amplifier designs, with the class AB RF amplifier being the most common type in conventional MRI scanners [28]. Switched mode amplifiers such as class D and E are also available [28], but they are nonlinear and their control requires special design. Class D and E amplifiers are well-suited for on-coil amplifiers [28, 29]. All these designs have some common characteristics, such as operating in a narrow band around the Larmor frequency of the hydrogen atoms and delivering up to kW of RF power [30]; however, their efficiency varies. Class-E amplifiers are highly efficient and operate with power transistors with matching circuits tuned to the RF coil. Whereas conventional amplifiers are kept in the console room, switch-mode amplifiers can be mounted directly on the coil, enhancing efficiency and reducing cable losses. Figure 2.4 presents a schematic of a conventional class-E amplifier, while Figure 2.5(A) depicts the transmit chain architecture.

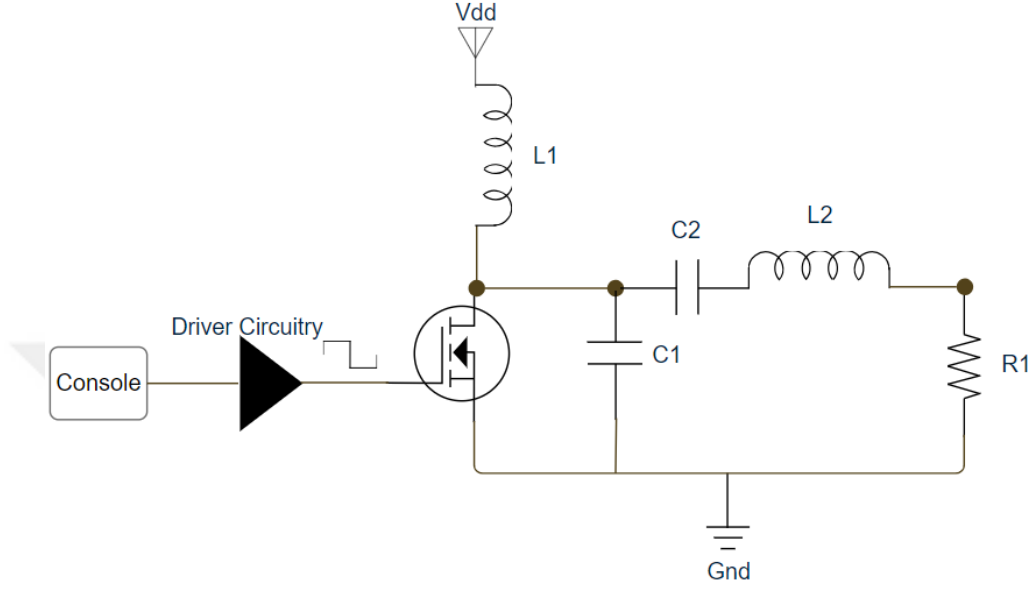


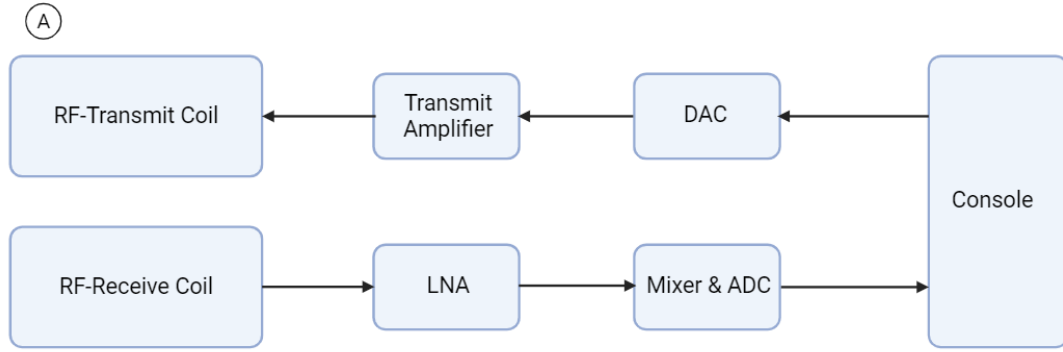
Figure 2.4: A schematic of a conventional Class-E Amplifier.

This design incorporates a shunt capacitor (C_1), including the parasitic capacitance of the transistor, to facilitate zero-voltage switching [30, 28, 29]. The L_1 inductor acts as a choke to isolate the DC supply, while the L_2 - C_2 network forms a resonant circuit tuned to the RF frequency [30]. A dedicated circuit generates PWM signals for transistor switching, which can be implemented digitally using FPGAs; this work has been done previously in UMRAM [29, 31]. The amplifier is controlled digitally, where an FPGA sends data to the gate of the transistor via the driver circuitry. The signals from the FPGA are LVDS, which are converted to single-ended and then pass through an op-amp with a specific gain and are connected to the transistor gate [29, 31].

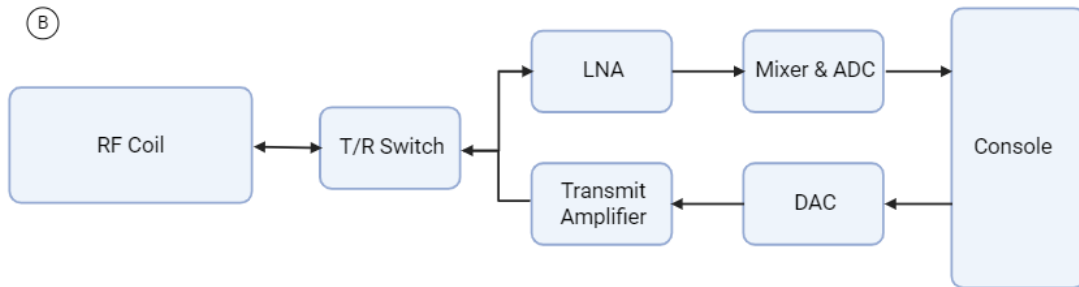
2.4 RF-Receive Array Technology

Once the RF pulse tilts the magnetization into the transverse plane, the relaxation process induces an alternating current in receive coils [32]. These receive coils may be receive-only coils or combined transmit/receive coils with a T/R switch, which

isolates the transmission path while receiving signals and vice versa. An RF coil functions as an LC circuit tuned to the Larmor frequency and designed to detect the weak MR signal emitted from the body. To improve signal integrity and reduce interference, receive coils employ shielding and decoupling components. Because the MR signal is very weak, each coil element incorporates a low-noise amplifier (LNA) to boost the signal, followed by a mixer to down-convert the high RF frequency signal to a lower intermediate frequency (IF). It then passes to an ADC, which samples and digitizes the MR signal for reconstruction on the PC [32]. Figure 2.5 presents a block diagram of separate receive and transmit channels (A) as well as a combined transmit/receive channel on a single coil (B).



(a) The console sends the RF transmission data to the DAC, RF amplifier, and the coil, and the receive coil receives the signal and sends it to the console using a preamplifier, receive amplifier + mixer, and ADC



(b) A combined Transmit/Receive coil and required hardware incorporated with a T/R switch.

Figure 2.5: RF transmit and receive block design.

The digitized data from the ADC typically travels over shielded coaxial cables or low-voltage differential signaling (LVDS) pairs to the console PC. Nonetheless, recent literature has explored alternative transmission methods, for example, digital RF-Over-Fiber Links for MRI receive coils [33] and wireless RF transmission [34].

2.5 Optical Fibers

A fiber optic cable transmits light by relying on the principles of refraction and reflection, specifically harnessing total internal reflection to confine light within the fiber core. When a beam of light strikes the interface between materials, part is reflected and the other is refracted; refracted light crosses the boundary, while reflected light remains within the original medium [35]. As the angle of incidence increases, the angle of refraction also increases, due to the differences in the refractive indices of the two media. Once the incident angle is greater than the critical angle, where the angle of refraction is 90° , then no light is refracted and all the light is reflected, and total internal reflection occurs [36, 37]. Figure 2.6 illustrates the principle of total internal reflection.

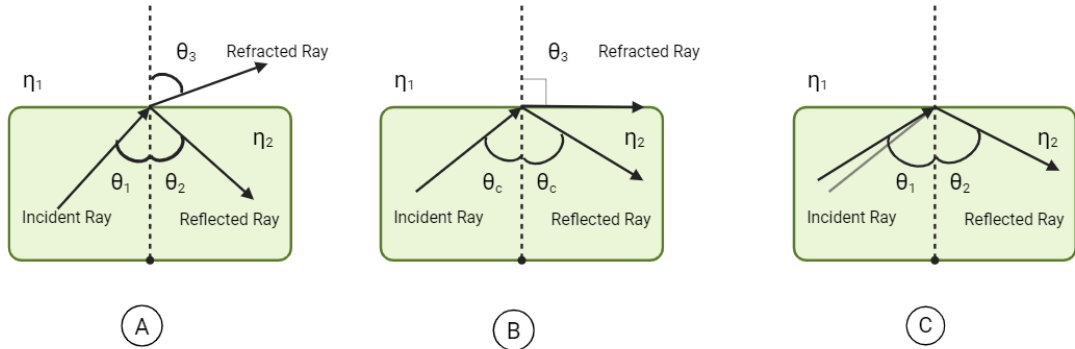
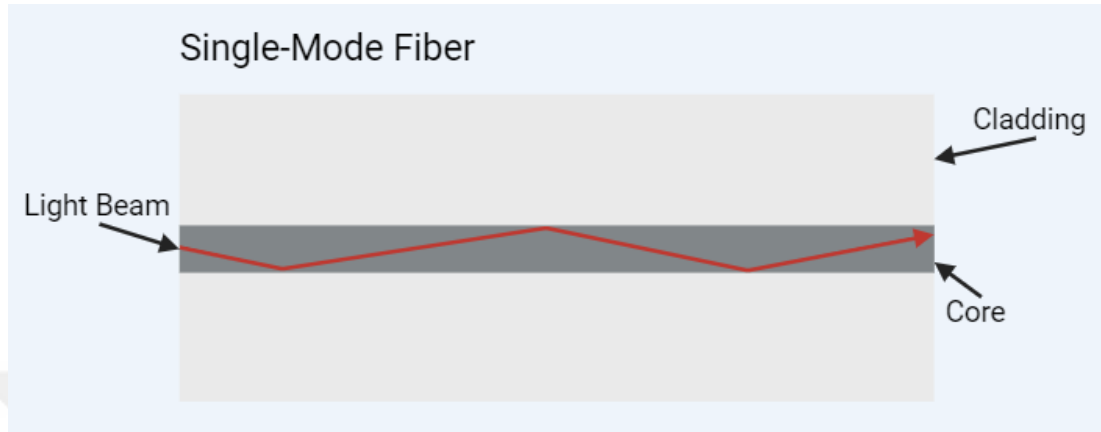
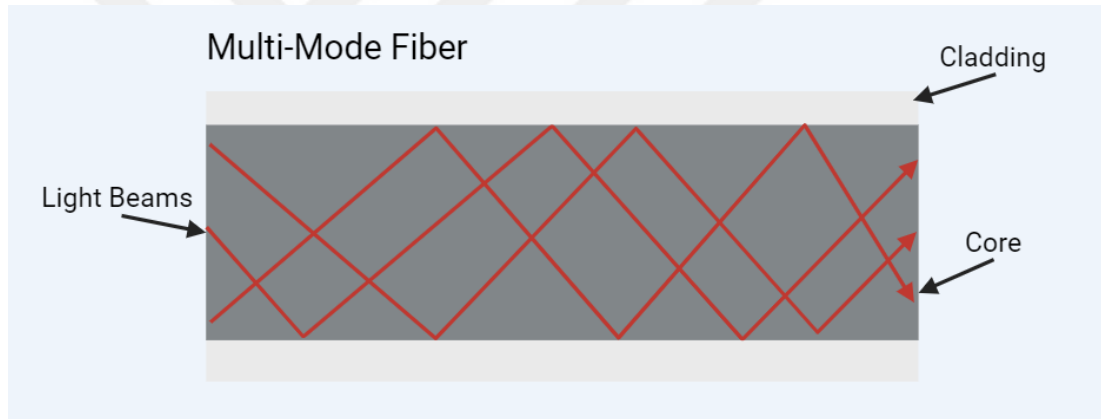


Figure 2.6: (A) Incident ray, reflected ray, and refracted ray at less than critical angles. (B) Incident ray at the critical angle at which the refracted ray is 90° . (C) The incident ray is greater than the critical angle when observing total internal reflection.

Fiber optic cable is more beneficial than conventional electrical systems as it has no conductive parts, making it immune to magnetic fields and ideal for MRI environments. With no current traversing the fiber and no conductive materials, there are no induced currents or forces, eliminating EMI artifacts. Therefore, replacing electrical cabling with optical fibers would make the MRI more reliable and artifact-free. There are two modes of fibers, Single-Mode Fibers (SMF) and Multi-Mode Fibers (MMF) [36]. SMF has a tiny core diameter ($< 10\mu\text{m}$) and a very large cladding; therefore, only one light ray is transmitted. MMF, on the other hand, has a larger core ($50\mu\text{m}$ to $60\mu\text{m}$) and a small cladding, allowing multiple light rays to travel simultaneously at different angles [36, 37]. Figure 2.7 illustrates the two modes of optical fibers and how the light propagates inside the core [36, 38].



(a) Light beam travelling within a single-mode fiber.



(b) Light beams travelling within a multi-mode fiber.

Figure 2.7: Comparison of a single-mode fiber vs a multi-mode fiber.

SMF can travel multiple kilometers without dispersion, while MMF can travel under a kilometer due to the dispersion effect [36]. There are two types of fibers which can be used, Glass or Plastic. Glass Optical Fiber (GOF) has a core made up of pure Silica (SiO_2) and the cladding is also made up of glass [38]. Plastic Optical Fiber (POF) has a core made up of a polymer material or polycarbonate, and the cladding is also made up of a similar material but with a different refractive index [39]. GOF components and tools are generally more costly and fragile compared to those used for POF.

2.6 Field Programmable Gate Arrays

Field-Programmable Gate Arrays (FPGAs) are integrated circuits composed of a grid of reprogrammable logic blocks. Unlike fixed-function ASICs or sequential CPUs, FPGAs offer reconfigurable hardware, enabling them to be reprogrammed in the field and tailored to different tasks. They are widely used for hardware acceleration in high-performance computing and prototype development [40]. Due to an array of logic elements and memory blocks, parallel operations can be done. They are commonly used in the telecommunications, automotive, and aerospace industries [40].

Configurable Logic Blocks (CLB), the fundamental building blocks of FPGAs, typically include logic gates, look-up tables (LUTs), and flip-flops [40]. Programmable interconnects link CLBs and I/O blocks, enabling designers to build custom routing paths for both internal logic and external interfaces using a Hardware Description Language (HDL) like Verilog and VHDL. I/O Blocks help to interface with external peripherals, and many new FPGAs have DSP blocks, internal Block RAM, and high-speed SerDes options [41]. Table 2.1 shows a comparison of FPGA, CPU, and ASIC:

Table 2.1: Comparison of FPGA, CPU, and ASIC features

Feature	FPGA	CPU	ASIC
Configurability	Reconfigurable	Fixed	Fixed
Parallelism	High	Massive	Optimized for specific task
Latency	Variable	Low	Low
Cost	Low	Moderate	High

Chapter 3

Methods

This section details the selection and roles of the two FPGAs and supporting hardware used in the thesis’s setup. The spectrometer FPGA was selected for spectrometer control and waveform generation, while the receiver FPGA was chosen based on requirements for optical channels, data throughput, and interface compatibility. We also reviewed prior networking models and developed a custom working model tailored to our two-stage optical communication system. Then, we present the proposed design components for the optical communication. Finally, we describe the integration of these components into the gradient, RF-transmit, and RF-receive chains.

3.1 FPGA Board & Supporting Hardware

Although all FPGAs provide general-purpose I/O (GPIO) for basic interfacing, some models include integrated multi-gigabit transceivers (MGTs) that enable high-speed serial communication over optical fiber. These dedicated MGTs convert parallel data to serial and transmit them via dedicated high-speed ports, supporting data rates from hundreds of Mbps up to tens of Gbps. The UMRAM

group selected the Kintex Ultrascale+ KCU-116 evaluation board as the spectrometer FPGA [42]. This board has 16 GTY (32.75 Gb/s) transceiver channels and four zSFP+ cages for optical interconnects, as shown in Figure 3.1 [42].

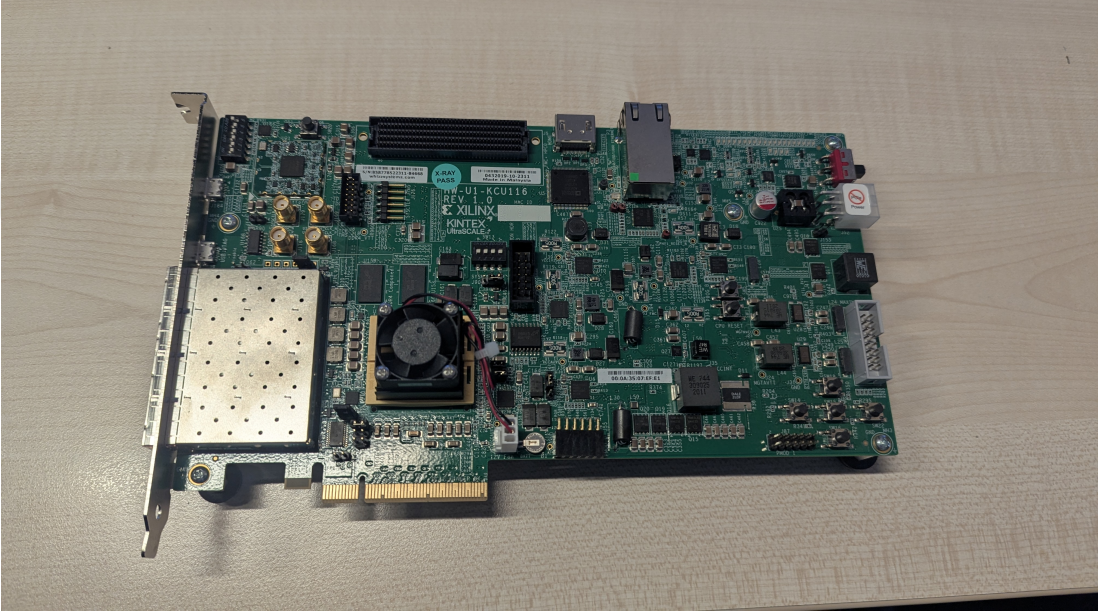


Figure 3.1: KCU 116 Evaluation Board.

Each zSFP+ cage on the KCU-116 board supports up to 28 Gbps line rates. SFP+ modules are compact, hot-swappable transceivers designed for fiber or copper links [43]. The zSFP+ cages require SFP+ modules, which convert an electrical signal to optical or vice versa. The optical module used here is the Broadcom AFBR-709SMZ multi-mode SFP+ transceiver [44], paired with multi-modal fiber optical cable for connectivity. These SFP+ components were chosen specially for this thesis to complete the high-speed optical stage of our two-stage communication architecture. Figure 3.2 presents the front and rear views of the SFP+ transceiver module.



(a) Front of SFP+ module showing the fiber inputs.



(b) Back of SFP+ module showing the copper connectors.

Figure 3.2: SFP+ Module AFBR-709SMZ

Figure 3.2a illustrates the SFP+ module's optical interface on the front side, while Figure 3.2b shows the rear side with its 20-pin differential serial I/O and control/power pins. Detailed pin assignments are listed in Table 3.1.

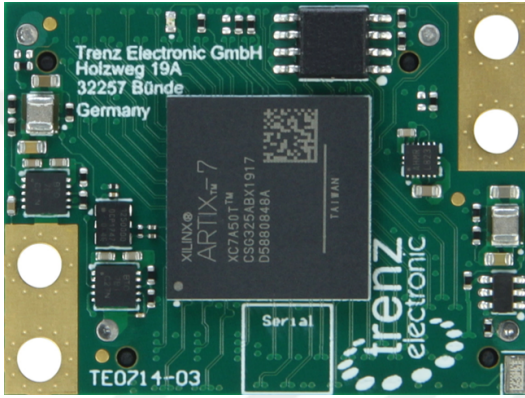
Table 3.1: SFP+ Module Copper Pin Functions by Group.

Group	Pins and Descriptions
Power	VccT (Pin 16), VccR (Pin 15)
Ground	VeeT (Pins 1, 17, 20), VeeR (Pins 10, 11, 14)
TX Data	TD+ (Pin 18), TD- (Pin 19)
RX Data	RD+ (Pin 13), RD- (Pin 12)
Control	TX Disable (Pin 3), TX Fault (Pin 2), LOS (Pin 8), RS0 (Pin 7), RS1 (Pin 9), Mod-Abs (Pin 6)
I^2C	SDA (Pin 4), SCL (Pin 5)

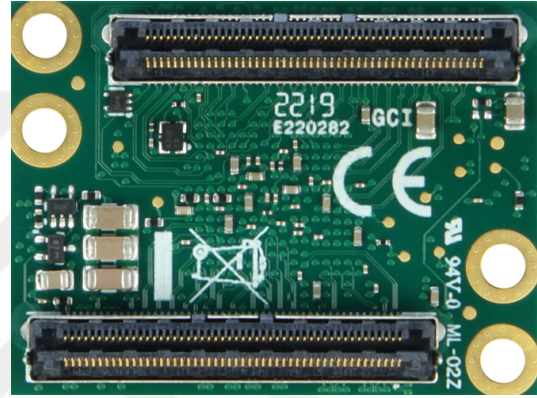
The SFP+ module transmits and receives laser-based signals, converting them to and from electrical signals. Its operation can be verified via oscilloscope measurements or monitored digitally using the FPGA’s Integrated Logic Analyzer (ILA). The power and ground pins supply a 3.3V supply to both the transmitter and receiver sides, with separate pins to isolate the two. The TX and RX Data pins carry the module’s differential serial data streams for transmission and reception, respectively. The control and status signals allow module management and fault detection. TX Disable disables laser transmission when driven high. TX Fault indicates a transmitter fault. LOS indicates receiver loss of signal. RS0 and RS1 pins are optional rate select pins, but are generally unused. Mod-Abs asserts when no module is present inside the cage. I^2C interface supports EEPROM management and diagnostics monitoring.

The KCU-116 FPGA is strong as it has a very powerful chip, offering high-speed I/O capability, 1GB DDR4 memory, multi-gigabit transceivers, and high-performance logic [43]. We refer to this as the **Spectrometer board** throughout this thesis. It handles all gradient, RF-transmit, and RF-receive array channels, which justify its high-performance FPGA and I/O capability. The UMRAM group previously selected this board; this work focuses solely on evaluating its optical-communication capabilities. The spectrometer board will send digital data to the array amplifiers. Hence, the array amplifiers also need a smart chip to decode the digital data and convert it into analog data, and an SFP+ transceiver

interface to receive and drive analog outputs. Previously, Basys 3 was considered due to availability, but it lacks transceiver capability; therefore, a different FPGA was required. The TE-0714 FPGA Module by Trenz Electronic [45] was selected as a cost-effective solution supporting SFP+ reception and GPIO interfacing, shown in Figure 3.3.



(a) Top side of the TE-0714 Evaluation Board.



(b) Bottom side of the TE-0714 Evaluation Board.

Figure 3.3: TE-0714 FPGA Evaluation Board.

The TE-0714 features four MGTs and approximately 138 GPIOs, which can support multiple channels. It has board-to-board (B2B) connectors to mount onto a baseboard. The TEBB-B0714 from Trenz Electronic [46] provides multiple GPIOs and includes an SFP+ cage. The baseboard is shown in Figure 3.4.

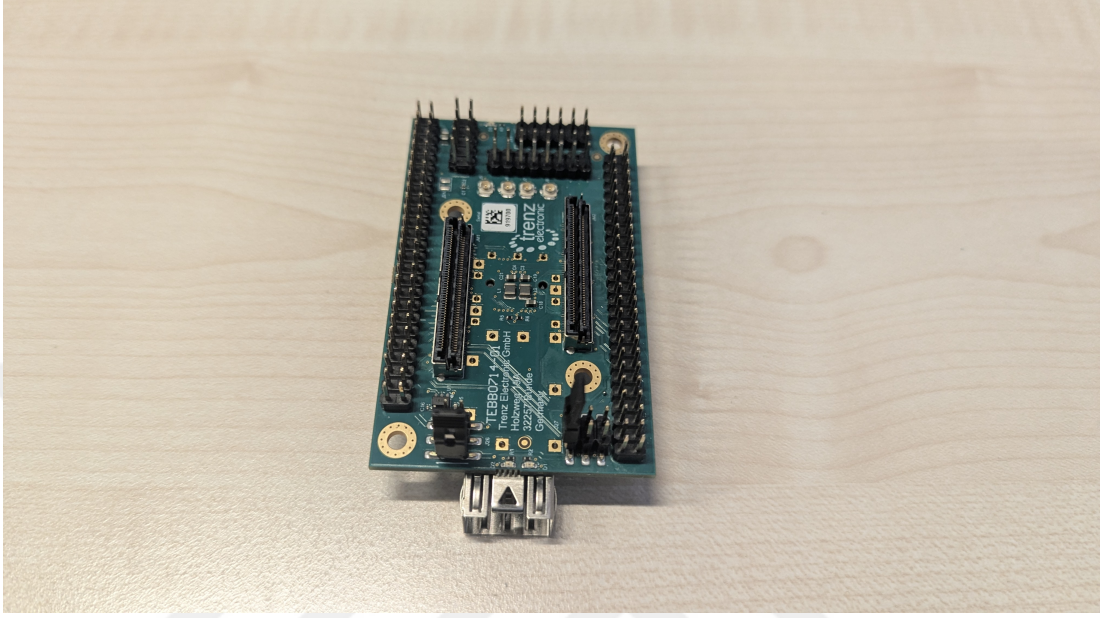


Figure 3.4: TEBB-0714 Baseboard for TE-0714 FPGA Evaluation Board.

We refer to these as the **Controller board**. The spectrometer board and controller boards need to communicate via an optical cable. The controller board generates the PWM waveforms to drive channel amplifiers, receives MR data from the RF receiver, and sends it back to the spectrometer board.

However, the controller board’s GPIO capacity is limited for high channel count. Scaling with multiple controller boards would require numerous costly SFP+ transceivers, driving up system cost. Therefore, we introduce a third board, the **Distributor board**. It receives data via SFP+ from the spectrometer board and distributes it to multiple controller boards via lower-cost POF or ethernet cable. This two-stage architecture ensures high channel count while keeping it cost-effective, since the POF requires cheaper optical hardware. Moreover, due to this design, the controller boards do not need high-speed optical transceivers and can use simpler boards, such as a custom baseboard with the TE0714 FPGA board or the Basys 3 evaluation board [47]. Figure 3.5 illustrates this two-stage optical system.

In this architecture, the spectrometer board sends data, via SFP+, to one or

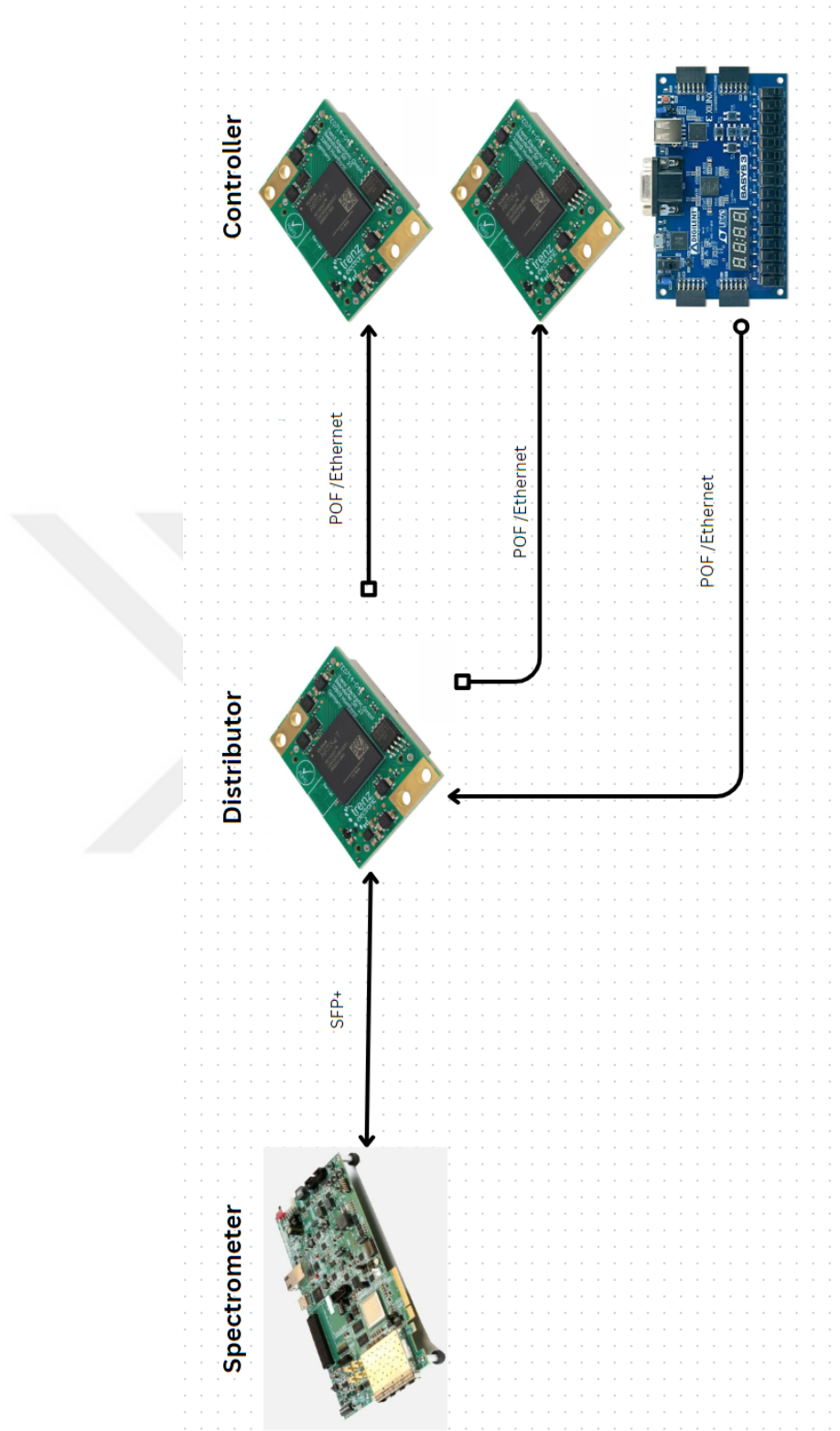


Figure 3.5: Proposed two-stage optical system block diagram.

more distributor boards, depending on channel counts. Each distributor board then forwards the data to the controller boards via cheaper POF or ethernet cables with less speed than the SFP+. These controller boards will manage the amplifier boards or MRI hardware components. For the second stage of the proposed optical system, an LED transmitter, IF-E99B [48], and a photodiode receiver, IF-D91B [49], are used with POF, enabling data rates up to 80 Mbps. Figure 3.6 shows an integrated transmitter-receiver module for these components created by Ege Aydin [1].

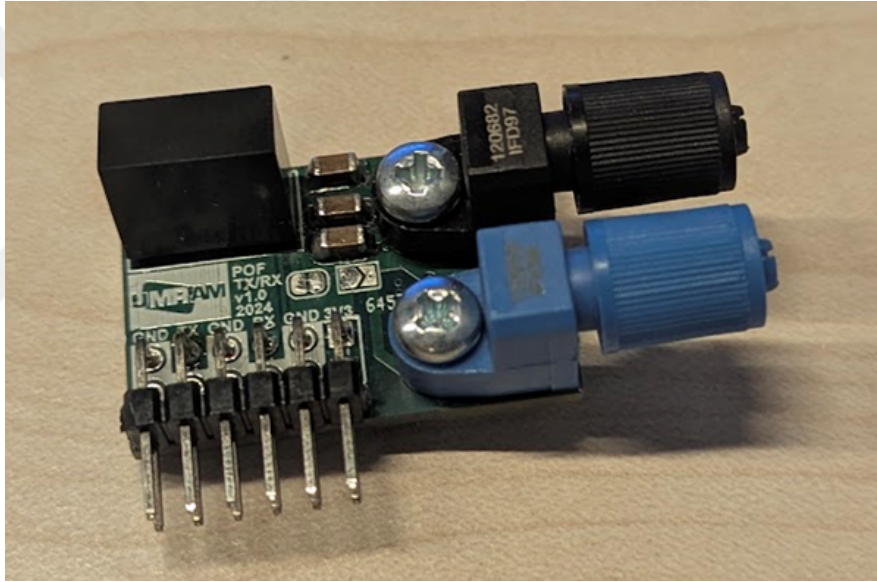


Figure 3.6: POF Transceiver Module custom-made in UMRAM by Ege Aydin [1].

The POF module is in a PMOD-compatible form that can be directly plugged into the PMOD ports of FPGA evaluation boards, such as Basys 3. The pin assignments are shown in table 3.2.

The POF module's PMOD connectors use a 12-pin layout compatible with standard PMOD ports. Most pins are ground or power; only two transmit and receive data lines enable direct access from FPGA logic.

Table 3.2: POF Module Pin Functions by Group

Group	Pins
Power	3.3V (Pin 6,12)
Ground	GND (Pins 1, 3, 4, 5, 7, 8, 9, 10, 11)
Transmit	TX (Pin 2)
Receive	RX (Pin 4)

3.2 Networking Model & IPs

The first step in developing an optical system was to select the hardware, which is discussed in section 3.1. The next step is to specify the data flow through the physical medium and its coordination through FPGA-based logic. FPGAs include built-in IP cores, such as transceiver controllers and Ethernet subsystems, to simplify the implementation of network layers. However, it is a prerequisite to understand how to control the transceiver, how different devices communicate, and how networking between devices occurs. This section contains some foundational background on networking layers, protocol-level communication, and FPGA integration strategies. Finally, we present a unified networking model for each MRI array subsystem (gradient, RF-transmit, RF-receive) with FPGA IP block details and interconnect structure.

3.2.1 7-layer OSI Networking Model

Networking systems follow a layered model, such as the seven-layer OSI framework, to standardize communication and simplify system design. Moreover, each layer handles specific responsibilities, which can be modified independently, improving modularity. This division enables each layer to implement standardized protocols, e.g., Ethernet on the data link layer, IP at the network layer, TCP at the transport layer, etc.

The first layer is the physical layer, which handles the transmission of raw bits via signals, voltage, or light, over a physical medium such as coaxial or fiber optic cables. It defines parameters such as encoding scheme, duplex mode, data rates,

and hardware characteristics like pin definitions and voltage levels [50]. In this design, the physical layer includes ethernet PHY chips and SFP+ transceivers modules. The second layer is the data link layer, which organizes raw bits into frames and ensures reliable transmission by providing error detection [50] and medium access control (MAC). In this design, implementations include FPGA-based MAC IP cores. The third layer is the network layer, which handles packet routing across multiple networks, using logical addressing such as IPv4/IPv6. It determines optimal paths and manages packet forwarding. Standard protocols at this layer include IP addressing, ICMP, etc [50].

In this design, the physical layer includes the SFP+ and POF modules and the FPGA transceivers. The configuration of those transceivers, such as clock control and serialization, belongs to the data link layer. The network layer design is crucial for the distributor board, which routes data from a single SFP+ cable to multiple POF channels of the controller board. Table 3.3 extends this view to include higher-level layers [51].

Table 3.3: 7-Layer Networking Model

Layer	Description
7. Application Layer	Human-computer application layer for end-user applications; provides services like HTTP, FTP, SMTP directly to software
6. Presentation Layer	Translates and formats data (e.g., encryption/decryption, compression)
5. Session Layer	Manages communication sessions between applications; handles connection setup and termination
4. Transport Layer	Ensures end-to-end communication reliability; handles segmentation, error recovery, flow control
3. Network Layer	Routes and forwards packets through multiple networks; uses logical addressing and routing protocols
2. Data Link Layer	Defines the format of data on the network; handles framing, MAC addressing, flow, and error control
1. Physical Layer	Transmits raw bit streams over physical media

While the first three layers form the foundation of our optical communication network, the remaining upper layers are typically handled within software or FPGA firmware. The transport layer (layer 4) manages data transport and checksums. Session layer (layer 5) manages communication sessions. Presentation layer (layer 6) manages data packaging, which the spectrometer board implements (another project by Mehmet Emin). Lastly, the application layer (layer 7) handles the human-computer interactions. The FPGA firmware within Vivado handles these layers.

3.2.2 Proposed Design Components for SFP+

FPGAs provide multi-gigabit transceivers (MGTs) for high-speed optical communication, which can be configured via built-in IP cores or custom HDL code blocks. All FPGAs have the Transceiver Wizard IP [52], which simplifies transceiver configuration through user-friendly presets and helper blocks. These are part of the FPGA chip, and require correct clocking, reference inputs, and alignment to operate reliably. Other IP blocks—such as DDR controllers or clocking modules—coexist on the device. Although transceiver IP availability varies across FPGAs, they share functional similarity. The IP can be configured with a preset or configured manually according to an industry standard. This IP operates at the physical layer (layer 1), handling raw bit transmission with serialization/deserialization.

Built atop the transceiver IP is the AXI 1G/2.5G Ethernet Subsystem IP [53], which supports 1Gbps and 2.5 Gbps modes and provides an AXI4-Stream interface to facilitate better data handshaking. It integrates the PHY transceiver and MAC blocks and operates at the data link layer (layer 2). It handles frames encapsulation and validation using error detection schemes [53]. Figure 3.7 shows the internal block diagram of the Ethernet Subsystem IP.

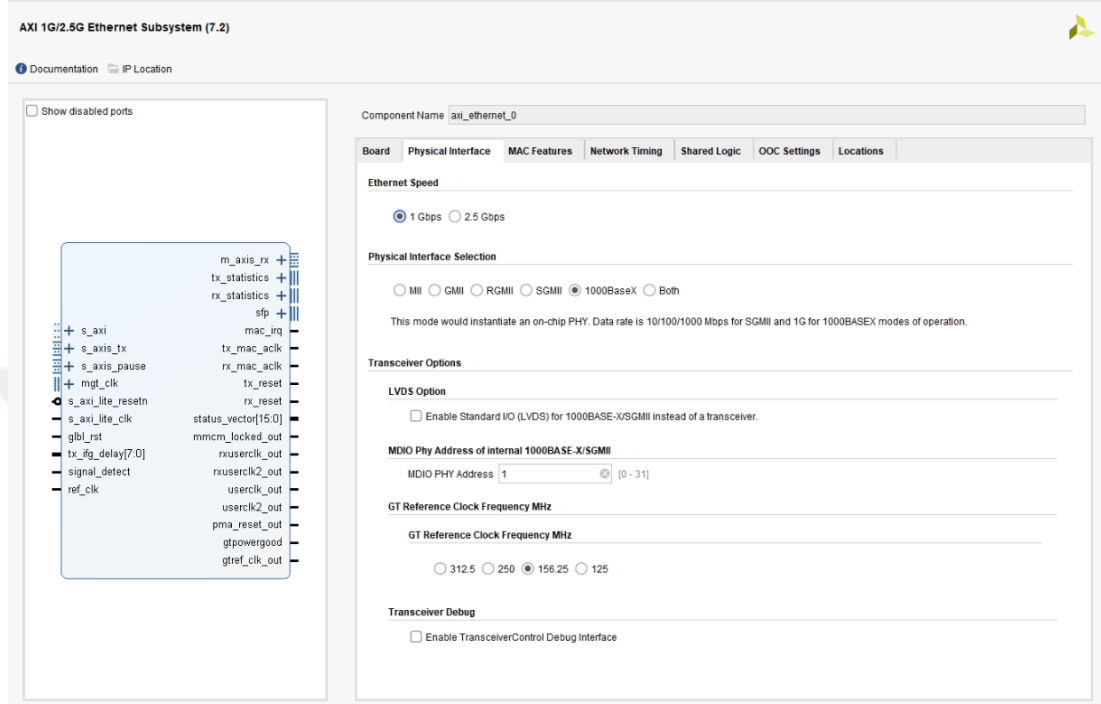


Figure 3.8: Configuration Setup of the AXI 1G/2.5G Ethernet Subsystem IP.

The correct configuration is crucial to ensure reliable and error-free data transfer between FPGAs. The same settings must be applied to the distributor board FPGA to maintain compatibility. A stable reference clock should be chosen to properly align serializer/deserializer timing, which is critical for safe communication. FPGA families vary in transceiver clock rates; some offer adjustable clocks, while others have fixed frequencies. Other tabs help to add more features to the IP, but they were left empty to allow only the basic configuration and more flexibility in the communication. Another important tab is the transceiver location tab, which selects the transceiver to use. As discussed in section 3.1, the KCU 116 provides 16 transceiver channels and 4 zSFP+ cages; therefore, transceiver to cage mapping is essential, which can be found in the documentation [42] or through manual IBERT test, discussed in section 4.1.

Moreover, the communication is asynchronous, meaning there is no shared clock, so the receiver must rely on embedded synchronization patterns to detect bit boundaries. Therefore, a standard protocol or preamble is necessary. The

input frames must adhere to the ethernet protocol rules explained in IEEE 802 Ethernet Standard [54]. This standard encapsulates the data with additional header and trailer frames that handle addressing and checksums to ensure reliable delivery and standardization. A standard ethernet packet comprises the following fields [54]:

- **Preamble:** 7 bytes
- **SFD (Start Frame Delimiter):** 1 byte
- **Destination Address:** 6 bytes
- **Source Address:** 6 bytes
- **Length/Type:** 2 bytes
- **Data (Payload):** 46–1500 bytes
- **Frame Check Sequence (FCS):** 4 bytes

The preamble is a bit pattern for clock synchronization between the sender and receiver. It is a series of fixed patterns that help the receiver to find the center of the incoming signal to sample it properly. The SFD is a fixed byte known by both the sender and receiver that the following data will be the proper payload. The FCS is a 32-bit CRC check for detecting transmission errors, which the MAC layer computes and verifies automatically. The MAC IP, inside the AXI 1G/2.5G Ethernet IP, automatically handles the preamble, SFD, and FCS generation, so they do not have to be supplied by the user. The network layer, or the user, provides the rest of the byte items to interpret and route data. Therefore, an interface needs to be designed for the network layer over this IP, which can control the communication and addressing of the payload. The destination and source addresses identify the receiver and sender's hardware address. The length/type field indicated either the payload's length or protocol type, e.g., IPv4, ARP, etc. The payload field contains the data that needs to be transmitted, which is length-constrained between 46 and 1500 bytes. Payloads outside this range are

not accepted, leading to issues with the error handling mechanism. These four fields are the task of the network layer, and they can be utilized in any way by just abiding by the main rule that the total bytes should be within the minimum and maximum limits. Therefore, a custom format can also be implemented to better utilize the channel for this application.

The ethernet standard framing introduces more overhead that becomes inefficient when sending small, frequent data to many endpoints, impacting synchronization across high channel counts. Therefore, an alternative approach is discussed in section 3.3. Furthermore, the essential fields, the preamble, the bits, and the CS, are provided by the IP, so when designing the network layer, a custom protocol can be utilized, giving more freedom and accommodating a higher number of channels in a single packet.

The ethernet subsystem IP uses AXI4-Stream format for high-throughput data flow. Another IP input is in AXI4-Lite format, which controls the internal memory elements of the IP, but only if necessary. AXI4-Stream is ideal for packet-based communication through FPGA logic. The block that sends the data is called the master block, and the block that receives the data is called the slave block. It has four essential signals:

- **Tdata:** 1 byte
- **Tvalid:** 1 bit
- **Tready:** 1 bit
- **Tlast:** 1 bit

The tdata field has the primary payload data that must be sent to the slave block. tvalid is asserted by the master block when the data is ready, and it acts as a signal to the receiver that the payload data on the tdata line is valid. tready is asserted by the slave block when it is ready to accept the data. Payload data is only transferred if both tvalid and tready are high. The master block asserts tlast

to indicate the end of the payload data and acts as a packet boundary. These four signals will help to communicate between VHDL blocks easily and efficiently.

3.2.3 Proposed Design Components for POF

As covered in Section 3.2.2. SFP+ interface operates via the AXI 1G/2.5G Ethernet Subsystem IP. However, the POF cannot support those high speeds. The required speed for the second stage is significantly lower, as discussed in Sections 3.3 & 3.4. Therefore, another approach is required to communicate between the distributor and controller boards. A Universal Asynchronous Receiver/Transmitter (UART) communication standard is proposed for that purpose. UART is an asynchronous serial protocol with separate wires for TX and RX, enabling full-duplex communication [55]. UART frames follow this structure:

- **Start bit** (logical '0')
- **Data bits** (e.g., 8 bits)
- **Optional Parity bit** (for basic error detection)
- **Stop bit** (logical '1')

In idle mode, the communication line is held high. Transmission begins with a start bit, pulling the communication line low and indicating to the receiver to begin sampling. Data bits are sent LSB first, optionally followed by a parity bit, then a stop bit pulls the communication line to high. The data rate, or baud rate (bits per second), is predetermined by both the transmitter and receiver and is crucial for correct transmission. The receiver monitors the transmission line, for a falling edge, to begin sampling at defined intervals. To accurately align with the bit boundaries, receivers oversample the incoming signal with a higher clock, usually x8 or x16, than the baud rate, and sample the data near the bit center to ensure accurate alignment of the incoming data. Once the stop bit is detected,

the UART logic flags the byte as valid and outputs it. Optional error detection is also done if parity is enabled.

Many FPGAs include built-in UART cores with fixed baud rates and simple interfaces. Typical built-in UART modules support standard baud rates like 9600 baud, or 115200 baud rate, approximately 100kbps. Because this design requires higher data rates, as discussed in the later chapters, we developed a custom UART code to support variable and elevated baud rates. The custom code supports dynamic baud rate configuration and is reusable for multiple applications. Figure 3.9 illustrates the flowchart of our custom UART transmitter. The complete VHDL source code is available in the project's GitHub repository (<https://github.com/aliomhammad/Thesis-code.git>).

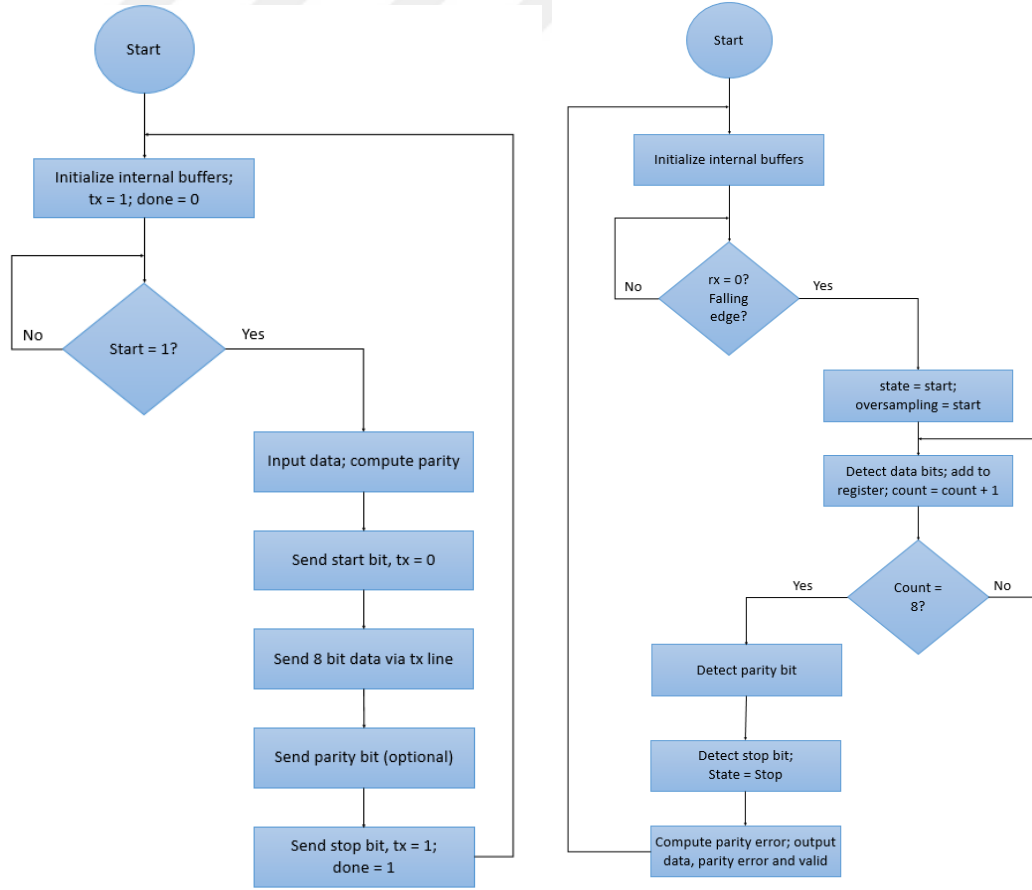


Figure 3.9: UART flowchart blocks.

As shown in Fig. 3.9a, the transmission line is held high. When a transmit request arrives, the transmitter sends a start bit (pulling the line low), announcing the beginning of a frame, followed by the data bits (LSB first). Optionally, it calculates and sends the parity bit after the data bits, and then sends the stop bit (returning the line high). Finally, a done flag is raised to acknowledge the completion of transmission, and the code reverts to the idle state and waits for new data. Figure 3.9b shows the receiver flowchart; upon detecting a falling edge, it begins oversampling at bit intervals, samples at midpoints, reconstructs the byte, optionally verifies the parity, and outputs the data. Finally, a valid flag is raised to signal the availability of the data, and the code reverts to monitor the transmission line for new incoming data.

3.3 Gradient & RF-Transmit Channel Integration

The subsequent architecture and data handling methods apply similarly to both the gradient and RF-transmit channels. The spectrometer board receives the data from a pulseq file [56], parses per-channel waveform parameters, formats them, and stores them in memory. This work was implemented by Mehmet Emin Ozturk. This data encodes the PWM information for each channel amplifier’s gate signals. Each channel requires **16-bit** data, which embeds the PWM information. Thus, channel data is structured as fixed-width 16-bit words. With data generated every 1 μ s, the minimum data rate required is 16 Mbps per channel. As noted in section 3.2.2, ethernet frames require at least 60 bytes with address information and payload, even if the payload data is very small, 2 bytes. This inefficiency motivates designing a custom networking layer approach.

Instead, our new approach defines a custom ethernet frame where each channel’s data occupies a fixed position within the payload, eliminating the need for separate address sections and reducing protocol overhead. It is a type of Fixed-Length Field Multiplexing where multiple data streams are combined onto a

single transmission channel. This enables packaging data from multiple channels in one frame, with fixed positions pre-defined and known by both transmitter and receiver. This reduces the overhead introduced by using the Ethernet protocol, which adds multiple bytes of address information for small payloads. This type of multiplexing is used in the telecommunication sector with Time-Division Multiplexing and Frequency-Division Multiplexing standards [57].

For this purpose, a code block in VHDL was written that takes the data from the memory for multiple channels and places it in a register. In the design, each channel is assigned 32 bits, for both positive and negative PWMs, concatenated with a one-byte header. To satisfy ethernet's minimum frame length requirements, padding is done only when the constructed payload is too short. Figure 3.10 illustrates the top-level ports of the code block.

```
entity custom_framing is
  Generic (
    Channels : integer := 1;
    Datawidth : integer := 32
  );

  Port (
    clk : in std_logic;
    reset : in std_logic;
    comments : in std_logic;

    nchannel_tdata : in std_logic_vector(Datawidth*Channels-1 downto 0);
    nchannel_tvalid : in std_logic;
    nchannel_tready : out std_logic := '0';

    frame_tdata : out std_logic_vector(7 downto 0) := "00000000";
    frame_tlast : out std_logic := '0';
    frame_tready : in std_logic;
    frame_tuser : out std_logic_vector(0 downto 0) := "0";
    frame_tvalid : out std_logic := '0'

  );
end custom_framing;
```

Figure 3.10: Top Level ports of the new framing VHDL code block.

The top-level module includes two generic values, "**Channels**" and "**Datawidth**", that set up the design for different hardware configurations. The clk, reset, and comments inputs are the control signals. The nchannel_tdata,

nchannel_tvalid, and nchannel_tready are inputs for all the channels that follow the AXI4-Stream format. The frame_tdata, frame_tvalid, frame_tready, and frame_tlast are the outputs of this block in burst mode, also in the AXI4-Stream format; frame_tuser is ignored. A flowchart showing the working of the code is provided in Figure 3.11. The complete VHDL source code is available in the project's GitHub repository (<https://github.com/aliomuhammad/Thesis-code.git>).



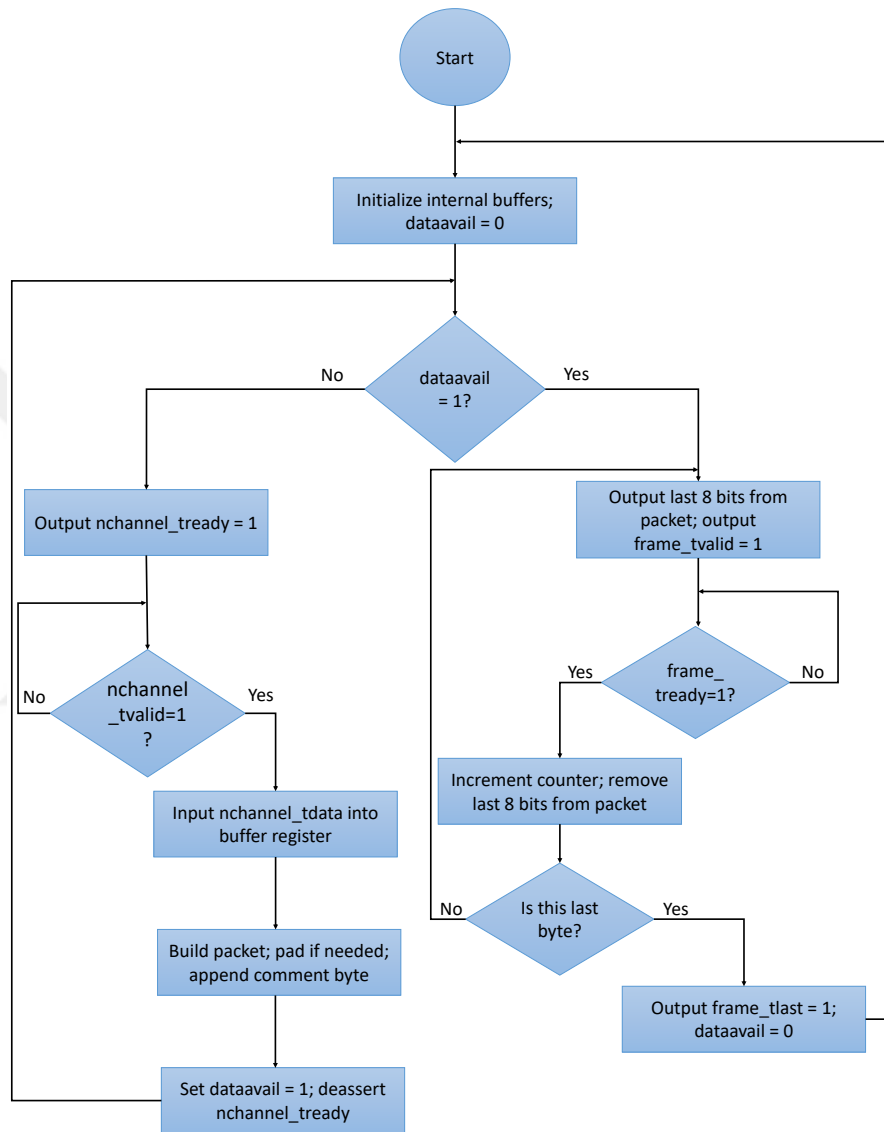


Figure 3.11: Custom framing block flowchart.

After reset, the code initializes all registers and control signals. Next, the module checks for new data. If available, it asserts the AXI control signals, loads

the data into a buffer, applies padding, if required, and appends the comment byte. It then waits for the ready control signals to be asserted. Then it transmits the frame byte-by-byte, tracking progress with a counter to prevent overruns. Once the counter reaches the total number of bytes to be sent, the tlast control signal is asserted with the last byte to mark the end of the frame. An internal reset clears the buffers and registers, and the logic loops to await new data.

This framed data is then transmitted through the optical fiber from the spectrometer board to the distributor board. The frame is parsed at the receiver to remove the padding and extract the comments byte. A symmetric de-framing VHDL module performs this. The spectrometer board's role in this chain is complete; further tasks will be discussed in Section 3.4. The distributor board then slices the received data to extract individual channel information for forwarding over the POF links. Therefore, another code block is required at the distributor board, which will forward the data to the channel outputs. This module shares the same channels and datawidth generics as the transmitter and must match identically to ensure correct data transfer. The flowchart for the custom de-framing code is shown in Figure 3.12. The complete VHDL source code is available in the project's GitHub repository (<https://github.com/aliomhammad/Thesis-code.git>).

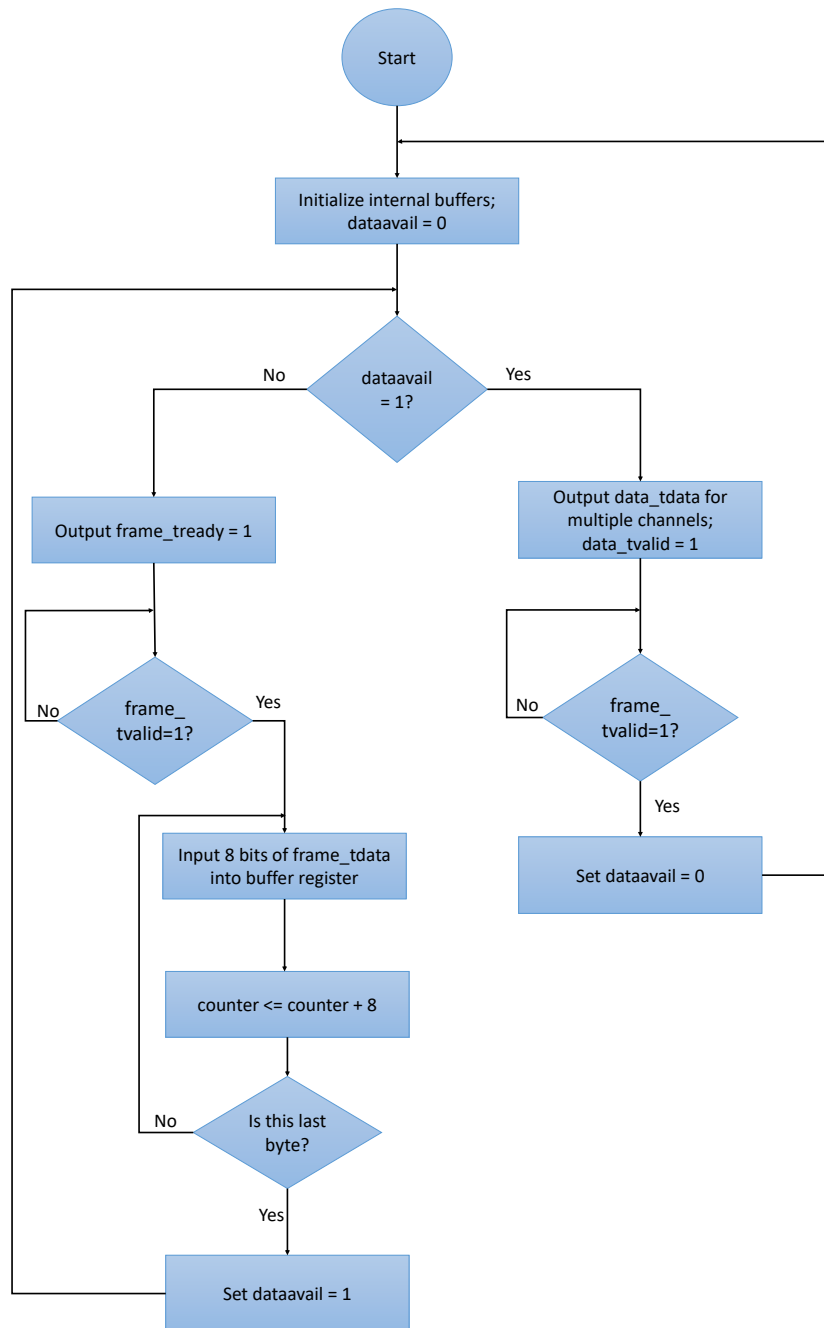


Figure 3.12: Custom de-framing block flowchart.

Upon reset de-assertion, the module initializes all internal registers and control signals. Then it will check if the data is available in the registers; if not, it will

assert the AXI control signal, `tready`, to initiate receiving the data. Data arrives one byte at a time until the `tlast` signal is asserted and the internal counter confirms that the full frame has been received. Once all the data is obtained and stored in a buffer, it de-asserts the input control signals and asserts the output control signals. Then, the module performs an internal reset of registers and control signals, returns to the initialization stage, and awaits new data; this cycle continues for each frame. The received data retains the same framing structure as transmitted by the spectrometer board. The distributor board then slices the packet and forwards it to the relevant channel via POF link.

Data forwarding over POF uses the custom UART developed in Section 3.2.3. Each channel requires 16 Mbps, and a single controller board handles four amplifier boards, so the minimum baud rate is 64 Mbps. The design targets a 100 Mbps UART baud rate for framing overhead, headers, and trailers. An intermediate module reads the data and forwards its contents one byte at a time to the UART transmitter, asserting the start pulse for POF transmission. Figure 3.13 shows this data forward code's flowchart. The complete VHDL source code is available in the project's GitHub repository (<https://github.com/aliomuhammad/Thesis-code.git>).

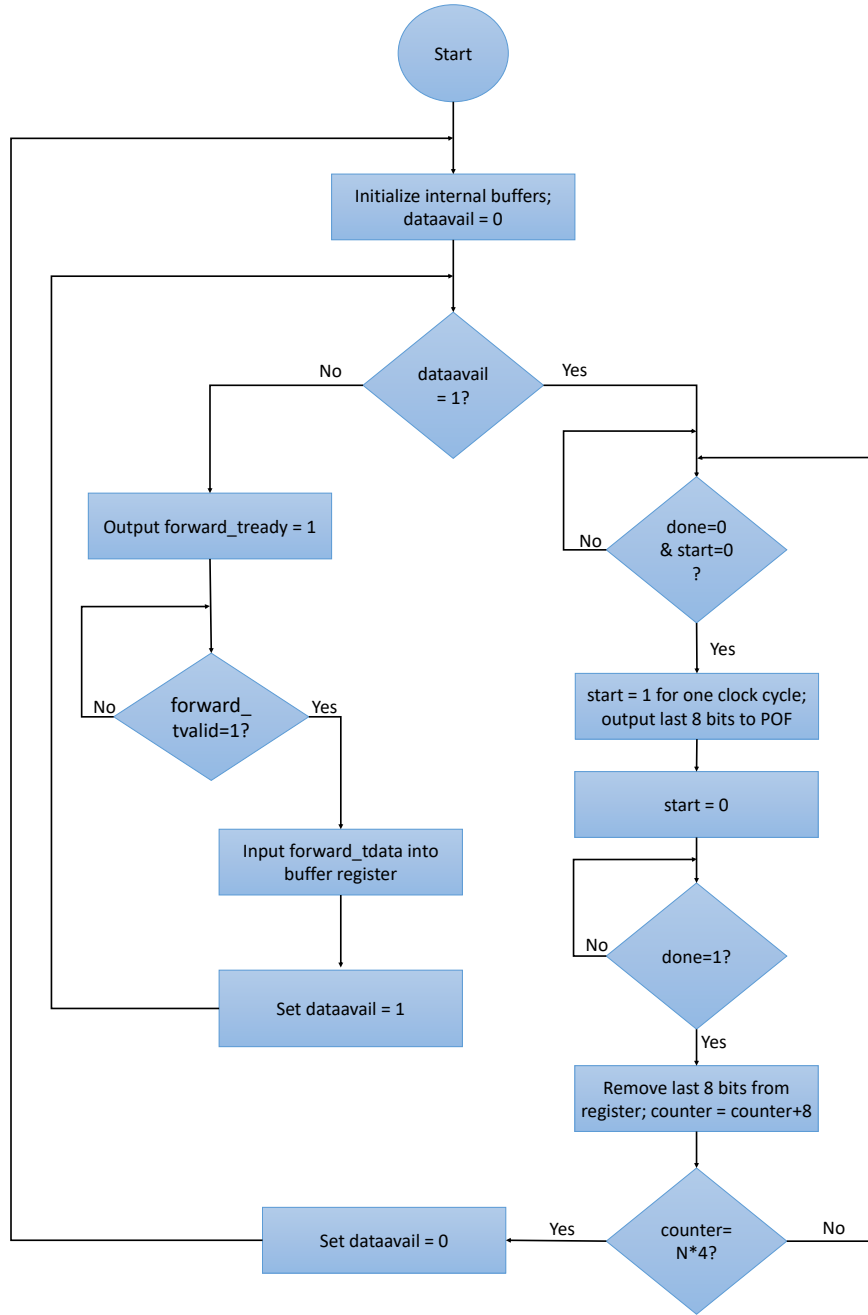


Figure 3.13: Data forward code block flowchart.

Upon reset, the module initializes the internal signals and buffers. It asserts the tready signal when data becomes available from the SFP+, and stores it in

a temporary register. When the UART transmitter is idle, the module extracts the lowest 8 bits, presents them to the UART block, and asserts a start pulse. Once the UART signals are done, the register shifts to discard the sent byte and repeats for the next byte until the entire register is empty. Then, it resets itself and awaits the next data frame. The incoming data is reassembled at the controller board and passed to the PWM generation logic to drive the amplifiers.

3.4 RF-Receive Channel Integration

In the RF-receive channel, digitized data originates in the MRI room from the RF coils and must be delivered to the console for image reconstruction, as outlined in section 2.4. Instead of coaxial cabling, this chain will utilize optical fibers; on-coil electronics and ADCs, to generate and transmit the data via the distributor board to the spectrometer board. The spectrometer board transfers the data to the console using the Peripheral Component Interconnect Express (PCIe) interface.

The controller board programs the ADC to initiate data streaming, which was implemented by Fatma Gul Uyar. The ADC outputs 32-bit samples at 9.6 MHz, corresponding to a required data rate of 9.6 Mbps over the optical link. The data is first transmitted using the POF UART interface. To accommodate the header, trailer, and optional parity bit, a 20 Mbps baud rate is chosen to ensure smooth data transfer. The distributor board buffers the full 32-bit and forwards them to the controller board via the SFP+ link. Its operation mirrors the framing and forwarding logic discussed in section 3.3. Once the data has arrived at the spectrometer board, it is stored in the on-board memory and then transferred to the console PC via the PCIe interface.

Since data arrives as AXI4-stream, it must be converted to AXI4-Full format for DDR4 writes, a memory-mapped handshaking protocol. AXI4-Full expands on the AXI4-stream format by providing five distinct handshake channels to enable bi-directional memory operations:

- **AW**: Write Address
- **W**: Write Data
- **B**: Write Response
- **AR**: Read Address
- **R**: Read Data

This format allows for structured read/write transactions; the master block sends the address/data; the slave block issues acknowledgments. This allows for simultaneous read/write operations and is a widely used standard by multiple memory-related IPs. A code block was written to convert the streaming data into a memory-mapped data by creating a simple FSM that waits till the input data is received based on the handshaking signals. Then, one by one, the AW, W, and B handshaking signals are asserted with the address and data values in the registers. Since the task is to only write to the memory slot, only write handshaking signals are asserted and not read. Once the data is converted, it is stored in the DDR4 memory in the FPGA evaluation board. The KCU 116 evaluation board has 2 gigabytes of DDR4 memory [42], which can be used to store the incoming data. Finally, PCIe is used to transfer bulk data from FPGA memory to PC memory efficiently.

PCIe is a high-speed serial interface, using scalable lanes that can be used as an expansion slot in computer motherboards [58]. It has scalable lanes (x1, x4, x8, x16) to connect hardware components such as mouse, image scanners, microphones, memory storage or FPGAs [58]. There are different generations, with each generation able to work with an older generation, with bandwidth increasing with each revision. FPGAs transceivers connect directly to PCIe slots, and vendor-supplied IPs enable easy configuration. For data transfer, we employ DMA/Bridge Subsystem for PCI Express IP, configured and validated with the help of Fatma Gul Uyar.

The subsystem supports both Direct Memory Access (DMA) and AXI Bridge modes. We opted for AXI Bridge mode, where the PCIe reads data from memory.

The subsystem IP simplifies high-throughput transfers from FPGA to PC with minimal software overhead, supporting bulk data movements. User-selectable memory pointers allow targeting specific DDR4 buffers for transfer. Once the data has been stored from the FPGA side, a simple Python script, written by Fatma Gul Uyar, will be used to control the PCIe from the PC side, which will extract and store the data in a file on the PC.



Chapter 4

Results

This chapter begins with hardware validation to confirm that the optical system and FPGAs function correctly within the two-stage architecture. Furthermore, we will verify the correct operation of individual systems by simulating the code blocks discussed in Chapter 3. Finally, a working solution of the gradient and RF-receive chains will be tested and verified by analyzing the resulting PWM waveforms and ADC data in the console PC storage.

4.1 IBERT test & Eye Test

Integrated Bit Error Ratio Test (IBERT) is a complete Vivado IP block which can be used to test and verify the working of the built-in transceivers in FPGAs [59]. It can be used to analyze the quality of an established link and verify the operating limits of high-speed transceivers under different parameters. It measures bit error rate by generating a known bit pattern, usually a Pseudo-random Binary Sequence (PRBS). Moreover, it can create digital eye diagrams to visualize the signal integrity. Eye diagrams can be used to visualize issues such as inter-symbol interference (ISI), jitter, and noise issues.

IBERT tests were done for two different speeds, 1 Gbps and 2.5 Gbps, for

each of the FPGAs. These tests can also be done for higher speeds, 28 Gbps for KCU-116 and 6.6 Gbps for TE-0714, but the SFP+ operates at 1 Gbps and 2.5 Gbps speeds only. Figure 4.1 shows the IBERT test results for the two speeds.

Name	TX	RX	Status	bits	Err...	BER	IBERT Re...	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE ...	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mo	
Ungrouped L																				
Link Group 0								Reset	PRBS 7-bit	PRBS 7-bit	0.01 dB (00000)	0.00 dB (00000)	950 mV (11000)	✓	Inject	Reset	Reset		None	
Link 0	Quad..	Quad..	0.992 Gbps	1.367E11	2E9	1.463E-11		Reset	PRBS 7-bit	PRBS 7-bit	0.01 dB (00000)	0.00 dB (00000)	950 mV (11000)	✓	Inject	Reset	Reset	Locked	Locked	None
Link Group 1								Reset	PRBS 7-bit	PRBS 7-bit	0.01 dB (00000)	0.00 dB (00000)	950 mV (11000)	✓	Inject	Reset	Reset		None	
Link 2	Quad..	Quad..	0.992 Gbps	1.367E11	0E0	7.313E-12		Reset	PRBS 7-bit	PRBS 7-bit	0.01 dB (00000)	0.00 dB (00000)	950 mV (11000)	✓	Inject	Reset	Reset	Locked	Locked	None

(a) IBERT test at 1 Gbps.

Name	TX	RX	Status	Bits	...	BER	BERT R	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE En	Inject Error	TX Reset	RX Reset	RX PLL St	TX PLL Sta	Loopback Mode	
Ungrouped Li																				
Link Group 0								Re	PRBS 7-bit	PRBS 7-bit	0.01 dB (00000)	0.00 dB (00000)	950 mV (11000)	✓	Inject	Reset	Reset		None	
Link 0	Quad..	Quad..	2.500 Gbps	1.611E	0E1	6.207E-13		Re	PRBS 7-bit	PRBS 7-bit	0.01 dB (00000)	0.00 dB (00000)	950 mV (11000)	✓	Inject	Reset	Reset	Locked	Locked	None
Link Group 1								Re	PRBS 7-bit	PRBS 7-bit	0.01 dB (00000)	0.00 dB (00000)	950 mV (11000)	✓	Inject	Reset	Reset		None	
Link 1	Quad..	Quad..	2.500 Gbps	1.593E	0E1	6.276E-13		Re	PRBS 7-bit	PRBS 7-bit	0.01 dB (00000)	0.00 dB (00000)	950 mV (11000)	✓	Inject	Reset	Reset	Locked	Locked	None

(b) IBERT test at 2.5 Gbps.

Figure 4.1: IBERT tests for KCU 116 Evaluation Board

A loopback test was performed on the KCU 116 evaluation board. An optical fiber was connected from the first SFP+ transceiver to the second, establishing two links for the tests shown in Figures 4.1a and 4.1b. These figures demonstrate that a stable link was established with 0.992 Gbps and 2.5 Gbps. Moreover, PRBS data is generated and checked at the receiver end. These patterns are standard for testing the reliability of a network. The IBERT test can use different patterns, headers, and trailers. The IBERT test can also vary the voltage swing, sweeping these parameters to confirm a reliable link. Similar tests were done with the TE-0714 FPGA evaluation board, and the results were similar; a good link was established. After confirming the functionality of the transceivers, an eye test was performed on a link between the KCU-116 and the TE-0714 evaluation boards. An eye diagram is a plot with an eye shape used to check the signal integrity of a high-speed communication link. It is created by superimposing multiple bit waveforms with different transitions aligned over a unit interval. It is a voltage vs time graph. The main parameter to analyze is the eye opening: its height indicates the noise margin between high and low voltages, and the width represents the jitter margin between rising and falling edges. The result for a communication link between the KCU 116 and TE 0714 evaluation boards at 2.5 Gbps is shown in Figure 4.2.

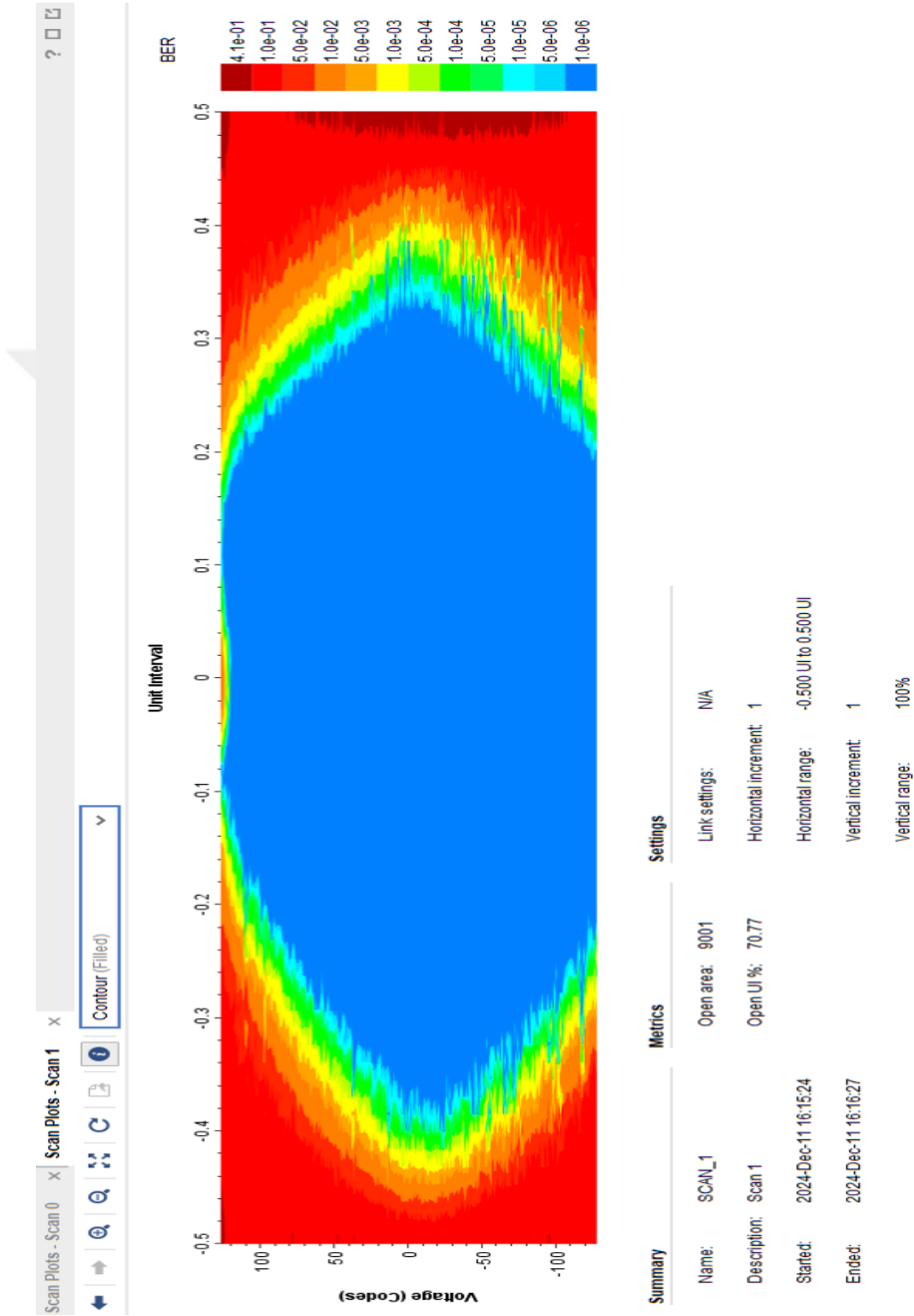


Figure 4.2: Eye diagram between KCU 116 FPGA and TE 0714 FPGA Evaluation Boards.

In Figure 4.2, the eye diagram has the unit interval on the x-axis and the voltage codes at the y-axis. As this is a digital diagram, the voltage levels are digitized with 128 bits for both the positive and negative parts. The eye opening shows approximately 70% open area, which is considered good. The contour map indicates that the center region is error-free with a Bit Error Rate (BER) of 1.0×10^{-6} , while the edges show a high BER, indicating higher noise. However, the BER is usually high at the edges due to the transition between high and low values. Therefore, this eye diagram is considered good regarding jitter and noise margin. Since the transceivers were connected to the SFP+ modules, the IBERT tests could be done; however, without the transceivers, a digital eye diagram cannot be implemented. Therefore, Ege Aydin created an analog eye diagram using an analog oscilloscope to visualize the POF performance. Compared to a digital eye diagram, an analog one has a low sampling rate, no BER detection, and jitter detection is also basic. It is suitable for waveform visualizing, rise/fall times, and noise and jitter visualization. A loopback test was done similarly for the POF module, and an analog eye diagram was created using an oscilloscope as shown in Figure 4.3 [1].

The eye opening shows a good vertical range with less noise in the high and low voltages, indicating good amplitude consistency around ~ 3.4 V. The horizontal width is also significant. However, the boundaries are relatively thicker, which indicates comparatively high jitter, though still within the picoseconds (ps) range. Therefore, the analog eye diagram shows a clean result with minimal ISI, noise, and jitter. The speed for this plot is 13.33 MHz or 26 Mbps. The ISI and jitter values increased as the speed increased, and the eye opening was also reduced. Figure 4.4 shows an eye diagram at 17 MHz or 34 Mbps speed, which is considered the limit for the POF module [1]. Increasing the speed beyond this gave very poor results; however, this maximum limit is perfect for this application, as the POF section in section 3.4 requires 20 Mbps speed, but for the gradient section 3.3, which requires 100 Mbps, an ethernet cable will be used inside a shielded box.

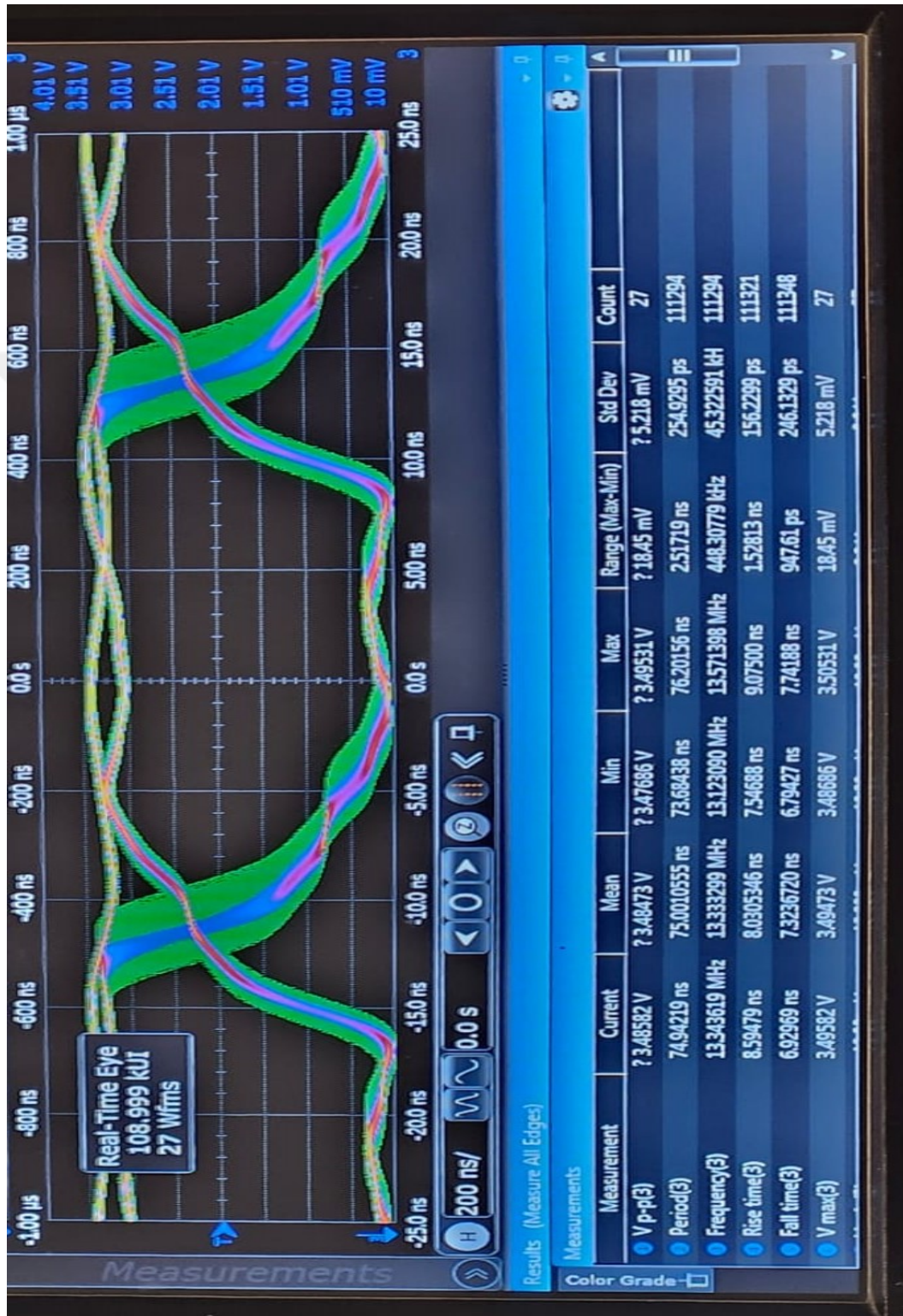


Figure 4.3: Eye diagram for the POF module at 26 Mbps done by Ege Aydin [1].

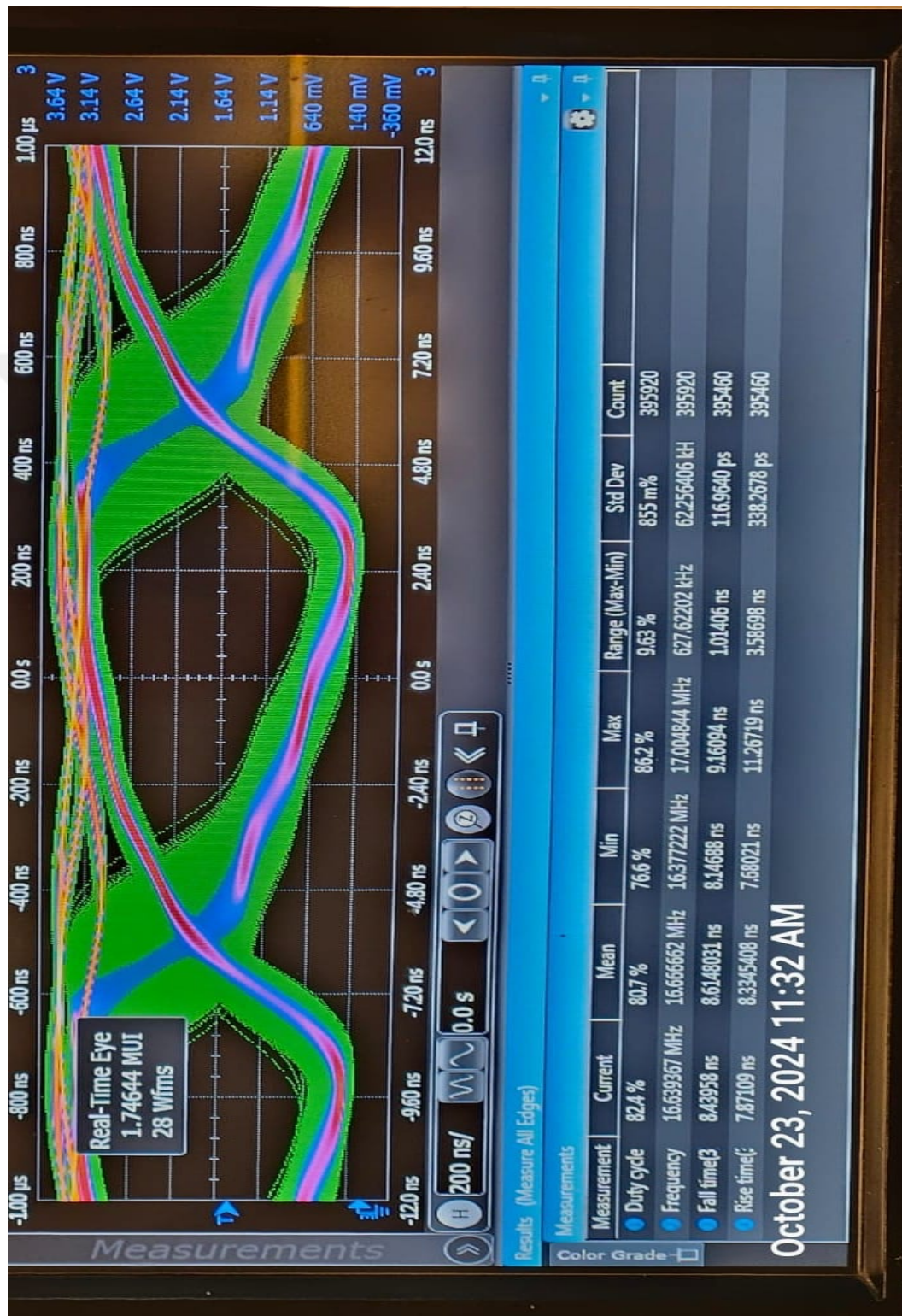


Figure 4.4: Eye diagram for the POF module at 34 Mbps done by Ege Aydin [1].

4.2 Gradient & RF-Transmit Chain

The previous section established that the hardware is compatible and its capabilities are sufficient for this thesis. In this section, the IPs and individual codes that were discussed in section 3.2.2, 3.2.3, 3.3, and 3.4 will be verified by showing ILA results or simulations.

The AXI ethernet IP blocks for both the FPGAs will be tested using two experiments. The first experiment uses an SFP+ loopback module, which internally routes the TX pin to the RX pin. These tests, performed without an external cable, verify the functionality of the AXI ethernet IP and its pin configurations. In the second test, data was generated on the spectrometer board, sent to the distributor board via the SFP+, and then routed back to the spectrometer board using an internal loopback in the code. The transmitted and received data were then compared on the spectrometer board. A code block generated a continuous single-byte sequence with an AXI-Stream format for this testing. The data was set to 64 bytes to meet the minimum ethernet packet size, and this sequence was then repeated. The ILA data is shown in Figure 4.5, and the experimental setup is shown in Figure 4.6.

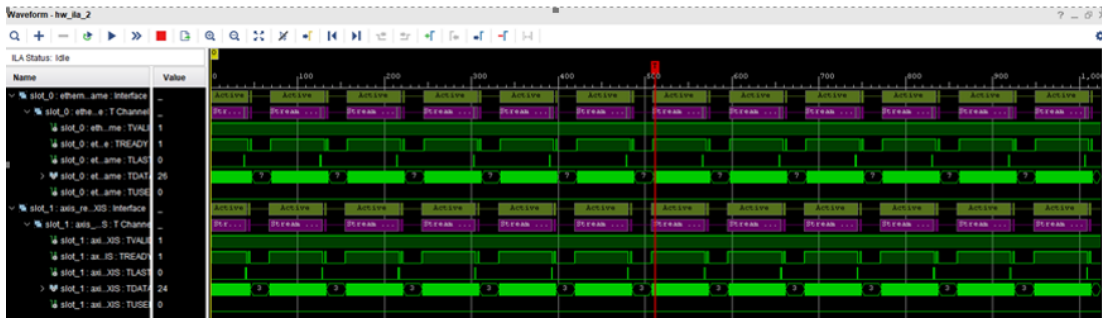


Figure 4.5: ILA data to test the ethernet IPs for SFP+ testing.

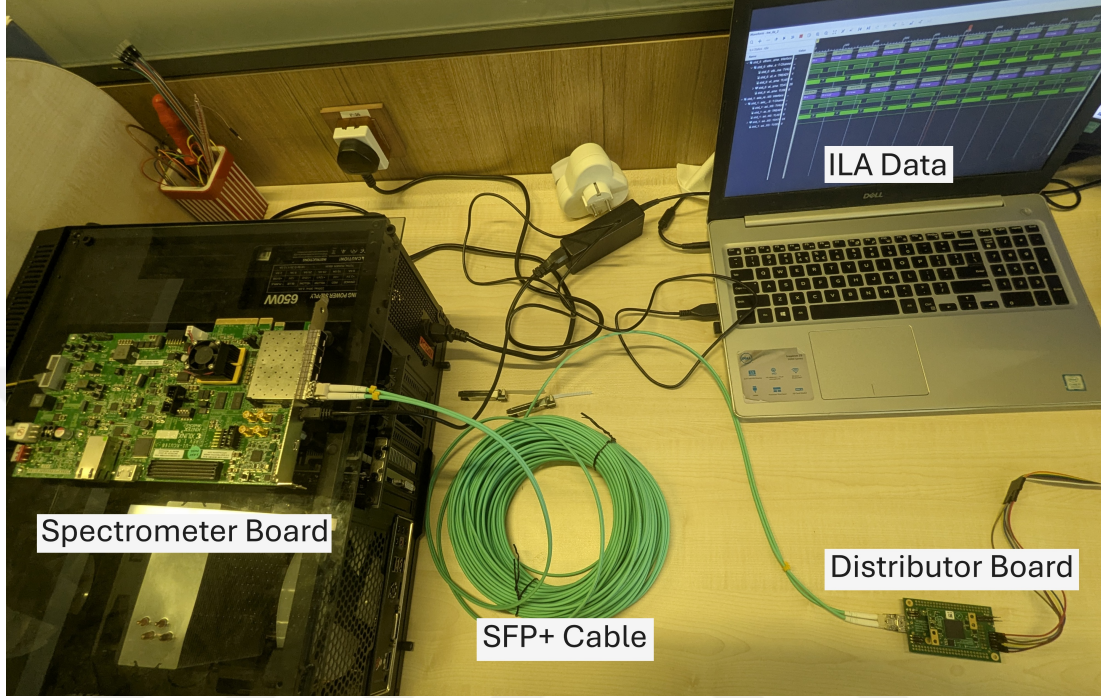


Figure 4.6: Experimental setup to test the ethernet IPs for SFP+ testing.

The experimental setup shows the spectrometer board as the KCU-116 Evaluation board, the distributor board as the TE-0714 Evaluation board mounted on the TEBB-0714 baseboard, the SFP+ cable, and the console PC showing the ILA data on the spectrometer board. The ILA data shows the two AXI-Streams for the transmitted and received data. Each packet is transmitted with a 64-byte length, with the tlast being asserted with the last byte, and the data is transmitted only when tvalid and tready are high. This verifies the working of the SFP+ between the two FPGA boards, the next part is to verify the working of the custom protocol code block defined in section 3.3.

The code blocks were combined with the AXI ethernet IP to test whether the custom protocol worked, and multiple real data streams were sent from the PC to the spectrometer board. It was encapsulated with the protocol and sent through the SFP+ to the distributor board. The headers and trailers were removed on the distributor board, and the packets were extracted. From the distributor board, they were looped back to the spectrometer board. Figure 4.7 shows the ILA data

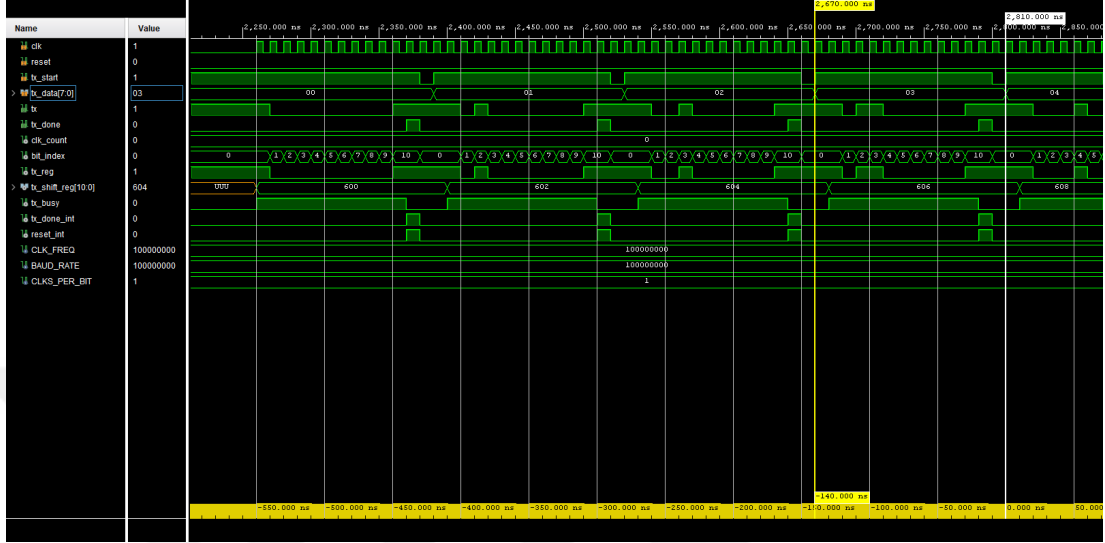


Figure 4.8: Simulation of UART transmitter block.

The simulation is shown in Figure 4.9 for the receiver part. For the receiver, the clock is four times faster than the transmitter clock to provide a sufficient oversampling rate. This clock speed was chosen to avoid the very high-speed clocks that can cause timing issues in Vivado. The code observes the rx line, which is connected to the tx line, and at the falling edge, it starts the sample_count, and at the middle of the sample_count, it adds the bit into the rx_shift_reg. It ignores the first bit as the start bit, and the following eight bits are added to the register as seen by the bit_index variable. While the code receives data, the receiving flag is TRUE, indicating that the FSM machine is extracting the data bits, and FALSE at the start and stop bits. Once all the bits are received, the data_valid signal is asserted for one clock cycle to be forwarded to another block for PWM generation. Again, it takes 140 ns to receive a byte similar to the transmission code. The rx_sync variable synchronizes the incoming rx signal with the high-speed clock. This is repeated for multiple values until all the bytes have been sent.

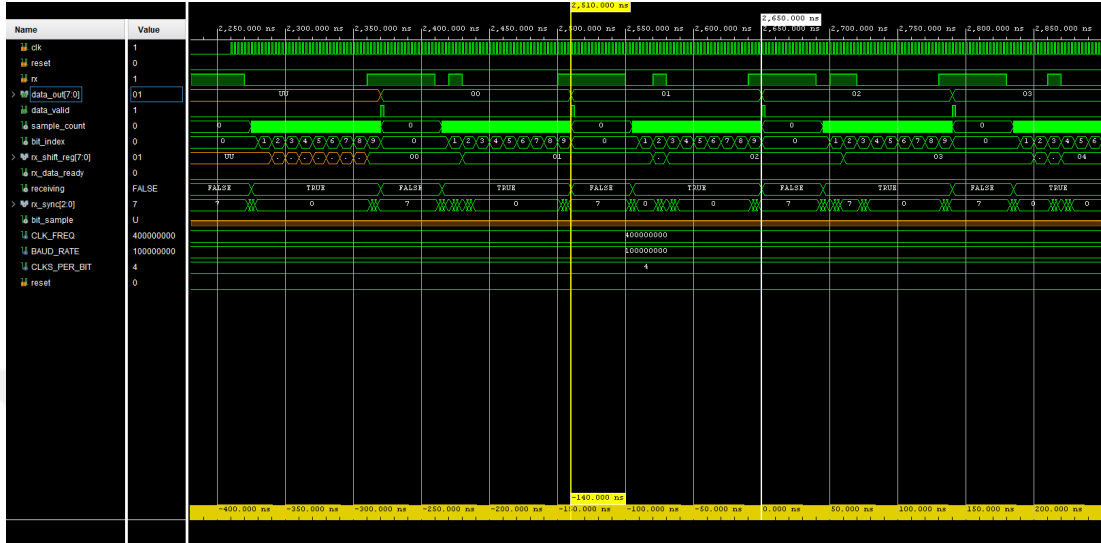


Figure 4.9: Simulation of UART receiver block.

Afterwards, the code was tested on the FPGA, and the ILA was used to check the correct working of the code blocks. A loopback code was created where the transmitter and receiver blocks were in the same block design and synced with the same clock domain. The ILA screenshot is shown in Figure 4.10. The counter_gen variable sends data to the transmitter block with an asserted start signal. The receiver then correctly receives the data and asserts the valid signal. This verifies the FPGA's I/O ability to work with 100 Mbps UART code without errors.

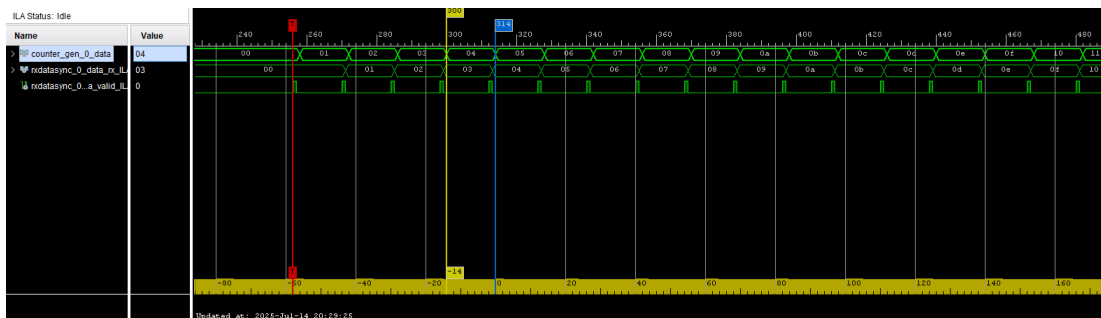


Figure 4.10: ILA test of the transmission and the receiver blocks.

Later, both the codes were combined, and the output waveforms were checked on the oscilloscope. The real data from the SFP+ was sent to the UART code

for four channels. The final PWM waveforms are shown in Figure 4.11. For the verification test, the data was sent repeatedly, resulting in the periodic waveform shown in the figure. The two plots should be PWM waveforms, but these are the required envelopes of the PWM signals. The two waveforms represent the positive and negative side PWMs, which, when subtracted, yield the voltage waveform required for the gradient coils. When this voltage signal is applied to the gradient coil, a trapezoidal current waveform is obtained, as shown in Figure 4.12.

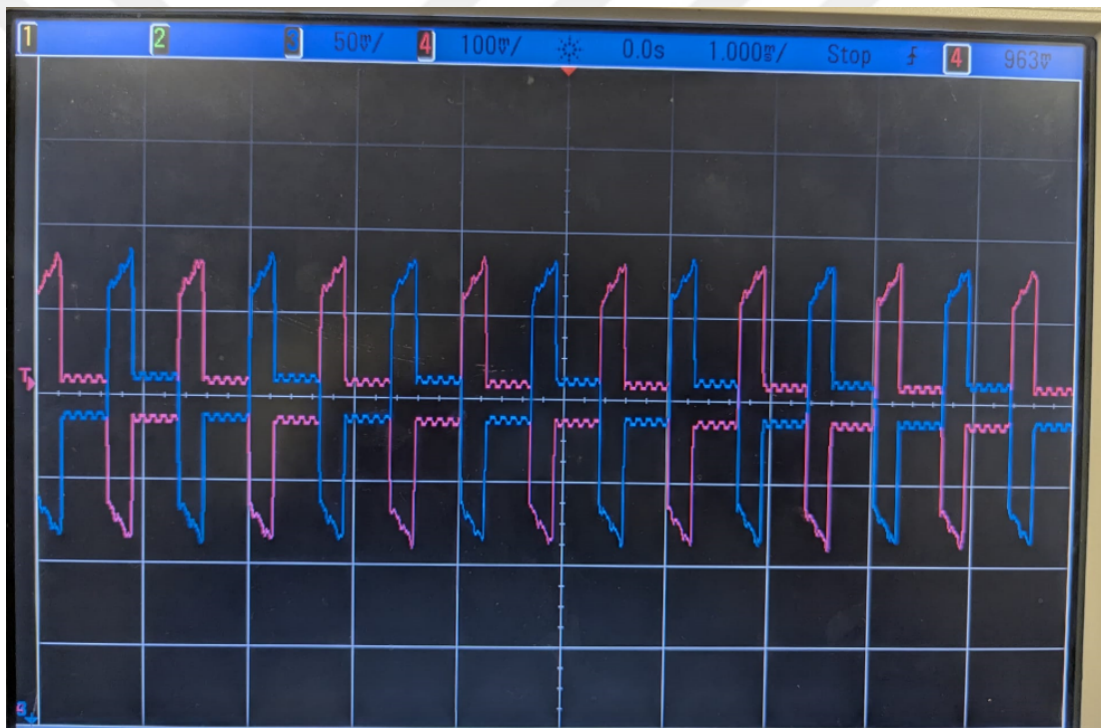


Figure 4.11: Positive and negative PWM envelopes for one channel of the gradient chain.

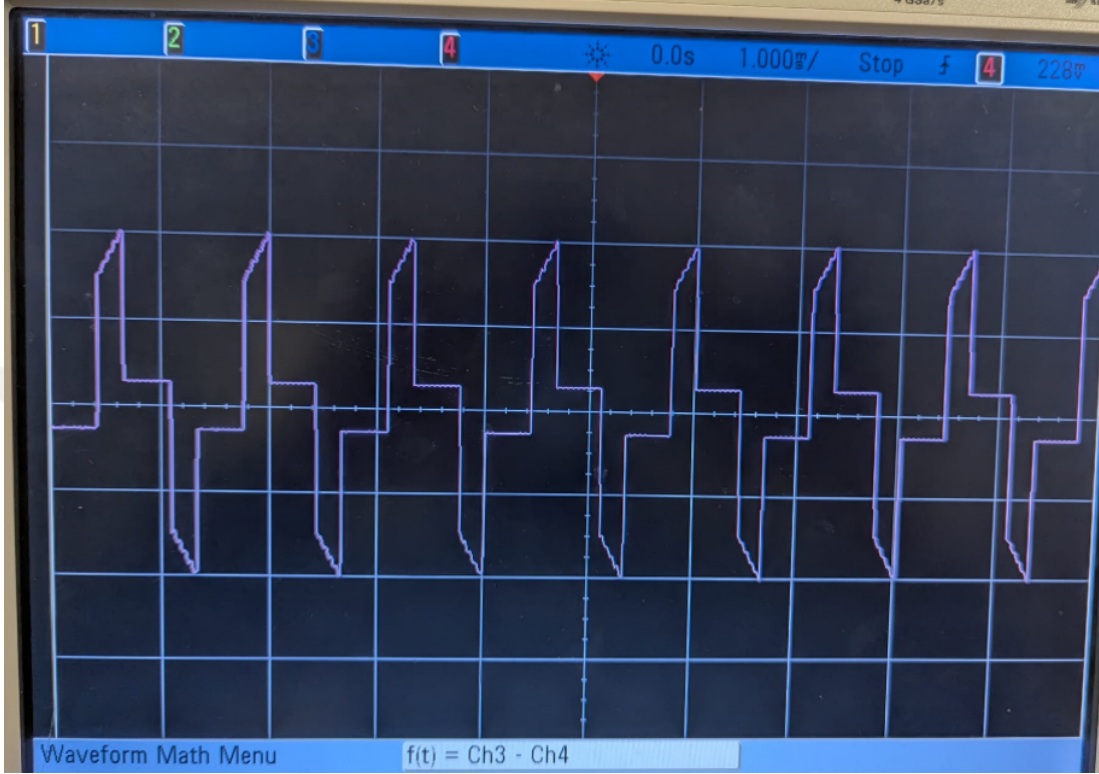


Figure 4.12: Voltage envelope of the gradient amplifier.

4.3 Radiofrequency Receive Chain

For the RF-receive chain, data from the ADC is sent to the controller board and then to the distributor board via a POF. This communication is done at 20 Mbps as the speed required is greater than 10 Mbps. The 32-bit data is sent to the distributor board one byte at a time. The distributor board receives and stores the data until all bits are received. The ILA data for the distributor board receiving the correct data and forwarding it in AXI-stream format is shown in Figure 4.13. The data is padded using custom framing code discussed in section 3.3, with the channel generic value set to 1. The frames are sent to the spectrometer board, and the data is extracted. The working of the SFP+ stage is similar to that discussed in the previous sections. The experimental setup is shown in Figure 4.14.

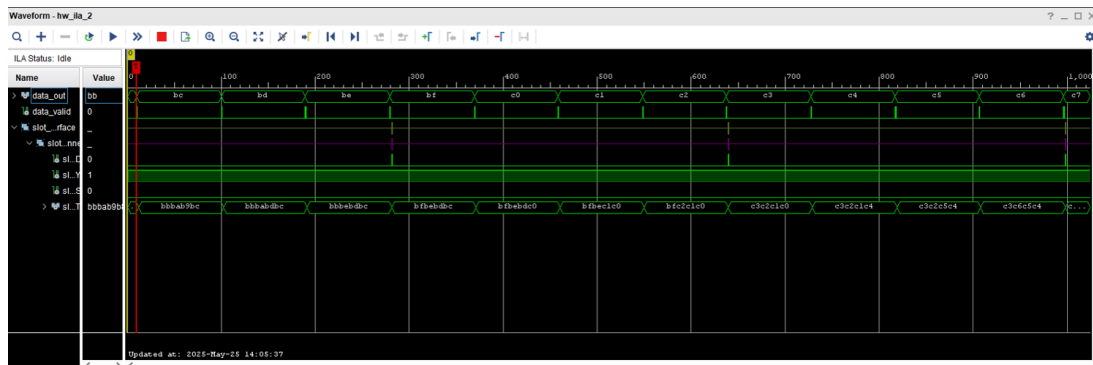


Figure 4.13: RF-receive POF stage working.

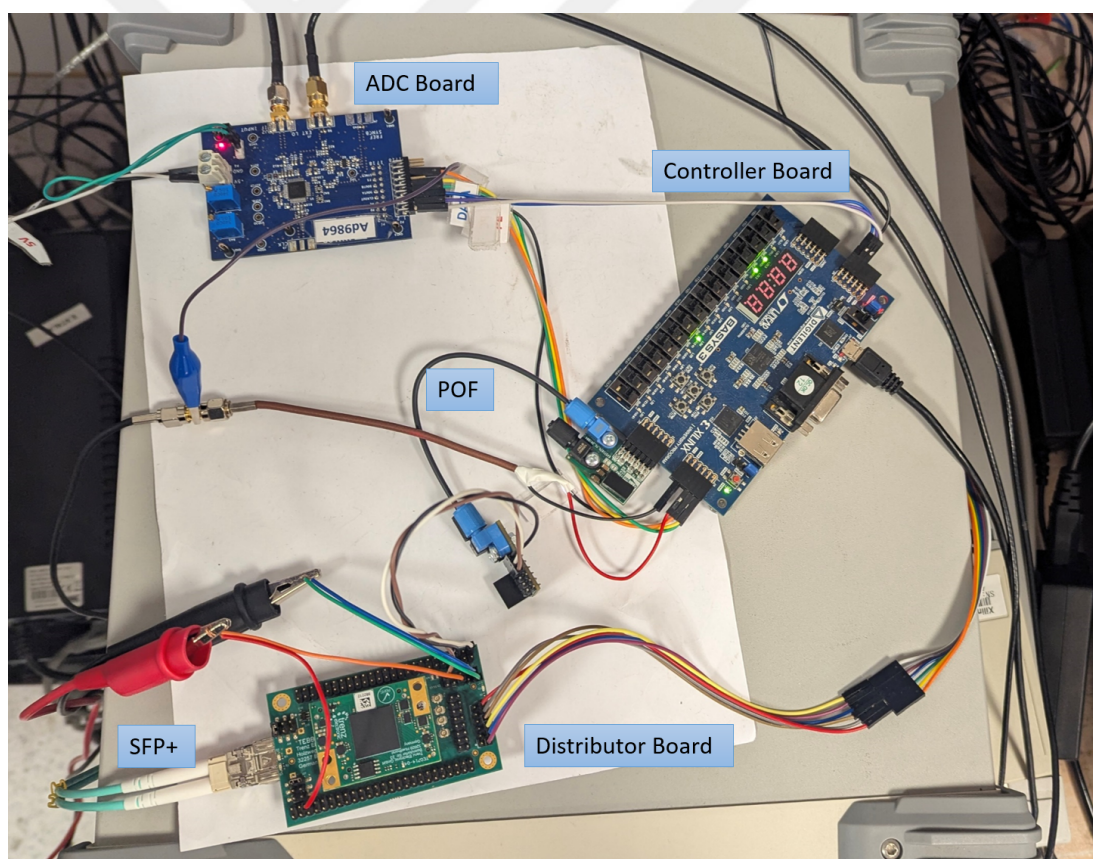


Figure 4.14: Experiment setup for the RF-receive chain.

Two separate experiments were done in collaboration with Fatma Gul. In the first experiment, the ADC sampled an RF signal at 123.25 MHz from an RF generator, extracted the in-phase and quadrature (I/Q) components, and stored

them in a 32-bit packet. These packets were then received using an SSI protocol by the Basys 3 FPGA. The code for receiving data from the ADC waits for a trigger. For this experiment, a VIO was used to simulate the trigger from an MRI machine to start receiving data. Once the trigger is received, the controller board FPGA takes a fixed number of samples and sends the data to the spectrometer board through the distributor board. The spectrometer board saves the data into the DDR memory, and then the PCIe transceiver can send the data to the PC using a python code from the PC side, as discussed in section 3.4. Afterward, the data was stored in a file on the PC, and the I/Q components were plotted to verify the optical channels' functionality and ensure no data loss during transmission. Figure 4.15 shows the I/Q data received for a small sample.

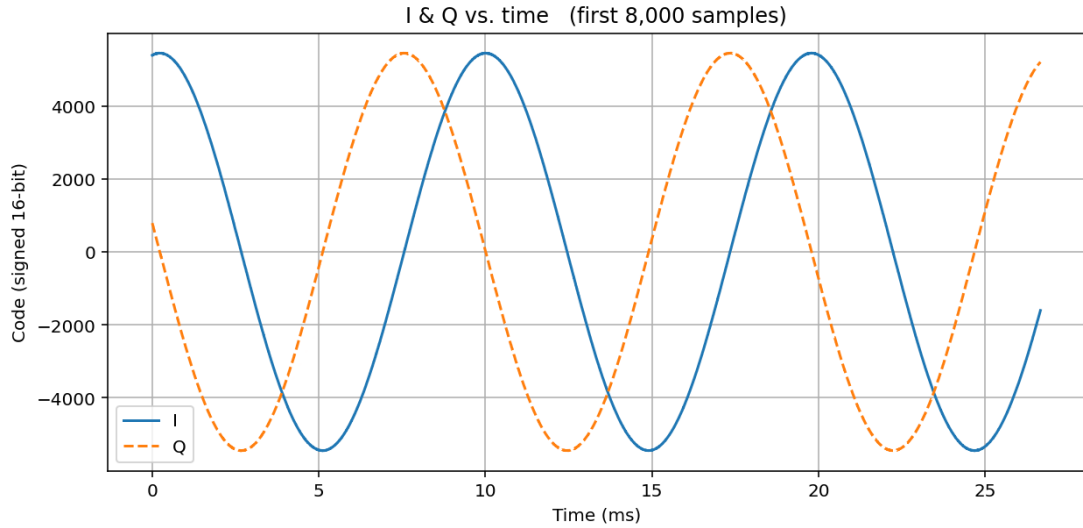


Figure 4.15: 8000 samples sent from the ADC to the spectrometer board and plotted on the PC.

Figure 4.15 shows the correct working of the communication link and the ADC. Moreover, the I/Q components have a 90° phase difference and the correct waveform, which verifies the proper working of the FPGA. The PC was able to successfully access the data from the FPGA via the PCIe transceiver with no sample loss. The maximum number of samples that can be taken upon the configuration selected for the PCIe and DDR memory is 2500000000 samples, and each sample is 4 bytes. Hence, given the configuration for this setup, the

maximum limit of the data that can be stored is 1 GB.

In the second experiment, actual data from the MRI were acquired and reconstructed on MATLAB. Data was acquired using the controller board and ADC setup. The data received were 32-bit samples with a sampling rate of 300 kHz. From the controller board to the distributor board, POF was used with the UART communication protocol at 20Mbps. From the distributor board to the spectrometer board, SFP+ was used at 2.5 Gbps to carry the data with the custom framing code explained in section 3.2.2. After receiving the data, it was transferred to the console PC via the PCIe slot. A Gradient Echo (GRE) sequence was designed with the number of samples as 256, repetition time (TR) as 120 ms, echo time (TE) as 4.3 ms, alpha as 30° , readout time as 3.2 ms, and the ADC sampling rate set to 300 kHz. With this data, each trigger would give 960 sample points, and the total points collected were 245760. The sequence was designed without RF spoiling and trigger signals to be captured by the ADC. A receive coil, designed in UMRAM, was used with a custom low-noise amplifier (LNA), designed by Fehmi Altunkas [60].

Figure 4.16 shows the raw Free Induction Decay (FID) signal acquired during the MRI experiment. The FID is the fundamental signal detected in an MRI scanner after an RF pulse excites the spins in the sample. The two lines on the plot, labeled 'x' and 'y', represent the in-phase (I) and quadrature (Q) components of the complex MR signal. These components are collected from the MR receiver and are crucial for reconstructing the final image. The plot shows a strong signal at the center of the acquisition, which rapidly decays over time due to $T2^*$ relaxation and gradient encoding. The signal is strongest in the middle of the acquisition because this is when the echo is at its peak. The noise floor is also visible, appearing as small, random fluctuations before and after the main signal. This plot confirms that the optical communication link successfully transmitted the raw, time-domain MR signal from the scanner to the console PC without significant data loss or distortion.

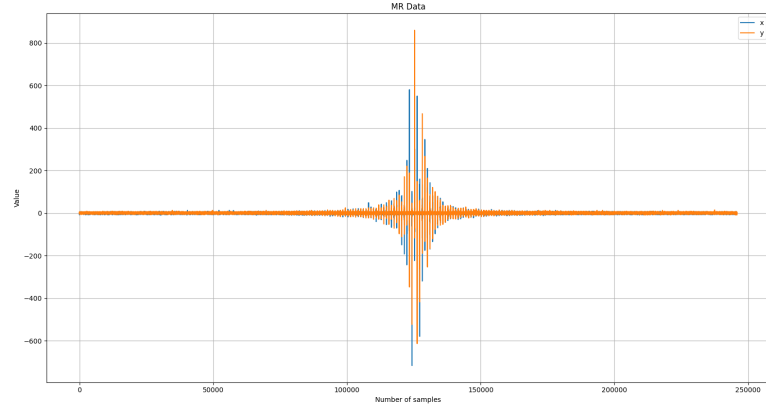


Figure 4.16: Raw data acquired for the GRE sequence.

Figure 4.17 shows the zoomed version of Figure 4.16, which provides a more detailed look at the received signals. It isolates two echoes within the acquired data. The plot shows two separate signal peaks, each representing an echo. Similar to the full plot, these peaks consist of two components, 'x' and 'y', corresponding to the I and Q components of the MR signal. These components are essential for capturing the full phase and magnitude information of the signal. The zoomed view makes it easier to observe the rapid oscillations within each echo. The signal's amplitude is highest at the center of the echo and goes down towards the edges, reflecting the natural decay of the signal.

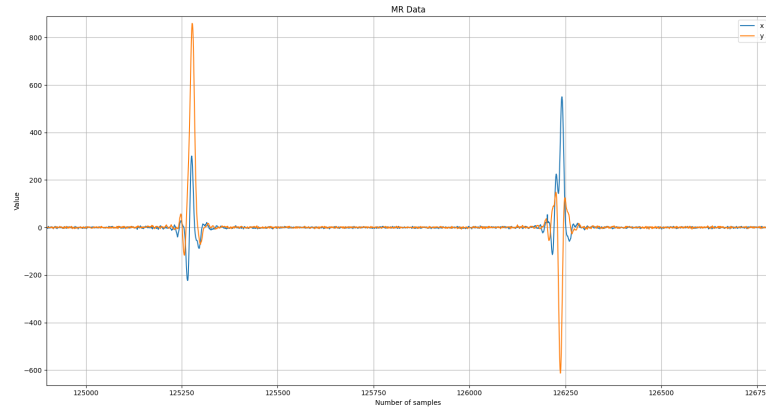


Figure 4.17: K-space image for the cylindrical saline phantom.

Figure 4.18 is a representation of the k-space data, which is the spatial frequency domain of the MR image. The image shows the raw data as it was received, arranged into a grid. The central region of k-space contains data corresponding to the low spatial frequencies, which determine the overall contrast and brightness of the final image. The outer regions of k-space contain data for the high spatial frequencies, which define the finer details and edges. The bright signal in the center of the image indicates that the system successfully acquired the data. The color scale (blue to yellow) represents signal intensity, with yellow being the highest. This image proves that the data was not only transmitted but was also correctly organized in the spatial frequency domain, ready for image reconstruction.

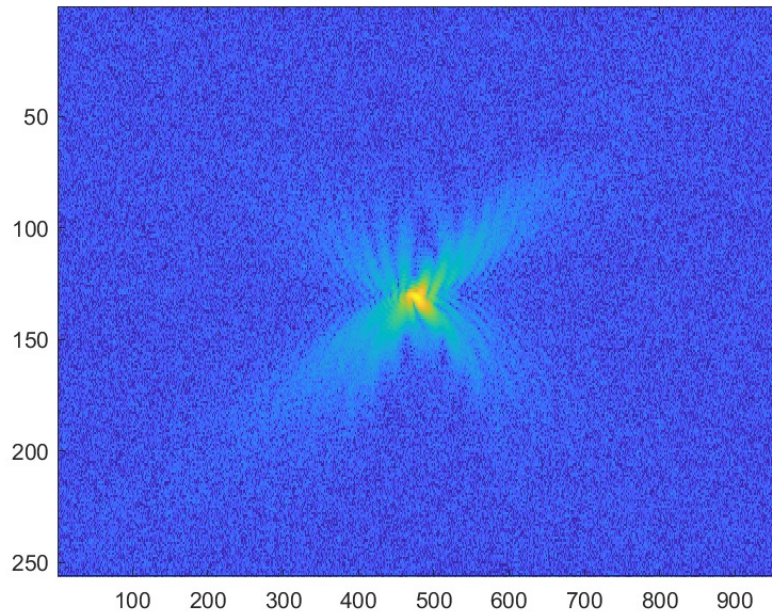


Figure 4.18: K-space image for the cylindrical saline phantom.

Figure 4.19 is the reconstructed image of a cylindrical saline phantom. This image is generated by applying a two-dimensional inverse Fourier transform to the k-space data. The reconstructed image is in the spatial domain, where pixel intensity represents the MR signal strength at a specific location. The image clearly shows the cylindrical shape of the saline phantom. The bright spots and

artifacts around the edges of the cylinder and at the bottom are likely due to the imperfections in the MR acquisition process, such as B0 field inhomogeneity, or possibly noise in the received data. However, the overall shape and uniform intensity of the phantom in the central area demonstrate that the optical communication system and the associated signal processing successfully acquired, transmitted, and reconstructed a clear MR image. A cylindrical saline phantom was used for imaging purposes, and the image from the MR machine receive system is also shown in Figure 4.20 for comparison.

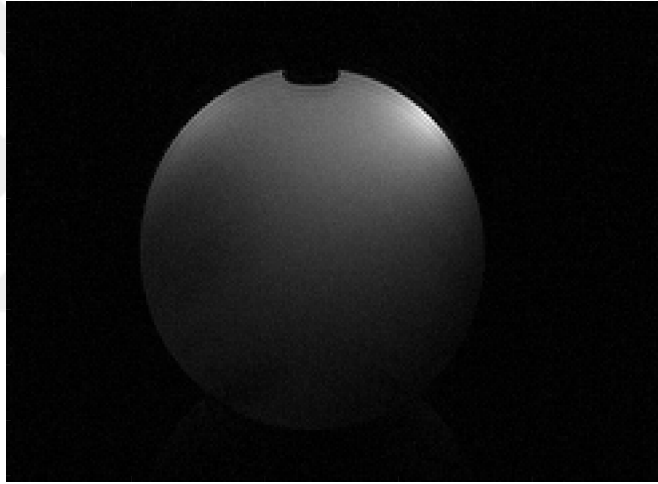


Figure 4.19: Reconstructed image of a cylindrical saline phantom.

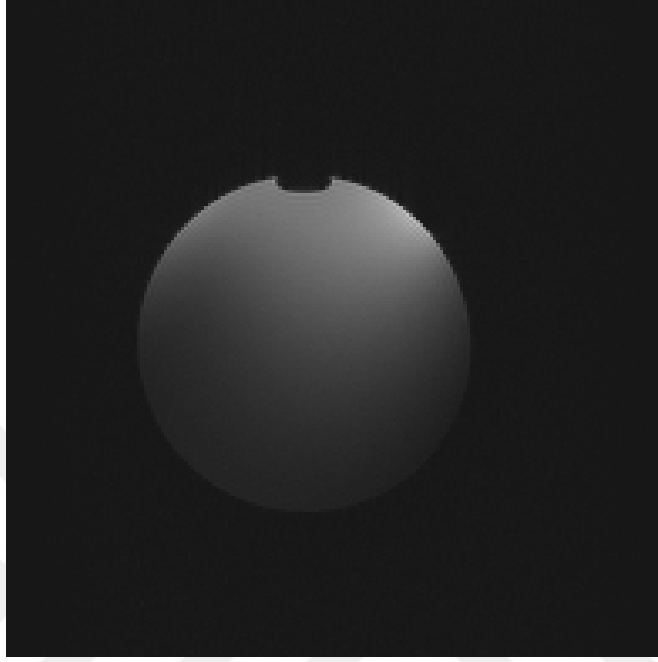


Figure 4.20: Image acquired by Siemens MRI system of cylindrical saline phantom.

Comparing Figure 4.19 and Figure 4.20, the Siemens image exhibits a higher Signal-to-Noise Ratio (SNR), resulting in a cleaner image. In contrast, our image shows a visibly lower SNR, evidenced by the grainy texture and higher background noise. This may be due to the long coaxial cable between the LAN and ADC in our experimental setup, Figure 4.14. This connection is not ideal and introduces signal degradation. However, the main motivation is the successful capturing of the raw data without any loss in samples, validating the optical fiber communication system. Despite the difference, the phantom's cylindrical shape and intensity are preserved, confirming the communication network's capability of handling MR data from acquisition to image reconstruction.

Chapter 5

Discussion & Conclusion

As the number of channels increases for the array configurations, the number of cables, the supporting electronics, and shielding components increases. This creates a dense structure around the coils, which can counteract the benefits of the array system by introducing new challenges. The bulky cabling and the electronics need to be isolated from the EMI generated by the switching electronics. To mitigate these issues, optical fibers can transfer data using light as a medium, traveling inside a glass or plastic core.

Optical fibers have been used in the communication industry for transferring data, as they can transfer data over longer distances at higher speeds with minimal loss. In MRI, previous literature shows that optical fibers have been used for RF reception. Moreover, with the increased channels in the new array system, handling the large number of coaxial cables and on-coil electronics, which can shield the inner coils and interfere with the fields, would be challenging. Therefore, converting the current system into optical fibers is crucial for better efficiency. Furthermore, this approach addresses the issues of excess cabling in an array system by significantly reducing the number of cables required per channel. Only a few optical cables could be used with the proposed architecture. The SFP+ part works at 2.5 Gbps for the gradient system and the POF at 100 Mbps. This provides a maximum of 25 channels for the controller board. Since each

controller board can handle four amplifier boards, this allows for 100 channels for gradient or RF-transmit with just one SFP+ cable. For the RF-Receive part, this number is greater; the POF works at 20 Mbps; therefore, the maximum number of channels that can be used is 125 with just one SFP+ cable.

Modern MRI systems often require a high number of channels, with some research systems using 84-channel gradient coils and commercial systems supporting up to 128 receive channels. The work presented in this thesis can accommodate any number of channels up to the maximum limit. These numbers can be increased by utilizing better IPs or custom code for the SFP+. Currently, the speed is limited by the IPs being used, but the maximum speed of the transceivers is higher, 28 Gbps for the KCU-116 FPGA and 6.6 Gbps for the TE 0714 FPGA evaluation boards. The basic transceiver IP, discussed in section 3.2.2, can handle these high-speed rates, but its configuration proved more challenging. The transceiver IP worked in loopback mode but proved more difficult when communicating between the two evaluation boards. This could be due to multiple reasons, such as comma-alignment, which is used for bit ordering. Since there is no shared clock, the internal clocks could not have locked properly to the incoming data. Other resets or calibrations in each of the IPs may also be contributing factors. With the configuration of the basic transceiver IP, the maximum speed that can be reached between the spectrometer and distributor boards is 6.6 Gbps. With this, a higher number of channels can be accommodated with just one SFP+ link. The 6.6 Gbps limit is for the TE0714 FPGA board, whereas the KCU116 transceiver can go up to 28 Gbps. However, the AXI 1G/2.5G Ethernet Subsystem IP proved to be a robust solution, as it handled the physical and MAC layers, which would otherwise have required user-defined designs for the transceiver IP. Future work can focus on this to facilitate higher speeds and more freedom in designing the network layer. Future work could focus on overcoming the configuration complexities of the basic transceiver IP, which would unlock higher speeds and even greater channel density.

In the UART communication, the custom code presented in section 3.2.3 works up to 20 Mbps, and the POF module presented can work up to 34 Mbps, with the newer version of the POF module working up to 80 Mbps. However, the

ADC sample tests in section 4.3 had some instances where the data was not sent properly, and the waveform appeared with glitches. This is inevitable in any communication, but error correction techniques help mitigate these mismatches or missing data. The current algorithm for the POF has error detection with the help of parity bits, but no error correction techniques. To quantitatively assess the link’s reliability, a formal BER test needs to be done. This test would involve transmitting a known data pattern, such as a Pseudo-random Binary Sequence (PRBS), and comparing the incoming data in a loopback configuration. Establishing this BER benchmark is essential for validating the effectiveness of any new communication system. Therefore, to improve the communication, the current custom UART code is under development to include error-correction techniques and to use the error-detection parity bits better.

The two-stage architecture is proposed to improve the hardware cost and reduce overhead when working with multiple channels. The distributor board is the TEBB-0714 baseboard, a multi-purpose PCB with multiple GPIOs. For better accessibility and connector coupling, a dedicated distributor board should be designed to accept SFP+ inputs and output at least 100 channels of POF with specialized connectors for improved coupling and noise immunity. This distributor board will be positioned closer to the coil and will require a shield cage to protect itself from the harsh magnetic environment and protect the MRI from the device’s EMI. Moreover, the on-coil amplifiers and the controller boards must be closer to the coil; therefore, they must be protected and placed inside a shielded box. For that purpose, a Eurocard cage, proposed by Ege Aydin, has been selected, which will have multiple slots to slide PCBs inside and a back plane that can connect the different PCBs or to the outside hardware. The distributor board PCB must conform to the Eurocard cage format to be installed within the cage. This will protect the PCBs from external EMI from reaching the surrounding environment.

In conclusion, we have proposed a fiber optic network with a two-stage architecture utilizing SFP+ and POF cables. This system replaces bulky copper wires with light-carrying optical fibers containing no conductive parts. It can mitigate the interaction between the cables and minimize the losses incurred. Hardware for

this architecture was selected, and FPGAs were used to control the electronics and generate the required signals. Inexpensive FPGAs were also used to distribute the digital data to the network and facilitate high-speed communication. The network layer design was created and verified, and the correct application was tested with waveform validation on the oscilloscope and Python.



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