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BOLU ABANT İZZET BAYSAL UNIVERSITY
INSTITUTE OF GRADUATE STUDIES
Department of Physics

THE INFLUENCE OF GAMMA IRRADIATION ON CHARGE STORAGE CAPABILITY OF $HFO_2/DY_2O_3/AL_2O_3$ BASED CHARGE TRAPPING MEMORY CELL

MASTER OF SCİENCE

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BOLU, HAZİRAN - 2023

APPROVAL OF THE THESIS

THE INFLUENCE OF GAMMA IRRADIATION ON CHARGE STORAGE CAPABILITY OF $HFO_2/DY_2O_3/AL_2O_3$ BASED CHARGE TRAPPING MEMORY CELL submitted by **Racheal CHIRWA** and defended before the Examining Committe Members listed below in partial fulfillment of the requirements for the degree of **Master of Science** in **Department of Physics, Institute of Graduate Studies of Bolu Abant Izzet Baysal University in 13.06.2023** by

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ABSTRACT

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MSC THESIS
RACHEAL CHIRWA
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INSTITUTE OF GRADUATE STUDIES
DEPARTMENT OF PHYSICS
(SUPERVISOR :PROF.DR. ERCAN YILMAZ)

BOLU, JUNE 2023
(XİV +73)

The impact of annealing temperature and Cs-137 gamma-ray irradiation on $Al/HfO_2/Dy_2O_3/Al_2O_3/n\text{-}Si$ (100) charge trapping memory (CTM) devices has been examined in this thesis. E-beam evaporation and RF magnetron sputtering procedures were both used to deposit the thin films. The samples were annealed at 300^oC, 500^oC, 700^oC and 900^oC in N_2 ambient for 40min, while one sample was left as-deposited. The XRD and AFM were used to study the crystalline structure and surface textures of the thin film. It has been observed that the sample annealed at 900^oC had only one weak peak (400) of Dy_2O_3 while other samples turned amorphous. With an increase in annealing temperature, the surface textures have been found to diminish. The lowest RMS value of 2.06nm was found at 900^oC. The impact of frequency and annealing temperature on the CTM devices has been investigated through C-V curves. We found that interface state density had a huge impact on the value of capacitance in the accumulation region. It has also been found that the C-V curves decreased with an increase in the annealing temperature between 500^oC and 900^oC. This might be plausibly due to the formation of dangling bonds and interfacial layers at higher annealing temperatures. The C-V curves have been observed to be shifted to the positive and negative direction, respectively. The memory window (ΔV_{fb}) were analysed and studied through the C-V hysteresis curves for various annealing temperature at -10V to +10V and back. The device annealed at 500^oC was found to have a larger ΔVfb of 0.44V compared to other devices. The ΔVfb were obtained at different sweeping between ±10V and ±12. The largest memory window of 8.22V was achieved at ±12V for the device annealed at 700^oC. This could be related to the good charge storage capability. The effect of radiation on CTM devices has also been studied intensively through C-V curves by using Cs-137 gamma-ray source in different doses of 4Gy to 128Gy. There was a shift both in ΔV_{mg} and ΔV_{fb} evinced from the C-V curves due to the ΔN_{ot} and ΔN_{it} charges that were generated by irradiation. Moreover, the memory window was found to increase with an increase in the radiation dose.

KEYWORDS: Charge Trapping memory device, Thin films, Gamma irradiation, CTM, PDA, C-V

ÖZET

$HFO_2/DY_2O_3/AL_2O_3$ TABANLI YÜK YAKALAMA BELLEK HÜCRESİNİN YÜK DEPOLAMA KAPASİTESİ ÜZERİNE GAMA IŞINIMININ ETKİSİ. PROGRAMINIZI SEÇİNİZ ADINIZI SOYADINIZI GIRINIZ BOLU ABANT İZZET BAYSAL ÜNİVERSİTESİ LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ FİZİK ANABİLİM DALI

(TEZ DANIŞMANI: PROF.DR. ERCAN YILMAZ)

BOLU, HAZİRAN - 2023
(XİV + 73)

Bu çalışmada Al/ $HfO_2/Dy_2O_3/Al_2O_3$/n-Si (100) şarj yakalama hafızalı (CTM) cihazlarında tavlama sıcaklığı ve gama ışını ışınlamasının etkisini araştırdık. Bu amaçla, Elektron demeti buharlaştırma (E-beam) ve RF şaçtırma teknikleri kullanılarak ince filmler büyütüldü. Örnekler 300^{o}C, 500^{o}C, 700^{o}C ve 900^{o}C sıcaklıklarda azot ortamında 40 dakika boyunca tavlanmıştır bir örnek ise olduğu gibi bırakılmıştır. İnce filmin kristalin yapısını ve yüzey dokularını araştırmak için X-Işını Kırınımı (XRD) ve Atomik Kuvvet Mikroskobu (AFM) ölçümleri yapılmıştır. 900^{o}C'de tavlanan numunenin 400 Dy2O3'te sadece bir zayıf pik'e sahip olduğu, diğer numunelerin ise amorf hale geldiği gözlenmiştir. Yüzey dokularının, tavlama sıcaklığındaki artışla azaldığı bulunmuştur. 2.06nm'lik en düşük Kök Ortalama Kare (RMS) değeri 900 ^{o}C'de bulundu. Ayrıca, frekans ve tavlama sıcaklığının CTM cihazının elektriksel davranışı üzerindeki etkisi, Kapasitans-Voltaj (C-V) eğrileri aracılığıyla araştırılmıştır. Arayüz durum yoğunluğunun, birikim bölgesindeki kapasitans değeri üzerinde son derece önemli bir etkiye sahip olduğunu bulduk. C-V eğrilerinin, tavlama sıcaklığının 500^{o}C ile 900^{o}C arasındaki artışıyla azaldığı da gözlenmiştir. Bu azalma yüksek tavlama sıcaklığında oluşan sarkan bağların ve ara yüzey tabakasının oluşumu ile ilgilidir. C-V eğrilerindeki pozitif ve negatif kaymalar, oksit tabakasında etkili pozitif ve negatif oksit yüklerinin varlığı ile ilişkilendirilmiştir. -10V ila +10V'da çeşitli tavlama sıcaklıkları için C-V histersis eğrileri incelendiğinde, 500^{o}C'de tavlanan aygıtın diğer aygıtlara kıyasla 0.44V daha büyük bir ΔV_{-fb}'ye sahip olduğu bulunmuştur. Ayrıca, ±10V ile ±12 arasındaki voltajlarda ΔV_{-fb} ölçüldü ve 700^{o}C'de tavlanan cihaz için ±12V'da 8.22V'luk en büyük bellek penceresi elde edildi. Bu durum cihazın iyi şarj depolama kapasitesi olmasıyla alakalıdır. CTM cihazına, Cs-137 gama ışını kaynağı kullanılarak 4Gy ile 128Gy arasında değişen farklı gama radyasyon dozlarda ışınlanmısı ile C-V eğrileri üzerinden radyasyonun etkisi yoğun bir şekilde incelenmiştir. Işınlama tarafından üretilen ΔN_{ot} ve ΔN_{it} yükleri nedeniyle hem ΔV_{mg} hem de ΔV_{fb}'de C-V eğrilerinden öngörülen bir kayma vardır. Radyasyon dozu arttıkça bellek penceresi değerinin arttığı tespit edilmiştir.

ANAHTAR KELİMELER; Şarj Yakalama bellek cihazı, İnce filmler, Gama ışınlaması, CTM, PDA, C-V.

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LIST OF ABBREVIATIONS AND SYMBOLS

AFM: Atomic Force Microscopy

CG: Control Gate

ALD: Atomic Layer Deposition

C_{ox}: Oxide Capacitance

CTM: Charge Trapping Memory

CTL: Charge Trapping Layer

C-V: Capacitance Volatage

EEPROM: Electrically Eraseable programmable Read Only Memory

EPROM: Eraseable programmable Read Only Memory

FN: Fowler- Nordheim

FG: Floating Gate

I-V: Current Voltage

MO: Metal Oxide Semiconductor

MIS: Metal Insulator Semiconductor

NVM: Non-Volatile Memory

PDA: Post Deposition Annealing

SONOS: Silicon Oxide Nitride Oxide Silicon

TEM: Transmission Electron Microscopy

TID: Total Ionization Dose

P/E: Program/Erase or Programming/Erasing

VM: Volatile Memory

XRD: X-RAY Diffraction

ACKNOWLEDGEMENTS

Firstly, I would like to express my sincere gratitude to my supervisor, Prof.Dr. Ercan YILMAZ for outstanding support, encouragement and guidance throughout my research. It is my great honor to be one of Prof.Dr. Ercan Yılmaz's student.

Many thanks to my friend and collegue Alex MUTALE for his tiresless help he rendered with the fabrication and in collection of results for this thesis. I would also like to express my sincere thanks to my friend and collegues who helped me throughout my master's study. They are, Mailes.C. ZULU, Emre DOĞANCI, Ozan YILMAZ and Umutcan GURER

My deepest gratitude goes to my parents, Francis and Ruth Chirwa for their encouragement, support, patience and their endless love. Lastly, I would like to thank all my family members for their encouragement.

This study was supported by the Presidency of Turkey, Presidency of Strategy and *Budget under Contract Number;2016K12-2834*.
The author would like to extend sincere gratitute to the NÜRDAM for allowing me to use the equipments during the course of this research work.

1.INTRODUCTION

The flash memory based devices have received an increadible amount of attention in the last decades, due to their wide range of applications such as radiation senosors, electronic devices and nanotechnologies(1–4). Tremendous growth has been witnessed in the semiconductor technologies and the devices based on flash memory are being of dominance Flash memories devices are data storage units used in morden electronic devices(5–7). These memories devices are classified into two groups namely;(a) volatile memory (VM) and (b) non-volatile memory (NVM)(2,8,9).

The only difference between these two memory devices is that in volatile memories, data is lost when power is switched off, while in non volatile memory can retain data even after power is turned off. The flash memory is an example of a non volatile memory. While dynamic random access memory (DRAM) and static random access memory (SRAM) are examples of volatile memories which are essential components widely used in computers(1,10). There has been a decline in the scaling down of volatile memory deivces, while for non volatile memory device it has been constant. The memory devices has become smaller size while having a higher bit density, thus resulting in higher performace(11–13).

With the growing demand of non-volatile memories have attracted research interest from various researchers. A MOSFETs based on charge trapping memmory devices consists of a floating gate (FG) and its main function is to store charges in the storage medium. Also it depends on the threshold voltage shift because of the injected electrons in the charge storage medium(14–16).

During the last decades, Si_3N_4 and SiO_2 have been used in CTM devices however, owing to their low dielectric constant and small conduction band offset These resulting in poor performance and high-power consumption of devices based on CTM cells(6,17,18). Therefore, to overcome such stated challenges, several high-k materials have been investigated by various researchers and these are ZrO_2, HfO_2, Yb_2O_3, Y_2O_3, Er_2O_3, Al_2O_3 and many more. These high-k materials have been used as blocking, tunnling and charge trapping layers in CTM devices(11,19–22).

For instance, Sahin et *al;* used HfO_2 as the tunnling layer. They found that Gemanium atoms diffused into HfO_2 atoms during the deposition and annealing temperature(23). Lan et *al*; also used Al_2O_3 as both blocking and tunneling layers. They found that by increasing the number of Al_2O_3 layers could lead to an improvement of the charge storage capability after Rapid thermal annealing treatment(24). Morevoer, Pan et *al*; fabricated CTM devices and Y_2O_3 was used as the charge trapping layer. They found that the XPS results showed the formation of a thicker Yittrium silicate(25). To our knowledge, however, there has not yet been any work done in previous research using HfO_2, Dy_2O_3 and Al_2O_3 as the blocking, charge trapping and tunneling layers, respectively.

Therefore, in this study we have investigated the effect of post deposition annealing temperature and cobalt gamma irradiation on $HfO_2/Dy_2O_3/Al_2O_3$/n-Si sttucture. This is due to their unique electrical properties of afromentioned high-k materials such as large conduction band offset, high dielectric constant, wide energy band gap and low leakage current(26–28).

2.AIM AND SCOPE OF THE STUDY

The purpose of this work is to look into how the Cs-137 gamma irradiation and annealing temperatures affect the charge trapping memory (CTM) cells made of $HfO_2/Dy_2O_3/Al_2O_3$/n-Si (100). E-beam and RF sputtering techniques were used to deposit the thin films, respectively. One sample was left as-deposited, and the other samples were annealed for 40 minutes at various temperatures of 300°C, 500°C, 700°C, and 900°C in a N_2 environment. XRD and AFM techniques were used to examine the surface morphologies and crystalline structures. Through C-V curves at 1MHz, the electrical characteristics of the devices, such as flatband voltage and memory window, were acquired and investigated.

Then, using a CS-137 gamma irradiation source with a dosage rate of 497Gy/h, we looked at the effects of gamma irradiation on CTM devices at various doses of 0Gy, 4Gy, 8Gy, 16Gy, 32Gy, 64Gy, and 128Gy. The C-V measurements were carried out both before and after the 1MHz gamma radiation. Additionally, the results of our experiment have been thoroughly examined and contrasted with those found in other investigations.

2.1 Thesis outline

The content of each chapter of this thesis is as follows:

Chapter 1, General overview of flash memories is discussed. The volatile memory (VM) and non-volatile memory (NVM) devices are also analyzed. The works that have been done by several resarchers are also reviewed.

Chapter 2, The rest of this chapter contains the literature review and detailed explanation the MOS capacitor and its working principle. The oxide charges in MOS capacitor have been discussed. The effect of radation in material and in MOS capaictor have been reviewed. In addition, the basic working principle of charge trapping memory cells is also reviewed.

Chapter 3, Provides the fabrication processes of charge trapping memory cells. Also, provides the materials that were used during the experiment. The characterization techniques that were used in this work have been added.

Chapter 4, Provides the experimental results that have been obtained in this thesis. The findings from our experiment have been contrasted with those found in the literature by other researchers.

Chapter 5, The obtained results have been discussed in detail.

Chapter 6, The conclusion of the study as well as the recommendations

2.2 Litrature review

2.2.1 Non volatile memory (NVM) cells

There has been an explosive growth in the portable elctronic devices world market of recent. Due to this explosion, the NVM in semiconductor industry has received alot of attention. The main types of NVM are; Electrically Erasable Programmable Read-Only Memory (EEPROM) and Flash. These have received a tremedous amount of attention because of their capability to continue scaling down and improved performance(29–31). There are two transistors that are in an EEPROM cell while only one transistor in the flash cell. Because of their differences in transistors, the flash memories provide a higher chip densisty than EEPROMs. Charges are stored in the floating gate in both the EEPROMs and flash memories(32–34).

During the last decades, flash memories have gained more advantage over other NVMs because they possess the ability to be programmed and erased several times, high data storage density and are easy to fabricate too, hence lower cost(35–37). The composition of the flash memory can be likened to that of a MOSFET Unlike the MOSFET, the flash memory consists of charge storage layer between the substrate and the gate, whereas the MOSFET is made up of several

parts namely (a) gate, (b)a gate insulator, (c) subtrate, (d) drain, (e) source and (f) channel(36–38).

A flash is a combination of EEPROM's enhanced functionality and EPROM's density. With the select transistor absent, it resembles EEPROM memory. It's name originates from it's quick erasing technique. Flash memory is currently the most produced memory due to it's favourable properties and new applications, which are driving the market at a faster average annual rate than DRAM and SRAM(39–41). Flash memory can be employed into two alternative architecturres, depending on their applications. Fast reading and random memory access are feature of NOR flash memory that are important for retrieving data from the memory. While the NAND has tremendous density and quick write speeds, it reads data slowly(42–44).

Due to its unique characteristics, high performance and low cost, the floating gate has stood out in the semiconductor market. Figure 1.1 shows the structure of the FG flash memory. As shown in the figure, the FG flash memory is placed between two insulating thin films (42,43,45). The nature of the FG is to store charges. The highly doped poly-Si gate is separated by the tunnel layer. The tunnel layer acts as the barrier to block charges from leaving the FG. An insulating material is prefered for the tunneling layer, this is because, during programming or erasing the electrons can pass through during tunneling. The blocking layer is made of insulating material as well(38,43,46).

2.3. Structure of metal oxide semiconductor (MOS) capacitor

MOS is a heart of MOSFTEs device and made of three layers namely;(a) semiconductor material and then (b) oxide layer that could be SiO2 or high-k dielectric material and last one (c) metallic layer which is generally Al(47–49). Figure 2.1. shows schematic representation of MOS capacitor.

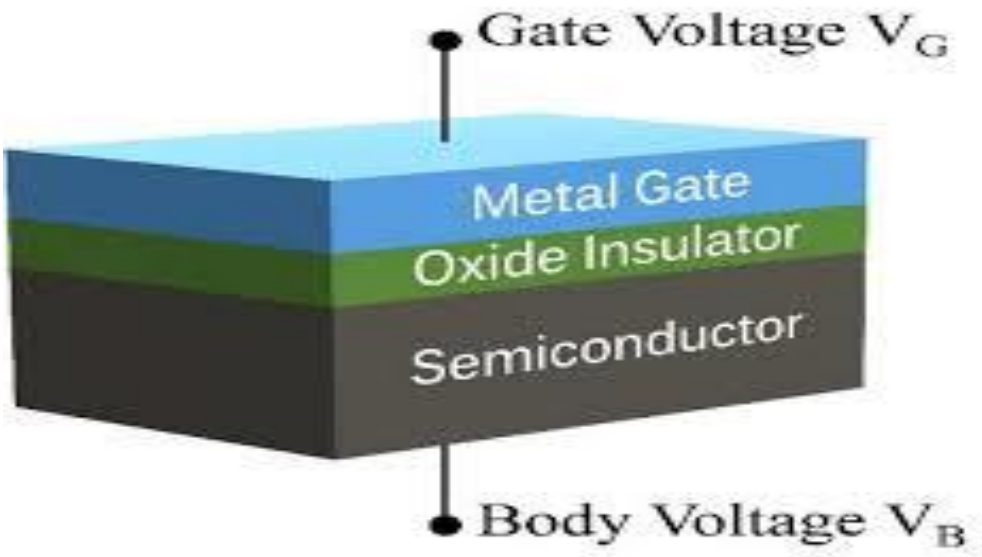


Figure 2.1. Schematic representation of MOS structure.

2.4 Ideal MOS capacitor

There are four conditions that we have to consider for an ideal MOS capacitor. The first condition, the work function (ϕ_m) of a metal and that of the (ϕ_s) semiconductor are equal. Second condition, the oxide does not possess any charges inside. In other words, no charges within the oxide layer. Third condition, the oxide possesses infinity resistivity, which means there will be no current flowing through the oxide regardless of the applied voltage. Fourth condition, there is no surface states at the oxide-semiconductor interface. Moreover, the energy bands of an ideal an MOS capacitor there always horizontal Therefore, the MOS capacitor will be working under equilibrium condition(50–52).

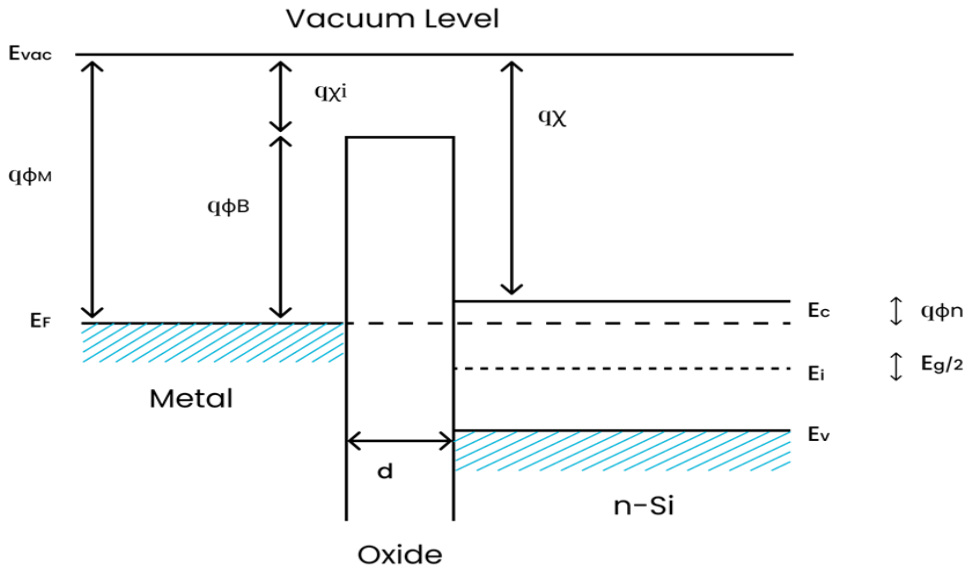


Figure 2.2. Schematic representation of energy band diagram of an ideal MOS capacitor for n-type Si substrate.

2.4.1 Accmulation region

When the positive voltage is provided to the gate terminal of a metal, the positive charges will be accumulated at the oxide/metal interface. The electric fields (E) that have been induced will move away from the oxide/semiconductor interface. Since electrons are majority charge carriers in the n-type Silicon. These charges will move towards the semiconductor/oxide interface. In other words, they will attract to the positive charges that have already been accumulated at the gate due to different polarities. Therefore, the MOS capacitor will be working under accumulation region and the energy bands will bend downwards(50,53,54) as shown in Figures.

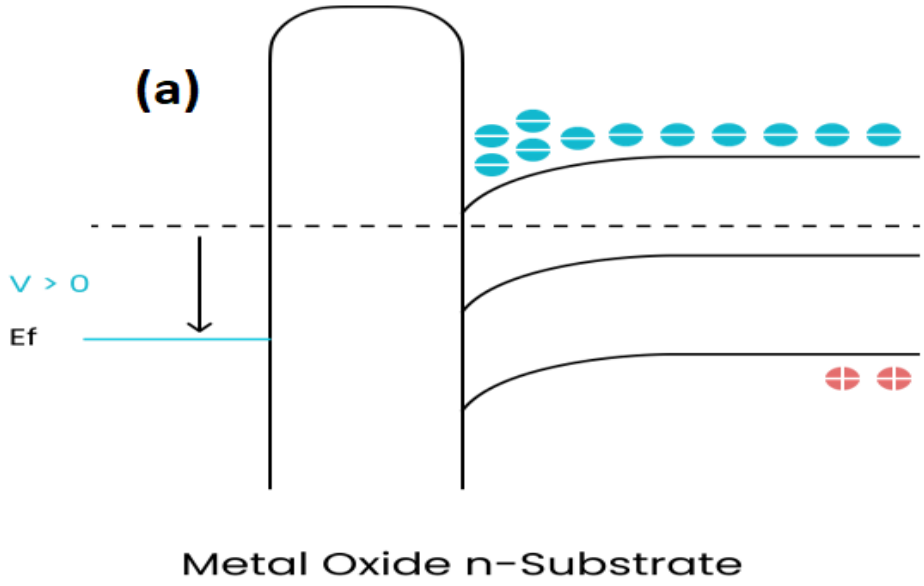


Figure 2.3. (a) Schematic representation of energy band diagram of n-type MOS capacitor during accumulation region.

2.4.2.Depletion region

When the small negative voltage is provided to the gate terminal, the negative charges will be accumulation at the gate/oxide interface. Since electrons are majority charge carriers in the n-type Si. These charges will move away from the semiconductor/oxide interface. In other words, these charges will be repelled from the negative charges that have been induced at the gate as the result of same polarity. The electric field that has been induced will move upwards. Therefore, the MOS capacitor will be operating under depletion region and the energy bands will bend downwards(49,55,56) as shown in Figure 2.4(c).

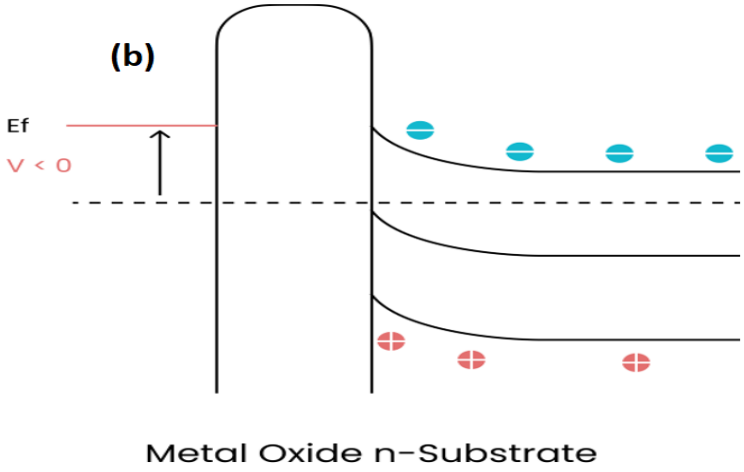


Figure 2.4.(b) Schematic representation of energy band diagram of n-type MOS during depletion region.

2.4.3. Inversion region

When more negative voltage is provided to the gate terminal, the electric fields will increase more rapidly as the results more amount of induced space region. Also, more negative and positive charges will be absorbed and then across the two sides of the oxide. But the electric field will be in the same direction or move upwards. The MOS capacitor will be working under the inversion region and the energy bands will be bend more downwards(57–59). as shown in Figures.

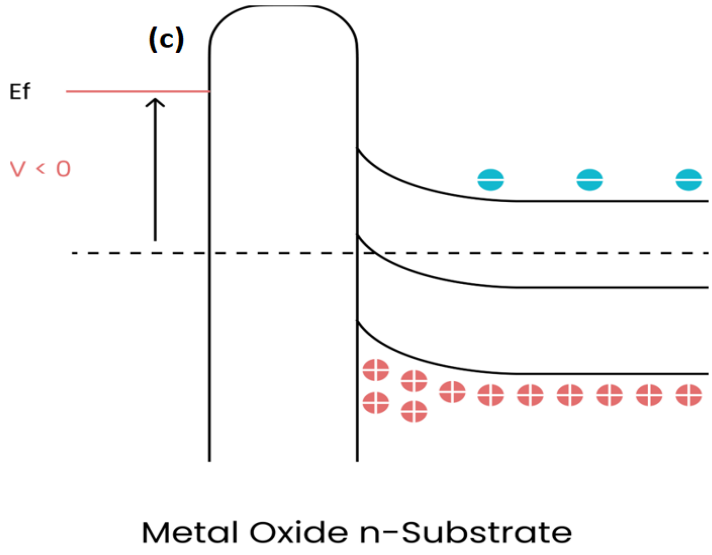


Figure 2.5.(c) Schematic representation of energy band diagram of n-type MOS capacitor during inversion region.

2.4.4.MOS capacitor oxide charges

Generally, there are four types of charges namely; (a) fixed oxide charges, (b) mobile ionic charges, (c) interface trapped charges and (d) oxide trapped charges. These charges affect electrical characteristics of an ideal MOS capacitor is given in Figure 2.5.

(a) Fixed oxide charges (Q_f,N_f).

The fixed oxide charges Q_t normally exists near the interface and are highly immobile under the influence of an electric field. These charges are always positive near the oxide/semiconductor interface because there is no two oxygen atoms for one silicon transition layer. So all the silicon atoms by the bonding. Hence, there is always a positive charge that is generated during the oxidation. The Q_{it} can be reduced in argon or oxygen during high annealing temperature(60–62).

(b) Mobile ionic charges (Q_m, N_m)

The mobile ionic charges generated by ionic impurities in the oxide layer such as Na+, Li+, K+, and H+. These charges can lead to the shift in the C-V curves and metal atoms are too prevalent(63,64).

(c) Interface trapped charges (Q_{it}, N_{it}, D_{it})

The interface states charges are located at the oxide/semiconductor interface with energy states in the silicon forbidden bandgap and which can exchange charges with silicon within a very short period of time. Qit can be either positive or negative within oxide/semiconductor interface. These charges are caused by oxidization induced defects, structural defects, metal impurities and ionizing radiation. For the present MOS capacitors most of these charges can be neutralized during low annealing temperature in hydrogen ambient at 450^{o}C(65–67).

(d) Oxide trapped charges(Q_{ot}, N_{ot})

The oxide trapped charges can be also either positive or negative due to holes and electrons within the oxide. The Q_{ot} are generated by x-ray radiation on hot electron injection. These charges are distributed within the oxide layer. However, no cure Q_{ot} and measured neutrality. Moreover, on electrical properties, charges can have a big impact on the fabricated MOS capacitors and therefore leading to the poor performance.(67–70).

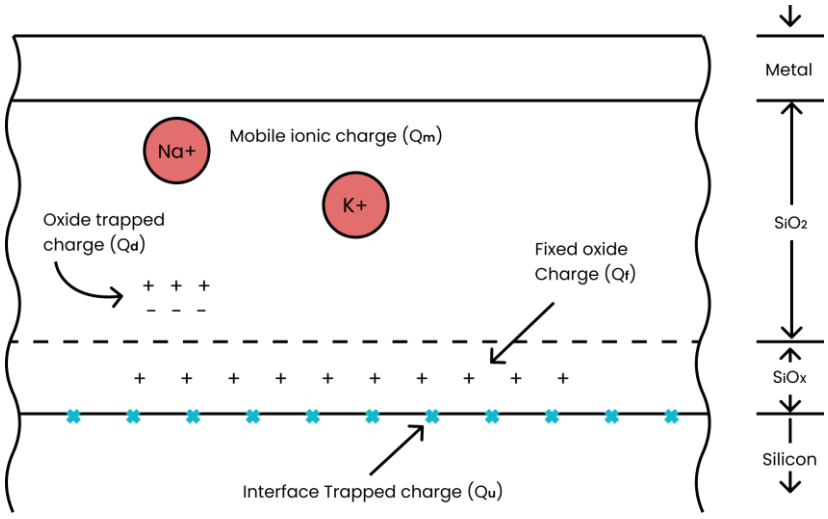


Figure 2.6. Schematic representation of oxide charges in MOS capacitor.

2.5. Radiation effect in material

Whenever we investigate nuclear reaction various kind of nuclear particles are produced. Nuclear particles are very tightening, and we cannot see them through microscope techniques. The best way to detect them by is using advanced equipment's which are known as detectors. The detector is just an instrument or solid material, in which some external nuclear particle passes through and then generates different kinds of phenomena. Moreover, if the detector is well successful for detecting that phenomenon. Subsequently, it can tell us which particle is involved and the energy of the particle involved and other such parameters(50,71,72). Therefore, from that perspective is very important to understand various kinds of interaction of nuclear radiation with matter. Because it can lead us to develop various sorts of equipment's or nuclear detectors which can detect different kinds of particles. Nuclear particles can be divided in three groups namely: (a) gamma photons or simply photons which are emitted in a nuclear reaction, (b) charge particles one of them could be electron or positron and (c) alpha particle or some other isotope or heavy charge nuclei. Depending upon which particle is released in a nuclear. It can generate different sorts of phenomena, after entering in the material medium(73–76).

Whenever gamma radiation is emitted in some kinds of nuclear reaction, and this can lead to the production of various phenomena in a material medium. These phenomena can be categorized in three groups as follow: (i) Photoelectric effect (ii) Compton effect and (iii) Pair production.

(i) Photoelectric effect

Whenever some kinds of high energetic particle incident onto the surface of the material and this resulting in the rejection of electrons. This process is known as photoelectric effect as shown in Figure 2.6. In other words, when some sorts of nuclear gamma radiation pass through the material medium and then it results in the emission of free charge carriers, which are known as electrons. Therefore, this in case the kinetic of electron can be found by using the equation below(50,77).

$$E=h\nu - \phi_m \qquad (2.1)$$

Where h is a Planck's constant of 6.63×10 -34 J.s, v is the incident frequency of a photon and ϕm is work function of the material. The above equation was discovered by Albert Einstein and thereafter in 1921, he was awarded Noble price in Physics due to this equation. Understanding Photoelectric effect is quite easy because charge carriers, which are electrons, are usually tightly bound to each atom within a given material. To free these charge carriers a certain amount of energy in the form of heat or radiation must be applied to the material. So, when the incident of nuclear radiation falls onto the material medium, it basically interacts with the electrons which are tightly bound in the atomic structure of an atom(71,74,78). If the energy of incident photon is quite enough and then electron can absorb that energy and become free from the potential of the atom itself. The excess amount of energy usually gets converted into the kinetic energy of charge carrier(electron). Since the ionization energy of electron is not very high to induce the Photoelectric effect. Therefore, there is no need for huge amount of energy photon. Generally, Photoelectric effect usually can be induced by low energy photon or photons which have less than(E<0.1MeV). Moreover, Photoelectric is generally seen for gammas which are very low energy and the effect of this is just to free up electrons or ionizing the material(72,74,78,79).

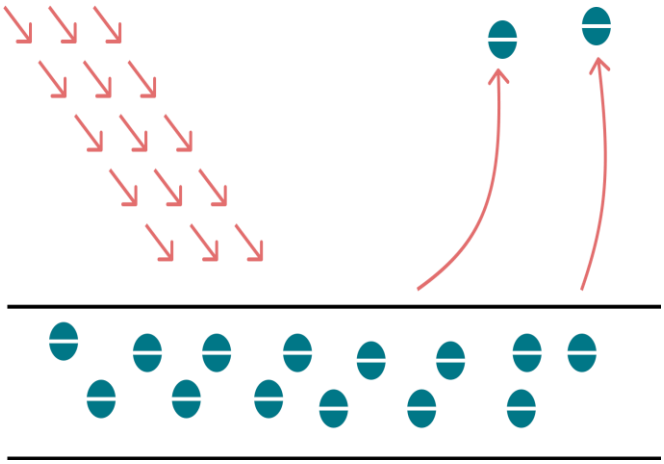


Figure 2.7. Schematic representation of Photoelectric effect process

(ii) Compton effect

Compton Effect generally occurs for higher energy detecting photons. When energy having E=hv interacts with some electrons which might be tightly bound within an atom or might be free electron in that case. The photon has to have huge amount of energy and it will be a free electron and it will elastically scatter from the electron. There will be also scattered radiation having certain frequency which is less than the incident radiation(71,80,81).This process is called Compton effect and the equation associated with Compton equation which is basically gives the change in the incident radiation and scattered as(71,73,82),shown in Fig 2.7. Therefore, the kinetic energy of electron is given by

$$\lambda' - \lambda = \frac{h}{moc}(1 - cos\theta) \qquad (2.2)$$

The high energy photon not only ionizes the material medium but also get scattered from the medium with frequency which is less than the incident frequency. This type of phenomena is more dominant for energy photon having in the range of 0.1< E10 MeV(73,82).

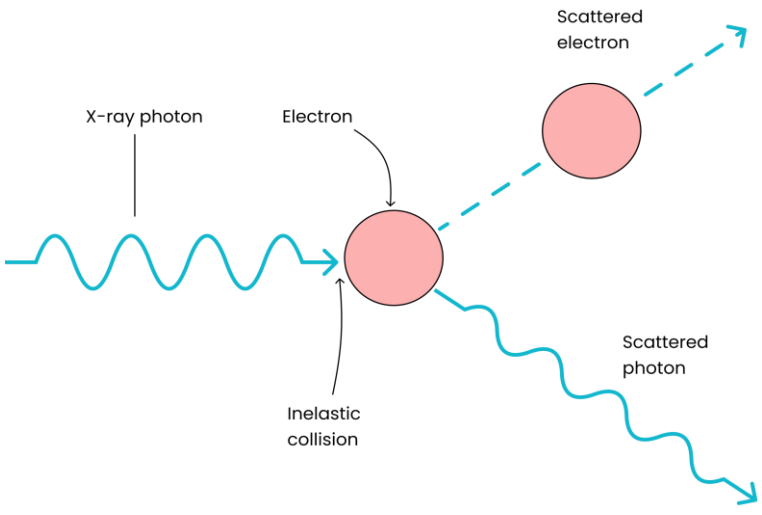


Figure 2.8. Schematic reprensetation of Compton effect process.

(iii) Pair production

To understand pair production, the thing, we need to understand pair annihilation. When the particle let's suppose an electron or positron comes together and then leads to the creation of pure energy. The reverse to this kind of process is also possible. Where pure energy gets transform into a matter version of an electron and anti-matter version of an electron is called Pair production(83,84). So, when some huge amount of energy of gamma photon comes close to some sorts of external nucleus and the potential field of that nucleus. The energy of gamma photon can result in the creation of an electron as well as positron as shown in Figure. Since the radiation energy is creating matter the energy of the radiation must be greater than the rest mass energy of both these particles and is given by(50,71,84).

Therefore, this kind of process is not possible for low energy detecting particle. This process only occurs for extremely high energy detecting particle, which has an enough amount of energy to create this kind of electrons and positron pair in the first place. Moreover, this process is more dominat for energy greater E> 1.0MeV(83,84).

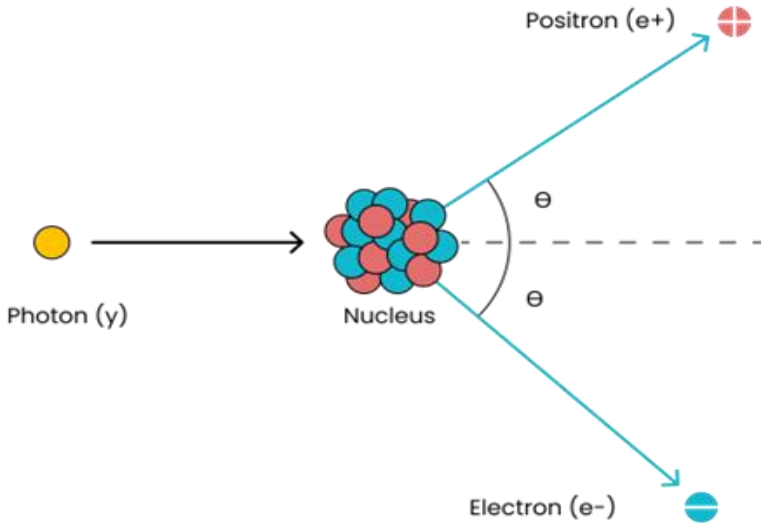


Figure 2.9. Schematic representation of Pair production process.

2.5.1 Radiation effect in MOS capacitor

Figure 2.9, shows energy band diagram of the MOS structure during irradiation. It consists of gate electrode, gate oxide silicon interface and semiconductor substrate which is silicon. When the positive gate voltage is applied, it pulls down the gate electrode and then electric field is induced across the oxide. So, the negative charges which are electrons in the conduction band of oxide layer will move towards the gate. Then, these charges are attracted to positive gate voltage(85–87). Moreover, the basic working principle of the MOS capacitor has already been explained in the previous section.

When the MOS capacitors are exposed to high energetic particles such as gamma irradiation. This radiation is absorbed and resulting in the creation of electrons-holes pairs within the oxide layer. Because gate oxide is one of the most sensitive parts in the MOS capacitor. After that, both electrons and holes will move in the opposite direction due to the existence of electric field. The electrons in the conduction band of gate oxide will be removed and then leaving behind holes in the oxide layer(88–90).

The holes that have already been created in the gate oxide, are slightly immobile compared to electrons. So, they start moving in a hopping mechanism as shown in Figure 2.9. Thereafter, they start falling into the low-level traps. In other words, in low energy level traps alongside the valence band edge and in the hopping mechanism. These positively charges which are holes, they start moving from trap to trap towards the interface. Due to the presence of positively voltage, the holes will be pushed up(88,91,92).

The traps are generally bounded by hydrogen and protons. The hydrogen is released by holes that already been moved into the traps. Afterwards, there will be a dual effect of holes that moves in the right side and continue releasing protons and hydrogen ions. In the presence of induced electric field, the hydrogen ions are also accelerated to the right side(88,90,92). Once the holes reach the interface, there is always large population of deep level of traps. These traps are located at the center of the band gap. Again, in the oxide there is band gap which is located between valance and conduction bands. Then, the deep traps will be in the middle of energy band gap(86,90,93).

Therefore, the holes will start moving downwards towards the interface and subsequently the holes will be trapped within the gate oxide. This kind of process is so known as quasi static or quasi stable trapping state. Since the holes are trapped in the oxide, they are no longer free to move from place to another. This process is like the proton transport, the protons will reach the interface and then produce the interface state defects. These charges can be positively charged, negatively charged or neutral. They depend on the kind of defects that are generated(94–97). Moreover, all the process can be seen in Figure 2.9.

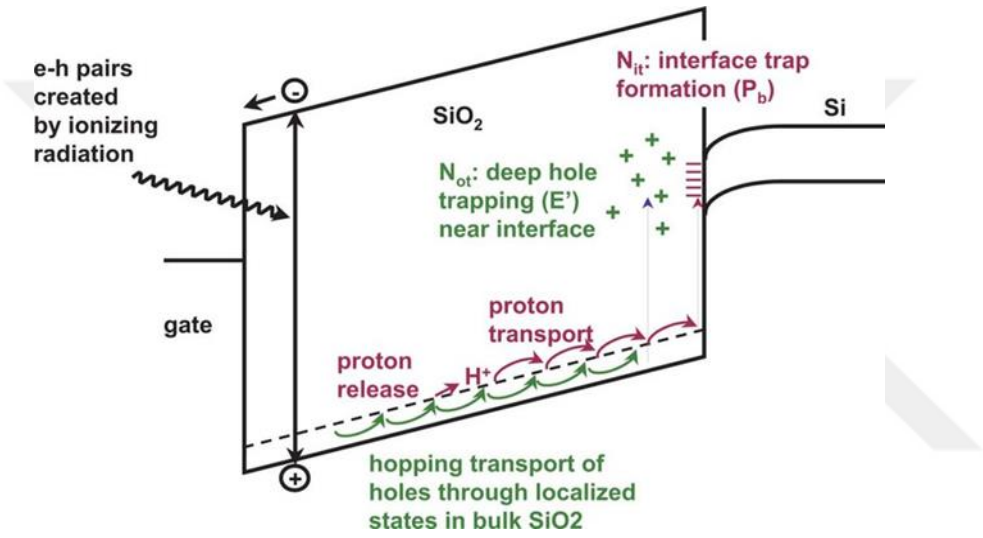


Figure 2.10. Schematic representation the change of energy band within the MOS capacitor under irradiation.

2.6 Charge trapping memory (CTM) cell

The design of the charge trapping memory cell is alike to that of the MOS capacitor. The only difference between the two is that, between the blocking layer and the tunneling layer, a charge trapping layer is added. Figure 2.10, shows the cross section of the CTM device. The unique feature of a charge trapping layer, distingues it from other flash memories. The CTL which is sandwiched betweeen the blocking layer and the tunneling layer acts as the charge storage. The layer between the gate and the charge trapping layer is the blocking layer. While the tunneling layer is between the substrate and the charge trap(98–101).

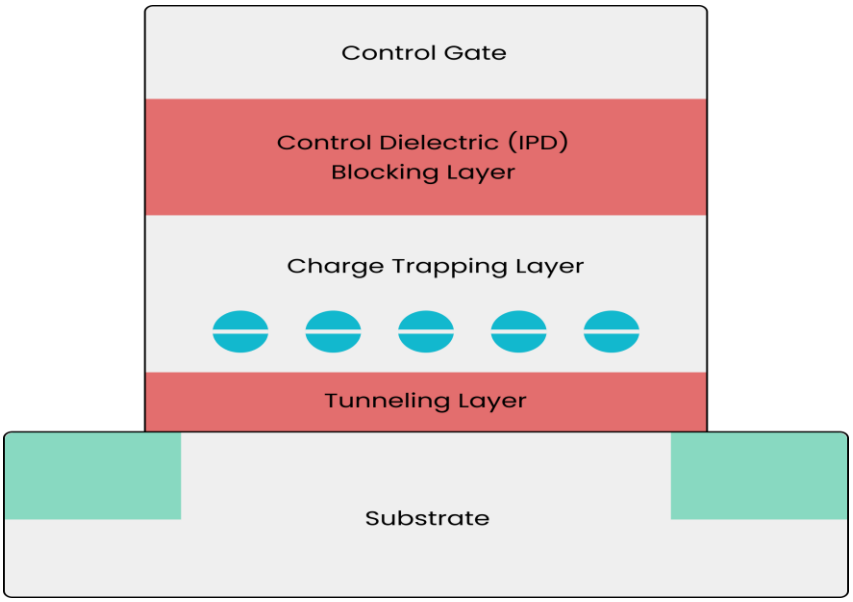


Figure 2.11. Schematic representation of charge trapping memory(CTM) cell.

2.6.1 Basic working princple of CTM cell

When a positive pulse is placed at the gate, the electrons are injected into the charge trap dielectric. When this occurs, the CTM cell is the said to be in program mode. When a negative pulse is placed at the substrate, it causes the holes from the substrate to migrate into the CTL. During this occurance, the CTM is said to be in erase mode. The insertion and removal of charges in the CTM determines the digital ‘’1’’ and’’0’’ which are called as program and erase respectively(100–102). Meanwhile, if the pulse is removed from the substrate, the charges may move back to the CTL. The duration of thses charges in the CTL is dependant on the high band offset on the interface of CTL-TL and BL-CTL interface, they can prevent the charges from moving back to the substrate and/or discharge to the control gate. Due to this possibility, the thickness of the BL is very important. The thickness of the BL has a huge impact on the program/erase speed of the CTM(103–105).

2.6.2 Blocking layer (BL)

Over the last decades, SiO_2 was the prefered material to use in the early makings of the SONOS memory. The SiO_2 was chosen on account of its large ΔE_c with respect to the CTL. As ealier stated, the sole purpose of the BL is to block the charges from the gate enetering the CTL and vice versa prevent the charges in the CTL from leaving the BL. In the SONOS devices, the erase speed is determined by the mixture of electron and hole direct tunneling through a blocking layer from the control gate(106–109). The replacement of SiO_2 with a high-k material causes the band bending at the electric field in the blocking layer to decrease while in the charge trap and tunnel layer they increase. A blocking layer has to be thicker than the other layers in order to reduce back tunneling from gate to the trap layer. Besides, it should create superior interface with the CTL and the gate(39,40,110).

2.6.3 Charge trapping layer (CTM)

The charge trap layer is a very critical layer of the CTM cell. This is because that is where the charges are stored and it has impact on the program and erase execution of the memory. Therefore, the charge trap layer has to be optimized. In the SONOS the Si_3N_4 was set as the charge trap material. The primary reasons why Si_3N_4 came about to be used as a charge trap was because of its high trap density, good thermal stability with tunnel layer and blocking layer. Nevertheless, due to the scaling down, Si_3N_4 is no longer befitting to be used as a charge trap layer, due its low dielectric constant(k~7) and a small conduction-band offset relative to SiO_2 (39,44,45,111,112). For this reason, quiet a number of reseachers have been done on high-k materials in order to replace Si_3N_4. Materials with high-k such as Yb_2O_3, Gd_2O_3, ZrO_2, Ta_2O_5, Y_2O_3 are some of the high-k which have been implemented as replacements of charge trapping layers. Moreover, the replacement needs to possess a high trap density, a lower conduction band offset reciprocal to the tunneling layer (TL) and a higher electrical breakdown than that of the TL(33,113,114).

2.6.4 Tunneling layer (TL)

Besides improving the blocking layer (BL) and charge trapping layer (CTL) in the CTM cell. The TL too has not been left out. SiO_2 was implemented as TL in both the FG and SONOS memories. Despite the many works that have been carried out to improve the TL, none of them have shown very excellent properties much better than SiO_2. The TL is made to facilitate electron tunneling during programming and erasing process, unlike the BL, which is always necessary for total electron blocking. In this situation, the physical thickness advantage of high-k dielectric is no longer useful because a thicker TL significantly slows down the device's operation(115–117). High trap density in the tunnel layer will cause a significant leakage current and low breakdown, electric field, which will result in poor endurance characteristics. Hence, until a high-k dielectric material with good quality on Si could be created, thermally generated SiO_2 with low trap density is still frequently utilized as a tunneling layer. Therefore, a high-k material with excellent qualities will deliever greater retention properties without compromising operating speed. It will as well permit further scaling down of the device(116,118,119).

2.6.5 Program/erase speed

In order for data to be stored in a flash cell, a minimal ΔV_T should be attained by erase and erase. The programming speed occurs immediately a postive bias pulse is placed on the control gate (CG), electrons present in the substrate are shot up into the charge trapping layer thereby attaining a new V_T. However, the erase speed measurement is observed when a negative bias pulse is put on the CG, some holes that are in the substrate are pushed up into the charge trapping layer while some electrons in the charge trap fall back into the substrate which brings about another V_T (95,120–122). The difference between these two V_T values is know as ΔV_T. In the SONOS device, it is observed that programming speed is

faster than erasing speed. This is due to the small barrier height for electrons (3.2eV) that holes (4.7eV) at the SiO_2/Si interface. There are typically two ways to describe the P/E speeds. The initial strategy to fix the applied voltage and pulse duration and larger $\Delta V_{T\,means}$ faster P/E. Second is V_T correction and lower applied voltage and short pulse time means faster P/E(123–125).

2.7 Programming mechanisms in CTM cell

There are two main methods used to program a flash memory cell: Fowler-Nordheim (FN) and the Channel Hot Electron (CHE).

2.7.1 Fowler-nordheim programming

The fowler-nordheim programming is carried out by maintaing source, drain, and bulk grounded while delivering a positive high voltage to the control gate terminal (approximetly 20V). Due to the FN tunneling of charge from the channel to the floating gate, a gate current is produced by the high electric field generated through the tunnel oxide. Through the triangular energy barrier of the tunnel oxide, electrons in this tunnel effect move from the silicon conduction band into the floating gate(124,126,127). There are more trapped electrons in the floating gate after the FN programming. The electric field across the tunnel oxide also reduces This leads in the reduction of floating gate potenital. As long as the electric field in the tunnel oxide has not cancelled. The charge injection will keep going due to the interpoly dielectric layer's maximum drop potential. Due to the fact that there is no current flowing across the channel, despite the operation's modest speed (order of milli seconds) and it uses very little energy(27,32,49,112).

2.7.2 Channel hot electron programming in CMT cell

The channel hot programming is carried out by applying a positive high voltage on the gate of +10V and drain of 5V terminals. While keeping the bulk and source grounded. The high lateral electric field created by drain/source bias

accelerates the electrons first significantly in the pinchoff area. The verticle electric field created by the postive voltage given to the gate electrode allows the electrons to be injected into the floating gate after they have attained a high kinetic energy(26,48,118). Channel hot electron (CHE)programming is quicker than FN. In addition, the CHE is ineffiecent (just a small number of electrons are injected relative to the total number of electrons flowing from the source to the drain, which leads to significant power cosumption(33,34,128).

2.7.3 Memory window

The memory window is one of an important property in the CTM cell. An estimation of the tunneling layer wearing out can be made using the "memory window ", which is defined as the difference between program flatband voltage and erase flatband voltage. This is because as the capacitor is programmed and erased, strong electric field stress and high injection current flow through the tunneling layer, causing flaws in the tunneling layer(129–131).

2.8 Characterization techniques

During the last last decades, several equipments have been developed for the thin film characterizations. For instance, x-ray diffraction (XRD) and atomic force microscopy (AFM) techniques. These techniques can be used investigate the crystalline structures and surface morphologies of the fabricated material(132–134). In the following subsections, the stated above tecniques will be reviwed.

2.8.1 X-ray diffraction (XRD) technique

The atomic and molecular structure of a material can be ascertained by using the x-ray diffracation (XRD) method. In order to do this, incident X-rays are used to irradiate a sample of the material, which is then subjected to measurements of the X-ray intensities and scattering angles The structure of the material can be ascertained from the examination of scattered from the

examination of the position in the angle and intensity of the scattered X-ray are shown as a function of the scattering angle(135,136). Not only can the average location of the atoms in the crystal be measured, but it is also possible to find out how the actuals tructure differeds from the ideal one(),due to, for instance, to internal stress or defects.(135–137).

When light waves with a small enough wavelength strikes a crystal lattice, they diffract from the lattice points. The diffracted parallel waves constructively interfere and produce audible peaks in intensity at particular angles of incident. W.H. Bragg an english physict recorgnized the relationship and came up with the equation below know as Bragg's law(135,136).

$$n\lambda = 2d \sin\theta \qquad (2.3)$$

2.8.2 Atomic force microscope (AFM)technique

Using an equipement called Atomic Force Microscope, samples can be examined and described at the microscopic level. Therefore, we may examine surface properties with a precision that is quiet exact and ranges around 100μm to about less than 1μm. Atomic force microscope works by sensing surface areas by employing an extremely sharp tip on a micromachined silicon tip. The technique varies significantly across various oprating modes but it involves diagonal scanning a sample across the surface line by line(138–140). Contact mode and dynamic or tapping, mode are the two most common operating modes. Compared with other forms of microscopy, AFM posses more advantage than SEM. Because AFM is able to offer 3-dimensional surface information. Apart from imaging, AFM can also be utilised to control the molecules as compared to SEM(139–141).

3.MATERIALS AND METHODS

In this section explains the steps that were carried out to fabricate the charge trapping memory (CTM) devices. The fabrication of $HfO_2/Dy_2O_3/Al_2O_3$ CTM device was carried out in class 100 clean room at NÜRDAM.

3.1 Samples preparation and the cleaning of wafers

To remove some of the impurities from the surface of the wafers. The wafers were cleaned by using RCA cleaning processes. We used the n-type (100) Si wafers with a resistivity of 1-10Ω.cm. The steps were done as follows:

Firstly, organic Cleaning-200ml of deionized water (H_2O),40ml of NH_4OH and 40ml H_2O_2 equivalent to the ratio (5:1:1) solution was prepared. This solution was heated upto 80^oC. The wafers were placed in the solution for 17min. Secondly, metallic cleaning the wafers were placed in 180ml deionized wafer (H_2O),30ml HCl and 30ml H_2O_2 mixture of volume ratio (6:1:1) for 17min. Lastly, the wafers were submerged in H_2O (100ml) and HF (1ml) solution for 15seconds. Moreover, each step the wafers were rinsed with water and dried in N_2 And all the cleaning processes were carried out by using the equipment in picture 3.1.

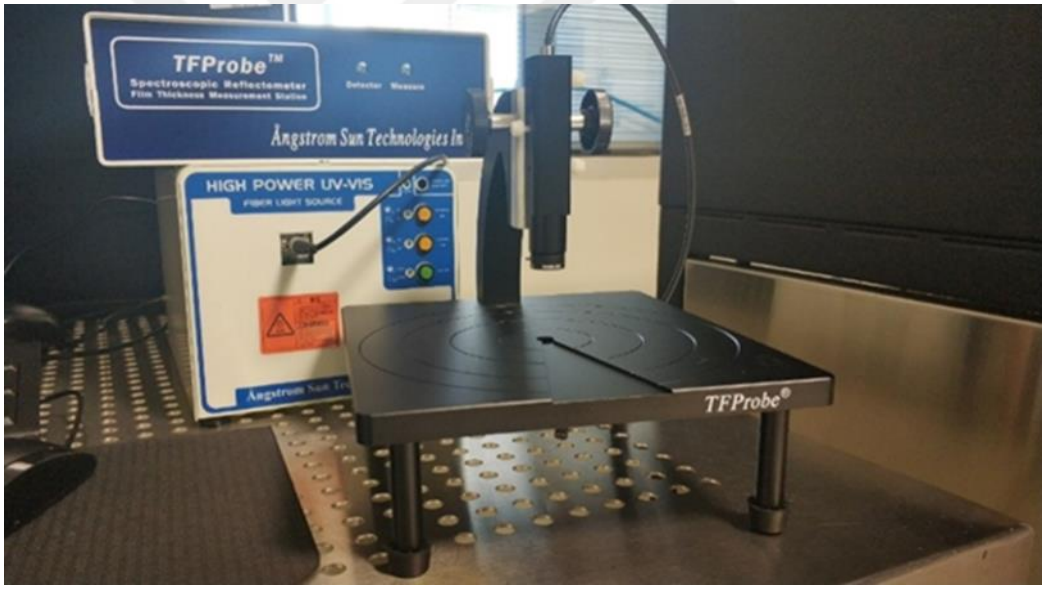
Picture 1. Wet chemical benches for wafer cleaning in NÜRDAM at Bolu Abant Izzet Baysal University.

3.2 Fabrication of charge trapping memory devices

Following the RCA cleaning procedures, the wafers were immediately moved to the RF magnetron sputtering method for the deposition of the tunnelling layer using 99.99% pure Al_2O_3. Pre-sputtering was done to clean the target of contaminants for 15 minutes. Following that, deposition was carried out at substrate temperatures of 250°C, $6.8x10^{-4}$Pa deposition pressure, and 200W of RF power for 150 seconds. The wafers were then placed into an E-beam evaporation process to deposit a charge trapping layer of Dy_2O_3. Deposition parameters included a substrate temperature of 100 °C, a deposition rate of 0.60 mA, a pressure of $5.5x10^{-3}$, and a deposition time of 100s. Once more, the samples were moved to the magnetron sputtering method to deposit a blocking layer using a 99.99% HfO_2 target. Pre-sputtering took place for 15 minutes before to deposition. Then, HfO_2 thin films were deposited onto the wafers at a substrate temperature of 100°C, a deposition pressure of $6.6x10^{-4}$Pa, and a deposition power of 200W for 4min. The samples were separated into four sections after the deposition process, leaving one sample to remain as-deposited. The samples were

then exposed to annealing temperatures of 300^{o}C, 500^{o}C, 700^{o}C, and 900^{o}C for 40 minutes in a N_2 environment. The samples were fed into an RF magnetron for sputtering after the annealing procedure in order to create the gate electrodes and back contacts. By sputtering the Al target for 1 hour at 200W power, a metallic shadow mask with a 1.5mm diameter was created for gate electrodes. As the Al was sputtered for 45 seconds, the back contact was created. A schematic diagram of the fabricated charge trapping memory (CTM) is shown in Figure 3.1. Using a Keithly SCS system, the C-V measurements were performed at 1MHz.

Afterwards, the device which was annealed at 700^{o}C was exposed to Cs-137 gamma ray source at different doses of 0Gy, 4Gy, 8Gy, 16Gy, 32Gy, 64Gy and 128Gy with a dose rate of 497Gy/h as shown in picture 6. Morevoer, the C-V measurements were performed before and after gamma irradiation at 500kHz without appliying external voltage.



Picture 2. Angstrom Sun spectroscopic reflectomemter used for measuring the thickness of the deposited thin film in NÜRDAM at Bolu Abant Izzet Baysal University.

Picture 3. Annealing furnance in NÜRDAM at Bolu Abant Izzet Baysal University.

Picture 4. RF magnetron sputtering technique in NÜRDAM at Bolu Abant Izzet Baysal University.

Picture 5. E-beam eveporation technique in NÜRDAM at Bolu Abant Izzet Baysal University.

Picture 6. Schematic representation of Cs-137 gamma ray radiation source at TAEK.

Table 1. Deposition conditions during the fabrication of CTM device.

High-k material	**Substrate Temperature(^{o}C)**	**Deposition time(s)**		**Pressure (Pa)**
HfO_2	250	240		6.6×10^{-4}
Dy_2O_3	100	100		7.3×10^{-4}
Al_2O_3	250	150		6.8×10^{-4}

3.3 Crystalline structure and surface roughness characterization

Over the last decades, several methods have been developed for the characterization of various materials. To study the crystalline structures and surface roughness of the CTM cells, we used XRD and AFM techniques.

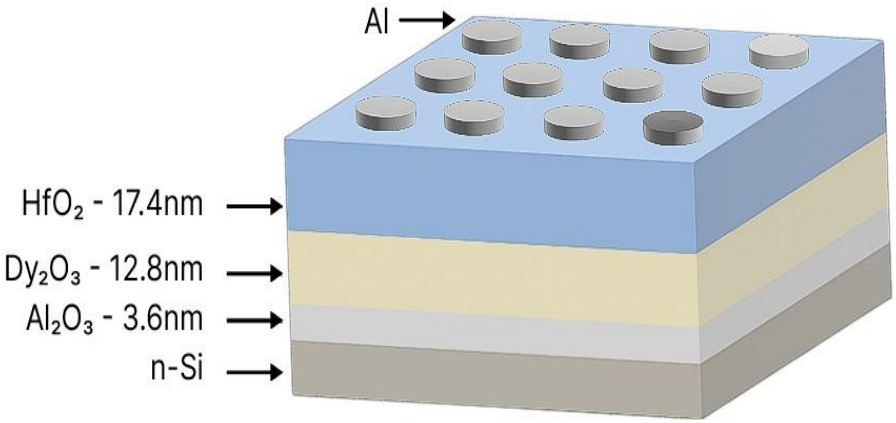


Figure 3.12. The cross section of fabricated Al/HfO2/Dy2O3/Al2O3/n-Si(100) CTM device.

3.3.1 X-ray diffraction (XRD)

The XRD analysis was carried out to analyse and study the crystalline structure of $HfO_2/Dy_2O_3/Al_2O_3$/n-Si (100). The angle was arranged between 2θ =10^o and 80^o with a step angle of 5.0^o. The XRD technique which was used during the course of this study in Picture 3.7. This system is located in the Department of Physics at Bolu Abant Izzet Baysal University.

PICTURE 7. Rigaku MultiFlex X-Ray Diffractometer in the Department of Physics at Bolu Abant Izzet Baysal University.

3.3.2 Atomic force microscopy (AFM)

The surface roughness of the CTM cells was investigated by AFM technique for the as-deposited and 700^{o}C and 900^{o}C annealed samples by scanning the thin films in the dimension s of 3μm×3μm. The AFM technique which was also used during the course of this study in Picture 3.8. The AFM technique is situated at Central Laboratory in Middle East Technique University (METU), Ankara.

PICTURE 8. Atomic force microscopy (AFM) technique at Central Laboratory in Middle East Technical University (METU).

4. RESULTS

4.1 Crystalline structure, surface roughness and electrical properties studies

In this section we have presented the results that were obtained during the experiment of this investigation. Our experimental findings have been contrasted with findings from previous investigations.

4.4.1 X-ray diffraction (XRD) studies

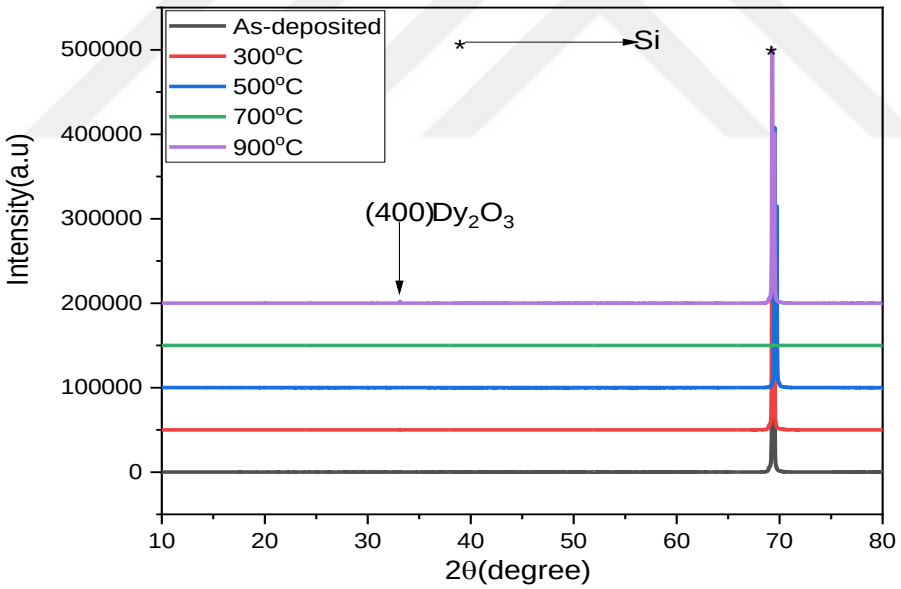
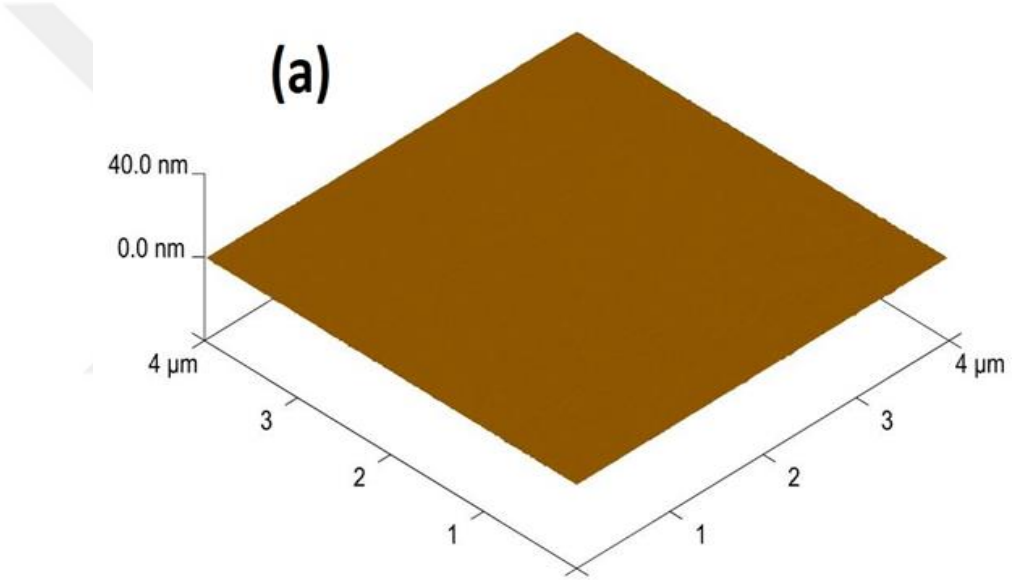


Figure 4.1. XRD spectras of $HfO_2/Dy_2O_3/Al_2O_3$/n-Si(100) for as-deposited and annealed samples at 300°C, 500°C, 700°C, and 900°C in N_2 ambient for 40min.

Figure 4.1, shows the XRD patterns of $HfO_2/Dy_2O_3/Al_2O_3$/n-Si (100) as-deposited and annealed samples thin films at 300°C, 500°C, 700°C, and 900°C in N_2 ambient for 40min. The XRD patterns for the as-deposited and annealed samples at 300°C, 500°C, 700°C show that no peaks were present. In other words,

the thin films turned into amorphous. However, when the post deposition annealing temperature increased up to 900^{o}C, only one peak was present in the XRD pattern. This peak belongs to Dy_2O_3 thin film with a preffered oreintation of (400) and indexed number (86-1327) according to International Centre for Diffraction Data (ICDD).

4.4.2 Atomic force microscopy (AFM) studies



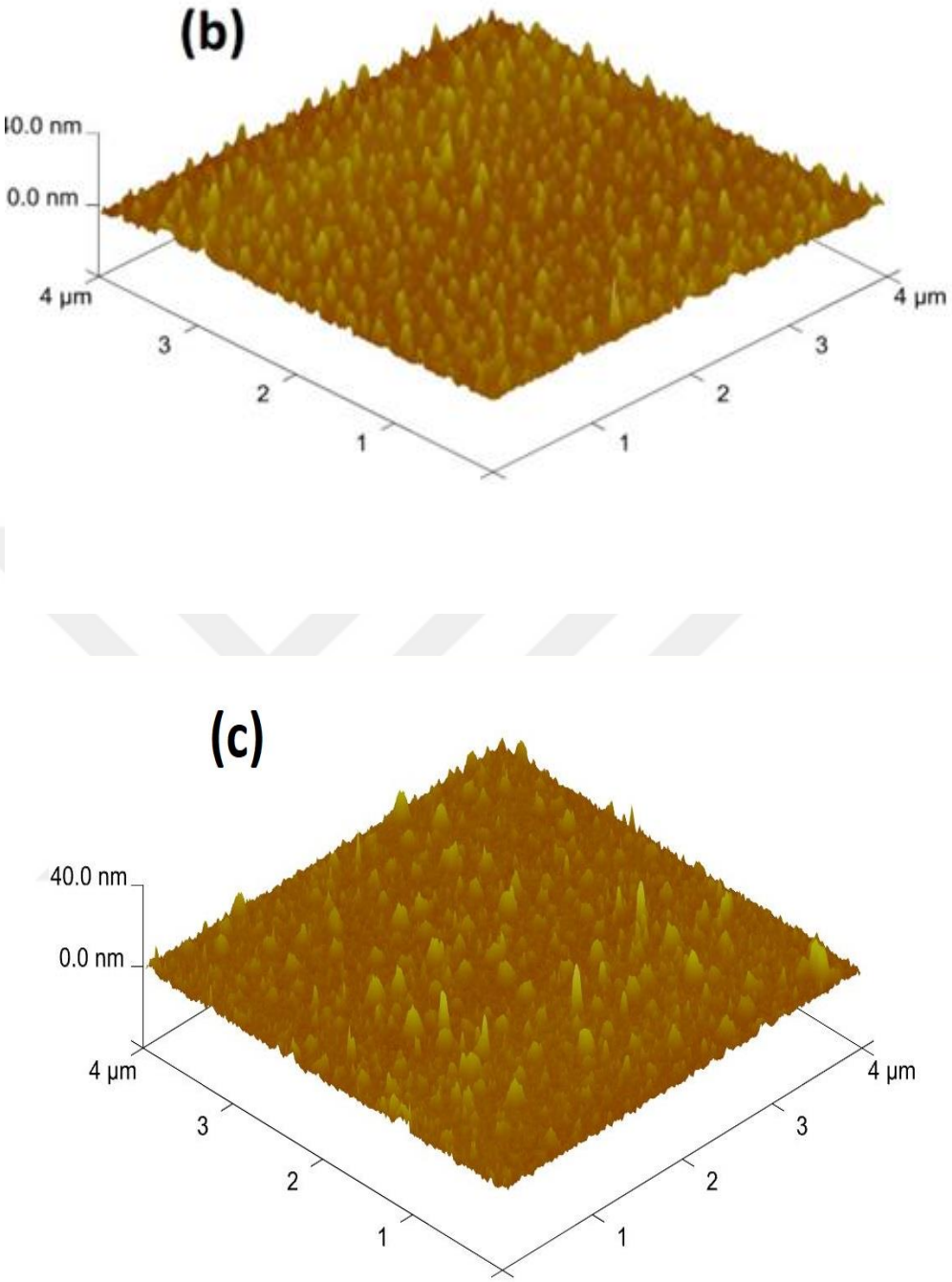


Figure 4.2. AFM surface roughness of $HfO_2/Dy_2O_3/Al_2O_3$/n-Si(100) for (a)as-deposited and annealed samples at (b) 700^{o}C and (c) 900^{o}C in N2 ambient for 40min.

The surface roughness of the CTM cells was investigated by AFM technique for the as-deposited and 700^{o}C and 900^{o}C annealed samples by scanning the thin films in the dimension s of 4μm×4μm as shown in Figure 4.2. The root mean square(rms) of the three samples were 0.192nm, 2.50nm and 2.06nm, respectively. It is observed that the as-deposited has RMS value of 0.19nm and this value is comparable to the RMS value (0.17nm) for NiO_2(142) However, when the annealing increased up to 900^{o}C, we found the RMS value (2.06nm). This value is lower than the RMS value of (3.79nm) for Gd_2O_3 thin films and the sample was treated in RTA at 900^{o}C in N_2 for 30s(143).

4.3.3 Electrical characterization studies

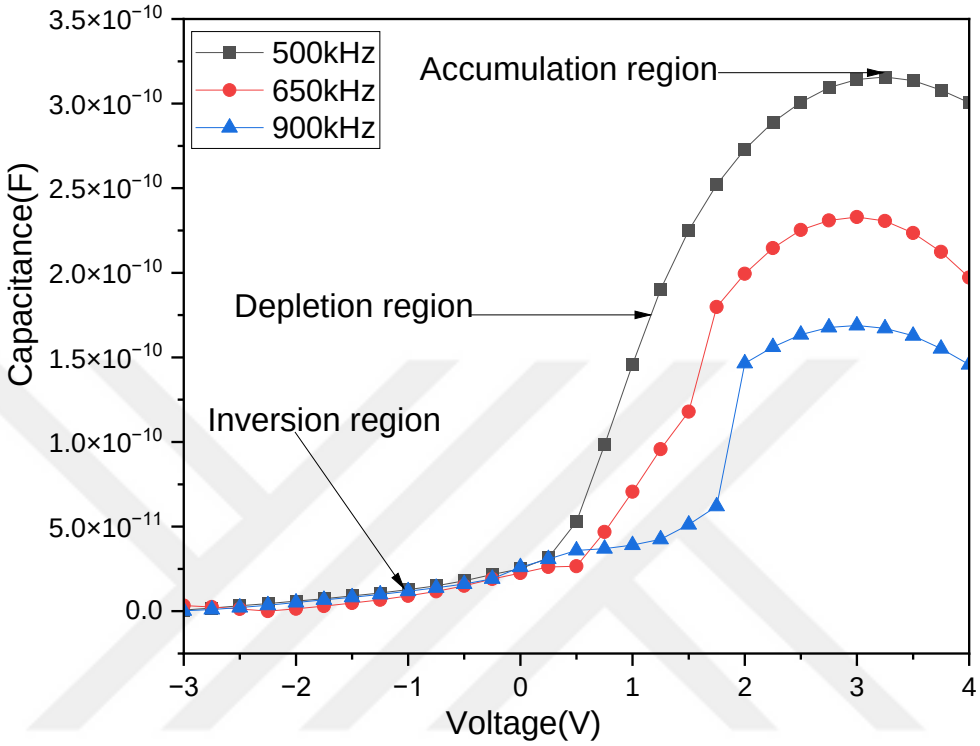


Figure 4.3. The C-V curves of Al/HfO_2/Dy_2O_3/Al_2O_3/n-Si(100)/Al CTM device measured at various frequncies of 500kHz-900kHz.

As shown in Figure 4.3, the C-V curves were measured at various frequencies ranging from 500 kHz to 900 kHz as part of our investigation into the impact of frequency on CTM cells. As the applied voltage frequency increased, it was found that the capacitance in the accumulation zone dropped. On the other hand, as the applied frequency rises, the C-V curves migrated towards the negative sides. Through C-V curves, the interface states were also investigated and analysed. The Hill-Cole man method (144,145) was used to obtain the interface states density (Dit). At frequencies of 500 kHz, 650 kHz, and 900 kHz, respectively, the calculated Dit values are 6.22x10^9 eV^{-1} cm^{-2}, 6.82x10^9 eV^{-1} cm^{-2}, and 2.12x10^9 eV^{-1} cm^{-2}. Figure 4.4 also shows the Dit values as a function of frequency.

$$D_{it} = \frac{2}{qA} \frac{(G_m/\omega)max}{\left(((G_m/\omega)max)C_{ox}\right)^2 + \left(1 - {}^{C_c}/_{C_{ox}}\right)^2} \quad (4.1)$$

Where q is the electronic charge and the gate electrode of a CTM device, G_m, $_{max/}\omega$ is the maximum corrected conductance corresponding to the peak,ω is the angular frequency equal to 2πf, C_{ox} =C_{acc} is the oxide capacitance in the accmulation region, and C_c is the corrected capacitance value.

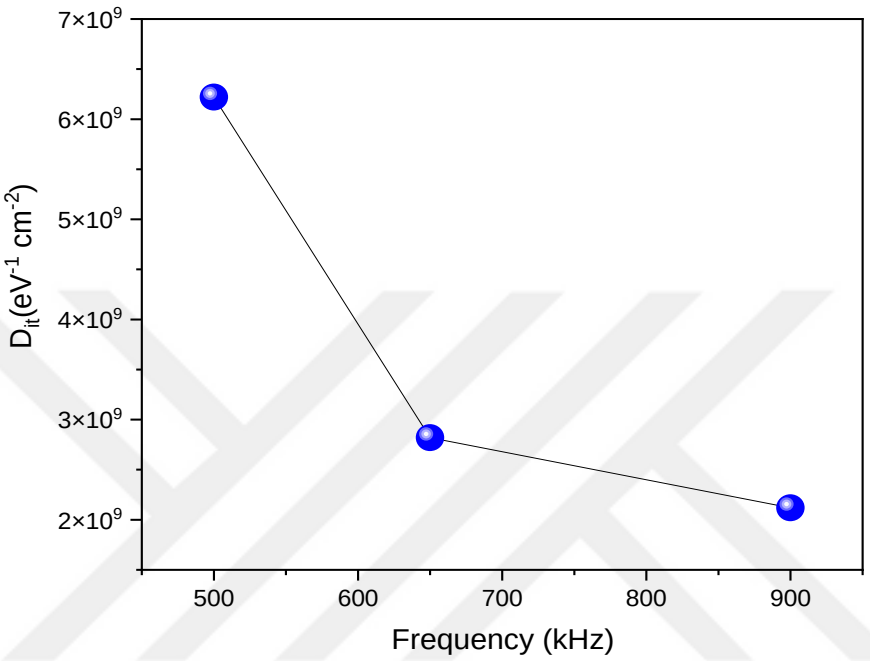


Figure 4.4. Interface states density of Al/HfO_2/Dy_2O_3/Al_2O_3/n-Si(100)/Al CTM device as a function of different frequncy of 500kHz-900kHz.

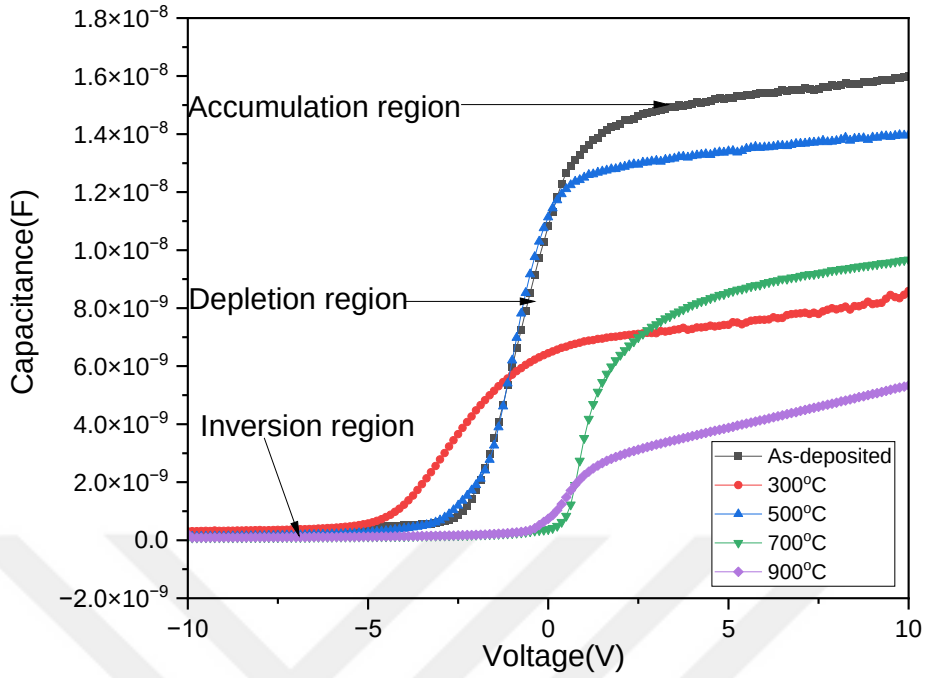


Figure 4.5. The capacitance-voltage(C-V) curves of Al/HfO_2/Dy_2O_3/Al_2O_3/n-Si (100)/Al CTM devices for as-deposited and annealed device at 300°C, 500°C,700°C, and 900°C in N_2 ambient for 40min and measured at 1MHz.

Figure 4.5 shows the capacitance-voltage (C-V) curves of Al/HfO_2/Dy_2O_3/Al_2O_3/n-Si (100) of as-deposited and annealed device at 300°C 500°C 700°C, and 900°C and measured at 1MHz. The C-V curves show that the capacitance decreased as the annealing temperature increased. Other researchers, also found the similar results. For instance, et al Zhang *et al*; found the capacitance to decrease with increasing annealing temperature(146). Mutale *et al;* also investigated the effect of PDA on charge trapping memory devices. They discovered that as the PDA increased, the accumulation's capacitance value reduced (145).

Table 2. The obtained electrical parameters from C-V curves of $Al/HfO_2/Dy_2O_3/Al_2O_3$/n-Si (100)/Al CTM devices for as-deposited and annealed devices at 300°C, 500°C, 700°C, and 900°C in N_2 ambient for 40min.

Temperature(°C)	V_{fb}(V)	Q_{eff}(cm^{-2})×10^{12}	D_{it}(eV^{-1} cm^{-2})
As-deposited	0.07	-1.90	3.34×10^{13}
300	-1.58	3.62	6.76×10^{12}
500	0.22	-2.41	2.33×10^{13}
700	1.77	-6.89	1.42×10^{13}
900	0.71	-1.16	2.86×10^{12}

The effective oxide charges(Q_{eff}) were calculated from the following equation(147,148).

$$Q_{eff} = \frac{C_{ox}(W_{ms} - V_{fb})}{qA} \qquad (4.2)$$

Where is the W_{ms}(-0.27V) work function difference between the metal and semiconductor, V_{fb} is the shift in the flat band voltage other parameters, however, have been specified in Eq. (1). The calculated Q_{eff} of as-deposited and annealed devices at 300°C 500°C, 700°C and 900°C are -1.90×10^{12} cm^{-2}, 3.62×10^{12} cm^{-2}, -2.41×10^{12} cm^{-2}, $-6.89\times10^{12}cm^{-2}$, and -1.16×10^{12} cm^{-2}, respectively. The Q_{eff} have been also Tabulated in Table 4.1 and plotted in Figure 4.6. For as-deposited sample (-1.90×10^{12} cm^{-2}) can be compared to the as-deposited sample (1.01×10^{12} $cm^{-2)}$ of MOS capacitors with TiO_2 and HfO_2 (149).The Q_{eff}(-1.16×10^{12} cm^{-2}) of 900°C can be also compared to the Q_{eff}(-1.03×10^{12} cm^{-2}) of device annealed at 400°C(150). Moreover, Gao *et al*; investigated the effect of annealing temperature MOS devices with HfO_2 and Q_{eff} value is -6.54×10^{11} cm^{-2} and annealed at 300°C(151).

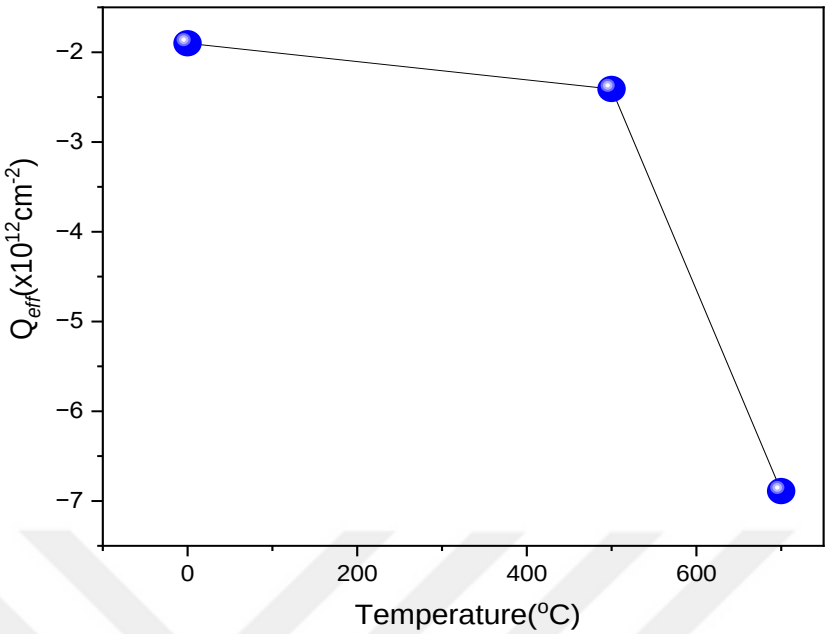


Figure 4.6. Effective oxide charges as a function of annealing temperature of as-deposited and annealed device at 500°C and 700°C.

We investigated how annealing temperature affected interface states D_{it}. The D_{it} values were obtained using Eq.1. For as-deposited and annealed devices at 300°C 500°C, 700°C and 900°C 3.34×10^{13} eV^{-1} cm^{-2} 6.76×10^{12} eV^{-1} cm^{-2}, 2. 33×10^{13} eV^{-1} cm^{-2} , 1.42×10^{13} eV^{-1} cm^{-2} 2.86×10^{12} eV^{-1} cm^{-2}, respectively. The lowest D_{it} value(2.86×10^{12} eV^{-1} cm^{-2}) of 900°C and is compared to the value(1.26×10^{12} eV^{-1} cm^{-2}) of Dy_2O_3 thin film(152). Zang *et al;* reported the D_{it} value ($2.26\times10^{12}eV^{-1}$ cm^{-2}) of MOS capacitor with TiO_2 with HfO_2 and annealed at 800°C(146). Matocha *et al;* found D_{it} value on the order of 10^{12} eV^{-1} cm^{-2} for GAN based device(153). In additonal Gao *et al;*also found D_{it} value($2.83\times10^{12}eV^{-1}$ cm^{-2}) for the device annealed 500°C(151).

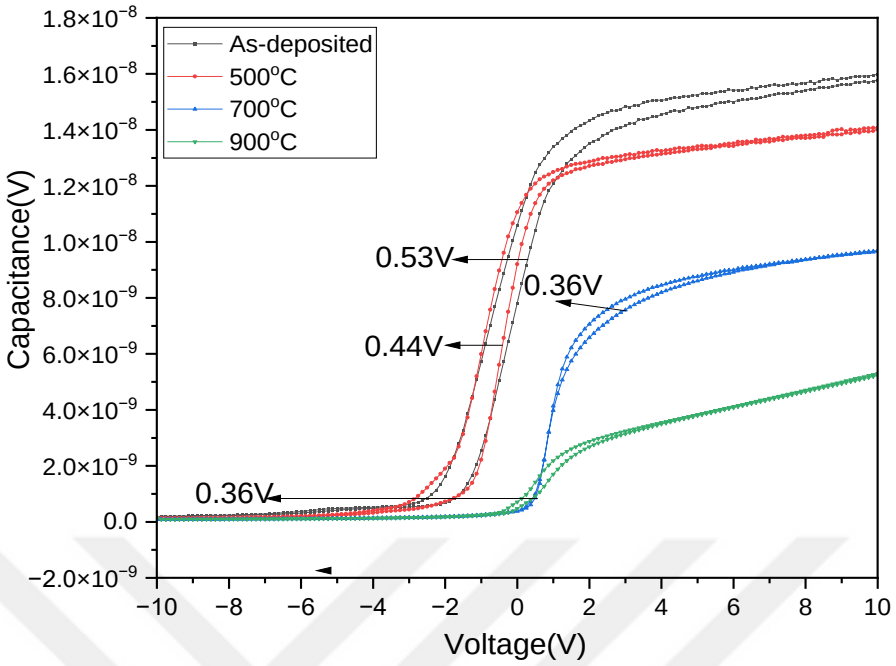


Figure 4.7. The capacitance-voltage (C-V) curves hysterisis curves of Al/HfO_2/Dy_2O_3/Al_2O_3/n-Si(100)/Al for as-deposited and annealed devices at 500°C, 700°C, and 900°C in N_2 ambient and measured at 1MHz.

Figure 4.7, shows the hysteresis C-V curves of as-deposited and annealed devices at 300°C, 500°C, 700°C, and 900°C. The obtained memory window are 0.53V, 0.44V, 0.36V, and 0.36V. It is observed that the memory window decreased with an increase in the annealing temperature. The larger (0.44V) memory window for the device annealed at 500°C. Zhu also found the memory window to increase with an increase in the PDA and then decreased and the reported memory window are 3.92V, 8.48V and 0.24V of 700°C,800°C, 900°C. While Yan *et al* observed the memory window increased as the annealing temperature increased and then suddenly decreased. The reported memory are 1.75V, 2.07V and 1.63V corresponding to 700°C, 750°C, and 800°C(154).The interface trap charge densities (N_{it})were calculated from the following Equation(147).

$$N_t = \frac{C_{ox}\Delta V_{fb,hystersis}}{qA} \qquad (4.\ 3)$$

Where $\Delta V_{fb}, hystersis$ is voltage, while additional parameters are defined in Eq. (1). The obtained interface trap charge densities of as-deposited and annealed device at 500°C, 700°C, and 900°C are 2.96×10^{12} cm^{-2}, $2.16\times10^{12}cm^{-2}$, $1.22\times10^{12}cm^{-2}$ and 4.25×10^{11} cm^{-2} corresponding to memory window of 0.53V, 0.44V, 0.36V, and 0.36V, respectively. The N_{it} value has been Tabulated in Table 4.2 and plotted in Figure 4.8. For as-deposited (2.96×10^{12} cm^{-2}) is compared to the

N_{it} value (2.05×10^{11} cm^{-2}) of MOS capacitors with HfO_2(151). The lowest N_{it} (4.25×10^{11} cm^{-2}) of 900°C is the in line with a N_{it}(2.74×10^{11} $cm^{-2)}$ of HfO_2 thin fims and then device was annealed at 800°C(155) Zang et al; reported the N_{it} value($7.5\times10^{12}cm^{-2}$) of CTM devices with HfO_2 and SiO_2 thin films(156). Furthermore, Kim et al; also reported the N_{it} value of ($2.0\times10^{12}cm^{-2}$) with a ΔV_{fb} 3.8V for CMT devicees with SiO_2 deposited into Germanium (Ge) and thereafter annealed at 700°C(157).

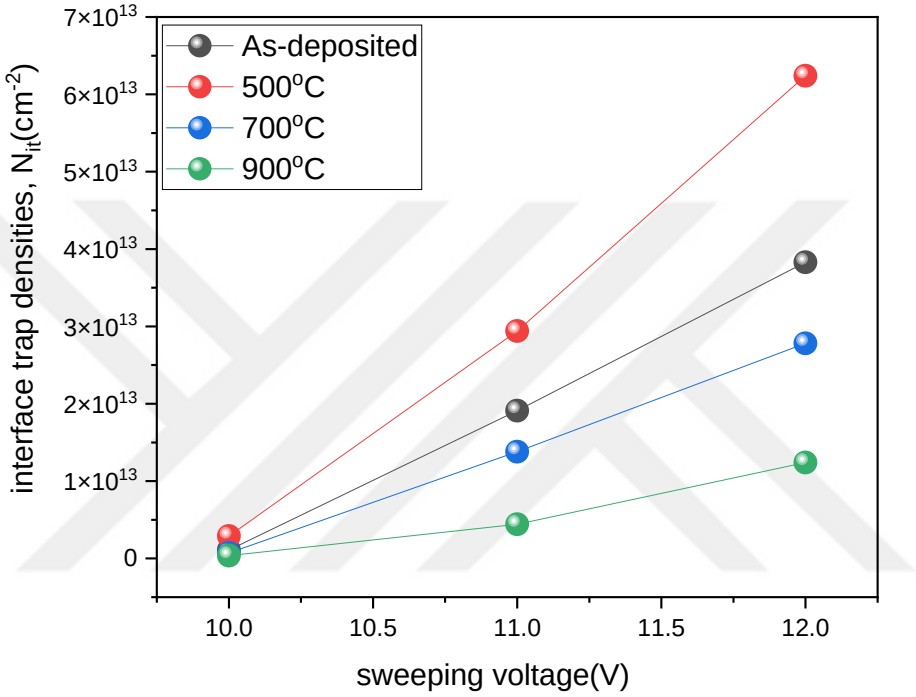


Figure 4.8. Interface trap densities (N_{it}) as a function of sweeping voltage for as-deposited sample and annealed at 500°C, 700°C, and 900°C.

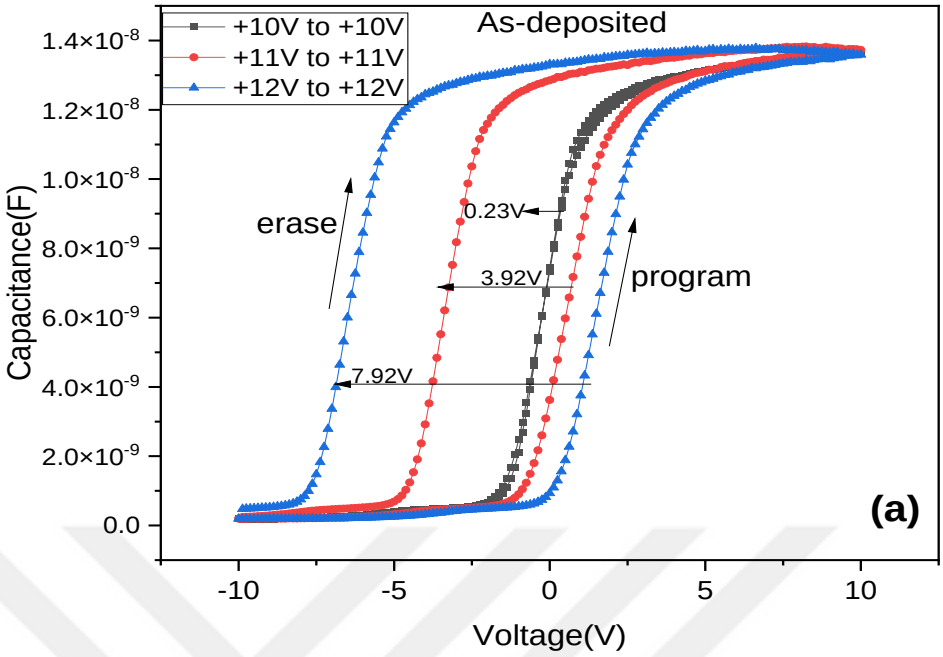


Figure4.9. The capacitance-voltage (C-V) curves hysterisis curves of Al/HfO_2/Dy_2O_3/Al_2O_3/n-Si(100)/Al CTM device for as-deposited sample at different applied gate voltage of ±10V and ±12V and measured at 1MHz.

The C-V curves of as-deposited sample at different applied hysteresis gate voltage is given in Figure 4.9. It has been demonstrated that the capacitance in the accumulation region and the memory windows increased as the applied voltage was raised. The obtained memory windows for as-deposited sample are 0.23V, 3.92V and 7.92V corresponding to ±10V, ±11V and ±12V.

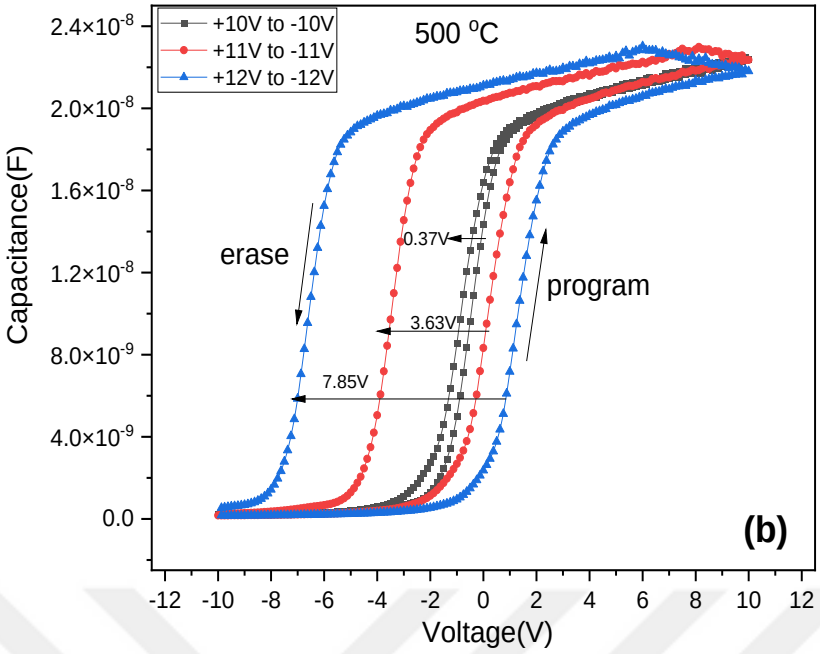


Figure 4.10. The capacitance-voltage (C-V) curves hysterisis curves of $Al/HfO_2/Dy_2O_3/Al_2O_3/n\text{-}Si$ (100)/Al CTM device annealed at 500°C in N2 ambient for 40min at different applied gate voltage of ±10V and ±12V and measured at 1MHz.

Figure 4.10, also shows the C-V curves for the device annealed at 500°C. We also found that the memory window increased with applied gate voltage. The achieved memory windows of this device are 0.37V, 3.63V and 7.85 corresponding to ±10V, ±11V and ±12V. The obtained memory window for various applied gate voltage as a function of the applied gate voltages from ±10V to ±12V

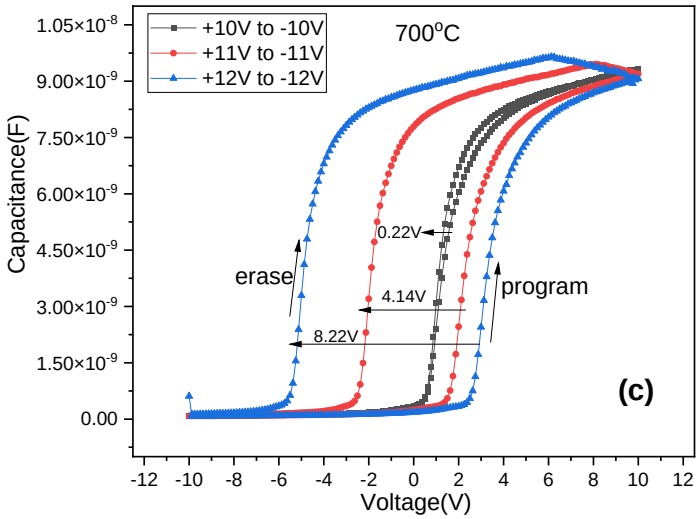


Figure 4.11. The capacitance-voltage (C-V) curves hysterisis curves of $Al/HfO_2/Dy_2O_3/Al_2O_3/n\text{-}Si(100)/Al$ CTM device annealed at 700°C in N_2 ambient for 40min at different applied gate voltage of ±10V and ±12V measured at 1MHz.

The C-V curves of hysteresis have been given in Figure 4.11, for the device annealed at 700°C. The applied hysteresis gate voltage for this device is similar to the as-deposited and device which was annealed at 500°C and 900°C. The calculated memory windows of applied hysteresis voltage ±10V, ±11V and ±12V are 0.22V, 4.14V and 8.22V, respectively. Our results are comparable to the results reported by several researchers. For instance, Zhu et al; fabricated CTM device with TiO_2 and ZrO_2 as the charge trapping. The hysterisis window was arranged between ±4V and ±12V. They found the memory window 2.5V, 5.2V, 8.5V, 11.9V, and 15.5V. Tang et al also fabicated CTM cell with a structure p-$Si/SiO_2/ZrO_2/Al_2O_3$. They found the memory window of 2.4V, 6.8V and 2.4V and the device was also annealed at 800°C.

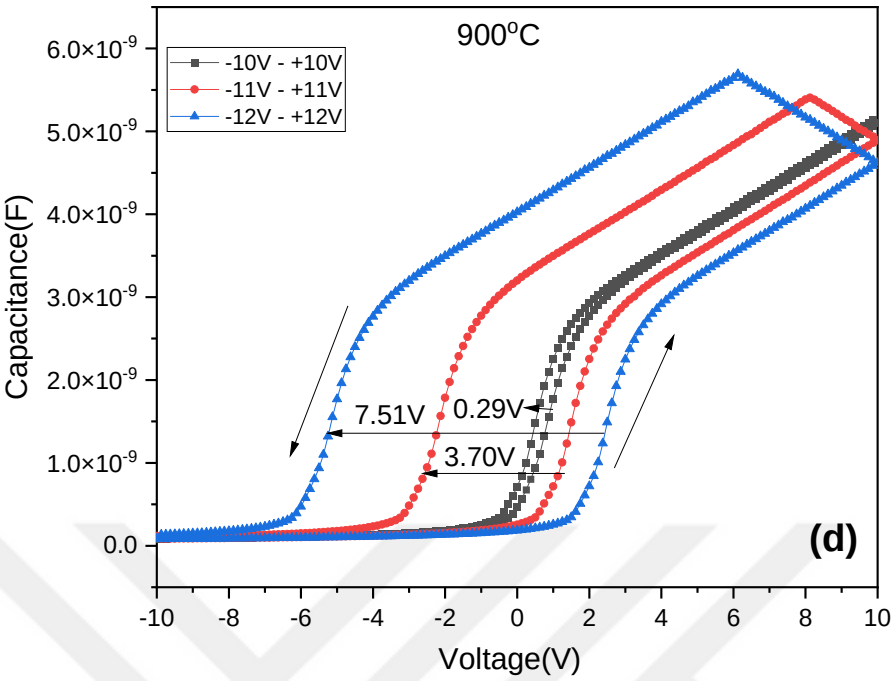


Figure 4.12. The capacitance-voltage (C-V) hysterisis curves of $Al/HfO_2/Dy_2O_3/Al_2O_3/n\text{-}Si$ (100)/Al CTM device annealed at 900°C in N_2 ambient for 40min at different applied gate voltage of ±10V and ±12V and measured at 1MHz.

The C-V hysterisis curves of CTM device at diffferent sweeping voltage of ±10V and ±12V measured at 1MHz. The obtained memory window are 0.29V, 3.70V and 7.51V correspoding to ±10V, ±11V, and ±12V. The memory window is shown to increase as the applied sweeping gate voltage rises.

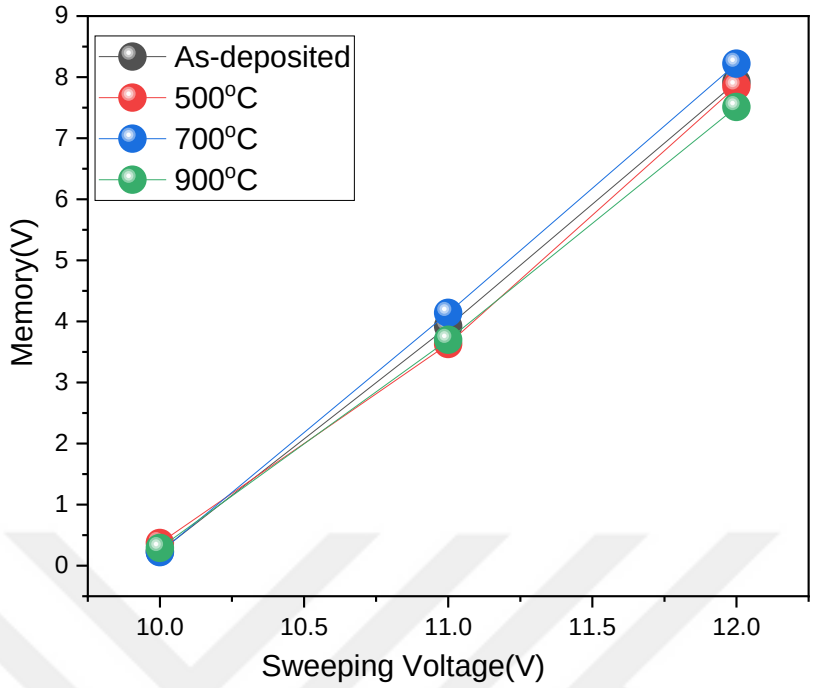


Figure 4.13. Memory window as a function of sweeping voltages of ±10V to ±12V.

Table 3. The obtained electrical parameters of Al/HfO_2/Dy_2O_3/Al_2O_3/n-Si (100) /Al CTM devices for as-deposited and annealed devices at 500°C, 700°C and 900°C for various sweeping voltage of ±10V to ±12V.

Temperature(°C)	Sweeping voltage(V)	Memory window(ΔV_{fb})	N_{it}(cm^{-2})
As-deposited			
	±10	0.23V	1.10×10^{12}
	±11	3.92V	1.91×10^{13}
	±12	7.92V	3.83×10^{13}
500	±10	0.37V	2.90×10^{12}
	±11	3.63V	2.94×10^{13}
	±12	7.85V	6.24×10^{13}
700			
	±10	0.22V	7.11×10^{11}
	±11	4.14V	1.38×10^{13}
	±12	8.22V	2.78×10^{13}
900			
	±10	0.29V	3.68×10^{11}
	±11	3.70V	4.42×10^{12}
	±12	7.51V	1.24×10^{13}

4.4.4 Radiation response on CTM device

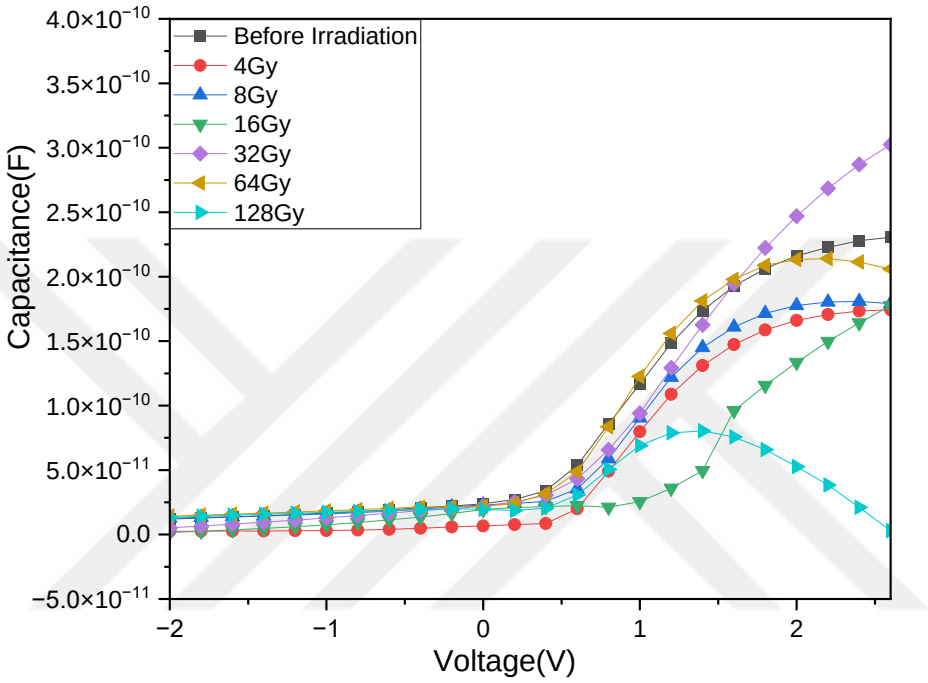


Figure 4.14. The C-V curves of Al/HfO_2/Dy_2O_3/Al_2O_3/n-Si(100) CTM device irradiated at doses in the range of 4Gy to 128Gy.

Figure 4.14. shows, the C-V curves of Al/HfO_2/Dy_2O_3/Al_2O_3/n-Si(100) CTM device irradiated by using Cs-137 gamma rays radiation source at Turkish Atomic Energy Authority(TAEK), Ankara, Turkey. There is no significant change in the value of capacitance in the accumulation region between 4Gy and 16Gy. On the other hand, when the device was exposed to 32Gy, the capacitance value in the accumulation region increased significantly as compared to 64Gy and 128Gy. As may be noted from the same figure the C-V curves shifted toward the positive voltage side at 4Gy, 8Gy, 16Gy, 32Gy, and 128Gy as compared to 64Gy.

The shift in the mid-gap voltage(ΔV_{mg}) was observed due to the oxide trapped charges(ΔN_{ot}) generated by Cs-137 irradiation. Therefore, the value of ΔN_{ot} was obtained by using the following expression(158,159).

$$\Delta N_{ot} = -\frac{C_{ox}\Delta V_{mg}}{qA} \quad (4.4)$$

Where ΔV_{mg} is the shift in the midgap voltage prior to and after irradiation, while other parameters have been stated above. The obtained value of ΔN_{ot} are -9.49×10^{09} cm$^{-2,}$ -2.65×10^{10}cm^{-2}, -4.73×10^{10}cm^{-2}, 5.65×10^{10} cm$^{-2,}$ 2.93×10^{10} cm^{-2}, and -2.29×10^{11} cm^{-2} at 4Gy, 8Gy, 16Gy, 32Gy, 64Gy, and 128Gy, respectively. The values of ΔV_{mg} and ΔN_{ot} have also been tabulated in Table. The lowest negative ΔN_{ot} value (-9.49×10^{09} cm^{-2}) was found at 4Gy and can be compared to the ΔN_{ot} (-2.26×10^{11} cm^{-2}) reported by Kahraman *et al*(160). Other researchers have also found the the ΔNot value of -3×10^{12} cm^{-2} at 10kGy(159). On the other hand, we found positive ΔN_{ot} of 2.93×10^{10} cm^{-2} at 64Gy and this value is less than or well compared to the ΔN_{ot} (2.5×10^{12} cm^{-2}) at 10kGy of CTM device with HfO_2 and Al_2O_3(159,160). Kahraman *et al;* also reported the ΔN_{ot} in the range of 6.67×10^{10} cm^{-2} to 1.10×10^{12} cm^{-2}(158). Mang Ding reported the ΔN_{ot} in the range of 4.87×10^{11}cm^{-2} to 1.82×10^{12} cm^{-2} at different doses between 1.2Mrad and 4Mrad(161). Moreover, J. A Felix *et al*; found the ΔN_{ot} value between 2.98×10^{11} cm^{-2} and 2.65×10^{12} cm^{-2} of Al_2O_3/SiO_xN_y at 10Mrad (SiO_2)(162).

In addition, Cs-137 radiation also induces the interface trapped charges(ΔN_{it}) at the oxide/semiconductor interface. Hence, the shift in the flat band voltage(ΔV_{fb}) was observed on the C-V curves and the values of ΔV_{fb} are given in Table. So, the values of ΔN_{it} were calculated as follows(160,163).

$$\Delta N_{it} = -\frac{C_{ox}(\Delta V_{fb} - \Delta V_{mg})}{qA} \quad (4.5)$$

Where ΔV_{fb} is the shift in the flat band voltage before and after irradation, while other parameters have also been stated before. The obtained value of ΔN_{it} are 2.76×10^{10} cm^{-2}, -5.13×10^{10} cm^{-2}, -4.84×10^{10} cm^{-2}, 7.37×10^{10}cm^{-2}, and 3.51×10^{10} cm^{-2} at 4Gy, 8Gy,16Gy, 32Gy, 64Gy, and 128Gy, respectively. The value ΔN_{it}(3.51×1010 cm^{-2}) is found at 128Gy and is well compared with the value ΔN_{it}(6.20×10^{10} cm^{-2}) reported by Yilmaz *et al* at 8.0Gy(163). Kahraman *et al*; found the ΔN_{it} value of(7.11×10^{10} cm^{-2}) at 32Gy(158). Mang Ding also found the ΔN_{it} in the range 1.86×10^{12} cm^{-2} to 4.43×10^{12} cm^{-2} at various doses between 1.2Mrad and 4Mrad. N. Manikanthababu *et al*; found the ΔN_{it} value in the range

of 1.28×10^{11} cm^{-2} to 1.74×10^{11} cm^{-2} of HfO_2 based MOS device at different doses between 25Gy and 100Gy(164).

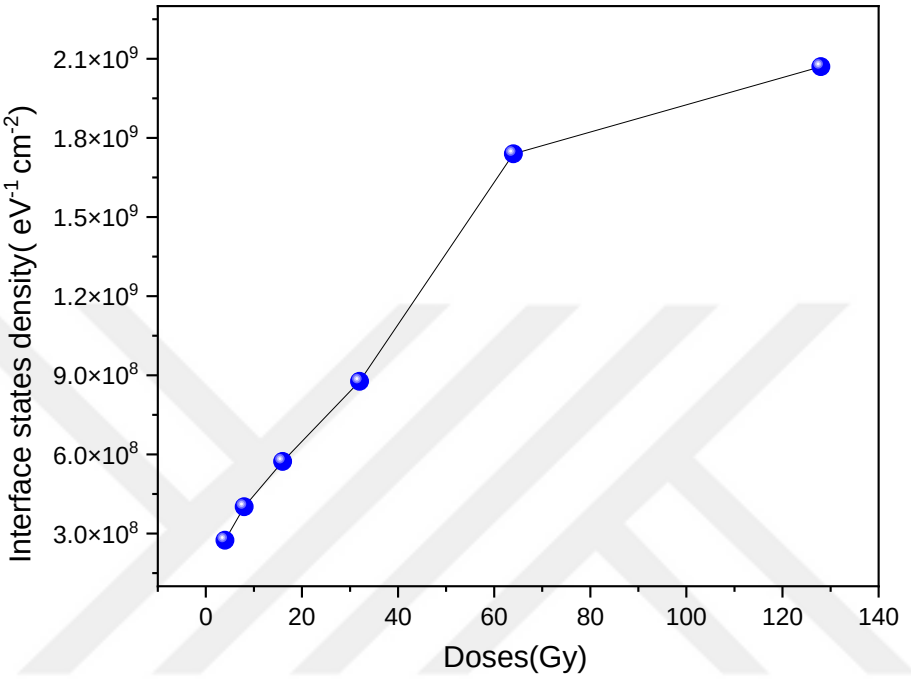


Figure 4.15. Interface states denisty as a function of doses for CTM device.

The interface states density (D_{it}) is one most important parameter also to investigate. The value of D_{it} was obtained by using Eq (1), above. The determined value of D_{it} are 2.74×10^{08} eV^{-1} cm^{-2}, 4.01×10^{08} eV^{-1} cm^{-2}, 5.73×10^{08} eV^{-1} cm^{-2}, 8.77×10^{08} eV^{-1} cm^{-2} 1.74×10^{09} eV^{-1} cm^{-2}, and 2.07×10^{09} eV^{-1} cm^{-2} at 4Gy, 8Gy, 16Gy, 32Gy, 64Gy, and 128Gy, respectively. We found the Dit value to increase with radiation dose. The lowest D_{it} value was found to be 2.74×10^{08} eV^{-1} cm^{-2} at 4Gy and this value is less than or line with the D_{it} value of 3.03×10^{11} eV^{-1} cm^{-2} at neutron fluence is 1.5×10^{13} n cm^{-3} (165). Spassov *et al*; found the D_{it} value in the range of 1.1×10^{12} eV^{-1} cm^{-2} and 6.4×10^{12} eV^{-1} cm^{-2} at different doses of 10kGy to 100kGy(159) Other researchers have reported the D_{it} value of 8.61×10^{09} eV^{-1} cm^{-2} for MIS schottky diodes at 50Gy(166).

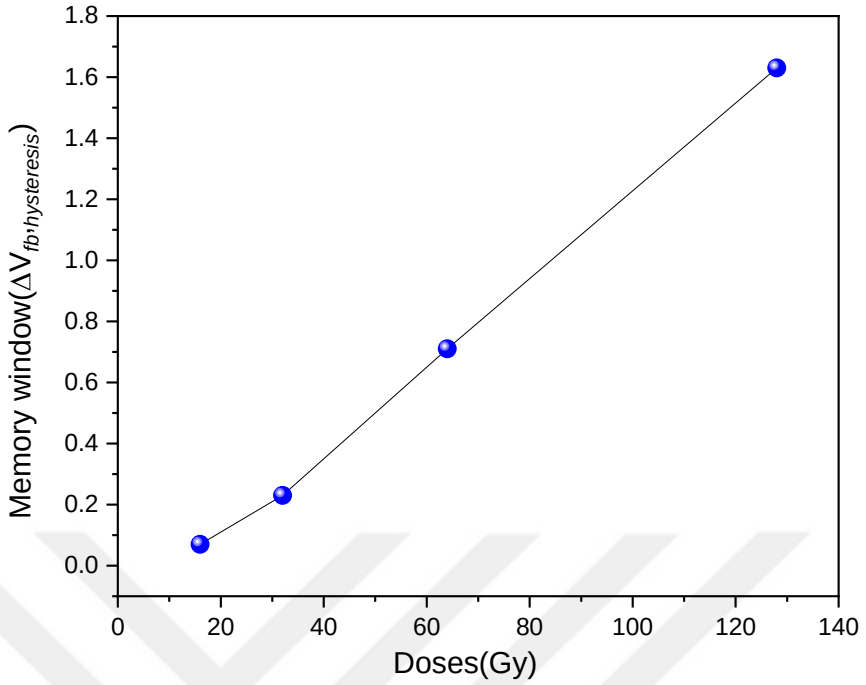


Figure 4.16. Memory window as a function radiation dose.

Finally, we studied also the effect radiation on memory window ($\Delta V_{fb,\ hysteresis}$) at various doses. The obtained memory window are 0.18V, 0.50V, 0.07V, 0.23V, 0.71V, 1.71V, and 1.63V corresponding to 4Gy, 8Gy, 16Gy, 32Gy, 64Gy, and 128Gy, respectively. The values of memory have also plotted in Figure and tabulated in Table

Table 4. the obtained electrical parameters of CTM device at different doses.

Doses (Gy)	**ΔV_{mg}(V)**	**ΔV_{fb}(V)**	**ΔV_{fb}, *hysteresis*(V)**
Before irradiation	0.36	1.75	0.48
4	0.16	-0.25	0.18
8	0.46	-0.02	0.50
16	0.59	1.23	0.07
32	-0.63	-0.09	0.23
64	-0.39	-1.37	0.71
128	2.34	1.10	1.63

Table 5. the obtained electrical parameters of CTM device at different doses.

Doses (Gy)	**$\Delta N_{ot}(cm^{-2})$**	**$\Delta N_{it}(cm^{-2)}$**	**D_{it} (eV^{-1} cm^{-2})**
Before irradiation	-2.92×10^{10}	1.13×10^{11}	4.78×10^{08}
4	-9.49×10^{09}	2.43×10^{10}	2.74×10^{08}
8	-2.65×10^{10}	2.76×10^{10}	4.01×10^{08}
16	-4.73×10^{10}	-5.13×10^{10}	5.73×10^{08}
32	5.65×10^{10}	-4.84×10^{10}	8.77×10^{08}
64	2.93×10^{10}	7.37×10^{10}	1.74×10^{09}
128	-2.29×10^{11}	3.51×10^{10}	2.07×10^{09}

5.DISCUSSION

Figure 4.1, shows XRD spectra of $HfO_2/Dy_2O_3/Al_2O_3$/n-Si (100) thin films for as-deposited and annealed samples at 300^{o}C, 500^{o}C, 700^{o}C and 900^{o}C. In the XRD spectra for the as-deposited and annealed samples at 300^{o}C, 500^{o}C, and 700^{o}C no peaks were present belonging to any of the deposited materials. In other words, we found that below the annealing temperature of 900^{o}C the thin films turned into amorphous. Other researchers found that the sample annealed at 600Oc no diffraction peak was present in the XRD patterns for doped Al-ZrO2(AZO) thin films deposited by sol-Gel method(167). Gurer et al; investigated the effect of gamma irradiation on Dy_2O_3 . For the unirradiated sample, they found that in the XRD patterns,one peak was present $\sim 2\theta$=29.56^o corresponding to peak intensity (222)(168) Pan and Yu, also observed similar results when they investigated the effect of annealing temperature on Pr_2O_3 thin films. They found that as-deposited sample and annealed samples at 700^{o}C and 800^{o}C no peaks were present in the XRD patterns(169). However, in this study, there was only one weak peak present in the XRD spectra when the annealing temperature increased up to 900^{o}C. This peak belongs to Dy_2O_3 thin film and corresponds to preferred orientation of (400) and indexed card number (86-1327) the International Centre for Diffraction Data (ICDD). Similar results were reported by C.H Kao et *al.* They found that when the annealing temperature increased to 900^{o}C, the peaks became the strongest for Gd_2O_3 thin films(170). Moreover, Pan and Yu, studied the impact of annealing temperature on Pr_2O_3 thin films. They found that when the annealing temperature increased up to 900^{o}C, the Pr_2O_3 thin films had one weak peak. They suggested that the formation of interficial layer is very possible at higher annealing temperatures(59).

Figure 4.2, shows the surface roughness of $Al_2O_3/Dy_2O_3/Al_2O_3$/n-Si(100) thin films for the as-deposited and 700^{o}C and 900^{o}C annealed samples. The root mean squared (RMS) of the three samples was 0.192nm, 2.50nm and 2.06nm, respectively. As shown in Figure 4.2, the surface roughness decreased as the annealing temperature increased to 900^{o}C. The main reason behind this is attributed to the formation of a well-crystallized Dy_2O_3 which is in line with the

XRD results and other researchers have observed similar results(171–173). However, the increase in the surface roughness for the sample annealed at 700^{o}C can allude to the larger grain size due to the enhancement of Dy_2O_3 crystallization under the high temperature annealing conditions as reported by previous studies(143,167).

The C-V curves of $Al/HfO_2/Dy_2O_3/Al_2O_3$/n-Si (100) CTM device measured at various frequencies of 500kHz- 900kHz has been given in Figure 4.3. It is observed that the value of capacitance in the accumulation region decreased with an increase in the applied voltage frequency. It has been reported that this could be attributed to the interface states density. These charges can be able to follow the ac signal when the C-V measurement has been performed at low frequencies. For this reason, they can contribute to the capacitance value in the accumulation regime (174–177). On the other hand, the trap charges hardly to follow ac signal when the C-V measurements have been performed at high frequency. As a result, the contribution of the capacitance value in the accumulation region is negligibly due to their larger carrier life (174,175,178). As discussed above Figure 4.4 shows also the plotted interface states as a function of frequency.

The C-V curves of $Al/HfO_2/Dy_2O_3/Al_2O_3$/n-Si (100) CTM cells for as-deposited and annealed devices at 300^{o}C, 500^{o}C, 700^{o}C and 900^{o}C are depicted in Figure 4.5. The device which was annealed at 300^{o}C had the lowest capacitance value in the accumulation region than the devices which were annealed at 500^{o}C and 700^{o}C. This could be related to the prevention of the formation of trap charges within the oxide during higher annealing temperatures according to the previous researchers(151,179,180). On the other hand,the value of capacitance in the accumulation decreased when the annealing temperature increased up to 900^{o}C. The behaviour of this capacitance value in the accumulation region could be related to the formation of dangling bonds, defects, interfacial layer during high annealing temperature. Other reseachers have also found similar results(147,181–184) For instance, Mutale *et al*; investigated the effect of PDA on MOS capacitors using Er_2O_3 as the dielectric layer. They found that the capacitance value decreased with an increase in the annealing temperature and this was due to the dangling bonds formation(175). S.k Chuah *et al*; also reported the fabrication of MOS capacitors with CeO_2 thin films. They found that the capacitance value decreased with an increase in the PDA and this was attributed

to the formation of interfacial between high-k /semiconductor material during high annealing temperature(185).

We have studied the effect of annealing temperature on the effective oxide charges (Q_{eff}) through the C-V characteristics at 1MHz. The positive shift in the flat band voltage (V_{fb}) has been observed for as-deposited and annealed devices at 500^{o}C, 700^{o}C and 900^{o}C. This suggests that there is negative effective oxide charges within the oxide layer(183–185). However, the negative shift in the V_{fb} is observed for the device annealed at 300^{o}C. This is attributed to the existence of positive effective oxide charges(175,177,181,186,187). The obtained Q_{eff} of as-deposited annealed devices at 300^{o}C, 500^{o}C, 700^{o}C and 900^{o}C are $-1.90\times10^{12}cm^{-2}$, $3.62\times10^{12}cm^{-2}$, -2.41×10^{12} cm^{-2}, $-6.89\times10^{12}cm^{-2}$ and -1.16×10^{12} cm^{-2}, respectively.

The effect of post-deposition annealing temperature (PDA) on interface states density (D_{it}) was also investigated through C-V curves. The obtained D_{it} values of as-deposited and devices annealed at 300^{o}C, 500^{o}C, 700^{o}C and 900^{o}C are $3.34\times10^{13}eV^{-1}$ cm^{-2} $6.76\times10^{13}eV^{-1}$ cm^{-2}, $2.33\times10^{13}eV^{-1}$ cm^{-2}, 1.42×10^{13} eV^{-1} cm^{-2} and 2.86×10^{12} eV^{-1} cm^{-2}, respecitvely. It is seen that there is some variation in the value of D_{it} with annealing temperature. In other words, D_{it} value decreased with an increase in the annealing temperature between 500^{o}C and 900^{o}C. This could be related to the formation of dangling bonds and interfacial layers during higher PDA. The capacitance value in the accumulation region may also contribute to this behaviour of interface states density(178,188,189).

The impact of annealing temperature on the memory window(ΔV_{fb}) was investigated through the C-V hysteresis curves and measured at 1MHz as shown in Figure. The voltage was swept from -10V to +10V and then back forth -10V. The obtained ΔV_{fb} of as- deposited and annealed devices at 500^{o}C, 700^{o}C, and 900^{o}C are 0.53V, 0.44V, 0.36V, and 0.36V, respectively. The largest memory window of 0.44V was obtained at 500^{o}C than other temperatures. This may be due to the formation of a well-crystallized structure and the large grain size in the charge trapping layer(182,190–192). On the other hand, ΔV_{fb} decreased with an increase in the annealing temperature. During higher annealing temperatures the charges are unable to pass through within the tunnelling oxide layer, thereby

allowing the charge trapping layer to accommodate only a few amounts of charges(190,193,194).

We have studied the effect of sweeping voltage on the memory of CTM devices for as-deposited(a) and annealed devices at (b) 500^{o}C, (b)700^{o}C, and(d) 900^{o}C as shown in Figure. The C-V hysteresis curves were carried out between ±10V to ±12V, respectively. For as deposited are 0.23V, 3.92V and 7.92V corresponding to ±10V, ±11V and ±12V, and annealed at 500^{o}C are 0.37V, 3.63V and 7.85 corresponding to ±10V, ±11V and ±12V, at 700^{o}C are 0.22V, 4.14V and 8.22V, correspoding to ±10V, ±11V, and ±12V. and 900^{o}C are 0.29V, 3.70V and 7.51V correspoding to ±10V, ±11V, and ±12V. The memory window(ΔV_{fb}) and the value of capacitance in the accumulation region increased with an increase in the sweeping voltage in all the devices in Figure 4.6(a-d) due to the increase in the charge trapping with increasing in the applied electric field as reported by(195) The device which was annealed at 700^{o}C had a largest memory window of 8.22V at ±12V than other devices. The smallest memory window of 7.51V was obtained at 900^{o}C by a sweeping voltage of ±12V. This behaviour of ΔV_{fb} could be attributed to two main reasons namely;(a) The tunneling layer may be affected due to at higher annealing temperature and (b) The concentration of oxygen vacancies could provide the defect energy levels resulting in the reduction of trap charges during higher annealing temperature(109,130,191). Furthermore, we have also investigated the effect of interface trap charge densities on the CTM devices as shown 4.8 We found that the device which was annealed at 500^{o}C had a highest N_{it} value 6.24×10^{13} cm^{-2} than other devices. This indicated that there are more trap charge densities in the device.

Finally, the effect of Cs-137 radiation on CTM devices was studied intensively through C-V curves at various doses. As shown in Figure 4.14, there is no significant change in the value of capacitance in the accumulation region between 4Gy and 16Gy. On the other hand, when the device was exposed to 32Gy, the capacitance value in the accumulation region increased significantly as compared to 64Gy and 128Gy. This is due to the defects that were generated during irradiation(158,161,165,166). As may be noted from the same figure, the C-V curves shifted toward the positive voltage side at 4Gy, 8Gy, 16Gy, 32Gy. This suggested that there was oxide trapped charges (ΔN_{ot}) in the CTM device

during the radiation(163,196–198). The obtained negative ΔN_{ot} were between -9.49 $\times 10^{09}$ cm^{-2} and -2.29$\times 10^{11}$ cm^{-2}. While the positive ΔN_{ot} were between 2.93$\times 10^{10}$ cm^{-2} and 5.65$\times 10^{10}$ cm^{-2}. Afterwards, the interface trapped charges ($\Delta N_{it)\ were}$ also obtained due to the shift in the flat band voltage. The positve ΔN_{it} was in the range of 2.43$\times 10^{10}$ cm^{-2} to 7.37$\times 10^{10}$ cm^{-2}. On the other hand, the negative ΔN_{it} -4.84$\times 10^{10} cm^{-2}$ to -5.13$\times 10^{10}$ cm^{-2}. Moreover, the shift in the flat band voltage could be attributed to the majority of charges which are either positive or negative polarities. Because electrons possess higher mobility and are easily swept away from the oxide layer and leaving holes behind. Hence the induced holes are captured within the oxide layer in which both electrons and holes traps exist(164,198–201).

Figure 4.15, shows the interface states density (D_{it}) as a function of radiation dose. We found that the value of D_{it} increased with an increase in the radiation dose exposure. This could be related to the passivation of silicon surface due to the deposition of high-k materials and semiconductors and the reduction in the number of recombination centres inside the high-k layers and semiconductor interface(159,166,198,199). The value of D_{it} was found in the range of 2.74$\times 10^{08}$ eV^{-1} cm^{-2} to 2.07$\times 10^{09}$ eV^{-1} cm^{-2}. Finally, the memory window was obtained through C-V hysteresis curves. It has been observed that the memory window increased linearly with an increase in the radiation dose as shown in Figure 4.16. This indicates that there was an improvement in the trapping process and some positive charges were trapped within the CTM device during high radiaition dose as reported by previous studies(164,197,202,203).

6. CONCLUSIONS AND RECOMMENDATIONS

This study was carried out to investigate the effect of post-deposition annealing and Cs-137gamma ray irradiation on $HfO_2/Dy_2O_3/Al_2O_3$ CTM cells. The high-k materials were deposited into n-Si (100) by using RF magnetron sputtering and E-beam evaporation techniques, respectively. The thin films were annealed at different temperatures 300^{o}C, 500^{o}C, 700^{o}C, and 900^{o}C. The crystalline structure and surface roughness were studied by XRD and AFM techniques. We found that the sample annealed at 900^{o}C had a weak peak corresponding to (400) of Dy_2O_3 thin films while other samples turned into amorphous. We also found that surface roughness decreased with an increase in the annealing temperatures. This was attributed to the formation of a well-crystallized in charge trapping layer.

We investigated the effect of frequency on CTM device. It was seen that the capacitance value in the accumulation region decreased with an increase in the applied voltage frequency. This could be related to the distribution of interface trap charges in the CTM device during C-V measurements. The C-V characteristics were also studied at different annealing temperatures on CTM devices. The C-V curves were observed to decrease with an increase in the PDA between 500^{o}C and 900^{o}C. The main reason behind this was to the formation of dangling bonds and interfacial layers during higher annealing temperatures. We also observed the C-V curves shifted both in the positive and negative direction, respectively. Moreover, the D_{it} decreased with an increase in the annealing temperatures of 500^{o}C to 900^{o}C.

We studied the impact of annealing temperature on the memory window(ΔV_{fb}) by sweeping voltage of -10V to +10V and forth back. It was found that the device annealed at 500^{o}C had the largest ΔV_{fb} of 0.44V compared to other devices. This may be due to the formation of a well-crystallized structure in the charge trapping layer. We have also investigated the influence of ΔV_{fb} at different sweeping voltage of ±10V to ±12V. The ΔV_{fb} and the capacitance value

in the accumulation region were found to increase with an increase in the sweeping voltage in all the devices. The device annealed at 700 ^{o}C had the largest ΔV_{fb} of 8.22V. The smallest ΔV_{fb} for the device annealed at 900^{o}C by sweeping voltage of ±12V. This was due to (i) tunnelling layer being too thick for the device annealed at 900^{o}C and thereby electrons found more difficult to penetrate into the tunnel oxide and (ii) The concentration of oxygen vacancies could providing the defect energy levels resulting in the reduction of trap charges at the higher annealing temperature.In addition, it was found that the device which was annealed at 500^{o}C had a highest N_{it} value 6.24×10^{13} cm^{-2} than other devices. This suggested there were huge amounts of trap charge densities in the device.

The effect of radiation on CTM devices has been studied through the C-V curves. We found that the C-V curves shifted toward the positive voltage side except for 64Gy. We obtained the negative and positive ΔN_{ot} and ΔN_{it} values that were induced by Cs-137 irradiation. The value of D_{it} increased with an increase in the radiation dose exposure. Finally, the effect of radiation on memory window (ΔV_{fb}, *hysteresis*) was studied through the C-V hysteresis curves. We observed that the memory window increased linearly at high doses of expose.

After a comprehensive study in this thesis to understand the effect of radiation on the $HfO2/Dy_2O_3/Al_2O_3$ CTM device. For future works, three recommendations would be given. Firstly, the deposition of thin films should be done by more precise techniques such as the atomic layer deposition (ALD) technique. Secondly, the source of radiation such as Cobalt-60 gamma should be used. Lastly, a different high-K material with a more larger dielectric constant must be considered.

7.REFERENCES

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