ABANT IZZET BAYSAL UNIVERSITY

THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

ELECTRICAL CHARACTERIZATION AND GAMMA IRRADIATION RESPONSE OF HFSIO4 METAL OXIDE SEMICONDUCTOR (MOS) CAPACITORS

MASTER OF SCIENCE

RAMAZAN LÖK

BOLU, MAY 2017

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DEPARTMENT OF PHYSICS

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APPROVAL OF THE THESIS

ELECTRICAL CHARACTERIZATION AND GAMMA IRRADIATION RESPONSE OF $HfSiO_4$ METAL OXIDE SEMICONDUCTOR (MOS) CAPACITORS submitted by **Ramazan LÖK** in partial fulfilment of the requirements for the degree of Master of Science in **DEPARTMENT OF PHYSICS, ABANT IZZET BAYSAL UNIVERSITY** by,

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To my family

DECLARATION

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Ramazan LÖK

ABSRACT

ELECTRICAL CHARACTERIZATION AND GAMMA IRRADIATION RESPONSE OF HfSiO4 METAL OXIDE SEMICONDUCTOR (MOS) CAPACITORS
MSC THESIS
RAMAZAN LÖK
ABANT IZZET BAYSAL UNIVERSITY GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
DEPARTMENT OF PHYSICS
(SUPERVISOR: PROF.DR HÜSEYİN KARAÇALI)

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The smallest pollution that will form or remain on the silicon wafers directly affects the performance of devices produced. Therefore, in the scope of the study, first RCA wafer cleaning procedure was applied in three stages. The first organic cleaning was intended to remove possible organic contaminants at the first stage with a 5: 1: 1 H_2O: H_2O_2: NH_4OH mixture. The second stege was ionic cleaning the purpose of this process was to remove the ionic and heavy metal impurities that may form on the Si wafers by a mixture of 6: 1: 1 H_2O: H_2O_2: HCl. In the third and final stage, a certain amount of oxide layer may grow spontaneously on the Si wafers. The diluted HF solutionwas used to remove the oxide. $HfSiO_4$ thin films were fabricated by RF sputtering system with the power of 200 W, 250W, 300W onto p-type (100) Si substrate and then annealed at 500 ^{0}C, 750, ^{0}C 1000 ^{0}C in Nitrogen environment for 40 minutes. . In addition, the produced thin films were transformed to MOS capacitors. The electrical characteristics of the capacitors were determined by C–V and G/ω–V measurements for several frequencies from 50 kHz to 1 MHz. The C–V characteristics of the MOS capacitors fabricated at 300 W and annealed at 750 C demonstrate better behavior compared to others MOS capacitors. So, to study their susceptibility to radiation, the capacitors were irradiated with a GAMMACELL 220 Co-60 radioactive gamma source up to 70 Gy at a rate of 0.0055 Gy / s. The 1 MHz C-V measurements of the samples were taken at each irradiation step and the radiation sensitivitiy of the devices were examined using flat band and midgap voltage shifts.

KEYWORDS: $HfSiO_4$, MOS Capacitor, Radiation Effects, Radiation Sensitivity

ÖZET

$HFSIO_4$ METAL OKSİT YARIİLETKEN (MOS) KAPASİTÖRLERİN ELEKTRİKSEL KARAKTERİZASYONU VE GAMMA RADYASYONU DUYARLILIKLARI
YÜKSEK LİSANS TEZİ
RAMAZAN LÖK
ABANT İZZET BAYSAL ÜNİVERSİTESİ FEN BİLİMLERİ ENSTİTÜSÜ
FİZİK ANABİLİM DALI
(TEZ DANIŞMANI: PROF. DR. HÜSEYİN KARAÇALI
BOLU, MAYIS - 2017

Silikon pullar üzerinde oluşacak ya da kalacak en küçük kirlilik üretilen cihazların performanslarının doğrudan etkilemektedir. Bu yüzden çalışma kapsamında ilk olarak RCA wafer temizleme prosedürü 3 aşamada uygulanmıştır. Birincisi Organik temizlik bu aşamada, 5:1:1 H_2O: H_2O_2: NH_4OH karışımı ile olası organik kirliliklerin kaldırılması amaçlanmaktadır. İkinci ise iyonik temizlik Bu işlemde amaç, Si yonga üzerinde oluşabilecek iyonik ve ağır metal kirliliklerin 6:1:1 H_2O:H_2O_2:HCl karışımı ile kaldırılmasıdır. Üçüncü ve son aşama ise oksit aşındırma belirli bir süre bekleyen Si yongalar üzerinde bir miktar oksit tabaka kendiliğinden büyüyebilir. Bu oksittin kaldırılması için seyreltilmiş HF çözeltisi kullanılır. $HfSiO_4$ ince filmler magnetron saçtırma yöntemiyle (100) yönelimli p-tipi Si alt taşlar üzerine 200 W, 250 W, 300 W sputter güçlerinde 300 nm kalınlıklarında büyütüldü. Daha sonra ise 500^0C, 750 ^{0}C, 1000 ^{0}C azot ortamında 40 dakika tavlandı. Bu farklı ince filimler MOS kapasitöre dönüştürülerek 50 kHz den 1 MHz farklı frekanslarda kapasitans-voltaj (C–V) ve kondüktans voltaj (G/ω–V) ölçümleri alıdı. Bu MOS kapasitörler arasında elektriksel olarak daha iyi sonuç veren MOS kapasitör son olarak radyasyonuna duyarlılıklarının çalışılması için 0' dan 70 Gy'e kadar GAMMACELL 220 Co-60 radyoaktif gamma kaynağı ile 0.0055 Gy/s doz hızında ışınlandı. Her bir ışınlama adımında örneklerin 1 MHz C-V ölçümleri alındı ve cihazların radyasyona duyarlılıkları düzbant (flatbad) ve ortabant (midgap) voltaj kaymaları kullanılarak incelendi.

ANAHTAR KELİMELER: HfSiO4, MOS Kapasitör, Radyasyon Etkileri, Radyasyon duyarlığı

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1 INTRODUCTION

Metal oxide semiconductor (MOS) structures, between metal and semiconductor layers are formed using a natural or artificial oxidation method of an insulating layer. In the production of MOS capacitors, high-purity metals such as gold (Au) and aluminum (Al) are generally used as metals, and silicon dioxide (SiO_2), hafnium dioxide (HfO_2) are used as an insulators. This is why the MOS capacitor looks like parallel plate capacitor (Ma and Chin, 1980; Sze, 1982). This is an important piece of a metal oxide semiconductor field effect transistor (MOSFET), an important device used in large-scale integration (Tugay, Yilmaz et al. 2012; Kahraman, Yilmaz et al. 2015). For this reason, all studies related to all kinds of the MOS devices firstly require a basic understanding of the MOS structure. In this respect, because of their rapid and economic efficiency the production of the MOS capacitors is very important. Because MOS capacitors provides important information about the characteristics of transistors in radiation measurement systems of computer applications. This structure is widely used in examining the electrical properties of thin insulating films and semiconductor surfaces. These MOS constructions were first fabrication by John L. Moll in 1959 with numerous works including experiments. Because of grown high quality oxide layer, leakage current and economic, the oxides used in these structures for many years are SiO_2. However, nowadays many researches are trying to produce new oxide layers because it is important to diversify the application areas of device performance of the MOS device (Kaya and Yilmaz, 2014; Kahraman, Yilmaz et al. 2015).Thin films have fabricated in various methods. These are evaporation, Chemical vapor deposition, and sputtering and sol-gel methods. Out of these methods sputtering is easier than other others method. It is also more economical and fast to set up the system used.

2 AIM AND SCOPE OF THE STUDY

Hafnium silicates (HfSiO4), It may be a good alternative gate material thanks to high dielectric constant. The hafnium silicate dielectric constant varies between 8 and 15 depending on the Hf content. It has excellent thermal stability, adequate band gaps, and compatibility for the future MOS- based devices. These characteristics of the hafnium silicate are related to the electrical stability of interface between gate oxide and underlying semiconductors (Felix, Fleetwood et al. 2002).

In this study, we investigate frequency dependent electrical characterization of the $HfSiO_4$ MOS capacitors. We have reported the results of a systematic investigation that the $HfSiO_4$ MOS capacitor devices characteristics are influenced by how oxide-semiconductor interface is affected. The electrical characterizations were investigated in the frequency range of 50 kHz to 1MHz by the capacitance- voltage (C-V) and conductance –voltage (G/ω-V) measurements at room temperature. The measured capacitance and conductance were corrected in order to eliminate series resistance effects and find the real MOS capacitance. The corrected conductance –frequency (G_p/ω-F) measurements at constant voltages were also examined to investigate interface states distribution of the devices . Also, the doping concentration (N_d), Fermi energy level (E_F), diffusion potential (V_d), and barrier height (Φ_B) of the $HfSiO_4$ as a function of frequency were obtained by corrected C_c^{-2}–V plots.

3 GAMMA RADIATION INTERACTION WITH MATTER

Because of having no charge, gamma rays are unaffected by Coulomb force. Gamma rays, which are electromagnetic force carriers, randomly interact when they enter the matter. The interactions of gamma rays depend on their energy. Basically, gamma rays make 3 basic interactions. These is photoelectric effect, Compton scattering and pair production

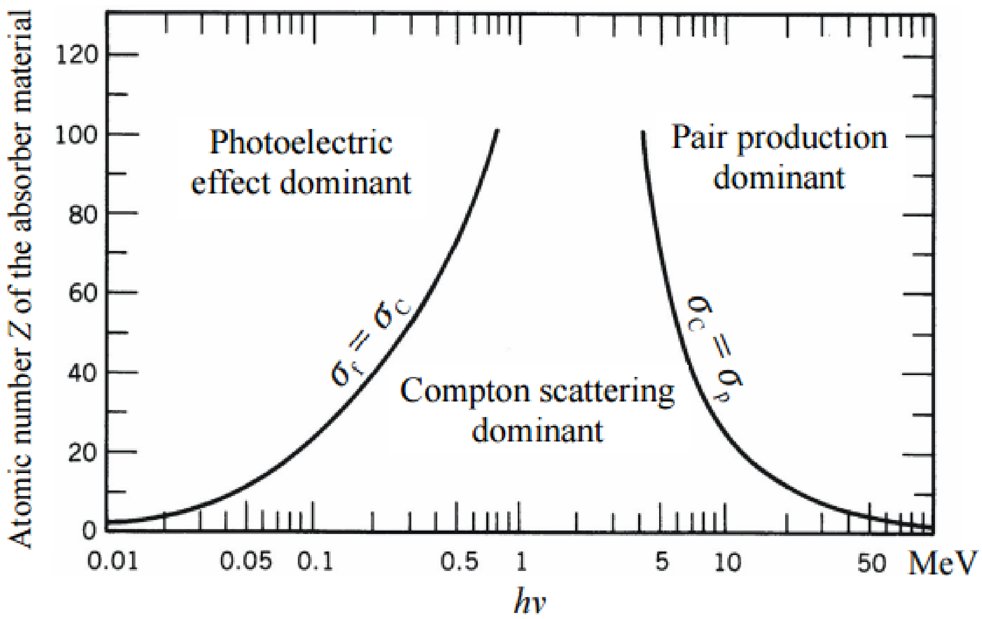


Figure 3.1. Interaction with different substances depending on the energies of the photons (Dressendorfer, 2002)

There is also another interaction addition these three basic interactions namely. Rayleigh scattering is classical coherent elastic scattering. In this case, the gamma rays (photon) can interact with the electron. However, atom cannot ionize. There is no change in the energy of the incoming photon and the scattering photon, only it deviates from the path of photons.

3.1 Photoelectric Effects

In the photoelectric event, a low-energy photon is absorbed by an atom and one electron of the atom is emitted by acquiring the kinetic energy of T_e. This emitted electron is called photoelectron. This event is also called photoelectric phenomenon. The energy required to release the electron is I_B if the frequency of the photon is ν,From energy conservation,

$$E = h\nu = I_B + T_e \quad (3.1)$$

$$T_e = h\nu - I_B \quad (3.2)$$

If the emitted electron is from the lower layer of atom, an electron descends from the upper layer to the lower layer (Fromhold, 1991). As a result, X-rays are emitted from the atom. This interaction mechanism is very important for atoms with high atomic number. The probability of a photoelectric event occurring increases with the atomic number Z of the absorbing medium, and this event decreases with increasing photon energy.

3.2 Compton Scattering

Gamma scattering are basically divided in two types; one is coherent scattering the other is incoherent scattering. In the coherent scattering, the energy of the gamma ray does not change, and this phenomenon occurs with low energy gamma rays. Incoherent scattering almost occurs with virtually free electrons. This event is called Compton scattering. Compton scattering, the incident photon with energy ($h\nu_i$), momentum (pc = E) impact stagnant electron with mass (m_e). The gamma ray is scattered energy ($h\nu_f$) by making an angle of θ with respect to arrival direction. The electron with energy $\sqrt{p_e^2c^2 + m_e^2c^4}$ is scattered back by φ angle by the direction of arrival.

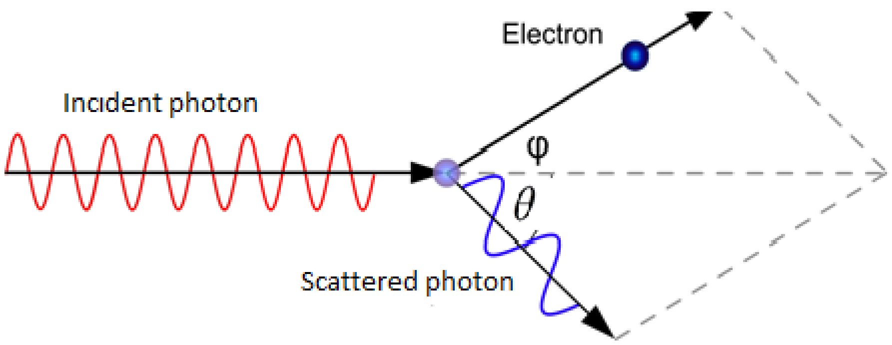


Figure 3.2. Compton Scattering

Conservation of energy

$$hv_i + m_e c^2 = hv_f + \sqrt{p_e^2 c^2 + m_e^2 c^4} \qquad (3.3)$$

Conservation of the momentum

$$\vec{p_i} = \vec{p_f} + \vec{p_e} \qquad (3.4)$$

$$p_e^2 = (\vec{p_i} - \vec{p_f}).(\vec{p_i} - \vec{p_f}) = (p_i^2 + p_f^2 - 2 p_i p_f Cos\theta) \qquad (3.5)$$

Using the Planck relation and the relativistic energy expression

Multiply by c^2 equation 3.5 and $pc = hv$

$$(p_e c)^2 = (hv_i)^2 + (hv_f)^2 - 2h^2 v_i v_f Cos\theta \qquad (3.6)$$

The energy conservation expression above can be squared to give

$$(p_e c)^2 = (hv_i)^2 + (hv_f)^2 - 2h^2 v_i v_f + 2m_e c^2 (hv_i - hv_f) \qquad (3.7)$$

Equation 3.6 and 3.7 can be equated to give

$$-2h^2 v_i v_f Cos\theta = -2h^2 v_i v_f + 2m_e c^2 (hv_i - hv_f) \qquad (3.8)$$

which can be rearranged equation 3.8

$$\frac{1}{hv_f} - \frac{1}{hv_i} = \frac{1}{m_e c^2}(1 - \cos\theta) \qquad (3.9)$$

$$\lambda_f - \lambda_i = \frac{h}{m_e c}(1 - \cos\theta) \qquad (3.10)$$

If $\cos\varphi$=-1, the photon will scattered back and the kinetic energy of the electron will be maximum. As a result of the event, the photon energy decreases. This photon can make photoelectric event, Compton scattering or escape the from environment. The electron that is scattered loses its energy by ionization, excitation or bremsstrahlung (Christillin, 1986).

3.3 Pair production

Pair production formation occurs bigger than energies 1.022 MeV. In this process, the photon disappears by producing an electron-positron pair.

From energy conservation;

$$E_{\gamma} = T_{+} + T_{-} + 2m_e c^2 \tag{3.11}$$

where E_{γ} is energy of the photon, T_{+} is kinetic energy of the positron, T_{-} is kinetic energy of the electron, $2m_e c^2$ are rest mass energy of electron and positron. In the case of pair production, a heavy atom is required for momentum conservation. However, the recoil of energy the atom is a neglected because it is so small.

Pair production is the inverse of extinction. The photon disappears when it combines with an electron in the environment and two annihilation photons emitted in opposite directions with energy 0.511 MeV. These annihilation photons can make photoelectric event, Compton scattering or escape the environment (Das, 2003).

3.4 Absorption of Gamma Rays

Unlike the charged particle, when the gamma ray interacts with matter, it loses all or most of its energy in a single event. The reduction of light in an environment is defined by the effective absorption coefficient (μ) which depends on the energy and frequency of the light. If I(x) is the intensity of the gamma at x, intensity in infinitesimal dx thickness is dI the following equation can be defined as follows for the intensity I(x) .

$$dI = I(x+dx) - I(x) = -\mu I dx \tag{3.12}$$

The minus sign here shows that the intensity of the light is decreasing with the increasing distance (Fromhold, 1991; Das, 2003). If the expression 3.12 is integrated with the initial intensity being I_0 at x = 0;

We get

$$\frac{dI}{I} = -\mu dx \tag{3.13}$$

$$\int_{I_0}^{I} \frac{dI}{I} = -\mu \int_{0}^{x} dx \tag{3.14}$$

$$I(x) = I_0 e^{-\mu x} \tag{3.15}$$

4 STRUCTURE AND WORKING PRINCIPLE OF THE MOS CAPACITOR (MOS)

4.1 Metal-Oxide-Semiconductor (MOS) Structure

MOS consists of a metal oxide semiconductor layer structure. The MOS structure is shown in Fig 4.1. This structure is composed of a semiconductor lower surface, a thin oxide layer and top metal contact. This metal contact is called gate. A second metal layer is coated to the other surface of semiconductor as an omics contact. The structure has a p-type substrate in figure 4. 1. This type of MOS capacitor is referred to as n-type MOS capacitor. So inversion region acts as an n-type semiconductor.(NURTAN, 2010)

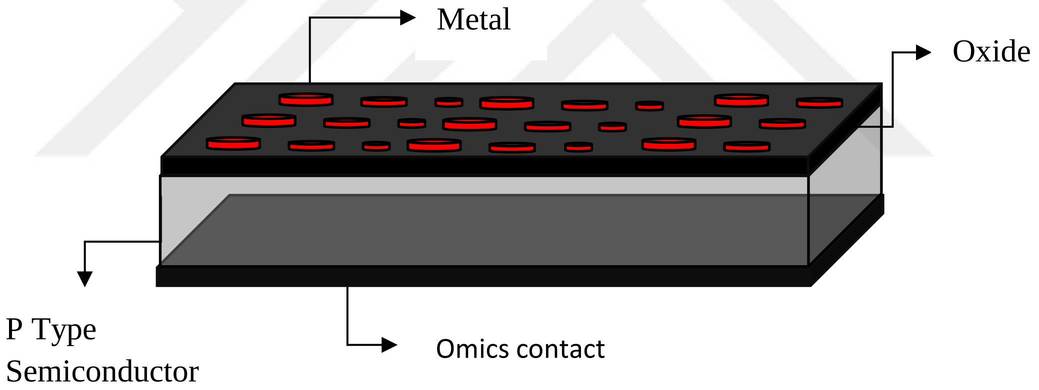


Figure 4.1. Basic MOS Structure

The structure's distinctive features are determined by the oxide-semiconductor interface properties. Such structure of the oxide layer must be of good quality. In addition, unsaturated bonds in the oxide-semiconductor interface are the qualifications required to be minimal. Depending on thin film deposition technique, it has been observed that MOS structure is shifting from the ideal characteristics because of unsaturated bond and impurities. Fixed oxide charge, interface charge, oxide trapped charge, mobile oxide charge are example of these impurities. (Sze, 1981; Nicollian and Brews, 1982; Bentarzi, 2011).

4.2 Ideal MOS Capacitor

Energy-band diagram of the unbiased ideal MOS structure is shown in Figure 4.2 for both n-type and p-type semiconductors.

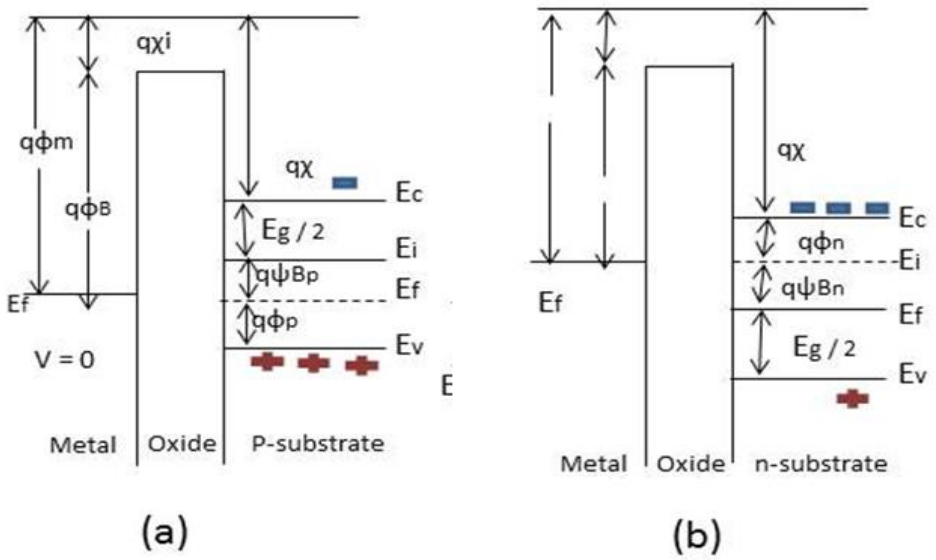


Figure 4.2. Metal-Oxide-Semiconductor Capacitor energy band diagram for P-type and N-type (Technology, 1997)

An ideal MOS capacitor is defined as,

- In zero applied bias, the energy difference between the metal work function Qm and the semiconductor work function Qs is zero. In other words work function difference between the metal and semiconductor is zero (Goetzberger, 1966).

$$\phi_{MS} = \phi_M - (\chi - \frac{E_g}{2q} - \Psi_{Bn}) = \phi_M - (\chi + \phi_n) = 0 \qquad \text{For n- type} \qquad (4.1\text{- a})$$

$$\phi_{MS} = \phi_M - (\chi + \frac{E_g}{2q} - \Psi_{Bp}) = \phi_M - (\chi + \frac{E_g}{q} - \phi_p) = 0 \qquad \text{For p- type} \qquad (4.2\text{- b})$$

where, χ and χ_i are the electron affinities for the semiconductor and oxide respectively, and Ψ_{Bn}, Ψ_{Bp}, ϕ_n, ϕ_p are the Fermi potentials with respect to the midgap and band edges (Gökcen, 2003) .

- Traps, fixed and mobile ions do not exist in the oxide and oxide semiconductor interface. The interface state and interface charge are also exist in oxide semiconductor interface
- The band gap of the oxide is so large that thermal charge carrier density is small enough to be ignored. There is no carrier transport through the insulator under dc biasing conditions or the resistivity of the insulator is infinite.
- The only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those with the equal but opposite sign on the metal surface adjacent to the insulator.(Nicollian, 1982; Technology, 1997)

4.3 Biasing the MOS Capacitor

When an ideal MOS capacitor is biased, three main regimes occurs depending on the type of substrate and bias direction in the semiconductor surface. The regimes are described as accumulation, depletion and inversion. In here for the P type- MOS capacitor, we explain relation between charge, dangling band and electric field (Grove, 1967).

4.3.1 Accumulation

When voltage, which is less than zero is applied to p-type MOS capacitor, an electric field occurs due to the applied voltage. Thanks to this electric field, holes will be attracted towards the semiconductor interface. So the MOS capacitor starts to store positive charges at the substrate surface. It causes the stored charges deflected up right in the conduction band. In this situation, it is called accumulation (Grove, 1967). The capacitance of MOS capacitor must be approximately equal to the oxide capacitance.

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_{o}}{d_{ox}} \tag{4.3}$$

where, ε_o is the permittivity of the free space, ε_{ox} the relative permittivity of oxide, and d_{ox} the oxide thickness. C_{ox} is oxide capacitance and expressed per unit gate area [F cms^{-2}] (Nicollian and Brews, 1982).In the accumulation condition, the Fermi level near the Si surface will move to a position closer to valance band edge as shown in Fig 4.3

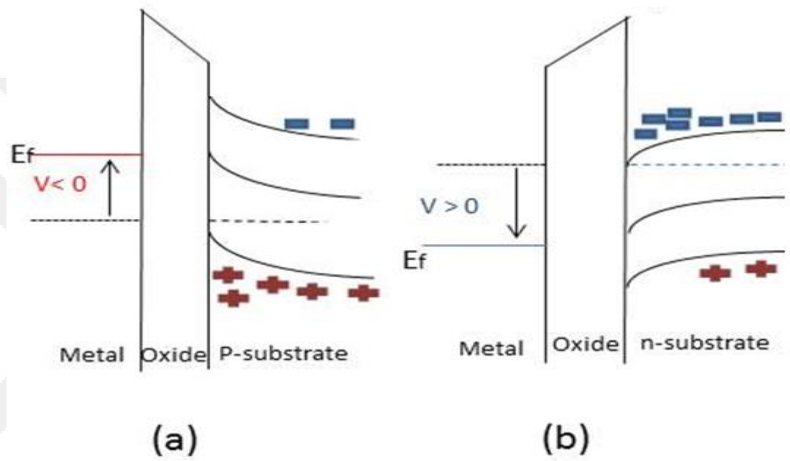


Figure 4.3. The energy bad diagram of MOS capacitor for accumulation,

4.3.2 Depletion

When a small positive voltage is applied to the metal plate, electric field is created in oxide away from the hole surface on the semiconductor surface. In this case, the hol density on the semiconductor surface becomes smaller than the hole density of the inner part of the semiconductor. Because of this, bands are bent downwards. So, Electrons start collecting in the regions near the semiconductor surface of the conduction band. On the semiconductor surface, the holes are reduced in a region with a width w which varies with the applied voltage. A depletion zone occurs. This event is called the depletion event. In the case of depletion, the space charge density is given by the following equation(Nicollian, 1982).

$$Q_{SC} = qN_A^- \omega = Q_A \tag{4.4}$$

where N_A^- is the ionized acceptor density, Q_A is the acceptor load in the unit surface. The MOS capacitance in this region is determined by the space charge capacitance and oxide capacitance. If high frequency voltage suddenly changed, inversion charge will be accumulating later depending on the speed of reunion of minority carriers. This is an unstable situation and identified as deep depletion. The thickness of the depletion zone is given by the following equation.

$$\omega = \varepsilon_s A_{OX} \left(\frac{1}{C} - \frac{1}{C_{OX}} \right) \tag{4.5}$$

Where ε_s is the dielectric constant of the semiconductor, A_{OX} is the oxide thickness C_{OX} is the oxide capacitance

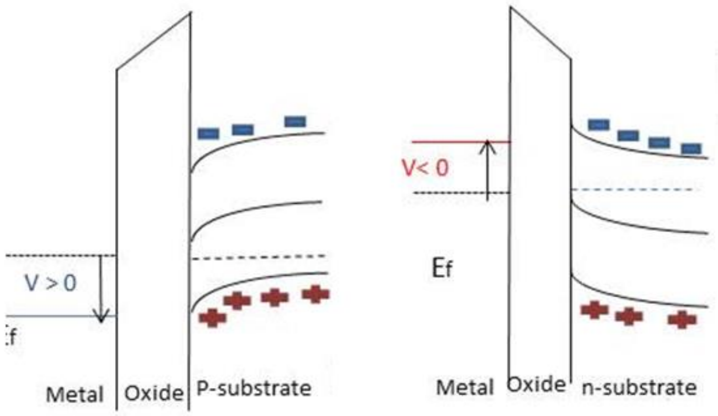


Figure 4.4. The energy bad diagram of MOS capacitor for Depletion

4.3.3 Inversion

When a big positive voltage is applied to the metal plate, bands are bent more downwards. Self-energy level (E*i*) falls below fermi energy level (E*f*). In that case the electrons which are minority carriers in the semiconductor surface begin to increase. The electron density is larger than the hole density. This is called the inversion of the p-type semiconductor surface.

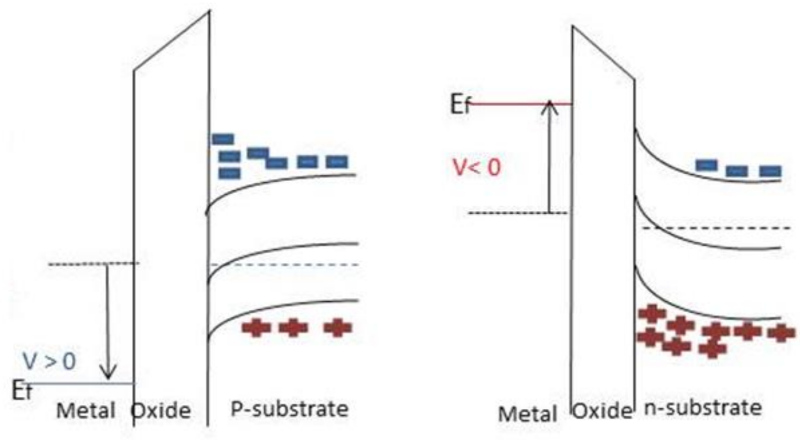


Figure 4.5. The energy bad diagram of MOS capacitor for Inversion

$$Q_{SC} = Q_N + Q_A \tag{4.6}$$

where Q_N is the charge of the electrons in the unit surface in the inversion region and Q_A is the charge of the acceptor in the unit surface (Gökcen, 2003).

5 NON-IDEAL MOS STRUCTURE

Ideal MOS structure is different from the real MOS structure. This difference is caused by the presence of the oxide charges and the work function difference that exists in practice For example, there is no space charge and mobile ionic charges in the ideal oxide layer and oxide semiconductor interface state. In real structure, the oxide and oxide semiconductor interface is not electrically neutral. Because of mobile ionic charges, fixed oxide charges, oxide trapped charges, and interface trapped charges, the MOS capacitor is deviated from the ideal characteristics of the MOS structures. These situations and classification of charge are demonstrated in Fig.5.1 (Hofstein, 1965).

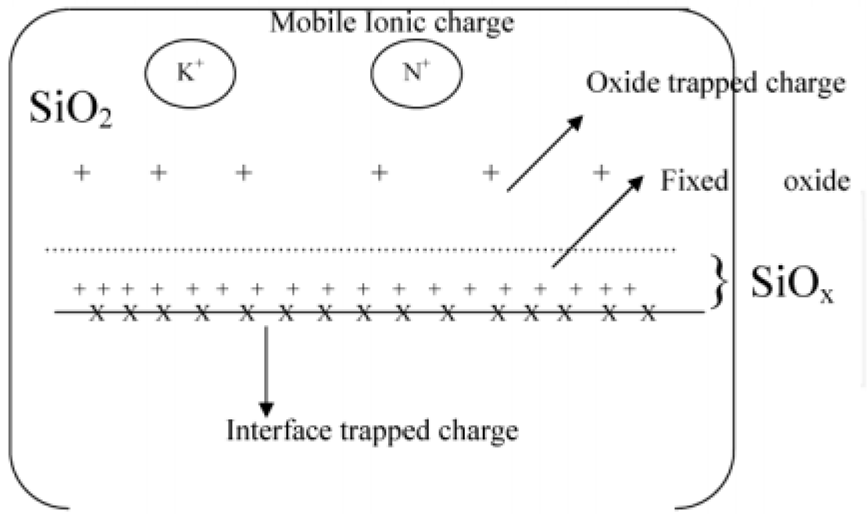


Figure 5.1. The impurity charges on the high-frequency MOS devices

5.1 Interface Trapped Charges

The definition of interface states has been investigated theoretically by Shockley, Tammi and other scientists. Due to interruption of the periodic lattice structure of a crystalline interface, interface states are shown that they are prohibited in the band gap. Interface states can be accessible in energy levels in the oxide-semiconductor interface in the forbidden band gap. There are two types of interface states. They behave like an acceptor or donor. Therefore, interface states can trap both positive and negative charges. Because of this, C-V curves can be shifted toward positive or negative voltages depending on trapped charges type. Frequency of the applied voltage during the measurement, it was observed that affect the interface states. So, number of trapped charges can show diversity depending on measurements standards (Taur and Ning, 1998).

5.2 Fixed Oxide Charges

Fixed oxide interface charges are located in the oxide and oxide-semiconductor interface. Because of the fact that the oxide and semiconductor have different crystal structures .The inevitable crystal defects cause local charges. Major characteristics of this charges, When the voltage applied oxide-semiconductor structure, It is independent of the charge status. Fixed oxide charges (Q_f) is generally positive. Fixed oxide charge can affect the electrical device characteristics. These charges shift the C-V measurements toward more negative voltages .So, the device deviates from expected case both for p-type and n-type semiconductor based MOS capacitors(Hofstein, 1965; Schroder 1998).

5.3 Mobile Ionic Charges

The mobile charges (Q_m) are located in the interface between metal and oxide or oxide and semiconductor layer. Because of relatively moveable, such charges can be dragged within the oxide due to the low temperatures. Motionless oxide charge can be distinguished from a moving ionic charge at low temperature under applied voltages. The density of the fix oxide charge may change during the process. Consequently, mobile ionic charge can come back and forth between metal-oxide semiconductor-oxide interfaces. So, ionic current may occurs in the structure. These mobile ions are Na^+, H^+, H^3O^+, K^+, and Li^+ . Because of the ionic current, the stability of the electrical MOS characteristics is greatly impaired. The mobile ionic charges can be found from the following equation

$$Q_m = \Delta FB \times C_{OX} \qquad (5.1)$$

where ΔFB and C_{OX} are flat band shift , oxide capacitance respectively

5.4 Oxide Trapped Charges

Oxide traps can occur due to many reasons. Structural defects, metal impurities, oxidation-induced defects, or other defects caused by radiation or similar bond breaking processes of dielectric layer are example of some reasons. These oxide traps may trap mobile charges in the structure known as oxide trapped charges denoted as $Q_{ox.}$ They may be exchange charges between oxide and interface at oxide/semiconductor. So, they are increased the number of charge density in the MOS capacitor. In the oxide layer, the trapped charges can be both positive and negative. But, generally they are positive. The C-V curves may shift the more negative voltages because of increases of positive charges in the structure. The sum of all oxide charges is also called effective oxide charge Q_{eff} as given in Eq (Aktag, Yilmaz et al. 2010; Ergin, Turan et al. 2010; Tascioglu, Tataroglu et al. 2010).

$$Q_{eff} = Q_m + Q_f + Q_{ox} + Q_{it} \qquad (5.2)$$

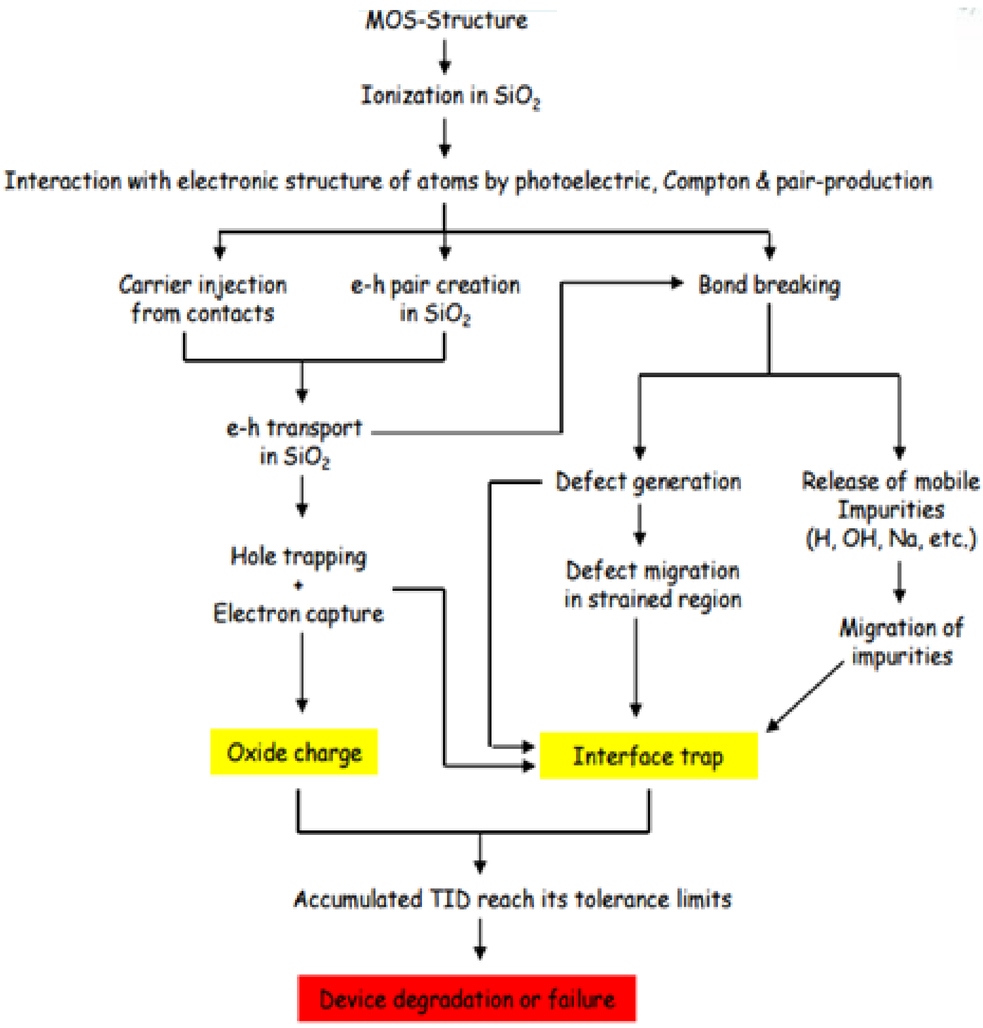


Figure 5.2. Radiation effects on metal oxide semiconductor

6 THE THEORY OF INTERFACE STATE DENSITY MOS STRUCTURE

In a MOS structure, the presence of interfacial traps and insulator charges will affect the ideal MOS characteristics. A foreign atom or a defect in the crystal structure of a semiconductor leads to the appearance of energy levels in the forbidden energy zone. During the construction of a MOS, there are defects that cannot be prevented even if the silicon surface is cleaned. If the irregularity of the crystal surface is also taken into account in the forbidden energy zone, a large number of energy levels come to the fore of the unit area

Although the theoretical estimates are that density of surface atoms is around 10^{15} cm^2 for density of surface states, the experimental results show that this is only 10^{11}-10^{12} cm^2. Surface states are divided into two classes which are the slow and fast. The slow surface state is found on the metal side of the insulator. Slow surface of the insulating states on the surface of the metal side is fund. These still charges in the insulating structure at sufficient temperature contain defects, particularly under high electric field. It tends to migrate within insulators which are formed by the moving ions. The slow surface states almost relieved by thermal oxidation. The slow surface states do not affect the MOS capacity

The fast surface states are located near the insulator semiconductor interface. They have the energy close to the center of the forbidden energy zone. Because of band bending, that surface potential is the change. It moves up and down according to the level of the unbending fermi energy. As a result, it makes a sudden charge exchanges with conductivity and valence band. Surface conditions with energies outside the forbidden energy zone are called constant surface conditions. And caring charge is also called constant surface charge or oxide charge.

Due to the trapped interface charge, which is at the semi-conductor-insulator interface, can quickly exchange the conductivity or the valence band of the silicon in a short time, these surface conditions are also referred to as surface recombination centers.

Distribution function for interface traps; for the donor and acceptor interface traps are given below

For the donor interface traps;

$$f_{SD}(E_t) = \frac{1}{1 + g\exp\left(\dfrac{E_F - E_t}{kT}\right)} \tag{6.1}$$

For acceptor type interface traps;

$$f_{SD}(E_t) = \frac{1}{1 + g\exp\left(\dfrac{E_t - E_F}{kT}\right)} \tag{6.2}$$

where, E_t is the interface trap level energy, E_F is the fermi energy level and g is the thermal state degeneration which is 2 for the donor traps, 4 for the receiver traps (Dokme, 2006). Under a bias, the interface trap levels, valence and conductivity bands and the Fermi level move up or down until it becomes fixed. This change leads to the change in MOS capacitance and ideal curve. The equivalent circuit including the effect of the interface traps is shown in Figure 6.1

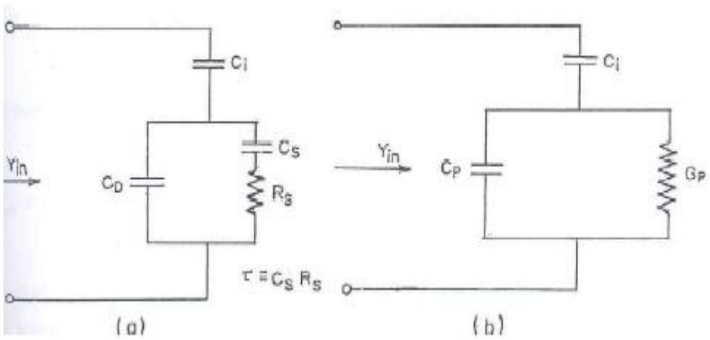


Figure 6.1. Equivalent circuit with interfacial trap effects.

where C_i is oxide layer capacitance of the insulating layer and C_D is the capacitance of the semiconductor depletion layer. C_S R_S multiplier as the lifetime of interface traps (τ) which defines the behavior of the interface traps. The parallel line of Figure (6.1) a, the frequency-dependent capacitance C_P and it can be written as a parallel connected frequency dependent conductivity G_P. Admittance in parallel line can be written as below.

$$Y = \frac{1}{z_1} + \frac{1}{z_2} = j\omega C_D + \frac{1}{Rs + \frac{1}{j\omega C_S}} = G_p + j\omega C_p \qquad (6.3)$$

where the conductivity ,G_P, and the capacitance ,C_P, can be written as follows

$$G_p = \frac{1}{R_p} = \frac{C_S \omega^2 \tau}{1+\omega^2 \tau^2} \qquad (6.4)$$

$$C_p = C_D = \frac{C_S}{1+\omega^2 \tau^2} \qquad (6.5)$$

The total impedance, Z, can be written as following equation,

$$Z = -j\left(\frac{1}{\omega C_i} + \frac{\omega C_p}{G_P^2 + \omega^2 C_P^2}\right) + \frac{G_p}{G_P^2 + \omega^2 C_P^2} \qquad (6.6)$$

Using eqs 5.3, 5.4 and 5.5 can be rewritten as

$$Y_T = -j\left(\frac{G_P^2 + \omega^2 C_P}{G_P}\right) + j\omega\left[\left(\frac{G_P^2 + \omega^2 C_P^2}{G_P^2 + \omega^2 C_P^2 + \omega C_P}\right)C_i\right] = G_{im} + j\omega C_{in} \qquad (6.7)$$

where Y_T is total admittance. If the series resistance exists and great, the measured conductance G_m and capacitance C_m are not real value (Dokme, 2006) . Equivalent circuit is shown in Figure 6.2

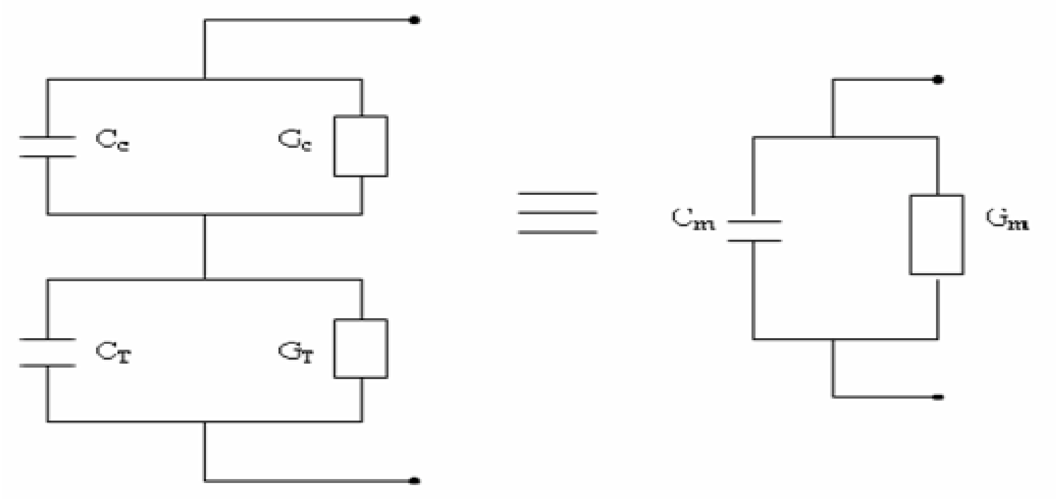


Figure 6.2. Equivalent circuit of the MOS Structure

$$Z_1 = \frac{1}{j\omega C_C + G_C} \tag{6.8}$$

$$Z_2 = \frac{1}{j\omega C_T + G_T} \tag{6.9}$$

$$Z = \frac{1}{j\omega C_m + G_m} \tag{6.10}$$

C_C and G_C can be analytically solved.

$$Z = Z_1 + Z_2 \tag{6.11}$$

$$Z_1 = Z - Z_2 \tag{6.12}$$

$$\frac{1}{Z_1} = j\omega C_C + G_C = \left(\frac{1}{j\omega C_m + G_m} - \frac{1}{j\omega C_T + G_T} \right)^{-1} \tag{6.13}$$

$$\frac{1}{Z_1} = \left[\left(\frac{\left(G_m G_T - \omega^2 C_m G_T\right) + j\omega\left(G_T C_m - C_T G_m\right)}{\left(G_T - G_m\right) + j\left(C_{T-} C_m\right)}\right)\right] \tag{6.14}$$

If we write $G_T = \frac{1}{R_S}$ and The value C_T is neglected, Corrected conductance is found as equation 5.15

$$G_C = \frac{\left(G_m - G_m^2 R_S\right) - \omega^2 C_m^2 R_S}{\left(1 - G_m R_S\right)^2 + \omega^2 C_m^2 R_S^2} \tag{6.15}$$

where, Rs is the series resistance the impedance is the real part of Z and can be calculated from the strongly accumulation values of C_m and G_m in the high frequency regime.

$$Z = \frac{1}{j\omega C_m + G_m} = \frac{G_m - j\omega C_m}{G_m^2 + \omega^2 C_m^2} = \frac{G_m}{G_m^2 + \omega^2 C_m^2} - \frac{j\omega C_m}{G_m^2 + \omega^2 C_m^2} \tag{6.16}$$

From Eq 5 .16 Rs has been calculated as

$$R_S = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \tag{6.17}$$

The Corrected capacitance is given by

$$C_C = \frac{C_m}{\left(1 - G_m R_S\right)^2 + \omega^2 C_m^2 R_S^2} \tag{6.18}$$

If Eqs (5.15) and (5.18) are rearranged

$$C_C = \frac{\left(G_m^2 + \omega^2 C_m^2\right) C_m}{a^2 + \omega^2 C_m^2} \tag{6.19}$$

$$G_C = \frac{\left(G_m^2 + \omega^2 C_m^2\right) a}{a^2 + \omega^2 C_m^2} \tag{6.20}$$

The corrected capacitance (C_c) and corrected conductance (G_c) are found as equation 5.19, 5.20 respectively. A is defined as

$$a = G_m - \left(G_m^2 + \omega^2 C_m^2\right) R_S \tag{6.21}$$

C_m and G_m are measured capacitance and measured conductance respectively.

6.1 Radiation Effect on MOS Structure

Effects of gamma ray on the MOS device generation of electrons- hole (e-h) pairs and defects sites in the oxide, interface between oxide and semiconductors. Some of these produced e-h pairs can be trapped by the defect in the structure, which leads to shift in the flat band, midgap and threshold voltages of measurement electrical characteristics. The detailed mechanism for the effects on the device structure of the irradiation is shown in Fig. 6.4. the MOS devices are more susceptible to ionization than displacement damage. Ionization is the production of e-h pairs in the semiconductor and oxide layers, as mentioned above. Atomic displacements cause a neighboring interstitial atom and vacancy and are less effective in the radiation response of the MOS devices (Dressendorfer, 2002).

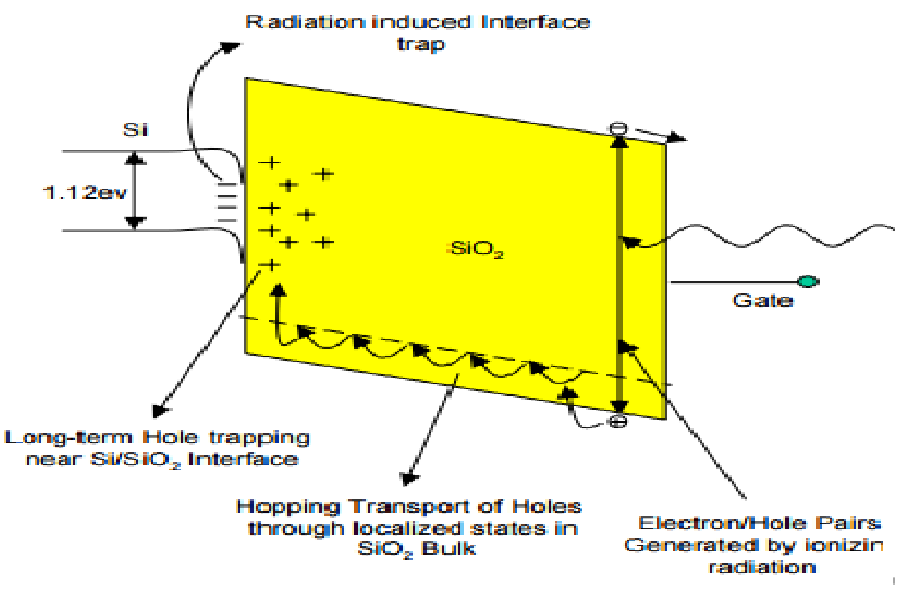


Figure 6.3. The effects induced by ionizing radiation in an MOS device (Oldham, 2003).

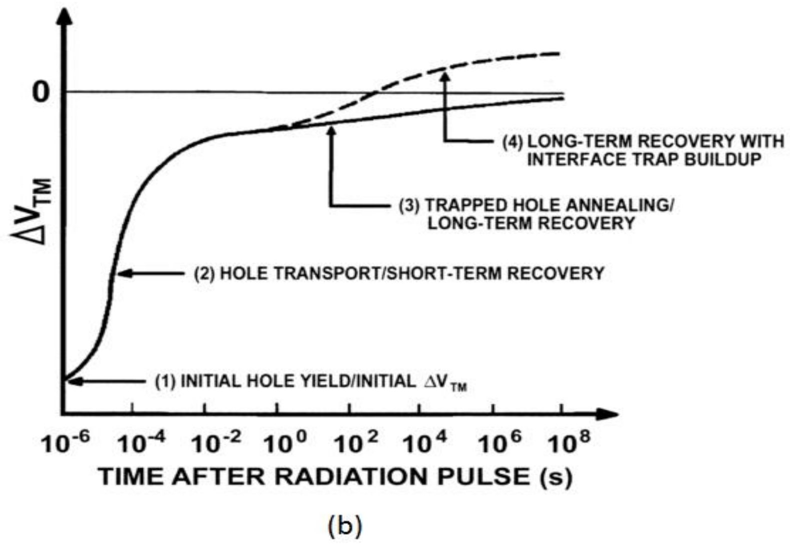


Figure 6.4. Time dependent threshold voltage changes occurring after the irradiation process (Oldham and McLean, 2003)

The radiation sensitive part of the MOS structure is the oxide layers. The ionizing radiation can create an enormous number of electron-hole pairs in a few pico-seconds in devices. The electrons are much more mobile than the holes, So they immediately disappear from the metal contacts, and some of these pairs are neutralized by recombination after a few microseconds. The voltage shifts can be very high in only a few microseconds since because of high electron and hole yielding. These processes are depicted at first steps in Figs. 6.4 and 6.5. The holes begin to move towards the oxide-semiconductor interface through various characteristic transport mechanisms. The most accepted mechanism in this hole transport is called "hopping". The holes move in the oxide layer using the shallow trap states in the oxide layers and some of them are recombined with electrons along the path. The recombination effect and hole transportation on voltage shifts are depicted in the second part of Fig. 6.4 and 6.5. The holes are trapped by deep traps when they approach the oxide layer and the semiconductor interface. These deep trap situations are permanent traps and cause permanent changes in the flat band, midgap, and threshold voltage. These situations have got a very significant effect on the voltage shifts in the devices. The interface traps created by radiation can be defined as the last important parameter in the radiation sensitivity of device. These traps are the energy states of the forbidden energy band of the semiconductors, which are found in the oxide layer and at the semiconductor interface. And these are known as two groups as acceptor states and donor states. These energy states can trap mobile charges depending on their type, which will contribute voltage shift in the structure. The place and the effects on the device characteristics of this case are depicted in the last part of Figure 6.4 and 6.5.

Voltage shift in the devices is positive Fig. 6.5. The number of negatively charged interface states is greater than the number of trapped holes. As a result this is known super recovery effects.

6.2 Theory of Traps Generated by Radiation

The ionizing radiation is very complex to interact with the gate oxide materials and its interface of the MOS capacitor. Accumulation of trapped charges and enhancement of bulk oxide traps; these are two important events which are crucial to understand the response of these devices to radiation. The charges trapped by the radiation are directly proportional to the amount of energy accumulated in the target oxide materials and devices. Some researchers have found that the average energy to create e-h pairs is equal to 18 eV for the conventional SiO2 oxide layer. Depending on the type of oxide layers, this value can change if it is small. Compared to electrons, holes are immobile. May be trapped in the oxide layer by shallow and especially deep traps, which may lead to cumulative net charge density. Deep traps, which are located near the interface, occur in the oxide layer. There are uncompleted bonds in the transition region. This region contains excess semiconductor or oxygen vacancies. The bonds can break with irradiation, which can trap mobile charges. Broken bonds may act as donor sites or acceptor sites, depending on the type of bonding. Acceptor and donor sites can trap mobile negative and positive charges.

For example in conventional SiO2, broken bond or strained on the structure, there is an oxygen atom that is missing in the usual lattice configuration, leaving a weak Si-Si bond behind it. Thus, every Si atom can trap positive charge, or back bond three oxygen atoms. And the lattice relaxes as in Fig.6.6

Defects are found in the oxide and semiconductor interface. Radiation leads to these defects. The interface traps occur when reaching the radiation interface region or when the oxide is completely absorbed. The e-h pairs and the transport of these mobile charges may cause interface states. The idea is that all the models are compatible with the literature; radiation-dependent interface traps precursors are Si atoms attached to three Si atoms and a hydrogen atom.

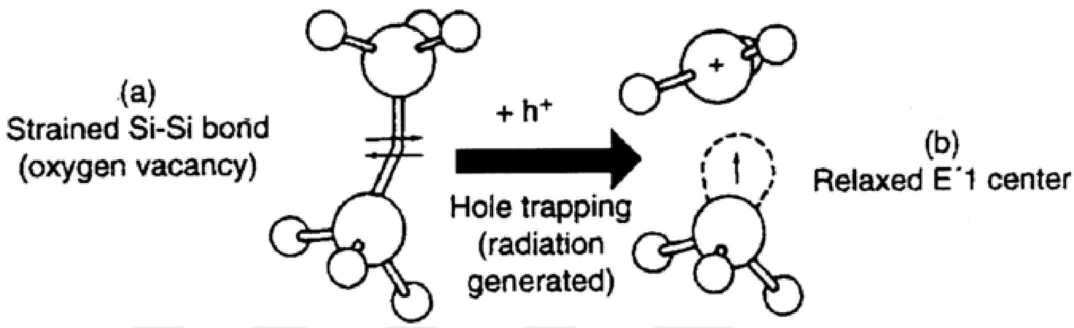


Figure 6.5. Simple hole trapping mechanism on the SiO2 layer (Oldham and McLean, 2003)

When the bond between Si and H is broken it has not passivated electrically active defects are left with a dangling bond. It is clear that the dominate process progresses in two stages involving hopping transport of protons. The cases of the first process, the hole created by the radiation are transported in the oxide as free hydrogen atoms the form of protons. The case of the second process, when protons do interact reached the interface, and breaks the Si-H bonds there to bring H and trivalent Si defects. Moreover, accumulation of extreme mobile charges near the depletion zone and especially at the interface under strong inversion zones results in a decrease in surface potential. This causes an increase in the capacitance value.

Semiconductor surface potential (Ψ_r) can be derived by using 1D Poisson equation.

$$\frac{d^2\Psi_r}{dx^2} = -\frac{\rho_r(x)}{\varepsilon_s} \tag{6.14}$$

where ε_s is the permittivity of semiconductor is, $\rho_r(x)$ is the volume charge density in the irradiated state andby the following equation.

$$\rho_r(x) = q(N_D - N_A + p_r - n_t) \quad (6.15)$$

For any surface potential, it can calculate following equation the steady state intensity of electrons and holes as follows for uniform irradiation.

$$n_r = (n_{p0} + \Delta n)e^{(\beta\Psi_r)} \quad (6.16)$$

$$p_r = (p_{p0} + \Delta n)e^{(-\beta\Psi_r)} \quad (6.17)$$

Where, the redundant e-h pairs created per volume are defined as Δn which is given by;

$$\Delta n = g_0 \dot{D} \tau_r \quad (6.18)$$

Here, g_0, $\dot{D}$ and τ_r are carrier creation rate in terms of (carrier/ m^3xrad), the incident dose-rate (rad/s) and mean lifetime of carriers in irradiated conditions respectively. The average lifetime of the carriers is affected by the carriers produced in the substrate.

$$\frac{\tau_r}{\tau} = \frac{n_{p0}}{n_{p0} + \Delta n} \quad (6.19)$$

Where τ is average lifetime of minority carriers under unirradiated condition. τ_r Can obtain utilizing the by means of Eqs. 6.18 and 6.19

$$\tau_r = \frac{-n_{p0} + \sqrt{n_{p0}^2 + 4g_0 \dot{D} n_{p0} \tau}}{2g_0 \dot{D}} \quad (6.20)$$

In the irradiated condition, the electric field in the surface is given as below.

$$\Im_{sr} = -\frac{\partial \Psi_r}{\partial x}|_{x=0} = \pm \frac{\sqrt{2}kT}{qL_D} F\left(\beta \Psi_{sr} \frac{n_{p0} + \Delta n}{p_{p0}} \right) \tag{6.21}$$

Where L_D is Debye length, and derivated by

$$L_D = \left[\frac{kT\varepsilon_s}{(p_{p0} + \Delta n)q^2} \right]^{1/2} \tag{6.22}$$

Gauss's law can be given as per unit area required to create field, as given in the following equation.

$$Q_{sr} = -\varepsilon_s \Im_{sr} = \pm \frac{\sqrt{2}kT}{qL_D} \varepsilon_s FF\left(\beta \Psi_{sr} \frac{n_{p0} + \Delta n}{p_{p0}} \right)$$

Due to the radiation, fix oxide charge can be accumulated. By changing the charge at the interface, a change in the flat band voltage can occur. The applied voltage (V) in the irradiated condition depends on the surface potential and is as follows,

$$V = -\frac{Q_{sr}}{C_{ox}} + \Psi_{sr} + \Delta V_{fb} \tag{6.23}$$

Flat band shift is given in the following equation.

$$\Delta V_{fb} = \frac{q}{C_{ox}} (\Delta N_{it} - \Delta N_{ot}) \tag{6.24}$$

Here, C_{ox} is oxide capacitance per unit area of the layer, ΔN_{it} and ΔN_{ot} is changes in interface state charges , changes in oxide trapped charges per unit area created by irradiation and respectively. Here it is important, excessive carrier due to radiation in radiation-induced changes at the interface, the trapped charge density (ΔN_{it}) can be given following equation;

$$\Delta N_{it} = k_g f_y D t_{ox} f_{it}(N_{it}) \tag{6.25}$$

where, f_y is the probability density that the e-h pairs escapes from recombination, D is indicent radiation dose in terms of energy E, $f_{it}(N_{it})$ is interface trapped charges generated per unit irradiation-induced e-h pair, k_g is the number of generated e-h pairs per unit dose. N_{it} is a function of the surface potential which is the interface charge per N_{it} unit area, and it is expressed by the following expression.

$$N_{it} = \int_{E_{VB}+q\Psi_s}^{E_{CB}} D_{it}(E_t) f(E_t) dE_t \tag{6.26}$$

where the valence band on the Si surface and the conductive band boundaries are (E_{VB}+qΨ_s) and E_{CB} respectively. $D_{it}(E_t)$ can be expressed as the energy band gap distribution interface state. Oxide trap charge density can be expressed by the following formula;

$$\Delta N_{ot} = F_H f_T \tag{6.27}$$

Here F_H being total number of holes created in oxide layer can be expressed by the following formula

$$F_H(\Im_{ox}, E) = t_{ox}\lfloor k_g(E) f_y(\Im_{ox}, E) D \rfloor$$

where f_t being fraction of radiation generated holes layer can be expressed by the following formula

$$f_T = \sigma_{ht}(\Im_{ox}) \overline{\overline{N}}_{ht} \Delta x \tag{6.28}$$

where Δx is expressed by the width of the hole-trapping regions. σ_{ht}, is the local oxide field dependent cross section of hole traps capturing holes, $\overline{\overline{N}}_{ht}$ is average density of hole traps, $\overline{\overline{N}}_{ht}$ is average density of hole traps, σ_{ht} is the cross-section of the perforated traps depending on the local oxide area.

7 MATERIALS AND METHODS

7.1 Fabrication of MOS

Two main processes were followed to fabricate MOS capacitors. First one is that, all samples were cleaned up considering the standard Radio Corporation of America (RCA) cleaning process. The second process is deposited $HfSiO_4$ layer and metallization to make metal contacts. These two processes are explained as follows in details in the following sections.

7.2 Cleaning Process of Wafers

A well-cleaned semiconductor wafer is important in preventing many surface defects. The wafer should be cleaned very well in order to fabricate high-quality MOS capacitors with a flawless interface. Non-clean wafer deviates from impaired electrical measurements and may cause the sample to degradate. In order to remove organic substances and heavy metal impurities, the chemical cleaning process was done in an ultrasonic bath in a clean room. 4-inch diameter p-type boron doped single crystal (100) Si wafers with a thickness of 500 μm were used to fabricate the MOS structure. Deionized water with a resistance of about 18 Mohm was used in the cleaning process. Chemical cleaning operations were performed in an ultrasonic bath. All materials were sterilized on boiling water before being used in MOS production. Thereafter, Using hydrogen peroxide, acetone solution and deionized water, wafers were cleaned. The samples were ultrasonically washed for 5 minutes in a beaker containing methanol, isopropanol, acetone, nitric acid and hydrofluoric acid.

7.3 Fabrication of Al/HfSiO4/p-Si MOS Capacitors

Radio frequency magnetron sputtering sytem is one of the best methods for depositing thin films with lower contamination at lower temperatures, higher deposition rates with lower voltage operation, and higher quality layer growth. So, after surface cleaning, a wafer was loaded in the chamber of the sputter system for deposited the $HfSiO_4$ onto Silikon layer. The sputtering system was depicted in figure 7.1. HfSiO4 target is 4 inch sizes and 99.99% purity. It was used for the deposition of oxide layers. The pressure of the sputtering system chamber was set as follows $4.0x10^{-4}$ Pa.

Figure 7.1. The magnetron DC/RF sputtering system in Nuclear Radiation Detector Center (NURDAM) Abant İzzet Baysal University**.**

then the pre-sputtering were made abouth 3 hours in order to get rid of any impurities on the halfnium target surface at 300 W and commercial sputtering was performed after the pre-sputtering in same parameters for 30 min. Finished the deposition of HfSiO4 oxide layer, the HfSiO4/p-Si films were annealed at 750 C for 40 min in the Nitrogen ambient and the thickness of the film was measured by spectroscopic reflectometer which was found as 300 nm. The spectroscopic reflectometer is shown figure 7.2

After annealing is finished, high-purity aluminum (Al) metal (99.999 %) was deposited by sputtering technique onto the whole back surface of the wafer After this steps ,Schottky contact was also formed by sputtering of Al dots with diameter of about 1.5 mm.

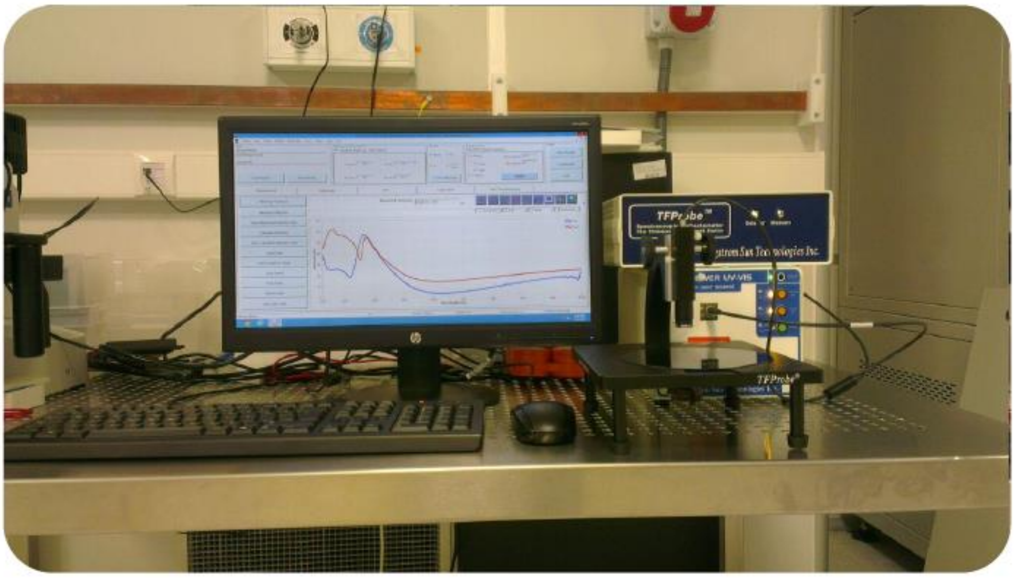


Figure 7.2. The spectroscopic reflectometer in NURDAM

7.4 Measurement Materials and Irradiation of Fabricated Devices

The electrical characterizations were examined by Impedance Analyzer (MODEL HIOKI 3532-50 LCR meter) it is located in Nuclear Radiation Detector Center Abant Izzet Baysal University Fig. 8.3. The capacitance–voltage (C–V) and conductance–voltage (G/ω –V) measurements for fabricated Al/HfSiO4/p-Si (MOS) capacitor were performed at different frequencies of 50, 100, 250, 500 750 kHz and 1 MHz at room temperature before the irradiation of MOS capacitor.

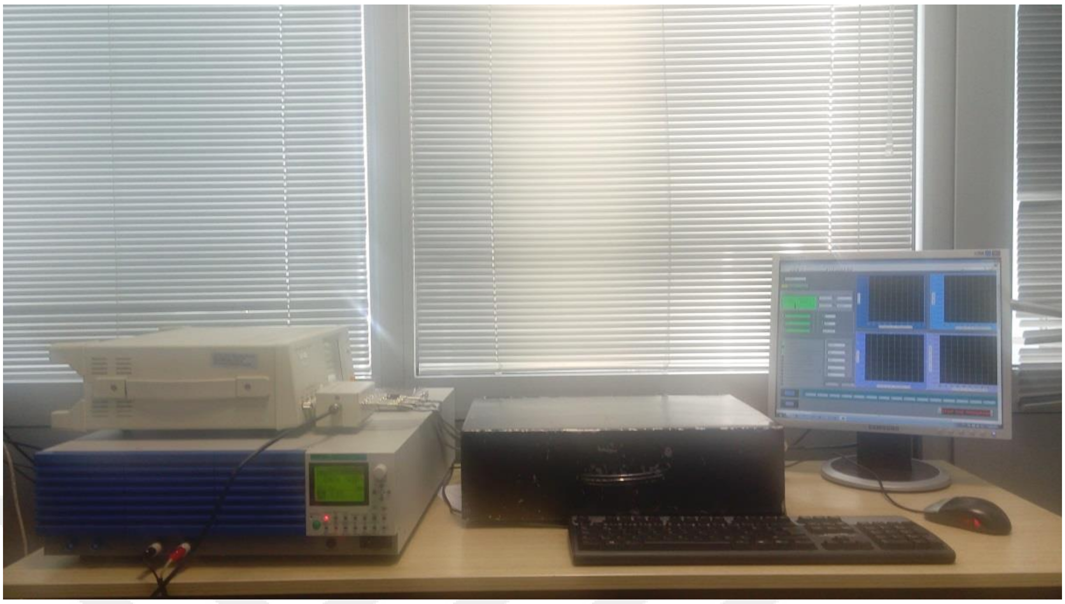


Figure 8.3. Impedance Analyzer (MODEL HIOKI 3532-50 LCR meter)

After the analysis of the measured electrical throughput, the Al/HfSiO4/p-Si MOS capacitor samples were irradiated 2, 4, 6, 12, 36, 70 grays using a Co-60 gamma-ray source at a dose rate of 0,0055 Gy/s. The average energy of the gamma radiation used in this study is 1.25 MeV. The radiation source is placed in the lead shield. The distance between the MOS capacitors fabricated with the radiation source is about 30 cm. The Capacitance and Voltage measurements were performed prior to and after irradiation at high frequency (1 MHz) by using an Impedance Analyzer (MODEL HIOKI 3532-50 LCR meter).

8 EXPERIMENTAL RESULTS AND DISCUSSION

8.1 Results for the Fabricated MOS Capacitors

The capacitance voltage (C –V) and conductance voltage (G/ω –V) measurements were examined for frequency range from 50 kHz to 1 MHz at room temperature to study electrical instability and possible usage of $HfSiO_4$ in MOS based technology. The measured capacitance and voltage characteristics curves of the $HfSiO_4$ MOS capacitors at different frequencies are illustrated in Fig.8.1.

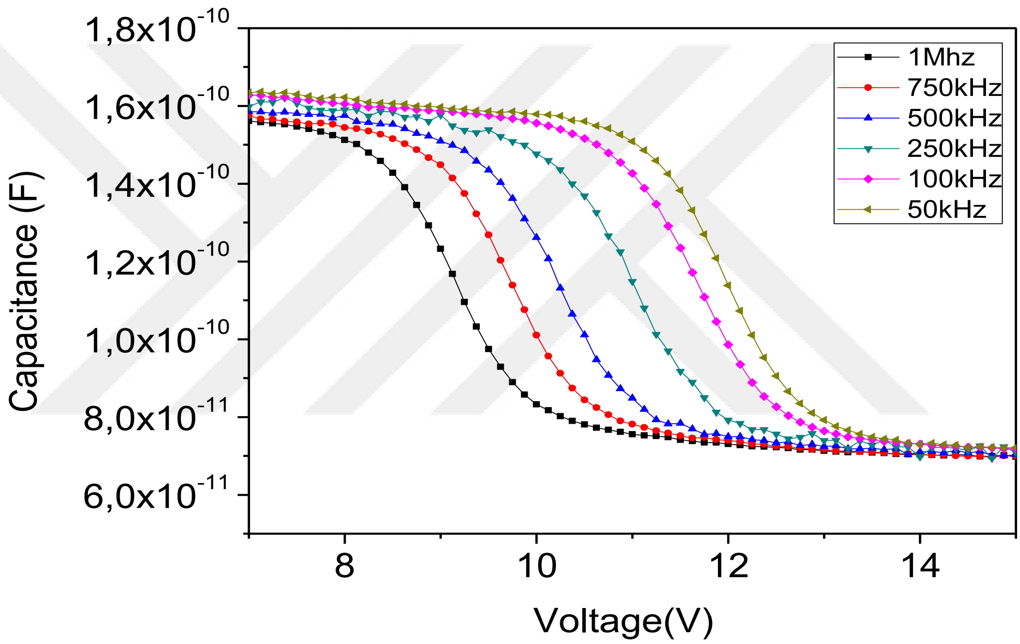


Figure 8.1. C-V characteristic of HfSiO4 MOS Capacitor in various frequencies ranges from 50 kHz and 1 MHz

Each C –V curves shows three regimes of accumulation-depletion-inversion region. It was observed that each capacitance curve is a function of frequency and applied voltage. Especially, Flat band voltages have been observed to be very sensitive to the applied A.C voltage frequency. and it shifted to higher values than ideal one (- 0.55 V) constantly by increasing the frequency. The reason for this behavior can explained to the frequency dependent interface states and border traps localized close the interface between $HfSiO_4$/Si that exchange mobile carriers with Si (Fleetwood, 1996). The contribution of these two trap state influence on the flat band contribution are going to be discussed further in detail.In addition, it can be seen in Fig 8.1, the measured capacitance decreases with increasing voltage frequency.

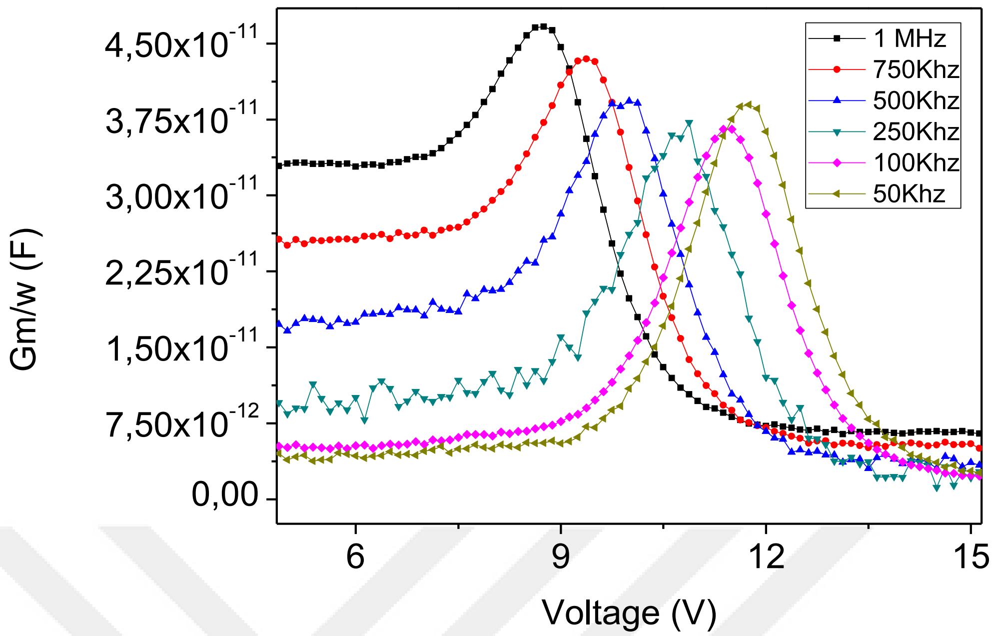


Figure 8.2. Conductance curves for HfSiO4 MOS capacitor for different frequencies

This behavior may be caused by time dependent surface states and interface state. The changing measured capacitance curve characteristics can be explained by the equivalent capacitance circuit (Kimoto, Satoh et al. 2009; Kaya, Lok et al. 2014) observed in Fig 8.3.

In the Fig 8.3 At the lower frequencies (<500 kHz) the effective capacitance C_{LF} expressed as

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_{sc} + (C_{it} / 1 + \omega^2 \tau^2)} \tag{8.1}$$

where C_{ox}, C_{sc}, are the oxide capacitance, space charge capacitance while C_{it} and R_{it} capacitance and resistance associated with the interface traps respectively and ω ($\omega = 2\pi f$) is angular frequency. Interface trap lifetime (τ), which is on the order of 10^{-6}-10^{-7} in the literature, is defined as product of C_{it} and R_{it}. The $\omega\tau$ is very small at lower frequency, i.e., $(\omega\tau)^2$ can be neglected in the Eq.8.1 (Gong, Li et al. 2009; Kahraman, Yilmaz et al. 2015).

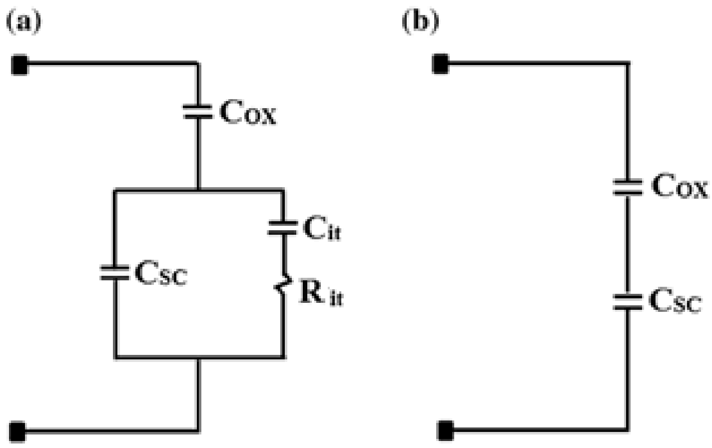


Figure 8.3. Equivalent circuit diagram under a-) low and b-) high frequency regions of MOS capacitors.

This means that if interface trapped charges and defects are easily follow the applied voltage, it can be to yield an excess capacitance at the lower frequencies. On the other hand, interface states can not contributed to the total capacitance at the high frequencies (500 kHz >) (De Carlan, Price et al. 2008; Kimoto, Satoh et al. 2009) since interface states are not as much as fast enough to rearrange in response of the applied voltage excitation by virtue of $\omega\tau > 1$. The effective capacitance represented by C_{HF} is expressed in Eq. 8.2.

$$\frac{1}{C_{HF}} = \left(\frac{1}{C_{ox}} + \frac{1}{C_{sc}} \right) \quad (8.2)$$

when considering the contribution ınterface state of the device characteristics, the C-V curves shows three different regimes in all frequencies which are inversion, depletion and accumulation. In addition to these, C –V curves do not show kinks measured capacitance at all frequencies. The meaning of this is to highlight that there is a low defect and a good interface between the $HfSiO_4$ and p-Si (Mandic, Cindro et al. 2007; Kahraman, Yilmaz et al. 2015; Kaya and Yilmaz, 2015). Moreover, it can be seen in Fig. 8.1 that each Capacitance voltage curves shifted to right side with increasing voltage frequency. The variation in C –V curves may be caused by frequency dependent surface states. The interface states and series resistance are examples of frequency dependent surface states.

The conductance is a very crucial parameter to investigate interface quality of the fabricated devices (Ravotti, Glaser et al. 2007). When a small AC signal is applied to MOS devices, the conductance losses is caused by interaction between interface states and majority carrier densities in the silicon (Kahraman, Yilmaz et al. 2015). Hence, it has been a direct measure of interface states and mobile carriers of Si. Interface traps somewhere near the band edge can easily intercept and release carriers under different gate voltage influencing the charge and field distribution caused with different curves ideal behavior of MOS devices. Frequency dependent measured conductance is illusrated in Fig.8.2. The measured conductance curves increase by increasing applied voltage frequencies, except at 50 kHz. In addition, measured G/ ω –V curves peaks move toward higher voltages with decreasing frequency. Possible reasons for this behavior may be related to the relaxation time of trap states, series resistance, interfacial dielectric layer and the density of state (Ravotti, Glaser et al. 2007).

Serial resistance corrections have been applied to device specifications to remove potential noise effects in device characteristics. The measured admittance, Yma, at strong accumulation of the MOS structure using the parallel RC circuit is equivalent to the total circuit admittance (Nicollian and Brews, 1982; Gong, Li et al. 2007).

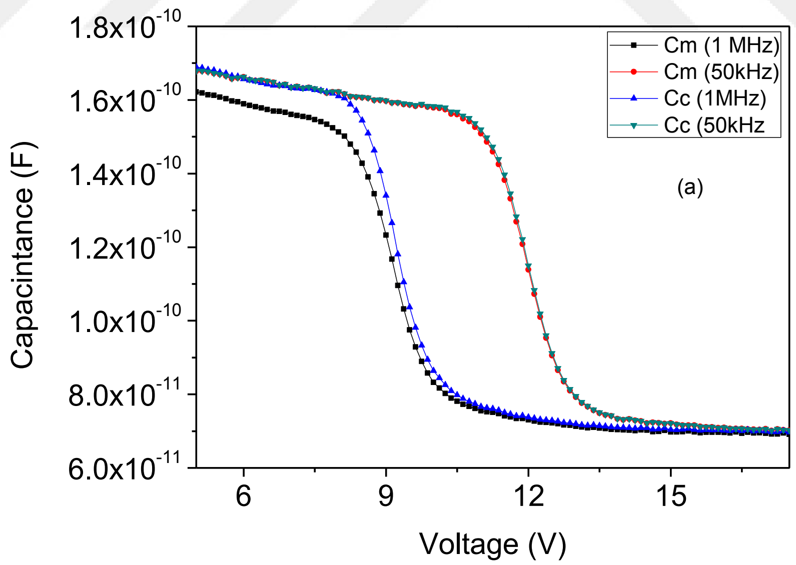
$$Y_{ma} = G_{ma} + j\omega C_{ma} \tag{8.3}$$

Comparing the real and imaginary part of the impedance, the series resistance is given by Eqs 5.17 (Kaya, Yilmaz et al. 2015).

The R_s values of the Halfnium Silicate MOS capacitor were calculated and tabulated 7.1. It has been observed that the series resistance values decreased with increasing applied frequency.These behaviors may be releted with by re-contraction and re-ordering of defect sites under frequency dispersion

(Lipovetzky, Redin et al. 2007; Kaya, Lok et al. 2014; Kaya and Yilmaz, 2015). In order to remove series resistance effect from the G-V, G/ ω –V curves, the correction of capacitance and conductance characteristic can be calculated by Eqs. 7.19 and 7.15

The characteristics of the measured device, to compare the corrected capacitance and conductance curves are shown in Figures 8.4 (a) - (d). As seen in Figs. 8.4 (a) and (c), the series resistance (R_s) deviates from the device characteristics, especially, for high frequency measurements. However, The corrected conductance deviated from original ones. the corrected capacitance did not deviate from the originals. The measured conductance curves almost increase with increasing frequency while they decrease constantly after correction was performed. This behavior is expected as indicated in the literature (Tataroglu and Altindal, 2008; Xiao and Huang 2010; Kaya and Yilmaz, 2015). Series resistance effect masked the device characteristics. This indicates that it is an important parameter and elimination must be done before detailed electrical analysis.



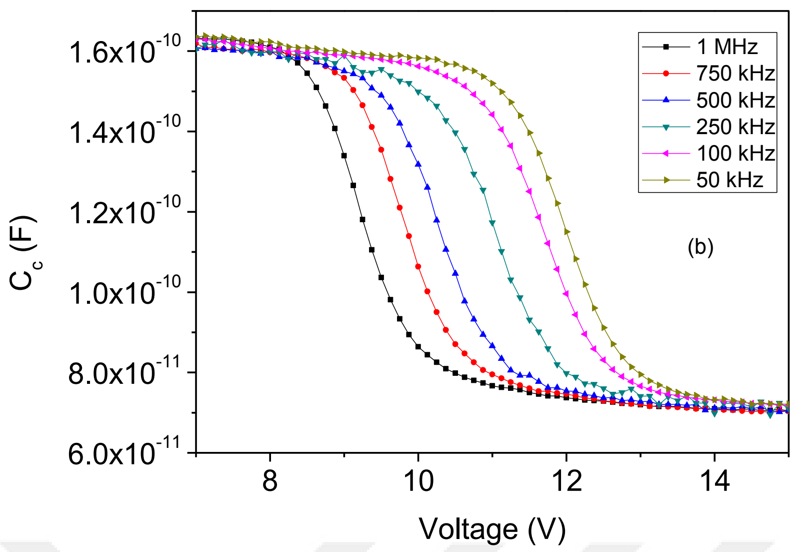
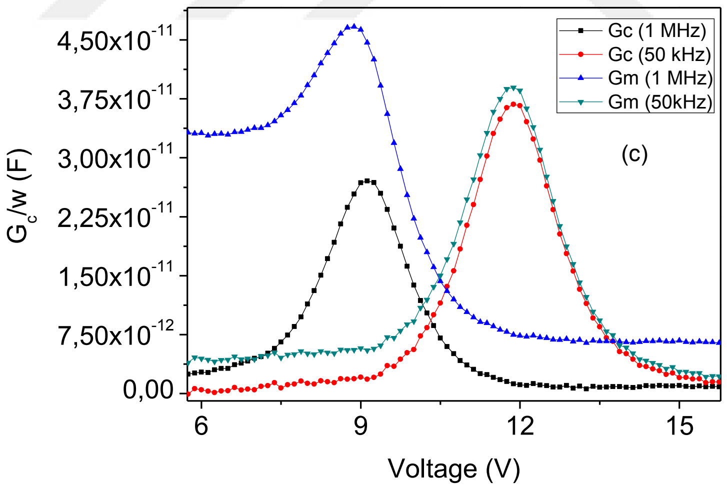


Figure 8.4. Variations on the (a) corrected and measured capacitance for 50 kHz and 1 MHz frequencies, (b) corrected capacitance for various frequencies between 50 kHz and 1 MHz,



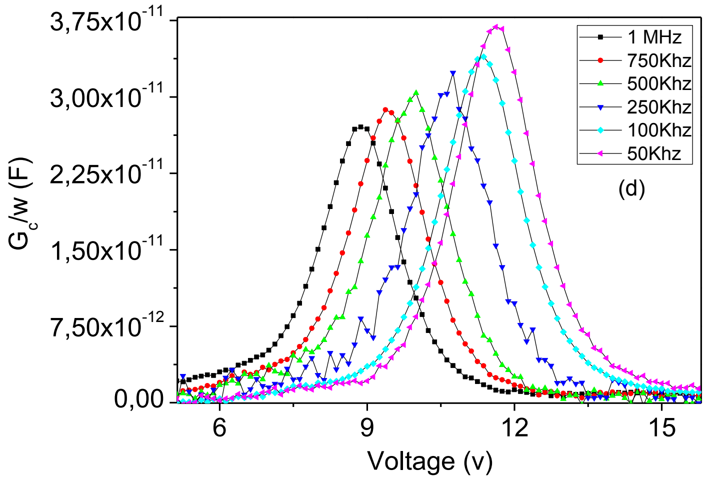


Figure 8.4. (c) corrected and measured conductance for 50 kHz and 1 MHz, (d) corrected conductance for various frequencies between 50 kHz and 1 MHz

Density state of interface state (D_{it}) which is crucial parameter affecting capacitance and voltage characteristic can be found using equation 8.4 (Mahajan, Khairnar et al. 2014).

$$D_{it} = \frac{2}{Aq} \frac{G_{c,\max} / \omega}{\left(G_{c,\max} / \omega C_{ox}\right)^2 + (1 - C_c / C_{ox})^2} \tag{8.4}$$

where, A,q are the front area of the MOS capacitor, the elementary charge respectively C_{ox} is the oxide capacitance whose value is 3.59x10^{-9} F, $G_{c,max}$ /w is peak value of corrected $G_{c,max}$ /w-V curve, C_c is corrected capacitance of the MOS corresponding to $G_{c,max}$ /w. Some required values and calculated density of state values are given Table 8.1 and 8.2.

Table 8.1. Various calculated frequency-dependent electrical parameters for HfSiO4 MOS capacitors

Frequency (kHz)	R_s (Ohm)	$G_{c,max}$ ($x10^{-11}$)	C_c ($x10^{-11}$)	D_{it} ($x10^{10}eV^{-1}$ cm^{-2})	N_{bt} ($x10^{11}cm^{-2}$)
50	460	2.68	1.50	10.00	5.81
100	285	2.55	1.49	8.92	4.62
250	215	3.01	1.36	8.36	5.49
500	200	3.22	1.25	7.91	5.85
750	193	3.36	1.30	7.66	5.44
1000	183	3.67	1.50	7.30	5.40

Table 8.2. Barrier potentials and related electrical parameters under frequency dispersion of HfSiO4 MOS Capacitors

Frequency (kHz)	V_D (eV)	N_d ($x10^{15}cm^{-3}$)	E_F eV	$\Delta\ \Phi_B$ (meV)	Φ_B (eV)
50	10.90	2.34	0.241	32.9	10.70
100	10.60	2.26	0.242	32.4	10.30
250	10.00	2.31	0.241	32.1	9.76
500	9.24	2.43	0.240	31.9	8.96
750	8.71	2.58	0.238	31.8	8.44
1000	8.08	2.71	0.237	31.5	8.04

Frequency dependent interface state density under frequency dispersion is also depicted in Fig 8.5.

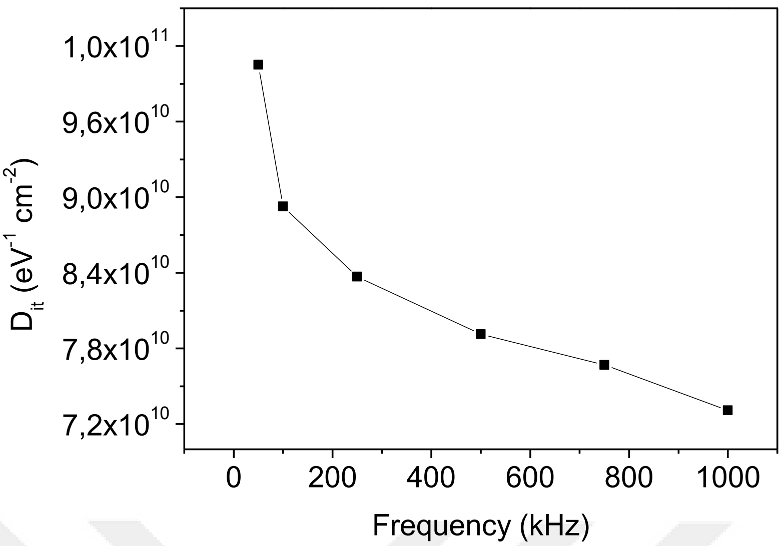


Figure 8.5. Variations of Dit as a function voltage for HfSiO4 MOS capacitor

The D_{it} values decrease with increasing applied voltage frequency as expected (Jaksic, Kimoto et al. 2006; Haran, Murat et al. 2007) and the order of D_{it} approximately was calculated as 10^{11} cm^{-2}. The calculated values are higher than the values of MOS devices with conventional SiO2 dielectric layer.But, It is the same rank with reported in other promising dielectric. (Shahjahan, Takahashi et al. 2002; Tirmali, Khairnar et al. 2011; Panda and Tseng, 2013, Kaya and Yilmaz, 2015). Since the D_{it} values are in expected order, the abnormal changes of the V_{fb} under frequency dispersions probably were caused by border states. In order to calculate the border state density, the capacitance hysteresis were measured and then corrected. The corrected capacitance hysteresis curve is depicted in Fig. 8.6 for 1 MHz and 50 kHz.

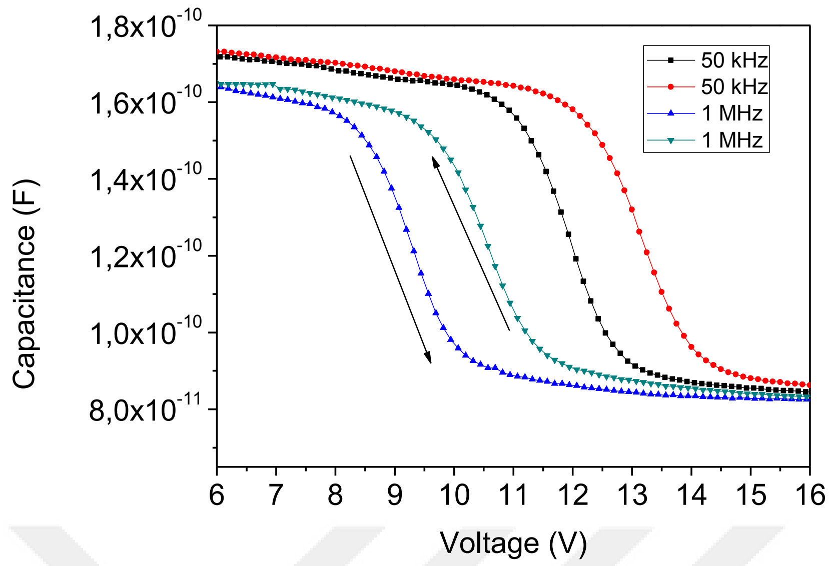


Figure 8.6. Hysteresis C–V characteristics Halfnium Silicate MOS capacitor for 1 MHz and 50 kHz

Assuming the total contribution interface states almost zero for flat band shift in hysteresis (Verrelli, Galanopoulos et al. 2010; Nedev, Manolov et al. 2012), Using the hysteresis curve obtained from flat band voltage shift (ΔV_{fb}) and the border state density (N_{bt}) in oxide layers were approximately calculated by following equation

$$N_{bt} = \frac{(C_{acc} \bullet \Delta V_{FB})}{qA} \tag{8.5}$$

The usual N_{bt} values are in the order of 10^{10} cm^{-2} for the real MOS devices. But, for the $HfSiO_4$ MOS capacitors, it is in the order of 10^{11}. Hence, the abnormal frequency variations on the flat band voltages of the devices may be attributed to the frequency dependent border states. Moreover, the observed hysteresis is counter-clockwise, which clearly demonstrates a greater reduction in acceptor-like border traps. Thus, the donor-like border traps play the dominant role (Briere, Beddar et al. 2005; Makowski, Grecki et al. 2006).

The intercept of C_c^{-2} versus V is plotted in Fig 8.7. It was demosrated that the linearity of the obtained $C_c^{-2} - V$ curves indicates the uniform distribution of interface states in the devices structure. The relation between C_c^{-2} and V can be expressed as in the following equation (Jaksic, Rodgers et al. 2006; Zeyrek, Turan et al. 2013).

$$C_c^{-2} = \frac{2(V_0 + V)}{\varepsilon_s \varepsilon_0 q A^2 N_d} \tag{8.6}$$

where V_0 is the applied voltage and V_0 $(=V_D - kT/q)$ is the intercept of the C_c^{-2} versus V plot with the voltage axis at various frequencies from 50 kHz to 1 MHz, ε_s, ε_0 and N_d are relative permittivity of Si, the permittivity of free space and doping concentration obtained from the slope of C_c^{-2} versus V characteristics respecrively.

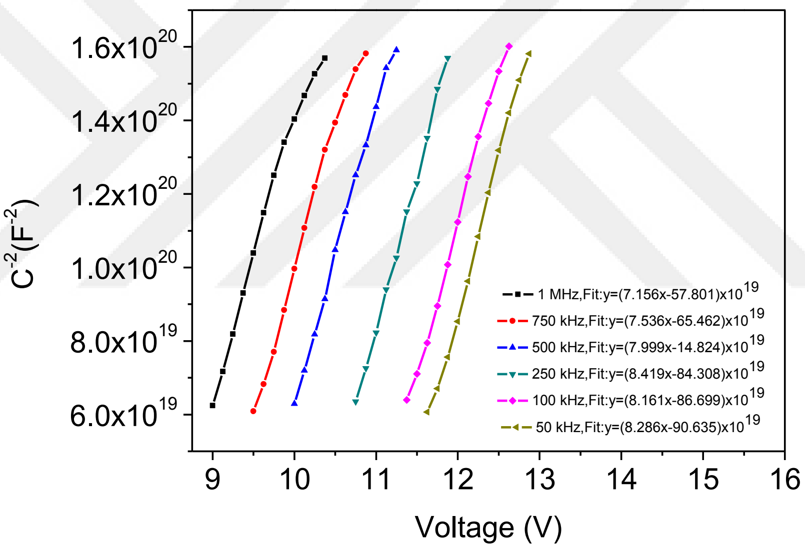


Figure 8.7. C^{-2} - V characteristics and corresponding linear fit function of Halfnium Silicate MOS capacitors at various frequencies from 50 kHz and 1 MHz

The barrier potentials values (Φ_B) can be obtained from the equation 8.7

$$\phi_B = V_0 + \frac{kT}{q} + E_F - \Delta\phi_B = V_D + \frac{kT}{q}\ln\left(\frac{N_c}{N_d}\right) - \Delta\phi_B \tag{8.7}$$

where E_F ,N_c are the energy difference between the valance band edge and bulk Fermi level , the effective density of state in conduction band respectively. Barrier potential, $\Delta\phi_B$, can be calculated from the following equation.

$$\Delta\phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}} \quad (8.8)$$

where E_m is the max electric field. Calculated electrical characteristic are tabulated in Tables 8.1 and 8.2. Diffusion potentials are located at the positive voltage since the negative charges are trapped in the MOS structure by virtue of the fabrication process. Furthermore, When applied voltage frequency increases, The doping concentration are decreased because of increase in the slope of C_c^{-2} versus V plot. As the data in Table 8.2. show E_f decreased with increasing in frequency except at 50 kHz. When increasing frequency,the diffusion of charge carriers from interface defects decreased So, the position of the Fermi level can be changed a little with the applied voltage (Yahia, Fadel et al. 2012; Kaya and Yilmaz 2015). Moreover, V_D and $\Delta\phi_B$ decreased with increasing applied voltage. This may depend on the presence of the interface layer $HfSiO_4$, especially, time dependent interface state at the $HfSiO_4$/Si interface. Otherwise, the Φ_B values varied from 10.7 to 8.04 V depending on the charge accumulations due to time dependent trap sites.

8.2 Results for Irradiated MOS Capacitors

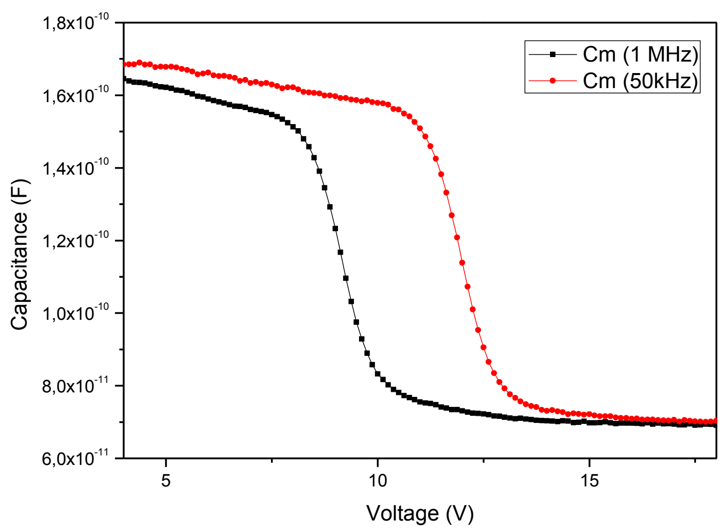


Figure 8.8. The capacitance – voltage characteristics of Al/HfSiO4/p-Si/Al capacitors measured at high (1 MHz) and low (50 kHz) frequencies.

The initial interface trap density (N_{it}) which varies by the fabrication process is a crucial parameter to specify device compatibility for microelectronics. Hence, we firstly calculated the initial interface trap density before the irradiation response of the $HfSiO_4$ dielectric. Several methods have been used to calculate the N_{it} of the conventional MOS capacitors (Nicollian and Brews 2003, Yilmaz, Dogan et al. 2008, Ergin, Turan et al. 2010, Kaya, Aktag et al. 2014, Tecimer, Uslu et al. 2014). Among them, the high and low frequency capacitance method is accurate and easiest one to calculate N_{it}. Hence, capacitance characteristics of the Al/$HfSiO_4$/p-Si/Al capacitors measured at high (1 MHz) and low (50 kHz) frequencies and results are shown in Fig.8.8. It is seen that the capacitance curve shifts to more positive voltage in low frequency measurement due to time dependent charges. In addition, the N_{it} was determined by the following equation.

$$qAN_s = N_{it} = \left(\frac{1}{C_{HF} - C_{OX}}\right)^{-1} - \left(\frac{1}{C_{LF} - C_{OX}}\right)^{-1} \quad (8.9)$$

where CHF and C_{LF} are high and low frequency capacitance, respectively. A is the capacitor area, C_{ox} the is oxide capacitance whose value is $1{,}04\text{x}10^{-9}$. Using Eq. 1, the N_{it} value was found as $9{,}91\text{x}10^{-11}$ $eV^{-1}cm^{-2}$. This calculated N_{it} value is in accord with reported electrical characteristics for the MOS based technology (Castagne and Vapaille, 1971; Dokme and Altindal, 2007).

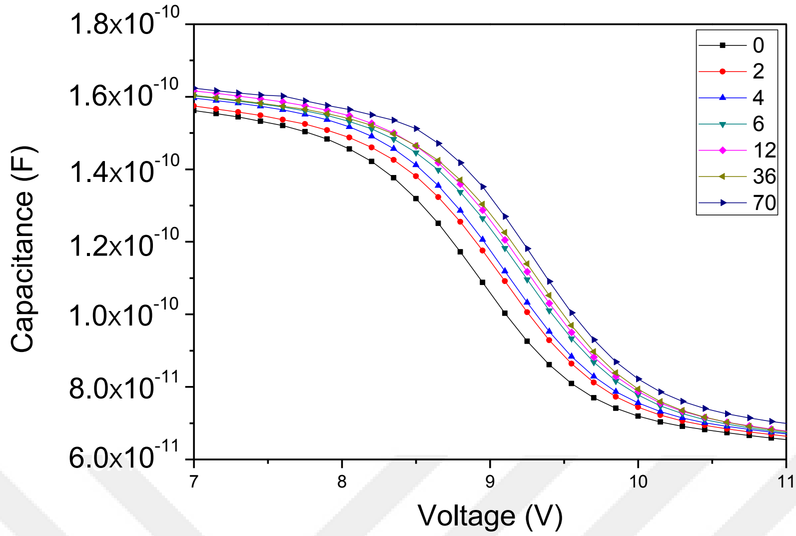


Figure 8.9. C–V curves of HfSiO4 MOS capacitor before and after gamma irradiation at

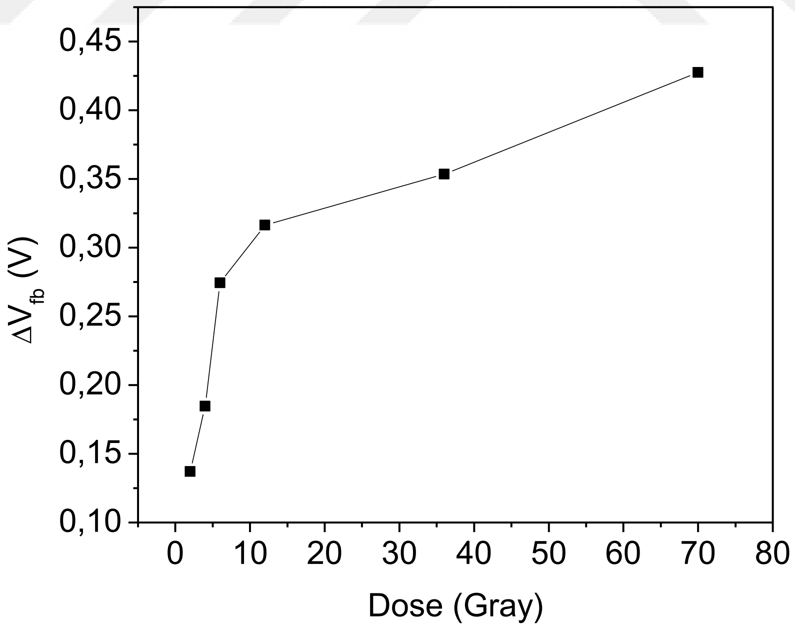


Figure 8.10. Flat band voltage shift of HfSiO4 MOS capacitor from 2 to 70 Gray.

Ionizing radiation may create defects which are interface traps and the oxide traps in the metal oxide semiconductor devices. These defects affect electrical characteristics of the MOS based devices (Kaya and Yilmaz, 2014). The ionizing radiation gives rise to shift in the position of the flat band voltage of the C–V curve along the voltage axis due to variation of total trapped charge density generated by irradiation (Yilmaz, Kaleli et al. 2007). The conventional capacitance- voltage characteristics of devices are delicate tools to investigate the irradiation effects on the electrical characteristics of the MOS based devices. Thanks to the flat band and mid gap voltage shift, change of interface trapped charge density and change of the oxide-trapped charge densities can be determined. Hence, after exposing to different levels of the gamma-radiation dose, the capacitance–voltage (C–V) characteristics of the Al/$HfSiO_4$/p-Si/Al capacitors were measured at considerable high frequency (1 MHz) to eliminate contribution of the parasitic effects of the interface state in the measured capacitance. The measured C–V curves of the Al/$HfSiO_4$/p-Si/Al capacitors before and after the gamma-irradiation are depicted, respectively, in Fig. 8.9. We have observed that, the C–V characteristics of the Al/$HfSiO_4$/p-Si/Al capacitors shift toward more positive voltages with increasing the radiation dose. During the irradiation process, enormous numbers of electron and hole pairs are generated in oxide layer. Some of these charges, which escaped from the initial recombination, were trapped by defects in the oxide layer and oxide/semiconductor interface (Kaya and Yilmaz, 2014). Depending on the sing of the trapped charges, flat band voltage can shift to either right or left.

The electrons are much more mobile than the holes. So, most probably expected result is that the positive charges are trapped in the device structure leading to negative flat band/ midgap voltage shift (Knoll, 2000). In contradistinction to this, the C–V characteristics of the Al/HfSiO4/p-Si (MOS) capacitors show that flatband and mid gap voltages shift toward positive values. This indicates the negative charges are trapped in the devices structure of the Al/$HfSiO_4$/p-Si (MOS) capacitor. On the other hand, capacitance values slightly increase with increasing radiation dose as seen in Fig 8.9. There are two possible reasons which affect the increased capacitance. The first possible reason can be the contribution of generated interface states to measured capacitance. If the generated interface states lifetime is higher than the applied voltage frequency they can follow the applied voltage signal. Hence, they can act as an additional capacitance to measured capacitance (Tataroglu and Altindal, 2006; Kaya, Yilmaz et al. 2015). The second reason might be that the radiation may passivate the trap densities in the device. This leads to rise in the capacitance characteristics (Ma, 1989).

In addition, the flat band voltage shift with respect to the given doses gives the sensitivity of the dielectric layer, which is also important knowledge for the usability of the MOS based devices in the radiation environment either as a dosimetric purpose or as resistive materials to irradiation. Therefore, the flat band voltage changes with respect to the given dose curves of the Al/$HfSiO_4$/p-Si/Al capacitors as shown in Fig 8.10. The response of these devices shows linearity from 2 to 12 Gy. But, the linearity is degraded after 12 Gy. Additionally, it was also observed that the flat band voltage shift is very small for the Al/$HfSiO_4$/p-Si/Al capacitors compared to SiO_2 based devices (Felix, Fleetwood et al. 2002). The sensitivity of devices obtained from the flat band voltage shift is 4.41 mV/Gy for 300 nm thick Al/$HfSiO_4$/p-Si/Al capacitors. This value is 41 mV/Gy for non-biasing 400 nm-thick SiO_2 (Pejovic, 2015). The sensitivity for the SiO_2 layer is proportional to square of the oxide thickness (Pejovic, 2015). Hence, the sensitivity of SiO_2 layer, having 300 nm that is the same gate oxide thickness as studied Al/HfSiO4/p-Si/Al capacitors, is nearly 28 mV/Gy. Comparing these values, it is seen that $HfSiO_4$ dielectrics approximately 6.5 times insensitive than conventional SiO_2 layer. Consequently, Al/$HfSiO_4$/p-Si/Al capacitors does not give good linearity and it is relatively insensitive to used MOS based radiation measurement devices, such as RadFETs etc. However, although it has acceptable capacitance rise up on irradiation, it may have important usage as radiation hard materials.

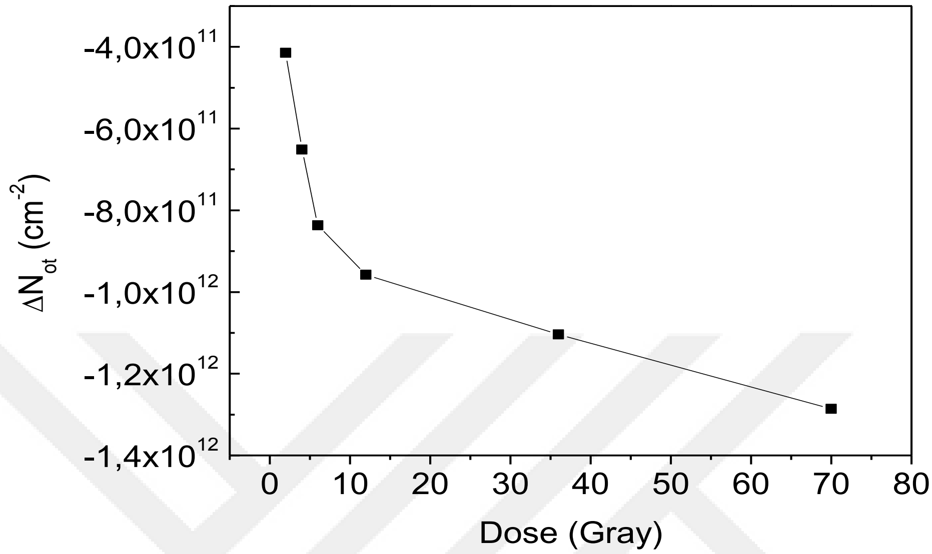


Figure 8.11. Radiation induced oxide trap density, ΔNot, of Al/HfSiO4/p-Si/Al capacitors

The radiation induced trapped charges in the oxide (ΔN_{ot}) were determined from the mid-gap voltage shifts due to the interface states which are expected to be neutral at mid-gap level and would not contribute to the mid-gap voltage shift. The ΔN_{ot} densities can be calculated by the following equation

$$\Delta Not = -\frac{C_{ox}\,\Delta V_{mg}}{qA} \qquad (8.11)$$

where, C_{ox} is the oxide capacitance with value of $1,04x10^{-9}$ F, q = ($1.602x10^{-19}$ C) is electric charge, A is the capacitor area and ΔV_{mg} is the midgap voltage changes. From Eq. 8.11, ΔN_{ot} was calculated to be nearly $4.075x10^{11}$ cm^{-2} for exposed 2 Gy, and $1.282x10^{12}$ cm^{-2} after the exposed 70 Gy respectively.

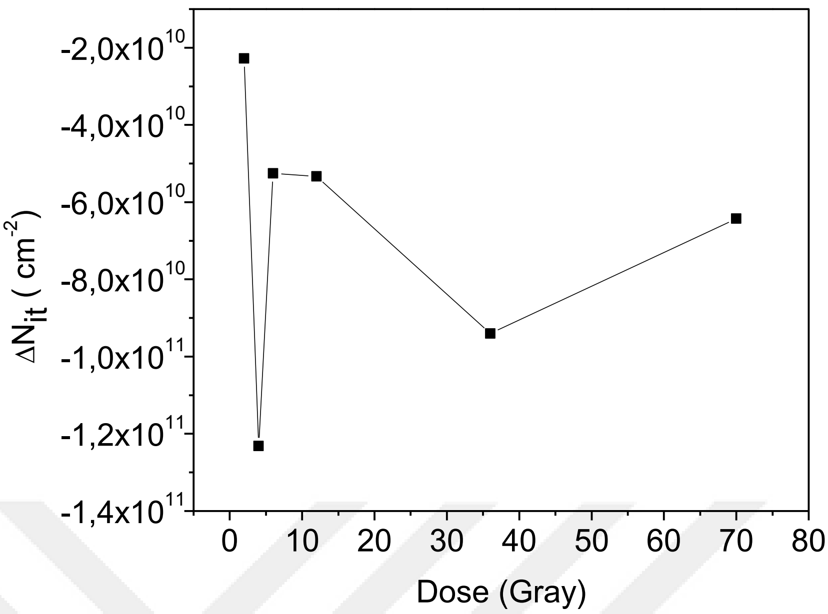


Figure 8.12 Radiation induced interface trap density, ΔNit, of Al/HfSiO4/p-Si/Al capacitors

The radiation induced interface trap density (ΔN_{it}) was calculated through following equation,

$$\Delta N_{it} = -\frac{C_{ox}\,(\Delta V_{fb} - \Delta V_{mg})}{qA} \quad (8.12)$$

where C_{ox} is the oxide capacitance, q is electric charge, and A is the capacitor area. ΔN_{it} is approximately $7.055\text{x}10^{10}$ cm^{-2}, $6.41\text{x}10^{10} cm^{-2}$ after the radiation 2 and 70 grays respectively for $HfSiO_4$ MOS capacitor.

The distribution of calculated ΔN_{ot} and ΔN_{it} values of the Al/$HfSiO_4$/p-Si/Al capacitors are shown in Figs. 8.11 and 8.12. Comparing these two figures, each shows different behaviors. It can be seen in Fig. 8.11 that there is almost linearly an increase from 2 to 12 Gy for the ΔN_{ot}. This means that the ΔN_{ot} in the oxide layer increased. On the other hand, density of interface state response is very confusing. When the Al/$HfSiO_4$/p-Si/Al capacitor was irradiated first time for 2 Gy, density of the interface state increased, dramatically. The first response might have been with a splash of radiation. After that, it is decreased from 2 to 4 and 36 to 70 Gy. This behavior may be related to passivation. The passivation of the dielectric layer shows different behavior for different exposed doses (Kaya and Yilmaz, 2014). So, the behavior of interface state density is attributed to the passivation of the dielectric/semiconductor interfaces. In addition, these results have demonstrated that the total charge (oxide trapped and interface trapped charges) is enhanced in the device structure due to irradiation effects explained herein before. However, the calculated charge densities are still in order of 10^{11}-10^{12} cm^{-2}. These values are still are acceptable for the MOS devices used in the microelectronic.

9 CONCLUSION

In summary, the electrical characteristics and radiation response of Al/$HfSiO_4$/p-Si MOS capacitor have been investigated at the room temperature. According to the electrical results of the study, the capacitance and conductance are sensitive to applied voltage frequency due to frequency dependent charges, e.g., interface states, border traps, and series resistance. Seri resistance decreases with increasing applied voltage frequency and the series resistance corrections must have been performed before detailed electrical analysis to obtain accurate results. The calculated D_{it} values were found to be in the order of 10^{10} $eV^{-1}.cm^{-2}$, which is in good agreement with other reported dielectric layer for MOS based technology. In addition, high sensitivity of the V_{fb} voltage variations was attributed to the interface states, especially, time dependent border states. On the other hand, it is observed that barrier potential values are also sensitive to the applied voltage frequencies. However, its values are expectable for elimination of leak charge injection from the substrate into the dielectric and thus the tunneling effect does not significantly occur. In conclusion, fabricated $HfSiO_4$ dielectric layer exhibits demanding electrical characteristics to be used in MOS- based technologies.

The effects of gamma-ray irradiation on the Al/$HfSiO_4$/p-Si/Al capacitors have been analyzed. The initial interface strap density caused by fabrication was found to be $9{,}91x10^{-11}$ $eV^{-1}cm^{-2}$ by using HF-LF capacitance method which is suitable for MOS based devices. It was observed that irradiation slightly raises the capacitance characteristics of device and also cause the flat band voltages shift toward more positive voltages due to electron trapping on the device structure. In addition, the numbers of oxide trap charges are generated much more than interface trap charges. So, the oxide trap charges are more effective comparing to the interface trap charges for the flat band voltage shift in the $HfSiO_4$. Comparing the changes of electrical characteristics of the Al/$HfSiO_4$/p-Si/Al capacitors with conventional SiO_2 based devices, it has seen that $HfSiO_4$ based devices are more insensitive to irradiation. Hence, one may conclude that hafnium silicate can be a good radiation-hardened dielectric material in the future applications where high irradiation field exist such as nuclear reactors and space.

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