THE DESIGN AND TRANSPORT PROPERTIES OF NANO-DEVICES BASED ON TWO-DIMENSIONAL SEMICONDUCTORS

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By

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The design and transport properties of nano-devices based on two-dimensional semiconductors
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We certify that we have read this dissertation and that in our opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

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ABSTRACT

THE DESIGN AND TRANSPORT PROPERTIES OF NANO-DEVICES BASED ON TWO-DIMENSIONAL SEMICONDUCTORS

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Ph.D. in Materials Science and Nanotechnology
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As the semiconductor industry approaches the fundamental physical and electrostatic limits of traditional silicon-based transistors, the transition toward atomically thin channel materials has become imperative to sustain technological scaling. This thesis presents a proof-of-concept study on the design and transport properties of nano-devices based on two-dimensional (2D) semiconductors by evaluating their feasibility as a modular platform for next-generation nanoelectronics. Utilizing a comprehensive first-principles and quantum transport-based computational methodology that combines Density Functional Theory (DFT) with the Non-Equilibrium Green's Function (NEGF) formalism, the research systematically evaluates device performance under the ballistic transport limit.

This investigation starts with Metal-Semiconductor-Metal (MSM) systems to clarify how channel length and electrode doping govern current flow at nanometer scales. The analysis then advances to p-n junctions to capture the influence of built-in electrostatics on tunneling-driven rectification. The study is followed by p-i-n field-effect transistors as intermediate architectures where gate electrodes serve as active control elements. Finally, the study is finalized with the assessment of MOSFET architectures where the integrated effects of contacts, channel transport and electrostatic control are evaluated within a unified device concept.

It is evaluated that architectural optimization is as critical as material selection in the deeply scaled 2D regime. In particular, underlap engineering is identified as a practical instrument to tune source and drain electrostatics and screen drain-induced field penetration without altering the intrinsic channel material. The results demonstrate that incorporating such optimized geometries significantly boosts on-state currents and improves energy efficiency. Furthermore,

these improvements enable devices to meet or surpass ITRS-2028 high-performance targets. Ultimately, this thesis presents prototype devices that demonstrate the extraordinary potential of 2D semiconductors for high-performance transistor operation when their atomically thin nature is paired with precise electrostatic engineering.

Keywords: Non-Equilibrium Green's Function (NEGF), Ballistic Transport, High-performance Nanoelectronic Devices, 2D Semiconductors, Density Functional Theory (DFT).

ÖZET

İKİ-BOYUTLU YARI İLETKENLERE DAYALI NANO-CİHAZLARIN TASARIMI VE TAŞIMA ÖZELLİKLERİ

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Yarı iletken endüstrisi, geleneksel silikon tabanlı transistörlerin temel fiziksel ve elektrostatik sınırlarına yaklaşırken, teknolojik ölçeklemeyi sürdürebilmek için atomik kalınlıkta kanal malzemelerine geçiş zorunlu hale gelmiştir. Bu tez, iki boyutlu (2B) yarı iletkenlere dayalı nano-aygıtların tasarımı ve taşınım özelliklerine yönelik bir kavram kanıtlama (proof-of-concept) çalışması sunmakta ve bu aygıtların yeni nesil nanoelektronik için modüler bir platform olarak uygulanabilirliğini değerlendirmektedir. Yoğunluk Fonksiyonel Teorisi (DFT) ile Denge Dışı Green Fonksiyonu (NEGF) formalizmini birleştiren kapsamlı, birinci ilkeler ve kuantum taşınım temelli hesaplamalı bir yöntem kullanılarak, aygıt performansı balistik taşınım sınırında sistematik biçimde incelenmiştir.

Bu inceleme, nanometre ölçeklerinde kanal uzunluğu ve elektrot katkılamasının akım akışını nasıl belirlediğini açıklığa kavuşturmak amacıyla Metal-Yarı İletken-Metal (MSM) sistemleriyle başlar. Analiz daha sonra, yerleşik elektrostatik potansiyelin tünellemeye dayalı doğrultma üzerindeki etkisini yakalamak için p-n eklemlerine ilerler. Çalışma, kapı elektrotlarının etkin kontrol elemanları olarak görev yaptığı ara mimariler olan p-i-n alan etkili transistörlerle sürdürülür. Son olarak, kontakların, kanal taşınımının ve elektrostatik kontrolün bütünleşik etkilerinin tek bir aygıt kavramı içinde değerlendirildiği MOSFET mimarilerinin incelenmesiyle çalışma tamamlanır.

Derin ölçeklenmiş 2B rejimde mimari optimizasyonun, malzeme seçimi kadar kritik olduğu sonucuna varılmaktadır. Özellikle, kanal malzemesinin içsel özelliklerini değiştirmeden kaynak (source) ve dren (drain) elektrostatiklerini ayarlamak ve drenden kaynaklanan alanın kanala nüfuzunu perdelemek için underlap mühendisliği pratik bir araç olarak belirlenmiştir. Sonuçlar, bu tür optimize

edilmiş geometrilerin dahil edilmesinin iletim (on) durum akımlarını belirgin biçimde artırdığını ve enerji verimliliğini iyileştirdiğini göstermektedir. Ayrıca, bu iyileştirmeler aygıtların ITRS-2028 yüksek performans hedeflerini karşılamasını veya aşmasını mümkün kılmaktadır. Sonuç olarak, bu tez, atomik incelikteki yapılarının hassas elektrostatik mühendislikle birleştirilmesiyle, 2B yarı iletkenlerin yüksek performanslı transistör çalışması için olağanüstü potansiyelini gösteren prototip cihazlar sunmaktadır.

Anahtar sözcükler: Denge Dışı Green Fonksiyonu (NEGF), Balistik Taşınım, Yüksek Performanslı Nanoelektronik Aygıtlar, İki Boyutlu (2B) Yarı İletkenler, Yoğunluk Fonksiyonel Teorisi (DFT).

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In the words of Steve Jobs, "You can't connect the dots looking forward; you can only connect them looking backwards. So you have to trust that the dots will somehow connect in your future." In this same spirit, I recall the day I wrote the very first email to my advisor, Engin Durgun, almost seven years ago. I had no idea at the time how that decision would shape my life. Looking back on all the days and long nights at UNAM, connecting these precious dots creates a picture whose details will be remembered with endless gratitude. I am thankful for his vision, expertise, and perspective, which have been instrumental in shaping this research and my development as a scientist. Throughout these years, he was not only an advisor who dealt exclusively with research but also an inspiring role model who demonstrated how to approach the difficult challenges of life with patience and grace. Every step of this journey was fruitful. It was a privilege, Hocam.

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To my mother,

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Ord. Prof. Dr. Cahit Arf
Atatürk University
1958

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Chapter 1

Introduction

1.1 Background and Context

1.1.1 From Vacuum Tubes to the Solid-State Era

The trajectory of human civilization in the 20th and 21st centuries has been unavoidably linked to the capacity to manipulate electron transport. This capability was initially realized through the bulky and thermally inefficient vacuum tubes. The first vacuum tube as a practical rectifying diode was invented and patented by John Ambrose Fleming in 1904 and transformed into amplifying elements by Lee de Forest's triode in 1906 [3]. These two advancements are considered the groundwork for the first generation of computing machines. However, their large size, high power consumption, and heat generation imposed severe practical limits on circuit complexity and operating stability. For the next stage of electronic technologies, miniaturization and integration of these devices were essential. The resolution to this complication was found as the point-contact semiconductor amplifier in polycrystalline germanium by John Bardeen and Walter Brattain when they worked under William Shockley in 1947 at Bell Laboratories [4, 5]. It was the precursor to the Bipolar Junction Transistor (BJT) and marked the

transition from thermionic emission in vacuum to minority carrier injection in solids. Hence, the solid-state era was initiated.

Although BJTs represented a major advance and enabled the earliest integrated circuits, their operation requires a continuous base current to regulate the collector current. That requirement introduced static power consumption and ultimately constrained scalability toward highly integrated systems. To overcome that, Dawon Kahng and Mohamed Atalla from Bell Labs demonstrated the metal–oxide–semiconductor field-effect transistor (MOSFET) [6]. The MOSFET introduced a voltage-controlled switch using a capacitive gate structure and theoretically drew zero static current. In spite of the fact that early MOSFETs were 100 times slower than contemporary BJTs, that approach effectively solved static power consumption issues. Additionally, due to their planar geometry, MOSFETs were inherently scalable and enabled the complementary MOS (CMOS) logic that supports the modern digital world [7].

1.1.2 Moore's Law and the Dennard's Scaling Era

The rapid industrial scaling of MOSFETs was reflected in Gordon Moore's 1965 observation [8] that the number of components on an integrated circuit roughly doubled each year. This observation is codified as Moore's Law and became a self-fulfilling prophecy that drives investment and innovation cycles in the semiconductor industry for more than five decades. The main mechanism behind this exponential growth was formulated as Dennard scaling and it is introduced by Robert Dennard in 1974 [9]. Dennard's scaling rules postulated that if the physical dimensions of a MOSFET (channel length L, width W, oxide thickness t_{ox}) and the supply voltage (V_{DD}) were reduced by a dimensionless factor κ (where $\kappa > 1$), the internal electric fields would remain constant. Consequently, the power density would remain invariant while the switching speed increased by κ and the device area decreased by κ^2. In other words, these quantities would be reduced to about 70 % of their previous values from one technology generation to the next. However, as feature sizes approached the nanometer regime in the

early 2000s, Dennard scaling began to break down because the supply voltage could no longer be reduced in step with device dimensions. A key reason was the subthreshold swing (SS), which quantifies how efficiently the gate voltage drives the drain current from the off-state to the on-state. In a conventional MOSFET, SS has a thermal lower bound of approximately 60 mV dec^{-1} at room temperature, meaning that the gate voltage must change by at least ~ 60 mV to increase the current by one decade [10]. As a result, power consumption and heat dissipation increased significantly as integration density continued to rise [11]. To enable continued progress despite the end of Dennard's law, circuits were designed to reduce clock frequencies and combine multiple cores. That transition triggered the shift from single-core to multi-core architectures and indicated the end of consistent clock frequency scaling around 2005. This situation resulted in parallel systems that are energy-efficient but have slower individual cores than their predecessors [12].

1.1.3 3D Integration and Post-Moore Era

At the device level, continued scaling began to yield diminishing performance returns after the early 2000s. In particular, it was observed that dimension scaling was no longer sufficient to improve the switching speed. As a result, new materials, device architectures and process innovations were needed to sustain the performance improvements traditionally associated with Moore's Law [13]. The first major shift occurred at the 90 nm technology node with the introduction of strain engineering since the application of strain alters the carrier band structure to boost mobility [14]. Subsequently at the 45 nm node, traditional SiO_2 was replaced by high-κ[2] dielectrics like HfO_2 to improve gate capacitance and minimize leakage [15]. After the 32 nm technology node, the industry shifted from planar MOSFETs to three-dimensional (3D) FinFET architectures which were originally proposed by Hisamoto *et al.* in 1998 [16]. In 2011, Intel introduced its 22 nm bulk-silicon FinFET technology. With this technology, the gate can surround three sides and provides much better electrostatic control on the channel by raising the channel into a vertical fin. This triple-gate design offered significantly

higher immunity to short-channel effects such as source-to-drain tunneling [17]. As scaling progressed, silicon FinFETs have started to transition toward gate-all-around (GAA) designs such as nanosheet FETs. Unlike the tri-gate technology, the gate encloses the channel on all four sides in the GAA design and even in this architecture, fundamental constraints remain.

Within the post-Moore era, dimensional scaling remained a bottleneck even for other conventional bulk materials, such as SiGe and III–V compounds. As these materials are thinned to the atomic limit, their bulk properties degrade significantly due to quantum confinement effects. Furthermore, even assuming atomically smooth interfaces can be achieved, the dominance of surface states in ultra-thin bulk channels severely compromises carrier mobility [1]. Besides, the stacked nanosheet process flow increases structural complexity and can introduce extra parasitic capacitance and series resistance [18]. Consequently, there is a critical need for alternative device concepts and material platforms capable of maintaining high performance at atomic thicknesses.

1.1.4 The Promise of Steep-Slope Architectures

In parallel with the continuous scaling of conventional MOSFETs, alternative device architectures have been proposed to surpass the thermionic 60 mV dec^{-1} limit in SS and reduce power dissipation. Conventional MOSFETs are bound by this thermionic limit and necessitates the "steep-slope" technologies to enable further voltage scaling. One notable example is the negative-capacitance field-effect transistor (NC-FET), which integrates a ferroelectric layer into the gate stack [19]. Recent reviews highlight that the core advantage of NCFETs lies in their ability to provide internal voltage amplification through the negative capacitance effect. This allows the device to overcome the fundamental Boltzmann limit at room temperature. However, a critical aspect of their operation is the management of hysteresis loops caused by charge trapping or ferroelectric domain switching. Strategies such as utilizing van der Waals ferroelectric heterostructures or optimized dielectric engineering are currently being investigated to stabilize

this effect for reliable low-power switching [20]. Another promising direction is the cold-source (or Dirac-source) FET (CS-FET). In this device, the carrier-injection source is engineered to filter out high-energy carriers which enables steeper turn-off characteristics and lower leakage [21]. This architecture fundamentally differs from barrier-controlled devices due to its utilization of density-of-states (DOS) engineering. For instance, Graphene Dirac sources or "cold" metals with natural bandgaps are utilized to effectively filter out high-energy carriers. This allows steep switching characteristics with a SS less than 60 mV dec^{-1} at room temperature. In addition to a low SS, a significant merit of CS-FETs is maintaining high on-state currents (I_{on}) and high transconductance efficiency. Therefore, these devices overcome the low-drive-current limitations [22]. Tunnel FETs (TFETs) exploit band-to-band tunneling to enable ultra-steep switching and operation at reduced supply voltages[23], whereas strain-effect transistors (SETs) utilize mechanical strain to modulate the channel band structure and induce abrupt changes in carrier injection and transport [24]. On the other hand, spin-FETs harness spin-polarized carrier injection and spin-dependent transport to realize low-voltage logic switching with potentially sub-thermionic slopes [25]. Collectively, these emerging paradigms provide complementary pathways toward the development of ultra-low-power nanoelectronics.

1.1.5 The Promise of Two-Dimensional Materials

Considering the physical limitations inherent in geometric scaling discussed in previous sections, it is evident that the development of novel materials and design paradigms are imperative to sustain and enhance technological advancements [26]. Rather than further thinning bulk semiconductors with 3D unit cells, atomically thin two-dimensional (2D) materials may offer a more promising route to transistors with gate lengths of 15 nm and below [27]. The International Roadmap for Devices and Systems (IRDS, successor to the ITRS, International Technology Roadmap for Semiconductors) projects that the vertical stacking of logic devices represents the primary pathway to sustain the exponential growth of transistor density [1]. Besides, according to the ITRS 2013 report, transistor scaling is projected to

reduce the gate length (L_g) to as small as 5.1 nm for high-performance (HP) devices by 2028 [28]. At this point, 2D semiconductors have emerged as an attractive technology offering a compelling solution to these challenges. Figure 1.1 summarizes the historical co-evolution of gate length reduction and transistor density against the IRDS roadmap, highlighting the shift from dimensional to functional scaling and the emerging need for three-dimensional logic integration beyond 2030.

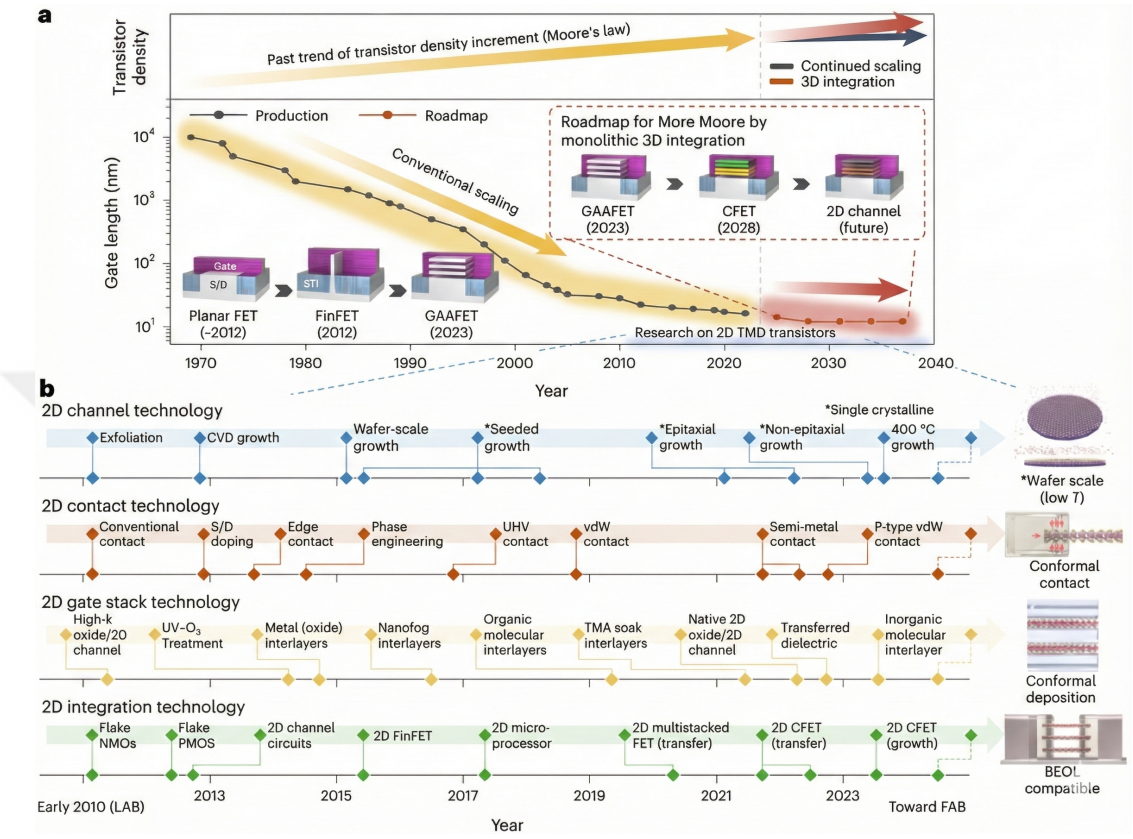


Figure 1.1: Historical evolution of gate length and transistor density, benchmarked against the IRDS roadmap. **a)** The shift from conventional (dimensional) scaling to functional scaling has sustained Moore's law to date; beyond 2030, continued progress is expected to require three dimensional logic integration, analogous to the transition already adopted in memory technologies. **b)** Key technological advances enabling 2D TMD based transistors over the past decade. UHV, ultrahigh vacuum; UV–O_3, ultraviolet–ozone; BEOL, back end of line. LAB and FAB on the x-axis denote research laboratories and manufacturing facilities, respectively. (Reproduced from [1])

In comparison to devices built on bulk semiconductor channels, transistors based on 2D materials provide stronger electrostatic gate control since the channel is intrinsically atomically thin [29]. Because their surfaces are largely free of dangling bonds, 2D semiconductors can retain strong electronic and optical performance even down to monolayer thickness. This contrasts with conventional

bulk semiconductors where surface and interface dangling bonds often create trap states that degrade device behavior [30]. Characterized by unique electrical conductivity and superior carrier transport properties, 2D materials present a promising solution to the challenges faced by conventional bulk semiconductors at the nanoscale [31, 32]. With their high carrier mobility [33, 34, 35] enabling rapid charge transport and excellent thermal conductivity [36] facilitating efficient heat dissipation, these atomically thin materials exhibit remarkable electronic properties. The inherent characteristics make 2D materials highly promising candidates for the next-generation electronic devices which require not only high-speed data processing but also enhanced thermal management to ensure device reliability and performance. 1.2 illustrates the trend of transistor scaling alongside the evolution of device architectures and materials. As highlighted by the red dashed line, 2D transistors offer a pathway for continued scaling down to sub-5-nm or sub-3-nm nodes.

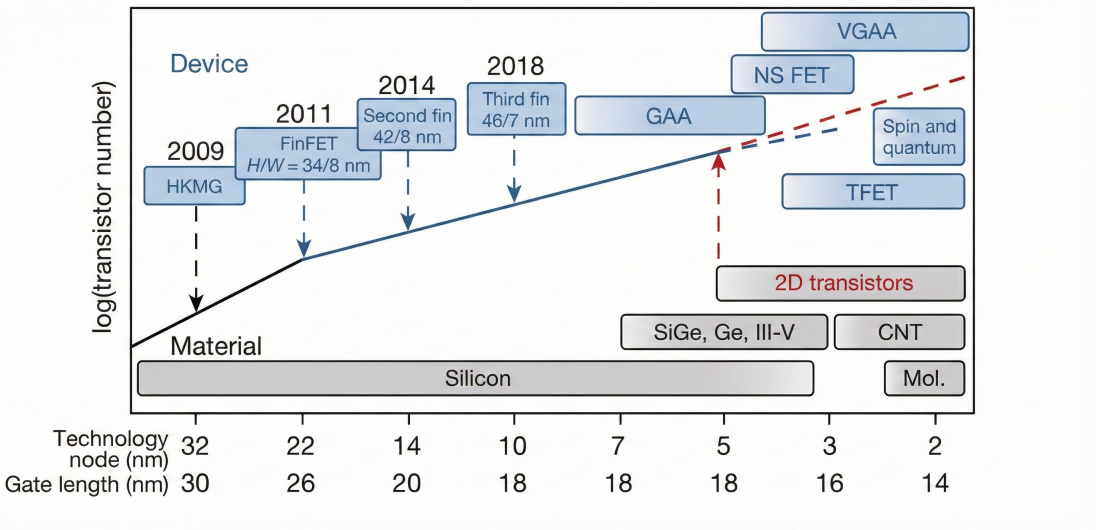


Figure 1.2: Illustration of transistor scaling trends concerning physical gate length and technology node. Abbreviations used in the figure include HKMG for high-κ dielectric and metal gate, NS FET for nano-sheet FET, CNT for carbon nanotube, and Mol. for molecules. (Reproduced from [2])

Since 2004, extensive research has focused on graphene. It was the first 2D material to be studied extensively and revealed a broad set of distinctive electronic

and photonic phenomena. However, because pristine graphene lacks an energy bandgap, it is mainly suited to radio-frequency electronics. It is revealed that it is not ideal for digital logic, which requires both a high on-current and a very low off-current. Consequently, the research focus shifted toward Transition Metal Dichalcogenides (TMDs) such as MoS_2 and WS_2. These materials possess finite bandgaps in the 1–2 eV range. Mentioned bandgap values make them ideal candidates for low-power digital logic and CMOS applications. Over the past decade, the performance of TMD-based transistors has improved drastically and has approached the benchmarks set by silicon devices. For example, MoS_2 has been demonstrated as a high-performance transistor channel material. An electron mobility of up to 3.4×10^4 cm^2 V^{-1} s^{-1} has been reported at cryogenic temperature [37]. The on/off ratio can exceed 10^8 [38] and a contact resistance as low as 0.2 $k\Omega\,mm$ has also been reported [39]. At room temperature, an I_{on} of 0.83 $mA\,mm^{-1}$ has been demonstrated [40]. In addition, an intrinsic power gain up to 50 GHz has been achieved [41]. Because 2D semiconductors have atomically smooth surfaces and are largely free of dangling bonds, their measured mobility depends only weakly on body thickness. In the sub-5 nm regime, this mobility can remain substantially higher than that of conventional bulk channels. This characteristic is therefore attractive for continued device scaling toward the 7 nm and 5 nm technology nodes [30]. Nevertheless, room-temperature field-effect mobility in 2D TMDs is still modest. This has intensified the search for alternative 2D semiconductors beyond TMDs. Representative candidates include group IV and V materials, Other directions include VIB monolayers, group IV–V and IV–VI compounds, and MXenes. Additionally, perovskite-based 2D materials, including inorganic perovskites and organic–inorganic hybrid perovskites, are another active area [30].

1.2 Thesis statement

Modern society depends on electronic systems whose performance requirements continue to intensify as new application domains expand. Demands arising from data-driven computing, artificial intelligence, high-bandwidth communication, and

sensing translate directly into the need for microprocessors and nanoelectronic platforms. These platforms are required to deliver higher speed and functionality while limiting energy consumption and heat generation. As addressed in the previous sections of the thesis, the historical strategy of improving performance primarily through the geometric scaling of silicon-based transistors is approaching a regime where further miniaturization becomes increasingly constrained. Sustaining strong electrostatic control is difficult at nanometer dimensions. Accordingly, leakage currents grow, and interface and contact effects become dominant. This situation makes it challenging to simultaneously achieve low standby power, high drive capability, and reliable switching. All these conditions reveal the necessity of new materials that possess the essential properties and different approaches that are compatible with today's technology. One of the promising charge-based approaches for the solution is to produce a new generation of field-effect transistors using 2D materials. Beyond traditional 3D bulk semiconductors, there is a large family of single or multi-atom-thick 2D semiconductors. These systems can exhibit excellent electronic and optical properties compared to their 3D counterparts. Experimental and theoretical studies on this subject reveal the potential of this approach. In this scope, the thesis aims to design low-power and high-performance FET and MOSFET devices approximately 5 nm in size using 2D semiconductors. The rationale behind the thesis is to start by investigating a relatively simple system, the Metal-Semiconductor-Metal (MSM) device, followed by the pn junction, the p–i–n FET and finally the MOSFET. It demonstrates a systematic bottom-up progression through device architectures to evaluate 2D semiconductors as a platform for next-generation nanoelectronics. Using a comprehensive first-principles and quantum transport-based computational methodology, the thesis begins with metal-semiconductor-metal devices to resolve contact-limited transport and clarify how channel length and electrode doping govern current flow at nanometer scales. It then advances to the pn junction to capture how built-in electrostatics and tunneling produce rectification. Building on this foundation, the thesis introduces the p-i-n field-effect transistor as an intermediate architecture, where a gate electrode serves as an active control element. Ultimately, the work led to the development of a MOSFET architecture where the combined effects of contacts, channel transport, and electrostatic control

are assessed in a device concept. A further thesis outcome is that architectural optimization must be treated as an equal partner to materials selection in 2D nanoelectronics. In particular, underlap (UL) engineering is identified as a practical instrument to tune source and drain electrostatics without changing the channel material itself. Within the thesis's device hierarchy, this concept becomes critical at the MOSFET stage, where UL complements double gate electrostatics in the deeply scaled regime. Overall, this thesis serves as a proof of concept demonstrating that 2D semiconductors can support competitive transistor operation. It is demonstrated that this performance is achievable when their atomically thin nature is combined with optimized electrostatics, including specific gate geometries such as UL.

Chapter 2

Theoretical Framework

2.1 Density Functional Theory

2.1.1 The Many-Body Problem and the Born-Oppenheimer Approximation

The fundamental behavior of matter at the atomic scale is governed by the laws of quantum mechanics. Describing the properties of materials ranging from isolated molecules to extended solids requires determining the behavior of their constituent nuclei and electrons. The non-relativistic state of such a system is completely described by the wavefunction (Ψ) which is obtained by solving the time-independent Schrödinger equation:

$$\hat{H}\Psi = E\Psi \tag{2.1}$$

Here, $\hat{H}$ represents the Hamiltonian operator, E is the total energy of the system, and Ψ is the eigenstate. For a system consisting of N electrons and M nuclei, the full Hamiltonian is composed of five distinct contributions:

$$\hat{H} = -\frac{\hbar^2}{2}\sum_{A=1}^{M}\frac{\nabla_A^2}{M_A} - \frac{\hbar^2}{2m}\sum_{i=1}^{N}\nabla_i^2 + \frac{1}{2}\sum_{A=1}^{M}\sum_{B\neq A}^{M}\frac{Z_A Z_B e^2}{|\mathbf{R}_A - \mathbf{R}_B|} + \frac{1}{2}\sum_{i=1}^{N}\sum_{j\neq i}^{N}\frac{e^2}{|\mathbf{r}_i - \mathbf{r}_j|} - \sum_{i=1}^{N}\sum_{A=1}^{M}\frac{Z_A e^2}{|\mathbf{r}_i - \mathbf{R}_A|} \tag{2.2}$$

These terms represent the kinetic energy of the nuclei, the kinetic energy of the electrons, the potential energy of the nucleus-nucleus repulsion, the potential energy of the electron-electron repulsion, and the potential energy of the electron-nucleus attraction, respectively. The wavefunction Ψ depends on the coordinates of all N electrons and M nuclei and results in a problem of $3(N + M)$ dimensions.

Solving this differential equation analytically is impossible for all but the simplest systems, such as the hydrogen atom. The primary obstacle is the electron-electron interaction term. Because the motion of any single electron is coupled to the motion of all other electrons via Coulombic repulsion, the wavefunction cannot be separated into a product of single-particle wavefunctions. This coupled behavior constitutes the "many-body problem".

This complexity is reduced by exploiting the fact that nuclei are much heavier than electrons. A proton is approximately 1836 times heavier than an electron. Consequently, electrons respond almost instantaneously to any displacement of the nuclei. The timescales of electronic and nuclear motion can therefore be decoupled via the Born-Oppenheimer approximation which assumes that the electrons adjust instantaneously to the configuration of the heavier and effectively stationary nuclei. Under this approximation, the nuclei are treated as fixed point charges. The electronic Hamiltonian ($\hat{H}_e$) is solved for a fixed nuclear configuration $\{\mathbf{R}\}$:

$$\hat{H}_e \Psi_e(\mathbf{r}, \mathbf{R}) = E_e(\mathbf{R})\Psi_e(\mathbf{r}, \mathbf{R}) \tag{2.3}$$

The kinetic energy of the nuclei is neglected in this electronic problem, and the nucleus-nucleus repulsion is treated as a constant additive term to the total energy. The resulting electronic energy $E_e(\mathbf{R})$ defines the adiabatic potential energy surface when calculated as a function of the nuclear positions. The potential energy surface determines the motion of the nuclei. This effectively reduces the

complex coupled problem into two smaller consecutive tasks. The electronic structure is first solved at fixed nuclear positions and the nuclear dynamics are subsequently determined on the calculated potential surface. While the Born-Oppenheimer approximation simplifies the Schrödinger equation significantly, the electronic problem remains a formidable many-body challenge due to the electron correlation inherent in the Hamiltonian.

2.1.2 The Hohenberg-Kohn Theorems

Hohenberg and Kohn formulated two essential theorems that serve as the basis for the Density Functional Theory framework [42]. These theorems shifted the focus from the complex many-body wavefunction to the simpler electron density.

Theorem 1 establishes a one-to-one mapping between the external potential and the electron density which is stated as "The ground-state energy determined by solving the Schrödinger equation is a unique functional of the electron density.". Specifically, the external potential $V(\mathbf{r})$ is uniquely determined by the electronic density $n(\mathbf{r})$, within a trivial additive constant. Since $n(\mathbf{r})$ uniquely determines the $V(\mathbf{r})$, and the kinetic and electron–electron interaction operators are universal, the many-electron Hamiltonian is thereby fixed. Consequently, the ground state density determines the wavefunction and all derived physical properties which implies that the complex multidimensional wavefunction can be effectively replaced by the 3D electron density as the central variable.

Theorem 2 extends the variational principle to the density. Conventionally, the ground-state energy E is determined via the Rayleigh-Ritz minimal principle using trial wavefunctions Ψ_{trial}:

$$E = \min \frac{\langle \Psi_{\text{trial}} | H | \Psi_{\text{trial}} \rangle}{\langle \Psi_{\text{trial}} | \Psi_{\text{trial}} \rangle} \quad . \tag{2.4}$$

Hohenberg and Kohn demonstrated that this minimization can be formulated in terms of trial charge densities. For a non-degenerate ground-state, the energy

minimum is attained if and only if the trial density corresponds to the true ground-state density. The energy functional is given by:

$$E_V[n] = F[n] + \int n(\mathbf{r})V(\mathbf{r})d\mathbf{r} \quad . \tag{2.5}$$

The term $F(n)$ is defined as a universal functional. It is independent of the specific external potential $V(\mathbf{r})$ and is expressed as:

$$F[n] = \langle \Psi[n]|\hat{T} + \hat{U}|\Psi[n]\rangle \quad . \tag{2.6}$$

Here, $\Psi(n)$ represents the ground-state wavefunction associated with a potential $\hat{U}$ that generates the density n. While these theorems provide the rigorous basis for DFT, the direct application is hindered by the lack of an exact form for the kinetic energy functional. This limitation leads to errors which are subsequently addressed through the implementation of the Kohn-Sham equations.

2.1.3 The Kohn-Sham Formalism

While foundational, the Hohenberg-Kohn theorems offer no practical guidance for constructing the universal functional $F(n)$. The primary obstacle is the kinetic energy. Determining the kinetic energy of interacting electrons directly from the density is mathematically impossible. Kohn and Sham addressed this in 1965 by introducing an auxiliary non-interacting system so that the kinetic energy can be computed exactly from single-particle orbitals [43]. In this scheme, the system is assumed to consist of non-interacting particles moving in an effective local potential, $V_{eff}(\mathbf{r})$. The critical constraint is that the ground-state density of this fictitious, non-interacting system, $n_s(\mathbf{r})$, must equal the ground-state density of the real, interacting system, $n(\mathbf{r})$.

Since the auxiliary particles do not interact, the many-body wavefunction is simply a Slater determinant of single-particle orbitals (ϕ_i). The kinetic energy

can then be computed exactly:

$$T_s[n] = -\frac{1}{2}\sum_{i=1}^{N}\langle\phi_i|\nabla^2|\phi_i\rangle \quad . \tag{2.7}$$

T_s represents the kinetic energy of the non-interacting system and it is not identical to the interacting kinetic energy $T(n)$; the difference is included in the exchange-correlation energy (E_{xc}). The total energy functional is partitioned to account for this discrepancy, as well as the non-classical electron-electron interaction. The difficult terms are grouped into the E_{xc}. The functional becomes:

$$E[n] = T_s[n] + \int V_{ext}(\mathbf{r})n(\mathbf{r})d\mathbf{r} + E_{Hartree}[n] + E_{xc}[n] \quad . \tag{2.8}$$

Here, $E_{Hartree}$ is the classical electrostatic repulsion energy. E_{xc} is defined as the residual:

$$E_{xc}[n] = (T[n] - T_s[n]) + (E_{ee}[n] - E_{Hartree}[n]) \quad . \tag{2.9}$$

Minimizing the energy functional with respect to the orbitals, subject to the orthonormality constraint $\langle\phi_i|\phi_j\rangle = \delta_{ij}$, yields the single-particle Kohn-Sham equations:

$$\left(-\frac{1}{2}\nabla^2 + V_{eff}(\mathbf{r})\right)\phi_i(\mathbf{r}) = \epsilon_i\phi_i(\mathbf{r}) \quad . \tag{2.10}$$

The effective potential (V_{eff}) acts as the local field experienced by the non-interacting electrons. It is composed of the external potential, the Hartree potential, and the exchange-correlation potential:

$$V_{eff}(\mathbf{r}) = V_{ext}(\mathbf{r}) + \int \frac{n(\mathbf{r}')}{|\mathbf{r} - \mathbf{r}'|}d\mathbf{r}' + V_{xc}(\mathbf{r}) \quad . \tag{2.11}$$

where $V_{xc}(\mathbf{r}) = \frac{\delta E_{xc}[n]}{\delta n(\mathbf{r})}$. These equations form a closed loop. The potential depends on the density, which depends on the orbitals, which in turn depend on the potential. Solutions must be found iteratively using a self-consistent field (SCF) cycle.

2.1.4 Effective Non-Interacting Representation of the Interacting Many-Body System

The practical utility of the Hohenberg-Kohn theorems is severely limited by the kinetic energy functional ($T[n]$). No exact explicit form exists for an interacting electron gas and approximations are inevitable. Instead, one introduces a non-interacting reference system constructed to reproduce the exact ground-state density of the interacting electrons. This recasts the many-body problem into an effective single-particle description, with the remaining many-body effects absorbed into $E_{\text{xc}}[n]$.

The mapping relies on the critical assumption of representability. It is postulated that for any interacting ground-state $n(\mathbf{r})$ there exists a unique $V_{eff}(\mathbf{r})$ capable of generating that exact same density in a non-interacting system. The densities are forced to be identical:

$$n(\mathbf{r}) = n_s(\mathbf{r}) = \sum_{i=1}^{N} |\phi_i(\mathbf{r})|^2 \quad . \tag{2.12}$$

This substitution completely transforms the problem. The wavefunction of the interacting system is a complex high dimensional object whereas the ground state of the auxiliary system is defined by a Slater determinant of single particle orbitals (ϕ_i). The kinetic energy of this non-interacting system (T_s) is easily computed:

$$T_s[n] = -\frac{1}{2} \sum_{i=1}^{N} \langle \phi_i | \nabla^2 | \phi_i \rangle \quad . \tag{2.13}$$

2.1.5 The Exchange-Correlation Functional

While the Kohn-Sham framework is exact in principle it is approximate in practice. The role of $E_{\mathrm{xc}}[n]$ is therefore not to represent a small correction, but to collect the genuine many-body physics that is missing from the non-interacting reference system and from the classical mean-field treatment of Coulomb repulsion.

Since the exact analytical form of $E_{xc}[n]$ is unknown for any realistic system, approximations are mandatory. The most fundamental approximation is the Local Density Approximation (LDA) [44]. Here, the exchange-correlation energy density at a point $\mathbf{r}$ is assumed to be equal to that of a homogeneous electron gas (HEG) with the same density $n(\mathbf{r})$. LDA often overbinds molecules while surprisingly successful for solids.

To correct these errors, the Generalized Gradient Approximation (GGA) [45] is employed. The functional is formulated to depend not only on the local density but also on the gradient of the density $\nabla n(\mathbf{r})$ which allows the method to account for spatial variations and captures the inhomogeneity of the electron distribution more effectively.

2.1.6 The Bloch Theorem and Plane Wave Basis Sets

Crystalline solids are distinguished by their intrinsic long range periodic order and this translational symmetry is not merely a geometric feature but the fundamental mathematical principle that enables the great simplification necessary to render the problem solvable. The potential experienced by an electron, $V(\mathbf{r})$, is periodic with the lattice: $V(\mathbf{r}+\mathbf{R}) = V(\mathbf{r})$ for any lattice vector $\mathbf{R}$. Bloch's theorem represents the direct mathematical consequence of the crystal's periodicity. It states that the eigenstates of the one-electron Hamiltonian can be expressed as the product of a plane wave and a function with the periodicity of the crystal lattice. The wavefunction $\psi_{n\mathbf{k}}(\mathbf{r})$ is given by:

$$\psi_{n\mathbf{k}}(\mathbf{r}) = e^{i\mathbf{k}\cdot\mathbf{r}} u_{n\mathbf{k}}(\mathbf{r}) \quad . \tag{2.14}$$

Here, n is the band index and $\mathbf{k}$ is a wave vector confined to the first Brillouin zone. The function $u_{n\mathbf{k}}(\mathbf{r})$ preserves the periodicity of the potential, such that $u_{n\mathbf{k}}(\mathbf{r} + \mathbf{R}) = u_{n\mathbf{k}}(\mathbf{r})$.

Since $u_{n\mathbf{k}}(\mathbf{r})$ is periodic, it can be expanded as a Fourier series in terms of reciprocal lattice vectors, $\mathbf{G}$. Consequently, the total wavefunction is written as a linear combination of plane waves:

$$\psi_{n\mathbf{k}}(\mathbf{r}) = \sum_{\mathbf{G}} c_{n,\mathbf{k}+\mathbf{G}} e^{i(\mathbf{k}+\mathbf{G})\cdot\mathbf{r}} \quad . \tag{2.15}$$

This expansion transforms the Schrödinger equation from a differential equation in real space into a matrix eigenvalue problem in reciprocal space. The coefficients $c_{n,\mathbf{k}+\mathbf{G}}$ are the unknowns to be determined. The infinite nature of the summation over the reciprocal lattice vectors $\mathbf{G}$ presents a computational hurdle. To achieve practical implementation a finite basis set must be established using a kinetic energy cutoff (E_{cut}) which ensures that only plane waves with kinetic energy less than this value are included and allows for calculation convergence.

$$\frac{1}{2}|\mathbf{k} + \mathbf{G}|^2 \leq E_{cut} \quad . \tag{2.16}$$

The accuracy of the resulting calculation exhibits a strict dependency on the magnitude of the E_{cut}. Due to the systematic error introduced by the necessary truncation of the infinite basis set, the convergence of the total energy with respect to the E_{cut} must be established rigorously for every studied system.

2.1.7 Pseudopotentials

Although the plane wave basis set offers mathematical convenience, it exhibits a significant limitation when applied to core electrons. In the proximity of the atomic nucleus, the deep singular potential leads to a rapidly varying all-electron wavefunction, and, in addition, the valence states must be orthogonal to the occupied core orbitals. This orthogonality imposes rapid oscillations or nodes on the valence wavefunction which demand a prohibitively large E_{cut} for accurate resolution that leads to an extreme increase in computational cost. Pseudopotential methods exploit the fact that core electrons are tightly bound and typically remain close to their atomic character in chemical environments (frozen-core approximation). Both the strong Coulomb potential near the nucleus and the core electrons are effectively replaced by a smoother potential known as the pseudopotential (V_{ps}). The motion of the valence electrons is governed by this screened potential. The resulting pseudo wavefunction ($\psi_{ps}(\mathbf{r})$) designed to be free of oscillations inside a core cutoff radius (r_c). Beyond this r_c, the $\psi_{ps}(\mathbf{r})$ and the corresponding V_{ps} are strictly required to reproduce the properties of the true all-electron system:

$$\psi_{ps}(\mathbf{r}) = \psi_{AE}(\mathbf{r}) \quad \text{for} \quad r > r_c \quad . \tag{2.17}$$

The implementation of the V_{ps} drastically lowers the necessary size of the plane-wave basis set. The scattering characteristics of the ion are strictly maintained. However, the highly demanding core potential singularity is smoothed out, thereby significantly improving the overall computational efficiency. A schematic comparison between the true all-electron potential and wavefunction versus their pseudo counterparts is shown in Figure 2.1.

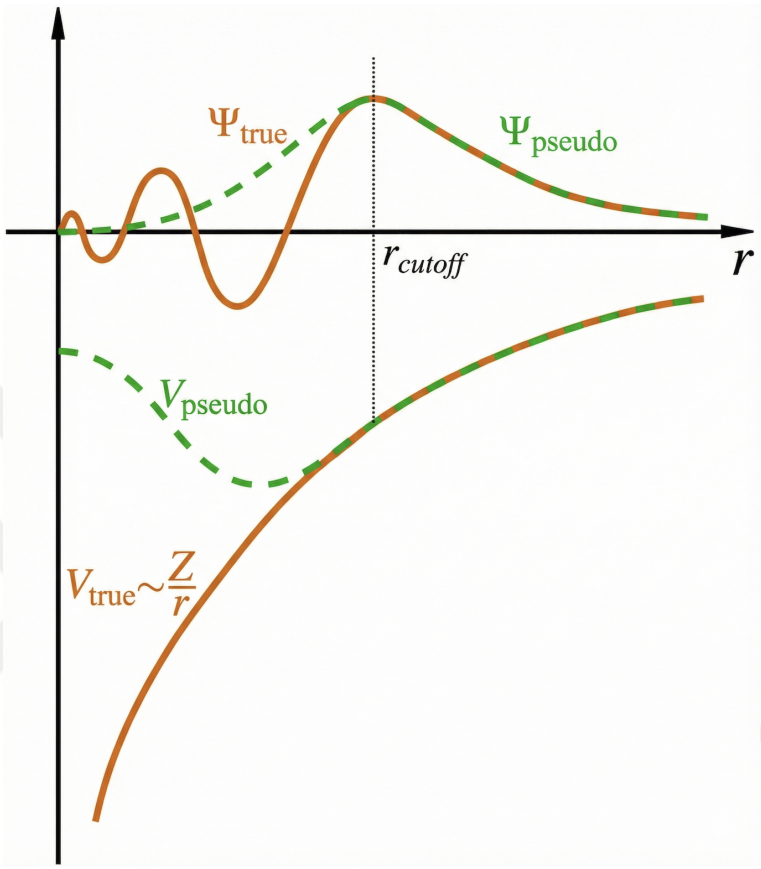


Figure 2.1: Schematic illustration of the pseudopotential approximation. Inside the cutoff radius r_{cutoff}, the singular true potential (V_{true}) and the highly oscillatory true wavefunction (Ψ_{true}) (orange solid lines) are replaced by a smoother pseudopotential (V_{pseudo}) and a nodeless pseudo wavefunction (Ψ_{pseudo}) (green dashed lines). For $r > r_{cutoff}$, the pseudo and true quantities coincide.

Various schemes exist for generating these effective potentials starting with norm conserving pseudopotentials which enforce the strict condition that the charge enclosed within the core r_c for the $\psi_{ps}(\mathbf{r})$ must exactly equal that of the true all electron wavefunction [46, 47]. Despite their accuracy, these potentials can remain "hard" particularly for elements like oxygen or most transition metals. Ultrasoft pseudopotentials subsequently relax this norm conservation constraint which allows for the generation of significantly smoother $\psi_{ps}(\mathbf{r})$ and requires even lower E_{cut} [48]. Lastly, the projector augmented-wave (PAW) method can be regarded as a unifying framework that combines the computational efficiency

of pseudopotentials with an explicit reconstruction of the all-electron behavior in the vicinity of each nucleus. In this method, a smooth $\psi_{ps}(\mathbf{r})$ is used on the real-space grid or in a plane-wave basis. Atom-centered augmentation functions and projector operators are introduced within predefined augmentation spheres to recover the correct nodal structure and the charge density of the all-electron wavefunction [49].

2.2 First-Principles Quantum Transport

2.2.1 Density Functional Theory in Localized Basis Sets

While plane-wave expansions are ubiquitous in bulk electronic structure calculations, they are ill-suited for the open geometries and vacuum regions inherent to device simulations. A Linear Combination of Atomic Orbitals (LCAO) representation is employed instead. This approach facilitates a localized matrix picture of the Hamiltonian which is critical for scaling to large systems. The Kohn-Sham (KS) wavefunctions ψ_α are constructed in a set of finite-range basis functions ϕ_i:

$$\psi_\alpha(\mathbf{r}) = \sum_i c_{\alpha i}\phi_i(\mathbf{r}) \quad . \tag{2.18}$$

Substitution of this expansion into the KS equation yields the generalized matrix eigenvalue problem for the coefficients $c_{\alpha i}$:

$$\sum_j H_{ij}^{KS} c_{\alpha j} = \epsilon_\alpha \sum_j S_{ij} c_{\alpha j} \quad . \tag{2.19}$$

The Hamiltonian matrix elements $H_{ij}^{KS} = \langle\phi_i|\hat{H}^{KS}|\phi_j\rangle$ and the overlap matrix elements $S_{ij} = \langle\phi_i|\phi_j\rangle$ are computed via integration over the electronic coordinates.

To reduce computational cost, explicit calculation of core electrons is avoided. Norm-conserving pseudopotentials (PPs) are utilized to describe the interaction

between valence electrons and the ionic cores (nuclei + frozen core electrons). These potentials may include scalar-relativistic effects or fully relativistic spin-orbit coupling generated by solving the Dirac equation for the isolated atom.

The basis functions ϕ_{nlm} are numerical atomic orbitals rather than analytical Gaussians. They take the form:

$$\phi_{nlm}(\mathbf{r}) = \chi_{nl}(r)Y_{lm}(\hat{\mathbf{r}}) \tag{2.20}$$

where Y_{lm} and χ_{nl} are spherical harmonics and radial functions, respectively. A defining feature of this basis is that the radial functions vanish identically beyond a specified finite range. This property is paramount. It ensures that both H and S are stringently sparse and elements corresponding to atoms separated by distances greater than the sum of their orbital radii are exactly zero.

The electron density is reconstructed on a real-space grid from the density matrix D_{ij}:

$$n(\mathbf{r}) = \sum_{ij} D_{ij}\phi_i(\mathbf{r})\phi_j(\mathbf{r}) \quad . \tag{2.21}$$

For equilibrium systems (bulk and molecules), the density matrix is obtained by diagonalizing the Hamiltonian. In the non-equilibrium device configurations discussed in subsequent sections, D_{ij} is calculated via the Green's function method.

The Hamiltonian matrix elements H_{ij}^{KS} often involve two centers that are orbitals centered on atoms A and B. Such terms are called two-center integrals because the integrand depends only on the relative geometry of two atoms. Thanks to the form (2.21) the 3D integrals over $\mathbf{r}$ can be transformed into analytic/angular parts and numerical 1D integrals over the radial coordinate $\mathbf{r}$. These radial integrals are evaluated using Fourier-transform method that is fast and accurate [50]. When the effective KS potential $V_{eff}(\mathbf{r})$ is built from the full electron density and all nuclei, the matrix elements are formed as $\langle\phi_i|V_{eff}(\mathbf{r})|\phi_j\rangle$. Since the integrand depends on many atomic centers at once, these multi-center integrals are evaluated

by sampling $\phi_i(\mathbf{r})$, $\phi_j(\mathbf{r})$ and $V_{eff}(\mathbf{r})$ on the grid points and numerically integrating over the real-space grid. This grid-based representation of the potential allows the seamless inclusion of external electrostatic fields such as metallic gates, via the Poisson equation.

2.2.2 The Open System Geometry

Standard electronic structure methods are typically restricted to two geometric extremes such as finite clusters or periodic crystals. However the theoretical treatment of an atomic-scale contact coupled to bulk electrodes demands a method capable of modeling an infinite and non-periodic system. Truncating the leads to finite dimensions by breaking translational symmetry along the transport axis z introduces artificial scattering at the boundaries. This renders such approximations unsuitable for transport phenomena. Furthermore, the application of a voltage bias drives the electronic subsystem out of equilibrium. Consequently, the modeling framework must explicitly describe a non-equilibrium state wherein the external electrodes are maintained at distinct electrochemical potentials.

The system is partitioned into the left electrode (L), the central contact region (C), and the right electrode (R) to address the infinite nature of the device. A schematic representation of this partitioning is shown in Figure 2.2. The L and R regions represent semi-infinite bulk reservoirs extending to $z = -\infty$ and $z = +\infty$, respectively. These reservoirs are maintained in thermodynamical equilibrium and characterized by fixed electrochemical potentials μ_L and μ_R. While the system remains open along the transport direction z, periodicity is typically retained in the transverse directions (x, y). Bloch's theorem is thus exploited in the transverse plane. So, it allows the sampling of the transverse Brillouin zone to describe the extended states.

The central region C includes the scattering nanostructure along with sufficient layers of the electrode material to ensure proper coupling. A critical feature of this formalism is the utilization of localized atomic orbitals with finite range. The system can be partitioned since Hamiltonian interactions are zero beyond a specific

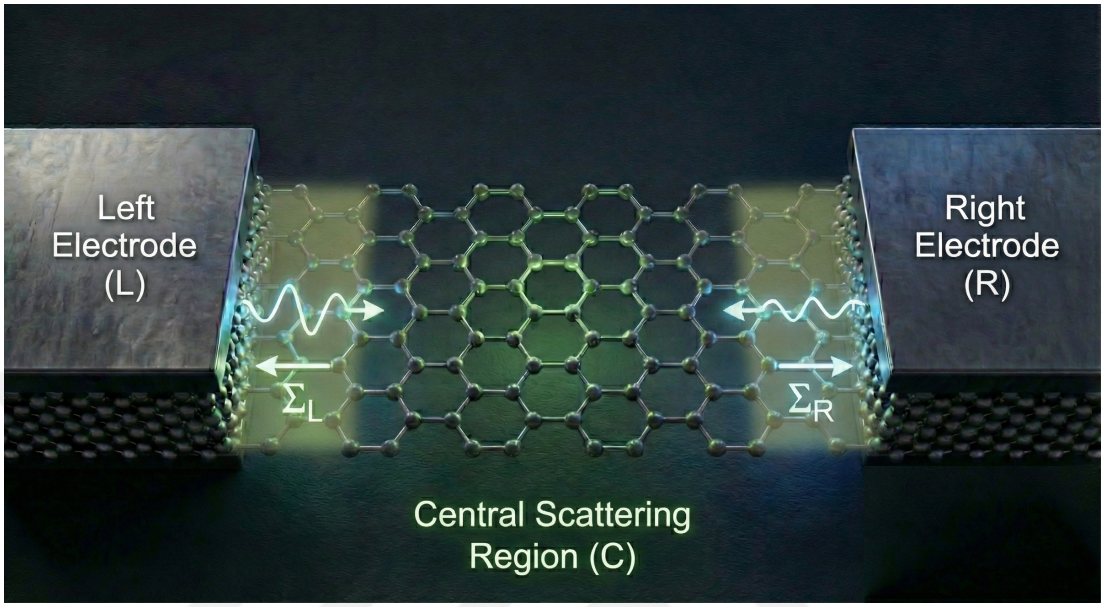


Figure 2.2: Schematic of the two-probe geometry partitioned into Left Electrode (L), Central Scattering Region (C), and Right Electrode (R). The central region contains sufficient buffer layers to match the bulk potentials at the boundaries.

cutoff distance. The C is defined to be large enough that basis functions in the L possess zero overlap with those in the R. Thus, all matrix elements connecting L directly to R are strictly zero. Consequently, the Hamiltonian and overlap matrices adopt a block-tridiagonal form. Since direct coupling between L and R is eliminated, interaction occurs exclusively through the contact region. This is not only a numerical convenience. On the contrary, it is a physical requirement for the modular construction of the Green's function.

The definition of the central region requires rigorous attention. It comprises the scattering object such as a molecule, interface or defect. Crucially, portions of the electrode material are designated as electrode extensions. The size of these extensions is dictated by the screening length of the material. The screening approximation means that electrostatic disturbances induced by the scatterer are assumed to be fully screened within the boundaries of C. At the interfaces $L - C$ and $C - R$, the electronic structure is matched to that of the bulk. It is assumed that the Hamiltonian and density matrix elements in the electrode extensions have converged to their bulk values. This match permits the use of Dirichlet

boundary conditions for the Hartree potential (V_H) at these interfaces. It also fixes the potential to the bulk values (V_{bulk}) that is shifted by the applied bias voltage (V_{bias}):

$$V_H(\mathbf{r})|_{L/R} = V_{bulk} \pm \frac{V_{bias}}{2} \quad . \tag{2.22}$$

If the current density is high or the screening is poor, the length of C must be expanded until this matching condition is satisfied. Failure to ensure sufficient screening results in unphysical scattering at the boundaries which contaminates the transport signal.

2.2.3 The Non-Equilibrium Green's Function (NEGF) Formalism

The density matrix is the central quantity in the Non-Equilibrium Green's Function (NEGF) formalism. In a non-equilibrium steady state, it cannot be obtained by simple diagonalization of the Hamiltonian. Instead, the NEGF formalism provides a rigorous framework to calculate the electron density and transport properties of the open system [51]. This approach seamlessly handles the infinite nature of the electrodes and the non-equilibrium occupation numbers driven by the applied bias.

2.2.3.1 Definition of the Retarded Green's Function

The key operator is the retarded Green's function matrix $G(\epsilon)$ of the central region and describes how an electron with energy ϵ propagates through the scattering region, including escape into the electrodes. It is constructed from the Hamiltonian H and overlap S matrices of the scattering region. Additionally, it is renormalized by the coupling to the semi-infinite electrodes. Physically, it encodes all information needed to compute local densities, currents and transmission.

Mathematically, it is the inverse of an effective non-Hermitian operator and the formal definition is:

$$G(\epsilon) = [(\epsilon + i\delta_+)S - H - \Sigma^L(\epsilon) - \Sigma^R(\epsilon)]^{-1} \quad . \tag{2.23}$$

Here, δ_+ is an infinitesimal positive number that ensures causality. In this context, causality means that the system's response occurs only after a perturbation is applied. The matrices H and S are finite which correspond only to the central region C defined in the previous section. The terms $\Sigma^L(\epsilon)$ and $\Sigma^R(\epsilon)$ are the retarded self-energies of the left and right electrodes, respectively. Inversion of the full matrix is required at each energy point ϵ. Since the Hamiltonian is stored in a sparse format, block diagonal inversion techniques [52] are utilized to compute the necessary elements of G. Specifically, those required for the density matrix and transmission coefficients are computed.

2.2.3.2 Electrode Self-Energies

The self-energies $\Sigma^{L/R}(\epsilon)$ encapsulate the entire effect of the semi-infinite electrodes on the central region. They act as non-Hermitian boundary conditions that allow electrons to enter and leave the scattering region. Physically, they shift the energy levels (real part) and broaden the states (imaginary part) within the contact.

These matrices are computed from the surface Green's functions of the uncoupled bulk electrodes. Recursion methods [53] that exploit the sparsity of the electrode Hamiltonian are employed to enhance for computational efficiency in the calculations of the current study. Once Σ is known, the coupling strength is quantified by the broadening matrix Γ:

$$\Gamma^{L/R}(\epsilon) = i[\Sigma^{L/R}(\epsilon) - (\Sigma^{L/R}(\epsilon))^\dagger] \quad . \tag{2.24}$$

This matrix governs the rate at which electrons scatter into and out of the device.

2.2.3.3 Spectral Density Matrices

The connection between the Green's function and the scattering states is established via the spectral density matrix. The density matrix is split into contributions originating from the left and right electrodes: $D = D^L + D^R$. The spectral density injected from the left electrode, $n^L(\epsilon)$, is expressed as:

$$n^L(\epsilon) = \frac{1}{2\pi} G(\epsilon)\Gamma^L(\epsilon)G^\dagger(\epsilon) \quad . \tag{2.25}$$

An analogous expression exists for $n^R(\epsilon)$. These matrices represent the local density of states weighted by the coupling to the respective electrode. The diagonal elements correspond to the electron density at a specific energy and position resulting from scattering states incoming from the leads.

2.2.3.4 The Non-Equilibrium Density Matrix

The total density matrix D is the integral of the spectral densities weighted by the Fermi-Dirac distribution functions $f(\epsilon, \mu_{L/R})$ of the reservoirs.

$$D = \int_{-\infty}^{\infty} d\epsilon \left[n^L(\epsilon) f\left(\frac{\epsilon - \mu_L}{k_B T_L}\right) + n^R(\epsilon) f\left(\frac{\epsilon - \mu_R}{k_B T_R}\right) \right] \quad . \tag{2.26}$$

Direct numerical integration of this expression along the real energy axis is computationally unstable and inefficient due to the sharp peaks in the density of states (van Hove singularities). To circumvent this, the integral is decomposed into an equilibrium part and a non-equilibrium correction [51]. The equilibrium part is integrated over a complex contour comprising a line segment deep in the complex plane, a circle segment enclosing the Fermi poles, and a a line returning to the real axis. The function is smooth in the complex plane, requiring far fewer energy points for convergence.

$$D = D^L_{eq} + \Delta^R_{neq} \tag{2.27}$$

The non-equilibrium term, Δ^R_{neq}, accounts for the bias window where $\mu_L \neq \mu_R$.

This term must be integrated along the real axis, but only within the narrow energy range defined by the applied bias.

$$\Delta^R_{neq} = \int n^R(\epsilon)\,[f_R(\epsilon) - f_L(\epsilon)]\,d\epsilon \tag{2.28}$$

A double contour scheme is often employed to symmetrize the integration error and ensure proper weighting of bound-states that may shift into the bias window. This separation of the integral enables efficient self-consistent calculations even under high bias voltage.

2.2.4 Electrostatics and Self-Consistency under Bias

The determination of the electrostatic landscape is the backbone of the self-consistent cycle. The electron density $n(\mathbf{r})$, constructed from the non-equilibrium density matrix, serves as the source term for the Hartree potential $V^H(\mathbf{r})$. This potential is obtained by solving the Poisson equation on a real-space grid:

$$\nabla^2 V^H(\mathbf{r}) = -4\pi n(\mathbf{r}) \quad . \tag{2.29}$$

This equation links the quantum mechanical charge distribution to the classical electrostatic field. It is solved in conjunction with the external potential arising from the ionic cores and any applied gate voltages. The total effective potential V_{eff} is then updated, closing the self-consistent loop.

2.2.4.1 Boundary Conditions and Poisson Solvers

Solving the Poisson equation requires the imposition of physically motivated boundary conditions (BCs) on the simulation cell facets. The choice of BCs is dictated by the system geometry and the dimensionality of the transport problem.

- **Periodic BCs:** Utilized for bulk calculations and in the transverse directions (x, y) of device configurations, ensuring continuity of the potential across unit cell boundaries.
- **Multipole BCs:** Employed for isolated molecules. The potential at the boundary is extrapolated from the monopole, dipole, and quadrupole moments of the internal charge distribution, ensuring correct asymptotic behavior for charged species.
- **Dirichlet and Neumann BCs:** These are critical for the transport direction (z) in open systems. Dirichlet conditions fix the potential value $V_0(\mathbf{r})$ at the boundary, while Neumann conditions fix the gradient (electric field).

In the two-probe device geometry, Dirichlet BCs are imposed at the interfaces between the central region and the electrodes. The potential values at these boundaries are not arbitrary; they are matched to the bulk electrode potentials, shifted rigidly by the applied bias voltage V_{bias}:

$$\mu_L - \mu_R = -eV_{bias} \quad . \tag{2.30}$$

This creates a defined potential drop across the scattering region. The Poisson equation is typically solved using Fast Fourier Transform (FFT) [54] techniques for periodic directions, often combined with finite-difference methods for non-periodic directions.

2.2.4.2 The "Spill-in" Terms

Calculating the electron density solely from the central region's density matrix (D^{CC}) is insufficient. The wavefunction extends across the artificial boundaries separating the central region from the semi-infinite electrodes. Neglecting the contributions from the electrode subblocks (D^{LC}, D^{CL}, etc.) leads to significant errors in the density and potential near the interfaces. These contributions are termed "spill-in" terms [55].

The electron density is rigorously reconstructed as:

$$n(\mathbf{r}) = \sum_{i,j \in \mathbf{C}} D_{ij}^{CC} \phi_i \phi_j + \sum_{i \in \mathbf{L}, j \in \mathbf{C}} D_{ij}^{LC} \phi_i \phi_j + \dots \tag{2.31}$$

Inclusion of these spill-in terms for both the electron density and the Hamiltonian integrals is mandatory. It ensures a seamless matching of the potential at the boundaries and critically stabilizes the convergence of the non-equilibrium self-consistent cycle.

2.2.4.3 Iterative Mixing and Convergence

The interdependence of the potential and the density necessitates an iterative solution. An initial guess for the potential is used to calculate the Hamiltonian, which yields a new density matrix via the NEGF formalism. This new density generates a new potential. Direct substitution is often unstable. Instead, the input potential for the next iteration is constructed by mixing the output potential with the input of the previous steps (e.g., using Pulay mixing). Convergence is achieved when the changes in the density and total energy fall below a strict tolerance. In open systems, the changing particle number adds complexity, requiring the minimization of a grand canonical potential rather than the standard internal energy.

2.2.5 Electronic Transport and Observables

Once the non-equilibrium density matrix has converged, the electronic structure of the open system is fully determined. The focus then shifts to calculating the transport observables that physically characterize the device.

2.2.5.1 Transmission Coefficients and the Landauer-Büttiker Formula

The primary observable in a two-probe transport setup is the steady-state electrical current I. Within the coherent transport regime the current is governed by the Landauer–Büttiker formalism neglecting inelastic scattering. It relates the macroscopic current to the microscopic probability of an electron transmitting from the left reservoir to the right reservoir.

The current $I(V)$ at a bias voltage V is calculated by integrating the transmission coefficient $\mathcal{T}(\epsilon)$ over the energy window defined by the electrochemical potentials of the electrodes:

$$I = \frac{2e}{h} \int_{-\infty}^{\infty} d\epsilon \mathcal{T}(\epsilon) \left[f\left(\frac{\epsilon - \mu_L}{k_B T_L}\right) - f\left(\frac{\epsilon - \mu_R}{k_B T_R}\right) \right] \quad . \tag{2.32}$$

The transmission coefficient $\mathcal{T}(\epsilon)$ quantifies the transparency of the scattering region at a specific energy ϵ. It is rigorously derived from the retarded Green's function $G^r(\epsilon)$ and the electrode broadening matrices $\mathbf{\Gamma}^{L/R}(\epsilon)$:

$$\mathcal{T}(\epsilon) = \mathrm{Tr}\left[G(\epsilon) \mathbf{\Gamma}^L(\epsilon) G^\dagger(\epsilon) \mathbf{\Gamma}^R(\epsilon) \right] \quad . \tag{2.33}$$

This trace formula encapsulates all interference effects within the central region. At zero temperature, the integral simplifies to the range $[\mu_L, \mu_R]$. At finite temperatures, the Fermi functions introduce thermal broadening, allowing contributions from states outside this window.

2.2.5.2 Finite-Bias Effects on Electronic Structure

The application of a finite bias voltage V does more than simply open an integration window for the current. It fundamentally alters the electronic landscape of the device. The electrostatic potential profile changes, often non-linearly. In systems with poor screening, the potential drop may not be smooth but can concentrate

at interfaces or specific bonds. Furthermore, the bias induces a re-hybridization of orbitals. Resonances that are sharp at zero bias may shift in energy or broaden as the coupling to the electrodes changes with the potential. A linear response approximation (using the zero-bias transmission for all voltages) fails to capture these effects. Full self-consistency at each bias point is required to correctly predict non-linear phenomena such as negative differential resistance or the saturation of conductance at high voltages.

Chapter 3

A Prototype 2D Metal-Semiconductor-Metal Device

3.1 Motivation

The semiconductor industry's quest for miniaturization has driven the exploration of new materials and innovative designs. Among these, 2D semiconductor materials have emerged as promising candidates due to their unique electrical conductivity and superior carrier transport properties, which address the limitations of conventional bulk semiconductors at the nanoscale. Understanding the electronic transport properties of 2D materials is essential for unlocking their full potential in emerging nanoelectronic applications.

Recently, we have designed 2D Janus Ge_2PAs (also referred to as GePAs), predicting that this structure would demonstrate exceptionally high and anisotropic carrier mobility along with robust thermodynamic stability [56]. The distinct electronic behavior of 2D Ge_2PAs arises from the specific bonding environment of atoms along one of the in-plane directions, which enables carrier mobility that

surpasses even the ultrahigh mobility observed in few-layered black phosphorus [57]. Moreover, the Ge_2PAs monolayer exhibits a strong optical absorption coefficient in both the visible and near-infrared (NIR) regions of the spectrum, significantly enhancing its ability to harvest photons across a wide range of wavelengths. Its anisotropic nature, combined with high carrier mobility along a particular direction, facilitates the efficient transport of photo-generated carriers, minimizing recombination losses and enabling a fast photoresponse. These combined properties make the Ge_2PAs monolayer an ideal candidate for broad-spectrum photodetectors capable of operating effectively in the visible and NIR regions [58].

While theoretical examinations based on density functional theory (DFT) provide valuable insights into the electronic properties of materials, it is imperative to assess the transport characteristics of devices fabricated with these materials for practical applications. The fundamental architecture, consisting of a semiconductor material sandwiched between two metal electrodes, is a common feature present in virtually every device system. Motivated by the promising properties of Janus Ge_2PAs monolayer, we conduct DFT simulations combined with the Nonequilibrium Green's Function (NEGF) method to investigate the impact of external factors, such as channel length and electrode doping concentration, on the performance of Ge_2PAs-based two-terminal metal-semiconductor-metal (MSM) devices in the ballistic region (sub-10 nm). To begin with, we obtain the electronic band structure of the pristine monolayer. Subsequently, we model the two-probe MSM nano-device and demonstrate the transmission coefficients ($[T(E)]$) of the devices under varying bias voltages. Next, we investigate the dependence of the I-V characteristics of the devices on different channel lengths and electrode doping concentrations. Finally, we explore the Schottky barrier (SB) heights and discuss their effect on carrier transport.

3.2 Methodology

The geometry optimization and electronic structure calculations were conducted using the DFT approach implemented in the Vienna Ab initio Simulation Package

(VASP) [59, 60]. The generalized gradient approximation with the Perdew-Burke-Ernzerhof (GGA-PBE) formalism [61] was chosen to approximate the exchange-correlation functional. Ion-electron interactions were treated using the projected augmented wave method (PAW) with a plane-wave cutoff energy of 530 eV [49]. The Brillouin zone (BZ) was sampled with a $24 \times 4 \times 1$ k-point mesh centered at Γ using the Monkhorst-Pack scheme [62]. To eliminate artificial interactions, a vacuum space of approximately 15 Å was introduced, which was found to be sufficient. Van der Waals (vdW) interactions were described using the Grimme method (DFT-D3) [63]. The lattice parameters and atomic positions were iteratively adjusted until the forces on the atoms were below 0.01 eV/Å, and the energy difference between consecutive steps was smaller than 10^{-5} eV.

The device model was constructed directly using the optimized structure, and simulations of the $T(E)$ and the I–V characteristics were conducted using the QuantumATK package [64]. QuantumATK provides a reliable framework for evaluating transport properties by integrating DFT calculations in conjunction with the Non-Equilibrium Green's Function (NEGF) technique [51]. The NEGF-DFT formalism was employed to model a two-probe system, which is divided into three regions: the left electrode (drain), the central region (channel), and the right electrode (source). The electrodes were modeled as semi-infinite periodic systems, with their properties were calculated using standard DFT techniques to define boundary conditions for the central region. The calculations began with an initial guess for the electron density, which was used to determine the effective potential (V_{eff}), including contributions from the Hartree and exchange-correlation terms. Using this effective potential, the Kohn–Sham Hamiltonian was constructed, and the Green's function for the central region was computed. The Green's function incorporated the coupling to the electrodes through self-energy terms (Σ^L and Σ^R). The density matrix was then derived from the Green's function, accounting for the coupling matrices (self-energy contributions) and the Fermi–Dirac distributions of the electrodes. The electron density was iteratively updated from the density matrix until convergence was achieved for V_{eff} and charge density. Once the system was converged, the transmission function ($T(E)$) was calculated.

In these simulations, the carrier transport direction was set along the x-axis,

with Monkhorst-Pack k-grid sampling specified as $201 \times 2 \times 1$. The atomic cores were represented using PseudoDojo pseudopotentials [65], and a medium numerical basis was utilized for the expansion of the wave function. The density mesh cutoff energy was set to 105 Ry to balance computational efficiency and accuracy. The electrode temperature was maintained at 300 K. Bulk properties were assigned to the left and right electrodes, and the initial step in the device simulation involved conducting bulk calculations for each electrode with Dirichlet boundary conditions applied at both the left and right boundaries. Periodic boundary conditions were applied in the directions perpendicular to the electron transport directions.

The self-consistent solution for the transmission coefficient $[T(E, V_b)]$ under different biases (V_b) was obtained using the retarded Green's function [66]:

$$T(E, V_b) = Tr[G(E, V_b)\Gamma^L G^\dagger(E, V_b)\Gamma^R] \tag{3.1}$$

where $\Gamma^{L(R)}$ is the broadening function of the left(right) electrode given by $\Gamma^{L(R)} = 1/i(\Sigma^{L(R)} - (\Sigma^{L(R)})^\dagger)$ with self-energy of the left(right) electrode $\Sigma^{L(R)}$. Applying a V_b across the device results in a shift of the chemical potentials of the left (μ_L) and right (μ_R) electrodes to $\mu_L = E_F + eV_b/2$ and $\mu_R = E_F - eV_b/2$, respectively. The current flow along the transport direction is then driven by the difference in chemical potential between the left and right electrodes. The current induced by a V_b, i.e., the I-V characteristics for the two-terminal system, was calculated using the Landauer-Büttiker formula within the framework of quantum transport formalism. This involves integrating the $T(E, V_b)$ within the bias window, which ranges from $-eV_b/2$ to $+eV_b/2$:

$$I(V_b) = \frac{2e}{h} \int_{\mu_L}^{\mu_R} T(E, V_b)[f_L(E, V_b) - f_R(E, V_b)]dE \tag{3.2}$$

where $f_L(E, V_b)$ and $f_R(E, V_b)$ are the Fermi distribution of the left and right electrodes, respectively.

3.3 Structural and Electronic Properties

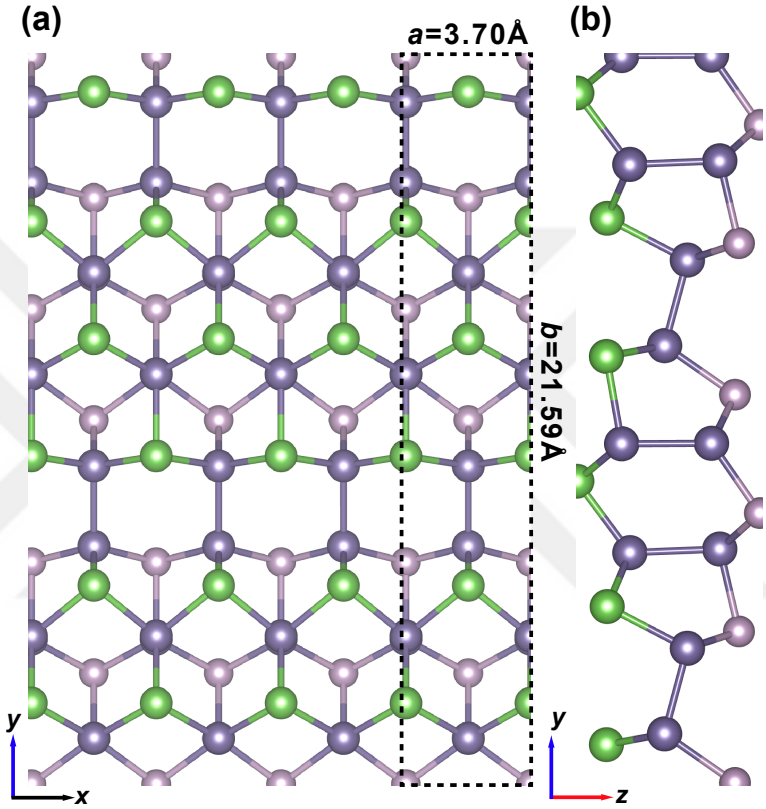


Figure 3.1: (a) Top and (b) side views of Janus Ge_2PAs monolayer. The dashed black rectangle denotes the unit cell. Germanium, phosphorus and arsenic atoms are depicted as purple, pink and green spheres, respectively.

This section of the thesis explores the structural characteristics of the 2D Ge_2PAs monolayer, as initially proposed in our previous work [56]. Inspired by recent advancements in ternary monolayer synthesis [67, 68] and the successful realization of 2D GeP [69] and GeAs [70], we designed 2D Ge_2PAs by substituting arsenic atoms into the topmost layer of 2D GeP. Upon substitution, the Janus Ge_2PAs monolayer exhibits the monoclinic C_s point group (Cm space group), distinguished by broken symmetries such as rotational and inversion symmetries, unlike the GeP and GeAs counterparts, which belong to the C_{2h} point group (C2/m space group). The Ge_2PAs structure adheres to the general electron counting rule, with germanium (Ge) atoms displaying 4-fold coordination, while phosphorus (P) and arsenic (As) atoms exhibit 3-fold coordination. This coordination pattern is

achieved through sp^3 hybridization, underlying the specific geometric arrangement of orbitals in the material. As shown in Fig. 3.1(a), the rectangular unit cell of Ge_2PAs consists of 12 Ge, 6 P, and 6 As atoms. The optimized lattice constants are $\boldsymbol{a}$ = 3.70 Å and $\boldsymbol{b}$ = 21.59 Å. The thermodynamic, mechanical, vibrational, and thermal stabilities have been previously demonstrated through cohesive energy analysis, phonon-dispersion calculations, and molecular dynamics simulations [56]. Considering the experimental progress on 2D Ge-based binary structures [69, 70] and 2D Janus materials [67, 68], the realization of Ge_2PAs monolayers and their integration into 2D heterostructures can be anticipated.

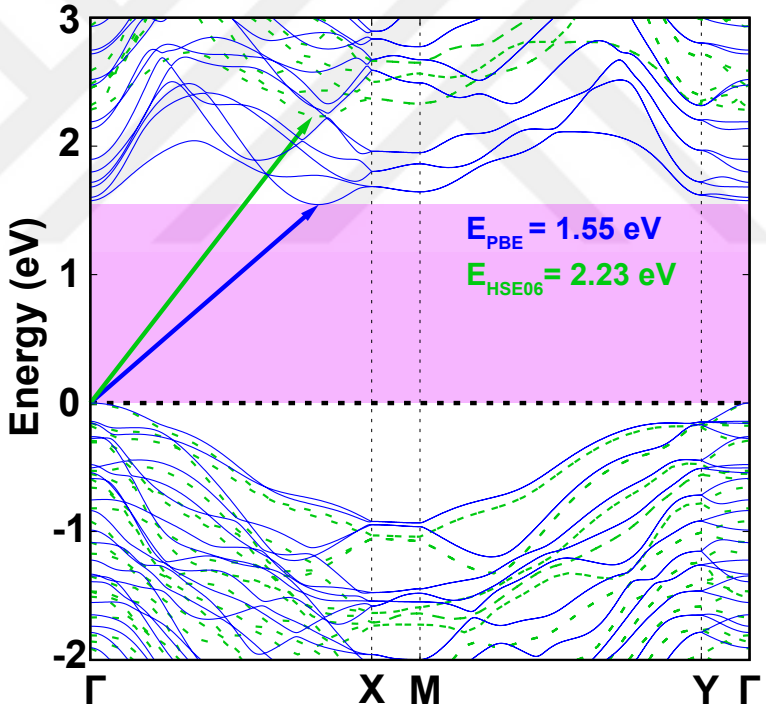


Figure 3.2: The electronic band structure of Ge_2PAs monolayer. The results for PBE and HSE06 are shown with solid blue and dashed green lines, respectively. The Fermi level is set to zero.

The investigation of the electronic properties of materials is of profound significance, representing the foundational framework for the strategic design and optimization of materials tailored for electronic devices. In this respect, our attention now turns toward the analysis of the electronic characteristics of the

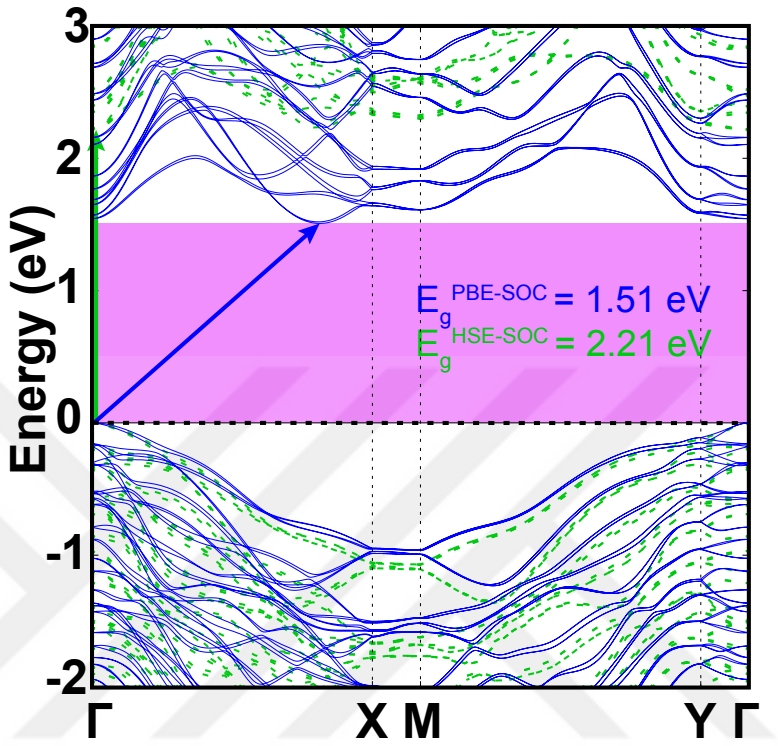


Figure 3.3: The electronic band structure of Ge_2PAs monolayer. The results for PBE+SOC and HSE06+SOC are shown with solid blue and dashed green lines, respectively. The Fermi level is set to zero.

monolayer. Fig. 3.2 illustrates the electronic band structure of the Ge_2PAs monolayer, computed using GGA-PBE and HSE06 methods. The determined band gap values are 1.55 eV and 2.23 eV for PBE and HSE calculations, respectively. Given the potential impact of spin–orbit coupling (SOC) on the band structure, we also examined the band structures of the monolayer with SOC, as shown in Fig. 3.3. The results indicate that SOC exerted only a minimal influence on the calculated band structure, with no significant alteration to the characteristics and shapes of the electronic bands. The observed variations in the dispersion profiles along the $\Gamma - x$ and $\Gamma - y$ directions near the Fermi level indicate a notable in-plane anisotropy. This anisotropy, evident in dispersion profiles, is underscored by quantitative evidence from mobility values reported in our previous study [56], where electron and hole mobilities in the x-direction have been found to be much higher than those in the y-direction.

3.4 2D Metal–Semiconductor–Metal Device Architecture

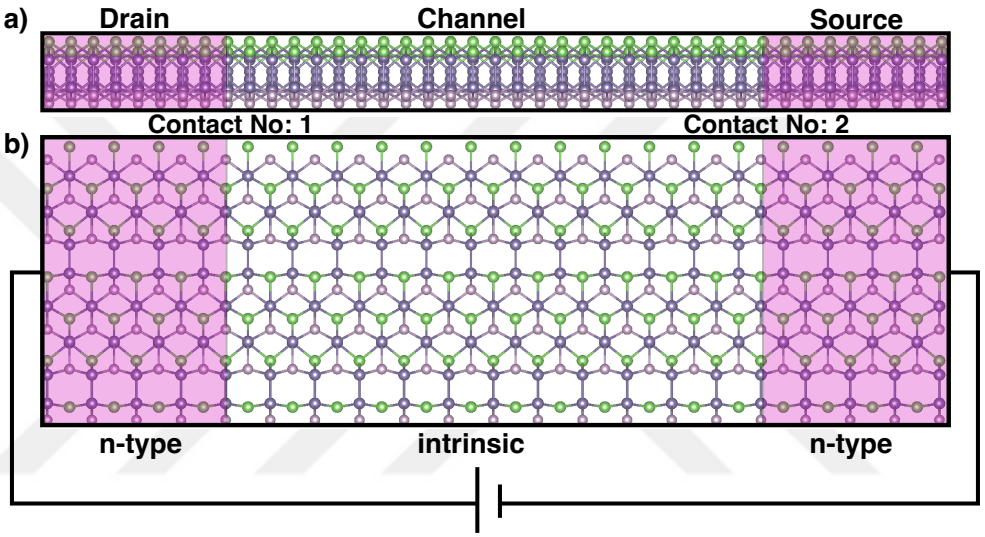


Figure 3.4: Schematic diagrams of the two-probe configuration in (a) side view and (b) top view. Germanium, phosphorus, and arsenic atoms are presented as purple, pink, and green spheres, respectively.

Acknowledging the fundamental importance of 2D semiconductors in modern technology, a comprehensive understanding of electronic properties and their direct correlation with transport properties is pivotal for advancing current technologies. Considering the anisotropic electronic properties of 2D Janus Ge_2PAs monolayer, we investigated its transport properties by focusing on the high mobility direction as the preferred transport axis. In addition to its low carrier mobility, the y-direction also exhibits a significantly larger lattice constant ($\boldsymbol{b}$ = 21.59 Å). As a result, achieving proper electrostatic screening in this direction requires device lengths that exceed the ballistic transport regime. Therefore, we limited our analysis to the x-direction. Fig. 3.4 illustrates the schematic design of a two-probe MSM nano-device used in our simulations. In this schematic, the pink-shaded areas represent the left and right electrodes, while the unshaded area depicts the channel region. The setup involves connecting a left and a right semi-infinite

electron reservoir through a central region that encompasses the interfaces under consideration.

The contact interface between a semiconductor and its external metallic electrodes is crucial for both device performance and the accurate assessment of the material's transport properties [71]. The interface characteristics are primarily governed by the SB, which represents the difference between the metal's work function and the electron affinity of the semiconductor. This difference creates an energy barrier that hinders the flow of charges between the semiconductor and the metal [72]. While SB can provide useful rectifying properties and enable high-speed switching in certain systems, in some cases the presence of an SB is undesirable due to its association with increased energy consumption and the complications it poses in directly examining the intrinsic characteristics of semiconductor materials, especially for 2D semiconductor devices [71]. Thus, within semiconductor device engineering, achieving low SB values or Ohmic contact remains a central goal to reduce energy consumption and extend device lifespan. Common contact types typically consist of three main configurations: top contact, side contact, and vdW contact. However, these contacts often create challenges in achieving Ohmic or low SB behavior in real devices due to the presence of defects, vdW gaps, and manufacturing difficulties. To address these challenges, a novel type of configuration called atomic-level seamless contact has been developed [73]. This approach involves directly connecting low-dimensional metals and semiconductors with native chemical bonds, resulting in a contact that mitigates factors such as lattice mismatch between different materials and ensures a consistent and homogeneous environment for evaluating transport properties.

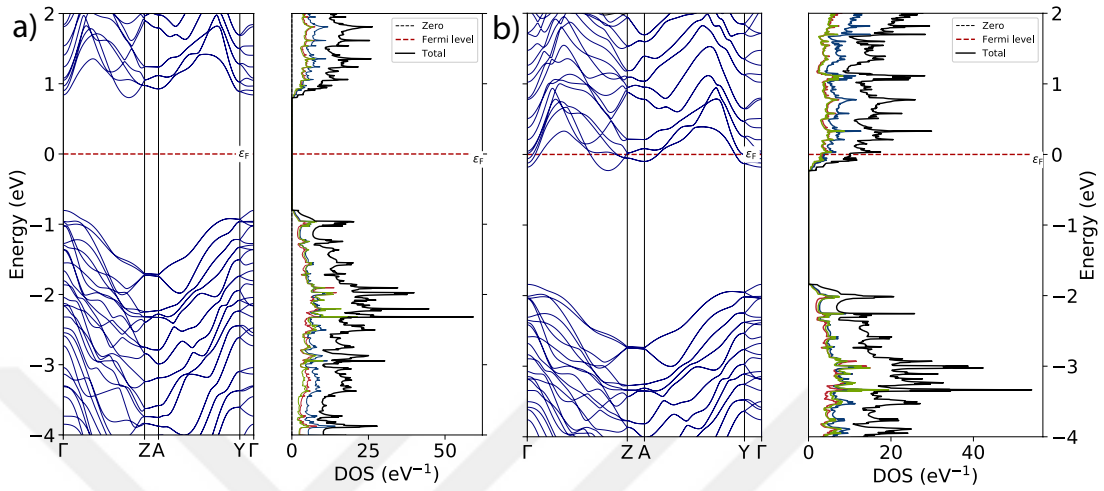


Figure 3.5: Band structures and projected density of states of (a) undoped and (b) n-type doped Ge_2PAs electrode with a value of 2.25 $\times$ 10^{14} cm^{-2} doping concentration are presented, respectively. The Fermi level is set to zero.

We adopted a strategy commonly found in the literature [74, 75, 76, 77, 78, 79, 80], utilizing intrinsic 2D Ge_2PAs as the channel material while employing highly doped Ge_2PAs for both electrodes. In this respect, we employed the electrostatic doping method, which involves introducing localized charges that are individually attached to each atom [51, 55]. This method has been demonstrated experimentally and has been shown to achieve electrically tunable doping levels of up to 10^{14} cm^{-2} in ultra-thin TMDs [81]. It is important to note that the structural stability is maintained under electrostatic doping, and the overall band structure, aside from the expected Fermi level shift, remains essentially unaltered as shown in Fig. 3.5. This assumption is supported by experimental evidence obtained from two-terminal graphene devices [82].

When the metallicity of the electrodes is ensured through doping, the resulting structure can be simplified into a MSM configuration. An MSM structure essentially consists of two back-to-back Schottky contacts [83]. Each metal-semiconductor junction forms an SB due to the work function difference between the metal and the semiconductor. This arrangement is crucial for controlling the current flow through the device. Under an applied voltage, the two contacts exhibit

different behaviors. Contact No. 1 undergoes reverse bias, where the voltage enhances the SB and hinders charge carrier injection from metal to semiconductor. Conversely, Contact No. 2 experiences forward bias, where the voltage reduces the SB and facilitates charge carrier injection. This differential biasing of the two contacts creates a potential difference across the semiconductor layer, driving the flow of current. By manipulating the SB heights through controlled biasing, MSM devices enable modulation of charge carrier transport and, consequently, the device's electronic characteristics.

3.5 Bias–Dependent Transmission Spectra as a Function of Channel Length and Electrode Doping Concentration

In our investigation of the transport properties within the 2D Janus Ge_2PAs structure, we considered a range of electrode doping concentrations to mimic metallic electrodes with different work functions. Since the work function of a material directly depends on factors such as density of states (DOS), temperature, carrier density, and doping concentration [84], adjusting these parameters can emulate the characteristics of various metallic materials. In the present case, the selected doping concentrations for the electrodes are 0.015, 0.045, and 0.075 e/atom, corresponding to 4.51×10^{13}, 1.35×10^{14} and 2.25×10^{14} cm^{-2}, respectively, which fall within experimentally achievable limits [81]. At the first concentration level, the Ge_2PAs electrodes begin to exhibit metallic properties. At the second and third concentrations, they represent scenarios of moderate and heavy doping, respectively [85, 86]. Under these conditions, the Fermi level of the electrodes is shifted 0.02 eV, 0.16 eV, and 0.24 eV above the conduction band minimum. Furthermore, we systematically investigated three channel lengths: 3.0, 4.5, and 6.5 nm at each doping level, aiming to identify the shortest possible sub-10 nm device configuration. Additionally, we also considered heavier doping concentrations of 3.16×10^{14} cm^{-2} and 6.01×10^{14} cm^{-2} for the longest case. This exploration was

designed to elucidate how variations in channel length and doping concentration influence the electronic transport properties of the Janus Ge_2PAs-based MSM devices.

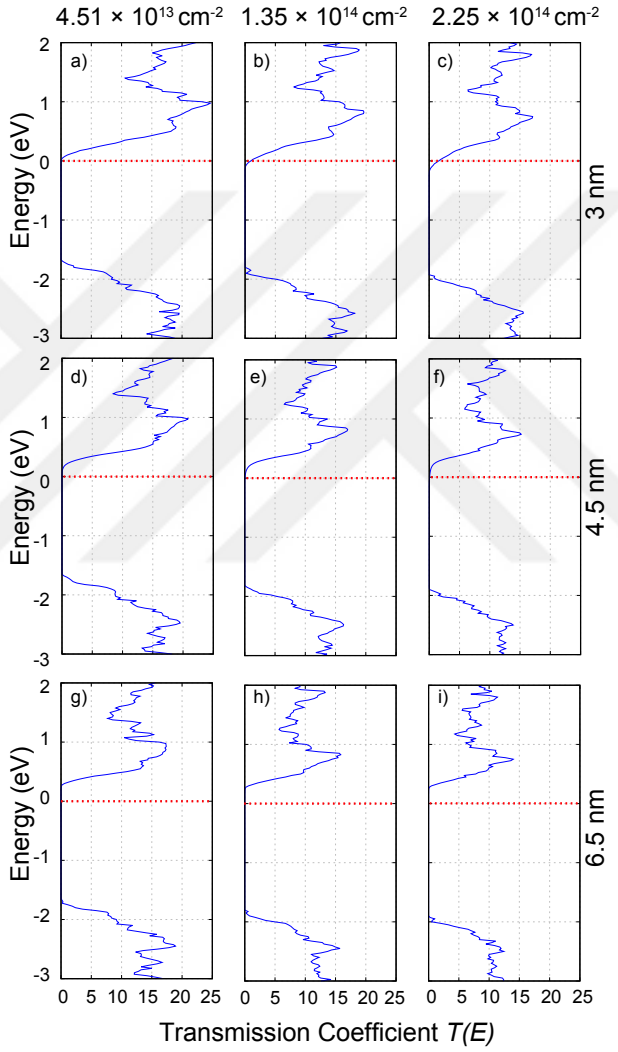


Figure 3.6: Transmission spectra of devices with increasing electrode doping concentration from left to right. (a-c) 3 nm (d-f) 4.5 nm (g-i) with 6.5 nm channel length under 0 V bias

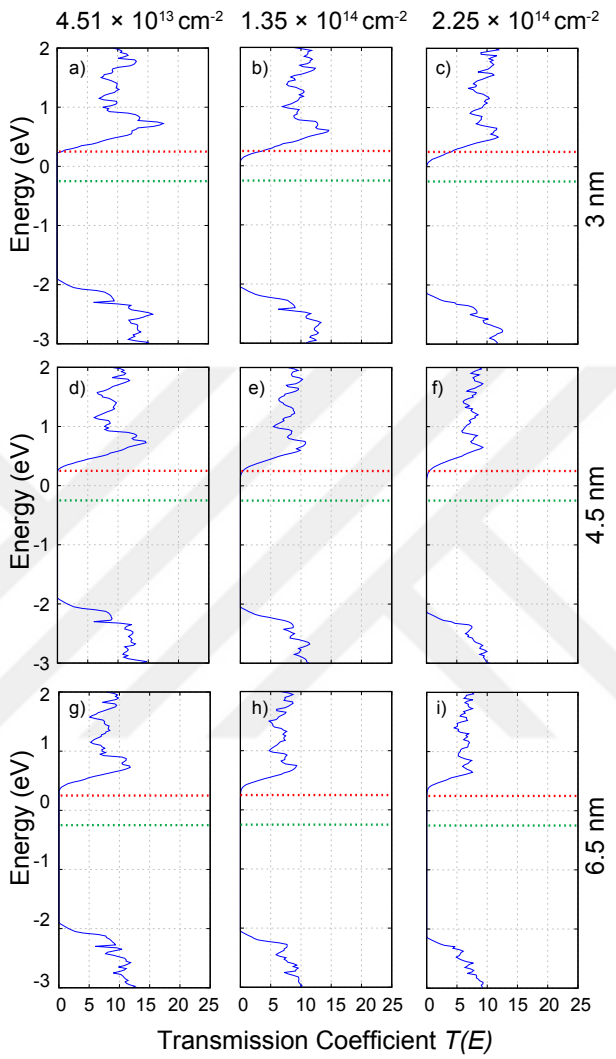


Figure 3.7: Transmission spectra of devices with increasing electrode doping concentration from left to right. (a-c) 3 nm (d-f) 4.5 nm (g-i) with 6.5 nm channel length under 0.5 V bias

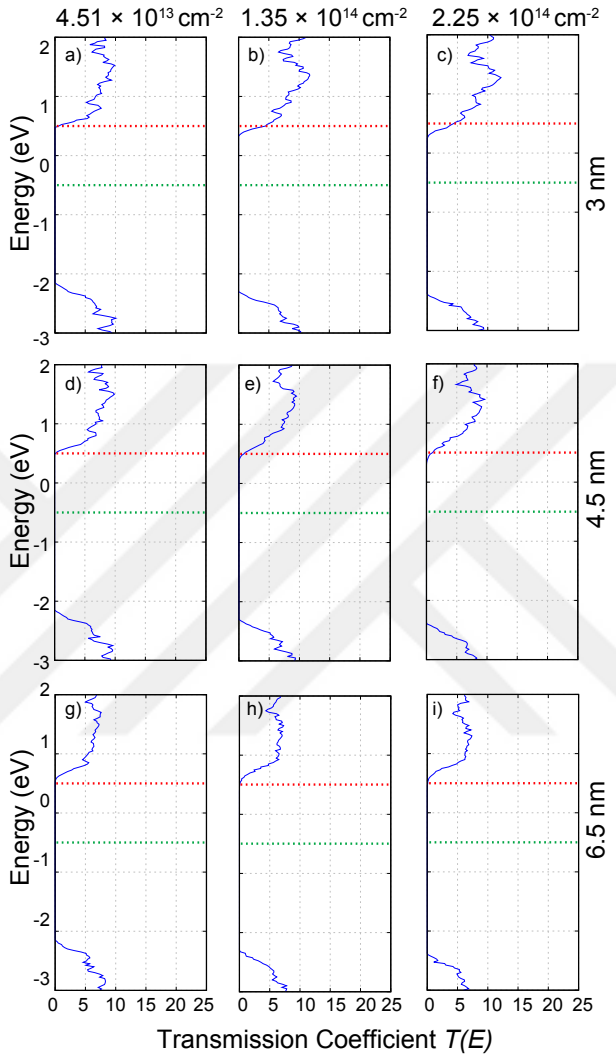


Figure 3.8: Transmission spectra of devices with increasing electrode doping concentration from left to right. (a-c) 3 nm (d-f) 4.5 nm (g-i) with 6.5 nm channel length under 1 V bias

To investigate ballistic transport in devices with the specified parameters, we began by calculating the transmission spectra under equilibrium (0 V) and non-equilibrium conditions (0.5 V and 1 V). The complete set of results is presented in Figs. 3.6, 3.7 , and 3.8 for bias voltages of 0 V, 0.5 V and 1 V, respectively. Each figure employs a consistent layout: the plots from left to right within rows correspond to devices with increasing doping concentrations at a constant channel length, while plots from top to bottom within the columns belong to devices with

increasing channel length at a constant doping concentration. In the transmission spectra for 0 V bias,red dashed lines denote the Fermi level of the device. Similarly, for biased cases, red and green dashed lines represent the Fermi levels of the right and left electrodes, respectively.

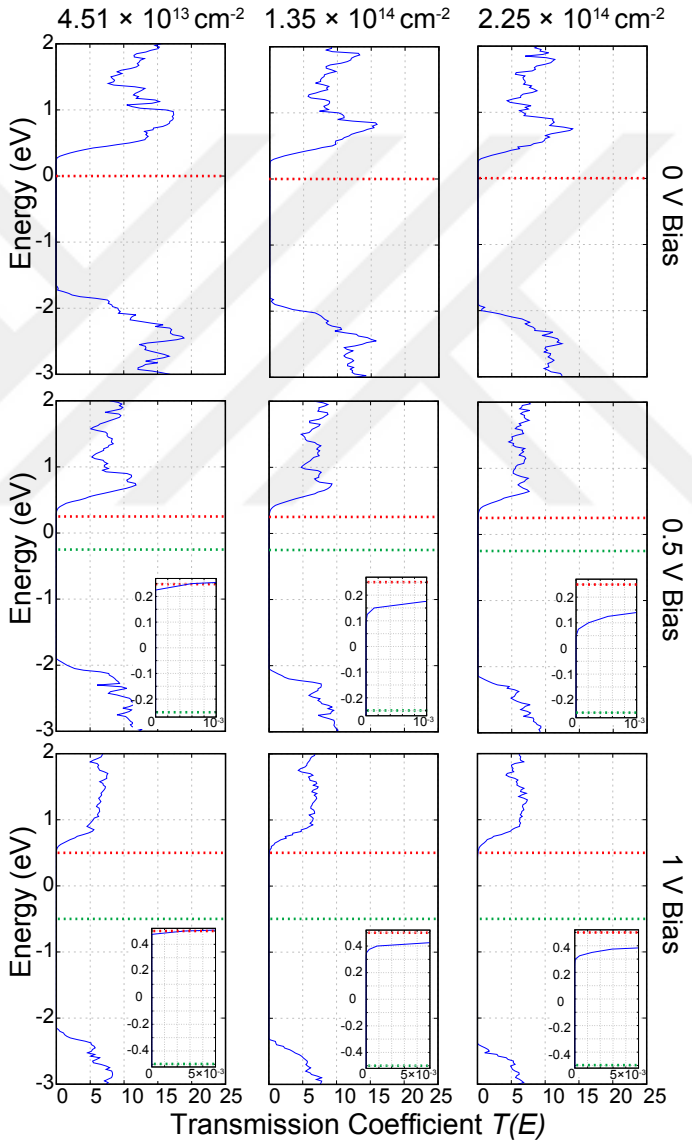


Figure 3.9: Transmission spectra of devices with 6.5 nm channel length and 4.51 $\times$ 10^{13}, 1.35 $\times$ 10^{14} and 2.25 $\times$ 10^{14} cm^{-2} under 0, 0.5 and 1 V biases. In the first row (0 V bias), red dashed lines indicate the Fermi level of the devices. In biased cases, the red and green dashed lines represent the Fermi levels of the right and left electrodes, respectively.

We selected the results of the longest device (channel length of 6.5 nm) as the representative case to discuss the physical picture in the remainder of this section of the thesis. Transmission spectra of the 6.5 nm device under bias voltages of 0 V, 0.5 V and 1 V are shown in the Fig. 3.9. Plots progress from left to right for increasing doping concentration. At zero bias, the transmission spectra exhibit a transmission gap, indicative of the semiconducting nature of the channel. The width of this gap is influenced by the electrode doping, with a slight increase observed for higher doping levels. When a finite bias is applied, transmission within the bias window becomes evident, which signifies the presence of current flow through the device. The inset of Fig. 3.9 further demonstrates that the transmission probability within the bias window is enhanced with increasing bias voltage. Additionally, a positive correlation is observed between electrode doping concentration and the overall transmission values.

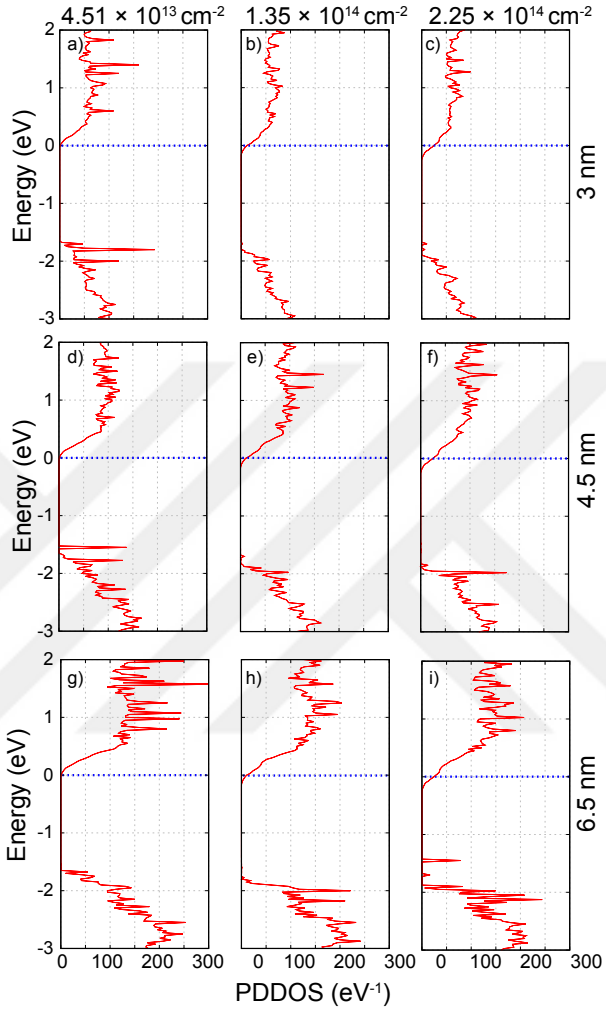


Figure 3.10: Projected density of states of devices with increasing electrode doping concentration from left to right. (a-c) 3 nm (d-f) 4.5 nm (g-i) with 6.5 nm channel length under 0 V bias

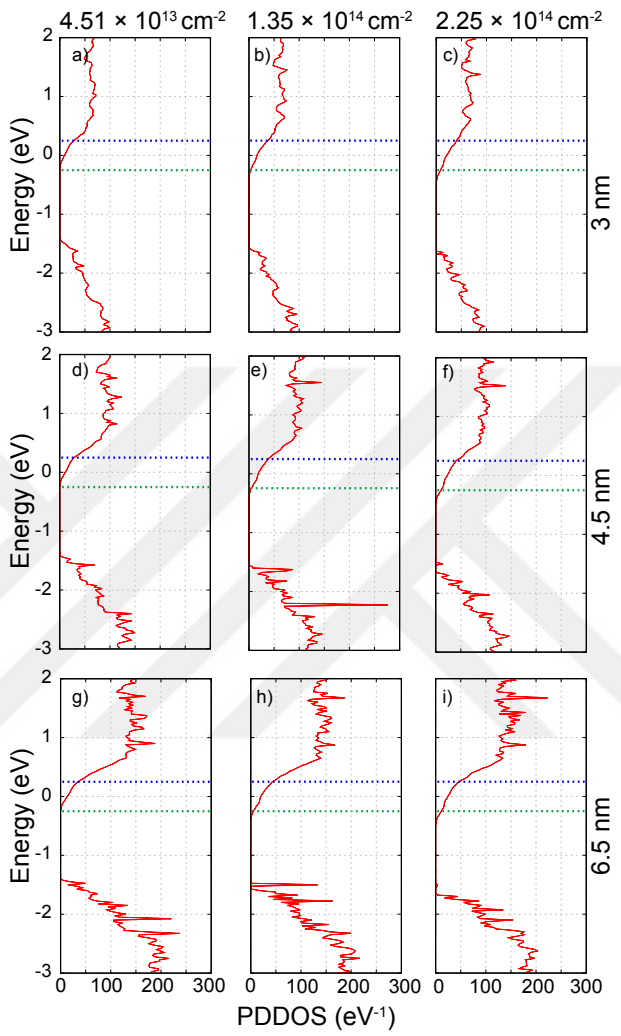


Figure 3.11: Projected density of states of devices with increasing electrode doping concentration from left to right. (a-c) 3 nm (d-f) 4.5 nm (g-i) with 6.5 nm channel length under 0.5 V bias

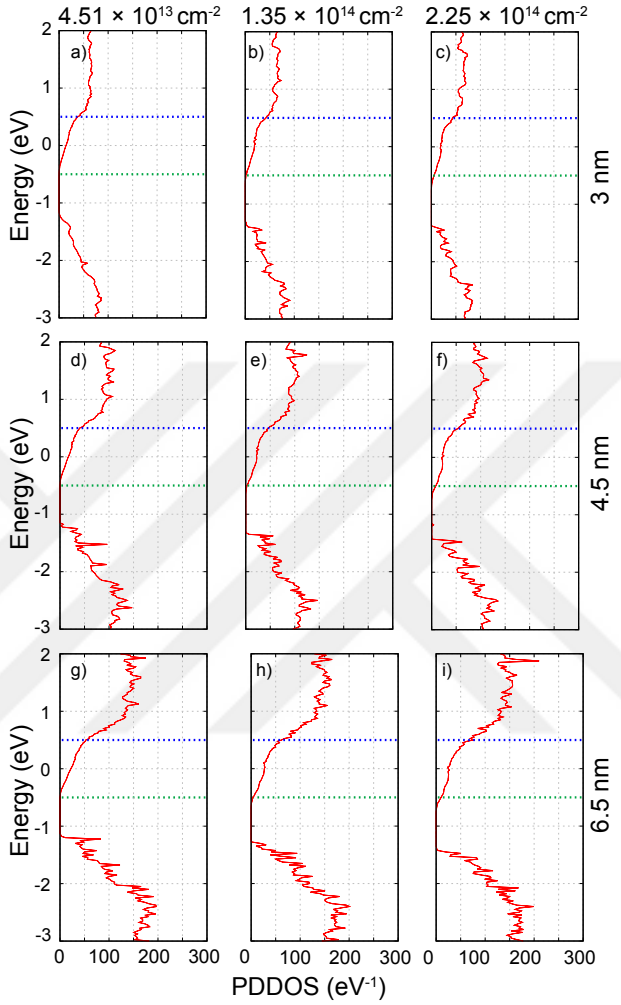


Figure 3.12: Projected density of states of devices with increasing electrode doping concentration from left to right. (a-c) 3 nm (d-f) 4.5 nm (g-i) with 6.5 nm channel length under 1 V bias

3.6 Projected Device Density of States Under Applied Bias

To elucidate the origin of the observed transmission values and their dependence on applied bias, we calculated the bias-dependent projected device density of states (PDDOS). The complete set of results for bias voltages of 0 V, 0.5 V,

and 1 V are presented in Figs. 3.10, 3.11 , and 3.12, respectively. These figures maintain the same organizational layout as the provided transmission spectra data. The blue dashed lines at 0 V of PDDOS plots indicate the device's Fermi level. Similarly, for biased cases, the blue and green dashed lines represent the Fermi levels of the right and left electrodes, respectively. The results for 6.5 nm device under different biases are shown in Fig. 3.13. A strong correlation is observed between the PDDOS pattern and the previously discussed transmission spectra. Both diagrams for the devices in equilibrium conditions (0 V bias) depict a wide energy range around the Fermi level with low PDDOS values, signifying the semiconducting nature of the Janus Ge_2PAs monolayer. Under a finite bias, a non-zero DOS emerges within the bias window. Within this window, regions with the highest DOS contribute most significantly to the overall transmission observed in the system, facilitating the current flow through the device. The observed correlation between the higher transmission values and the increased electrode doping concentration can be attributed to the corresponding rise in the DOS across the device. This enhancement in the DOS directly influences the electronic behavior of the device. Moreover, the bias level effectively amplifies the DOS within the bias window, further increasing the availability of electronic states for transmission.

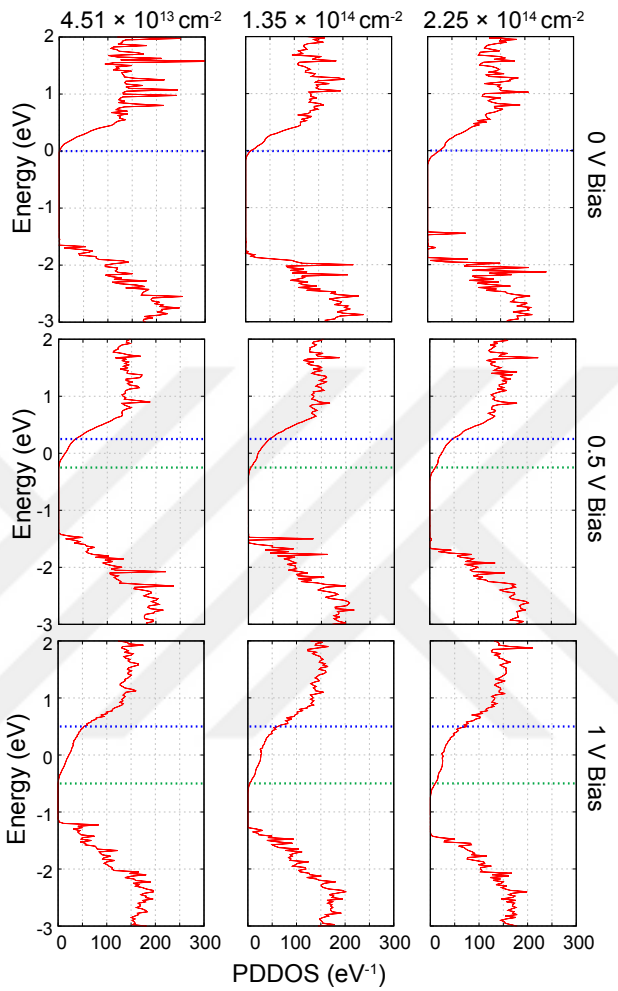


Figure 3.13: Projected device density of states (PDDOS) of devices with 6.5 nm channel length and 4.51×10^{13} , 1.35×10^{14} and 2.25×10^{14} cm^{-2} under 0, 0.5 and 1 V biases. In the first row (0 V bias), blue dashed lines indicate the Fermi level of the devices. In biased cases, the blue and green dashed lines represent the Fermi levels of the right and left electrodes, respectively.

3.7 Current–Voltage Characteristics

We proceeded to examine the I-V characteristics of the modeled devices at 300 K. For these calculations, the applied bias voltage was swept across two electrodes within the range of -1 to +1 V, in increments of 0.1 V. To ensure computational

efficiency and convergence, the density matrix obtained from each previous bias step was used as the initial guess for the subsequent calculation. The resulting I-V curves are presented in Fig. 3.14 and Fig. 3.15. The I-V curves exhibit a noticeable symmetry in the forward and reverse currents across various applied bias voltages, consistent with the design of symmetrical electrodes in the MSM configuration. However, an apparent deviation is observed for the device with a 3 nm channel length, which exhibits significantly higher current levels.

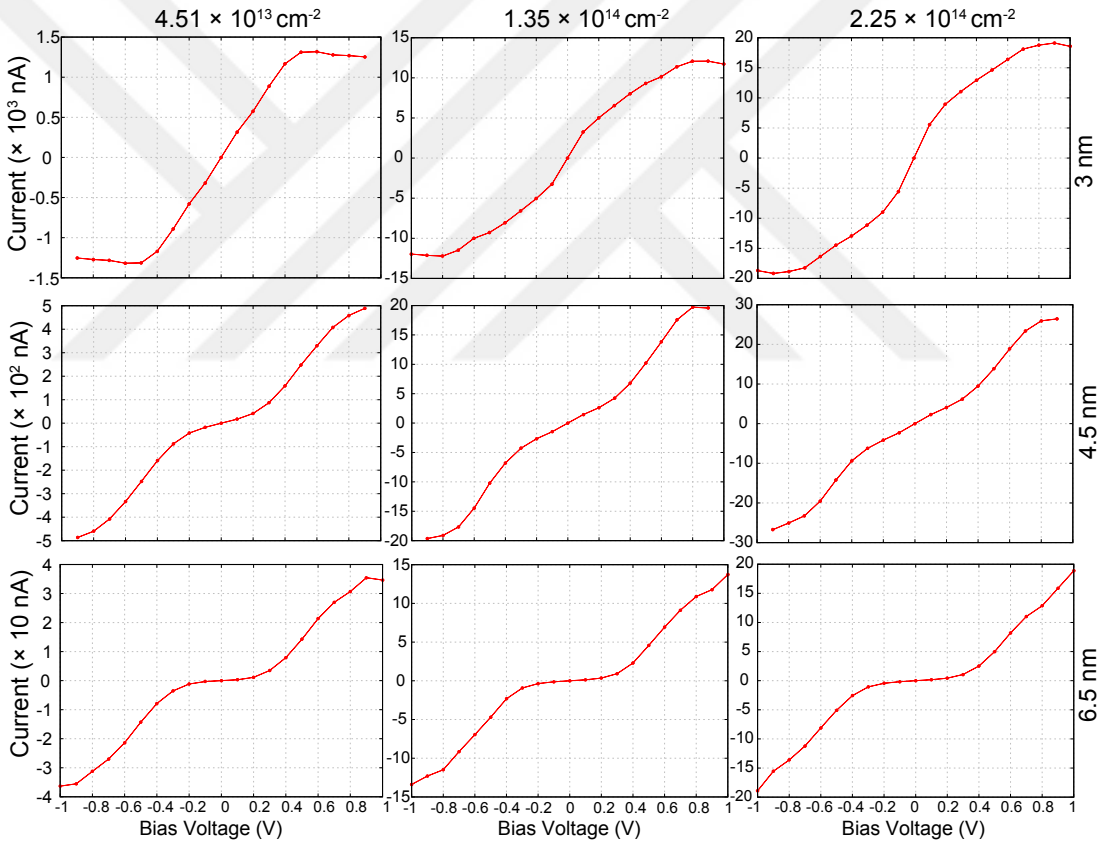


Figure 3.14: Computed I-V characteristic curves of Ge_2PAs devices with increasing electrode doping concentration from left to right. The first row displays the I-V curves for a channel length of 3 nm, the second row for 4.5 nm, and the third row for 6.5 nm.

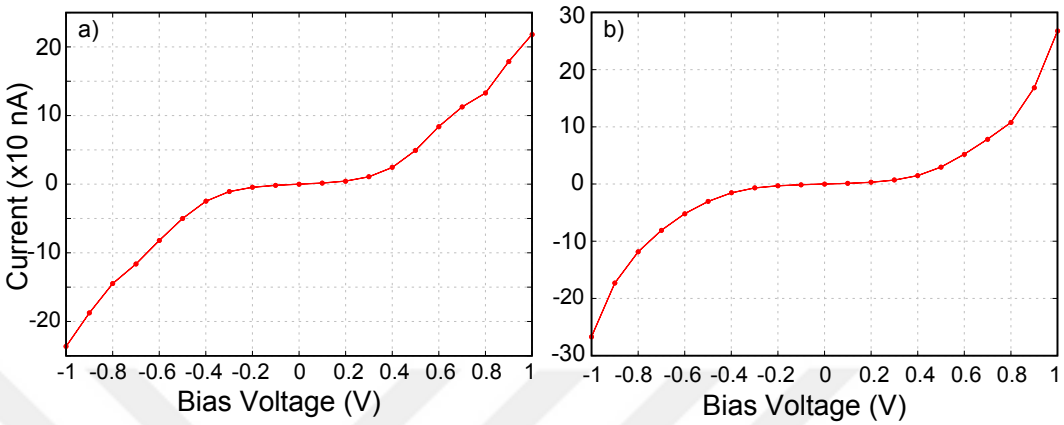


Figure 3.15: Computed I-V characteristic curves for the Ge_2PAs device with doping concentrations of (a) 3.16×10^{14} cm^{-2} and (b) 6.01×10^{14} cm^{-2}, and a channel length of 6.5 nm.

3.8 Hartree Difference Potential Analysis

To elucidate the behavior that is observed in the previous section, we calculated the Hartree Difference Potential (HDP) and its spatial derivative along the transport direction at 0 V bias for all device configurations, as provided in Figs. 3.16 and 3.17. In the NEGF formalism, it is crucial for the electrostatic potential to reach equilibrium and becomes flat before reaching the electrode boundary. However, the shortest device configuration does not satisfy this criterion. Furthermore, while the HDP profile improves for devices with a 4.5 nm channel length, they still exhibit high current in the low bias region, which deviates from the expected behavior for a semiconducting channel. Consequently, it is determined that the shortest operable device should have a channel length of 6.5 nm, aligning with typical behavior observed in theoretical and experimental studies of MSM devices [87, 88]. Furthermore, while the observed trends suggest a transition from coherent ballistic transport to electrostatic breakdown governed by channel length and doping concentration, defining a quantitative threshold remains challenging within the scope of the coherent NEGF framework.

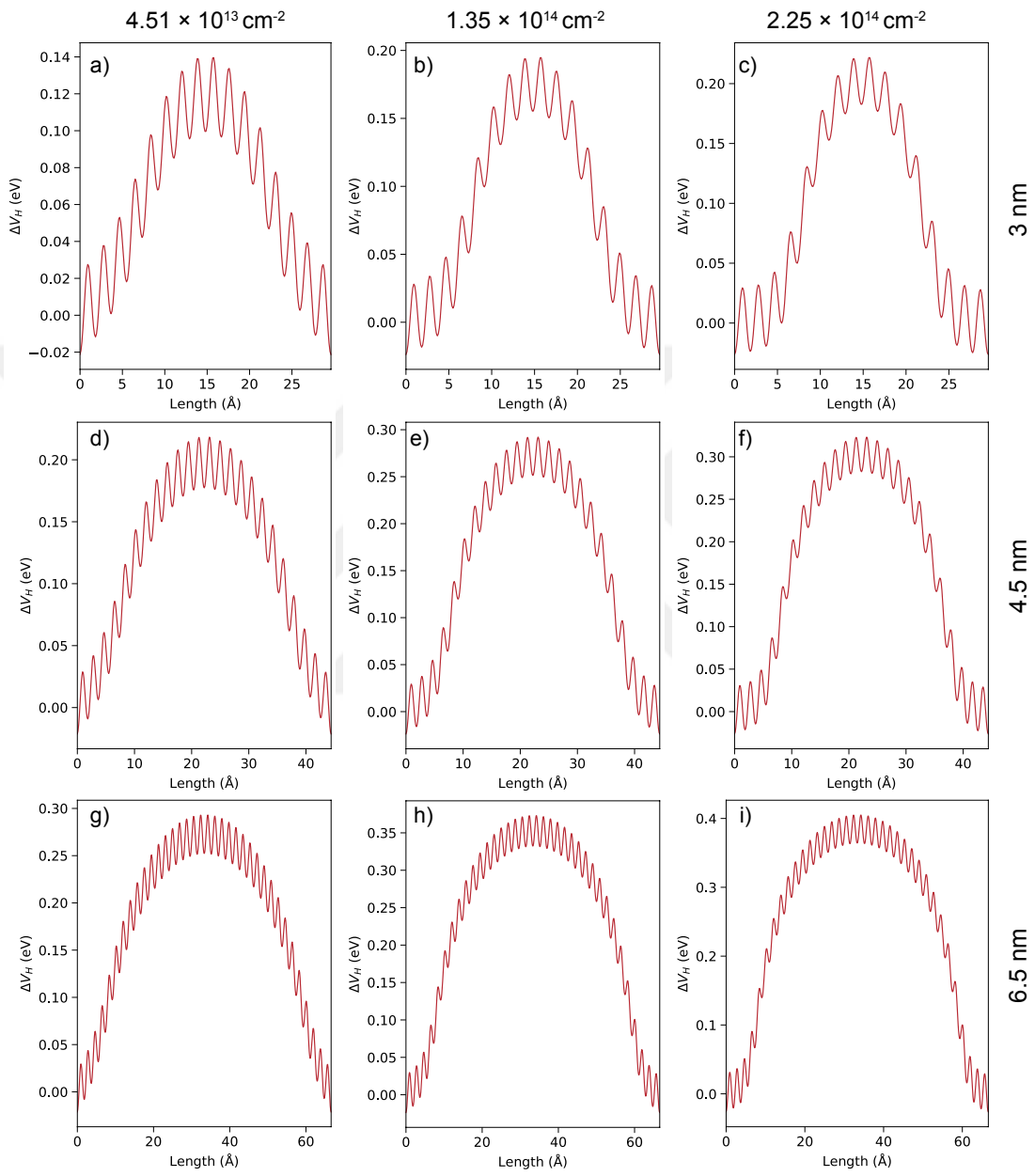


Figure 3.16: Hartree Difference Potential of devices with increasing electrode doping concentration from left to right. (a-c) 3 nm (d-f) 4.5 nm (g-i) with 6.5 nm channel length under 0 V bias

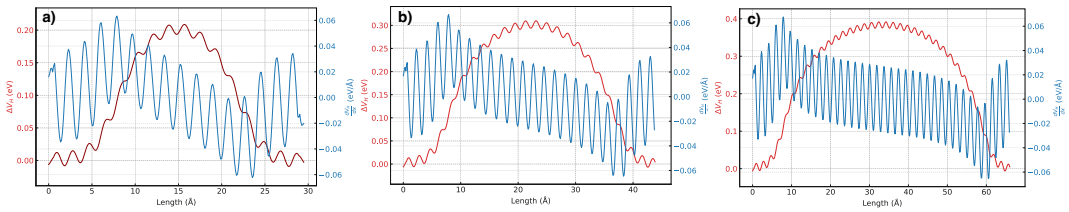


Figure 3.17: Hartree difference potential and its derivative along the transport direction for Ge_2PAs MSM devices with electrode doping of 2.25×10^{14} cm^2 and channel lengths of (a) 3 nm, (b) 4.5 nm, and (c) 6.5 nm.

3.9 The Differential Conductance and the Impact of p-type Doping

Increasing the electrode doping concentration leads to a considerable enhancement in the current values. This result aligns with the Landauer-Büttiker formula, which suggests that the magnitude of the current can be accurately calculated by integrating the area of transmission spectra within the bias window. The observed non-linearity in the I-V curves suggest that the electrical behavior at the metal-semiconductor interface is predominantly governed by the SB. To provide additional insight, we calculated the differential conductance, $G = dI/dV$ for the 6.5 nm MSM device with an electrode doping concentration of 2.25×10^{14} cm^{-2}. As shown in Fig. 3.18, the resulting curve exhibits a minimum near zero bias, indicating suppressed carrier injection due to the SB, followed by a monotonic increase at higher biases.

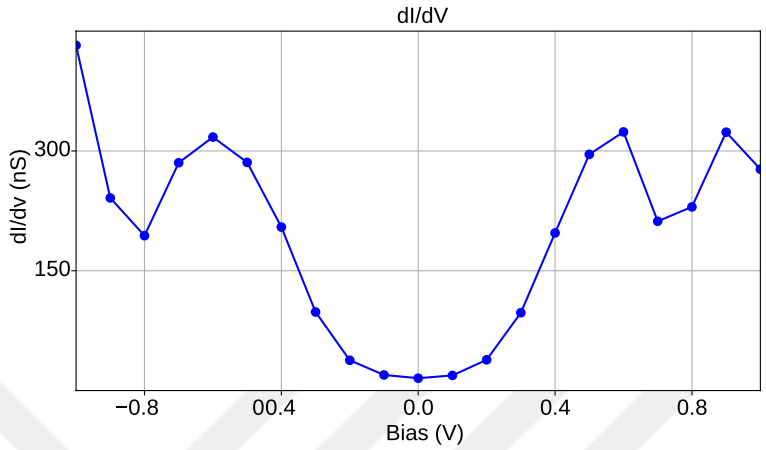


Figure 3.18: Differential conductance dI/dV as a function of bias voltage for the 6.5 nm Ge_2PAs MSM device with an electrode doping of $2.25{\times}10^{14}$ cm^{-2}

This trend is consistent with enhanced tunneling and thermionic emission as the barrier width and height are reduced with increasing bias. Such behavior serves as a useful proxy for characterizing bias-dependent contact resistance under ideal ballistic conditions. Additionally, for this configuration, the I_{off} and I_{on} are calculated to be 3.9×10^{-11} A and 1.9×10^{-7} A, respectively, resulting in an on/off ratio of $\sim 4.9 \times 10^3$, also illustrated in Fig. 3.19. This level of performance is regarded as adequate for applications including low-power switching circuits, sensing devices, and early-stage prototype designs, where a moderate on/off ratio combined with pronounced SB modulation can provide sufficient signal contrast for device functionality [89, 90, 91].

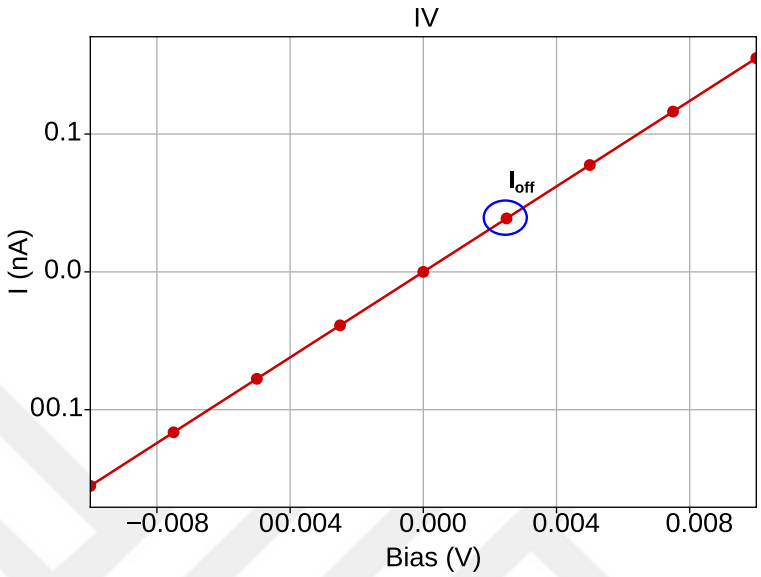


Figure 3.19: Current–voltage (I–V) characteristics of the 6.5 nm Ge_2PAs MSM device along the x-direction with a doping concentration of 2.25×10^{14} cm^{-2}, calculated in a narrow bias range to extract the on/off current ratio.

To address the possible impact of p-type doping, we performed additional calculations using the longest device configuration and the highest doping concentration. The results reveal that the transport behavior under p-type doping is nearly identical to that observed for n-type doping (Fig. 3.20). This similarity extends to trends in current magnitude and overall transport characteristics, which are in line with the intrinsic properties of the material. As demonstrated in our previous study [56], the hole mobility of the 2D Ge_2PAs is comparable to its electron mobility along the high-mobility direction. This equivalence in carrier mobility explains the observed similarities in transport behavior between p-type and n-type doping scenarios.

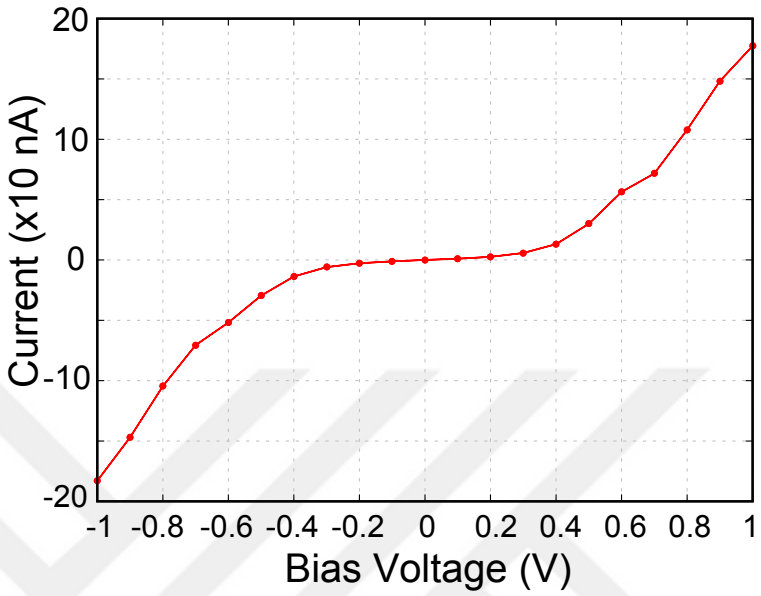


Figure 3.20: Computed I-V characteristic curve for the p-type Ge_2PAs device with a doping concentration of 2.25×10^{14} and a channel length of 6.5 nm.

3.10 Influence of Bias and Doping on Schottky Barrier Formation

To understand the role of the Schottky mechanism in devices with a 6.5 nm channel length, we analyzed how the SB height (SBH) varies with applied bias and doping concentration. Projected local density of states (PLDOS) calculations were performed at zero and finite bias voltages for different doping levels. PLDOS offers a comprehensive view of the device band diagram, facilitating a detailed analysis of the SB. The SBH is determined by the energy difference between the Fermi level of the metal and the conduction band minimum (CBM) of the semiconductor at the metal-semiconductor interface. Under equilibrium conditions (zero bias), this energy difference can be equivalently expressed as the difference between the metal's work function and the semiconductor's electron affinity. When a bias is applied, the SBH is estimated by the energy difference between the CBM of the metallic electrode and the CBM of the semiconductor region [80]. The complete

set of results is presented in Fig. 3.21 and Fig. 3.22, where the latter specifically highlights the conduction band edges for a clearer depiction of the SBH values. Different colors represent absolute values of the DOS, with the intensity increasing from black to red, as indicated by the color bars on the right-hand side.

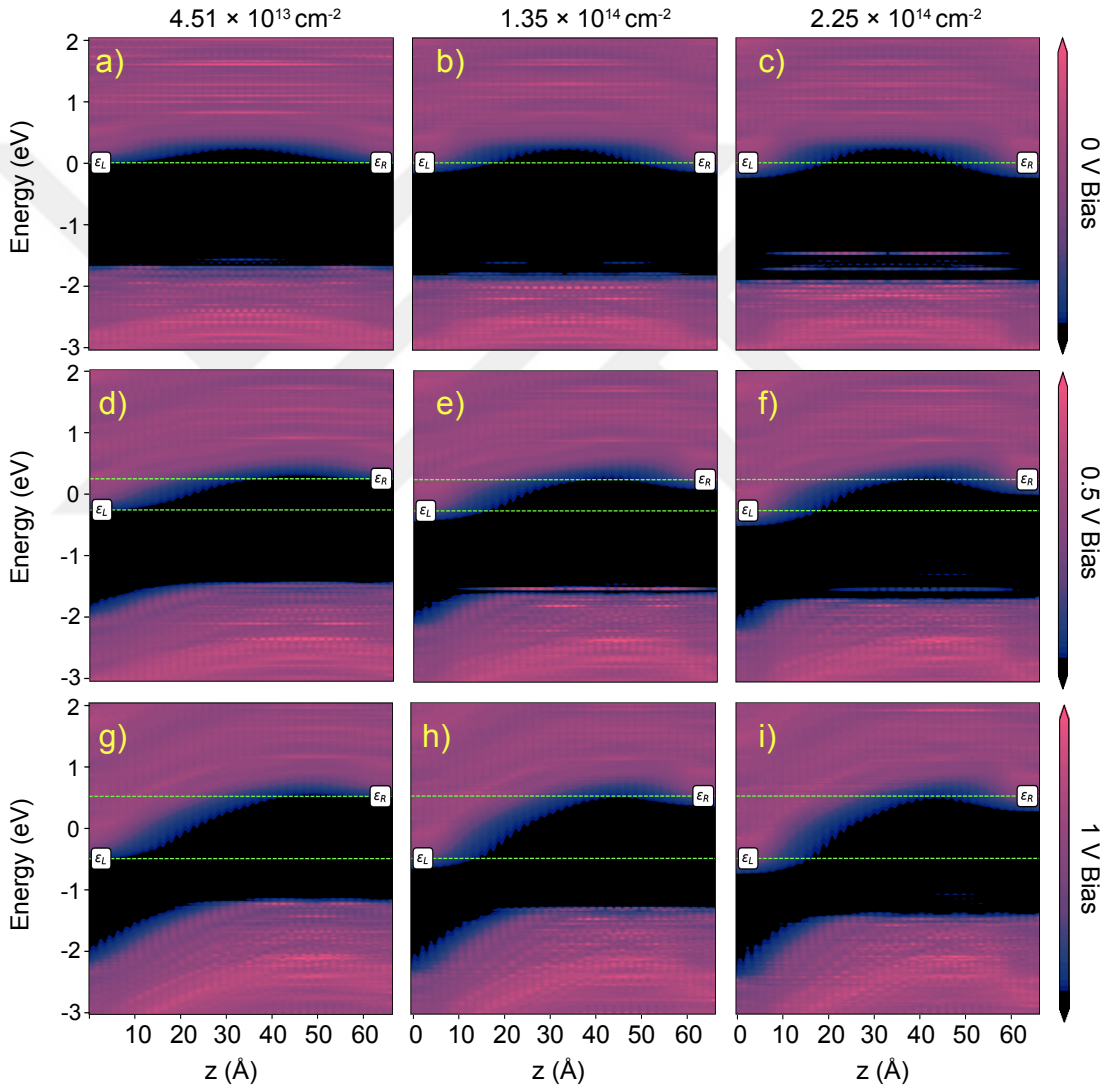


Figure 3.21: Projected local density of states of devices with 6.5 nm channel length under (a-c) 0 V bias, (d-f) 0.5 V bias, (g-i) 1 V bias

Fig. 3.22 (a-c) depict the PLDOS under equilibrium (zero bias) conditions for varying doping levels. These results demonstrate that increasing the electrode doping concentration leads to a shift of the Fermi level (green dashed lines) toward

higher energies within the conduction band. However, the SBH itself remains unaffected at zero bias. In contrast, the SBH increases with doping under finite bias conditions, as shown in Fig. 3.22 (d-f) and (g-i) for voltages 0.5 V and 1 V, respectively. For devices with low doping concentration, the SBH exhibits a decrease with increasing bias voltage. This behavior facilitates easier transport of charge carriers across the barrier.

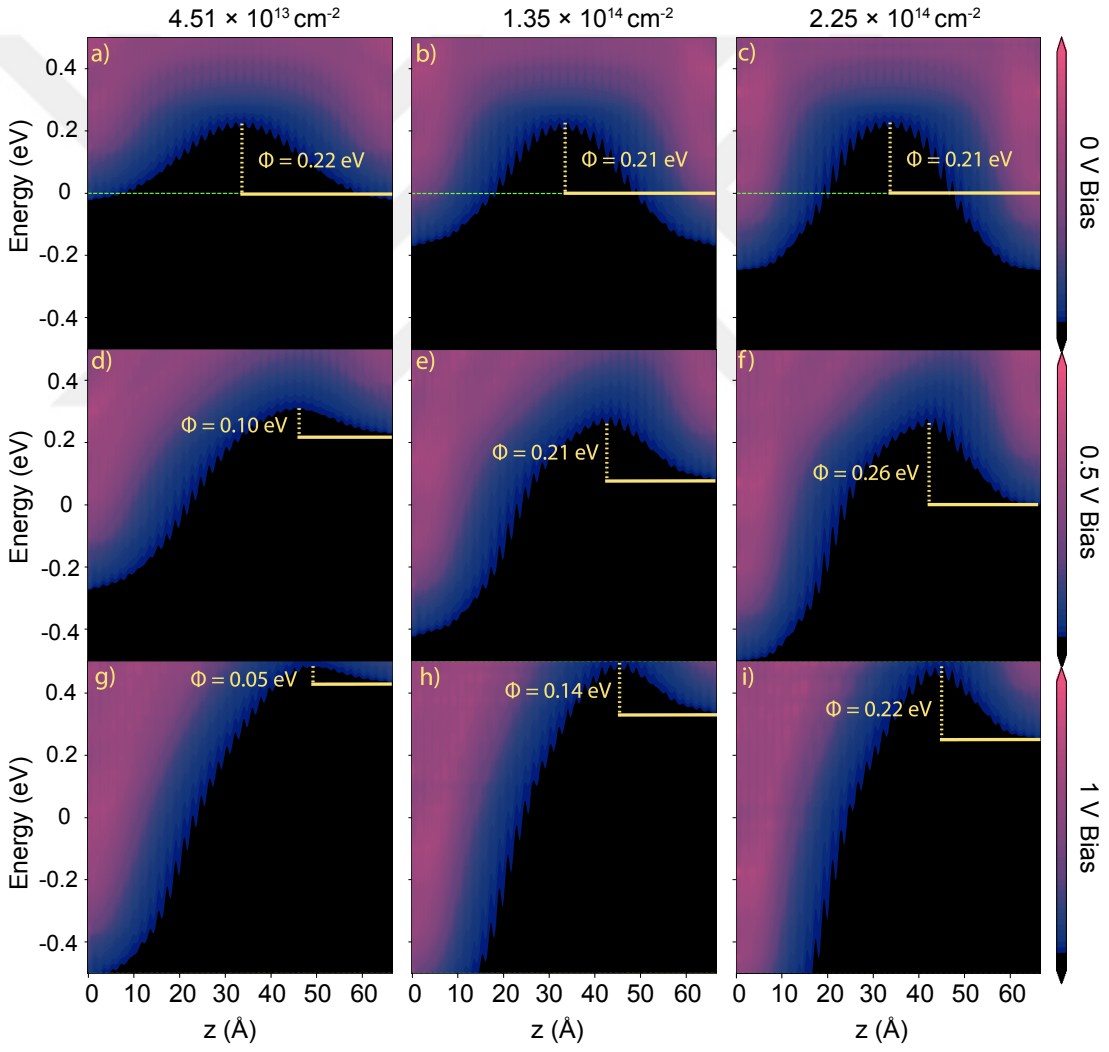


Figure 3.22: Schottky barrier heights of devices with 6.5 nm channel length under (a-c) 0 V bias, (d-f) 0.5 V bias, (g-i) 1 V bias

However, this trend is not observed at medium and high doping levels. This

can be attributed to a narrowing of the depletion region with higher doping, leading to a more stable barrier height [92]. Additionally, we found that for each bias value, the SB width decreases with increasing doping concentration. Since tunneling probability increases with reduced spatial distance, the higher doping level of the electrodes leads to enhanced tunneling current. Given the high current observed at elevated bias levels and the concurrent increase in SBH, which inhibits thermionic emission, it can be inferred that tunneling becomes the dominant transport mechanism as the bias voltage increases. It should also be noted that SB height and width can be modulated by external factors, such as strain engineering, which results in a significant current enhancement across all bias voltages, as demonstrated in Fig. 3.23.

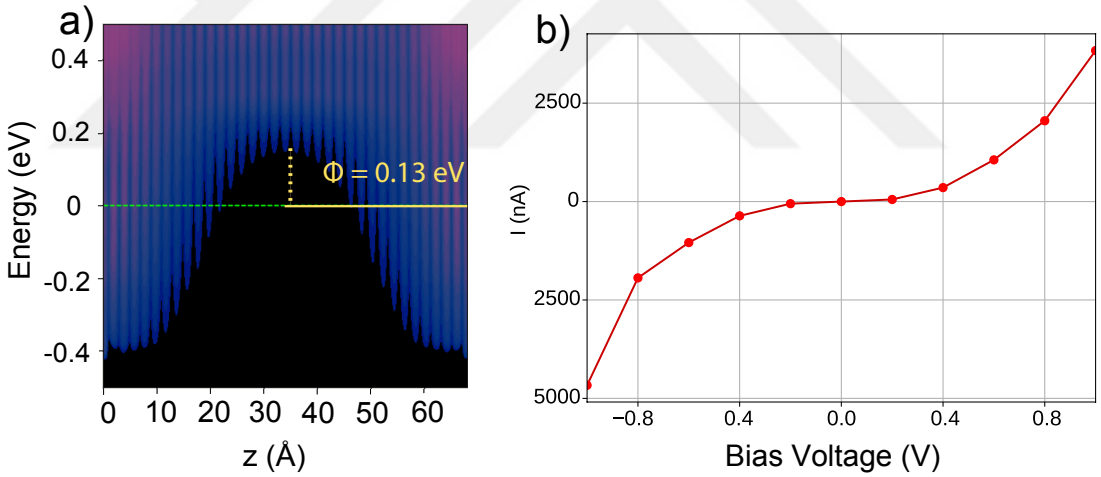


Figure 3.23: (a) Projected local density of states (PLDOS) for the 6.5 nm Ge_2PAs MSM device under 4% tensile strain. (b) Corresponding I–V characteristics.

3.11 Conclusion

In this part of the thesis, we thoroughly investigated the electronic transport properties of the 2D Janus Ge_2PAs monolayer, demonstrating its potential as a channel material in MSM (metal-semiconductor-metal) devices. Our calculations revealed the distinct electronic characteristics of the Janus Ge_2PAs monolayer,

including its anisotropic, quasi-direct band structure and the negligible spin–orbit coupling (SOC) effect. By simulating a range of electrode doping concentrations and channel lengths, we systematically explored their impact on device performance. The results indicate that a minimum channel length of 6.5 nm is necessary for a device to exhibit typical MSM behavior. Furthermore, the doping concentration of the electrodes significantly influences the current values. Higher doping levels lead to enhanced currents due to an increased density of states (DOS) and more efficient tunneling current facilitated by a reduced SB width. We further examined the SB height (SBH) under different bias conditions and doping concentrations. While the SBH remains constant at equilibrium with increased doping, it increases under finite bias, influencing charge carrier transport. The dominance of tunneling current at higher biases underscores the critical role of electrode doping in optimizing device performance. This comprehensive analysis provides valuable insights into the design and optimization of 2D Janus Ge_2PAs-based MSM devices. Our findings contribute to the broader understanding of electronic transport in 2D materials and pave the way for future experimental and theoretical investigations in the field of nanoelectronics.

Chapter 4

2D Backward Diodes and p–i–n FETs

4.1 Motivation

Over the past few decades, the extraordinary physical and chemical characteristics exhibited by 2D materials have attracted widespread scientific attention. This drives a surge of theoretical and experimental investigations aimed at unveiling their fundamental properties and exploring their potential for next-generation technological applications [93, 94, 95]. The broad applicability of 2D materials based on their versatile electronic and structural properties positions them as promising competitors to challenge the long-standing dominance of silicon in the semiconductor industry. This challenge is particularly evident with the growing demand for high-performance nanoscale devices and next-generation electronic technologies [96, 97, 98]. Within this context, monolayer group-III monochalcogenides (MX, M = Ga, In; X = S, Se, Te) have emerged as a compelling family of 2D semiconductors [99, 100]. Their electronic structure together with their intrinsically high carrier mobilities, underpins their promising role in future applications including electronics, optoelectronics, nonlinear optical devices, and photodetectors [101, 102, 103, 104]. In support of their technological potential, monolayers of

GaS, GaSe, and InSe have been successfully synthesized by mechanical exfoliation of bulk crystals as well as chemical vapor deposition methods [105, 106, 107].

Within this material family, 2D GaSe distinguishes itself through a combination of mechanical robustness and tunable electronic structure. Its high 2D Young's modulus ($\sim$819 $\pm$ 127 N m^{-1}) [108] is accompanied by a strain-tunable bandgap, while the valence band displays a characteristic 'Mexican-hat' dispersion that has been suggested to be advantageous for FET operation [109]. Beyond these intrinsic attributes, 2D GaSe offers band-edge alignment suitable for solar water splitting and displays promising thermoelectric behavior with figures of merit reported to be up to $\sim$ 2.43 [110]. Experimentally, mono- and few-layer GaSe field-effect devices have achieved mobilities in the range of 0.6-20 cm^2 V^{-1} s^{-1} together with on/off current ratios of 10^4–10^5 [111, 112]. GaSe-based photodetectors exhibit high responsivity and external quantum efficiencies approaching $\sim$ 1367 % which outperforms several benchmark 2D semiconductors such as MoS_2 [113]. Contact engineering via GaSe/graphene heterostructures further enables control over the Schottky barrier [114]. Despite these advances, the scalability and versatility of GaSe monolayers across distinct device geometries remain open questions that necessitate systematic investigation.

To address this gap, we carry out a comprehensive study of the electronic transport properties of 2D GaSe nano-devices by combining density functional theory (DFT) with nonequilibrium Green's function (NEGF) simulations. The main objective is to clarify how GaSe behaves when incorporated into different device architectures and to benchmark its potential against the requirements of next-generation logic technologies. We begin with p–n junction diodes, where we reveal an unconventional backward rectification behavior arising from tunneling-assisted transport. The analysis is then extended to p–i–n field-effect transistors (FETs) in which we explore how electrostatic gating modulates the backward diode response. Finally, we examine double-gate MOSFETs with channel lengths of about 5 nm, evaluating their transfer characteristics, on/off ratios, gate capacitances, intrinsic delay times, and power–delay products in comparison with ITRS-2028 high-performance targets. By addressing these complementary device designs, our work highlights the GaSe monolayer as a versatile 2D semiconductor. It combines

backward-diode operation with high-performance transistor capabilities which offers a pathway toward future nanoscale electronic applications.

4.2 Methodology

Geometry optimization and electronic structure calculations were performed using the DFT approach as implemented in the Vienna Ab initio Simulation Package (VASP) [59, 60]. The exchange-correlation functional was approximated using the generalized gradient approximation (GGA) with the Perdew-Burke-Ernzerhof (PBE) formalism [61]. Ion-electron interactions were modeled using the projected augmented wave (PAW) method with a plane-wave cutoff energy of 500 eV [49]. The Brillouin zone was sampled with a $12 \times 12 \times 1$ k-point mesh, employing the Monkhorst-Pack scheme [62]. To avoid spurious interactions, a vacuum space of approximately 20 Å was included. The lattice parameters and atomic positions were iteratively optimized until the forces on the atoms were less than 0.01 eV/Å. The energy difference between successive steps was reduced until it has a value less than 10^{-5} eV.

The Device models were constructed using the optimized structure. Simulations of the transmission coefficients $[T(E)]$ and the I–V curve were performed using the QuantumATK package [64], which accomadates a reliable means of assessing transport properties by integrating DFT calculations with the NEGF technique [51]. The Monkhorst-Pack k-grid sampling was set to $1 \times 2 \times 201$. Atomic cores were represented using PseuDodojo pseudopotentials [65], and a medium numerical basis was used for wave function expansion. The density mesh cutoff energy was set to 105 Ry to balance computational efficiency and accuracy. The electrode temperature was maintained at 300 K. Bulk properties were assigned to the left and right electrodes, with initial bulk calculations for each electrode conducted using Dirichlet boundary conditions (BCs) at both boundaries. Periodic BCs were then applied perpendicular to the electron transport directions. The self-consistent solution for the transmission coefficient $[T(E, V_b)]$ under different biases (V_b) was obtained using the retarded Green's function [66]:

$$T(E, V_b) = Tr[G(E, V_b)\Gamma^L G^\dagger(E, V_b)\Gamma^R] \tag{4.1}$$

where $\Gamma^{L(R)}$ is the broadening function of the left(right) electrode given by $\Gamma^{L(R)} = 1/i(\sum^{L(R)} - (\sum^{L(R)})^\dagger)$ with self-energy of the left(right) electrode $\sum^{L(R)}$. Applying a V_b across the device results in a shift of the chemical potentials of the left (μ_L) and right (μ_R) electrodes to $\mu_L = E_F + eV_b/2$ and $\mu_R = E_F - eV_b/2$, respectively. The flow of current along the transport direction is consequently obtained due to the difference in chemical potential between the left and right electrodes. The current induced by a V_b, namely the I-V characteristics, is calculated using the Landauer-Büttiker formula within the framework of quantum transport formalism that integrates $T(E, V_b)$ within the bias window, which is $[-eV_b/2, +eV_b/2]$:

$$I(V_b) = \frac{2e}{h}\int_{\mu_L}^{\mu_R} T(E, V_b)[f_L(E, V_b) - f_R(E, V_b)]dE \tag{4.2}$$

where $f_L(E, V_b)$ and $f_R(E, V_b)$ are the Fermi distribution of the left and right electrodes, respectively.

4.3 Structural and Electrical Properties

Before examining the transport properties of the 2D GaSe nano-devices, we first describe the structural and electronic characteristics of GaSe monolayer. The optimized structure adopts a hexagonal arrangement with a four-atom Se–Ga–Ga–Se basis, belonging to the D_{3h} space group. The calculated lattice constant of 3.82 Å is consistent with previous theoretical reports [100, 115], which confirms the precision of our approach. The optimized atomic configuration of GaSe monolayer, together with its electronic band structure, is provided in Figure 4.1a and Figure 4.1b, respectively . The pristine GaSe monolayer exhibits an indirect band gap of 1.85 eV, in line with previous reports. To further validate the electrostatic doping approach adopted in this work, the band structures of both *p*- and *n*-type

doped GaSe monolayers are also presented in Figure 4.1c and 4.1d, respectively. As expected, electrostatic doping leads to a rigid shift of the Fermi level while leaving the intrinsic band dispersion essentially unaltered, thereby ensuring that the underlying material characteristics remain preserved under applied doping.

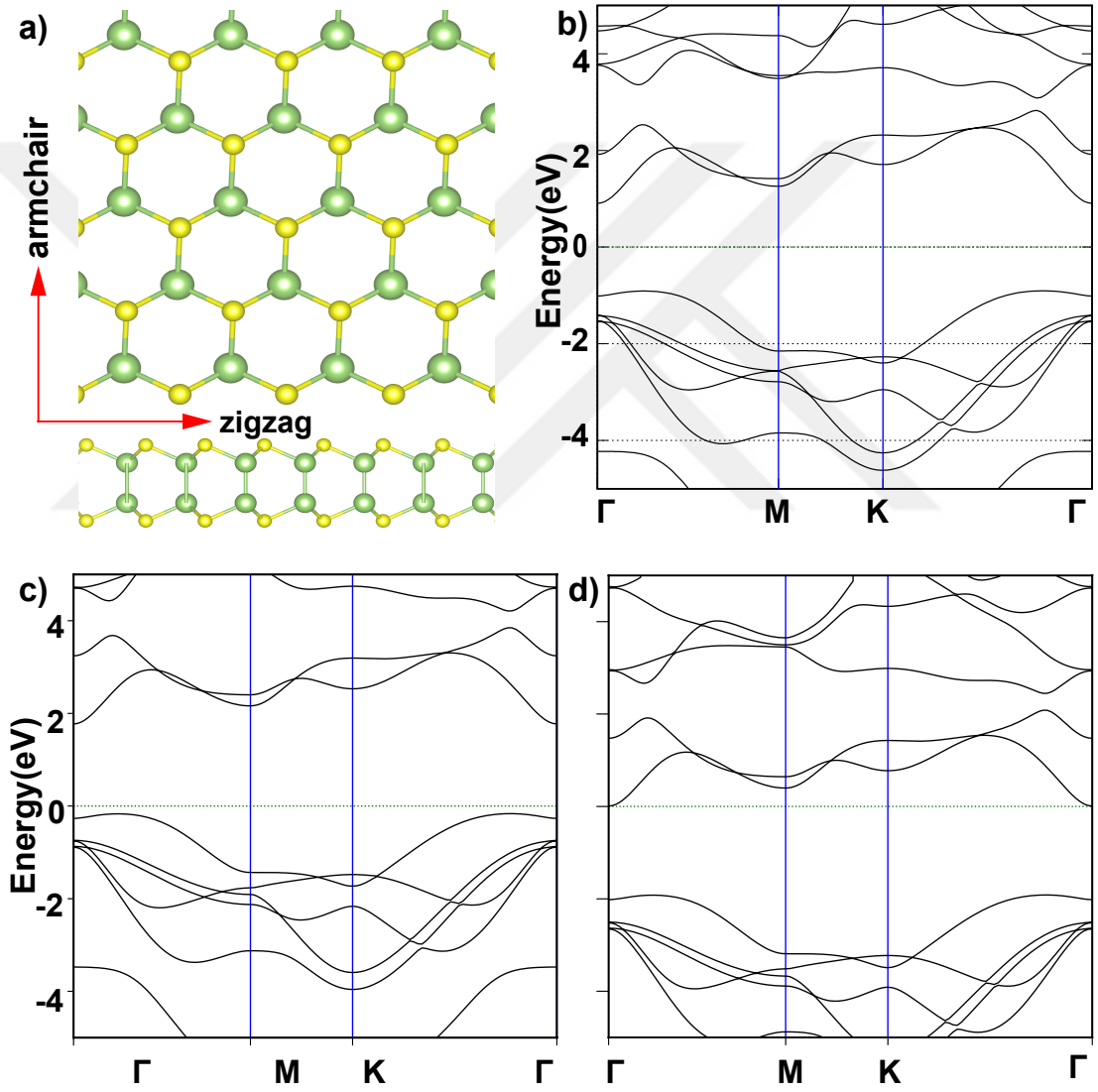


Figure 4.1: (a) Optimized atomic configuration of the GaSe monolayer. (b) Electronic band structure of pristine GaSe. (c) Band structure of p-type and (d) n-type doped GaSe.

4.4 Backward Diode Behavior of p–n Junctions

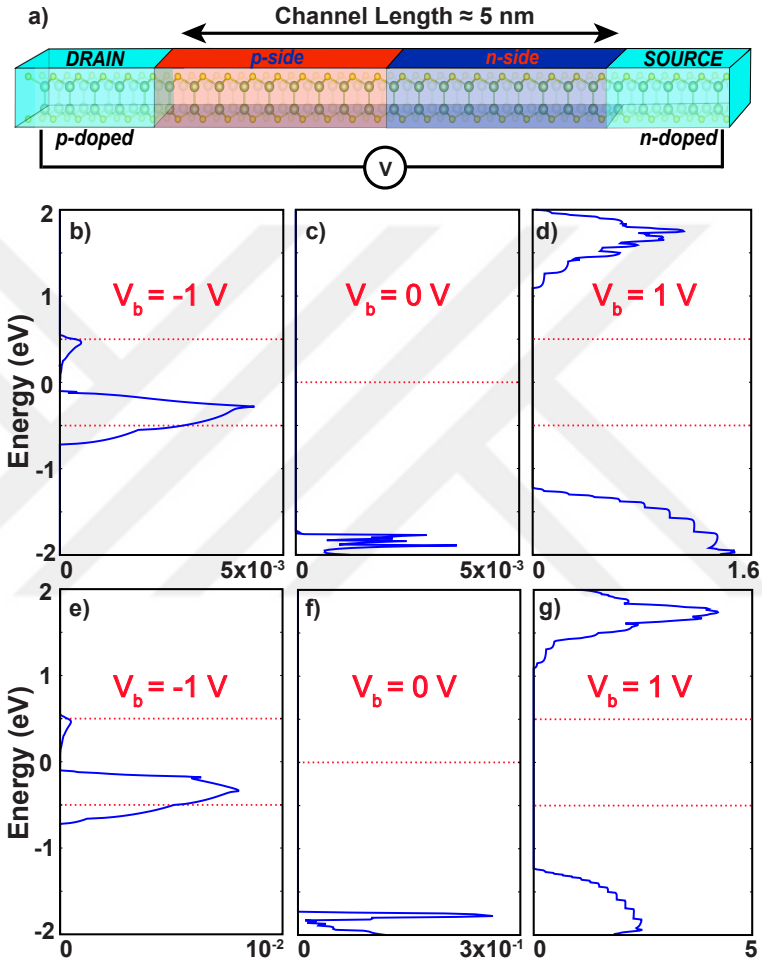


Figure 4.2: (a) Schematic and transmission spectra of (b)-(d) armchair-type (e)-(g) zigzag-type 2D GaSe p-n junction diode nano-devices

In this part of the thesis we investigate the transport properties of GaSe-based nano-devices. Figure 4.2a illustrates a schematic of the p–n junction diode constructed from monolayer GaSe using electrostatic doping. In this approach, the *p*- and *n*-type regions are realized by introducing atomic compensation charges, which effectively modify the local electron density of selected atoms relative to the pristine neutral case [55, 51]. Specifically, *p*-doping corresponds to decreasing, while *n*-doping corresponds to increasing, the number of electrons in the system.

This method has been extensively employed in modeling 2D nano-devices, as it enables precise control over carrier concentrations while preserving the intrinsic band structure of the host material [81]. Besides, this assumption is supported by experimental observations from two-terminal graphene devices, confirming the stability of the band structure under electrostatic doping [82]. In our design, each diode consists of two semi-infinite electrodes, the drain (D) and source (S), connected through a central scattering region that forms the p–n junction. The length of this central region is approximately 5 nm, while the doping concentration is set to $\sim 8.5\times10^{13}$ cm^{-2} for p-side and $\sim 3.2\times10^{13}$ cm^{-2} for n-side. The source of this asymmetric doping is to achieve the highest doping for each side before the onset of metallicity. This setting for the doping concentration is also applied for p-i-n FET and MOSFET architectures in the subsequent sections. The corresponding transmission spectra of the devices, displayed in Figures 4.2b–d for the armchair direction and Figures 4.2e–g for the zigzag direction, reveal the energy-resolved transmission pathways across the junction. In each set, the left, middle, and right panels correspond to applied biases of –1 V, 0 V, and 1 V, respectively. Notably, the spectra demonstrate that carrier transport channels emerge only within the reverse-bias window while they remain absent in the forward-bias case, which clearly illustrates the backward diode nature of the GaSe p–n junction in the –1 V to +1 V interval.

To see the effect of these features, we calculated the current–voltage response and it is presented in Figure 4.3. The main plot shows the conventional rectifying behavior expected for a p–n junction under large forward bias, where the current rises steadily once the barrier is overcome. By contrast, the inset highlights the interval between –1 V and +1 V, where the backward diode characteristics are most evident. Within this low-bias regime, the current in the reverse direction is markedly larger than that in the forward direction, which reflects the enhanced tunneling pathways and favorable band alignment of GaSe monolayer. This duality sets the junction apart from conventional rectifiers by combining the typical forward conduction of p–n devices with a pronounced reverse-bias response, as reported for heavily doped single-layer MoS_2 p–n junctions [116].

To gain deeper insight into this mechanism, we calculated the projected local

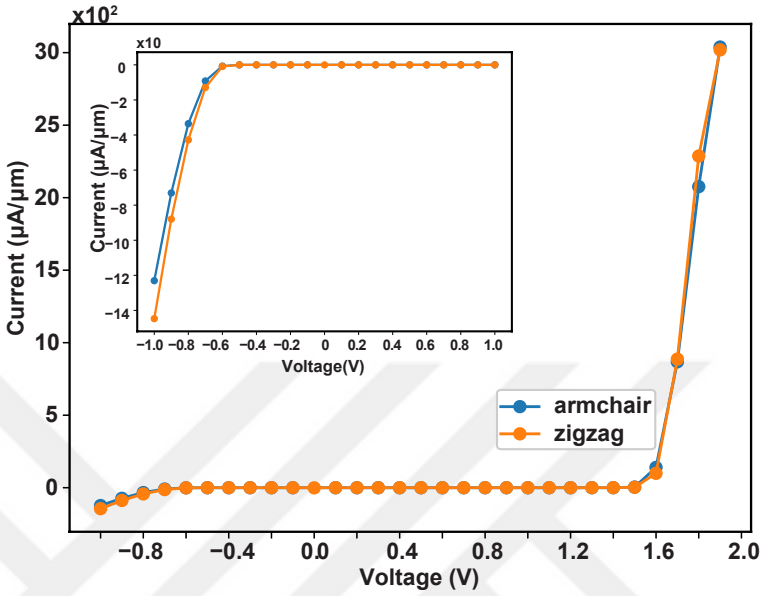


Figure 4.3: Calculated current–voltage characteristics at 300 K of 2D GaSe p–n junction diode nano-devices along the armchair and zigzag directions. The main panel shows the rectifying behavior under forward bias, while the inset highlights the current response in the negative bias region.

density of states (PLDOS) of the armchair and zigzag 2D GaSe p–n junctions under applied biases of –1, 0, and 1 V, as shown in Figures 4.4a–c and 4.4d–f, respectively. Under reverse bias, the bands of the *p*- and *n*-doped electrodes shift upward and downward, such that more electronic states enter the bias window compared with the equilibrium case. At –1 V (Figures 4.4a and 4.4d), band overlap occurs between the conduction states of the drain and the valence states of the source which allows efficient electron tunneling and giving rise to the backward current. In this configuration, carriers can tunnel from the valence band of the *n*-side into the conduction band of the *p*-side, which accounts for the pronounced reverse-bias transport. In contrast, when a forward bias of 1 V is applied (Figures 4.4c and 4.4f), the drain and source bands shift in opposite directions, which further opens the energy gap across the junction and suppresses any band overlap, thereby eliminating tunneling channels. At higher forward bias voltages, once the overlap becomes negligible, the tunneling contribution vanishes and the transport is dominated by thermally assisted carrier emission.

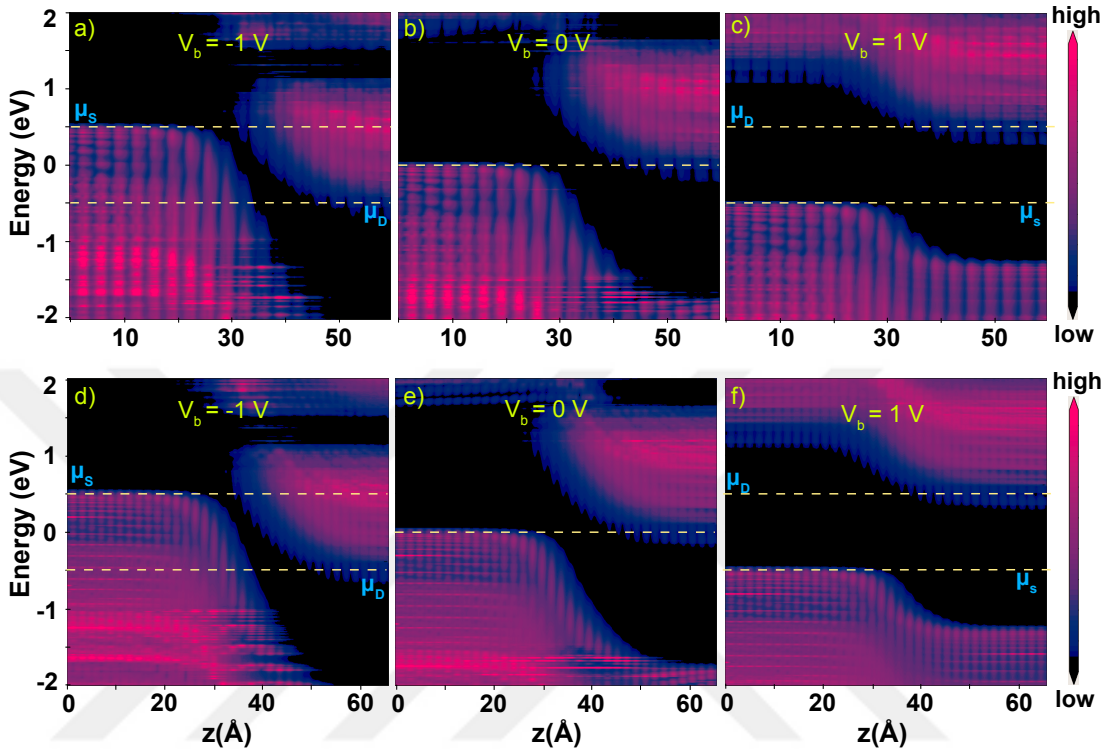


Figure 4.4: Calculated PLDOS of 2D GaSe p–n junction diode nano-devices under applied biases of –1 V, 0 V, and 1 V for (a–c) the armchair and (d–f) the zigzag transport directions. The horizontal dashed lines indicate the electrochemical potentials of the source (μ_S) and drain (μ_D)

4.5 Field-effect Behavior of p-i-n FET Devices

Having established the backward diode response of GaSe p–n junctions, we now turn to the field-effect characteristics of p–i–n FET configurations. Figure 4.5a shows the schematic design of a double-gate device, where the intrinsic channel of length ∼5 nm is electrostatically modulated by top and bottom gates separated from the channel by dielectric layers. In this architecture, the source and drain electrodes are doped with opposite polarity, forming a p–i–n junction whose transport properties can be tuned by the applied gate bias. Such designs are particularly promising for enhancing carrier control in short-channel 2D devices while minimizing leakage currents.

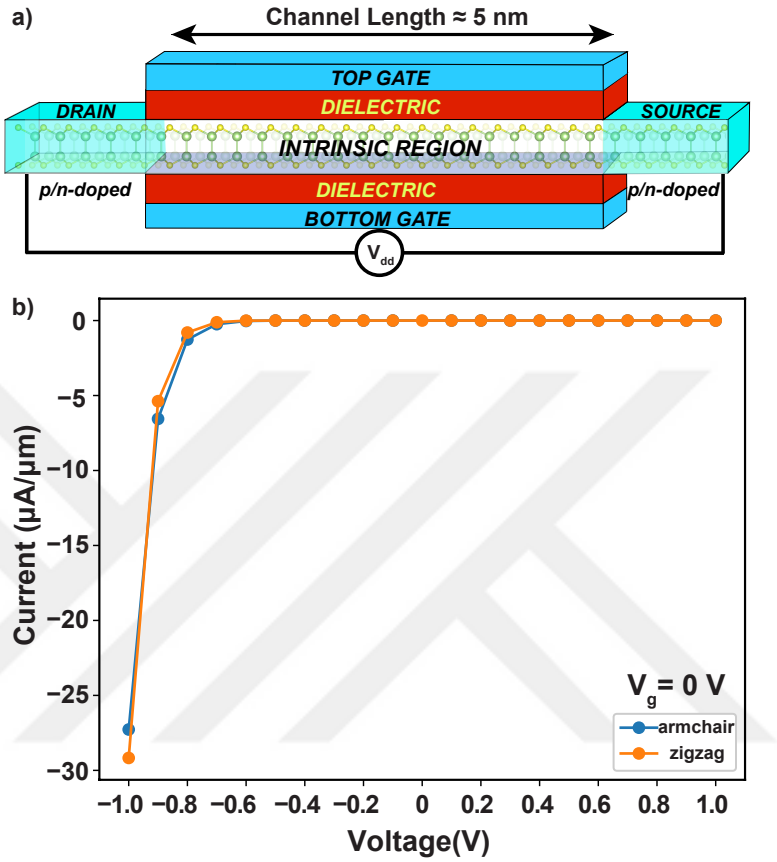


Figure 4.5: (a) Schematic representation of double-gate 2D GaSe nano-devices, which can operate either as p–i–n FETs when the drain is p- and the source is n-doped, or as MOSFETs when both contacts are of the same doping type. (b) Calculated current–voltage characteristics at 300 K of the p–i–n FET configuration along the armchair and zigzag directions at zero gate bias.

The calculated current–voltage characteristics at 300 K for the p–i–n FETs are presented in Figure 4.5b. At zero gate bias, both armchair and zigzag transport directions display rectifying features which is consistent with the backward diode-like behavior discussed in Section 3.2. Upon applying a gate, the backward-bias response is initially suppressed at $V_g = 1$ V and $V_g = 2$ V. For stronger gating, $V_g = 3$ V and $V_g = 4$ V (see Figures 4.6c and 4.6d, respectively), current increases markedly with gate voltage, indicating that electrostatic modulation has driven additional transmission channels into the bias window. Overall, GaSe p–i–n FETs merge backward diode-like rectification with selective gate tunability since modest

positive gates can suppress conduction, whereas stronger gates restore and enhance current.

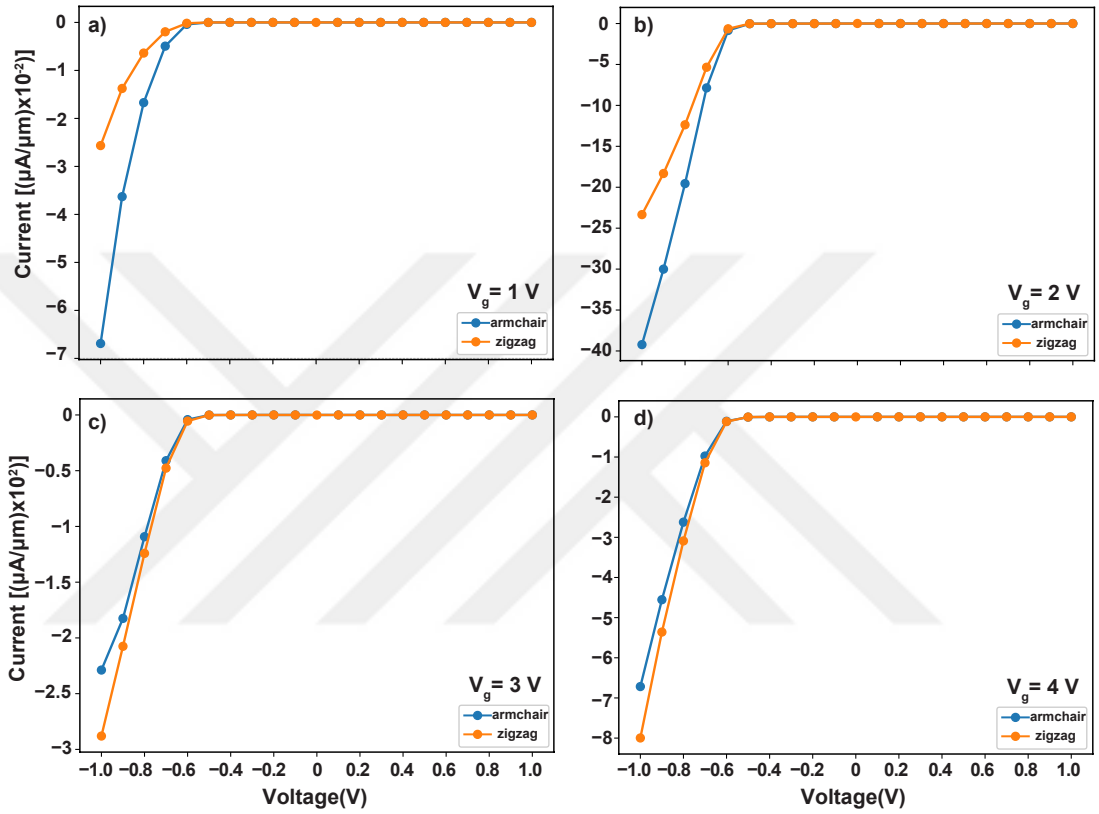


Figure 4.6: Calculated current–voltage characteristics at 300 K of 2D GaSe p–i–n FET nano-devices along the armchair and zigzag directions under different gate voltages: (a) $V_g = 1$ V, (b) $V_g = 2$ V, (c) $V_g = 3$ V, and (d) $V_g = 4$ V.

4.6 Field-effect Behavior of MOSFET Devices

We next examine the field-effect response of double-gate GaSe MOSFETs. As depicted in Figure 4.5a, the same platform used for the diode studies—top and bottom gates separated from an intrinsic channel of length $L_g \approx 5$ nm by dielectric layers—realizes MOSFET operation when the source and drain share the same doping type (p or n). In this configuration, there is no built-in p–n junction. Instead, transport is governed by gate-induced band bending and barrier modulation within the intrinsic region. Throughout this section we set the gate

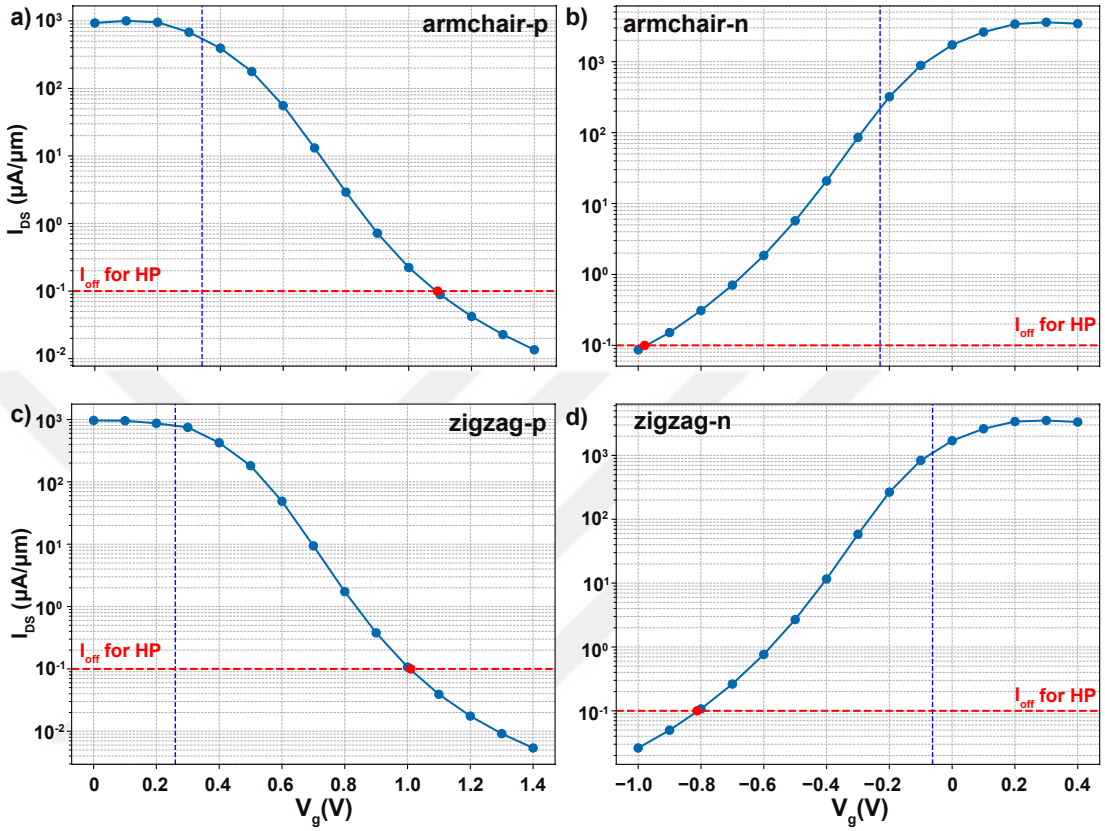


Figure 4.7: Transfer characteristics ($I_{\rm ds}$–V_g) at 300 K of 2D GaSe MOSFET nanodevices along the armchair and zigzag directions: (a) armchair-p, (b) armchair-n, (c) zigzag-p, and (d) zigzag-n. The red dashed line indicates the high-performance (HP) $I_{\rm off}$ limit.

dielectric to SiO_2 with relative permittivity $\kappa = 3.9\epsilon_0$ and choose the supply voltage $V_{\rm dd} = 0.64$ V, consistent with the ITRS-2028 high-performance (HP) requirements for $L_g \sim 5$ nm logic devices. The transfer characteristics $I_{\rm DS}$–V_g at 300 K for armchair-p, armchair-n, zigzag-p, and zigzag-n MOSFETs are presented in Figure 4.7a–d. In all cases, the off-state current $I_{\rm off}$ satisfies the HP requirement of 0.1 μA/μm (red dashed guideline in Figure 4.7). Device specifications are benchmarked against the ITRS-2028 HP targets and the values are summarized in Table 1. We define the on-state gate voltage as: .

$$V_{\rm on} = V_{\rm off} + V_{\rm dd}, \tag{4.3}$$

and use $I_{\rm on} \equiv I_{\rm DS}(V_{\rm on})$ as a primary figure of merit, since larger $I_{\rm on}$ directly

Table 4.1: Ballistic Transport Properties of 2D DG GaSe MOSFETs without the UL along the armchair and zigzag directions with the ITRS 2028 for HP standards.

	$I_{\mathbf{off}}$ (μA/μm)	$I_{\mathbf{on}}$ (μA/μm)	$I_{\mathbf{on}}/I_{\mathbf{off}}$	C_g (fF/μm)	τ (ps)	**PDP** (fJ/μm)
ac-n	0.1	251	2.5×10^3	0.40	1.02	0.06
ac-p	0.1	562	5.6×10^3	0.55	0.63	0.10
zz-n	0.1	1160	11.6×10^3	0.44	0.24	0.06
zz-p	0.1	797	8×10^3	0.57	0.46	0.10
ITRS-2028	0.1	900	9×10^3	0.60	0.423	0.24

enables faster switching. The extracted on/off ratios span 2.5×10^3 (armchair-n), 5.6×10^3 (armchair-p), 8.0×10^3 (zigzag-p), and 1.16×10^4 (zigzag-n), indicating robust gate control across both crystallographic orientations. To quantify the switching speed, we evaluate the intrinsic delay time τ following:

$$\tau = \frac{C_g V_{\mathrm{dd}}}{I_{\mathrm{on}}}, \tag{4.4}$$

where C_g is the total gate capacitance. C_{fr} denotes the fringing capacitance and in ultra-scaled devices, C_{fr} provides a significant contribution and is commonly approximated as twice the channel capacitance We decompose:

$$C_g = C_{\mathrm{ch}} + C_{\mathrm{fr}}, \qquad C_{\mathrm{fr}} \approx 2\, C_{\mathrm{ch}}, \qquad C_{\mathrm{ch}} = \frac{\partial Q_{\mathrm{ch}}}{\partial V_g}, \tag{4.5}$$

with Q_{ch} the total channel charge. For the double-gate GaSe MOSFETs considered here, C_g falls in the range 0.40–0.57 fF/μm, in line with the ITRS-2028 HP target (0.60 fF/μm). According to $\tau \propto C_g/I_{\mathrm{on}}$, faster switching is achieved by maximizing I_{on} and minimizing C_g. The resulting delay times given in Table 1 show that the zigzag-n device attains $\tau = 0.24$ ps—comfortably within the HP target (0.423 ps)—while the zigzag-p device is close (0.46 ps). The armchair-p and armchair-n devices exhibit larger delays (0.63 ps and 1.02 ps, respectively). These

trends underscore the advantage of the zigzag channel for high-speed operation. Energy efficiency is captured by the power–delay product:

$$\mathrm{PDP} = \frac{\left(Q_{\mathrm{on}} - Q_{\mathrm{off}}\right) V_{\mathrm{dd}}}{W}, \tag{4.6}$$

with W the channel width and $Q_{\mathrm{on/off}}$ the channel charges at $V_{\mathrm{on/off}}$. All GaSe MOSFET configurations yield PDP values in the range 0.06–0.10 fJ/μm—well below the ITRS-2028 HP guideline (0.24 fJ/μm). Taken together with the on/off ratios above, these results indicate that double-gate GaSe MOSFETs can simultaneously achieve low standby power (I_{off} at the HP limit), competitive drive currents (particularly in the zigzag orientation), and sub-target energy per switch, making them promising candidates for ultra-scaled, high-performance logic at $L_g \approx 5$ nm.

4.7 Conclusion

In conclusion, for the present part of the thesis we have performed a comprehensive first-principles investigation of the transport characteristics of 2D GaSe nanodevices across three complementary device architectures: p–n junction diodes, p–i–n FETs, and double-gate MOSFETs. Our results demonstrate that GaSe p–n junctions exhibit a pronounced backward diode behavior. The reverse current within the low-bias window (-1 to $+1$ V) surpasses the forward current due to efficient tunneling as supported by the PLDOS analysis. By extending the device design to p–i–n FETs, we show that gate modulation enables selective control of this backward conduction where moderate gate voltages ($V_g = 1$–2 V) suppress tunneling-driven reverse current, while stronger gating ($V_g = 3$–4 V) restores and enhances carrier transport. Finally, our assessment of double-gate GaSe MOSFETs with channel lengths of ~ 5 nm highlights their strong competitiveness against ITRS-2028 high-performance targets. In particular the zigzag-n configuration achieves an on/off ratio of 1.2×10^4, an intrinsic delay time of 0.24 ps, and a power–delay product as low as 0.06 fJ/μm. All of these values surpass or closely

match the HP benchmarks. These findings establish GaSe monolayer as a versatile 2D semiconductor capable of integrating backward diode functionality with gate-tunable p–i–n operation and high-performance MOSFET behavior. Our work emphasizes the technological promise of 2D GaSe as a platform for future ultra-scaled nanoelectronic devices that bridges unconventional rectifying mechanisms with practical transistor performance metrics required for next-generation logic applications.

Chapter 5

High-Performance and Energy-Efficient Sub-5 nm 2D Double-Gate MOSFETs

5.1 Motivation

The continuous demand for high-performance (HP), energy-efficient transistors is driving research beyond conventional silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs), which face critical scaling limits. To address this challenge, new channel materials and device architectures are being explored. The emergence of 2D materials has introduced new possibilities to overcome the scaling limitations of bulk MOSFETs [31, 117, 94, 118, 119]. Atomically thin channels provide superior electrostatic control, effectively mitigating short-channel effects that plague conventional silicon-based devices [120, 121]. Moreover, their high carrier mobility, tunable bandgaps, and excellent scalability make 2D materials highly attractive for further transistor miniaturization while maintaining both high performance and low power consumption [122, 38]. Among them, graphene has attracted particular attention due to its exceptional carrier mobility [122]; however, the absence of an intrinsic bandgap severely restricts its application in digital

electronics [123, 27]. In contrast, semiconducting transition metal dichalcogenides (TMDs) such as MoS_2 possess intrinsic bandgaps, making them more suitable for field-effect transistors where high on/off current ratios are essential [38, 121, 124, 125]. Recent studies have further demonstrated the feasibility of 2D transistors with L_g below 5 nm, highlighting their potential to complement or replace silicon in future device architectures [126]. Computational investigations have played a critical role in this progress, providing detailed insight into the electronic and transport properties of 2D MOSFETs and consistently underscoring their suitability for HP nanoscale applications [127, 128, 129, 130, 131, 132, 78, 133, 134, 135, 136]. As research advances, the integration of 2D materials into MOSFET technology offers a promising pathway to sustain Moore's law and enable further reductions in device size without compromising performance.

In recent years, 2D group IV–V semiconductors have emerged as promising candidates for next-generation electronic devices owing to their unique electronic properties [30]. While single-element 2D materials and other families such as TMDs, black phosphorus, and related semiconductors have been extensively investigated, binary compounds formed by group IV elements (Si, Ge) with group V elements (P, As) remain relatively underexplored. The successful synthesis of layered compounds such as SiP, SiAs, GeP, and GeAs has recently stimulated both experimental and theoretical efforts to uncover their electronic potential [137, 138]. Bulk GeAs and SiAs are known to crystallize in monoclinic layered structures (C2/m), which can, in principle, be exfoliated into stable monolayers [139, 140, 141]. Computational studies further support this possibility, showing that monolayers such as A_2B_2-type SiP in the $P\bar{6}m2$ structure can be readily obtained from their bulk counterparts, suggesting their applicability in nanoscale devices [142]. Subsequent investigations have predicted that stable group IV–V monolayers (e.g., SiP, SiAs, GeP, GeAs) can exist in two competing crystal structures with nearly degenerate formation energies, highlighting the feasibility of multiple configurations [143]. Electron counting rules also indicate that these compounds could adopt geometries analogous to group III–VI semiconductors, further supporting their structural stability [144]. Recent computational studies on their electronic and vibrational properties revealed that, with the exception of

certain carbon-based systems (e.g., CP and CAs), most group IV–V monolayers favor the P$\bar{6}$m2 structure as the energetically most stable phase [145].

Despite its promising electronic properties, previous studies on SiAs have primarily focused on the monolayer derived from its bulk form, while the P$\bar{6}$m2 monolayer structure remains relatively unexplored. To address this gap, we investigate the potential of 2D SiAs as a channel material for sub-5 nm double-gate (DG) MOSFETs by combining first-principles calculations with the Non-equilibrium Green's function (NEGF) formalism. By demonstrating the intrinsic device-level performance of monolayer SiAs within the ballistic regime, this work provides a proof-of-concept that structurally robust Group IV–V compounds can complement conventional 2D semiconductors and enable continued transistor scaling beyond current material limits. After analyzing the electronic structure of SiAs, we design DG MOSFET models to evaluate their ballistic transport characteristics. To optimize device performance, we examine the effects of source and drain doping concentrations as well as the incorporation of underlap (UL) regions between the gate and source/drain contacts. Key performance metrics, including the on/off current ratio (I_{on}/I_{off}), SS, gate capacitance (C_g), power–delay product (PDP), and intrinsic delay time (τ), are systematically evaluated. In addition, the projected local density of states (PLDOS) and transmission spectra [$T(E)$] are analyzed to elucidate the role of gate control and to highlight the performance improvements achieved through UL architectures.

5.2 Methodology

First-principles calculations were performed within the framework of density functional theory (DFT) using the Vienna Ab initio Simulation Package (VASP) [59, 60]. The exchange–correlation energy was described using the generalized gradient approximation (GGA) with the Perdew–Burke–Ernzerhof (PBE) functional [61], and the projector augmented-wave (PAW) method [49] was employed to treat electron–ion interactions. A plane-wave cutoff energy of 530 eV was chosen to ensure reliable convergence of the total energy. A vacuum spacing of 25 Å was

applied along the out-of-plane direction to avoid interactions between periodic images. The Brillouin zone was sampled with a $16 \times 16 \times 1$ Monkhorst–Pack k-point mesh [62]. Structural relaxations were performed until the forces on individual atoms were less than 0.01 eV/Å, and the total energy convergence threshold was set to 10^{-5} eV.

The charge transport properties of 2D DG SiAs MOSFETs were evaluated under the ballistic limit using the DFT + NEGF formalism. This coherent-transport assumption excludes inelastic scattering processes, such as electron–phonon interactions, which correspond to the intrinsic upper bound of device performance. The approximation is justified for sub-10 nm channel lengths, where the carrier mean free path exceeds the device dimension and ballistic conduction dominates [29, 146]. The Landauer–Büttiker approach, as implemented in NEGF, provides the appropriate theoretical framework for describing ballistic quantum transport, whereas the Boltzmann transport equation governs the phonon-limited diffusive regime. The present simulations provide a meaningful benchmark for the maximum achievable performance of SiAs MOSFETs under ideal conditions.

Accordingly, the transport characteristics of 2D DG SiAs MOSFET were investigated by DFT + NEGF formalism [51] as implemented in QuantumATK [64]. A double-ζ polarized (DZP) basis set was adopted together with Fritz Haber Institute (FHI) pseudopotentials [147]. A density mesh cutoff of 75 Hartree and a Monkhorst–Pack $1\times20\times200$ k-point grid were used to ensure high accuracy in transport calculations. All calculations were carried out at 300 K. In the device configuration, the source and drain electrodes were modeled as heavily n(p)-doped SiAs monolayers. Doping was implemented by distributing additional charge uniformly across the atoms in the respective regions, providing reliable electrical contact between the electrodes and the channel [148]. The electrostatic potential was obtained self-consistently by solving the Poisson equation on a real-space grid, with periodic boundary conditions in the transverse direction, Neumann conditions perpendicular to the SiAs plane, and Dirichlet conditions along the transport direction to maintain charge neutrality in the electrodes.

The drain current (I_{ds}) under an applied bias voltage (V_{dd}) and gate voltage

(V_g) was calculated using the Landauer–Büttiker formalism [149]:

$$I_{ds}(V_{dd}, V_g) = \frac{2e}{h} \int_{-\infty}^{+\infty} T(E, V_{dd}, V_g) \left[f_S(E - \mu_S) - f_D(E - \mu_D) \right] dE. \quad (5.1)$$

where $T(E, V_{dd}, V_g)$ is the transmission coefficient, $f_S(E - \mu_S)$ and $f_D(E - \mu_D)$ are the Fermi–Dirac distribution functions of the source and drain electrodes, and μ_S and μ_D denote their electrochemical potentials, respectively.

5.3 Structural and Electronic Properties

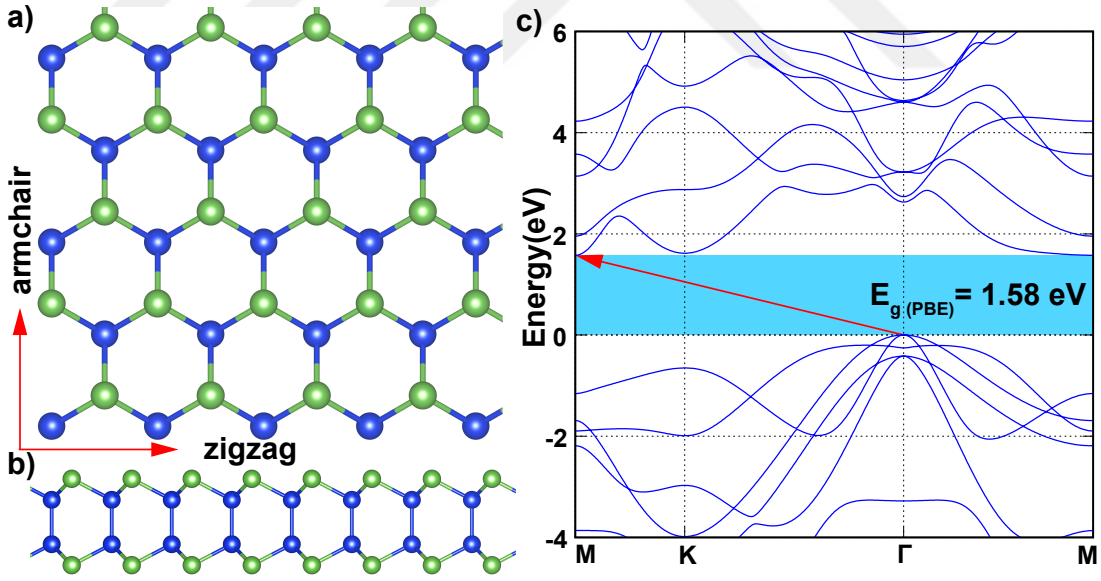


Figure 5.1: a) Top and b) side views of the 2D SiAs. The Si and As atoms are presented in blue and green spheres, respectively. c) Band structure of the SiAs monolayer calculated at the PBE level.

Before analyzing the transport performance of the DG MOSFET model, we first examine the structural and electronic properties of the SiAs monolayer. As shown in Figure 5.1a, the relaxed SiAs monolayer features an As–Si–Si–As stacking sequence, resulting in a hexagonal crystal structure with P$\bar{6}$m2 symmetry. Silicon atoms form covalent bonds with arsenic atoms, yielding a crystal geometry

analogous to group III–VI hexagonal layered chalcogenides, such as InSe [100]. Each Si atom is coordinated to three neighboring As atoms in a hexagonal arrangement, while the top and bottom planes are connected by Si–Si bonds and exhibit mirror symmetry. The optimized lattice constant of the SiAs monolayer is calculated to be 3.66 Å, in agreement with previous theoretical reports [145, 150], confirming the accuracy of the structural model.

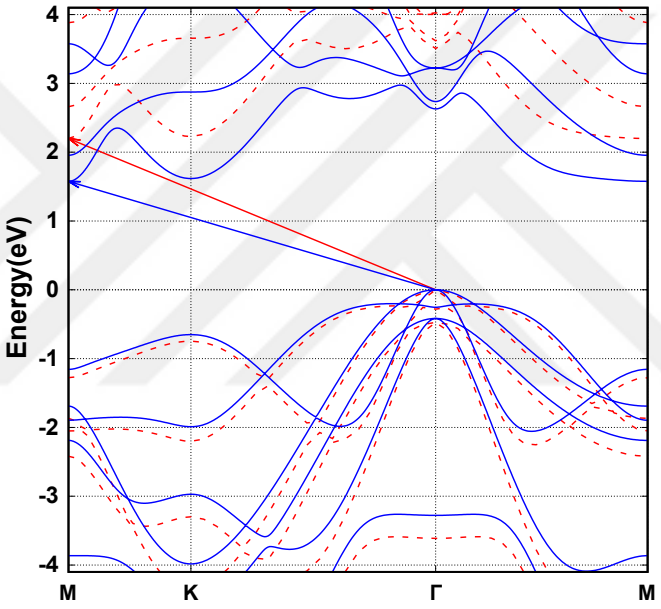


Figure 5.2: Band structure of the SiAs monolayer calculated at the PBE level (solid blue line) and HSE06 level (red dashed line).

The electronic band structure of the SiAs monolayer, calculated using the PBE functional, is shown in Figure 5.1b, while the corresponding result obtained with the HSE06 functional is provided in Figure 5.2. 2D SiAs is identified as an indirect semiconductor with a bandgap of 1.58 eV, where the conduction band minimum (CBM) lies at the M point and the valence band maximum (VBM) at the Γ point, consistent with previous studies [145, 150]. The hybrid HSE06 functional further predicts a larger bandgap of 2.22 eV. The effective masses of electrons and holes were calculated along the armchair and zigzag directions of the SiAs monolayer, yielding m_h^{AC}=0.52 m_0, m_h^{ZZ}=0.09 m_0, m_e^{AC}=2.72 m_0, and m_e^{ZZ}=0.13 m_0. It should

be emphasized that the effective mass alone cannot be directly correlated with device performance, particularly in the ballistic regime of sub-5 nm MOSFETs. In long-channel or diffusive devices, carrier mobility generally scales inversely with effective mass, so lighter carriers typically yield higher mobility and faster switching [117]. However, as the channel length approaches the quantum limit, very light effective masses enhance source-to-drain tunneling, degrade electrostatic control, and increase off-state leakage [151, 76]. Simultaneously, a small effective mass reduces the density of states, implying that materials with light carriers require higher V_g to accumulate sufficient charge and sustain high on-currents [152, 153]. Conversely, materials with moderately heavier masses and lower mobility can suppress tunneling and become advantageous for ultra-scaled (< 5 nm) channels [30]. These competing mechanisms make it difficult to establish a simple monotonic relationship between effective mass and device performance, which is instead governed by the combined influence of quantum tunneling, mode count, and electrostatic control.

5.4 2D Double-Gate MOSFET Device Architecture

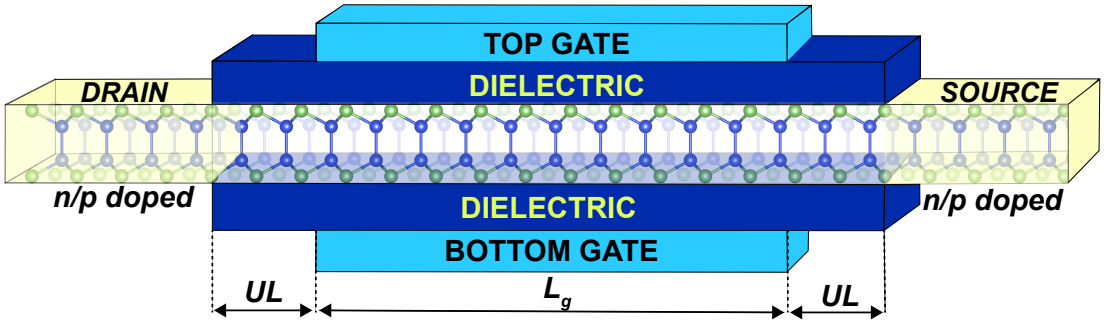


Figure 5.3: Structural diagram of the 2D DG SiAs MOSFETs.

The schematic structure of the DG SiAs monolayer MOSFET is shown in Figure 5.3. Compared with single-gate configurations, DG architectures provide stronger

electrostatic control and improved channel modulation, thereby enhancing overall device performance [154]. The channel region consists of intrinsic SiAs monolayers, while the source and drain electrodes are modeled as heavily n-type or p-type doped SiAs, depending on the configuration. The transport direction is considered along both the armchair and zigzag orientations. Doping of the source and drain regions is implemented through electrostatic doping technique, where localized charges are introduced on individual atoms. This approach allows for continuous tuning of the doping concentration up to 10^{14} cm^{-2}, as demonstrated for ultra-thin TMDs [81]. Importantly, electrostatic doping preserves the overall band structure of the 2D material, apart from shifting the Fermi level, in agreement with experimental observations on two-terminal graphene devices [82]. The L_g is varied by 3, 4, 5 and 6 nm, with SiO_2 ($\kappa = 3.9\ \epsilon_0$ with equivalent oxide thickness of 0.41 nm in compatible with ITRS standards) as the gate dielectric. The V_{dd} is chosen as 0.64 V, in accordance with the ITRS 2028 HP requirements. To further improve channel control, symmetric UL regions of 1 nm and 2 nm are introduced between the gate and source/drain, as UL architectures are known to reduce leakage currents and improve performance in the sub-5 nm regime [126]. The resulting device specifications are benchmarked against the ITRS 2028 HP standards for $L_g \approx 5$ nm MOSFETs. Table 5.1 summarizes the technical parameters, including the off-state-current (I_{off}), which meets the ITRS requirement of 0.1 μA μm^{-1} across all UL configurations, and the I_{on}. The on-state voltage (V_{on}) is determined using the relation of $V_{dd} = |V_{on} - V_{off}|$, where V_{on} and V_{off} are the gate voltages in the on- and off-states, respectively [155].

5.5 Influence of Doping Concentration on Device Performance

Accurate control of doping concentration ($N_{e/h}$) in the source and drain regions is critical for efficient carrier injection and overall device performance. To examine this effect, the $I - V_g$ characteristics of n- and p-type DG SiAs monolayer MOSFETs with a 5 nm L_g were calculated along both the armchair and zigzag transport

directions for doping concentrations of 2×10^{13}, 3×10^{13}, 5×10^{13}, 7×10^{13}, and 10^{14} cm^{-2}. As shown in Figure 5.4, the concentration of 5×10^{13} cm^{-2} yields the most favorable performance in devices without UL regions, providing a balanced I_{on}/I_{off} ratio and overall optimized characteristics. On the other hand, devices incorporating 1 nm and 2 nm UL structures (See Figures 5.5 and 5.6, respectively.) exhibit their best performance at a higher doping concentration of 10^{14} cm^{-2}. These results indicate that the optimal doping level depends sensitively on the UL length, underscoring the importance of fine-tuning electrode doping to maximize the performance of DG SiAs MOSFETs.

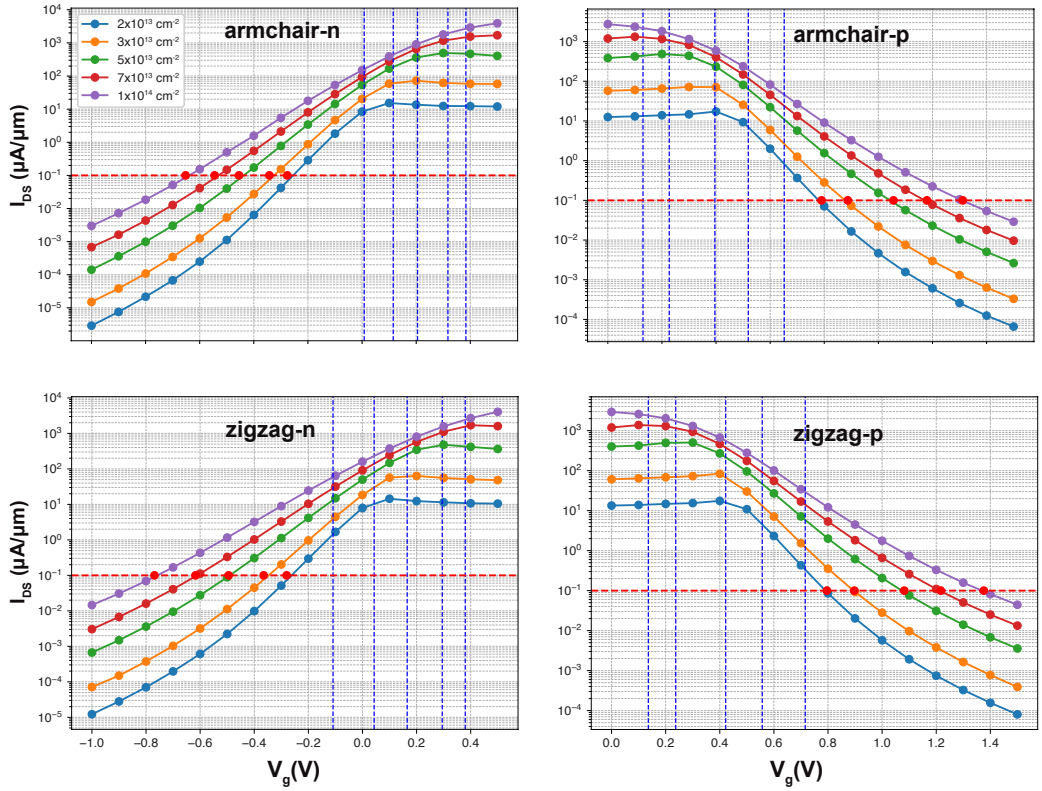


Figure 5.4: Transfer characteristics of n- and p-type DG SiAs monolayer MOSFETs without UL with different doping concentrations along the armchair and zigzag directions, respectively.

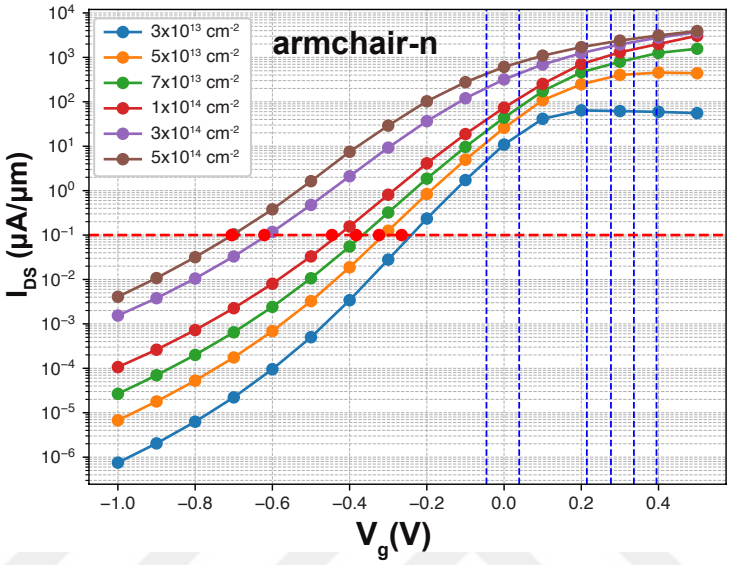


Figure 5.5: Transfer characteristics of n-type DG SiAs monolayer MOSFETs with 1 nm UL for different doping concentrations along the armchair direction.

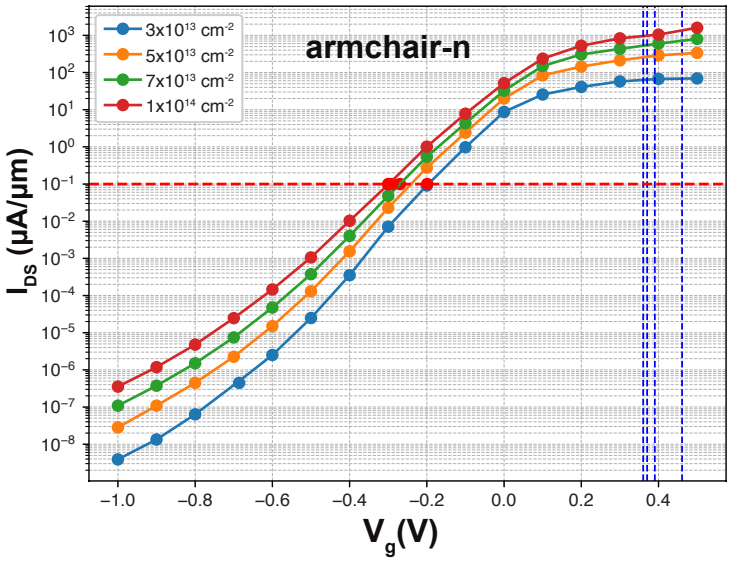


Figure 5.6: Transfer characteristics of n-type DG SiAs monolayer MOSFETs with 2 nm UL for different doping concentrations along the armchair direction.

5.6 Influence of Source/Drain Underlap Modulation on Transfer Characteristics

For logic transistors, the I_{on} is a key figure of merit, as higher values directly translate into faster switching speeds. Figure 5.7a–d presents the $I - V_g$ characteristics of 2D DG SiAs monolayer MOSFETs for n- and p-type devices along both the armchair and zigzag directions, with and without UL structures. In devices without UL (blue curves), a doping concentration of 5×10^{13} cm^{-2} yields a maximum I_{on} of 3.8×10^2 μA μm^{-1}, which falls short of the ITRS 2028 HP requirement. To enhance device performance, UL regions (an uncovered section of the channel by the gate electrode) of 1 nm and 2 nm are introduced, as shown by the orange and green curves in Figure 5.7. The UL increases the effective source-to-drain barrier length, suppressing tunneling leakage and mitigating short-channel effects, though it requires balancing against weaker gate control in the uncovered region. The results demonstrate that appropriate UL modulation significantly boosts device performance, with all UL configurations achieving I_{on} values above the ITRS HP target. The improvement is primarily attributed to reduced electrode-channel coupling, which significantly decreases tunneling leakage current and effectively mitigates short-channel effects. In particular, the 1 nm UL design attains an I_{on} of 12×10^3 μA μm^{-1}, clearly surpassing the ITRS 2028 HP standard. In contrast, when benchmarked against the ITRS 2028 low-power (LP) criteria ($I_{on} = 295$ μA μm^{-1} at $I_{off} = 5 \times 10^{-5}$ μA μm^{-1} and $V_{dd} = 0.64$ V), the simulated 2D DG SiAs MOSFETs exhibit lower drivability. The highest I_{on} achieved in our simulations is 47 μA μm^{-1} for the n-type armchair configuration with a 2 nm UL, while other geometries yield smaller values. These results indicate that the current design is optimized for HP rather than LP operation.

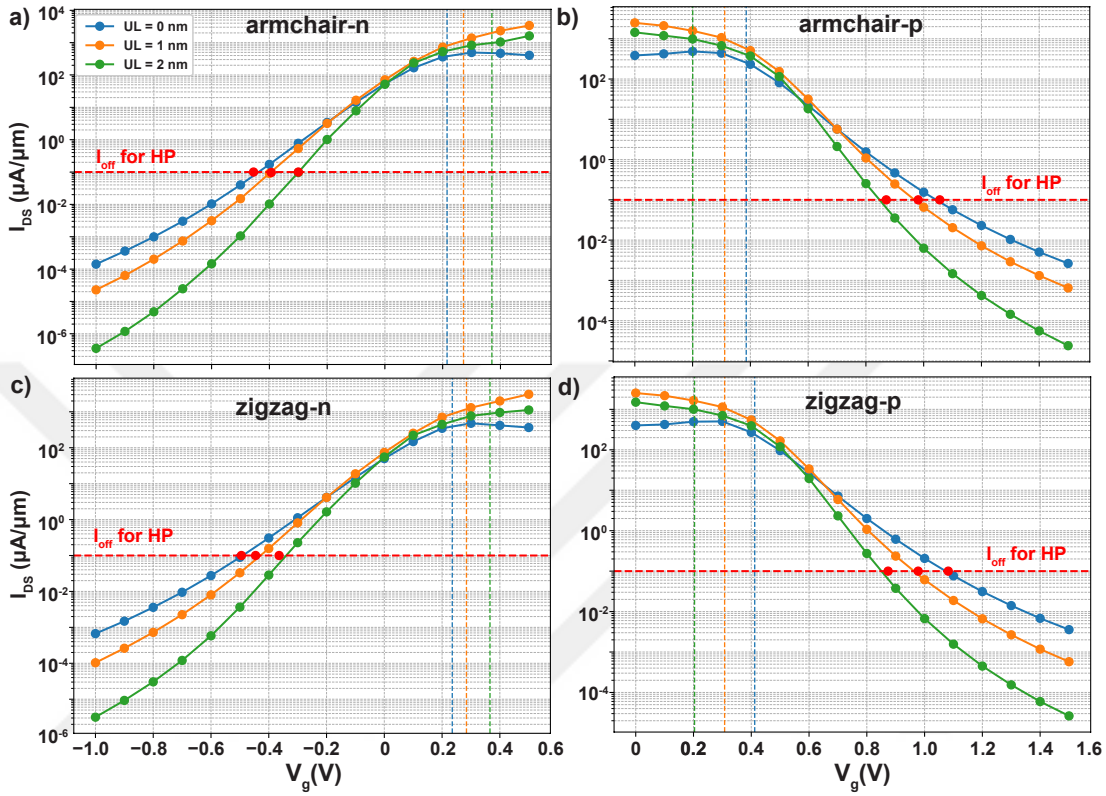


Figure 5.7: Transfer characteristics of armchair- and zigzag-directed 2D DG SiAs MOSFETs with and without the UL region.The dashed horizontal red lines indicate the ITRS-2028 HP I_{off} target (I_{off} = 0.1 μA μm^{-1})

5.7 Underlap Engineering and Its Impact on Electrostatic Gate Control

To illustrate the role of gate control and the effect of UL length on device performance, we calculated the projected local density of states (PLDOS) for DG SiAs monolayer MOSFETs with UL = 0 nm and 1 nm, as shown in Figure 5.8. The PLDOS was evaluated at three V_gs: V_{off}, an intermediate bias of –0.1 V, and V_{on}. A key parameter in this analysis is the effective barrier height (Φ_B), defined as the energy difference between the CBM in the channel and the energy level of the source. A higher Φ_B suppresses electron injection from source to drain in

the off-state, while a reduced barrier facilitates transport in the on-state. For the device without UL ($UL = 0$ nm), the PLDOS maps in Figure 5.8a–c reveal clear modulation of Φ_B with gate bias. At V_{off}, the barrier height is 0.36 eV, effectively blocking carrier transport. At –0.1 V, Φ_B decreases to 0.07 eV, allowing limited injection. Under V_{on}, Φ_B vanishes, indicating that a V_{dd} of 0.64 V is sufficient to lower the CBM and enable efficient current flow between the source and drain.

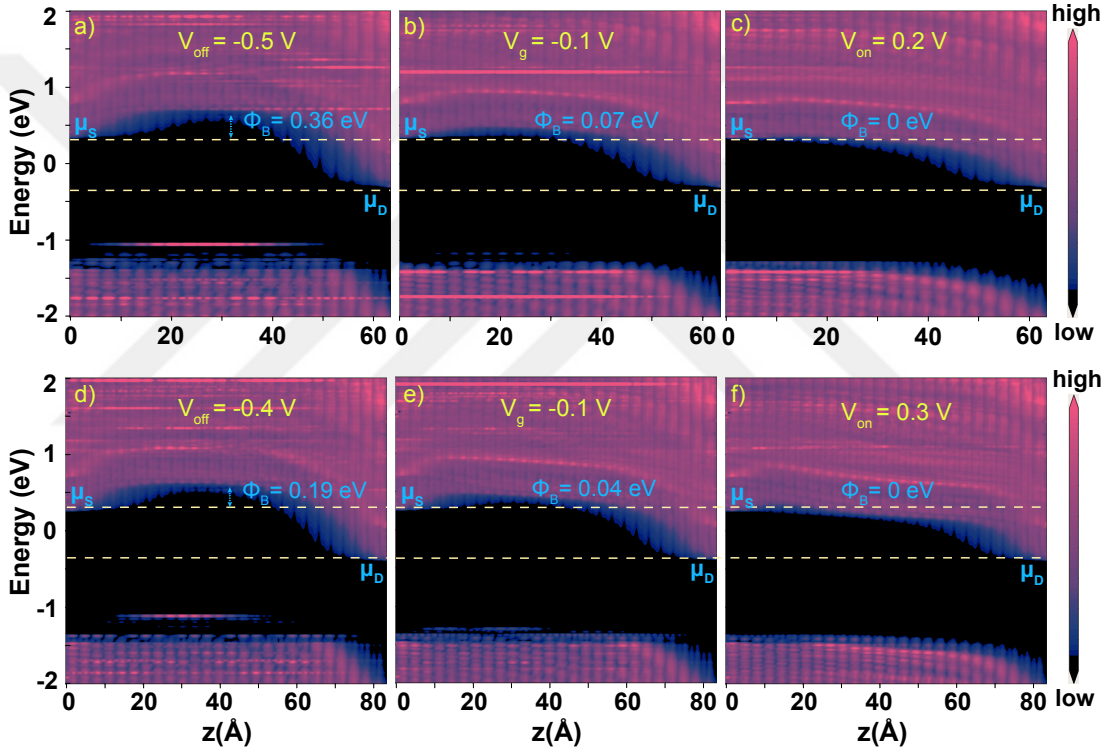


Figure 5.8: The projected local density of states of 2D DG SiAs MOSFETs with the gate-source voltage of a) -0.5 V, b) -0.1 V, and c) 0.2 V for $UL = 0$ nm and d) -0.4 V, e) -0.1 V and f) 0.3 V for $UL = 1$ nm. Yellow dashed lines represent the Fermi level of the source and drain, and Φ_B represents the barrier height.

When a 1 nm UL structure is introduced (Figure 5.8d–f), the gate electrode loses part of its ability to directly control the UL region. In MOSFETs, the gate modulates the channel potential by creating an electrostatic barrier that governs electron transport between the source and drain. However, with a UL configuration, a small gap remains between the gate edge and the channel near the source, which is not directly influenced by the gate. As a result, the potential

in this uncovered region remains lower than in a fully gated channel, yielding a reduced Φ_B of 0.19 eV in the HP off-state. As the V_g increases from the off-state toward the on-state, Φ_B is gradually lowered and eventually reaches 0 eV, allowing efficient current flow across the channel. Interestingly, the PLDOS reveals that with a 1 nm UL, there is a noticeable increase in the electronic states below μ_S, indicating a higher density of available carriers that can be injected into the channel. This enhanced carrier injection is directly reflected in the transport characteristics: the I_{on} rises from 383 μA μm^{-1} without UL to 1206 μA μm^{-1} with a 1 nm UL, surpassing the ITRS 2028 HP standard. These results highlight how UL engineering can substantially improve device performance by facilitating more efficient electron transport in the on-state. In contrast, when the UL length is extended to 2 nm, the gate loses further control over the UL region, which weakens electrostatic coupling and reduces the ability to modulate the potential barrier effectively. This diminished control results in less optimal transport characteristics and degraded performance. Consequently, our analysis is limited to UL lengths up to 2 nm in order to ensure a balance between improved carrier injection and adequate gate control.

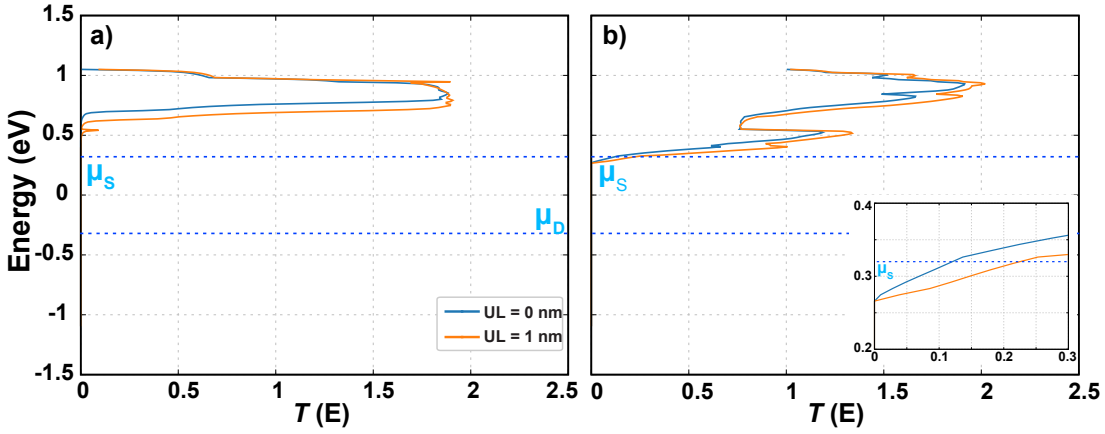


Figure 5.9: Transmission spectra of 2D DG SiAs MOSFETs with varying UL lengths at a) off-state and b) on-state conditions.

Beyond the insights provided by the PLDOS, the transmission spectra T(E) further clarify the performance enhancement introduced by the 1 nm UL structure. Figure 5.9a shows T(E) at I_{off}, while Figure 5.9b presents the corresponding results at I_{on}. In both cases, the edge of T(E) near μ_S is noticeably higher for

the device with a 1 nm UL compared to the configuration without UL. This increase in T(E) reflects a greater probability for electrons to traverse the channel, thereby facilitating more efficient transport from source to drain. The enhanced transmission directly explains the observed rise in I_{on}, as carriers encounter reduced resistance in the presence of the UL structure.

The PLDOS and transmission analyses clearly indicate that an UL length of 1 nm provides effective electrostatic control over the channel region. In this configuration, the drain-induced field penetration is efficiently screened while strong gate modulation is maintained. In contrast, configurations without UL region suffer from pronounced drain coupling and elevated leakage currents, whereas longer underlaps (UL = 2 nm) weaken gate influence, resulting in suppressed I_{on}. It is worth emphasizing that the observed improvement in device performance does not simply arise from an increase in the effective channel length but rather from the optimal electrostatic isolation that the UL region provides between the source and drain. If the enhancement in the I_{on} were primarily driven by the effective channel length rather than the UL configuration, one would expect a continued increase in I_{on} as the UL is extended. For instance, using a 2 nm UL on each side of a 5 nm gate increases the effective channel length to 9 nm, yet it does not produce a higher I_{on} compared to the 1 nm-UL device (effective length of 7 nm). The absence of such an improvement clearly indicates that the performance enhancement originates from optimized electrostatic screening rather than geometric elongation of the channel. The UL should therefore be regarded as a system-specific engineering parameter that can be tuned to suppress short-channel effects and stabilize the channel potential.

5.8 Influence of Gate Length Modulation on Transfer Characteristics

Building on this optimized configuration, the influence of L_g variation was subsequently examined to assess the scalability of the 2D SiAs channel. Transfer

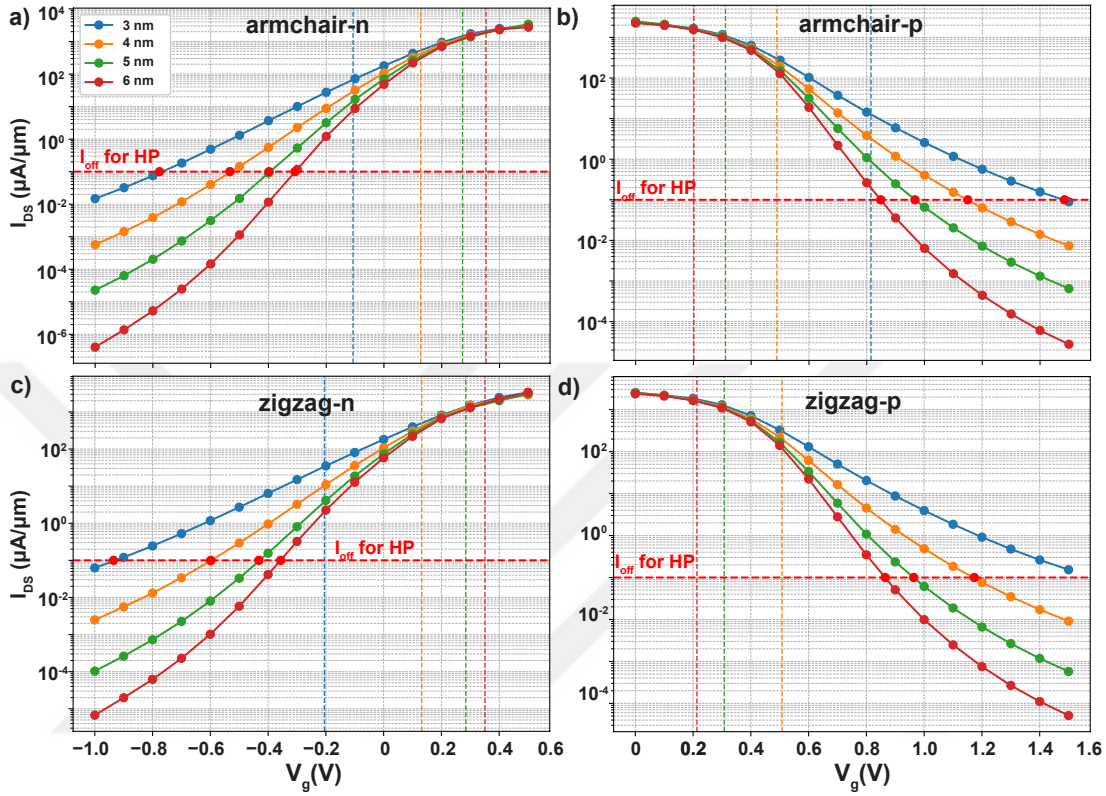


Figure 5.10: Transfer characteristics of 2D DG SiAs MOSFETs with varying gate lengths (L_g = 3, 4, 5, and 6 nm) along (a,b) the armchair and (c,d) the zigzag transport directions for n-type and p-type configurations, respectively. The dashed horizontal red lines indicate the ITRS-2028 HP target (I_{off} = 0.1 μA μm^{-1}). The UL length is fixed at 1 nm for all devices.

characteristics were evaluated for L_g = 3, 4, 5 and 6 nm along both armchair and zigzag directions for n- and p-type channels with UL = 1 nm applied to all devices (shown in Figure 5.10). The 5 nm-gate device corresponds to the ITRS 2028 HP dimensional target (5.1 nm) and was adopted as the reference configuration. Increasing the L_g to 6 nm enhances I_{on} and steepens the subthreshold slope due to improved electrostatic control, although it exceeds the ITRS scaling limit. In contrast, shortening the gate to 3–4 nm leads to reduced I_{on} and a less steep transfer slope, signaling the onset of short-channel effects and source-to-drain tunneling that degrade gate control. The observed scaling trend aligns well with previous studies on sub-10 nm 2D transistors [29], including phosphorene [135], MoS_2 [124, 127], and germanane [156], where ballistic transport and quantum

tunneling limit further performance enhancement at extreme channel dimensions. Collectively, these results demonstrate that beyond a critical L_g, electrostatic integrity, rather than geometric scaling, governs the attainable device performance. Consequently, the 2D DG SiAs MOSFET with $L_g = 5$ nm and $UL = 1$ nm offers an optimal balance between I_{on} and compliance with the ITRS 2028 scaling objectives.

Table 5.1: Ballistic Transport Properties of 2D DG SiAs MOSFETs with and without the UL along the armchair and zigzag directions with the ITRS 2028 for HP standards.

	UL	**SS**	I_{off}	I_{on}	I_{on}/I_{off}	C_g	τ	**PDP**
	(nm)	(mV dec^{-1})	(μA μm^{-1})	(μA μm^{-1})		(fF μm^{-1})	(ps)	(fJ μm^{-1})
ac-n	0	159	0.1	383	3.8×10^3	0.54	0.91	0.10
	1	133		1206	12×10^3	0.66	0.35	0.12
	2	118		984	9.8×10^3	0.51	0.33	0.09
ac-p	0	185	0.1	262	2.6×10^3	0.50	1.21	0.08
	1	142		1007	10×10^3	0.55	0.35	0.09
	2	112		986	9.9×10^3	0.43	0.28	0.07
zz-n	0	180	0.1	393	3.9×10^3	0.55	0.89	0.10
	1	139		1209	12×10^3	0.66	0.35	0.12
	2	125		892	8.9×10^3	0.52	0.37	0.09
zz-p	0	188	0.1	249	2.5×10^3	0.49	1.26	0.08
	1	138		1096	11×10^3	0.52	0.31	0.09
	2	117		996	10×10^3	0.42	0.27	0.07
ITRS-2028	-	-	0.1	900	9×10^3	0.60	0.423	0.24

5.9 Key Device Performance Metrics and Benchmarking

In addition to I_{on} and I_{off}, the transfer characteristics curve also yields another essential performance metric: The SS reflects the switching efficiency of a MOSFET, since it quantifies how effectively the V_g modulates the channel current in the subthreshold region. It is calculated according to the relation [157]:

$$SS = \frac{\partial V_g}{\partial \log I_{ds}} \tag{5.2}$$

A lower SS indicates that a smaller V_g is sufficient to induce a significant change in drain current, enabling faster switching and improved power efficiency. The ideal SS for MOSFETs is approximately 60 mV dec^{-1} at room temperature [158], though reaching this value in ultra-scaled devices is hindered by short-channel effects and leakage currents. The calculated SS values for all configurations are summarized in Table 5.1. Our results show that the UL structure has a pronounced impact on switching efficiency. While devices without UL exhibit the largest SS, the 1 nm UL configuration achieves values in the range of 133–142 mV dec^{-1}. Further improvement is observed for the 2 nm UL configuration, where SS decreases to 112–125 mV dec^{-1}. This enhancement is attributed to reduced short-channel effects and improved electrostatic control provided by the UL regions, establishing UL engineering as an effective strategy for optimizing the switching characteristics of 2D SiAs MOSFETs.

Fast switching is another crucial requirement for digital circuits and HP devices, as it directly impacts the efficiency and speed of modern electronic systems. The switching speed of a MOSFET is often characterized by the intrinsic delay time (τ), defined as [157]:

$$\tau = \frac{C_g \cdot V_{dd}}{I_{on}}, \tag{5.3}$$

where C_g is the total gate capacitance. The total capacitance is expressed as $C_g = C_{ch} + C_{fr}$, where C_{fr} is assumed to be twice the intrinsic channel capacitance C_{ch}, calculated as

$$C_{ch} = \frac{\partial Q_{ch}}{\partial V_g}, \tag{5.4}$$

with Q_{ch} denoting the total charge in the channel. The calculated C_g values for DG SiAs MOSFETs fall within 0.42–0.66 fF μm^{-1}, satisfying the ITRS requirements across most device configurations. For n-type devices with a 1 nm UL, C_g can be further optimized by tuning the UL length, providing an additional pathway to enhance device performance. According to the above relation, faster switching requires minimizing C_g while maximizing I_{on}, thereby reducing τ. The calculated delay times, summarized in Table 5.1, show that UL engineering plays a decisive role: devices without UL exhibit longer delays, whereas UL configurations reduce τ to 0.27–0.37 ps. This substantial reduction underscores the effectiveness of UL structures in boosting switching speed, positioning DG SiAs MOSFETs as competitive candidates for next-generation HP applications.

The power–delay product (PDP) is another critical metric for assessing MOSFET performance, particularly in terms of energy efficiency. It is defined as

$$PDP = \frac{(Q_{on} - Q_{off}) \cdot V_{dd}}{W}, \tag{5.5}$$

where W is the channel width, and Q_{on} and Q_{off} are the total charges in the channel in the on- and off-states, respectively. The PDP represents the energy dissipated during a single switching event, making it a direct measure of power consumption per operation. As summarized in Table 5.1, all DG SiAs MOSFET configurations yield PDP values in the range of 0.07–0.12 fJ μm^{-1}, which are significantly lower than the ITRS 2028 HP targets. These results demonstrate that SiAs transistors combine high performance with excellent energy efficiency, underscoring their promise for ultra-scaled, LP logic applications.

To place the performance of 2D DG SiAs MOSFETs in context relative to other emerging 2D semiconductors, we compared their key device metrics with the reported values for MoS_2[127], InSe [131], and germanane [156] FETs under similar HP 5 nm node conditions. For the n-type operation, the 2D DG SiAs MOSFET delivers an I_{on} of 1209 μA μm^{-1} with a SS of 139 mV dec^{-1}, outperforming MoS_2 (473 μA μm^{-1}, SS = 58 mV dec^{-1}) and germanane (900 μA μm^{-1}, SS = 136 mV dec^{-1}), and approaching the performance of InSe (1538 μA μm^{-1}, SS = 112 mV dec^{-1}). Similarly, the p-type SiAs device achieves an I_{on} of 1096 μA μm^{-1} with an SS of 138 mV dec^{-1}, surpassing MoS_2 (439 μA μm^{-1}, SS = 46 mV dec^{-1}) and germanane (729 μA μm^{-1}, SS = 79 mV dec^{-1}), while remaining comparable to InSe (1146 μA μm^{-1}, SS = 112 mV dec^{-1}). These comparisons show that the SiAs monolayer offers a well-balanced combination of high current drivability and moderate subthreshold characteristics, maintaining nearly similar performance for both carrier types. Considering these results, SiAs monolayer is positioned as a competitive 2D semiconductor capable of sustaining HP transistor operation at the sub-5 nm scale.

5.10 Conclusion

In this section of the thesis, the ballistic transport properties of DG SiAs monolayer MOSFETs with $L_g \approx 5$ were investigated using first-principles calculations combined with the NEGF formalism. Key device metrics, including I_{on}, SS, C_g, τ, and PDP, were systematically analyzed to assess the suitability of SiAs for ultra-scaled transistor applications. Our results demonstrate that UL engineering plays a decisive role in optimizing device performance. In particular, the 1 nm UL configuration yields a remarkable increase in I_{on} up to 1206 μA μm^{-1}, surpassing the ITRS 2028 HP requirement. The inclusion of UL regions also reduces SS values to 112–142 mV dec^{-1} and shortens the intrinsic delay time to 0.27–0.37 ps, enabling high-speed operation. Furthermore, all device configurations exhibit PDP values well below the ITRS targets, confirming excellent energy efficiency. By overcoming the scaling limitations of conventional silicon-based MOSFETs, DG SiAs monolayer transistors emerge as strong candidates for next-generation

semiconductor technologies. Their ability to deliver high I_{on}, competitive switching characteristics and low power consumption positions SiAs as a promising 2D material for ultra-scaled, energy-efficient logic applications.

Chapter 6

Final Remarks and Outlook

6.1 Final Remarks and Outlook

This thesis has presented a comprehensive investigation into the design and transport properties of nano-devices based on 2D semiconductors. The investigation is driven by the critical need to identify materials and architectures capable of sustaining transistor scaling beyond the limits of silicon technology. This work systematically evaluated the electronic and ballistic transport characteristics of Janus Ge_2PAs, GaSe, and SiAs monolayers across diverse device configurations ranging from simple Metal-Semiconductor-Metal structures to complex Double-Gate MOSFETs by employing a theoretical framework that combines Density Functional Theory with the Non-Equilibrium Green's Function formalism. The findings emphasize the potential of these materials for high-performance logic applications while highlighting the necessity of architectural optimization.

The initial phase of this research focused on the Janus Ge_2PAs monolayer and revealed its potential as a channel material in Metal-Semiconductor-Metal devices. The study demonstrated that the electronic behavior of these devices is governed by an interplay between channel length and electrode doping concentration. It was established that a minimum channel length of 6.5 nm is required to observe typical

Metal-Semiconductor-Metal behavior. The analysis further demonstrated that increasing electrode doping concentrations enhances current values. This occurs because higher doping increases the density of states and narrows the Schottky barrier. High doping thereby facilitates efficient tunneling at higher bias voltages.

Building on the initial study of the Metal-Semiconductor-Metal architecture, the research expanded to examine 2D GaSe nano-devices in increasingly complex configurations. This hierarchy included p-n junction diodes, p-i-n Field-Effect Transistors, and Double-Gate MOSFETs. Crucially, the GaSe p-n junctions demonstrated distinct backward diode characteristics. In this regime, the reverse current notably surpasses the forward current, a phenomenon driven by efficient interband tunneling at low bias. The study further demonstrated that this backward conduction can be selectively controlled in p-i-n Field-Effect Transistors via gate modulation. For high-performance logic applications, the zigzag-n configuration of GaSe Double-Gate MOSFETs were particularly effective. In terms of key figures of merit such as switching speed and on/off ratio, the device performance aligns with the ITRS-2028 High-Performance standards.

The final investigation addressed the scalability of 2D SiAs monolayers in sub-5 nm Double-Gate MOSFETs. This portion of the work emphasized the critical role of UL engineering in optimizing device performance. The results showed that introducing a 1 nm UL region effectively screens the channel from drain-induced fields without compromising gate control and leads to an increase in on-state current. The optimized SiAs devices exhibited power-delay products significantly below industry benchmarks that highlight their superior energy efficiency. This performance validates their suitability for ultra-scaled, energy-efficient logic applications. Collectively, these studies illustrate that performance enhancement in 2D nanoelectronics relies not only on the intrinsic properties of the material but also on precise electrostatic engineering.

The findings and constraints of this study highlight a number of directions for future investigation. The current transport simulations operate under the ballistic limit. This assumption excludes inelastic scattering processes such as electron-phonon interactions. While this assumption is justified for the sub-10

nm channel lengths, future studies that incorporate scattering mechanisms can provide a more accurate estimation of device performance. Additionally, the device models employed electrostatic doping to simulate contacts. Future work can focus on modeling explicit metal-semiconductor interfaces that are critical challenges in the experimental realization of 2D electronics. Finally, extending the device architectures to include realistic high-k dielectrics would provide valuable guidance for the next-generation semiconductor technologies.

Looking ahead, artificial intelligence and machine learning present a major opportunity to revolutionize the optimization of 2D devices. Machine learning potentials can bridge the gap between cost and accuracy to facilitate large-scale simulations. These simulations effectively capture crucial factors such as inelastic scattering and thermal effects, beyond the ballistic limit. Additionally, AI-driven inverse design algorithms can efficiently explore the vast space of device parameters.

6.2 Publication List

- Mohammad Abboud, Dogukan Hazar Ozbey, and Engin Durgun, "Strain-induced structural phase transition in GeN monolayer," *Applied Surface Science* **567**, 150793 (2021). DOI:10.1016/j.apsusc.2021.150793

- Mohammad Abboud, Dogukan Hazar Ozbey, Mehmet Emin Kilic, and Engin Durgun, "Investigation of anisotropic mechanical, electronic, and charge carrier transport properties of germanium-pnictogen monolayers," *Journal of Physics D: Applied Physics* **55**, 185302 (2022). DOI:10.1088/1361-6463/ac4cf9

- Dogukan Hazar Ozbey, Mehmet Emin Kilic, and Engin Durgun, "Two-dimensional Janus GePAs Monolayer: A Direct-Band-Gap Semiconductor with High and Anisotropic Mobility for Efficient Photocatalytic Water Splitting," *Physical Review Applied* **17**, 034043 (2022). DOI:10.1103/PhysRevApplied.17.034043

- Dogukan Hazar Ozbey, Mehmet Emin Kilic, and Engin Durgun, "Promising anisotropic mechanical, electronic, and charge transport properties of 2D InN alloys for photocatalytic water splitting," *Applied Surface Science* **638**, 157982 (2023). DOI:10.1016/j.apsusc.2023.157982

- Saliha Mutlu, Bülend Ortaç, Dogukan Hazar Ozbey, Engin Durgun, Sevil Savaskan Yilmaz, and Nergis Arsu, "Laser-Driven Rapid Synthesis of Metal-Organic Frameworks and Investigation of UV-NIR Optical Absorption, Luminescence, Photocatalytic Degradation, and Gas and Ion Adsorption Properties," *Polymers* **16**, 217 (2024). DOI:10.3390/polym16020217

- Dogukan Hazar Ozbey, Mirali Jahangirzadeh Varjovi, Gözde Özbal Sargın, Haldun Sevinçli, and Engin Durgun, "Structural, electronic, vibrational, and thermoelectric properties of Janus Ge_2PX (X = N, As, Sb, and Bi) monolayers," *Physical Review B* **110**, 035411 (2024). DOI:10.1103/PhysRevB.110.035411

- Taylan Gorkan, Dogukan Hazar Ozbey, Mehmet Emin Kilic, and Engin Durgun, "Two-dimensional 2γ-In_2Se_3 in bilayer-like coloring triangle lattice: Mechanical, electronic, transport, and photocatalytic properties," *Physical Review Materials* **8**(11), 114001 (2024). DOI:10.1103/PhysRevMaterials.8.114001

- Dogukan Hazar Ozbey, Gözde Özbal Sargın, V. Ongun Özçelik, and Engin Durgun, "Electronic transport properties of Janus Ge_2PAs monolayer: A prototype two-dimensional metal–semiconductor–metal device" *Journal of Applied Physics)* **138**(8) (2025) DOI:10.1063/5.0283827

- Gözde Özbal Sargın, Mirali Jahangirzadeh Varjovi, Dogukan Hazar Ozbey, Haldun Sevinçli, and Engin Durgun, "Computational investigation of electronic, vibrational, and transport properties of silicon phosphide nanoribbons," *Physical Review Materials* **9**(10) p.104002 (2025) DOI:10.1103/16sl-zs96

- Taylan Gorkan, Dogukan Hazar Ozbey, Cem Sevik, Milorad V. Milošević and Engin Durgun, "Flat Bands vs Dirac Nodal Lines in the Bilayer Kagome Lattices" *Resubmitted*

- Dogukan Hazar Ozbey and Engin Durgun, "High-Performance and Energy-Efficient Sub-5 nm 2D Double-Gate MOSFETs Based on SiAs Monolayers" *Accepted in Advanced Electronic Materials (in press)*

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