ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES

PhD THESIS

Arzu TÜRKSOY

IMPLEMENTATION OF ACTIVE CELL BALANCING CIRCUIT FOR BATTERY MANAGEMENT SYSTEM IN ELECTRIC VEHICLES

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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ABSTRACT

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In electric vehicles (EVs), a battery management system (BMS) is used to prevent the harmful effect of intercellular imbalance in the battery pack consisting of many cells, to improve the pack capacity and to keep the cells in a safe operating range. Battery balancing system (BBS) is designed to eliminate imbalances between cells and keep the SOC or terminal voltage of each cell equal. The performance of BBS is expressed by the available capacity and balancing speed at the end of balancing. The increase in balancing speed and efficiency is largely dependent on the balancing control strategy. In this thesis, control strategies are proposed for two different active balancing topologies. In the first of the proposed designs, an optimal balancing control strategy for a single flyback converter- based cell-to-pack balancing topology is developed to minimize balancing time and maximize the balancing efficiency. While the shortening of the balancing time provides a safer battery use, the usable capacity of the battery increases with the increase in efficiency. This means longer ranges for electric vehicles. In the second of the designs, a novel balancing control strategy for a multiple flyback converter-based cell-to-pack-to-cell balancing topology is developed to minimize balancing time and maximize the balancing efficiency. With the proposed control strategy, the switching losses and the charging losses in the balancing circuit are minimized by ensuring the use of the power circuit with minimum time.

Key Words: Battery Management System, Active Battery Balancing, Balancing Control Strategy, Electric Vehicles.

ÖZ

DOKTORA TEZİ

ELEKTRİKLİ ARAÇLARDA BATARYA YÖNETİM SİSTEMİ İÇİN AKTİF HÜCRE DENGELEME DEVRESİNİN UYGULANMASI

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Elektrikli araçlarda çok sayıda hücreden oluşan pil paketindeki hücreler arası dengesizliğin zararlı etkisini önlemek, paket kapasitesini iyileştirmek ve pilleri güvenli bir çalışma alanında tutmak için batarya yönetim sistemi kullanılmaktadır. Batarya dengeleme sistemi, hücreler arasındaki dengesizlikleri ortadan kaldırmak ve her hücrenin SOC veya terminal voltajını eşit tutmak için tasarlanmıştır. Batarya dengeleme sisteminin performansı, dengeleme sonunda mevcut kapasite ve dengeleme hızı ile ifade edilir. Dengeleme hızı ve dengeleme verimliliğindeki artış, büyük ölçüde dengeleme kontrol stratejisine bağlıdır. Bu tezde, iki farklı aktif dengeleme topolojisi için kontrol stratejileri önerilmiştir. Önerilen tasarımların ilkinde, dengeleme süresini en aza indirmek ve dengeleme verimliliğini en üst düzeye çıkarmak için tek bir flyback dönüştürücü tabanlı hücreden pakete şarj transferi yapan dengeleme topolojisi için en uygun dengeleme kontrol stratejisi geliştirilmiştir. Dengeleme süresinin kısalması daha güvenli bir akü kullanımı sağlarken, verim artışı ile birlikte akünün kullanılabilir kapasitesi de artmaktadır. Bu da elektrikli araçlar için daha uzun menzil anlamına gelmektedir. Tasarımların ikincisinde, dengeleme süresini en aza indirmek ve dengeleme verimliliğini en üst düzeye çıkarmak için çoklu geri dönüş dönüştürücü tabanlı hücreden pakete paketten hücreye enerji aktarımı yapan dengeleme topolojisi için yeni bir dengeleme kontrol stratejisi geliştirildi. Önerilen kontrol stratejisi ile güç devresinin minimum sürede kullanılması sağlanarak, dengeleme devresindeki anahtarlama kayıpları ve şarj kayıpları minimize edilmiştir.

Anahtar Kelimeler: Batarya Yönetim Sistemi, Aktif Batarya Dengeleme, Dengeleme Kontrol Stratejisi, Elektrikli Araçlar.

EXTENDED SUMMARY

In recent years, the extensive use of oil resources in internal combustion engine (ICE) vehicles has caused serious problems, such as increasing CO_2 emissions and depletion of the ozone layer. Also, with the depletion of fossil fuels and high crude oil prices, environmentally-friendly EVs have become an attractive choice for the automobile industry. However, the wide adoption of EVs needs further improvements in rechargeable batteries and their BMS. Because the battery is seen as one of the major obstacles to the mass marketing of EVs. Different ways are carried out to increase the pack capacity of the existing battery pack. One of these is to develop battery chemistry offering higher energy density. The other way is to increase the capacity of the battery pack with additional cells.

Among the existing battery technologies, lithium-ion (Li-ion) batteries have salient features in terms of higher energy density, lower self-discharge rate, higher specific power, and high lifecycle. However, a single Li-ion cell provides a maximum of 4.2 V. So, a battery pack consists of hundreds of cells connected in series or/and parallel to meet the voltage and capacity requirements of EVs. However, cell imbalances increase as the number of cells increases, and it exacerbates with the repeated charging and discharging cycles over time. The imbalances often arise from unavoidable internal factors such as the feature of material, imperfection of cell production, and assembly technique. This causes variations in the initial conditions, such as internal resistance (Ri), capacity, state of charge (SOC), and self-discharge rate (SD-rate). On the other hand, external factors which mainly arise from the charging/discharging current and localization of cells leads to the temperature and depth of discharge (DOD) variations between the battery cells. Discharging/charging of the series battery pack must stop when any cell reaches the lower/upper cut-off voltage so-called "safe operating voltage limits" to prevent safety hazards. On the other hand, the total usable capacity of the battery pack is limited by the cell with minimum capacity. Therefore, in case of considerable imbalance, capacity utilization drops drastically, affecting the battery pack's overall service performance.

A BMS is implemented to preclude the detrimental effect of cell imbalance, ensure the improvement of the pack capacity and keep each cell within a safe operating region. The battery balancing system (BBS) which is a core function of BMS is designed to eliminate the imbalances among the cells and keep the SOC or terminal voltage of each cell equal. The BBS monitors a battery pack in use, identifies the charge state of each cell, and detects imbalances between cells. If the imbalance exceeds a certain threshold, it distributes energy between the high and low-charged cells. A BBS consists of a hardware and software part that is described as a balancing circuit and a balancing control strategy (BCS), respectively. BBSs are divided into two main categories dissipative, called passive balancing, and non-dissipative called active balancing, according to the energy transfer mode. A passive balancing consumes the excessive energy of any high-charged cell using a shunt resistor connected in parallel and converts it to heat. Passive balancing performs with two different circuits, such as fixed shunt resistors and switched shunt resistors. Although it has a simple implementation and is cost-effective, it suffers from several issues, such as low balancing efficiency and large heat generation. Also, passive balancing can be performed only when the battery pack is in charging condition. On the other hand, active balancing transfers the energy from a high-charged cell into a low-charged cell using power electronic circuits. There are three topological approaches to active balancing: cell-to-cell (CTC), cell-to-pack (CTP), pack-to-cell (PTC), and cell-to-pack-to-cell (CTPTC). CTC topologies transfer energy between high-charged cells and low-charged cells. CTP topologies transfer the excess energy of the high-charged cell to the battery pack; likewise, PTC topologies transfer the energy from the battery pack to the weak cells. Also, by integrating PTC and CTP, it is also possible to achieve efficient balancing by providing simultaneous charging and discharging of individual cells. CTP and PTC balancing topologies can achieve high balancing currents due to the fact that the voltage difference between the cell and the pack is larger than the voltage difference between any two cells. A large balancing current increases the balancing speed and consequently minimizes the balancing time.

In addition to the topology selection, the selection of the power electronics circuit suitable for the topology is an important issue. Active balancing circuits are divided into three categories in the literature. These are capacitor-based, inductor/transformer-based, and DC-DC converter-based balancing circuits. In general, each balancing circuit design (combining balancing topology and balancing circuit design) has its own advantages and disadvantages in terms of speed, accuracy, efficiency, and cost. Among them, DC-DC converter-based CTP or PTC balancing circuits have superior features due to their high-speed balancing performance, lower charge losses, compact designs, and easy controllability.

Among the various DC-DC converter types, the flyback converter is widely used for CTP or PTC balancing topologies in the existing literature. They provide a safer balancing process in terms of providing insulation between the battery pack and the cell. Also, it can provide a large balancing current to minimize the balancing time.

There are two different balancing circuit scheme which is used flyback converter. The first is the single (common) flyback converter scheme, which allows sequential charging or discharging of unbalanced cells. In single flyback converter-based CTP or PTC balancing circuits, only one cell can be discharged or charged at any given time by design nature. The flyback converter operates in buck and boost modes, respectively. The second balancing scheme is a multiple flyback converter-based balancing scheme, called an individual cell balancer (ICB), in which a flyback converter is used for each cell ensuring simultaneous charging or discharging. The first balancing scheme is more inexpensive and smaller in size; however, the second scheme offers a faster balancing process, is more compact, and is convenient for increasing cell numbers.

Balancing control strategy (BCS) is of utmost importance for balancing performance which defines in terms of balancing time and usable capacity. Increasing the usable capacity is achieved by a balanced battery pack. It is important that this balancing is completed as soon as possible. Considering the BEV may be charged to 80% with direct current fast charging (DCFC) equipment in only 20 minutes to 1 hour, the balancing process must be completed before this time range to maximize the usable capacity.

Each flyback converter-based balancing scheme uses a different BCS to implement the balancing process. Control strategies use a control algorithm that is designed to complete balancing in minimum time. These algorithms make decisions according to the control variable used in their input. These control variables can be the terminal voltage of the cell or SOC information. SOC information cannot be measured directly like the terminal voltage of a cell, and it is expressed using advanced techniques such as high-level estimation methods. However, since they provide more accurate information about the internal state of Li-ion battery cells, they provide more precise and reliable balancing. There are many different control algorithms using the same control variable. For single flyback converter-based balancing schemes, studies have been carried out on algorithms that determine the charge or discharge order of these cells without using any mathematical model or balancing current control. Cells are connected to the converter input terminal via the switch matrix, and the MOSFET switch of the flyback converter is triggered by fixed-duty cycle PWM to provide maximum balancing current for minimizing balancing time. However, if there is more than one unbalanced cell in the battery pack connected in series, it creates repetitive charge-discharge cycles. This results in longer balancing time, lower balancing efficiency, and shortening of battery life, especially in EV battery packs with a large number of cells.

On the other hand, ICB-based CTPTC with multiple flyback converters has the advantage of the hardware in terms of balancing speed. However, controlling the balancing process with BCS, which provides a high balancing current causes the intermediate cells to reach the balanced region earlier than the other cells, as stated in the CTP topology. In order for these cells to remain in the stable region, they must be exposed to charged/discharged with high currents. In the studies in the literature, BCSs have been proposed, which provides the cells to come to the balanced region at the same time by estimating the balancing currents of each cell to eliminate the repetitive charge-discharge cycles. Even if the amount of energy consumed on the switches is reduced, the simultaneous operation of all converters still suffers high power losses.

In this thesis, new BCSs are presented to overcome the problems encountered in single unidirectional flyback converter-based CTP and multiple bidirectional flyback-based CTPTC individual cell balancing topologies. First, a two-stage BCS is proposed for the single flyback converter-based CTP topology, which objectively determines the minimum balancing time by eliminating repetitive charge/discharge cycles. In order to achieve simultaneous discharging of battery cells, the variable switching time dividing method is developed in the first stage of developed BCS. In order to eliminate repetitive cycles, a novel optimization algorithm is developed that obtains discharging current of each cell in the second stage. The benchmark is realized for the proposed BCS and existing rule-based BCS in terms of the balancing time and the balancing efficiency. The performed case study has demonstrated that balancing speed is greatly shortened. Second, a novel BCS is developed for ICB-based CTPTP balancing topology for reducing overall energy consumption on the balancing circuit as well as minimizing the balancing time. The proposed strategy achieves these goals by using the minimum balancing circuitry at any time interval and prioritizing charging the cell with the lowest SOC.

The proposed BCS significantly reduces the control complexity of the system, which is important considering the requirement of a huge number of cells for EVs.

The two proposed topology and control strategies were designed and analyzed with detailed simulation studies using the MATLAB/Simulink simulation program. Moreover, the BBS developed for the ICB-based CTPTC topology has been applied experimentally. Different initial SOC differences were considered as case studies, and the performance of the BCS developed with the experimental results was verified.

GENİŞLETİLMİŞ ÖZET

Son yıllarda içten yanmalı motorlu araçlarda petrol kaynaklarının yoğun kullanımı CO2 emisyonlarının artması, ozon tabakasının incelmesi gibi ciddi sorunlara yol açmaktadır. Ayrıca, fosil yakıtların tükenmesi ve yüksek ham petrol fiyatları ile çevre dostu EA'lar otomobil endüstrisi için cazip bir seçim haline geldi. Bununla birlikte, EA'ların geniş çapta benimsenmesiyle, şarj edilebilir pillerde ve bunların batarya yönetim sistemlerinde (BYS) daha fazla iyileştirmeye ihtiyaç duyulmaktadır. Çünkü pil, EA'ların kitlesel pazarlamasının önündeki en büyük engellerden biri olarak görülmektedir. Mevcut pil paketinin paket kapasitesini artırmak için farklı yöntemler uygulanmaktadır. Bunlardan biri, daha yüksek enerji yoğunluğu sunan pil kimyasını geliştirmektir. Diğer yol ise, pil takımının kapasitesini ek hücrelerle artırmaktır.

Mevcut pil teknolojileri arasında, lityum-iyon (Li-ion) piller, daha yüksek enerji yoğunluğu, daha düşük kendi kendine deşarj oranı, daha yüksek özgül güç ve yüksek kullanım ömrü açısından öne çıkan özelliklere sahiptir. Bununla birlikte, tek bir Li-ion hücre maksimum 4,2 V sağlar. Bu nedenle, bir pil paketi, EV'lerin voltaj ve kapasite gereksinimlerini karşılamak için seri ve/veya paralel bağlanmış yüzlerce hücreden oluşur. Ancak hücre dengesizlikleri hücre sayısı arttıkça artar ve zamanla tekrarlanan şarj ve deşarj döngüleri ile şiddetlenir. Dengesizlikler genellikle malzemenin özelliği, hücre üretiminin kusurlu olması ve montaj tekniği gibi kaçınılmaz iç faktörlerden kaynaklanır. Bu, iç direnç (Ri), kapasite, şarj durumu (SOC) ve kendi kendine deşarj oranı gibi başlangıç koşullarında değişikliklere neden olur. Öte yandan, esas olarak şarj/deşarj akımından ve hücrelerin lokalizasyonundan kaynaklanan dış etkenler, pil hücreleri arasında sıcaklık ve deşarj derinliği farklılıklarına neden olur. Güvenlik tehlikelerini önlemek için herhangi bir hücre "güvenli çalışma voltajı limitleri" olarak adlandırılan alt/üst kesme voltajına ulaştığında seri pil paketinin boşalması/şarjı durmalıdır. Diğer yandan, pil paketinin toplam kullanılabilir kapasitesi, minimum kapasiteye sahip hücre ile sınırlıdır. Bu nedenle, önemli bir dengesizlik durumunda, kapasite kullanımı büyük ölçüde düşer ve bu da pil takımının genel hizmet performansını etkiler.

Hücre dengesizliğinin zararlı etkilerini önlemek, paket kapasitesinin iyileştirilmesini sağlamak ve her hücreyi güvenli bir çalışma bölgesinde tutmak için bir BMS uygulanmaktadır. BYS'nin temel işlevi olan batarya dengeleme sistemi (BDS), hücreler arasındaki dengesizlikleri ortadan kaldırmak ve her bir hücrenin SOC veya terminal voltajını eşit tutmak için tasarlanmıştır. BYS, kullanımda olan bir pil takımını izler, her bir hücrenin şarj durumunu tanımlar ve hücreler arasındaki dengesizlikleri saptar. Dengesizlik belirli bir eşiği aşarsa, enerjiyi yüksek ve düşük yüklü hücreler arasında dağıtır. Bir BDS, sırasıyla dengeleme devresi ve dengeleme kontrol stratejisi olarak tanımlanan bir donanım ve yazılım bölümünden oluşur. BDS'ler, enerji aktarım şekline göre, pasif dengeleme adı verilen tüketen ve aktif dengeleme adı verilen tüketmeyen olarak adlandırılan iki ana kategoriye ayrılır. Pasif dengeleme, paralel bağlı bir şönt direnci kullanarak herhangi bir yüksek şarjlı hücrenin aşırı enerjisini tüketir ve onu ısıya dönüştürür. Pasif dengeleme, sabit şönt dirençler ve anahtarlamalı şönt dirençler olmak üzere iki farklı devre ile gerçekleştirilir. Basit bir uygulaması olmasına ve uygun maliyetli olmasına rağmen, düşük dengeleme verimliliği ve büyük ısı üretimi gibi çeşitli sorunlardan muzdariptir. Ayrıca, pasif dengeleme yalnızca pil takımı şarj durumundayken gerçekleştirilebilir. Öte yandan aktif dengeleme, güç elektroniği devrelerini kullanarak enerjiyi yüksek şarjlı bir hücreden düşük şarjlı bir hücreye aktarır. Aktif dengeleme için üç topolojik yaklaşım vardır: hücreden hücreye (HH), hücreden pakete (HP), paketten hücreye (PH) ve hücreden pakete (HPH). HH topolojiler, enerjiyi yüksek şarjlı hücre ile düşük şarjlı hücre arasında aktarır. HP topolojiler yüksek şarjlı hücrenin fazla enerjisini pil takımına aktarır, benzer şekilde PH topolojiler ise enerjiyi pil takımından zayıf hücrelere aktarır. Ayrıca, PH ve HP'yi entegre ederek, tek tek hücrelerin aynı anda şarj edilmesini ve boşaltılmasını sağlayarak verimli dengeleme elde etmek de mümkündür. HP ve PH dengeleme topolojileri ile, hücre ile paket arasındaki gerilim farkının herhangi iki hücre arasındaki gerilim farkından daha büyük olması nedeniyle yüksek dengeleme akımına ulaşılabilir. Büyük bir dengeleme akımı, dengeleme hızını artırır ve sonuç olarak dengeleme süresini en aza indirmektedir.

Topoloji seçiminin yanı sıra topolojiye uygun güç elektroniği devresinin seçimi de önemli bir konudur. Aktif dengeleme devreleri literatürde üç kategoriye ayrılmaktadır. Bunlar kapasitör tabanlı, indüktör/trafo tabanlı ve DA-DA dönüştürücü tabanlı dengeleme devreleridir. Genel olarak, her dengeleme devresi tasarımının (dengeleme topolojisi ve dengeleme devresi tasarımını birleştiren) hız, doğruluk, verimlilik ve maliyet açısından kendi avantajları ve dezavantajları vardır. Bunlardan DA-DA dönüştürücü tabanlı HP veya PH balans devreleri, yüksek hızlı dengeleme performansı, daha düşük şarj kayıpları, kompakt tasarımları ve kolay kontrol edilebilmeleri bakımından üstün özelliklere sahiptir.

Çeşitli DA-DA dönüştürücü türleri arasında, flyback dönüştürücü, mevcut literatürde HP veya PH dengeleme topolojileri için yaygın olarak kullanılmaktadır. Pil takımı ile hücre arasında yalıtım sağlaması açısından daha güvenli bir dengeleme işlemi sağlarlar. Ayrıca dengeleme süresini en aza indirmek için büyük dengeleme akımı sağlayabilir.

Flyback dönüştürücü kullanılan iki farklı dengeleme devre şeması vardır. Birincisi, dengesiz hücrelerin sıralı olarak yüklenmesine veya boşaltılmasına izin veren tek (ortak) geri dönüş dönüştürücü şemasıdır. Tek geri dönüş dönüştürücü tabanlı CTP veya PTC dengeleme devrelerinde, tasarım doğası gereği herhangi bir zamanda yalnızca bir hücre deşarj veya şarj edilebilir. Geri dönüş dönüştürücü, sırasıyla düşüren ve yükselten modunda çalışır. İkinci dengeleme şeması, bireysel hücre dengeleyici (ICB) adı verilen çoklu geri dönüş dönüştürücü tabanlı bir dengeleme şemasıdır ve her hücre için aynı anda şarj veya deşarj sağlayan bir geri dönüş dönüştürücü kullanılır. İlk dengeleme şeması daha ucuzdur ve boyut olarak daha küçüktür, ancak ikinci şema daha hızlı bir dengeleme süreci sunar, daha kompakttır ve hücre sayısını artırmak için uygundur.

Dengeleme kontrol stratejisi (DKS), dengeleme süresi ve kullanılabilir kapasite açısından tanımlanan dengeleme performansı için son derece önemlidir. Kullanılabilir kapasitenin artırılması, dengeli bir pil paketi ile sağlanır. Bu dengelemenin bir an önce tamamlanması önemlidir. BEA'ın doğru akım hızlı şarj (DAHŞ) ekipmanı ile sadece 20 dakika ile 1 saat arasında %80'e kadar şarj edilebileceği düşünüldüğünde, kullanılabilir kapasitenin en üst düzeye çıkarılması için dengeleme işleminin bu zaman aralığından önce tamamlanması gerekir.

Flyback dönüştürücü tabanlı her dengeleme şeması, dengeleme sürecini gerçekleştirmek için farklı bir DKS kullanır. Kontrol stratejileri, dengelemeyi minimum sürede tamamlamak için tasarlanmış bir kontrol algoritması kullanır. Bu algoritmalar girdilerinde kullanılan kontrol değişkenine göre karar verirler. Bu kontrol değişkenleri, hücrenin terminal voltajı veya SOC bilgisi olabilir. SOC bilgisi, bir hücrenin terminal voltajı gibi doğrudan ölçülemez, üst düzey tahmin yöntemleri gibi ileri teknikler kullanılarak ifade edilir. Ancak Li-ion pil hücrelerinin iç durumu hakkında daha doğru bilgi sağladıkları için daha hassas ve güvenilir dengeleme sağlarlar. Aynı kontrol değişkenini kullanan birçok farklı kontrol algoritması vardır. Tek flyback dönüştürücü tabanlı dengeleme şemaları için, herhangi bir matematiksel model veya dengeleme akımı kontrolü kullanmadan, bu hücrelerin şarj veya deşarj sırasını belirleyen algoritmalar üzerinde çalışmalar yapılmıştır. Hücreler, anahtar matrisi aracılığıyla dönüştürücü giriş terminaline bağlanır ve geri dönüş dönüştürücüsünün MOSFET anahtarı, dengeleme süresini en aza indirmek için maksimum dengeleme akımı sağlamak üzere sabit görev döngülü PWM tarafından tetiklenir. Ancak seri bağlı akü paketinde birden fazla dengesiz hücre varsa, tekrarlayan şarj-deşarj döngüleri oluşmaktadır. Bu, özellikle çok sayıda hücreye sahip EA batarya paketlerinde daha uzun dengeleme süresine, daha düşük dengeleme verimliliğine ve pil ömrünün kısalmasına neden olur.

Öte yandan, çoklu flyback dönüştürücülere sahip HPH topolojisi, dengeleme hızı açısından donanımsal avantaja sahiptir. Ancak dengeleme işleminin yüksek dengeleme akımı sağlayan DKS ile kontrol edilmesi, HP topolojisinde belirtildiği gibi ara hücrelerin dengeli bölgeye diğer hücrelerden daha erken ulaşmasına neden olur. Bu hücrelerin kararlı bölgede kalabilmeleri için yüksek akımlarla şarj/deşarj edilmeleri gerekir. Literatürdeki çalışmalarda tekrarlayan şarj-deşarj döngülerini ortadan kaldırmak için her bir hücrenin dengeleme akımlarını tahmin ederek hücrelerin aynı anda dengeli bölgeye gelmesini sağlayan DKS'ler önerilmiştir. Bunlar, anahtarlarda tüketilen enerji miktarı azaltsalar bile, bütün dönüştürücülerin eşzamanlı çalışması yine de yüksek güç kayıplarına neden olmaktadır.

Bu tezde, tek flyback dönüştürücü tabanlı HP ve çoklu flyback dönüştürücü tabanlı HPH bireysel hücre dengeleme topolojilerinde karşılaşılan sorunların üstesinden gelmek için yeni DKS'ler sunulmaktadır. İlk olarak, tekrarlayan şarj/deşarj döngülerini ortadan kaldırarak minimum dengeleme süresini amaçlayan tek flyback dönüştürücü tabanlı HP topolojisi için iki aşamalı bir DKS önerilmiştir. Geliştirilen DKS'nin ilk aşamasında, pil hücrelerinin aynı anda boşalmasını sağlamak için değişken anahtarlama süresi bölme yöntemi geliştirilmiştir. Tekrarlayan döngüleri ortadan kaldırmak için, ikinci aşamada her bir hücrenin deşarj akımını elde eden yeni bir optimizasyon algoritması geliştirilmiştir. Önerilen DKS ve mevcut kural tabanlı DKS için dengeleme süresi ve dengeleme verimliliği açısından kıyaslama gerçekleştirilmiştir. Gerçekleştirilen vaka çalışması, dengeleme hızının büyük ölçüde kısaldığını göstermiştir. İkinci olarak, dengeleme devresindeki genel enerji tüketimini azaltmak ve dengeleme süresini en aza indirmek için çoklu flyback dönüştürücü HPH dengeleme topolojisi için yeni bir DKS geliştirilmiştir. Önerilen strateji, herhangi bir zaman aralığında minimum dengeleme devresini kullanarak ve en düşük SOC'a sahip hücreyi şarj etmeye öncelik vererek bu hedeflere ulaşır.

Önerilen BCS, EA'lar için çok sayıda hücrenin gerekliliği göz önüne alındığında önemli olan kontrol sistemin karmaşıklığını önemli ölçüde azaltmaktadır.

Önerilen iki topoloji ve kontrol stratejisi, MATLAB/Simulink benzetim programı kullanılarak detaylı benzetim çalışmaları ile tasarlanmış ve analiz edilmiştir. Ayrıca HPH topolojisi için geliştirilen batarya dengeleme sistemi deneysel olarak uygulanmıştır. Farklı başlangıç SOC farkları vaka çalışmaları olarak ele alınmış ve deneysel sonuçlarla geliştirilen DKS'nin performansı doğrulanmıştır.

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LIST OF ABBREVIATIONS

BCS : Balancing Control Strategy
BEV : Battery Electric Vehicle
BMS : Battery Management System
CBS : Cell Balancing System
CE : Charge Efficiency
CTC : Cell to Cell
CTP : Cell to Pack
CTPTC : Cell to Pack to Cell
DC : Direct Current
DCM : Discontinuous Conduction Mode
DOD : Depth of Discharge
EV : Electric Vehicle
FLC : Fuzzy Logic Control
GA : Genetic Algorithm
ICB : Individual Cell Balancer
ICE : Internal Combustion Engine
MPC : Model Predictive Control
NN : Neural Network
NNLS : Nonnegative Least Square
OCV : Open Circuit Voltage
PID : Proportional Integral Derivative
PTC : Pack to Cell
PHEV : Plugin Hybrid Electric Vehicle
PWM : Pulse Width Modulation
SC : Switched Capacitor
SMC : Sliding Mode Controller
SOC : State of Charge

1. INTRODUCTION

In this chapter, the research methodology of the thesis is introduced. Initially, the importance of BMS for EV applications is given, and then a brief review of CBSs is presented. Appropriate design considerations of active battery balancing topologies, circuits, and balancing control strategies are expressed in detail. Secondly, detailed information is given about DC-DC converter-based active CBS, and design considerations are handled extensively. The quality of the active CBSs defined in terms of balancing speed and balancing efficiency. At the end of this chapter, the research objectives, the contribution of the thesis, and the organization of the thesis are given.

1.1. Background and Motivation

Electric Vehicles (EVs) have gained significant attention due to the serious consequences of the use of fossil fuels such as gasoline, diesel oil, and LPG in internal combustion engines, which leads to carbon emissions and greenhouse gases. Also, limited sources of fossil fuels and consequently rising crude oil prices make an attractive choice the various EV technologies such as hybrid electric vehicles (HEV), plugin hybrid electric vehicles (PHEV), and pure electric vehicles or battery electric vehicles (BEV) for the automobile industry. Electric car registrations worldwide have exhibited accelerated development, surpassing 6 million units in 2021. Global plug-in (BEV&PHEV) electric car sales and market share for selected regions between 2016 and 2021 are illustrated in Figure 1.1 (IEA,2022).

The widespread use of EVs requires improvements in rechargeable battery technologies. Various types of battery technologies such as lead-acid, nickel-cadmium (Ni-Cd), nickel-metal hydride (Ni-MH), sodium-sulfur (Na-S), lithium-ion (Li-ion) are used in EVs. Specific power and specific energy are important performance parameters that affect the acceleration and driving range of a vehicle, respectively. Apart from these features, safety, lifespan, manufacturing cost, and environmental impact are also considerable criteria. The typical characteristics of batteries are summarized in Table 1.1 (Manzetti and Mariasiu, 2015; Hannan et al., 2017; Liu et al., 2017; Shen et al., 2018). It is seen that the Li-ion battery is a promising energy storage technology that has a higher energy density, specific energy, and specific power characteristics compared to other batteries. In addition, because of having no memory effect, long life cycles, and no toxic materials such as lead or cadmium that will affect the environment, the lithium-based battery is rapidly increasing its market growth. But, the specific energy and terminal voltage of a Li-ion battery cell are not yet sufficient to meet the needs of an EV.

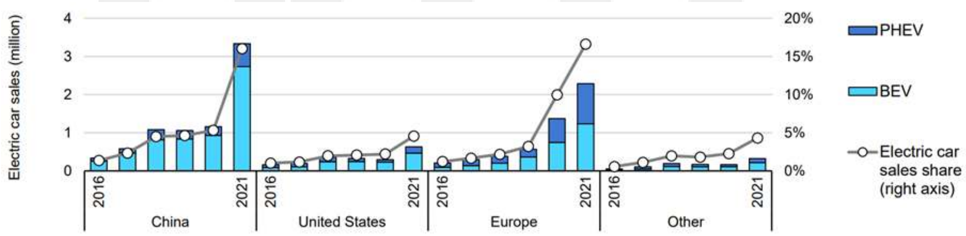


Figure 1.1. Annual sales and market share of EVs worldwide for 2016-2021 (IEA, 2022)

The battery pack in an EV consists of many cells connected in series to meet the high voltage requirements of EVs. However, the inconsistency of the cells resulting from the manufacturing, non-uniform temperature distribution among the cells, and different speeds of degradation of each cell causes voltage and SOC imbalances between the cells. These imbalances become prominent after several charge /discharge cycles and lead to reduce the usable capacity of the battery pack. On the other hand, Li-ion battery cells have more safety precautions than other battery technology as NiMH. Therefore, battery operation must be halted while the lower charged cell reaches the low limit of predefined operational safety region limits, even if the more charged cell still has energy. So, BMS is crucial to allow all cells in the battery pack to operate in favorable conditions, avoid imbalances and ensure the effective pack capacity.

Table 1.1. Typical characteristics of battery technologies

Battery Type	Specific Energy (Wh/kg)	Specific Power (W/kg)	Nominal cell voltage (V)	Operating Temp. (°C)	SD-rate (% loss per month)	Life Cycle (# of cycles)	Merits	Demerits
Lead acid	30-50	150-180	2	-15/50	5%	1200-1800	Low cost, low self-discharge rate	Low specific energy
Ni-Cd	40-55	150-350	1.2	-40/60	20%	1500-3000	Fast charging with minimum stress, long service life	The high cost (10 times of lead-acid), Cd toxicity, Memory effect
Ni-MH	60-100	150-300	1.2	-40/50	30%	500-3000	High specific energy	high self-discharge rate, memory effect
Ni-Zn	60-70	150-300	1.7	-10/50	20%	300-500	No heavy toxic materials, High cell voltage, good temperature range	Short life cycles, High cost
Na-S	100-150	120	2	300/350	0%	2500-4000	Very long cycle life, high energy density, no self-discharge Low material cost	Thermal management issues
Na-NiCl (ZEBRA)	90-120	150	2.6	250/350	0%	2500-3000	Long cycle life, high stored energy, no self-discharge, higher cell voltage than Na-S	Thermal management issues
Li-ion	120-250	500-2000	3.6	-20/60	1-3%	1500-3000	High specific energy, high specific power, low discharge rate, no memory effect High cell voltage	Very high cost, needs protection circuit for overcharge and over-discharge

Simply, a cell balancing system (CBS) is carried out by the BMS to keep the state-of-charge (SOC) or terminal voltage of each cell in the series connected string balanced (i.e., equal). Figure 1.2 illustrates the cell imbalances and cell balancing among the serially connected N-cell. Generally, there are two types of balancing methods dissipative and non-dissipative. In dissipative balancing, also known as passive balancing, the excess energy in the cell with a high charge is converted into heat through the shunt resistance until it is balanced with the cell with a low charge state. This method, although inexpensive and easy to apply, is wasteful of energy. The non-dissipative method, also known as active cell balancing

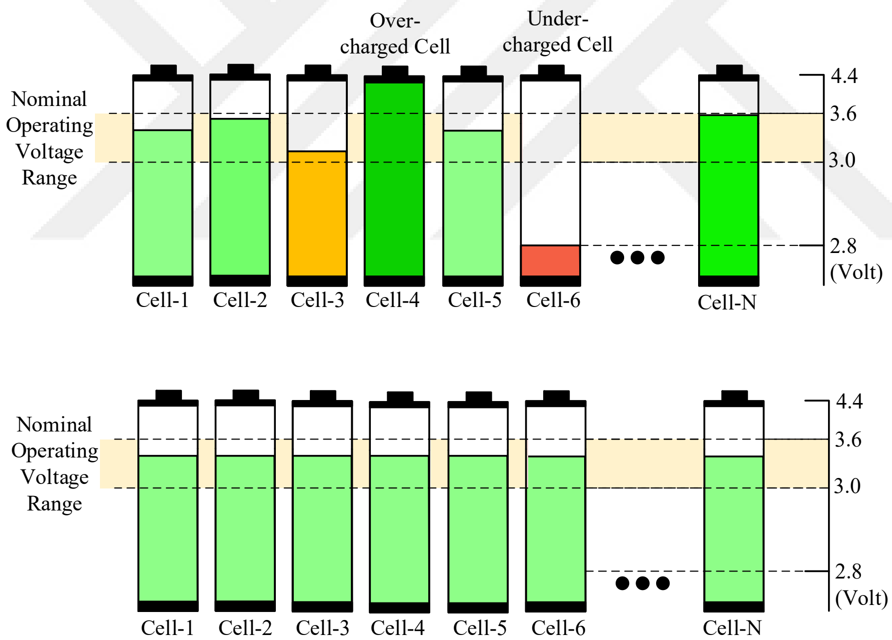


Figure 1.2. Cell imbalances among the N-cells. b) Cell balancing of a battery pack.

is based on the principle of redistributing the excess energy in the strong cell to weak ones through power electronics. Active balancing methods provide utilization of all stored energy in the battery pack. Active battery balancing is performed with four basic topological approaches: CTC, CTP, PTC, and CTPTC. The CTC approach transfers the excessive energy of any strong cell to an adjacent weak cell or another cell directly. In CTP balancing topologies, the excess energy is drawn from the highly charged cell and redistributed to the pack. Conversely, the PTC approach transfers the excess energy from the pack to the weak cells. By combining the CTP and PTC, it is possible to transfer the energy bidirectional as called CTPTC balancing topology.

There are a number of researches on balancing circuits for the active CBS. The energy to be transferred is temporarily stored in a capacitor or inductor. Balancing circuits are primarily categorized into two ways. The first class is switched capacitor and switched inductor (or multi-winding transformer). These are easy to control and design. However, in single capacitor/inductor configurations, only one cell can transfer the energy at any time, which causes a long balancing time. On the other hand, multiple configurations of them are restricted in many ways. While the number of winding that is dependent on the magnetic core limits in the practical application of the inductive method is a challenge, the small voltage difference still is a functional problem for a multi-capacitor balancing circuit. The second class is DC-DC converter-based balancing circuits. The DC-DC converter-based active balancing circuit can overcome the concerns that the aforementioned circuits face. It is a more advanced balancing circuit configuration that provides excellent controllability of each cell or battery module thanks to its modular designs. Furthermore, DC-DC converter-based balancing circuits can achieve CTP, PTC, and CTPTC balancing approaches. So, the high balancing current due to the high voltage difference between the pack and the cell ensures a high balancing speed (Baronti et al., 2014; Gallardo-Lozano et al., 2014; Caspar et al., 2016; Carter et al., 2020).

The balancing control strategy (BCS) is the other significant part of CBS besides the hardware design. Different types of BCS can be used by each balancing technique to regulate the cell currents for individual cells. A control strategy makes decisions according to the input control variable that describes each cell's energy (charge amount). Control variables generally are terminal voltage and SOC. Terminal voltage is easy to measure; however, it does not give accurate information about the releasable capacity of the battery in a flat area of the OCV-SOC curve of the Li-ion cell. Because the terminal voltage of a cell barely changing in the flat area corresponds to more than 10% SOC differentiation. SOC is needed an advanced estimation algorithm, but it ensures a more precise balancing process.

After the control variable monitoring, the BCS is responsible for selecting the discharged cell and keeping the balancing current at the highest possible value within certain limits in line with an objective. Maximum allowable balancing current is directly related to balancing topology, balancer circuit, and control decisions. While BCSs are developed, balancing time and balancing efficiency, have always been handled as performance indicators. Control strategies can be categorized into two main groups: control algorithm-based balancing strategies and rule-based balancing strategies. First, control algorithm-based strategies include modern control algorithms such as optimal control (OC), model predictive control (MPC), sliding mode control (SMC), and intelligent control algorithms such as fuzzy logic control(FLC), neural network (NN)-based algorithm, genetic algorithm (GA). Secondly, rule-based balancing strategies are relatively simple and easy to implement, including types such as mean algorithm, difference algorithm, mean-difference algorithm, and maximum-minimum algorithm (Feng et al., 2019; Turksoy et al.,2020).

CBS is a significant and mandatory part of the BMS, increasing the usable capacity of the battery pack for the extended range of the EV, ensuring the long cycle life of the battery cells, and preventing the battery from malfunctions. However, low-cost cell balancing topology and its balancer circuit, modular balancing topology design of the high amount of cells, and a fast and efficient balancing process in all charge/discharge/standby states are still being studied in detail. To alleviate these shortcomings, many circuit topologies with suitable control techniques are highlighted in the literature. To ensure high balancing speed, modular design, and low cost, the investigations focus on CTP, PTC, and CTPTC topologies. Also, from the standpoint of ensuring increased balancing efficiency, various DC-DC converter topologies are introduced to the BCS potential of CBS. Furthermore, different control strategies are developed to improve efficiency, overcome the limited functions for balancing requirements, and reduce the complexity of the control structure.

1.2. Research Objectives

The limited capacity of battery pack consisting of Li-ion battery cells is still an issue that needs to be resolved in EVs. Thus, EVs need to enhance efficient and reliable BMS. Usable capacity in a battery pack limited by cell with the lowest charge capacity. Active cell balancing, which transfers the energy between the more charged and lower charged cells, is the most efficient method to increase the usable capacity. However, the design of the balancing topology and balancing control strategy, which will quickly realize efficient charge transfer among cells, remains challenging. The fast balancing control is essential in increasing the range of EVs in case of discharge and reaching the cells to maximum energy in case of fast charging. In addition, the highly efficient balancing system design is vital to minimize charge loss of the battery pack.

The objectives of the presented research have been prepared to overcome the shortcomings mentioned above.

The objectives of the thesis are given as follows:

- It is aimed to examine the SOC estimation techniques in terms of accuracy, adaptability, and complexity.
- Active cell balancing power topologies and their control structures will be

examined profoundly, proposing the circuit topology with the best result.

- It aims to comprehensively compare the proposed and existing balancing control strategy for commonly used balancing topology in terms of the control variable, convergence speed, and complexity level financial outgoings.
- Proposing a novel balancing control strategy to attain a fast balancing process.
- It is aimed to provide a detailed design procedure for proposed designs and their controllers with theoretical analysis and simulation case studies.

1.3. Contribution of Thesis

The main contributions of this thesis are given as follows:

- A novel BCS is developed to minimize the balancing time in CTP active balancing topology. With the proposed control strategy, balancing time is reduced 56 %, shorter than the conventional balancing algorithm.
- A novel BCS is developed for CTPTC active balancing topology to maximize the balancing efficiency and reduce balancing time.
- A detailed comparison study is presented between the proposed CBS and the existing CBS regarding efficiency, cost, and advantages.
- A detailed design approach based on theoretical analysis and simulation studies for CBS is presented.
- The improved CTPTC-based active cell balancing control system is experimentally implemented.

1.4. The Organization of the Thesis

The organization of the thesis is as follows:

Chapter 1: Introduction

The importance and need of active CBS, the most important part of EVs, has been introduced and motivation has been provided for this thesis. Also, the research objectives, the contribution of the thesis, and the organization of the thesis are given.

Chapter 2: State-Of-The-Art Cell Balancing Methods

In this chapter, the state-of-the-art active CBS topologies and control strategies are investigated in detail by providing a summary of related literature.

Chapter 3: Overview of Battery Cell Modelling and SOC Estimation

In this chapter, the battery cell modeling and SOC estimation techniques in the literature are explained rigorously. Kalman Filter-based SOC estimation method and 2^{nd} order Thevenin equivalent cell model are described in detail.

Chapter 4: Design and Analysis of Proposed CTP Active CBS

In this chapter, an analysis of the proposed CBS to reduce balancing time and increase the balancing efficiency of the CTP balancing topology is presented by providing information about the utilized balancing topology, balancer circuit, and its operating principles. Furthermore, the design procedure of the entire circuit is provided rigorously. Finally, the performance of the developed BCS has been tested with various case studies in Matlab/Simulink simulation environment.

Chapter 5: Design and Implementation of Proposed CTPTC Active CBS

In this chapter, the design and implementation of the proposed CTPTC active CBS are presented by providing information about the utilized balancing topology, balancing circuit, and BCS. The design considerations of the entire balancing circuit and proposed BCS are provided rigorously. Furthermore, the experimental design procedure and PCB design of the whole balancing circuit and

PCB design are explained in detail. Developed CBS verified by simulations and experimental results.

Chapter 6: Conclusion and Future work

Concluding remarks and main contributions of the thesis are given in this chapter. Also, the future perspectives of the thesis work are discussed.
The organization of the thesis is illustrated in Figure 1.3.

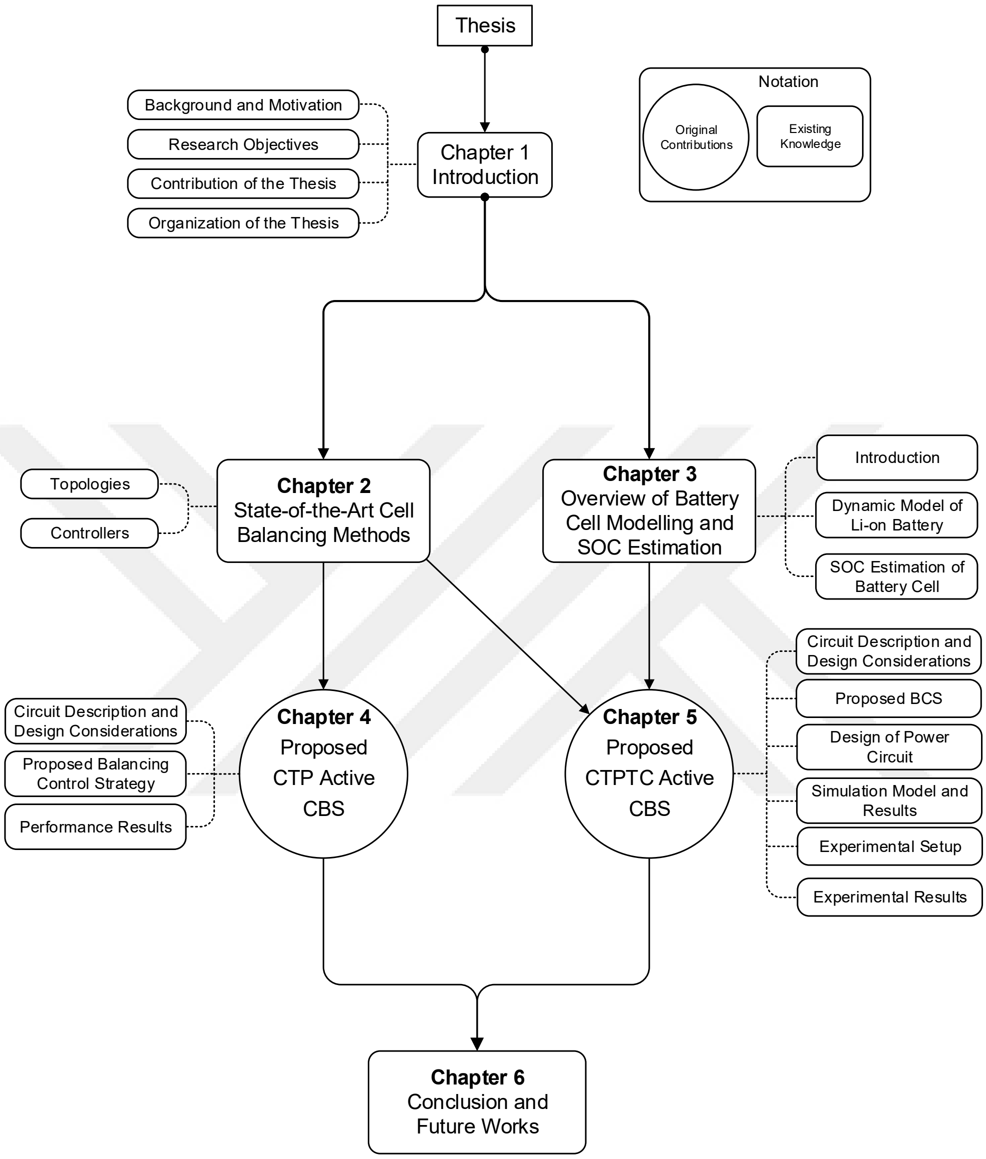


Figure 1.3. The organization of the thesis

1.5. Summary

Firstly, the background and motivation of the thesis are provided in this chapter. Then, based on this information, the research objectives of the thesis are determined, and all the contributions of the thesis are presented. Finally, the organization of the thesis has been given.

2. STATE-OF-THE-ART CELL BALANCING METHODS

In this section, an overview of the cell balancing system by providing a summary of related literature is presented in detail. In addition, detailed explanations of balancing configurations and control strategies are given.

2.1. Passive Cell Balancing

In the passive balancing method, the excess energy in the cell in a high-charge state is converted into heat through the parallel shunt resistance until it is equalized with the cell in a low-charge state. The logic of this balancing is that the cells with higher voltage will discharge with a higher current than the cell with lower voltages. Mainly, passive balancing topologies can be classified as fixed shunt resistors and switched shunt resistors. The fixed shunting resistor topology, as shown in Figure 2.1 (a), enables the current to be bypassed through the resistor to limit the voltages of each cell in the battery pack. On the other hand, as shown in Figure 2.1 (b), in the switched shunting resistor topology, the way the current is bypassed is controlled by switches connected to each resistor in series.

Passive cell balancing is a simple and easy-to-apply method; however, energy recovery does not exist due to it being wasted as heat through the resistive element. In addition, low balancing speed and thermal problems make it an ineffective balancing method.

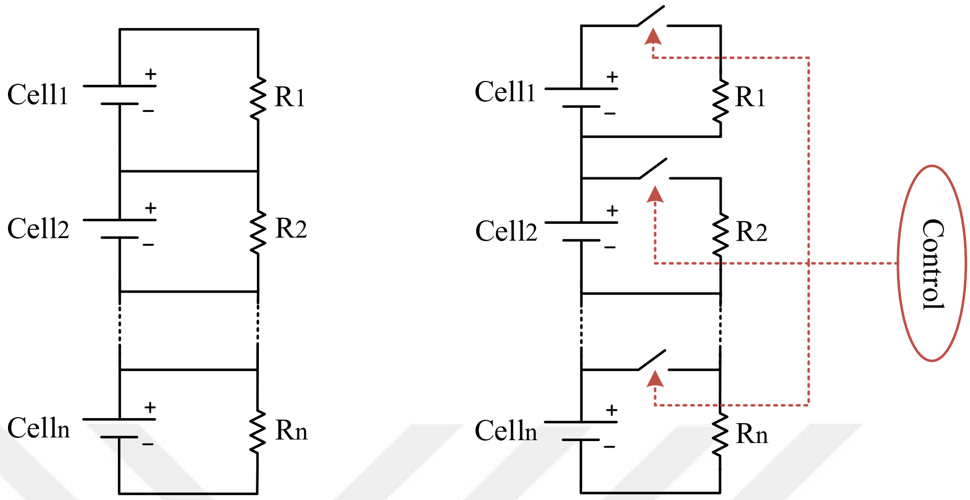


Figure 2.1. Passive balancing topologies (a) Fixed shunting resistor topology (b) switched shunting resistor topology.

2.2. Active Cell Balancing

The general idea behind active balancing is transferring the excess energy among the cells through an external circuit or energy storage devices such as a capacitor and inductor. Two major active balancing topologies are capacitor/inductor shuttling and DC-DC converter-based balancing topologies.

2.2.1. Capacitor/Inductor Based Balancing Topologies

This balancing topology uses the capacitor or inductor as an external storage device and shuttles the energy among cells. The main capacitor-based cell balancing topologies are single-switched capacitors, multiple-switched capacitors, and double-tiered switched capacitors, as illustrated in Figure 2.2. The switching principle of the multiple-switched capacitor (SC) consists of two straightforward states. In the first state, the odd-numbered switches are turned on, and the voltages of the same numbered cell ($Cell_1$) and capacitor (C_1) have become the same. In the second state, the same capacitor (C_1) is connected in parallel with the adjacent cell

(Cell$_2$) with the turn-on of even-numbered switches, and this operation continues until the voltages of all cells are balanced (Baughman and Ferdowsi, 2008; Daowd et al., 2013).

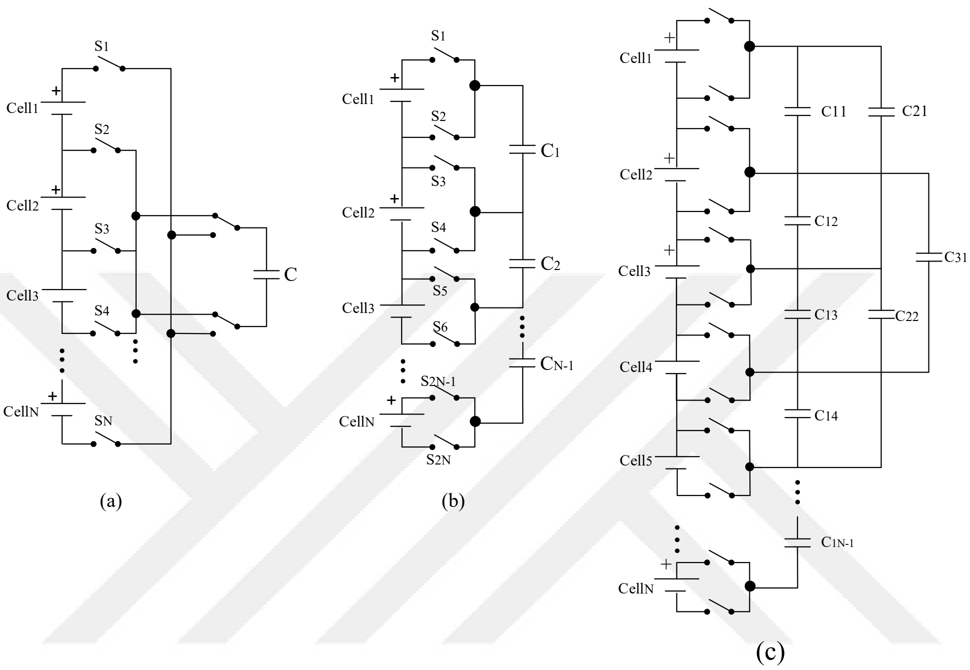


Figure 2.2. Capacitor-based active balancing topology (a) single switched capacitor (b)multiple switched capacitor (c) double-tiered switched capacitor

In a single SC, topology cells are balanced with similar logic, but only one capacitor is used. As a result, the number of circuit components is considerably reduced, but the balancing time is longer than the multiple SC topology. The double-tired SC is a pseudonym of SC topology that uses a second capacitor tier to reduce the balancing time (Singirikonda and Obulesu, 2021). However, the number of capacitors increases according to the other SC derivations.

The operating principle of the single switched inductor is similar to the single SC, the only difference being that the inductor is used as an energy storage element. Although all shuttling balancing topologies are easy to control and design, they have the disadvantages of having many switching elements and low balancing speeds.

2.2.2. DC-DC Converter-Based Balancing Topologies

The DC-DC converter is a way that provides controlling and converting the DC voltage level to another level. A DC-DC converter ensures power transfer between the discharged cell(s) and charged cell(s) or battery pack in a CBS. While selecting appropriate DC-DC converter circuits, capabilities such as the number of circuit components, galvanic isolation, power rating, energy conversion efficiency, and voltage conversion ratio must be considered. The number of circuit components significantly affects the complexity of the balancing system, and it straight influences the cost and size. The conversion efficiency will directly contribute to balancing efficiency. With this background, an overview of DC-DC converters commonly utilized in cell balancing applications is carried out by summarizing their operating principle and design properties.

2.2.2.1. Bidirectional Buck-Boost Converter

A bidirectional buck-boost converter-based balancing circuit consists of an inductor and two power MOSFETs with body diodes, as shown in Figure 2.3. In the balancing operation, this converter is operated in buck mode. The switch of the high-charged cell ($Cell_i$) is closed, and the energy is stored in the inductor, as shown in Figure 2.3 (b). The voltage across the inductor becomes the voltage of $Cell_i$. The voltage across the inductor is

$$V_L = V_{cell_i} = L\frac{di_L}{dt} \tag{2.1}$$

The rate of change of the inductor current is constant and the preceding equation is expressed as

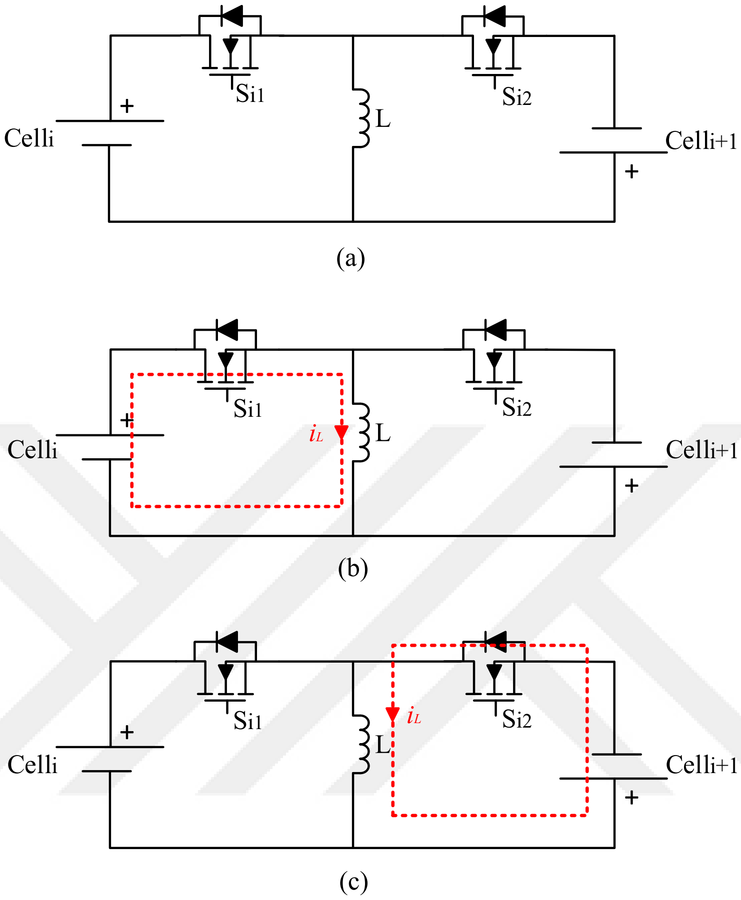


Figure 2.3. Basic schematic diagram bidirectional buck-boost converter

$$\frac{\Delta i_L}{\Delta t} = \frac{V_{cell_i}}{L} = \frac{\Delta i_L}{DT} \tag{2.2}$$

where D is the duty cycle of the PWM signal, and T is the period of the switching signal. When the related switch (S_{i1}) is closed, the change of inductor current is

$$\left(\Delta i_L\right)_{closed} = \frac{V_{cell_1} DT}{L} \tag{2.3}$$

This switch is open, and the energy on the inductor is transferred to the low voltage cell ($Cell_2$) via the body diode of MOSFET of the $Cell_2$, as shown in Figure 2.3 (b). The voltage across the inductor is

$$V_L = V_{cell_{i+1}} = L\frac{di_L}{dt} \tag{2.4}$$

And the change in the inductor current is as follows:

$$\left(\Delta i_L\right)_{open} = \frac{V_{cell_{i+1}}\left(1-D\right)T}{L} \tag{2.5}$$

For steady-state operation, the net change in inductor current must be zero over one period.

$$\left(\Delta i_L\right)_{closed} + \left(\Delta i_L\right)_{open} = 0 \tag{2.6}$$

$$\frac{V_{cell_i}DT}{L} = \frac{V_{cell_{i+1}}\left(1-D\right)T}{L} \tag{2.7}$$

The voltage conversion ratio of the buck-boost converter is expressed as follow:

$$\frac{V_{cell_{i+1}}}{V_{cell_1}} = \frac{D}{\left(1-D\right)} \tag{2.8}$$

A bidirectional buck-boost converter is one of the most common converter types used in adjacent CTC balancing topology (Ma et al.,2018; Liao and Chen, 2022). For example, N-1 buck-boost converters are used for N battery cells, as illustrated in Figure 2.4. The power rating of the buck-boost converters is low because the maximum value of terminal voltage can be the maximum cell voltage. So, the power loss of the balancer circuit is lower than the other active balancing circuits. However, buck-boost converter-based adjacent CTC balancing topology completes the balancing process for a long time, especially in case of large imbalances and the increasing number of cells (Wang et al., 2022).

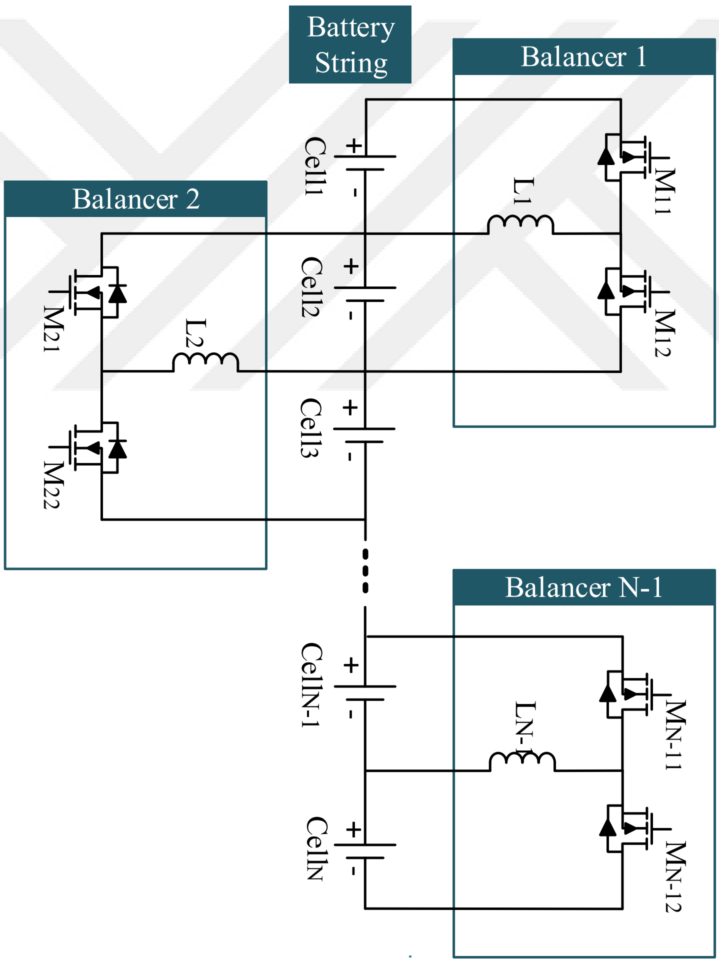


Figure 2.4. Bidirectional buck-boost converter-based adjacent CTC balancing topology

2.2.2.2. Bidirectional Cuk Converter

A bidirectional Cuk converter circuit consists of two inductors, an energy transferring capacitor, and two power MOSFETs with body diodes, as shown in Figure 2.5. Unlike the buck-boost converter, where the inductor is responsible for energy transfer, the capacitor provides the energy transfer for the Cuk converter. For achieving cell balancing, PWM signals which control the MOSFETs' being on and off time, drive the converter circuit.

Assuming charge transfer i-th cell to (i+1)-th cell, in this case, $Cell_i$ is the high-charged (high voltage) cell and will be discharged. In the initial condition, inductor currents are zero, and the capacitor voltage equals the ($Vcell_i$+$Vcell_{(i+1)}$). S_{i1} is closed, and the inductor L_{i1} stores the energy from $Cell_i$ during the turn-on time of S_{i1}. The capacitor discharges the L_{i2} and $Cell_{(i+1)}$, and L_{i2} stores the energy, as shown in Figure 2.5 (b).

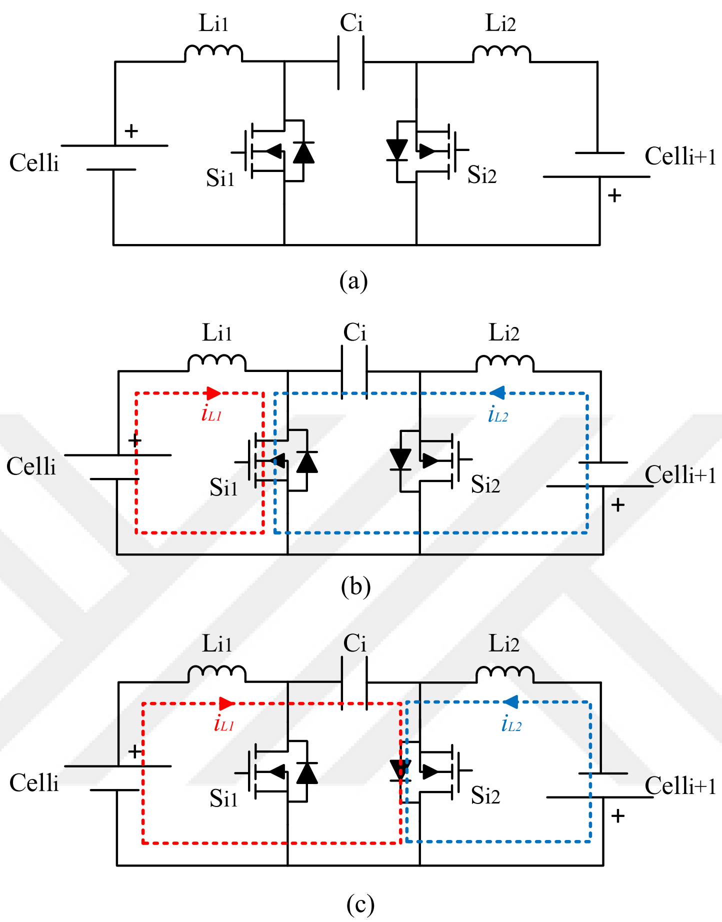


Figure 2.5. Basic circuit diagram bidirectional Cuk converter

The Capacitor current with the switch closed is

$$(i_C)_{closed} = -I_{Li2} \tag{2.9}$$

The voltage across L_{i1} and L_{i2} are

$$V_{Li1} = V_{celli} = L_{i1}\frac{di_{Li1}}{dt} \tag{2.10}$$

$$V_{Li2} = V_{celli} = L_{i2} \frac{di_{Li2}}{dt} \qquad (2.11)$$

With the switch on for time DT, the change in inductor current of L_{i1} and L_{i2} are

$$\Delta i_{Li1} = \frac{V_{cell_i} DT}{L_{i1}} \qquad (2.12)$$

$$\Delta i_{Li2} = \frac{V_{cell_i} DT}{L_{i2}} \qquad (2.13)$$

Minimum inductor sizes for continuous current are

$$L_{i1} \geq \frac{V_{cell_i} DT}{\Delta L_{i1}} \qquad (2.14)$$

$$L_{i2} \geq \frac{V_{cell_i} DT}{\Delta L_{i2}} \qquad (2.15)$$

In the second state, as shown in Figure 2.5 (c), S_{i1} turns off, the body diode of S_{i2} turns on, the capacitor is charged by L_{i1}, and stored energy in L_{i2} continues to charge $Cell_{(i+1)}$. The Capacitor current in the second state is

$$(i_c)_{open} = I_{Li1} \qquad (2.16)$$

For one switching period average capacitor current is zero. With the switch on for time DT and off for (1-D)T.

$$(i_C)_{closed} DT + (i_C)_{open}(1-D)T = 0 \tag{2.17}$$

The power absorbed by the $Cell_{i+1}$ is equal to the power supplied by the $Cell_i$

$$-V_{cell_{i+1}} I_{Li2} = V_{cell_i} I_{Li1} \tag{2.18}$$

Combining Eqs. (2.17) and (2.17), the voltage conversion ratio of the Cuk converter is expressed as

$$\frac{V_{cell_{i+1}}}{V_{cell_i}} = -\frac{D}{(1-D)} \tag{2.19}$$

The balancing logic of the Cuk converter-based balancing topology is in the same manner as the buck-boost topology. Also, the bidirectional Cuk converter is one of the most common converter types used in adjacent CTC balancing topology (Ouyang et al.,2017; Zheng et al.,2018). For example, N-1 Cuk converters are used for N battery cells, as illustrated in Figure 2.6. The power rating of the Cuk converters is low because the maximum value of terminal voltage can be the maximum cell voltage. So, the power loss of the balancer circuit is lower than the other active balancing circuits. However, Cuk converter-based adjacent CTC balancing topology completes the balancing process for a long time, especially in case of large imbalances and the increasing number of cells (Wang et al., 2022).

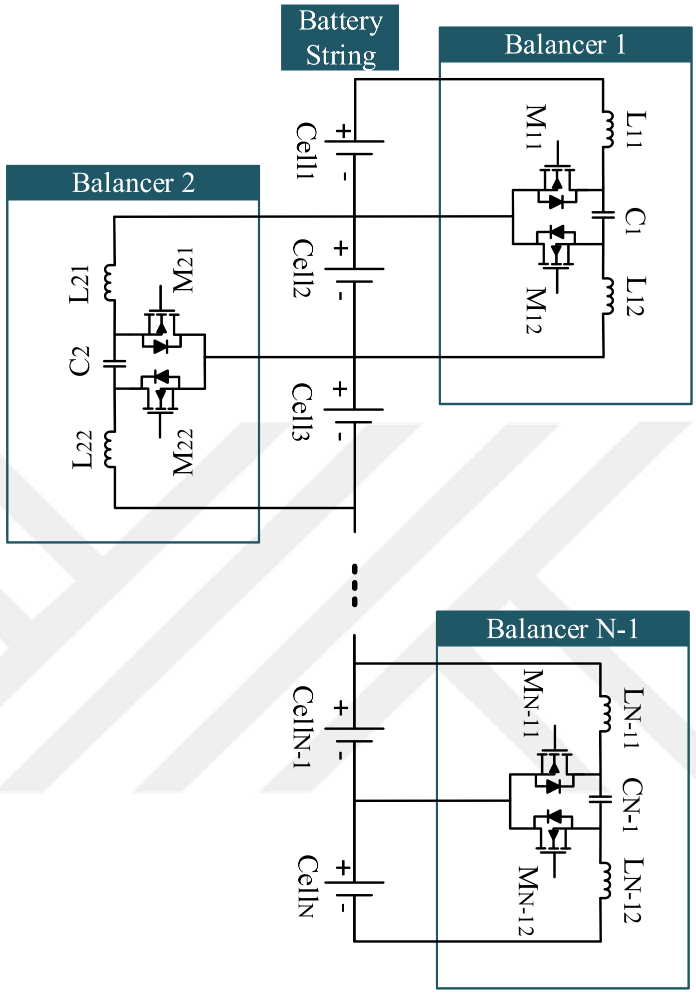


Figure 2.6. Bidirectional Cuk converter-based adjacent CTC balancing topology

2.2.2.3. Flyback Converter

The flyback converter is the most commonly utilized converter type for a cell balancing system. This converter is a derivation of the buck-boost converter. The only difference between them, the energy storage element is the magnetization inductance of the transformer in a flyback converter. The presence of the transformer increases voltage gain compared to the buck-boost type. The flyback converter is used for CTP and PTC balancing topology. Also, the bidirectional structure of the flyback converter is utilized to simultaneously charge and discharge individual cells by integrating CTP with PTC. Flyback converter has a low number of components which consists of a transformer and a switch for unidirectional structure or two switches for bidirectional configuration.

The basic operating principle of the flyback converter consists of two main states, illustrated in Figure 2.7. In the first state, the switch is closed, and the diode on the secondary side is reverse-biased because of winding polarities and $V_{celli}=V_1$. Energy is stored in the magnetization inductance of the transformer during the on-time of the MOSFET, as shown in Figure 2.7 (b). Current through the source (cell) is equal to the current of the magnetization inductance L_M.

Current in the magnetization inductance is

$$V_{cell_i} = V_1 = L_m \frac{di_{L_M}}{dt} \tag{2.20}$$

$$(\Delta i_{L_M})_{closed} = \frac{V_{celli}}{L_m} DT \tag{2.21}$$

where L_m is the magnetization inductance, D is the maximum duty cycle, and T is the switching period.

In the second state, the switch is open, the stored energy is transferred to the secondary side, and the output (pack) is fedded because the diode is forward-biasing. The transformer secondary voltage V_2 becomes $-V_{pack}$. The voltage across Lm is as follows:

$$V_1 = -V_{pack}\left(\frac{N_1}{N_2}\right) \tag{2.22}$$

where the (N_1/N_2) is the turn ratio of the transformer.

Voltage and current are as follows:

$$V_1 = V_{cell_i} = L_m \frac{di_{L_M}}{dt} = -V_{pack}\left(\frac{N_1}{N_2}\right) \tag{2.23}$$

$$(\Delta i_{L_M})_{open} = \frac{-V_{pack}}{L_m}(1-D)T\left(\frac{N_1}{N_2}\right) \tag{2.24}$$

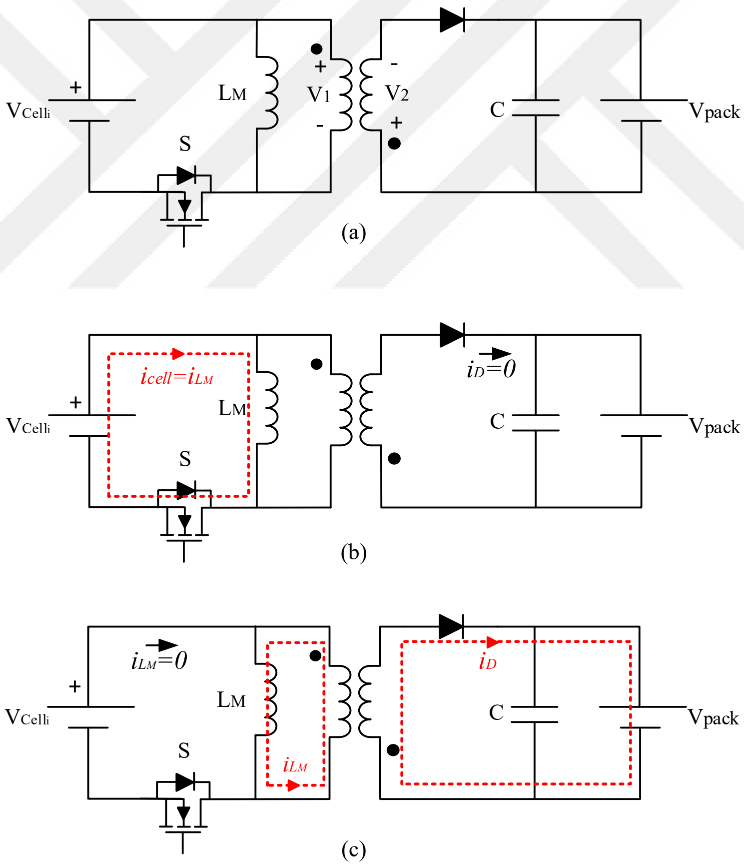


Figure 2.7. Basic circuit diagram flyback converter

For the steady-state operation, the total change in inductor current must be zero over one period.

$$\left(\Delta i_{L_M}\right)_{closed} + \left(\Delta i_{L_M}\right)_{open} = 0 \tag{2.25}$$

$$\frac{V_{cell_i} DT}{L_M} = \frac{V_{pack}\left(1-D\right)T}{L_M}\left(\frac{N_1}{N_2}\right) \tag{2.26}$$

The voltage conversion ratio of the flyback converter is expressed as

$$\frac{V_{pack}}{V_{cell_i}} = \frac{D}{\left(1-D\right)}\left(\frac{N_2}{N_1}\right) \tag{2.27}$$

To reduce transformer size and system cost and increase efficiency, the flyback converter is operated in Discontinuous Conduction Mode (DCM). For the DCM for the flyback converter, the current in the transformer increases linearly when the switch is closed. However, when the switch is open, the current of the inductor current decreases to zero until the next switching cycle (Hart, 2011). The magnetization current, primary current, and secondary current waveforms for DCM operation are given in Figure 2.8.

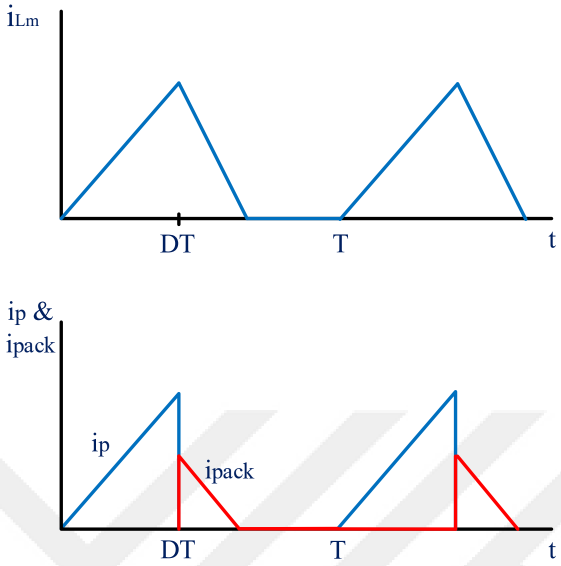


Figure 2.8. The magnetization current, primary current, and secondary current waveforms for DCM operation

The average cell current during one switching period is as follows:

$$I_{cell} = \frac{1}{2}\frac{V_{celli}}{L_m}D^2T \tag{2.28}$$

Power supply by input is equal to the output power in ideal condition

$$I_{cell}V_{cell} = P_{out} \tag{2.29}$$

$$\frac{V_{cell}{}^2 D^2 T}{2L_M f} = P_{out} \tag{2.30}$$

And the minimum value of the L_M in DCM is calculated as follows:

$$L_M = \frac{V_{cell}{}^2 D^2 T}{2P_{out}} \tag{2.31}$$

The turn ratio of the transformer is calculated as given below.

$$n = \frac{N_2}{N_1} = \frac{V_{pack}(1 - D - D_{dw})}{V_{cell_i} D} \tag{2.32}$$

Where D_{dw} duty ratio of the dwell time. The switch and the secondary side diode are turned off during the dwell time.

Many cell balancing topologies using the flyback converter circuit are designed. Flyback converter-based topologies are evaluated into two main categories. First of all, CTP or PTC topologies provide the energy flow of a single converter with a switch matrix between cell and pack, as illustrated in Figure 2.8 (a). In balancing topologies with single flyback converters, only one cell can be charged or discharged at any time. In the second category, simultaneous charge and discharge of individual cells are possible through the multiple flyback converter-based CTPTC topology, as illustrated in Figure 2.8 (b). Here, the converter can be a unidirectional or bidirectional structure. A unidirectional flyback converter makes it possible to discharge high-energy cells to the pack by providing only CTP charge flow or to charge low-energy cells from the pack by delivering only PTC charge flow. On the other hand, the bidirectional flyback converter makes it possible for any cell to be discharged or charged.

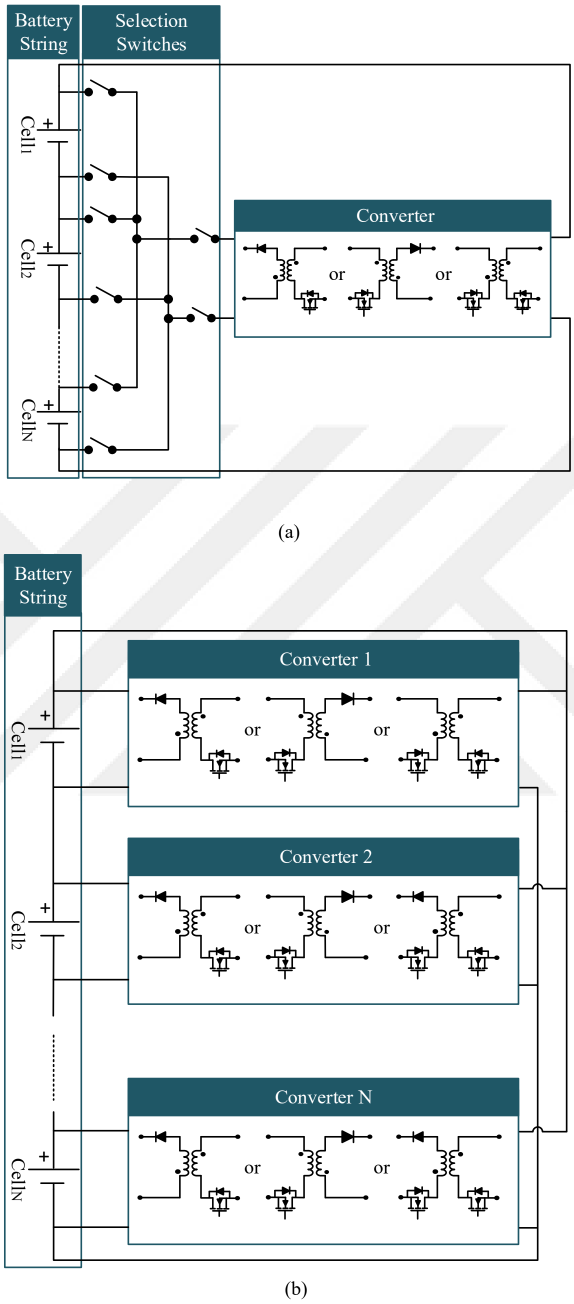


Figure 2.9. Flyback converter-based CTP/PTC balancing topologies (a) single flyback converter-based balancing (b) multiple transformer-based balancing

2.2.2.4. Dual Active Bridge Converter

The dual active bridge (DAB) converter is an isolated converter type that has a bidirectional power transfer capability. The considerable advantage of the DAB converter is that it has a higher voltage range and power capacity, according to the counterpart isolated converters (Karshenas et al.,2011; Zhifu et al., 2017). DAB converter consists of a transformer with high leakage inductance and two H-bridges, including four switches on both sides of the transformer. The energy is instantaneously stored in the leakage inductance of the transformer.

DAB converters can be utilized in cell balancing hardware, especially in case of the number of series-connected cells increases (Sun et al., 2015; Karthikeyan and Gupta, 2017). DAB converter-based CTP-PTC balancing topology is demonstrated in Figure 2.10. It is operated in boost mode when energy is transferred to the CTP and in buck mode when energy is transferred to the PTC. Corresponding equations for the voltage gain ratio in buck and boost mode are given as follows:

$$V_{pack} = \frac{N_2}{2N_1(1-D_1)} V_{cell} \tag{2.33}$$

$$V_{cell} = 2\frac{N_1}{N_2} D_2 V_{pack} \tag{2.34}$$

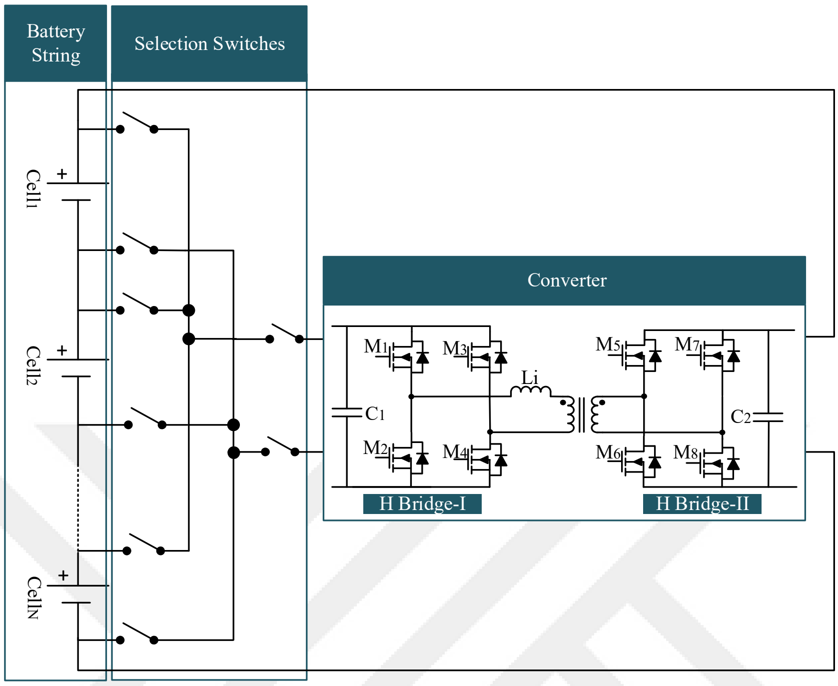


Figure 2.10. DAB converter-based cell CTP/PTC balancing topologies

2.3. Balancing Control Strategy of Active Balancing

The balancing control strategy (BCS) controls the balancing circuit by a specific algorithm to meet the expectations of CBS. BCS is responsible for selecting the cell(s) to be discharged or charged and adjusting the balancing current of the selected cell(s) by a PWM signal. It is the current that passes through the energy storage element in a balancing circuit. The high balancing current increases the balancing speed and minimizes the balancing time. However, the maximum balancing current brings the intermediate cells to the acceptable SOC range before the higher and lower SOC cells. To keep the intermediate cells in an acceptable SOC range, they are exposed to repeated charge/discharge cycles with the maximum current. These repeated cycles cause to decrease in the balancing efficiency because of energy losses on the switches. Further, the life cycle is affected by this significantly.

Balancing speed and balancing efficiency have always been handled as two significant objectives when designing control strategies. BCS mainly consists of two control parts. The high-level control algorithm computes the allowable maximum balancing current of the cell(s) according to the dynamic behavior of the battery cell and balancing topology. The main objective of the high-level control algorithms is to ensure balancing time minimization and minimum energy loss according to the maximum balancing current and charge/discharge current of the entire battery pack. The low-level controller provides tracking of the current based on the circuit parameters (inductor, capacitor, resistance) and signal parameters (switching frequency). Then it generates the PWM signal to keep the balancing current at the desired level. This section explains commonly utilized control algorithms in balancing strategies in detail.

2.3.1. Rule-based Balancing Control Strategy

Rule-based control strategies use a set of rules to eliminate the initial SOC imbalance of the battery system. They are relatively simple, easy implementation and have high data accuracy.

Rule-based (RB) algorithm uses the average of balancing variables of all the cells in a battery pack as the reference object, computes the difference of each battery's SOC or voltage to the average, and then charges low-charged cell(s) or discharges high charged cell(s). The RB algorithm is based on the logic of determining the degree of imbalance of each cell. Then, the balancing scenario and balancing currents of the cells are determined according to the balancing ability of the topology (Feng et al., 2019; Turksoy et al.,2020). The PWM signal with the fixed duty cycle adjusts the balancing current to its maximum value. RB algorithms have been widely adopted in balancing control strategies. Wang et al. proposed a mean-difference algorithm for single bidirectional flyback converter-based balancing topology. The proposed algorithm has allowed energy to be transferred from the pack to cells with a lower SOC than the average SOC. The second step of the algorithm has completed the balancing process by ensuring that the cells above the average SOC have transferred their energy to the pack. Charging and discharging operations were carried out from the cells with the maximum difference from the average SOC to the cells with the minimum. (Wang et al., 2015). Hoque et al. developed a balancing circuit using two unidirectional flyback converters, one for PTC and the other for CTP. The terminal voltage of the randomly selected cell, which is out of the balanced range, has been discharged and charged if it is above or below the average voltage value of the pack, respectively (Hoque et al., 2016). The RB balancing algorithm easily implemented a control strategy; however, it suffers from overbalancing and repeated balancing that cause increased energy consumption and balancing time.

2.3.2. Control Algorithm-Based Balancing Control Strategy

Control algorithm-based balancing control strategies utilize a control technique to eliminate imbalances among a series of connected cells. It is more complex and needs a description of the battery and balancer circuit models. The main goal of this high-level control algorithm is to define the charge/discharge currents (balancing current) of each cell which brings all cells to the balanced region in line with the balancing objective. All balancing control algorithms have an objective function, such as balancing time minimization, energy consumption minimization, or capacity maximization. The defined currents are then tracked by a low-level control algorithm that calculates the duty cycle of the PWM signal. In this section, various control algorithms used for cell balancing control are examined in detail.

2.3.2.1. Model Predictive Control Algorithm

Model Predictive Control (MPC) is a feedback control algorithm that needs a mathematical model of the system to make predictions about the future outputs of the system to be controlled. The simple representation of MPC is shown in Figure

2.10. Prediction is based on a system model over a finite time interval called the forecast horizon. The solution to the optimization problem creates the control vector, in which the first element of the optimal array is injected into the system. Then, the problem is solved again for the next time interval using the updated system information. Using the process model, MPC obtains the control signal that minimizes a specified objective function (Qin and Badgwell, 2003; Beccuti et al., 2007). During this optimization, constraints can be placed on system outputs and/or control movements throughout the prediction horizon for system stability (Richards and How, 2006).

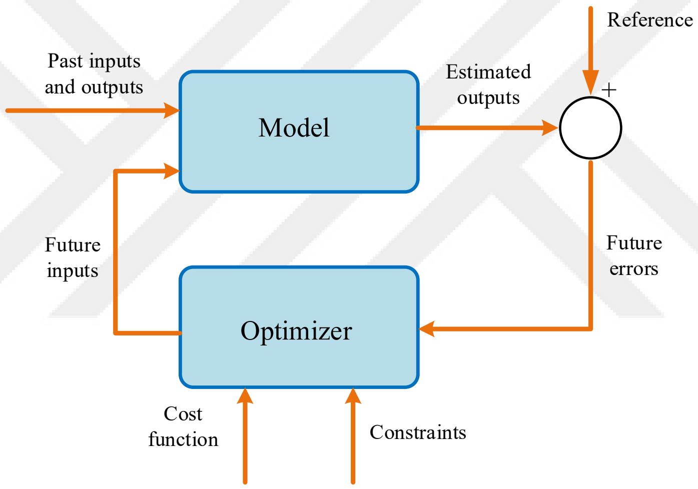


Figure 2.11. Schematic representation of MPC algorithm

In cell balancing systems, MPC estimated the balancing current of each cell by taking the minimum balancing time as an objective function. Energy efficiency is also improved with the MPC algorithm-based balancing strategies that avoid repeated balancing during the balancing period. However, modeling a battery cell with different charge and discharge characteristics and integrating the efficiency of the balancing circuit into the model of the entire balancing system is a very complex process. Repeated equalization will definitely occur if the charge/discharge efficiency of cell and topology efficiency are neglected.

2.3.2.2. Fuzzy Logic Control Algorithm

The fuzzy logic controller (FLC) control is a good candidate for controlling challenging and complex systems to describe mathematical models. The FLC comprises the fuzzifier, inference engine, rule base, and defuzzifier, as shown in Fig. 17. The process of turning system input data into symbolic values, which are linguistic qualifiers, is known as the fuzzifier process. Rule base characterizes the control rules which define the connections between the input and output based on the information about the system. Finally, the defuzzifier creates the actual values after the inference engine unit has operated the fuzzy values with fuzzy rules (Yilmaz et al.,2019).

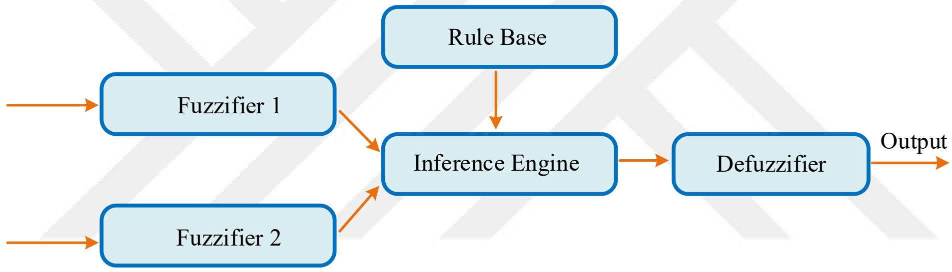


Figure 2.12. Schematic representation of FLC

Researchers utilized FLC for the ICB topologies such as adjacent CTC and the multiple flyback converter-based CTP/PTC (Ma et al., 2018; Wang et al., 2018; Wang et al.,2022; Zheng et al., 2018). While the controller inputs can be taken as the voltage difference between cells, cell voltage, SOC difference between cells, and average SOC, the output has always been balancing current.

The CBS has a nonlinear structure. Therefore, internal resistance, capacity, and charge-discharge parameters change dynamically. As a result, the characteristics of the charge/discharge of a new battery and a half-life battery are quite different. In addition, the topology efficiency makes it complicated to establish an accurate model of the CBS. FLC allows the behavior of a complex nonlinear CBS to be described simple because it does not require the model. However, expert knowledge of the system is needed when creating fuzzy rules. Insufficient knowledge causes poor balancing precision and a false balancing process.

2.3.2.3. Adaptive Neuro-Fuzzy Inference System Control Algorithm

The adaptive neuro-fuzzy inference system (ANFIS) is an intelligent control method that hybridizes FLC and neural network (NN). In FLC, the knowledge describing the expected behavior of a system creates the fuzzy rules set. This is an error-prone process. In the static system, it can be overcome by the tremendous effort of the system expert. However, many rules are required in dynamic systems such as CBS, which is very delicately obtained.

ANFIS method utilized the parallel computation and learning capability of NNs and the inference feature of FLC. It is used to model the black-box system defined with the given input-output data sets in the best way with the most appropriate network structure and parameter sets. The fuzzy system is subjected to a learning process that enables the adaptive adjustment of the fuzzy rules. ANFIS network, as shown in Figure 2.12, consists of five nodes having a particular function and bidirectional links. Connections between nodes show an indeterminate weight. All or some parameters of these nodes can be adaptive. Adaptation is created by specifying the outputs of these nodes with variable parameters. The learning rules determine how changeable parameters should be changed to minimize the difference between the output of the entire network and the target value (García et al., 2013).

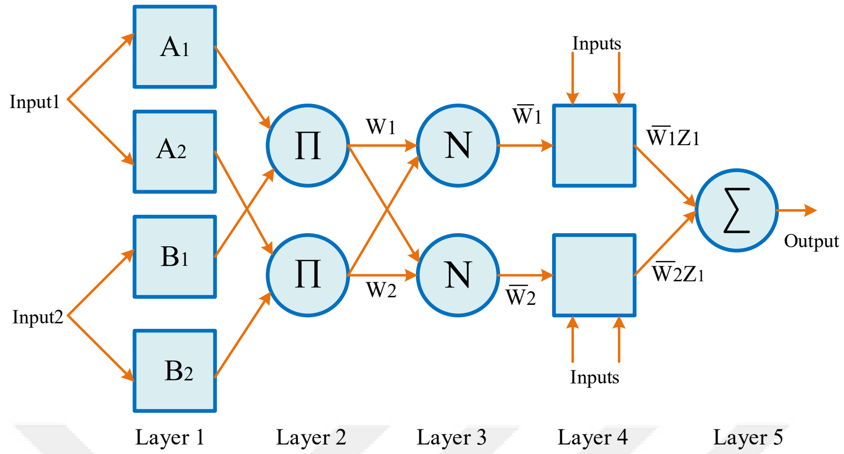


Figure 2.13. Schematic representation of ANFIS

There are several studies in the literature that developed an ANFIS-based control strategy. These studies have been tested for adjacent CTC topology and have revealed a more accurate and reliable balancing process than FLC (Nguyen et al.,2014; Nguyen et al., 2015). However, the training process of ANN algorithms requires an experimental dataset, which complicates the control system.

2.3.2.4. Genetic Algorithm

Genetic algorithm (GA) is a method utilized to produce the best solutions to optimization and local search problems by the inspired evolutionary process. In multidimensional state space, it operates iteratively according to the survival of the fittest.

A genetic algorithm is realized in basically five main steps as follows (Mit, 1998; Toledo et al., 2014):

- Genetic representation: The first step begins with generating the population of the problem. The population created for the GA algorithm is formed by gathering candidate solutions, also called individuals. Then the genetic representation of the candidate solutions to an optimization problem is obtained.

- Definition of fitness function: The fitness of each possible candidate is evaluated with a fitness function. The objective function of the optimization problem defines the fitness function.
- Selection: Selection is the process of selecting stronger individuals from the parents to create a new population.
- Crossover: Crossover is a process that creates new individuals by transferring the genetic material of two individuals.
- Mutation: The mutation process is the process of randomly appointing a gene in the chromosomes of the newly formed individual to another one by a mutation rate.

The iteration is realized by implementing the 2nd step to the 4th until the termination criteria are ensured.

A GA-based balancing strategy is developed for the PTC balancing topology. SOC and balancing current variables have been used to define the population, and minimum balancing time is used to determine the fitness function (Zhang et al.,2015; Zhang et al., 2016). GA algorithm is a more advanced algorithm than the balancing as mentioned earlier control algorithm. However, the design procedure is too complex for a BCS.

2.4. Literature Survey of the Active Cell Balancing System

When the literature is examined in detail, it is seen that there are dozens of balancing circuits and a wide variety of control strategies. The majority of these control strategies are heuristic. Therefore, it is complicated to classify them and make performance evaluations. For this reason, the examination field is narrowed to create a more reliable comparison with the proposed CBS. Recent publications on CBS using a DC-DC converter controlled by SOC-based BCS are provided in detail, and the performance of the examined studies is summarized in Table 2.1. It is noted that balancing speed is related to balancing current magnitude, the initial SOC difference (ΔSOC_{dif}) between a cell with maximum SOC and a cell with minimum SOC, the number of cells, the rated capacity of the cell, and desired SOC margin at the end of the balancing process. In this context, it should be known that the balancing process, which starts with the same SOC difference and is completed in a much shorter time, may be performed with a high balancing current, a low number of cells, or a cell with low-rated capacity.

Wu et al. proposed a FLC- based BCS for bidirectional Cuk converter-based direct CTC balancing topology. In the study, it is aimed to shorten the balancing time. A balancing system design for six series connected Li-ion batteries of 2.2 Ah has been made. FLC output is balancing current, and balancing control is provided so that its value is between 0-5 A. The results were taken in the simulation environment, and the balancing was completed in 429 s at standby condition (no-load current and no charge current).

Ouyang et al. proposed a SMC- based BCS for bidirectional Cuk converter-based adjacent CTC balancing topology. In the study, it is aimed to shorten the balancing time. SMC is used to provide maximum balancing current to the balancing system. A balancing system design for four series connected Li-ion batteries of 3.1 Ah has been made. And the maximum allowable balancing current is adjusted to 1 A for the converter operated in DCM. The results were taken in the experimental prototype, and the balancing was completed in 2286 s at standby condition.

Table 2.1. The conducted studies for DC-DC converter-based active CBS with SOC-based BCS

References	**Balancing Topology-Balancing Circuit**	**Balancing Algorithm**	**# of Cells**	**Initial ΔSOC_{dif}**	**End of ΔSOC_{dif}**	**Balancing Time**	**Initial SOCavg**	**End of SOC_{avg}**
Wu et al., 2021	Direct CTC -Cuk converter	FLC	6	18 %	1.02%	429 s	67.16%	66.98%
Ouyang et al., 2017	Adjacent CTC -Cuk converter	SMC	4	11%	2 %	2286 s	76.75%	~75%
Liao and Chen, 2022	Direct CTC-Buck-boost converter	FLC	9	19%	2.16%	2974 s	65.44%	64.36%
Ma et al., 2018	CTC-Buck-boost converter	FLC	32	20%	Less than 0.5%	1150 s	N/A	N/A
Wang et al., 2015	PTC-Single Flyback	Mean-difference algorithm	12	5.2%	1.5 %	4640 s	~28	~23%
Wang et al., 2015	CTP-Single Flyback	Mean-difference algorithm	12	5.2%	1.5 %	3260 s	~28	~26
Imtiaz et al., 2013	CTP-Single Flyback	Heuristic with Fixed duty cycle	4	37 %	4%	~5500s	N/A	N/A
Zhang et al., 2015	PTC-Multiple Flyback	GA	12	30 %	0.1%	799 s	N/A	~60 %
Wang et al., 2022	CTPTC-Multiple Flyback	MPC	5	13%	Less than 1 %	292 s	74 %	73.3%
Wang et al.,2018	CTPTC-Multiple Flyback	FLC	4	80 %	0.1%	3480 s	62,25%	56%
McCurlie et al.,2016	CTPTC-Multiple Flyback	MPC	6	27 %	2%	1260 s	68,35	69 %

Liao and Chen proposed a two-stage FLC-based BCS for bidirectional buck-boost converter-based CTC balancing topology. A balancing system design has been made for nine series connected Li-ion batteries, grouped in three of 3.2 Ah. In the first stage, in-group balancing was performed by six cell selection MOSFETs and a buck-boost converter-derived balancer circuit consisting of 1 inductor, 4 MOSFETs, and four diodes. In the second stage, two classical buck-boost converter circuits composed of 1 inductor and 2 MOSFETs were used for balancing between groups. FLC output is designed as a balancing current, and balancing control is provided so that its value is between 0-5 A. The simulation results compared with adjacent CTC topology. They indicated that equalization time is reduced by about 23.70% according to the maximum algorithm. Although the number of inductors is diminished, many MOSFETs are used, and the control structure is complicated according to the adjacent CTC balancing system (Liao and Chen, 2022).

Ma et al. proposed a two-stage FLC- based BCS for bidirectional buck-boost converter-based adjacent CTC balancing topology. A balancing system design has been made for four groups, each having eight series-connected Li-ion batteries of 1.6 Ah. In the first stage, in-group balancing was performed by seven buck-boost converter-derived balancer circuits consisting of 1 inductor and 2 MOSFETs. And three buck-boost converters were used for balancing between 4 groups in the second stage. FLC output is designed as a balancing current, and balancing control is provided so that its value is between 0-4 A. The simulation and experimental results were compared with the mean-difference algorithm to validate the superiority of the developed BCS. They indicated that equalization time is reduced by about 22% (Ma et al, 2018).

Wang et al. compared the balancing performance of CTP and PTC energy transfer modes using a single bidirectional flyback converter and a switch matrix balancing hardware. The CBS was the mean-difference algorithm with fixed duty cycle current control. In the study performed with 12 cells connected in series, the balancing times for 1.5% end-of-balancing ΔSOC_{dif} were measured as 3260 s and 4640 s for CTP and PTC, respectively. It is revealed that CTP energy transfer is more appropriate in terms of SOC_{avg} loss and balancing time. However, repeated charge-discharge cycles could not be avoided. (Wang et al., 2015).

Imtiaz et al. proposed a BCS for a single unidirectional flyback converter-based CTP balancing topology. The proposed BCS consists of a cell selection algorithm to prioritize charging the cell with the lowest SOC by the cells with the higher SOC. In addition, a fixed duty cycle at maximum value has been applied to the relevant discharge switches of each cell so that the converter will operate in DCM. Although balancing was started with 37 % initial ΔSOC_{dif}, balancing was completed in a shorter time compared to the mean-difference algorithm. However, repetitive charge-discharge cycles became inevitable because all cells were discharged with the same current (Imtiaz et al., 2013).

Zhang et al. proposed a GA-based BCS for multiple unidirectional flyback converter based- PTC balancing topology. Unlike topologies with a single flyback converter, this topology allows simultaneous discharge of each cell. So high balancing speed can be achieved since this topology can provide simultaneous discharge and high balancing current. GA is used to estimate discharging current of each cell, preventing repeated charge-discharge cycles. The balancing process for 12 cells connected in series was started with a 30% initial $\Delta SOC_{dif,}$ and this difference was reduced to 0.1 % in 799 s (Zhang et al., 2015).

McCurlie et al. proposed a MPC-based BCS for multiple bidirectional flyback converter based- CTPTC balancing topology. High balancing speed can be achieved with this topology, which allows simultaneous charging and discharging of cells. MPC estimates discharging and charging current of each cell, preventing repeated charge-discharge cycles. The balancing process for six cells connected in series started with 27 % initial ΔSOCdif, which is reduced to 2 % in 1260 s (McCurlie et al., 2016).

Wang et al. proposed a FLC-based BCS for multiple bidirectional flyback converter based- CTPTC balancing topology. FLC is used to adjust the discharging and charging current of each cell. The balancing process for four cells connected in series was started with 80 % initial ΔSOCdif, and this difference was reduced to 0.1 % in 3840 s (Wang et al.,2018).

Wang et al. proposed a MPC-based BCS for multiple bidirectional flyback converter based- CTPTC balancing topology. MPC is used to adjust the discharging and charging current of each cell. The balancing process for five cells connected in series was started with 13 % initial ΔSOCdif, and this difference was reduced to about 1 % in 292 s. The simulation and experimental results were compared with FLC-based BCS to validate the superiority of the developed BCS. The balancing time of FLC is found to be 654 s. (Wang et al.,2018).

2.5. Summary

In this chapter, state-of-the-art CBS technologies are investigated rigorously. Active CBS topologies and their balancing control strategies are explained in detail. Finally, a detailed literature survey of active CBS is conducted by summarizing related literature.

3. OVERVIEW OF BATTERY CELL MODELLING AND SOC ESTIMATION

3.1. Introduction

An efficient BMS is required to manage crucial tasks such as monitoring the battery, estimating battery states, balancing control, protecting the battery, recording critical data, and communicating. BMS ensures that each cell in the battery pack operates under favorable conditions by these vital functions. Also, all parts of BMS interact with each other. For example, a CBS requires SOC information of each cell for implementation of balancing control in BMS. In general, SOC is expressed as the ratio of the releasable capacity of the battery to its nominal capacity and cannot be measured directly on the battery using a sensor. Therefore, it is necessary to estimate the state of charge by using measurable values. However, it is challenging to estimate the actual charge state due to uncertainties such as the non-linear characteristics of the Li-ion battery, the effect of temperature, changing power demand, and aging of the battery. In the literature, many methods for estimating the SOC of Li-ion batteries are proposed by researchers. Direct measurement-based methods such as the Coulomb counting (CC) method, open-circuit voltage (OCV) method, electrochemical impedance spectroscopy (EIS), and artificial intelligence-based SOC estimation methods such as neural network (NN), fuzzy logic (FL), adaptive neuro-fuzzy inference system (ANFIS), and support vector machine (SVM) are light-weighted SOC estimation methods. Though these methods are low-cost and easy to apply in calculating SOC, each of them has some drawbacks (Zou et al., 2014; Ng et al., 2009; Lee et al., 2008; Rodrigues et al., 2000; Tong et al., 2016; Chemali et al., 2018; Singh et al., 2006; Li et al., 2007; Hu et al., 2015; Zahid et al., 2018; Antónet al., 2013).

Table 3.1. Advantages and disadvantages of SOC estimation methods

Categories	Method	Advantages	Disadvantages/Limitations
Direct measurement	OCV	• High estimation accuracy • Easy to implement	• Not suitable for online estimation because of a very long-standing time to reach the equilibrium condition. • Not applicable for discharging conditions.
	CC	• Simple method • Easy to implement	• Accumulation of measurement errors and disturbances. • Difficult to the determination of initial SOC, which causes a cumulative error. • Dependent on the accuracy of the current sensor
	EIS	• Low cost • Sensitive to SOC variations	• Not suitable for online application • A proper electrochemical model is necessary • Dependence of battery impedance on aging and temperature changes.
Learning algorithm	NN FL SVM ANFIS	• Good adaptability to the nonlinearity of the battery's model without any physical knowledge. • High estimation accuracy • Online implementation after the offline training process	• Impossible to collect the input parameters to cover the conditions affecting the SOC. • Requires large memory unit • Complex computation and time-consuming
Adaptive filter algorithm	KF-based H-∞ PF	• High estimation accuracy • Fast convergence at the wrong initial SOC • Online implementation	• Requires the high accuracy of the battery model • Obtaining a battery model is difficult due to uncertain factors such as aging and temperature. • Needs complex mathematical calculations

On the other hand, model-based SOC estimation methods present highly accurate SOC estimation and eliminate the insufficiencies of early mentioned techniques. These advanced methods are adaptive filter-based algorithms. The Kalman filter (KF) and its derivatives are well-known and commonly used candidates in this class. The KF-based algorithm estimates the states of the battery system by using the input and output information of the battery model and previous estimations. The model voltage is compared to the measurement voltage, and this difference is scaled with a factor known as Kalman gain for updating. Then, the model is fed back with this gain to improve the next estimations. KF, which can only be used in linear systems, is used by being linearized for the battery model with non-linear characteristics. So, extended KF (EKF), unscented KF (UKF), sigma point KF (SPKF), double expanded KF, adaptive EKF (AEKF), adaptive UKF, and the other derivatives are developed for SOC estimation for battery cell (Mastali et al.,2013; Tian et al., 2014; Chen et al., 2019; Ramadan et al., 2017; Zheng et al., 2018; Peng et al., 2019; Shrivastava et al., 2019; Xu t al., 2022; Tong et al.,2022; Lin et al., 2021; Zhang et al., 2022). Particle filter (PF) and H-∞ filter, the other filter-based methods, had been proposed to state the estimation of a nonlinear system without a linearization process. However, computational burden, especially in high dimensional systems, is an obstacle to these filters' well-performing (Wang et al.,2014; Charkhgard et al., 2015; Tulsyan et al., 2016).

Adaptive filter-based SOC estimation methods need a certain battery model that reflects the characteristics of the battery. There are different techniques related to dynamic battery modeling methods in the literature. These methods include empirical, electrochemical, and data-driven and equivalent circuit models. The empirical model is a simple and fast method based on creating a physical model of the system with the help of physical equations and determining model parameters with experimental results. However, the accuracy performance is low. The electrochemical model is a highly complex method based on the processes of the internal chemical structure of the battery. Therefore, this method is not used much for battery cell modeling. The data-driven battery modeling is a method that relies on building the battery model by establishing a relationship between terminal voltage output variable and input variables such as current, SOC, and temperature through a machine learning algorithm (Li et al., 2017; Fan, 2020; Liu et al., 2020). Finally, the battery model created with an equivalent circuit model (ECM) enables mathematical operations and increases the accuracy performance of the battery model. There are several ECMs used in the literature: the Rint model, the PNGV model, and the Thevenin model. Among them, Thevenin equivalent circuit-based battery models have good features in terms of computational burden and precision, making them widely used in EV applications (Hu and Peng, 2012; Fotouhi et al., 2016; Zhang et a., 2018; Peng et al., 2018; Zhang et al., 2018). To approximate the battery cell dynamics, the equivalent circuit consists of an internal resistance (R_0), controlled voltage source (U_{OCV}) directly related to the SOC, and resistor/capacitor (RC) networks.

In this thesis, an equivalent circuit model of the 2nd-order Thevenin ECM was obtained for the battery model, and this model was used in the design of the UKF, which is a model-based SOC estimation method.

3.2. Dynamic Model of Li-ion Battery

Thevenin ECM, included in the electrical circuit model, can be modeled in different degrees. Figure 3.1 shows the 2nd order Thevenin ECM. The circuit consists of an internal resistance (R_0), a controlled voltage source (U_{OCV}), and two resistor/capacitor (RC) networks connected in series. The U_{OCV} represents the open-circuit voltage of the battery cell and has a direct relationship with the SOC. R_0 is internal resistance; R_1 and C_1 are electrochemical polarization resistance and capacitance, respectively; R_2 and C_2 are concentration polarization resistance and capacitance. And U_T is the terminal voltage of the battery cell.

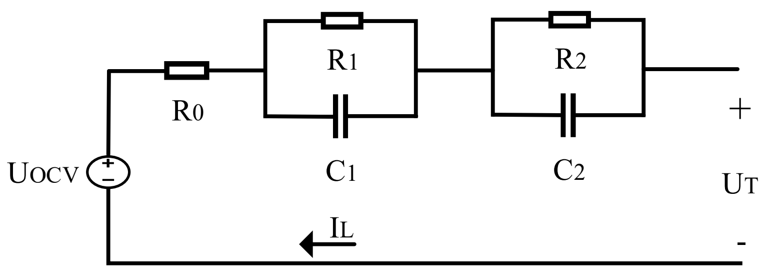


Figure 3.1. 2nd order Thevenin ECM of the battery cell

The U_T is expressed as follows, where U_1 and U_2 represent the voltage drops on the first and second RC networks, respectively. I_L is operation current, which is positive during discharge and negative during charge. Accordingly, the equations of the 2nd order Thevenin ECM are given in Eq. (3.1)- Eq. (3.3) as follows:

$$U_T = U_{OCV} - R_0 I_L - U_1 - U_2 \tag{3.1}$$

$$C_1 \frac{dU_1}{dt} = -\frac{U_1}{R_1} + I_L \tag{3.2}$$

$$C_2 \frac{dU_2}{dt} = -\frac{U_2}{R_2} + I_L \tag{3.3}$$

According to the above equations, the combined dynamic battery model is constructed using the second-order Thevenin model, OCV method, and CC method. SOC is obtained from the load current by using the CC method. The definition of the CC method is as follows:

$$SOC(t) = SOC(t_0) + \frac{1}{C_n} \int_0^{T_{bal}} i_L(t)\,dt \tag{3.4}$$

where *SOC(t)* is the current SOC, *SOC(t_0)* is the initial SOC, C_n is the maximum available capacity.

The OCV technique establishes the relationship between OCV and SOC. OCV is the difference in electrical potential between the two terminals of the battery while not connected to an electrical load. The rest points of the OCV of the test data are used in the curve fitting procedure to obtain the non-linear relationship between OCV and SOC. With this background, the state-space representation of the combined dynamic battery model is expressed below equations.

$$x = \begin{bmatrix} SOC & U_1 & U_2 \end{bmatrix} \tag{3.5}$$

$$\dot{x} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \frac{-1}{R_1 C_1} & 0 \\ 0 & 0 & \frac{-1}{R_2 C_2} \end{bmatrix} x + \begin{bmatrix} \frac{-1}{C_n} \\ \frac{1}{C_1} \\ \frac{1}{C_2} \end{bmatrix} I_L \tag{3.6}$$

$$y = \begin{bmatrix} f\left(OCV, SOC\right) & -1 & -1 \end{bmatrix} x + R_0 I_L \tag{3.7}$$

3.3. KF- Based SOC Estimation of Battery Cell

The KF is a filter that can predict the states of the system from the input and output information of the model in linear dynamic systems. The KF consists of two phases: predicting and updating. The calculations in these two stages are given below.

Prediction step

$$\hat{x}^{-}_{k|k-1} = A_k \hat{x}_{k-1|k-1} + B_k u_k \tag{3.8}$$

$$P^{-}_{k|k-1} = A_k \hat{P}_{k-1|k-1} {A_k}^T + Q_k \tag{3.9}$$

Updating step

$$K_k = P_{k|k-1} {C_k}^T \left(C_k P_{k|k-1} {C_k}^T + R_k \right)^{-1} \tag{3.10}$$

$$\hat{x}_{k|k}^{-} = \hat{x}_{k|k-1}^{-} + K_k\left(y_k - C_k\hat{x}_{k|k-1}\right) \quad (3.11)$$

$$P_{k|k} = (I - K_kC_k)P_{k|k-1} \quad (3.12)$$

where K is the Kalman gain, P is the state estimation covariance matrix, Q is the input covariance matrix, and R is the output covariance matrix.

However, the UKF, which does not require linearization, uses real nonlinear models and a roughly Gaussian distribution of the random state variable when estimating the SOC of the battery. Unlike the traditional KF, the UKF consists of four major steps: initialization, sigma point calculation, state prediction, and measurement update (Muratoğlu and Alkaya, 2019).

3.4. Summary

In this section, the electrical equivalent circuit model of a Li-ion battery cell and SOC estimation methods are developed to estimate the rate of available cell capacity, which is not directly measured in a battery cell, and are addressed in detail. Among them, the KF-based SOC estimation method has high accuracy and fast convergence. However, this method needs an exact model of the cell. Therefore, in this thesis, UKF from the KF family is used to estimate the SOC of each cell which is a control input of the proposed BCS.

4. DESIGN AND ANALYSIS OF PROPOSED CTP ACTIVE CBS

In this section, an analysis of the proposed CBS to reduce balancing time and increase the balancing efficiency of the CTP balancing topology is presented by providing information about the utilized balancing topology and its operating principles. Furthermore, the design procedure of the entire circuit is provided rigorously. Finally, the performance of the developed BCS has been tested with various case studies in Matlab/Simulink simulation environment.

4.1. Introduction

The CTP balancing topology stands out among the active cell balancing topologies for the balancing control facility of the BMS, thanks to its high balancing speed. For the CTP balancing topology, the DC-DC converter circuit is a good candidate due to its range of power capability, a wide range of voltage, and some types providing isolation between cell and pack. As a balancer circuit for CTP balancing, the flyback converter is a commonly used type thanks to its isolated nature, higher energy-transferring ability than the buck-boost converter, and simple design and less component according to the counterparts. Furthermore, the single unidirectional flyback converter-based CTP has only one transformer for N-cell with a series connected that guarantees a smaller size and price. On the other hand, BCS aims to reach the average SOC of all cells in minimum time. But this topology allows only a cell to discharge at any interval, causing longer balancing time.

An accurate and reliable balancing process is related to the decisions taken by the control system. Further, balancing time and balancing efficiency are related mainly to balancing strategy besides the topological improvements. Balancing strategies are responsible for selecting the cells to be charged and discharged and adjusting the balancing current, taking into account the characteristics of the balancing topology. BCS uses control algorithm(s) for adjustment of the current. When designing the BCS, the objectives of this algorithm can be minimizing the time or maximizing the balancing efficiency. While a high balancing current guarantees minimum balancing time, as we mentioned before, it causes repeated charge-discharge cycles to keep intermediate cells in a reasonable SOC range. Repeated cycles decrease balancing efficiency, which becomes problematic regarding usable capacity and battery life. So, the design of appropriate CBS that copes with repeated cycles is a crucial subject.

Researchers have offered many BCS for single flyback converter-based CTP balancing. These strategies include a rule-based algorithm called the cell selection algorithm based on determining the order in which cells will be discharged to reach the reasonable SOC range. Here, the switches of the cells to be discharged are controlled with a fixed duty cycle PWM signal, which will provide the maximum balancing current. Thus, none of them could achieve the simultaneous balancing of the cells and eliminate the repeated charge-discharge cycles.

In this study, a novel BCS has been developed for single flyback converter based- CTP active balancing, which significantly shortens the balancing time and provides a more efficient balancing process. Furthermore, with developed BCS, repeated charge-discharge cycles are eliminated. This is achieved by three major algorithms as follows:

- A cell selection algorithm provides that the switching period is divided into as many sub-periods as the number of cells so that the discharge currents are simultaneously withdrawn from the cells.
- A high-level control algorithm enables the estimation of the discharge currents of each cell with a proposed high-level control algorithm.
- A low-level control algorithm calculates the duration of these sub-periods (i.e., duty cycles of PWM) for supplying estimated discharge currents.

The description of the CTP balancing topology, the design criteria of the balancer circuit, and the proposed control algorithms for the developed BCS are presented meticulously in the following section.

4.2. Circuit Description and Design Consideration of the Balancing Topology

In CTP balancing, the flyback converter is used as an energy-transferring circuit raising the voltage of a cell to pack voltage. The balancing topology for four series connected cells is shown in Figure 4.1. The topology consists of one flyback transformer, six power MOSFETs, and seven fast recovery diodes. S_1 is discharging switch of $Cell_1$, S_2 and S_4 are discharging switches of $Cell_2$, S_3 and S_5 are discharging switches of $Cell_3$, and S_6 is discharging switch of $Cell_4$.

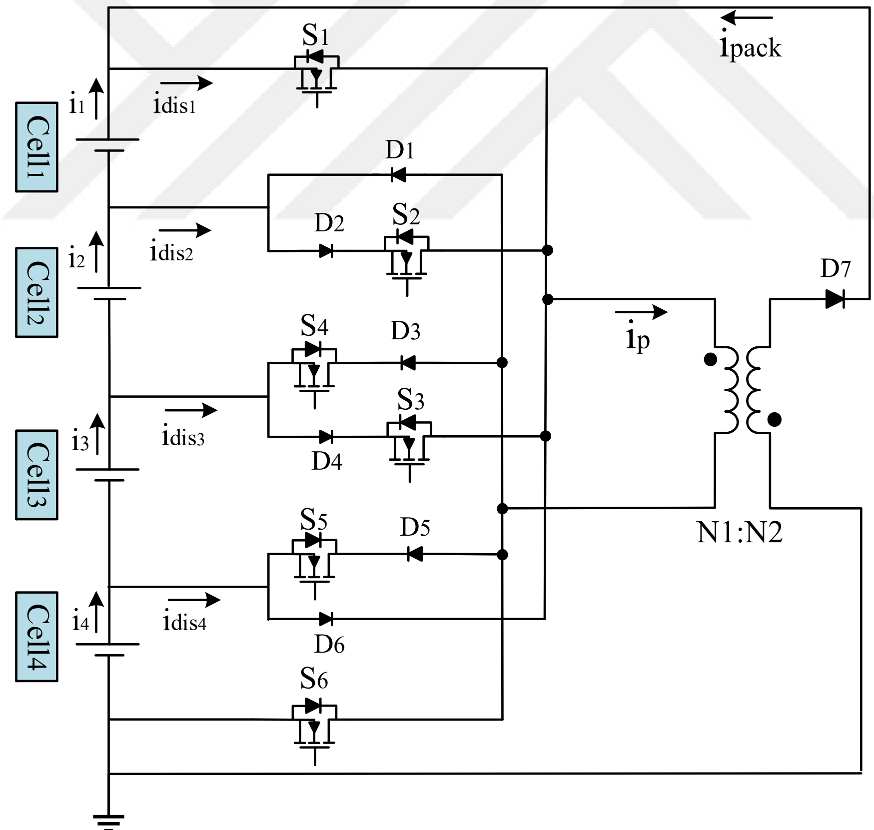


Figure 4.1. The single flyback converter based balancing CTP balancing topology

Determination of the operation mode of the converter is a crucial factor in the design procedure of the flyback converter as it affects transformer size, switching stress, and efficiency. The converter is operated in DCM mode ensures a higher efficiency rate when compared to CCM mode. Because DCM operation removes reverse recovery loss on the diode. Regarding the transformer size, DCM needs a smaller inductance means that smaller transformer size. With this motivation, the flyback converter is designed according to the DCM operation mode requirements.

A detailed explanation of the operating principle with the mathematical expression of the flyback converter in DCM is given in Section 2. Utilizing Eq. (2.21), the magnetization current is as follows:

$$I_{Lm(peak)} = \frac{V_{cell}}{L_m} DT \tag{4.1}$$

Magnetization current also equals the discharging current passing through the related switches.

$$I_{Lm(peak)} = I_{dis(i)} = I_p \tag{4.2}$$

The average discharging current during conduction time (DT) is expressed using Eq. (2.28) as given below.

$$I_{Lm(avg)} = \frac{1}{2} \frac{V_{cell}}{L_m} D^2 T \tag{4.3}$$

Hence, magnetization inductance which is the significant value to store sufficient energy, is calculated by utilizing Eq. (2.31),

$$L_M = \frac{{V_{cell}}^2 D^2 T}{2P_{out}} \tag{4.4}$$

Circuit elements of the converter are calculated to the following input and output specifications: Cell voltage: Vcell=3-4.2 V, Pack voltage: Vpack=12-16.8 V, Maximum output power: Ppack=5 W, Maximum duty cycle: D=0.45 switching frequency: f=5kHz,

The maximum value of the magnetization inductance of the designed flyback converter is calculated as 36.45 uH.

It should be noted that the maximum duty cycle occurs at the lowest input voltage, and pack voltage is the sum of the voltages of four cells. The turn ratio of the transformer is calculated as five by utilizing Eq. (2.32) as follows;

$$n = \frac{N_2}{N_1} = \frac{V_{pack}(1 - D - D_{dw})}{V_{cell(\min)} D} \tag{4.5}$$

4.3. Proposed Balancing Control Strategy

The developed strategy is explained by examining the three main control algorithms in the following sections.

4.3.1. Proposed Cell Selection Algorithm

The proposed cell selection algorithm determines the order in which a switching period is shared by cells. The balancing process starts with the selection algorithm sorting and comparing the SOC value of the cells. Then, it creates the discharge order list from cells with low SOC to cells with high SOC. Finally, the switching period is divided into N-1 sub-periods for the simultaneous discharging process of the cells in the order list. Accordingly, the algorithm generates turn-on or off signals for switches of the relevant cells.

The cell switches with the lowest SOC are turned off until the end of the balancing process. So, the lowest charged cell never discharged to the pack during the balancing process; it only charged by pack current. The remaining switches are operated according to the order list.

The operating principle of the balancing circuit with the proposed cell selection algorithm will be described with a random selection of initial SOC for four cells as follows: $SOC_2<SOC_4<SOC_3<SOC_1$.

For the initial SOC case considered above, S2 and S4 are turned off during the balancing process. However, in the first sub-period S6, second sub-period S3, and S5, the third sub-period S1 is turned on. The current waveforms during the balancing process are given in Figure 4.2.

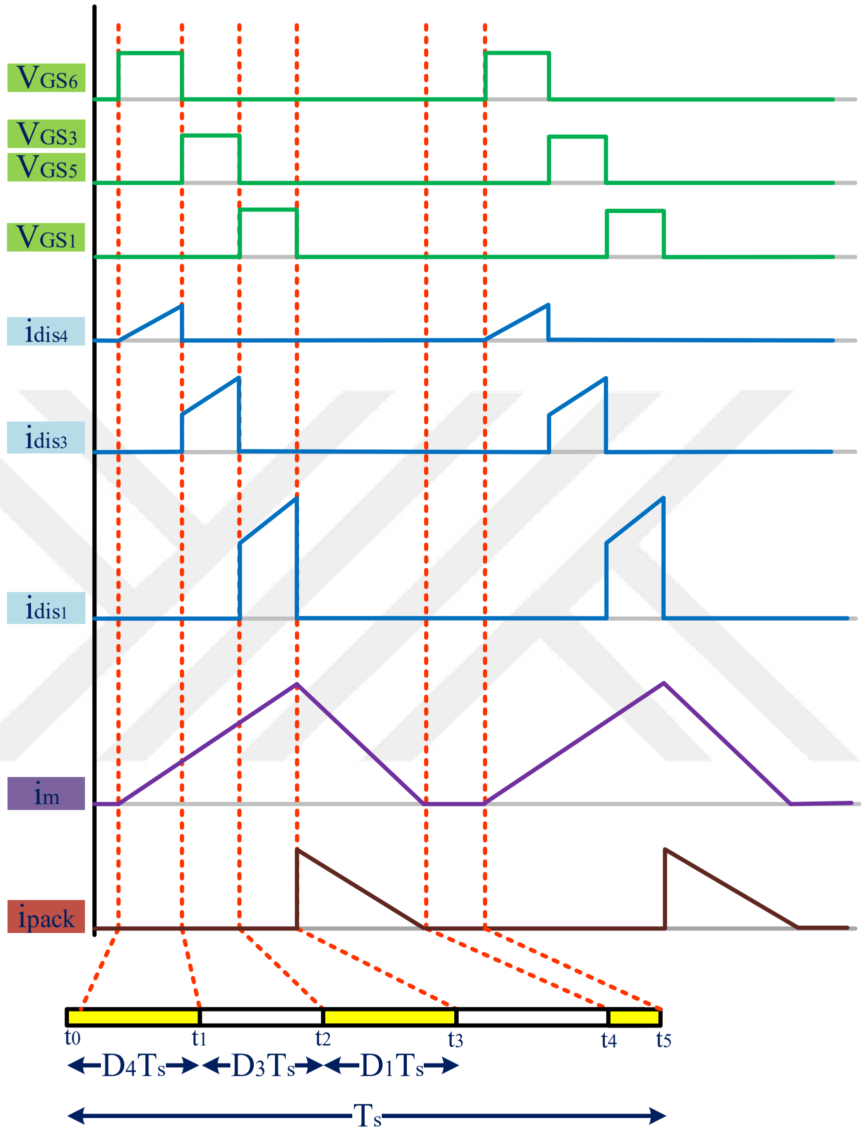


Figure 4.2. Current waveforms of the operating states

Interval (t_0-t_1): At the beginning of the sub-period, S6 is turned on, and all other MOSFET switches are turned off, as shown in Figure 4.3 (a). When S6 turns on, $Cell_4$ is connected to the primary side of the flyback converter, and energy begins to be stored in the magnetization inductor of the transformer. The inductor current rises linearly from zero. The peak discharging current supplied by the corresponding cell ($Cell_4$) is

$$I_{dis4(peak)} = \frac{V_{cell4}}{L_m}(t_1 - t_0) \tag{4.6}$$

(t_1- t_2) is on time of the S6, it is expressed as follows:

$$t_1 - t_0 = D_4 T_s \tag{4.7}$$

Where is the magnetization inductance of the transformer, V4 is the terminal voltage of the $Cell_4$, and D_4 is the duty cycle of the switching signal for the related switch.

Peak discharging current is derived as given below by substituting Eq. (4.7) into Eq. (4.6).

$$I_{dis4(peak)} = \frac{V_{cell4}}{L_m} D_4 T_s \tag{4.8}$$

The reverse polarity of the main diodes and body diodes of closed switches guarantee that related discharge current will not flow to the other cell.

Interval (t_1-t_2): S3 and S5 are turned on, and all other switches are turned off, as shown in Figure 4.3 (b). The peak discharging current supplied by the corresponding cell ($Cell_3$) is

$$I_{dis3(peak)} = I_{dis4(peak)} + \frac{V_{cell3}}{L_m}(t_2 - t_1) \quad (4.9)$$

$$t_2 - t_1 = D_3 T_s \quad (4.10)$$

Substituting Eq. (4.8) and Eq. (4.10) into Eq. (4.9), the peak discharging current is derived as given below.

$$I_{dis3(peak)} = \frac{V_{cell4}}{L_m} D_4 T_s + \frac{V_{cell3}}{L_m} D_3 T_s \quad (4.11)$$

Interval (t_2-t_3): S1 is turned on, and all other switches are turned off during this time interval, as shown in Figure 4.3 (c). The peak discharging current supplied by the corresponding cell ($Cell_1$) is as follows:

$$I_{dis1(peak)} = I_{dis3(peak)} + \frac{V_{cell1}}{L_m}(t_3 - t_2) \quad (4.12)$$

$$t_3 - t_2 = D_1 T_s \quad (4.13)$$

Substituting Eq. (4.11) and Eq. (4.13) into Eq. (4.12), the peak discharging current is derived as given below.

$$I_{dis1(peak)} = \frac{V_{cell4}}{L_m} D_4 T_s + \frac{V_{cell3}}{L_m} D_3 T_s + \frac{V_{cell1}}{L_m} D_1 T_s \quad (4.14)$$

The peak value of the magnetization current is equal to the peak discharging $I_{dis1(peak)}$.

$$I_{m(peak)} = \frac{T_s}{L_m}\left(V_{cell4}D_4 + V_{cell3}D_3 + V_{cell1}D_1\right) \tag{4.15}$$

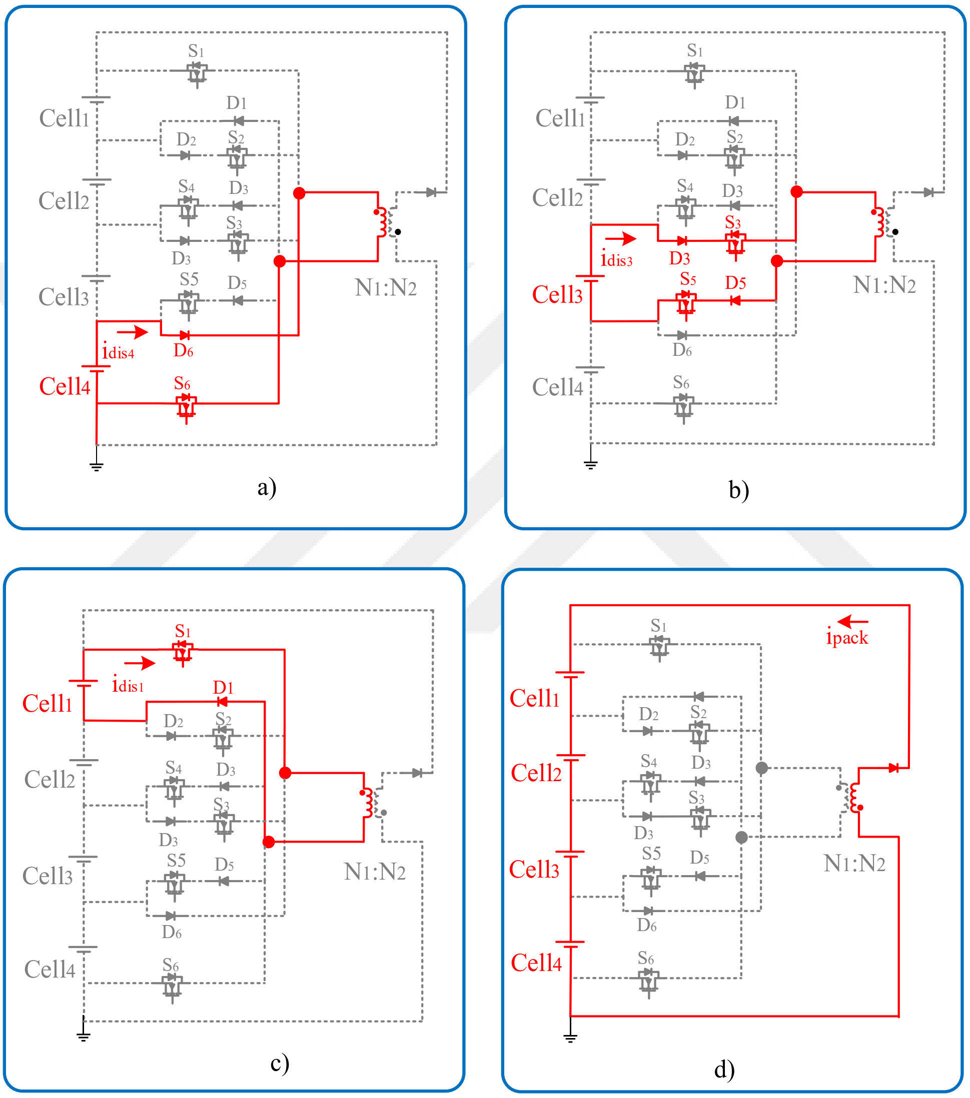


Figure 4.3. Operating states of balancing topology

Interval (t_3-t_4): All cell switches are turned off, and the secondary side diode conducts as shown in Figure 4.3 (d). The energy stored in the inductance of the transformer is transferred to the pack. The peak pack current is

$$I_{pack(peak)} \cong \frac{N_1}{N_2} I_{m(peak)} \tag{4.16}$$

Interval (t_3-t_5): This time interval is called dwell time in the DCM operation of the flyback converter. All voltages and currents are zero.

4.3.2. Proposed High-Level Control Algorithm

First, the battery balancing system description must be defined to develop the high-level balancing control algorithm. This explains the ideal energy transfer dynamic behavior of the balancing topology. Moreover, the SOC change of each cell during the balancing process can be described in detail.

.

4.3.2.1. Charge Transferring Model of CBS

In a battery cell, SOC is the ratio of the current releasable capacity in a battery cell to its total charge capacity of it. The total charge capacity in units Ah is specified by the manufacturer. And stored energy increases or decrease when a cell charges or discharges with a current. In this manner, the SOC of a cell is expressed as follows:

$$SOC(t) = SOC(t_0) + \frac{1}{Q_{\max}} \int i(t)dt \tag{4.17}$$

Where SOC(t_0) is the initial SOC, Q_{max} is the total charge capacity in units Ah, and *i* is the current through the cell.

SOC change according to the time is expressed as

$$\Delta SOC = SOC\left(t\right) - SOC(t_0) = \frac{1}{Q_{\max}} \int i(t)dt \tag{4.18}$$

In the CTP balancing topology, the supplied energy (charge) by a cell is equally distributed to all cells in the pack. The connection between N cells (i.e., how charge transfers) can be expressed with a topology matrix (Preindl et al., 2013, McCurlie et al., 2015).

$$T = \begin{bmatrix} \frac{1}{N}-1 & \frac{1}{N} & .. & \frac{1}{N} \\ \frac{1}{N} & \frac{1}{N}-1 & .. & 0 \\ \vdots & \vdots & & \vdots \\ \frac{1}{N} & \frac{1}{N} & .. & \frac{1}{N}-1 \end{bmatrix}_{NxN} \tag{4.19}$$

The charge that each cell transfers to the pack during balancing time are as follows:

$$Q_x = T_{bal} \begin{bmatrix} I_{dis1} \\ I_{dis2} \\ \vdots \\ I_{disN} \end{bmatrix}_{Nx1} \tag{4.20}$$

where T_{bal} is the total balancing time, I_{dis} is the discharge current of the cells, as given in Figure 4.1. Maximum charge capacity can be written as a diagonal matrix for cells 1 to N.

$$Q = \begin{bmatrix} Q_{\max} & 0 & .. & 0 \\ 0 & Q_{\max} & .. & 0 \\ : & : & : & : \\ 0 & 0 & 0 & Q_{\max} \end{bmatrix}_{NxN} \tag{4.21}$$

SOC is written in vector form as follows:

$$SOC = \begin{bmatrix} SOC_1 & . & . & SOC_N \end{bmatrix}_{Nx1}^{\mathrm{T}} \tag{4.22}$$

SOC change of each cell can be represented for CTP at the end of balancing time T_{bal} is

$$\Delta SOC = SOC(T_{bal}) - SOC(t_0) = Q^{-1} Q_x T \tag{4.22}$$

Eq. (4.22) is identical to Eq. (4.18). Therefore, it can be seen that $Q^{-1}Q_xT$ this denotes each cell's change rate of SOC.

4.3.2.2. Proposed Optimal Control Algorithm

The proposed optimal control (OC) algorithm ensures the minimum balancing time by applying the maximum balancing current to the cell with the maximum SOC difference. At the end of balancing SOC, all cell is equal to the average value of SOC. In this manner, the balancing time is calculated as follows:

$$SOC_j(T_{bal}) = \frac{1}{N} \sum_{1}^{N} SOC_j = SOC_{avg} \tag{4.23}$$

$$\left| \Delta SOC_{\max} \right| = \frac{I_{\max}}{Q_{\max}} T_{bal} \tag{4.24}$$

Utilizing from Eq. (4.24),

$$T_{bal} = \frac{Q_{max}}{I_{max}} \left| \Delta SOC_{max} \right| \tag{4.25}$$

Substituting Eq. (4.25) with the matrix form into Eq. (4.20), Q_x is derived as given below.

$$Q_x = Q^{-1} \frac{\left| \Delta SOC_{max} \right|}{I_{max}} \begin{bmatrix} I_{dis1} \\ I_{dis2} \\ : \\ I_{disN} \end{bmatrix}_{Nx1} \tag{4.26}$$

Then rearranging the Eq. (4.22),

$$\frac{I_{max}}{\left| \Delta SOC_{max} \right|} \begin{bmatrix} \Delta SOC_1 \\ . \\ . \\ \Delta SOC_N \end{bmatrix} = T \begin{bmatrix} I_{dis1} \\ . \\ . \\ I_{disN} \end{bmatrix} \tag{4.27}$$

Remark 1

From Eq. (4.27),

- If $\Delta SOC_j < 0$. The negative sign indicates that the j^{th} cell will be discharged to the pack through the DC-DC converter.
- If $\Delta SOC_j > 0$. A positive sign only indicates that the j^{th} cell is to be charged by the pack through the DC-DC converter.

Problem 1

Utilized topology allows only one direction charge transfer through the flyback converter. Therefore, the cell(s) below the SOC_{avg} never charge through the flyback converter. So, the optimal discharge currents must be calculated considering the topology capability.

Proposition 1

Eq. (4.27) can be described as a constrained least square problem. This problem is solved in a mathematical optimization algorithm called non-negative least-squares (NNLS). The NNLS optimization algorithm optimizes the non-negative solutions of the x values of a battery system model defined as Cx=d in Eq. (4.27) in a way that provides the minimum Euclidean norm (Turksoy and Teke, 2023).

Solving non-negative least-squares (NNLS) curve fitting problems of the form,

$$\arg\min_{x} \left\| Cx - d \right\|_2^2, \text{ subject to } x \geq 0 \tag{4.28}$$

where $d = \frac{\Delta SOCI_{\max}}{\Delta SOC_{\max}}$, $x = I_{disj}$, $C = T$ is the topology matrix of the system, and $\left\| .. \right\|_2^2$ denotes the Euclidean norm, and d is the Nx1 matrix.

The NNLS problem is described as a quadratic programming problem due to the nonlinear characteristics of the battery system.

$$\arg\min_{x \geq 0} \left(\frac{1}{2} x^T Q + c^T x \right) \tag{4.29}$$

where $Q = C^T C$ and $c = -C^T d$

To solve this problem, the active-set method algorithm was defined by (Lawson and Hanson, 1995).

4.3.3. Low-Level Control

The high-level control algorithm and the selection algorithm define the average discharge currents and discharge sequence list that will bring all cells to the SOC_{avg} in minimum time. A low-level control generates the PWM signal to actuate estimated discharge currents. The waveform of the primary-side current of the transformer, as shown in Figure 4.4 is utilized to describe the average discharge currents.

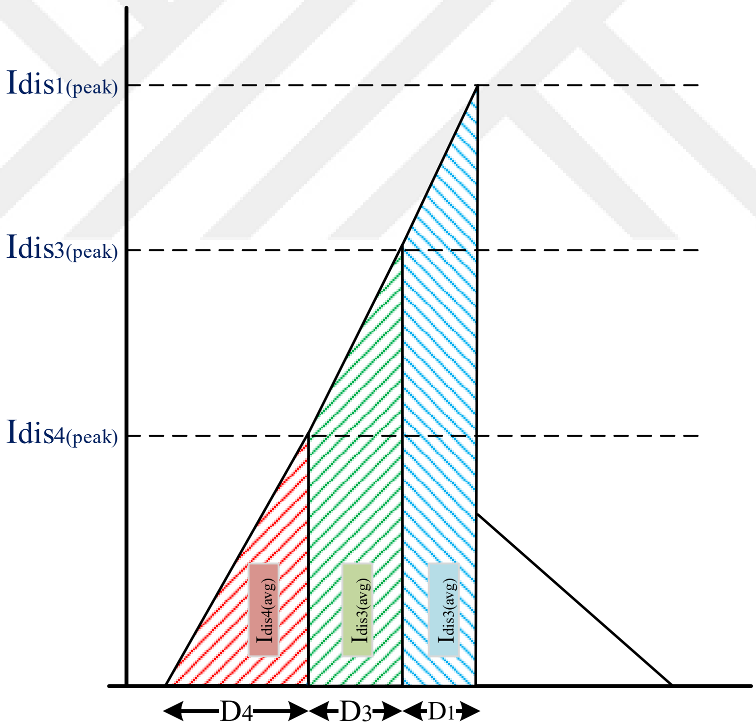


Figure 4.4. Primary side current of the flyback converter

The graph shows red, green, and blue scanned areas correspond to the average discharge currents of $Cell_4$, $Cell_3$, and $Cell_1$, respectively. These areas are calculated as

$$I_{dis4(avg)} = \frac{1}{2}\left(I_{dis4(peak)}\right)D_4 = \frac{T_s}{2L_m}\left(V_{cell4}D_4^{\,2}\right) \tag{4.30}$$

$$\begin{aligned} I_{dis3(avg)} &= \frac{1}{2}\left(I_{dis4(peak)} + I_{dis3(peak)}\right)D_3 \\ &= \frac{T_s}{2L_m}\left(2V_{cell4}D_4D_3 + V_{cell3}D_3^{\,2}\right) \end{aligned} \tag{4.31}$$

$$\begin{aligned} I_{dis1(avg)} &= \frac{1}{2}\left(I_{dis3(peak)} + I_{dis1(peak)}\right)D_1 \\ &= \frac{T_s}{2L_m}\left(2V_{cell4}D_4D_1 + 2V_{cell3}D_3D_1 + V_{cell1}D_1^{\,2}\right) \end{aligned} \tag{4.32}$$

When the $I_{dis4(avg)}$, $I_{dis3(avg)}$, and $I_{dis1(avg)}$ were calculated by the proposed high-level control algorithm are put into the Eq. (4.30), Eq. (4.31), and Eq. (4.32), the solution set gives the duty cycles D_4, D_3, and D_1 of related cells.

It should be noted that the charge efficiency (CE), expressed as electron transfer efficiency in a battery, is described as $\eta=1$ during discharging and $\eta<1$ for charging. This means that when a cell spends 1 unit of capacity, the cell which becomes charged with this capacity does not keep all of the sent capacity. Further, none of the balancing circuits is operated 100% efficiency. Both of these cause a decrease in the average SOC over time. For this reason, the developed control strategy optimizes the balancing currents when the difference between the initial SOC_{avg} and current SOC_{avg} is higher than a threshold value to adapt to the average SOC loss. The flowchart of the proposed BCS is given in Figure 4.5.

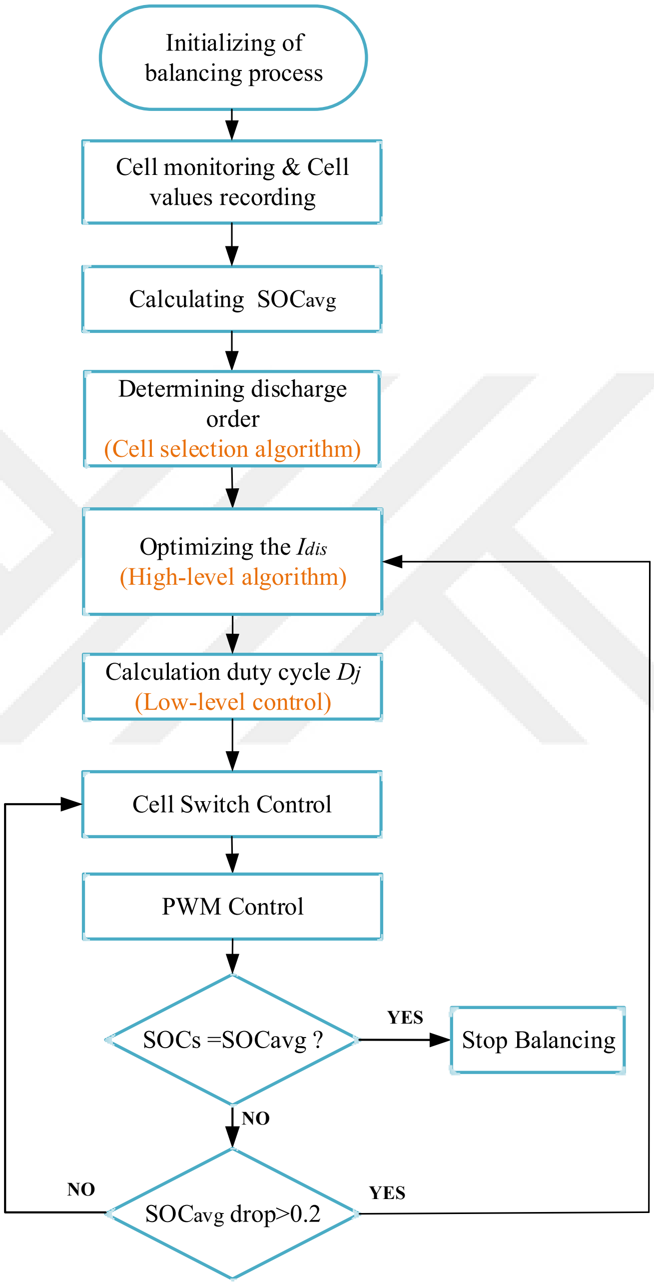


Figure 4.5. Flowchart of the developed BCS

4.4. Performance Results

To evaluate the performance of the developed BCS for single flyback converter-based CTP active balancing, the system has been designed and tested in the MATLAB/Simulink environment. The simulation parameters of the designed system are given in Table 4.1. Also, the performance result of the proposed BCS has been compared with the commonly used rule-based balancing control algorithm.

Table 4.1. Simulation parameters of the designed balancing system

Parameter	Symbol	Value
Transformer magnetization inductance	Lm	36 uH
Transformer turn ratio	N_1/N_2	1:5
Switching frequency	f_s	5 kHz
Maximum duty cycle	D_{max}	0.45
Maximum discharging current	I_{max}	1 A
Number of cells	-	4
Rated cell capacity	Q	3.2 Ah
Nominal cell voltage	V_n	3.6 V
Sample time of the simulation	T_{sample}	1 us

In this study, the performance results of the proposed BCS at 18 % initial SOC difference with four cells are presented. The initial SOC of each cell is also set at 94%, 76%, 87%, and 80%. The proposed BCS defines the discharge order list $\mathrm{Cell}_2 < \mathrm{Cell}_4 < \mathrm{Cell}_3 < \mathrm{Cell}_1$ according to the cell selection algorithm. In this situation, Cell_2 never discharges during the balancing process. Therefore, the maximum balancing current is implemented to the highest charged cell, which is Cell_1, for providing minimum balancing time. The estimated discharging current has been estimated as $\mathrm{I}_{\mathrm{dis1}} = 1.022\mathrm{A}$, $\mathrm{I}_{\mathrm{dis2}} = 0$, $\mathrm{I}_{\mathrm{dis3}} = 0.677\mathrm{A}$ and, $\mathrm{I}_{\mathrm{dis4}} = 0.246\mathrm{A}$

by the NNLS algorithm. At the beginning of the balancing, duty cycles are calculated as D_1=0.1330, D_2=0, D_3=0.1332, and D_4=0.1421 by the low-level control method. Accordingly, the secondary side diode is forward-biased after (D_1+D_2+D_4)Ts seconds, and the total stored energy is transferred to the pack. This means energy is stored for 83.75 microseconds of the one switching time. The discharge currents of the related cell and primary and secondary side (pack) currents of the flyback converter during the balancing process are illustrated in Figure 4.6.

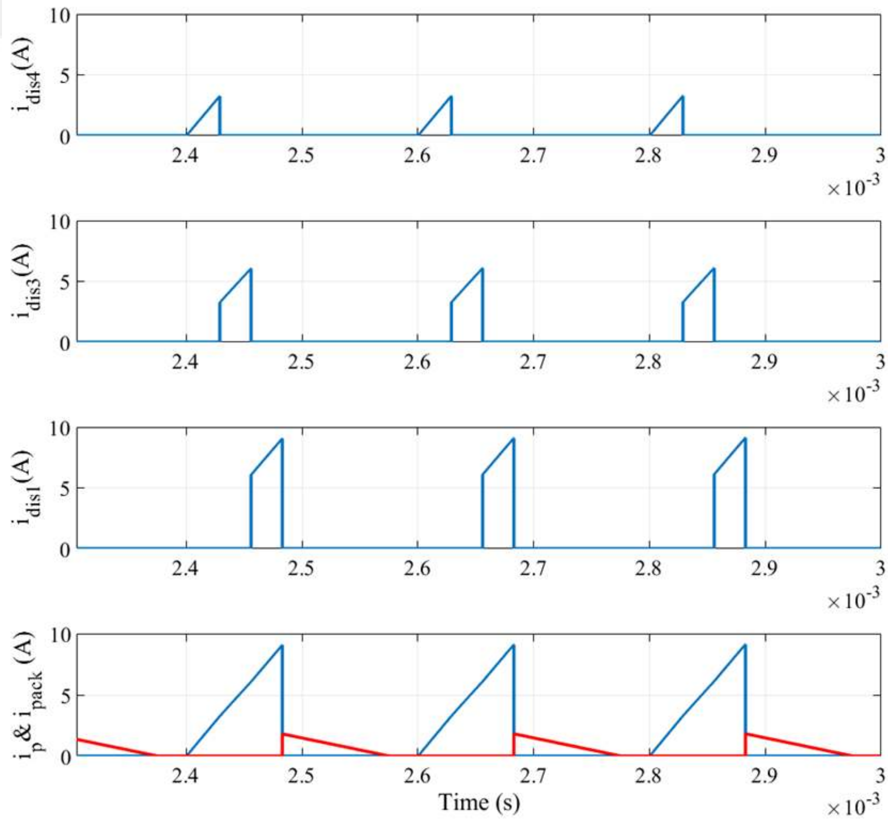


Figure 4.6. Discharging, primary and secondary-side currents

The SOC profiles of cells in the balancing process controlled by the proposed BCS and rule-based approach are shown in Figure 4.7 and Figure 4.8. It is concluded that the balancing process completes in the 1760s with the proposed BCS and 4000s with the mean-difference algorithm. Further, it is deduced that the balancing time with the proposed BCS is 56% shorter than the mean-difference algorithm. Because it never allows repeated charge-discharge cycles. Figure 4.9 and Figure 4.10 illustrate the balancing current profiles of the cells in the balancing controlled by the proposed BCS and mean-difference approach, respectively. It can be seen that the currents frequently increase and decrease from the maximum to the minimum at a later stage of balancing controlled by the mean-difference algorithm. This current change corresponds to frequent turned-on turned-off of the switching components causing high switching losses. Figure 4.11 and Figure 4.12 show the terminal voltage graph of the cells in the balancing process controlled by the proposed BCS and mean-difference algorithm, respectively. Although the difference between cell voltages is very low, the SOC differences can be very high. From this point of view, it is clear that SOC-based balancing strategies will achieve higher accuracy cell balancing.

On the other hand, SOC_{avg} has declined from 84.25% to 82.61% in balancing controlled by the proposed BCS and 82.47% by the mean-difference algorithm. It is obvious that the energy loss of the proposed BCS and mean difference algorithm remain almost the same. In Table 4.2, the comparison of the performance results of flyback converter-based CTP balancing controlled by the proposed BCS and mean-difference algorithm are given in detail. It can be concluded from the table that BCS improves the balancing performance in terms of balancing speed and efficiency.

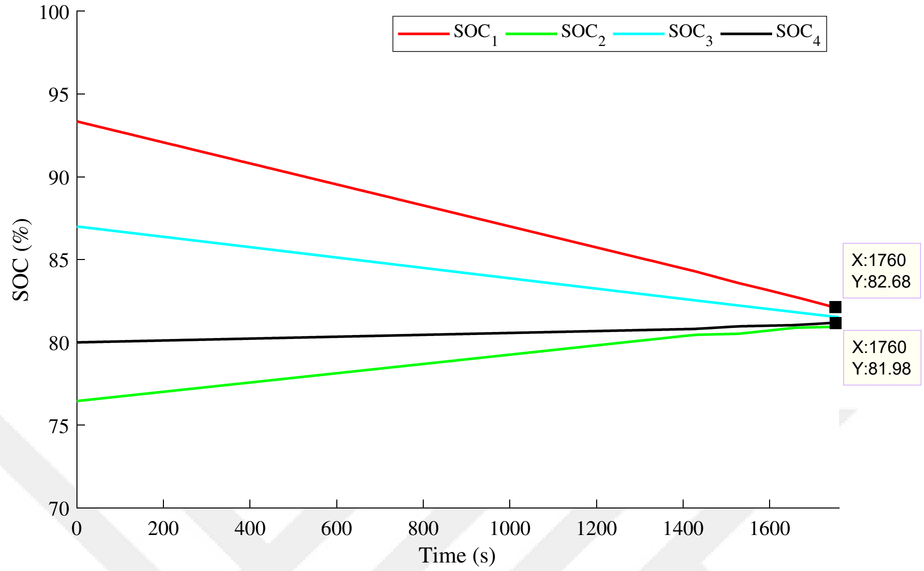


Figure 4.7. SOC profiles during balancing controlled by proposed BCS

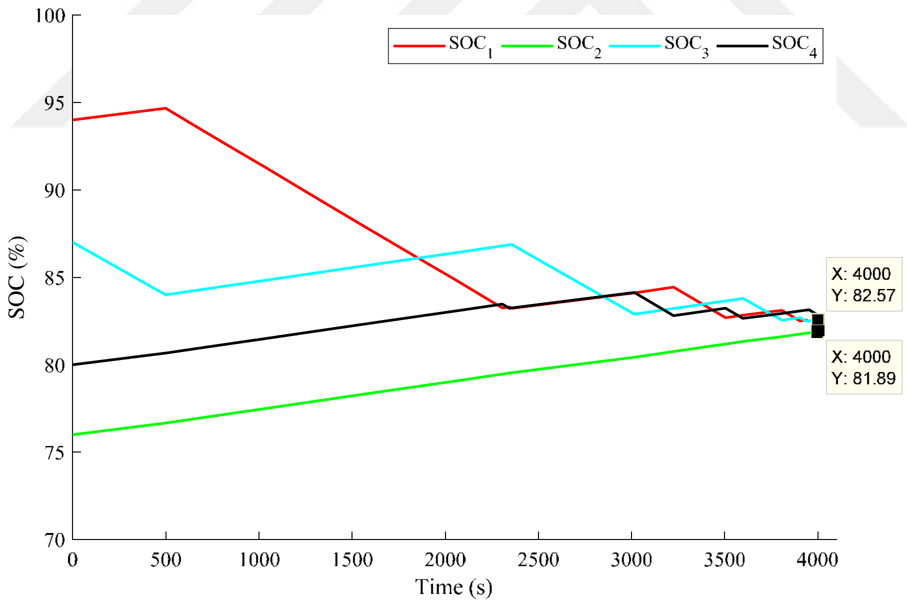


Figure 4.8. SOC profiles during balancing controlled by the mean-difference algorithm

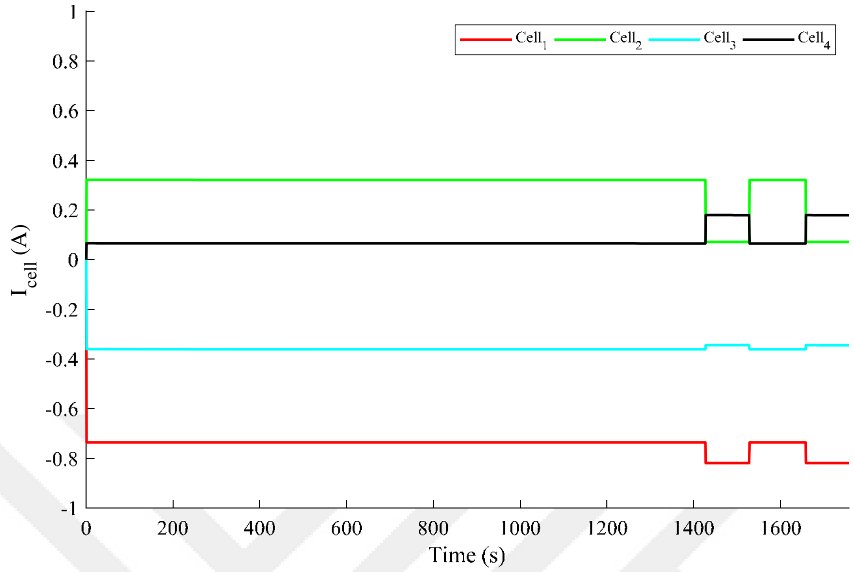


Figure 4.9. Cell currents during balancing controlled by proposed BCS

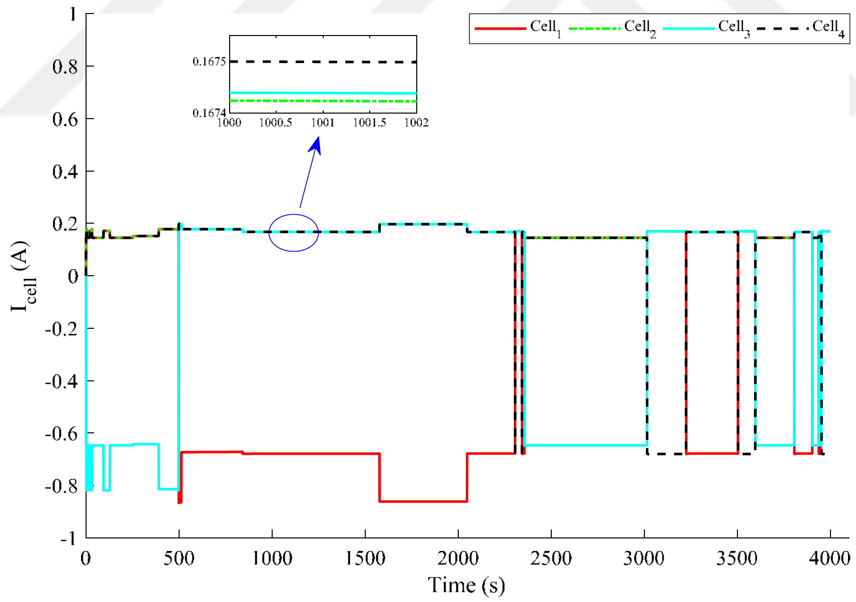


Figure 4.10. Cell currents during balancing controlled by mean-difference algorithm

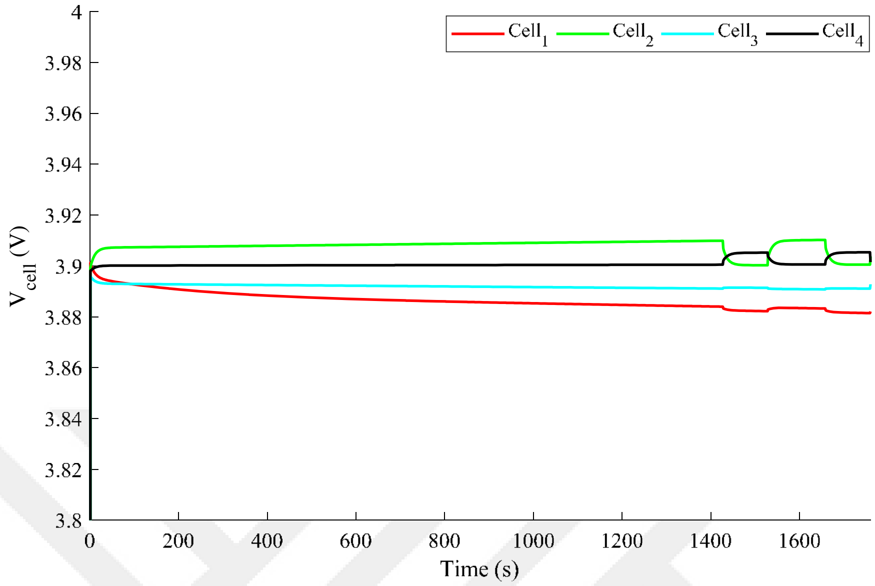


Figure 4.11. Terminal voltage graphs during balancing controlled by proposed BCS

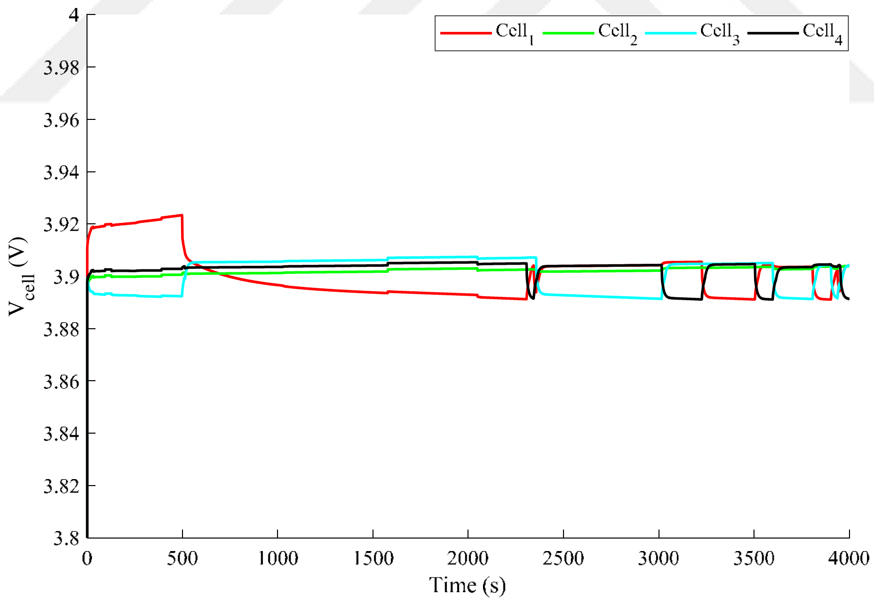


Figure 4.12. Terminal voltage graphs during balancing controlled by mean-difference algorithm

Table 4.2. Comparison of the proposed BCS and conventional BCS

Control strategy	**SOC_{avg} at end of balancing**	**Total balancing time**	**SOC_{avg} loss**
Mean-difference control algorithm	82.47%	4000 s	1.78%
Proposed NNLS-based optimal control algorithm	82.6 %	1760 s	1.64%

4.5. Summary

The description of the CTP balancing topology and the proposed control algorithms for the developed BCS for the CBS are explained in detail in this chapter. The operating principle of the CBS with the proposed BCS is also introduced. Finally, the balancing performance results are presented for CBS, which operated with a conventional rule-based control algorithm and proposed BCS. The proposed BCS achieves a significant reduction of balancing time is about 56%.

5. DESIGN AND IMPLEMENTATION OF PROPOSED CTPTC ACTIVE CBS

This section presents the proposed CTPTC active cell balancing system's design and implementation by providing information about the utilized balancing topology, balancing circuit, and BCS. The design considerations of the entire balancing circuit and proposed BCS are provided rigorously. Furthermore, the experimental design procedure and PCB design of the whole balancing circuit and PCB design are explained in detail. A simulation test has been performed Matlab/Simulink simulation program. In the experimental studies, the control signals produced by the proposed BCS were performed by the dSPACE DS1104 control board.

5.1. Introduction

The CTPTC balancing topology stands out among the active cell balancing topologies for the balancing control facility of the BMS, thanks to its highest balancing speed. In this topology, the charge is removed from one cell and distributed equally amongst all the cells in the pack. Likewise, the charge can be removed from the entire pack and placed back in a single cell. CTPTC topologies are available in two different styles of balancer circuit design. One of these is a one-balancer circuit for an N-series connected pack. The other is to design an individual cell balancer (ICB) for each cell in a pack. In a bidirectional ICB circuit, each cell has its charge flow path connecting it and the pack. This allows charge movement to and from multiple cells simultaneously.

For the CTPTC balancing topology, the bidirectional DC-DC converter circuit is a good candidate for a balancer circuit due to its power capability and wide voltage range. Furthermore, as a balancer circuit for CTPTC balancing, the bidirectional flyback converter is a commonly used converter type thanks to its isolated nature, higher energy-transferring ability, simple design, and less component according to the counterparts.

Besides the topological improvement, a good performed BCS also ensures balancing time minimization and especially energy consumption minimization in a CBS. Further, an accurate and reliable balancing process is related to the decisions taken by the BCS. BCSs, as mentioned before, are responsible for selecting the cells to be charged and discharged. Therefore, the balancing current adjustment considers the balance topology's charge-transferring ability.

In ICB circuit-based CTPTC balancing topologies, while the energy is transferred from the high-charged cell to the package, the MOSFET switch on the primary side of the flyback converter is in conduction. Conversely, while the transferred energy is transferred from the pack to the low-charged cell, the MOSFET switch on the secondary side of the flyback converter of the relevant cell is in conduction. With this background, significant reasons for energy losses during the balancing process;

- CE efficiency is a value between 0 and 1.
- The flyback converter efficiency is not 100%
- Switching losses

In all Li-ion battery cells, CE is related to the characteristics of the battery cell, and the loss of charge caused by its shortcomings cannot be avoided. But it can be reduced by minimized charge-discharge cycles. On the other hand, energy efficiency can be increased by increasing converter efficiency and using soft switching techniques. However, this exaggerates the already high cost and size of ICB-based CTPTC topologies. Therefore, the cheapest and most effective way of minimizing energy losses is to use a minimum number of charge-discharge paths to provide higher efficiency with less switching. This is possible with a well-designed BCS.

Many researchers have tried to bring all cells in minimum balancing time to balance with maximum balancing current by utilizing mean-difference and its derivatives-based BCS for ICB-based CTPTC. However, repeated charge-discharge cycles which arise from the reaching of intermediate cells to the balanced region earlier cause high energy losses and longer balancing time, as mentioned in the previous section. Some researchers, to prevent repeated charge-discharge cycles, proposed more advanced BCSs. These BCSs have used a complex control technique such as MPC that estimates the charge-discharge currents of each cell, and controllers such as PID and sliding mode controller (SMC) that provide bidirectionally adjustment of these balancing currents. Although they largely avoid repetitive cycles, they need accurate cell and system models and have more complex control structures. Also, large memory requirements when considering using hundreds of cells in the EV make designed BCS impractical. In addition, the rule-based and advanced BCSs are designed to ensure that all four MOSFETs and all flyback transformers are in conduction during the balancing process. However, it means insufficient improvement in reaching the desired energy efficiency and increasing the usable capacity. In this study, a BCS is developed to minimize energy losses and the balancing time. Developed BCS has many advantages. First, it is easy to implement, independent of the cell and system model. Second, repetitive charge-discharge cycles are eliminated. Third, it dramatically reduces the overall system's total energy consumption.

The following sections present the description of the ICB-based CTPTC balancing topology, the design criteria of the balancer circuit, and the developed BCS in detail. Furthermore, the experimental design procedure and PCB design of the overall system are provided rigorously.

5.2. Circuit Description and Design Consideration of the Balancing Topology

Figure 5.1. gives a schematic representation of the ICB-based CTPTC topology to be implemented for a four-cell battery pack implemented using a

multiple flyback converter. This topology consists of N flyback transformer, 2N power MOSFETs, and 2N capacitors. S_{jp} where (j=1…N) is the primary switch turned on when the cell discharges to the pack. S_{js} is the secondary switch that is turned-on when the cell is charged from the pack.

Determination of the operation mode of the converter is a crucial factor in the design procedure of the flyback converter as it affects transformer size, switching stress, and efficiency. The converter is operated in DCM mode ensures a higher efficiency rate when compared to CCM mode. Because DCM operation removes reverse recovery loss on the diode. Regarding the transformer size, DCM needs a smaller inductance means that smaller transformer size. With this motivation, the flyback converter is designed according to the DCM operation mode requirements.

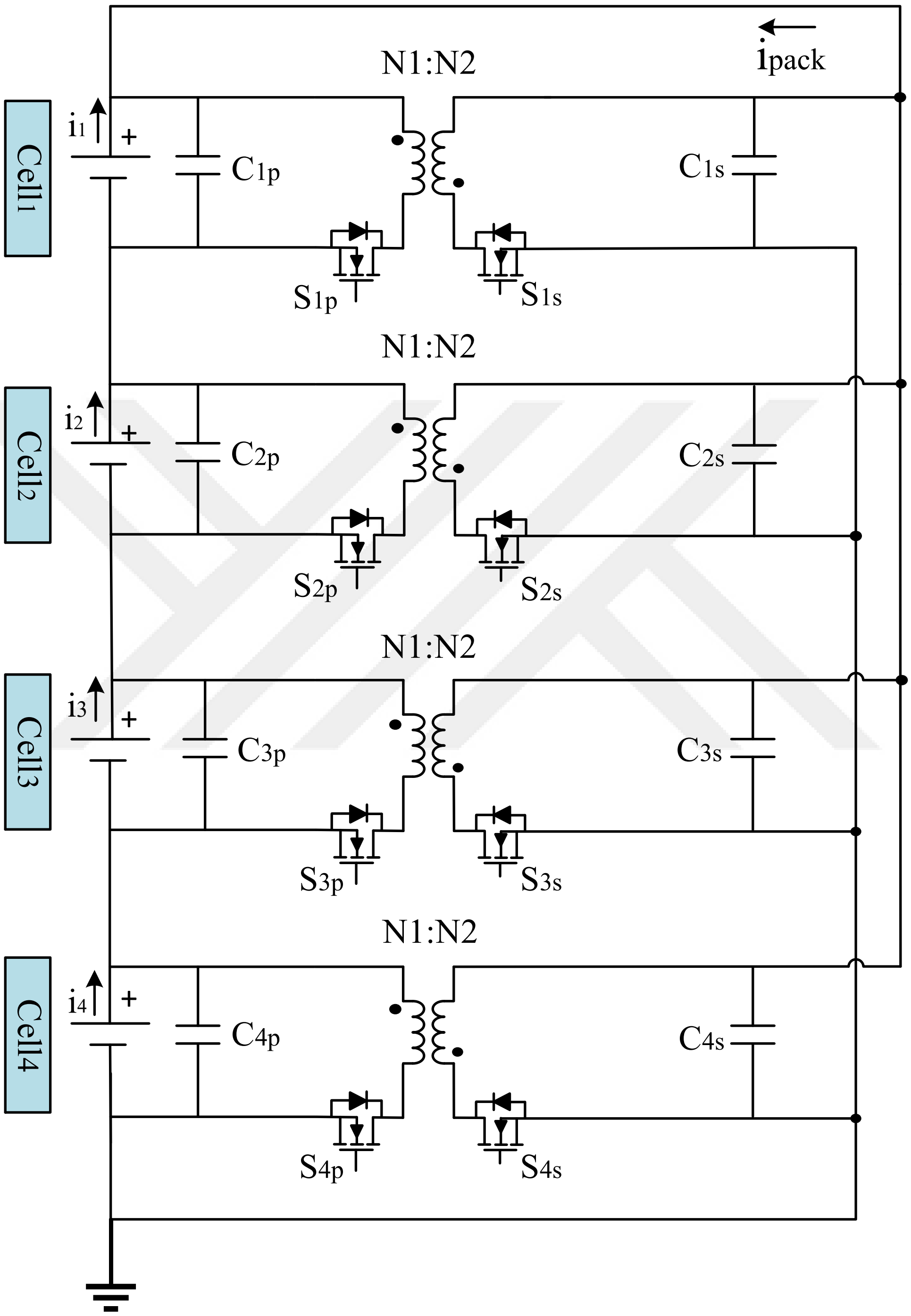


Figure 5.1. Multiple flyback converter-based CTPTC balancing topology

5.2.1. Flyback Converter Design and Component Selection

The design of a flyback converter involves numerous significant trade-offs and design decisions. Each stage of the design process for a straightforward flyback converter will be covered in the following sections. The proposed design flow is depicted in Figure 5.2.

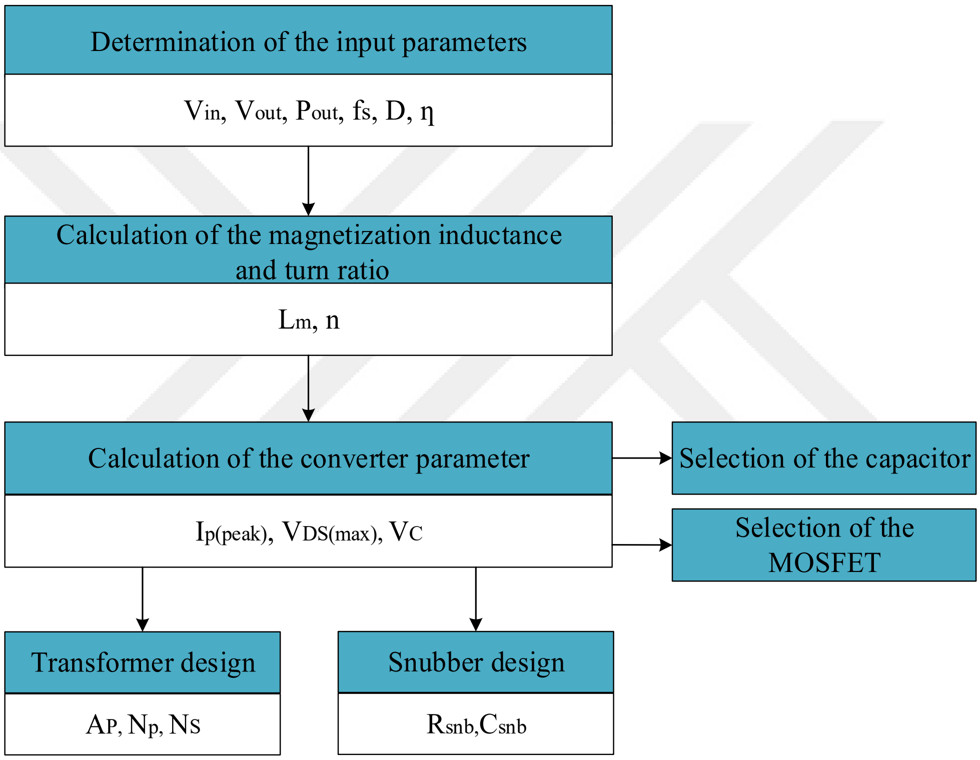


Figure 5.2. Design procedure of flyback converter

5.2.1.1. Determination of Input Parameters

Table 5.1. Design parameters of flyback converter

Direction	Parameter	Symbol	Value
CTP	Input voltage	V_{cell}	3 V-4.2 V
	Output voltage	V_{pack}	12-16.8 V
	Switching frequency	f_s	5 kHz
	Maximum duty cycle	D_1	0.5
	Maximum output power	P_{pack}	5 W
	Expected efficiency	η	0.85
PTC	Input voltage	V_{pack}	12-16.8 V
	Output voltage	V_{cell}	3 V-4.2 V
	Switching frequency	fs	5 kHz
	Maximum duty cycle	D_2	0.7
	Maximum output power	P_{cell}	5 W
	Expected efficiency	η	0.75

In the bidirectional flyback converter design for cell balancing, the input voltage is equal to the cell voltage in the discharge direction (CTP) and the pack voltage in the charge direction (PTC). In real applications, using a li-ion battery under 20% SOC shortens the battery life due to the depth of discharge. For this reason, the cells should be charged when they reach 20% SOC. A Panasonic NCR1860B type li-ion cell has a voltage of almost 3 V at 20% SOC. This means the minimum input voltage in the discharge direction. The output voltage is the pack voltage, and its maximum value is approximately 16.8 V, four times the maximum cell voltage.

5.2.1.2. Calculation of Magnetization Inductance and Turn ratio

The worst-case scenario is when the converter operates at a maximum duty cycle, minimum input voltage, and maximum power. The maximum magnetization inductance is calculated by adding the efficiency expression to Eq. (2.31) as follows:

$$L_{M(\max)} = \frac{V_{cell(\min)}{}^{2} D_1{}^{2} \eta}{2 f_s P_{out(\max)}} \quad (5.1)$$

$$\mathrm{L}_{\mathrm{M(max)}} = \frac{(3)^2 (0.5)^2 0.85}{2(5000)5}$$

$$\mathrm{L}_{\mathrm{M(max)}} = 38.25\mathrm{uH}$$

The same worst-case scenario is applied to calculate turn ratio of the transformer. It is noted that, when a cell is at a maximum voltage value, balancing is terminated for the protection of the battery, and also when a cell is at the minimum value the maximum output voltage is affected by this voltage drop. When these all considerations are into account maximum, output voltage is nearly 15.3 V. By using the Eq. (2.32), the turn ratio of the transformer is calculated as follows.

$$n = \frac{N_2}{N_1} = \frac{V_{pack(\max)}(1 - D_1)}{V_{cell(\min)} D_1} \quad (5.2)$$

$$\mathrm{n} = \frac{\mathrm{N_2}}{\mathrm{N_1}} = \frac{15.3\mathrm{x}(1 - 0.5)}{3\mathrm{x}0.5}$$

$$\mathrm{n} = \frac{\mathrm{N_2}}{\mathrm{N_1}} \approx 5.1$$

By calculating the turn ratio, the maximum value of the secondary side inductor of the transformer can be calculated below.

$$\sqrt{\frac{L_m}{L_s}} = \frac{N_1}{N_2} \tag{5.3}$$

$$\sqrt{\frac{38.25}{L_s}} = \frac{1}{5}$$

$$I_{s(max)} \approx 956uH$$

5.2.1.3. Calculation of the Converter Parameter

The value of the peak current passing through the primary is essential for choosing the suitable MOSFET and determining the number of turns of the transformer. Therefore, the primary peak current that the switch will have to withstand is calculated considering the worst case as follows.

$$I_{p(peak)} = \frac{V_{cell(\min)} D_1}{f_s L_m} \tag{5.4}$$

When the value of L_m is calculated in Eq. 5.1 is substituted in Eq. 5.4,

$$I_{p(peak)} = \frac{3x0.5}{5000x38.25x10^{-6}}$$

$$I_{p(peak)} \approx 7.85A$$

The voltage the primary side switch will have to withstand is calculated using Eq. 5.4.

$$V_{DS(\max)} = V_{cell(\max)} + \frac{D_1 V_{cell(\min)}}{1 - D_1} \tag{5.5}$$

$$V_{DS(max)} = 4.2 + \frac{0.5x3}{0.5}$$

$$V_{DS(max)} = 7.2V + \%20 \text{ safety margin} = 8.6V$$

This value is calculated for CTP direction. So, when the cell is charging, the voltage and current levels to which the secondary switch is exposed vary. Therefore, the secondary peak current and voltage value become as below.

$$I_{s(peak)} = \frac{12x0.7}{5000x956x10^{-6}}$$

$$I_{s(peak)} \approx 1.75A$$

$$V_{DS(max)} = 16.8 + \frac{0.7x12}{0.3}$$

$$V_{DS(max)} = 44.8V + \%20 \text{ safety margin} = 53.75V$$

To use an approximation for the value of the output capacitor required, firstly, the voltage across the capacitor must be expressed. For the CTP and PTC direction, output voltage ripple is calculated in Eq. 5.6 and Eq. 5.7, respectively (Daniel, 2011).

$$\frac{\Delta V_{pack}}{V_{pack}} = \frac{D_1}{Rf_s C_s} \tag{5.6}$$

$$\frac{\Delta V_{cell}}{V_{cell}} = \frac{D_2}{Rf_s C_p} \tag{5.7}$$

Where C_s is the secondary side capacitor of the converter that it is output capacitor in CTP operation, C_p is the primary side capacitor of the converter that it is output capacitor in PTC operation. C_s is calculated is calculated as 680 uF by using Eq. 5.6. C_p is calculated as 2030 uF by using Eq. 5.7.

5.3. Proposed Balancing Control Strategy

In this section, a balancing strategy is proposed to minimize the total capacity loss caused by the inevitable energy losses due to CE, switching, and converter in ICB-based CTPTC balancing topologies. The design procedure of the proposed algorithm, consisting of cell selection algorithm and low-level control, is meticulously explained.

5.3.1. Proposed Cell Selection Algorithm

The proposed cell selection algorithm is designed to ensure the batteries are balanced simultaneously by using a minimum number of charge and discharge paths. Also, one of the basic principles of the proposed algorithm is to transfer all of the energy released by any cell to the low-charged cell without being sent to the pack. Therefore, using a minimum number of charge-discharge paths and full energy utilization is carried out by switching on the MOSFETs and transformer in the path of the relevant cell within the framework of specific rules.

The operating principle of the balancing circuit with the proposed cell selection algorithm will be described with a random selection of initial SOC for four cells as follows: $SOC_2<SOC_4<SOC_3<SOC_1$.

Initializing of balancing: Difference between SOC_{min} and SOC_{max} is greater than %5 the balancing process is started: ($SOC_1 - SOC_2 >$%5). SOC value of the cells are sorted from minimum to maximum. Then they are labeled as below.

Highest charged cell=$Cell_1$, $SOC_{(highest)}=SOC_1$

Lowest charged cell=$Cell_2$, $SOC_{(lowest)}=SOC_2$

Intermediate cell with highest charged, $SOC_{inter(highest)}= SOC_3$

Intermediate cell with lowest charged, $SOC_{inter(lowest)}= SOC_4$

State 1: At the beginning of the state, S_{1p} is turned on, and S_{1s} is turned off. $Cell_1$ is connected to the primary side of the first flyback converter, and $Cell_1$ begins to discharge. At the same time, S_{2s} is turned-on. All released energy by Cell1 is transferred to Cell2 through the secondary side to the primary side of the second flyback converter, as shown in Figure 5.3 (a). So, $Cell_2$ is charged. The primary and secondary MOSFETs of $Cell_4$ and $Cell_3$ are turned-off. So, SOC_4 and SOC_3 do not increase or reduce during this state.

State 2: In the second state, two different cases can occur.

Case 1: The first case is that if SOC_3 becomes equal to SOC_1 before SOC_4 becomes equal to SOC_2, S_{3p} is turned on, then $Cell_3$ begins to discharge. Briefly, S_{1p}, $S_{3p,}$ and S_{2s} are turned on, and all other MOSFETs are turned-off, as shown in Figure 5.3 (b). This means that $Cell_1$ and $Cell_3$ discharge, and $Cell_2$ continues to charge.

Case 2: The second case is that if SOC_4 becomes equal to SOC_2 before SOC_3 becomes equal to SOC_1 before, S_{4s} is turned on, then $Cell_4$ begins to charge. Briefly, S_{1p}, S_{2s}, and S_{4s} are turned on, and all other MOSFETs are turned-off, as shown in Figure 5.3 (c). This means $Cell_1$ continues to discharge, and $Cell_2$ and $Cell_4$ charge through to the related flyback converter.

State 3: In the third state, four different cases can occur according to the cases of State 2. If the first case appears in the state 2, two different cases can occur in state 3.

Case 1: The first is that SOC_4 becomes equal to SOC_3 before SOC_4 becomes equal to SOC_2, S_{4p} is turned on, then $Cell_4$ begins to discharge. Briefly, S_{1p}, S_{3p}, $S_{4p,}$ and S_{2s} are turned on, and all other MOSFETs are turned-off, as shown in Figure 5.3 (d). This means $Cell_1$, $Cell_3$, and $Cell_4$ discharge, and $Cell_2$ continues to charge.

Case 2: The second is that if SOC_4 becomes equal to SOC_2 before SOC_4 becomes equal to SOC_3 before, S_{4s} is turned on, then $Cell_4$ begins to charge.

Briefly, S_{1p}, S_{3p}, $S_{2s,}$ and S_{4s} are turned on, and all other MOSFETs are turned-off, as shown in Figure 5.3 (e). This means $Cell_1$ and Cell3 continue to discharge, and $Cell_2$ and Cell4 charge.

If the second case occurs in the state 2, two different cases can occur in state 3.

Case 3: The first is that SOC_3 becomes equal to SOC_1 before SOC_3 becomes equal to SOC_4, S_{3p} is turned on, then $Cell_3$ begins to discharge. Briefly, S_{1p}, S_{3p}, $S_{2s,}$ and S_{4s} are turned on, and all other MOSFETs are turned-off, as shown in Figure 5.3 (e). This means Cell1 and Cell3 discharge, Cell2 and Cell4 continue to charge.

Case 4: The second is that if SOC_3 becomes equal to SOC_4 before SOC_3 becomes equal to SOC_1 before, S_{3s} is turned on, then $Cell_3$ begins to charge. Briefly, S_{1p}, S_{2s}, S_{3s}, and S_{4s} are turned on, and all other MOSFETs are turned-off, as shown in Figure 5.3 (f). This means $Cell_1$ continues to discharge, and $Cell_2$, Cell $_3$, and $Cell_4$ charge.

Stopping of balancing: The difference between SOC_{min} and SOC_{max} is greater than %5 the balancing process is completed: ($SOC_1 – SOC_2$<%1).

The flowchart of the proposed cell selection algorithm is given in Figure 5.4.

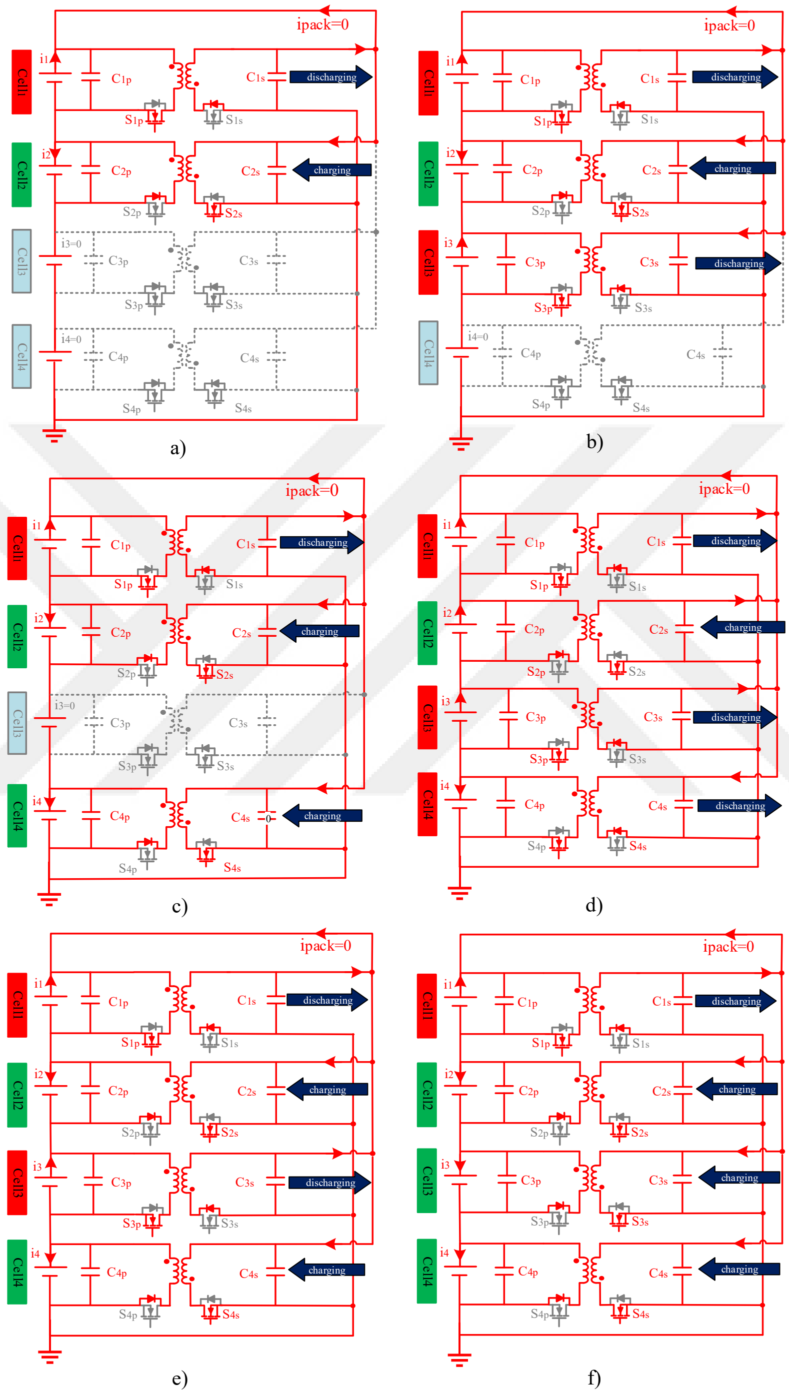


Figure 5.3. Operating states of balancing topology

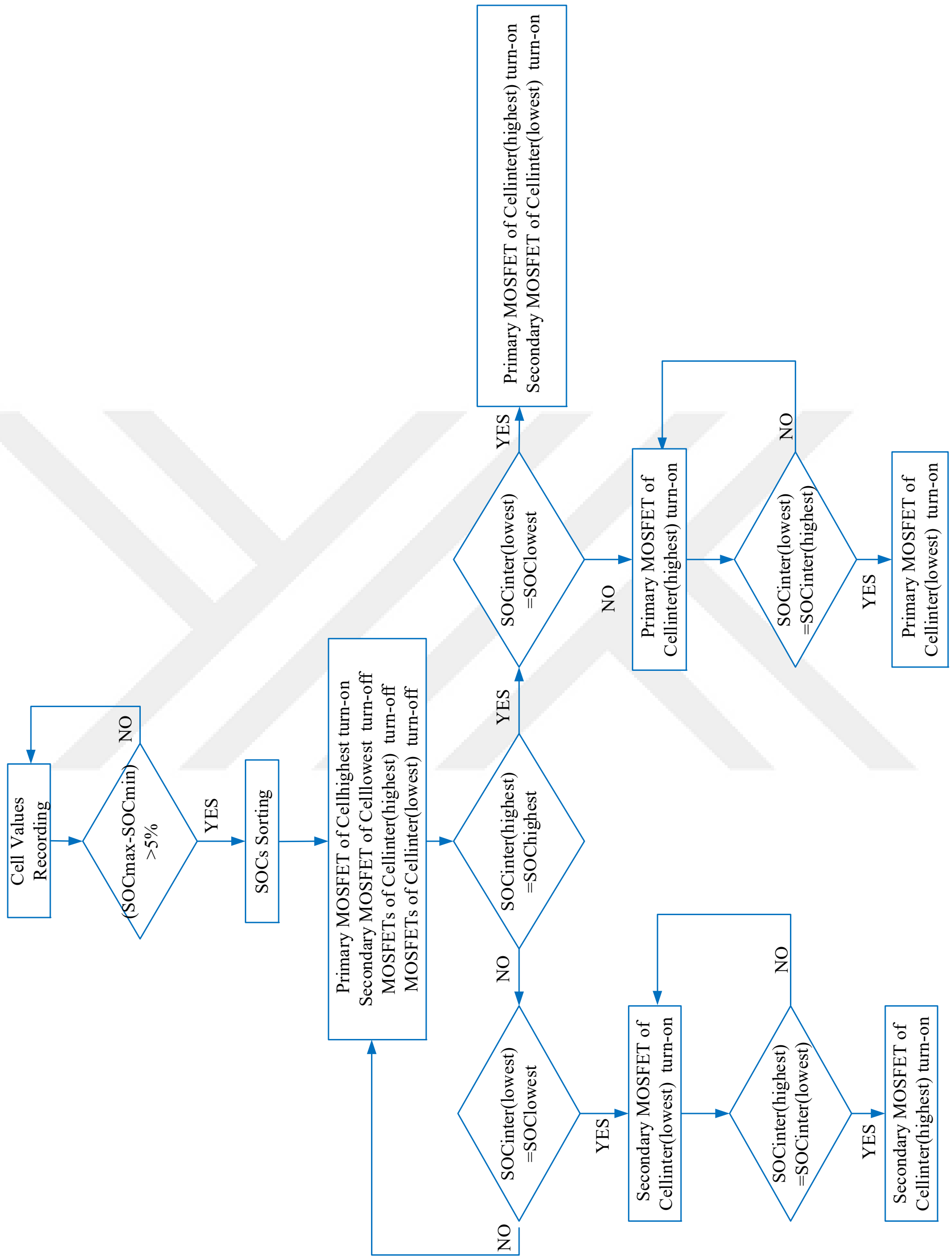


Figure 5.4. Flowchart of the proposed cell selection algorithm

5.3.2. Proposed Low-Level Controller

The proposed low-level controller adjusts the balancing current of each cell to ensure minimum balancing time and maximum utilization of releasable energy. Minimum balancing time is provided with all discharged cell(s) to be discharged with the maximum balancing current. The maximum utilization of releasable energy is ensured by keeping the pack current at zero at all operating states, so all released energy can be transferred to the low-charged cell.

The proposed low-level controller is a current tracking controller. It increases and decreases the on-time of the PWM signal sent to the MOSFETs by a specific value at each sample time to keep the current at the desired reference value. This is similar to PI control logic, but it does not need any control parameter or model of the balancing system. So, the proposed low-level controller is simple, easy to implement, and provides accurate current adjustment.

With this background of knowledge proposed current controller scheme provides two different references, current tracking controllers. One of them is implemented for keeping the current of related cell(s) at reference 1 A by adjusting the duty cycle of the PWM sent to the primary MOSFET(s) of the discharging cell(s), as shown in Figure 5.5 (a). The other is implemented for keeping the pack current at reference 0 A by adjusting the duty cycle of the PWM sent to the secondary MOSFET(s) of the charging cell(s), as shown in Figure 5.5 (b).

It is noted that the maximum allowable value of the average balancing current is determined as 1 A because of the charging current limitation and primary peak current limitation of the flyback converter.

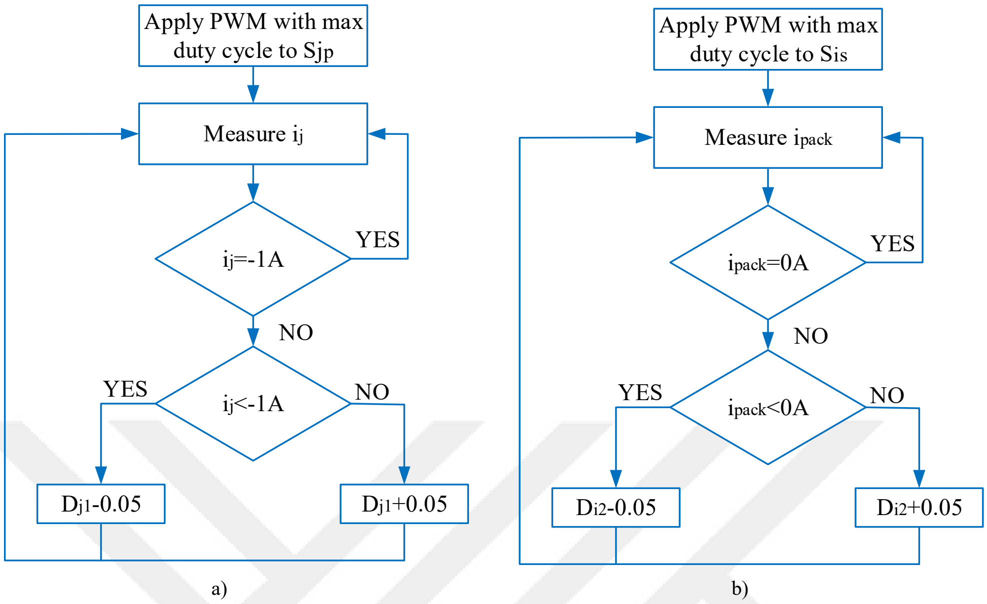


Figure 5.5. The proposed low-level controller scheme

5.4. Design of Power Circuit

In the scope of this thesis work, an experimental prototype of ICB- based CTPPTC active CBS with proposed BCS is designed and implemented. The implementation studies of the active cell balancing control system prototype are achieved in the Research Laboratory of Çukurova University Electrical and Electronics Engineering Department.

The simulation model is constructed in MATLAB/Simulink environment. The active CBS prototype design specifications are specified and validated by utilizing the simulation study results.

Power circuits and control systems are the two main components of an active CBS. The design processes for the power circuit, the selection of power components, the selection of suitable integrated circuits (ICs), and the design of the control system are introduced in depth in the following subsections.

5.4.1. Design of Flyback Converter Circuit

The main objective of this CBS prototype can be indicated as a functional ICB circuit with high performance and safe operation for ensuring CTPTC- based active balancing. The major part of the power circuit is the design of the bidirectional flyback converter. The implementation of the flyback converter is mentioned in section 5.2. The selection of the flyback transformer, which is a significant component is realized by using simulation results and considering calculated peak current, input voltage range, magnetization inductance, and turn ratio given in section 5.2. With this background of specifications, flyback transformer DA2034-AL from Coilcraft has been selected due to the lower cost and smaller footprint. DA2034-AL has been manufactured as four parallel connected primary windings and one secondary winding. The technical specifications of DA2034-AL are provided in Table 5.2.

Table 5.2. Technical specifications of DA2034-AL

Input voltage range	$I_{p(peak)}$	L_M at $I_{p(peak)}$	$L_{lk(p)}$	$L_{lk(s)}$	N_1/N_2
3V-300V	10A	9 uH	0.018Ω	1.75Ω	1:10

$L_{lk(p)}$ and $L_{lk(s)}$ are the leakage inductance of the primary and secondary sides, respectively. The magnetization inductance of 36 uH and a turn ratio of 5, determined by connecting the two primary windings, are connected in series. Then they are connected parallel to each other, are provided.

N-channel power MOSFET UF3710L-TQ2-R from UNISONIC TECHNOLOGIES has been selected due to having a lower cost, providing excellent $R_{DS(ON)}$ and operation lower gate voltages than the other switching components. Also, this MOSFET has been chosen considering the maximum $V_{DS(max)}$ calculations that the MOSFET can be exposed to in the bidirectional operation of the circuit. The technical specifications of UF3710L-TQ2-R are provided in Table 5.3.

Table 5.3. Technical specifications of UF3710L-TQ2-R

V_{DS}	I_D	$R_{DS(ON)}$	V_{GS}	Q_g
100V	57A	23 mΩ	10 V	130nC

The input and output capacitors are selected in light of calculations in Section 5.2.1.3. EEUTA1A222LB from Panasonic has been selected as the input (cell-side) capacitor. It is a film capacitor with a 10V voltage rating and a 2200 uF capacity rating. And EEUFC1E471 from Panasonic has been selected as the output (pack-side) capacitor. It is a film capacitor with a 25V voltage rating and a 470 uF capacity rating.

5.4.2. Design of Measurement Circuit

It is imperative to measure voltage and current signals sensitively to operate the CBS with high accuracy. The BCS of the balancing prototype measures eight signals, which are the voltages of four cells and currents of four cells.

Operational amplifiers (op-amps) are used to realize voltage measurement applications. Only the negative end of the first cell is connected to the ground directly. In light of this, the op-amp differential circuit is designed to measure individual cell voltage in a pack of series of connected cells. The cell voltage is measured by the LM358D operational amplifier from Texas Instrument. The utilized op-amp uses the 8-pin package, which reduces board size. LM358D consists of two independent op-amps and has the advantages of low input offset voltage and power drains appropriate for the operation of the battery. The technical specifications of LM358D are given in Table 5.4.

Table 5.4. Technical specifications of LMD358D

LM358D	
Supply voltage range	3-32 V
Input offset voltage	±2 mV at max. 25°C
DC voltage gain	100 dB

The constructed circuit schematic of the differential op-amp to measure the terminal voltage of the cell is illustrated in Figure 5.6. The first op-amp of LMD358D is used to get the difference, while the second is used to multiply it by the difference gain to bring it to the normal measuring range. Passive elements are selected so that the total gain of this circuit is set to 1.

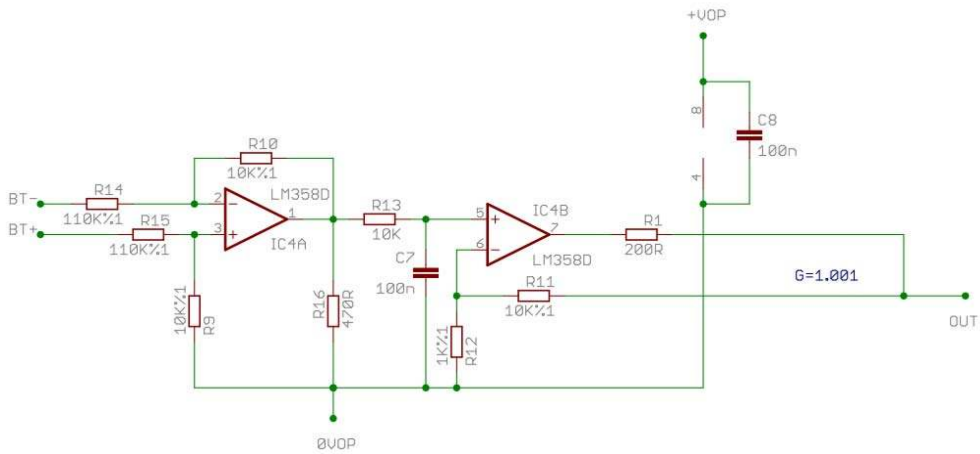


Figure 5.6. Circuit schematic of the differential amplifier to measure cell terminal voltage

To measure the cell current, ZXCT1107SA-7 high-side unipolar current sense monitor is utilized. The utilized IC uses the 3-pin package, is line powered, and does not need a separate supply rail. Cell current monitoring application two ZXCT1107SA-7 are used for measuring the current average magnitude and sign. One measures the positive current entering the positive end of the cell, and the other measures the negative current coming out of the positive end through a 1 Watt sensing resistance. These measurements are amplified with an LM358D op-amp IC, and then the difference between the outs of the op-amp is measured by a differential op-amp circuit. The constructed circuit schematic of the overall circuit to measure the average current through a cell is illustrated in Figure 5.7.

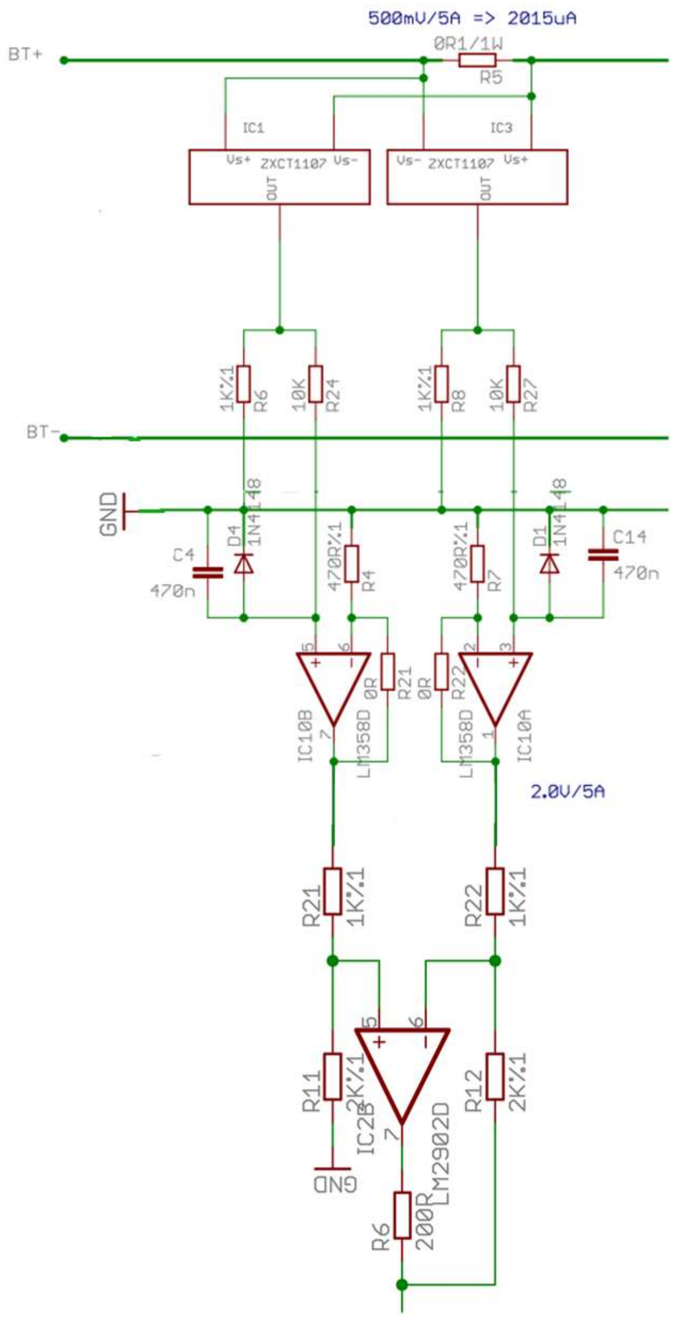


Figure 5.7. Circuit schematic of ZXCT1107SA-7 to measure average cell current

5.4.3. Design of FET Driver Circuit

The TLP250 from TOSHIBA is a MOSFET driver output optocoupler IC that has been used for triggering the gate of the power MOSFETs. It consists of a GaAlAs light emitting diode and an integrated photodetector. This optocoupler IC has isolation against voltages up to 2.5kV. The technical specifications of TLP250 are summarized in Table 5.5.

Table 5.5. Technical specifications of TLP250

TLP250	
Supply voltage range	10-35 V
Supply current	11 mA (max.)
Output current	±1.5 A (max.)
Switching time	1.5 us

The design procedure is straightforward, which can be attained from the application notes and datasheet of the TLP250. Any extra component is not required, so the driver circuit simplicity is achieved. Only for the stable supply voltage a B0515LM-1W DC-DC converter with 5-15V input-output voltage is utilized. The constructed power circuit schematic of the bidirectional flyback converter, which consists of the transformer, snubber circuits, and MOSFET driver circuits, is illustrated with the pin configuration in Figure 5.8.

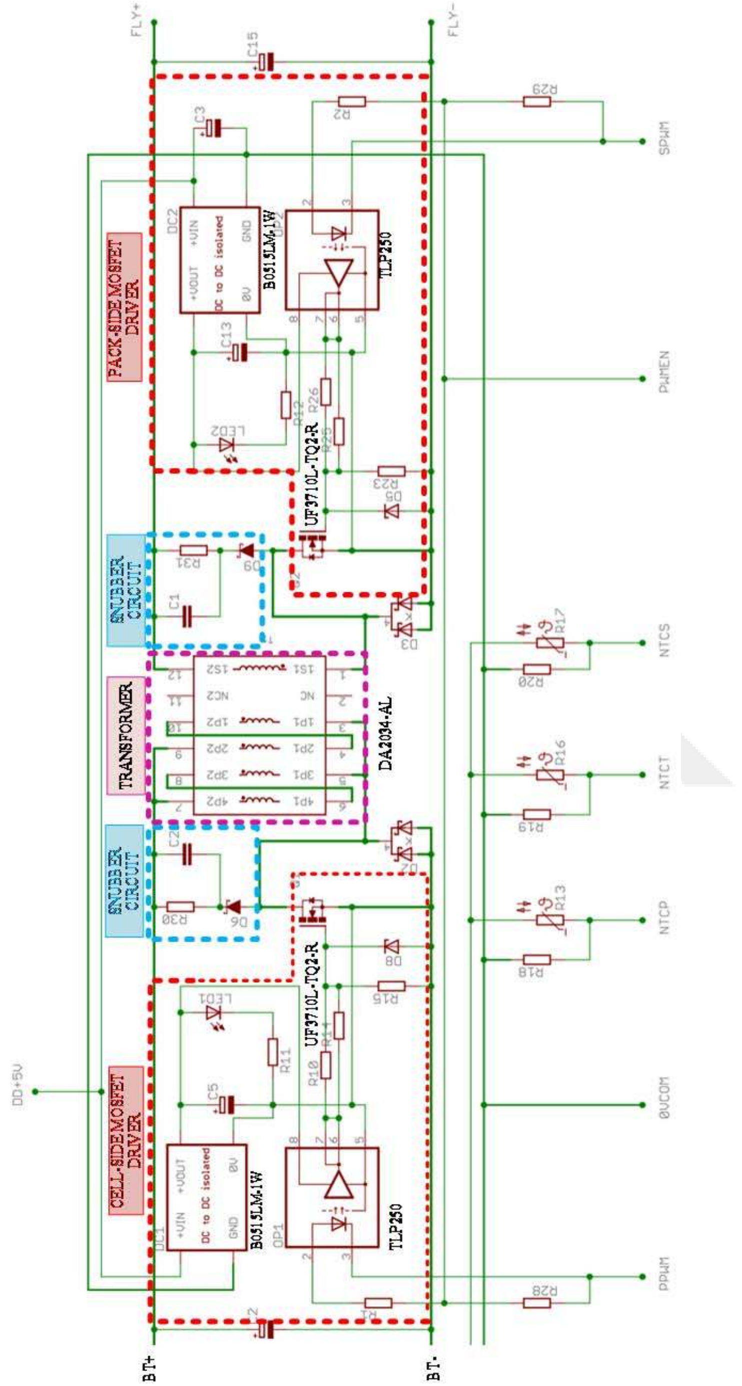
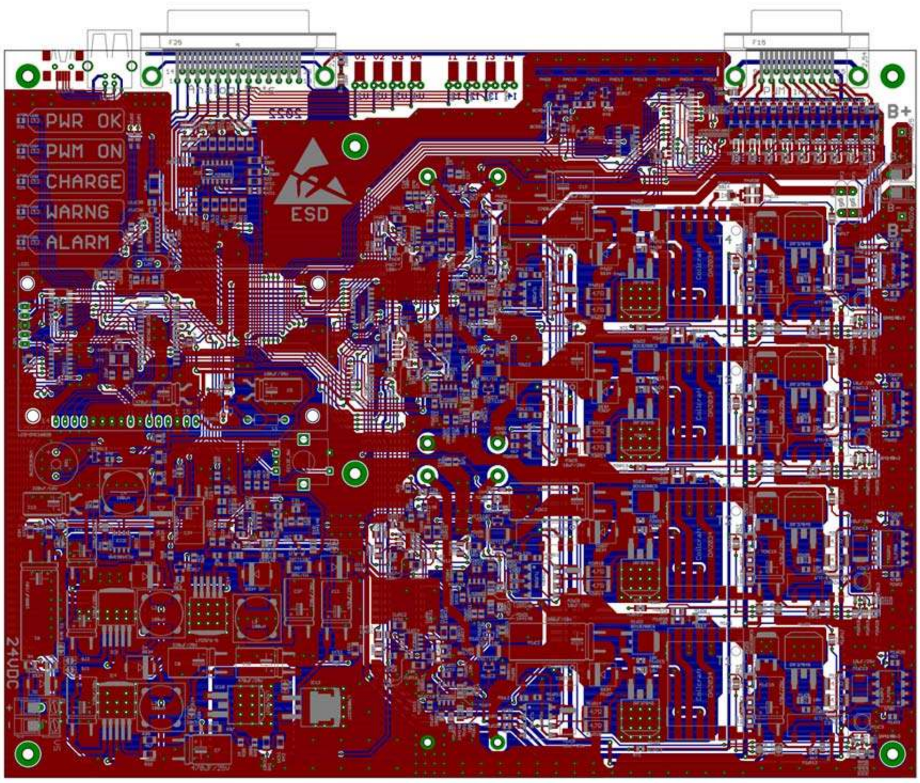


Figure 5.8. Circuit schematic of constructed bidirectional flyback converter

5.4.4. Hardware Implementation of the Power Circuit

The power circuit of the multiple flyback converter-based CTPTC active balancing prototype is implemented with a PCB. The control part includes measurement circuits, protection circuits, and gate driver circuits. The PCB design of the active balancing board has been performed using a PCB design software tool. The 2-D layout view, a view of the designed PCB board attained from PCB design, is shown in Figure 5.9. (a)-(b). The board is designed with two layers utilizing surface mount technology. The view of the constructed prototype is provided in Figure 5.10 by enumerating the main components.



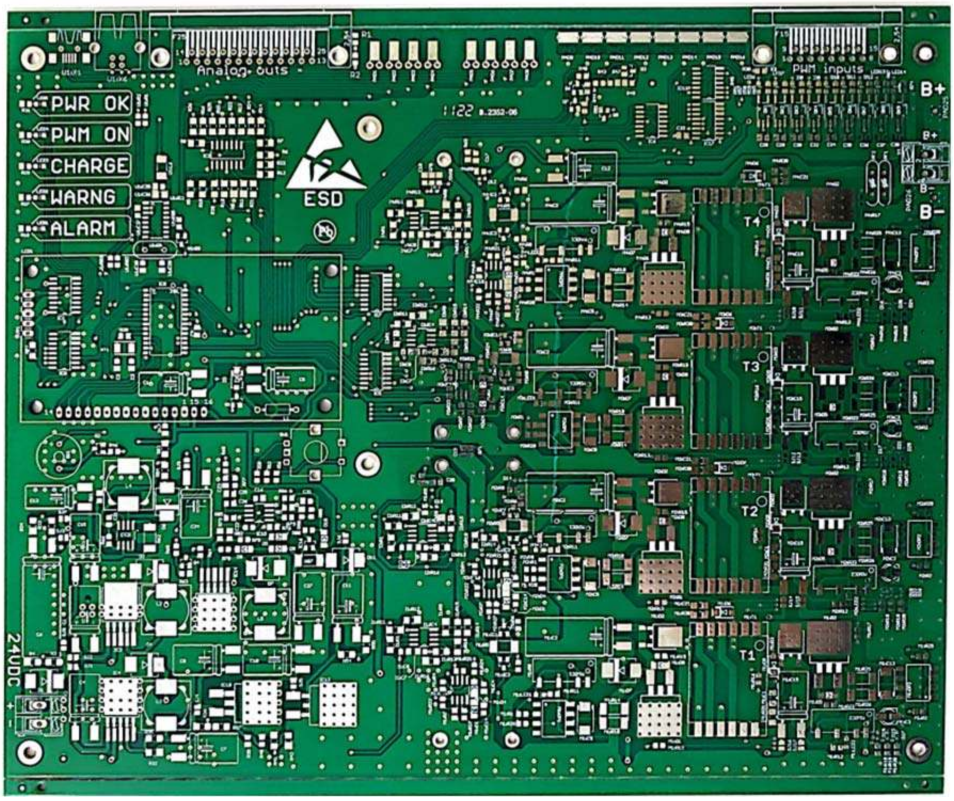


Figure 5.9. (a) The 2-D layout (b) The view of designed PCB board

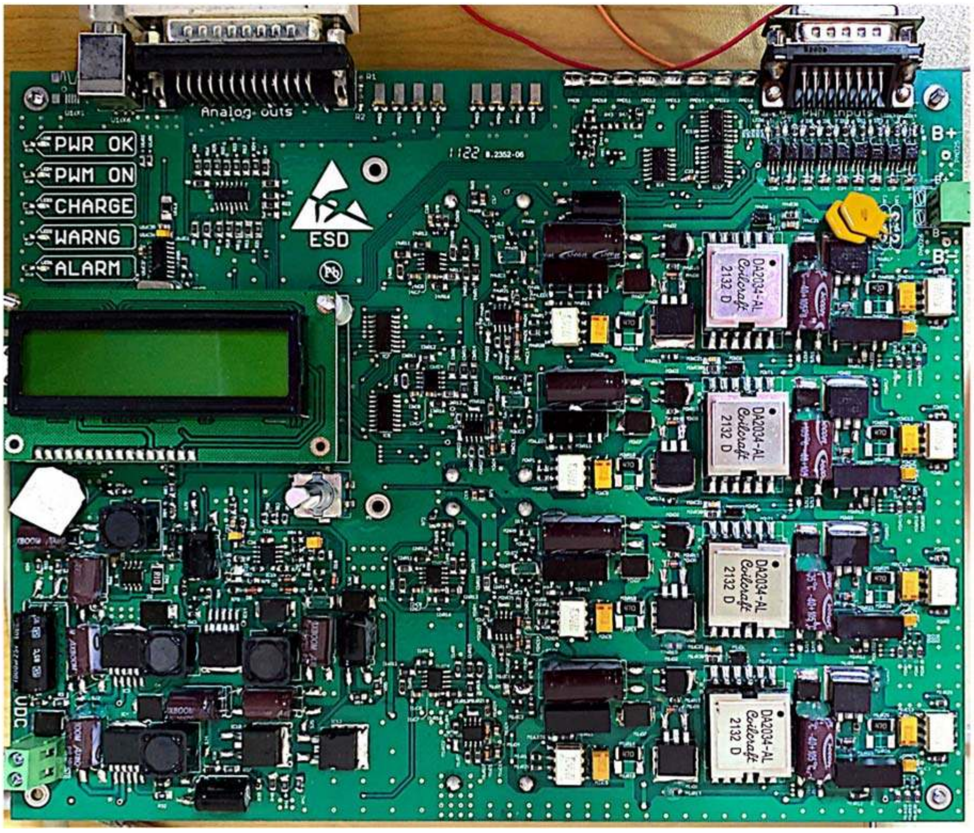


Figure 5.10. View of the constructed prototype

5.5. Simulation Model of Proposed CTPTC Active Cell Balancing System

Simulation of the improved active cell balancing system is conducted by employing the MATLAB/Simulink simulation program. The modeled battery cell and the components selected in the design of the flyback converter in Section 5.2 are injected into the designed simulation study. This made the simulation study very close to the real system. The response of the developed BCS in the balancing system is observed, and it is predicted that the expected performance could be obtained in the experimental studies. To validate the presented BCS, severe initial imbalance condition is executed. In this case, the measurements taken revealed the superiority of the proposed active cell balancing system.

5.5.1. Validation of Battery Cell Model

To evaluate the robustness of the created active cell balancing system, an accurate cell model is a crucial issue. Therefore, in all stages of this thesis, the Panasonic NCR18650B type li-ion battery cell is used. Specification of the NCR18650B li-ion cell is given in Table 5.6.

Table 5.6. Specification of Li-ion battery cell

Panasonic NCR18650B	
Nominal Voltage	3.6 V
Maximum Charge Voltage	4.2 V
Rated Capacity	3200 mAh

While obtaining the model of the cell, the discharge test is performed to obtain the cell terminal voltage, and the open circuit test is performed for the SOC-OCV relationship. With the obtained experimental data, the SOC-OCV characteristic of the cell can be obtained. Afterward, the 2nd order RC Thevenin electrical ECM of the battery cell is deduced. These modeling steps were performed rigorously to represent the SOC-OCV curve of the NCR18650B battery cell (Muratoğlu and Alkaya, 2019). The obtained SOC-OCV curve of the cell with the curve-fitting method is given in Figure 5.11, and the model is defined as a sixth-degree polynomial as below.

$$\begin{aligned} f(U_{ocv}, SOC) &= 16.07SOC^6 - 43.57SOC^5 + 37.89SOC^4 \\ &-5.85SOC^3 - 7.59SOC^2 + 4.41SOC + 2.8 \end{aligned} \tag{5.8}$$

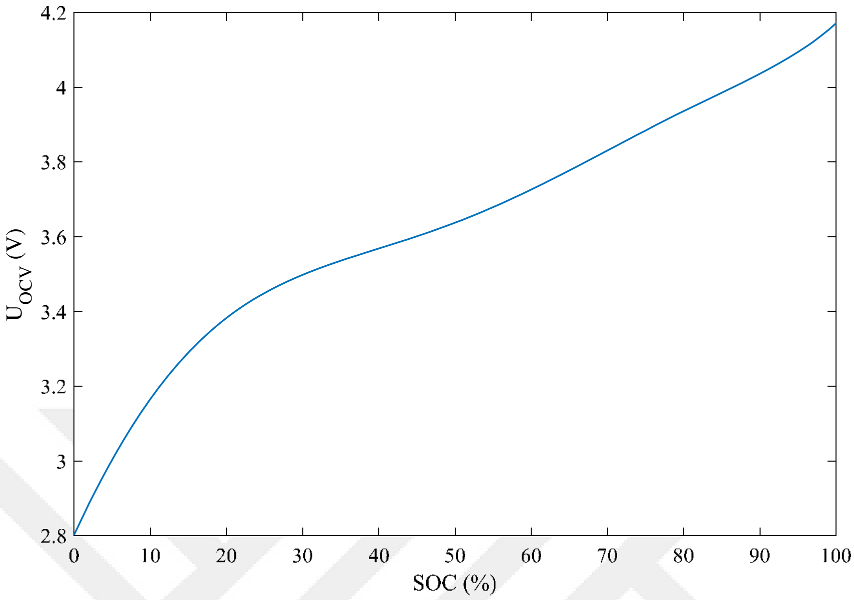


Figure 5.11. SOC-OCV curve of li-ion battery cell

The ECM parameters obtained as a result of parameter estimation were determined as follows.

$$
\begin{aligned}
R_0 &= 2.2236.e^{-33.8871.SOC} + 0.016 \\
R_1 &= 0.000124.e^{-25.0869.SOC} + 0.1656 \\
C_1 &= 738.6083.e^{-11.6207.SOC} + 690.5780 \\
R_2 &= 44.6259.e^{-333.6240.SOC} + 0.0257 \\
C_1 &= 6191.5.e^{-10.6698.SOC} + 4470.1
\end{aligned}
\tag{5.9}
$$

To use the battery model in the simulation study of CBS, capacitor and resistance values must be determined as an electrical component. The value of the capacitors and resistors, which vary depending on SOC, are modeled in the Simscape toolbox of Simulink, as demonstrated in Figure 5.12.

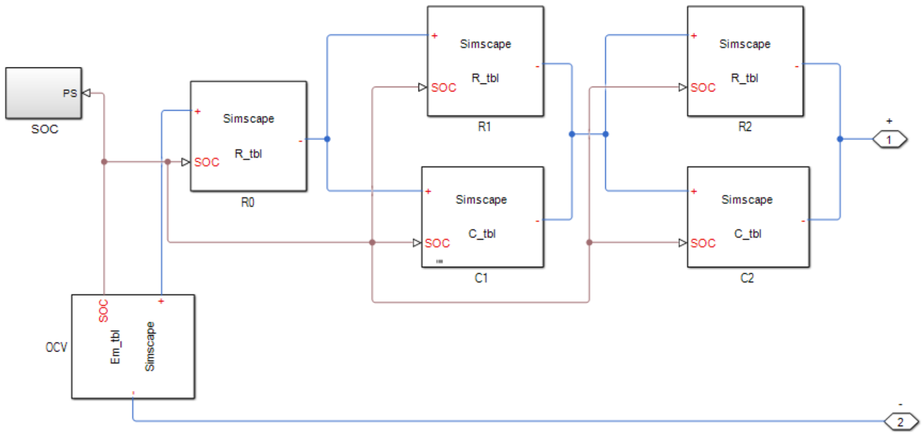


Figure 5.12. Simscape model of the li-ion battery cell

5.5.2. Simulation Results

The presented CBS is simulated to perform the performance evaluation. The performance of the developed CBS is measured under

the standby condition that batteries are not being charged or discharged from an external source or load. In other words, it is the case when there is only a balancing current in the circuit. The realization of the accurate balancing with any BCS in the standby condition means that it also will realize in the charging or discharging condition, too. The main power circuit parameters of the proposed system are tabulated in Table 5.7.

Table 5.7. Main balancing circuit parameter

Parameter	**Value**
Cell side capacitor	2020uF
Pack side capacitor	470 uF
Switching frequency	5 kHz
Magnetization inductance	36 uH
Primary side leakage inductance	0.69 uH
Secondary side leakage inductance	15.6 uH

In general, it can be said that the initial SOC difference above 20% means a severe cell imbalance. In this section, the performance results of the proposed BCS at 35 % initial SOC difference with four cells are presented. The battery cells' current should be maintained in (−1A, 1A). The initial SOC of each cell is 55%, 68%, 90%, and 78%, respectively. The bound of acceptable difference SOC of the cell is ΔSOC_{min} =1 %.

When results are examined, the proposed BCS made the decision to apply the maximum balancing current to $Cell_3$, which is the cell with the highest charge during the entire balancing process. The balancing current of $Cell_3$ oscillates around -1 A reference value. Until 1234 s, all released energy by $Cell_3$ is transferred to $Cell_1$, with the lowest SOC. During this time interval, relevant MOSFETs of $Cell_2$ and $Cell_4$ are turned off, and the pack current is kept at 0 A. Balancing current of $Cell_2$ and $Cell_4$ are 0 A. The average current through $Cell_1$ is measured as 0.65 A. The primary side current of each flyback converter at this time interval is shown in Figure 5.13. At 1234 s, $Cell_4$ begins to discharge; it charges $Cell_1$ with $Cell_3$ until 1841 s. In this time interval, the balancing current of $Cell_4$ and $Cell_3$ oscillates around -1 A, the current of $Cell_1$ oscillates at 1 A, and the current of $Cell_2$ remains at 0 A. At 1841 s, $Cell_2$ begins to charge. $Cell_3$ and $Cell_4$ charge $Cell_1$ and $Cell_2$ until the end of the balancing. In this time interval, the balancing current of $Cell_4$ and $Cell_3$ oscillates around -1 A, and $Cell_1$ and $Cell_2$ oscillate at 0.54 A. The obtained results are observed from the current graphic of cells is shown in Figure 5.14.

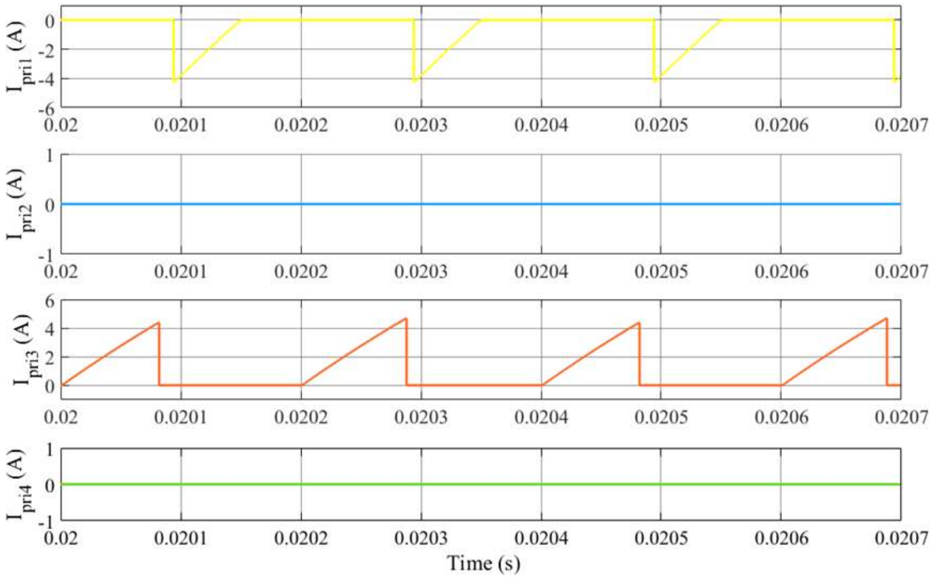


Figure 5.13. Primary side current of flyback converter when $Cell_3$ discharging and $Cell_1$ charging

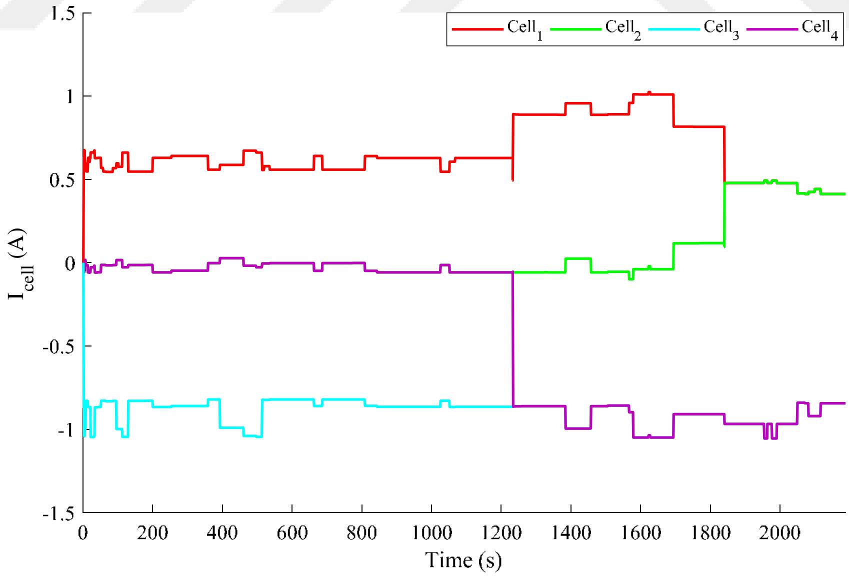


Figure 5.14. The current graphs of the proposed BCS at the severe initial imbalance

When the SOC change of the cells is investigated, it is seen that the repeated charged/discharge cycles are eliminated completely. The SOC profile of cells is shown in Figure 5.15. The result shows that the balancing process is completed at 2048 s. And it is clearly seen that the maximum SOC imbalance at the end of balancing is below 1%.

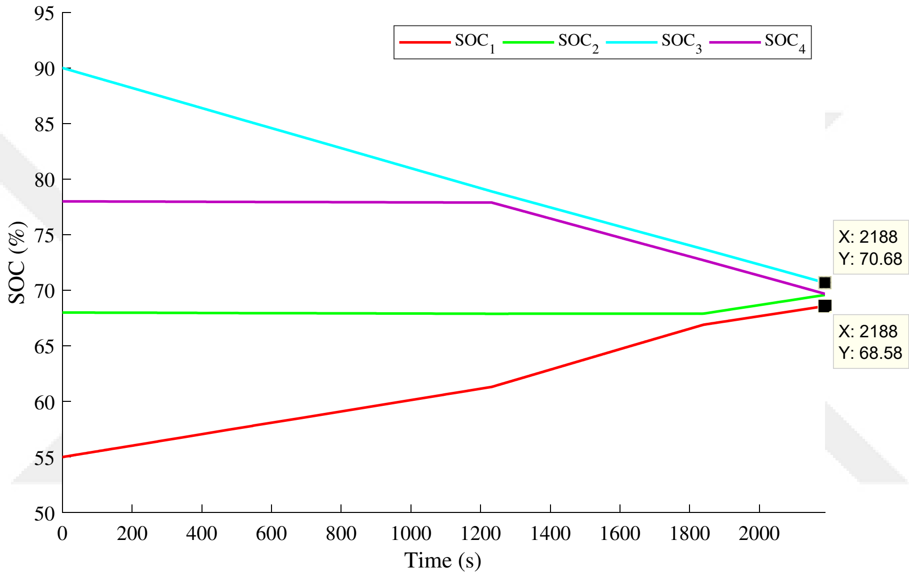


Figure 5.15. SOC graphs of the proposed BCS at the severe initial imbalance

Also, the terminal voltage of cells is measured simultaneously, as demonstrated in Figure 5.16. The measured average SOC (SOC_{avg}) of the battery cells is shown in Figure 5.17. SOC_{avg} has declined from 72.75 % to 69.63 %. It can be concluded that the SOC loss of the balancing system is 3.12 %.

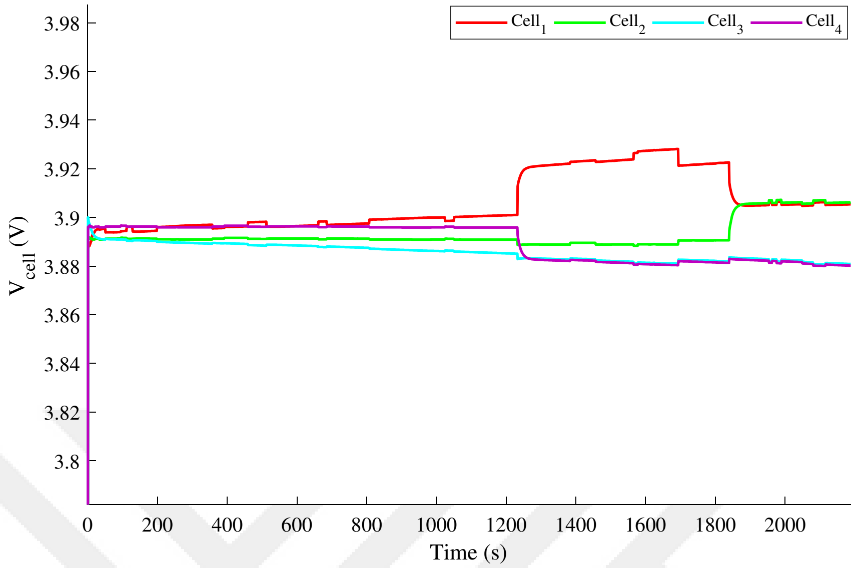


Figure 5.16. Terminal voltage graphs of the proposed CTPTC BCS at severe initial imbalance

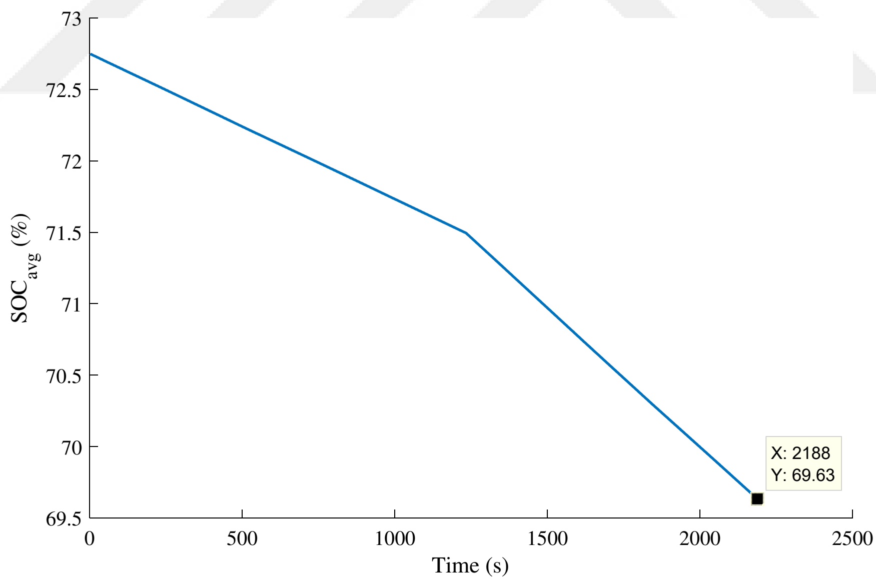


Figure 5.17. SOCavg change of the proposed BCS at the severe initial imbalance

5.6. Experimental Setup

In this thesis, the software of the system is performed by the dSPACE, which is powerful for real-time validation of the control algorithms. The real-time code for the controller board is generated and subsequently built by dSPACE using its real-time interface (RTI) implementation software. Some of the critical attributes of the dSPACE are summarized as: the direct interface of Simulink models, automatically generated controller code produced for hardware circuit, and simple graphical user interface for ease of operation.

A fully functional real-time control system, the dSPACE DS1104 R&D controller board is built around a 250MHz, 603 PowerPC floating point processor. In addition, the board has a slave-DSP subsystem for enhanced I/O based on the TMS320F240 DSP microcontroller. The technical specifications of the dSPACE DS1104 R&D controller board are given in Table 5.8. The interfacing unit CLP1104 Connector/LED Combi Panel provides a connection between the controller board and the constructed balancing circuit to be connected to the processor. Additionally, this panel has a series of LEDs that show the statuses of the digital signals sent to the hardware. The balancing control algorithm is developed in Simulink and executed using the dSPACE DS1104 controller board. For this purpose, RTI blocks provided by the implementation software of dSPACE are ensured to embed in the Simulink simulation model.

On the other hand, ControlDesk provides control and monitoring of experiments, recording experimental data, and stopping the real-time application. Further, it enables to access any I/O signals linked to the hardware components. The synoptic scheme of the experimental setup is illustrated in Figure 5.18.

Table 5.8. Technical specifications of dSPACE DS1104 R&D controller board

Parameter		**Specifications**
Memory	Global Memory	32 MB SDRAM
	Flash Memory	8MB
A/D converter	Channels	4 multiplexed channels (1x16-bit)
		4 parallel channels (4x12-bit)
	Resolution	Multiplexed channels: 16 bit
		Parallel channels: 12 bit
	Input Voltage Range	±10 V
	Offset Error	±5 mV
	Gain Error	Multiplexed channels: ±0.25 %
		Parallel channels: ±0.5 %
D/A converter	Channels	8 channels
	Resolution	16 bit
	Output Voltage Range	±10 V
	Offset Error	±1 mV
	Gain Error	±0.1 %
Digital I/O	Channels	20-bit parallel I/O Single bit selectable for input or output
	Voltage Range	TTL input/output levels
Slave DSP	Type	Texas Instruments TMS320F240 DSP
		16-bit fixed-point processor
	I/O channels	10 PWM outputs
		4 capture inputs
		1 serial peripheral interface
	Memory	64Kx16 external code memory
		28Kx16 external data memory
		4Kx16 dual-port memory for communication
		32KB flash memory

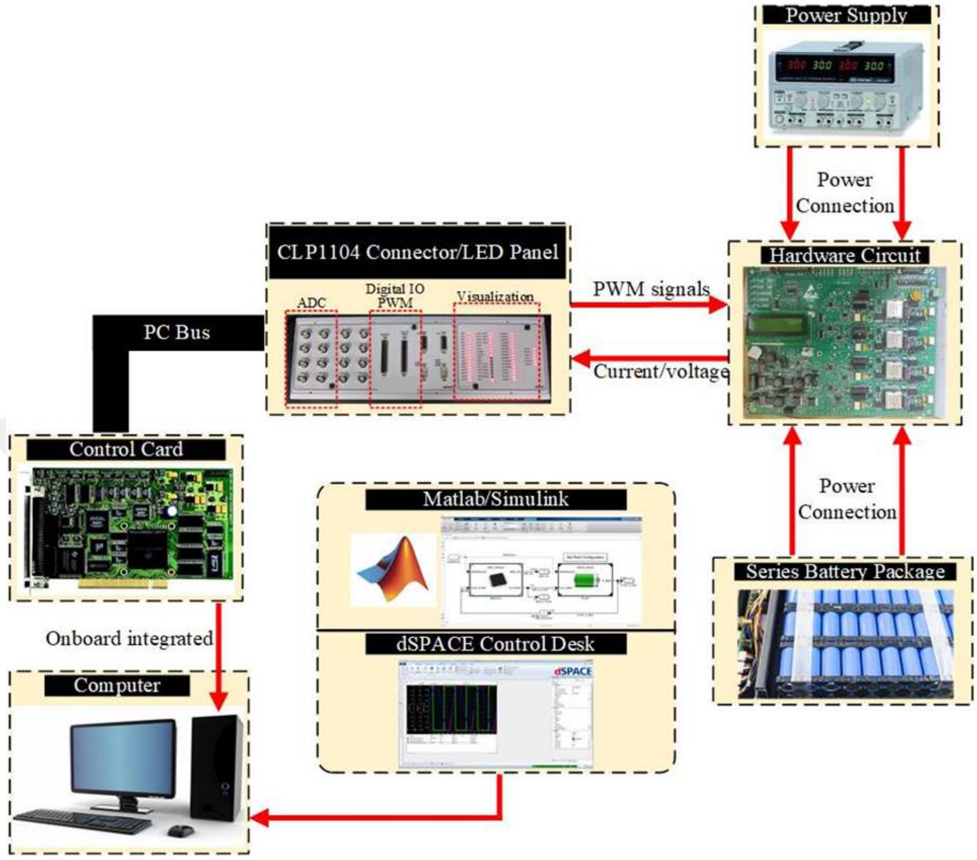


Figure 5.18. Synoptic scheme of the experimental setup

The constructed prototype needs a 24V constant supply voltage. TT-T-ECHNI-C power supply is used to provide a constant voltage to the circuit. Also, the balancing control system has been tested when cells are in charging condition. In the prototype, there is an onboard charger circuit with an output of a maximum of 1650 mA current. The charging current is adjusted with an external PWM signal sent from the signal generator. For providing a 1C charging current, the duty cycle of the PWM signal is set to 1.

Measurement of cell voltages and cell currents is essential for utilizing the UKF method for SOC estimation, designed BCS, and protection of the overall system. And ADC channels of the dSPACE are used to measure cell currents and voltages. Monitoring the measurements is ensured by ControlDesk software of the dSPACE and LCD panel on the constructed prototype. Also, all measurements have been recorded as (.mat) file.

The view of the experimental set-up in the laboratory is demonstrated in Figure 5.19.

Figure 5.19. The view of the experimental set-up

5.7. Experimental Results

In this section, the proposed BCS for the constructed prototype of active cell balancing is validated through case studies. A definition of balanced corresponds when the SOCs of all battery cells are within a 1% margin in this thesis work. But, it must be noted that SOC is more difficult to estimate with high precision, which is not the focus of this thesis. To obtain meaningful SOC value sampling period is set to 2 seconds. The cases are performed to test the accuracy of the balancing control with the proposed BCS at standby condition with different initial SOC imbalances and charging condition. During the balancing process, the SOC profile of the cells, the voltage and current of the cells, and the total SOC loss were measured.

5.7.1. Standby Condition

Standby condition is the state of batteries not being charged or discharged from an external source. In other words, it is the case when there is only a balancing current in the circuit. The realization of the accurate balancing with any BCS in the standby condition means that it also will realize in the charging or discharging condition, too.

5.7.1.1. Severe Initial Imbalance Condition

In general, it can be said that the initial SOC difference above 20% means a severe cell imbalance. In this section, the performance results of the proposed BCS at 35 % initial SOC difference with four cells are presented. The initial SOC of each cell is 55%, 69%, 90%, and 77.6%, respectively. When results are examined, the proposed BCS made the decision to apply the maximum balancing current to $Cell_3$, which is the cell with the highest charge during the entire balancing process. The balancing current of $Cell_3$ oscillates around -1A reference value. Until 1360 s, all released energy by $Cell_3$ is transferred to $Cell_{1,}$ with the lowest SOC. During this time interval, relevant MOSFETs of $Cell_2$ and $Cell_4$ are turned off, and the pack current is kept at 0 A. Balancing current of $Cell_2$ and $Cell_4$ are 0 A. The balancing current $Cell_1$ is measured as 0.67 A. At 1360 s, $Cell_4$ begins to discharge; it charges $Cell_1$ with $Cell_3$ until 1928 s. In this time interval, the balancing current of $Cell_4$ and $Cell_3$ oscillates around -1A, the current of $Cell_1$ oscillates at 0.95 A, and the current of $Cell_2$ remains at 0 A. At 1928 s, $Cell_2$ begins to charge. $Cell_3$ and $Cell_4$ charge $Cell_1$ and $Cell_2$ until the end of the balancing. In this time interval, the balancing current of $Cell_4$ and $Cell_3$ oscillates around -1 A, and $Cell_1$ and $Cell_2$ oscillate at 0.68 A. The obtained results are observed from the current graphics of cells, which are shown in Figure 5.20.

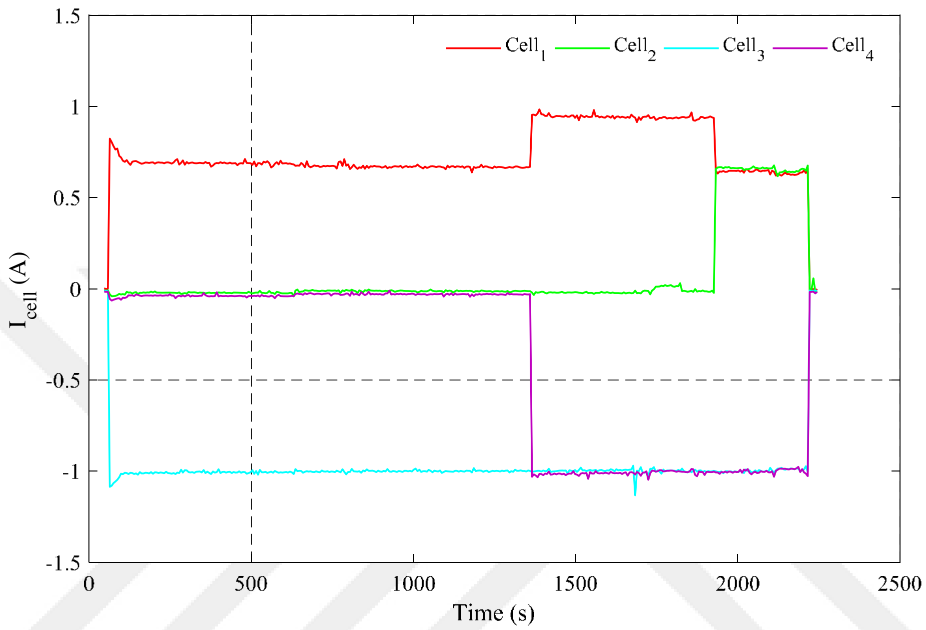


Figure 5.20. The current graphs of the CTPTC balancing with the proposed BCS at the severe initial imbalance

When the SOC change of the cells is investigated, it is seen that the repeated charged/discharge cycles are eliminated completely. The SOC profile of cells is shown in Figure 5.21. The result shows that the balancing process is completed at 2245 s. And it is clearly seen that the maximum SOC imbalance at the end of balancing is below 1%.

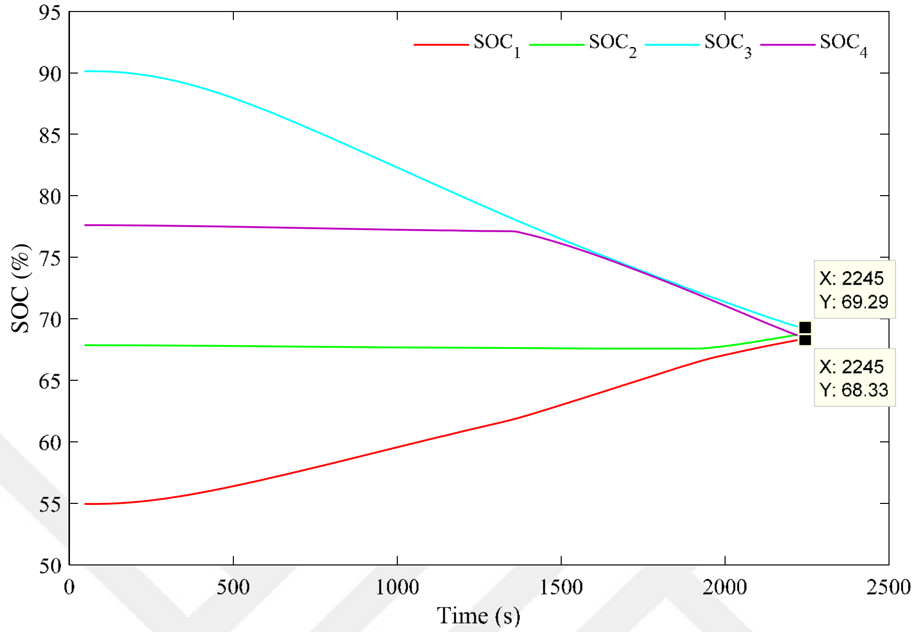


Figure 5.21. SOC graphs of the CTPTC balancing with proposed BCS at the severe initial imbalance

Also, the terminal voltage of cells is measured by ADC channels of dSPACE simultaneously. The results show that the voltage imbalance from 0.36 V at the beginning is reduced to the 0.12 V range, as demonstrated in Figure 5.22.

The measured SOC_{avg} change of the battery cells is shown in Figure 5.23. SOC_{avg} has declined from 72.64 % to 68.73 %. It can be concluded that the SOC loss of the balancing system is 3.91 %.

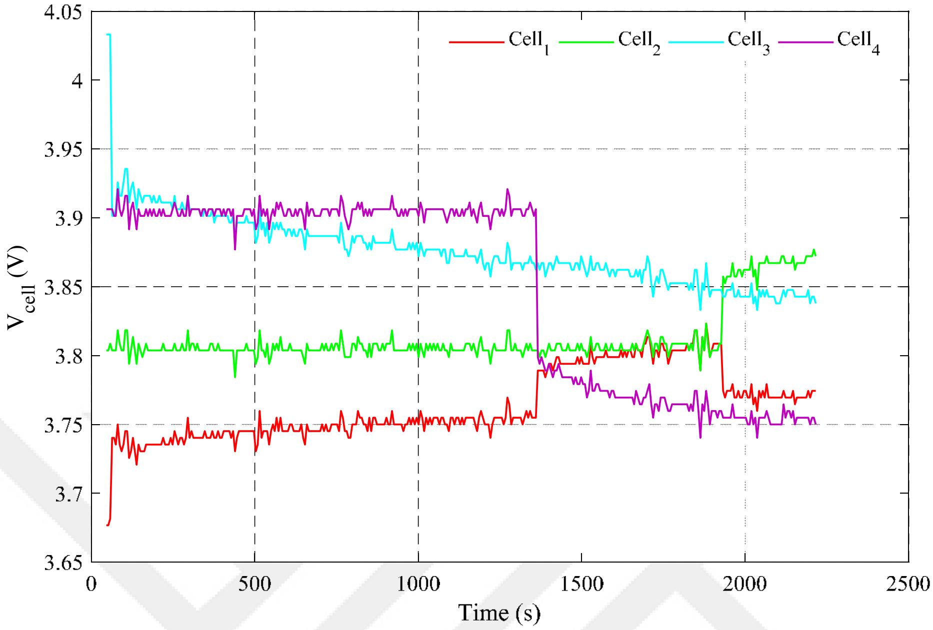


Figure 5.22. Terminal voltage graphs of the CTPTC balancing with proposed BCS at the severe initial imbalance

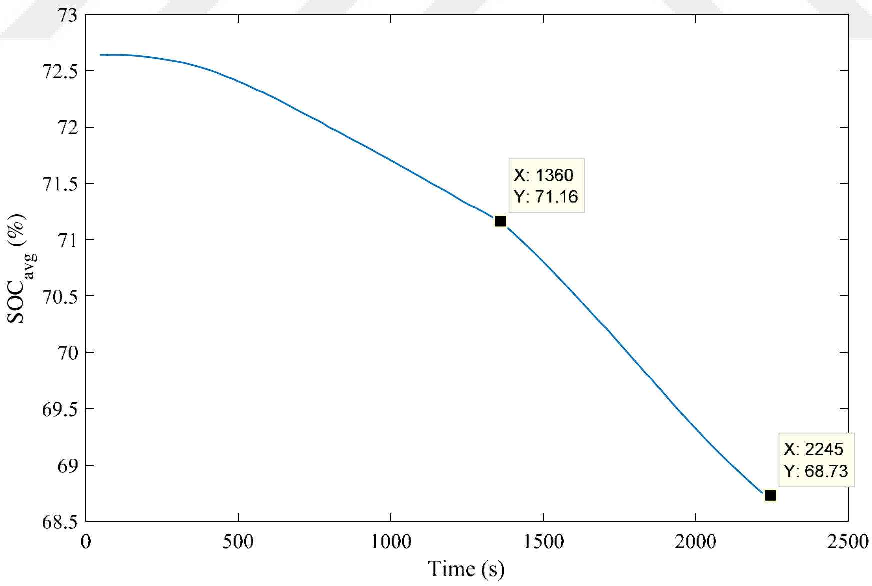


Figure 5.23. SOC_{avg} loss of the CTPTC balancing with proposed BCS at the severe initial imbalance

To verify the contribution of the proposed BCS to the balancing efficiency, balancing with an initial SOC with a similar SOC_{avg} value was performed with the mean-difference algorithm. Initial SOC values of each cell are 57.6%, 67.4%,89.85%, and 76.1%, respectively. From here, it is seen that the initial SOC difference is 32.25, and the initial SOC_{avg} value is 72.73. The SOC profile of cells is shown in Figure 5.24. It is clearly concluded that balancing is completed in 2025 s. This balancing time is a little shorter than the balancing process with the proposed BCS. This arises from the difference between their initial SOC differences.

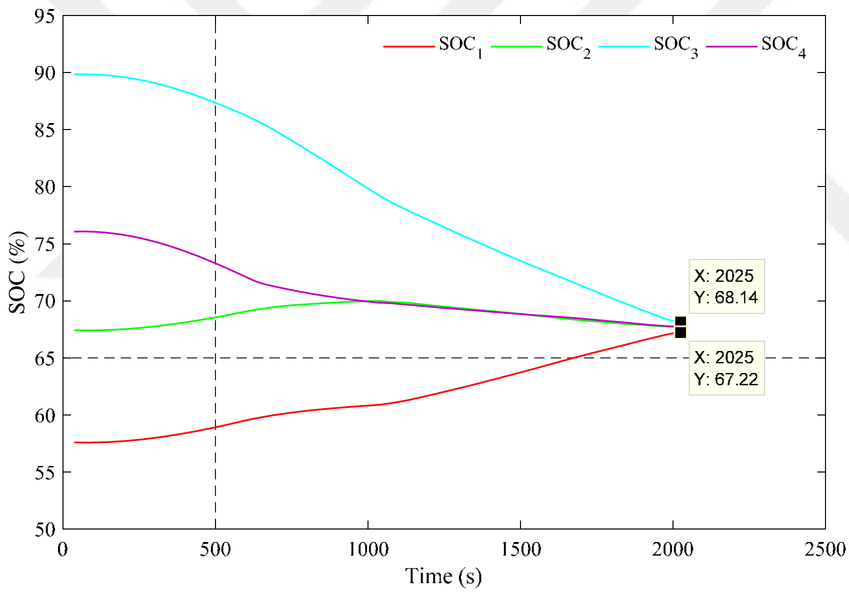


Figure 5.24. SOC graphs of the CTPTC balancing with mean-difference-based BCS at the severe initial imbalance

The measured SOC_{avg} change of the battery cells is shown in Figure 5.25. SOC_{avg} has declined from 72.73 to 67.7. It can be concluded that the SOC loss of the balancing system is 5.03 %. It is deduced that the overall balancing efficiency with the proposed BCS is 22.2% higher than that of the mean-difference algorithm.

A detailed comparison of performance results of the CTPTC balancing with proposed BCS and mean-difference-based BCS is given in Table 5.9.

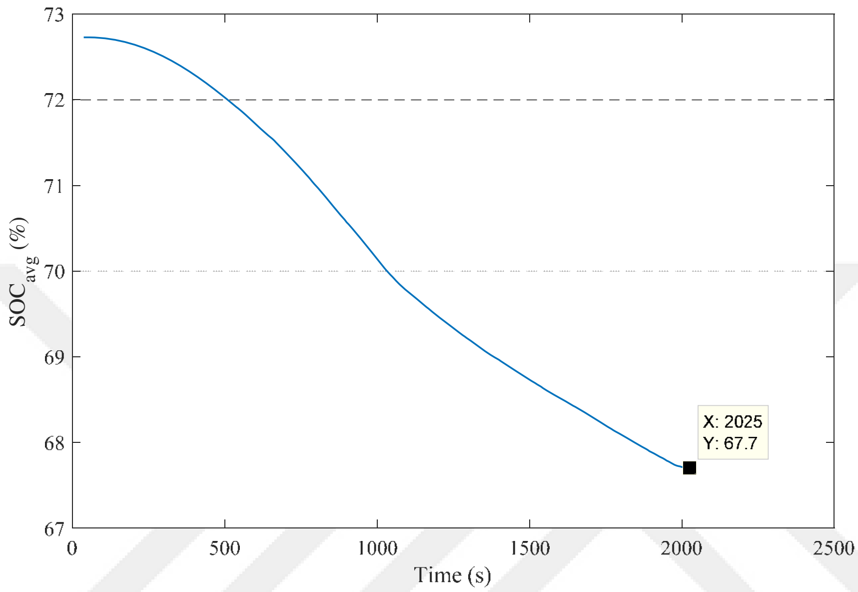


Figure 5.25. SOCavg loss of the CTPTC balancing with mean-difference-based BCS at the severe initial imbalance

Table 5.9. Comparison of the CTPTC and CTP active balancing

Balancing Topology	**Control strategy**	**Max. SOC difference at initial**	**Total balancing time**	**Initial SOC_{avg}**	**SOC_{avg} loss**	**SOC_{avg} loss (%)**
CTPTC	Mean-difference BCS	32.25	2025s	72.73	5.03	6.92
CTPTC	Proposed BCS	35	2245s	72.64	3.91	5.38

5.7.1.2. Smooth Initial Imbalance Condition

The performance results of the proposed BCS are tested at 16.6 % initial SOC difference with four cells presented. The initial SOC of each cell is 69.7%, 85.6%, 86.3%, and 71.6%, respectively. When results are examined, the proposed BCS made the decision to apply the maximum balancing current to $Cell_3$, which is the cell with the highest charge during the entire balancing process. The balancing current of $Cell_3$ oscillates around -1 A reference value. Until 152 s, all released energy by $Cell_3$ is transferred to $Cell_1$, which is with the lowest SOC. During this time interval, relevant MOSFETs of $Cell_2$ and $Cell_4$ are turned off, and the pack current is kept at 0 A. Balancing current of $Cell_2$ and $Cell_4$ are 0 A. The balancing current $Cell_1$ is measured as 0.7 A. At 152 s, $Cell_2$ begins to discharge; it charges $Cell_1$ with $Cell_3$ until 476 s. In this time interval, the balancing current of $Cell_2$ and $Cell_3$ oscillates around -1 A, the current of $Cell_1$ oscillates around 0.93 A, and the current of $Cell_4$ oscillates around 0 A. At 476 s, $Cell_4$ begins to charge. $Cell_2$ and $Cell_3$ charge $Cell_1$ and $Cell_4$ until the end of the balancing. In this time interval, the balancing current of $Cell_4$ and $Cell_3$ oscillates around -1 A, and $Cell_1$ and $Cell_2$ oscillate at 0.65 A. The obtained results are observed from the current graphic of cells is shown in Figure 5.26.

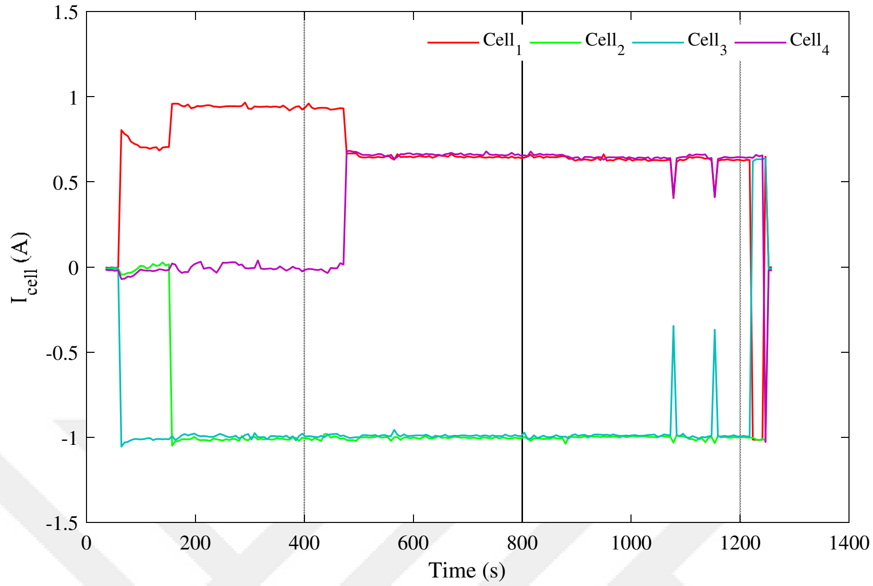


Figure 5.26. The current graphs of the proposed CTPTC BCS at the smooth initial imbalance

When the SOC change of the cells is investigated, it is seen that the repeated charged/discharge cycles are eliminated completely. The SOC profile of cells is shown in Figure 5.27. The result shows that the balancing process is completed at 1218 s. And it is clearly seen that the maximum SOC imbalance at the end of balancing is below 1%.

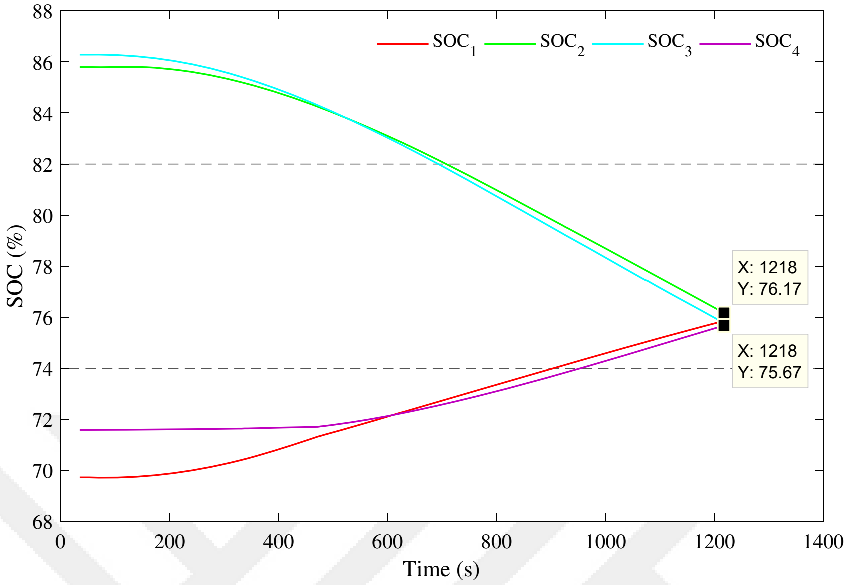


Figure 5.27. The SOC graphs of the proposed CTPTC BCS at the smooth initial imbalance

Also, the terminal voltage of cells is measured by ADC channels of dSPACE simultaneously. The results show that the voltage imbalance from 17 mV at the beginning is reduced to the 9 mV range, as demonstrated in Figure 5.28.

The measured SOC_{avg} of the battery cells is shown in Figure 5.29. SOC_{avg} has declined from 78.34% to 75.78%. It can be concluded that the SOC loss of the balancing system is 2.56 %.

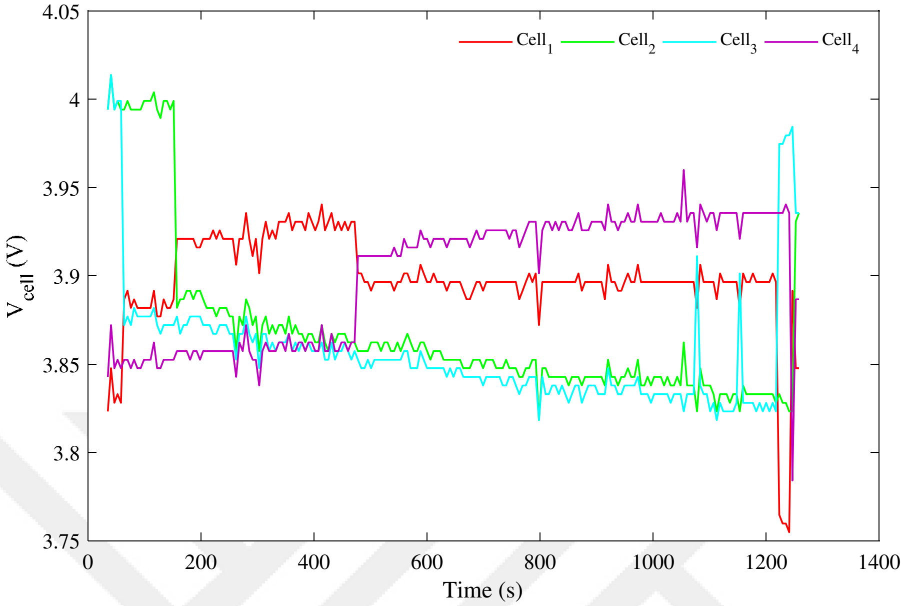


Figure 5.28. Terminal voltage graphs of the proposed CTPTC BCS at smooth initial imbalance

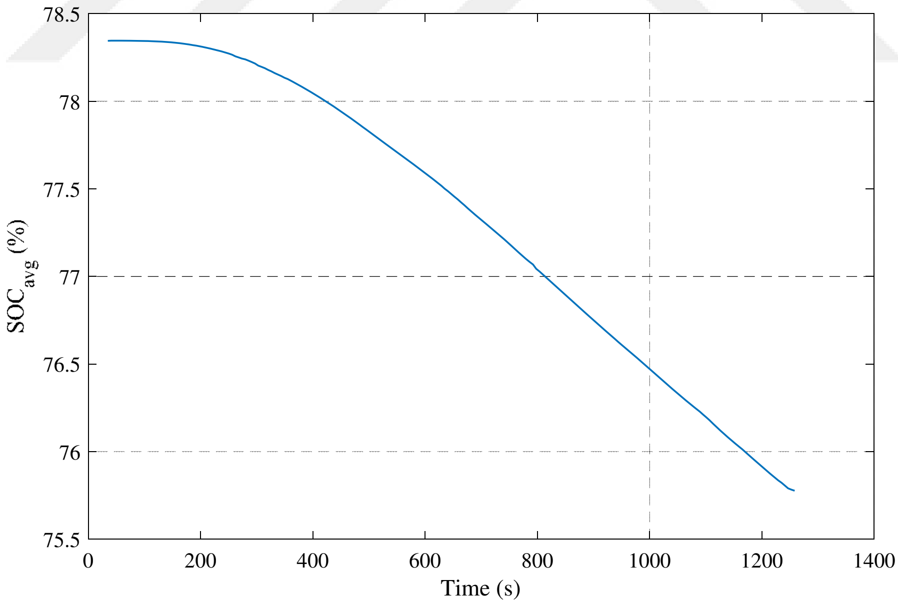


Figure 5.29. SOCavg loss of the proposed CTPTC BCS at the smooth initial imbalance

5.7.2. Charging Condition

In the case of charging, the current passing through the battery is the sum of the balancing current and the charge/discharge current. The battery charging circuit, which is fed constant DC voltage at the input on the constructed prototype, is designed to apply constant charging current to the cells. The value of the charging current is controlled by the duty cycle of the PWM signal applied to a charger MOSFET. If the duty cycle of the PWM is 1, 1C charging current starts to flow through the batteries. The appropriate charging current for the NCR18650B type Li-ion battery is given as 0.5 C in the datasheet. For this reason, the PWM duty cycle applied to the charger MOSFET is set as 0.4 in this thesis.

In this section, the performance results of the proposed BCS at 12.88 % initial SOC difference with four cells are presented. The initial SOC of each cell is 88.2%, 90.47%, 77.6%, and 81.87%, respectively. BCS initially all the energy of $Cell_2$ with the highest charge is transferred to $Cell_3$ with the lowest charge. Meanwhile, the charge and discharge MOSFETs of the intermediate cells are turned off. The BCS applies PWM to the charge MOSFET of the low-charged cell so as to keep the balancing-induced current delivered to the pack at 0 A. This ensures that the intermediate cells are only charged with the charging current. If the SOC difference between any cell(s) falls below the threshold value, the proposed cell selection algorithm performs the control of the relevant MOSFETs. The low-level controller always keeps the balancing-induced pack current at 0 A reference. The obtained results are observed from the current graphic of cells is shown in Figure 5.30. It is seen that balancing is terminated at about 1320 s, and all cells continue charging. After this point, when the SOC difference between the cells exceeded the threshold value, the balancing strategy was activated. This causes the current oscillation at the later stage of the balancing process.

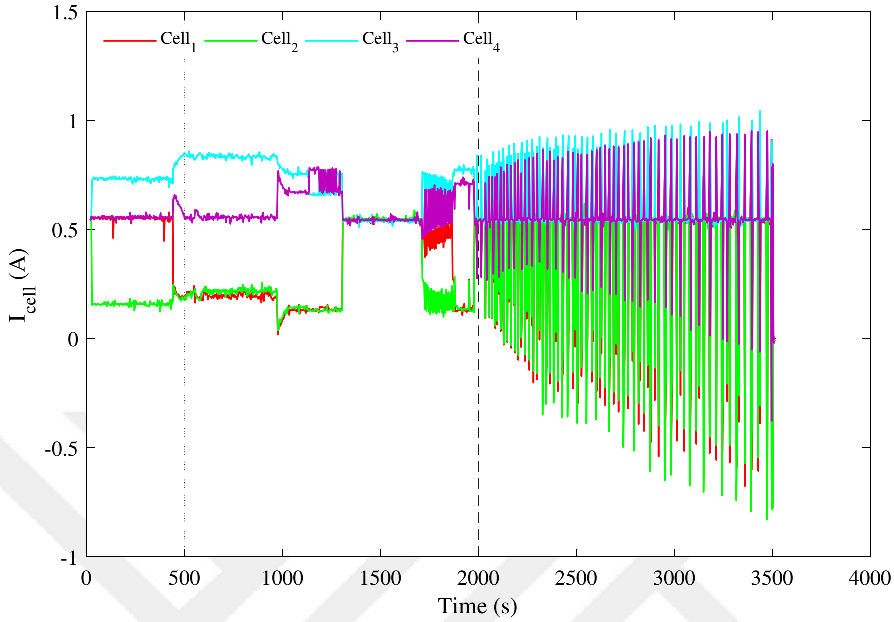


Figure 5.30. The current graphs of the proposed CTPTC BCS at charging condition

When the SOC change of the cells is investigated, it is seen that the cells are charged in a balanced. SOC profiles and terminal voltages of the cells are shown in Figure 5.31 and Figure 5.32, respectively. The result shows that the charging process is completed at 3494 s. Also, charging is stopped when any cell reaches 98% SOC to prevent damage due to any fault measurement of SOC and voltage in Li-ion cells.

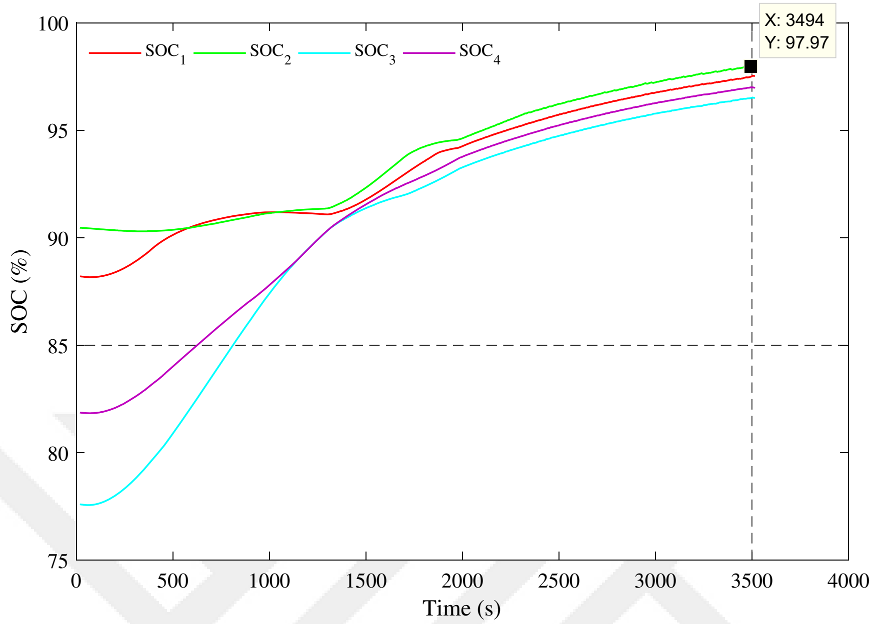


Figure 5.31. The SOC graphs of the proposed CTPTC BCS at charging condition

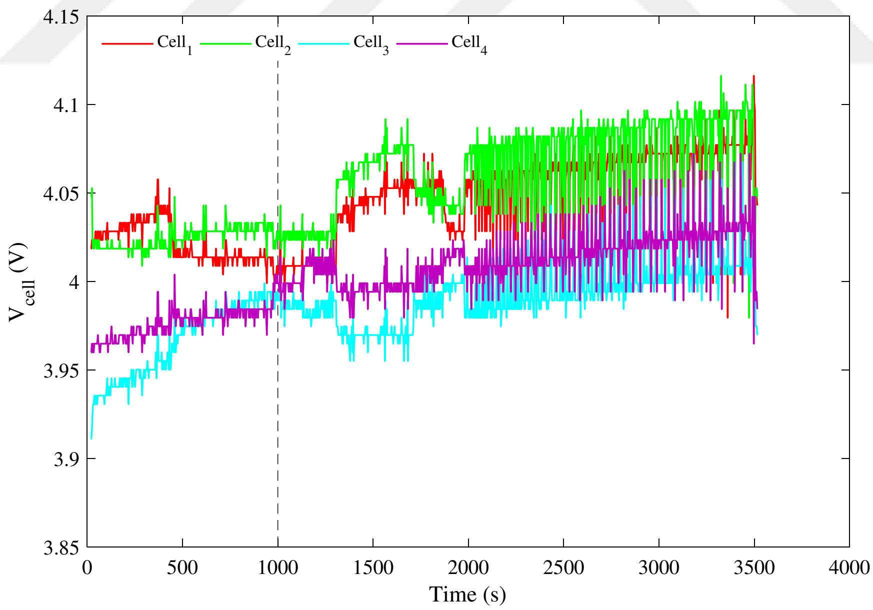


Figure 5.32. The voltage graphs of the proposed CTPTC BCS at charging condition

5.8. Summary

Circuit description and operation principles of developed active CBS are explained in this chapter. The proposed BCS and low-level control are also introduced in this chapter. The proposed BCS of the designed CTPTC balancing topology is expressed in detail with the help of an explanatory flowchart. The design of the power circuit and control system are presented with mathematical equations. Furthermore, the development of real-time operation of active CBS is explained. Schematic designs and the PCB layout of the overall system are also presented in this chapter. The experimental design requirements of a laboratory prototype of developed active CBS and preliminaries are given. An experimental set-up of designed active CBS is constructed to verify the performance of the real battery system. In the later phase of the section, the presented active CBS is verified through simulation by conducting a severe imbalance case study. Significantly, the experimental results are obtained to verify the developed CBS by conducting severe and smooth imbalances, also charging condition cases.

6. CONCLUSION AND FUTURE WORK

In this section, the main contributions of the thesis are summarized, the concluding remarks related to the thesis are emphasized, and the aspects of the thesis for future studies are discussed.

6.1. Concluding Remarks and Discussion

The interest in EV technology has been increasing in recent years due to its superiority over traditional internal combustion engine vehicles. However, battery performance, which limits vehicle range, is still the biggest obstacle to their proliferation. Although only battery chemistry seems to affect battery performance, BMS quality also greatly affects battery performance. Therefore, well-designed BMS has a critical role in the development of EV technology.

Hundreds of Li-ion battery cells that make up the battery packs of EVs have charge imbalances caused by manufacturing, different aging effects, and different assembly layouts. And the usable capacity and lifetime of a battery pack are limited to the cell with the lowest SOC. So, an active CBS, which is one of the core functions of BMS, which increases the usable capacity of the battery by transferring the energy in the high-charged cells to the low cells, has an important place in EV application. An active CBS consisting of hardware and software suffers from problems such as balancing speed and charge transferring efficiency. Although balancing speed and efficiency have been increased with topological improvements, high levels have not been reached yet. This gap has motivated our attempts to develop new BCSs to increase balancing speed and charge transfer efficiency.

In this thesis, different BCSs have been proposed for CTP and CTPTC active balancing topology, which are topologically higher balancing speeds. In the first of the proposed designs, a novel BCS for a single flyback converter-based CTP balancing topology is developed to minimize balancing time. The charge transferring model of overall CTP CBS is described meticulously. Since each cell is described by its capacity and SOC, the developed BCS is based on a general battery pack model that may be used for cells with various capacities. Also, developed BCS can be combined with various CTP topologies which can be described with a topology matrix. The other of the main contributions of the developed BCS is that the balancing process operates at the balancing limits early described. The CBS with BCS is constructed at MATLAB/Simulink simulation program. The performance results of the CBS are compared with the results of the traditional BCS (Mean-difference algorithm) at 18 % initial SOC imbalance case. In the traditional BCS, the balancing is completed at 4000s. With the developed BCS, this time value has been reduced to 1760s. In addition to reducing the amount of balancing time with the proposed BCS, little improvements have been observed in the balancing efficiency. SOC loss is measured as 1.78 % in traditional BCS, while this value has been decreased to 1.64% with the proposed BCS. With the obtained results, it is concluded that the proposed BCS for designed balancing topology ensures an accurate, efficient, and very fast balancing process.

In the second of the designs, a novel BCS for a multiple flyback converter (ICB)- based CTPTC balancing topology is developed to maximize the balancing efficiency. A rigorous model of the balancing system with a novel BCS is presented in detail. An experimental prototype is also implemented for four series of connected cells. The design stages of the system with the proposed BCS structure are meticulously explained. The superiority of the proposed CBS is analyzed for different initial SOC at standby conditions and charging condition. It is clearly confirmed that the presented BCS achieves promising results in terms of charge transferring efficiency. According to the design specifications of the prototype system, the design of the CTPTC active cell balancing circuit is performed using the theoretical calculations and the simulation studies accomplished in MATLAB. In the design stages of the CBS, the main balancer circuit, the design of measurement, gate driver circuits, onboard charger circuit, and the PCB design of the overall system are performed. The prototype of the active CTPTC balancing system is completed with the power circuit and the control system implementation with real-time operation by using dSPACE. The performance result has been compared with the commonly used balancing control algorithm called the mean-difference algorithm. In the balancing operation with a mean difference-based control strategy, 6.92% of the total capacity of the cells is lost. However, this value has been measured as 5.38% with balancing operation with developed BCS. It is concluded that the developed strategy operates the balancing process with 22% lower energy loss.

6.2. Future Work

Possible study topics related to this thesis planned to be carried out in the future are listed below.

- It is planned to verify the CTP CBS design whose performance is tested with an experimental prototype,
- The power circuit of the ICB-based CTPTC balancing system will be modified to reduce the size and number of components,
- The proposed BCS for ICB-based CTPTC balancing topology will be verified for balancing control of a large battery pack.

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