NOVEL MATERIALS FOR THIN-FILM MEMORY CELLS

A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND

ELECTRONICS ENGINEERING

AND THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

MASTER OF SCIENCE

By

Furkan Çimen

August, 2014

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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The tremendous growth in consumer electronics market increased the need for low-cost, low-power and high quality memory chips. This challenge is further aggravated by the continuous increase in density and scaling of the gate length, since it creates a major challenge for current nonvolatile flash memory devices to maintain reliability and retention. Therefore, it is imperative to find new materials and novel fabrication processes to be incorporated in memory cells in order to keep up with the enormous rate of increase in consumer needs.

In the first part of this thesis, we demonstrate a charge trapping memory with graphene nanoplatelets embedded in atomic layer deposited ZnO. We first introduce the fabrication process for the memory device and then investigate the memory characteristics. Our experimental analysis on the memory cell shows a large threshold voltage V_t shift ($4V$) at low operating voltages ($6/-6V$), good retention ($>$ 10 years), and good endurance characteristics ($> 10^4$ cycles). The resulting memory behavior is also verified by theoretical computations.

In the second part, we demonstrate the use of laser-synthesized indium-nitride nanoparticles (InN-NPs) as the charge trapping layer in the memory cell. We first introduce the indium-nitride nanoparticle synthesis and then detail the fabrication process of the memory device. The experimental analysis of the memory cell results in a noticeable threshold voltage V_t shift ($2V$) at low operating voltages ($4V$) in addition to the similar retention and endurance performance with the graphene-based memory cells. The memory behavior was also verified with theoretical computations for the InN-NPs based memory cells.

In the last part of this thesis, we demonstrate a memory device with a gate stack fabricated in a single ALD step. Single-step all-ALD approach avoids the risk of contamination and incorporation of impurities in the gate stack. It also

allows low-cost production by eliminating multiple equipment utilization. Motivated by these, we first present the fabrication process of the memory device and then explain the experimental and theoretical characterization and analysis. The memory effect of the thin-film ZnO charge-trapping memory cell is verified by a $2.35V$ hysteresis in drain current vs. gate voltage curve. The resulting memory behavior is also verified by physics-based TCAD simulations.

Keywords: charge trapping memory, non-volatile memory, graphene nanoplatelets, indium-nitride nanoparticles, atomic layer deposition, ZnO, gate stack.

ÖZET

İNCE-FİLM BELLEK HÜCRELERİ İÇİN ÖZGÜN MALZEMELER

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Ağustos, 2014

Elektronik ürün sektöründeki gelişmeler düşük maliyetli, düşük güç tüketimli, yüksek hafıza kapasiteli aynı zamanda yüksek kaliteli bellek çiplerine olan ihtiyacın ve talebin artmasına neden olmuştur. Günümüz sabit bellek aygıtlarında bileşen yoğunluğu ve küçülen transistör ebatları nedeniyle bellek güvenilirliği ve dayanıklılığı konusunda sorunlar yaşamadan daha fazla boyut küçültmek, yeni malzemeler kullanmadan mümkün olmamaktadır. Bu nedenle, yeni materyaller ve özgün üretim teknikleri bulmak suretiyle tüketici ihtiyaç hızına yetişebilecek bellek aygıtları geliştirilmesi elektronik endüstrisi için zorunluluk haline gelmiştir.

Bu tezin ilk bölümünde atomik katman biriktirme yöntemiyle kaplanan ZnO içine gömülü grafen nanoplaka yapısını yük tutucu katman olarak kullanan bir bellek aygıtını tanıttık. Öncelikle bellek aygıtının üretim sürecini anlatıp daha sonra aygıtın bellek karakteristiklerini inceledik. Bellek hücresi üzerinde gerçekleştirdiğimiz elektriksel analizler, üretilen belleğin düşük çalışma voltajlarında $(6/-6V)$ yüksek bir eşik voltajı (V_{th}) kayması $(4V)$, depolanan bilginin uzun süre muhafazası (>10 yıl) ve başarılı dayanıklılık karekteristiklerine ($>10^4$ yazma-silme) sahip olduğunu göstermiştir.

Tezin ikinci bölümünde lazer ablasyon sentezi ile üretilmiş İndiyum-Nitrür nanoparçacıklarını yük tutucu katman olarak kullanan bir bellek aygıtını tanıttık. Öncelikli olarak indiyum-nitrür nanoparçacıkların sentezinden kısaca bahsettikten sonra bellek hücresinin üretim sürecinin detaylarını anlattık. Elektriksel özelliklerinin analizleri, üretilen bellek hücresinin grafen tabanlı belleğe benzer hafıza saklama süresi ve dayanıklılık özelliklerinin yanısıra düşük yazma voltajlarında $(4V)$ kaydadeğer eşik voltajı (V_{th}) kaymasına $(2V)$ sahip olduğunu göstermiştir. Üretilen aygıtın bellek karakteristikleri aynı zamanda teorik analizler ve hesaplamalarla da desteklenmiştir.

Bu tezin son bölümünde atomik katman kaplama yöntemiyle tek seferde bütün kapı katmanının üretildiği bir bellek hücresini sunduk. Bütün katmanların tek seferde üretilmesi katmanlar arasında kirlenme riskini ve istenmeyen atomların karışma ihtimalini azaltır. Aynı zamanda farklı ekipman kullanımını ve üretim basamaklarını azaltması nedeniyle bu üretim tekniği daha düşük maliyetli üretim sreçlerine olanak sağlar. Bunlardan hareketle, bellek hücresinin üretim süreci ve aygıt yapısı anlatıldıktan sonra üretilen belleğin deneysel ve teorik karakteristik analizleri yapıldı. Yük tutucu katmanın ince-film ZnO olduğu bellek hücresinin hafıza özelliği savak akımı-kapı voltajı grafiğindeki $2.35V$ histerez ile doğrulanmıştır. Sonuç olarak ortaya çıkan belleğin hafıza özellikleri aynı zamanda TCAD simulasyon çalışması aracılığıyla karşılaştırılarak da benzer sonuçlar elde edilmiştir.

Anahtar sözcükler: yük yakalamalı bellek, kalıcı bellek, grafen nanoplakalar, indiyum-nitrür nanoparçacıklar, atomik katman kaplama, ZnO, kapı yığını.

Acknowledgement

First, I would like to thank my supervisor, Dr. Ali Kemal Okyay, for his guidance, support and tremendous patience throughout my study. He was always there to encourage and help me when I needed. I would also like to thank Dr. Bülend Ortaç and Dr. Necmi Bıyıklı for their stimulating discussions and support. I have always been inspired by their expertise during my research studies. I would also give my special thanks to Dr. Orhan Güvenen for his huge trust in me and my thesis committee members Dr. Mehmet Bayındır and Dr. Aykutlu Dana.

There are a number of people from my research colleagues, who helped me along the way. I am very thankful to Feyza Bozkurt, Fatih Bilge Atar and Nazek El-Atab for their helps and friendship on the way of my M.Sc. degree. This thesis would not have been possible without their contributions. In addition, I would like to thank my research group friends, Ali Cahit Köşger, Sami Bolat, Oğuz Hanoğlu, Levent Erdal Aygün, Burak Tekcan, Ayşe Özcan, Elif Özgöztaşı, Enes Battal, Şeyma Canik, Amin Nazirzadeh, Amir Ghobadi, Gamze Ulusoy, Muhammad Maiz Ghauri, and Berk Berkan Turgut for our wonderful late night studies and discussions.

One of the most important aspects of my studies was the opportunity to work in UNAM (National Nanotechnology Research Center). I thank my UNAM friends Çağla Özgit, Ahmet Emin Topal, Adem Saraç, Mehmet Kanık, Semih Yaşar, İnci Dönmez, M. Alican Noyan, and Fatma Gül Maraş.

Outside the laboratory, there are some friends who directly or indirectly contributed to my M.Sc. studies. I thank my college friends Hasan Hamzaçebi, Serkan Sarıtaş, Ahmet Yükseltürk, Uğur Yılmaz, İsmail Uyanık, Ali Kök, Hale Nur Kazaçeşme, Büşra Altınsoy, Elif Eser, Alexandra Zehra Aksu and Osman Gümüş. I would also like to thank my colleagues Dr. Orhan Şengül, Dr. Cüneyt Utku, Hakan Özyürek and Dr. Levent Şahin.

I am also appreciative of the financial support from the Scientific and Technical

Research Council of Turkey (TÜBİTAK). This work was supported by TÜBİTAK through grant numbers 109E044, 112M004, 112E052, 112M482, and 113M815.

Finally, but forever I owe my loving thanks to my parents, Nazmi and Fatma Çimen, my sister, Meliha Çimen and my aunt Figan Yılmaz, for their undying love, support, encouragement and patience for my complaints.

It is said that a book's dedication is the most exquisite and soulful way to pronounce a name. I avow that it is as exquisite and as soulful to dedicate this one to you, without pronouncing yours.

Contents

List of Figures

Chapter 1

Introduction

In the past decade, the increased customer needs in electronics market also increased the need for novel electronics products, such as smart phones, tablets, mobile devices, and digital cameras [7, 8]. However, the existing nonvolatile flash memory devices cannot keep up with the tremendous speed in density and scaling of these electronics devices. Therefore, one of the most attractive research direction for electronics industry is to develop novel memory cells with low cost, low power consumption and high density.

The metal-oxide-semiconductor field-effect-transistor (MOSFET) is the basic memory structure used in electronic devices. The initial ideas of field-effect transistors was first demonstrated by Lilienfeld and Heil in the early 1930s [9]. Subsequent studies of Scockley and Pearson on Ge based bipolar point-contact transistor and then Ligenza and Spitzer's work on MOS systems are followed by the first use of MOSFET concept by Atalla [10].

The consumer requirements for high performance and dense integrated circuits (ICs) also require a scaling down in the simplest memory cell. The traditional approach in IC industry is to scale down the transistor sizes and optimize their structure in an IC in order to maximize density. However, this approach is limited with technological challenges and increasing fabrication costs. After a certain point, the optimization will reach a limit, where further scaling down will not be

possible or practical without change in choice of materials.

Motivated by these problems, the goal of this thesis is to find novel materials in order to enhance the memory characteristics of the memory cells which will delay the need for scaling. Our approach is to utilize different materials, which have promising features for advancement of electronic devices. Additionally, we also demonstrate the use of atomic layer deposition (ALD) in order to build gate-stack of memory cells at single-step with high impurity and low cost, which will also be imperative for future memory devices.

1.1 Methodology

In this section, we aim to explain the methodology followed in this thesis. As explained above, novel materials and structures must be used in order to pave the way towards high quality and high density and low cost memory devices. Therefore, we propose the use of graphene nanoplatelets and indium-nitride nanoparticles embedded in ALD deposited ZnO layer as the charge trapping materials in the memory cells.

In our design of the memory structure, we deposit graphene nanoplatelets (or indium-nitride nanoparticles) sandwiched between ZnO layers in the charge trapping layer. The charge trapping layer is where the electrons are trapped during the *program* operation and released during the *erase* operation. The additional ZnO layers in the charge trapping layer increases the retention characteristics of the memory cell, since ZnO acts as an extra energy barrier for the trapped electrons and hence prevent them from back-tunneling.

In fabrication process, we utilize the ALD approach as much as possible for the memory cells with graphene nanoplatelets and indium-nitride nanoparticles. As will be explained in related chapters, fabrication of the memory structure starts with an ALD process, where we deposit tunnel oxide and ZnO layer in a single ALD step. Then, we lay out the graphene nanoplatelets (or indium-nitride nanoparticles) on top of the ZnO. The final step is again an ALD process, where

we deposit the second ZnO layer and blocking oxide. By using this fabrication process, we can benefit from the advantages of ALD such as accurate thickness control and high uniformity.

As a last device, we propose an all-ALD approach, where active area of a memory cell is grown in a single ALD step by utilizing ZnO as the charge trapping layer. Despite limited performance of this new device, the single-step production advantage of this memory cell is promising for future low cost memory cell development.

1.2 Contributions

The primary contribution of this thesis is introduction of graphene nanoplatelets and indium-nitride nanoparticles for charge trapping agents in new memory cells. Our studies show that graphene nanoplatelets and indium-nitride nanoparticles based memory cells (sandwiched between ZnO layers) provides high retention and endurance characteristics for the memory cells as well as high threshold voltage shift. We show experimental analysis, which are verified by theoretical computations, to systematically evaluate the memory characteristics of the fabricated devices.

We also propose an ALD based fabrication approach, where we can deposit a memory cell in a single ALD step. This approach is advantageous due to its low production cost and elimination of contamination and impurities. The memory behavior of the fabricated device is also verified by experimental analysis and TCAD simulations.

1.3 Organization of Thesis

We begin the thesis by explaining the fundamentals of ALD in Chapter 2. We introduce necessary background for the ALD technique with the details of ALD

growth cycle. The advantages and limitations of ALD are also mentioned in this chapter. We then continue with thin film transistor and memory basics in Chapter 3. The basic transistor and memory structure along with working principle are also presented in this chapter.

In Chapter 4, we introduce our work for enhancing memory effect with embedded graphene nanoplatelets in ZnO charge trapping layer. The fabrication processes of the memory device and characterization studies are also explained in this chapter.

Chapter 5 details the fabrication process of the memory device with indium-nitride nanoparticles embedded in ZnO charge trapping layer. The experimental and theoretical analysis performed to characterize the memory behavior are also discussed in this chapter.

We finally present thin-film transistor memory cell with ZnO charge trapping layer whose gate-stack grown in a single ALD step in Chapter 6. We detail the motivation, fabrication process and experimental analysis of the memory cell in this chapter. We also provide TCAD simulations to support the electrical measurements. We then summarize the thesis with concluding remarks and future directions in Chapter 7.

Chapter 2

Fundamentals of Atomic Layer Deposition

This chapter introduces necessary background for the atomic layer deposition (ALD) technique as well as details of the ALD growth process and its properties. We present advantages and disadvantages of the ALD process mainly used for our applications.

2.1 Introduction

Atomic layer deposition (ALD) is a thin film deposition technique similar to chemical vapor deposition (CVD) [11, 12]. The ALD technique employs self limiting or sequentially saturative surface reactions onto various substrates with a precise controlled way [11]. Thickness control at atomic scale can be achieved by deposition of alternating chemicals called precursors. At each step, precursors decompose on the substrate surface to form a single layer of atoms due to their self-limiting property. The desired film thickness is obtained by repeating this sequential process on the substrate surface [12].

Although ALD is a CVD technique in principle, it has a major difference from

standard CVD, since it breaks the CVD reaction into two half-reactions, where the precursor materials are kept separate by sequentially releasing them [11, 12]. Actually, this specific feature enables ALD to build alternating mono-layers.

ALD principle is based on an initial study called molecular layering, which was published in early 1960s. Prof. V. B. Aleskovskii proposed the concept of molecular layering to modify the surfaces of sorbents and catalysts [13]. As an experimental application of this concept, they were able to realize the sequential exposure of $TiCl_4$ and H_2O to form TiO_2. Then, Suntola and co-workers were the first ones, who developed a film deposition technique called atomic layer epitaxy (ALE), which is called ALD later, based on the idea of molecular layering in 1970s [14]. They also developed reactors for the implementation of ALE for an industrial project to manufacture thin film electroluminescent (TFEL) flat-panel displays. These TFEL displays remained as the sole industrial application of ALE for a long time until the increased interest of silicon-based microelectronics.

Starting from 1990s, the increased trend for scaling down in Si-based microelectronics required technique that produce very thin, highly conformal films with precise thickness control. This was the breakpoint for ALD to be a commercially important technique for industry due to its ability to deposit high quality thin films with an excellent surface control at the atomic level over large areas at low temperatures.

Nowadays, ALD allows depositing a wide variety of materials, such as nitrides (semiconductors, dielectrics, metal compounds), oxides, fluorides, sulphides, selenides, tellurides, II-IV, III-V compounds, as well as elemental materials [11].

2.2 ALD Growth

ALD film deposition is a repetitive cyclic process, which consists of four main parts in each cycle. Each cycle in ALD film growth results in a deposition of mono-layer of the composition of different precursors. The repetition of this process yields the desired film thickness. Before giving the details of ALD growth

cycle, we first define the four main steps for easy understanding of the ALD process (illustrated in Fig. 2.1).

1. Exposure of Precursor #1
2. Purge #1
3. Exposure of Precursor #2
4. Purge #2

The first step of an ALD cycle starts with the pulse of first precursor onto the substrate surface. When the substrate surface is exposed to the molecules of the first precursor in an appropriate temperature and gas flow rate, a mono-layer of the reactant is chemisorbed onto the surface (see Fig. 2.1 (a)). Then, the excess

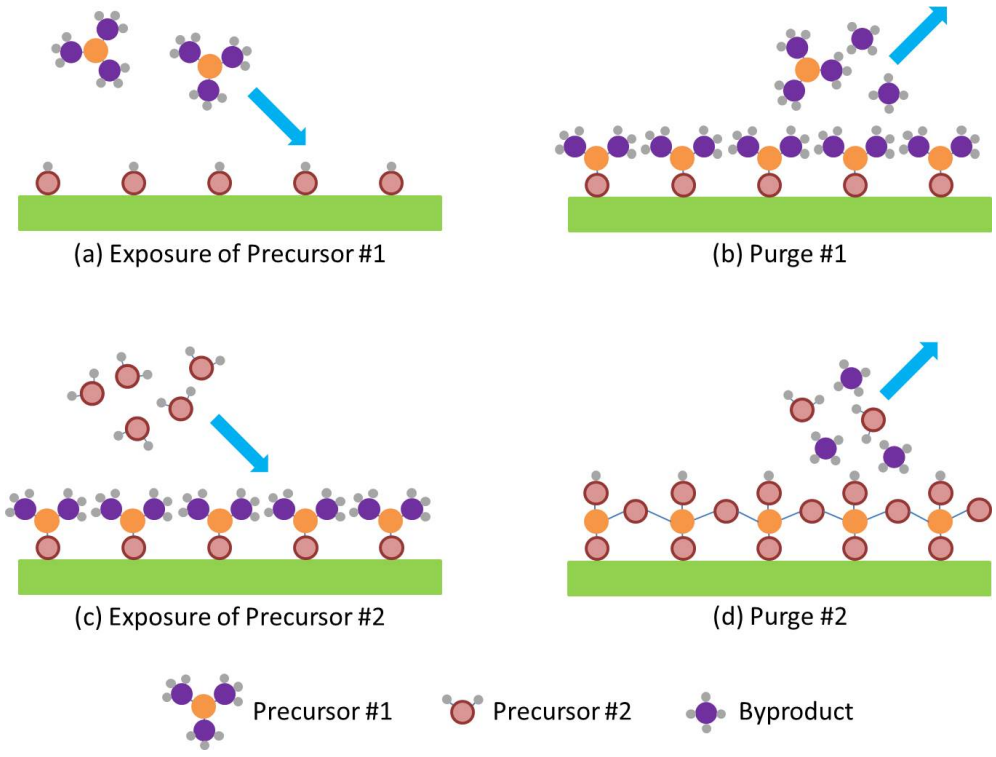

Figure 2.1: A schematic representation of an ideal ALD process cycle

reactant is purged out of the process chamber by using an inert gas pulse. This phase is called Purge #1 (see Fig. 2.1 (b)). The second precursor (reactant) is

then pulsed onto the substrate, whose surface is covered with the decomposed reactant of the first precursor. In this step, the second precursor undergoes an exchange reaction with the first precursor and creates another layer on top of the first one (illustrated in Fig. 2.1 (c)). The exchange reaction between the two precursors also yields a gaseous side product in the chamber. Therefore, another purge phase is required to remove this byproduct and excess molecules of the second precursor with the use of an inert gas (see Fig. 2.1 (d)).

Due to the self-limiting property of the ALD process, only a mono-layer of the applied precursor material is deposited onto the substrate surface at each cycle. Repetition of this step results in a layer-by-layer growth of the film by allowing a control of the film thickness at atomic level. This is the key notion to understand and develop ALD-based processes.

Another fundamental parameter of the ALD process is to adjust the appropriate chamber temperature for a successful ALD growth. Since the second precursor undergoes an exchange reaction with the first one, the chamber temperature must be high enough to break the chemisorption bond of the previous precursor. However, it needs to be low enough at the same time so that precursors breakdown only on the surface of substrate and the first mono-layer on the surface is kept until the second reaction occurs.

2.3 Advantages and Limitations of ALD

ALD provides a very simple way for producing uniform and high quality thin films due to its significant advantages with respect to other deposition techniques. Some key advantages of the ALD process can be summarized as below.

- **Accurate thickness control:** Since cyclic deposition steps of ALD process are self-limiting, each step builds only a mono-layer of the applied precursor. Therefore, accurate thickness control can be achieved by choosing the number of ALD cycles during the coating process. Since each cycle results in one atomic layer, the thickness of the final product can be controlled at

the atomic scale as well. This is one of the major advantages of the ALD process for its promising role in microelectronic industry.

- **High conformity and trench fill:** If the pulse and purge phases in ALD process are long enough, the surface of the substrate becomes saturated even at very deep trenches and high aspect ratio features. Also long purge durations removes all the excess precursors and byproducts of decomposed precursors so it restricts the deposition of the film to only one layer per cycle. With this property ALD results in very effective conformal deposition as well as high quality trench-fill capability.

- **Low temperature process:** ALD layer deposition is a chemical process, in which chemical bonds are broken in order to deposit the next layer on top of the previous one. Due to the low energy requirements of the chemical processes, it is possible to produce high quality films in low temperatures.

- **Reproducibility:** Self-limiting property makes the ALD process very reproducible and easy to implement.

In the light of the aforementioned advantages, ALD became a widely preferred technique for producing high quality thin films. However, there are also some drawbacks and limitations of the ALD process, which needs to be kept in mind.

- **Reaction time:** One of the main limitations of the ALD process is its slow reaction time. Therefore, ALD is mainly used for processes such as microelectronics, which does not require thick films.

- **Substrate purity:** High purity of the substrates in ALD process has a significant importance. This limitation brings additional costs to the process and constraints to integration of ALD process to multiple step processes.

- **Precursor constraints:** Since the precursors must be volatile but not subject to decomposition, there is a limitation on the chemicals that can be used for ALD process.

2.4 ALD Precursors

As explained in Section 2.3, there are some limitations on the ALD precursors. This section focuses on the requirements of precursors for the ALD process [11].

Volatility:
Due to the chemical nature of the process, precursors must be volatile at a reasonable temperature to produce sufficient vapor pressure. At this point, vapor pressures and the highest applicable source temperatures are the key elements that define the volatility of the precursors.

Stability against self-decomposition:
As explained in Section 2.2, the deposition temperature in the chamber must be low enough so that precursors do not decompose in the gas phase, since this will damage the self-limiting growth property of the ALD process. Therefore, decomposition experiments on both the bare substrate and the previously deposited films need to be performed to understand precursor decomposing temperature.

Decomposition of the precursors may cause incorporation of contaminants in the film, which decreases the quality of the product. Therefore, decomposition should be kept minimum and mostly on the surface of the substrate until reaching a self-limiting growth.

Aggressive and complete reactions:
ALD systems allow the comfortable usage of the precursors, which aggressively reach with each other. This is mainly due to its property of separate deposition of the precursors. This kind of reactants are preferable in ALD systems since aggressive reactions result in shorter cycle times. However, because of this extra safety precautions should be taken against mixing the precursors with each other.

No etching reactions:
Some precursors undergoes etching reactions with the consecutive precursor. To avoid this situation, examination of the reactions between the precursors should be performed prior to the production stage.

Non-reactivity of the byproducts:
The resulting byproducts of the precursors must be non-reactive and evacuated from the chamber easily with the use of an inert gas. When the byproducts are reactive, they start damaging the chamber walls and some times they readsorb on the film surface. This situation decreases the growth rate of the film and increases the contamination of the films.

Others:
Some other limitations on precursor selection can be summarized as low cost, easy synthesis and handling, non-toxicity and environmental friendliness.

2.5 ALD Equipments

The ALD equipments can be divided into two categories based on their method of pulsing the precursors: flow-type ALD reactors with inert gas valving and flow-type ALD reactors with moving substrates. The details about these types and different classification methods for the ALD reactors are left out of scope of the current work, since we will use the available ALD reactor in our labs for this thesis.

We use Savannah S100 ALD reactor (photographed in Fig. 2.2) from Cambridge Nanotech Inc for the works presented in this thesis. The Savannah S100 is a flow-type ALD reactor with a $4''$ diameter and $0.25''$ deep reaction chamber. The reaction gases are pumped continuously with a single injection point and a single evacuation point. The single-injection point ALD reactors mostly causes non-uniformities in film thickness. Therefore, a shower-head injector is preferred to improve the gas distribution and reduce the non-uniformities. The user interface program of Savannah S100 reactor is illustrated with the labels for the associated main components in Fig. 2.3.

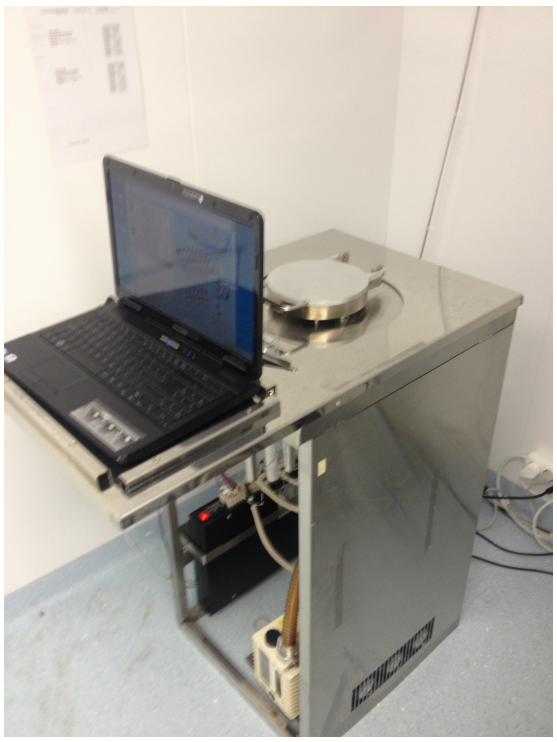

Figure 2.2: Cambridge Nanotech Savannah S100 ALD reactor used in this work

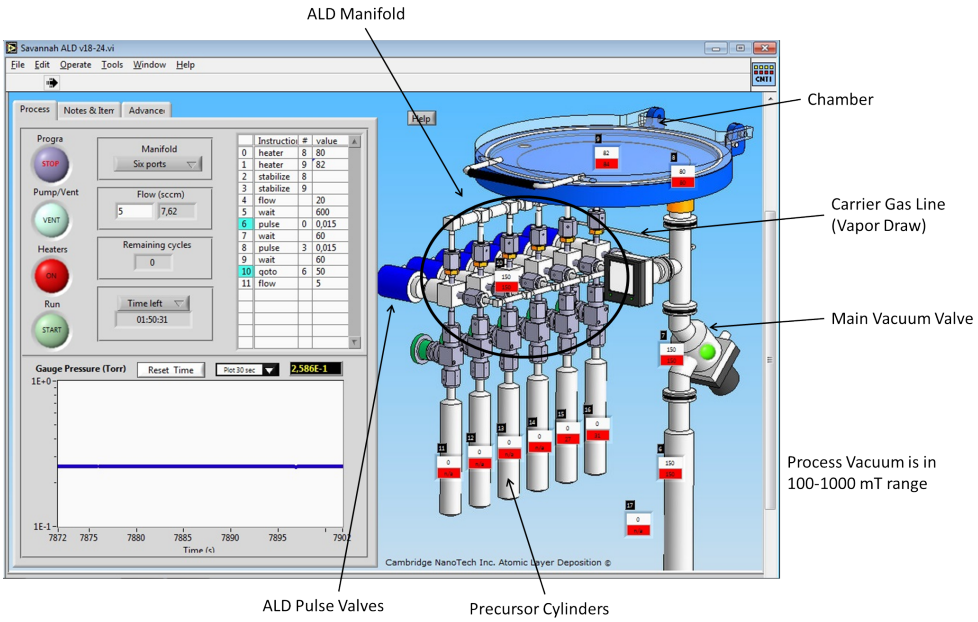

Figure 2.3: User interface program of Savannah S100 ALD reactor used in this work

2.6 ALD Window

In this section, we aim to define the concept of ALD window, which is a safe window for the ideal ALD processes in which growth rate is saturated at a monolayer of film per cycle [15]. Outside of this window, precursors may decompose in the gas phase and this may cause higher growth rates and lower thickness control and less conformal coatings. Additionally, reaction kinetics may cause incomplete saturation of the surface at lower temperatures. Therefore, identifying the ALD window for the process and working inside this window has a significant importance for the product quality. Fig. 2.4 below illustrates some possible effects of working outside the ALD window.

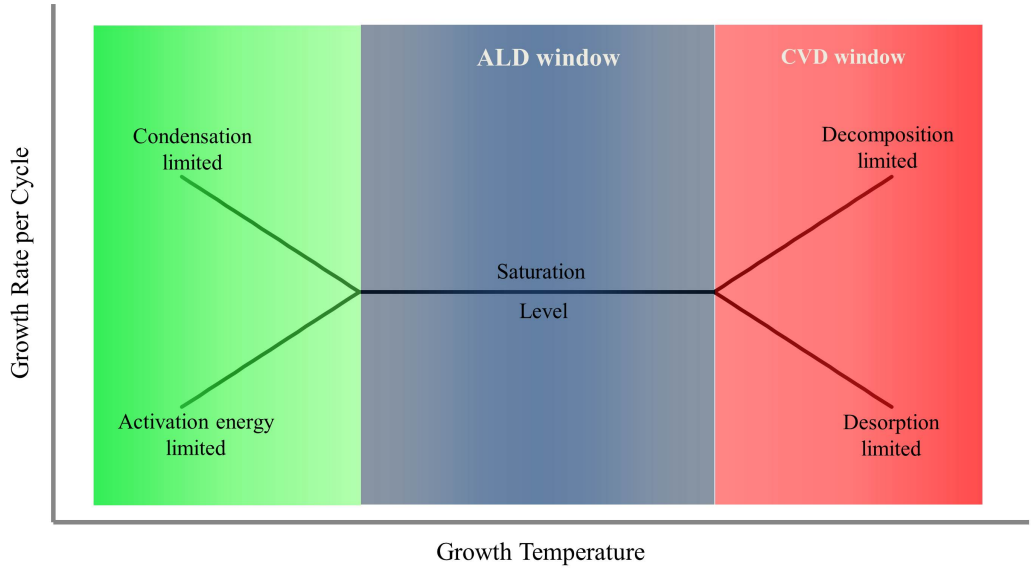

Figure 2.4: Growth rate vs. growth temperature including ALD window

2.7 Summary

Atomic layer deposition is a self-limiting thin film deposition technique based on similar principles with chemical vapor deposition. ALD is a cyclic process, where precursors are pulsed to the substrate surface in a cyclic manner to deposit a single layer of the reactant. Sequential repetition of this process allows the control

of the film thickness at the atomic scale. The purge process of the ALD cycle removes the byproducts of the ALD process, so one can obtain highly conformal films. The layer thickness control at atomic level and high conformity are the two main advantages of ALD to make it a preferred choice for the microelectronics and nanotechnology applications. In contrast to all these positive sides, ALD has some noteworthy disadvantages such as long process time and precursor limitations.

Chapter 3

Basics of Thin Film Transistors and Non-volatile Memory Devices

This chapter introduces necessary background for the thin film transistor and memory basics. The basic transistor and memory structure and working principle with some basic physics behind their operation are also presented in this chapter.

3.1 Metal-Oxide-Semiconductor Capacitor (MOSCAP) Structure

This section presents the basic Metal-Oxide-Semiconductor (MOS) structure in order to understand how an MOS Field Effect Transistor (MOSFET) operates and physics behind it. The MOS structure consists of an oxide layer that lies between a silicon substrate and a metal plate called gate as illustrated in Fig. 3.1 [16].

The energy band diagram of MOS structure for different states according to gate voltage, V_G, is shown at Fig. 3.2. We will explain concepts and states of the

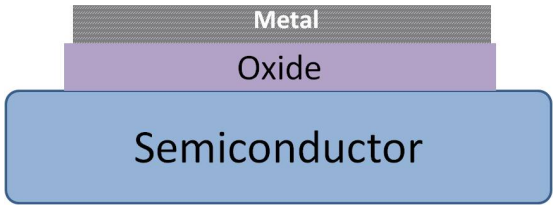

Figure 3.1: Basic MOS structure

MOS structure on this figure, however, we first need to make some definitions in order to make our point more understandable. In Fig. 3.2, $q\varphi_m$ represents the energy difference between Fermi level of the metal and conduction band of the oxide. Similarly, $q\varphi_s$ represents the work function at the semiconductor-oxide interface and $q\varphi_F$ is the energy difference between Fermi level and intrinsic level of the semiconductor.

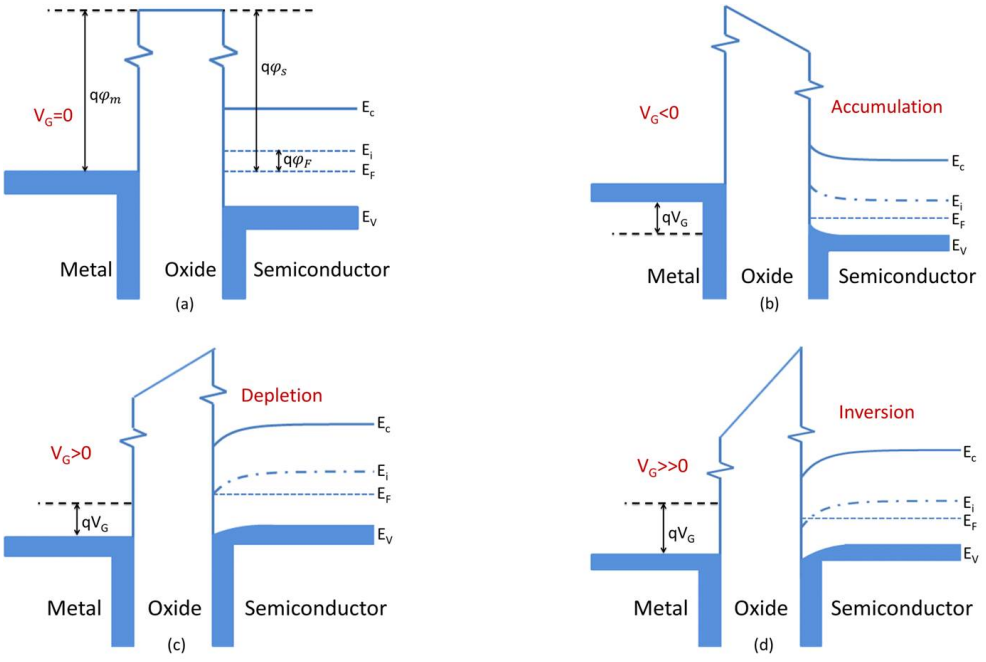

Figure 3.2: Energy band diagrams at different operating states of MOSFETs

Each sub-figure in Fig. 3.2 corresponds to a different state of the MOS structure based on the applied gate voltage and shows the change in the energy-band diagram and channel modification due to gate voltage. Fig. 3.2 (a) represents the state when the gate voltage is zero, $V = 0$. When the gate voltage, V, is different than zero (meaning that when a voltage is applied to the gate), an equal and

opposite signed charge accumulates at the metal-oxide and semiconductor-oxide interfaces. The sign of these accumulated charges determines the state of the MOS structure, which will be explained briefly in the following sections.

Accumulation:

When a negative voltage is applied to the metal gate, electrons are pushed away from semiconductor-oxide interface by electric field due to applied voltage so positive holes remain in the location of removed electrons. The applied negative voltage in the metal side increases the energy of the electrons in this side with respect to the ones in the semiconductor side. For an applied voltage, V_G, the difference between the Fermi level of metal and semiconductor becomes qV_G under negative bias. Since φ_m and φ_s are independent from the applied gate voltage, oxide band starts to bend as well as the energy bands of the semiconductor region near the interface due to increase in the hole concentration. The number of holes are larger than the equilibrium state and the interface becomes more p-type, in other words holes are accumulated and thus this state is called accumulation. Fig. 3.2 (b) illustrates this state and bending of the energy bands. It can be seen that Fermi level gets closer to the valence band which is an indication of increase in the hole concentration according to (3.1).

$$p = n_i e^{(E_i - E_F)/kT} \tag{3.1}$$

Depletion:

When the applied voltage at the metal part is reversed ($V_G > 0$), the whole story also becomes reversed. In the case of positive voltage at the gate, the electrons are pulled towards the semiconductor-oxide interface and they start to recombine with the holes. Since φ_m and φ_s does not depend on the applied gate voltage again, oxide band starts to bend in reverse direction under the effect of applied gate voltage. The difference $E_i - E_F$ decreases and at some voltage they overlap at oxide-semiconductor interface. When this happens the number of holes are equal to the number of electrons which is the intrinsic state of semiconductor according to (3.1). In this state the near field of oxide-semiconductor interface becomes depleted from mobile charge carriers. Thus, this state is called the depletion

state and change in energy band diagrams are illustrated in Fig. 3.2 (c).

Inversion:
If the positive applied gate voltage is further increased, it does not only deplete the region from the holes but it also increases the electron concentration at the interface. Therefore, the charge carriers at the interface becomes electrons instead of the holes which means the sign of charge carriers are inverted and this state is called the inversion state. Also the inversion of the charge carriers can be observed by the increase of Fermi level above the intrinsic energy level in Fig. 3.2 (d). The inversion property has a fundamental role for MOS transistor operation, which will be discussed later on.

3.2 Transistor Basics

The basic MOS structure described in Section 3.1 forms the basis for building MOS based transistor. The MOSFET is a MOS based transistor to amplify or switch electronic signals by controlling passing current with an applied voltage to the metal gate. Our goal in this section is to describe the MOSFET basics in order to develop the necessary background required to comprehend this thesis.

Let's first consider a current flowing through a slab of semiconductor as shown in Fig. 3.3.

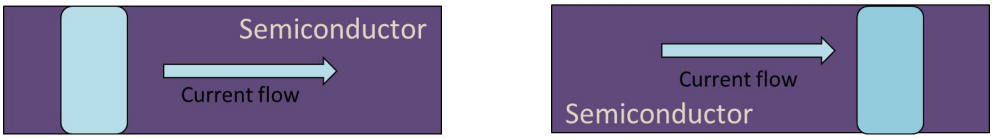

Figure 3.3: Current flowing through semiconductor slab by the migration of carriers

The current flowing in the semiconductor is defined as the amount of charge flowing per unit time or it can be expressed as the product of charge density and charge velocity. This brings us to the famous current equations, $I = Q/t$ and $Ampere = Colomb/second$ $(A = C/s)$. If we write this equation in a different

way with units, we obtain

$$I(A) = Q_d(\frac{C}{m})v(\frac{m}{s}). \tag{3.2}$$

Now, consider that we aim to control the flow of current in this substrate. Therefore, we first add two components source and drain to the substrate, which can be defined as the input and output of the semiconductor slab. Additionally, we construct another structure called gate, which will be used as a control input to regulate the flow of current from source to drain. Fig. 3.4 illustrates the simple transistor structure defined above.

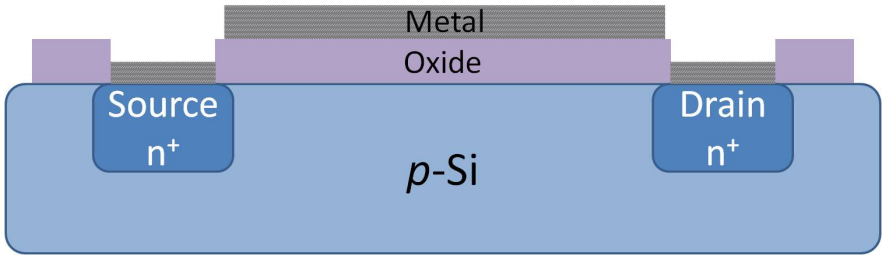

Figure 3.4: Simple transistor structure with gate, source and drain structures on semiconductor slab

As explained in Section 3.1, the inversion state of the MOS structure applying a voltage higher than threshold to the gate creates a layer at the interface between the semiconductor and gate oxide layer, where the electrons accumulates and form an n-type channel between n^+ source and drain allowing current flow from drain to source. We can also compute the charge density Q_d in the inversion layer for using in (3.2) as below

$$Q_d = WC_{ox}(V_{GS} - V_{th}). \tag{3.3}$$

Here, V_{GS} stands for the voltage difference between gate and source (generally source is connected ground so just applied voltage to the gate) and V_{th} represents the minimum required voltage to build inversion channel. When V_{GS} is equal to V_{th}, the inversion layer onset occurs at the oxide-semiconductor interface and charge transportation is possible when V_{GS} exceeds V_{th}.

Another actor in this game is the drain voltage. If the drain voltage is different than zero, source side channel potential 0 becomes V_D at the drain side. As

a result of this situation, voltage difference affecting channel at the drain side becomes $V_G - V_D$. Now, channel charge density at any point along the channel becomes

$$Q_d = WC_{ox}(V_{GS} - V_x - V_{th}), \tag{3.4}$$

where V_x represents voltage difference at point x.

Now, drain current can be calculated by using (3.2) and (3.4) as

$$I_d = -WC_{ox}(V_{GS} - V_x - V_{th})v, \tag{3.5}$$

where v represents the velocity of the electrons and defined as

$$v = \mu E. \tag{3.6}$$

Here, μ is the mobility of the charge carriers and E is the electric field in the channel due to V_D. These two components determines the velocity of the charges in the channel. Since the electric field created in the channel is $E = -\frac{dV}{dx}$, we can obtain the new drain current equation as

$$I_d = \mu WC_{ox}(V_{GS} - V_x - V_{th})\frac{dV}{dx}, \tag{3.7}$$

As explained above, voltage difference at the beginning of the channel is zero, and at the end of the channel is V_D, so drain current can be computed as

$$\int_0^L I_d dx = \int_0^{V_{DS}} \mu WC_{ox}(V_{GS} - V_x - V_{th})dV \tag{3.8}$$

which is solved as

$$I_D = \mu\frac{W}{L}C_{ox}[(V_{GS} - V_{th})V_{DS} - 0.5V_{DS}^2], \tag{3.9}$$

where L is the channel length.

The maximum current, I_{Dmax} occurs at $V_{DS} = V_{GS} - V_{th}$ as

$$I_{D,max} = 0.5\mu\frac{W}{L}C_{ox}(V_{GS} - V_{th})^2. \tag{3.10}$$

Actually these concepts can be better understood with an analogy from the real world. The famous water analogy makes the I_D and I_{Dmax} concepts clearer

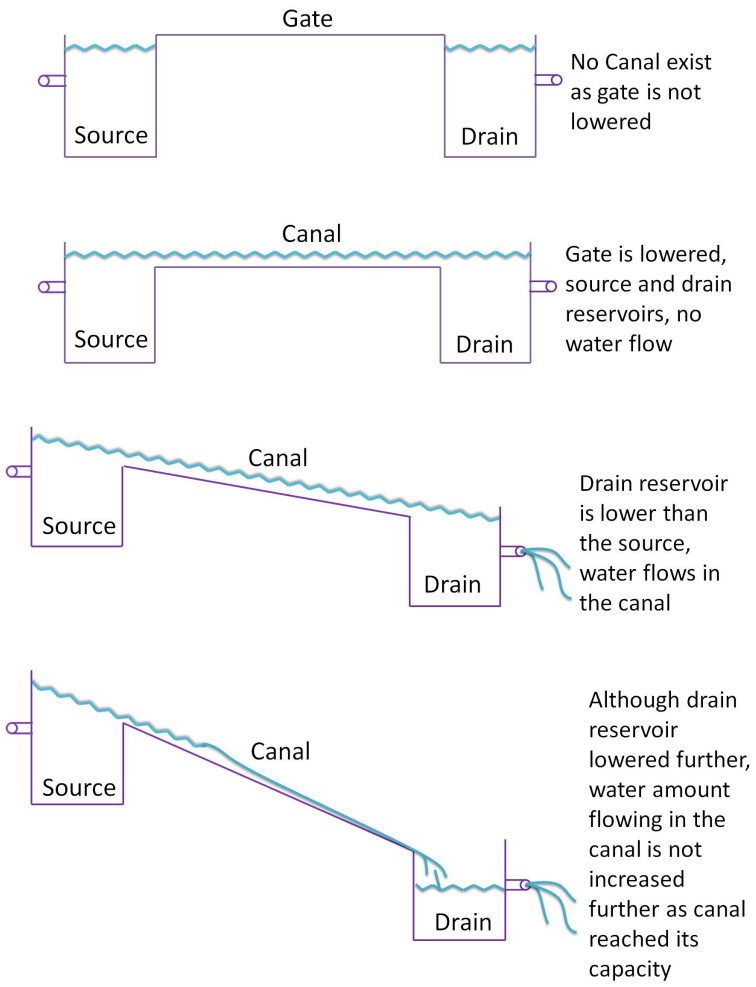

Figure 3.5: Water analogy of the transistor behavior

to understand. In the water analogy (simply illustrated in Fig. 3.5), the mobile carriers can be thought as water droplets. Source and drain can be modeled as deep reservoirs and the channel can be modeled as a water canal. When V_{GS} is not higher than V_{th} no channel forms as gate is not lowered in the analogy. When the source and drain reservoirs are at the same level, there will be no water flow in the canal. However, when the drain reservoir becomes lower than the source reservoir, water starts to flow from source reservoir to drain reservoir through the canal. The amount of water flow is limited with the canal capacity in this case. This means that further decreasing the drain reservoir cannot increase the amount of water flowing through the canal when the water flow is saturated due

to the canal capacity. The same concept also applies in physical transistors, so water analogy can be used to understand the transistor principles.

When we combine all the information about the transistor basics, we obtain a transistor, that will be fundamental part of a memory device in the following sections for this thesis (a basic n-channel transistor is illustrated in Fig. 3.6).

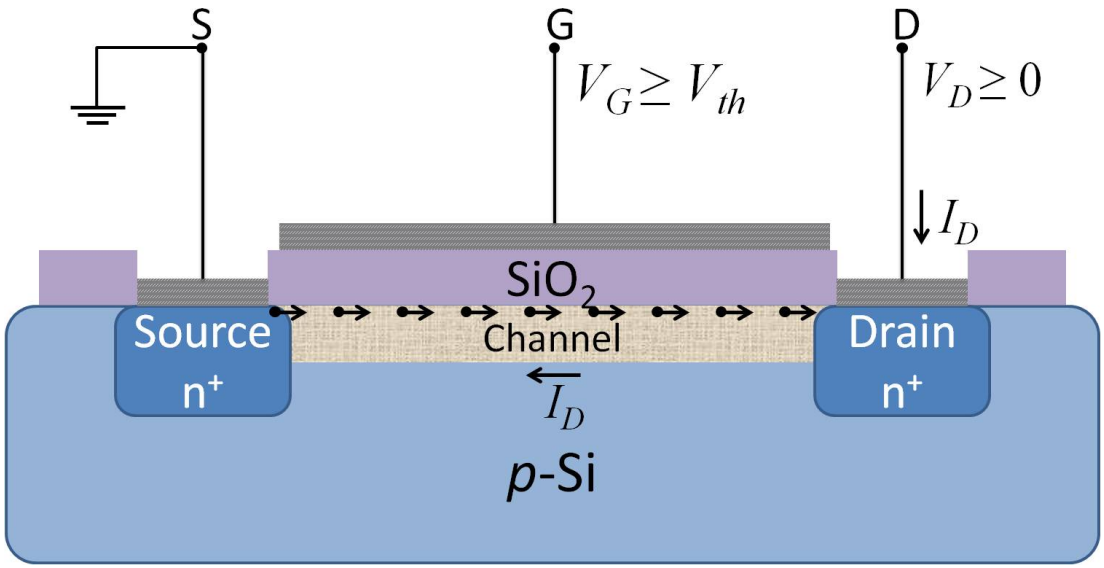

Figure 3.6: Basic n-channel transistor structure

3.3 Memory Basics

In this section, our goal is to give some background information on memory basics for transistors. Since the goal of this thesis is to build novel memory devices, a good understanding of the memory operations in transistors is crucial.

3.3.1 Basic Memory Cells Overview

Memory devices has a key role in almost all modern electronic devices, such as cell phones, personal computers, digital cameras, automotive systems, etc. Nowadays, memory capabilities of a device has a significant impact on the consumer

preferences and there is an increasing interest in building memory devices with higher storage capability and stability.

Recently, we are able to fabricate transistors on the order of tens of nanometers for memory and logic operations [17]. Achieving such a small scale in transistors increases our ability to store large amounts of data in smaller devices. However, increasing use of electronic devices also increases the amount of produced data. Therefore, we still need to conduct more research for developing new memory devices using novel materials and structures to achieve greater scalability, lower cost and higher storage capability.

3.3.2 Basic Nonvolatile Memory Cell Structure

In this part, we will start describing the basic nonvolatile memory cell structure. The memory cell structure is very similar to the MOSFET structure described in Section 3.2 with an additional layer embedded in the oxide layer for charge storage and retention. The basic structure of the memory cell based on a MOSFET is illustrated in Fig. 3.7.

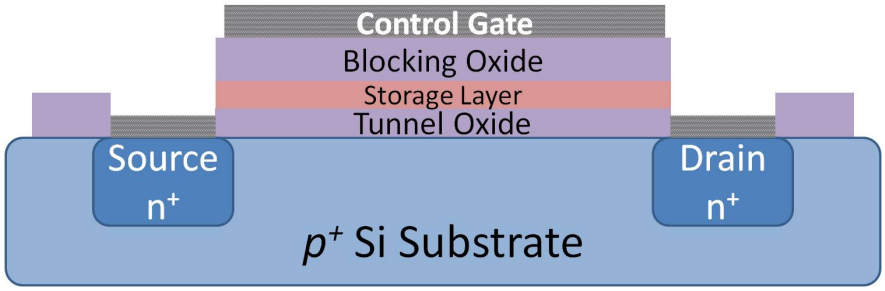

Figure 3.7: Basic nonvolatile memory cell structure

The storage layer in the transistor structure consists of a highly doped poly-silicon in the case of a floating-gate type memory but it is conventionally a nitride layer in the case of a charge-trapping memory. The blocking oxide and tunnel oxide layers are mostly SiO_2 due to being a high band gap ($9eV$) insulator and its excellent interface properties with Si. The main difference between them is blocking oxide layer is thicker than the tunnel oxide layer to prevent charge

leakage to the control gate, while tunnel oxide permits charge tunneling to the storage layer under the effect of a high electric field.

3.3.3 Basic Nonvolatile Memory Cell Operation

In this part, we will discuss the basic memory cell operation by describing them in the context of the previously defined transistor structure. The first memory operation we will focus on is the programming operation, where we write information to a transistor as illustrated in Fig. 3.8.

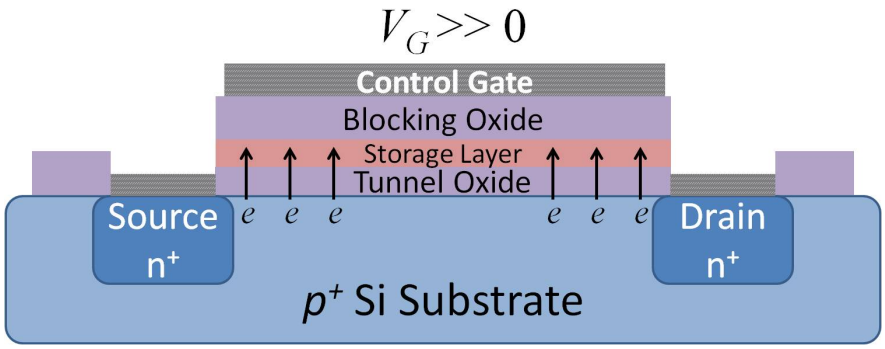

Figure 3.8: Programming of the memory device by applying a high positive gate voltage

In order to program the memory cell, we apply a high positive voltage at the gate, so that the electrons in the substrate channel will tunnel through tunnel oxide to the storage layer and will be trapped there, since they will be blocked by the blocking layer. Even if we remove the voltage at the gate, the electrons cannot tunnel through the tunnel oxide, since there will be no electric field to enable them pass through and they will be trapped in the storage layer until we apply a reverse voltage to the gate. This is how the memory devices can store an information.

The second operation we will discuss is the erase operation, which is mainly the inverse of the programming operation. When a high negative voltage is applied at the gate, the electric field repels the electrons in the storage layer and they tunnel through the tunnel oxide layer to go back to the substrate channel. After

this operation, the storage layer goes back to its neutral state, meaning that the stored information is erased from the memory. The electron transfer during the erase operation is also illustrated in Fig. 3.9.

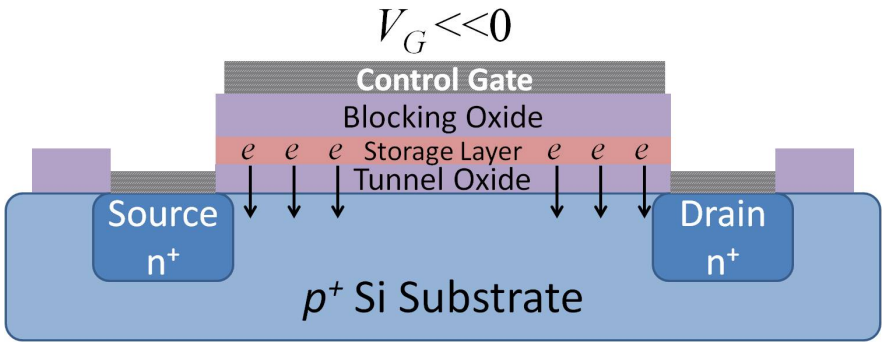

Figure 3.9: Erase operation of the memory device by applying negative gate voltage

The final state we will describe is the retention state, where no voltage is applied on the gate and electrons are trapped in the storage layer as shown in Fig. 3.10. Although ideally we do not desire any electron loss in the storage layer during the retention period, considerable amount of electrons may pass through tunnel oxide due to some defects in the memory device and unintentional back tunneling from the oxides. This is one of the main setbacks of the memory cells and we will analyze the electron loss of the developed memory cells in the following chapters.

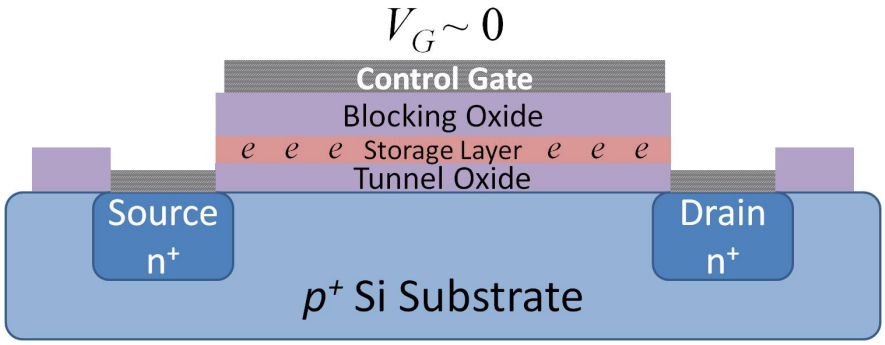

Figure 3.10: Retention state of the memory device with no applied gate voltage

The basic nonvolatile memory behavior is also shown in Fig. 3.11, where we can observe the drain current (I_{Drain}) with respect to the gate voltage (V_G). The

graph shows the charged and uncharged states of the memory device, where the electrons are trapped in the storage layer and where the memory is erased and electrons are removed from the storage layer, respectively. In this notation, $'0'$ represents the charged state and $'1'$ represents the uncharged state of the memory device.

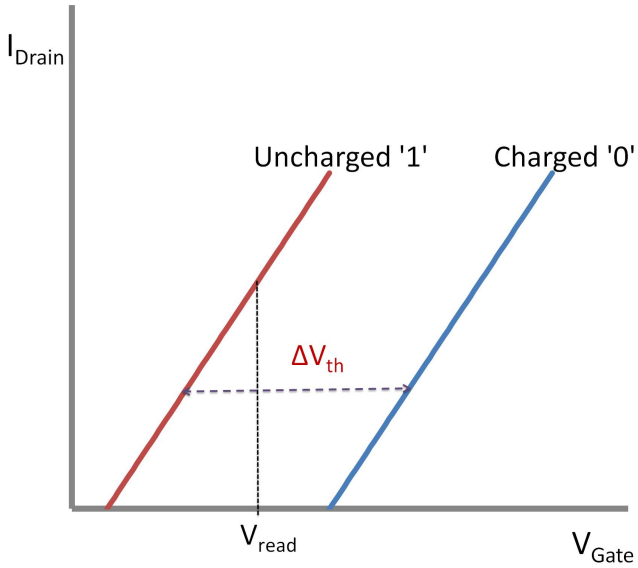

Figure 3.11: $I_D - V_G$ characteristics of a memory device.

The read operation is performed by applying a positive read voltage to the gate, V_{read}, and measuring the drain current. When it is charged, the threshold voltage, V_t, shifts towards right, so I_D changes according to (3.9), even the applied gate voltage is the same. The difference in the drain current between the charged and uncharged states is an indicator of the memory state [18, 19].

The threshold voltage of the memory can be computed using the following equation

$$V_t = V_{FB} - 2\phi_P + \frac{t_{ox}}{\epsilon_{ox}}\sqrt{2\epsilon_{Si}N_D(2\phi_P)}, \tag{3.11}$$

where ϕ_P is the potential of the Si substrate, t_{ox} is the thickness of the oxide, N_D is the doping of the substrate, ϵ_{ox} and ϵ_{Si} are the oxide and Si dielectric constants, and V_{FB} is the flat-band voltage given by

$$V_{FB} = \phi_m - \phi_s - \frac{t_{cntrl}Q_s}{\epsilon_{ox}}, \tag{3.12}$$

where ϕ_m and ϕ_s represents the work functions of the metal and MOS channel, respectively. Additionally, Q_s represents the areal density of a sheet charge located at a distance t_{cntrl} from the gate electrode.

When the memory is programmed, storage layer traps the electrons, the stored electron charge Q shifts the $I_D - V_G$ characteristics of the memory to the right by a voltage ΔV_t, which depends on the charge with the following relation

$$Q = \frac{C_t \Delta V_t}{q}, \tag{3.13}$$

where C_t represents the capacitance of the MOS memory per unit area and ΔV_t is the voltage shift [10]. As it seen from the (3.13) threshold shit is directly proportional to the amount of stored charge and inversely proportional to the capacitance of MOS memory, so it is important to store as much as charge in a small volume. Although the programming operation shifts the threshold voltage, erasing operation shifts it back to its original value as it removes stored charge from trapping layer, so write-erase operations are reversible.

3.3.4 Nanoparticles for Charge Storage

The increasing interest for the reliable and high capacity devices requires high density, low power consuming and low cost memory cells. Actually, programming and erasing phases of the floating-gate devices can be accelerated by reducing the tunnel oxide layer thickness below 2.5 nm, which would result in 100 ns programming and erasing times with an acceptable voltage below 10 V [20]. However, as a drawback of the thinner tunnel oxide, the retention time of the memory cell will be also reduced and increasing stress-induced leakage currents will reduce it further, resulting in an unreliable memory device. The problem of using thick tunnel oxide layers for reliable data operations is that they require high operating voltage and cause slow write-erase operations.

Embedding nanoparticles in the oxide have been proposed as a solution to this problem [21]. The main benefit of the embedding nanoparticles is that if a defect occurs in the tunnel oxide, nanoparticle based memories will only discharge the

charge on the nanoparticles present around the defect, while floating-gate devices will be totally discharged. This great feature of nanoparticles enable the use of thinner tunnel oxide layers, and consequently, lower operating voltages and higher speeds without compromising the good retention time (> 10 years).

3.3.5 Electrical Properties of Silicon Nanoparticles

As explained in the previous section, embedding of nanoparticles has some clear advantages to accelerate write/erase process while keeping the retention time in an acceptable level. In this part, we will discuss the use of silicon-based nanoparticles for this purpose. In the literature, majority of the silicon based nanoparticle embedding studies are based on Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) memory devices with $\geq 5nm$ silicon nanoparticles that exhibit bulk-like trapping characteristics [22, 23]. However, the fascinating speed of technology development demands better solutions that require nanoparticles of sub $3nm$ dimensions, which is actually a zero-dimensional regime.

Actually, decreasing the nanoparticle size has some effects on the structural and electrical characteristics of the particle. For example, when size of the nanoparticle is reduced, the bandgap increases due to quantum confinement in $0 - D$ [24], the dielectric constant decreases [25], their work-function increases [26], and electron affinity decreases [26].

In addition to above changes, the charging energy increases with decreasing size of the nanoparticle. The energy required to add a single electron or hole to the nanoparticle is represented by coulomb charging energy as

$$E = \frac{q^2}{C}, \tag{3.14}$$

where q is the coulomb charge and C is the capacitance of the particle. For nanoparticles (small conductors), it is convenient to compute the capacitance C by assuming that the conductor is a sphere of radius R. Since the capacitance is $C = Q/V$, we first compute V for the sphere. By using Gauss' law, the potential

at a point with radius r from the center of the sphere is given by

$$V = \frac{Q}{4\pi\epsilon r}. \tag{3.15}$$

Assuming the potential at infinity is zero, the potential of the sphere is computed as

$$V = \frac{Q}{4\pi\epsilon R}. \tag{3.16}$$

Now, we can compute the capacitance as

$$C = \frac{Q}{V} = 4\pi\epsilon R. \tag{3.17}$$

These calculations yield a Coulomb charging energy of silicon particles of size $2-nm$ as $1.1eV$. As a summary we can say that when the size of the nanoparticle decreases to the nm range, its charging energy increases and becomes higher than the room temperature thermal energy of $25meV$.

3.4 Summary

This chapter builds the necessary background for this thesis by explaining the memory devices starting from the basic MOS structure and continuing with the transistor and memory structures. We detail the concepts of simple transistor processes and their usage as memory cells. Then, we explained the memory concepts such as programming, erasing and retention of the memory information. As a concluding remark of this chapter, the use of nanoparticles for memory cells and their electrical characteristics is also represented.

Chapter 4

Graphene Based MOSCAP Memory

This chapter introduces our work for enhancing memory effect with embedded graphene nanoplatelets in ZnO charge trapping layer. We describe the fabrication processes, discuss the device characterization and analyze its memory behavior.

4.1 Introduction

The tremendous growth in the consumer electronic market such as smart phone, tablet, mobile devices and cameras increased the attention of researchers to build novel memory chips with low-cost, low-power consumption and high density [7, 8]. However, reliability and retention requirements bring a major limitation on developing high density and scaling of the gate length in current nonvolatile flash memory devices. Therefore, we require novel structures and materials to be incorporated in the memory cells, which will allow us to build high density but low-power memory devices.

The goal of this chapter is to utilize graphene, a single layer of two-dimensional

($2D$) sheet of carbon atoms arranged in a honeycomb lattice [1], and to investigate its characteristics as a memory device. Graphene is a two dimensional material and it exhibits exceptional characteristics such as high carrier mobility, large work-function, thermal conductivity, structural robustness and optical transparency [27, 28]. These great features attracted great efforts and research on studying graphene as a promising material in electronics as well as nonvolatile memory devices.

The existing works in the literature demonstrated the use of graphene oxide as a flash memory with large memory window and low operating voltage [29]. In this study, graphene oxide has been used as the floating gate of the memory. However, floating gate type memory is less efficient and has a single point of failure such as a possible defect in the tunnel oxide causes all the stored charge in the floating gate to leak out. Motivated by this problem, we demonstrate the use of graphene nanoplatelets embedded in a ZnO layer (GNIZ) as the charge storage media in charge trapping memory devices. We also compare the performance of this device with the control devices with only ZnO or graphene nanoplatelets (GN) with a thicker tunnel oxide. Thus, we can observe the effect of GNIZ on the retention and endurance characteristics of the memory.

4.2 Graphene Nanoplatelets

This section is devoted to giving some background information on our graphene nanoplatelets and general information about the advantages of graphene.

Graphene is a single layer of carbon atoms as a very thin, nearly transparent sheet. The most attractive properties of graphene is remarkably strong for its low weight and it conducts electricity and heat with great efficiency. The graphene has unique band diagram where there is no band-gap between valence and conduction bands and band diagram near K points (also called Dirac points) for low Fermi energies ($< 1eV$) shows linear cone shaped dispersion characteristic, unlike parabolic-like dispersion characteristic of ordinary semiconductors (see Fig.

4.1). In undoped single layer $2D$ graphene, the Fermi level passes through those K points [1, 30]. This unique band structure gives to graphene extraordinary electrical and optical properties. Since its first reliable production in 2004, the interest in using graphene in different applications increased quite rapidly.

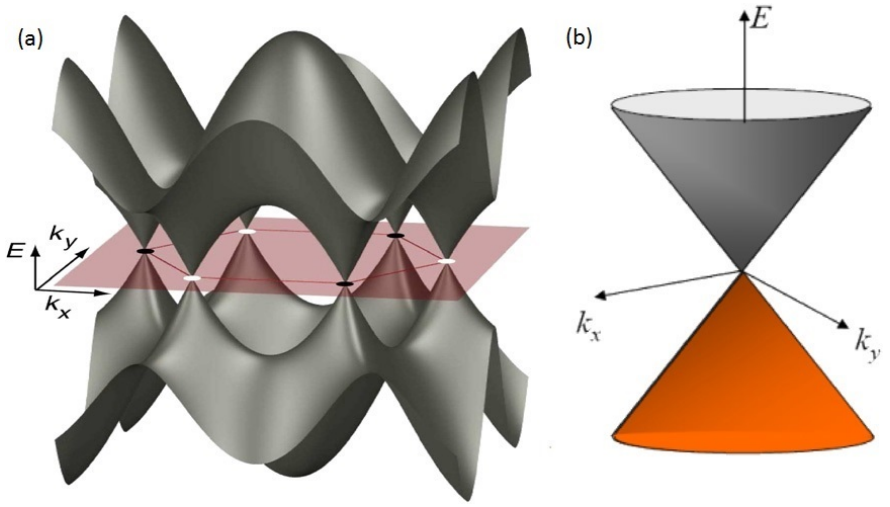

Figure 4.1: (a) Graphene band structure. (b) Magnified low-energy dispersion at one of the K points shows the electron-hole symmetric Dirac cone structure [1].

Graphene has a large application area such as medical devices (development of fast and efficient bioelectric devices with its high electric conductivity and thinness), electronics (development of LCD touchscreen thanks to its transparency), photovoltaics (low levels of light absorbed by graphene may enable it to become a cheaper alternative to silicon in photovoltaics) and storing electricity (will probably decrease charging time). Motivated by these large application areas of graphene due to its exceptional properties, our goal is to utilize graphene nanoplatelets for building low-cost and low-power memory cells.

In this work, we use pristine graphene nanoplatelets (NanoIntegris PureSheets Quattro grade). The graphene nanoplatelets we use has a graphene concentration of $0.05mg/mL$. The AFM analysis presented at product technical datasheet illustrates the flake area histogram for our graphene nanoplatelets in Fig. 4.2.

Fig. 4.3 shows an AFM image of several pristine graphene flakes on an SiO_2 substrate. The details about the use of graphene flakes in memory cell will be described in detail in the following section.

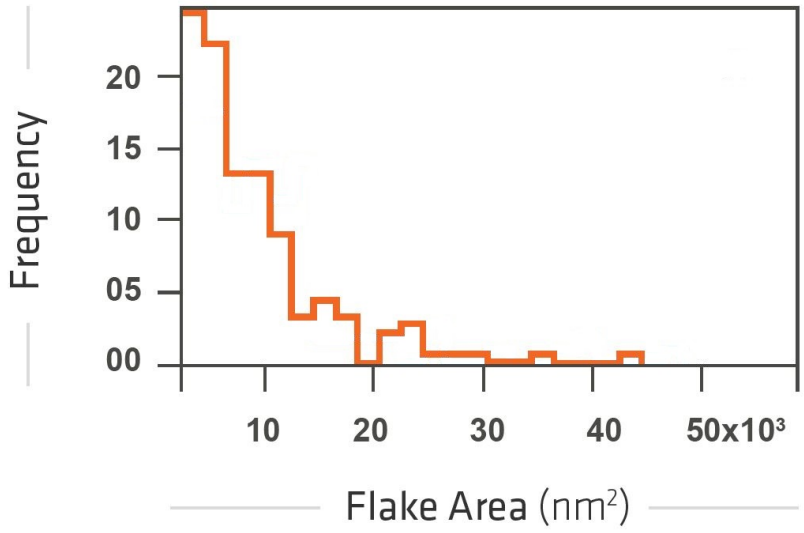

Figure 4.2: Flake area histogram for NanoIntegris PureSheets Quattro compiled by AFM analysis [2].

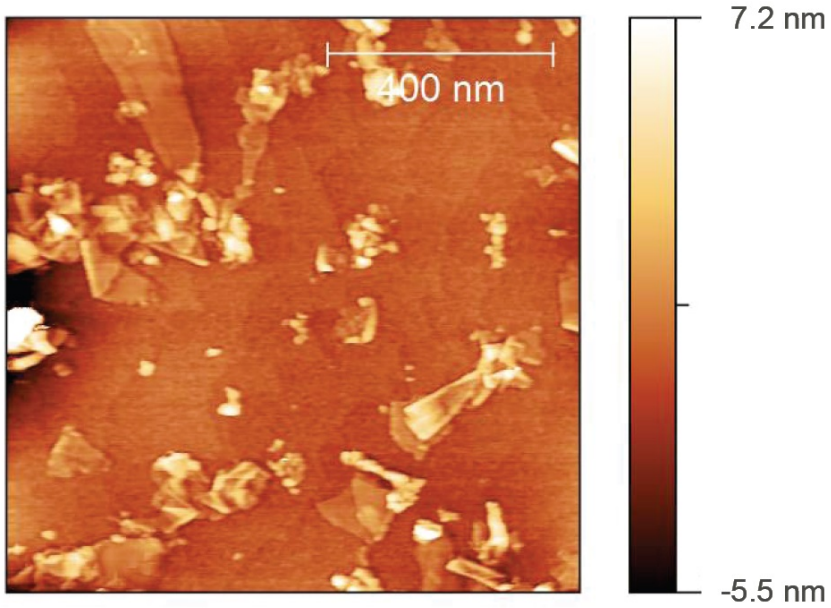

Figure 4.3: AFM image of several pristine graphene flakes on an SiO_2 substrate [2].

4.3 Fabrication

The MOS memory cells are fabricated on an $n^+ - type$ (111) (Antimony doped, 15-20 $m\Omega - cm$) Si wafer. The step by step procedure of the fabrication process is given below:

- 3.6-nm-thick Al_2O_3 tunnel oxide followed by 2-nm-thick ZnO are deposited at 250^oC using Cambridge Nanotech Savannah-100 ALD systems described in Section 2.5.
- Pristine graphene nanoplatelets (NanoIntegris PureSheets Quattro grade) are deposited by drop-casting technique.
- Samples are placed on hot-plate at 110^oC and $2 - 2.5$ ml of $0.05mg/ml$ graphene solution is drop-casted slowly by using plastic pipette and samples are left to dry for five minutes on hot plate.
- 2-nm-thick ZnO fallowed by 15-nm-thick Al_2O_3 blocking oxide is also ALD deposited at 250^oC.
- As a final step, 400-nm-thick Al layer with a diameter of 1 mm is sputtered using a shadow mask for the gate contact.

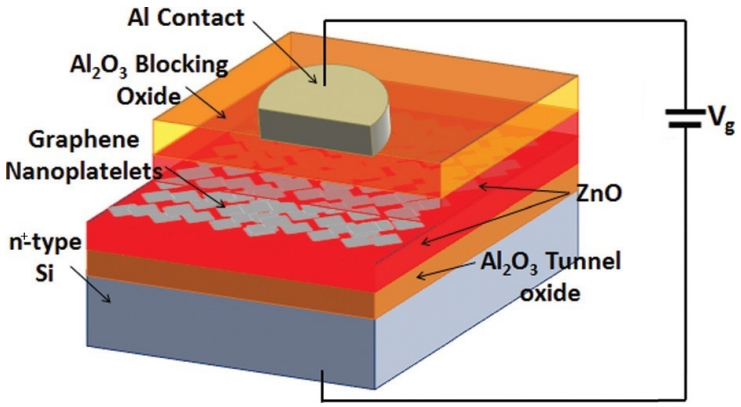

Figure 4.4: Cross sectional illustration of the fabricated MOS memory with GNIZ [3].

A cross-sectional illustration of the fabricated memory MOSCAP device structure is depicted in Fig. 4.4. Note that, structure of the control device with only GN is fabricated the same way but with a 5-nm-thick tunnel oxide.

4.4 Characterization

4.4.1 Gate Voltage Sweep Behavior

The goal of this section is to analyze the charging effect in the fabricated memory cells by studying the high frequency (1 MHz) $C-V_{Gate}$ curves of the programmed and erased states. For this purpose, the gate voltage of the memory cells is swept between -12 and $12V$ backward and forward by using Agilent-Signatone B1505A device analyzer. The measurements are performed on the devices with GNIZ, GN, and ZnO charge trapping layers, and the resulting memory hysteresis shows a $6.5V$, $5.5V$, and $0.9V$ V_{th} shift, respectively. Fig. 4.5 illustrates the high frequency $C-V$ measurement at $12/-12V$ for GNIZ memory structure, illustrated in Fig. 4.4.

The observed positive shift of the V_{FB} of the erased state in Fig. 4.5 indicates that a significant amount of electrons trapped at the interfacial or in the oxide layer. Actually, the decrease in the capacitance with the decrease in applied gate voltage is an indicator of the n-type Si substrate and n-type ZnO layer due to crystallographic defects such as interstitial zinc and oxygen vacancies [31, 32, 33, 6, 34, 5, 35]. Additionally, the gate voltage sweep from $12V$ to $-12V$, results in a positive shift in the $C-V$ curve. This positive shift indicates that the memory is being programmed by trapping electrons in the charge storage layer.

In order to make a fair comparison, the $C-V$ hysteresis measurement is repeated on the three fabricated devices GNIZ, GN, and ZnO at different sweeping voltages. In Fig. 4.6 the resulting V_{th} shifts for GNIZ, GN, and ZnO are plotted and they show that GNIZ memory device provides the largest memory window among the three memory devices. The main reason behind this is that GNIZ

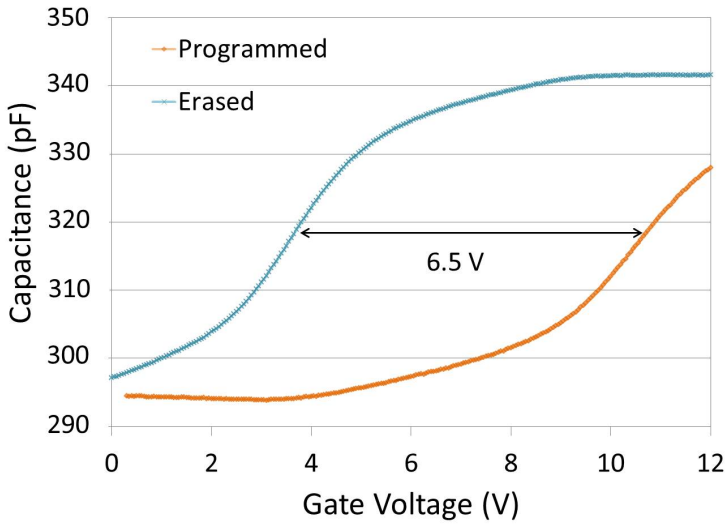

Figure 4.5: C-V measurement at 12/-12 V (forward and backward) of the memory with GNIZ. The measurement is done at room temperature.

memories have thinner tunnel oxide, which exponentially increases the charge emission and tunneling probability in addition to the additional trap states provided by the ZnO.

Another interesting result in Fig. 4.6 is that the memory with only ZnO layer does not provide a remarkable V_{th} shift even at high sweeping voltages $(12/-12V)$. This indicates that ZnO in the GNIZ structure provides few additional trap states. However, the usage of ZnO in the GNIZ structure mainly enhances the electron retention in the graphene nanoplatelets by reducing the charge back-tunneling probability.

Assuming that ZnO provides only few additional trap states, the filled charge trap states density of the graphene nanoplatelets can be calculated by adopting the following equation [5, 35, 36]:

$$N_{trap} = \frac{C_t \times \Delta V_{th}}{q}, \tag{4.1}$$

where C_t is the capacitance of the memory per unit area, ΔV_{th} is the V_{th} shift, and q is the elementary charge. The filled charge trap density is roughly about

$1.08 \times 10^{12} cm^{-2}$ at $6/-6V$ sweeping voltage, with a $4V$ V_{th} shift, and C_t is $43.31 nF/cm^2$.

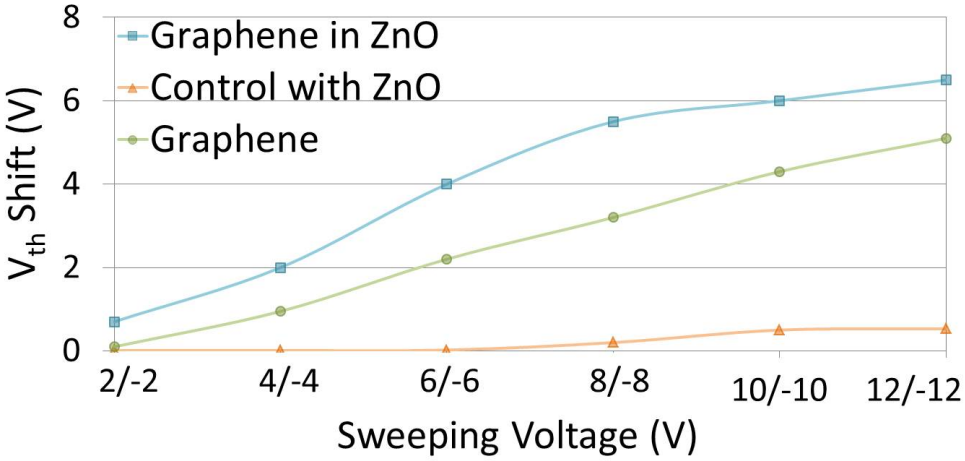

Figure 4.6: Measured V_{th} shifts at different gate voltage sweep for the three memory structures.

4.4.2 Retention Characteristics

In additional to the characterization of V_{th} shift vs. gate voltage sweep, we also investigated the retention characteristics. For this purpose, the V_{th} shift of the new programmed memory cell is measured at room temperature and degradation of it with time is plotted in Fig. 4.7. Normally, the thinner tunnel oxides cause a degraded retention characteristics in the memory cells. However, although the memory with GNIZ has a $1.4nm$ thinner tunnel oxide (28% thinner), it shows an improved retention characteristics, where the extrapolation to 10 years indicates a loss of 25% of the stored charge in the GNIZ memory as compared to 29% loss in the GN memory. The retention measurements show that the use of ZnO in the charge storage media allows for further scaling of the tunnel oxide thickness without degrading the retention performance of the memory.

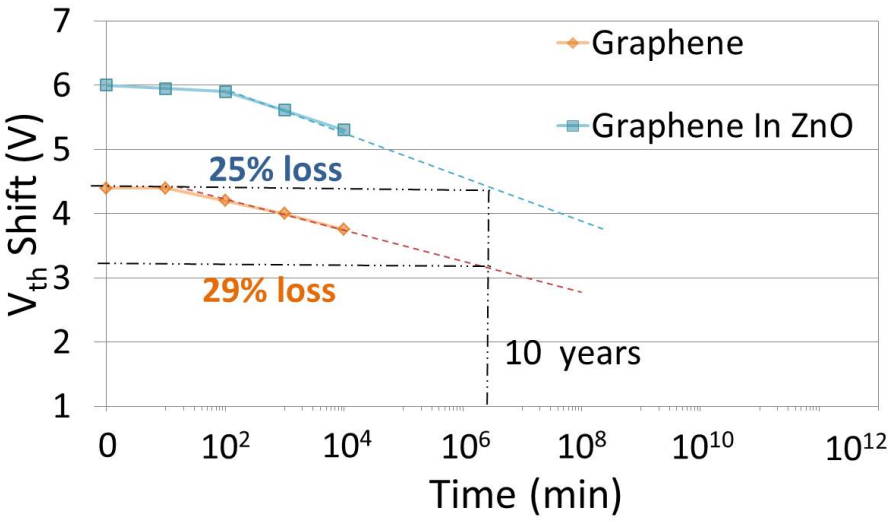

Figure 4.7: V_{th} shift vs. time extrapolated to 10 years with GNIZ and GN charge trapping layer.

4.4.3 Endurance Characteristics

In this part, we study endurance performance of the memories with GNIZ and GN charge trapping layer. In order to measure the endurance characteristics of the memories, a fresh memory cell hysteresis is measured at room temperature at $10/-10V$ forward and backward up to 10^4 cycles. The resulting threshold voltage shift vs. number of hysteresis measurement cycles is illustrated in Fig. 4.8. A slight reduction in threshold voltage after 10^4 cycles proves that the memory cell has a good endurance. In addition to these, we observe the benefit of integration of ZnO to the charge trapping layer, since GNIZ shows an improved endurance with respect to GN with a V_{th} shift reduction by 13.3%, while it is 17% in GN after 10^4 memory hysteresis cycles.

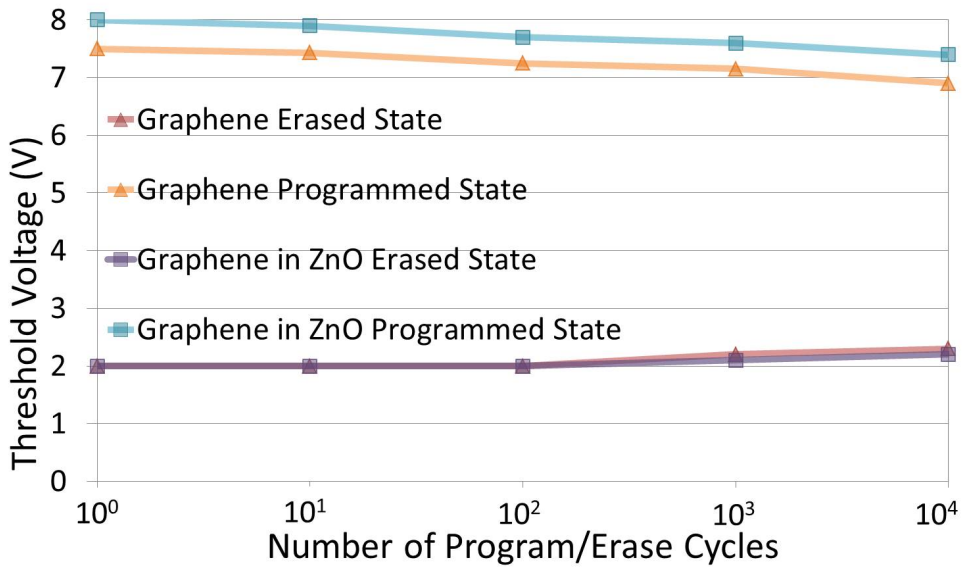

Figure 4.8: Endurance measurement showing threshold voltage shift vs. number of hysteresis measurement cycles.

4.4.4 Analytical Discussions

Fig. 4.9 illustrates the energy band diagram of the memory structure with GNIZ using the reported work-function, electron affinities, and band-gap of the used materials [32, 37, 38]. Since the conduction band offset between the Si substrate and tunnel oxide is smaller than the valance band offset, electron emission probability is higher. This was also observed in Fig. 4.5, where the positive shift of the programmed state indicated electron storage in the charge trapping layer.

As explained in Section 4.4.1, ZnO provides only few additional trap states. Due to this fact, the majority of the electrons are expected to tunnel through tunneling oxide to the ZnO layer and then be swept by the electric field and get trapped within the graphene nanoplatelets. In this structure, ZnO brings an additional potential barrier step, which reduces the probability of back-tunneling. Similarly, large conduction band offset between graphene and the tunnel oxide improves the retention characteristics by reducing the probability of back-tunneling. This theoretical analysis is also experimentally validated in Fig. 4.7.

The electric field across the tunnel oxide of the memory with GN is calculated

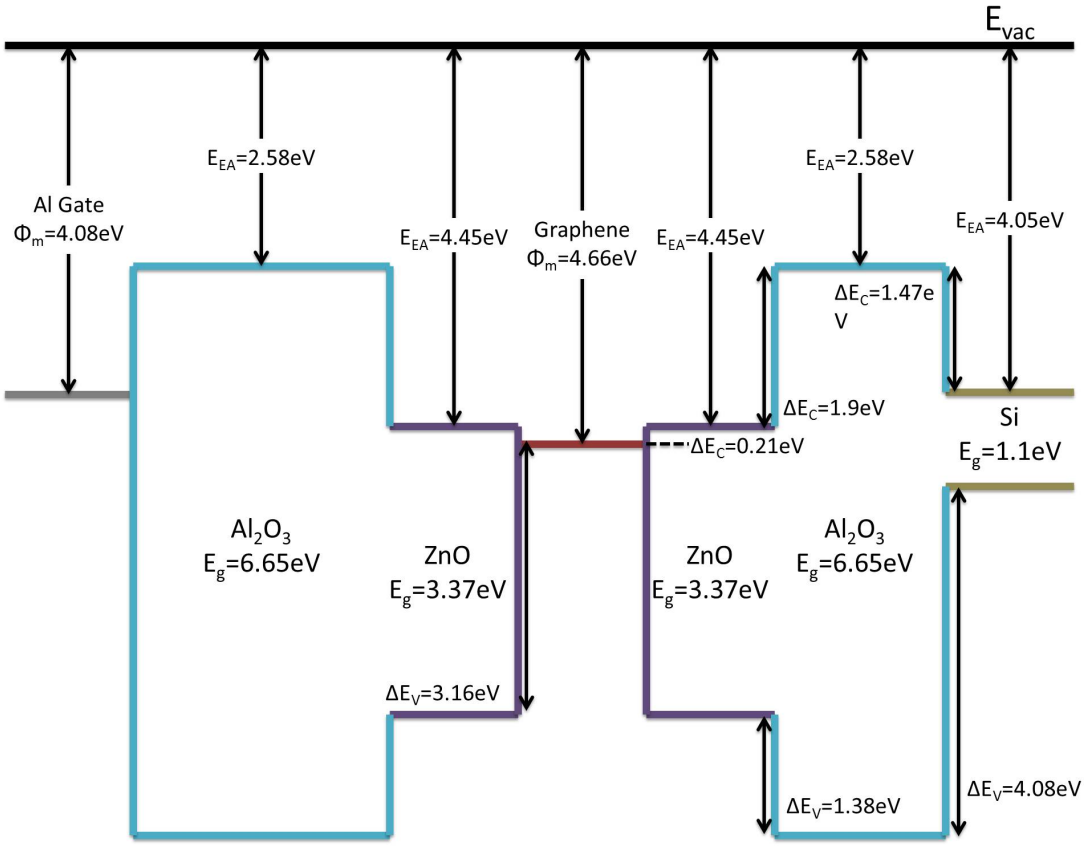

Figure 4.9: Energy band diagram of the memory with GNIZ charge trapping layer. The large conduction band offset between graphene and tunnel oxide exponentially reduces the charge leakage.

using the Gauss's law: [10]

$$\epsilon_1 E_1 = \epsilon_2 E_2 + Q, \tag{4.2}$$

$$V_g = V_1 + V_2 = d_1 E_1 + d_2 E_2, \tag{4.3}$$

where ϵ is the dielectric permittivity, E is the electric field in the oxide, Q is the stored charge in the graphene nanoplatelets, V is the voltage across the oxide, d is the oxide thickness, and subscripts 1 and 2 correspond to the tunnel and blocking oxides, respectively. By using (4.2) and (4.3), the resulting electric field in the tunnel oxide can be calculated as

$$E_1 = \frac{V_g}{d_1 + d_2(\frac{\epsilon_1}{\epsilon_2})} + \frac{Q}{\epsilon_1 + \epsilon_2(\frac{d_1}{d_2})}. \tag{4.4}$$

Now, our goal is to understand the tunneling mechanism in the memory cells

under the effect of applied electric field. Fig. 4.10 shows the natural logarithm of the V_{th} shift divided by the square of the electric field vs. the reciprocal of the electric field. The linear trend indicates that the dominant electron emission mechanism at an electric field $E \geq 5.57MV/cm$ (corresponding to a 6V gate voltage) in the tunnel oxide is Fowler-Nordheim (F-N) tunneling.

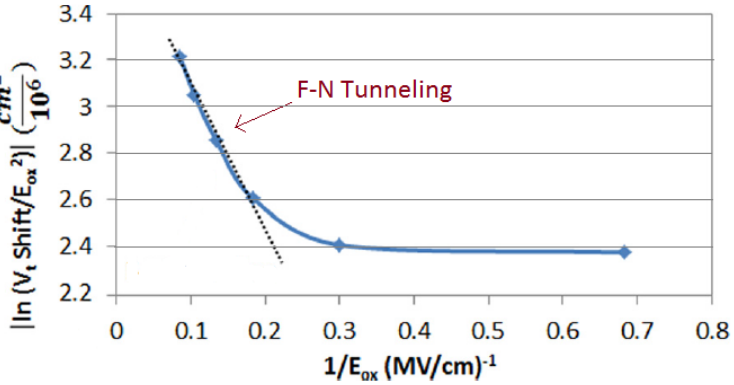

Figure 4.10: Plot showing the natural logarithm of the V_{th} shift divided by the square of the electric field is plotted vs. the reciprocal of the electric field. The linear trend indicates that Fowler-Nordheim is the dominant emission mechanism at an oxide electric field of $5.57MV/cm$ [3].

The F-N tunneling mechanism works as follows. First, the charges are injected by tunneling into the conduction band of the oxide through a triangular energy barrier. Then, they are swept by the electric field into the charge trapping layer. The emission rate of charges in F-N tunneling follows the equation: [10]

$$J = C_1 E_{ox}^2 e^{-\frac{C_2}{E_{ox}}}, \tag{4.5}$$

where J is the F-N tunneling current, E_{ox} is the electric field across the tunnel oxide, and C_1 and C_2 are constant terms of the effective mass and barrier height.

Note that all of the above calculations about the electric field was for GN not for GNIZ. The addition of ZnO to the charge storage media will definitely affect the electric field. Since the ALD ZnO is n-type, the electric field across the tunnel oxide is expected to be smaller than it was in the GN structure. However, in the case of GNIZ memory, the tunnel oxide thickness is $1.4nm$ thinner, which would increase the electric field linearly and electron tunneling probability exponentially.

Based on our observations in Fig. 4.6 (larger V_{th} shifts obtained with GNIZ), the electric field and tunneling probability through the tunnel oxide is expected to be larger in GNIZ case with respect to GN.

In CMOS technology, F-N is considered as the tunneling mechanism that requires the highest electric field [39, 40]. Therefore, F-N tunneling is expected to be the dominant electron emission mechanism in the GNIZ memory as well. Since F-N tunneling is independent of temperature [41], the retention of MOS memory structure with graphene-flakes embedded in ZnO is also expected to be independent of temperature. This situation was demonstrated in [41], where retention of MANAS (Metal-Al_2O_3-Nitride-Al_2O_3-Semiconductor) memory device, whose main mechanism is F-N tunneling, is independent of temperature.

4.5 Summary

In this chapter, the use of graphene nanoplatelets as the charge storage agents in charge trapping memory is demonstrated. The theoretical analysis and memory characterization experiments showed that use of a thinner tunnel oxide and the addition of ZnO to charge storage media showed an improved performance the memory, where $4V$ V_{th} shift is achieved at $6/-6V$, with an expected loss of 25% of stored charged after 10 years, and an endurance greater than 10^4 memory hysteresis cycles. The emission mechanism in such memory devices are found to be dominated by Fowler-Nordheim (F-N) tunneling (at electric fields higher than $5.57MV/cm$). As a result of all the aforementioned advantages and characterization results, this work shows that graphene nanoplatelets are a promising candidate for charge trapping layers in future low-power and low-cost nonvolatile memory devices.

Chapter 5

InN Based MOSCAP Memory

In this chapter, we introduce our work for enhancing memory effect via quantum confinement of charges in $16nm$ InN nanoparticles embedded in ZnO charge trapping layer. I will describe the fabrication processes, discuss the device characterization and analyze its memory behavior.

5.1 Introduction

The indium-nitride nanoparticles (InN-NPs) have some excellent optoelectronic properties such as high electron mobility, high saturation velocity due to low effective mass of charge carriers [42, 43], small band gap, terahertz/near-infrared emission, and high surface accumulation [44, 45, 46]. Emerging advantages of InN nanoparticles with respect to other materials, based on the aforementioned material properties, increased the interest for utilizing InN-NPs in different application areas.

One of the distinguishing property of InN-NPs is that they have the largest electron affinity among all semiconductors, which is estimated to be $5.5 - 6.1eV$ with respect to the vacuum level [47, 48]. The large electron affinity is a desired property for charge trapping materials in memory devices, since it affects the

retention performance of the memory device. The large electron affinity increases the energy barrier for electrons stored in InN-NPs, which exponentially reduces the charge leakage. That is why InN-NPs can improve the retention characteristics of the charge trapping memory cell.

One of the expected advantage of using InN-NPs in memory cells is to improve the retention characteristics of the charge trapping memory. However, tunnel oxide thickness and material have great impact on memory performance. Therefore, in order to make a fair comparison of InN nanoparticles performance directly with other materials, the gate stack of the memory structure has to be similar. Actually, in a previous work in our lab [33], a charge trapping memory with $2nm$ Si nanoparticles embedded in ZnO was demonstrated. The memory showed hole trapping with a 41% loss of the initial charge in 10 years and a reduced operations voltage. In fact, the very small electron affinity of the Si-NPs supports the observed results.

In this work, we aim to demonstrate the performance of the memory with laser-synthesized InN-NPs, which have a much larger electron affinity as compared to Si-NPs. Similar to memory device in Chapter 4, n-type ZnO grown by atomic layer deposition (ALD) [31, 32, 6, 34, 35] is also used as charge trapping layer in this memory device. Then, charge trapping characteristics of InN-NPs are explored using high frequency $C - V_{Gate}$ measurements on MOS charge trapping memory cells. The following sections describe the fabrication process of the memory device and its performance results as well as the theoretical memory behavior analysis.

5.2 Indium Nitride Nanoparticles: Preparation

This section briefly explains the preparation steps of InN-NPs. Currently, metal-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy are being used for growing high quality indium nitride at low pressures. However, this work concentrates on nanoparticle generation with laser ablation method.

Since the goal of this thesis is to build memory cells using InN-NPs, we leave the details of preparation process outside the scope of this work. The details of the synthesis process can be found in [4].

We use a commercial nanosecond pulsed neodymium-doped: yttrium aluminium garnet (ND:YAG) laser (Empower Q-Switched Laser, Spectral Physics) [4]. The InN-NPs were prepared by laser ablation process using this laser. For this preparation step, the laser was operated at $527nm$ with a pulse duration of $100ns$ and a repetition rate of $1kHz$. The laser output power was chosen to be $16W$ so pulse energy was $16mJ$ for this process.

The InN-NPs preparation starts by placing the target in a glass vial filled with $20ml$ ethanol solution. Then, the laser beam was focused on the target using a plano-convex lens with a focal length of $50mm$. The height of liquid layer over InN target is $5mm$. Under this configuration, the laser ablation lasted in 5 minutes. Fig. 5.1 shows a TEM image of the $16nm$ average sized spherical InN-NPs and their size distributions.

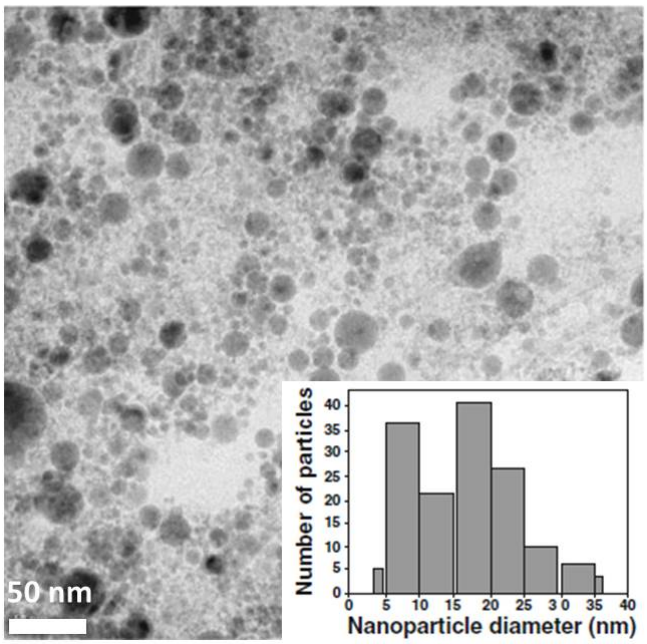

Figure 5.1: TEM image of the laser-synthesized non-agglomerate InN nanoparticles [4].

5.3 Fabrication

The MOS memory cells are fabricated on an $n^+ - type$ (111) (antimony doped, 15-20 $m\Omega - cm$) Si wafer. The step by step procedure of the fabrication process is given below:

- 3.6 -nm-thick Al_2O_3 tunnel oxide followed by 2 -nm-thick ZnO charge trapping layer are deposited at 250^oC using Cambridge Nanotech Savannah-100 ALD system.
- The InN-NPs in ethanol solution is spin casted onto the substrate with a spin speed of 700 rpm with 250 rpm/s ramp rate for 10 seconds. Then, samples were left to dry for 5 minutes on hot-plate at 110^oC.
- 2-nm-thick ZnO charge trapping layer fallowed by 15-nm-thick Al_2O_3 blocking oxide is also ALD deposited at 250^oC.
- As a final step, 400-nm-thick Al layer with a diameter of 1 mm is sputtered using a shadow mask for the gate contact.

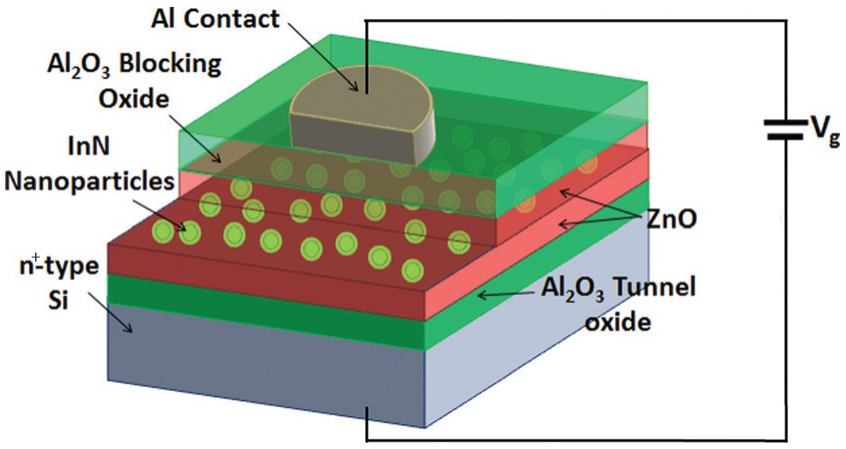

Figure 5.2: Schematic cross section of the fabricated charge trapping memory cell with embedded InN nanoparticles [5].

A cross-sectional representation of the fabricated memory device structure is depicted in Fig. 5.2.

5.4 Characterization

5.4.1 Gate Voltage Sweep Behavior

In this section, we aim to analyze the charge trapping characteristics of the InN-NPs by studying the high frequency (1 MHz) $C - V_{Gate}$ measurements of the programmed and erased states using Agilent-Signatone B1505A probe station-semiconductor parameter analyzer. First of all, we swept the gate voltage of MOS memory cell from $-2V$ to $2V$ but it was too low to achieve any noticeable charge trapping and no V_{th} shift was observed. Then, we increased the sweeping voltage range to $-10/10V$ and performed the gate voltage sweep of the memory cell forward and backward. The resulting memory hysteresis shows that programmed state is a shifted version of the erased state curve to the right, which indicates that electrons are being stored and a $5.5V$ V_{th} shift is achieved as plotted in Fig. 5.3. Our analysis of the $C - V_{Gate}$ measurements indicates that InN-NPs traps only electrons and not mixed charges unlike typical trapping materials [32, 6, 34, 4, 49].

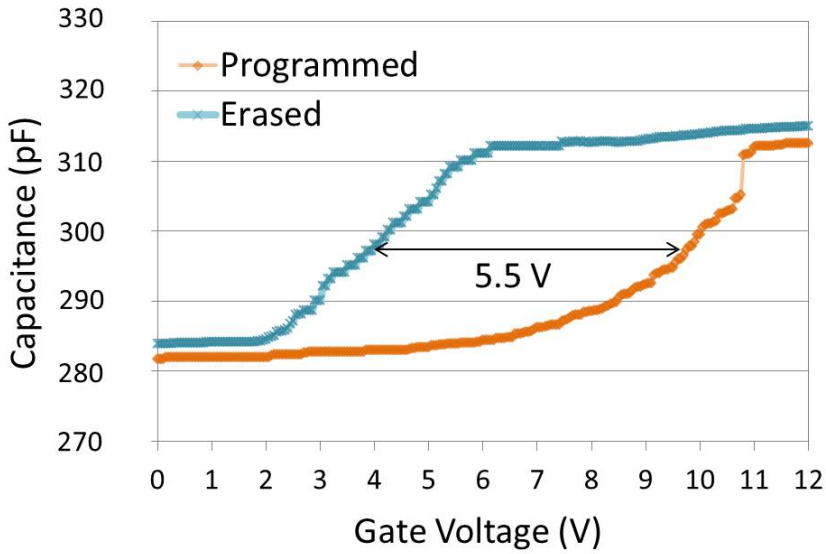

Figure 5.3: Hysteresis measurements using high frequency $C - V_G$ characteristics showing the obtained V_{th} shift with InN nanoparticles. The curves are obtained by sweeping the gate voltage from $-10V$ to $10V$ forward and backward.

Note that we use ALD-deposited ZnO, which has native crystallographic defects, such as oxygen vacancies and zinc interstitials that act as electron donors [31, 35, 50]. As a result of this, we observe that flat-band voltage is significantly shifted to the right in $C - V_{Gate}$ characteristics of the memory device. Fig. 5.4 illustrates V_{th} shifts of the memory device at different gate sweeping voltages. Our results show that the memories with embedded InN-NPs has a much larger measured memory hysteresis with respect to the control devices, which only have ZnO charge trapping layer without any nanoparticles.

The gate voltage sweep characteristics of the memory device (plotted in Fig. 5.4) shows that even in very low operating voltages such as $-4/4V$, we obtain a $2V$ V_{th} shift. This result confirms that InN-NPs act as charge trapping centers with high charge trapping density within the band-gap of ZnO.

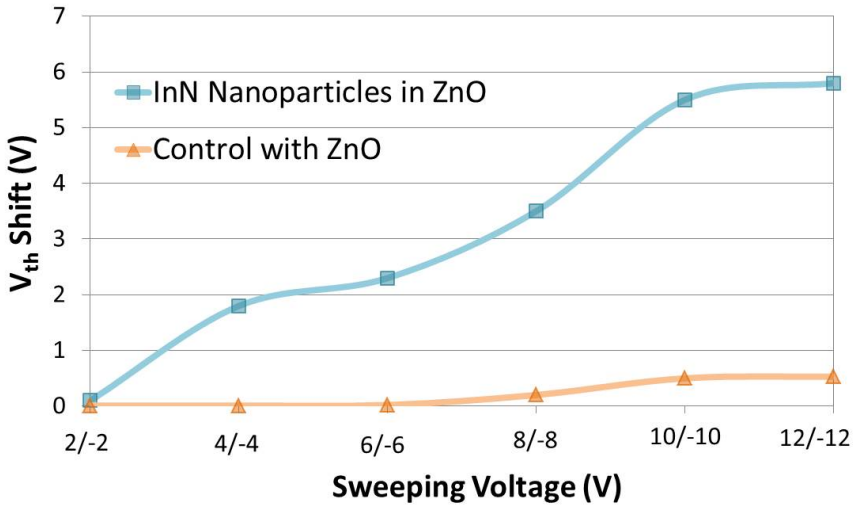

Figure 5.4: V_{th} shift vs. gate voltage sweep with InN nanoparticles.

Assuming that control device with only ZnO charge trapping layer shows a negligible memory window (based on our observations in Chapter 4 and low V_{th} shift in Fig. 5.4), the charge trap states density of the InN-NPs can be calculated using (4.1) [36]. At a gate voltage sweeping of $-10/10V$ and $C_t = 39.9nF/cm^2$, ΔV_{th} is $5.5V$ and corresponds to a filled charge trap states density of $1.37 \times 10^{12} cm^{-2}$ or equivalently $2.29 \times 10^{-7} C/cm^{-2}$. Similarly, at a gate voltage sweeping of $-4/4V$, the ΔV_{th} is $2V$, which corresponds to a filled charge trap states density of $4.78 \times 10^{11} cm^{-2}$ or $7.98 \times 10^{-8} C/cm^{-2}$.

5.4.2 Retention Characteristics

As a second step in device characterization, we aim to analyze the retention characteristics of the memory by plotting the measured V_{th} shift vs. time. Fig. 5.5 shows the retention characteristics of memory device with embedded InN nanoparticles in the charge trapping layer. The new memory device has an excellent retention characteristics, where 22% of the initial charge is lost in 10 years or a reduction of V_{th} shift from $5.5V$ to $4.4V$ in 10 years. Compared to retention characteristics of GNIZ (25% loss in 10 years) in Section 4.4.2, InN-NPs shows better results in retention characteristics of the memory cell.

Additionally, InN-NPs based memory cells exhibit better retention characteristics as compared to Si-NPs based ones. The larger electron affinity of the InN-NPs has a significant role in enhancing the retention property of the memory cells [4, 51].

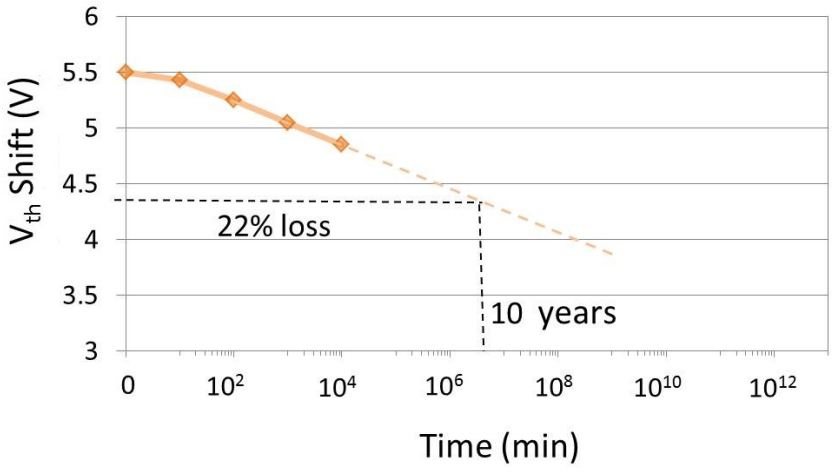

Figure 5.5: V_{th} shift vs. time measured for the memory structures with InN nanoparticles at room temperature. The plot shows a remarkable retention characteristics

5.4.3 Endurance Characteristics

In this part, we study endurance (reliability) characteristics of the memory cell with embedded InN-NPs. In order to quantify the endurance characteristics, we plot the threshold voltage shift V_{th} with respect to number of memory hysteresis. Fig. 5.6 plots the resulting V_{th} shift in the memory cell vs. 10^4 hysteresis cycles. In our experiments, the initial V_{th} shift of $5.5V$ reduced to $4.9V$, which means a loss of 11.8% of the initial charge. This little decrease in V_{th} shift represents a good reliability property of our fabricated memory devices. For example, we reported 13.3% loss of the initial charge for GNIZ memory cell in Section 4.4.3.

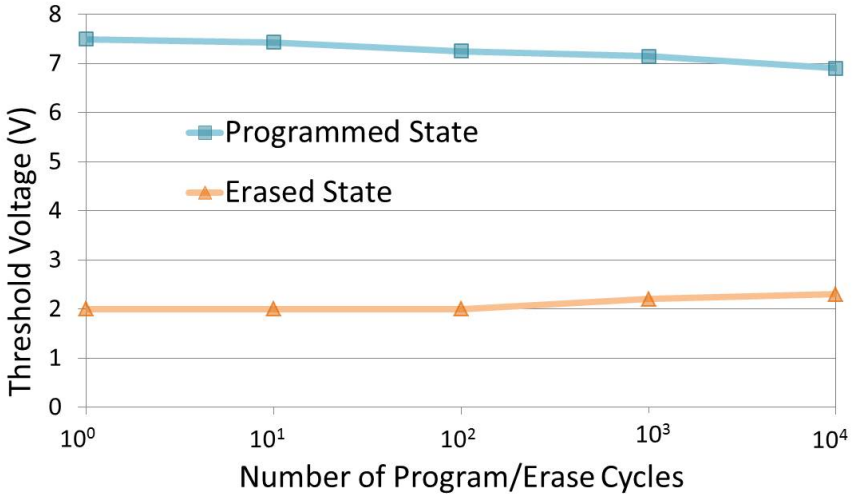

Figure 5.6: V_{th} vs. number of hysteresis measurement cycles. The plot shows excellent endurance characteristics.

5.4.4 Theoretical Analysis

Fig. 5.7 illustrates the energy band diagram of the memory structure with InN-NPs using the reported material properties for InN, ZnO, and Al_2O_3 [31, 33, 35, 47, 48] to better understand the physics behind InN-NPs based memory cells. The very first observation in the theoretical analysis of the energy band diagram shows a much smaller conduction band offset than valence band offset between Si channel and Al_2O_3 tunnel oxide ($\Delta E_c = 1.47eV \ll \Delta E_v = 4.08eV$). This is

why electron tunneling probability is higher than hole tunneling probability. This result supports the storage of electrons in the memory.

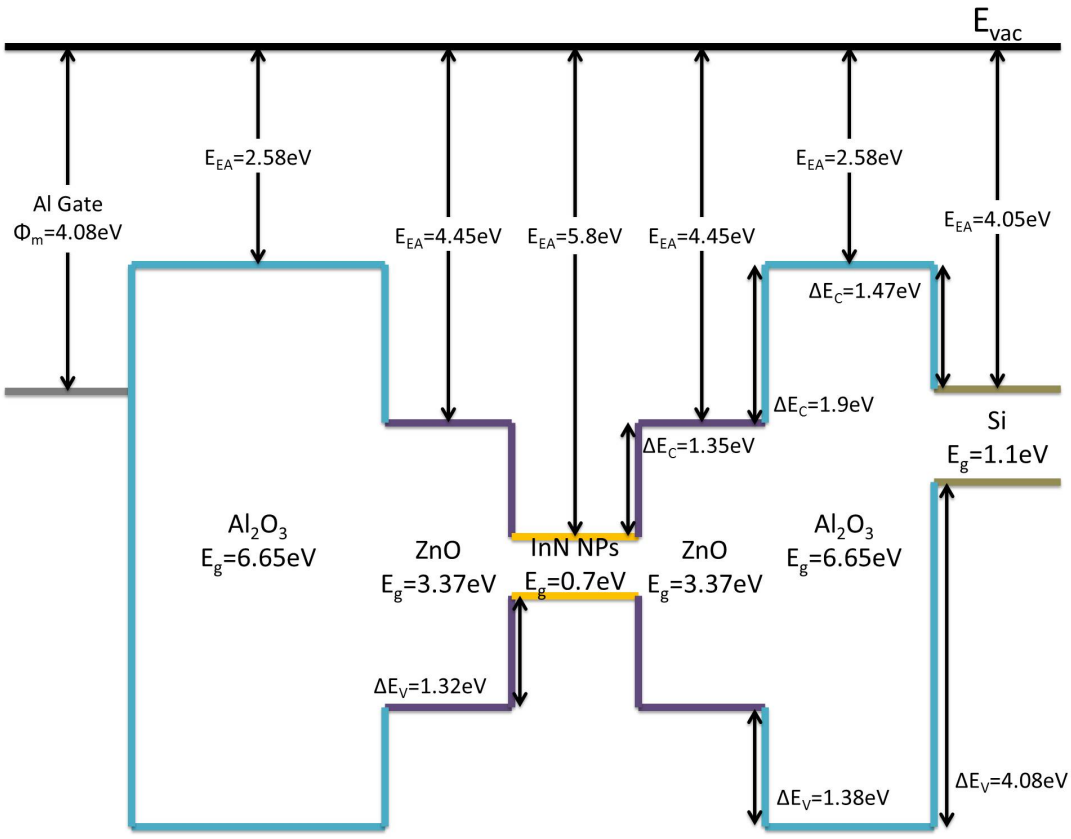

Figure 5.7: Energy band diagram of the memory structure with InN nanoparticles with zero applied bias.

Another analysis result is that addition of the InN-NPs to ZnO increases the energy barrier for electrons during discharge due to the large electron affinity of InN. Addition of InN to ZnO increases the energy barrier from $1.9eV$ to $3.25eV$, which exponentially reduces back-tunneling and enhances the retention characteristics of the memory device. This is the theoretical verification of the outstanding retention characteristics of Fig. 5.5.

In addition to the large electron affinity of InN, ZnO layer acts as an extra physical thickness (spacer) for electrons to overcome for discharge. This additional layer also increases the retention performance of the memory device. On the other hand, creating these extra barriers to increase retention performance might

also increase the required voltage to be applied for erase operations.However, thanks to n-type nature of the ZnO, it enhances the electric field across the tunnel oxide when a negative gate voltage is applied (during the erase operation); therefore required gate voltage for the erase operation can be reduced further.

Moreover, we calculated the trap lifetime of the electrons confined in the InN-NPs between the barriers formed by Al_2O_3 tunnel and blocking oxide. We first calculated the ground state energy of the electrons confined in $16nm$ InN-NPs by using the following equation [52]

$$E_0 = \frac{\hbar^2 \pi^2}{2m_0 L^2}, \tag{5.1}$$

where $\hbar$ is the reduced Plank's constant, m_0 is the electron effective mass in InN [53], and L is the thickness of the InN-NPs. By using (5.1), the ground state energy (E_0) for InN-NPs is calculated as $E_0 = 13.4meV$. Now, the tunneling probability can be approximated as [51]

$$T = 16 \times (\frac{E_0}{V_0}) \times (1 - \frac{E_0}{V_0}) \times e^{-2d\frac{\sqrt{2m_0(V_0 - E_0)}}{\hbar}}, \tag{5.2}$$

where V_0 is the potential energy of the barrier ($3.25eV$) and d is the thickness of the barrier. The transmission probability is calculated to be $T = 5.837 \times 10^{-22}$. In order to estimate the trap lifetime of the electrons, we calculate the attempt frequency v as

$$v = \frac{E_0}{2\pi\hbar} = 3.24 \times 10^{12} s^{-1}. \tag{5.3}$$

Now, trap lifetime of an electron confined in InN-NPs between barriers can be calculated using (5.2) and (5.3) as

$$\tau = (vT)^{-1} = 5.287 \times 10^8 s = 16.754 \quad years. \tag{5.4}$$

This theoretical estimation is in good agreement with the experimental long retention characteristics obtained in Section 5.4.2 of the memory structure with InN-NPs.

5.5 Summary

In this chapter, the use of InN-NPs in a memory cell is demonstrated. In the $C - V_{Gate}$ hysteresis measurements, the memory showed a large V_{th} shift at reduced operating voltages. The charge trapping characteristics of the InN-NPs is experimentally measured and a V_{th} shift towards right is observed; also the analysis of the energy band diagram supported the observed electron storage in the InN-NPs. The theoretical analysis confirmed the long retention time owing to the good confinement of charges in InN-NPs. The resulting advantages of InN-NPs embedded memory cells highlight their potential use for building low-cost and low operating voltage of charge trapping memory devices.

Chapter 6

All-ALD Thin Film Transistor Based Memory

This chapter presents thin-film ZnO charge trapping memory cell grown in a single ALD step. The following sections detail the motivation, fabrication process and experimental results, which are further verified by TCAD simulations.

6.1 Introduction

There has been an increasing interest in using metal-oxide semiconductors (ZnO and IGZO) as channel materials for thin-film transistors (TFTs). To produce low-cost flexible electronics, low-temperature process techniques have critical importance. Actually, there are various techniques in literature to deposit TFTs with ZnO channels such as sputtering [54, 55, 56, 57, 58], atomic layer deposition [59, 60, 61, 62], and pulsed laser deposition [63, 64]. The same low-cost, low-temperature process requirements also apply for functional electronics, such as integrated sensors and data storage devices. Actually, there are some examples flash memory devices with low-cost ZnO channel materials in literature [65, 66, 67, 68].

The aforementioned requirements for low-cost memory devices motivate the researches to concentrate on ALD technique, which is promising due to its exceptional features such as low-temperature growth, large-area uniformity, precise thickness control, highly conformal deposition, and scalability to roll-to-roll processes. In fact, memory devices using ALD deposited ZnO as channel are recently demonstrated [68]; however, the gate stack and the trapping layer are grown by the plasma-enhanced CVD technique in this study. Additionally, there are earlier examples on the use of wide band-gap amorphous semiconductors [66] and semiconductor nanoparticles [69] as both channel and trapping layers in memory devices. However, in these studies amorphous layers are deposited by RF sputtering [66], and ZnO nanoparticles are coated by solution processing [69].

Considering the previously used techniques in literature, ALD approach offers a simplified high-throughput single-step approach to obtain very high quality complete gate stacks. The single-step approach avoids risk of contamination or incorporation of impurities in gate stack. The ALD approach also increase the throughput significantly by eliminating multiple equipment utilization for the gate stack, and therefore offer a novel path for ultra-low-cost integrated devices.

In this study, we introduce a memory device with a gate stack fabricated in a single ALD step. We use wide band-gap ZnO as charge trapping and channel layer for concept demonstration. Fig. 6.1 illustrates the structure of an all-ALD memory cell with the ALD-deposited gate stack, the transistor channel (ZnO), tunnel oxide (Al_2O_3), charge trapping layer (ZnO), and charge blocking layer (Al_2O_3). We also compare the experimental results with physics-based TCAD simulations to provide further insight into the charge trapping mechanism.

6.2 Fabrication

Channel-last all-ALD memory devices are fabricated on a highly doped (10-18 $m\Omega - cm$) Si wafer. The following items explain the step by step procedures of the fabrication process. Note that all the layers in the active region of the device

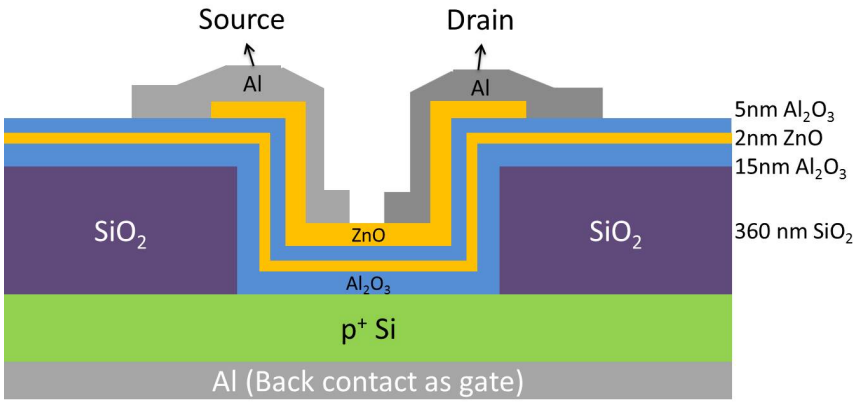

Figure 6.1: Schematic representation of the thin-film all-ALD memory cell.

is grown in a single continuous ALD step at 250^oC.

- 15-nm-thick Al_2O_3 blocking oxide layer is first deposited.
- Then, 2-nm-thick ZnO charge trapping layer is deposited.
- After that, 5-nm-thick Al_2O_3 tunneling oxide layer and 11-nm-thick ZnO channel are deposited.
- The top ZnO layer (channel) is patterned and etched for $2sec$ using a 5 : 95 $H_2SO_4 : H_2O$ solution.
- 100-nm-thick Al layer is thermally evaporated and patterned by a liftoff technique to form source and drain contacts.
- 360-nm-thick electron-beam evaporated SiO_2 layer is used for device isolation.
- Finally, the samples are annealed in forming gas ($H_2 : N_2$ 5 : 95) for 10 min at 400^oC.

We fabricated devices with different channel length, L, (2-150 μm) and width, W, (10-100 μm). Fig. 6.2 and Fig. 6.3 show the TEM image of the active channel area of the fabricated device and the layers of the active area of the thin-film all-ALD memory cell at atomic scale, respectively.

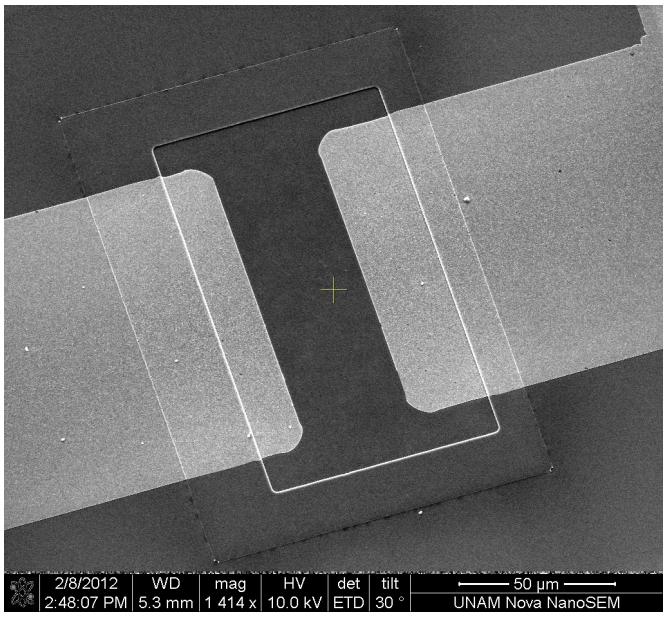

Figure 6.2: TEM image of the active channel area of the fabricated device.

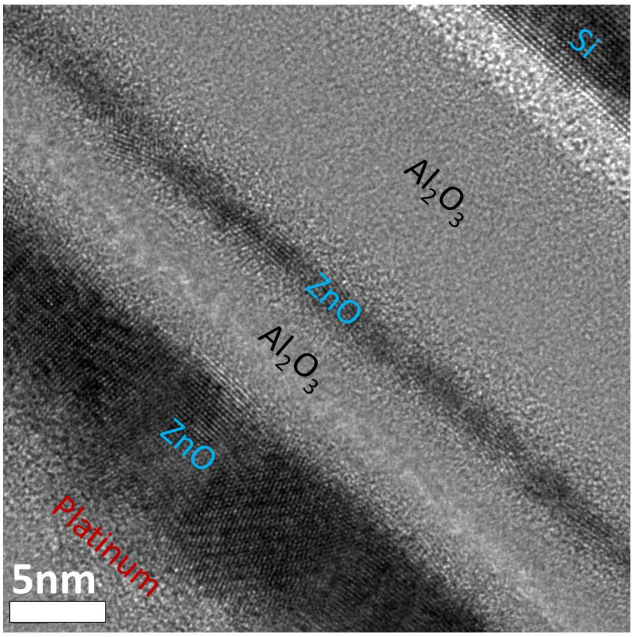

Figure 6.3: Cross-sectional TEM image of the active area of the thin-film all-ALD memory cell.

6.3 Characterization

In order to characterize the memory behavior of the fabricated devices, we measure the current voltage (I-V) characteristics of the devices using a Keithley 200 semiconductor parameter analyzer at room temperature. Fig. 6.4 shows the transfer characteristics $I_{Drain} - V_{Drain}$ of the fabricated memory cells for different gate biases.

The fabricated memory devices act as n-channel MOSFETs, since the ALD-deposited ZnO is n-type. This is mainly due to the native crystallographic defects such as interstitial zinc and oxygen vacancy that behave as electron donors [70, 71]. For a sample device with a gate length and a width of 50 μm, the maximum on-to-off ratio of 10^2 (limited by high effective doping concentration of the ZnO channel due to 250^oC deposition) is obtained with a sub-threshold slope of $720mV/dec$. The electron mobility μ_e in the ZnO channel is found to be $23cm^2/Vs$ using

$$I_{Drain} = (\frac{\mu_e \epsilon_0 \epsilon_r W}{2t_{ox}L})(V_{gate} - V_{th})^2 \tag{6.1}$$

in the saturation region ($V_{Drain} > V_{Gate} - V_{th}$), where ϵ_0 and ϵ_r are the dielectric constants of the vacuum and the Al_2O_3 ($\epsilon_r = 9.5$) layer, respectively. V_{th} is the threshold voltage and t_{ox} is the thickness of the gate insulator in this notation.

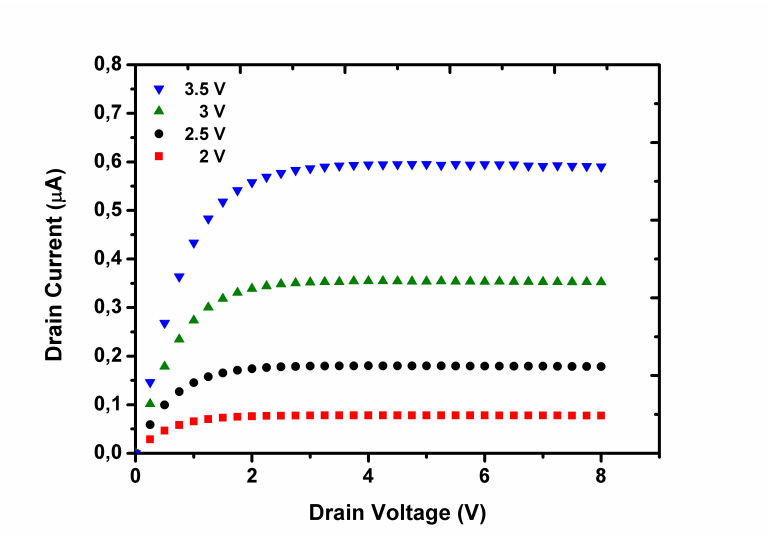

Figure 6.4: Measured $I_{Drain} - V_{Drain}$ of the thin-film all-ALD memory cell.

In order to show that the device has memory characteristics, $I_{Drain} - V_{Gate}$ hysteresis is measured. Fig. 6.5 shows a typical hysteresis behavior for $\pm 6V$ and $\pm 10V$ gate voltage sweeps, which verify the memory effect in the fabricated devices. According to our results (depicted in Fig. 6.5), there is a $2.35V$ hysteresis in the $\pm 10V$ gate voltage sweep. Control samples, with no ZnO trapping layer, show a $< 0.6V$ hysteresis, which is attributed to unintentional charge trapping in the gate oxide and the oxide-channel interface [72]. The fabricated devices exhibit poor retention characteristics potentially due to a continuous ZnO trapping layer.

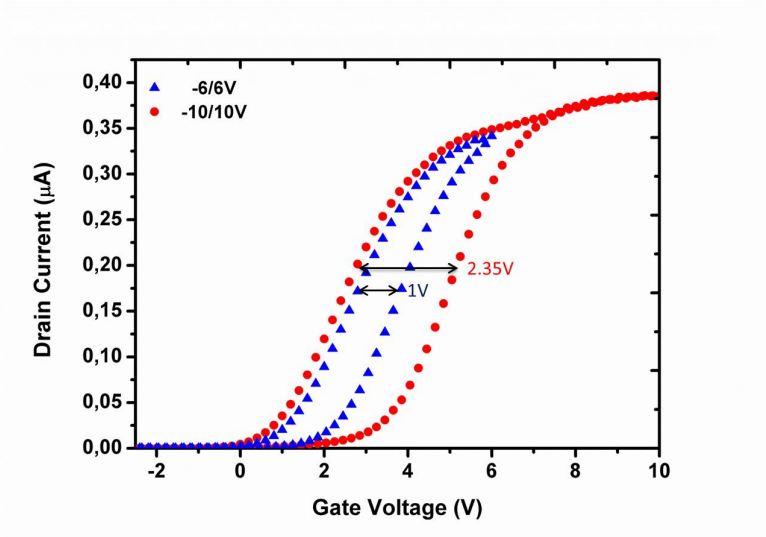

Figure 6.5: Measured hysteresis behavior of the $I_{Drain} - V_{Gate}$ characteristics with the gate voltage sweep.

6.4 TCAD Simulations

In addition to the experimental results, physics-based TCAD simulations are also performed in order to verify the memory characteristics of the device using Synopsys TCAD tools. Table 6.1 lists the material property data used for ZnO [73] and Al_2O_3 [74].

Fig. 6.6 illustrates the energy band diagram of the memory structure at zero applied voltage. Both Fowler-Nordheim and direct tunneling models were used throughout the *program* and *erase* cycles, allowing electrons to tunnel from the

Table 6.1: Material properties for ZnO and dielectric layers

	Al_2O_3	SiO_2	ZnO
Relative permittivity	9.5 (6 to 9)	3.9	8.75
Energy bandgap	6.65 eV	9 eV	3.37 eV
Electron affinity	2.58 eV	0.9 eV	4.45 eV
Electron tunnel mass	0.43 m_0	0.44 m_0	0.24 m_0
Hole tunnel mass	0.5 m_0	1 m_0	0.59 m_0

ZnO channel layer to the trapping layer, and vice versa. The simulation model includes energy states in the ZnO layer due to crystallographic defects such as interstitial zinc and oxygen vacancy.

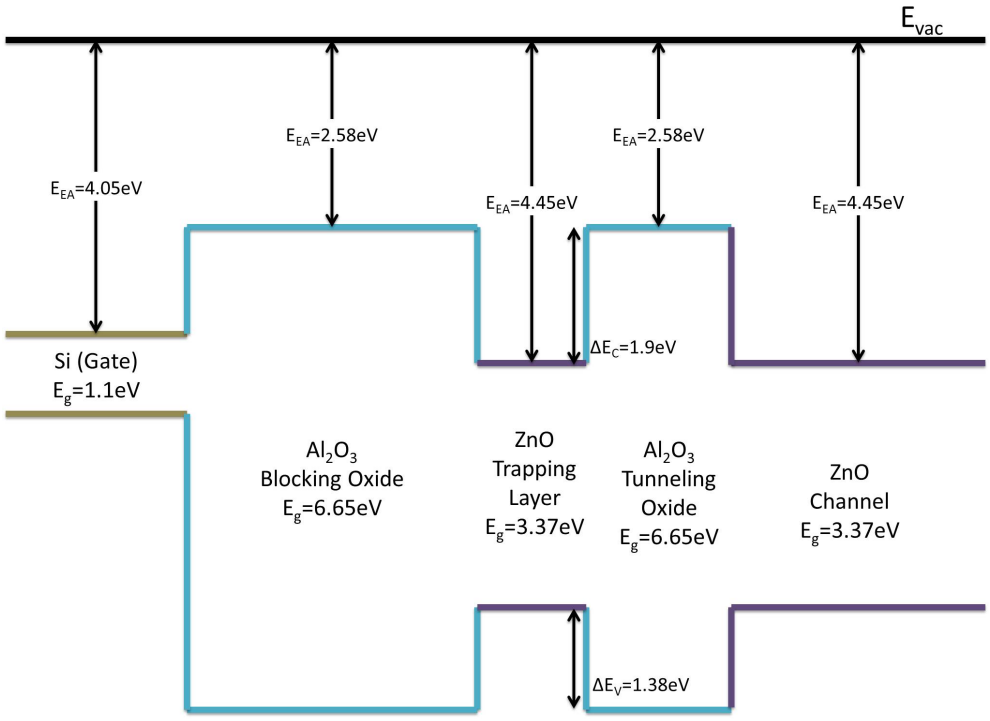

Figure 6.6: Energy band diagram of the memory cell.

Fig. 6.7 shows the $I_{Drain} - V_{Gate}$ characteristics for *program* and *erase* states, where we can observe $2.12V$ hysteresis. The V_{th} shift we obtain in TCAD simulations agrees well with the experimentally obtained V_{th} shift results. According to these results there are two possible trap states for the electrons that tunnel

through Al_2O_3 tunnel oxide; the electrons are either trapped due to confinement in a quantum well of $1.9eV$ formed by the conduction band offsets between ZnO and Al_2O_3 or they are trapped in the available energy states within the ZnO trapping layer.

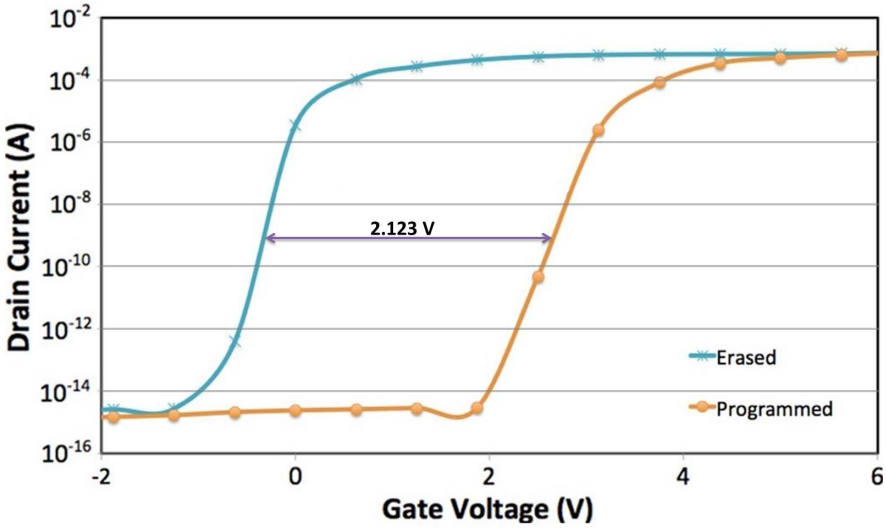

Figure 6.7: Computed $I_{Drain} - V_{Gate}$ for program and erase states [6].

6.5 Summary

In this chapter, we explain the fabrication procedures and performed memory analysis (both experimentally and theoretically with TCAD simulations) for a thin-film charge-trapping ZnO memory cell using a single ALD step. Note that the fabrication of this type memory cell with the single ALD step is shown for the first time, in this study. In our experimental analysis, we showed $2.35V$ V_{th} shift in hysteresis between write and erase cycles. We then supported our results with TCAD simulations. Additionally, the ZnO transistor characteristics obtained a rank among the best reported in literature. Our results are promising for future low-cost, flexible, and transparent electronic applications.

Chapter 7

Conclusion and Future Directions

In this thesis, we focused on proof-of-concept low-cost and high quality memory cells by investigating different materials and production techniques for charge trapping layers in memory devices.

In the first part of this thesis, we presented a charge trapping memory cell with embedded graphene nanoplatelets. We explained the fabrication procedures for this memory cell and performed necessary memory characterization analysis both experimentally and theoretically. The memory cell shows a large threshold voltage shift ($4V$) at low operating voltages ($6/-6V$), good retention ($>$ 10 years), and good endurance characteristics ($> 10^4$ cycles). Comparison with control devices, embedding graphene nanoplatelets shows better V_t shift and retention characteristics. Additionally, the fabrication of this memory device is compatible with current semiconductor processing. Therefore, we believe that the proposed memory cell structure has a great potential in low-cost memory applications.

For the second part, we proposed the use of laser-synthesized indium-nitride nanoparticles as the charge trapping agents in the memory cell. We detailed the fabrication process for the InN-NPs based memory cell and performed memory characterization. The produced memory cell shows a noticeable threshold voltage shift of $2V$ even at low operating voltage of $4V$. The experimental and theoretical memory analysis shows that InN-NPs act as charge trapping centers and the

device shows memory behavior.

Finally, we demonstrated a memory device with a gate stack fabricated in a single ALD step. Note that production of memory devices in a single ALD step reduces the risk of contamination and incorporation of impurities in the gate stack. Therefore, the proposed fabrication process of this memory device is the fundamental contribution of this study. Thin-film ZnO is used as a channel material and charge trapping layer in the production of this memory device. The memory effect is verified by a $2.35V$ hysteresis in *drain current-gate voltage* curve. We also performed physics-based TCAD simulations to show that theoretical analysis are in very good agreement with the experimental results.

One of the main innovations needed for further increasing the performance of memory devices is to find novel high-κ dielectric insulators. Using these novel insulators for tunnel oxide increases the retention time by reducing back tunneling of stored charges and enables using thinner tunnel oxide layers to decrease applied program-erase voltage to the gate which leads low-power consuming memory devices. Also investigating new high-κ dielectrics provide an opportunity to better tunnel band engineering for further scaled charge trapping nonvolatile memory devices.Furthermore, developing exotic materials with high trapping density to be used as charge trapping layers are needed to achieve large threshold voltage shift even at low applied voltages. Finally investigating novel memory structures such as FinFET, Tri-gate transistor and finding new fabrication processes to embed novel charge trapping materials is crucial for scaling down and achieving low-cost, low-power-consuming memory devices.

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Appendix A

Publications

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