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# INVESTIGATION OF ELECTRICAL PROPERTIES OF METAL-POLYMER-SEMICONDUCTOR (MPS) STRUCTURES DEPENDING ON FREQUENCY AND VOLTAGE

**IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF SCIENCE IN PHYSICS**

**BY**

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July 2023

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## ABSTRACT

# INVESTIGATION OF ELECTRICAL PROPERTIES OF METAL-POLYMER-SEMICONDUCTOR (MPS) STRUCTURES DEPENDING ON FREQUENCY AND VOLTAGE

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This comprehensive study presents an in-depth exploration of modified gold (Au) on silicon (n-Si) diodes. The modification was performed by applying a Polyvinyl Alcohol (PVA) interfacial layer onto the n-Si wafer using the spin coating method, thereby creating an Au/PVA/n-Si diode with a Metal-Polymer-Semiconductor (MPS) structure. The properties and characteristics of these diodes were investigated and evaluated under room temperature conditions at two frequencies, 5kHz and 5MHz. The study systematically addressed the analysis of the direct and reverse bias current-voltage (I-V), capacitance-voltage (C-V), and conductance-voltage (G/ω-V) characteristics of the modified diodes. Key electrical parameters such as the ideality factor (n), series resistance (Rs), shunt resistance (Rsh), and barrier height ($\Phi_B$) were obtained from these bias voltage I-V characteristics, providing critical insight into the functioning and performance of the modified diodes. A variety of methods were employed for the computation of these parameters, including Cheung functions, Ohm's law, and Norde's method. The calculated series resistance (Rs) values were obtained from these methods and their implications were duly examined. Further examination was conducted on the admittance, C-V and G/ω-V characteristics of the modified Au/PVA/n-Si diode. This was did under two sets of conditions - dark and illuminated. The primary electrical parameters including the thickness of the depletion layer width ($W_D$) and the barrier height ($\Phi_B$(C-V)) were determined from the reverse bias $C^{-2}$-V curves for both sets of conditions. In an enlightening revelation, the study found a strong correlation between the illumination conditions and the voltage-dependent Rs values. These were obtained

using C-V and G/ω-V data under both dark and 100 mW/cm$^2$ illumination conditions. This study firmly establishes that the I-V, C-V, and G/ω-V characteristics of the Au/PVA/n-Si diode are heavily influenced by illumination. The evidence from this research provides a substantial understanding of the behavior of MPS structures. This is not only significant from an academic perspective but is also set to influence real-world applications. It unlocks new possibilities for the wider application of these structures in the fields of electronics and optics, giving researchers, engineers, and technologists an enriched perspective and a practical edge.

**2023, 48 pages**

**Keywords:** MPS structures, Electrical properties, Frequency and voltage dependence

# ÖZET

## METAL-POLİMER-YARI İLETKEN (MPS) YAPILARIN ELEKTRİKSEL ÖZELLİKLERİNİN FREKANS VE GERİLİME BAĞLI OLARAK İNCELENMESİ

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Bu kapsamlı çalışma, modifiye edilmiş altın (Au) üzerinde silikon (n-Si) diyotların detaylı bir incelenmesini sunar. Modifikasyon, n-Si wafere dönme kaplama yöntemi kullanılarak bir Polivinil Alkol (PVA) ara yüzey tabakası uygulanarak gerçekleştirilmiştir. Bu şekilde, bir Metal-Polimer-Yarı iletken (MPS) yapısına sahip bir Au/PVA/n-Si diyot oluşturulmuştur. Bu diyotların özellikleri ve karakteristikleri, oda sıcaklığında iki frekansta, 5kHz ve 5MHz'de araştırıldı ve değerlendirildi. Çalışma, modifiye edilmiş diyotların doğrudan ve ters polarizasyonlu akım-voltaj (I-V), kapasitans-voltaj (C-V) ve iletkenlik-voltaj (G/ω-V) özelliklerinin analizini sistematik bir şekilde ele aldı. İdealite faktörü (n), seri direnç (Rs), shunt direnç (Rsh) ve bariyer yüksekliği ($\Phi_B$) gibi anahtar elektriksel parametreler, bu polarizasyonlu voltaj I-V karakteristiklerinden elde edildi, bu da modifiye edilmiş diyotların işleyişi ve performansı hakkında kritik bir içgörü sağladı. Bu parametrelerin hesaplanması için Cheung fonksiyonları, Ohm kanunu ve Norde'nin metodu gibi çeşitli yöntemler kullanıldı. Hesaplanan seri direnç (Rs) değerleri, bu yöntemlerden elde edildi ve etkileri gerektiği gibi incelendi. Daha ileri inceleme, modifiye edilmiş Au/PVA/n-Si diyotun alınabilirlik, C-V ve G/ω-V karakteristikleri üzerinde gerçekleştirildi. Bu, iki farklı durumda - karanlık ve aydınlatılmış - yapıldı. Tüketim tabakasının genişliği ($W_D$) ve bariyer yüksekliği ($\Phi_B$(C-V)) dahil olmak üzere birincil elektriksel parametreler, her iki durum için de ters polarizasyonlu $C^{-2}$-V eğrilerinden belirlendi. Çalışma, aydınlatma koşulları ile voltaja bağlı Rs değerleri arasında güçlü bir korelasyon buldu. Bunlar, hem karanlık hem de 100 mW/cm$^2$ aydınlatma koşulları altında C-V ve G/ω-V verileri kullanılarak elde edildi. Bu çalışma, Au/PVA/n-Si diyotunun I-V, C-V ve G/ω-V karakteristiklerinin aydınlatma tarafından ağır bir şekilde etkilendiğini kesin bir şekilde

belirler. Bu araştırmadan elde edilen kanıtlar, MPS yapılarının davranışına yönelik önemli bir anlayış sağlar. Bu, sadece akademik bir bakış açısından değil, aynı zamanda gerçek dünya uygulamalarını da etkileyecek önemdedir. Elektronik ve optik alanlarda bu yapıların daha geniş bir uygulama olasılığını açığa çıkarır, araştırmacılara, mühendislere ve teknolojilere zenginleştirilmiş bir bakış açısı ve pratik bir avantaj sağlar.

**2023, 48 sayfa**

**Anahtar Kelimeler:** MPS yapılar, Elektriksel özellikler, Frekans ve voltaja bağlılık

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**Tahseen Jawad Kadhim ALGABRI**

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**CONTENTS**

## LIST OF SYMBOLS

| | |
|---|---|
| $\Phi_B$ | Barrier height |
| *C-V* | Capacitance-voltage |
| $E_C$ | Conductiance band |
| $G/\omega$-*V* | Conductiance-voltage |
| *I-V* | Current voltage |
| $E_F$ | Fermi energy level |
| *Eg* | Forbiden bandgap |
| *qVi* | Potential |
| $I_o$ | Saturation current |
| *Vi* | Voltage |
| $\Phi_m$ | Work function of the metal |
| $\Phi_s$ | Work function of the semiconductor |

## LIST OF ABBREVIATIONS

| | |
|---|---|
| $W_D$ | Depletion layer |
| Au | Gold |
| Nss | Interface states |
| MIS | Metal insulator semiconductor |
| MOS | Metal oxide semiconductor |
| MOSFET | Metal oxide semiconductor field effect transistors |
| MPS | Metal polymer semiconductor |
| MS | Metal-semiconductor |
| PPy | Polypyrrole |
| PS | Polystyrene |
| PVA | Polyvinyl Alcohol |
| PVP | Polyvinyl pyrrolidone |
| SD | Schottky diode |
| Ri | Structure resisitance |
| Rs | Series resistance |
| TE | Thermionic emission |

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# 1. INTRODUCTION

The growing recognition of metal-semiconductor (MS) structures' pivotal role in the production of technological devices has been observed over time (Reddy *et al.* 2011, Alptekin *et al.* 2019a). The evolving comprehension of the electrical and dielectric characteristics of MS structures has resulted in significant progress thus far, as evidenced by various studies (Alptekin *et al.* 2019b, Matsuura 1981, Sahay 1990, Kako 1996).

The identification of a potential barrier at the interface of MS structures, which are crucial components in semiconductor circuits, was first reported by Schottky in 1938. Consequently, the nomenclature used to denote these structures is schottky diodes (SDs), as a tribute to the significant contributions made by W. Schottky in this domain (Sharma 1984). The initial model proposed by Schottky and Mott for barrier heights ($\Phi_B$) in MS contacts (Mott 1938, Schottky 1938) acknowledged the presence of a substantial resistance exhibited by a thin interface layer, as observed in both theoretical and experimental investigations. It has been hypothesized that achieving vacuum level alignment between the metal and semiconductor requires their contact.

In 1947, a significant observation was made indicating that the metal work function experienced a reduction in correlation with the $\Phi_B$ owing to the interfacial states present in the semiconductor's band gap. This observation was reported by (Mönch,1990, Li 1960. Planar structures known as Schottky contacts have been utilized in the semiconductor industry to achieve uniform current distribution and contact potential across the junction area. These structures are formed by evaporating metal on specific regions of the semiconductor surface. (Sze *et al.* 2010). These structures are preferred due to their reduced series resistance, elevated power handling capability, and diminished signal interference.

Furthermore, the exceptional efficacy of MS architectures, attributed to the lack of recombination and production, has augmented their allure. Notwithstanding, these structures exhibit certain limitations such as susceptibility to surface contamination and inadequate endurance towards high-temperature processing. The impact of high temperatures on the electrical characteristics of the diode has been documented in various studies, including those conducted by (Demirezen *et al.* 2010, Tunç 2010, Tecimer *et al.* 2013). The process of annealing within the temperature range of 300-600C has been observed to decrease the resistance of the ohmic contact. However, this process has a negative impact on the rectifying properties of MS structures. Hence, various methodologies have been implemented to enhance the robustness, electrical conductivity, and overall functionality of MS architectures against extrinsic influences. The utilization of diverse interfaces has been explored for the development of structures such as metal oxide semiconductor (MOS), Metal insulator semiconductor (MIS), metal polymer semiconductor (MPS), or metal-ferroelectric-semiconductor (Sze *et al.* 2010, Card 1971, Gökçen *et al.* 2013).

In contemporary times, conventional interfacial insulation layers comprising $SiO_2$, $Si_3N_4$, $SnO_2$, and $TiO_2$ that are conventionally employed between metal and semiconductor have been progressively substituted by doped or non-doped polymers. This change can be attributed to the exceptional ductility of the latter material and its cost-effective and uncomplicated manufacturing procedure. The inherent low conductivity of polymers can be improved by incorporating appropriate amounts of metal or other materials, as reported by (Baraz 2017, Sharma *et al.* 2016, Ersöz *et al.* 2016).

The electrical conductivity properties of polymer materials have attracted significant attention in academic and industrial research domains, owing to their ability to enhance with the incorporation of fillers. Organic conductive polymer materials exhibit remarkable versatility in their potential applications for the fabrication of electronic and opto-electronic devices. These materials are highly appreciated for their numerous advantages such as their flexibility, ability to customize material properties, cost-

effective technology, low production costs, ease of manufacturing processes, and eco-friendly production methods (Baraz 2018, Ukah 2011).

The utilization of polymer materials has been extensively employed in the fabrication of diverse electronic devices such as light emitting diodes, organic light emitting diodes, Schottky barrier diodes (SBD), solar cells, and transistors, owing to their distinctive capacitance and conductivity properties (Baraz 2017, Gunaydin *et al.* 2018, Gümüş *et al.* 2015)

The utilization of various polymer materials such as polystyrene (PS), polyvinyl-alcohol (PVA), polypyrrole (PPy), Polyvinyl pyrrolidone (PVP), polyvinyl chloride, and polythiophene is feasible in the manufacturing process of MPS structures (Demir *et al.* 2018, Gümüş *et al.* 2015). From a materials engineering standpoint, the PVP polymer exhibits numerous favorable characteristics for device manufacturing technology. The cost-effectiveness of PVP production, minimal energy consumption, uncomplicated manufacturing methods, and favorable chemical characteristics for device utilization are the driving factors behind its widespread adoption in the industry (Crowell *et al.* 1966).

In the realm of structural fabrication, materials such as MS, MIS, or MPS often rely on silicon (Si) as the preferred semiconductor due to its stability and cost-efficiency. In the field of materials engineering, it is common to utilize gold (Au) as the primary material for rectifying contact in n-type semiconductors. On the other hand, aluminum (Al) and silver (Ag) are the preferred materials for p-type semiconductors, as long as they exhibit high purity levels of at least 0.99. The determination of work function for both the metal and semiconductor is a crucial aspect in the fabrication of these materials. The selection of a suitable metal with the appropriate work function is crucial and should be based on the type of semiconductor being utilized, whether it is n-type or p-type.

The incorporation of an insulate or polymeric layer at the metal-semiconductor interface results in enhanced structural performance and controlled modulation of interface charge transitions. In the process of interface layer selection, materials with high dielectric constants are favored for their ability to passivate the surface, reduce leakage

current, enable controlled current transmission, and offer rectifying properties. This is in line with the principles of materials engineering.

In this study, we evaluated the C-V and G/ ωV characteristics of an Au/PVA/n-Si (MPS) structure across a specified frequency spectrum. The evaluation of electrical characteristics of MPS structures and the investigation of current conduction mechanisms exhibit resemblances to those observed in MIS structures. The relevant equations that govern metal-insulator-semiconductor (MIS) structures in our empirical measurements and analyses has been employed. The observed high values of C and G/ω-V at low frequencies suggest the presence of a PVA interfacial layer. Additionally, the generation of interface states (Nss) at the PVA/n-Si junction and their durability may have an effect on this phenomenon. A PVA film was synthesized via spin-coating technique to coat the interface of Au/n-Si in this investigation. Electrical characterization of the Au/PVA/n-Si MPS structure was performed using C-V and G/ω-V measurements. Measurements were conducted at standard temperature and pressure and across a frequency spectrum spanning from 5kHz to 5MHz, while subjecting the sample to a voltage range of -4V to +4V. The obtained data enabled the determination of the essential electrical properties of the material's composition. Through examination of the I-V characteristics of the Au/PVA/n-Si structure at a temperature of 300 K, the diode parameters have been effectively identified. These parameters consist of the ideality factor (n), reverse saturation current ($I_0$), zero-bias $\Phi_{B0}$, structure resistance (Rs), and short-circuit resistance (Rsh). The voltage and frequency-dependent properties of the interface state density (Nss) were investigated using low-high frequency capacitance and Hill-Coleman techniques. The evaluation of the electrical characteristics of Rs was conducted by utilizing Ohm's law and Nicollian and Brews methodologies. Upon completion of an analysis of the Rs effect, we have acquired the altered C-V and G/ω-V characteristics.

The basic electrical as well as dielectric properties of MPS structures in the electronics sector are not yet fully understood despite their increasing usage. Comprehensive analysis of critical properties such as I-V, C-V, and G/ω-V is still required across a broad spectrum of frequencies, temperatures, and voltages. Additionally, the

comprehension and enhancement of conduction and polarization mechanisms in MPS structures are crucial for their operation and improvement and require further investigation. Furthermore, the comparative analysis between MPS structures and conventional MIS/MOS structures is inadequate, despite the potential of MPS structures as substitutes. The objective of this investigation is to tackle these concerns and add to the reservoir of expertise essential for the effective development and utilization of MPS configurations in the field of electronics.

The fundamental aim of this investigation is to acquire precise and comprehensive data regarding the fundamental electrical and dielectric characteristics of MPS architectures. The investigation of the I-V, C-V, and G/ω-V properties of these structures across a broad spectrum of frequencies, temperatures, and voltages will facilitate the attainment of this objective. The study aims to clarify the mechanisms of conduction and polarization in MPS structures, which have not yet been fully elucidated. The study further aims to identify how MPS structures can effectively replace traditional metal MIS/MOS structures in various electronic applications due to their advantageous properties. Additionally, this study's scope encompasses several key areas, beginning with the fabrication of interfacial layered MPS structures. Following the preparation phase, we will conduct a comprehensive analysis of the I-V characteristics of these structures to understand parameters like $\Phi_B$, ideality factor, series and short circuit resistances, and interface states. Alongside, we will examine C-V and G/ω-V characteristics in detail to investigate series resistance and the concentration of doping atoms. The experimental procedures will span a wide range of frequencies, temperatures, and voltages to ensure the comprehensiveness and applicability of our findings. Impedance spectroscopy will be employed as a strategic tool to scrutinize the intricate electrical behavior of MPS structures. One of the core components of the study is to elucidate the conduction and polarization mechanisms within MPS structures, which have not been thoroughly understood yet. Lastly, the study will draw comparisons between the results obtained from MPS structures and those from traditional metal MIS/MOS structures, underscoring the potential advantages and applications of MPS structures in the electronics industry.

## 2. LITERATURE REVIEW

The MPS structure comprising Al/P3HT/p-Si displays notable frequency-dependent sensitivity of capacitance and conductance, particularly at lower frequencies.The C-V plots exhibit a shift towards lower voltages in peak positions with increasing frequency, accompanied by a decrease in intensity as frequency rises. The insulator layer and interface states exert significant influence on the non-ideal behavior observed in both C-V and G-V characteristics of MIS Schottky diodes. The low cost and ease of fabrication make these structures more advantageous than traditional organic semiconductor-based devices (Yükseltük *et al.* 2019).

HgS-PVA nanoparticles were produced utilizing ultrasound-assisted methods and characterized through X-ray diffraction, SEM, and FTIR, as per the findings of (Ömer *et al.* 2019). The obtained optical band gap measurement was 2.4 eV, and it was observed to have a shift in the blue spectrum of 0.3 eV. SEM and FTIR analysis revealed the presence of nano-sized particles on the surface of the samples. Energy measurements were obtained between functional groups. Dielectric behavior was analyzed in a frequency range of 1 kHz-5 MHz. Division processes and states of the surface dominated the lower frequencies. The observed trend indicates a decrease in dielectric constant and an increase in AC electrical conductivity, which can be attributed to reduced division and series resistance effects.

Altndal *et al.* (2020) analyzed the influence of an inorganic/organic interfacial layer on the electrical and dielectric properties of Al/p-Si (MS) and Al/($Bi_2Te_3$- $Bi_2O_3$- $TeO_2$-PVP)/p-Si (MPS) type Schottky barrier diodes. An interfacial layer was synthesized utilizing ultrasound-assisted methodologies, and its structural and optical properties were evaluated via FE-SEM, XRD, EDS, and UV-V is techniques. The ($Bi_2Te_3$-$Bi_2O_3$-$TeO_2$-PVP) interlayer has been recognized as a promising alternative to traditional low-dielectric insulators.

In another study, (Hendi 2015) fabricated ZnO-GO nanocomposites and investigated their electrical properties under varying illumination conditions for photodiode

applications. The photoresponsivity of the ZnO-GO/p-Si diode, with a GO: ZnO ratio of 0.03 M, was found to be 0.5 A/W at 100 mW/cm$^2$, which was the highest observed. In this study, it was determined that the utilization of ZnO-GO composites is a viable method for the production of diodes with superior photosensitivity.

Additionally, (Halder *et al.* 2019) employed a hydrothermal method to fabricate $MoS_2$ and $MoS_2$-Graphene composites, and subsequently investigated their optical, electrical, and structural characteristics. An enhancement in photosensitivity of approximately 33 times was observed in composite-based diodes through current density-voltage measurements. This implies potential implementations in photosensitive apparatus.

The electrical as well as photoresponse features of an Au/($CoSO_4$-PVP)/n-Si MPS diode were investigated by (Tataroğlu *et al.* 2020) using spin-coating techniques. Diode parameters, namely n, b0, and Rs, were extracted through the utilization of both thermionic-emission and Norde methodologies. The current conduction mechanisms were analyzed by employing both forward and reverse ln ($I_F$)-ln ($V_F$) plots. An analysis of the voltage-dependent behavior of the capacitance and conductance characteristics was carried out at a frequency of 1 MHz. Additional electrical parameters were obtained by examining the capacitance-voltage characteristics. The voltage-dependent characteristics of Nss were ascertained via capacitance measurements conducted under conditions of dark illumination.

Elgazzar (2020) synthesized copper phthalocyanine and investigated its optical and structural properties. A peak at 2q = 6.75 was detected in the X-ray diffraction patterns, which was identified as the CuPc a-phase. Nanoparticles with an average diameter of 50 nm were dispersed within nanospheres, as evidenced by SEM images. The observed energy gap exhibited a range of 1.62 to 2.90 eV and was contingent upon the energy level of the incoming photon. A Schottky diode was produced via thermal evaporation utilizing Al/CuPc/n-Si/Al materials in the present investigation. The evaluation of electronic properties under low light conditions was conducted through the implementation of I-V, Cheung-Chung, and Norde models. An analysis was performed

on the inherent voltage at a frequency of 1 MHz and the photosensitive response to varying levels of illumination.

In this study, the response to light properties of an Au/($CoFe_2O_4$-PVP)/n-Si (MPS) diode were investigated by conducting current-voltage measurements under different lighting conditions, as reported by Buyukbas *et al.* (2021). The observed trend of increasing photocurrent with increasing light intensity, particularly in the reverse bias region, indicates the favorable response of the diode to illumination. A slope of 1.27 on the Iph-P plot with a double-logarithmic scale indicated a lower density of unoccupied trap levels. The thermionic emission hypothesis, which showed a reduction with an increase in light intensity, was used to estimate the electronic characteristics of the diode. The researchers came to the conclusion that the manufactured MPS diode is a good option for photovoltaic applications due to its strong photo response.

A Schottky device has been fabricated by (Attallah *et al.* 2021) using the Ag/PVA-Ag-Coumarin/n-Si structure. This device is deemed appropriate for optical photodiode applications. The PVA-Ag nano-composite was synthesized and Coumarin dye was incorporated. The device was fabricated using the spin-coating technique. The device exhibited a strong rectification property, leading to the formation of a Schottky junction. The observed device displayed increased values for junction characteristics, including series resistance, ideality factor, and height barrier. The device's capacitance-voltage characteristics displayed notable sensitivity to both the operating frequency and applied voltage.

The investigation of the C/G-V data for the PVP MS structure was conducted by Alptekin *et al*. (2019c), using biases of 4V and a frequency range of 1-500 kHz. Based on the findings of the investigation, it can be inferred that the capacitance and conductivity values at low frequencies were primarily influenced by the surface states (Nss) present in the insulation layer and MS interface.

Alphatekin *et al.* (2019) worked on MPS structures, with a focus on the Au/PVP/n-Si structures. The complex dielectric permittivity, electric modulus, and AC conductivity

were analyzed through the utilization of admittance spectroscopy. The investigation revealed notable frequency and voltage dependence of the magnetic permeability, magnetization, and alternating current values. Enhancements were made to the electrical conductivities of MPS structures, resulting in distinct DC and AC conductivities across various frequency ranges. The observed results present novel opportunities for the utilization of MPS, wherein the dielectric characteristics of the PVP polymer layer in the Au/PVP/n-Si configuration exhibit significant potential in the development of charge/energy storage devices.

The development and analysis of Au-n-Si structure with polyvinylpyrrolidone (PVP) polymer interlayers were investigated by (Alptekin and Altındal 2020). The obtained data from capacitance/conductance-voltage-frequency measurements exhibits encouraging avenues for investigating and utilizing these structures. The frequency-dependent electrical characteristics were observed to be highly sensitive owing to the influence of various factors such as the polymer interlayer, alterations in trap and state levels, and interfacial and dipole polarization. The investigation revealed a notable variation in capacitance and conductivity within the depletion region owing to Nss and polarization. The experimental results indicate a noteworthy enhancement in the operational efficiency of the device upon incorporation of a polyvinylpyrrolidone interlayer fabricated through spin-coating techniques at the gold/n-type silicon interface.

## 2.1 Metal Semiconductor Contacts

The MS contacts can be classified into two categories: rectifying and ohmic. The nature of the contact between the metal and semiconductor is dictated by the work functions of the chosen metal and semiconductor. This determines whether the contact is of the ohmic or rectifying type. In the context of materials engineering, it can be stated that a rectifier contact is formed between a metal and n-type semiconductor when the work function of the metal ($\Phi_m$) is greater than that of the semiconductor ($\Phi_s$). Conversely, an ohmic contact is formed when $\Phi_m$ is less than $\Phi_s$. The occurrence of ohmic contact in metal/p-type semiconductor contacts is dependent on the condition $\Phi_m > \Phi_s$, while

rectifier contact occurs when Φm<Φs, as stated by Pickard. The formation of ohmic and rectifying contacts is determined based on the work functions:

1. Metal/n-type semiconductor contacts

- An ohmic contact is formed when the work function of the metal ($\Phi_m$) has a lower value than the work function of the semiconductor of the n-type ($\Phi_s$). This is known as an ohmic contact ($\Phi_m<\Phi_s$) in materials engineering. The observed phenomenon can be attributed to the favorable energy level alignment between the metal and the semiconductor, which facilitates effective injection of charge carriers and results in a linear correlation between the voltage and current.
- A rectifying contact is formed when the work function of the metal ($\Phi_m$) is greater than the work function of the n-type semiconductor ($\Phi_s$). The observed rectifying behavior can be attributed to the notable energy barrier present at the MS interface. The contact exhibits rectifying behavior, facilitating unidirectional charge transport under forward bias while impeding it under reverse bias.

2. Metal/p-type semiconductor contacts

- An ohmic contact is formed when the work function of the metal ($\Phi_m$) is greater than the work function of the p-type semiconductor ($\Phi_s$). The alignment of energy levels between the metal and the semiconductor facilitates effective injection of charge carriers, resulting in a linear correlation between voltage and current.
- Rectifying contact ($\Phi_m<\Phi_s$): When the work function of the metal ($\Phi_m$) is less than that of the p-type semiconductor ($\Phi_s$), a rectifying contact is established. The presence of an energy barrier at the metal-semiconductor interface leads to rectifying characteristics, which permit current flow in the forward bias direction and hinder it in the reverse bias direction.

## 2.2 Schottky-Mott Theory in Metal-Semiconductor (MS) Conduction

Theoretical models proposed by Schottky and Mott have shed light on the mechanisms underlying the development of a potential barrier at the interface of metal-semiconductor (MS) contacts. As per the Schottky-Mott theory, the origin of $\Phi_B$ can be attributed to the variation in work functions of the metal and semiconductor upon their contact (Baraz 2018).

Upon achieving equilibrium among the metal and the semiconductor of the N type in the MS contact, the Schottky-Mott theory elucidates that the conduction band electrons of the semiconductor exhibit greater energy than those of the metal (Uslu *et al*. 2010). As a result, there is a persistent flow of electrons from the semiconductor to the metal until the levels of Fermi attain equilibrium. The aforementioned process results in a decrease in the population of unbound electrons located at the boundary of the semiconductor's energy band. As the electron's density diminishes, the separation between the conductivity band ($E_C$) and the Fermi level ($E_F$) widens. At thermal equilibrium, the elastic modulus ($E_F$) maintains a constant value. The transfer of electrons from the conduction band to the metal leads to the build-up of positively charged ions within the semiconductor. The process of transferring electrons from the semiconductor to the surrounding metal results in a reduction of electron charges in the semiconductor. The formation of a thin negative layer on the metal due to the accumulation of charges at the MS interface results in the generation of an electric field emanating from the semiconductor to the metal's surface.

The determination of $\Phi_B$ over an MS contact in thermal equilibrium is based on the principle of maintaining a constant vacuum level throughout the transition region. This is a crucial consideration for materials engineers. In order to achieve equilibrium, it is necessary for the vacuum level on the metal side to be in alignment with the vacuum level on the semiconductor side. The power band diagrams depicted in Figure 3.1 (a) and (b) demonstrate the energy levels of the semiconductor and metal materials prior to and following their contact. Figure 3.1(a) displays autonomous energy band diagrams of the metal and n-type semiconductor before their contact, where the metal has a work

function of Φm and the n-type semiconductor has a work function of Φs. The n-type semiconductor exhibits a higher EF level compared to the metal. Noticeable alterations arise in the power bands of the semiconductor, particularly in the state of thermal equilibrium, as illustrated in Figure 2.1(b), subsequent to the amalgamation of the metal and semiconductor.

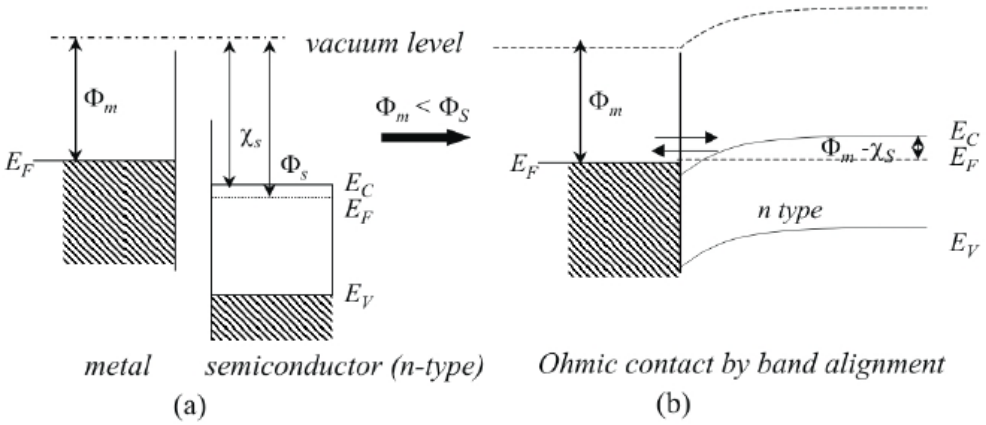


**Figure 2.1** Energy bands of electrons in metal/n-type (MS) interfaces: (a) independent states of metal and semiconductor; and (b) their thermodynamically equilibrated state following contact establishment (Roccaforte *et al.* 2005)

The extent of band bending observed on the side of the semiconductor corresponds to the disparity between the work functions as in Equation (2.1). This discrepancy can be elucidated as follows, as outlined in the studies by (Sharma 1984, Werner *et al.* 1991).

$$qV_i = \Phi_M - \Phi_S \tag{2.1}$$

Where $V_i$ represents the potential difference, $qV_i$ corresponds to the energy barrier encountered by electrons transitioning from semiconductor to metal. The disparity in energy levels between the conductivity band's baseline and $E_F$ is the energy barrier that is noticeable when transitioning from a metal to a semiconductor. Based on Equation (2.1), the energy required for an electron to transition from the semiconductors to the metal is represented by $qV_i$, which is equivalent to the semiconductor's level of energy $\Phi_B$. The Equation (2.2) represents the metal-side energy barrier is as follows:

$$\Phi_B = (\Phi_M - \chi_S) \quad (2.2)$$

The Equation can be written as (2.3) and (2.4):

$$\Phi_S = (\Phi_n + \chi_S) \quad (2.3)$$

$$\Phi_M = (qV_i + \Phi_S) \quad (2.4)$$

By incorporating both Equation (2.1) and Equation (2.2), we can derive the expression for $\Phi_B$ as follows in Equation (2.5):

$$\Phi_B = (qV_i + \Phi_n) \quad (2.5)$$

Where, $\Phi_n$equals ($E_F$), which denotes The disparity between the conduction range of the semiconductors and the Fermi level. Equation (2.1), often referred to as the Schottky barrier, was initially proposed by (Schottky1938). In this context, we have derived Equation (2.5), under the assumption that the surface dipole doping in $\Phi_M$ and $\Phi_S$remains unchanged following the contact between the metal and semiconductor. The $\Phi_B$ can be computed based on its distribution on the semiconductor surface. The value of $\Phi_B$ consistently exceeds the thermal energy, denoted as *kT/q*, at any given temperature. Therefore, the semiconductor surface transforms into a high-resistance depletion region that is free of mobile charges, as per (Mott 1938, Schottky 1938).

## 2.3 Structures Composed of Metal-Polymer and Insulator-Semiconductor

This section focuses on the structures composed of metal-polymer and insulator-semiconductor materials, exploring the intersection of these materials in their formation, properties, applications, and challenges.

### 2.3.1 Metal-polymer structures MPS

When metallic components are combined with polymeric substances, the resulting hybrid materials are referred to as metal-polymer structures. The materials in question have garnered significant attention due to their remarkable mechanical robustness, electrical conductive properties, thermal endurance, and chemical resilience. Several techniques, including melt blending, in-situ polymerization, and solvent casting, can be used to fabricate metal-polymer structures. In situ polymerization stands out among these approaches because it aids in keeping the metal particles evenly distributed throughout the polymer matrix, which is crucial to the composite's performance. Metal-polymer nanocomposites are an interesting hybrid structure, consisting of nanoscale metallic particles embedded in a polymer matrix. These materials are perfect for use in electronics, photonics, and biomedicine due to their exceptional mix of characteristics from their metal and polymer components. However, difficulties persist in regulating the metal particles' shape, distribution, and alignment inside the polymer matrix. Figure 2.2 gives a schematic representation of MPS configuration.

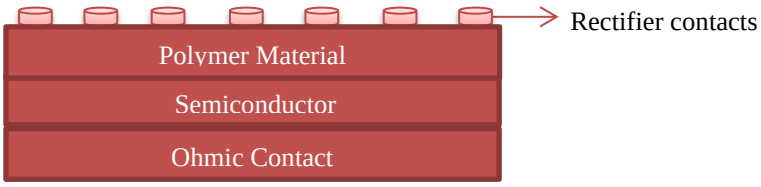


**Figure 2.2** MPS general configuration

### 2.3.2 Insulator-semiconductor structures

Insulator-semiconductor architectures are essential in today's electronics. Most digital integrated circuits rely on devices like this for their most fundamental building blocks, called metal-oxide-semiconductor field-effect transistors (MOSFETs). Typically, silicon (Si) serves as the semiconductor and silicon dioxide ($SiO_2$) as the insulator in such setups. The gate of the MOSFET is isolated by the insulator in these configurations, regulating the current carrying electrons from source to drain in the

semiconductor. The electrical parameters of the device, such as the threshold voltage and transconductance, are therefore profoundly influenced by the insulator-semiconductor interface. Interface states are a difficulty in these architectures because they can trap charge carriers and reduce device performance. The use of high-k dielectrics in place of $SiO_2$ and interface passivation techniques are two examples of the cutting-edge approaches being explored to reduce these contact states.

### 2.3.3 Intersection of metal-polymer and insulator-semiconductor structures

There is a growing interest in the intersection of metal-polymer and insulator-semiconductor structures. In such cases, a metal-polymer material could serve as the gate material in a MOSFET or other semiconductor device. This can potentially allow for new types of electronic devices with improved properties or novel functionalities, such as flexible and stretchable electronics, due to the inherent mechanical flexibility of polymers. However, several challenges need to be overcome to realize this potential. For instance, achieving good electrical contact between the metal-polymer and the semiconductor, ensuring the stability of the metal-polymer under device operation conditions, and managing the thermal expansion mismatch between the metal-polymer and the semiconductor are some of the issues that need to be addressed.

## 2.4 Energy-Band Diagram of Ideal MPS Device

The energy-band diagram of an MPS device in equilibrium, where no voltage is applied, is depicted in Figure 2.3. The diagram is a visual depiction that portrays the energy states of the valence and conduction bands in n-type semiconductors.

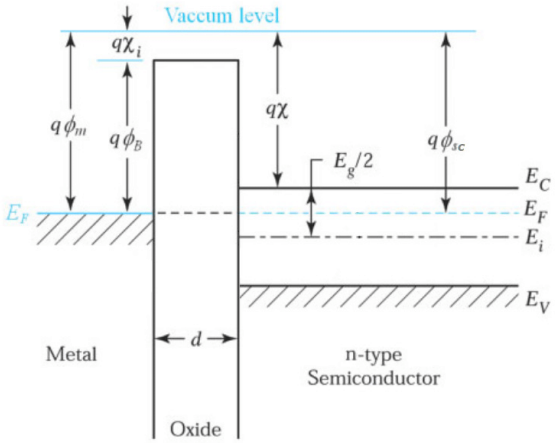


**Figure 2.3** Energy levels of the valence band and the conduction band for n-type semiconductors

The horizontal line depicted in the Figure represents the Fermi level, which is the comprehensive chemical potential for electrons. In n-type semiconductors, the donor energy levels present cause the Fermi level to shift towards the conduction band, leading to an increased likelihood of electrons occupying the conduction band. The energy gap or bandgap ($E_g$) is depicted in the diagram, which represents the energy disparity between the highest point of the valence band and the lowest point of the conduction band. This gap represents the minimum energy required to move an electron from the valence band into the conduction band, thereby transforming it from a bound state within an atom to a free state which can participate in conduction.

Understanding the energy-band diagram is crucial for analyzing the behavior of the MPS device. The diagram can assist in predicting how the device will respond under various conditions and biases, helping to inform design considerations and functionality optimization. By visualizing the position of energy bands, one can predict various properties and behaviours of the semiconductor, such as its conductivity, carrier concentration, and response to thermal energy. As such, the energy-band diagram is an invaluable tool for semiconductor device engineering and design. Continuing investigations into MPS device operation and optimization can further refine our understanding of these devices and lead to the development of more efficient and powerful semiconductor technologies. Future work in this area will benefit from both

theoretical analysis, such as energy-band modeling, and experimental validation of these models.

According to the findings of (Yücedağ 2007, Ersöz 2015), certain key features can delineate an ideal MIS structure. Notably, when no feed is present, the work function (Φms) is characterized by a value of zero. Φms is essentially the energy disparity between the metal's work function (Φm) and the semiconductor's work function (Φs). Therefore, in an ideal MIS system, under the conditions of zero feed, the work functions of the metal and semiconductor are equivalent, yielding no discernable energy difference between Φm and Φs. Equation (2.6) and (2.7) shos the work functions (Φms and Φs):

$$\phi_{\mathrm{ms}} = \phi_{\mathrm{m}} - \phi_{\mathrm{s}} = \left(\chi + \mathrm{E_g}/2\mathrm{q} - \psi_{\mathrm{B}}\right) = 0 \qquad \text{For n-type-si} \qquad (2.6)$$

$$\Phi_{ms} = \Phi_m - \left(\chi + \frac{E_g}{2q} - \psi_B\right) = 0 \qquad \text{For p-type-si} \qquad (2.7)$$

So, $E_g$ represents the semiconductor materials possess a characteristic known as bandgap or forbidden energy, and ψB signifies the difference in energy between the Fermi energy level ($E_F$) and the intrinsic Fermi energy level (Ei) is being discussed. In the absence of an applied voltage, the energy band arrangement adopts a flat state, which is commonly referred to as the flat-band condition. Under equilibrium, the energy band of the device remains flat with no gradient, indicating the absence of any external electric field.

## 2.5 MPS Structure Biasing

The response of an MPS device to an applied bias can be comprehended by analyzing the alterations in it bands diagram upon voltage application. The manipulation of energy bands' relative positions through the application of voltage induces changes in carrier behavior within the device. Upon application of a positive bias to the metal contact, the energy bands within the semiconductor material undergo an upward bending near the

metal-semiconductor (MS) interface. This results in a reduction of the barrier for the injection of electrons from the metal into the semiconductor. The phenomenon is commonly denoted as forward bias. When a device is under forward bias, conduction can occur as a result of majority carrier injection if the applied voltage surpasses the device's built-in potential. Alternatively, the application of a negative bias results in the downward bending of energy bands in the vicinity of the metal-semiconductor (MS) interface. This phenomenon leads to an elevation in the barrier for the injection of electrons from the metal to the semiconductor. The phenomenon being referred to is commonly known as reverse bias. The device exhibits a significant reduction in current flow under reverse bias due to the migration of majority carriers away toward the junction, leading to the formation of a depletion region. The degree of band bending and, consequently, the barrier for the carrier injection can be modulated by adjusting the amplitude of the applied bias. The capability to manipulate the carrier mobility renders MPS devices advantageous for diverse applications such as electronic changing and signal amplification. The proper biasing for an MPS structure is crucial for its optimal performance. It regulates the movement of charge carriers within the device, thereby influencing its electrical properties and overall functionality. The comprehension and regulation of bias is therefore crucial in the development and functioning of MPS-oriented apparatus.

### 2.5.1 Depletion region in metal phosphide emiconductor structures

The depletion region, also known as the depletion layer or depletion zone, is an intrinsic characteristic of semiconductor junctions, such as those found in Metal-Phosphide-Semiconductor (MPS) devices. It plays a significant role in determining the electrical properties and behavior of the device. When no bias is applied, the depletion region extends into the semiconductor from the interface between the metal and the semiconductor, characterized by a strong electric field created by the charge difference across the junction. Under reverse bias conditions, the depletion region widens, while under forward bias conditions, it narrows. Understanding the dynamics of the depletion region under different conditions is critical for the design and operation of MPS

devices, enabling their effective utilization in a wide array of electronic applications. (Rhoderick *et al.* 1988)

### 2.5.2 Accumulation in metal phosphide emiconductor structures

The accumulation layer is a key aspect of the operational behavior of Metal-Phosphide-Semiconductor (MPS) structures, and it plays a significant role in the functionality of such devices. It refers to the condition where an abundance of majority carriers is drawn to the surface of the semiconductor, usually due to the application of an external electric field. In an MPS structure, when a bias of the same polarity as the majority carriers is applied to the metal contact, the majority carriers are attracted towards the MS interface, creating an accumulation layer. This layer alters the electric field and band-bending conditions within the device, and is a critical factor in various device operations, such as conduction and capacitive behavior. Understanding the conditions under which accumulation occurs, and the effects it has on device operation, is essential for the effective design and utilization of MPS devices in electronic applications. (Rhoderick *et al.* 1988)

### 2.5.3 Inversion in metal phosphide emiconductor structures

Inversion is a key operating condition in Metal-Phosphide-Semiconductor (MPS) structures and is fundamental to the function of many semiconductor devices, such as MOSFETs. The inversion layer, also known as the inversion channel, forms when an external electric field forces the minority carriers in a semiconductor to accumulate at the semiconductor-insulator interface. This accumulation occurs to such an extent that the semiconductor surface near the interface contains a higher concentration of minority carriers than majority carriers, effectively inverting the type of semiconductor near the surface. Understanding this inversion condition is crucial for designing and optimizing MPS-based devices for a wide range of applications. This understanding of inversion will continue to drive innovation and advancement in semiconductor device technology. (Rhoderick *et al.* 1988)

## 2.6 Ideal MIS/MPS Structures and Electrical Properties

The fundamental electrical characteristics of optimal MIS or MPS structures are centered on their capacity to regulate current conduction through the manipulation of the charge distribution within the semiconductor. The physical properties of the materials, doping concentration, and applied voltage have a significant impact on the resulting properties. The determination of the threshold voltage (Vth) is a crucial aspect of MIS/MPS structures and is influenced by various factors such as the disparity in work function between the metal gate and the semiconductor, the capacitance of the insulator, and the bulk charge present in the semiconductor. The electrical capacitance of a material is dependent on the magnitude of the applied voltage and can be categorized into three distinct phases: accumulation, depletion, and inversion. The transport of the carriers across the junction governs the Current-Voltage (I-V) features of MIS/MPS devices. The MIS/MPS devices exhibit a gate voltage-dependent transition from non-conductive to conductive states. The breakdown voltage refers to the maximum voltage that a device can withstand under reverse bias conditions before it experiences breakdown and initiates a significant current flow (Zhang *et al.* 2020).

# 3. MATERIALS AND METHODS

## 3.1 Preparation of Au/PVA/n-Si MPS

Creating an MPS structure with a gold (Au) metal contact, polyvinylpyrrolidone (PVA) insulator, and n-type silicon (n-Si) semiconductor involves several important steps.

### 3.1.1 Crystal clearing

Given the sensitivity of semiconductor devices to impurities and surface defects, these cleaning steps are fundamental to the preparation of high-quality MPS structures. They significantly influence the final device's performance and reliability and contribute to the reproducibility of the device fabrication process. Future advancements in cleaning techniques will continue to enhance the quality and performance of semiconductor devices. For the creation of high-quality MPS structures, ensuring the cleanliness of the semiconductor crystal is critical. A well-cleaned crystal minimizes surface defects, which could otherwise impact the overall performance of the device. However, laboratory environments, chemical cleaning procedures, and sample growth can introduce impurities onto the crystal surface. Therefore, thorough cleaning procedures are essential. In this study, n-Si was employed as the semiconductor, featuring a (110) orientation, a thickness of 280 μm, a resistivity of 4.45 Ω.cm, and a Polyvinylpyrrolidone (PVA) thickness of 500 A.

### 3.1.2 Ohmic contact formation in Au/PVA/n-Si (MPS) structures

In the fabrication of Au/PVA/n-Si (MPS) structures or Schottky diodes, a critical step involves the creation of ohmic and rectifying contacts using a high vacuum metal evaporation system. The n-Si substrate, having undergone rigorous cleaning, is readied for ohmic contact deposition by placing a copper mask on it, with the matte side directed downwards. The substrate is then inserted into the thermal evaporation system, the chamber is sealed promptly, and the vacuuming process is initiated to reduce the

internal pressure to $10^{-6}$ Torr. When the target pressure is achieved, an electric current of about 35 A is passed through one of the filaments to trigger the evaporation of gold particles, which have been chemically cleaned to achieve a purity of 99.999%. To prevent evaporative foreign substances from adhering to the crystal, an initial shielding phase is employed wherein a metal curtain covers the matte surface of the crystal during the first stage of gold evaporation. Upon completion of this stage, the metal curtain is removed, enabling the evaporated gold particles to deposit onto the crystal's matte surface, forming a gold layer approximately 1500 Å thick. This meticulous process results in the formation of an ohmic contact, a crucial element ensuring the efficient and reliable operation of the MPS structures or Schottky diodes. The utilization of a copper mask is employed for the purpose of establishing ohmic contact shows in Figure 3.1.

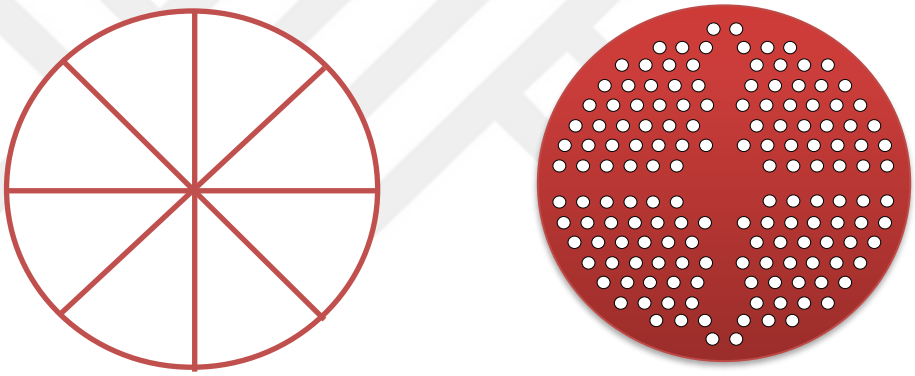

**Figure 3.1** Copper mask is employed for the purpose of establishing ohmic contact

To establish ohmic contact characteristics for the Au layer coated on the back surface, an annealing process was initiated. This was accomplished through the heating of a quartz tube by the current passing through the resistance wire, with the ambient temperature controlled by a dedicated control unit. A chromel-alumel thermo-couple, located where the sample was placed inside the quartz tube, further regulated the temperature. During the annealing process, a controlled $N_2$ gas flow was maintained, measured via a flowmeter. The gas used for the oxidation process was directed through a moisture trap (glass tube) attached to a liquid nitrogen container, as indicated in Figure 3.4, to remove any residual moisture. For about 60 minutes, the $N_2$ gas was

introduced into the medium at a rate of approximately 2 lt/min. This allowed gold to precipitate into the silicon crystal, giving the expanded gold layer the property of ohmic contact.

In this study, MS structures were fabricated on an n-type silicon (n-Si), (100) substrate with a thickness of 350 m and a resistivity of 10.cm. Under the same circumstances, the structures were made with and without a Polyvinylpyrrolidone (PVA) interlayer. After being immersed in methanol, the n-type silicon substrate was rinsed in ionized water with a resistance of 18 megaohms per centimeter. An ultrasonic bath was used to rinse the sample in ionized water for about 10 minutes after it had been etched in a hot solution of $H_2O$, $NH_4OH$, and $H_2O_2$ (65:13:13 v/v). After a second round of etching with an $H_2O$:HF (24:1 v/v) solution, the substrate was rinsed with ionized water and dried with dry nitrogen ($N_2$) gas. After a thorough cleaning in an ultrasonic bath, high-purity Au (99.995%) was deposited using a metal evaporation method on the n-Si substrate's back to a thickness of 1200 A. Throughout the procedure, the system pressure was maintained at 106 Torr. To achieve a low-resistance contact, an n-Si substrate that had been coated with Au was sintered in a nitrogen gas (N2) environment for 5 minutes at 500 degrees Celsius. The first type (Au/n-Si) MS structure was completed using Polyvinyl Alcohol (PVA) purchased from Sigma-Aldrich. The second kind of MPS structure was manufactured by dissolving PVA in ultrapure water to create a PVA solution. After mixing 1 gram of PVA with 9 grams of ultrapure water using magnetic stirring for 5 minutes, we now have a PVA-water combination. The coating process was carried out in two stages. The films were first spun for 30 seconds at 2000 RPM, and then again for another 30 seconds at 4000 RPM. Spin coating (Spin 150i apparatus with Polospro v3.16 software) was used to apply a PVA solution to the n-Si substrate. Finally, employing a metal shadow mask in a high vacuum metal evaporation system, 2 mm in diameter Au rectifying contacts with a thickness of 1200 were placed onto the PVA layer. (Alptekin *et al.* 2019a) stated that the manufacturing procedure for second-type MPS structures was successfully completed.

### 3.1.3 Formation of the insulating polymer layer using the spin coating method

The spin coating method has been widely used for many years in the production of thin film layers. The insulating polymer layer was formed using the spin coating method. The spin coating method is often preferred due to its advantages, such as not having to reach high temperatures during application, and being able to grow an insulating layer of desired thickness on almost all types of substrates (n-Si) (Alptekin *et al.* 2019b, Demirezen *et al.* 2010). The principle of the spin coating process is based on dropping a drop of the prepared solution onto the surface to be coated and then spinning it at high rotation speeds. The film thickness depends on the characteristics of the solution (viscosity, drying speed, solid ratio, and surface tensions) and the process conditions (rotation, acceleration). The film coating method by rotation can be divided into four stages: Accumulation (dropping), spinning, end of rotation (stop), and evaporation. The spin coating device is given below in Figure 3.2.


**Figure 3.2** Spin coating device

### 3.1.4 Creating the rectifier contact

The formation of the rectifier contact, or Schottky contact, is a critical step in the fabrication of Au/PVA/n-Si MPS structures. This is the junction where the metal (Au) comes into contact with the semiconductor (n-Si), forming a Schottky barrier that allows current flow in one direction and limits it in the other, thereby rectifying the current. After the insulating polymer layer has been created via the spin coating method, the final step in the preparation of the MPS structure is to form the rectifier contact. In this process, a thin layer of Au is evaporated onto the top surface of the PVA layer.

In this study, the n-Si crystal, coated with PVA, was placed on the copper mask as shown in Figure 4.1 with its shiny surface facing downwards. Au wire, chemically cleaned, with a diameter of 2 mm and length of 1 cm, was placed on the filament and evaporated in a vacuum of $10^{-6}$ Torr. This process resulted in the formation of Au rectifier contacts, 2 mm in diameter and 1200 Å in thickness, on the shiny surface of the crystal in the vacuum system. Thus, as depicted in Figure 3.3, the fabrication process of the Au/PVA/n-Si (MPS) structures was successfully completed.

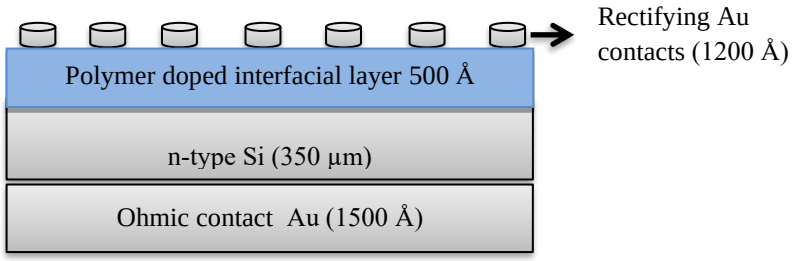


**Figure 3.3** The structure of Au/PVA/n-Si(MPS)

## 3.2 Experimental Measurement Process

### 3.2.1 I-V measurement system

The measurement process was conducted in the Solid State Laboratory at Gazi University's Faculty of Arts and Sciences. A Keithley 2400 current-voltage

measurement device, as shown in Figure 3.4, was utilized for current-voltage (I-V) measurements of the fabricated Au/PVA/n-Si (MPS) structures. This instrument is capable of both sourcing voltage to measure current and sourcing current to measure voltage. It has a wide measurement range, with voltage measurements from ±1 μV to ±200 V and current measurements from ±10 pA to ±1 A, delivering an accuracy of ±0.15%. The measurements were conducted via an IEEE-488 AC/DC converter board, controlled by a Hewlett Packard computer.


**Figure 3.4** Keithley 2400 current-voltage measurement device (Gazi university lab 2023)

### 3.2.2 C-V and G-V measurement system

The Hewlett Packard 4192A LF Impedance Analyzer was utilized to conduct C-V and G/ω-V measurements on the Au/PVA/n-Si (MPS) structure within the 5kHz-13MHz frequency range. The computer was connected to the analyzer through an IEEE-488 AC/DC converter card, which facilitated accurate management of the measurement and data acquisition procedures. The voltage-dependent capacitance (C-V) and conductance (G/ω-V) were measured over a voltage sweep of -4V to +5V with a step size of 0.05 V. The selection of the frequency range was made with the intention of obtaining comprehensive understanding of the electrical properties of the MPS device, encompassing both low and high frequencies. The experimental arrangement facilitated

the acquisition of comprehensive data regarding the dynamic capacitance and conductance alterations of the device in response to varying bias voltage. This information is crucial in comprehending the device's performance under diverse operational circumstances. The instrumentation employed for these measurements is depicted in Figure 3.5. The diagram depicted herein illustrates the experimental arrangement, elucidating the manner in which the MPS architecture is connected to the impedance analyzer and the computing system. The experimental measurements were conducted under controlled conditions to mitigate the impact of extraneous variables and to establish the dependability of the acquired data.


**Figure 3.5** Hewlett Packard 4192A LF Impedance Analyzer was utilized to conduct G/ω- V and C-V measurements on the Au/PVP/n-Si in an experimental setup (Gazi university lab 2023)

# 4. RESULTS AND DISCUSSION

## 4.1 Analysis of (I-V) Characteristics

Upon exposure to light, the device undergoes a process where in photons possessing adequate energy levels stimulate the movement of electrons from the valence band to the conduction band, resulting in the creation of electron-hole pairs. These pairs exhibit electrical conductivity under the influence of an external electric field (voltage). This leads to an increase in current at a given voltage, shifting the I-V curve upwards. The more intense the light (up to the saturation point), the more electron-hole pairs are generated, and the more the curve shifts. In the case of an MPS structure, the addition of the polymer layer could introduce additional complexity. The polymer could serve as a charge transport layer, facilitating the movement of electrons or holes, or it could serve as an energy barrier, impeding their movement. The I-V characteristics would depend on the specific properties of the polymer and its interactions with the metal and semiconductor layers. In Figure 4.1, Figure 4.2 the I-V characteristics of a MPS structure under both dark and illuminated conditions light at 100mW/cm$^2$ display different behavior due to photoexcitation of carriers and ln(I)-V characteristics, respectively, have a good rectification ratio in the voltage range of -4 to +4V.

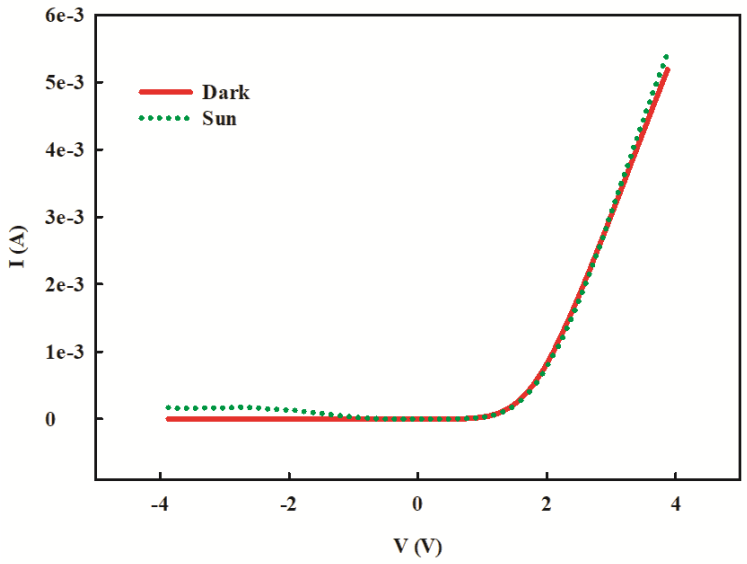


**Figure 4.1** I vs V graph for MPS in dark and under 100 mW/cm$^2$ conditions

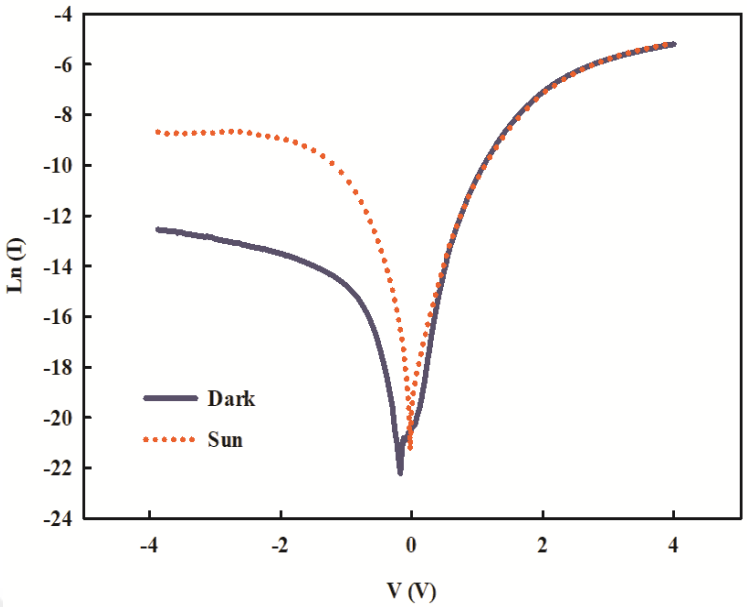


**Figure 4.2** Ln(I)-V graph for MPS in dark and under 100 mW/cm$^2$ conditions

The Thermionic-Emission (TE) theory can be utilized to discern the electrical characteristics of Metal/Semiconductor (M/S) diodes, both those with an inter-layer and those without. Particularly, this is applicable when the resistance (*Rs*) and n values exceed one. The evaluation of forward-bias IV data through the formula (*kT/q*) enables the calculation of several factors. These include the saturation-current, denoted either as *Is* or *Io*, *n*, and BH, which can be either voltage dependent or zero, represented as $\Phi_{B0}$ or $\Phi_{B,}$ respectively (İlke Taşçıoğlu *et al.* 2014). Equation (4.1) calculated the *I(V)*

$$I(V) = I_o \left[ exp\left(\frac{q(V-IR_S)}{nkT}\right) - 1 \right] \quad (4.1)$$

Where $I_o$ represents the saturation current, while *IRs* denotes the voltage drop resulting from series resistance. The variable $T$ denotes temperature and is quantified in the unit of Kelvin (K). The Boltzmann constant is denoted by $k$. Equation (4.2) shows the calaculation of $I_o$.

$$I_o = (S.A^*.T^2).exp\left(\frac{-q\Phi_{B0}}{kT}\right) \quad (4.2)$$

Where schottky contact area, denoted by $S$, and Richardson constant, denoted by $A^*$. For n-type Silicon (n-Si), the Richardson constant is commonly taken to be 112 A. $(cm^2K^2)^{-1}$. Using the extracted value of $I_o$ (the saturation current), we can get the value of $B_0$, which represents the zero-bias $\Phi_B$, in the following equation (4.3).

$$\Phi_{Bo} = \left(\frac{kT}{q}\right).ln\left(\frac{S\,A^*\,T^2}{I_0}\right) \quad (4.3)$$

In the linear regime, the slope of the natural logarithm (ln) of the current (I) versus voltage (V) curve plays a pivotal role in the formulation of Equation (4.4). Concurrently, the ideality-factor emerges as a crucial diode parameter, which can be ascertained employing Equation (4.1).

$$n = \frac{q}{kTtan(\theta)} = (\frac{q}{kT})\frac{dV}{dLn\,(I)} \quad (4.4)$$

The ideality factor exhibits a persistent inclination to exceed unity values, irrespective of the incidence or non-incidence of light, and even under an irradiance of 100 $mW/cm^2$. The escalation observed in ideality factor values can be attributed to various factors. The variables being examined include the presence of an interlayer consisting of (Au-PVA-n-Si) polymer, the existence of interface states referred to as Nss, the extent of the depletion layer width (Wd), the heterogeneity of the barrier, and the decrease in the ΦB caused by image force, as shows in Equation (4.5)

$$n(V) = 1 + (d_i/\varepsilon_i) \cdot [(\varepsilon_s/W_d) + qN_{ss}] \quad (4.6)$$

The potential influence of barrier inhomogeneity at the MS junction, especially the lower patches proximate to the average $\Phi_B$, may have a more pronounced effect on charge transport across the $\Phi_B$. The observed phenomenon could be associated with the heightened mobility of electronic charges within the lower barrier domains. This increased mobility subsequently results in a corresponding elevation in both the ideality factor and the current.

Also in Figure 4.3, the resistance-voltage (Ri-V) characteristics of a structure, both in dark conditions and under illumination 100 mW/cm$^2$, influenced by several factors, including the materials used in the structure, the quality of the interfaces, the nature of the junctions, and the intensity and wavelength of the illumination. Under dark conditions, the resistance is determined by the junction properties and the inherent electronic properties of the materials, while under illumination, photons with enough energy can generate electron-hole pairs in the semiconductor material, leading to an increase in current and therefore a decrease in resistance.

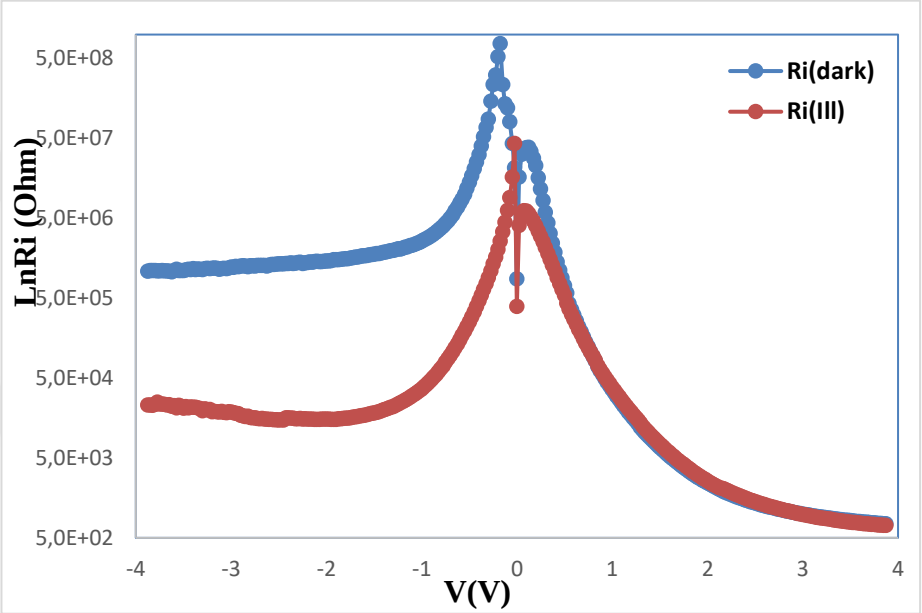


**Figure 4.3** The structure resistance Ri-V in dark and illumination 100 mW/cm$^2$

The plots dV/d(lnI) versus I and H(I) versus I in a MPS structure like Au/PVA/n-Si can be complex due to the various transport and recombination mechanisms that might be at play. In Figure 4.4, t, dV/d(lnI) represents the differential resistance as a function of the current, while H(I) refers to a mathematical transformation of the current, a derived quantity, or some other quantity that is a function of the current. The PVA layer in the MPS structure can significantly affect these plots, as it can serve as a transport layer, an additional barrier, or a trap layer, influencing the carrier transport and recombination mechanisms and altering the dV/d(lnI) and H(I) characteristics.

At high enough forward bias voltages, the I-V data of the Au-PVA-n-Si (MPS) Schottky Diode may be used to calculate n, Rs, and $\Phi_B$ using the corresponding Cheung functions as in Equation (4.5) and Equation (4.6).

$$dV/dln(I) = n \cdot (kT/q) + RsI \tag{4.5}$$

$$H(I) = V - n \cdot (kT/q) \cdot \ln (I/AA^*T^2) + R_sI = n\Phi_b + RsI \tag{4.6}$$

The plots of $dV/dln(I)$ against $I$ and $H(I)$ against $I$ are demonstrated in Figure 4.4

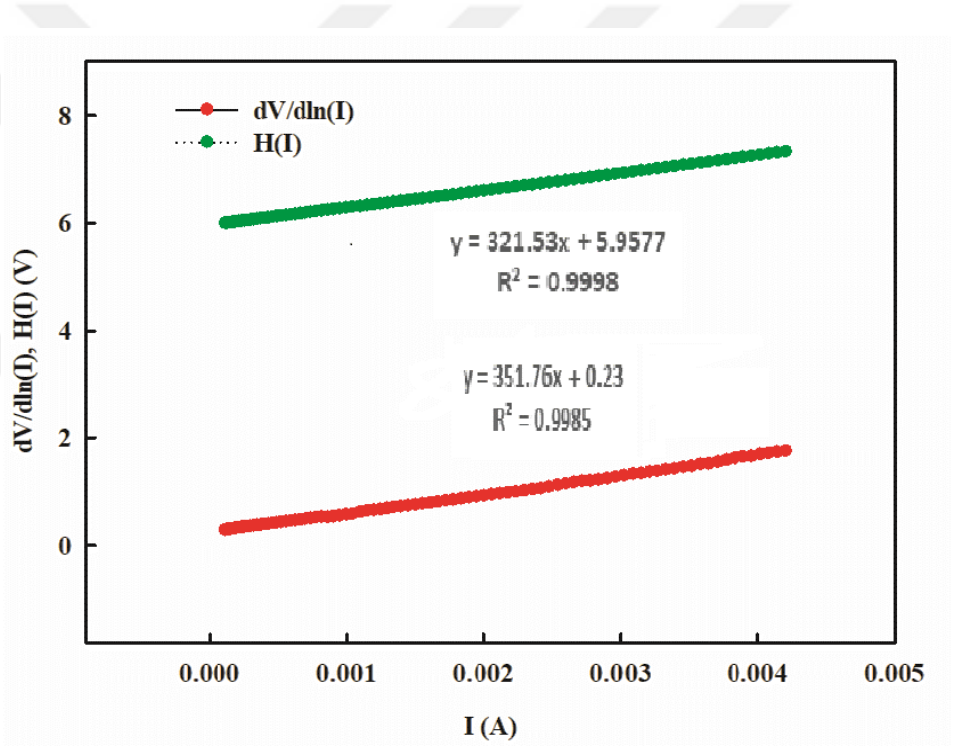


**Figure 4.4** dV/dln(I) and H(I) vs I curves of the MPS structure in dark

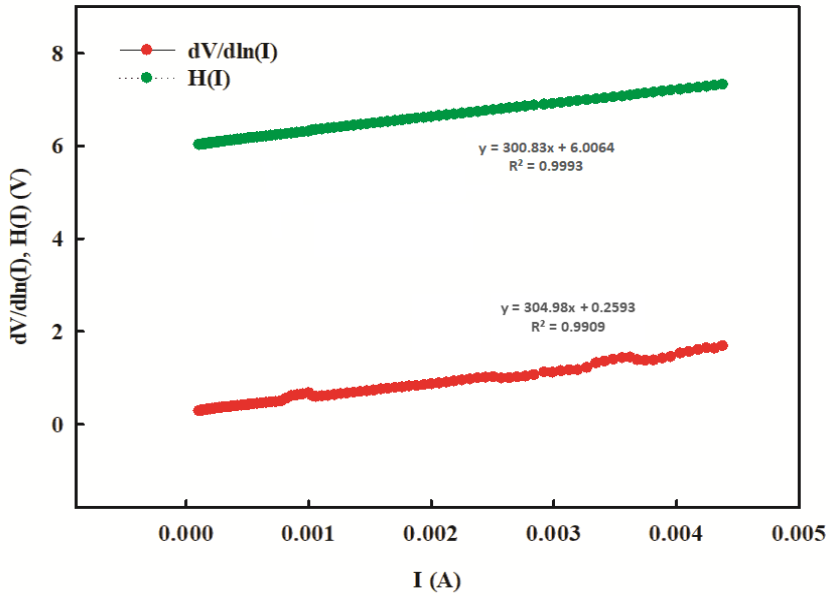


**Figure 4.5** dV/dln(I) and H(I) vs I curves of the MPS structure under illumination 100 mW/cm$^2$

Figure 4.5 and 4.6 shows the ln(I) against V for both types of diodes, the relationship between current and voltage exhibits a power-law behavior, represented by I~Vm. In this relationship, 'm' can be described as the slope of the respective plots for each region.

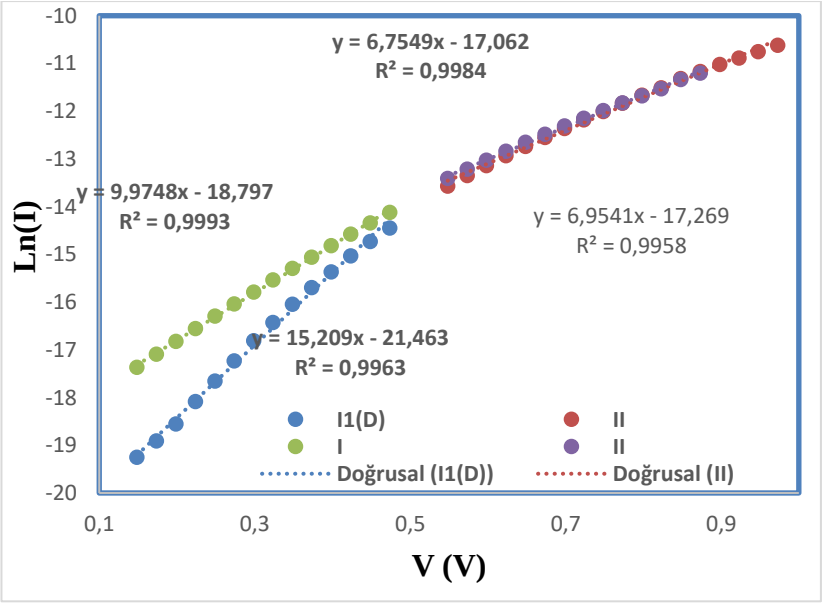


**Figure 4.6** ln(I) vs V of the MPS structure in dark and under illumination 100 mW/cm$^2$

For the illumination case, y = 10.16x- 18.864, with $R^2$ = 0.9988, indicates a strong positive linear relationship between y and x, where y might represent voltage or another response variable and x the independent variable I. The $R^2$ value near 1 suggests that this linear model explains about 99.88% of the variance in y, implying a very good fit. For the dark condition, the Equation is y = 15.032x- 21399 with $R^2$ = 0.9969 also, this suggests a strong positive linear relationship, though with a different slope and intercept, and the model explains about 99.69% of the variance in y, again a very good fit.

The utilization of the modified Norde function was employed to determine the $B_H$ and Rs values in both study cases as in Equation (4.7)

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q} \ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{4.7}$$

Where the current-voltage (I-V) characteristics obtained under forward bias are utilized to compute I(V), while γ, an integer without dimensions, must exceed the ideality factor obtained from the gradient of ln(I)-V curves for two structures.

Figure 4.7 shows the F(V) vs V graph between 0 – 4 V.

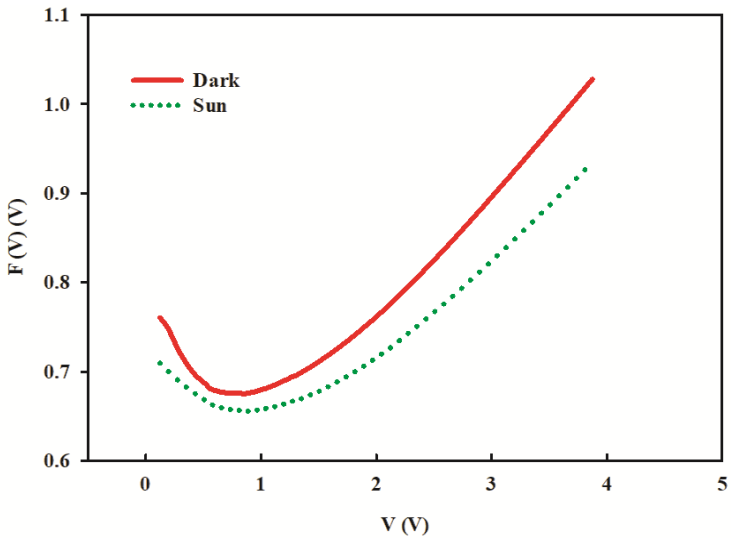


**Figure 4.7** F(V) vs V graph in dark and illamunation 100 mW/cm$^2$

Also, the Figure 4.8 shows the both types of diodes exhibit a power-law relationship between current and voltage. The $I_F$-V plots of the Au/PVA/n-Si under forward bias were analyzed in both dark and illuminated conditions using a double-logarithmic scale.

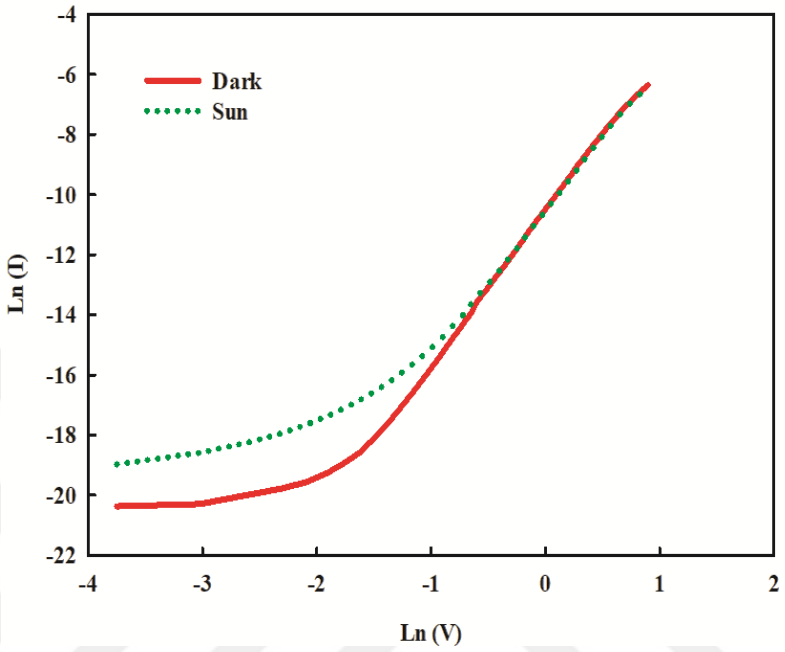


**Figure 4.8** Forward bias double-logarithmic ln$I_F$-lnV plots of the Au/PVA/n-Si in dark and illumatation cases

## 4.2 Analysis of Frequency Dependent (C-V) and (G/ω-V) Profiles Characterization

We could not measure under light at 5 kHz because there is too much noise for G/$\omega$.The observed C-V and G/$\omega$-V curves of the Au/PVA/n-Si (MPS) structure, as depicted in Figures 4.9, 4.10, and 4.11 for illumination and dark conditions, indicate a temperature-dependent behavior with respect to the applied voltage. The observed regions of accumulation, reversal, and depletion exhibit a distinct variation, with a more pronounced alteration in the agglomeration and depletion regions. The reduction in peak performance within the condensation zone is inversely proportional to the frequency, leading to an increase in series resistance and bending. The distribution of the voltage depletion layer on the diode is influenced by the resistance, interface layer, and applied voltage. The frequency-dependent variations of C and G/$\omega$ in the depletion and reversal

regions are responsible for the establishment of surface charges or traps in their respective states.

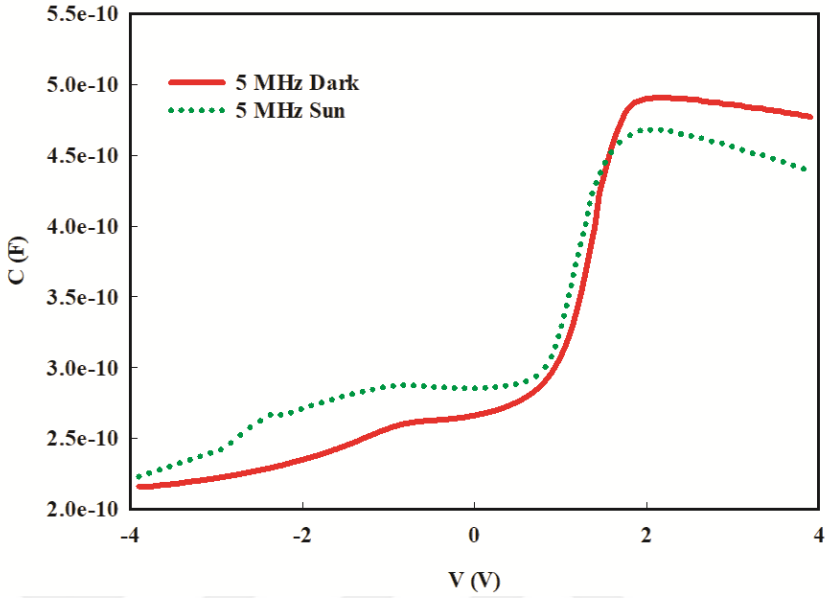


**Figure 4.9** Capacitance (F) - Voltage (V) for illumination mode 100 mW/cm$^2$ under reverse and forward biases

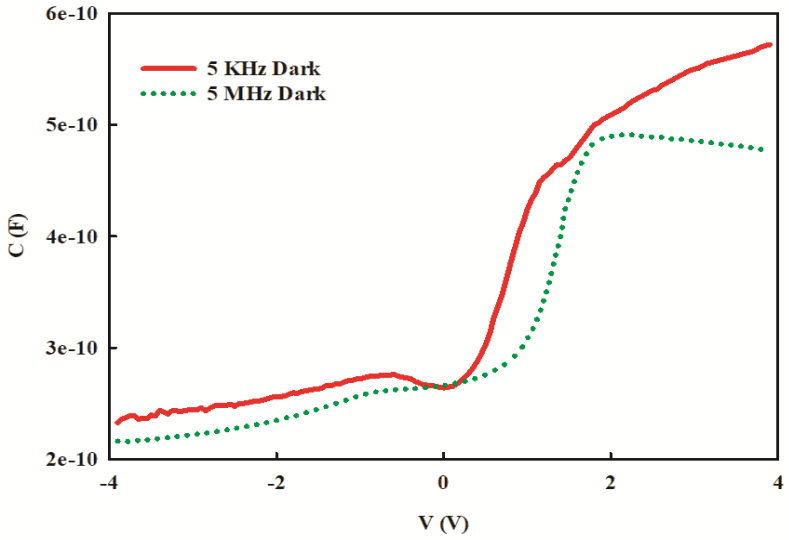


**Figure 4.10** Capacitance (F)- Voltage (V) for dark state under reverse and forward biases

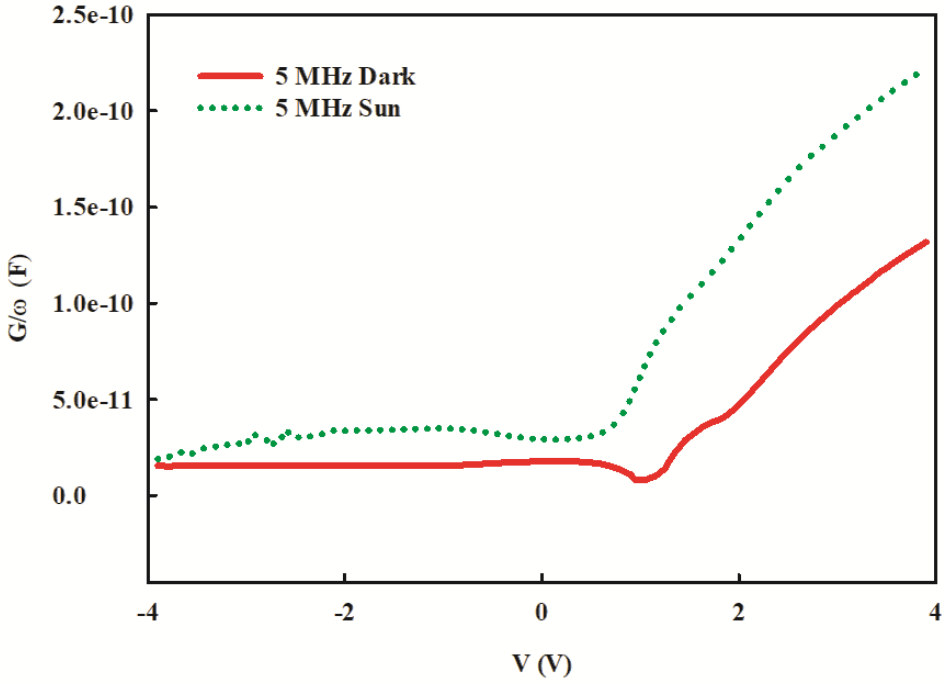


**Figure 4.11** Graphical representation of G/ω-V for each structure under reverse and forward biases

Conventionally, in a simple ohmic resistor, the resistance remains constant regardless of the applied voltage. However, your observations suggest a non-ohmic behavior where resistance increases with voltage. This might be attributed to phenomena such as electron trapping, barrier lowering or contact resistance changes that are prevalent in certain materials and structures. Also, given that this non-ohmic behavior is observed in both non-interlayered and polymer interlayered structures, the polymer interlayer doesn't seem to modify this aspect of the electrical behavior significantly. However, comparing the exact change in resistance with voltage across the two types of structures can provide insights into the subtle impacts of the interlayer. If the increase in resistance with voltage is less pronounced in the polymer interlayered structures, this suggests that the interlayer could be helping to stabilize the electrical behavior of the material. The fact that this increasing resistance trend is observed under both 100 mW/cm² illumination and in the dark condition suggests that the generation of photo-induced carriers does not drastically affect this aspect of the electrical characteristics. However, there might be a difference in the absolute resistance values or the rate of change of resistance with voltage under these two conditions. This could indicate that photo-

generated carriers are influencing the electrical properties but are not enough to switch the material to an ohmic behavior. Since the resistance is frequency-dependent, it's important to evaluate whether the rate of change of resistance with voltage also depends on the frequency. A strong frequency dependence might indicate that alternating current (AC) effects such as the skin effect or dielectric losses are playing a significant role in the observed behavior. The true value of Rs, as derived from the strong accumulation area at sufficiently high frequencies (f ≥ 0.5 MHz), is determined using Equation (4.8).

$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2} \tag{4.8}$$

Figure 4.12 shows the comparison of voltage (V) versus structure resistance (Rs) for Au/PVA/n-Si

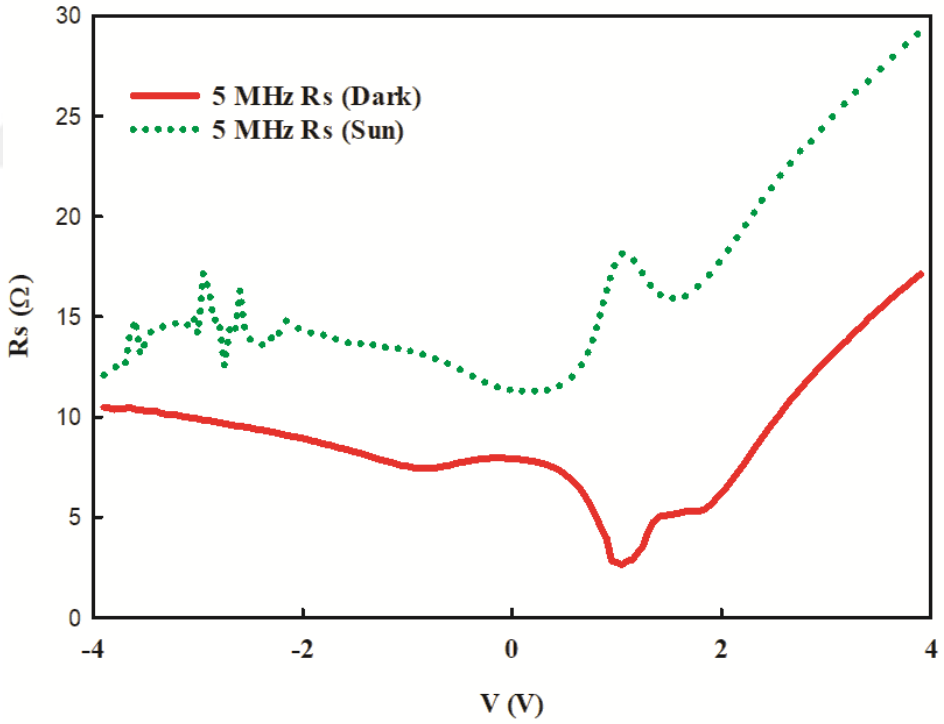


**Figure 4.12** Comparison of voltage (V) versus structure resistance (Rs)

The capacitance of the depletion layer in Schottky barrier diodes (SBDs), or structures of the Schotky type, varies with the applied reverse bias (VR) according to the following Equation (4.9)

$$C^{-2} = \frac{2(V_R+V_0)}{q\varepsilon_S N_D A^2} \tag{4.9}$$

Where The intercept of the $C^{-2}$ vs V plot at zero biases is denoted by $V_0$, while A represents the rectifier contact area of the structure. The $V_0$ and $N_D$ parameters were determined by analyzing the linear portion of the $C^{-2}$-V graphs for two distinct structures. The $E_F$ value was subsequently calculated using the relevant Equation (4.10)

$$E_F = \frac{kT}{q} \ln\left(\frac{N_C}{N_D}\right) \tag{4.10}$$

Figure 4.13 shows the reverse bias capacitance-voltage characteristics of an Au/PVA/n-Si structure at room temperature for frequency of 5 MHz. The plot exhibits a linear relationship with varying slopes across a wide range of reverse bias.

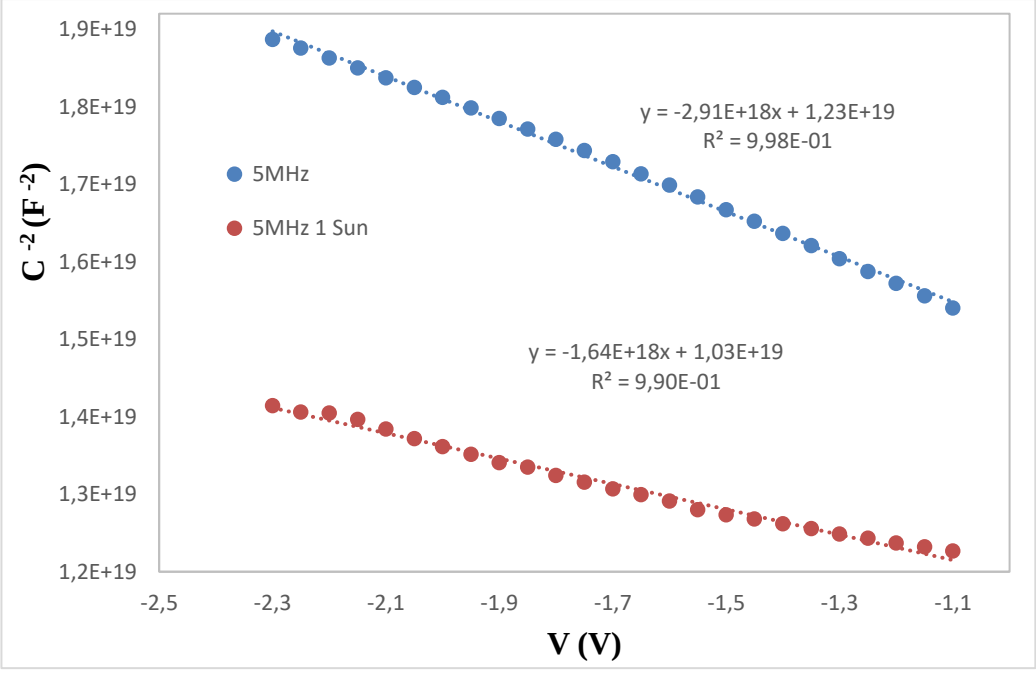


**Figure 4.13** $C^{-2}$ - V graph of the Au/PVA/n-Si structure for 5 MHz

Table 4.1 Shows the electrical characteristic of Au-PVA-n-Si with series resistance Rs and shunt resistance Rsh.

**Table 4.1** Electrical characteristic of Au-PVA-n-Si

| | **I(Dark)** | **II (Sun)** |
|---|---|---|
| $I_o$ (A) | $4.1e^{-10}$ | $3.16224e^{-8}$ |
| n | 2.5449 | 5.5575 |
| $\Phi_{B0}$ (eV) | 0.8183 | 0.7137 |
| $R_s$ (Ω) | 710 | 700 |
| $R_{sh}$ (MΩ) | 1.1 | 0.025 |

## 5. CONCLUSIONS AND RECOMMENDATION

This study focuses on the Au /PVA/n-Si. The crystals are fabricated using ultrasonic technology, with a melting point of 550°C. The crystals are cooled to a room temperature with a 99.995% melting point of Si and Au. The crystals are heated to 1200-1500 °C, with a melting point of 10-10 nm. The electrochemical properties of the crystals are studied using a G/ω-V and C-V electrode. The Hewlett Packard 4192A LF Electromagnetic Analysometer is used to analyze the C-V and G/w-V electrodes. An IEEE488 AC/DC converter is used to control and measure all electrodes. The study also investigates the use of magnetic polarization (MPS) techniques in C-V and G/w-V electrode methods. The investigation centers on the fundamental electrical and dielectric characteristics of MS architectures or SBD, along with the morphology of the barrier established at the M/S junction. In order to gather precise data, it is necessary to conduct I-V, C-V, and G/ω-V analyses on these structures across a broad spectrum of frequencies, temperatures, and voltages. The behavior of MPS structures, typically synthesized at the interface of metals and semiconductors, is akin to that of metal MIS/MOS structures. The electrical and dielectric properties of the MS structure are not ideal, as they only display conduction and polarization mechanisms within a limited range of frequency, voltage, or temperature. The objective of the investigation was to fabricate C-V structures using MPS structures and conduct G/ω-V measurements across a broad range of voltage and frequency to gain comprehensive insights into their dielectric characteristics. The electronics industry is observing a shift towards MPS structures as a replacement for MIS-type structures. This is primarily due to the superior mechanical strength, stability, and low temperature machinability of MPS structures, which are also cost-effective. The proposed study aims to investigate the fundamental electrical power of these structures. However, a comprehensive analysis of their conduction and polarization mechanisms, which are subject to frequency and voltage variations, is still pending across a broad spectrum of frequencies and voltages. This investigation analyzed the electrical characteristics of MPS structures containing interfacial layers across a broad range of frequencies and voltages. Precise quantification of I-V, C-V, and G/ω-V properties is employed to gather comprehensive insights into the formation of obstacles at the interface. Precise measurements of bias-

dependent current-voltage characteristics, barrier height ($\Phi_B$), ideality factor, series resistance, and short circuit current are commonly employed in materials engineering. Future work following the findings of this study will primarily focus on a deeper investigation of the electrical properties of MPS structures as they depend on frequency and voltage. Building on the insights gained, advanced characterization techniques will be employed to scrutinize the conduction and polarization mechanisms of MPS structures across an even broader range of frequencies and voltages. The methodology developed here will be expanded to explore the applicability of different material combinations and to enhance our understanding of the fabrication process using ultrasonic technology. Practical applications of MPS structures in real-world settings will be a significant focus, aiming to harness their demonstrated advantages such as mechanical strength, stability, easy and low-temperature machinability, and cost-effectiveness. Concurrently, comparative studies with MIS-type structures will be conducted to provide a comprehensive view of the electronics industry's evolving landscape. This multifaceted approach promises to usher in substantial advancements in the field of semiconductor technology.

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