INVESTIGATION OF NOVEL MEMRISTOR-MEMTRANSISTOR DEVICES FOR POTENTIAL NEUROMORPHIC COMPUTING APPLICATIONS VIA ALTERNATIVE SYNTHESIS ROUTES

Master's Thesis

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FINAL APPROVAL FOR THESIS

This thesis titled INVESTIGATION OF NOVEL MEMRISTOR-MEMTRANSISTOR DEVICES FOR POTENTIAL NEUROMORPHIC COMPUTING APPLICATIONS VIA ALTERNATIVE SYNTHESIS ROUTES has been prepared and submitted by Mustafa Yiğit ESEN in partial fulfillment of the requirements in "Eskişehir Technical University Directive on Graduate Education and Examination" for the Degree of Master's in Electrical-Electronics Engineering Department has been examined and approved on 21/07/2025.

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ABSTRACT

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Department of Electrical-Electronics Engineering

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Eskişehir Technical University, Institute of Graduate Programs, July 2025

Supervisor: Prof. Dr. Feridun AY

As the need for faster and more efficient data processing grows particularly with the rise of artificial intelligence (AI) applications conventional Von Neumann architectures face fundamental limitations due to the separation of memory and processing units. Memristors and memtransistors offer a promising alternative by enabling unified memory-computation architectures and emulating key features of biological synapses, making them strong candidates for neuromorphic computing. In this context, two-dimensional (2D) materials, such as transition metal dichalcogenides (TMDs), stand out for their atomic thickness, electrostatic tunability, and defect-engineering flexibility, all of which are critical for implementing low-power, high-density, and scalable memristive devices. However, challenges remain in achieving stable and reproducible switching behavior, largely due to defect-driven mechanisms such as ion migration, phase transitions, and filamentary conduction.

This thesis explores two experimental strategies to address these challenges using alternative fabrication methods. First, memtransistor structures based on monolayer MoS_2 were fabricated via chemical vapor deposition (CVD), and the effect of channel length on synaptic behavior and electrical performance was systematically investigated. The findings highlight how device geometry influences neuromorphic functionalities. Second, a novel fabrication route was developed for titanium-based memristors using plasma-enhanced atomic layer deposition (PEALD). While full MXene formation is still under study, the resulting crystalline TiC phase was successfully integrated into a vertical memristor structure, exhibiting reliable resistive switching and short-term synaptic plasticity.

Together, these results demonstrate the potential of 2D-material-based memristive systems for neuromorphic computing and provide insight into tunable, scalable, and CMOS-compatible fabrication routes.

Keywords: Memristor, Memtransistor, Neuromorphic computing, Plasma-enhanced atomic layer deposition, Titanium carbide.

ÖZET

ALTERNATİF SENTEZ YÖNTEMLERİYLE POTANSİYEL NÖROMORFİK HESAPLAMA UYGULAMALARI İÇİN YENİ NESİL MEMRİSTÖR-MEMTRANSİSTÖR CİHAZLARININ ARAŞTIRILMASI

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Yapay zekâ (AI) uygulamalarının yükselişiyle birlikte daha hızlı ve verimli veri işleme ihtiyacı giderek artarken, geleneksel Von Neumann mimarileri, bellek ve işlem birimlerinin ayrılığı nedeniyle temel sınırlamalarla karşı karşıya kalmaktadır. Memristörler ve memtransistörler, bellek ve hesaplama işlevlerini birleştiren mimarileri mümkün kılmaları ve biyolojik sinapsların temel özelliklerini taklit edebilmeleri sayesinde, nöromorfik hesaplama için umut verici bir alternatif sunmaktadır. Bu bağlamda, geçiş metali dikalkojenitleri (TMD'ler) gibi iki boyutlu (2D) malzemeler, atomik incelikleri, elektrostatik olarak ayarlanabilir yapıları ve kusur mühendisliği açısından sundukları esneklik sayesinde, düşük güç tüketimli, yüksek yoğunluklu ve ölçeklenebilir memristif aygıtların gerçekleştirilmesinde öne çıkmaktadır. Ancak, iyon göçü, faz geçişleri ve filaman oluşumu gibi kusur kaynaklı mekanizmalar nedeniyle kararlı ve tekrarlanabilir anahtarlama davranışının elde edilmesi hâlen önemli bir zorluk teşkil etmektedir.

Bu tezde, söz konusu zorlukların üstesinden gelmek amacıyla alternatif üretim yöntemlerine dayalı iki deneysel strateji araştırılmıştır. İlk olarak, kimyasal buhar biriktirme (CVD) yöntemiyle monolayer MoS_2 tabanlı memtransistör üretilmiş ve kanal uzunluğunun sinaptik davranış ve elektriksel performans üzerindeki etkisi sistematik olarak incelenmiştir. Elde edilen bulgular, aygıt geometrisinin nöromorfik işlevsellik üzerindeki belirleyici rolünü ortaya koymuştur. İkinci olarak, plazma destekli atomik katman biriktirme (PEALD) yöntemi kullanılarak titanyum tabanlı memristörler için yeni bir üretim yöntemi geliştirilmiştir. Tam MXene oluşumu hâlen araştırma aşamasında olmakla birlikte, ortaya çıkan kristal TiC fazı, dikey bir memristör yapısına başarıyla entegre edilmiş ve direnç değişimi ile kısa süreli sinaptik plastisite sergilemiştir.

Bu sonuçlar birlikte ele alındığında, 2D malzeme tabanlı memristif sistemlerin nöromorfik hesaplama için taşıdığı potansiyeli gözler önüne sermekte ve ayarlanabilir, CMOS uyumlu üretim yaklaşımlarına dair önemli içgörüler sunmaktadır.

Anahtar Sözcükler: Memristör, Memtransistör, Nöromorfik hesaplama, Plazma destekli atomik katman biriktirme, Titanyum karbür.

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Mustafa Yiğit ESEN

21/07/2025

STATEMENT OF COMPLIANCE WITH ETHICAL PRINCIPLES AND RULES

I hereby truthfully declare that this thesis is an original work prepared by me; that I have behaved in accordance with the scientific ethical principles and rules throughout the stages of preparation, data collection, analysis and presentation of my work; that I have cited the sources of all the data and information that could be obtained within the scope of this study, and included these sources in the references section; and that this study has been scanned for plagiarism with "scientific plagiarism detection program" used by Eskişehir Technical University, and that "it does not have any plagiarism" whatsoever. I also declare that, if a case contrary to my declaration is detected in my work at any time, I hereby express my consent to all the ethical and legal consequences that are involved.

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CONTENTS

Page

HEADER PAGE ..... **I**

FINAL APPROVAL FOR THESIS ..... **II**

SUPERVISOR APPROVAL ..... **III**

ABSTRACT ..... **IV**

ÖZET ..... **V**

ACKNOWLEDGEMENTS ..... **VI**

STATEMENT OF COMPLIANCE WITH ETHICAL PRINCIPLES AND RULES ..... **VII**

CONTENTS ..... **VIII**

LIST OF FIGURES ..... **XI**

GLOSSARY OF SYMBOLS AND ABBREVIATIONS ..... **XVI**

1. INTRODUCTION **1**

1.1. Memristor Missing Circuit Element **1**

1.2. Historical Perspective of Memristor and Memtransistor **2**

2. THEORETICAL BACKGROUND **5**

2.1. Three Fingerprints of Memristor **5**

2.1.1. Pinched hysteresis loop **5**

2.1.2. Hysteresis lobe area decreases with frequency **6**

2.1.3. Pinched hysteresis hoop shrinks to a single-valued function at infinite frequency **7**

2.2. Memristor Structures and Working Mechanisms **7**

2.2.1. Lateral memristors **8**

2.2.1.1. Defect-mediated lateral memristors ***9***

2.2.1.2. Phase-transition-mediated lateral memristors ***10***

2.2.2. Vertical memristors **11**

2.2.2.1. Phase-transition-mediated vertical memristors ***11***

2.2.2.2. Vacancy-formation-induced vertical memristors ***12***

2.2.2.3. Filament-formation-induced vertical memristors 13
2.2.2.4. Schottky barrier modulated vertical memristors 14
2.2.3. Heterojunction memristors 15
2.2.3.1. Filament formation mediated heterojunction structure 15
2.2.3.2. Vacancy migration mediated heterojunction structure 17
2.3. Memtransistor 17
2.3.1. Memtransistor classification and working mechanism 18
2.3.1.1. Ion vacancy 19
2.3.1.2. Filament formation 21
2.3.1.3. Ferroelectric 22
2.3.1.4. Charge trapping 24
2.3.1.5. Heterojunction 25
2.4. Memtransistor- Memristor Applications 27
2.4.1. Memristors as memory devices 27
2.4.2. Artificial intelligence 30
2.4.3. Synaptic electronics and neuromorphic systems 33
2.4.4. Optic, photonic devices 35
2.5. TMDs – 2D Material 38
2.6. Emulating Biological Synaptic Plasticity with Memristors 39
2.6.1. Short-term and long-term plasticity 41
2.6.2. Spike-timing-dependent plasticity 42
3. EXPERIMANTAL TECHNIQUES 45
3.1. Fabrication of Memtransistors 45
3.1.1. CVD growth of MoS_2 45
3.1.2. Optic litography 46
3.2. Characterization Techniques of MoS_2 Memtransistors 49
3.2.1. Raman, photoluminescence spectrum and AFM 49
3.2.2. Electrical characterization 51
3.2.3. Synaptic emulation 55
3.2.4. Effects of channel length on device performance 56
3.3. Fabrication of Titanium Carbide Memristors 57
3.3.1. Atomic layer deposition 57

3.3.2. PEALD growth of titanium carbide 59
3.3.3. Thermal evaporator: building top electrodes 64
3.4. Characterization of Titanium Carbide Memristors 65
3.4.1. SEM, XRD, Raman 65
3.4.2. Electrical characterization 69
REFERENCES 73
CURRICULUM VITAE

LIST OF FIGURES

Page

Figure 2.1. Pinched hysteresis loop (I–V characteristic) of a memristor..... 5

Figure 2.2. Frequency-dependent pinched hysteresis loop of potassium ion-channel memristor [15] 6

Figure 2.3. Summary of the memristor devices based on 2D materials including diverse types of materials (top row), three different types of memristor devices composed of lateral-, vertical-, and heterojunction-structures (middle row), and schematic illustration of general mechanisms in LRS and HRS (bottom row). [19] 8

Figure 2.4. a), EFM phase image of a MoS_2 memtransistor at V_D=5 V, V_S=0 V and Vtip=0 V (Vtip, voltage of the EFM tip) in the forward-biased HRS. D, drain; S, source. b), Line profiles of EFM phase along the red dashed line in a for EFM images taken in the forward-biased HRS, forward-biased LRS, reverse-biased HRS and reverse-biased LRS, respectively. c) Schematic of a MoS_2 memtransistor device built on 300-nm-thick thermal SiO_2 on doped Si [20] 10

Figure 2.5. Chemical Memristor devices operated by phase transition. a) Schematic image of the 1T-TaS_2 device and crystal structures depending on temperature. b) Phase diagram of 1T-TaS_2 depending on the temperature and the thickness. c) Resistance versus voltage and cycle number curves of memristive switching behavior measured at 90 K. [23] 11

Figure 2.6. I−V characteristic of MoS_2 nanosheets based switch. (a) Schematic structure of Ag/MoS_2/Ag switch. (b) Typical I−V characteristic of Ag/MoS_2/Ag switch at room temperature. (c) Typical I−V characteristic of Ag/MoS_2/Ag switch in the logarithmic scale at room temperature. (d) Typical I−V characteristic of Ag/MoS_2/Ag switch at the 1st (red), 500th (green), and 1000th (blue) cycle at room temperature [25]. 12

Figure 2.7. Vertical memristors induced by atomic-vacancy formation and migration. a) Schematic of Pd/WS_2/Pt memristor. b) Typical I–V curve operated at sub-1 V range. The inset shows the electroforming process. c) TEM image of WS_2 films in LRS induced by vacancy migration [26]. 13

Figure 2.8. Vertical memristors based on formation of metallic filaments. a) Schematic of Cu/MoS_2/Au memristor. b) Typical switching curve showing HRS and LRS transition. c) Schematics depicting filament formation and deformation causing resistance changes [28]. 14

Figure 2.9. Monolayer-MoS_2-based vertical memristors mediated by transport conversion from SE and DT. a) Schematic of the device with three-

atom thick MoS_2 channel. b) Cross-sectional TEM images of Au/MoS_2/Au structure. c) I–V curve indicating bipolar switching.[30]..... 15

Figure 2.10. Vertical memristors based on heterojunction-structures mediated by filament formation and charge trapping processes. a) Schematic of the Ag/ZrO_2/WS_2/Pt device. b) Typical I–V switching curve operated at the sub-0.6 V range. c) Schematic depicting the SET and RESET process induced by metallic filament formation. d) STDP characteristics with 0.8 V pulse amplitude and 100 ns pulse width [32]. 16

Figure 2.11. Memtransistor schematic representation [36] 18

Figure 2.12. Bipolar reversible and nonvolatile switching of nanoscale TiO_{2-2x} devices. a, An AFM image of 1 17 nano-crosspoint devices with 50 nm half-pitch. Pt nanowires fabricated by nanoimprint lithography sandwich a 50-nm-thick TiO_2 insulating thin film. b, The initial I2V curve of the device in its virgin (preswitching) state exhibits a rectifying characteristic. Inset: The 50-nm TiO_2 has two constituent layers; a near-stoichiometric TiO_2 layer rests on top of an oxygendeficient TiO_{2-2x} layer..... 20

Figure 2.13. Forming operation in the memtransistor device. a) Measured I_D–V_{DS} characteristic of the device during the forming process. Forming is evi-denced by the steep increase of current at V_{DS} = 1.8 V. A current limitation to IC = 0.8 μA was adopted to prevent destructive breakdown. b) Schematicof the MoS_2 memtransistor switching mechanism. For small V_{DS} the metallic electrodes are physically separated and the current is confined in thesemiconductor channel region. c) After forming or the set transition, a CF is formed between the two electrodes, thus enhancing conductance. The CF is then spontaneously dissolved as V_{DS} is decreased below a holding voltage. 22

Figure 2.14. The interlocked out-of-plane and in-plane ferroelectricity in multilayer 2H α-In_2Se_3. a) The α-In_2Se_3 crystal structures depicting the interlocked polarization mechanism in the OOP and IP orientations. The yellow and blue balls represent Se and In atoms, respectively. After large bias poling that exceeds the coercive voltage, the central Se atoms, which are the origin of the interlocked spontaneous polarization, move toward the bottomright direction, simultaneously reversing the OOP and IP dipoles (State 1 → State 2). b) Piezoresponse hysteresis loops (three cycles) for a multilayer α-In_2Se_3 crystal. c) The OOP and IP phase images after forward (+8 V) and reverse (−8 V) DC bias written in the outer square and two inner rectangles. Scale bar: 500 nm [46]. 23

Figure 2.15. Schematic diagrams of the working mechanism in terms of charge trapping/detrapping (i: initial state V_{DS} = 0, ii: under V_{DS} > 0, iii: under V_{DS} 0, iii: under V_{DS}) 24

Figure 2.16. Circuit and schematic representation of diagrams of the synaptic barristor consisting of a vertically integrated WO_{3-x} memristor and WSe_2/graphene barristor. b) Schematic illustration of the monolithic oxidation process by UV-ozone treatment. This process converts the topmost WSe_2 layer to amorphous WO_3–x. c. 25

Figure 2.17. Characterizations of vdW M-FE-S heterojunctions. a) Schematic illustration of M-FE-S memristor. b) A typical pinched I–V curve obtainedin a vdW M-FE-S heterojunction, showing characteristic memristive behavior [57] 26

Figure 2.18. The first I-V cycle of rGO/nFE-MXene/rGO, rGO/FE-MXene/rGO and rGO/FE-MXene/nFE-MXene/rGO memory devices illustrating a comparison of device switching behaviors (b) Conduction mechanism for SET and RESET states in rGO/FE-MXene/nFE-MXene/rGO trilayer device [58] 28

Figure 2.19. a) Representative schematic I–V characteristics of the four types of two-terminal memristors. b) Schematic for a metal-TMDC-metal lateralstructure, in which two metallic electrodes are connected to the TMDC layer (functional material). Two Schottky contacts are formed at the metal-TMDCcontact and TMDC-metal contact. 29

Figure 2.20. One to one correspondence of the nociceptor system in the human body and an artificial nociceptor circuit consisting of a diffusive memristor (threshold switch). a When a noxious stimulus is received from a free nerve ending, the nociceptor compares the amplitude of the signal with a threshold value and decides whether an action potential should be generated and sent to the brain via the spinal cord (central nervous system). b An electrical pulse applied on the device emulates the external stimulus. When the pulse amplitude is higher than the threshold voltage of the diffusive memristor, the device is turned ON, and current pulses are generated 31

Figure 2.21. Chemical Brain dynamics and spatiotemporal information processing based on in-sensor RC. (A) Schematic of the cognitive task implemented on a biological RC sys-tem. Language learning is carried out by the visual cortex, which can perform time-series computations for sequential inputs. (B) Transport behaviors reflecting thecharge trap/detrap dynamics in SnS with an optical microscopy image of the device (inset with a scale bar of 2 m). The first and final cycles are green and red colors,respectively, and the electrical (C) and optical (D) pulse switching characteristics. Electrical pulses (4.5 V and 20 ms) with an interval of 10 ms were used in (C). Opticalpulses with a wavelength of 725 nm, a power of 43 mW, and a width of 3 s were used in (D). The read voltage was 0.5 V. (E) Normalized photocurrent (PC) under continuousoptical stimuli with 455, 638, 725, and 811 nm. (F) Acceptor states (Ea) are occupied by electrons in p-type SnS with the Fermi level (Ef) close to the valence band inconventional transport. (G) With a Vd exceeding a threshold voltage (Vth), the

electrons trapped at acceptor states are recombined with holes, decreasing the channelcurrent. (H) Under light illumination, electrons are excited and trapped in the donor states created by S atomic vacancies, producing more holes in the valence band andleading to greater conductivity (photogating effect [73]). 32

Figure 2.22. a) Schematic structure of the Al/Ti_3C_2Tx/Pt device and Ti_3C_2Tx atomic structure (Tx stands for surface termination). b) Typical I–V curves of the device. c) Illustration of synaptic plasticity adjustment between axons and dendrites. d,f) Measured and simulated device potentiation (1st to 20th pulse) and depression (21st to 40th pulse) curves under the application of successive AC pulses. Positive bidirectional pulse train with different parameters is used to excite or inhibit synapses. g–i) Initial data of continuous pulse regulation with different pulse durations. 34

Figure 2.23. a) Schematic of human visual system and human brain for obtaining picture, pattern recognition and information storage. b) Schematic diagram of the optoelectronic memristors array, single optoelectronic cell and artificial sensing-memory-computing system [89]..... 37

Figure 3.1. Schematics of the growth zone of the CVD system. 46

Figure 3.2. Schematical representation of the fabricated MoS_2 based device 47

Figure 3.3. Optical microscopy image of 7 μm channel length. 48

Figure 3.4. (a): AFM image of monolayer MoS_2 flake. (b):The thickness profile of MoS_2 49

Figure 3.5. PL spectrum with Gaussian fit of MoS_2 50

Figure 3.6. Raman spectrum of mono-layer MoS_2 51

Figure 3.7. Chemical Memtransistor I_{DS}-V_{DS} characteristics measured under ambient conditions. All plots were acquired with a drain-to-source voltage range of 5 V–5 V, V to 50 V, and a channel width of 10 μ m. Plots (a) and (b) correspond to L CH =15 μ BG set m, with (a) presented on a linear scale and (b) on a semi-logarithmic scale. Plots (c) and (d) correspond to L CH = 7 μ m, with (c) presented on a linear scale and (d) on a semi-logarithmic scale. of paracetamol. 52

Figure 3.8. I_{DS}-V_{DS} characteristics under ambient and dark conditions with a channel length of L_{CH}=7 μ m. All graphs are obtained under a drain-to-source voltage range 5 V–5 V, with (a) at V_{BG} = 0 V and (b) at V_{BG} = 50 V, both plotted on a linear scale. 53

Figure 3.9. The impact of different gate voltages (V_{BG}) on memtransistors with a channel length of 7 μm. Specifically, (a) V_{BG} = 0 V, (b) V_{BG} = 25 V, and (c) V_{BG} = 50 V. Similarly, subplots (d) and (e) compare the I_{DS}-

V_{DS} curves for memtransistors with the same channel lengths (15 gate voltages at ambient conditions.) 54

Figure 3.10. I_{DS} current characteristics obtained by consecutive pulses to simulating presynaptic pulse stimuli: (a) + 5 V, (b) – 5 V of amplitudes. 56

Figure 3.11. Schematic of ALD process flow [125] 58

Figure 3.12. Schematic of PEALD process flow to Titanium Carbide thin film growth 61

Figure 3.13. Schematic representation of the effect of changing the exposure time to methane plasma on the amount of carbon deposition. 62

Figure 3.14. Optical images of annealing conditions on copper substrates 63

Figure 3.15. Vertical structure titanium carbide memristor a) schematic, b) optical image c) Probe station 64

Figure 3.16. SEM images of Titanium Carbide growth experiments exposed to CH_4 plasma for 2 seconds and different annealing conditions a) H_2 700 °C, b) Ar 700 °C, c) Ar 1000 °C. 65

Figure 3.17. XRD measurements of post-annealing experiments (CH_4 plasma for 2 sec.) 66

Figure 3.18. Raman spectra of Titanium Carbide growth experiments exposed to CH_4 plasma for 2 seconds and different annealing conditions. 67

Figure 3.19. Effect of changing the CH_4 plasma exposure time on the same substrates and the same annealing conditions. 67

Figure 3.20. a) Pinched hysteresis loop observed when a sinusoidal wave is applied to the memristor. b) DC characterization I-V graph. c) When a current above 25 V is applied, the memristor enters a short-circuit state and enters a very low resistance state. d) Short-term depression and potentiation behavior with successive pulses applied to the memristor. 69

GLOSSARY OF SYMBOLS AND ABBREVIATIONS

1T1R	:	One Transistor – One Resistor
2DLMs	:	Two-dimensional layered materials
AFM	:	Atomic Force Microscopy
ALE	:	Atomic Layer Epitaxy
ALD	:	Atomic Layer Deposition
ANN	:	Artificial Neural Networks
BE / TE	:	Bottom Electrode / Top Electrode
CDW	:	Charge Density Wave
CNN	:	Convolutional Neural Network
DT	:	Direct Tunneling
FETs	:	Field Effect Transistors
FG	:	Floating Gate
GB	:	Grain Boundary
HRS / LRS	:	High Resistance State / Low Resistance State
IMC	:	In-Memory Computing
LTD / LTP	:	Long-Term Depression/ Long-Term Potentiation
NVM	:	Non-Volatile Memory
PEALD	:	Plasma-Enhanced Atomic Layer Deposition
RRAM	:	Resistive Random Access Memory
SE	:	Schottky Emission
SEM	:	Scanning Electron Microscopy
SNNs	:	Spiking Neural Networks
STDP	:	Spike-Timing Dependent Plasticity
STD / STP	:	Short-Term Depression / Short-Term Potentiation
TMD/TMDCs	:	Transition Metal Dichalcogenides
TMO	:	Transition Metal Oxide

1. INTRODUCTION

1.1. Memristor Missing Circuit Element

The concept of the memristor, short for memory resistor, was first proposed by Leon Chua in 1971[1]. The proposition came about as he identified a theoretical shortfall in circuit theory. In the realm of electrical engineering, circuits are essentially based on four main variables: current (i), voltage (v), charge (q), and magnetic flux (φ). These variables are related to each other through passive circuit elements.

Electric charge flowing in a conductor, known as current (i), is measured in amperes (A).

Voltage (v): The potential difference between two points, responsible for driving current, measured in volts (V).

Charge (q): A property of matter carried by particles like electrons and protons, measured in coulombs (C).

Magnetic flux (φ) is the overall magnetic field which passes through an assigned surface, measured in webers (Wb).

Under the context of conventional circuit theory, the resistor (R), capacitor (C), and inductor (L) form relationships between the three elements:

Voltage and current define a resistor: $v = R \times i$

Charge and voltage define a capacitor: $q = C \times v$

Current and flux define an inductor: $\varphi = L \times i$

However, the single critical piece which provided distinct correlation between charge (q) and magnetic flux (φ) was missing. This lack was addressed in his work entitled "Missing Circuit Element," in which Chua provided the mathematical theory for the new passive device intended to relate the two parameters. The device was named the "memristor" from the blending of the word "memory" with "resistor" as it describes its capability to retain its previous resistance value in accordance with the current or voltage history [1]. One of the basic properties of the memristor is non-volatility. When voltage or current is applied, the device resistance is altered. When the input is stopped, the resistance stays in its current state, actually exhibiting a "memory" effect. This makes it suitable for use in memory storage and neuromorphic computing applications.

Despite the varied forms and terminologies used to describe variable resistors, Chua suggested that a genuine memristor should exhibit one defining characteristic alone: the

existence of a pinched hysteresis loop in the I-V characteristic curve under sinusoidal excitation as an input voltage. The characteristic curve should display zero current at the zero point of the voltage, crossing the origin, representing the absence of phase shift characteristic of capacitors or inductors. This is the distinguishing effect inherent in the device and is considered to be the basic defining characteristic of the memristor [2].

Chua formulated the basic concepts of incremental memristance (M), or the rate of change of voltage with respect to charge, and its reciprocal, incremental memductance (W). He described this relation mathematically as

$$M(q) = d\varphi/dq$$

Later on, Chua's original model received moderate attention because a number of resistive switching devices were developed that could not be sufficiently explained by his early theory. In order to clarify the intricacies presented by these new devices, Chua and Kang introduced a more generalized model called memristive systems that included a broader range of behaviors and mechanisms. This development allowed many previously misunderstood devices to be correctly classified and led to increased activity and interest in memristor research [2].

This extension of the definition enabled the development of the memristor, attracting more researchers and promoting accelerated technical progress. It also helped to accelerate the efforts to apply memristors to real-world applications, particularly in the fields of memory and neuromorphic computing systems [3].

1.2. Historical Perspective of Memristor and Memtransistor

Leon Chua originally conceived the idea of the memristor in 1971 [1,3]. He argued that the device should be accepted as the fourth basic circuit element, in addition to the resistor, capacitor, and inductor. Unlike the conventional elements which form relationships between pairs of parameters like voltage, current, charge, and magnetic flux, the memristor is defined according to its particular relationship between charge and magnetic flux. Chua explained that the device has the memory of its past resistance in terms of the voltage or current it has already experienced, which would be useful in applications in memory storage [4] or in attempts to simulate human thinking in its own electronic or microcircuits [5].

During the long time after the development of this theory, researchers created devices with resistance switching properties but were largely unaware of their potential

assignment as memristors, partly as the idea had its dissemination severely constrained. With the technology in CMOS reaching limitations[6] inherent in it, an increasing need arose for new memory technologies.

In the year 1995, a group of researchers at HP Labs led by R. Stanley Williams began working to examine an innovative nanoscale device [7]. They were guided in their research by an unorthodox computing framework named Teramac, which had the crossbar structure. They created a device with two platinum contacts with a molecular thickness in between them. These devices were found to have fast state-switching properties with their resistance being dependent on the time the device is exposed to the voltage. Although the underlying reason behind the observed phenomenon at the time was unclear.

Later, a researcher named Greg Snider came across Chua's previous work and noticed that the current–voltage characteristic curve of their device was similar to Chua's "pinched hysteresis loop," which is a memristor identifier. This discovery allowed for an easier understanding that their device was indeed a real memristor.

Further experiments showed that switching was not caused by the molecule layer but by changes in a thin titanium dioxide (TiO_2) film. When voltage was applied, oxygen vacancies moved inside the material. A positive voltage pushed these vacancies to a region, making it more conductive (SET state). A negative voltage moved them back, making the material less conductive (RESET state). This behavior helped them create a mathematical model of memristor function and confirmed that memristors were not only theoretical—they could be built and tested in the lab [7].

After this breakthrough, researchers focused on optimizing memristors for use in non-volatile memory technologies like resistive random-access memory (RRAM)[8–10] and neuromorphic computing [11,12]. They tested diverse materials, including metal oxides and organic films, with the goal of creating faster, more reliable, and easier-to-produce devices. Memristors became key devices for mimicking human cognitive processes in systems since they have the capacity to store and process information at the same time, much like biological synapses.

Neuromorphic computing is a field that started in the 1980s, aiming to build systems that copy the way the brain works. Because memristors can act like synapses, they became a key technology in this area. By the 2010s, memristors were widely used in artificial neural networks for machine learning and pattern recognition[11,12].

In 2018, a research team introduced a novel device called the memtransistor, which combines the functionalities of a transistor and a memristor, and features three terminals instead of the conventional two [13]. Having an extra terminal allows for greater control and enables the device to perform more complex synaptic tasks, including spike-timing-dependent plasticity (STDP), a function essential to learning in neural networks. Memtransistors are considered a breakthrough in neuromorphic computing because they can carry out both memory storage and signal processing tasks in a single device. Having these two functions in one helps achieve energy efficiency and space saving, making them beneficial for advanced artificial intelligence systems. They are now being integrated into experimental neural circuits to enable learning and adaptive processes, similar to how biological synapses operate.

2. THEORETICAL BACKGROUND

2.1. Three Fingerprints of Memristor

2.1.1. Pinched hysteresis loop

A pinched hysteresis loop is identified as an intrinsic property of a memristor. The property appears in the voltage-current (V–I) plane upon periodic excitation of the device through a sine wave. The distinguishing feature of such a loop is that it returns to a single point of origin regardless of driving signal amplitude or driving signal frequency. This phenomenon describes the concurrent movement of current and voltage towards a common coordinate of zero [14].

Notably, the loop should persistently proceed to its original location on the V–I plane after every cycle, thus maintaining its pinched shape. Irrespective of fluctuations or differences in speed or the amplitude of the applied signal, the loop automatically crosses through the origin. This indicates that under all input conditions, the memristor has a stable response and returns a closed loop that defines its memory-like behavior. The hysteresis loop is a phenomenon brought about by interactions among a memristor's state variables and their evolution over time. The memristor basically has the ability to store information based on its past electrical inputs and then drive its current operating behavior, thus leading to the typical hysteresis loop.

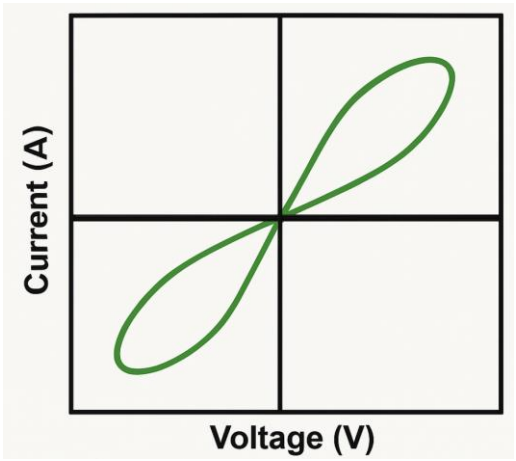

Figure 2.1. *Pinched hysteresis loop (I–V characteristic) of a memristor*

The pinched hysteresis loop has been considered to be the defining trait of memristive behavior. A device, which can produce a similar loop only at definite frequencies or amplitudes, but cannot sustain such behavior under all operating conditions, would not be an ideal memristor. Additionally, while specific devices might

produce such a loop under limited conditions, their failure to produce such behavior when exposed to different inputs confirms that such devices are not meeting the memristor criteria.

2.1.2. Hysteresis lobe area decreases with frequency

The second key property of a memristor is that an increase in the frequency of the input signal leads to a sustained decrease of the pinched hysteresis loop area. At high frequencies, the behavior of the memristor becomes ever more like that of a linear resistor, making it difficult to observe the hysteresis effect. At frequencies above a critical value, a significant shrinkage of the loop width takes place.

This happens when the internal state of the memristor, i.e., its memory, does not respond properly to high-frequency signals. Since memristance, i.e., the extent of resistance shown by the memristor, depends on the total charge or flux passing through it over a time interval, faster signals do not provide enough time for such accumulation. Thus, the change in memristance decreases, causing the loop area to shrink [15].

A key property of memristors is hysteresis loop contraction upon an increase of frequency, which differentiates them from memory-related devices like capacitors or inductors, which have different frequency responses.

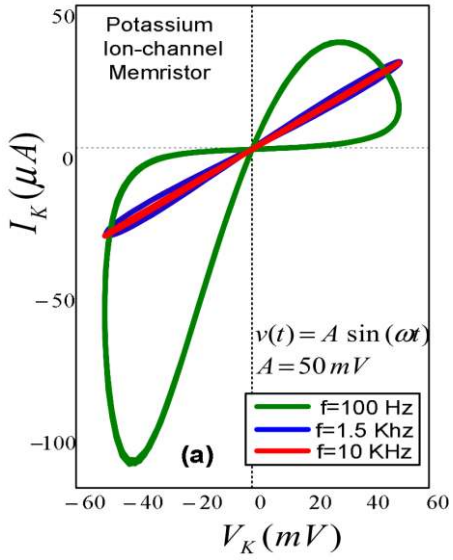

Figure 2.2. *Frequency-dependent pinched hysteresis loop of potassium ion-channel memristor [15]*

2.1.3. Pinched hysteresis hoop shrinks to a single-valued function at infinite frequency

The third fundamental property of memristors is experienced when the input signal frequency tends towards infinity. When there is an increase in frequency, pinched hysteresis loop's HRS and LRS tend to move closer towards each other. This brings about the collapse of such a loop into a single-valued function, which appears to be a linear curve in voltage–current (V–I) space [15].

At very high frequencies, the memristor fails to demonstrate memory behavior and instead displays behavior typical of an ordinary resistor. At such a stage, the slope of the curve indicates the limiting resistance (or conductance) of the memristor. Such an occurrence indicates that the device is unable to hold any preceding states since the rate of refreshing of the state variable stored within it is not sufficient. The memristor behavior, therefore, becomes linear and follows rules stipulated in Ohm's Law.

It is an important property for proper identification of authentic memristors, since various nonlinear devices often show a similar pinched hysteresis loop. However, if these devices are unable to converge to a single-valued function at high frequencies, then they are not full-fledged memristors [16].

The above conditions and parameters are widely referred to in order to define an ideal memristor. However, it has been observed that recent research and prototypes of memristors are not necessarily intended to fulfill all these ideal qualities. This is due to the realization that memristors are used in various fields that each have different operational demands. For instance, when a memristor is intended to act as a transistor substitute, it is important to define a clear differentiation between states of high and low resistance. If, on the other hand, a memristor is intended to model synaptic behavior, an incrementally changing and multi-step resistance would be appropriate. Such variability implies that there could be different conceptual frameworks and expectations about the operational characteristics of memristors depending upon the particular application in question.

2.2. Memristor Structures and Working Mechanisms

As memristors gained popularity, scientists began to test whether different materials could also exhibit memristive behavior. To fully realize the potential of these memristors and integrate them into the chip industry, the structure and architecture of the materials

play a critical role. In particular, 2D material-based memristors have come into focus, and it has been observed that many different materials can show memristive behavior, such as MoS_2, WS_2, h-BN, and others [17,18]. These types of memristors can be classified based on their device geometry and working mechanisms.

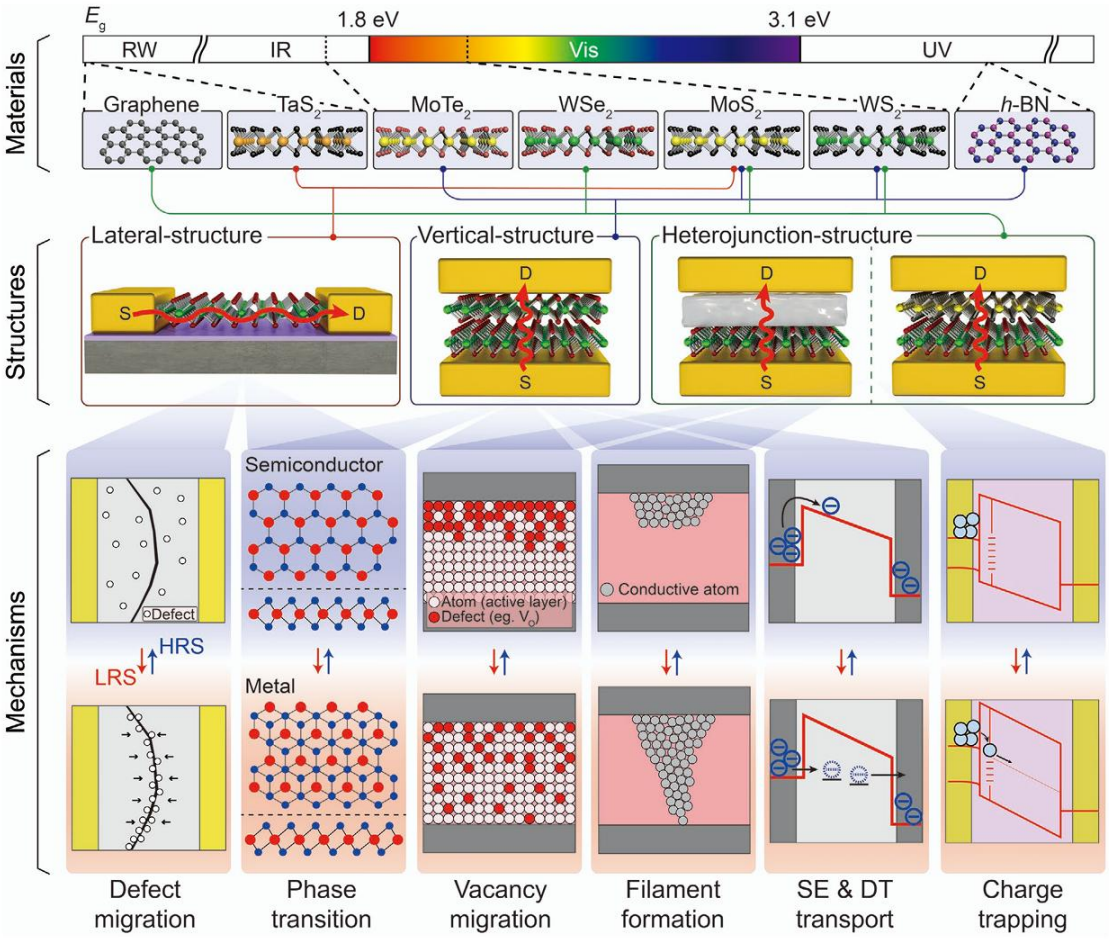

Figure 2.3. *Summary of the memristor devices based on 2D materials including diverse types of materials (top row), three different types of memristor devices composed of lateral-, vertical-, and heterojunction-structures (middle row), and schematic illustration of general mechanisms in LRS and HRS (bottom row). [19]*

2.2.1. Lateral memristors

Lateral memristors follow a structure similar to that of traditional field-effect transistors (FETs) [20]. Lateral memristors usually comprise metal electrodes and transition metal dichalcogenide (TMD) channels placed horizontally on a dielectric substrate. In this configuration, electric current travels in-plane, and memristic properties result from atomic defect motion or localized phase transitions in the TMD channel.

Lateral devices can be converted into memtransistors through electrostatic gate tunability and multi-terminal structures. These lateral architectures are especially useful in controlling the channel length, which helps optimize the output for mimicking neuromorphic behaviors. Using this approach, LTP, LTD, and STDP have been successfully emulated [21].

There are also different opinions regarding the underlying mechanism responsible for the resistance change in memristors fabricated with lateral geometry.

2.2.1.1. Defect-mediated lateral memristors

Memristors controlled by lateral defects are largely synthesized using transition metal dichalcogenides (TMDs), where molybdenum disulfide (MoS_2) is one specific example. In these devices, the reported memristive behaviors are due to defect motion, primarily sulfur vacancy movement along grain boundaries. These defects play an important role in controlling the device conductance in the processes of electroforming, SET, and RESET. Intersecting, bridging, and dividing grain boundary geometries have been reported, each having different switching behaviors.

GB memristors generally have the largest resistance ratios coupled with the minimum SET voltages. In addition, the location of the gate electrode in lateral memristors makes it easier to adjust parameters such as the SET voltage and the resistance state. Such an ability to adjust makes the device more appropriate for complex applications.

A good example is the MoS_2-based memtransistor, a device that combines the properties of both transistors and memristors. Because defects can move around in the device through its lateral structure, the device can simulate biological processes such as LTP and LTD.

A previous example of this investigation is represented in the work by Hersam et al. in 2015. In 2018 [20], the same researchers utilized an analogous experimental setup, terming the device as a memtransistor. They explained that sulfur vacancies have the potential to act as n-type semiconductors and form a Schottky barrier. This barrier raises due to factors derived from vacancy migration, which impacts the resistance across the SET and RESET processes shown in Figure2.4 a) and b) One major feature is that the Schottky barrier provides controllability to the memristive properties. Through the variation in gate voltage, the resistance state and the SET voltage can be controlled,

improving the device's versatility. Such an ability aids in the fabrication of multi-terminal devices and the simulation of synaptic functionality, something that is challenging to achieve using traditional two-terminal memristors.

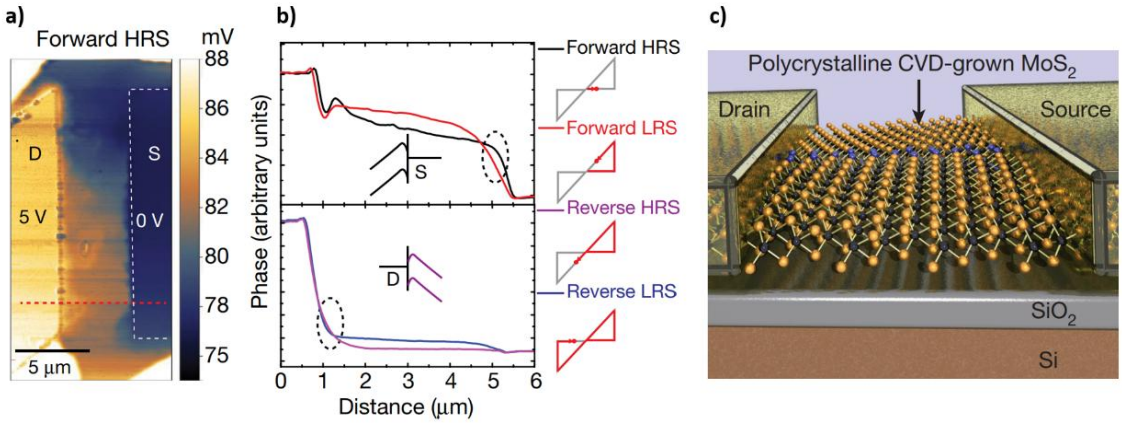

Figure 2.4. *a), EFM phase image of a MoS_2 memtransistor at V_D=5 V, V_S=0 V and Vtip=0 V (Vtip, voltage of the EFM tip) in the forward-biased HRS. D, drain; S, source. b), Line profiles of EFM phase along the red dashed line in a for EFM images taken in the forward-biased HRS, forward-biased LRS, reverse-biased HRS and reverse-biased LRS, respectively. c) Schematic of a MoS_2 memtransistor device built on 300-nm-thick thermal SiO_2 on doped Si [20]*

2.2.1.2. Phase-transition-mediated lateral memristors

Phase-transition-mediated memristors take advantage of phase changes in 2D materials, which depend on the material's thickness [22,23]. One example is TaS_2-based memristors, which use charge density wave (CDW) transitions to change resistance. These transitions happen when voltage creates heat, and this heat causes the material to switch between different crystalline phases for example, from a nearly commensurate CDW (NCCDW) phase to a commensurate CDW (CCDW) phase. This phase change results in memristive switching [23].

Another example is seen in the case of MoS_2, where the semiconducting phase 2H can be converted to the metallic phase 1T' by the application of an electric field. Since these two phases have different electrical properties, this transition therefore changes the resistance in the device.

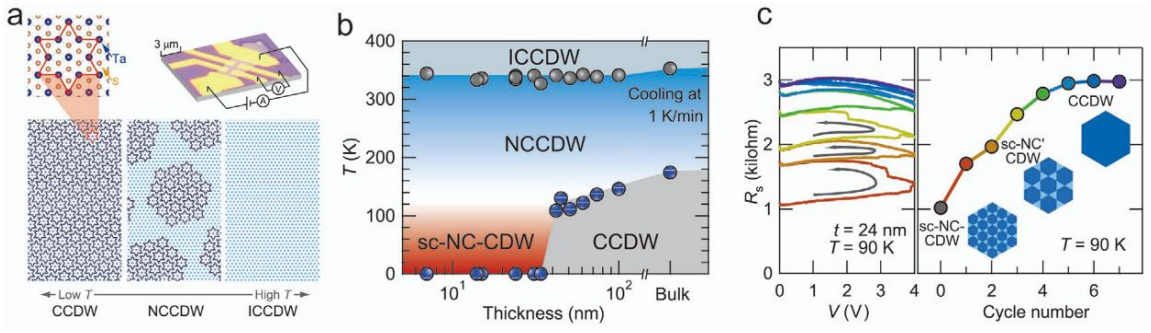

Figure 2.5. *Chemical Memristor devices operated by phase transition. a) Schematic image of the 1T-TaS_2 device and crystal structures depending on temperature. b) Phase diagram of 1T-TaS_2 depending on the temperature and the thickness. c) Resistance versus voltage and cycle number curves of memristive switching behavior measured at 90 K. [23]*

2.2.2. Vertical memristors

In vertically structured memristors, the electrodes are represented as bottom electrode (BE) and top electrode (TE). One of the main advantages of this architecture is that it allows for high-density integration. Unlike lateral architectures, there is no problem of electrodes taking up too much space[24].

This structure can be made using different materials and includes various working mechanisms such as phase-transition, vacancy formation-induced, filament formation, and Schottky barrier modulated memristors. There are examples where the same material is used in both lateral and vertical memristor designs. However, the explanations for their switching mechanisms are often different.

2.2.2.1. Phase-transition-mediated vertical memristors

In the particular type of vertical memristors, the switching mechanism is due to phase transition processes in transition metal dichalcogenides (TMDs) such as MoS_2. Device fabrication is based on the vertical metal–TMD–metal configurations. With the voltage application, the phase is changed from the semiconducting (2H) phase to the metallic (1T) phase. This phase change leads to large decreases in resistance, thus switching the device from the high-resistance state (HRS) to the low-resistance state (LRS).

This phase transition is usually caused by Joule heating — the heat generated by current flow — which gives enough energy to change the atomic structure. In MoS_2, the metallic 1T phase has a distorted lattice and overlapping energy bands, which allow better

conductivity than the 2H phase. As a result, the device shows bipolar switching, and the transition between HRS and LRS can happen at low voltages [25].

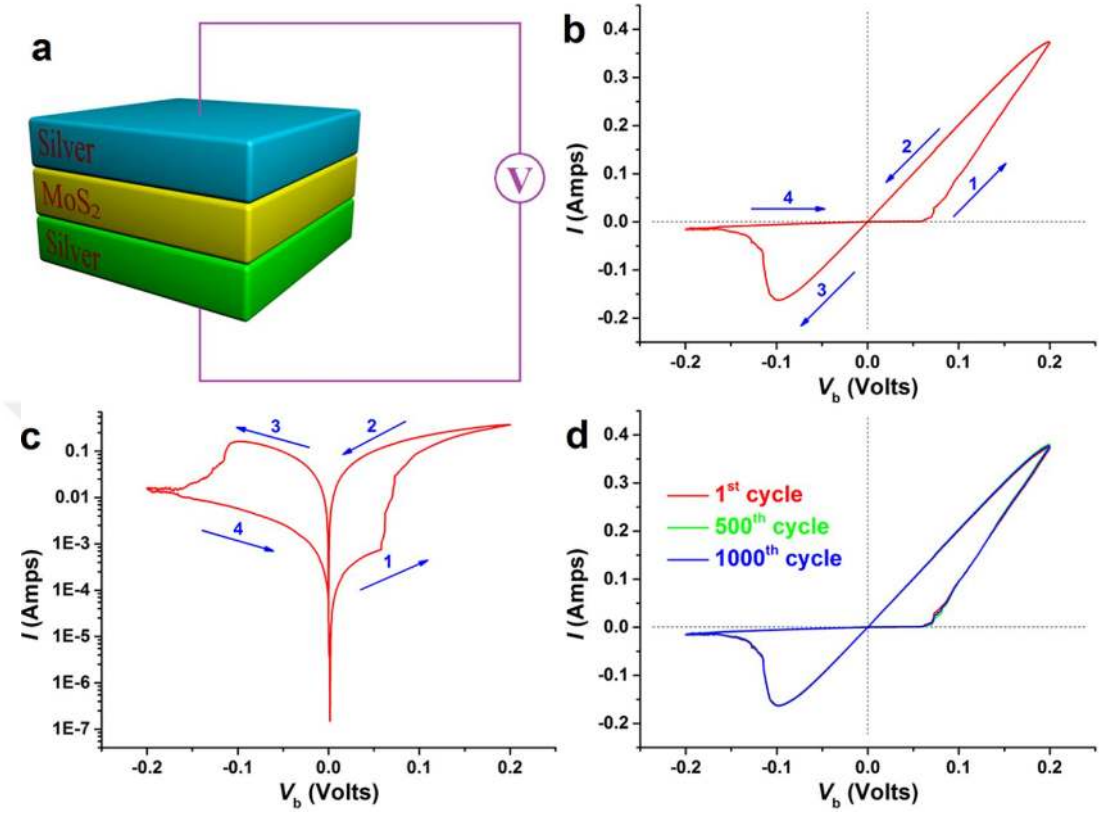

Figure 2.6. *I−V characteristic of MoS_2 nanosheets based switch. (a) Schematic structure of Ag/MoS_2/Ag switch. (b) Typical I−V characteristic of Ag/ MoS_2/Ag switch at room temperature. (c) Typical I−V characteristic of Ag/MoS_2/Ag switch in the logarithmic scale at room temperature. (d) Typical I−V characteristic of Ag/MoS_2/Ag switch at the 1st (red), 500th (green), and 1000th (blue) cycle at room temperature [25].*

2.2.2.2. Vacancy-formation-induced vertical memristors

In these memristors, the switching process depends on the formation and migration of atomic vacancies in the active layer, typically a transition metal dichalcogenide like WS_2. The main defects of importance are vacancies of sulfur, which trap charges and affect the conductivity of the material [26,27].

When voltage is applied, these vacancies move and create conductive paths in the material. This movement changes the resistance, causing a transition from HRS to LRS. For example, in Pd/WS_2/Pt structures, applying voltage increases the number of sulfur vacancies, which improves conduction and switches the device to the low-resistance state. [26]

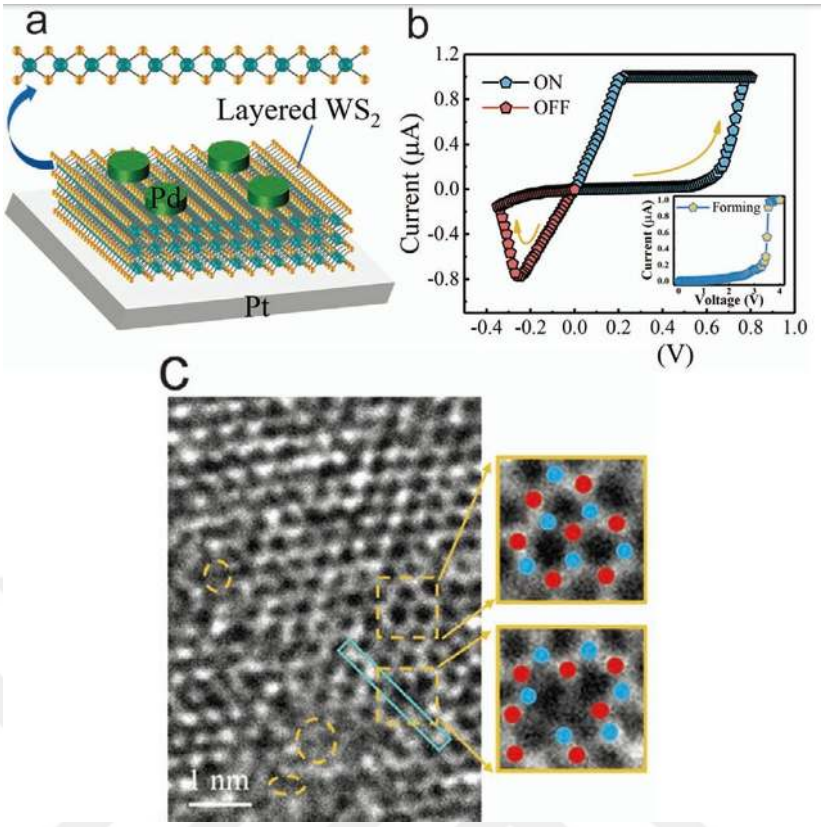

Figure 2.7. *Vertical memristors induced by atomic-vacancy formation and migration. a) Schematic of Pd/WS_2/Pt memristor. b) Typical I–V curve operated at sub-1 V range. The inset shows the electroforming process. c) TEM image of WS_2 films in LRS induced by vacancy migration [26].*

2.2.2.3. Filament-formation-induced vertical memristors

These devices work by forming and breaking down metallic filaments in the active layer[28,29]. With the application of a positive bias, as in the case of a Cu/MoS_2/Au arrangement, metal ions, including copper, move into the layer, forming a conductive filament that connects the two electrodes. A drop in resistance results, causing the device to switch to low-resistance state (LRS) from high-resistance state (HRS).

The size and number of these filaments can be changed by changing voltage and current parameters. During the process of SET, the filament expands and contracts between the electrodes. During the process of RESET, though, the reverse voltage causes the dissolution of the filament, and the device returns to the state of high resistance.[28]

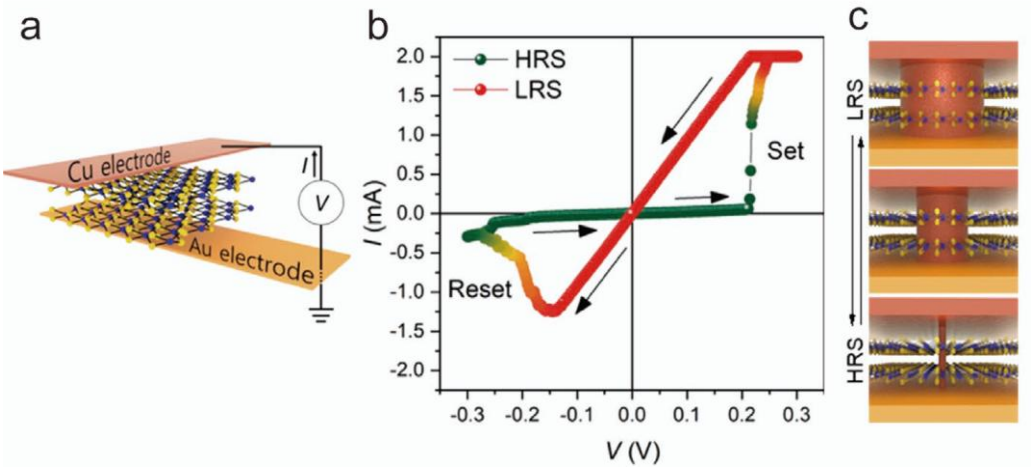

Figure 2.8. *Vertical memristors based on formation of metallic filaments. a) Schematic of Cu/MoS_2/Au memristor. b) Typical switching curve showing HRS and LRS transition. c) Schematics depicting filament formation and deformation causing resistance changes [28].*

2.2.2.4. Schottky barrier modulated vertical memristors

These memristors use a Schottky barrier at the interface between a TMD and metal electrodes to control switching. The Schottky barrier is an energy barrier that affects how easily electrons can pass through the device. In devices like Au/MoS_2/Au, this transition is due to the shift from Schottky emission (SE) to direct tunneling (DT) [30]. In the high-resistance state (HRS), the device is in operation when the current is restricted by the Schottky barrier. When direct tunneling is triggered by electrons, the device switches to the low-resistance state (LRS). This is a reversible phenomenon and operates with low voltages, usually below 1V, thus making it extremely energy efficient. The formation and rupture of conductive filaments at the interface enable the control of resistance. With their ability for bi-directional switching, ultra-thin form factor, and low power consumption, they have great potential to be used in wearable and flexible neuromorphic electronic systems.

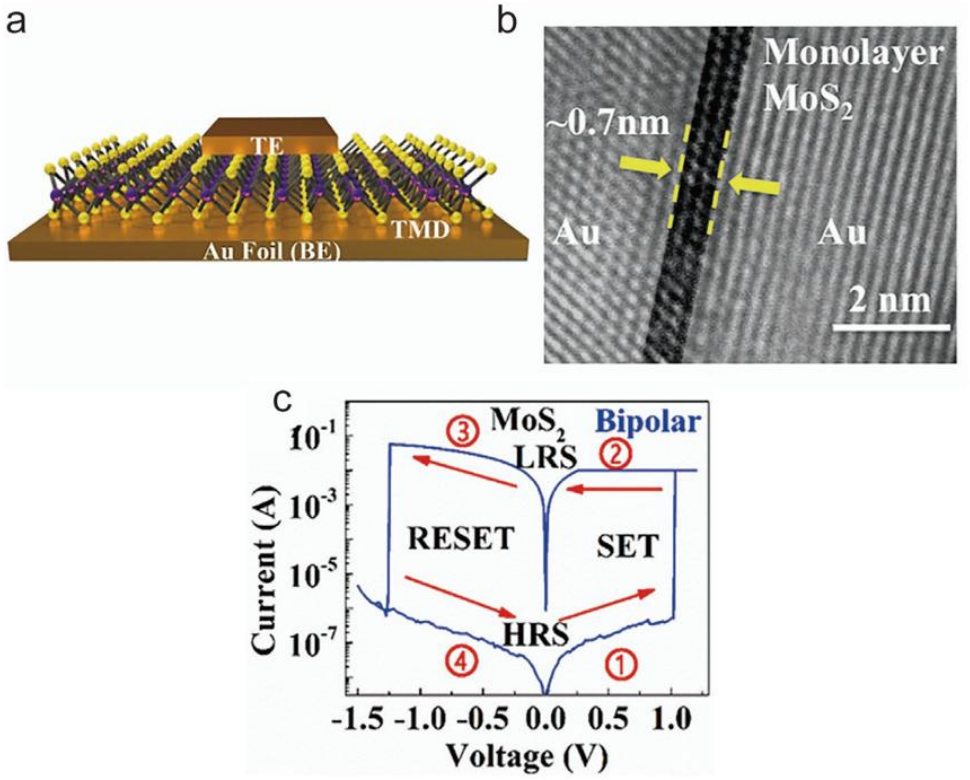

Figure 2.9. *Monolayer-MoS_2-based vertical memristors mediated by transport conversion from SE and DT. a) Schematic of the device with three-atom thick MoS_2 channel. b) Cross-sectional TEM images of Au/MoS_2/Au structure. c) I–V curve indicating bipolar switching.[30]*

2.2.3. Heterojunction memristors

Previously discussed memristors had only one type of 2D material placed between the terminals. However, in heterojunction structures, at least two different materials are in contact to form the active region [31].

More interestingly, these materials can be combined either by direct growth or transfer methods, which creates new opportunities for tuning the band structure and controlling the switching mechanisms in heterostructure memristors.

2.2.3.1. Filament formation mediated heterojunction structure

These memristors function via mechanisms related to the formation and dissolution of metallic filaments in the heterojunction layer consisting of a blend of three-dimensional (3D) and two-dimensional (2D) materials. Some examples of such compounds used together to form the active region are ZrO_2 and WS_2. Under an applied voltage, metal ions, mainly from silver or copper top electrodes, move into the layer, forming a conductive filament bridging the ZrO_2/WS_2 interface. This filament provides contact

between the two electrodes, essentially switching the device into low-resistance state (LRS) from high resistance state (HRS) [32].

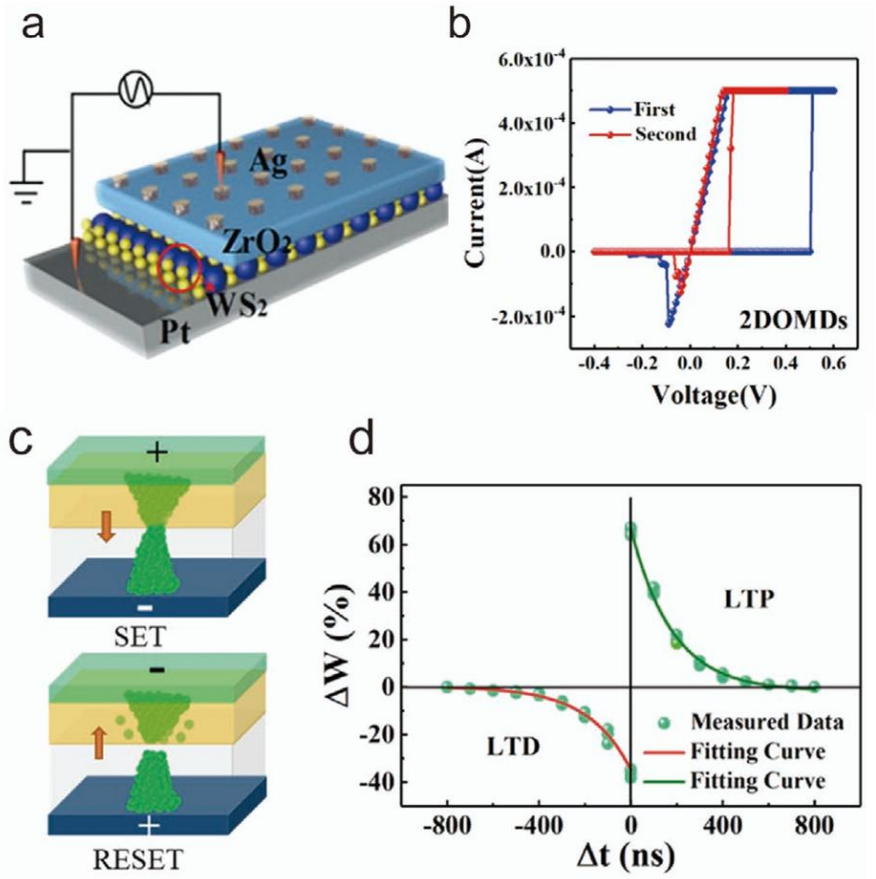

Figure 2.10. *Vertical memristors based on heterojunction-structures mediated by filament formation and charge trapping processes. a) Schematic of the Ag/ZrO_2/WS_2/Pt device. b) Typical I–V switching curve operated at the sub-0.6 V range. c) Schematic depicting the SET and RESET process induced by metallic filament formation. d) STDP characteristics with 0.8 V pulse amplitude and 100 ns pulse width [32].*

- SET Process: A positive voltage creates and grows the filament, reducing the resistance.
- RESET Process: A reverse voltage breaks the filament, returning the device to its HRS.

The heterojunction formed between WS_2 and ZrO_2 provides reinforced control over the growth of the filaments. As a result, it is characterized by low voltage, stable switching properties, and very high longevity. The filamentary formation property of the interface has low levels of randomness and allows high switching velocities in the nanosecond order.

2.2.3.2. Vacancy migration mediated heterojunction structure

In this type of memristor, the switching is caused by the movement of atomic vacancies, especially oxygen vacancies, inside the active layer of the heterojunction. These devices are usually made by combining transition metal oxides (like WO_x) with 2D materials such as WSe_2 or MoS_2.

The application of voltage promotes the diffusion of oxygen vacancies to the interface, leading to the creation of an electric pathway and decreasing resistance.

RESET Process: Applying a reverse voltage moves the vacancies back, breaking the path and restoring high resistance.

Some memristors have an adjustable Schottky barrier, which is controlled by gate voltage. A good example is in the case of WO_x/WSe_2/graphene synaptic barristors, where the height of the WSe_2/graphene barrier is dynamically modulated. This feature extends the functionality of the device, as it is capable of more advanced synaptic operations, such as heterosynaptic plasticity, emulating how the strengths seen in biological systems are modified by a tertiary neuron.

2.3. Memtransistor

The introduction of gate-tunable memristors, known as memtransistors, is a breakthrough by combining the properties of both memristors and transistors [33]. These three-terminal devices take advantage of the merits of memristors to enable parallel computing while also acting as intrinsic selectors in memory arrays [34]. Thanks to their non-volatile memory (NVM) and gate control capabilities, memtransistors can perform operations inspired by biology. Therefore, memtransistors provide great benefits for applications such as in-memory computing (IMC) and neuromorphic systems, especially in environments such as crossbar arrays [35].

Unlike passive memristors, memtransistors are active components that need an external power source to operate. In earlier research, some devices showing memtransistor-like features were mistakenly identified as memristors, mainly because the definitions were unclear at the time. Today, memtransistors are recognized separately, especially because they work based on filament, ion, or vacancy movement, and because their conductance can be adjusted through an electrostatic gate. Currently, most memtransistors are made using 2D materials, especially transition metal dichalcogenides (TMDCs) [36].

Sangwan et al. described a memristive behavior by adding a gate terminal to a traditional two-terminal memristor in 2015. Their article, titled "Gate-tunable memristive phenomena mediated by grain boundaries in single-layer MoS_2," presented how the memristive response could be controlled using the gate [37]. This device did not entirely live up to L. Chua's definition of a memristor [1], but it presented an innovative method for controlling memristive features. Later on, in 2018, multi-terminal memtransistors based on polycrystalline monolayer MoS_2 appeared [38]. These devices had non-volatile memory characteristics and could control parameters related to resistance alteration using the gate. This ability makes them suitable for neuromorphic computing, where proper simulation of synaptic behavior is required.

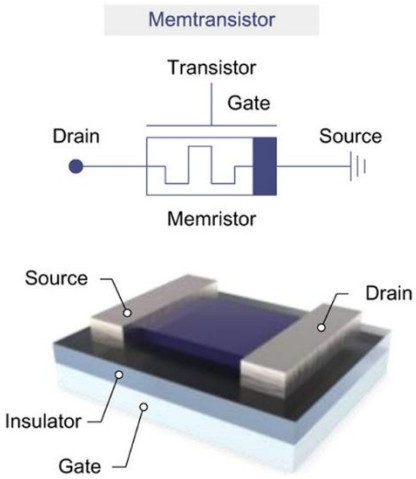

Figure 2.11. *Memtransistor schematic representation [36]*

2.3.1. Memtransistor classification and working mechanism

Memtransistors appear in many forms, including versions that show operating mechanisms comparable to those of memristors, including ion vacancy migration and phase change effects. However, the existence of a third terminal in memtransistors provides properties that are different when compared to two-terminal memristors. Adding one more terminal to the device changes the reaction to voltage or current, causing the properties to diverge without changing the basic operating principles. As such, it is crucial to update the mechanisms that are specific to memtransistors [39].

The basic mechanisms in memristors can be grouped under six major categories: ion vacancy migration, filament formation, ferroelectric effects, tunneling, charge trapping, and phase transitions [36]. All these mechanisms depend on the changes in the solid state properties of the material, which can be modifications in the band structure, structural changes, or phase transitions.

Memtransistors mimic properties of memristors, yet their progress is hindered by three major issues:

Incorporating semiconducting materials is necessary, although most memristors make use mostly of oxides. They rely on artificial defects that control electron or hole transport to change resistance, unlike traditional FETs made with single-crystal materials. They mostly depend on ultrathin 2D semiconductors to make electrostatic gating possible.

2.3.1.1. Ion vacancy

In traditional electronic devices, dopants are homogeneously spread across the material, yet through the application of an electric field, the excess acceptors or donors provided by the dopants move around in the channel. For the TiO_x memristors, the movement of oxygen vacancies is the most important factor [40], resulting in inhomogeneous doping affecting the Schottky barrier.

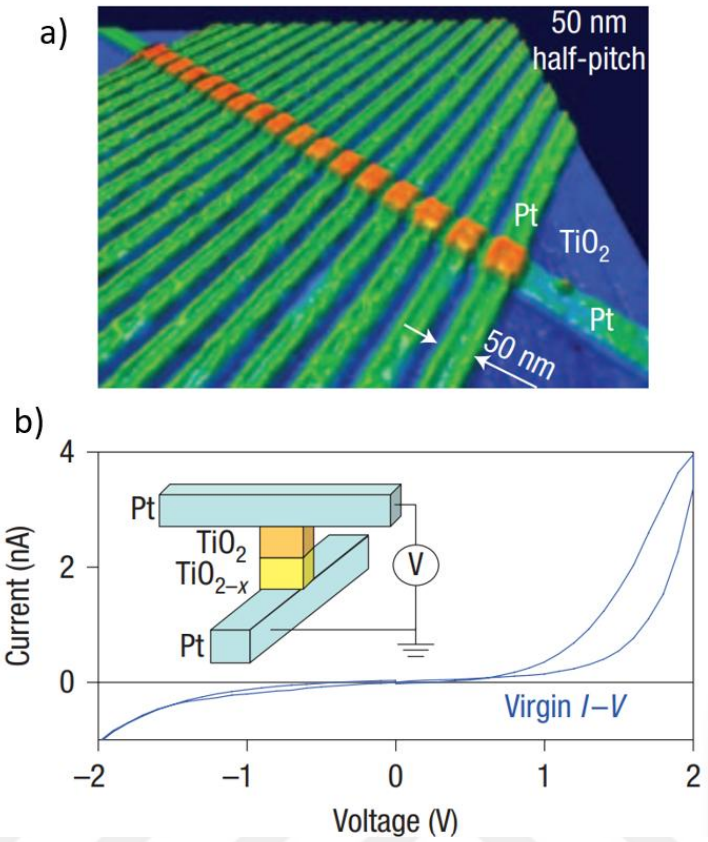

Figure 2.12. *Bipolar reversible and nonvolatile switching of nanoscale TiO_{2-2x} devices. a, An AFM image of 1 17 nano-crosspoint devices with 50 nm half-pitch. Pt nanowires fabricated by nanoimprint lithography sandwich a 50-nm-thick TiO_2 insulating thin film. b, The initial I2V curve of the device in its virgin (preswitching) state exhibits a rectifying characteristic. Inset: The 50-nm TiO_2 has two constituent layers; a near-stoichiometric TiO_2 layer rests on top of an oxygendeficient TiO_{2-2x} layer*

On the other hand, the first reported memtransistor based on MoS_2 is characterized by sulfur vacancies, which move along the grain boundary under an electric field. They act similarly to dopants, effectively changing the dopant concentration and the Schottky-barrier modulation [13]. In addition, single-layer MoS_2 offers the functionality of gate tuning through electrostatic gating, which is not present in compounds like TiOx.

For vacancy mechanisms, mobility is supported by the introduction of an electrical field. Their mobility depends on various parameters, such as their size, their number, and the spatial properties of their corresponding defects. To obtain more precise grain boundary control, methods based on helium beam-induced grain boundary engineering have been introduced. They help in improving sulfur vacancy migration efficiency. Similar concepts have also been extended to other classes of materials. Examples include

ultrathin two-dimensional metal-oxide (TMO)-based memtransistors such as 2-nm SnO_3, which have been designed to examine these phenomena more deeply.

For vacancy migration and electrostatic gating to be effective, semiconductor devices must have a thinned thickness to achieve and ensure homogeneous defect distribution. However, vacancy migration generally requires high activation energies, especially in cases concerning two-dimensional defects such as grain boundaries. Therefore, this necessity imposes the requirement for high operating voltages, which is unfavorable for applications that try to conserve power.

In this regard, researchers have proposed the application of compounds that promote high ion vacancy mobility, such as the employment of superionic conductors [41]. Also, the use of compounds such as $LixMoS_3$ [42] has been proposed, which provide easy paths to vacancy diffusion without compromising their semiconducting properties.

Although both of these strategies are promising, they still face many challenges, especially with phase transitions and the use of 3D oxide materials. However, with continued progress in material synthesis techniques, it may become possible to create memtransistors that operate with much lower power consumption.

2.3.1.2. Filament formation

Memories are created through an electroforming mechanism, whereby an electric field creates a conductive path between two electrodes that are placed in a semiconducting substance [43,44]. In the case of memtransistors, changes in conductance depend upon the creation or destruction of the filament.

The effectiveness is limited to the off state, as the on state is based on the existing metal-to-metal contact. In the off state, the structure reverts to metal–semiconductor–metal configuration, thus making it possible to control the device. In Ag–MoS_2 memtransistors, gate-controlled resistive switching is due to the Ag ion migration (Figure 2.13) [45]. The ions help to form a conductive filament; additionally, by way of electrostatic gating, the MoS_2 channel, being in the off state, can be tuned to different levels of memory.

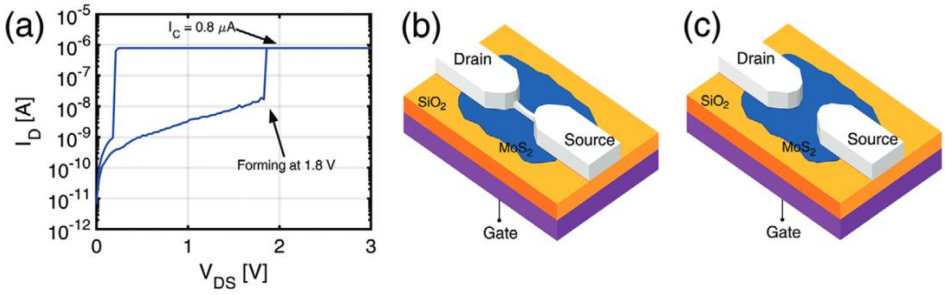

Figure 2.13. *Forming operation in the memtransistor device. a) Measured I_D–V_{DS} characteristic of the device during the forming process. Forming is evi-denced by the steep increase of current at V_{DS} = 1.8 V. A current limitation to IC = 0.8 μA was adopted to prevent destructive breakdown. b) Schematicof the MoS_2 memtransistor switching mechanism. For small V_{DS} the metallic electrodes are physically separated and the current is confined in thesemiconductor channel region. c) After forming or the set transition, a CF is formed between the two electrodes, thus enhancing conductance. The CF is then spontaneously dissolved as V_{DS} is decreased below a holding voltage.*

Despite their particular limitation—such as unbalanced silver distribution and diminished stability in very thin channels (for example, 18 nm)—these devices are still very suitable for application in ultra-dense memory owing to their capability to provide an effective on/off ratio as well as low operating voltage.

2.3.1.3. Ferroelectric

Ferroelectricity is the ability of certain materials to create an electric polarization which can be controlled using an external electric field [46,47]. A specific example is seen in a three-terminal device based on van der Waals α-In_2Se_3, where it was shown that the Schottky barrier can be tuned through voltage-controlled in-plane ferroelectric switching (Figure 2.14) [48].

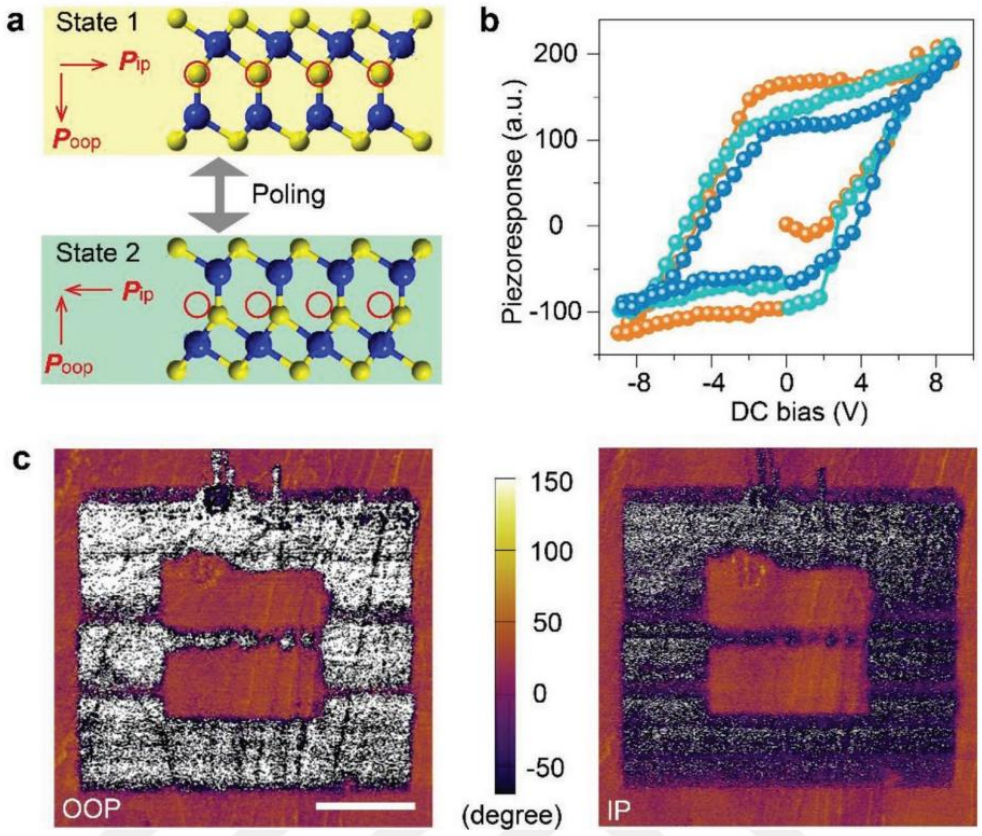

Figure 2.14. *The interlocked out-of-plane and in-plane ferroelectricity in multilayer 2H α-In_2Se_3. a) The α-In_2Se_3 crystal structures depicting the interlocked polarization mechanism in the OOP and IP orientations. The yellow and blue balls represent Se and In atoms, respectively. After large bias poling that exceeds the coercive voltage, the central Se atoms, which are the origin of the interlocked spontaneous polarization, move toward the bottomright direction, simultaneously reversing the OOP and IP dipoles (State 1 → State 2). b) Piezoresponse hysteresis loops (three cycles) for a multilayer α-In_2Se_3 crystal. c) The OOP and IP phase images after forward (+8 V) and reverse (−8 V) DC bias written in the outer square and two inner rectangles. Scale bar: 500 nm [46].*

Because α-In_2Se_3 is both thin and a 2D semiconductor, it is highly sensitive to electrostatic gating. This property allows its channel conductance to be tuned by the gate. The in-plane polarization of the material can be changed by coupling it with out-of-plane polarization, which adds more control to the system.

The device further demonstrates variable photocurrent due to its memristive switching property, which further augments the functionality of the device [49]. Utilizing the optical properties and gate-control functionality of α-In_2Se_3, it is feasible to build a multimodal reservoir computer. The device in question can potentially perform heterosynaptic plasticity by having both optical and electrical control mechanisms.

It is also possible to grow the range of ferroelectric memtransistors by including other 2D ferroelectric materials, such as GeS [50]. Compared to devices based on ion

vacancy mechanisms, ferroelectric memtransistors offer advantages because they do not need artificially created defects. Since they are made with highly crystalline materials, they also provide faster switching, due to the small atomic movements required for ferroelectric-resistive switching.

2.3.1.4. Charge trapping

Charge storage in field-effect transistors (FETs) is the build-up of electric charges, i.e., electrons or holes, in the dielectric film or in the semiconductor/dielectric interface. It is usually due to defects, contamination, or the native electrical properties of semiconductor and dielectric materials used [51]. These trapped charges can be the cause for compromising the functionality and reliability of FETs. Despite these issues, FETs are still being used to develop the state-of-the-art non-volatile memory (NVM) devices.

For example, the adsorption of atmospheric gas molecules by WSe_2 memtransistors leads to charge confinement, yielding multilevel data retention—a key part of the device functional paradigm (Figure 2.15) [52]. Interacting with atmospheric conditions causes the emission and trapping of electrons at the air–semiconductor interface, which alters the carrier density and yields high hysteresis. Through gate voltage tuning, it is then possible to manipulate the treatment of the trapped and emerging carriers, making gate-tunable memristive switching feasible.

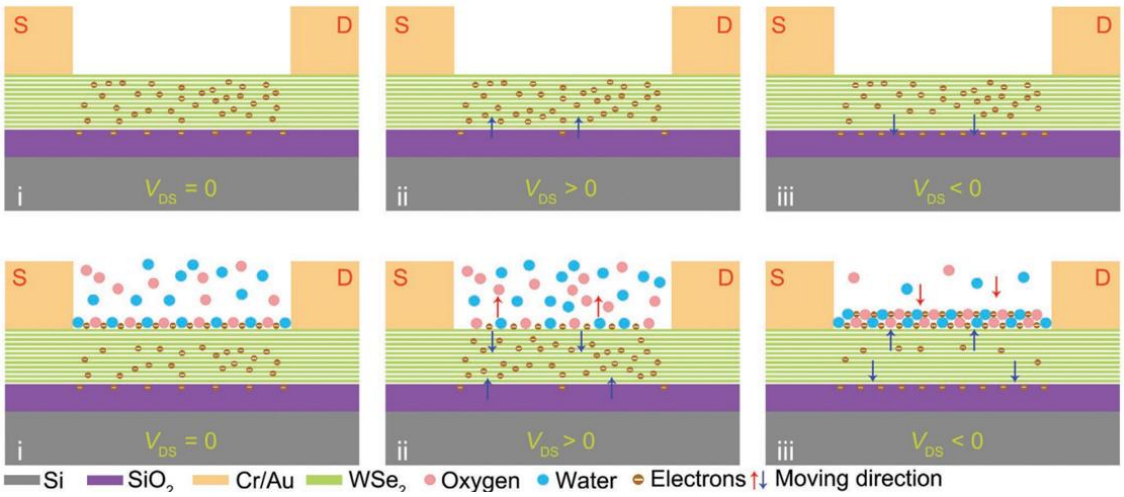

Figure 2.15. *Schematic diagrams of the working mechanism in terms of charge trapping/detrapping (i: initial state V_{DS} = 0, ii: under V_{DS} > 0, iii: under V_{DS} 0, iii: under V_{DS})*

On the other hand, in unexposed dual-gate MoS_2 memtransistors, there is a clocking-bipolar switching phenomenon over a spectrum of gate voltage values [53]. In these devices, there is the formation of space-charge region at the MoS_2-Al_2O_3 interface, thereby causing band bending in the MoS_2 material. The shape of the hysteresis loop is controlled by the processes of emptying and filling in traps in the MoS_2 or the Al_2O_3 layers.

Although charge-trapping-based memtransistors show promise for building stable NVM devices, they still face challenges such as slow switching speeds and high operating voltages, especially when additional charge storage layers are not included in the design.

2.3.1.5. Heterojunction

Because of the difficulty in achieving full memtransistor behavior in a single material, researchers have looked at heterojunctions that combine traditional semiconductors with other materials—often insulators—to create properties similar to those of memristors. The ultimate goal is to create memtransistors using simple material combinations.

First, a vertical structure was formed using layers of graphene/WSe_2/WO_{3-x} (Figure 2.16)[54]. In this structure, the graphene/WSe_2 interface modulates the size of the Schottky barrier to act as a barristor. At the same time, oxygen vacancy in WO_{3-x} provides the memristor properties. Through the combination of qualities of the barristor and the oxide memristor, this structure is a synaptic device, offering gate-controllable changes in synaptic weight.

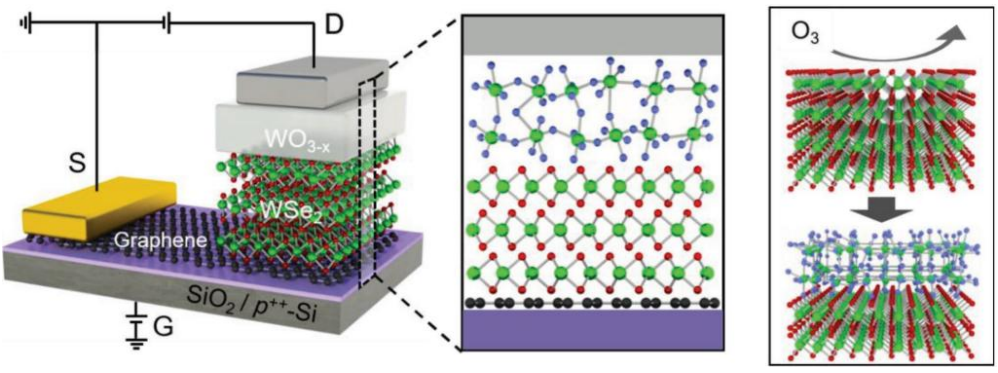

Figure 2.16. *Circuit and schematic representation of diagrams of the synaptic barristor consisting of a vertically integrated WO_{3-x} memristor and WSe_2/graphene barristor. b) Schematic illustration of the monolithic oxidation process by UV-ozone treatment. This process converts the topmost WSe_2 layer to amorphous WO_3–x. c.*

In the second design, the memtransistor utilizes a heterojunction of MoS_2, h-BN, and graphene through a tunneling mechanism [55]. In this setup, MoS_2 is used as the channel, h-BN as the tunneling barrier, graphene as the back gate, and a gold layer is used as the floating gate (FG). The current is increased through electron accumulation in the FG when a positive voltage is applied to the drain. In addition, the device allows for the removal of these electrons when a negative voltage is applied. Such a working principle enables memristive switching through electrostatic potential, similar to the operation of tunneling RAM [56]. The device showed multilevel resistance switching, analog weight modulation, fast switching capability (50 ns), and low energy consumption (around 7.3 femtojoules). In the third example, gate-programmable multistate memory was displayed, using a multilayered structure consisting of graphite, $CuInP_2S_6$, and MoS_2 in an MFS structure (Figure 2.17) [57]. In this device, the voltage across the drain controls the state of polarization in $CuInP_2S_6$, hence affecting the height of the existing energy barrier between MoS_2 and $CuInP_2S_6$. Unlike conventional ferroelectric tunneling junctions, this particular structure allows for dynamic tuning of the height of the barrier through gate voltage. Multistate memory was exhibited by the device, such that the on/off current ratio was as high as 10^5, which represents an effective strategy to mitigate problems related to high-power consumption and voltage requirements typically experienced by conventional single-device memtransistors

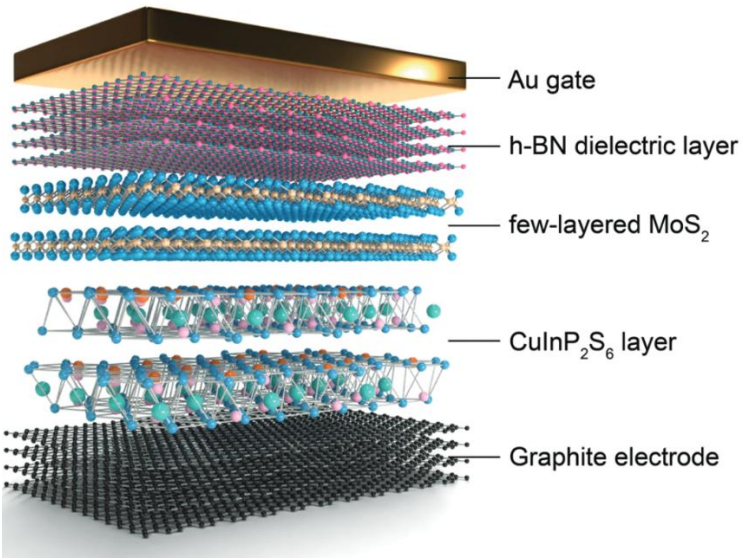

Figure 2.17. *Characterizations of vdW M-FE-S heterojunctions. a) Schematic illustration of M-FE-S memristor. b) A typical pinched I–V curve obtainedin a vdW M-FE-S heterojunction, showing characteristic memristive behavior [57]*

2.4. Memtransistor- Memristor Applications

2.4.1. Memristors as memory devices

Within the fast-growing area of electronics, memristors based on two-dimensional (2D) materials have emerged as a pioneering technology, exhibiting significant promise throughout a wide range of application fields, especially for high-density memory systems Figure 2.18 [58]. The existing memory devices are regarded as intrinsic building blocks of contemporary computing designs, enabling improved mechanisms for information storage and retrieval. The unique features based on memristors from 2D materials make them competitive contenders for replacing conventional memory technologies. Advances in electronic systems from mobile devices to artificial intelligence (AI) have been linked to developments within memory technologies throughout history.

Traditional memory technologies such as DRAM (dynamic random-access memory), SRAM (static random-access memory), and flash memory are all based primarily on silicon-based CMOS (complementary metal–oxide–semiconductor) technologies, which are now facing critical issues of scaling down further. Memristors are being heralded as an emerging alternative to future technologies, mainly due to their non-volatility, lower power dissipation, and suitability for integration at very high densities. Among these memristors based on 2D transition metal dichalcogenides (TMDCs), those that show lower switching voltages, gate-tuneable switching, and design flexibility are suitable for various memory applications such as volatile and non-volatile memory and level storage.

While computing has been enhanced by in-memory databases (IMDs) that are CMOS-based, these face integration and scalability issues. There has been recent research into IMDs based upon 2D materials to overcome these challenges. The single-crystal-like surface of 2D materials, which is free from dangling bonds, is important for designing new IMD systems with improved performance when compared to traditional CMOS systems.

This section presents a summary of recent developments in memristor arrays based on 2D materials, showing how they could overcome CMOS limitations and contribute to faster and energy-efficient AI chips. For example, a memristor made from 2D cobalt–nickel (Co-Ni) layered double hydroxide (LDH) nanosheets showed bipolar resistive

switching and non-volatile memory behavior[59]. Its gradual switching mimicked biological synapses, making it suitable for neuromorphic applications.

Fatima et al. [58] introduced a free-standing carbon-based 2D memristor, incorporating materials like graphene and MXene to fabricate flexible memory devices. Their design included structures like rGO/GO/rGO and MXene/GO/MXene, which demonstrated both capacitive and resistive switching behaviors, supporting self-powered memory functions. Another study combined Ti_3C_2Tx MXene and graphene oxide (GO) with bismuth ferrite ($BiFeO_3$), achieving both NDR and resistive switching. These devices showed strong durability and stable operation for flexible electronics [60].

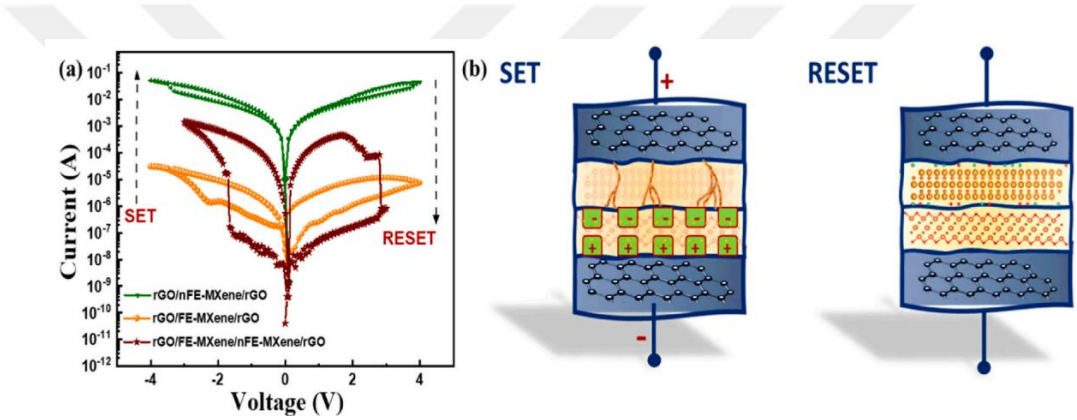

Figure 2.18. *The first I-V cycle of rGO/nFE-MXene/rGO, rGO/FE-MXene/rGO and rGO/FE-MXene/nFE-MXene/rGO memory devices illustrating a comparison of device switching behaviors (b) Conduction mechanism for SET and RESET states in rGO/FE-MXene/nFE-MXene/rGO trilayer device [58]*

Zhou et al.[61] highlighted how 2D TMDC-based memristors could be more tunable and efficient than traditional transition metal oxide (TMO) memristors. Their designs included four types of resistance switching behaviors, largely influenced by Schottky barrier modulation and defect-driven current rectification (Figure 2.19). Gu et al. [62] demonstrated memory devices using MoS_2 and WS_2, showing their potential to go beyond the von Neumann architecture. By tuning the sulfurization process, they improved the uniformity and size of 2D films.

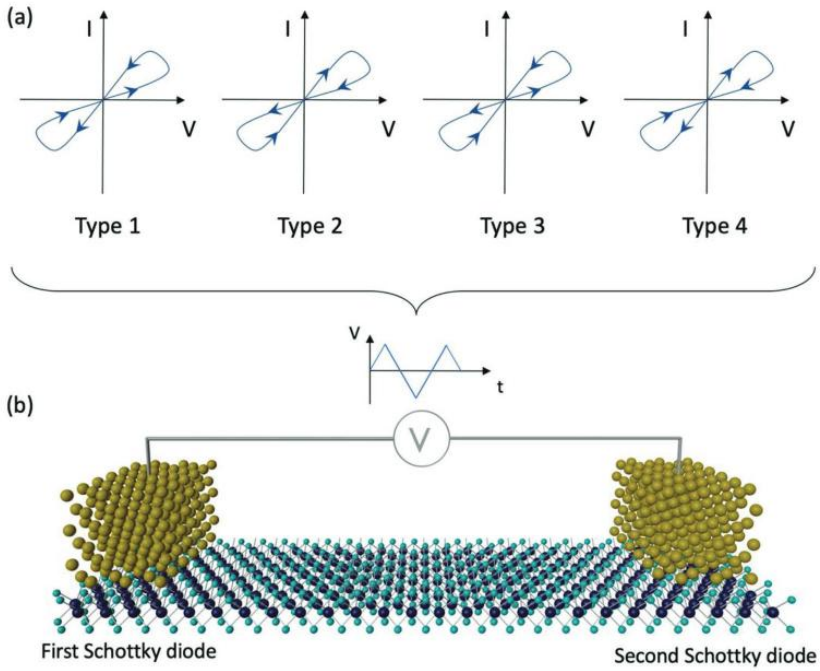

Figure 2.19. *a) Representative schematic I–V characteristics of the four types of two-terminal memristors. b) Schematic for a metal-TMDC-metal lateralstructure, in which two metallic electrodes are connected to the TMDC layer (functional material). Two Schottky contacts are formed at the metal-TMDCcontact and TMDC-metal contact.*

The utilization of 2DLMs has been studied in the fields of RRAM, MRAM, and FeRAM [63]. A prototype has been built using $MoTe_2$ memory and WSe_2 selectors. Such observations suggest that 2D materials are likely to outperform silicon when considering operational speed, density, and energy efficiency. Special importance has been assigned to exploring two-dimensional TMDCs for their improved mobility, which is key to realizing fast switching [64]. New 1T1R 2D crossbar arrays have been conceived for in-memory computing to provide improved bandwidth and integration levels compared to traditional systems.

Memristors based on 2D materials like graphene, h-BN, and TMDs have reached key milestones: ON/OFF ratios up to 10^8, switching voltages as low as 0.05 V, switching speeds of 1.5 ns, and power consumption as low as 1 fW [65]. These characteristics make them attractive for intelligent nanoelectronic applications [66], though challenges like improving switching speed and device yield remain. A SnSe-based memristor with ferroelectric polarization control was shown to support multi-level storage, logic operations, and photoresponse memory [67]. Mitra et al. [68] investigated how 2D materials contribute to resistive switching by simulating how different electrode types (passive vs. active metals) affect switching mechanisms. Their results suggested that

mechanisms like B–N bond formation and S atom release at defects are key to achieving reliable switching.

2.4.2. Artificial intelligence

Computer science scholars have long pursued extending the roles of computing systems from mere processing of information to realms like learning, skill acquisition, and scientific inquiry. The central notion behind artificial intelligence (AI) is based on developing machines capable of mimicking processes of the human brain, such as solving and making decisions. Advances in AI have largely resulted from activities focused on duplicating organizational layout and working mechanisms of the human brain through mechanisms of machine learning and neuromorphic computing designs that mimic neuronal and synaptic processes.

Recent developments identified 2DLM-derived memristors as scalable and promising candidates for changing computational frameworks in the field of artificial intelligence (AI). The central goal of AI is to create systems capable of solving tasks that are highly complex using effective and reliable computing frameworks. The distinct qualities of two-dimensional materials combined with memory and switching capabilities associated with memristors provide significant avenues for the advancement of technologies related to AI. The 2D material-based memristors have the capability to enable fast, power-effective, and adaptive computing systems compliant with the exacting requirements of AI algorithms.

As AI develops, there is a growing need for in-memory computing technologies, supported by improvements in both algorithms and hardware. Neuromorphic systems continue to evolve by integrating analog computation, memory storage, and brain-inspired processing functions. Memristive circuits based on 2D materials are expected to help AI applications such as image and speech recognition, language processing, and autonomous systems. For example, Yoon et al. [69] developed a 2D memristor that successfully acted as a nociceptor, imitating biological functions like non-adaptation and sensitization in a small and scalable device (Figure 2.20.). They also built a thermal nociceptor module, showing that artificial nociceptors can be integrated into AI systems like robots. These devices demonstrated adaptive switching properties and variable response thresholds, similar to how biological tissues react to injury.

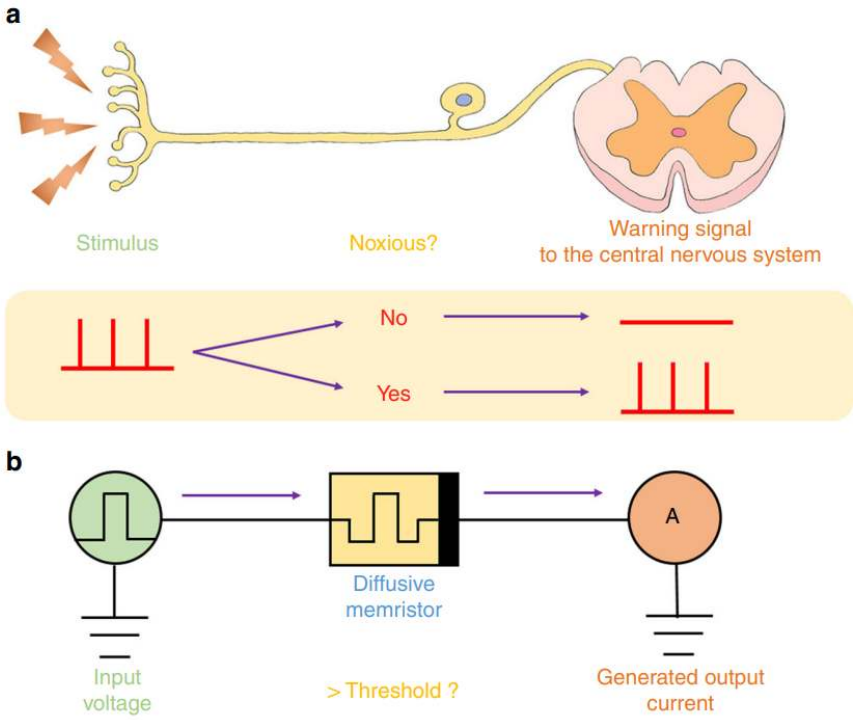

Figure 2.20. *One to one correspondence of the nociceptor system in the human body and an artificial nociceptor circuit consisting of a diffusive memristor (threshold switch). a When a noxious stimulus is received from a free nerve ending, the nociceptor compares the amplitude of the signal with a threshold value and decides whether an action potential should be generated and sent to the brain via the spinal cord (central nervous system). b An electrical pulse applied on the device emulates the external stimulus. When the pulse amplitude is higher than the threshold voltage of the diffusive memristor, the device is turned ON, and current pulses are generated*

Resistive switching based memristor devices have been proposed to be an energy-efficient and compact alternative for traditional transistors in artificial neural network construction by combining memristor synapses and CMOS neurons[70]. A 2D memristor device exhibited exemplary low power consumption by using only 7.35 nW or 100 nA and delivering an accuracy rate of 90.37% for pattern recognition operations [71].

Additionally, memristors based on 2D h-BN (hexagonal boron nitride) thin down to sub-nanometer thicknesses (between 8 and 10 nm) recorded quick functioning under minimal voltage conditions and proved to be superior to traditional memristors [72]. Arrays of such h-BN memristors with an Au/h-BN/Ti configuration, with active area of 3 μm × 3 μm, successfully performed primary machine learning operations like dot product computation and linear regression, thus proving 2D materials capable of facilitating compact and power-efficient artificial intelligence hardware.

Sun et al.[73] demonstrated one such language-acquisition reservoir computing system based on 2D SnS (tin(II) sulfide) memristors. The devices manifested critical

features such as nonlinearity, high dimensionality, and fading memory, which are respectively reflected through. The devices exhibited discrete memristive behavior and possess an accuracy of 91% for classification of short Korean sentences due to their presence of distinct dual-type defect states. They exhibited direct response to optical stimulation, which allows for in-sensor processing of time-based information and reduces system cost and complications (Figure 2.21).

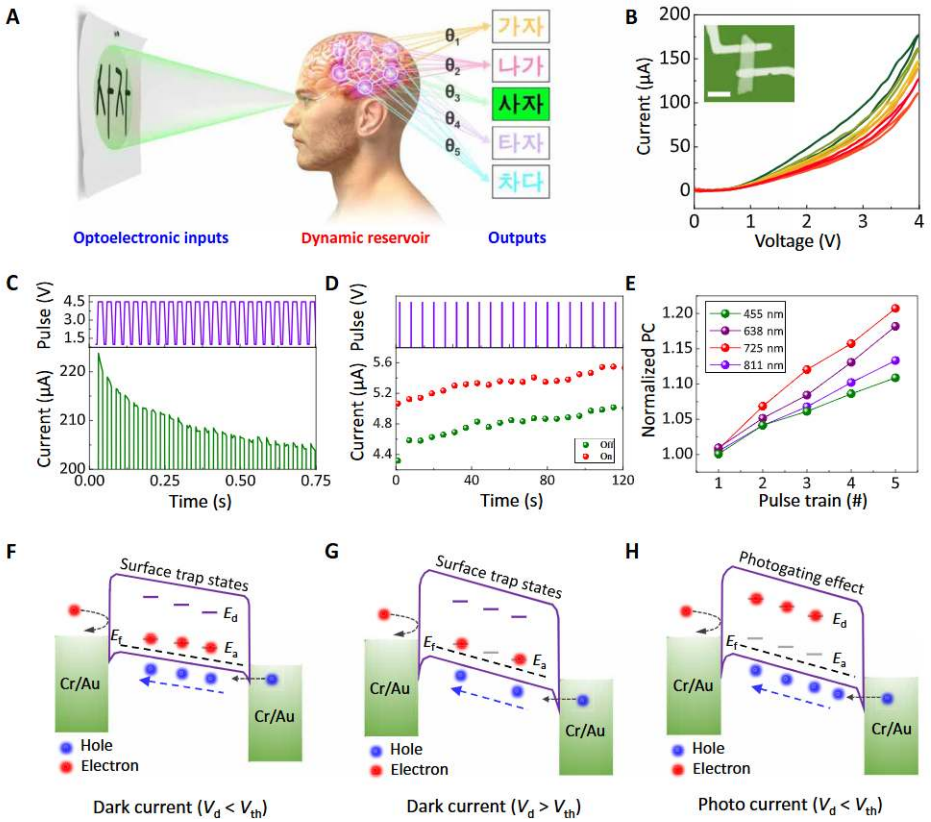

Figure 2.21. *Chemical Brain dynamics and spatiotemporal information processing based on in-sensor RC. (A) Schematic of the cognitive task implemented on a biological RC sys-tem. Language learning is carried out by the visual cortex, which can perform time-series computations for sequential inputs. (B) Transport behaviors reflecting thecharge trap/detrap dynamics in SnS with an optical microscopy image of the device (inset with a scale bar of 2 m). The first and final cycles are green and red colors,respectively, and the electrical (C) and optical (D) pulse switching characteristics. Electrical pulses (4.5 V and 20 ms) with an interval of 10 ms were used in (C). Opticalpulses with a wavelength of 725 nm, a power of 43 mW, and a width of 3 s were used in (D). The read voltage was 0.5 V. (E) Normalized photocurrent (PC) under continuousoptical stimuli with 455, 638, 725, and 811 nm. (F) Acceptor states (Ea) are occupied by electrons in p-type SnS with the Fermi level (Ef) close to the valence band inconventional transport. (G) With a Vd exceeding a threshold voltage (Vth), the electrons trapped at acceptor states are recombined with holes, decreasing the channelcurrent. (H) Under light illumination, electrons are excited and trapped in the donor states created by S atomic vacancies, producing more holes in the valence band andleading to greater conductivity (photogating effect [73]).*

2.4.3. Synaptic electronics and neuromorphic systems

Neuromorphic computing describes computer architectures inspired by how biological nervous systems function. These computer architectures utilize power-efficient, event-based, and heavily parallelized hybrid analog-digital circuits to carry out neural calculations. A germane example of such is spiking neural networks (SNNs), wherein computing takes place merely upon spike transmission and reception between individual neurons. Neurons sum weighted spikes, process them, and produce output spikes when a specified threshold is reached. This synchronized dynamic allows them to perform operations like pattern recognition, decision-making, and learning. Neuromorphic systems are further capable of enabling lifelong learning under supervised and unsupervised learning paradigms.

Material selection is key to designing successful neuromorphic systems. Among materials, two-dimensional layered materials (2DLMs) are especially prominent by virtue of their exceptionally thin characteristics, which enable improved switching rates, lower power consumption, and larger storage capacities. Their ability to mimic synaptic plasticity has paved the way for computing methods based on brain-like approaches. The memristors formed from these materials are equipped with processing ability, self-learning capability, and reliability. These devices are applied across a range of fields, such as pattern recognition, machine learning, and artificial intelligence systems. Future exploratory efforts are aimed at optimizing their reliability, durability, and energy efficiency, thus making them fit for application purposes under real-world conditions.

For instance, Yan et al. [74] developed a 2D Ti_3C_2Tx MXene memristor that could switch between STP and LTP within 10 nanoseconds, demonstrating biological synapse-like behavior (Figure 2.22 a-i). Another study used amorphous boron nitride (a-BN) for CMOS-compatible memristors, achieving multiple conductance levels and high pattern recognition accuracy (95.8%) [75]. WSe_2-based memristors, grown using salt-assisted CVD, showed reliable switching and mimicked both short- and long-term synaptic behaviors [76].

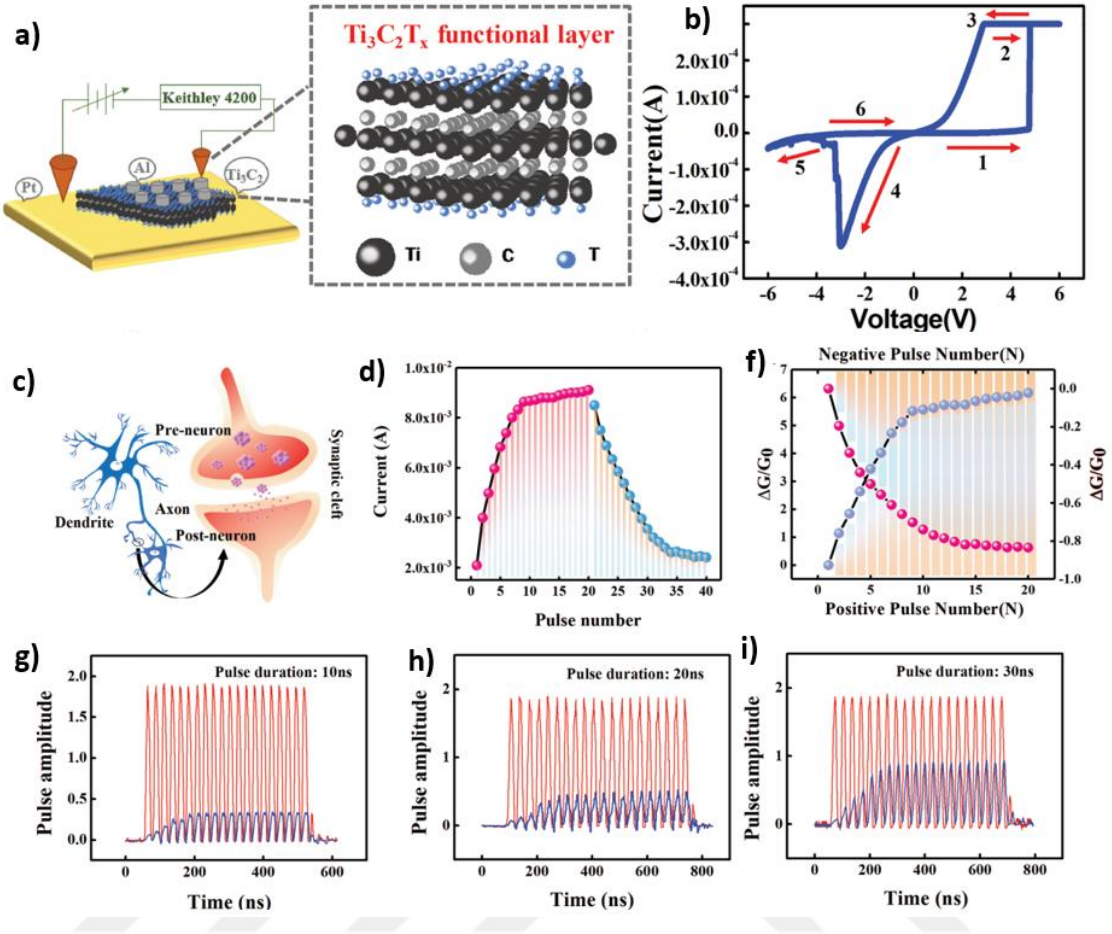

Figure 2.22. *a) Schematic structure of the Al/Ti₃C₂Tx/Pt device and Ti₃C₂Tx atomic structure (Tx stands for surface termination). b) Typical I–V curves of the device. c) Illustration of synaptic plasticity adjustment between axons and dendrites. d,f) Measured and simulated device potentiation (1st to 20th pulse) and depression (21st to 40th pulse) curves under the application of successive AC pulses. Positive bidirectional pulse train with different parameters is used to excite or inhibit synapses. g–i) Initial data of continuous pulse regulation with different pulse durations.*

Xu et al. [77] demonstrated a vertical MoS_2 memristor that had very low switching voltages (0.1–0.2 V) and exhibited spike-timing-dependent plasticity (STDP), an essential feature of biological learning mechanisms. Similarly, WS_2-based memristors had fast switching times (13–14 ns) and had very low power consumption, validating their feasibility for low-power neuromorphic computing purposes. Other devices, such as $MoSe_2/MoS_2$ junctions [78] and 2H-$MoTe_2$ thin films [79], further demonstrated essential synaptic operations like potentiation and depression.

Novel devices like laser-induced graphene (LIG) memristors [80] and oxygen-passivated MoS_2-based synapses exhibited improved switching behavior and significant endurance. Janus MoS_2 devices, which are based on their asymmetrically surface-

functionalized design, enabled an evolution from short-term potentiation (STP) to long-term potentiation (LTP) by using optical and electrochemical stimuli. This highlights the importance of incorporating optical inputs into developing state-of-the-art, energy-effective neuromorphic systems [81].

Additional innovations include the use of 2D $PdSe_2$ with Al_2O_3 layers, improving multi-level resistance switching [82], and hBN-based memristors utilizing stochastic resonance to support biological-like signal processing [83]. Li et al. [84] reported a high-performance Ag/IPS-based memristor using van der Waals metallic 2D materials, reaching 10^8 ON/OFF ratios and attojoule-level power consumption, showing excellent potential for CNN-based AI applications.

Finally, Chen et al. [85] developed a flexible $CuInS_2$-based 2D memristor with low-power operation (<10 nW) that replicated LTP/STP, paired-pulse facilitation, and STDP. When integrated with convolutional neural networks, the device achieved 96.7% accuracy on MNIST and 81.4% on Fashion-MNIST, confirming its usefulness in flexible neuromorphic systems.

2.4.4. Optic, photonic devices

2D memristors offer new prospects for improving photonic and optoelectronic systems to overcome memory limitations by incorporating memory and resistive switching functions into a single device. The characteristics enable brain-like calculations to be carried out in situ. Coupling photonic and artificial neural networks (ANNs) makes scaling up photonic neuromorphic computing systems simpler [86]. Unlike oxide-based conventional memristors, devices based on 2D materials have advantages like scalability, fast speed, long lifespan, and minimal power consumption, which make them suitable for memory and computing-intensive applications.

Thanks to their plasticity, 2D material memristors can mimic biological synapses, a property that is beneficial for pattern recognition and image storage applications. The strong light-matter interaction in 2D materials makes them highly compatible with the development of photonic memory and artificial synapse devices. 2D photonic memristors have also shown potential in numerous applications, such as image sensing, logical operations, and neuromorphic systems, with benefits that include low switching voltages, high integration densities, and flexible design platforms [87].

Another advantage is that the properties of 2D materials can be tuned by applying a gate voltage, enabling improved management of resistance states, volatile memory, and storage capacity. The bioelectric signals of memristors based on 2D materials, in specific configurations, can imitate transfer of calcium ions (Ca^{2+}) between neurons. Also, their high sensitivity to light allows it to act as a presynaptic signal, hence enabling construction of energy-efficient photoelectronic synapses.

Recent studies have shown that 2D synaptic devices can complete tasks like image classification and data encoding within nanoseconds. Because of these properties, 2D material memristors are considered promising for high-speed imaging, 3D memory, and depth sensing. The progress in this area is helping to create practical photonic ANNs, which may significantly improve both optoelectronics and photonics.

Various groups have investigated this topic with improved accuracy. For example, Zhou et al. [88] fabricated a memristor based upon an Ag/GQDs/TiOx/FTO structure that displayed bipolar resistive switching and negative photoconductance (NPC) behavior in their high-resistance condition. The phenomenon that was discovered has been explained by oxygen vacancy migration and interaction that takes place at the interface of GQD–TiOx upon light incidence. Their observation proved that through interface control, NPC behavior can be exploited in memristive devices to contribute to progress in the area of optoelectronic devices.

Wang et al. [89] presented 2D memristors that combine perception, memory, and processing in one device, helping build compact artificial visual systems (see Figure 2.23). These devices performed well in neuromorphic computing, with 86.7% accuracy in face recognition and logic operations like AND/OR gates using photoelectric control. The 5×5 array structure they used highlights the potential of these devices in small, integrated neuromorphic systems.

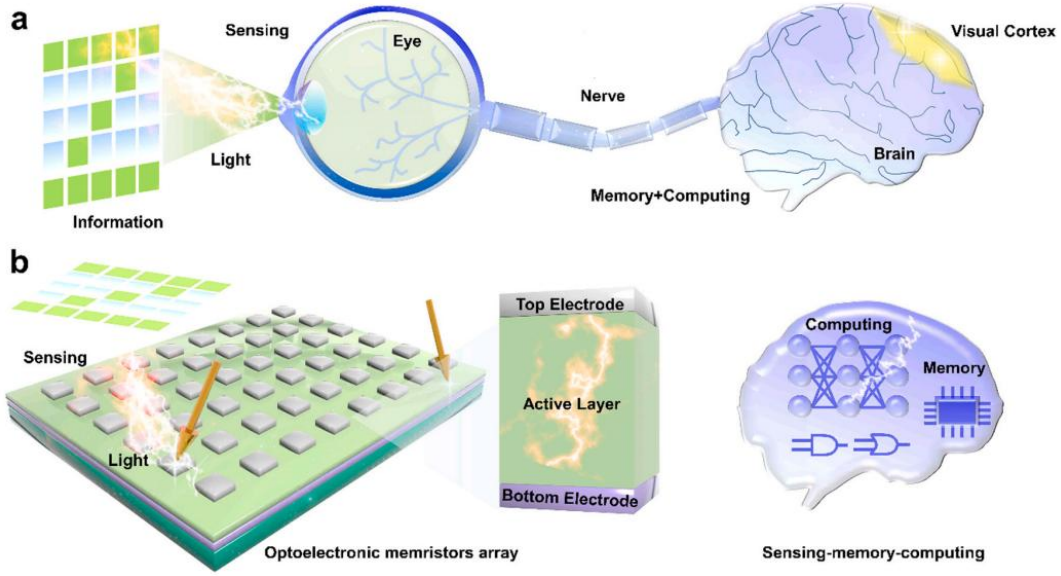

Figure 2.23. *a) Schematic of human visual system and human brain for obtaining picture, pattern recognition and information storage. b) Schematic diagram of the optoelectronic memristors array, single optoelectronic cell and artificial sensing-memory-computing system [89].*

To sum up, 2D memristors can significantly impact optoelectronic and photonic devices, especially since light can be used to control resistive switching. This helps reduce power consumption and supports adaptive artificial neural networks for brain-inspired computing. Materials like graphene, graphene oxide (GO), and MoS_2 have special optical properties that make them suitable for real-time sensing and data processing.

Some designs utilize quantum dots (QDs) to control resistance by inducing phase transitions and mimicking neuronal activity. Unlike traditional supercomputers needing high energy expenditure, the human brain is capable of performing complex operations using around 20 watts. A memristor based on 2D BiOI was formed through low-power operation and displayed electrical and optical synaptic plasticity, which makes it suitable for vision sensors based on retinal mechanisms [90].

As a further example, graphene and hBN have been mixed together to produce memristors that are tunable through optics and have multiple states of resistance. Photodoping through transfer of charge between graphene and hBN has been employed to modulate the conductance of the device [91]. A CeO_2/MoS_2 junction has also been employed to build an optoelectronic memristor that detects color, evidenced by a simulated traffic light application within a 7×7 array [92]. This system further demonstrated human-like pain sensing for application to electronic eyes and robotic systems. Finally, Shamila et al. [93] investigated In_2S_3-based 2D memristors with good

resistance switching behavior and fast programming times (~39 μs at 880 nm). The devices showed excellent performance in optical logic operations and neuromorphic computing with high recognition accuracy rates for numeric digits (98.19%) and alphabetical letters (99.18%).

2.5. TMDs – 2D Material

The recognition of the unusual properties of graphene has led scientists to seek out further two-dimensional (2D) materials for their electronic and optoelectronic applications. Of relevance in this area are transition metal dichalcogenides (TMDs), which have attracted much interest, and there are about 39 distinct compounds identified (excluding variations involving alloys)[94]. The common structural formula for TMDs is MX_2, where M is a transition metal (e.g., Mo, W, or Ti) and X is a chalcogen atom that can be S, Se, or Te[95]. Their crystalline geometry consists of a layer of a metal atom surrounded by chalcogen atom layers, resulting in a hexagonal lattice arrangement.

Transition metal dichalcogenides (TMDs) exist in different crystalline structures, most commonly 2H (semiconducting, trigonal prismatic) and 1T (metallic, octahedral) phases[94]. The most important feature of monolayer TMDs is an indirect-to-direct bandgap transition when compared to their bulk counterparts. For instance, a monolayer MoS_2 has a direct bandgap about 1.9 eV while their bulk counterpart has an indirect bandgap of about 1.2 eV[96]. This bandgap is important for light absorption and emission processes and hence, TMDs are desirable for devices like photodetectors and transistors[97].

Furthermore, TMDs have surfaces free of dangling bonds, making them more environmentally stable and reducing the occurrence of unwanted interface trap states[98]. However, CVD-grown or exfoliated materials can still present defects, such as sulfur vacancies, that can influence their electronic properties. Also, the strong spin–orbit coupling in TMDs leads to band splitting at specific points in the Brillouin zone (e.g., K and K'), enabling studies in fields like valleytronics and quantum information technologies [99].

Thanks to their tunable bandgaps, high ON/OFF ratios, and mechanical and thermal robustness, TMDs—especially MoS_2 and WS_2—are considered promising materials for future low-power, high-performance electronic and optoelectronic systems[100].

Among the numerous transition metal dichalcogenides (TMDs), molybdenum disulfide (MoS_2) stands out for its direct bandgap of approximately 1.8–1.9 eV when it is in monolayer form, which well matches the visible light spectrum. In addition, it possesses high photoresponsivity, excellent mechanical properties, and long-term stability in ambient environments, thus making it a strong contender for the development of a variety of electronic and optoelectronic devices.

Moreover, CVD techniques make it possible to grow large-area monolayer MoS_2 with high crystal quality, which is important for scalable device fabrication. Compared to exfoliated flakes, CVD-grown MoS_2 provides better uniformity and is more suitable for integration into devices. Beyond its optical and electrical properties, MoS_2 memtransistors have shown potential to mimic synaptic plasticity, which is crucial for neuromorphic computing.

By changing fabrication parameters like channel length, one could control device parameters such as hysteresis, modulation of conductance, and short-term plasticity, and hence devices could be designed mimicking biological synapses. Therefore, MoS_2 has been chosen as the main material for research to test how applicable it is for synaptic devices based on memtransistors[18].

2.6. Emulating Biological Synaptic Plasticity with Memristors

Traditional computing architectures, especially the von Neumann architecture, are increasingly failing to cope with the rising demands for quick and power-conscious processing of data, thereby causing a significant bottleneck. The need for intensive data processing has further deepened with the wider adoption of artificial intelligence across fields. A feasible strategy for countering such a bottleneck would be to embrace neuromorphic computing based on the working principles of the human brain. Although complete brain function is not fully understood, mimicking the essential building blocks can help design more intelligent and effective hardware for future artificial intelligence systems.

Within this academic framework, synaptic electronics is an emerging science field committed to designing electronic systems that mimic biological neurons and their synaptic connections[101]. Drawing on knowledge from an extremely wide range of fields such as computer science, neuroscience, physics, materials science, electrical engineering, and artificial intelligence, synaptic electronics seeks to realize neural

systems that are capable of learning, adaptation, and optimal performance similar to human intellect [102]. At present, hardware arrangements that mimic synaptic processes are envisioned to be competitive solutions to overcome the intrinsic limitations of the von Neumann computer architecture based on a physical separation between processors and memory. However, several issues persist. Current fabrication methods are limited by integration and scalability issues, and by a lack of plasticity, which prevents artificial systems from replicating the complexity and efficiency of their natural counterparts. However, a perfect copy of the human brain is not what is sought, but rather an efficient artificial hardware that takes cues from its elementary working principle to accomplish intricate tasks. Of particular interest has been the improvement of devices that can mimic synaptic plasticity, a key factor that supports learning, memory, and neural growth.

Synaptic devices based on synaptic electronics utilize artificial electronic devices, like two-terminal memristors and three-terminal field-effect transistors (FETs), to mimic biological synaptic plasticity in biomimetic systems [103]. Specifically, memristors formed from 2D nanomaterials have proved their importance as key devices for neuromorphic computing due to their simple device designs, potential for integration at electronic densities, and ability to mimic the synaptic plasticity of biological systems. These features hold out a very promising route to hardware-oriented artificial intelligence systems [104].

In biological synapses, plasticity refers to the ability of synaptic connections to change in response to experience. This change, driven by electrochemical signals and temporal dynamics between neurons, is emulated electronically through electrical pulses. The mechanism of synaptic plasticity in artificial devices depends strongly on the physical properties of the active material. To integrate such systems with chip technologies, various 2D materials have been explored (see references). Numerous devices have been fabricated using different working principles and architectures, including sandwich-structured memristors [57], floating-gate structures [105], electrolyte-gated transistors [106], and ferroelectric-gated transistors [47,50].

Synaptic weight variables within such systems can be instantaneously varied based on external inputs, leading to different states of conductance. The adaptation of such weights often depends upon the temporal aspects of presynaptic spikes, such as spike rate, duration, width, and their sequential order. This ability to modulate instantaneously is a key distinguishing characteristic of synaptic devices compared to conventional memory

devices. Even through significant experimental initiatives to replicate biologically-inspired plasticity into artificial synaptic devices, their dynamic operations are not entirely similar to biological function. Nevertheless, these dynamic behaviors are needed to enable neuromorphic operations seen in natural organisms [107,108]. Synaptic plasticity is often divided according to temporal dynamics related to synaptic strengthening into two primary classes: short-term plasticity (STP), which lasts from several seconds to several minutes, and long-term plasticity (LTP), which involves longer-lasting modifications . Moreover, repetitive stimulation can trigger switching from an STP to an LTP. Moreover, synaptic devices can be engineered to exhibit a wide range of synaptic phenomena, ranging from paired-pulse facilitation (PPF), a quintessential example of an STP, to spike-timing-dependent plasticity (STDP), and excitatory and inhibitory plasticity, where synaptic strengthening or weakening happens based on an external stimulus [109].

2.6.1. Short-term and long-term plasticity

Short-term plasticity (STP) is an important neural process exhibited as transient changes in synaptic conductance, creating a kind of temporary memory within synaptic connections. This process is characterized by the ability of synapses to customize their response to new stimuli, which leads to either an increase or a decrease of their output depending upon previous experiences. Through dynamic synaptic weight modulation over time, STP enables quick adaptation of the brain to new information [110]. Such fleeting adaptations are critical for learning during short periods, for attention-related processes, and memory consolidation, thus enabling projects toward emulating these features in neuromorphic systems using artificial synaptic devices.

Deswal et al. [111], in their "NbO_x-based memristor as artificial synapse emulating short-term plasticity," investigated the electronic simulation of this biological process. They proved that, under specific conditions, voltage pulses could cause temporary changes in the conductivity of the device. For example, significant increases in conductivity resulted when a series of 10 V pulses applied for 0.5 seconds each had intervening intervals of 2 seconds. However, delivering these same pulses using intervals of 10 or 20 seconds had no such effect. This phenomenon exactly parallels the analogous biological process in which proximate-timed stimuli increase learning. The same authors additionally proved that pulses spaced closely together could produce synaptic memory-

like phenomena such as paired-pulse facilitation and post-tetanic potentiation. Furthermore, it was revealed that increases in conductance due to repeated stimulation decayed over time by a slower process, thus imprinting memory of stimulating history upon the system. All these results provide strong evidence of emulation of short-term plasticity successfully and efficiently by electronic circuits built using specific materials systems beyond traditional synaptic models found in biology. Long-term potentiation (LTP) and long-term depression (LTD) are basic processes that ensure lasting synaptic plasticity. LTP is characterized by synaptic strengthening after prolonged stimulation compared to LTD, which involves synaptic weakening resulting from decreased or antagonistic synaptic activity. These two opposing processes together are the neurobiological basis for learning and memory processes. The reinforcement and long-term storage of information are related to LTP, while LTD is significant in eliminating redundant or irrelevant information as a means of enabling the system to process huge volumes of information efficiently.

In their article titled "Mimicking Synaptic Plasticity and Neural Network Using Memtranstors"[112] the author emulated biological phenomena by utilizing an innovative electronic device called the memtranstor. The memtranstor is built from multiple layers of ferromagnetic and ferroelectric materials, with magnetoelectric (ME) coupling between them, and a parameter called transtance enables information storage. Their experimental observations reflected phenomena characteristic of long-term potentiation (LTP) and long-term depression (LTD) through series of electrical pulses that caused increments or decrements, respectively, of memtranstor's ME voltage (VME). A series of positive pulses, for example, elicited reactions analogous to excitatory postsynaptic potentials (EPSPs) and caused an increase in VME to persist for a period long after the pulses had stopped, which is typical of LTP. Application of negative pulses caused a reduction of VME, effectively mimicking LTD. The linear correspondence between states of VME and numbers of pulses and stability of created states validated the device’s ability to model mechanisms related to long-term memory.

2.6.2. Spike-timing-dependent plasticity

Spike-timing dependent plasticity (STDP) is a biological learning principle where synaptic strength is altered by temporal relations between presynaptic and postsynaptic spike trains[113]. This principle states that if a presynaptic spike follows by a

postsynaptic spike, reinforcement is experienced by the synapse—a process called long-term potentiation (LTP)—leading to an increase in synaptic weight. On the contrary, if a postsynaptic spike precedes a presynaptic spike, synaptic effectiveness is decreased through a process called long-term depression (LTD). STDP is based fundamentally upon spike temporal differences to determine both the learning direction and magnitude and therefore represents a time-sensitive version of Hebb's learning rule.

In experiments conducted by Shen et al. [114], spike-timing-dependent plasticity (STDP) was successfully replicated using Ni/PMN-PT/Ni memtranstors. Under these experimental conditions, synaptic weight proved to be the magnetoelectric voltage (VME) of the memtranstor. Electrical pulses of a series were applied to mimic pre- and post-synaptic spikes, and time difference (Δt) between them controlled the applied overall voltage to the device.

The experimental parameters were outlined as follows:

- Each spike pulse had a duration of 10 milliseconds.
- Presynaptic action potentials were elicited by gradually increasing voltages from −1 V to −25 V.
- Postsynaptic spikes were rectangular pulses of +25 V and −25 V.
- The spike interval Δt was varied within limits from −90 milliseconds to +90 milliseconds.
- The test employed pre/post spike pairs of 1, 10, and 100 to look at different levels of interaction.

The electronic emulation of STDP was realized as when the presynaptic action potential preceded the postsynaptic action potential by a time interval Δt and the electrical impulses coincided within this timescale, the total voltage applied to the device exceeded the potentiation threshold (Vth_1), resulting in an increase of VME, which is a sign of long-term potentiation (LTP). If, on the other hand, the postsynaptic action potential came before the presynaptic one, the ensuing voltage exceeded the depression threshold (Vth_2), and a decrease in VME resulted, thus promoting long-term depression (LTD).

In addition to this time-sensitive emulation, a simplified STDP scheme was also tested. In this version, spike pairs consisting of two oppositely directed pulses with fixed amplitude and durations of 60 ms and 10 ms, respectively, were applied. It was observed that when the absolute value of Δt was less than 50 ms, the STDP effect consistently appeared. This result indicates that learning in such devices depends not only on the

timing between spikes but also on the number of repeated spike interactions. In conclusion, both the exponentially time-dependent and simplified forms of STDP were successfully emulated using memtransistor devices. These results demonstrate that the time-dependent learning behaviors observed in biological systems can be effectively reproduced in hardware through carefully designed electronic architectures.

3. EXPERIMANTAL TECHNIQUES

This sub-section provides the fabrication and characterization steps followed here. Monolayer MoS_2 was initially prepared through chemical vapor deposition (CVD). Device geometry was patterned using optical lithography, followed by metal deposition for contact formation. Electrical and optoelectronic characterization was performed for the analysis of device performance. Besides electrical characterizations, structural and optical characterizations such as atomic force microscopy (AFM), Raman spectroscopy, and photoluminescence (PL) spectroscopy were used to confirm the quality of the material and thickness of the layer. All the techniques were chosen to explain the physical and functional properties of memtransistors that were prepared.

3.1. Fabrication of Memtransistors

3.1.1. CVD growth of MoS_2

The synthesis of two-dimensional (2D) materials typically depends on two general methodologies: top-down methods like exfoliation[115], and bottom-up approaches, represented by chemical vapor deposition (CVD). Among the methodologies, CVD has emerged as a particularly effective method for producing large-area, high-quality 2D layers[116]. Although mechanical exfoliation can yield defect-free monolayers, its scalability is limited, making it less suitable for industrial-scale applications. Similarly, liquid exfoliation could lead to higher yields but often suffers from non-uniform thickness and smaller flake sizes. In contrast, CVD offers unique merits with regard to the synthesis of large-area films, reproducibility, and relatively low production costs. This technique involves the chemical reaction of vapor-phase precursors, either gaseous or solid, under controlled conditions to synthesize thin films on a substrate. The exact parameters, such as the precursor type, temperature, pressure, and carrier gas flow rates, have a significant influence on the quality and morphology of the product material. Considering that each 2D material (like graphene, MoS_2, and WS_2) has different behaviors during growth, it is necessary to optimize the CVD parameters based on each target material[18].

In the current research, monolayer MoS_2 flakes were synthesized by a thermal chemical vapor deposition (CVD) process in a single-zone quartz tube furnace. The fabrication process used solid precursors, which include molybdenum trioxide (MoO_3, Sigma-Aldrich, 99.5%) and sulfur powder (S, Sigma-Aldrich, 99.5%) [117].

The SiO_2/Si was oriented in a downward direction and placed immediately above a quartz boat filled with about 1 mg of MoO_3 powder. Another quartz boat filled with about 150 mg of sulfur powder was placed upsteam with a spacing of about 16 cm from the MoO_3. The entire system was purged periodicaly during the entire process with a constant supply of high purity nitrogen (N_2) gas flowing at a rate of 400 standard cubic centimeters per minute (sccm)[118].

The growth process included heating the MoO_3 zone up to 700 °C with a ramp rate of nearly 20 °C/min. The sulfur boat was initially kept at room temperature, slowly undergoing temperature elevation via natural convection as the furnace temperature increased. Upon maintaining the desired temperature for the MoO_3 precursor, sulfur vapor diffused in the reaction zone, enabling the nucleation followed by the growth of MoS_2 over the SiO_2/Si substrates. The system was kept at the set temperature for nearly 10 minutes with a subsequent phase of natural cooling under the flow of nitrogen. The methodology allowed for the synthesis of top-quality, contiguous, triangular monolayer MoS_2 flakes favorable for further fabrication of devices. Careful control of precursor weights, spatial arrangements, growth temperatures, and the carrier gas atmosphere was critical in achieving replicable results with a minimal occurrence of secondary phases or multilayer domains.

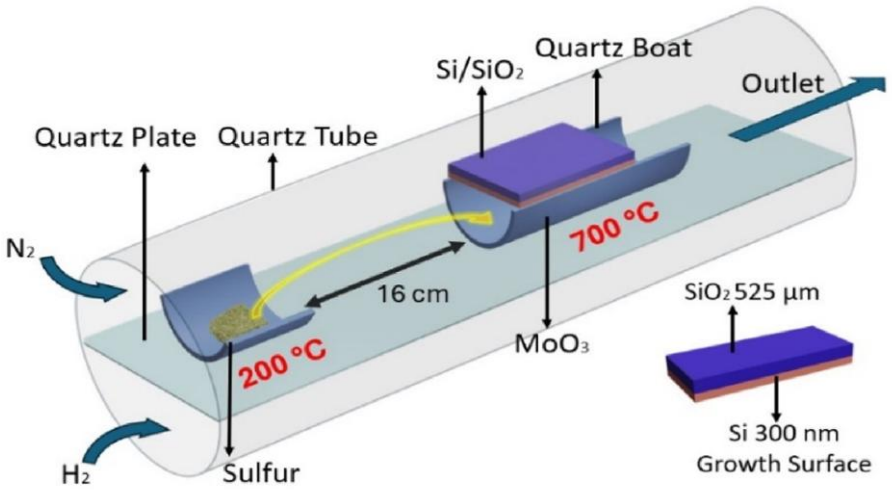

Figure 3.1. *Schematics of the growth zone of the CVD system.*

3.1.2. Optic litography

Photolithography is also known as optical lithography and is a basic microfabrication technology used for duplicating geometrical configurations onto a

surface of a substrate. The process involves coating the substrate with a photoresist, followed by exposure under ultraviolet light through a photomask possessing the desired pattern to finally form the patterned transfer.

One of the main advantages of the optical lithography is its fast processing, its cost-effectiveness, as well as its compatibility with large substrate areas, which qualifies it for both experimental studies and volume manufacturing. In spite of the resolution limitation by the wavelength of light used, the optical lithography is still a reliable method for the patterning of devices for the micrometer domain, such as transistors, sensors, and optoelectronic devices that utilize 2D material. The overall success of the lithographic process depends on a myriad of interdependent variables that include the material and thickness of the photoresist, the dose of exposure, the accuracy of the alignment, as well as the optimization of the development process. Careful control of these procedures ensures a high-fidelity pattern transfer, which is essential for the fabrication of functional and reproducible electronic devices.

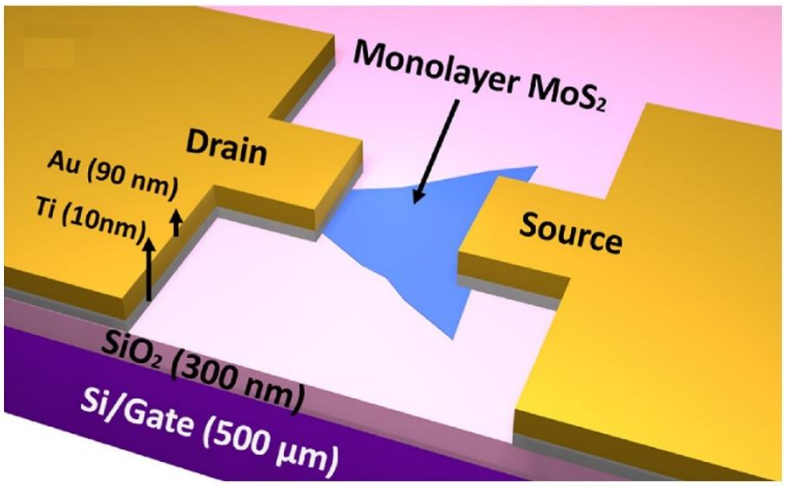

Figure 3.2. *Schematical representation of the fabricated MoS_2 based device*

After the synthesis of the monolayer MoS_2 flakes over the SiO_2/Si substrates, the regions for the drain and the source electrode were patterned using optical lithography. The fabrication process was carried out as follows:

Photoresist Coating: The substrate was spin-coated with a positive-tone photoresist (AZ5214) at 3000 rpm for 30 seconds, resulting in a uniform resist layer of about 1.5–1.6 µm thickness.

Soft Baking: The coated substrate was baked on a hot plate set at 110 °C for 60 seconds, allowing solvents to evaporate and promoting resist adhesion.

Mask Alignment and UV Exposure: With the help of an optical mask aligner, the patterned device was precisely aligned with the MoS_2 flakes. Then, ultraviolet exposure for 15 seconds using a 30 W ultraviolet light was carried out, which caused changes in the exposure regions of the photoresist.

Development: The substrate was immersed in a 1:4 DI water:AZ400K developer solution, dissolving the UV-exposed photoresist areas and revealing the patterned regions.

Metal Deposition: After patterning, a 5 nm-thick adhesion layer made of titanium (Ti) was deposited, followed by the thermal evaporation of a 100 nm-thick gold (Au) contact layer.

Lift-Off Process: The sample was soaked in acetone, removing the remaining photoresist along with any metal atop it. This left behind the desired electrode structures directly contacting the MoS_2 flakes.

The precise fabrication of back-gated MoS_2-based memtransistor devices with well-defined channel geometries, needed for further electrical and optoelectronic analysis, was made possible with the aid of optical lithography.

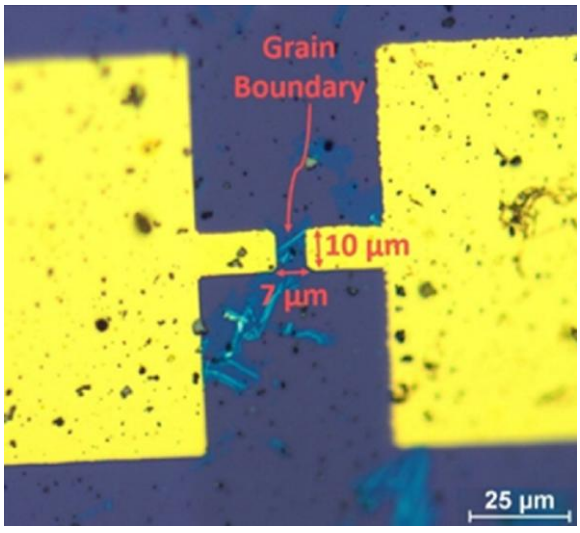

Figure 3.3. *Optical microscopy image of 7 µm channel length.*

3.2. Characterization Techniques of MoS_2 Memtransistors

3.2.1. Raman, photoluminescence spectrum and AFM

Raman and photoluminescence (PL) spectroscopy are widely used non-destructive methods used to examine two-dimensional materials regarding their crystallinity, thickness, doping concentration, and defect density. Raman spectroscopy works on the principle of inelastic scattering of monochromatic light, usually from a laser, in interaction with phonons or molecular vibrations in the material. For 2D materials such as MoS_2, the vibrational modes E_2g and A_1g are important markers of layer thickness, where the distance between these peaks increasingly varies from monolayer to multilayer structures.

Photoluminescence spectroscopy, by contrast, studies the light emitted by a material after laser excitation. For monolayer MoS_2, the photoluminescence spectrum often shows emission peaks related to neutral excitons (A and B), trions (A^-), and biexcitons (AA)[119], which correspond to different charge carrier recombination processes. The positions and relative heights of the peaks are indicators of optical quality and provide direct information about the level of doping and the presence of defects.

The combination of the two techniques reinforces the insight of the structural and optical properties of MoS_2-based devices. In this research, Atomic Force Microscopy, complemented with spectroscopic analysis, was used for the purpose of confirming the monolayer structure of the MoS_2 flakes. The AFM image, as shown in Figure 2(a), shows a triangular flake, with the associated height profile given in Figure 2(b), which shows a height of around 0.77 nm, which is consistent with the predicted result for monolayer MoS_2.

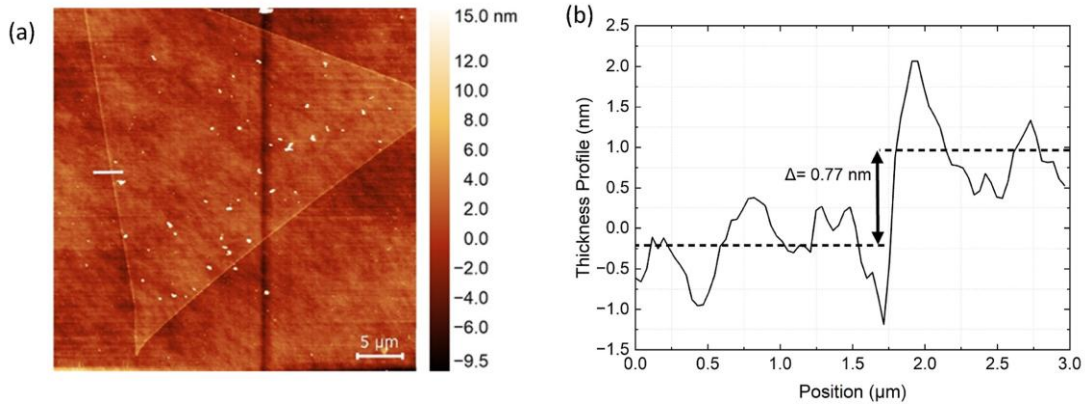

Figure 3.4. *(a): AFM image of monolayer MoS_2 flake. (b):The thickness profile of MoS_2*

The room temperature photoluminescence (PL) spectrum of the above-mentioned flake, excited by a 532 nm (2.33 eV) laser, is shown in Figure 3.5. The spectrum exhibits three main emission peaks that are recognized as the A-exciton, A^- trion, and B-exciton. By using Gaussian function fitting on the raw PL data, the peak energies were found to be 1.82 eV for the A-exciton, 1.83 eV for the A^- trion, and 1.97 eV for the B-exciton. The dominance of the A-exciton peak over the others suggests the presence of a high-quality monolayer structure, which is generally characteristic of pristine CVD-grown MoS_2 samples[120].

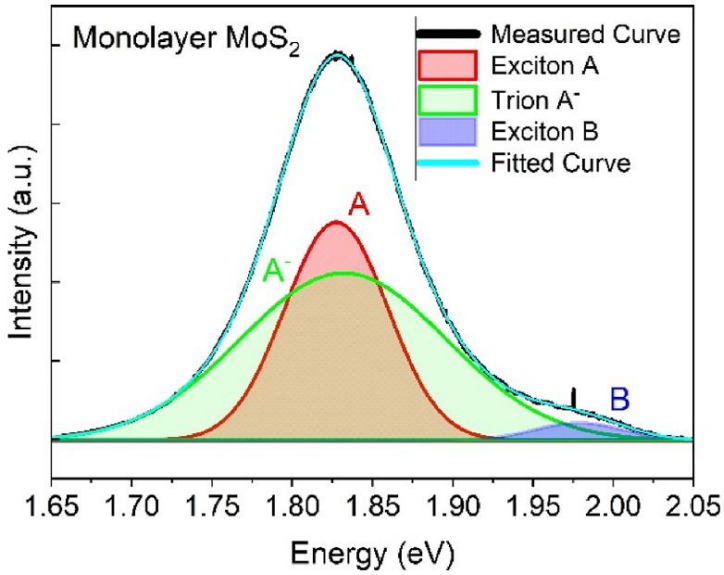

Figure 3.5. *PL spectrum with Gaussian fit of MoS_2*

Apart from the case of the photoluminescence (PL), Figure 3.6 shows two peaks whose positions are characteristic of the in-plane E_2g and out-of-plane A_1g vibrational frequencies. The two peaks are separated by a measured 17.9 ± 0.1 cm^{-1}, which is consistent with monolayer MoS_2 characteristics according to previously reported values[120].

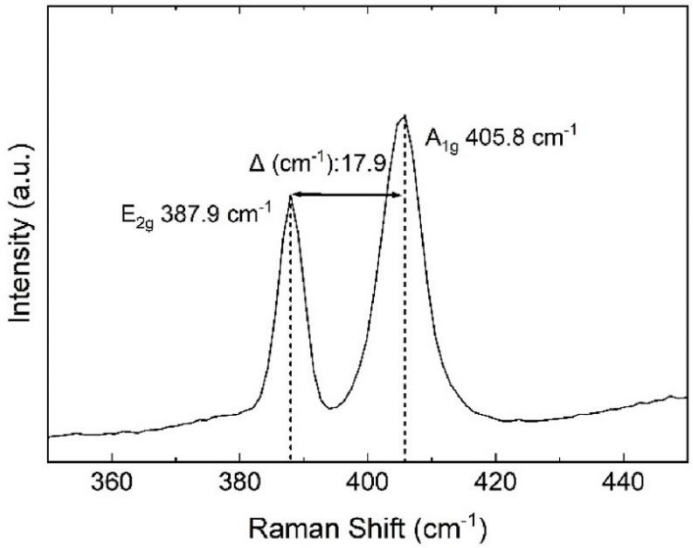

Figure 3.6. *Raman spectrum of mono-layer MoS_2*

3.2.2. Electrical characterization

The electrical characterization of memtransistor devices is critical for an understanding of their intrinsic operation mechanism. In particular, for 2D material-based devices like MoS_2 memtransistors, the process facilitates the identification of essential parameters like the hysteresis window, resistive switching, carrier transport mechanisms, and the impact of external factors like gate and drain voltages. Via the analysis of current-voltage (I–V) characteristics under different conditions (e.g., illumination, gate bias, and channel length), one is able to draw meaningful conclusions about the performance of the device for applications in neuromorphic computing and memory storage.

The electrical characteristics of the CVD-synthesized monolayer MoS_2 memtransistors with two different channel lengths of 15 μm and 7 μm under both ambient and dark conditions were thoroughly analyzed. The devices were fabricated using a typical back-gate field-effect transistor (FET) configuration with the Ti/Au contacts deposited over the Si/SiO_2 substrates. For the studies of the resistive switching (RS) characteristics, direct current current-voltage (DC I–V) measurements were made by varying the drain voltage from −5 V to +5 V with a constant gate bias of 50 V.

As shown in Figure 3.7(a), the 15-μm channel length device had a well-defined hysteresis loop in the linear-scale IDS–VDS plot, reflective of stable resistive switching (RS) behavior. The semi-logarithmic plot given in Figure 3.7 (b) also supports the fluctuation of current over many orders of magnitude. A similar analysis for the 7-μm

channel length memtransistor is described in Figure 3.7 (c) and Figure 3.7 (d), with the hysteresis loop much more prominent and with larger drain currents for the same scope of applied biases. The increased current with decreasing channel lengths can be related to the increased electric field within the active area, thus favoring efficient transfer of charges and mobility of defects.

Notably, the memristive properties arose without the need for an electroforming process, hence the simplification of operation and the reduction of fabrication complexity. Arrows in every subfigure represent the path of the voltage sweeps used (0 → +5 V → 0 → –5 V → 0). The results validate the reversible resistive switching characteristics of the devices without the application of external forming protocols.

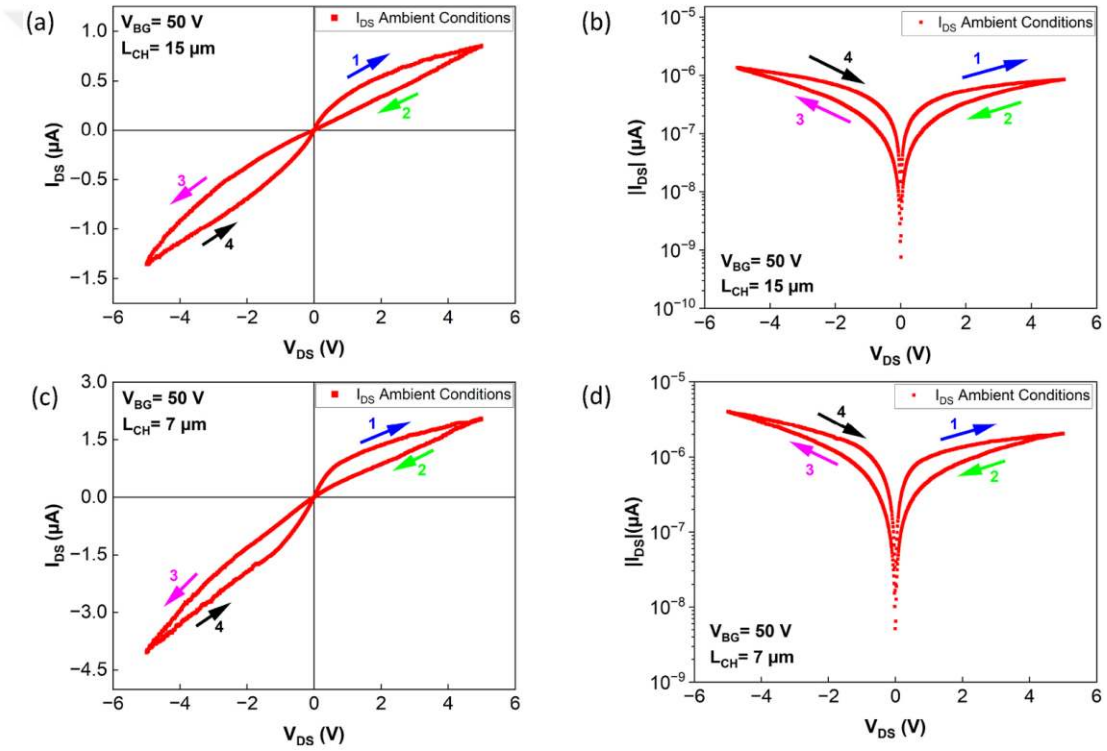

Figure 3.7. *Chemical Memtransistor I_{DS}-V_{DS} characteristics measured under ambient conditions. All plots were acquired with a drain-to-source voltage range of 5 V–5 V, V to 50 V, and a channel width of 10 µ m. Plots (a) and (b) correspond to L CH =15 µ BG set m, with (a) presented on a linear scale and (b) on a semi-logarithmic scale. Plots (c) and (d) correspond to L CH = 7 µ m, with (c) presented on a linear scale and (d) on a semi-logarithmic scale. of paracetamol.*

The photocurrent contribution was evaluated by studying the current-voltage (I–V) characteristics under both dark and illumination conditions for the 7 µm device, as shown in Figure 3.8 (a)–(b). In dark conditions, a symmetrical hysteresis loop is confirmed even under a gate bias of 0 V, which proves the capability of memristive functionality maintenance by the drain bias alone. In contrast, when under illumination, symmetry is

broken, which is due to the contribution of photoexcited carriers to the entire current. The result proves that MoS_2-based memristors are light-sensitive hybrid devices with both photonic as well as electronic switching functions.

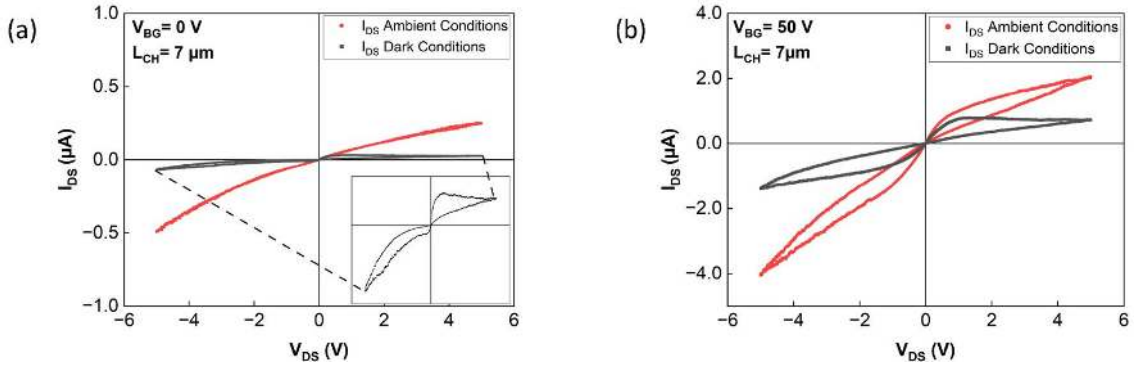

Figure 3.8. *I_{DS}-V_{DS} characteristics under ambient and dark conditions with a channel length of L_{CH}=7 µm. All graphs are obtained under a drain-to-source voltage range 5 V–5 V, with (a) at V_{BG} = 0 V and (b) at V_{BG} = 50 V, both plotted on a linear scale.*

A comparative analysis of the effects due to channel length and gate voltage is shown in Figure 3.9 (a)–(e). The I_{DS}–V_{DS} characteristics measured at V_{BG} values of 0 V, 25 V, and 50 V for the device with a 7 µm channel length are shown in Figure 3.9 (a)–(c). The increase in the gate voltage led to higher current levels as well as broader hysteresis loops, indicating an improvement in channel conductivity. Figure 3.9 (d) and Figure 3.9 (e) compare the electrical performance of the devices with 15 µm and 7 µm channel lengths at fixed gate biases. The device with the shorter channel length consistently showed higher drain currents, supporting the argument that a decrease in channel length enhances the electric field across the MoS_2 flake and promotes the migration of sulfur vacancies, a mechanism known to be responsible for the resistive switching phenomena in MoS_2-based memtransistors.

In the absence of gate bias, the two devices both displayed hysteresis, though at lower current densities. The observation reaffirmed the presence of memristive action irrespective of gate control. The results clearly demonstrate the critical impact of channel geometry, gate modulation, and intrinsic defect dynamics in the devices' operation.

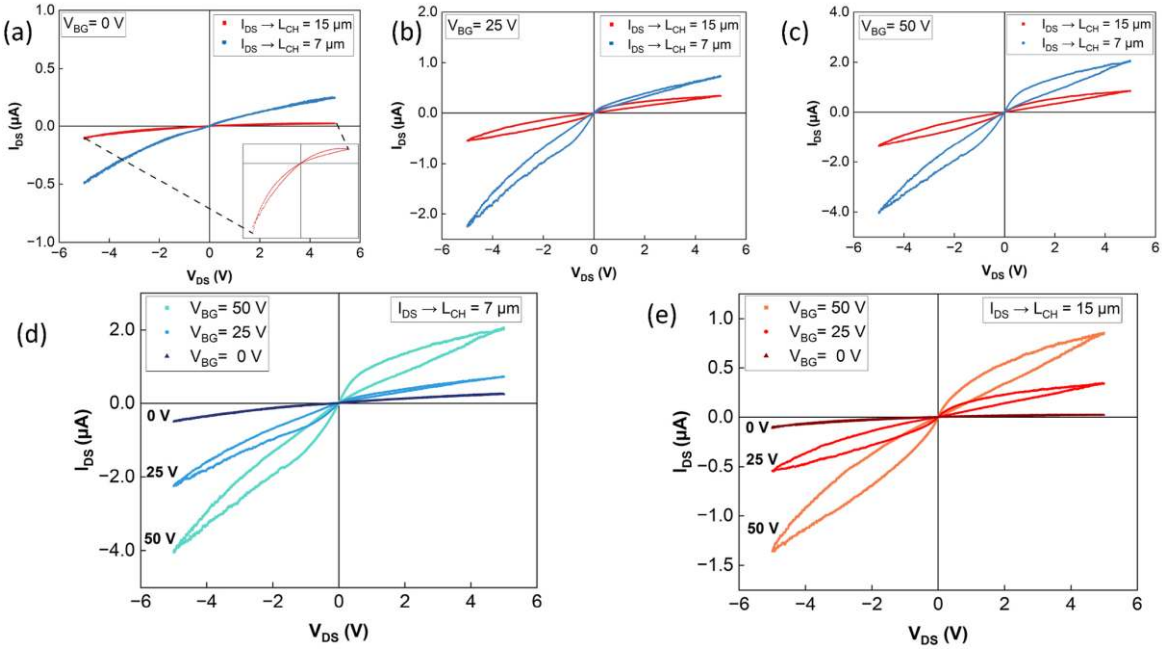

Figure 3.9. *The impact of different gate voltages (V_{BG}) on memtransistors with a channel length of 7 µm. Specifically, (a) V_{BG} = 0 V, (b) V_{BG} = 25 V, and (c) V_{BG} = 50 V. Similarly, subplots (d) and (e) compare the I_{DS}-V_{DS} curves for memtransistors with the same channel lengths (15 gate voltages at ambient conditions.)*

In their studies of the mechanisms responsible for memristors, Hersam and colleagues suggested a theoretical model revealing that grain boundaries and sulfur vacancy diffusion are essential for the creation of a low-resistance conduction channel, which enhances the induced resistive switching of such devices[20]. In the course of such analysis, different grain boundary orientations, namely, intersecting, bridging, and bisecting—were characterized, with the focus lying in the vital role sulfur vacancies forming around such domains play in triggering resistance modification. Later, in a 2018 publication, the same research group put forward an alternative mechanism of operation for a different memtransistor configuration [13]. Such a model suggested that polycrystalline MoS_2 with a large density of sulfur vacancies behaved as the dynamic medium that allowed such vacancies to move along the grain boundary under an external electric field. The vacancy displacement permitted the formation of Schottky barriers across the interfaces of the MoS_2 with the metal electrodes, leading to resistance fluctuations. With great efforts made to achieve a better grain boundary alignment within a bridging configuration during the fabrication of devices, slight misalignments remained unavoidable, especially when channels of different lengths are fabricated from the very same flake.

It is widely accepted that both grain boundaries and sulfur vacancies are the primary factors responsible for resistive switching in memtransistors[19][121]. In our earlier work, we performed DFT calculations alongside controlled aging experiments. Our findings showed that sulfur vacancy defects play a dominant role in the switching behavior, and that reducing these defects—by optimizing the growth rate—can significantly improve the long-term stability of monolayer MoS_2 films [122].

The rising need for efficient handling of both data processing and storage, along with the limitations in conventional von Neumann architecture, is fueling a renewed interest in neuromorphic computing. The novel methodology is based on the functional structure of the human brain, which supports simultaneous handling and storage of information through a single architecture[123]. The basic distinction between the functional components and the memory components in conventional architecture creates a strong limitation in terms of communication. Neuromorphic computing overcomes the limitations by emulating the human brain's structural aspects, thus supporting the execution of the functionality with improved efficiency[124]. In this regard, memtransistors have emerged as the most viable options to overcome the von Neumann bottleneck, as simulating synaptic weights is a critical functionality necessary for neuromorphic hardware.

3.2.3. Synaptic emulation

In addition to exhibiting basic memory properties, MoS_2 memtransistors also exhibit the capability to mimic synaptic functions, an essential feature for neuromorphic computing. In the synapses of living organisms, synaptic weight changes via activity-dependent plasticity are a main factor in the process of learning and memory. Memtransistors mimic this effect by changing their channel conductance continually with external voltage stimuli.

Figure 3.10 (a) and Figure 3.10 (b) show the results of the pulse tests carried out to explore the dynamics of STP in the fabricated devices. In Figure 3.10 (a), 10 consecutive positive voltage pulses with an amplitude of +5 V and a pulse width of about 25 μs were applied to a memtransistor with a channel size of 7 μm. After each successive application of a pulse, the increase in the output current was noted, marking the existence of the potentiation phenomenon. Similarly, Figure 3.10 (b) shows the response of the device to a series of negative voltage pulses with the amplitude of −5 V. Interestingly, following

repeated stimuli, an increase in the basal current was realized, exhibiting a phase delay effect in which the return current did not immediately return to its previous level. The phase delay behavior is a commonly known phenomenon in memristive devices, with ion migration playing a pivotal role.

The basic process is attributed to the sulfur vacancy or ionized defect complex dynamics in the MoS_2 channel, which are induced by electrical pulses. With repeated occurrences of such pulses with poor recovery intervals, the movable species are unable to return to their starting positions, causing an increase in current.

Additionally, this process is in line with the concepts of Hebbian learning, which state that a decrease in the temporal gap between pre-synaptic and post-synaptic events strengthens the synapse. As a result, the induced potentiation demonstrates the capability of such devices to mimic spike-timing-dependent plasticity (STDP), a basic process in neuromorphic networks.

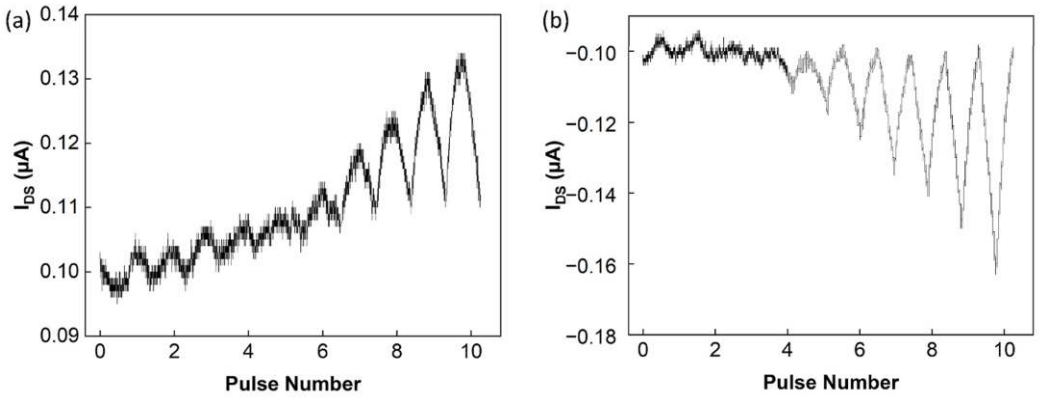

Figure 3.10. *I_{DS} current characteristics obtained by consecutive pulses to simulating presynaptic pulse stimuli: (a) + 5 V, (b) – 5 V of amplitudes.*

3.2.4. Effects of channel length on device performance

Channel length represents a key geometric parameter that influences the electrical properties and synaptic function of memtransistor devices. In 2D material-based transistors, reducing the channel length generally results in the enhancement of drain current due to the shorter carrier transport path and increased strength of the electric field.

In the present investigation, a detailed analysis of the electrical characteristics of MoS_2 memtransistors with channel lengths of 7 and 15 μm (see Figure 3.9) was carried out. Shorter channel devices exhibited:

- Increased output currents under the same gate and drain bias conditions.

- Broader hysteresis windows imply a higher occurrence of charge trapping and defect movement.
- And enhanced asymmetry under illumination, attributed to the stronger effect of photo-generated carriers interacting with localized states.

The enhanced hysteresis characteristics in short-channel devices indicate an increased effect of defects and interface states, which can act as reservoirs of ions when an electric field is applied. The above characteristics are beneficial for the application of memristive and synaptic devices, for which careful control over the conductance is essential.

- However, overly short channel lengths can lead to negative effects, such as:
- Increased leakage currents
- Reduced ON/OFF ratios
- And device instability due to excessive defect-mediated conduction pathways.

Therefore, it is critical to carefully examine the optimum balance between channel length, operation voltage, and stability of the device in MoS_2-based memtransistor devices for practical applications in neuromorphic computing and memory.

3.3. Fabrication of Titanium Carbide Memristors

3.3.1. Atomic layer deposition

Atomic Layer Deposition (ALD) is a method for thin-film deposition that enables precise and regular build-up of layers. This process was originally suggested by Tuomo Suntola and his colleagues in the early 1970s. The original name for this process was Atomic Layer Epitaxy (ALE), with emphasis on the inherent nature of the growth one layer at a time. The essence of ALD is based upon a sequence of chemical reactions that employ a minimum of two different precursor gases. These gases are fed into the reaction chamber in a highly controlled cyclic manner. Each cycle aims to deposit one atomic layer on the surface.

Since the process is conducted in a step-by-step manner, the film thickness can be efficiently controlled by adjusting the number of cycles. The major parameters that control the process are the length of precursor pulses, the purging time, the reaction waiting time, and the range of thermal and pressure variables. These parameters can be optimized for a given material and its application.

The ALD cycle includes the following steps:

1. The first precursor (usually a non-metal gas) is pulsed into the chamber and reacts with the surface.
2. Unreacted gas and by-products are removed by purging with an inert gas.
3. The next precursor, typically a metal compound, is introduced to react with the residual surface species.
4. Another purge step follows to clean the chamber again.

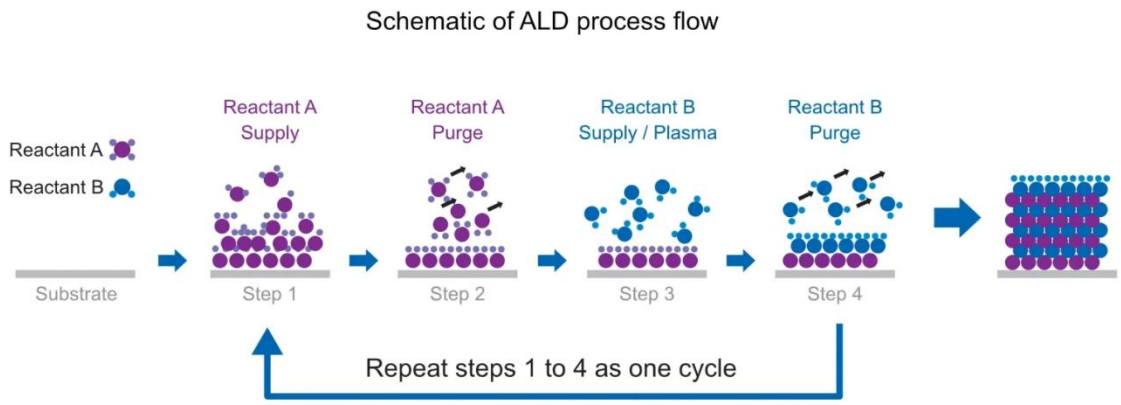

Figure 3.11. *Schematic of ALD process flow [125]*

The above steps are repeated until the desired thickness is obtained. The thickness increment per cycle generally ranges between 0.1 Å and 1 Å, depending on the particular reactor and the process temperature. The duration of a single cycle ranges from a few seconds to several minutes.

Figure 3.11. show the working steps of ALD in detail. First, the initial precursor sticks to the surface. Then the system is purged to clean it. The second precursor is added and reacts with the surface. After the final purge, the surface is ready for the next cycle.

ALD has several important advantages:

- Precise thickness control
- Ability to grow multilayers
- Low contamination
- Outstanding consistency due to its self-regulating nature.
- Outstanding reproducibility
- Dense and smooth films
- Capability to deposit at low temperatures

- High conformality for 3D and high-aspect-ratio structures

Thanks to these advantages, ALD is widely used in advanced technologies such as integrated optical circuits and nanoscale optoelectronic devices.

3.3.2. PEALD growth of titanium carbide

The first MXene material was produced in 2011 by Naguib et al. at Drexel University. They produced it through selective etching away of the aluminum (Al) layers from a MAX phase compound, i.e., Ti_3AlC_2, with hydrofluoric acid. Upon this etching, the resulting layered material was termed MXene, where "M" is a transition metal (e.g., titanium), "X" is carbon and/or nitrogen, and "Tx" is the surface termination groups like –OH, –O, or –F. The general formula for the MXenes is $M_{n+1}X_nTx$, where n = 1, 2, or 3. MXenes' structure consists of metal and carbon atoms as layers stacked together, a form of two-dimensional (2D) lattice. In the case of Ti_3C_2Tx, the structure consists of three layers of titanium alternately with two layers of carbon between them, and the resulting structure is a Ti–C–Ti–C–Ti sequence. MXenes are present as thin sheets stacked one over the other in cross-section, more of a sandwich structure. Such unusual architecture makes the MXenes extremely electrically conductive, flexible, and with a large surface area, making them a possible candidate for a variety of applications.

To obtain the MXene structure, a plasma-enhanced atomic layer deposition (PEALD) system with nine steps was used. In the first step, the titanium precursor $TiCl_4$ is introduced into the reaction chamber to uniformly coat all available surfaces. Then, an N_2 purge is applied to remove any unreacted or weakly bonded $TiCl_4$ molecules. To further clean the chamber, the pressure is reduced (pump-down step). The remaining $TiCl_4$ layer is then exposed to hydrogen plasma, which removes chlorine atoms from the surface, leaving behind a single layer of titanium atoms. Excess Cl, HCl, and H_2 are flushed away using nitrogen gas. After another pump-down, the titanium layer is exposed to methane (CH_4) plasma, allowing carbon atoms to deposit and bind to the titanium. In the ninth step, a final nitrogen purge and pump-down are applied. To approach the Ti_3C_2 MXene structure, one more titanium layer is deposited on top. Due to the nature of the ALD process, the resulting structure is initially amorphous. Therefore, a high-temperature annealing process is necessary to achieve a crystalline MXene phase. In this study, some parameters were kept constant while one parameter was varied to observe its effect on MXene formation. Different experimental sets were carried out under various annealing

temperatures and gas atmospheres. One of the key parameters studied was the exposure time to methane plasma. This step must be carefully optimized, as excess carbon between titanium layers can hinder the formation of the desired MXene crystal structure.

$TiCl_4$ precursor injection: $TiCl_4$ gas is introduced into the reaction chamber to coat all exposed surfaces.

N_2 purge: Nitrogen gas is used to remove any unreacted or loosely bonded $TiCl_4$ molecules from the chamber.

Pump down: The pressure is reduced to eliminate remaining nitrogen and prepare for the next step.

H_2 plasma exposure: The surface is exposed to hydrogen plasma to remove chlorine atoms, leaving behind a single layer of titanium.

Exhaust removal: Excess Cl, HCl, and H_2 are removed from the chamber using nitrogen flow.

Second pump down: The pressure is reduced again to clean the chamber before carbon introduction.

CH_4 plasma exposure: Methane plasma is applied to deposit carbon atoms onto the titanium layer.

Final N_2 purge and pump down: Nitrogen is used to purge the chamber, followed by pressure reduction to remove residual gases.

Additional Ti layer deposition: One more Ti layer is deposited to form a Ti–C–Ti sandwich structure that resembles the early stage of Ti_3C_2 MXene.

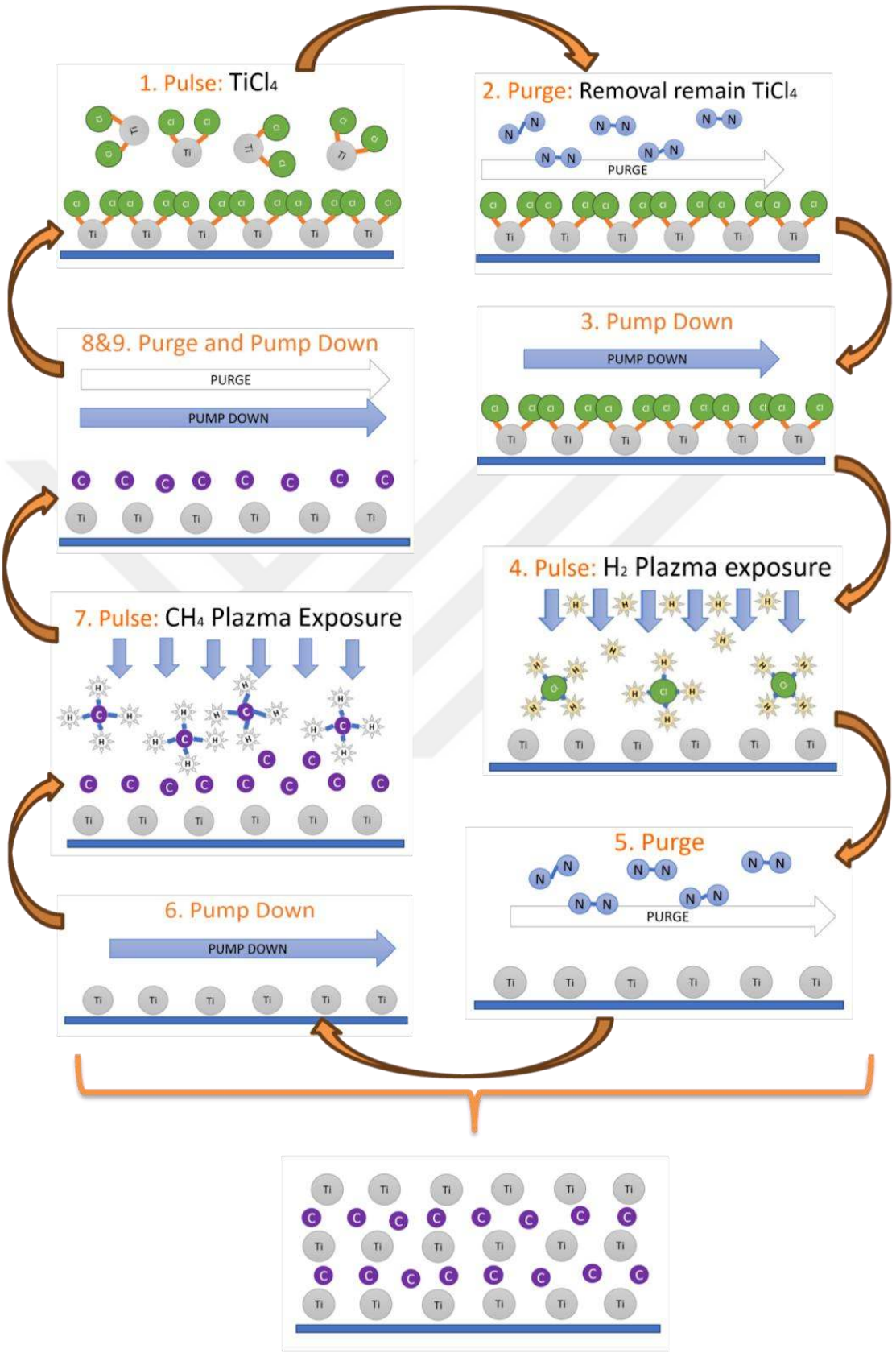

Figure 3.12. *Schematic of PEALD process flow to Titanium Carbide thin film growth*

In order to observe the effect of the exposure time to methane gas plasma, all parameters were kept constant and the duration of exposure to methane gas was kept variable. Because the amount of carbon to be deposited between the Titanium layers will play an important role in matching both the Mxene structure and the stoichiometric ratio (Figure 3.13). At the same time, this system offers versatile opportunities in terms of defect engineering in memristor production. Depending on the resistance and working mechanism, it is possible to dope with different layers and even create oxide layers in between. The durations of exposure to methane gas were determined as 0.5 seconds, 2 seconds and 10 seconds, respectively. The coating was carried out with 70 cycles. In order to observe the effect of the growth effect on the substrate selection, 4 different substrates were selected. These were titanium and copper foil, silicon and silicon dioxide (100) substrates.

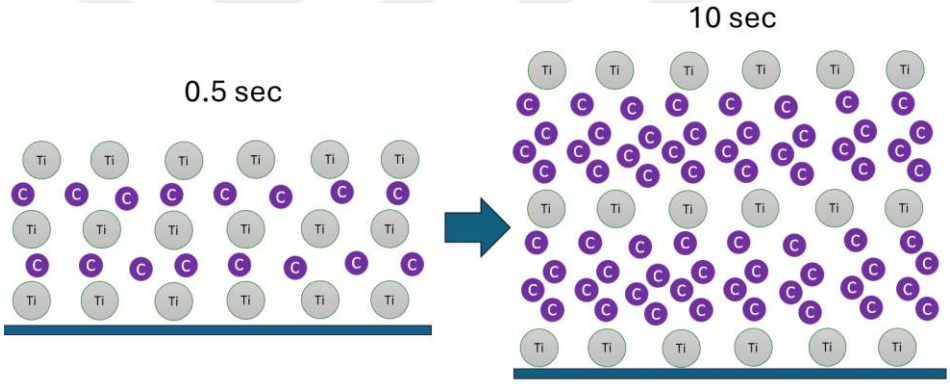

Figure 3.13. *Schematic representation of the effect of changing the exposure time to methane plasma on the amount of carbon deposition.*

Since the obtained structures are amorphous. The samples were annealed to obtain crystal structures. Annealing was carried out at 100 sccm for one hour in a hydrogen environment at 700 degrees Celsius, and in an argon environment at 700 and 1000 degrees. The 100x optical images of the obtained results (for copper substrates) are as in (Figure 3.14).

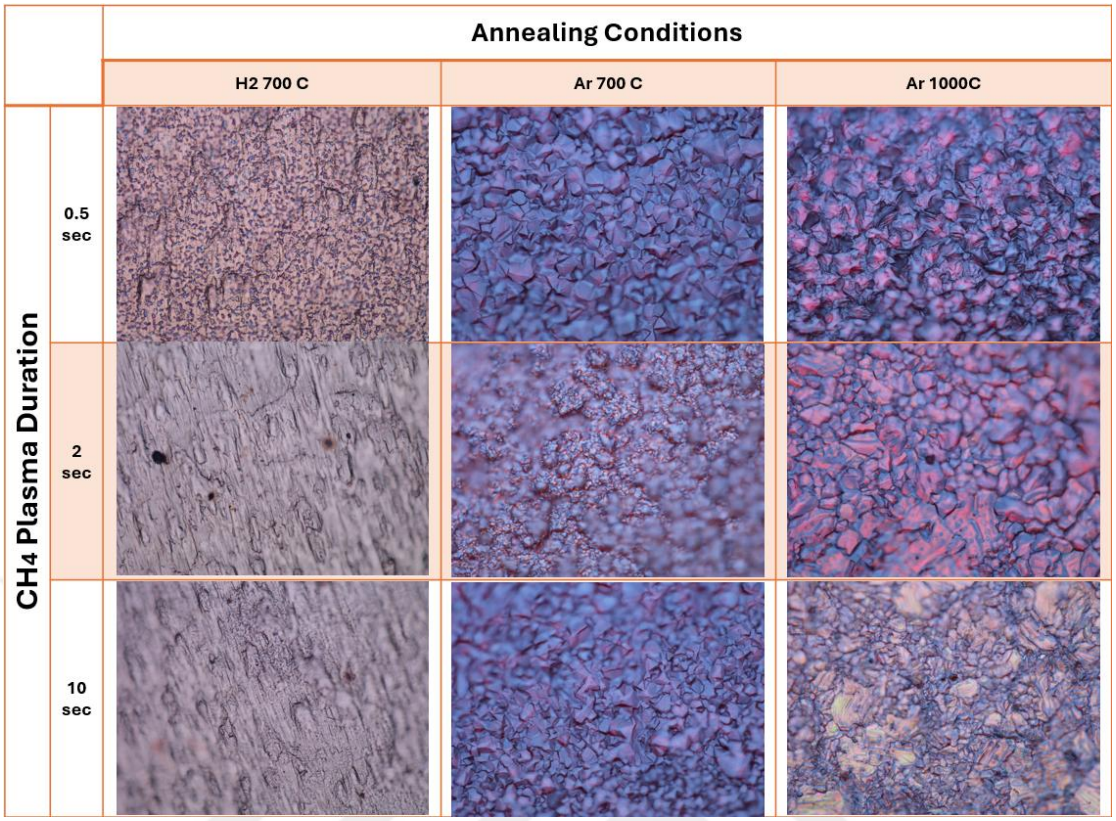

Figure 3.14. *Optical images of annealing conditions on copper substrates*

3.3.3. Thermal evaporator: building top electrodes

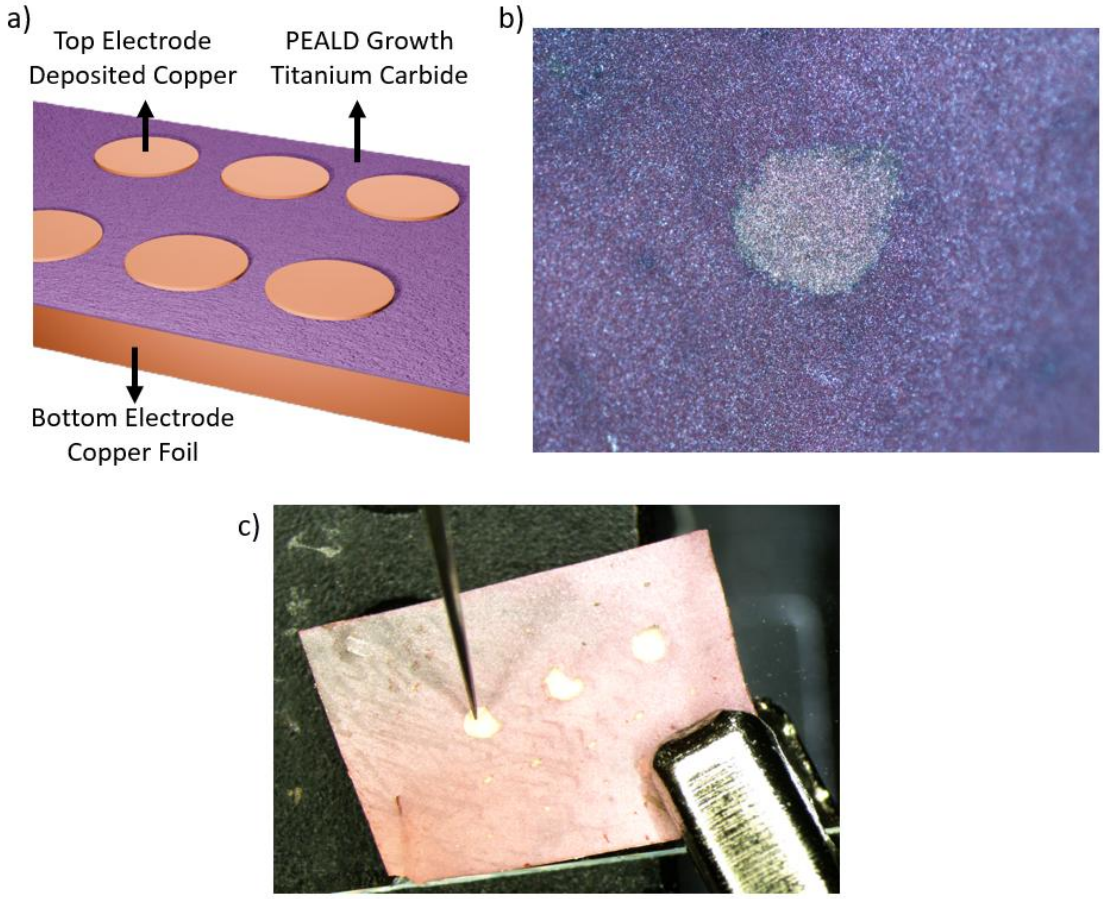

Figure 3.15. *Vertical structure titanium carbide memristor a) schematic, b) optical image c) Probe station*

In the current study, copper (Cu) was used as the electrode material, deposited over a titanium carbide (TiC) layer as in Figure 3.15. The use of copper offers many benefits relative to the application of interest. First, it has an outstanding electrical conductivity, which helps to minimize the total series resistance of the device, thus ensuring efficient transmission of the current. In addition, the work function of Cu, around 4.65 eV, is close to that of TiC, which typically ranges between 4.6 and 5.0 eV. This similarity improves the chances of forming an Ohmic contact rather than a Schottky barrier, ensuring a more linear I–V characteristic and lower contact resistance. Copper also exhibits desirable adhesion to a broad range of surfaces, including ceramic-based materials like TiC, and can be easily deposited using common methods such as sputtering or thermal evaporation. Its relatively low cost and availability make it a practical choice for experimental designs. However, some factors must be considered, including Cu's tendency to oxidize following exposure to ambient atmosphere, leading to increased

contact resistance. In addition, Cu atoms have the potential to diffuse into the substrate layers with extended periods of operation or under thermal stress, which may enhance memristive behavior however potentially affecting device stability.

3.4. Characterization of Titanium Carbide Memristors

3.4.1. SEM, XRD, Raman

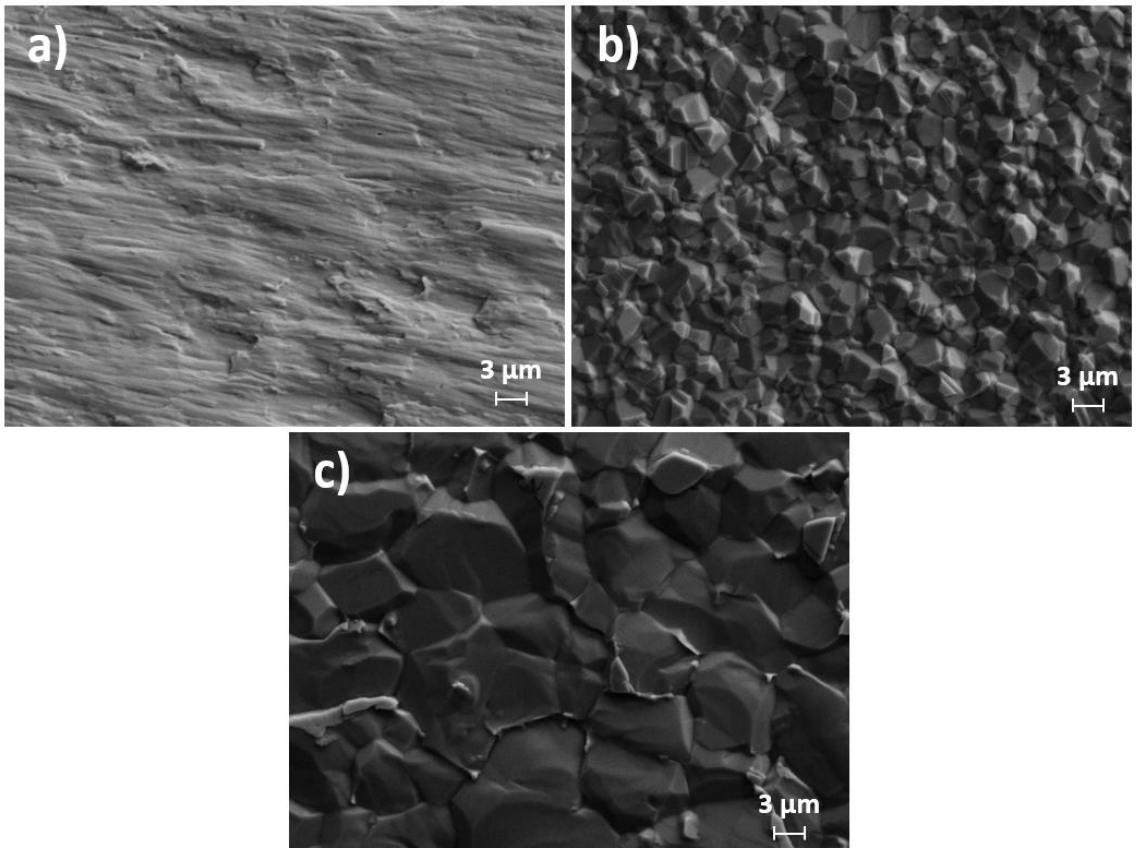

Figure 3.16. *SEM images of Titanium Carbide growth experiments exposed to CH_4 plasma for 2 seconds and different annealing conditions a) H_2 700 °C, b) Ar 700 °C, c) Ar 1000 °C.*

Figure 3.16 presents the SEM images of copper substrates that were exposed to CH_4 plasma for 2 seconds, followed by annealing under different atmospheric conditions. In the experiments conducted under an argon atmosphere, the formation of copper oxides was observed. The crystalline structures visible in the SEM images are primarily attributed to these copper oxide phases. This oxidation is likely a result of residual oxygen or trace impurities in the argon gas, which can lead to the formation of CuO or Cu_2O during high-temperature annealing[126].

In contrast, annealing carried out in a hydrogen environment did not result in such oxidation. Hydrogen, acting as a reducing gas, effectively suppressed the formation of copper oxides, thereby maintaining the metallic state of the substrate.

This interpretation is further supported by the XRD analysis presented in Figure 3.17, where samples annealed in argon exhibit diffraction peaks characteristic of copper oxide phases. On the other hand, the sample annealed in a hydrogen atmosphere shows diffraction peaks (43 °, 50 °, 74 °) corresponding to the cubic crystal structure of titanium carbide (TiC), suggesting successful conversion into a crystalline carbide phase under reducing conditions[127].

However, no clear evidence of typical MXene phase peaks was detected in the XRD pattern, indicating that the structure may not exhibit (in the region between 6–9°) the expected layered morphology of $Ti_3C_2T_x$ MXene[128].

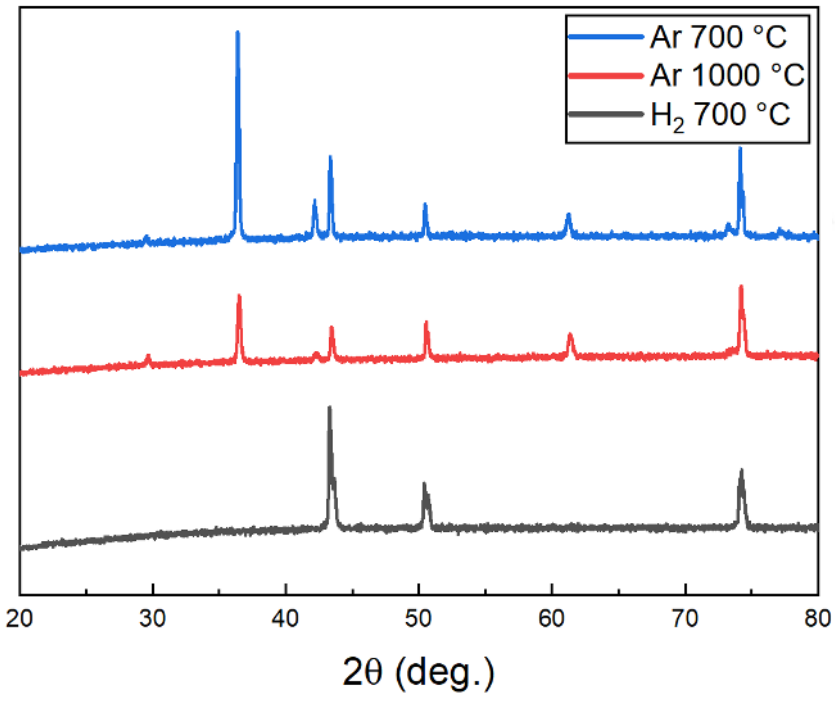

Figure 3.17. *XRD measurements of post-annealing experiments (CH_4 plasma for 2 sec.)*

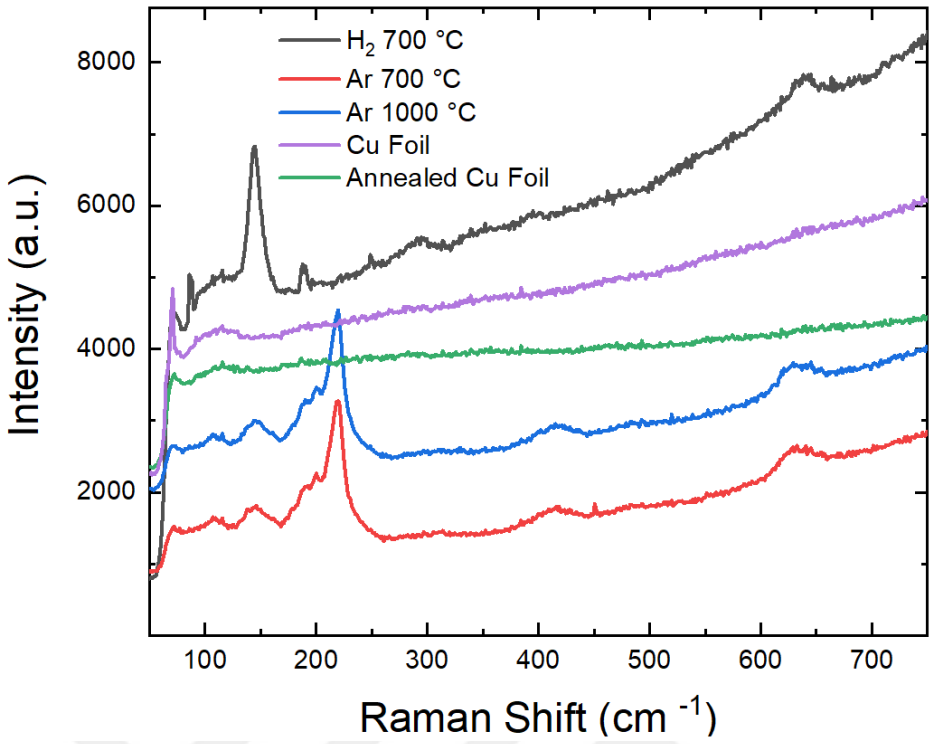

Figure 3.18. *Raman spectra of Titanium Carbide growth experiments exposed to CH_4 plasma for 2 seconds and different annealing conditions.*

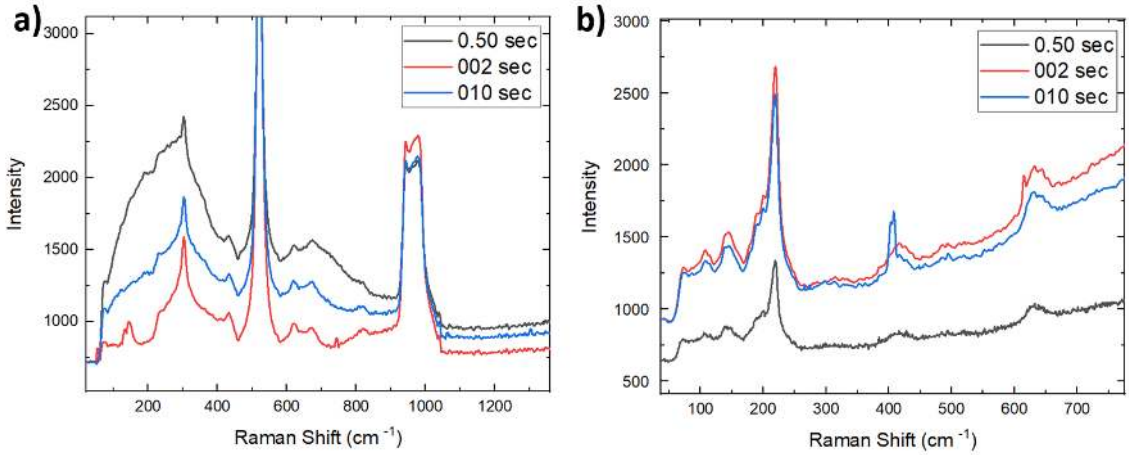

Figure 3.19. *Effect of changing the CH_4 plasma exposure time on the same substrates and the same annealing conditions.*

Raman spectroscopy is a widely used method to study the structural and vibrational properties of 2D materials such as MXenes. In this study, Ti_3C_2Tx thin films were analyzed using Raman spectroscopy, and the results were compared with previous findings in the literature.

According to Sarycheva et al. [129], Ti_3C_2Tx MXene shows several characteristic Raman peaks. These include a resonance peak around 120–125 cm^{-1}, attributed to

plasmon interactions, and vibration modes such as A_1g (Ti, C, Tx) near 200–210 cm^{-1}, Eg (Tx groups like –O, –OH, –F) between 366–506 cm^{-1}, and A_1g (C) vibrations around 710–740 cm^{-1}. Additionally, D (~1380 cm^{-1}) and G (~1600 cm^{-1}) bands are often observed due to carbon impurities or graphitization effects.

In another study, L. Wang et al. [130] identified peaks at 149, 268, 403, and 608 cm^{-1}, with the 608 cm^{-1} peak specifically associated with carbon atom vibrations in Ti_3C_2Tx. Similarly, Kaipoldayev et al. [127] reported that Raman peaks around 263, 325, 456, and 665 cm^{-1} are related to TiC formation, especially at high substrate temperatures. They also found that a substrate temperature of 450 °C is optimal for well-crystallized TiC, confirmed by both Raman and EDS analysis.

In our study, several Raman features were observed that agree with and complement the literature. Notably: The resonance peak at 120–125 cm^{-1}, commonly reported by Gogotsi[129] , was not clearly detected in our measurements. This peak is often observed using longer excitation wavelengths (e.g., 785 or 633 nm), which were not used in our setup.

Clear peaks were observed at 140, 185, and 207 cm^{-1}, consistent with flake vibration modes involving Ti and C atoms [129]. The 140 cm^{-1} peak showed a linear trend with certain processing parameters.

A broad band ranging from 240 to 450 cm^{-1} was detected. This range includes contributions from surface functional groups (e.g., –OH at ~383 cm^{-1}, =O at ~379 cm^{-1}) and may overlap with Raman features of cubic TiC [127]. The lack of a sharp peak at ~300 cm^{-1} on Si/SiO_2 substrates is likely due to signal interference from the strong silicon peak in this region.

In the 550–740 cm^{-1} range, distinct peaks around 620 and 670 cm^{-1} were identified. These are attributed to in-plane (Eg) and out-of-plane (A_1g) carbon vibrations between titanium layers [129].

A weak Raman band at 855 cm^{-1} was observed in samples processed via ALD and experiments. This peak is likely associated with TiO_2 formation.

The D and G bands (~1350 and ~1600 cm^{-1}, respectively) were detected and are generally linked to graphitic carbon structures, carbon shells, or contamination[129]. However, a strong correlation with processing parameters was not observed.

A comparative analysis of samples deposited on different substrates showed that the 240 cm^{-1} TiC peak was suppressed or hidden by the strong 300 cm^{-1} silicon-related

band on Si/SiO_2, while it was clearly resolved on Ti foil. These findings were supported by additional measurements on bare Si substrates, which showed strong peaks at 300, 520, and 900 cm^{-1} due to the substrate itself.

Overall, our Raman results are in good agreement with the literature, while also providing new insight into peak behavior depending on the substrate and processing method. These findings will guide the optimization of Ti_3C_2Tx film quality and structural control in future experiments.

3.4.2. Electrical characterization

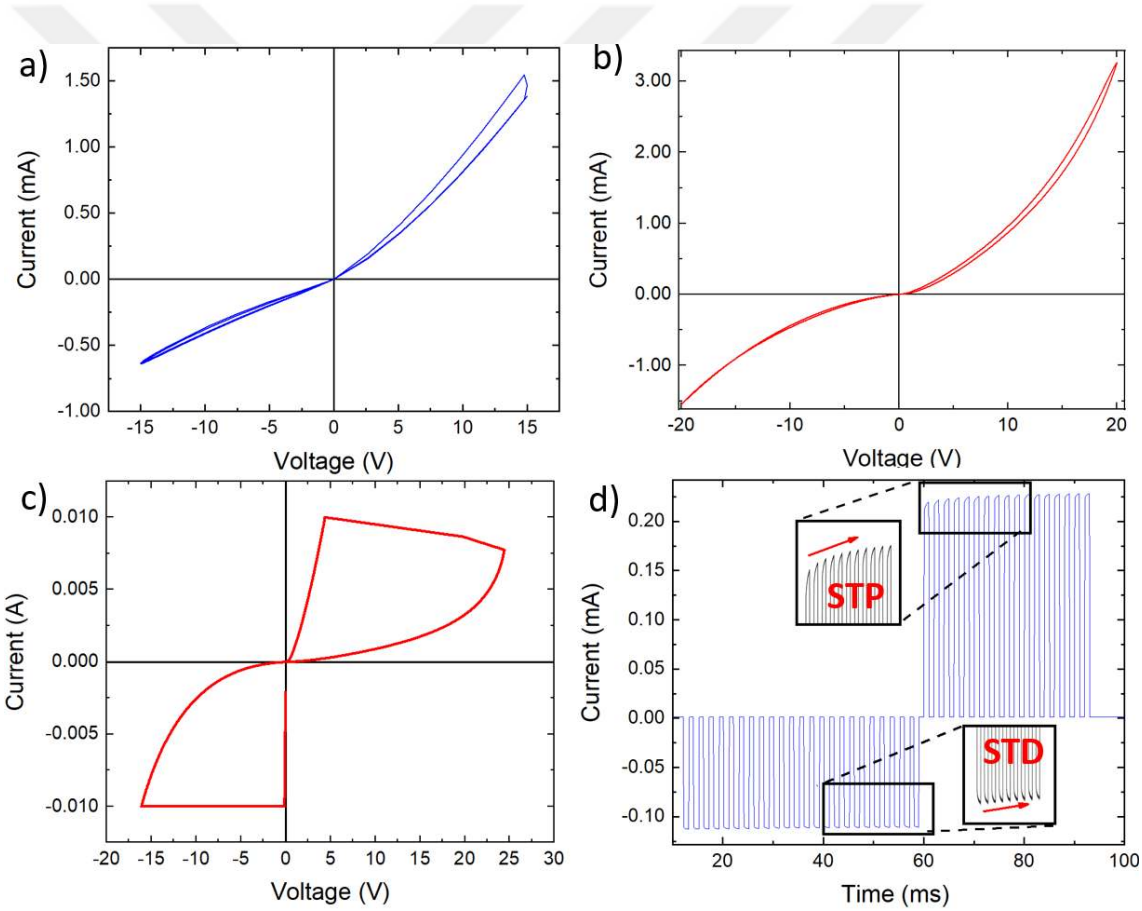

Figure 3.20. *a) Pinched hysteresis loop observed when a sinusoidal wave is applied to the memristor. b) DC characterization I-V graph. c) When a current above 25 V is applied, the memristor enters a short-circuit state and enters a very low resistance state. d) Short-term depression and potentiation behavior with successive pulses applied to the memristor.*

Their synaptic and electrical properties have been confirmed by various measurements. The pinched hysteresis loop, one of memristive circuits' basic characteristics, was

confirmed by applying a sinus voltage to the device. On its I–V response measurement, its path changes and crosses the origin, and thus exhibits a looped path Figure 3.16 a), such that the device "remembers" its applied voltage history. As this way was proven, this phenomenon confirms that the device's resistance varies corresponding to the voltage history from the input, one among ideal memristors' basic features.

To gain additional insight on the electrical characteristics, a DC voltage sweep was applied to the device Figure 3.16 b). The thereby-wrought I–V curve exhibited an undeniable nonlinear relationship between current and voltage. The current increased significantly while the voltage was increasing, which showed that the resistance was going down. Such voltage-dependent resistance provides further evidence that the device consisted of many states of resistance, crucial to its applications such as analog memory and neuromorphic computing.

However, when the voltage was higher than 25 V, the device showed an abrupt and permanent switching to a very low resistance state Figure 3.16 c). Such a phenomenon was generally indicated by a switching like a so-called soft breakdown or switching, such as switching like a short circuit. The likely cause is that there is defect migration or filament formation within the active layer, which generates an irreversibly conductive path between electrodes. Even though such a state offers large current conduction, such a state need not always be reversible and therefore might put a constraint on the lifetime of the device unless properly handled. Other than electrical properties, the synaptic plasticity, which characterizes the device, was further studied. By applying an alternating cycle between positive and negative voltage pulses, a device was capable of reproducing a short-term synaptic response using an alternating cycle between positive and negative voltage pulses. While repeatedly subjected to pulsing several times, current slowly rose (short-term potentiation, STP), which bears resemblance to how biological synapses are strengthened by repeated excitation stimuli. Conversely, another sequence to slow down pulsing slowed current (short-term depression, STD), which bears resemblance to how synaptic efficacy may degrade by time or by certain stimulus patterns. These findings confirm that the memristor device that was fabricated was capable of reproducing major synaptic operations, and thus, promises to mimic neuromorphic hardware.

4. CONCLUSION AND FUTURE OUTLOOKS

Since their theoretical prediction and subsequent realization, memristors and memtransistors have received considerable attention as promising candidates for next-generation electronic systems—particularly for non-volatile memory and neuromorphic computing. Their ability to emulate synaptic behavior, retain memory with low power consumption, and enable scalable architectures makes them highly suitable for the development of energy-efficient and intelligent hardware. This thesis contributes to the field by experimentally exploring the fabrication, characterization, and electrical performance of 2D material-based memristive devices.

The research consists of two experimental approaches. In the first part, memtransistor structures based on chemical vapor deposition (CVD)-grown MoS_2—widely recognized in the literature for their stability and suitability in neuromorphic applications—were fabricated. The aim was to investigate the effect of channel length, a key architectural parameter defined by the spacing between electrodes, on memristive behavior and electrical performance. The findings provide useful insights into how channel geometry influences switching behavior in two-dimensional semiconductor devices, which show promising synaptic responses.

In the second part, a novel fabrication route was investigated for the development of titanium-based memristors using plasma-enhanced atomic layer deposition (PEALD). Titanium-based materials have long been of interest due to their memristive switching potential, with early demonstrations using titanium oxides. More recently, Ti_3C_2 MXene has shown great promise due to its high stability and ability to emulate synaptic functions. However, traditional synthesis methods like selective etching from MAX phases present challenges in terms of scalability, uniformity, and integration with existing semiconductor processes.

To overcome these limitations, PEALD was employed as a promising alternative. This method offers precise thickness control, excellent conformality over complex surfaces, and compatibility with doping and defect engineering—features that are critical for adapting memristive devices to modern chip technologies. While the formation of Ti_3C_2 MXene structure remains under investigation, the synthesized material exhibited a crystalline TiC phase, which was successfully integrated into a vertical memristor configuration.

Electrical measurements confirmed resistive switching behavior, indicating the potential of this approach for further optimization. The proposed strategy combines the advantages of both titanium oxide and MXene-based memristors, suggesting a more controllable and scalable pathway for future device fabrication and integration into neuromorphic computing platforms.

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