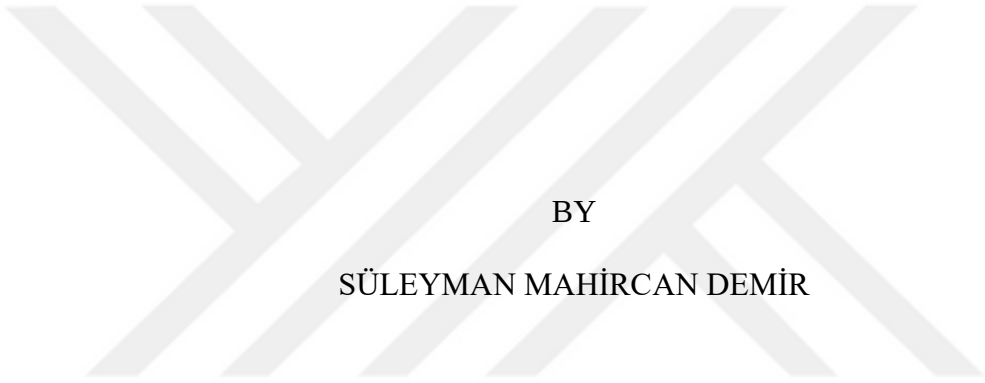


DESIGN OF FULLY INTEGRATED MILLIWATT THERMOELECTRIC
ENERGY HARVESTING INTERFACE CIRCUIT FOR WIRELESS BODY
SENSOR NETWORKS

A THESIS SUBMITTED TO
THE BOARD OF GRADUATE PROGRAMS
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MIDDLE EAST TECHNICAL UNIVERSITY, NORTHERN CYPRUS CAMPUS



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ABSTRACT

DESIGN OF FULLY INTEGRATED MILLIWATT THERMOELECTRIC ENERGY HARVESTING INTERFACE CIRCUIT FOR WIRELESS BODY SENSOR NETWORKS

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Master of Science, Electrical and Electronics Engineering
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September 2020, 96 pages

Wireless body sensor networks have drawn significant attention for providing out-of-hospital diagnosis and remote abnormality monitoring, which are vitally important for millions of people suffering from chronic diseases. Batteries powering these sensor networks hurt their mobility and longevity due to their bulkiness and down-time during charging or replacement. Therefore, this study focuses on thermoelectric energy harvesting from body heat, and targets eventual replacement of batteries by generating power levels above 1 mW using a fully integrated interface circuit component. The 180nm standard CMOS circuit, designed using Cadence IC design suite, contains the first optimized implementation of a previously developed quadrupling oscillator concept, a charge-pump based DC-DC converter, and a maximum power point tracking circuitry. Simulations using the electrical model of a commercial TEG module show that the DC-DC converter is capable of up to 1.5 mW output power, and 2 V output voltage, with 37% interface circuit efficiency when the TEG voltage is 500 mV. Minimum input voltage for the converter startup is found as 92 mV in the post-layout simulations. The interface circuit simulations with MPPT achieve 1.24 mW output power and 1.5 V output voltage for the TEG voltage of 500 mV. In the corresponding circumstance, the interface circuit efficiency is recorded as %20. The optimized interface circuit can be utilized to power up WBSN and enables batteryless sensor network operations.

Keywords: Energy harvesting, integrated circuits, thermoelectric energy harvesters, interface circuit, 1 mW power generator, wireless body sensor networks

ÖZ

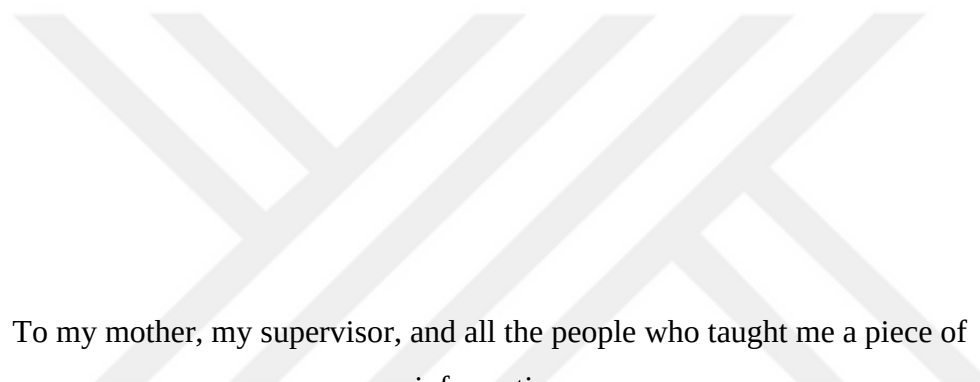
KABLOSUZ VÜCUT SENSÖR AĞLARI İÇİN TAM ENTEGRE MİLİVAT TERMoeLEKTRİK ENERJİ TOPLAMA ARAYÜZ DEVRESİ TASARIMI

Demir, Süleyman Mahircan
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği
Tez Yöneticisi: Prof. Ali Muhtaroglu

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Kablosuz vücut sensörü ağları milyonlarca kronik rahatsızlığa sahip insanın hastane dışı tanı ve anormal durumların izlenmesi amacıyla oldukça önem kazanmıştır. Bu sensör ağlarına güç veren piller, hantal yapıları ve sınırlı enerji depolama yetenekleri nedeniyle ağların hareketlilik ve ömürlerine zarar verir. Bu nedenle bu tez çalışması vücut sıcaklığı ve termoelektrik jeneratörlerden yararlanıp nihai olarak bataryaların yerini almayı hedefleyen tamamen entegre bir arayüz devresinden 1 mW üzerinde bir çıkış gücü elde etmeyi amaçlar. Cadence IC dizayn yazılımı kullanılarak tasarlanan standart 180nm CMOS devresi önceden dizayn edilen giriş voltajını dört katına çıkaran bir osilatör konsepti, şarj pompası temelli bir DC-DC dönüştürücü ve bir maksimum güç takibi devresinden oluşur. Mevcut bir termoelektrik jeneratör (TEJ) elektriksel modeli kullanılarak elde edilen simülasyon verilerine göre, DC-DC dönüştürücü 500 mV TEJ voltajında 37% verimlilik ile 2V çıkış voltajı ve 1.50 mW çıkış gücü sağlayabilir. Dönüştürücünün minimum başlangıç voltajı tasarım sonrası simülasyonlarda 92 mV olarak bulunmuştur. DC-DC dönüştürücü ve MPPT devresinden oluşan tamamen özerk arayüz devresi 500 mV TEJ voltajı ile 1.5V çıkış voltajı ve 1.24 mW çıkış gücü sağlar. Aynı koşullarda, arayüz devresi verimliliği %20 olarak kaydedilmiştir. Optimize edilen arayüz devresi rahatlıkla kablosuz vücut sensör ağlarını aktive etmek için kullanılabilir ve bataryasız sensör devrelerinin operasyonunu etkinleştirebilir.

Anahtar Kelimeler: enerji toplama, entegre devreler, termoelektrik enerji üreteçleri, arayüz devresi, 1 mW güç jeneratörü, kablosuz vücut sensör ağları



To my mother, my supervisor, and all the people who taught me a piece of
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LIST OF ABBREVIATIONS AND ACRONYMS

ABBREVIATIONS AND ACRONYMS

V	Voltage
I	Current
R	Resistance
P	Power
L	Inductor
C	Capacitor
f	Frequency
η	Efficiency (%)
g_m	Transconductance
TEG	Thermoelectric Generator
μ CU	Microcontroller Unit
MEMS	Microelectromechanical Systems
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
Low V_t	Low Threshold Voltage
LDO	Low Dropout Regulator
WSN	Wireless Sensor Network
WBSN	Wireless Body Sensor Network
WPAN	Wireless Personal Area Network
IoT	Internet of Things
IC	Integrated Circuit
VLSI	Very Large-Scale Integration

CHAPTER 1

INTRODUCTION

Internet of Things (IoT) refers to the interconnection of physical devices from micro-scale electronic circuits to large servers through the Internet [1]. A white paper by Cisco Internet Business Solutions Group estimates the “birth” of IoT was sometime between 2008 and 2009. The group reported the total number of devices connected to the Internet was 12.5 million in 2010, which means 1.84 devices per capita as the world population was 6.8 billion that year. They also predicted that the number of devices connected to the Internet per capita would hit approximately 6.58 in 2020 by considering the world population growth and developments in smart devices [2]. Therefore, it is not surprising to observe how fast these internet-connected devices, which may store, process, and send/receive data, are changing the human lifestyle. IoT provides effective solutions for a wide range of applications: smart cities, smart grids, security, transportation, logistics, retails, industrial applications, healthcare, etc. [3]. Recently, there is significant research focusing on the design and development of miniaturized sensor networks with wireless data transmission capabilities within the framework of IoT [4]. These networks are called Wireless Sensor Networks (WSNs). Fundamentally, WSNs have three basic functions: sensing, data processing, and wireless communication. They consist of sensors and relay nodes, which may have different power consumption, data handling capacity, and communication range [5]. Application-oriented data collection is performed by using these “smart” relay nodes [6]. Contingent upon the application domain and deployment area, design consideration of these networks can be as follows: network size, scalability, energy constraints, reliability, robustness, etc. Energy constraints can be thought of as the biggest challenge for the ubiquitous utilization of WSNs.

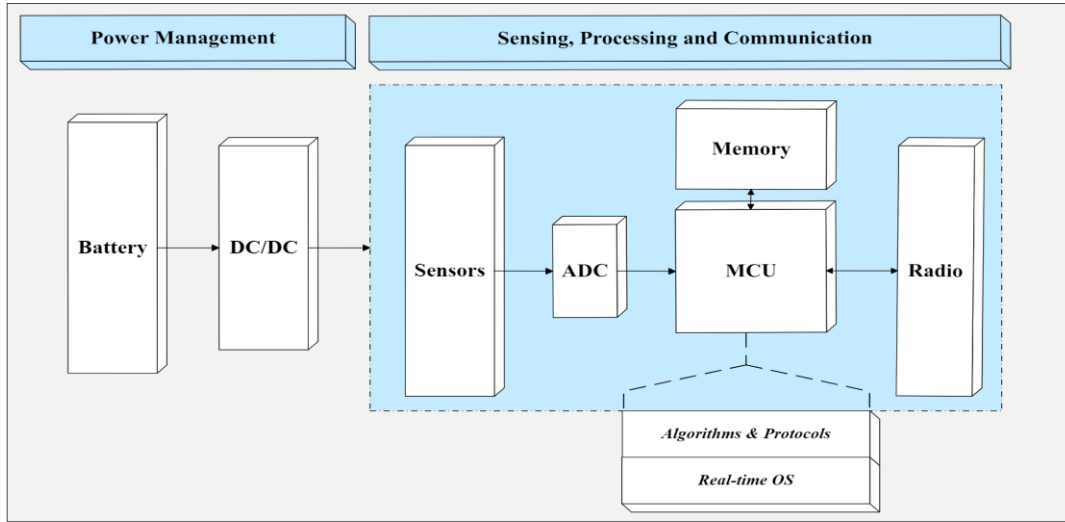


Figure 1.1. Typical wireless sensor node system architecture [7].

1.1 Wireless Body Sensor Network Fundamentals

Figure 1.1 shows a typical WSN architecture. Advances in WSNs enabled the utilization of the sensor networks for e-health purposes. E-health, which means the integration of information and communication technologies (ICT) with health systems, simply offers low-cost personalized healthcare to patients and increases real-time efficiency by delivering remote health services [8]. Wireless Personal Area Network (WPAN) is a substantial element for e-health systems. It can be defined as a network of wireless devices centered around an individual's life. WPANs particularly used in monitoring human body variables such as ECG, EEG, EMG, heart rate, blood pressure, glucose, and temperature are called Wireless Body Sensor Networks (WBSNs) [9]. Similar to WSN architectures, WBSNs are composed of intelligent sensor nodes that can perform a task and communicate with other nodes, including a central node. The central node handles the communication with the outside world. Generically, new generation WBSNs exploit cloud computing infrastructure to deal with a large amount of contextual data [10]. Cloud computing provides utilization of heterogeneous sensors, data storage scalability, energy-efficient data management, global access to the processing and storage infrastructure, and straightforward results sharing [11].

Table 1.1 Commercially available Wireless Body Sensor Networks

Application Domain	Product	Company	URL	Recorded Signals	Battery Life
Health	VitalSense	Philips Respironics	www.actigraphy.com	Dermal temperature, ambient temperature, heart and respiration rate	10 days with up to 10 sensors online
	Zephyr	Medtronic	www.zephyranywhere.com	ECG, respiration, core body temperature, accelerometry, time, location	24 hours per full charge
Fitness	Polar OH1	Polar	www.polar.com	PPG, 3D-acceleration	12 hours per full charge
	Apple Watch	Apple	www.apple.com	ECG, heart rate, activity	18 hours per full charge
Wellness	Charge 4	Fitbit	www.fitbit.com	Heart rate, sleep activity, location	Max. 7 days (up to 5 hours when using GPS)
	Vivoactive	Garmin	www.garmin.com	Activity, heart rate, accelerometry	Max. 3 weeks (up to 10 hours when using GPS)
Sleep	Oura Ring	Oura	www.ouraring.com	Sleep activity, heart rate, body temperature, accelerometry	Up to 7 days per charge
	WithingsMove	Withings	www.withings.com	Activity and sleep tracking	Up to 18 hours per charge
Brain-computer interface (BCI)	Mindwave Headset	NeuroSky	www.neurosky.com	EEG	8 hours per charge
	Epoc+ Headset	Emotiv	www.emotiv.com	EEG (14 Channel), motion sensing	12 hours per charge

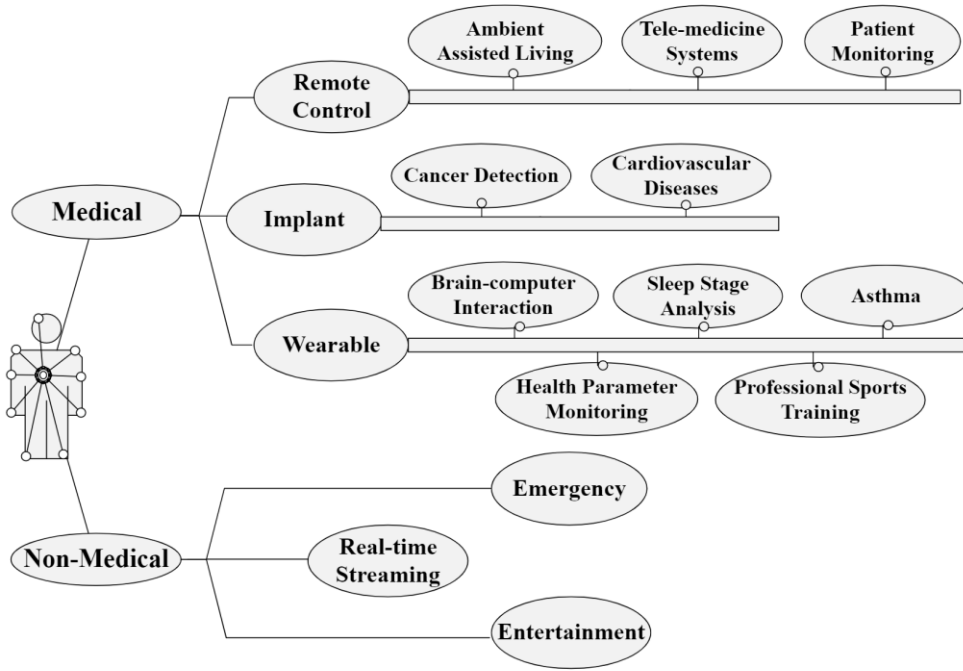


Figure 1.2. Wireless body sensor node applications (based on [12]).

1.2 Energy Harvesting for WBSN Applications

As depicted in Figure 1.2, WBSNs are used in various medical and non-medical applications. A recent article [13] discusses the possibility of helping to spot severe acute respiratory syndrome coronavirus 2 (SARS-CoV-2, aka HCoV-19), which causes fatal coronavirus disease (COVID-19), by using some of the WBSN examples presented in Table 1.1. According to the article, a person has realized that his “readiness,” a well-being indicator measured by his smart ring, was registering far below normal values just before he has been tested positive for COVID-19. Considering the fact that how profoundly SARS-CoV-2 has jolted the globe in 2020 by wreaking a pandemic, it may be expected to observe the ubiquitous utilization of WBSNs in the future to detect highly contagious diseases similar to COVID-19. Also, these networks provide unobtrusive sensing for the acquisition of health data, which is considered a cornerstone in health informatics [14]. Since the potential is enormous, WBSNs have attracted the attention of both academia and industry.

However, just like every technological development has, there are challenges for these networks. Some of these challenges are data management and processing, system interoperability, sensor heterogeneity, privacy and security, data validation and consistency, system programming, sensor stream management, energy consumption, and wireless communication, including coexistence issue, i.e. multi-systems operating in the same frequency band such as Industrial Scientific and Medical (ISM) band and Wi-Fi [10], [15].

Among those, energy consumption and management is an arduous challenge due to stringent power limitations eventuated from the miniaturization of these networks. Traditionally, electrochemical batteries are used to power up WBSNs. Zinc-air, lithium, and alkaline are the three common battery chemistries. Among them, zinc-air batteries have the highest energy density; yet their lifetime is very short compared to lithium and alkaline batteries. On the other hand, alkaline batteries are commonly used for consumer electronics due to their lower cost. However, their energy density is lower than the lithium batteries. A standard non-rechargeable lithium battery provides 2880 J/cm^3 energy density and 3-4V of output potential. That means a typical AAA lithium battery weighing roughly 10 grams can continuously supply $100 \text{ }\mu\text{W}$ of power for one year [16], [17]. Therefore, powering WBSNs using batteries is not feasible for long-term operation and portability. Moreover, lithium batteries cost higher than the other two aforementioned battery types despite their combination of high power density and longevity. Hence, there is a compromise between cost and lifetime for the battery-powered sensor networks. Adopting rechargeable batteries may seem to be a good solution for the above-mentioned problems. Nonetheless, maintenance required to recharge the batteries may not be economical or even achievable depending on the deployment area of the networks. Furthermore, the utilization of batteries is impractical for implant applications. Besides cost, mobility, and longevity problems, the disposal of batteries is another aspect which is needed to be taken into account. Batteries comprise of chemicals, and their disposal may cause serious environmental pollution. Rechargeable batteries cannot stop the exponential increase in electronic waste (e-waste) disposal.

Typically, the lifespan of rechargeable lithium batteries is between 2 to 4 years [18]. Considering the increasing number of IoT devices and consumer electronics, the amount of battery disposal can be very large in the future. Proper disposal or recycling of these e-wastes is the most desirable solution to prevent the disintegration of chemicals into the environment; nevertheless, the recycling rate of lithium-containing wastes was only 1%, while the global recycling rate of the batteries is still far below 10% [19], [20]. Thus, more sustainable solutions are of great importance to replace batteries.

Figure 1.3 depicts the different facets of power management, particularly for microelectronic computing systems. Energy harvesters (a.k.a. energy scavengers) are one of the most promising solutions to deal with battery-originated problems. Simply, the harvesters scavenge power from human activity or derive limited energy from environmental sources such as heat, light, vibrations, or radio waves [21].

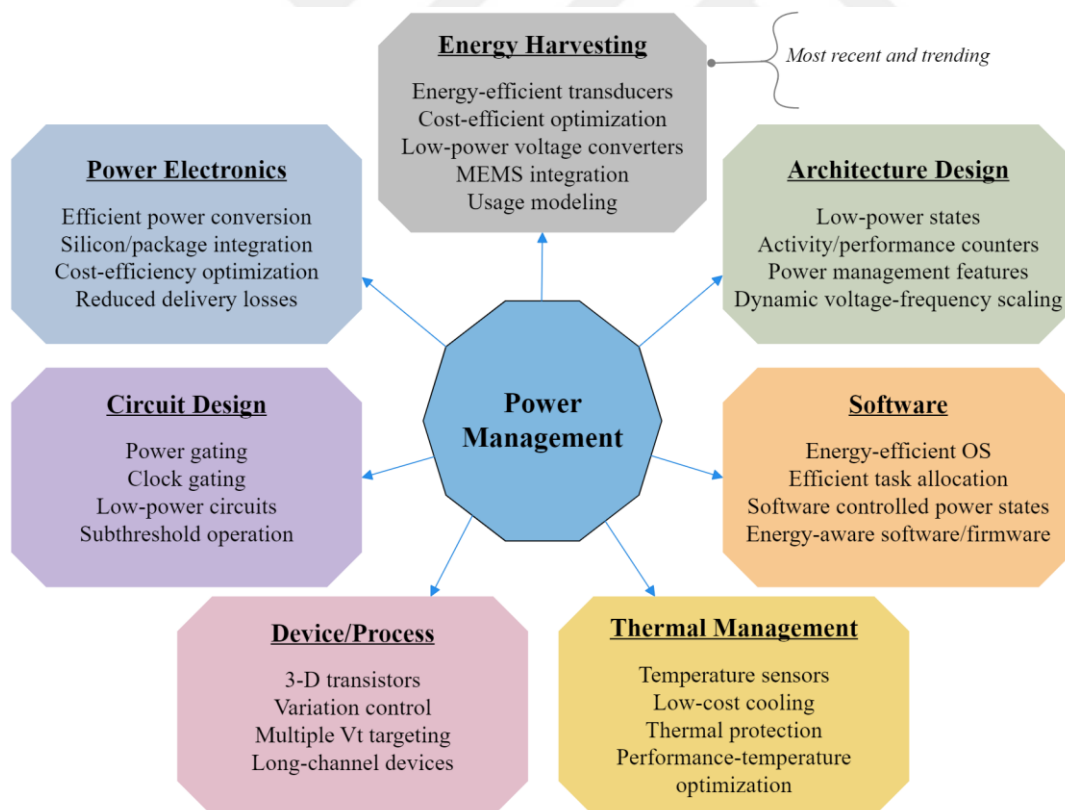


Figure 1.3. Power management facets [22].

Harvested energy might be used to recharge or replace batteries contingent on the amount of extracted power. Energy harvesters, which are often referred to as micro-power generators, are the ultimate sustainable solution for power management as the ambient energy sources practically never run out [1]. In addition to their potential of providing a sustainable solution, advances in micro-electromechanical systems (MEMS) improve the practicability of the harvesters [23]. Therefore, it is expected to observe irrepressible employment of energy harvesters for powering up WBSNs.

1.3 Interface Circuits and Design Considerations

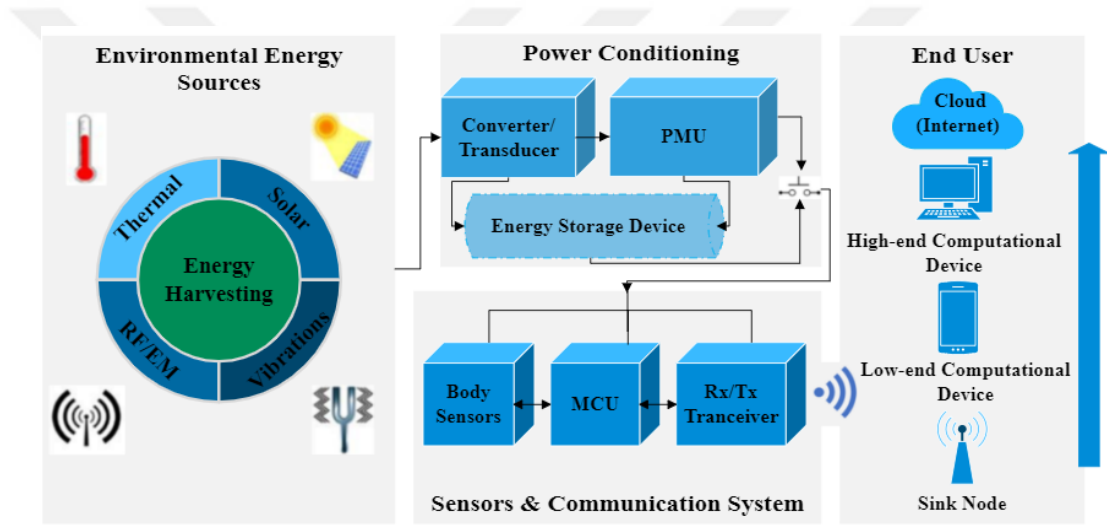


Figure 1.4. WBSN platform enabled by energy harvesters (based on [24], [25]).

As presented in Figure 1.4, a standard WBSN node consists of various sensors, an embedded processing unit, and a transceiver. Among those, the transceiver is the most power-hungry unit. The typical active mode power consumption rate of a low-power transceiver module is in the range of hundreds of mWs [26]. This rate reduces to $<100 \mu\text{W}$ by means of duty cycling thanks to the utilization of wake-up radio technology, part of IEEE's standard: IEEE Std 802.11 (i.e. Wi-Fi(R)) [27]. Moreover, the minimum active mode power consumption of state-of-the-art ultra-low-power microcontrollers is not less than $20 \mu\text{W}/\text{MHz}$ [4]. Usually, the clock speed of these devices is between 8 to 10 MHz. It means that the power consumption

of an ultra-low-power embedded processing unit will be in the range of hundreds of μWs . By adding the power required for the sensing units, the overall power consumption of a regular WBSN node varies between hundreds of μWs to a few mWs . However, energy harvesters cannot directly supply power to the sensor nodes due to the following considerations: Output power of the harvesters strongly depends on the density of the environmental energy sources. Ambient energy density alterations (causing variable output impedance for the energy harvesters) and sensor node impedance fluctuations (causing variable input impedance) reveal impedance matching problems leading to a substantial reduction in power transfer. Furthermore, the output voltage level of the harvesters might be far below the required supply voltage level of the electronics within the node. Different electronic circuits may need different supply voltage levels. The output voltage of some harvesters is in AC form, whereas the loads often require DC. For these reasons, it is essential to implement an efficient interface circuit between energy harvesters and loads.

Figure 1.5 depicts a typical energy harvesting micro-system consisting of a transducer, an interface circuit, and a load. It is anticipated that a standard interface circuit performs maximum power point tracking, voltage rectification/conversion, and voltage regulation. However, the efficiency of these operations is of the utmost importance to extract maximum available power from the transducer. As shown in the figure, one or more voltage conversion operations may be performed before supplying power to the load. Each stage bears some losses and substantially reduces the energy transferred. Therefore, designers should be aware of the design considerations presented in Figure 1.6 to develop the optimal interface circuit for a specific WBSN application. Although it is desirable to improve system efficiency and increase output power, sometimes it may not be possible to achieve them simultaneously. For instance, overall efficiency can be very low for some systems due to subcircuit losses, yet the output power requirement could be met. Likewise, individual subcircuit blocks might be adjusted for reducing losses to increase efficiency, but the adjustments may lead to impedance mismatch issues, causing a reduction in output power. Thus, application-oriented evaluation is essential.

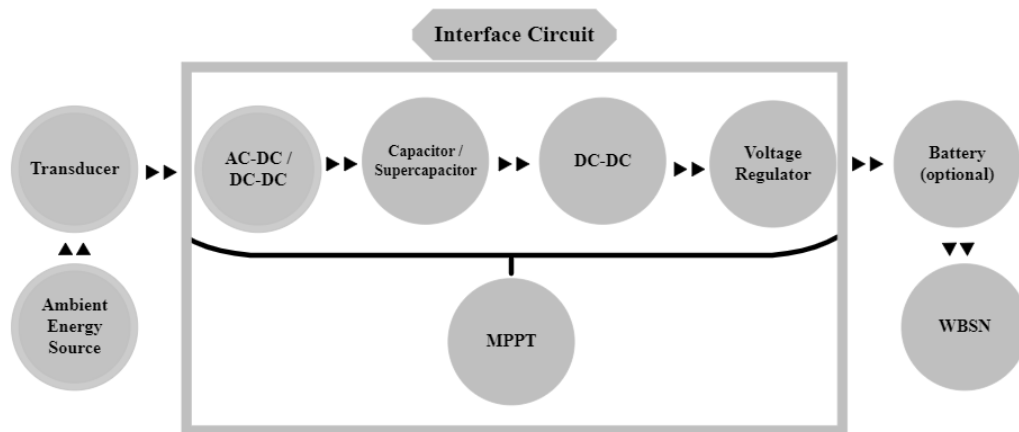


Figure 1.5. Quintessential energy harvesting interface circuit (based on [4], [28]).

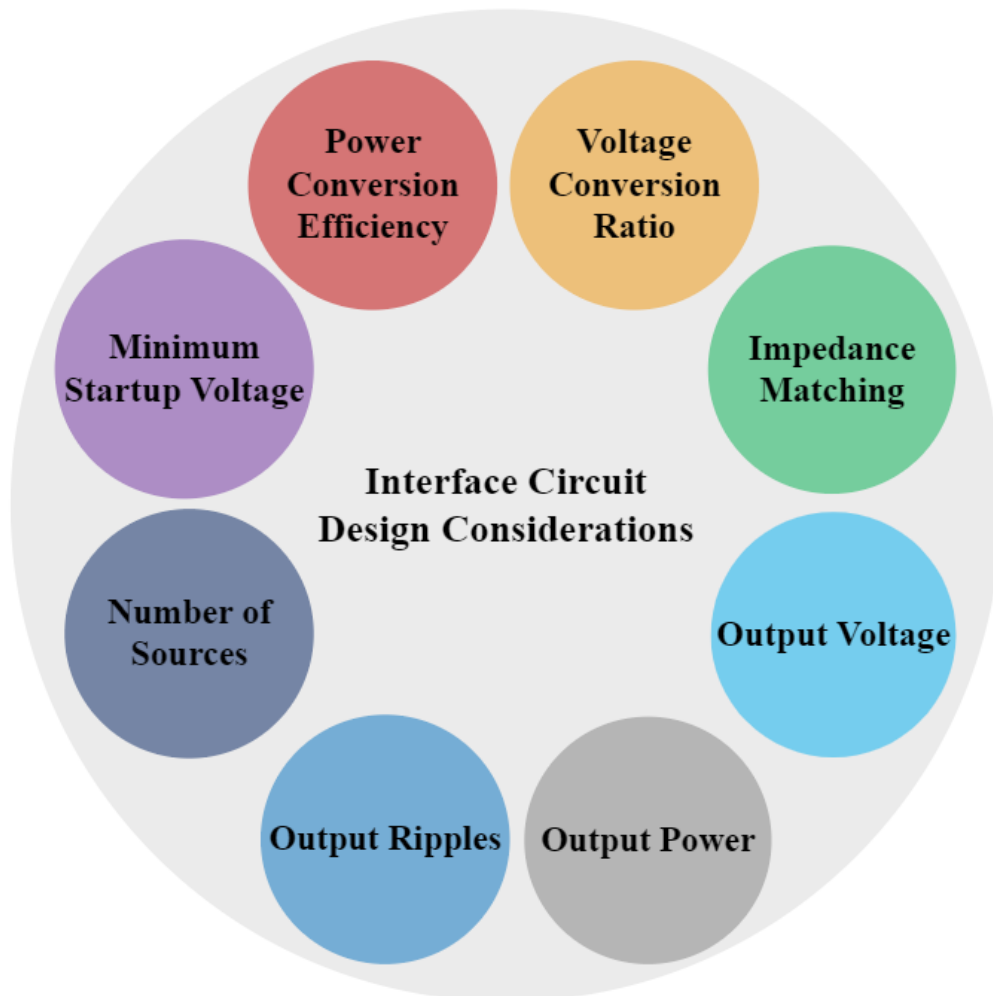


Figure 1.6. Interface circuit design considerations (based on [29], [30]).

1.4 Thesis Objectives

The aim of this work is to develop a fully integrated, self-starting, ultra-low voltage interface circuit for thermoelectric energy harvesting operations in order to achieve output power in the range of milliwatt. Most fully integrated solutions in the literature are able to reach hundreds of microwatts output power under maximum power delivery condition; however, this amount is challenging for critical healthcare applications under the paradigm of WBSNs. As aforementioned, only μ CUs consume power in the range of hundreds of μ Ws. Furthermore, transceivers require mWs of power without duty-cycling. Considering the fact that there are certain healthcare applications that do not allow the utilization of duty-cycling mode, it is crucial to enhance the output power of the fully integrated interface circuits. Moreover, thermoelectric generators provide less than 100 mV output voltage when there is a limited temperature gradient; hence, a minimum startup voltage of less than 100 mV is within the scope of this thesis.

A comprehensive list of the objectives of this thesis is as follows:

- Examination of characteristics of the DC-DC converters designed by the METU NCC Energy Harvesting research group;
- Analysis of the MPPT circuit proposed by the Energy Harvesting team to improve the existing DC-DC converter architecture;
- Optimization of the voltage quadrupling LC-tank oscillator for 5-stage charge pump architecture;
- Optimization of the low dropout (LDO) voltage regulator to obtain higher regulated output voltage level;
- Simulation of the DC-DC converter for 1 mW output power;
- Simulations of the fully autonomous interface circuit;
- Layout-based implementation of the DC-DC converter in 180 nm standard CMOS process technology.

1.5 Thesis Organization

The rest of the thesis is organized as follows: Environmental energy sources for micro-scale energy harvesting, together with characteristics of micro-power generators, are presented in Chapter 2. The advantages and disadvantages of each harvesting technique are discussed in this section. Some of the existing techniques in the literature are summarized for providing insight. This chapter aims to provide the necessary background for energy harvesting.

Chapter 3 starts with the fundamentals of DC-DC converters, including power and efficiency calculations. Different types of existing oscillator and charge pump architectures are introduced in this part. Working principles of the proposed voltage quadrupling LC-tank oscillator and charge pump circuit are also provided. The overall circuit diagram of the DC-DC converter that is capable of providing more than 1 mW output power is presented and explained in detail. Also, the generic view of the fully integrated autonomous interface circuit is provided here.

Chapter 4 introduces the model-based analysis of the DC-DC converter. Then, the simulations are delivered for the verification of the DC-DC converter and the full autonomous interface circuit. Cadence software suite [31], one of the most common and reliable computer-aided design (CAD) tools for analog and digital integrated circuits, is used for circuit- and layout- level implementations of each sub-block. UMC 180 nm standard CMOS process technology [32] is selected as the implementation technology due to its maturity and reasonable tape-out price. The DC-DC converter and the fully integrated autonomous interface circuit simulations for 1 mW output power and minimum startup conditions are also presented here.

Finally, a comparison of the outcomes with the related work presented in the literature is provided in Chapter 5. The thesis is concluded with the discussion of the optimization studies and possible future works.



CHAPTER 2

BACKGROUND

Miniaturization is one of the most recent trends in sensor network design. Advances in MEMS technology and integrated circuits accompany this miniaturization vogue. As aforementioned in Chapter 1, the existence of batteries in sensor networks not only creates cost, longevity, and disposal issues but also prevents volume minimization and harms mobility. Therefore, an alternative approach for replacing batteries must address the battery-originated consequences. The potential of energy harvesters makes them one of the most promising successors. On the other hand, the amount of energy available from tiny harvesters is very limited. Also, harnessed energy profoundly depends on the magnitude and availability of energy sources in the vicinity. The practicality of energy harvester utilization can only be measured if the energy scavenged is higher than the energy consumed by a circuit block in a time frame. Therefore, careful analysis of the sensor network application is indispensable before the incorporation of appropriate energy harvesting mode. In fact, available energy sources for energy harvesting can be classified under two main categories: Human body and ambient. Figure 2.1 depicts these categories and their sub-categories. This study elaborates on ambient energy sources. The following sub-sections elaborate on the ambient energy harvesting techniques.

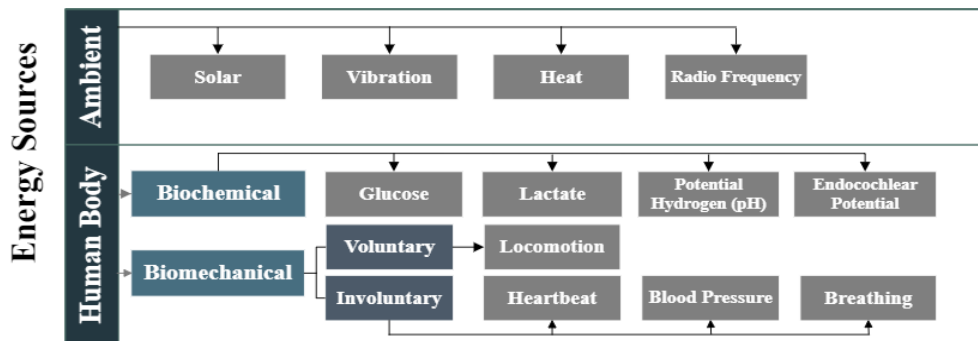


Figure 2.1. Classification of energy harvesting sources [33].

Table 2.1 Ambient energy sources and characteristics of energy harvesters [1].

	PV Solar	Thermoelectric	Piezoelectric vibration	Electromagnetic vibration	Ambient RF
Power density	Outdoor: 100mW/cm ² Indoor: <100μW/cm ²	50-100 μW/cm ² per °C	10-200 μW/cm ³	1-2 μW/cm ³	0.0002-1 μW/cm ²
Output voltage	0.5 V max	10-100 mV	10-20 V (open ckt)	few 100 mV	3-4 V (open ckt)
Availability	Lighted environment	Surfaces with ΔT	Hz-kHz vibration	Hz vibration	Vicinity to radiation source
Pros	High power density Well developed technology	Non-intermittent/less intermittent than alternatives	High voltage Well developed technology	Well developed	Antenna can be integrated Widely available
Cons	Intermittent Highly dependent on light	Low voltage Need ΔT	Highly variable output Large area High output impedance	Bulky Low power density Low output voltage	Very sensitive to distance of the RF source

2.1 Photovoltaic (Solar) Energy Harvesting

Photovoltaic (PV) energy harvesting employs sunlight or any artificial light to produce electrical energy. The procedure is performed in three fundamental steps: PV cells, which are composed of semiconductor materials, absorb the energy from photons when they are exposed to light; absorbed energy releases electrons from the semiconductor materials; negatively charged electrons and positively charged holes are collected in opposite electrodes [34]. Since the electrons and holes are separated, the presence of a load connected to the electrodes allows the flow of free electrons generating an electrical current thanks to the p-n junction effect [35].

The equivalent circuit model of a PV cell is presented in Figure 2.2 below. Photocurrent generated by the incident light, which is directly proportional to light irradiance, Shockley diode current, equivalent shunt resistor, and series resistor modeling parasitics are represented by I_{pv} , I_d , R_p , and R_s , respectively. In order to approximate the efficiency of a PV cell, the ratio of maximum power (P_{max}) to the product of open-circuit voltage (V_{oc}) and short-circuit current (I_{sc}) should be calculated. This term is referred to as the fill factor. As the behaviors of PV cells are non-linear, it is critical to detect the operation point at which the product of the output voltage and current is maximum. In addition, variable light irradiance substantially alters the output impedance of the cell, causing impedance mismatch with the load. Hence, the use of circuits enabling maximum power point tracking is a necessity.

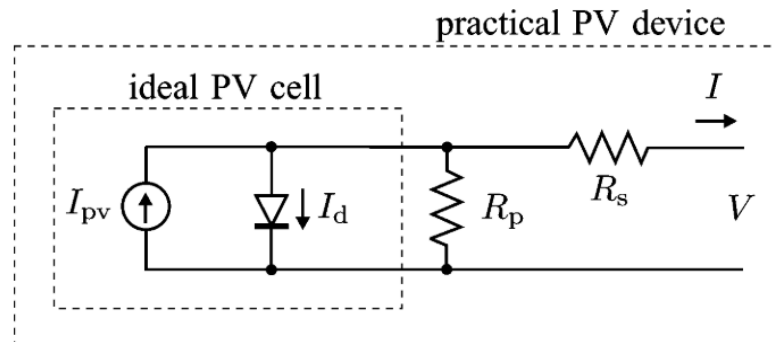


Figure 2.2. Photovoltaic cell equivalent circuit [36].

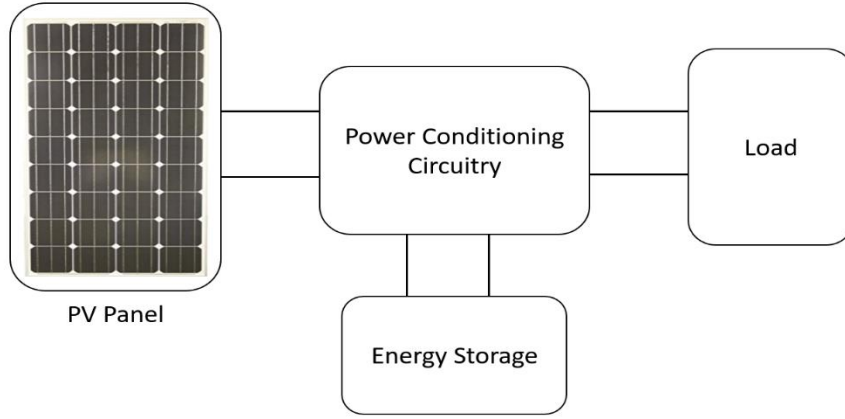


Figure 2.3. Quintessential PV energy harvesting system [37].

The efficiency of a PV cell is defined by [38]:

$$\eta = \frac{V_{oc}I_{sc}FF}{P_{inc}} \quad (2.1)$$

P_{inc} represents the solar power incident on the cell, and FF denotes the fill factor in equation (2.1). It is discernible that the efficiency of solar cells could be maximized by swelling up the values of the parameters in the numerator. V_{oc} and I_{sc} values arrive from the PV cell size and material properties. On the other hand, the fill factor can be explicitly described as:

$$FF = \frac{P_{max}}{V_{oc}I_{sc}} = \frac{V_{mp}I_{mp}}{V_{oc}I_{sc}} \quad (2.2)$$

The voltage and current required to generate maximum power are denoted as V_{mp} and I_{mp} , respectively. As equation (2.2) implies, the full potential of a PV cell can be reached, i.e. maximum power can be extracted when V_{mp} and I_{mp} are simultaneously obtained for any given load. The essentiality of an interface circuit with maximum power point tracking capability, as aforesaid, is therefore proven. Considering this necessity, it is of great significance to develop low-power high-efficiency maximum power point trackers (MPPTs) to extract maximum available energy from PV cells.

Historically, maximum power point (MPP) tracking methods have been classified under two main categories: large-scale PV harvesting systems that utilize MPPT architectures based on digital signal processors (DSPs) or microcontroller units (μ CUs); small-scale PV harvesting systems that utilize MPPT architectures without DSPs or μ CUs [39]. The main reason behind this difference is that the corresponding technologies introduce additional power consumption, which becomes extremely important for micro-scale energy harvesting systems. Notwithstanding, new MPP methods and algorithms have been emerged and become viable as the importance of micro-scale energy harvesting has peaked. For instance, [40] proposes a time-domain hill-climbing MPPT architecture for reusing the power information from the former output regulation to jettison power-hungry analog circuits such as current sensors or operational amplifiers (op-amps). Simply, they propose a method to adjust the input impedance of the charge-pump architecture, which is used for DC-DC conversion and will be discussed in Chapter 3, to match it with the variable PV output impedance at any given time. Conventionally, voltage-controlled oscillators (VCOs) are employed to change the clock frequency of a charge pump, which modifies the input impedance. However, frequency modulation requires power-hungry op-amps. The authors suggest an architecture that changes the total capacitor value of the charge pump to alter its input impedance. This procedure does not require power-hungry analog circuits, yet it increases the chip size. Although there is a compromise between chip size and power consumption, the method can be beneficial for specific very-low-power applications where the chip size does not matter. The same group of researchers bring their studies forward in [41] and propose a two-dimensional (2D) MPPT structure, which reconfigures the number of charge pump stages and alters the switching frequency. The benefit of this approach is revamping the charge pump impedance in two different ways to exploit a wider input range for various energy sources and optimize harvesting efficiency simultaneously. The authors claim that the algorithm can be adopted for various energy sources such as a PV cell and a thermoelectric generator (TEG). Examples aiming to improve the efficiency of MPPTs for PV harvesting systems can be diversified further as it is still a focal point.

Even though different MPPT algorithms boost the extracted output power from PV cells, there are still challenges to their employment for indoor applications. As depicted in Table 2.1, the power density of a typical PV cell is less than $100 \mu\text{W}/\text{cm}^2$ for indoor conditions, whereas it is $100 \text{ mW}/\text{cm}^2$ for outdoor. The significant reduction in power density between indoor and outdoor conditions compels designers to deal with this sudden change that makes the utilization of PV cells comparatively harder for wearable electronics and causes the production of rather sophisticated interface circuits.

Nonetheless, fast-developing semiconductor technology helps the development of more effective PV cells. Customarily, the efficiency of PV cells ranges roughly from %30 (monocrystalline cells) to %5 (thin-film cells) [42]. Yet, a wide diversity of researches on PV energy harvesting systems escalates their efficiency and employability. Some of these researches are: minimizing series resistance (R_s) to maximize FF [38]; harvesting solar energy in the ultraviolet (UV) frequency spectrum instead of the visible spectrum by using antenna based solar cells [43]; specializing MPPT algorithms for flexible thin-film PV modules [44]–[46]; designing artificial material (metamaterial) based PV cells to achieve higher absorption rates in different frequency spectra [47]–[50]. To sum up, PV energy harvesting will remain to draw researchers' attention due to their promising potential.

2.2 Thermoelectric (Temperature Gradient) Energy Harvesting

It is possible to generate electrical energy from temperature difference by using thermoelectric generators (TEGs). TEGs are solid-state energy converters, which consist of an array of $2N$ pellets from p- and n-type semiconductor materials forming N thermocouples [51]. The semiconductor materials in thermocouples are joined electrically in series and thermally in parallel [52]. In order to adjust the output voltage and current of a TEG, thermocouples could be connected in matrix form. The number of series thermocouples determines the output voltage level, whereas the number of parallel thermocouples determines the output current level [53].

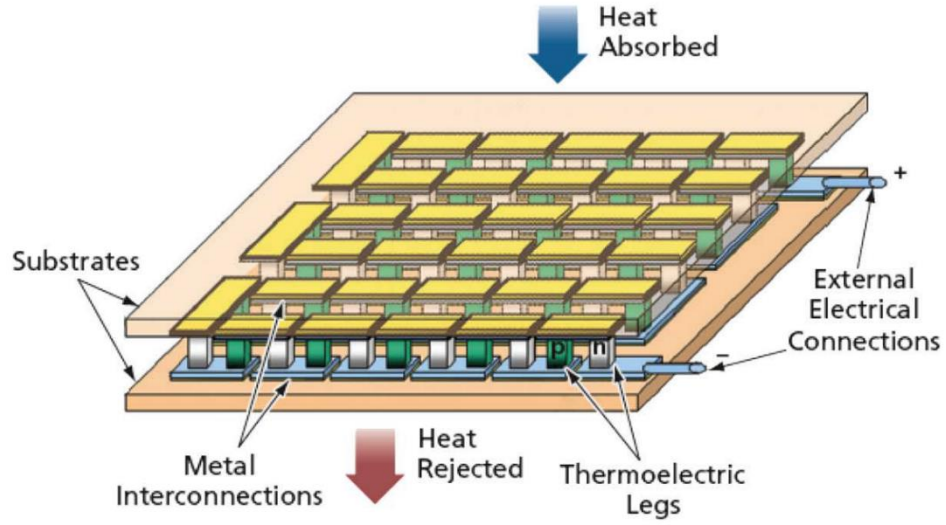


Figure 2.4. Generic thermoelectric generator structure [54].

The operation of TEGs depends on three principal effects: the Seebeck effect, the Peltier effect, and the Thomson effect [34]. Among those, the Seebeck effect describes an important energy conversion phenomenon: an electromotive force (emf) can be generated by a circuit which is composed of two dissimilar semiconductor materials, e.g. p- and n-type materials, in case a temperature gradient is provided between the junctions. The induced emf, i.e. potential difference, can be defined as:

$$V_{TEG} = \alpha \Delta T \quad (2.3)$$

The terms ΔT and α in equation (2.3) refer to the temperature gradient and the Seebeck coefficient, respectively. Simply, the Seebeck coefficient is a measure of open-circuit emf generated in response to the temperature gradient across the junctions in Volts per Kelvin (V/K) [55]. By considering the phonon-drag effect, which is known as the dragging of electrons because of the heat flow in a lattice and boosts the Seebeck coefficient, an inversely proportional relationship between the Seebeck coefficient and conduction electron density could be estimated [56]–[59]. Hence, the highest Seebeck coefficients are observed in semiconductors since they have relatively few conduction electrons compared to metals. The highest Seebeck coefficient belongs to selenium (Se) with 900 $\mu\text{V/K}$ at room temperature [60].

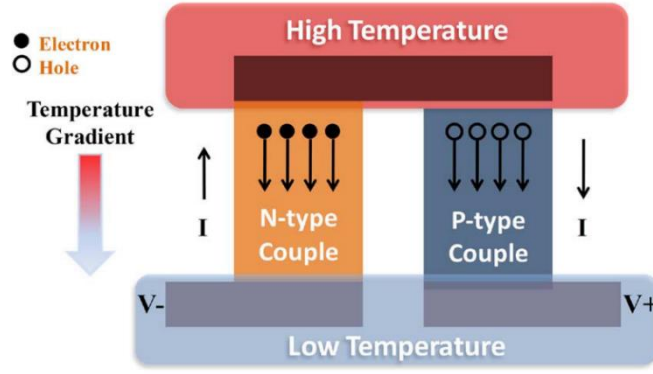


Figure 2.5. Micro-TEG operation mechanism illustration [61].

The maximum efficiency of a TEG is given by the Carnot efficiency [42]:

$$\eta = \frac{T_h - T_c}{T_h} \quad (2.4)$$

T_h and T_c in equation (2.4) represent the hot and cold surface temperatures in Kelvin, respectively. Due to the limited Seebeck coefficient (α), output voltages of TEGs are relatively low. The typical output voltage of a standard TEG varies between 20-400 mV for wearable applications in which the temperature gradient between the surfaces is scant [62]. Therefore, an interface circuit with voltage boost capability is necessary to use TEGs for powering up WBSNs. Metal-oxide semiconductor field-effect transistors (MOSFETs), which are the building blocks of interface circuits, need hundreds of mVs input voltage to exceed the threshold level required to commence operating. Thereby, a cold startup feature that enables the voltage step-up with very low input voltage levels is also highly desirable.

A TEG interface circuit based on a single-inductor dual-output boost converter is presented in [63]. The system architecture is composed of an off-chip inductor (33 μ H) and an on-chip DC-DC converter with control circuitry. In addition, all external, one input capacitor (1 μ F), one storage capacitor (100 nF), and one control circuit supply capacitor (30 nF) are employed. The load has been modeled as a resistor. The on-chip components have been implemented in 180 nm CMOS process technology. The total chip area is 2.3 mm² while the active area occupies only 0.3 mm².

Basically, the authors aim to reduce the power consumption and minimize the losses of the interface circuit by using a system-level methodology and ultra-low-power circuit techniques. In addition, they use zero-current switching (ZCS) and zero-voltage switching (ZVS) techniques in the control circuitry to achieve high conversion efficiency. The minimum startup voltage is reported as low as 15 mV. The peak conversion efficiency of the system is %86.6 at 30 μ W input power. Another interface circuit for thermoelectric energy harvesting is presented in [54]. The system has been designed in 350 nm CMOS process technology to harvest human body temperature specifically. The building blocks are a startup circuitry, a storage circuitry, and a DC-DC step-down converter. One input capacitor, one startup capacitor, one storage capacitor, and one load capacitor are integrated into the system. Once the input capacitor voltage achieves 1 V across its terminals, the mechanically assisted startup circuit, which contains an inductor, is activated until the startup capacitor is charged up to 1.8 V. This voltage cannot be directly used to supply the load since the capacitance value is very small and the voltage across the capacitor would drain very fast. Therefore, the storage circuitry acting like a buffer charges the storage capacitor, which is expected to be more than 1.8 V since the size of the capacitor is chosen accordingly. Instead of the traditional technique of boost converter utilization in thermoelectric harvesting systems, the authors implemented a step-down converter to regulate the voltage in the storage capacitor to 1.8 V when its voltage level exceeds 2.4 V. The advantage of this work is 1.8 V output voltage can be achieved from 25 mV input voltage which might be provided by a single TEG with only 1°K temperature gradient between its surfaces. The minimum startup voltage is reported as low as 35 mV, yet the system can operate with 25 mV after the startup. The end-to-end peak efficiency of this study is %58. Another work [64] presents a DC-DC step-up converter for very low input voltage applications. The converter has two main parts: a feedforward low startup control circuitry part is employed when the input voltage level is between 40 mV to 150 mV and provides high duty cycle pulse width modulation; and if TEG voltage surpasses 150 mV, a feedback circuitry part is activated as it provides better accuracy for output voltage.

Thermoelectric energy harvesting research is not only concentrated on the interface circuits. For instance, the authors in [65] examine the parasitic components at skin/TEG and TEG/ambient interfaces and propose an accurate TEG model for wearable electronics. They presented a custom-designed TEG with improved material properties by using their TEG model and observed a 3x improvement in output power. In another work [66], a cold startup feature has been investigated with a TEG that can provide a potential difference when the temperature gradient is low. The authors achieved 23 mV input voltage with only a 0.6 °C temperature gradient (ΔT). It has been claimed that an energy harvesting system could be activated with this input voltage level roughly in 3 minutes. The aim of the study is experimentally showing the minimum temperature gradient at which an embedded processor operates to allow for wireless communication. In [67], the authors present a novel thermoelectric energy harvesting circuit with a reconfigurable TEG array which requires neither an inductor nor a flying capacitor. The proposed architecture is able to achieve voltage conversion and MPP tracking simultaneously by reconfiguring the TEG array to improve power conversion efficiency over the conventional conversion mechanisms.

As one can realize, thermoelectric energy harvesting is an attractive research area, particularly for wearable applications due to the natural temperature gradient provided by the human body [68]. Furthermore, TEGs offer ease of incorporation since they are light-weighted, acoustically silent, robust, reliable, and relatively long-lasting [69]. Also, it is easy to electrically model them by using an independent voltage source in series with a resistor. The value of the resistor ranges from a few ohms to tens of ohms [70]. As aforesaid, a thermally parallel combination of TEGs refers to an electrically series connection. Thus, if more than one TEG is necessary for certain applications, it would be enough to increase the resistor value to update the electrical model. Also, TEGs are free of moving parts, which enables considerable miniaturization. The existence of CMOS compatible TEG versions even makes thermoelectric energy harvesting more appealing for WBSN applications since miniaturization and integration are acutely substantial.

2.3 Vibration Energy Harvesting

Recently, harnessing kinetic energy to empower miniaturized electronic devices becomes very attractive as human and machine motion provide vibrations that are usually wasted. Harvesting the wasted vibrations, which vary in magnitude and frequency, as a substitute for batteries in low-power applications, particularly medical, are in great demand [71]. There are three different energy conversion techniques to scavenge electrical power from vibrations: electromagnetic, electrostatic, and piezoelectric transduction [72]. The following subsections expatiate these three energy conversion mechanisms.

2.3.1 Electromagnetic Energy Harvesting

Electromagnetic transduction is one of the most common electrical generation techniques, particularly in macro-scale applications [71]. Lately, it is also employed in micro-scale applications to empower WBSNs by taking advantage of the human movement. Fundamentally, electromagnetic transduction is based on Faraday's law of electromagnetic induction. This law states that the alteration in magnetic flux that is linked with a coil induces a potential difference across the coil, allowing a current passing through the circuit [73]. Kinetic energy is used to change the magnetic flux; therefore, generated output power profoundly depends on input vibration magnitude and frequency. Conventionally, permanent magnets, and printed coils are utilized in micro-scale applications. For instance, the authors in [74] proposed an electromagnetic (EM) energy harvester prototype that is made of a four-pole arrangement of neodymium-iron-boron (NdFeB) permanent magnets, copper wire wound coil, and FR4 material. They designed a folded cantilever structure from an FR4 sheet with 300 μm thickness to reduce the operating frequency by keeping the device footprint relatively small. The maximum output power of 19.3 μW at 1.5-g acceleration across 1 $\text{k}\Omega$ load resistance has been recorded. They also investigated both mechanical impact and bistability for wideband operation.

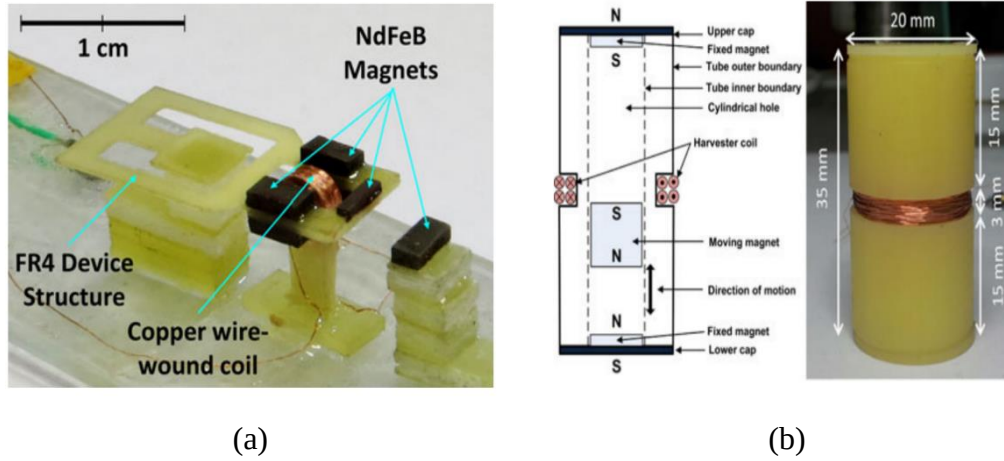


Figure 2.6. Fabricated EM energy harvester prototypes (a) folded harvester presented in [74], (b) cylindrical harvester presented in [75].

A fully integrated battery-free EM energy harvesting system has been proposed in [75]. The authors have been utilized an EM harvester consisting of fixed and moving magnets inside a cylindrical tube and a harvester coil wrapped around the tube. Generated AC current is fed to the novel fully integrated interface circuit, which is composed of active and passive AC-DC doublers and a DC-DC converter. The overall system provides 2.48 V to a resistive load of 4.4 M Ω when the EM harvester operates under 0.5-g, 10 Hz vibration. Another EM harvesting interface circuit presented in [76] eliminates standby power consumption by shutting down the interface circuit when AC input voltage amplitude is less than 0.6 V. The proposed circuit can provide up to 3 V regulated DC output with 1.5 V AC input amplitude. The overall system achieves %60 efficiency and provides 3.9 mW output power with the same input. However, it employs an off-chip inductor to boost the voltage level.

Despite the impressive advances in micro-scale EM energy harvesting applications, there are still significant challenges for their employment. The output power of small-scale EM harvesters is significantly lower compared to other energy harvesters, and that makes their implementation relatively harder. Moreover, their integration with MEMS technology is still a challenging process, and a dramatic decrease in magnetic flux is observed when the magnet sizes are downscaled [23].

2.3.2 Electrostatic Energy Harvesting

Electrostatic transduction is realized through the capacitance alteration of initially charged variable capacitors. Conductors forming the capacitors change their position in response to a motion or vibration; thus, energy stored in the capacitors alters, and mechanical energy is converted into electrical energy [77]. However, there is a need for a separate pre-charge source to initiate the scavenging process. Notwithstanding, the authors in [78] presented an electret-based electrostatic μ -power generator that does not require a separate charge source. The proposed μ -power generator makes use of a variable capacitor polarized by an electret, which is a permanently polarized dielectric substance (analogous to a permanent magnet). The initial polarization eliminates the pre-charge source requirement, yet the harvested power thoroughly rely upon the primary polarization source. The most noticeable advantage of electrostatic energy harvesters is their compatibility with the CMOS process and MEMS technology [79]. Nevertheless, conductor displacement limitation, mechanical stop, initial polarization necessity, the impact of parasitic capacitances, low power density, and high output impedance are the main problems against the widespread utilization of this type of conversion mechanism [23].

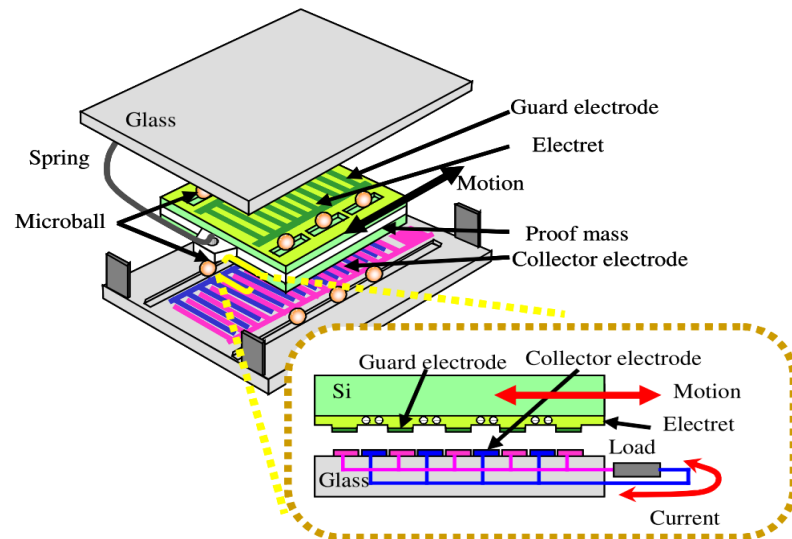


Figure 2.7. Electrostatic micro-power generator example [80].

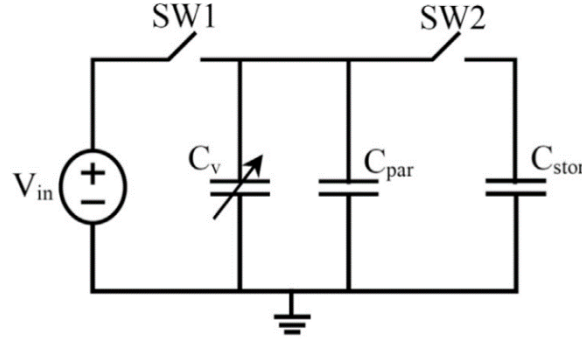


Figure 2.8. Electrostatic converter simple circuit representation [81].

There are studies on interface circuit development for electrostatic energy harvesting in the literature. For example, in [82] self-biased DC-DC buck converter is proposed. The full system also contains a fully analog MPPT circuitry and AC-DC converter. The proposed MPPT algorithm matches the input resistance of the converter with the source resistance of the harvester. The interface circuit has been implemented in 0.25 μm TSMC Bipolar-CMOS-DMOS (BCD) process, yet it requires two discrete components: a 10 mH inductor and a 100 nF input capacitor. The overall system achieves maximum %88.7 end-to-end efficiency while the maximum MPPT efficiency reaches almost %100. The DC-DC converter is able to accept input voltage in the range of 5-60 V and steps it down to 2-5 V. Input power range is reported as from 25 μW to 1.6 mW. The same group has reduced the minimum input power to 1 μW in [83]. Furthermore, they were able to achieve a significant reduction in interface circuit power consumption by decreasing it from 5 μW to 0.5 μW . However, they have employed five discrete components (an inductor, two capacitors, and two resistors) to achieve these advancements. In another work [84], 1x1 mm² 0.7 μm BiCMOS electrostatic energy harvesting IC has been proposed. The IC charges and holds the potential difference across a vibration-sensitive variable capacitor so that an ambient vibration separates the conductor plates and decreases the capacitance value leading to the generation of a current flowing into a battery. Based on the experimental results, the authors reported the time necessary to charge a 1 μF capacitor from 3.5 V to 3.81 V as 35 seconds.

Despite the works delineated above, there are still challenges for the utilization of electrostatic energy harvesting circuits, and further studies are essential to increase their efficiency and employability.

2.3.3 Piezoelectric Energy Harvesting

Piezoelectric transduction is the most promising energy conversion mechanism among the vibration-based energy harvesting techniques due to their ability to produce higher output power for a given size and compatibility with MEMS technology [85]. This type of conversion mechanism arises from the direct piezoelectric effect, which was first discovered by Pierre and Jacques Curie brothers in 1880 [86]. The direct piezoelectric effect states that certain solid materials with no inversion symmetry, such as ceramic and crystals generate electrical charges when an external force is applied [87]. Similarly, the reverse piezoelectric effect, the fact that an external electric field applied to so-called piezoelectric materials causes a mechanical deformation, had been discovered by Gabriel Lippmann in 1881.

The authors of the work [87] explain the piezoelectric effect clearly by means of Figure 2.9. Below the Curie temperature ($\sim 570^\circ\text{C}$) denoted as T_C , asymmetric electric dipoles are created as the charge center of the material shifts away from the geometric center. If a strong electric field is applied, the material is polarized, and the groups of dipoles are aligned, leading to the exhibition of piezoelectric properties.

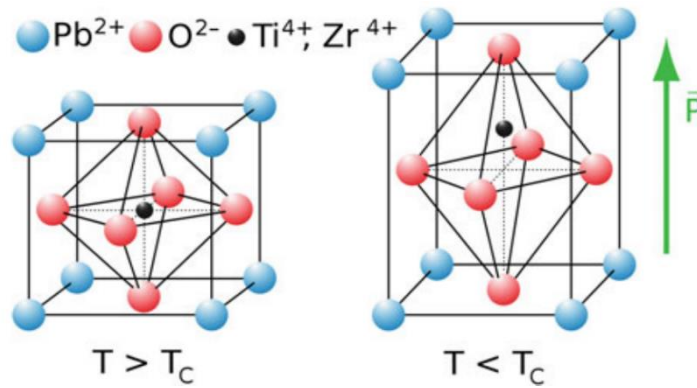


Figure 2.9. Lead zirconate intrinsic piezoelectric effect [87].

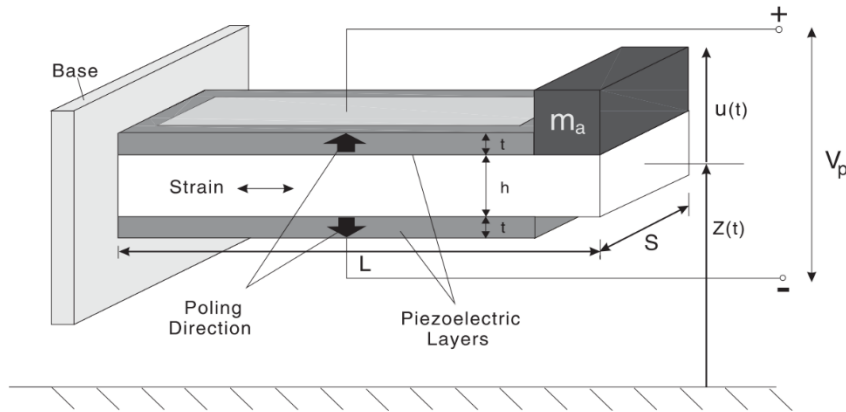


Figure 2.10. Piezoelectric-based micro-power generator illustration [88].

Above the Curie temperature, the material is depolarized, and it loses piezoelectric characteristics. Recently, lead zirconate titanate (PZT) is the most commonly used piezoelectric material; therefore, the reader may assume PZT when it is written piezoelectric material for the rest of this work.

Piezoelectric materials could be employed in different geometries to harvest vibrations. The most prevalent geometric structure is the cantilever beam as this type of structure provides low resonant frequencies, could even be reduced further by adding a tip mass, as shown in Figure 2.10, and a high level of strain in the piezoelectric materials [89], [90]. Besides, it could be compactly implemented with MEMS technology to occupy a very low volume that is particularly valuable for wearable applications. Cantilever beam structure might be configured in two different forms: unimorph and bimorph. Unimorph configuration is formed by one piezoelectric material placed on top of a beam, whereas bimorph configuration is formed by two piezoelectric layers placed on top and bottom of the beam [89]. The advantage of the bimorph configuration is that the output voltage or current of the harvester can be doubled by setting up the cantilever beam for series and parallel operations, respectively [87].

A clear and detailed analysis of the effectiveness of vibration-based energy harvesters is presented by Roundy in [91]. The power density of a PZT is defined as:

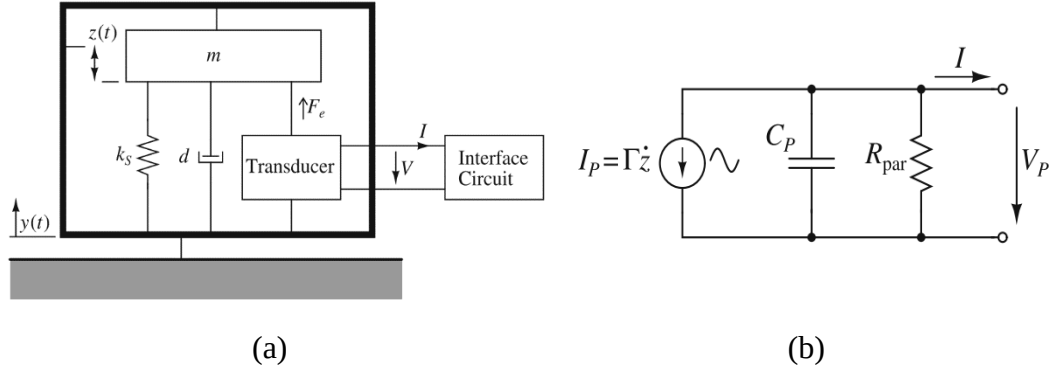


Figure 2.11. Model of (a) a kinetic energy harvester with lumped elements, (b) PZT equivalent circuit [87].

$$p_{max} = \frac{k^2 \rho (QA)^2}{4\omega} \quad (2.5)$$

The term k represents the coupling coefficient, the ratio of the converted energy under no-load condition to the total energy inputted to the system, ρ represents the proof mass material density, Q is the quality factor, A is the acceleration, and ω is the excitation frequency. The power density p_{max} is given in $\mu\text{W}/\text{cm}^3$ [91]. In order to achieve higher power density, the coupling coefficient and/or proof mass density might be boosted. On the other hand, frequency and power relation is more complicated. An inversely proportional relationship between the extracted power and resonance frequency is observed when mass acceleration multiplication (QA) is kept constant by setting the excitation frequency to a certain level. In case the excitation frequency is set to a level where the proof mass displacement is constant, proportionality between the extracted power and the third power of the resonance frequency is observed [23].

Figure 2.11 depicts the generic mechanical model of kinetic energy harvesters. As one can realize, kinetic energy harvesters can be modeled as second-order spring-mass systems where k_s represents the stiffness, m is the seismic mass, and d is the damper, which models the mechanical damping due to air resistance and friction.

F_e represents the restoring force on the mass due to electromechanical feedback when an interface circuit is connected to the transducer. This force causes extra electrical damping, d_e . The additional electrical damping plays an important role in the energy conversion mechanism. The work done by the seismic mass against the restoring force is converted into electrical energy [87]. The uppermost limit of the power generation from a transducer is contingent upon the damping force [92]. For instance, if the external vibration is fixed and centered around a single frequency, a low damping factor would be necessary to obtain higher power generation, whereas, in case the vibration frequency diverges with respect to time, a higher damping factor would be more beneficial to broaden the bandwidth. Luckily, it is possible to control the damping factor to achieve the optimum performance by changing the electrical load connected to the transducer or similarly varying the input impedance of the interface circuit [93].

The studies on piezoelectric energy harvesting in the literature concentrates on different aspects. For example, the authors in [94] studied the multiple piezoelectric bimorph configurations for broadband piezoelectric energy harvesting. They employed different piezoelectric bimorphs with different aspect ratios and operating frequencies. Two important outcomes have been observed in terms of PZT connection patterns. The first observation is that the operating frequency band of the harvesting structure can be widened out by configuring the bimorphs with different aspect ratios in series. The second observation is operating frequency band of the harvesting system can be shifted towards the ambient vibration frequency domain by varying the bimorphs connected in parallel. In another study [95], a piezoelectric interface circuit has been proposed for wireless remote power supply. The interface circuit is composed of an AC-DC rectifier, a switch-mode DC-DC converter, and a 3V electrochemical battery. The DC-DC converter is employed to control the direction of the power flow. An adaptive control technique is used for the DC-DC converter to transfer maximum available power from the harvester at any given time. The authors claim that power transfer is boosted by %400 when the adaptive DC-DC step-down converter is utilized compared to the case in which it is not employed.

The same group of authors presented another work [96] utilizing a DC-DC step-down converter in discontinuous conduction mode to optimize the duty cycle that maximizes the extracted power from the harvester. The difference of this study from the previous one [95] is its simpler design as the previous study of the authors has the bottleneck of empowering the adaptive control circuitry while maintaining to provide sufficient power level for an additional electronic load. The work [96] claims that the duty cycle of the converter becomes constant as the excitation force increases, which makes the control of the step-down circuitry relatively easier. The authors show a %325 increase in extracted power from the transducer by accurately predicting the optimal duty cycle compared to the case in which the step-down converter is not utilized. In [97], a self-powered interface circuit to harvest energy from acoustic vibration by using MEMS PZT has been proposed. The circuit is adaptable to the different vibration levels, i.e. provides minimum power losses when the input power is limited and adjusts itself well when higher input power levels are achieved. 180 nm high-voltage CMOS process technology has been used to implement the interface circuit. It is reported that the proposed system achieves %84.4 charging efficiency when the excitation frequency is 390 Hz, PZT open-circuit voltage is 4.75 V, and the input power is 78 μ W. Moreover, the charging efficiency stays around %47 when the input power is 3.12 μ W.

Figure 2.11 (b) presents the electrical equivalent circuit of a PZT. The model consists of a current source in parallel with an output capacitor. Parallel resistance R_{par} represents the parasitics due to dielectric losses since the output capacitor is not a perfect insulator. The normative value of the resistor R_{par} is higher than 10 M Ω and usually neglected [87]. The output power of a PZT is ultimately dependent on the ambient vibration magnitude, material characteristics, and cantilever structure. In addition, as the output power is in AC form, AC-DC rectifiers are essential building blocks of piezoelectric energy harvesting interface circuits. However, since the output impedance of the piezoelectric transducers is capacitive, it is relatively high ($\sim 200 \text{ k}\Omega - 10 \text{ M}\Omega$) [23]. This hinders the development of more effective front-end interface circuits and rectifiers, and further studies are required.

Table 2.2 Comparison of the kinetic energy conversion mechanisms [79], [98].

Type	Practical Max. Energy Density	Aggressive Max. Energy Density	Advantages	Disadvantages
Electromagnetic	24.8 mJ/cm ³	400 mJ/cm ³	Simple interface Low output impedance No external source needed	Low output voltage for small circuits
Electrostatic	4 mJ/cm ³	44 mJ/cm ³	Easy integration	External source needed
Piezoelectric	35.4 mJ/cm ³	335 mJ/cm ³	No external source needed	Complex interface High output impedance

2.4 Ambient Radio Frequency (RF) Harvesting

Newly, ambient RF harvesting has drawn significant attention since RF sources have become ubiquitous and abundantly available in most environments [4]. Although the available power density is comparatively limited for ambient RF harvesting as presented in Table 2.1, the amount of harvested energy could still be enough to power up WBSN platforms, particularly when they operate in low duty-cycle mode [99]. In fact, wireless power transfer has two fundamental categories: near-field and far-field. Near-field power transfer is realized through inductive coupling or magnetic resonance coupling technique, whereas far-field power transfer is realized through the utilization of antennas [24]. Since near-field power transmission requires calibration and resonator alignment, they are not quite useful for remote charging. On the other hand, far-field power transfer is very useful for empowering a large number of WSNs and/or WBSNs in a wide area thanks to the employment of antennas [100]. Figure 2.12 depicts an example of an embedded wireless energy harvesting system to harvest digital TV signals. As one can realize, a typical wireless energy harvesting system is composed of an antenna, impedance matching circuit, rectifier, battery/supercapacitor, and μ CU. Generally, the full system is referred to as the rectifying antenna, so-called rectenna, since it converts RF signals to the usable DC power [101]. The conversion efficiency of a quintessential RF harvesting system varies between %50 and %75 over a 100 m range of input power [99], [102].

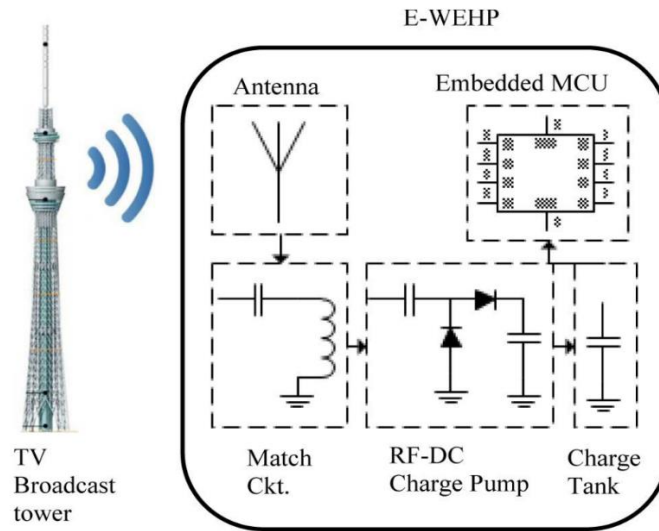


Figure 2.12. Embedded wireless energy harvesting prototype for digital TV signal harvesting [103].

Some harvestable ambient RF sources are listed below [104]:

- AM Radio Band (550 kHz – 1605 kHz)
- FM Radio Band (87.5 MHz – 108 MHz)
- TV Band (41 MHz – 950 MHz)
- GSM Band (0.85 GHz – 0.90 GHz and 1.8 GHz – 1.9 GHz)
- CDMA Band
- 3G Band
- 4G Band
- ISM Band (2.4 GHz)
- WiFi Band (2.45 GHz and 5.8 GHz)

Among these omnipresent ambient RF sources, GSM and WiFi are commonly explored in the literature. Regular antenna sizes for these frequency bands in the range of 10-50 cm² and lower frequency broadcasting signals require relatively larger antennas for rectenna operation [105]. Besides the antenna size and efficiency, impedance matching, device parasitics, harmonic generation, and threshold and reverse-breakdown voltage of non-linear devices are important parameters to decide the overall efficiency of the harvesting system [106].

Table 2.3 Comparison of some ambient RF sources [104].

Source	Efficiency	Energy Level	Limitation
GSM	Low	mW	0 – 100m
TV	Low	μ W	0 – 4 km
WiFi	Low	nW - μ W	0 – 10 m
AM	Low	μ W - mW	0 – 20 km

There are alluring studies in the literature to convert RF into DC power. For instance, in [107], passive rectifier circuitry has been designed by using floating gate transistors as rectifying diodes. The authors proposed a 36-stage rectifier implemented in 0.25 μ m CMOS technology to convert RF signals in the frequency range of 902 – 928 MHz into DC power. It has been reported that the overall system can rectify input voltage as low as 50 mV. The voltage conversion ratio for this input level has been stated as 6.4. The system can operate as long as the input power is 5.5 μ W or higher. With the optimization for a far-field operation, the circuit could work at a distance of 44 meters from a 4W effective isotropic radiated power (EIRP) source. In another work [108], the authors proposed an integrated input matching network and 17-stage rectifier by exploiting a fully passive threshold self-compensation scheme for RF signals at 915 MHz. The circuitry has been implemented in 90 nm CMOS technology, and the results have shown that the circuit can deliver 1 V DC output voltage to a capacitive load when the input power level is as low as 4 μ W. Moreover, the authors achieved 1.2 V DC output with 13.1 μ W input power when the circuit is driving 1 M Ω load. In [109], a broadband 1 x 4 quasi-Yagi antenna array and a dual-band rectifier have been implemented to harvest RF signals in GSM-1800 and UMTS-2100 bands. The authors reported that with the dual-tone input power density of 455 μ W/m², a DC output voltage of 224 mV had been achieved with %40 power conversion efficiency when driving a 5 k Ω resistive load. It has also been mentioned that 300-400 mV DC output could be obtained by harnessing relatively low ambient RF power.

To sum up, ambient RF harvesting is a promising and sustainable solution to empower WBSNs thanks to the ubiquitous availability of RF signals. On the other hand, ambient RF provides very low power density, and they are thoroughly sensitive to the distance of the radiation source that makes their implementation relatively harder. However, they offer efficient and fully integrated rectenna solutions thanks to the studies on efficient integrated antenna design and shrinking semiconductor technology. Therefore, it is reasonable to expect further studies on RF energy harvesting systems in the future as the ambient RF signals will continue to be part of our daily lives.

2.5 Hybrid Energy Harvesting

Basically, hybrid energy harvesting is the utilization of multiple ambient energy sources to extract further electrical power from each source simultaneously. Considering WBSNs, there are multiple ambient sources that can be harvested, such as temperature gradient between the body and ambient, vibration due to body movement, solar light, and surrounding ambient RF signals. However, it is not an easy study as much as it sounds. Every energy harvesting transducer has inherent electrical and material characteristics that bring different limitations [110]. Hence, interface circuit designers must be aware of the characteristics of different harvesters to harness power from multiple sources.

Endeavors on hybrid energy harvesting systems will be provided in this paragraph to provide an insight to the reader. A multiple-input DC-DC converter topology has been suggested by [111]. The proposed circuit topology supports buck, boost, and buck-boost modes of operations. Furthermore, the converter provides a positive output voltage without any need for additional transformers and can bidirectionally operate without any additional converters. A single inductor is shared by multiple inputs to reduce the number of components and circuit size. This topology or similar topologies are very beneficial to simultaneously harvest multiple energy sources like solar and temperature gradient that provide DC output by using a single converter.

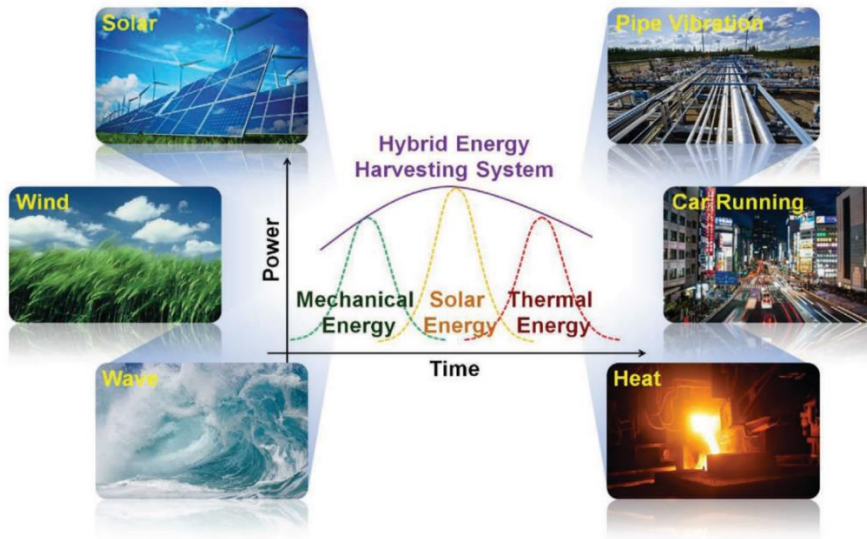


Figure 2.13. Sustainable hybrid energy harvesting system illustration [112].

Another work [113] proposes a circuit to harvest indoor light and temperature gradient by using a single power management circuit. The authors reported $621 \mu\text{W}$ output power, a triple of that with the conventional thermal energy harvesting method when indoor solar irradiance is 1010 lux, and temperature gradient is 10°K . In [114], the authors suggested a system comprising of piezoelectric and magnetostrictive transducers. The authors aimed to expand vibration bandwidth by combining two different harvesting systems. The proposed harvesting scheme achieves 6.53 V output at the resonance frequency of 59.6 Hz. A triple hybrid micropower generator has been presented in [115]. Electromagnetic, piezoelectric, and thermoelectric energy harvesting circuits have been combined into a single DC supply. The full system achieves 1.2 V and $24 \mu\text{W}$ while driving a load resistance higher than $50 \text{ k}\Omega$ and can generate up to $110 \mu\text{W}$ output power. Moreover, endeavors on the integration of multiple transducers in material levels have been summarized in [112].

In conclusion, hybrid energy harvesting is an upcoming trend in energy scavenging to extend onboard features and communication range of WBSNs [1]. However, further studies are needed to create a standalone system and implement a single power supply module with multiple sources.

CHAPTER 3

INTERFACE CIRCUIT DESIGN

A brief introduction to energy harvesting interface circuit design and fundamentals of energy harvesting methods have been provided in Chapter 1 and 2, respectively. As discussed previously, a constant temperature gradient between the human body and the surrounding environment makes thermoelectric energy harvesting relatively more applicable for WBSNs. Another advantage of this type of harvesting is that TEGs provide DC output power, which does not require rectification. Therefore, this study focuses on thermoelectric energy harvesting interface circuit design to power up WBSNs. In this chapter, a fully integrated autonomous interface circuit design for thermoelectric energy harvesting is presented to extract 1 mW power from TEGs. The circuit consists of a DC-DC converter and an MPPT circuitry. The details of the subcircuits are going to be delivered in the following sections, together with the related work in the literature. However, it is beneficial to define interface circuit efficiency, output power, and DC-DC converter types to clear the aim of this work.

The power budget is very stringent for low-power energy harvesting interface circuits. Thus, efficient circuit design with minimum energy losses is one of the key challenges for circuit designers. The efficiency of an interface circuit is defined as:

$$\eta = \frac{P_{out}}{P_{in}} \times 100 = \frac{V_{out}I_{out}}{V_{in}I_{in}} \times 100 \quad (3.1)$$

In fact, it is possible to talk about two different efficiencies for any given energy harvesting system. End-to-end efficiency can be described as the overall efficiency in which losses due to the internal resistance of micro-power generators are taken into account. We can also define interface circuit efficiency, which only considers the input and output power of an interface circuit. Both will be provided in this study.

Even though efficiency is a substantial term for the evaluation of feasibility, output voltage and power are likewise vital. If the output voltage or power requirement of a load cannot be met by the energy harvesting system, efficiency loses its importance. Hence, this work first aims to obtain an output power in the range of mW, which could be adequate for most WBSNs with or without duty cycling mode.

The typical output voltage of a standard TEG is only a couple of hundred millivolts. This voltage level is not enough to power electronic circuits. Therefore, DC-DC converters are the essential blocks for this type of energy scavenging to boost up the output voltage. Conventionally, there are two types of DC-DC boost converters: Traditional boost converters with inductors and switching transistors and charge pump based boost converters. The first type of converters utilize inductors as energy storage elements, and the output voltage level is set by the duty cycle of the switching transistors. Although traditional boost converters provide high efficiency and high output power, the necessary inductor size is significantly larger than the maximum inductor size that can be integrated on a chip. Contrarily, charge pump based boost converters employ capacitors as energy storage elements. The capacitors are used to transfer the stored energy from one stage to another. Hence, a higher number of charge pump stages can achieve higher output voltage since a stage voltage is determined by the accumulation of previous stage voltages. Despite the fact that existing capacitors substantially contributes to the dynamic power dissipation ($P_{loss_dyn} = CV^2f$), ease of integration favors the utilization of this converter topology. Since the aim of this work is proposing a compact, low-cost, low-power, robust, and reliable interface circuit, which can be realized through integration, charge pump based topology is chosen as the conversion mechanism.

3.1 Charge Pump Circuits

As briefly explained above, charge pump DC-DC converters are favorable for energy harvesting interface circuits since they provide ease of integration. Fully integrated solutions are very desirable; they are even inevitable for implant WBSN applications.

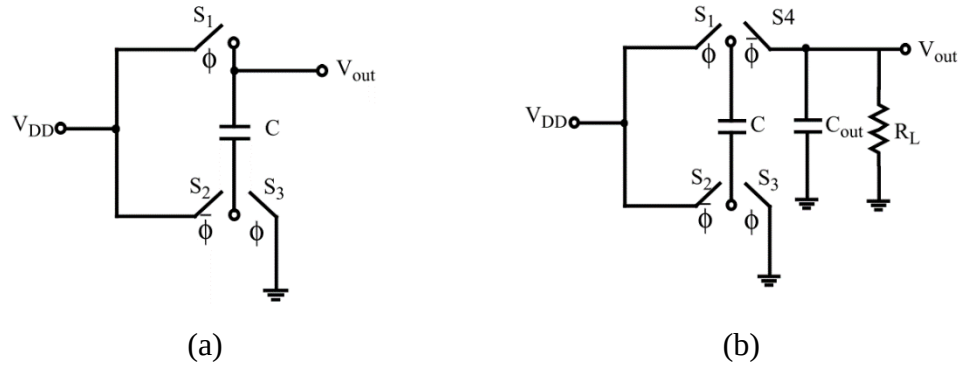


Figure 3.1. Voltage doubler (a) simple circuit diagram (b) practical circuit diagram with the RC load [116].

Charge pump circuits generate a voltage level higher than its input voltage. In [116], the author explains how this is possible by using a simple voltage doubler circuit depicted in Figure 3.1 (a). Two out of phase signals are used to control the switches. During the clock phase ϕ , the capacitor is charged up to V_{DD} since S_1 and S_3 switches are closed. Then, S_1 and S_3 switches are opened, and S_2 is closed in the second clock phase. While the capacitor maintains its charge from the previous phase ($C \times V_{DD}$), the bottom plate of the capacitor has a potential of V_{DD} . During the second clock:

$$V_{DD}C = (V_{out} - V_{DD})C \quad (3.2)$$

Therefore;

$$V_{out} = 2V_{DD} \quad (3.3)$$

As one can realize that the output of the charge pump is double that of the input voltage when there is no load. On the other side, the voltage doubler circuit with RC load has been presented in Figure 3.1. (b). It can be seen that the circuit has been modified to have four switches. The ideal output voltage for this circuit is:

$$V_{out} = \frac{2V_{DD}C}{C + C_{out}} \quad (3.4)$$

The presence of a variable resistance R_L generates output voltage ripple. This unwanted ripple voltage may be suppressed by increasing the load capacitance, C_{out} . Yet, equation (3.4) shows that this arrangement also reduces the output voltage.

Figure 3.2 below shows the Cockcroft-Walton charge pump topology, one of the first charge pump topologies. The aim of the topology is obtaining an output voltage, which is more than double the input. It has been achieved by cascading multiple capacitors serially. When S_1 and S_2 switches are tied to the ground and node 2, respectively, C_1 and C_4 are charged by the input voltage, V_{in} . Once the switches change their position, C_4 shares its potential with C_2 , and they both have equal potential, $V_{in}/2$ (assuming capacitance value of all capacitors are the same). Then, S_1 and S_2 switches are tied again to their primary positions, ground, and node 2, so that capacitor C_4 and C_5 are charged up to V_{in} and $V_{in}/4$, respectively, since C_4 is connected to the input and C_2 and C_5 are tied in parallel by this arrangement. If this procedure is repeated for a couple of cycles more, the charging and charge sharing process continues until $3V_{in}$ potential is achieved at the output terminal [72]. Even though the approach seems straightforward and extendable for higher output voltage levels by adding more capacitors, the efficiency of the topology drops significantly for more transistors in series because of large on-chip stray capacitance in case the circuit is implemented in monolithic form. Additionally, the output impedance substantially increases with the addition of more capacitors [116].

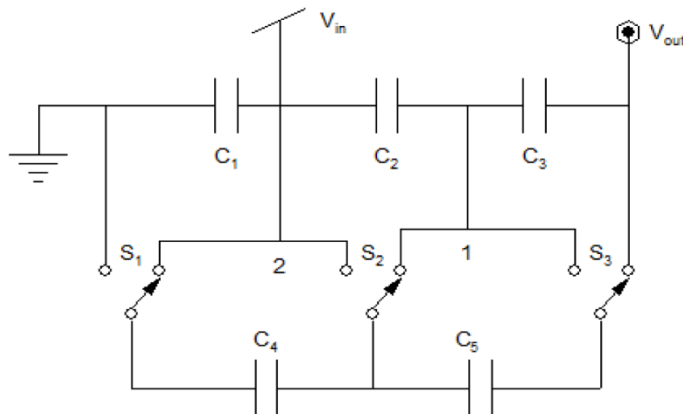


Figure 3.2. Cockcroft-Walton charge pump circuit [72].

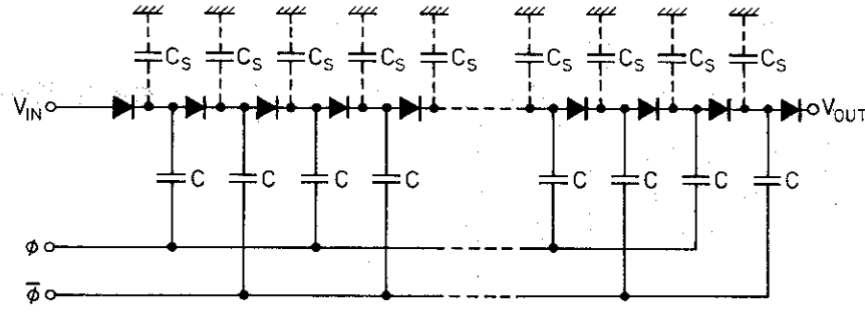


Figure 3.3. Dickson charge pump circuit [117].

Cockcroft-Walton charge pump circuit topology has been revised by Dickson to eliminate the associated problems. Dickson charge pump topology has been illustrated in Figure 3.3. Lower capacitors, denoted as “C,” are charged and discharged in accordance with the two out-of-phase clock signals. By taking advantage of the unidirectional behavior of diodes, each stage voltage C_S is charged by the previous stage voltage, except the first stage, to deliver one stage potential to another. In the end, each stage would benefit from this charge transfer by having higher potential than its previous. This resolves the problem related to the stray capacitance existence and enables efficient monolithic form implementations. In addition, the total number of multiplier stages does not affect the circuit’s drive capability [116]. In order to increase the integration feasibility of this topology for ultra-low-voltage applications, diodes, and stray capacitors could be replaced by MOSFETs and junction parasitic capacitances [118]. The output voltage of NMOS connected Dickson topology is given by [119]:

$$V_{out} = V_{in} + \frac{C}{C + C_s} NV_{CLK} - (N + 1)V_t \quad (3.5)$$

where V_{out} , V_{in} , C , C_s , N , V_{CLK} , and V_t represents charge pump output voltage, source voltage, charge pump capacitance, parasitic capacitance in each stage, the total number of stages, clock signal (ϕ) amplitude, and MOSFET threshold voltage, respectively. Among these parameters, the MOSFET threshold voltage plays an important role in the gain and efficiency of the circuit.

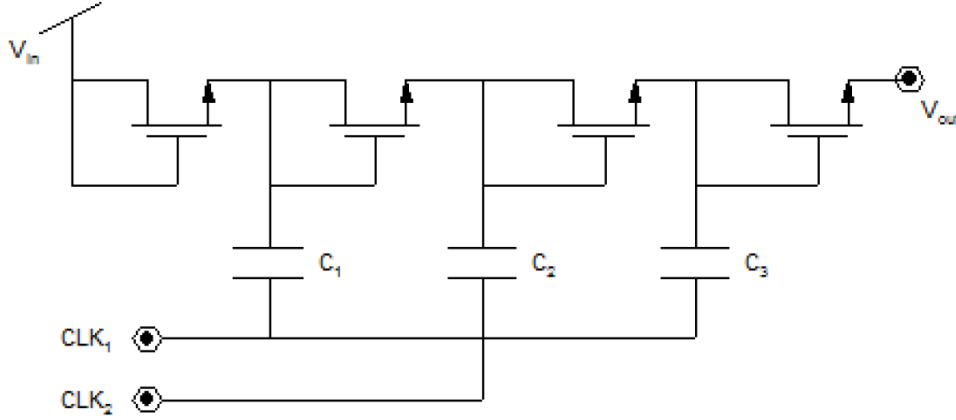


Figure 3.4. Dickson charge pump by using NMOS switches [72].

The threshold voltage of a standard MOSFET device can be described as [120]:

$$V_t = V_{t0} + \gamma(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}) \quad (3.6)$$

where V_{t0} is the zero-bias threshold voltage, γ is the body effect coefficient, V_{SB} is the source to bulk potential difference, and ϕ_F is surface potential. Generally, in most low-cost CMOS process technologies, the body of the device is tied to the ground. Thus, source to bulk potential increases with the number of charge pump stages resulting in a significant increase in threshold voltage. This means the voltage drop in each stage increases proportionally. Furthermore, the leakage current of each MOSFET has a huge impact on the efficiency and gain of the converter. As a result, Dickson charge pump topology is not the most proper solution for ultra-low-voltage circuits, and further improvements are needed for higher gain and better efficiency.

3.2 Dual-Phase Charge Pump Circuit

In order to overcome the limitations of Dickson charge pump topology, there are plenty of optimization studies in the literature. Some of them are briefly summarized and discussed in [121]. One of the most interesting topologies, which is also the core of the charge pump structure we are going to utilize, has been presented in [122].

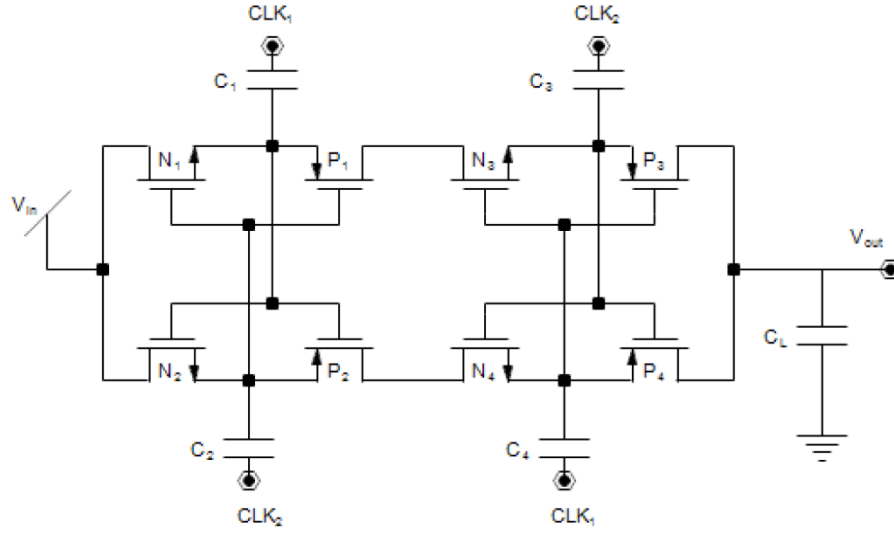


Figure 3.5. Dual-phase cross-connected charge pump topology [122].

The circuit in Figure 3.5 has been proposed to solve the threshold voltage drop issue associated with Dickson charge pump topology. Each stage is composed of two cross-coupled NMOS and PMOS pairs and two capacitors. Out-of-phase clock signals drive the charge pump switches to accumulate charge on the capacitors. Then, this charge is transferred to the next stage with high efficiency. The working principle of the circuit relies on MOSFET fully “ON” and “OFF” switching. Therefore, the leakage current is minimized. When CLK_1 is low and CLK_2 is high, N_2 and P_1 are OFF, whereas N_1 becomes ON. Hence, C_1 is charged until it reaches the source voltage amplitude. In opposite clock signal configuration, N_2 becomes ON, whereas N_1 and P_2 are turned OFF, resulting in a series connection between the source and the capacitor C_2 . Meanwhile, the source of N_1 achieves $2V_{in}$ thanks to the series connection of C_1 and clock signal. Simultaneously, P_1 is switched “ON” and allows the charge transfer to the second stage. Similar behavior is observed on the other side of the circuit as the clock signals oscillate. If we assume an ideal scenario in which the threshold voltage drop is zero and there is no clock signal attenuation, the output voltage of an N -stage charge pump can be found by:

$$V_{out_N} = V_{in} + NV_{CLK} \quad (3.7)$$

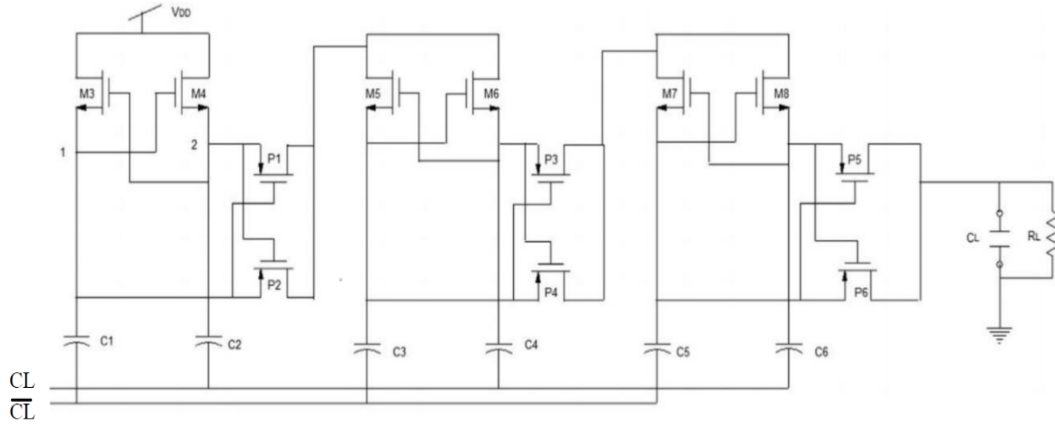


Figure 3.6. Charge pump topology utilized in the interface circuit [123].

Although dual-phase cross-coupled charge pump topology is an attractive approach for low voltage applications, achieving the threshold voltage of the MOSFETs could be challenging for ultra-low voltage applications. Moreover, the maximum voltage swing between two consecutive charge pump stages may reach $2V_{in}$ leading to a voltage overstress on the gate oxide. The version which has been designed by the METU NCC Energy Harvesting team and employed in this study with some modifications is illustrated in Figure 3.6. High-performance, low V_t MOSFETs are used to start the circuit even with very low input voltages. However, this substantially increases the overall power consumption. Thus, model-based optimization for circuit parameters has also been proposed to decrease the leakage in [123]. Figure 3.7 shows the circuit's working principle.

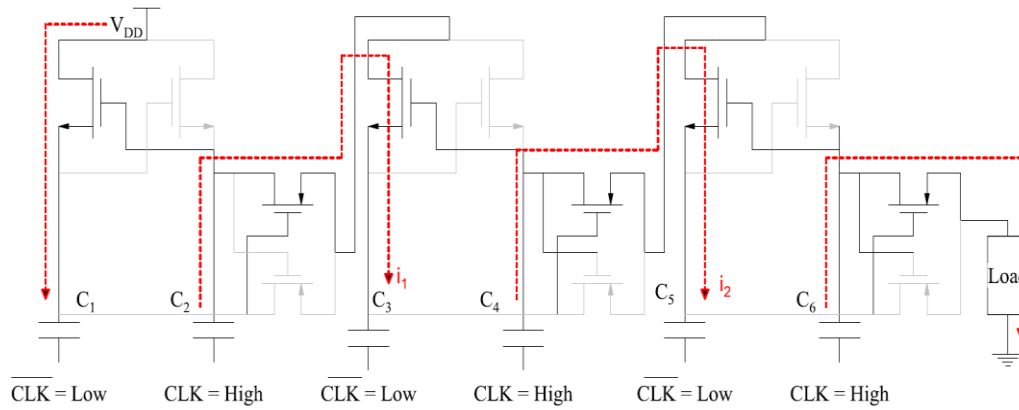


Figure 3.7. Three-stage charge pump circuit working principle [124].

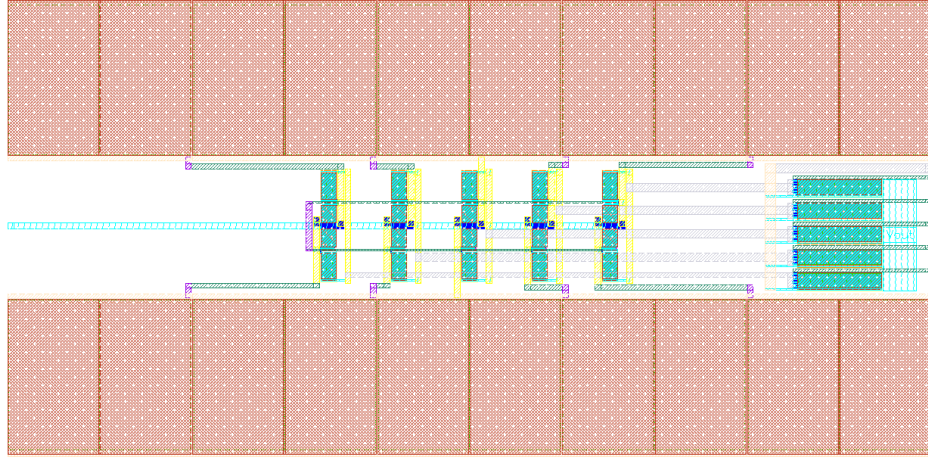


Figure 3.8. Five-stage reconfigurable charge pump layout (277x558 μm^2).

3.3 Charge Pump Clock Signal Generation

Out-of-phase clock signals are crucial for charge pump circuits and profoundly affect the output voltage, as shown in equation (3.7). Oscillating clock signals not only charge the flying capacitors but also control the charge pump MOSFET switches. For this reason, low phase noise and high gain oscillating signal generators are of great importance for the charge pump DC-DC converters.

It is essential to understand how a circuit can oscillate. Simply, negative feedback systems might oscillate; in other words, oscillators are poorly designed feedback amplifiers [125]. The transfer function of the oscillatory system in Figure 3.9 is:

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 + H(s)} \quad (3.8)$$

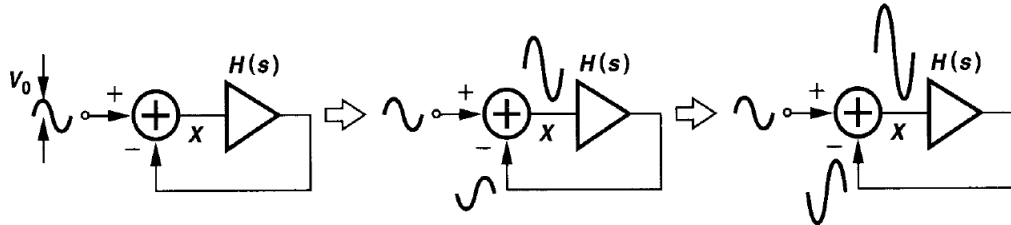


Figure 3.9. Oscillatory system evaluation with time [125].

If a negative feedback system has a loop gain which satisfies the following two criteria, so-called Barkhausen criteria, then the system may oscillate at ω_0 .

$$|H(j\omega_0)| \geq 1 \quad (3.9)$$

$$\angle H(j\omega_0) = 180^\circ \quad (3.10)$$

Oscillators could be divided into two major categories depending on the shape of the oscillating signals; square-wave oscillators and sine-wave oscillators. The most typical examples of the square- and sine- wave oscillators for microelectronic systems are ring and LC tank oscillators, respectively, and they are briefly introduced in the following subsections together with their pros and cons.

3.3.1 Ring Oscillators

Ring oscillators are composed of an odd number of CMOS inverters with short-circuited input and output configuration. This configuration allows a total phase shift of 360° or equivalently $\angle H(j\omega_0) = 180^\circ$ for a negative feedback loop, which satisfies the Barkhausen criteria. The ideal voltage swing of the oscillation signal is $0 - V_{in}$.

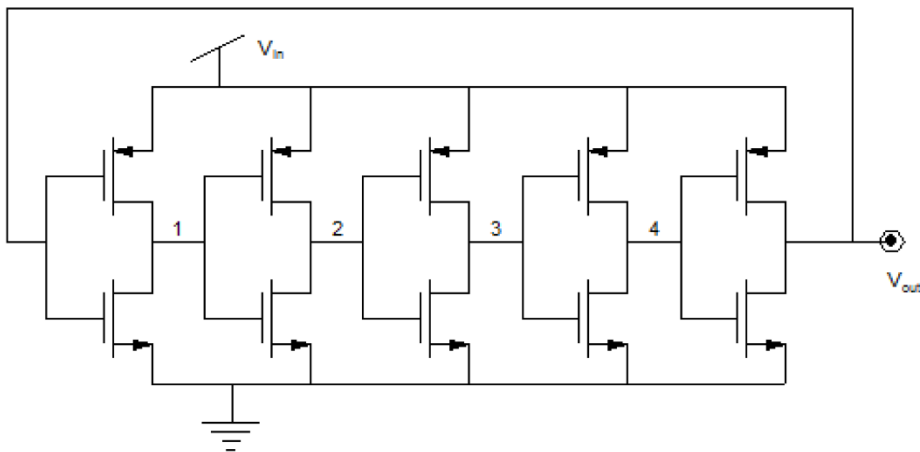


Figure 3.10. Five-stage CMOS ring oscillator circuit diagram [72].

The frequency of a ring oscillator is a function of inverter chain propagation delay and could be controlled through the bias current. Assuming the propagation delay of a single inverter is t_{pd} , then the oscillation frequency of an N-stage ring oscillator is:

$$f = \frac{1}{2Nt_{pd}} \quad (3.11)$$

As the reader can realize from the equation (3.11), frequency is inversely proportional to the total number of inverter stages. This is an important advantage for the circuits that require high-frequency clock signals. Ease of integration and its smaller structure compared to its counterparts make ring oscillators attractive for most applications. On the other hand, ring oscillators have a couple of disadvantages. These can be summarized as follows:

- Clock signal amplitude is limited by the input signal.
- Operation failure is observed when the input voltage is less than the MOSFET threshold voltage, which is typical for low voltage applications.
- A large number of buffer circuits required to swell out current drivability of the oscillator causes a consequential dynamic and static power dissipation.
- Environmental conditions affect the inverter propagation delay leading to undesirable variations in oscillation frequency.

To conclude, despite its compact structure, performance deterioration of ring oscillators, exclusively in ultra-low voltage applications, has led researchers to investigate alternative oscillator circuits.

3.3.2 LC Tank Oscillators

As the name states, LC tank oscillators consist of inductors and capacitors and take advantage of LC resonance operation to sustain oscillation. They are commonly used in microwave and telecommunication applications [4]. The two-port network representation of a quintessential LC tank oscillator is illustrated in Figure 3.11.

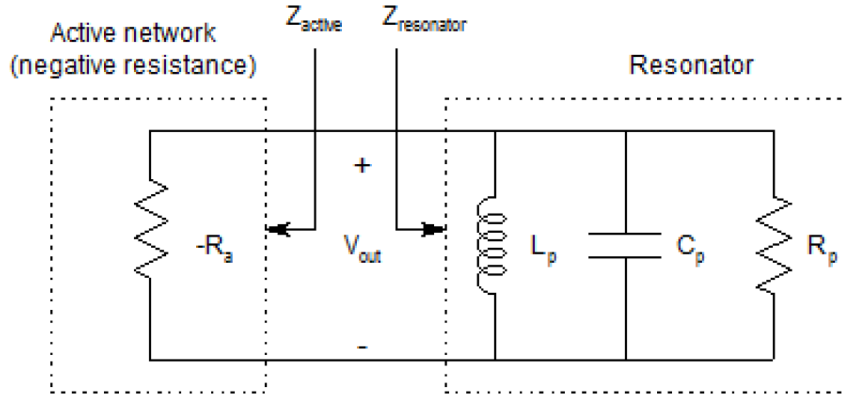


Figure 3.11. Two-port network representation of an LC tank oscillator [126].

L_p , C_p , R_p , and $-R_a$ represents the ideal inductance, ideal capacitance, parallel resistance to model resonator circuit real losses, and active network resistance, respectively. In order to maintain continuous oscillation, resonator real losses must be compensated by the active network negative resistance, i.e. summation of R_p and $-R_a$ should be zero. The resonator impedance, $Z_{resonator}$, can be derived by calculating the parallel combination of the resonator inductance, capacitance, and resistance:

$$Z_{resonator} = \frac{\omega^2 L_p^2 R_p + j\omega L_p R_p^3 (1 - \omega^2 L_p C_p)}{\omega^2 L_p^2 + R_p^2 (1 - \omega^2 L_p C_p)^2} \quad (3.12)$$

At the resonance frequency, capacitive and inductive reactances are equal to each other; therefore, the resonator impedance is going to be purely real. Hence, the resonant frequency, f_0 , can be found as:

$$f_0 = \frac{1}{2\pi\sqrt{L_p C_p}} \quad (3.13)$$

The necessary switching frequency of the charge pump MOSFETs is in the range of hundreds of MHz for constant charge delivery with minimum output ripple. Therefore, nH range on-chip inductors and pF range on-chip capacitors could be employed to generate the necessary oscillation by using a fully integrated approach.

However, integrated inductors occupy a significant chip area, and their parasitic resistance is substantially greater than their off-chip counterparts. Additionally, essential active network negative resistance has been implemented through cross-coupled NMOS or PMOS pairs by taking advantage of the current mirror principle. Hence, optimizations of inductors and MOSFETs are vital to reduce the parasitics and balance the real losses. Thus, design optimization methodology is mandatory to benefit from a fully integrated approach. There are good examples of design optimization works in the literature [127]–[129]. In this study, we are going to use an LC tank oscillator architecture to provide out-of-phase clock signals to the charge pump circuitry since LC tank oscillators could start operating with input voltage levels lower than MOSFET threshold voltage, which is extremely critical for ultra-low voltage applications, and their output voltage is able to exceed the supply voltage thanks to the presence of inductors. The oscillator architecture utilized in this work is elaborated in the following section.

3.4 Optimized Quadrupling LC Tank Oscillator Circuit

A novel voltage quadrupling LC tank oscillator architecture has been proposed by METU NCC Energy Harvesting team members in [72], [130]. Figure 3.12 depicts the advanced version of the quadrupling oscillator circuit. In the previous studies, the team has employed an additional capacitor to create two synchronously operating LC tank circuits: primary LC tank circuit consisting of L_1 and C_1 , secondary LC tank oscillator consisting of L_2 and C_2 . As the reader may realize, the version which is going to be used in this study does not include the external primary capacitor (C_1) and utilize cross-coupled NMOS pair parasitic capacitance instead. This saves the total chip area and eliminates the parasitic components that the external capacitor introduces. CLK_1 and CLK_2 terminals provide two out-of-phase sinusoidal clock signals, which is necessary for charge pumps. The advantage of this structure is that the CLK signal amplitude becomes at least four times larger than the DC supply voltage. Also, low phase noise and frequency stability are other prominent features.

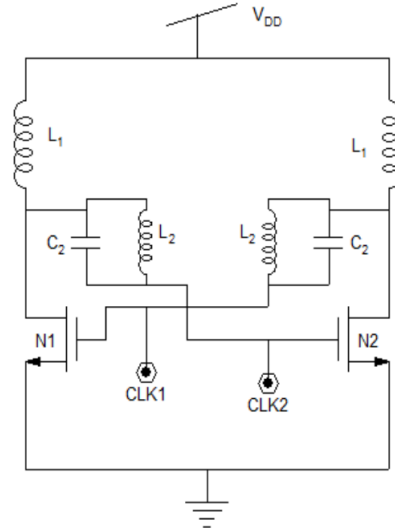


Figure 3.12. Voltage quadrupling LC tank oscillator used in this work.

The primary LC tank network works as a simple LC resonance circuit and provides voltage doubling. The details of this network could be found in [123]. The secondary LC tank operation principle has been summarized by [72], and the half-circuit model array showing the different states of the tank is illustrated in Figure 3.13 below. The capacitor C_L represents the effective capacitance between the clock node and AC ground, which is the addition of the secondary tank inductor and capacitor node capacitances, NMOS gate capacitance, and load capacitance. Assuming the capacitors are initially discharged, C_2 and C_L are fully charged once N_2 is turned off. Meanwhile, CLK_1 output is greater than the node A potential, which is expected to be more than $2V_{DD}$, as depicted in Figure 3.13 (a). Therefore, these two capacitors are discharged through L_2 by accumulating magnetic energy in the inductor. As the secondary capacitor also discharges simultaneously, there is no backward current flowing into the primary LC tank. Discharging of C_2 and C_L leads to the maximum current flow through the secondary inductor, while node A and CLK_1 potential become zero, as presented in Figure 3.13 (b). Later, L_2 starts sinking current in the same direction and charges the capacitors. However, N_2 is switched on in this time interval, and some of the current flow through the transistor sinking to the ground. In the end, CLK_1 reaches its most negative potential by hitting $-2V_{DD}$, as illustrated in Figure 3.13 (c). Afterward, the capacitors begin to discharge through the

secondary inductor. Simultaneously, the primary tank capacitor is fully charged, and the primary inductor current starts going through the secondary inductor since the CLK_1 potential is negative with respect to the ground connection in the NMOS drain. Fully discharged capacitors stop sinking current, and zero potential at node A is transferred to CLK_1 point. By its nature, the inductor resists the change in current. Hence, L_2 releases the stored magnetic energy by generating current in a clockwise direction. This inductor current charges the capacitors, yet the current passing through the C_2 capacitor sinks to the ground since the transistor is on, and the ground potential is conveyed to node A, as shown in Figure 3.13 (d). Thenceforth, N_2 is turned off, and C_2 current diminishes. In the meantime, CLK_1 voltage rises, and most of the current start flowing through the load, as depicted in Figure 3.13 (e). Accordingly, C_L current peaks and eventually boosts the CLK_1 potential further. The boosted potential at CLK_1 with respect to node A curtails the current going through C_L and increases the current flowing through C_2 once again in a clockwise direction. CLK_1 voltage peaks at $4V_{DD}$ when C_L is fully charged, as shown in Figure 3.13 (f). The layout implementation of the quadrupling oscillator is presented in Figure 3.14.

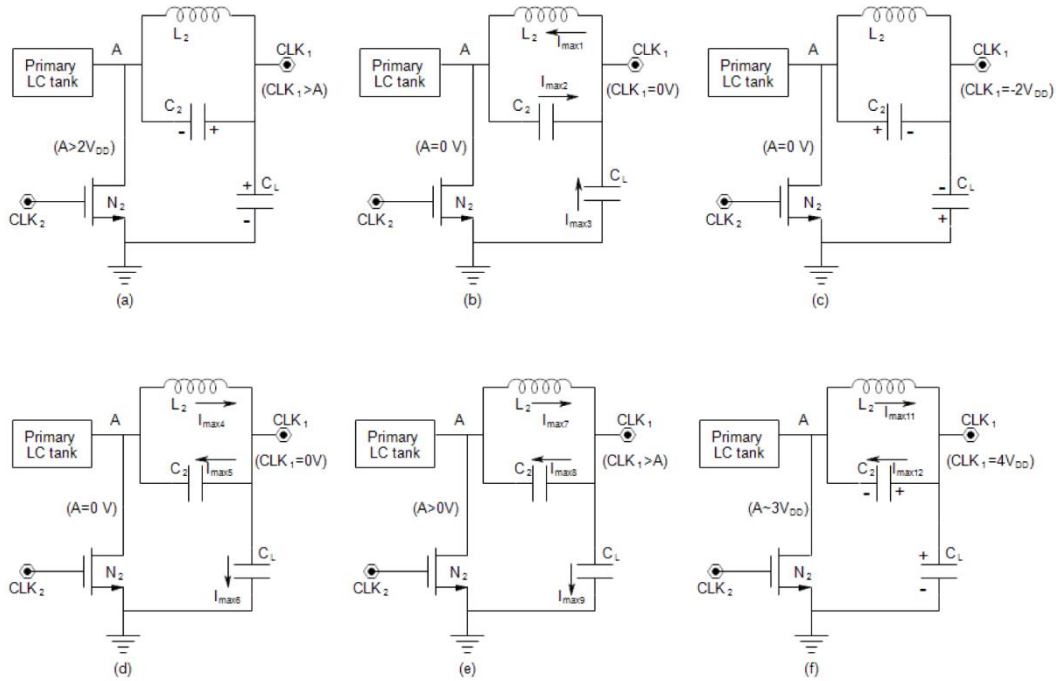


Figure 3.13. Secondary LC tank analysis by using half-circuit models [72].

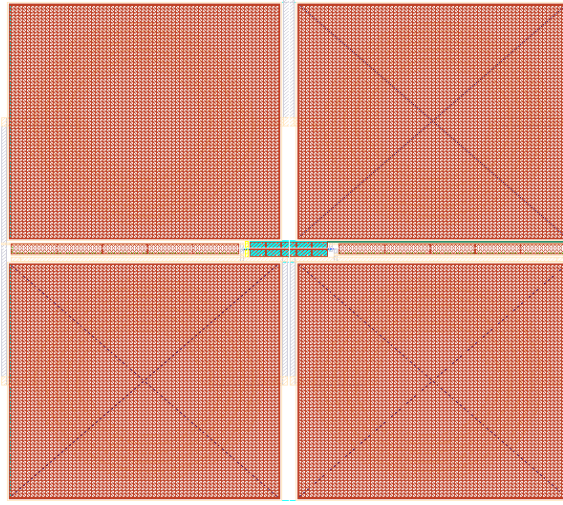


Figure 3.14. Voltage quadrupling LC tank oscillator layout ($1200 \times 1200 \mu\text{m}^2$).

3.5 DC-DC Converter Architecture

The proposed DC-DC converter topology is presented in Figure 3.15. It consists of a voltage quadrupling LC tank oscillator and a five-stage charge pump circuit. The subcircuits have been introduced in the previous sections. However, one can realize that there are five additional PMOS devices attached to the output of each charge pump stage. This structure has been proposed by [131] to adjust the input impedance of the charge pump circuit by controlling the path to the output. The aim is to keep track of MPP. MPPT algorithm and circuit details are provided in the next section.

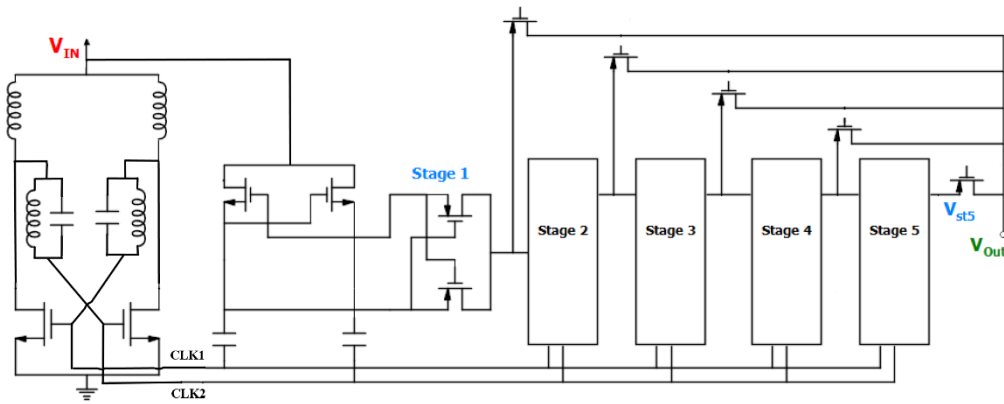


Figure 3.15. Proposed DC-DC converter with reconfigurable charge pump.

3.6 Maximum Power Point Tracking

Maximum power point tracking is an output power optimization phenomenon by providing impedance matching between the source and the load. In the context of this study, the source and the load are the thermoelectric generator and the interface circuit, respectively. As explained in Chapter 2, thermoelectric generators can be modeled as an independent voltage source, V_{TEG} , in series with a resistance, R_{TEG} . V_{TEG} represents the open-circuit voltage, and R_{TEG} represents the output resistance of the micro-power generator.

In WBSN applications, the temperature gradient, ΔT , between the human body and the ambient is employed. Typically, the temperature difference between the cold and hot surface of TEGs is very limited and vary from less than 0.5 °K to more than 10 °K depending on the ambient temperature, physical activity of the person, and so on [67], [68]. Fluctuating temperature gradient alters the output power and impedance of the harvester. Therefore, MPPT utilization becomes inevitable, particularly for WBSNs in which ΔT is limited.

Usually, maximum power point tracking for TEG applications is performed by measuring open-circuit voltage and setting the interface circuit input voltage to half of the open-circuit voltage [132]–[134]. However, these MPPT mechanisms involve disconnecting TEGs from interface circuits to sample TEG open-circuit voltage and/or interface circuit input voltage. As a consequence, there are cutoffs in power delivery to the output; thus, a storage element is needed for continuous power supply. This increases the system volume and complexity. Also, the differences between charge pumps with ring oscillators and charge pumps with LC tank oscillators should be taken into consideration. Load impedance or the number of charge pump stages does not affect voltage peak-to-peak and the oscillation frequency of ring oscillators. In contrast, they affect LC tank oscillators since their output impedance is much higher than the output buffering stage of a standard ring oscillator. As a result, the input impedance of a charge pump circuit with an LC tank oscillator is nonlinear, and it should be taken into account as well for MPP tracking.

A novel MPPT algorithm and circuitry was proposed by the METU NCC Energy harvesting team in [135] for charge pump-based DC-DC converters driven by LC tank oscillators. The idea takes advantage of the inversely proportional relationship between the charge pump input impedance and the number of charge pump stages. On the other hand, changing the number of charge pump stages simultaneously alters output power, efficiency, input impedance, and dynamic and static power dissipations. Besides, a higher number of charge pump stages increases the loading of the LC oscillator, leading to a decrease in oscillation peak-to-peak amplitude. Therefore, the proposed MPPT algorithm keeps track of the maximum power point by considering all these facts and refraining from disconnecting TEGs.

An adjustable number of charge pump stages is created by adding a minimum number of PMOS switches to the system. Using the minimum number of switches and optimized low V_t PMOS devices minimize the leakage current and voltage drop, respectively. The reconfigurable charge pump is employed to change the number of charge pump stages connected to the load while the stage voltage is maintained since there is no disconnection among the paths. To control these switches, a control circuitry consisting of a digital MPPT block, a comparator, and a regulator circuit is implemented. The control circuitry is powered by the charge pump stage-5 voltage, the maximum available voltage in the system for any given input voltage.

Although there is a direct relationship between the number of charge pump voltage boost stages and voltage conversion ratio (VCR) for a fixed excitation clock (oscillator output) amplitude, higher, the number of charge pump stages reduces the oscillation amplitude in this system, causing a decrease in output voltage. Hence, there is a certain number of stages providing the maximum output voltage, therefore the maximum output power, for each specific load. The maximum input power delivered to the interface circuit happens when the output impedance of the oscillator is equal to the input impedance of the interface. Therefore,

$$P_{in,MAX} = \frac{(V_{TEG})^2}{4R_{TEG}} \quad (3.14)$$

From equation (3.14), we can interpret that the utilization of micro-power generators with lower R_{TEG} values maximizes the deliverable input power. Yet, TEGs with low R_{TEG} suffer from low Seebeck coefficients requiring a higher temperature gradient, ΔT , to reach the minimum startup voltage. Thus, it is reasonable to accept that maximum input power depends only on V_{TEG} and R_{TEG} and is fixed for any given ΔT . So, it is essential to maximize the amount of power delivered to the load so that the efficiency of the system increases. The overall system efficiency can be calculated by:

$$\eta = \frac{P_{out}}{P_{in,MAX}} = \frac{\frac{(V_{out})^2}{R_L}}{\frac{(V_{TEG})^2}{4R_{TEG}}} = \left(\frac{V_{out}}{V_{TEG}}\right)^2 \times \frac{4R_{TEG}}{R_L} \quad (3.15)$$

As the reader may realize, optimization of output voltage for any given ΔT would maximize the output power and efficiency. Hence, the MPPT algorithm tries to find the optimal number of charge pump stages to maximize output power. It is worth emphasizing that increasing the number of charge pump stages does not always increase the output voltage since it also affects the loading on the LC tank oscillator. Moreover, unlike the conventional inductive boost converter topology in which the efficiency is constant for all impedance values, matching charge pump input impedance with harvester output impedance does not guarantee the maximum power extraction in this topology as the change in input voltage alters the efficiency. Thus, the ultimate goal is to maximize output power for any pair of V_{TEG} and R_L .

Furthermore, the output voltage must be regulated for batteryless operations. Therefore, any voltage level higher than the target voltage is stepped down to the desired level by using low dropout (LDO) voltage regulators. Achieving the target voltage with the minimum number of charge pump stages is one of the goals since it minimizes the circuit losses and decreases the oscillator loading effect.

By considering all the facts mentioned above, the proposed MPPT algorithm aims to follow two major rules:

1. Delivering the target output voltage by searching the charge pump stages;
2. Reducing the number of charge pump stages while maintaining the target output voltage to reduce the circuit losses.

The MPPT algorithm is depicted in Figure 3.16. The solid lines show the searching path followed to reach the target voltage and the dashed lines illustrate the stage minimization path while maintaining the target output voltage. Plainly, the MPPT starts searching from stage-5. The reason for that is enabling cold startup even with very low supply voltage levels. Afterward, the output is compared with the target voltage. In case the output voltage is less than the target voltage, the number of stages is decreased by one so that the loading effect on the oscillator is reduced by increasing the charge pump input impedance leading to higher input voltages. This may lead to a higher output voltage. The algorithm checks whether the target voltage is achieved or not after each stage reduction. When the target voltage is found, the stage will be selected; yet MPPT continues working on finding the minimum number of stages to achieve the same target voltage. If the target voltage is found with a lower number of stages, the circuit is locked in that stage, and MPPT is turned off.

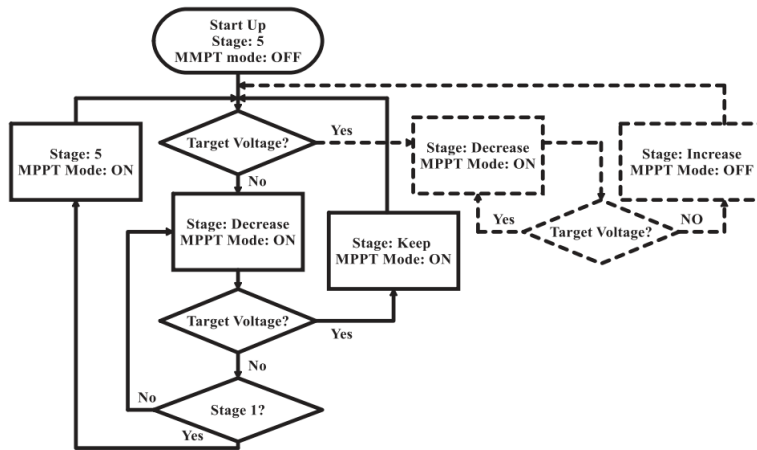


Figure 3.16. Novel MPPT algorithm for charge pump-based DC-DC converters driven by LC tank oscillator [135].

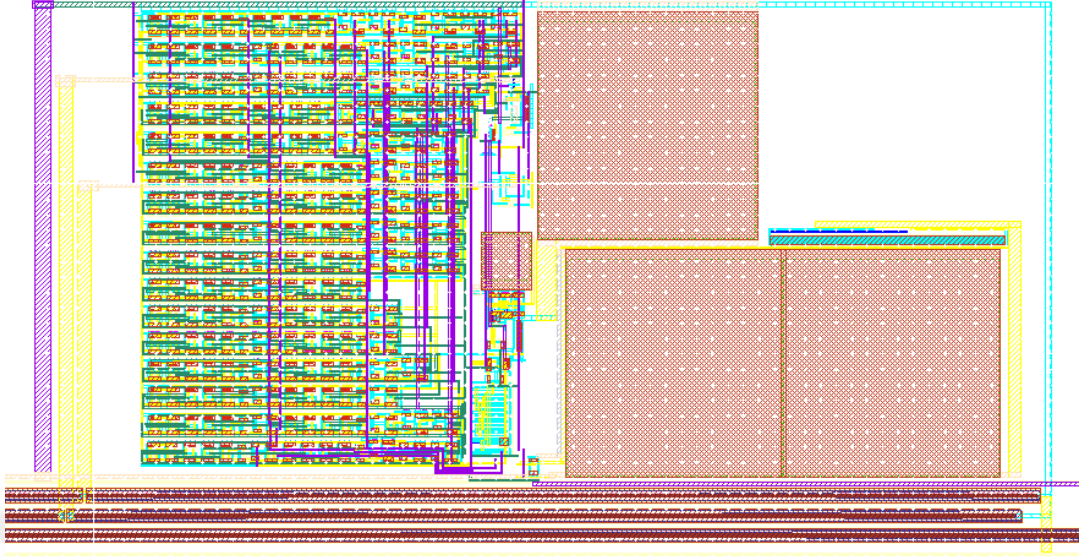


Figure 3.17. MPPT circuitry layout (179x329 μm^2).

3.7 Fully Integrated Milliwatt Interface Circuit Design

A fully integrated autonomous interface circuit design for milliwatt range power extraction from TEGs is presented in Figure 3.17. The circuit consists of a five-stage charge pump driven by the voltage quadrupling LC tank oscillator and an MPPT circuitry, which is composed of a digital MPPT block, a comparator, and a voltage regulator. A subthreshold finite state machine (s-FSM) is used to implement the MPPT algorithm with minimum power consumption. Charge pump stage-5 voltage, V_{st5} , is used to power the control circuitry. As long as V_{TEG} hits the minimum startup voltage, the initialization circuit sets the output of the s-FSM to the stage-5 potential for high VCR and activates the MPPT block. The outputs of the MPPT block is used as an input to the multiplexers controlling the PMOS switches. Once the MPPT_n signal is high ($n=2,3,4,5$ as it is unlikely to achieve the target voltage with a single-stage charge pump), V_{Reg} is selected. In that case, stage- n is going to be open, and the op-amp, together with the PMOS switches, creates an LDO regulator to set the output voltage to the desired level. This voltage level can be configured through adjustments to the voltage reference circuit.

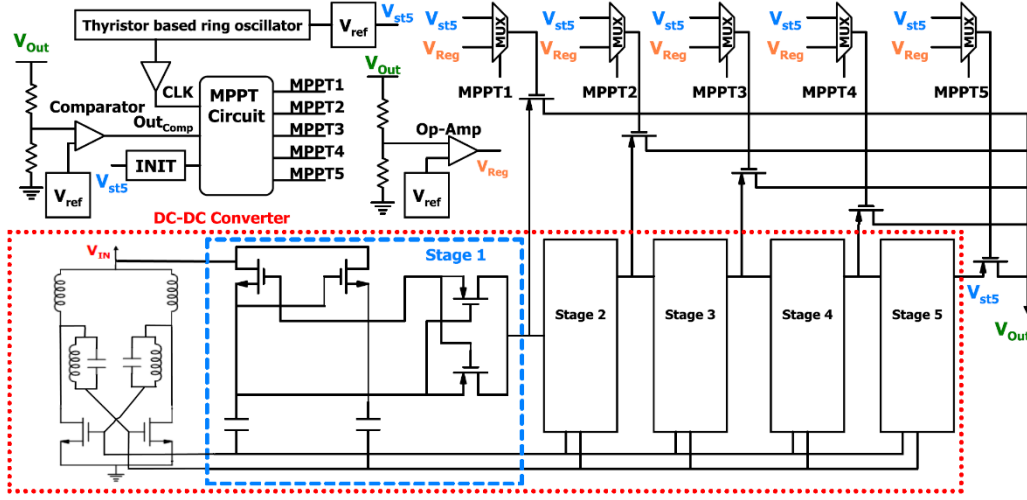


Figure 3.18. Fully integrated autonomous power management circuit design for milliwatt range power extraction from TEGs.

The layouts of the five-stage reconfigurable charge pump, voltage quadrupling LC tank oscillator, and MPPT circuitry in UMC 180 nm CMOS process technology are depicted in Figure 3.8, Figure 3.14, and Figure 3.17, respectively. The five-stage reconfigurable charge pump circuit occupies a chip area of 0.15 mm^2 , whereas the oscillator occupies 1.44 mm^2 . Furthermore, the MPPT occupies an area of 0.06 mm^2 . The total chip shown in Figure 3.19 occupies a chip area of 1.89 mm^2 without pads. Therefore, despite the large on-chip inductors, which are essential to achieve milliwatt range output power, the power management circuit can be fully integrated for a low-cost, low-power, and reliable solution for powering up WBSNs.

To sum up, a fully integrated autonomous milliwatt interface circuit design for thermoelectric energy harvesting is optimized in this study as an advanced version of the work presented by the METU NCC Energy Harvesting team in [135]. In the previous version, the maximum output power of 0.5 mW has been reported by the team members, which is the state-of-the-art among the fully integrated solutions. In this work, we are aiming to achieve higher output power in the milliwatt range to enable batteryless standalone WBSNs architectures. The next chapter presents the model-based verification and simulation results of the proposed interface circuit.

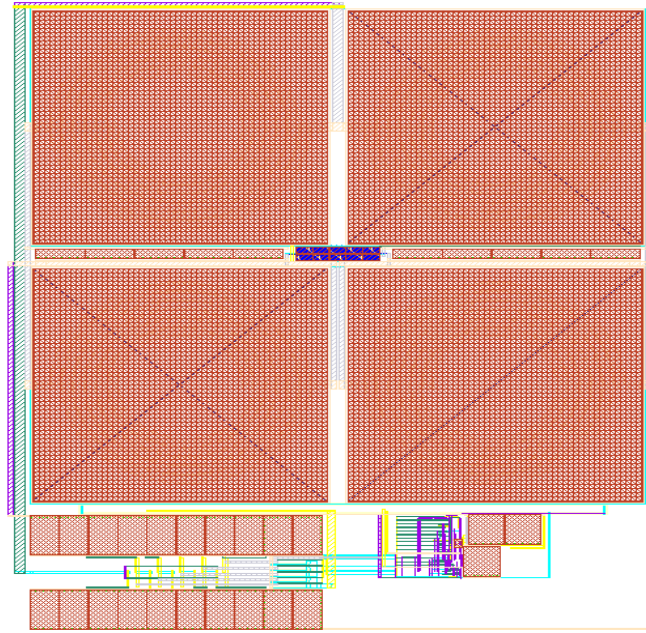


Figure 3.19. Full system layout implementation (1243x1521 μm^2).



CHAPTER 4

CIRCUIT VERIFICATION

In this chapter, a model-based circuit analysis of the DC-DC converter is introduced. Simulation results for the model verification are presented. Furthermore, the DC-DC converter and fully autonomous power management circuit with MPPT are simulated to achieve milliwatt range output power. Efficiencies and output powers for different conditions are examined in detail. Additionally, the minimum startup conditions for both architectures are investigated by using UMC 180 nm standard CMOS process technology in Cadence IC Design suite.

4.1 DC-DC Converter Model-based Analysis

The proposed DC-DC converter architecture is composed of a five-stage charge pump circuit and a voltage quadrupling LC tank oscillator for charge pump clock generation. In order to optimize the converter, transfer function and frequency calculation of the oscillator must be derived. Figure 4.1 below depicts the half-circuit small-signal model of the voltage quadrupling LC tank. L_1 and L_2 represent the primary and secondary tank inductors. R_{p1} is the equivalent parallel resistance of the primary inductor series resistance, whereas R_{s2} is the secondary inductor self-resistance. C_1 is the sum of the parasitic capacitances at the NMOS drain terminal. C_2 represents the secondary tank capacitor. Lastly, C_L models the effective capacitance between the CLK node and AC ground. According to this model, the transfer function of the voltage quadrupling LC tank oscillator is:

$$\frac{V_o}{V_{in}} = \frac{-g_m}{\frac{(1 - \omega^2 L_2 (C_2 + C_L))}{(1 - \omega^2 L_2 C_2) R_{p1}} + j \left[\frac{(1 - \omega^2 L_2 (C_2 + C_L))}{(1 - \omega^2 L_2 C_2)} \left(\omega C_1 - \frac{1}{\omega L_1} \right) - \omega C_L \right]} \quad (4.1)$$

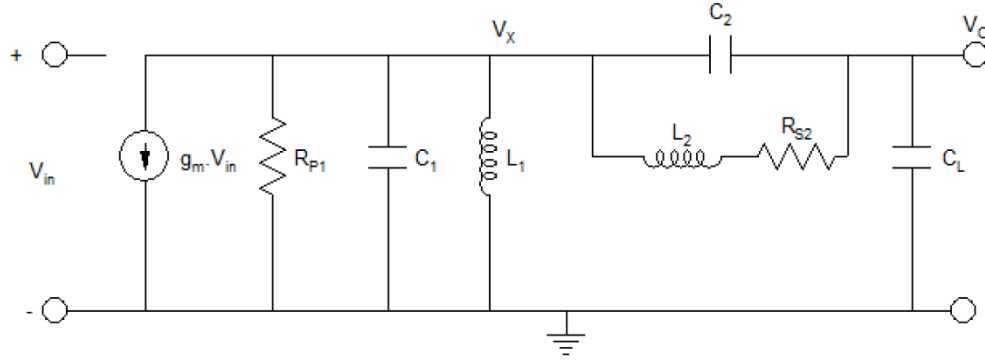


Figure 4.1. Quadrupling LC tank oscillator half-circuit small-signal model [72].

The phase shift between CLK₁ and CLK₂ outputs has to be π . Therefore, the frequency could be derived by using the imaginary part of the equation (4.1). Hence,

$$\omega^4 \{L_1 L_2 [C_1 C_2 + C_L (C_1 + C_2)]\} - \omega^2 [L_1 C_1 + L_2 C_2 + C_L (L_1 + L_2)] + 1 = 0 \quad (4.2)$$

where,

$$\omega^2 = \frac{b \pm \sqrt{b^2 - 4a}}{2a} \quad (4.3)$$

$$a = L_1 L_2 [C_1 C_2 + C_L (C_1 + C_2)] \quad (4.4)$$

$$b = L_1 C_1 + L_2 C_2 + C_L (L_1 + L_2) \quad (4.5)$$

Equation (4.3) yields two positive solutions for ω ; however, the following two conditions must be satisfied:

$$b^2 \geq 4L_1 L_2 [C_1 C_2 + C_L (C_1 + C_2)] \quad (4.6)$$

$$\omega^2 < \frac{1}{L_2 (C_2 + C_L)} \quad (4.7)$$

So, the angular frequency, ω , can be written as:

$$\omega = \sqrt{\frac{b - \sqrt{b^2 - 4a}}{2a}} \quad (4.8)$$

where a and b are defined by equation (4.4) and equation (4.5), respectively.

The accuracy of the model-based frequency analysis has been tested by changing the primary and secondary tank capacitors. The voltage quadrupling LC oscillator parameters are presented in Table 4.1. The primary capacitor section is intentionally left NA since no external capacitor is utilized. The capacitance needed for the primary LC tank operation is created by using the NMOS drain parasitics. The parasitic capacitance at the drain terminal can be altered by changing the multiplier. Each multiplier adds roughly 1.72 pF capacitance to the drain terminal for this design in UMC 180 nm technology. In this circuit, the NMOS multiplier of 5 is chosen to create approximately 8.6 pF primary capacitance. Moreover, the gate capacitance of the NMOS device is equally important to calculate the frequency since C_L parameter in the frequency equation contains the gate parasitic capacitance. In our design, the gate capacitance for the given size of the transistor is found roughly 1.8 pF based on the simulation results. By using these parameters, model-based calculations are performed by keeping one capacitor fixed and the other one sweeping. The simulation results with no load are also shown in Figures 4.2 and 4.3. The results are accurate, yet the discrepancy increases slightly as the capacitance increases because of the simplifications made for equation derivations and neglected small parasitics.

Table 4.1 Voltage quadrupling LC tank oscillator circuit parameters.

Component	Parameters	UMC Technology Cell Name
NMOS pair	W/L = 600 μ m/240 nm Multiplier = 5	N_LV_18_MM
Inductors	Inductance = 14 nH Width = 20 μ m Diameter = 238 μ m Turn = 5.5	L_SLCR20K_RF
Primary Capacitor	NA	NA
Secondary Capacitor	10 pF	MIMCAPS_MM

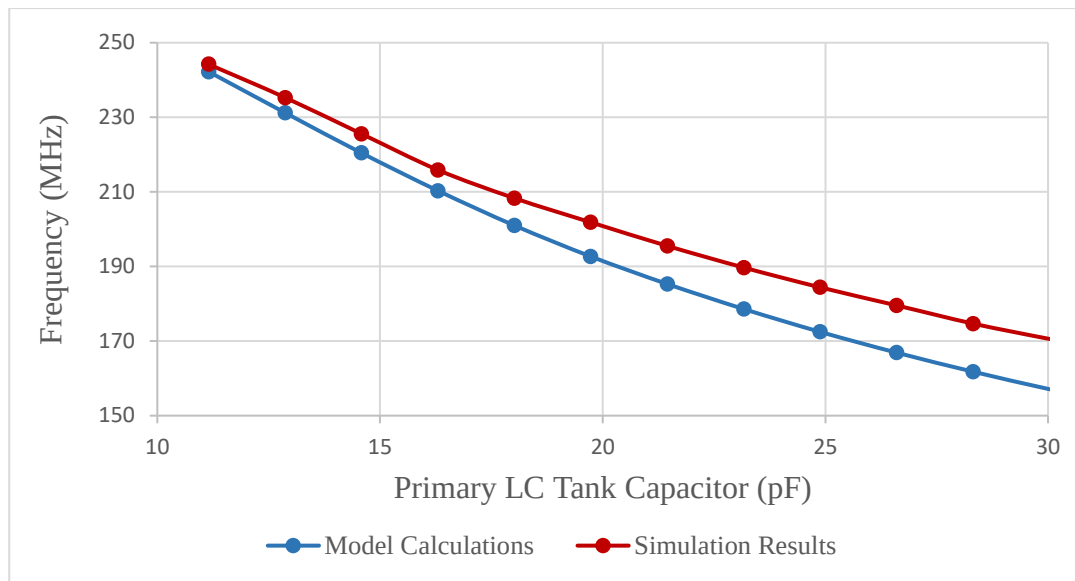


Figure 4.2. Oscillation frequency variation with respect to primary capacitor.

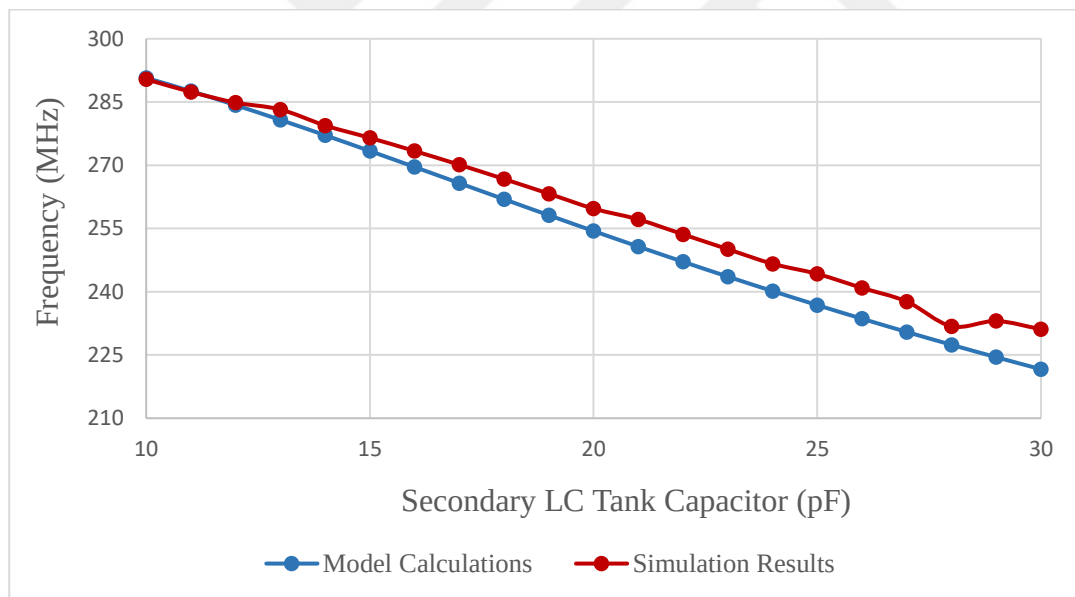


Figure 4.3. Oscillation frequency variation with respect to secondary capacitor.

Another important criterion is the impedance matching between the LC tank and the charge pump circuit. Model-based analysis of the impedance matching allows minimum size circuit elements, which reduces the energy losses. Figure 4.4 illustrates the lumped-element half-circuit model of the N-stage DC-DC converter. L_1 , R_{P1} , and C_{L1} represent the primary LC tank inductance, inductor parallel resistance, and NMOS drain parasitic capacitance. L_2 , C_{L2} , and R_{S2} model the secondary LC tank inductance, secondary LC tank capacitance, and the inductor series resistance. C_p is the total capacitance at LC oscillator NMOS gate terminal referenced to AC ground, including the corresponding equivalent parallel capacitance of the first stage charge pump. On the other side, the charge pump switches are modeled as series resistances. Their parasitic capacitances are ignored for this model. The last stage of the charge pump includes only one flying capacitor, one PMOS ON resistance, and the load resistance (R_L). First, we can start by calculating the LC tank impedance. The total LC tank impedance can be divided into two: Primary LC tank impedance and secondary LC tank impedance. Starting from the primary LC tank impedance, Z_{LC1} :

$$(Z_{LC1})^{-1} = \frac{1}{\frac{1}{j\omega C_1}} + \frac{1}{R_{P1}} + \frac{1}{j\omega L_1} = \frac{j\omega C_1 R_{P1} j\omega L_1 + j\omega L_1 + R_{P1}}{R_{P1} j\omega L_1} \quad (4.9)$$

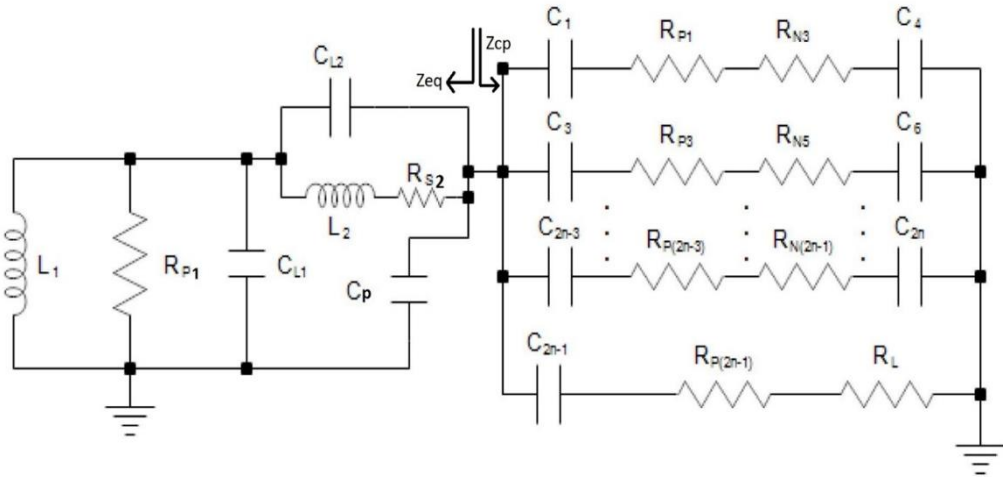


Figure 4.4. N-stage DC-DC converter lumped-element half-circuit model.

Therefore, the primary LC tank impedance can be written as:

$$Z_{LC1} = \frac{R_{P1}j\omega L_1}{R_{P1}(1 - \omega^2 L_1 C_1) + j\omega L_1} \quad (4.10)$$

Similarly, we can calculate the secondary LC tank impedance, Z_{LC2} as:

$$(Z_{LC2})^{-1} = \frac{1}{\frac{1}{j\omega C_2}} + \frac{1}{R_{S2} + j\omega L_2} = \frac{j\omega C_2 j\omega L_2 + j\omega C_2 R_{S2} + 1}{R_{S2} + j\omega L_2} \quad (4.11)$$

Hence,

$$Z_{LC2} = \frac{R_{S2} + j\omega L_2}{1 - \omega^2 L_2 C_2 + j\omega C_2 R_{S2}} \quad (4.12)$$

As the primary and secondary LC tank impedances have been calculated, the total LC tank impedance can be derived as:

$$Z_{LC} = Z_{LC1} + Z_{LC2} = \frac{R_{P1}j\omega L_1}{R_{P1}(1 - \omega^2 L_1 C_1) + j\omega L_1} + \frac{R_{S2} + j\omega L_2}{1 - \omega^2 L_2 C_2 + j\omega C_2 R_{S2}} \quad (4.13)$$

It is clear that the total impedance at the oscillator side (denoted as Z_{eq}) is the parallel combination of Z_{LC} and C_p . So, the total LC tank impedance, Z_{eq} , is:

$$Z_{eq} = \left(\frac{1}{\frac{1}{j\omega C_p}} + \frac{1}{Z_{LC}} \right)^{-1} = Z_{eq} = \frac{Z_{LC}}{j\omega C_p Z_{LC} + 1} \quad (4.14)$$

It is worth noting that the series resistance of the inductor is found as 1.25Ω from the simulation results. In order to achieve the impedance matching, the quadrupling oscillator impedance should be equal to the five-stage charge pump impedance. Thus, the charge pump impedance, Z_{CP} , is calculated as:

$$Z_{CP} = Z_{CP1} // Z_{CP2} // Z_{CP3} // Z_{CP4} // Z_{CP5} = \frac{1}{\sum_1^n \left(\frac{1}{Z_{CPn}} \right)} \quad (4.15)$$

Each charge carrying path network impedance can also be written as:

$$Z_{CP1} = (R_{P1} + R_{N3}) - j\left(\frac{1}{\omega C_1} + \frac{1}{\omega C_4}\right) \quad (4.16)$$

$$Z_{CP2} = (R_{P3} + R_{N5}) - j\left(\frac{1}{\omega C_3} + \frac{1}{\omega C_6}\right) \quad (4.17)$$

$$Z_{CP3} = (R_{P5} + R_{N7}) - j\left(\frac{1}{\omega C_5} + \frac{1}{\omega C_8}\right) \quad (4.18)$$

$$Z_{CP4} = (R_{P7} + R_{N9}) - j\left(\frac{1}{\omega C_7} + \frac{1}{\omega C_{10}}\right) \quad (4.19)$$

$$Z_{CP5} = (R_{P9} + R_L) - j\left(\frac{1}{\omega C_9}\right) \quad (4.20)$$

By using the provided equations together with the frequency calculation, we try to match the quadrupling oscillator output impedance with the charge pump input impedance to achieve the maximum power transfer and minimize the energy losses. Table 4.2 presents the five-stage charge pump circuit design parameters. The reader may recall the oscillator parameters by reviewing Table 4.1. Charge pump NMOS and PMOS devices have been characterized in simulations to find their ON resistance, which is important for impedance calculation and circuit optimization. The last version of the PMOS and NMOS devices provide 40 Ω and 15 Ω ON resistances, respectively.

Table 4.2 Five-stage charge pump circuit design parameters.

Component	Parameters	UMC Technology Cell Name
Charge Pump NMOS	W/L = 100 μm /240 nm Multiplier = 1	N_LV_18_MM
Charge Pump PMOS	W/L = 150 μm /240 nm Multiplier = 1	P_LV_18_MM
Charge Pump Capacitors	10 pF	MIMCAPS_MM

Figure 4.5 illustrates the variation of DC-DC converter output power with load resistance when the supply voltage is 0.2 V. As one can realize from the figure, the output power peaks at 6 k Ω load resistance by reaching approximately 300 μW . To confirm the impedance matching, a calculator has been created. Then, the oscillator and charge pump impedances were calculated. The results show that the quadrupling oscillator output impedance (43.44 Ω) and charge pump circuit input impedance (43.40 Ω) are very close to each other at 6 k Ω . Hence, impedance matching could be achieved for any given load by using this analytical model calculator.

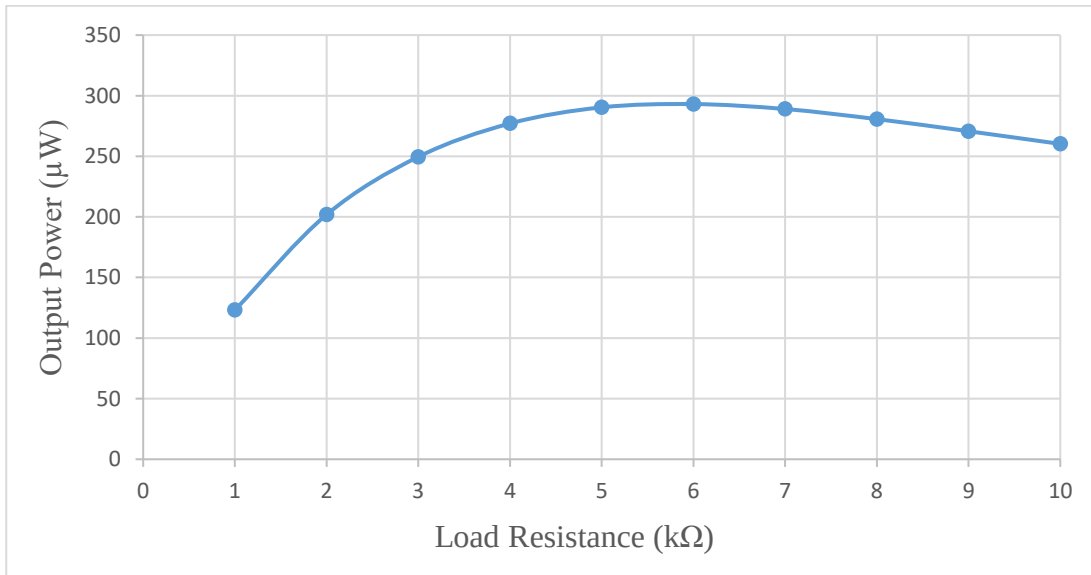


Figure 4.5. DC-DC converter output power variation with load for 0.2V input.

4.2 DC-DC Converter Simulation Results

In this section, simulation results for the DC-DC converter are provided. The converter has been simulated in Cadence using UMC 180 nm standard CMOS technology. In order to obtain accurate results, the electrical model of a real-life TEG has been used. TECTEG brand TEG2-126LDT model thermoelectric generator has been employed since it provides high output voltage with low-temperature gradients, and it is particularly designed for wearable applications. The performance characterization of TEG2-126LDT is presented in [70]. The matched load resistance of the model is mentioned as 5-6 Ω in the corresponding paper and the datasheet of the product. Thus, a series resistance of 5 Ω per TEG is used for the simulations.

4.2.1 Pre-Layout Simulation Results

Figure 4.6 depicts the stage outputs of the DC-DC converter for the minimum startup condition. The converter starts providing a voltage boost when TEG voltage reaches 96.5 mV. It has been assumed that this voltage can be achieved with only one TEG, and 1 M Ω load has been used for the simulation. Under these circumstances, the average interface circuit input voltage becomes 90.77 mV. Even with this input, the converter can provide 1.3 V output voltage by employing a 5-stage charge pump.

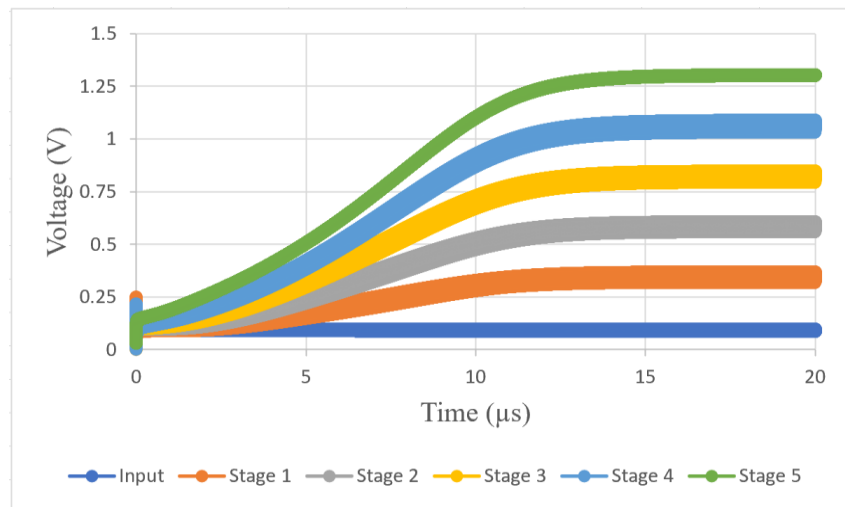


Figure 4.6. DC-DC converter stage outputs for the minimum startup condition.

Figure 4.7 shows the converter simulation to extract 1 mW output from the TEG. In practice, the TEG model provides a maximum of 353 mV output voltage when the temperature gradient is 20 °C between the hot and cold surfaces. Since 20 °C temperature gradient is not a probable condition, it has been assumed that at least two TEGs would be necessary to reach approximately these voltage levels. Therefore, an independent voltage source in series with 10 Ω series resistance has been utilized to perform the corresponding simulation. The results prove that the converter can achieve 1 mW output power at 4 k Ω load resistance in parallel with 10 pF capacitor when the TEG voltage is 361 mV, which could be achieved with a temperature gradient a little bit higher than 10 °C. For this condition, the interface circuit input becomes 239.11 mV, output voltage hits 2.00 V, and the output current reaches 501.25 μ A. If we assume that the temperature gradient is lower than 10 °C, and three TEGs are necessary, which means TEG series resistance of 15 Ω , then the output power becomes 1 mW when the input voltage is 415 mV. In this particular point, input voltage, output voltage, and output current become 229.21 mV, 2.00 V, and 500.42 μ A, respectively. The result is observed with the same load, 4 k Ω resistor, in parallel with 10 pF capacitor.

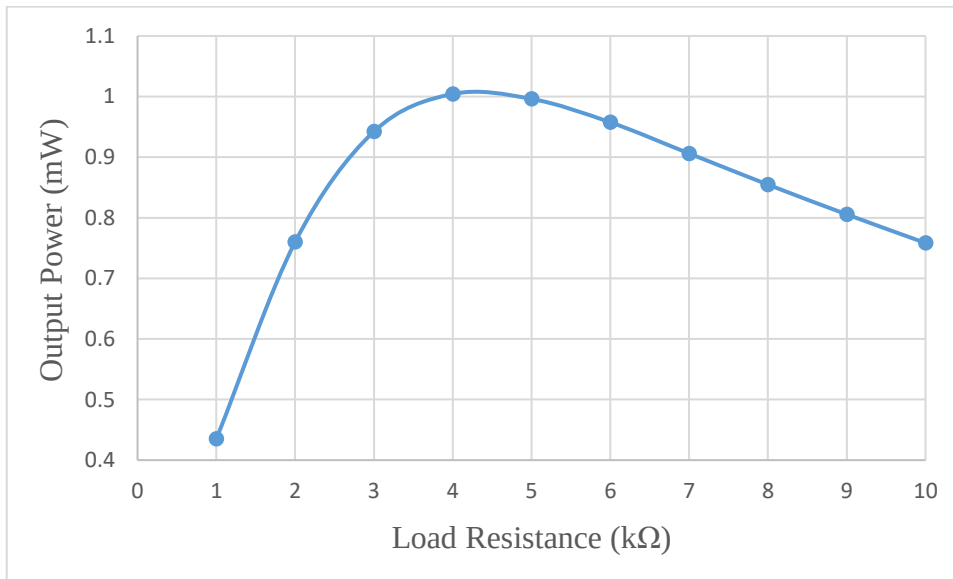


Figure 4.7. DC-DC converter simulation for 1 mW output power.

Moreover, it is possible to place three serially connected TEGs in a human body, thanks to the compact structure of the utilized TEG model ($40 \times 40 \text{ mm}^2$). Therefore, TEG output voltage may reach 500 mV easily when the temperature gradient is around 10°C , which is typical between the human body ($35.5\text{-}36.5^\circ\text{C}$) and room temperature ($20\text{-}25^\circ\text{C}$). Figure 4.8 depicts the output power simulation results for 500 mV input voltage. The output power peaks at 1.54 mW, which is enough to power up some WBSN architectures without duty cycling mode of operation, for $4 \text{ k}\Omega$ load resistor in parallel with 10 pF load capacitor. In this specific load condition, output voltage, output current, and input voltage are 2.49V, $620 \mu\text{A}$, and 271.25 mV, respectively. To sum up, two or three TEGs in series would be enough to extract 1 mW output power when the temperature gradient is around 10°C .

Figures 4.9 and 4.10 illustrates the interface and end-to-end efficiencies of the DC-DC converter architecture. The efficiency of the interface circuit (the converter without TEG) reaches more than 37% when the TEG voltage is 500 mV. On the other hand, peak interface efficiency is around 35% for the TEG voltage of 361 mV. The highest end-to-end efficiency of the converter for 500 mV TEG voltage is recorded as a little bit more than 20%. For the TEG voltage of 361 mV, the maximum end-to-end efficiency is observed as nearly 24%.

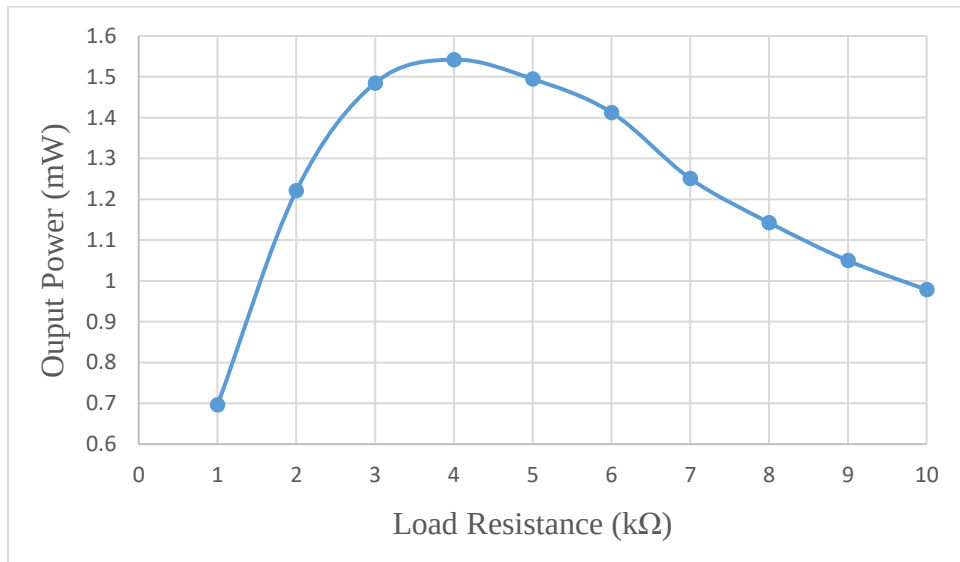


Figure 4.8. DC-DC output power for 500 mV TEG voltage.

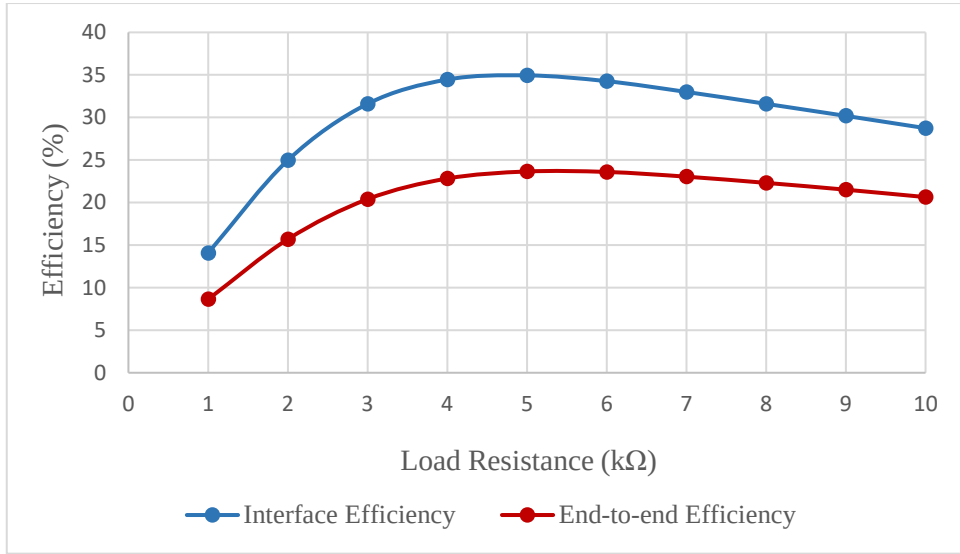


Figure 4.9. DC-DC converter efficiency with load for 361 mV TEG voltage.

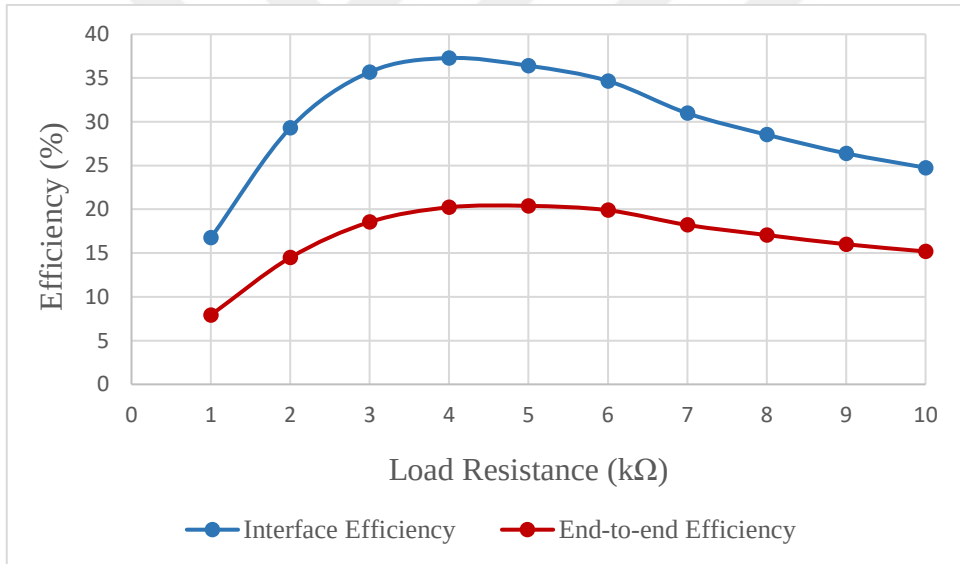


Figure 4.10. DC-DC converter efficiency with load for 500 mV TEG voltage.

4.2.2 Post-Layout Simulation Results

The DC-DC converter layout, together with the MPPT implementation in UMC 180 nm standard CMOS technology, has been presented in Figure 3.19. In this subsection, post-layout simulation results of the converter are going to be presented to compare the results with pre-layout outputs and show the effect of parasitics.

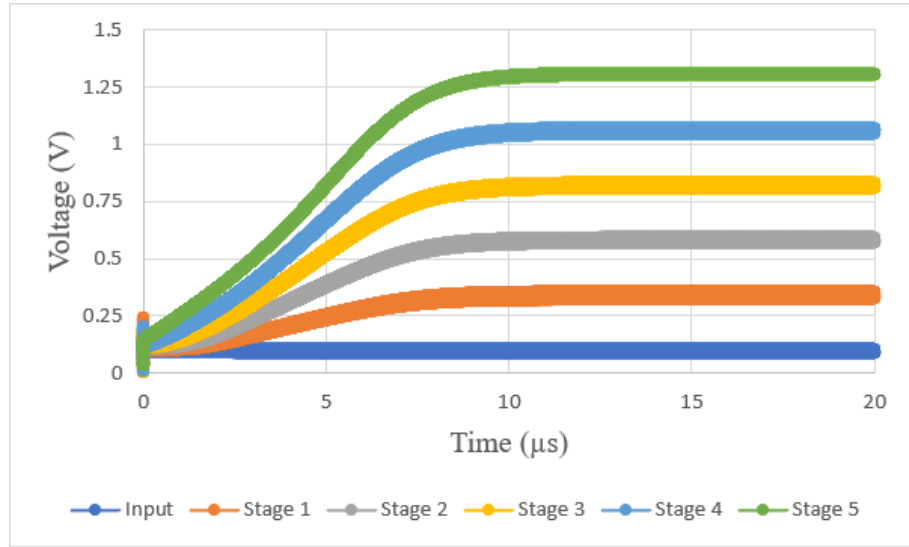


Figure 4.11. DC-DC converter post-layout stage outputs for minimum startup.

Figure 4.11 above depicts the DC-DC converter post-layout simulation results for the minimum startup condition. After the parasitic extraction, the converter starts providing a voltage boost up when the TEG voltage reaches 97.5 mV. The interface circuit input voltage level has been observed as 91.73 mV while the load resistance is 1 MΩ. Even though there is a slight increase in the startup voltage compared to the pre-layout simulations, the converter still could supply 1.3 V output voltage by using the 5-stage charge pump structure.

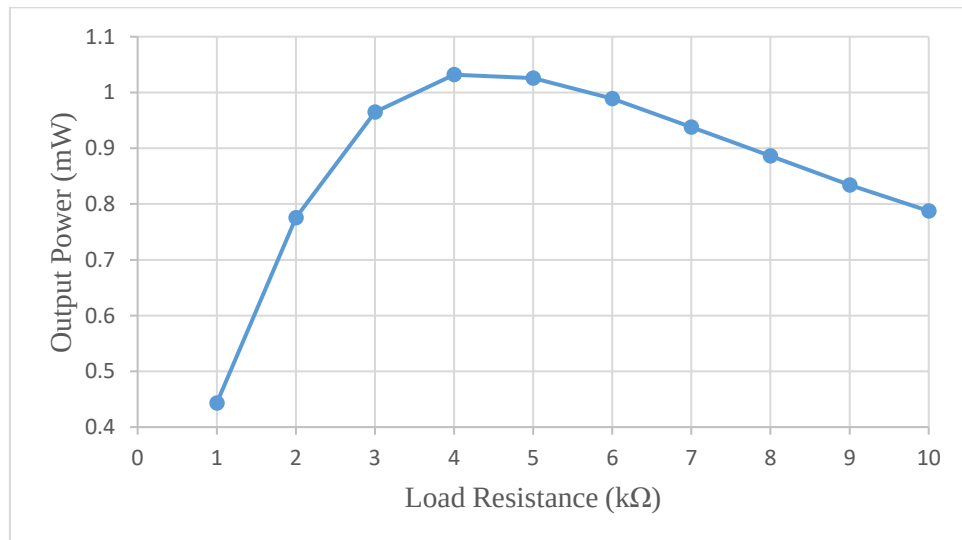


Figure 4.12. DC-DC converter post-layout simulation for 361 mV TEG voltage.

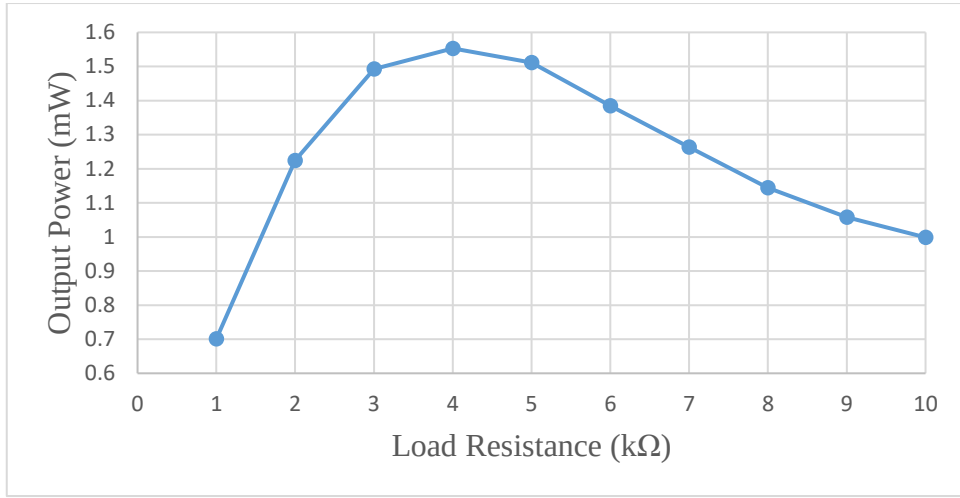


Figure 4.13. DC-DC converter post-layout simulation for 500 mV TEG voltage.

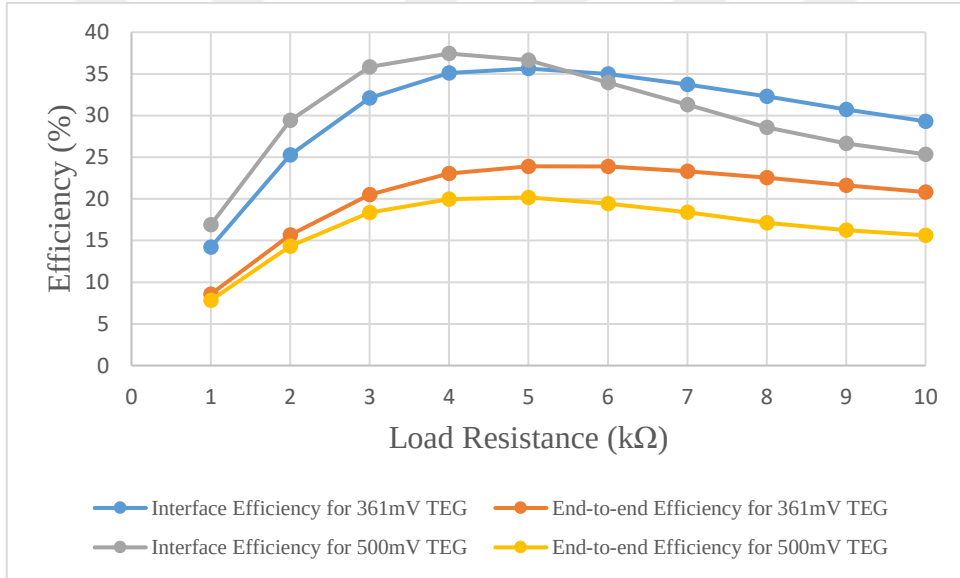


Figure 4.14. DC-DC converter post-layout efficiencies with respect to load.

DC-DC converter post-layout simulation results are presented in Figures 4.12 and Figure 4.13 for 361 mV and 500 mV TEG voltages, respectively. After post-layout simulations, a decrease in clock amplitude and angular frequency have been observed. Although this shows that the loading on the quadrupling LC tank increases, the parasitic capacitances provide better impedance matching at maximum power points, leading to a slight increase in output power. Similarly, the same effect has been observed in the efficiency calculation, as can be seen in Figure 4.14.

To sum up, roughly 1% decrease in clock frequency and 1.7% decrease in clock signal peak-to-peak amplitude have been observed in the post-layout simulations. This is due to the parasitic capacitances. Yet, the parasitic components also contribute to the charge pump capacitance and help the impedance matching. Thus, approximately the same output power has been observed when performing the post-layout simulations by excluding parasitic resistances.

4.3 Fully Autonomous Interface Circuit Simulation Results

The DC-DC converter and the MPPT circuitry creates the fully autonomous interface circuit introduced in this study. The circuit validation of the full system is presented in this section. The system has been simulated for different conditions.

The first two conditions are depicted in Figures 4.15 and 4.16 below. First, the interface circuit has been tested for the TEG voltage of 500 mV. In this circumstance, the input voltage of the interface circuit varies between 0.265 mV and 0.350 mV. The full system achieves as high as 1.24 mW output power with 20% efficiency for the three-stage charge pump configuration when the output is regulated at 1.5 V. An LDO regulator using large PMOS switches have been utilized to regulate the output voltage. When the stage voltage is much larger than the target voltage, a substantial voltage drop occurs on the PMOS switches since the transistor on resistance increases to boost voltage drop. Because of this, a significant current reduction arises. This eventually decreases the output power. Therefore, lower load resistances are used in the simulations compared to the DC-DC converter simulations since lower resistance provides a lower voltage boost and decreases the difference between the stage and target voltage. Moreover, the results can be compared with the METU NCC Energy Harvesting team's previous study, in which the team employs voltage doubling LC tank oscillator [135]. Once the TEG voltage reaches 500 mV, the previous interface circuit achieves 0.469 mW with the two-stage charge pump connected to the output. Therefore, almost 2.65 times higher output power is achieved with the newer version in which the quadrupling LC oscillator is utilized.

The system has been simulated with 450 mV TEG voltage as well. The results show that the maximum output power of 823 μ W with 18% interface efficiency is achieved at 3 k Ω with the three-stage charge pump connected to the output. On the other hand, the results presented in [4], which is again the previous version of this study with a voltage doubling LC tank, achieve approximately 10% efficiency, which corresponds to 125 μ W output power with the same TEG voltage at 10 k Ω load resistance. Hence, the enhancement can be observed one more time.

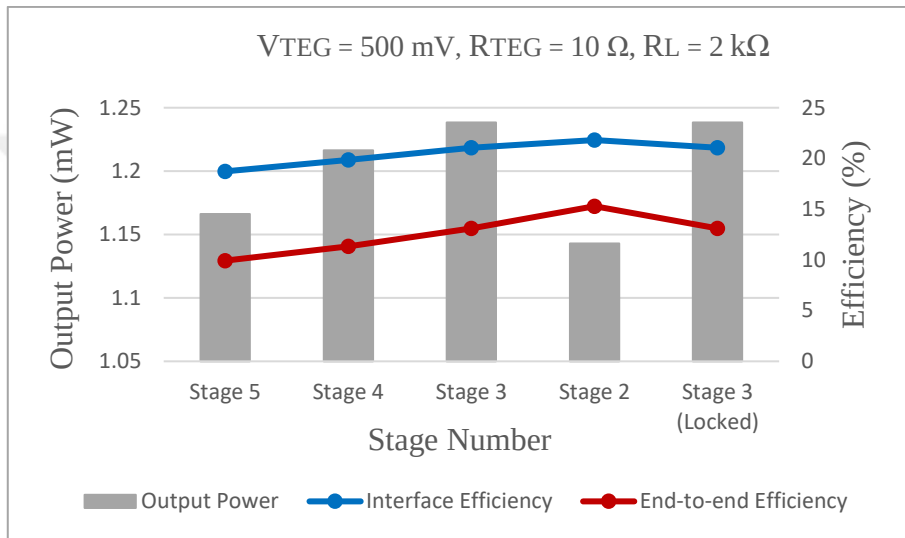


Figure 4.15. Full system simulation result for 500 mV TEG voltage.

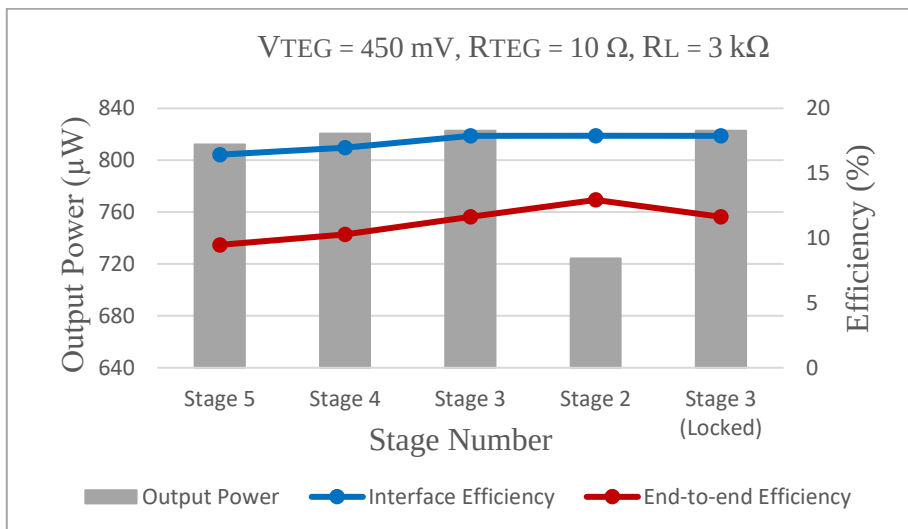


Figure 4.16. Full system simulation result for 450 mV TEG voltage.

Lastly, the full system has been simulated for the minimum startup voltage. It has been observed that the interface circuit starts the voltage boost and achieves more than 1V when the TEG voltage is 96.5 mV, and the load resistance is 1 M Ω . In this condition, the input voltage of the full system varies between 91.3 mV and 92 mV. Thus, the full system can start working with an input voltage less than 100 mV, which can be easily extracted from off-the-shelf TEG devices similar to the one used in this work when they are exposed to low temperature gradients. Comparatively, the results of the previous version of this circuit, which is presented in [135], show that the oscillation starts with 140 mV input voltage, whereas 170 mV input voltage is needed to start voltage boost. Therefore, a significant advancement is observed for the minimum startup condition as well. To conclude, even though further improvements are needed for the MPPT algorithm and circuits, advancements have been observed compared to the previous version of the study, and more than 1 mW output power has been achieved with a fully integrated solution which to the best of our knowledge is the state-of-the-art.



CHAPTER 5

CONCLUSION

In this thesis work, an optimized fully-integrated autonomous milliwatt thermoelectric energy harvesting interface circuit for WBSN applications has been presented. The study is built upon the voltage quadrupling LC tank oscillator and the MPPT architecture, which were previously introduced by the METU NCC Energy Harvesting team and optimized in this work for the five-stage charge pump circuit topology. The optimized circuit is able to achieve a regulated output voltage of 1.5 V, which is the typical output voltage of a single alkaline button cell battery. Furthermore, an output power of 1.24 mW has been obtained, which enables powering up some WBSN systems even without the duty-cycled operation. These results pave the way for batteryless electronics. Furthermore, the DC-DC converter minimum startup voltage is found as 92 mV in the post-layout simulations, which can be easily extracted with a single commercial TEG device. The full system minimum input voltage for the startup is as low as 98 mV, which is still far below our previous studies. The comparison of this study to the state-of-the-art in the literature is presented in Table 5.1.

Table 5.1 Comparison of this work with state-of-the-art in the literature.

Reference	Fully Integrated	MPPT	Regulated V_{out}	Max. P_{out}	Separate Startup	Peak Efficiency	Min. V_{in} for startup	Process
[135]	Yes	Yes	1 V	0.5 mW	No	*30%	170 mV	180 nm
[136]	Yes	Yes	1 V	0.3 mW	Yes	*83%	350 mV	65 nm
[137]	No	Yes	1.8 V	1 mW	Yes	*81%	250 mV	180 nm
[138]	No	No	1-1.8 V	2.1 mW	No	79%	82 mV	180 nm
[139]	Yes	Yes	(No) 1.1 V	4.5 μ W	No	*57%	(NA) 2.8 nW	180 nm
[140]	No	Yes	1 – 1.6 V	0.4 mW	No	60%	190 mV	180 nm
This work	Yes	Yes	1.5 V	1.2 mW	No	22%	98 mV	180 nm

* End-to-end efficiency

5.1 Future Work

The simulation results show that the DC-DC converter efficiency is higher than the full system efficiency. Therefore, further optimization of the MPPT algorithm and circuitry can be investigated. Besides, the full-chip layout with the DC-DC converter and the MPPT circuit is going to be finalized, and it is going to be sent for fabrication. After the fabrication process, the discrepancies between the measurements and simulation results are going to be studied. Furthermore, energy harvesting from hybrid sources is going to be investigated to increase the output power and efficiency further to create a standalone system that can operate even when only one of the ambient energy sources is available. After the power management studies, a real-life WBSN prototype using flexible TEG devices and/or other types of CMOS compatible micro-power generators is going to be created for various body signal measurements.

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