

**DESIGN, IMPLEMENTATION,
MANUFACTURING AND MEASUREMENTS
OF DICKSON CHARGE PUMP CIRCUITS
FOR CAPACITIVE MICROMACHINED
SENSOR BIASING**

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By
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Design, Implementation, Manufacturing and Measurements of Dickson
Charge Pump Circuits for Capacitive Micromachined Sensor Biasing
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January 2019

We certify that we have read this thesis and that in our opinion it is fully adequate,
in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

DESIGN, IMPLEMENTATION, MANUFACTURING AND MEASUREMENTS OF DICKSON CHARGE PUMP CIRCUITS FOR CAPACITIVE MICROMACHINED SENSOR BIASING

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This work presents the design and testing process of Dickson charge pump circuits for micromachined sensor biasing. Necessary blocks of different types of circuits with different functions are examined such as inverters, diode connected MOSFETs, ring oscillators, bond PADs, charge pump stages. Layouts for these circuits are designed and simulated using extracted parameters. The designed circuits are operating using a 5 Volts supply to generate output voltage levels of 12-15 Volts. Finalized layouts are placed on a chip using 0.35 μm process. Designed chip is manufactured and bonded on a test PCB for verification. Measurement results are given and analyzed. Layout and circuit design improvements are proposed and simulated for proof. Steps for future improved designs and precautions are provided. This work enables the way for better functioning charge pump topologies and designs in the future.

Keywords: charge pump, dickson charge pump, CMOS IC design.

ÖZET

KAPASİTİF MİKRO İŞLEMELİ SENSÖR SÜRÜLMESİ İÇİN DICKSON ŞARJ POMPASI DEVRELERİNİN TASARIM, GERÇEKLEME, ÜRETİM VE ÖLÇÜMLERİ

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Bu çalışma kapasitif mikroişlemeli sensörlerin sürülmesi için Dickson şarj pompası devrelerinin tasarım ve test süreçlerini incelemektedir. Birbirinden farklı işlevlere sahip devrelerin alt bileşenleri incelenmiştir, örneğin: invertör devreleri, diyot bağlantılı tranzistörler, halka osilatörler, bağlantı pedleri, şarj pompaları. Bu devrelerin layout tasarımları yapılmış ve parazitik elemanlar hesaplanıp devreler simüle edilmiştir. 5 Volt kaynak gerilimi ile beslenen devreler ile 12-15 Volt çıkış gerilimi elde edilmesi amaçlanmıştır. Sonlandırılan layout tasarımları $0.35\ \mu\text{m}$ 'lik üretim teknolojisine sahip bir çipe yerleştirilmiştir. Tasarlanan çip üretilmiş ve bir test kartına tel bağlaması ile bağlanmıştır. Ölçüm sonuçları sunulmuş ve incelenmiştir. Sonuçlardan yola çıkarak layout ve devre tasarımlarının daha iyi çalışacak versiyonları tasarlanmış ve simüle edilmiştir. Gelecekteki tasarımların daha sağlıklı yapılabilmesi için gereken adımlar sunulmuş ve alınabilecek önlemler önerilmiştir. Bu çalışma gelecekte istenilen şartları fonksiyonel olarak sağlayan ve doğrulanabilecek olan tasarımların yaratılması için bir ön ayak olmuştur.

Anahtar sözcükler: şarj pompası, dickson şarj pompası, CMOS entegre devre tasarımı.

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Chapter 1

Introduction

1.1 Motivation and Background

The majority of electronic devices and circuits have a single connection to a single power source. That power source can be a battery, a line connected power supply or a combination of both. In either case, in most situations, the inner circuitry does not use the given DC supply voltage as is. Many different circuits use different voltage levels optimized for their specific functions. It is not uncommon to encounter that even some individual integrated circuits (ICs) might require different supply voltages for different circuits within them. Therefore the need for converting the supply voltage level to other needed different voltage levels required by the following circuits. This is where power converter circuits and topologies come into the picture.

These bus voltage DC-DC converters can be designed to perform many different tasks depending on the application and system specifications. They can be isolated or non-isolated; regulated or unregulated; step-up converter or step-down converters. There could also be protection features such as over current, undervoltage, overvoltage, inrush current limiting circuitry integrated into the

converter design depending on the system needs. However each integrated feature increases the overall cost, size and complexity of the design. There are many varieties of converter topologies where given a unique application usually a specific topology is more suitable than the others. Choosing the right topology for the application can save the designer money, time and effort.

In applications such as portable electronics, mobile devices, sensory circuits, digital clocked circuits and wireless systems power requirements are typically strict. Many of such systems employ batteries where voltage levels are mostly around 5 Volts or less due to both current battery technology. In such applications higher voltages than the battery voltage might be needed, which would make the use of step-up converters necessary. Step-up converters can be divided into two main categories which are: inductor based converters and inductorless converters. Inductor based converters use an inductor to store and deliver energy to produce higher voltages than the input supply. Such converters can also use transformers to provide isolation where it is needed. Simplest topology of an inductor based non-isolated step-up converter is a boost converter which is seen in Figure 1.1.

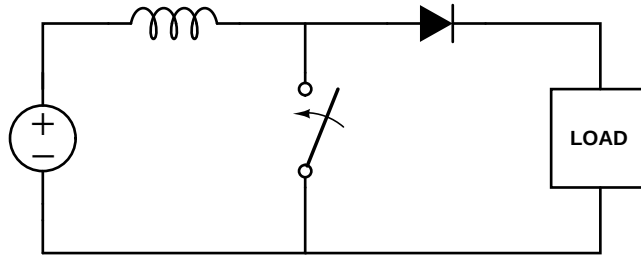


Figure 1.1: Boost Converter Topology

Simple boost converter is useful in applications where a medium to moderately high power is needed by the load. However for light to very light loads, the use of a boost converter becomes more and more disadvantageous due to the size and cost of an inductor which is a bulky component. Very low power step-up converter applications are quite common in most circuit boards such as: high side NMOS switching of half bridge topologies, high side static NMOS gate drive circuits, low power op-amp supply generations, high voltage ADC reference supplies. In such

common and low power applications inductorless step-up converters are found to be cheaper, simpler and easier solutions than inductor based converters.

Inductorless step-up converters also use a switching element to control the power transfer, however instead of using an inductor as a charge storage element, these topologies use capacitors. A commonly used example could be given as a simple bootstrap circuit which is used in NMOS based switching bridge topologies. In such circuits the high side NMOS requires a drive voltage at its gate which is higher than the bus voltage. That higher voltage is generated by the use of a bootstrap circuit where a capacitor and a diode is utilized to generate a floating power supply for the high side drive circuitry which can be seen in Figure 1.2. The circuit charges the bootstrap capacitor to the internal supply voltage through the diode when the low side MOSFET is turned on. When the drive circuitry turns off the low side MOSFET, and starts turning on the high side MOSFET the diode turns off and the capacitor acts as a floating power supply.

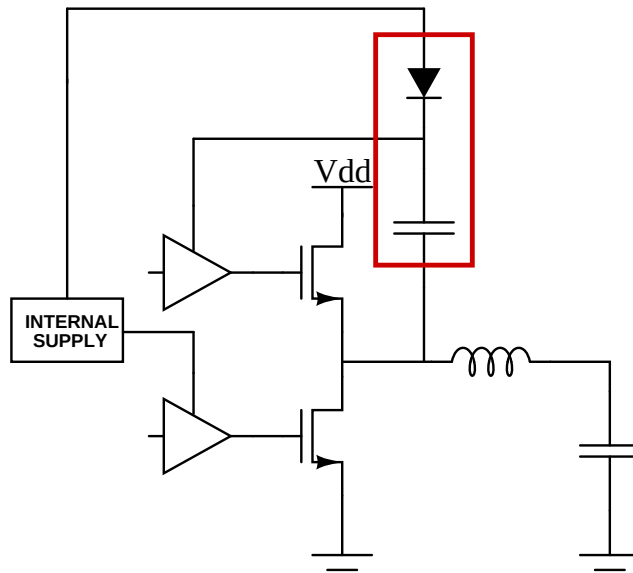


Figure 1.2: Bootstrap Circuit

Bootstrap circuitry exploits the fact that there is a periodically switching node where the boost capacitor can be connected to. However not all circuits have such switching nodes and not all of them are suitable for bootstrapping either.

For example a high side NMOS transistor is commonly used for inrush limiting and input voltage-current protection applications [2, 3]. An example hot swap control circuitry is shown in Figure 1.3. Hot swap control allows designers to protect the system from high inrush currents, short circuits and potential load failures affecting the system power rail. In such applications the MOSFET, in steady state, is either fully on or fully off. To turn the MOSFET fully on, there still is the need for a gate voltage higher than the bus voltage. Since there is not a switching node, bootstrapping cannot be easily implemented. Almost all high side static NMOS transistor control ICs in the market today solves this issue by using a voltage step up topology called: Charge Pumps (CPs) [4, 5, 6].

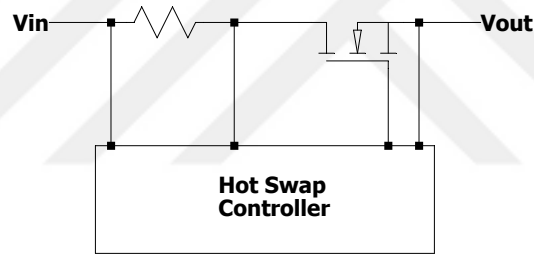


Figure 1.3: High Side Hot Swap Controller

A charge pump is a capacitor based switching converter which converts an input voltage to a different voltage level by pumping charges through capacitors to generate a desired output voltage. Output voltage of a charge pump circuit can be negative, positive, higher or lower than the input voltage. Several commonly used charge pump topologies and their working principles are explained in detail in Chapter 2.

1.2 Research Objectives

In this presented work a charge pump topology was implemented on a silicon chip manufactured with $0.35\mu\text{m}$ CMOS process to function as a bias circuitry for a capacitive load. The charge pump based bias circuits and required timing control circuits are designed. Main objective was to have a step-up circuit which works with 5 Volts supply and boosts it up to 15 Volts, then after some configurable time the converter reduces the output voltage to 12 Volts and keep it at that level indefinitely.

The intended load of the circuit is a capacitive load which, ideally, would have very small amounts of leakage currents. Therefore the designed converter can have a very low output power capability. This allowed us to use smaller pump capacitors and therefore to have a smaller circuit on the silicon die.

CMOS inverter based ring oscillators were used for generating the switching clock signals. Different timing circuitry designs were implemented to provide the time delay after which the converter reduces the output voltage slightly. Timing circuitry was used together with a control circuit which effectively disabled several stages of the charge pump converter.

Overall, the designed circuitry can be used as a proof of concept for our requirements and with several adjustments it can be adapted to different applications requiring simple timing and voltage step-up solutions.

1.3 Thesis Outline

Chapter 2 provides an overview of charge pump topologies, important figures of merits, working principles and a literature summary of those topologies. Chapter 3 gives the design specifications of this work, and explains the circuit blocks in detail. Also post-layout SPICE simulation results, layout drawings of the circuits are shown. Chapter 4 provides experimental results of the manufactured circuits

and compares the results with post-layout SPICE simulations and these results are examined to draw conclusions for improving future designs.



Chapter 2

Overview of Charge Pump Topologies

CPs can easily be built with discrete components without taking up much space on the circuit board due to low power requirements. High voltages can be generated on a board to supply power to different chips and parts of the system. Due to the switching nature of CP converters, in noise sensitive applications a low dropout linear regulator can be used to filter high frequency noise of the CP.

Charge Pumps are not necessarily always built with discrete components. Since parallel plate capacitors are compatible with planar CMOS technology of today, such converters can be integrated directly into silicon chips. Such integrated charge pump circuits can be used for many different applications and purposes inside the IC and on the circuit board as well.

The current trend in miniaturizing CMOS circuits and reducing power consumptions caused a reduction in MOSFET threshold voltages as well as operating supply levels. However many parts of ICs might still need high voltages to operate, such as MEMS devices, EPROM programmers and power switches [7, 8, 9]. Such chips often use integrated charge pump circuits to generate the required higher voltage levels while maintaining the low voltage supply rail. Moreover,

chip integrated CPs also find uses in areas such as energy harvesting circuits, subthreshold voltage reference generation, voltage inverter, fast NMOS based LDOs and system on chip applications [10, 11]. The integration of this multi-functional circuit allows for more compact, more optimized and simpler designs for electrical engineers and IC manufacturers.

Simplest form of voltage amplification circuitry was Greinacher voltage doubler, and it was proposed by Heinrich Greinacher [12]. The circuit was composed of a clamp circuit followed by a peak holder which is shown in Figure 2.1. The operation principle was that an AC input voltage was clamped by a clamp diode which forced the clamp capacitor to charge up to a DC voltage level of peak input voltage. Therefore the clamp node would be the DC offset version of the input voltage with double the peak voltage. The output peak holder circuit simply rectifies this signal to achieve a DC voltage at the output where the DC value was double the input peak voltage.

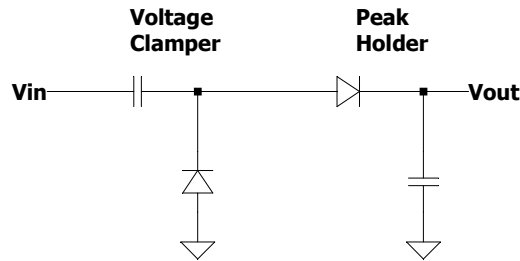


Figure 2.1: Greinacher Voltage Doubler

First commonly used charge pump topology was proposed by Dickson in 1976 [13]. This circuit was presented as an improvement over an older proposed charge pump topology by Cockcroft and Walton [14]. Cockcroft & Walton multiplier was used in 1930s to generate megavolts and kilovolts of voltage levels from lower AC or DC voltages. Such voltage levels were specifically used in particle accelerators and nuclear energy research. The inventors of this topology received the Nobel Prize in physics for their work on nuclear experiments with accelerated particles [15]. The circuit, shown in Figure 2.2, was utilizing capacitors and diodes to gradually pump charges across the ladder to achieve high voltages. It

can actually be seen as a cascaded form of a Greinacher voltage doubler. The top side capacitors C1 and C3 capacitors are working together with D1 and D3 to clamp the AC input signal to the anode voltage of the respective diodes. Anode of D1 is at ground, therefore C1 charges up to a DC voltage to offset the input signal up. Then D2 and C2 acts as a peak holder circuit to charge C2 to double the peak input voltage. This pushes the anode voltage of D3 upwards which in return clamps the cathode voltage to two times the input peak voltage. This consecutive voltage boosting results in significantly higher voltages at the output.

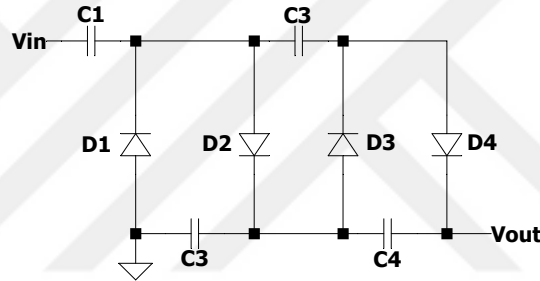


Figure 2.2: Cockcroft & Walton Voltage Converter

Cockcroft & Walton converter allowed each capacitor to charge up to twice the input peak voltage value. This property of the converter allowed designers to use capacitors with lower voltage ratings than the expected output voltage. Reduced stress also made using smaller components possible. However this topology had several shortcomings as well. For this topology to have high conversion ratios, the stray capacitances had to be much smaller than pumping capacitors. Therefore large capacitor values were required which made implementing this topology on a silicon die harder. Moreover, as the number of stages increased the output impedance of this circuit also increased due to serially connected capacitors in the power path. Thus, achieving high output currents became more challenging as more stages were cascaded. To overcome these shortcomings and to have a more reasonable monolithic voltage step up converter, Dickson proposed his topology.

Dickson charge pump is also comprised of capacitors and diodes as it can be seen in Figure 2.3. $\Phi 1$ and $\Phi 2$ are two non-overlapping 180 degrees out of phase

clock signals which usually have amplitudes same as the input voltage amplitude. Main operational difference of Dickson charge pump compared to Cockcroft & Walton converter is that it does not use a time varying input voltage but instead uses clock signals to gradually pump charges across diodes. The operation principle of this topology is explained more in detail in Chapter 3. This topology offered less sensitivity to stray capacitances, lower output impedances and higher output currents thus making the use of smaller capacitors possible. This allowed designers to successfully implement this topology on integrated circuits. Dickson charge pump's main challenge is that as the number of stages increase to have a larger output voltage, the capacitor voltage stresses also increase. The last capacitor of the cascaded topology has to endure the full range of output voltages. Moreover due to this voltage increase at each cascaded node, if the diodes are implemented by using diode connected NMOS transistors, due to the body effect the loss of each stage increases. An improved version of Dickson's topology was proposed as the bootstrapped Dickson charge pump.

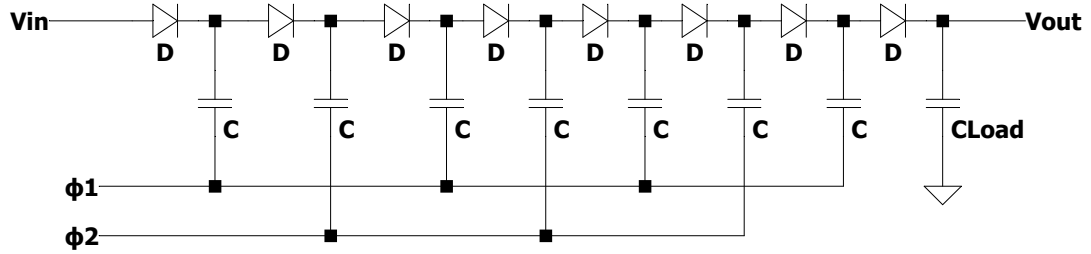


Figure 2.3: Dickson Charge Pump

The body effect induced threshold voltage shift problem of classical Dickson charge pumps were solved by the introduction of bootstrapped Dickson charge pumps [16, 17]. In this topology a bootstrap MOSFET drive circuitry is built around each stage to use the MOSFETs in their triode region. The bootstrap circuit is shown in Figure 2.4. During the time interval where a transfer switch is OFF, the bootstrap circuitry charges a capacitor to supply voltage. When the clock phase changes, the bootstrap circuitry connects this charged bootstrap capacitance across the transfer switch's gate and drain terminals as shown in Figure 2.5. This in return reduces the threshold voltage drop across the transfer switch

and therefore increases efficiency. Due to the increased efficiency, for a given required voltage gain, less number of stages can be used compared to the Dickson Charge Pump. However a tradeoff has to be made and taken into account since the bootstrapped topology comes with increased complexity, increased number of clock signals and extra circuitry. This topology is especially useful for applications where the input voltage supply is low and therefore diode forward voltage losses start to dominate.

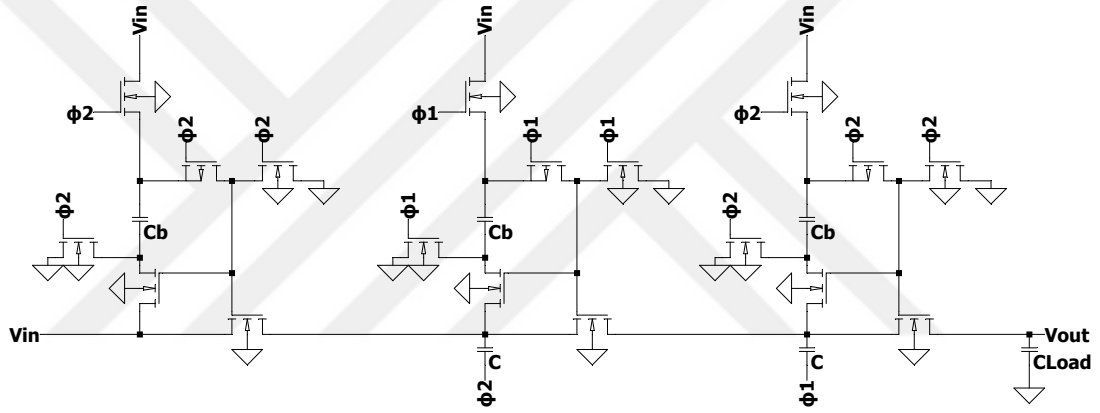


Figure 2.4: Bootstrapped Dickson Charge Pump

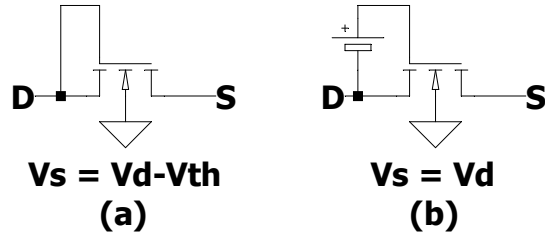


Figure 2.5: Transfer switch in ON state.

a) Dickson Charge Pump, b) Bootstrapped Dickson Charge Pump

Another variant of bootstrapped Dickson Charge Pump is shown in Figure 2.6. This topology uses boost transistors and additional clock control signals to use the transfer switches in their triode regions [18]. During a charge transfer interval from stage node N to stage N+1, the pump clock signal connected to node N becomes high which turns ON the boost transistor of stage N, TBN. Turned

on boost transistor shorts the gate and source of the transfer switch T_N , at the same time charges the boost capacitor C_{BN} to the node voltage. Then boost control signal connected to $C_{BN}+1$ becomes high, boosting the gate voltage of T_{N+1} through previously charged $C_{BN}+1$. This turns the T_{N+1} fully ON and reduces transfer losses. Although different bootstrap topologies exist, the aim remains the same which is solving the threshold voltage loss of Dickson Charge Pump.

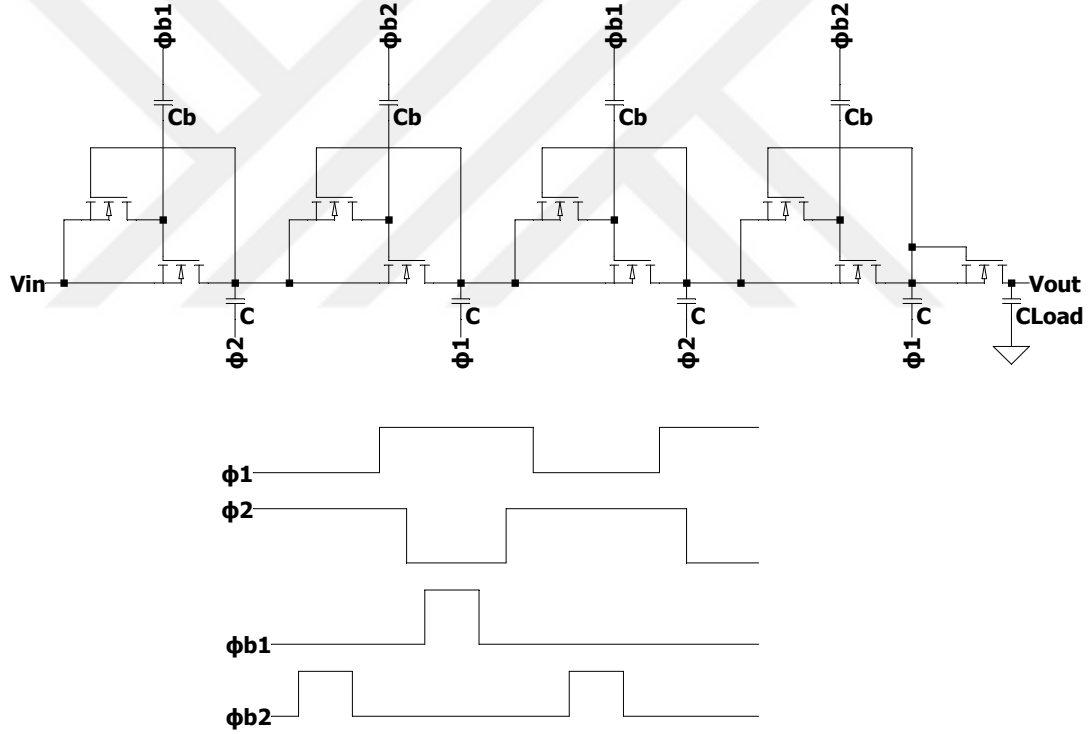


Figure 2.6: Boosted Charge Pump

Another improved topology derived from regular charge pumps was the double charge pump topology [19]. This topology uses two parallel connected regular charge pump circuits as seen in Figure 2.7. The pump capacitances are reduced in half to keep the total pump capacitance the same. Again two out of phase clocks are used to drive the pump capacitors, however the difference is that the at each half cycle of a clock, only one of the two parallel charge pump circuits charge the output. This in return reduces the ripple in half by effectively doubling the

output ripple frequency seen by the output capacitor. Output voltage and gain per stage are not affected by the use of this topology.

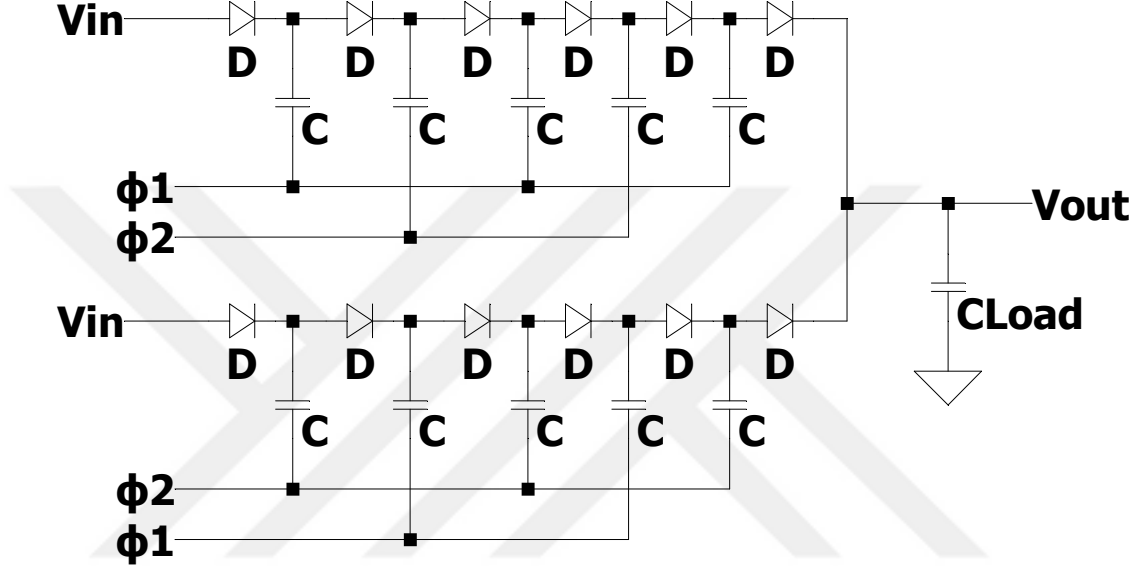


Figure 2.7: Double Charge Pump Topology

Another variety of charge pump topologies can be named as series-parallel charge pumps. This topology, as the name implies, connects charge pump capacitors in parallel and in series periodically as it can be seen in Figure 2.8 [20, 21]. At the first half of the period the pump capacitors are charged to the input voltage, then all the pump capacitors are connected in series by switches. Thus a voltage gain of N is achieved, where N is the number of pump capacitors. This topology has the disadvantage of having large inrush currents due to simultaneous charging of pump capacitors in parallel. This can induce unwanted stresses in the circuit and to the supply. To overcome this problem a circuit was proposed by Hara et al [22]. The proposed circuit utilized a network of switches and diodes to achieve a timing in which individual pump capacitors are charged one by one. This would reduce the input inrush current greatly by reducing the capacitive loading.

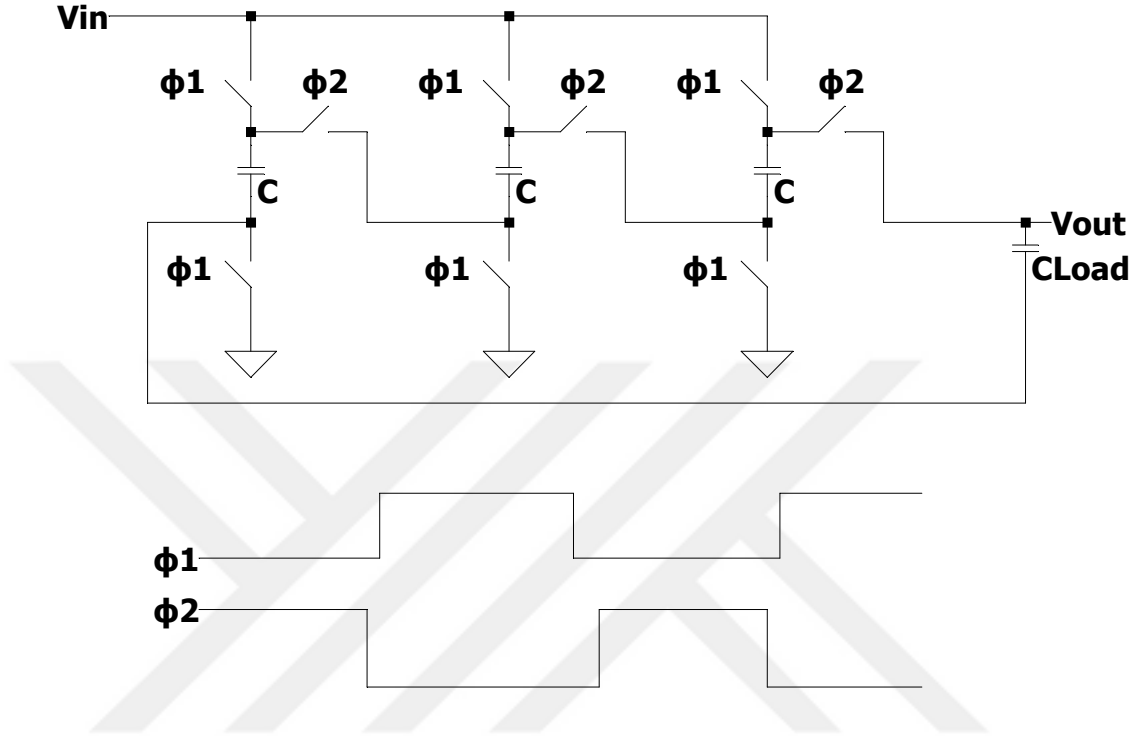


Figure 2.8: Series-Parallel Charge Pump Topology

In some applications several different output voltages might be needed in different time intervals. Such ICs might benefit from using an adaptive charge pump topology where the effective number of stages of the charge pump can be changed during the circuit operation by controlling its driving clock signals and phases of those clocks in relative to one another [23, 1]. Adaptive control provides flexibility to the designer and allows the circuit to operate at an optimum operation point for a given load and desired output voltage. An example circuit of an adaptive charge pump which can act as a pump with 1, 2 or 3 stages is shown in Figure 2.9. The circuit always uses the same total capacitance to pump charges, therefore it uses silicon area efficiently.

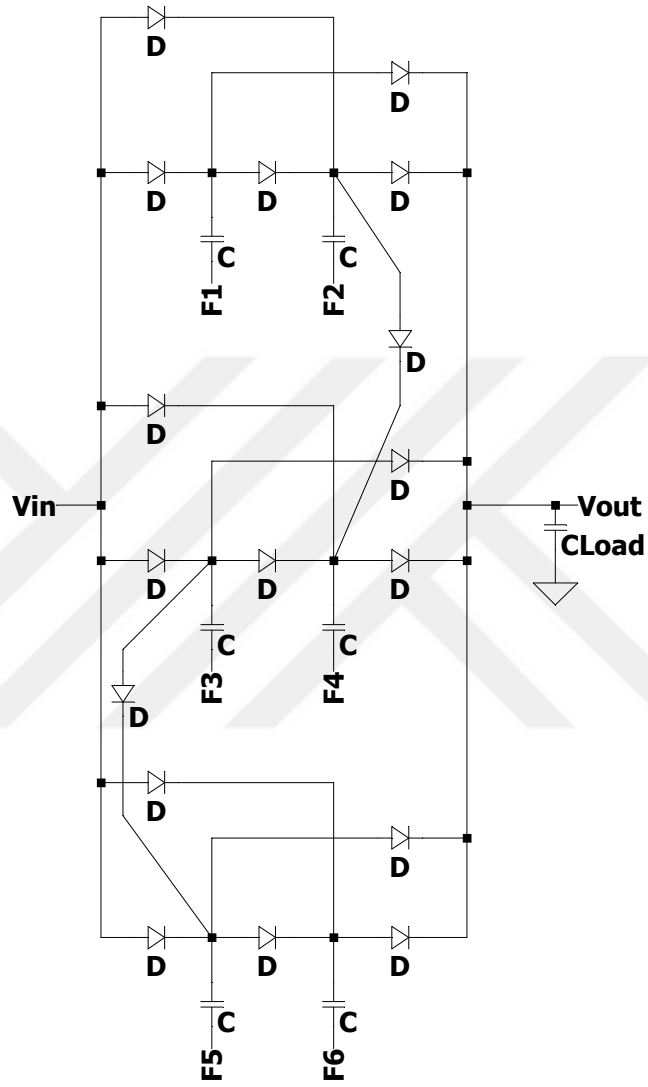


Figure 2.9: Adaptive Charge Pump Topology [1]

Chapter 3

Design and Simulation

In this chapter the design requirements are laid out and the Dickson Charge Pump topology is explained in detail. Then sub-circuit blocks used in the design are shown. Their working principles are explained and schematics are given. Designed layout figures are provided as well as post-layout simulations which verify the expected operation of the circuits.

These sub-circuit blocks are used together in a way to create several main circuit blocks. Those main blocks are also explained, their schematics, layouts and post-layout simulations are provided. All the simulations are done with Spectre.

3.1 Design Specifications

The bias signal needed by the expected load is basically a DC voltage which is generated by the 5 Volts supply rail. 15 Volts bias has to be achieved and kept constant for some undetermined amount of time, after which the bias voltage should reduce to 12 Volts. The desired output voltage waveform is shown in Figure 3.1.

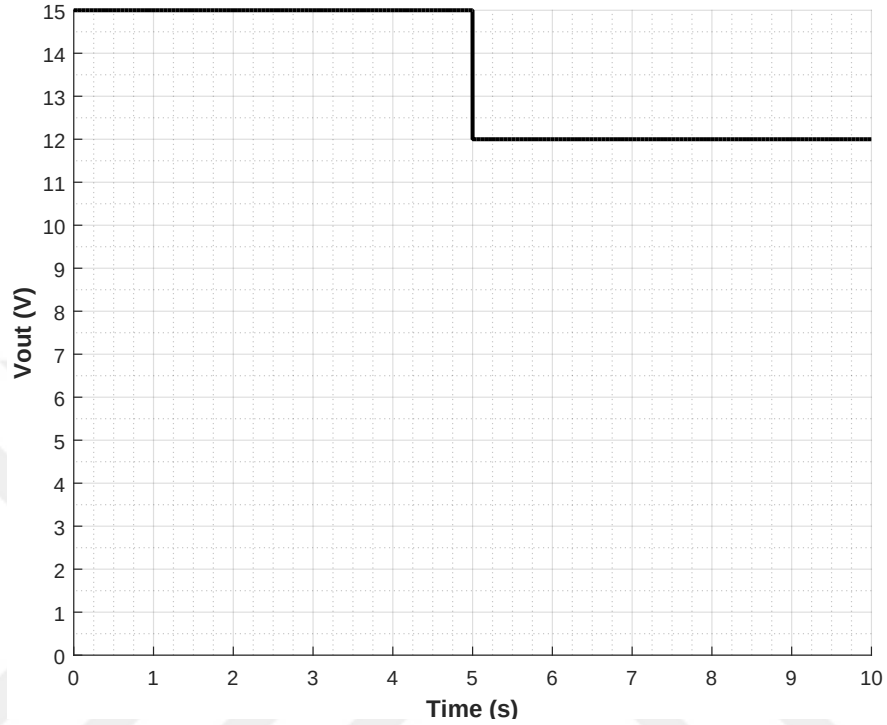


Figure 3.1: Desired Output Voltage Waveform

Moreover, it was required that the circuitry should not need any external control or trigger signals to operate. Therefore any necessary control signals, clocks and triggers should be generated internally.

The expected load of this circuit is of capacitive nature, thus DC current loading is expected to be minimal.

These requirements were satisfied in this thesis by using PMOS based Dickson Charge Pumps. Clock signals were generated internally with ring oscillators. Delay timing required for the output voltage reduction was achieved with three different approaches: External capacitor programmed delay, Surface leakage current based delay, OFF PMOS current based delay. Following sections explain these circuits in detail.

3.2 Detailed Analysis of Dickson Charge Pump

In this thesis, charge pump circuits were derived from the classical Dickson Charge Pump topology [13]. Therefore prior to going into detail of the designed blocks, it is needed to understand the operation principles behind Dickson's topology. The circuit including stray capacitors C_s and pump capacitors C is given in Figure 3.2. Charge transfer devices are shown as diodes.

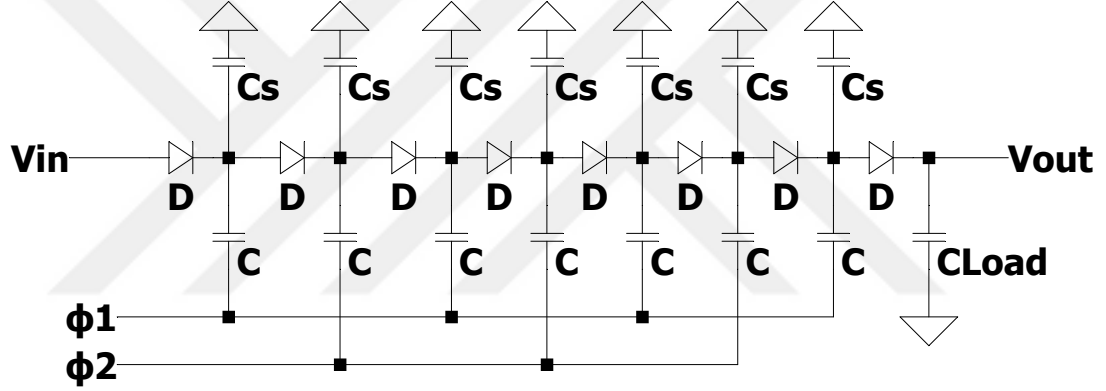


Figure 3.2: Dickson Charge Pump with Stray Capacitances

In the given circuit, Φ_1 and Φ_2 are two out of phase clock signals with amplitude equal to the supply voltage as shown in Figure 3.3. V_{in} is the input voltage which is usually tied directly to the available voltage supply.

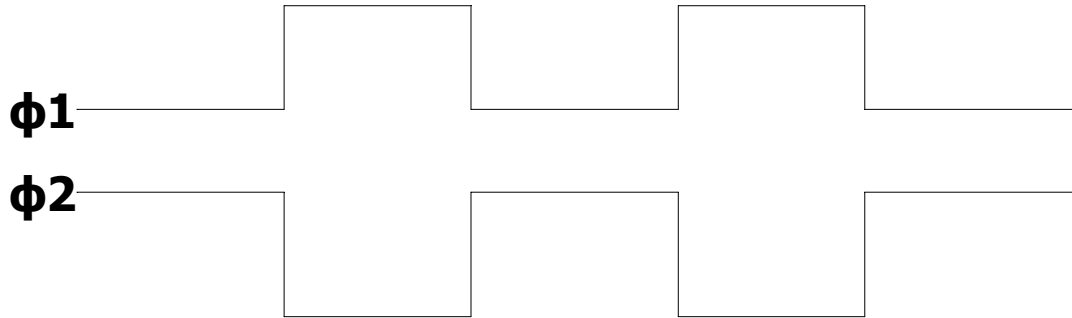


Figure 3.3: Dickson Charge Pump Clock Signals

In order to derive the output voltage, the voltage difference between two cascaded stages $V_N - V_{N-1}$ should be calculated where N corresponds to stage number. Nodes between stages are numbered as it is shown in Figure 3.4.

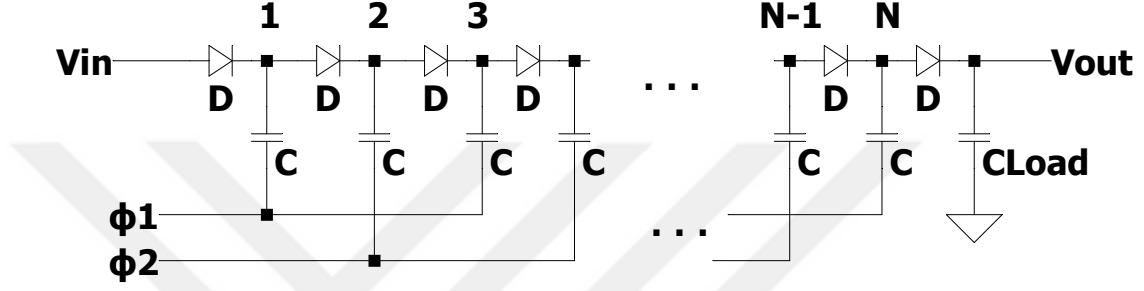


Figure 3.4: Dickson Charge Pump Node Numbering

First, an expression of voltage gain per stage is derived under the assumption of steady state operation and zero output current. In steady state, no load condition diodes no longer transfer charges across stages since there is no load and all the capacitors are assumed to be fully charged. Voltage difference between two consecutive stages can be calculated using the Equation 3.1 where V'_ϕ is the voltage variation due to the clock signal driving Nth node and V_D is the forward diode voltage.

$$V_N - V_{N-1} = V'_\phi - V_D \quad (3.1)$$

Due to steady state analysis, V'_ϕ can easily be calculated by ignoring the charge transfer diode. Thus, during the pumping phase the Nth stage becomes the equivalent circuit shown in Figure 3.5.

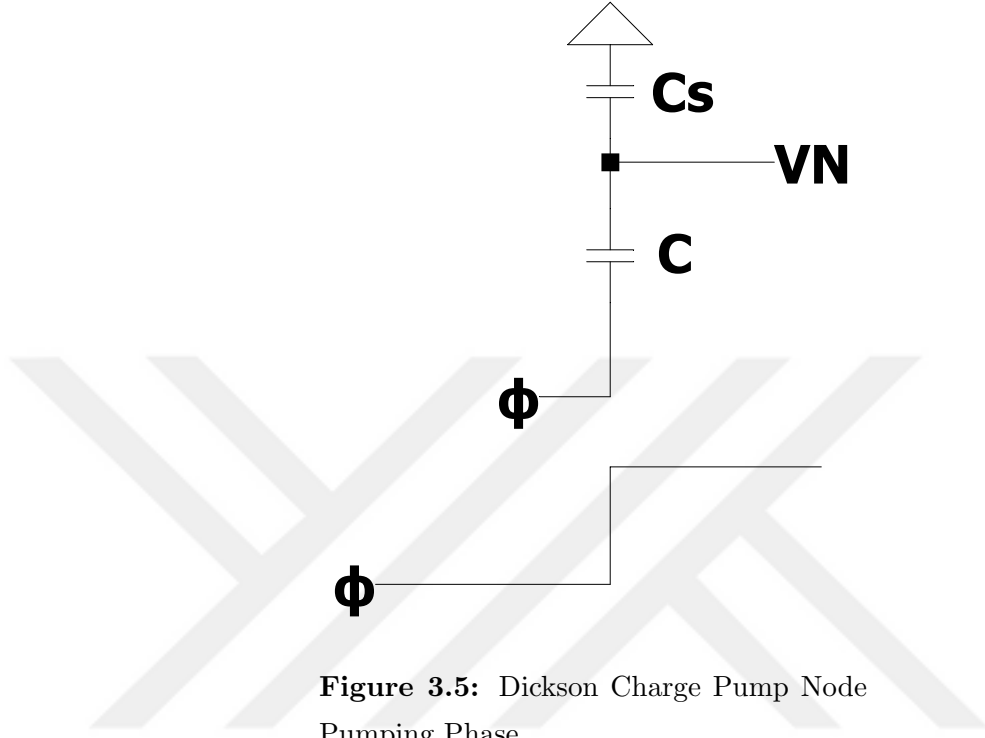


Figure 3.5: Dickson Charge Pump Node
Pumping Phase

During the pumping phase, the pumped charge ΔQ is stored equally in both capacitors. Assuming the clock amplitude is V_Φ then the overall voltage change across two capacitors is V_Φ . This change is equal to the individual voltage changes across both capacitors ΔV_C and ΔV_{CS} which are the voltage changes across pump capacitor and stray capacitor respectively. Naming the voltage increase at the node due to the pumping clock as V'_Φ , the following equations are derived.

$$\Delta V_C = \frac{\Delta Q}{C}, \quad (3.2)$$

$$\Delta V_{CS} = \frac{\Delta Q}{CS}, \quad (3.3)$$

$$V_\Phi = \Delta V_C + \Delta V_{CS} = \frac{\Delta Q}{C} + \frac{\Delta Q}{CS}, \quad (3.4)$$

$$\Delta Q = V_\Phi \times \left(\frac{1}{C} + \frac{1}{CS} \right), \quad (3.5)$$

$$V'_\Phi = \Delta V_{CS} = \frac{\Delta Q}{CS}, \quad (3.6)$$

$$V'_\Phi = V_\Phi \times \left(\frac{C}{C + CS} \right). \quad (3.7)$$

The resulting Equation 3.7 implies two things. First, as the stray capacitance increases, the voltage seen at the pumping node due to the pumping clock decreases. Second, in an ideal circuit where there is no or negligible stray capacitance; the node voltage would see a voltage swing equal to the clock amplitude. Using Equation 3.7 and 3.1, the Equation 3.8 is derived for one stage gain of a zero output current Dickson charge pump.

$$V_N - V_{N-1} = V_\Phi \times \left(\frac{C}{C + CS} \right) - V_D \quad (3.8)$$

The results so far were under the zero output current assumption, however a charge pump exists so that it can provide some current to a designated load. Therefore the analysis has to be extended for a loaded case where the load current is I_O . Steady state assumption still holds and does not change the final DC results. Let the clock frequency be f_Φ and the clock period be T_Φ . Once every period some charge will be pumped from each stage to the output. When there is no load current, this charge becomes zero at steady state. However when there is load current, in order to keep the output voltage level constant, the output capacitor has to be supplied the charge equivalent of the load's charge consumption. During a switching period, the charge consumed by the load can be calculated using Equation 3.9.

$$Q_{\text{Out}} = I_O \times T_\Phi = \frac{I_O}{f_\Phi} \quad (3.9)$$

This constant charge has to come from each charge pump stage since they are serially connected. Thus an output current will load every stage equally. The node voltage reduction can be calculated using the following equations where ΔQ_S is the charge coming from stray capacitance, ΔQ_C is the charge coming from pump capacitance and ΔV_L is the node voltage reduction due to output current.

$$\Delta Q_S = CS \times \Delta V_L, \quad (3.10)$$

$$\Delta Q_C = C \times \Delta V_L, \quad (3.11)$$

$$\Delta Q_S + \Delta Q_C = Q_{\text{Out}} = (C + CS) \times \Delta V_L. \quad (3.12)$$

$$\Delta V_L = \frac{I_O}{f_\Phi \times (C + CS)}. \quad (3.13)$$

Combining the previous results using Equations 3.8 and 3.13 the Equation 3.14 is derived.

$$V_N - V_{N-1} = V_\Phi \times \left(\frac{C}{C + CS} \right) - V_D - \frac{I_O}{f_\Phi \times (C + CS)} \quad (3.14)$$

The result in Equation 3.14 is given for a gain of one stage. To derive the total output voltage, this result has to be generalized to an N stage Dickson Charge Pump with V_{in} input voltage. The voltage gain of N cascaded stages $\Delta V_{N\text{stage}}$ would be equal to:

$$\Delta V_{N\text{stage}} = N \times \left[V_\Phi \times \left(\frac{C}{C + CS} \right) - V_D - \frac{I_O}{f_\Phi \times (C + CS)} \right] - V_D$$

The additional V_D loss comes from the output diode. This expression gives the voltage gain from input to output, thus the output voltage V_{out} can be calculated using the input voltage and derived equations as follows:

$$V_{\text{out}} = V_{in} + N \times \left[V_\Phi \times \left(\frac{C}{C + CS} \right) - V_D - \frac{I_O}{f_\Phi \times (C + CS)} \right] - V_D \quad (3.15)$$

The derived equation assumes a constant output voltage, however under loading, the output voltage will deviate around its DC average value. This output ripple is due to the fact that during half of the switching period, the output capacitor is disconnected from the charge pump circuit and is supplying the load current all by itself. This causes a voltage drop at the output which is named output ripple voltage; V_{ripple} and it can be calculated using Equation 3.17 which

is derived as follows where Q_{ripple} is the charge supplied by the output capacitor C_O during the half cycle of the switching period T_ϕ :

$$Q_{\text{ripple}} = I_O \times \left(\frac{T_\phi}{2}\right), \quad (3.16)$$

$$V_{\text{ripple}} = Q_{\text{ripple}} \times \frac{1}{C_O} = I_O \times \left(\frac{T_\phi}{2}\right) \times \frac{1}{C_O}. \quad (3.17)$$

Thus, Dickson Charge Pump topology's voltage gain and output ripple properties are analyzed and several important conclusions can be made. Using Equation 3.14 it can be concluded that the voltage amplification prevails as long as the condition given in Equation 3.18 is satisfied. This equation summarizes the fact that to have a higher current capacity, the circuit has to have larger pump capacitors in order to maintain its gain. Moreover, smaller stray capacitances correspond to larger gain. Also the switching frequency appears to be an important parameter which can be increased to reduce the pump capacitor sized without changing the output voltage. This result appears to be similar to what it widely known from power electronics where the passive filter and magnetic component sizes tend to become smaller as the switching frequency increases. Furthermore, higher switching frequency also results in lower output voltage ripple as seen in Equation 3.17.

$$V_\Phi \times \left(\frac{C}{C + CS}\right) - V_D - \frac{I_O}{f_\Phi \times (C + CS)} > 0 \quad (3.18)$$

Up to this point the transfer switch element of the Dickson Charge Pump was assumed to be a normal diode. However usually this diode is created with a diode connected NMOS transistor as shown in Figure 3.6. Gate and Drain terminals of the NMOS device are connected together forcing the device to work under saturation. When a voltage is applied to the Drain terminal, the transistor turns ON after the difference between its gate and source terminals exceed its threshold voltage V_{TH} . Thus, by operating in saturation region, the transistor clamps its gate to source voltage V_{GS} to V_{TH} . Since the gate and drain terminals are shorted, in overall this configuration clamps drain to source voltage V_{DS} to V_{TH} , thus satisfying the Equation 3.19.

$$V_S = V_D - V_{TH} \quad (3.19)$$

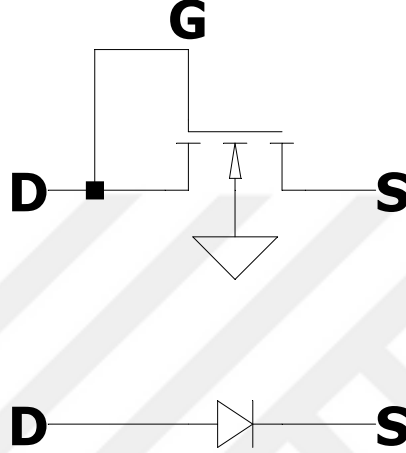


Figure 3.6: Diode Connected NMOS Transistor

Clearly the Equation 3.19 can be modeled as a diode with forward voltage drop of V_{TH} . Therefore it is necessary to examine the threshold voltage of an NMOS enhancement transistor which is given in Equation 3.20 [24].

$$V_{TH} = V_{T0} + \frac{\sqrt{2q\epsilon_{Si}N_A}}{C_{OX}}(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}) \quad (3.20)$$

Where;

V_{SB} : Source to body voltage,

V_{T0} : Threshold voltage when V_{SB} is zero,

Φ_F : Fermi potential,

ϵ_{Si} : Permittivity of Silicon,

N_A : Acceptor doping density,

q : Charge of an electron,

C_{OX} : Gate oxide capacitance per unit area.

According to Equation 3.20 the threshold voltage shows dependence on V_{SB} which is known as the body effect. In Dickson Charge Pump, as previously

explained, the source voltage increases in each stage by the amount given in Equation 3.14. Therefore when NMOS devices are used as transfer elements, as the stage number increases, the V_{SB} also increases. This in return increases the threshold voltage of the transistor thus increasing the loss component given as V_D in Equation 3.14. For these reasons when using diode connected NMOS devices, the body effect and the threshold voltage increase has to be taken into account and in fact after enough number of stages, the voltage gain per stage might become negative due to large threshold voltages.

To conclude, Dickson Charge Pump topology's main operating principles are explained and several expressions were derived for voltage gain, voltage ripple, threshold voltage shift due to body effect. This thesis's work is different than the general Dickson topology in which PMOS diode elements were used to negate the body effect threshold voltage shift of NMOS devices. Moreover grounded input voltages was used in charge pump circuits to enable integration of several timing control and trigger circuits. Following section explains the designed sub-circuit blocks and continues with final main circuits.

3.3 Sub-Circuit Blocks

In this section sub-circuit blocks are described in detail and their layouts are shown. Furthermore, post-layout SPICE simulations are given. The design used in this work uses the 350 nm AMS process with four metal and two polysilicon layers.

3.3.1 CMOS Inverter for Ring Oscillator

As it was explained in Section 3.2, a Dickson Charge Pump uses two out of phase clock signals to drive pumping capacitors. In this work a ring oscillator was used to generate these clock signals. A ring oscillator is basically an odd number CMOS inverters with certain delays, connected in a cascaded manner

which results in an astable operation where the output oscillates.

The basic block of the oscillator is a CMOS inverter with a capacitive load at the output as shown in Figure 3.7. 500nm, 5 Volts compatible transistors are used and widths are chosen as $1.0\mu\text{m}$ for top PMOS and $0.8\mu\text{m}$ for bottom NMOS transistor.

Capacitive load of 100fF is connected at the output of the inverter to increase the delay time from input to output. This increase of the delay translates into a reduction in the clock frequency of the ring oscillator as it is explained in Subsection 3.4.1.

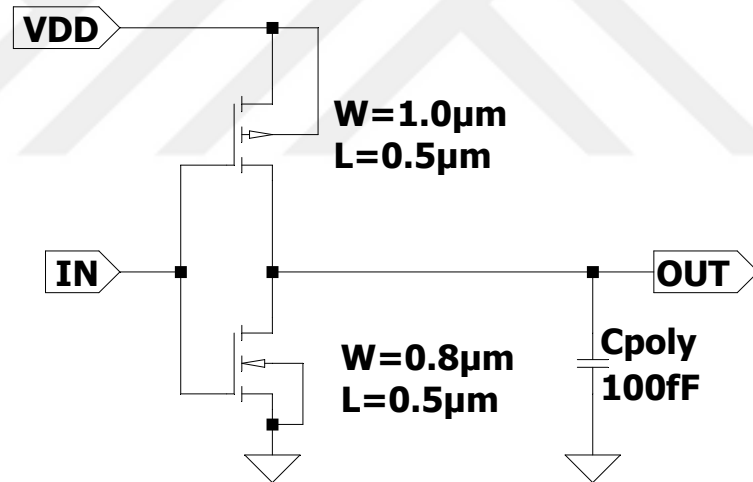


Figure 3.7: 1-Stage Inverter with Capacitive Load Circuit

The layout of the circuit is shown in Figure 3.8. The 100fF output delay capacitor is realized by using parallel plate polysilicon capacitor. The layout dimensions are $17.45\mu\text{m} \times 16\mu\text{m}$.

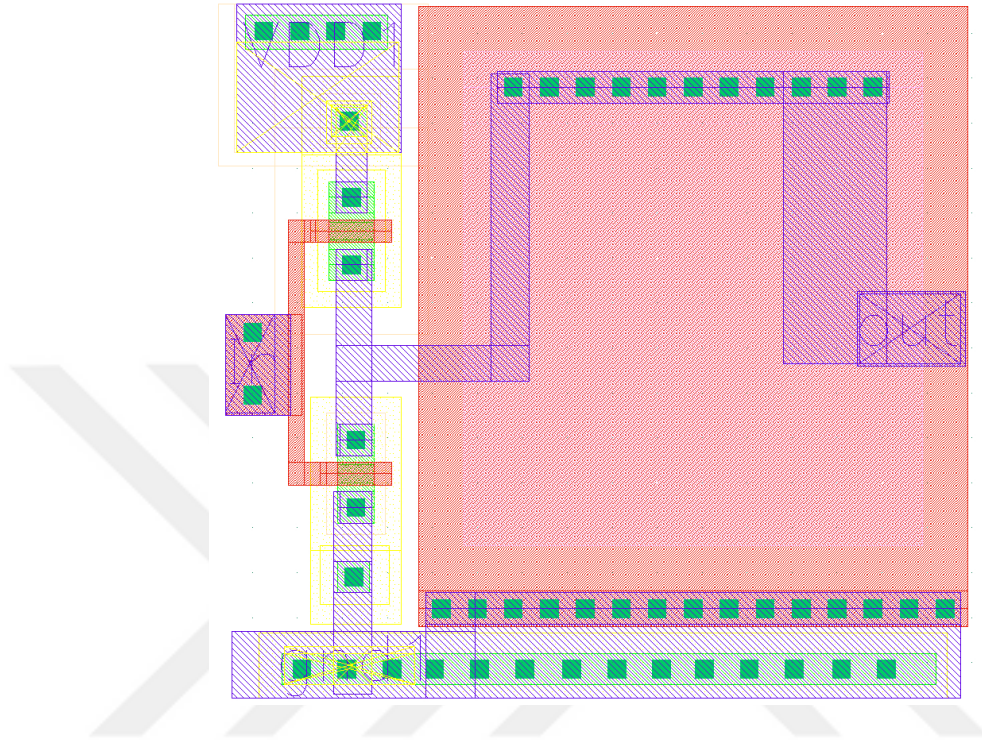


Figure 3.8: 1-Stage Inverter Layout

Post-layout parameters were extracted and the circuit was simulated using Spectre. Transfer characteristics of this inverter circuit is shown in Figure 3.9.

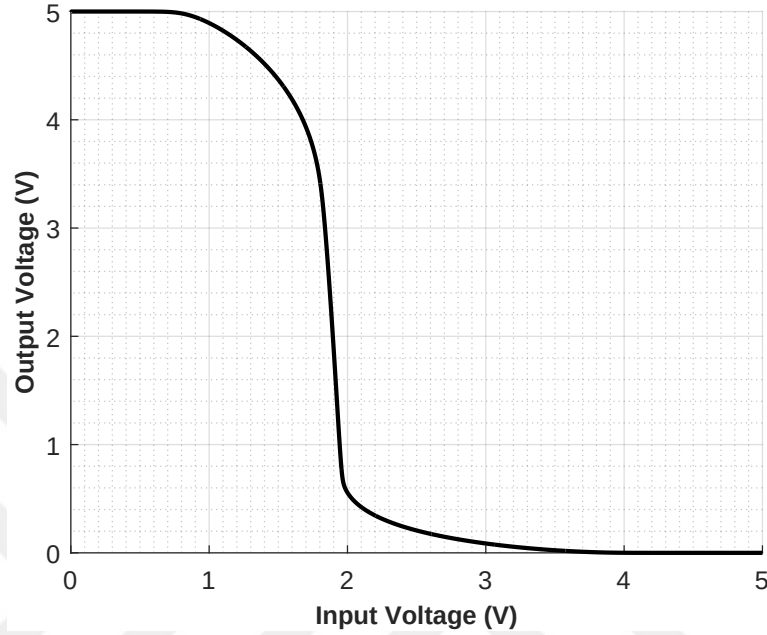


Figure 3.9: 1-Stage Inverter with Capacitive Load Transfer Characteristics Post-Layout Simulation

3.3.2 1-Stage Charge Pump Block

Transfer switches of the designed circuit are based on the body diodes of PMOS transistors. PMOS devices are selected so that all the devices have separate body connections with possibly different voltage levels. This allowed us to alleviate the body bias threshold voltage shift problem linked to NMOS devices.

Available capacitor types of the manufacturer's CMOS process are examined. It is understood that in order to achieve a high pumping capacitance a high capacitance per unit area is needed. There were three seemingly appropriate options which are gate capacitances of 3.3V and 5V MOSFETs as well as Poly1-Poly2 capacitance. Another constraint when selecting the right capacitor is the breakdown voltage characteristic of the capacitor. In the Dickson charge pump topology, the capacitors will be facing higher and higher voltage stresses as the stage numbers increase. The pump capacitor of the last stage will undergo a stress voltage equal to the value of the expected output. The breakdown voltages

of 3.3V and 5V MOSFET gate oxides are given as 8 and 15 Volts respectively whereas the breakdown voltage of Poly1-Poly2 capacitor is given as 30 Volts. Therefore Poly1-Poly2 capacitor is chosen.

300fF polysilicon capacitors are used as charge pump capacitors. Maximum voltage stress expected by the pump capacitors is simply the maximum output voltage value. In the used CMOS process the breakdown voltage of pump capacitors was 30 Volts, therefore the expected maximum output voltage value of 15 Volts does not exceed the tolerance levels of these capacitors. Since the expected load of the circuit is of capacitive nature, the transfer devices will not endure high DC currents. If an application was to require higher DC output currents then wider transfer devices has to be used.

Body, source and gate connections of PMOS transistor devices were shorted, leaving the body diode available for conduction whenever the drain voltage becomes higher than the source voltage. Maximum reverse voltage stress seen by the devices are 5 Volts, which is the ideal maximum pump voltage increase from one stage to the next. As the number of stages increase, the body voltage of PMOS devices also increase. This causes a Body to Substrate reverse voltage stress and its maximum value is equal to the expected maximum output voltage value of 15 Volts. This does not exceed the 32 Volts N-well to substrate threshold limit specified by the manufacturer.

The primary building block of the charge pumps is shown in Figure 3.10. Three terminals of the block are identified as CLK, Vhigh and Vlow. CLK is the charge pumping clock signal which is the output of a ring oscillator. Vlow is the low voltage side of the device, anode of the body diode. Vhigh is the high voltage side of the device, cathode of the body diode. The charge pump cell transfers charges from Vlow side to the Vhigh side whenever the CLK signal is low and there is a higher voltage at the Vlow side.

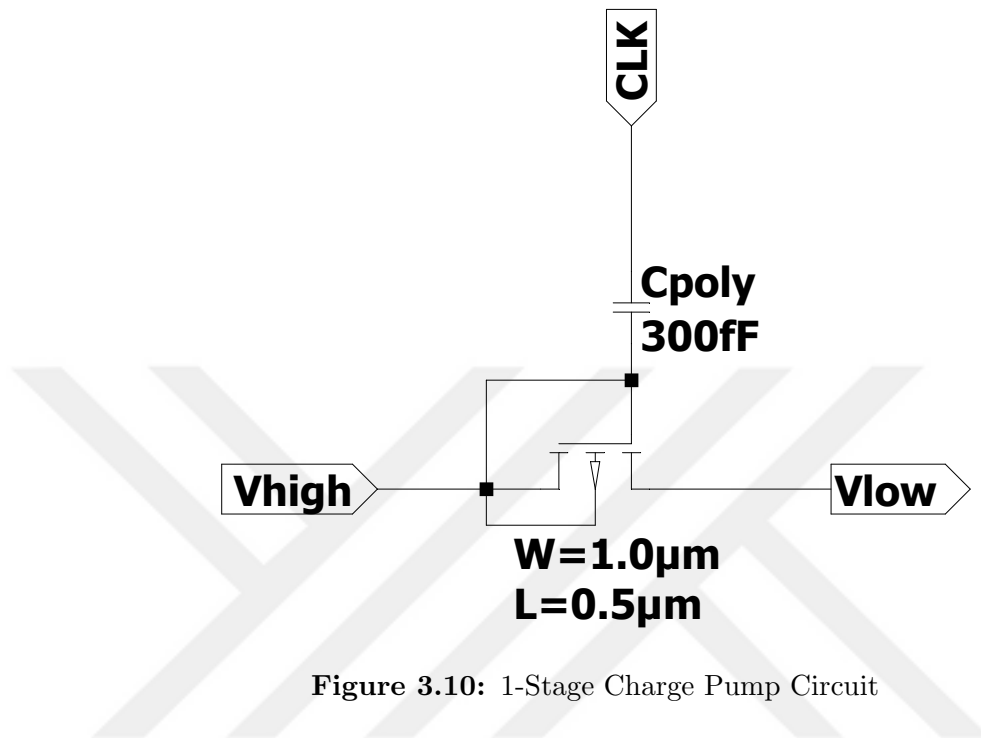


Figure 3.10: 1-Stage Charge Pump Circuit

The layout of 1-stage pump is given in Figure 3.11. The layout dimensions are 24 μ m x 22.5 μ m.

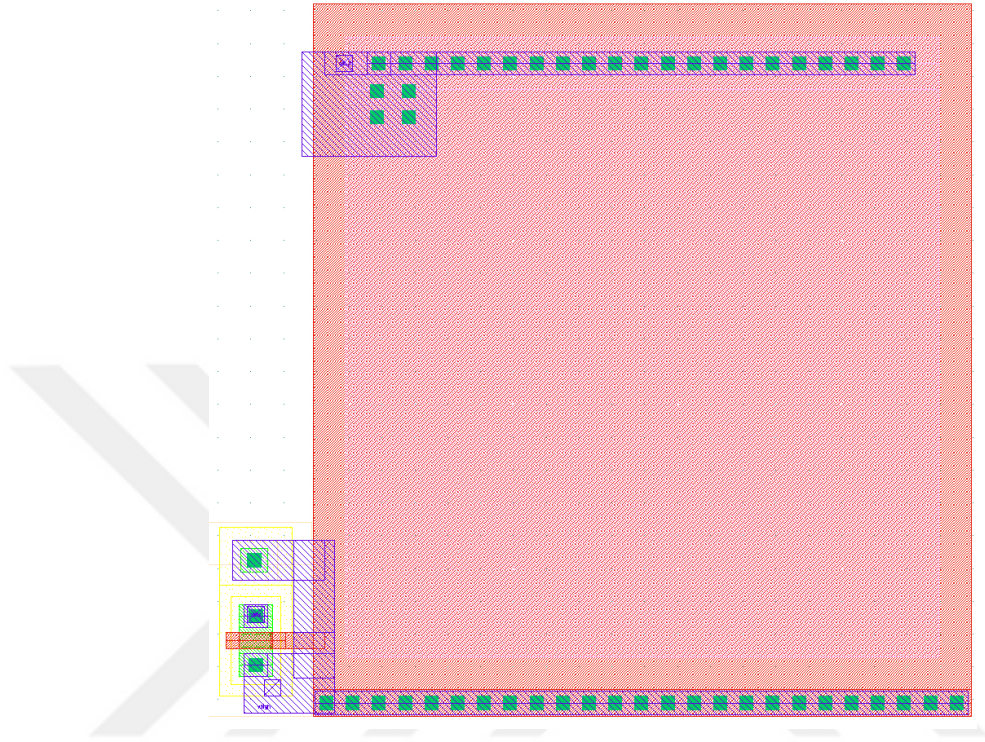


Figure 3.11: 1-Stage Charge Pump Layout

Since the transfer devices of the circuit are operated as diodes, at each stage, there will be a diode forward voltage drop. It is important to characterize this voltage drop to correctly estimate the needed number of stages for a given application. A post-layout simulation on extracted parameters was done to accurately show this diode voltage drop. The test circuit and the result is shown in Figure 3.12. The observed voltage drop of 0.8 Volts is in agreement with the manufacturer specifications.

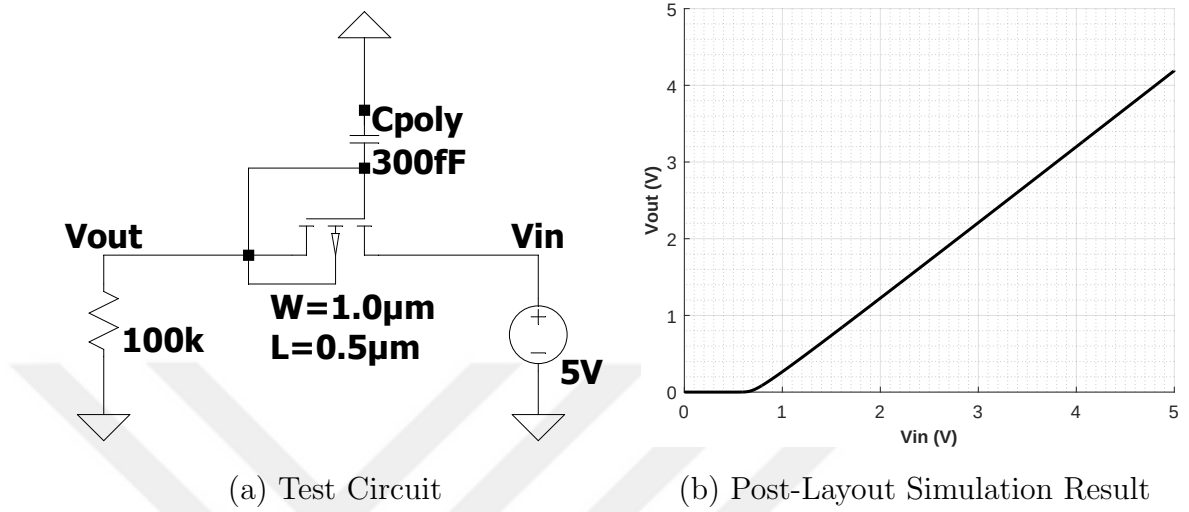


Figure 3.12: 1-Stage Charge Pump Diode Characteristics Post-Layout Simulation

3.3.3 Capacitive Timer Block

To achieve output voltage reduction after a certain amount of time, the circuit has to include timing circuits. One of the simplest and commonly used timing circuits is of course an R-C timer. A capacitive timer block was designed to serve as a time trigger control circuitry. The schematic is shown in Figure 3.13. Apart from supply and ground connections, there are three terminals of this block: Ctimer, Turn_OFF_Delay and Turn_On_Delay. Ctimer is a terminal connected to a pad of the manufactured chip where it can be accessed externally. An external capacitor connected between this pad and ground allows the user to program the delay time by selecting an appropriately sized delay capacitor. The time constant of the circuit is based on the connected capacitor value, internal resistor of 6.66 k Ω and the inverter threshold.

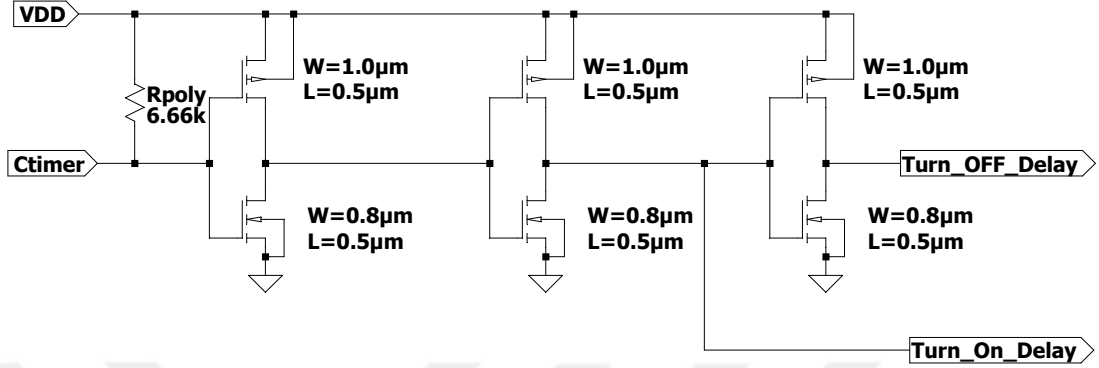


Figure 3.13: Capacitive Delay Timer Circuit

The operation of the circuit begins with the power up of the IC. Following the power up, the externally connected timing capacitor begins to charge up towards 5 Volts. When the voltage across the capacitor is lower than the V_{IH} of the input inverter, the input inverter output voltage stays at 5 Volts. It follows that the Turn_On_Delay voltage is LOW and Turn_OFF_Delay voltage is HIGH. When the capacitor charges above the V_{IH} , the input inverter changes state and other inverters follows as well. Thus after a time, determined by the capacitor value and internal circuit parameters, the Turn_On_Delay voltage becomes HIGH and Turn_OFF_Delay voltage becomes low. These voltages can be used to trigger any circuitry of choice.

At a given time t_1 , the voltage of the capacitor is given by Equation 3.21. Assuming that the initial capacitor voltage is zero then the trigger delay time t_{delay} can be calculated using Equation 3.22. Using these equations the capacitor value for the desired delay time can be calculated where V_C , V_{IH} and V_{DD} are capacitor voltage, inverter input high threshold and supply voltage respectively.

$$V_C = V_{DD} \times (1 - e^{-t_1/RC}) \quad (3.21)$$

$$t_{delay} = -RC \times \ln(1 - \frac{V_{IH}}{V_{DD}}) \quad (3.22)$$

The layout of the designed capacitive timer block is given in Figure 3.14. The

layout dimensions are $26.25\text{ }\mu\text{m} \times 15.25\text{ }\mu\text{m}$.

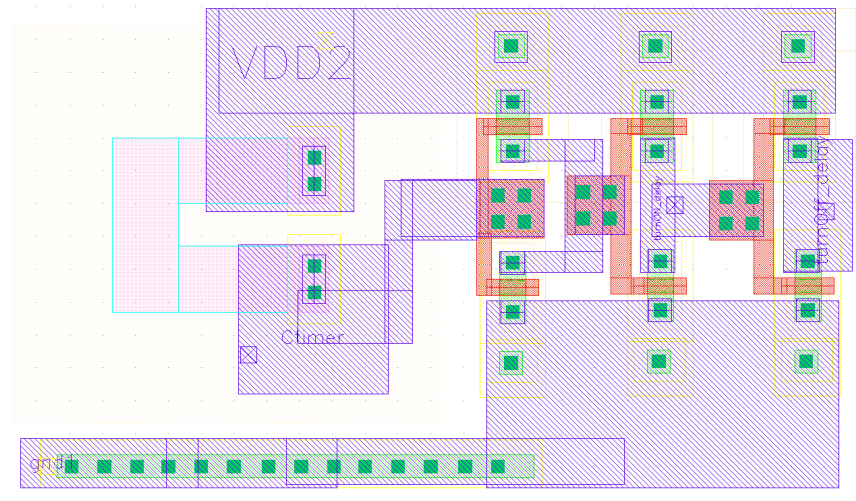
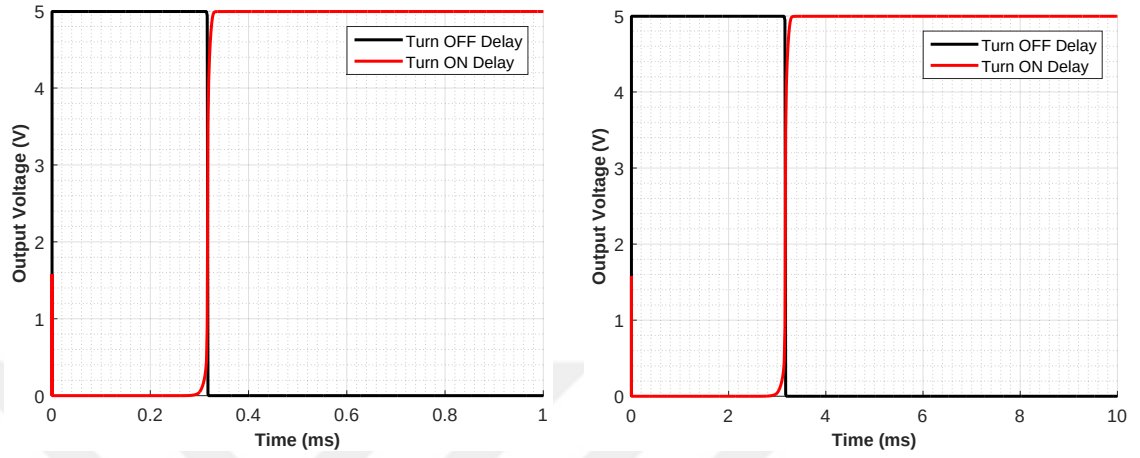


Figure 3.14: Capacitive Delay Timer Circuit Layout

In order to verify the timing controllability of the designed capacitive timer block, post-layout simulations were performed using extracted parameters. Two different cases were simulated using Spectre with two different standard valued timing capacitor values: 100nF and 1000nF . The resulting output signal waveforms are shown in Figure 3.15. 100nF capacitor resulted in 0.3ms delay whereas 1000nF capacitor resulted in 3ms delay. This is expected due to the increased time constant of the circuit as the capacitor value increases



(a) 100nF Delay Capacitor

(b) 1000nF Delay Capacitor

Figure 3.15: Capacitive Delay Timer Circuit Post-Layout Simulation

Using Equation 3.22 and the results of Figure 3.15, V_{IH} is extracted to be 1.81 Volts. For the circuit given in Figure 3.13, using Equation 3.22 the external capacitor value vs trigger delay graph is plotted as shown in Figure 3.16.

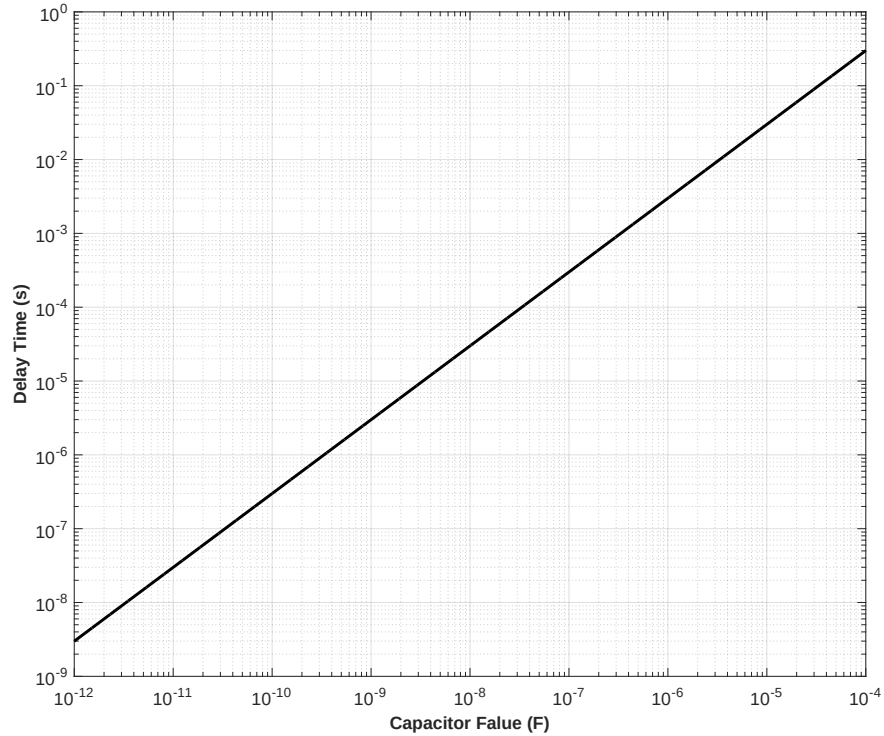


Figure 3.16: Capacitance vs Delay

3.3.4 Leakage Delay Block

The capacitive timer block which is explained in the previous subsection uses an internal resistor and an external capacitor to delay the triggering event. Another approach was shaped which uses both R and C components internally. This could have been achieved straight forwardly however in order to have long enough time delays the needed component values increase. This causes enlargement of the circuit area which is not desired. Thus, instead of using a determined value for a resistor we chose to use surface leakage path as a resistor.

Surface leakage properties of a chip mainly depends on the manufacturing process and the impurities in the environment. Therefore it is not possible to estimate the value of surface leakage, however in the past it was observed in our research group that such leakage paths exist and they can in fact charge MOSFET gate capacitances and turn floating gate MOSFETs ON. The circuit model is given in Figure 3.17.

The operation principle is exactly the same as the capacitive delay block. In leakage delay block, a 784fF polysilicon capacitor is used as the delay capacitor and according to the Equation 3.22 a delay will occur.

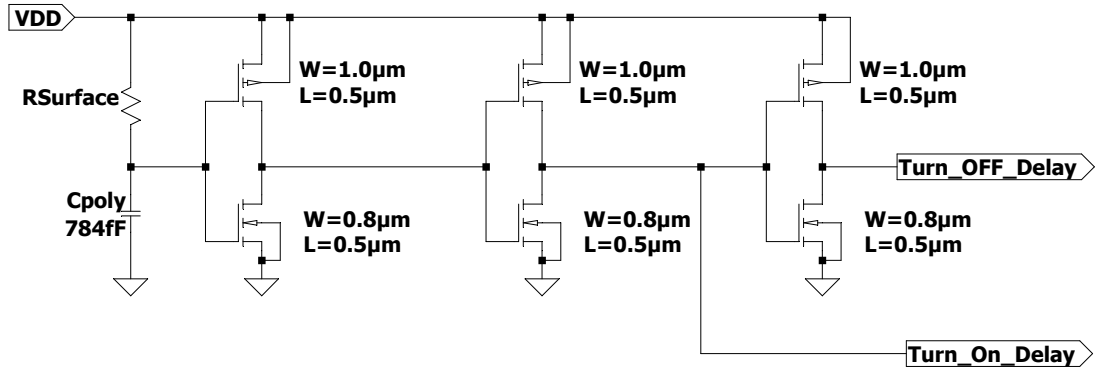


Figure 3.17: Leakage Delay Timer Circuit

The layout of this circuit is given in Figure 3.18. The surface leakage path is created using closely deposited metal paths on the same layer. The leakage paths were drawn equal thus, ignoring any leakage of the polysilicon delay capacitor,

The layout of this circuit is given in Figure 3.20. The layout dimensions are $60.75\text{ }\mu\text{m} \times 36.55\text{ }\mu\text{m}$.

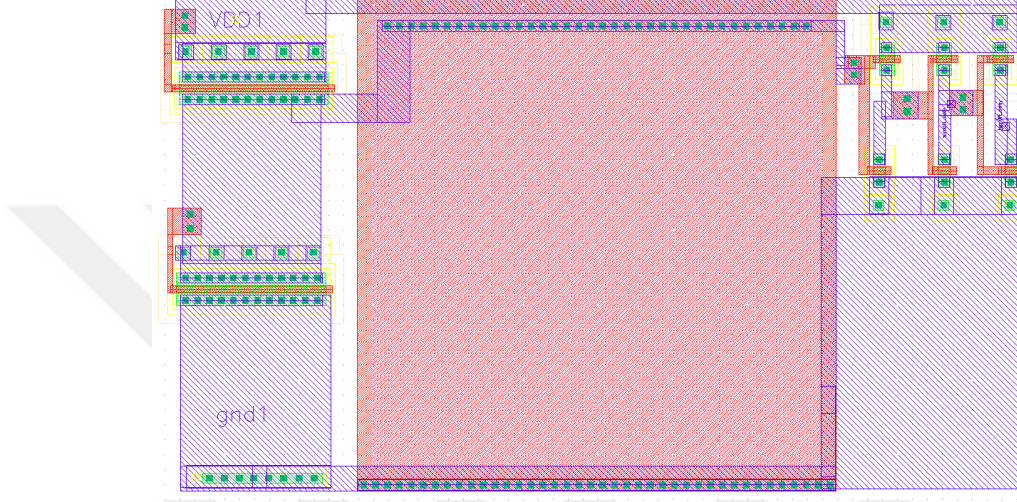


Figure 3.20: OFF PMOS Delay Timer Circuit Layout

3.4 Main Circuit Blocks

This section describes the main circuit blocks designed in this thesis. These main blocks are created by combining the sub-circuit blocks explained in the Section 3.3.

3.4.1 11 Stage Ring Oscillator

Dickson Charge Pumps require two out of phase clock signals to drive the charge pump stages as explained in Section 3.2. In this work, these clock signals were generated using a ring oscillator. A ring oscillator is an astable oscillating circuit created by cascading an odd number of inverters and tying the output to the input.

Odd number of stages provide the necessary condition for instability and the output oscillates between two possible values of the output inverter stage: 0

Volts and the supply voltage. In this thesis 11 stages of inverters were cascaded to create the oscillator as shown in Figure 3.21. The inverters used in each stage are same and the one explained in subsection 3.3.1.

11 Stage Ring Oscillator

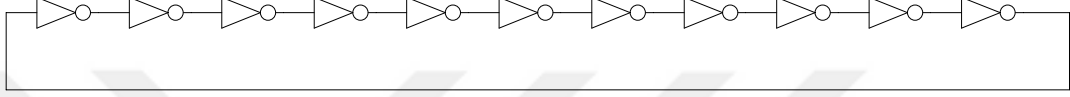


Figure 3.21: 11 Stage Ring Oscillator Circuit

Each stage of the cascaded ring delays the signal for a certain time t_{inverter} . For N stages, the total delay at the output becomes $N \times t_{\text{inverter}}$. Then, the oscillation frequency can be calculated using Equation 3.23.

$$f_{\text{oscillation}} = \frac{1}{2 \times N \times t_{\text{inverter}}} \quad (3.23)$$

The ring oscillator as shown in Figure 3.21 has a single clock output. In order to generate two out of phase clock signals, an output stage is required. This output stage will generate the clock signals to drive the pumping capacitors. Therefore this stage should be sized enough to handle the current draw needed by the pump capacitors. In this thesis a buffer circuit was designed with wide output transistors to provide enough current. The circuit consists of two parallel buffer legs where the bottom leg inverts the signal and the top leg inverts it twice to generate the same clock signal. This topology, shown in Figure 3.22, generates the necessary clock signals from the ring oscillator output.

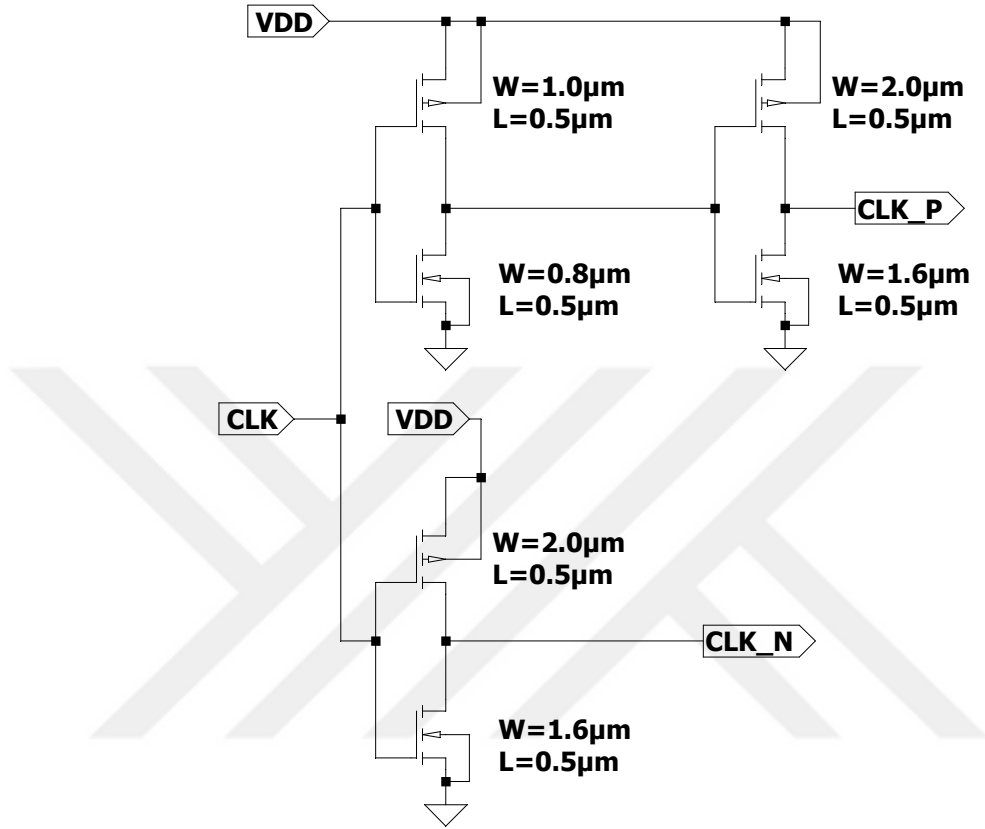


Figure 3.22: Ring Oscillator Output Stage Circuit

Ring oscillator is connected directly at the input of this output buffer circuitry. Since the ring drives two parallel inverters with high impedance inputs, the buffer stage will not load the oscillator and therefore will not interfere with its operation. The overall circuit is shown in Figure 3.23.

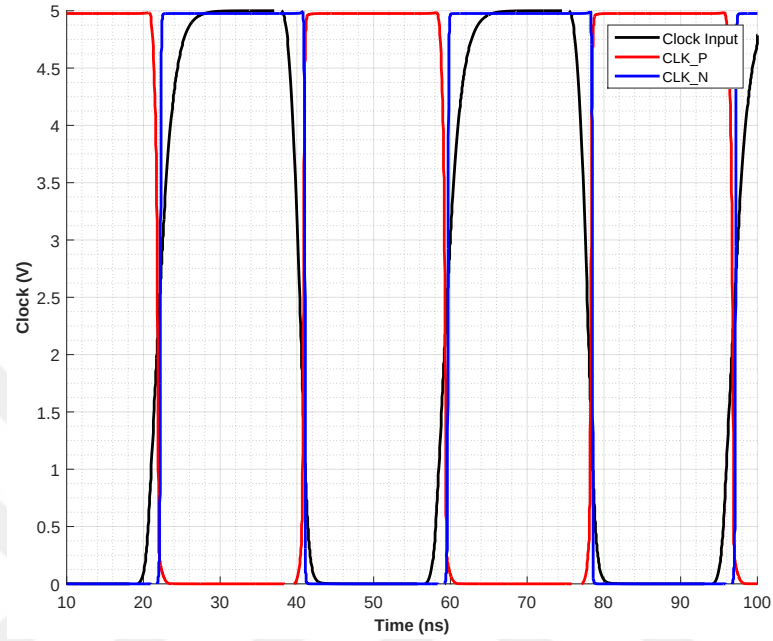


Figure 3.24: 11 Stage Ring Oscillator Transient Simulation with Output Stage

Ring oscillator layout is shown in Figure 3.25 which is basically 11 inverters, which was shown in Figure 3.8, cascaded. The layout dimensions are $71\text{ }\mu\text{m}$ x $49\text{ }\mu\text{m}$.

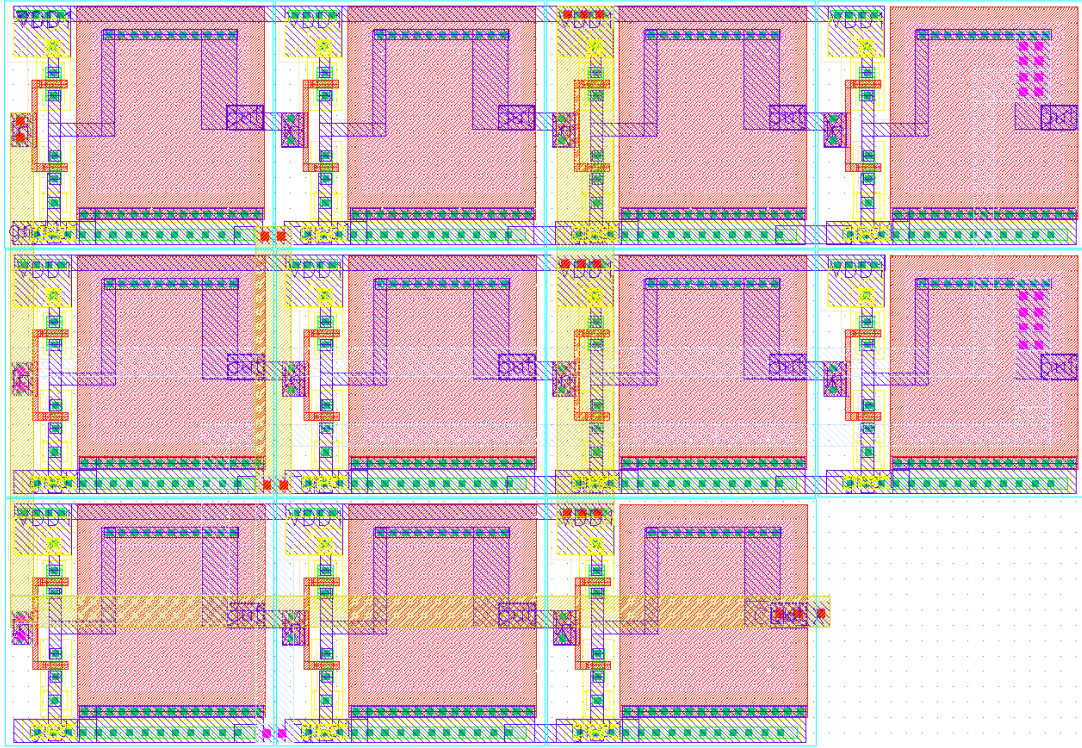


Figure 3.25: 11 Stage Ring Oscillator Layout

The completed oscillator layout with output stage and two complementary clock outputs is shown in Figure 3.26. The layout dimensions are $60.75\text{ }\mu\text{m}$ x $36.55\text{ }\mu\text{m}$.

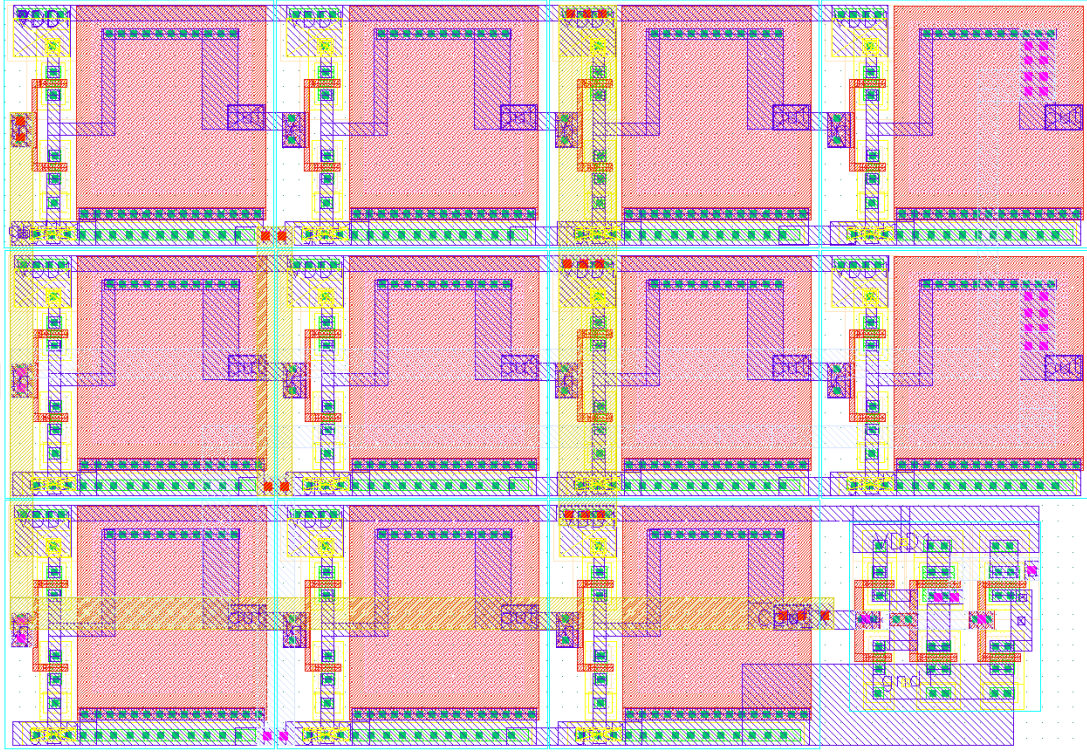


Figure 3.26: 11 Stage Ring Oscillator with Output Stage Layout

Post-layout SPICE simulations of the ring oscillator is carried out using extracted parameters. Resulting oscillating waveform is shown in Figure 3.27 where 11 Stage 100fF cascaded inverter ring oscillator generates 22 MHz square wave.

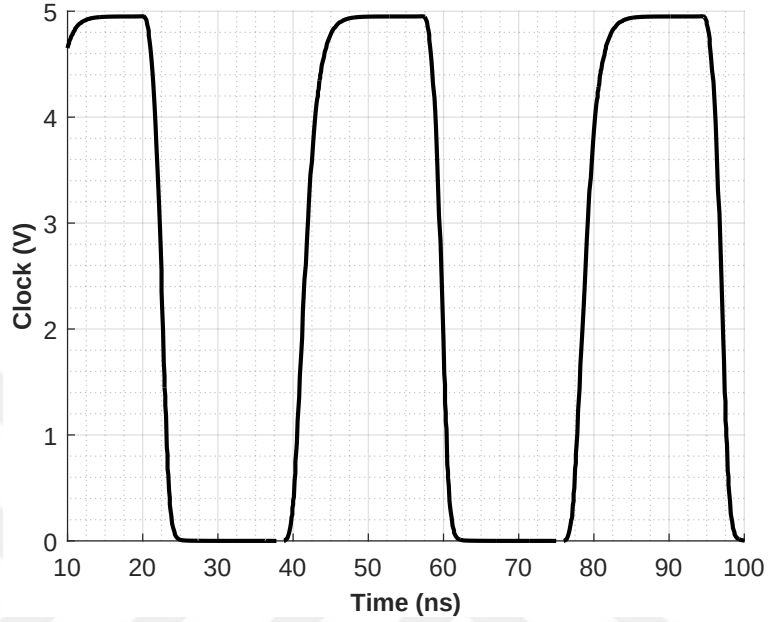


Figure 3.27: Ring Oscillator Post-Layout Simulation

3.4.2 Three Stage Charge Pump

A three stage charge pump circuit was designed using the charge pump blocks shown in Figure 3.10. The designed charge pump circuit is given in Figure 3.28. CLK_N and CLK_P signals are two out of phase clock signals which were generated using the ring oscillator circuit shown in Figure 3.23.

Unlike the usual Dickson Charge Pump topology described in Section 3.2, the circuit in this work has a grounded input signal at the first stage. This clamps the first pumping stage voltage to above ground level. Using grounded input reduces the available output voltage level by an amount equal to the supply voltage. However by grounding the input, any intentional or unintentional grounding in the following stages do not short the supply thus providing additional design flexibility. This will be explained more in the following subsection.

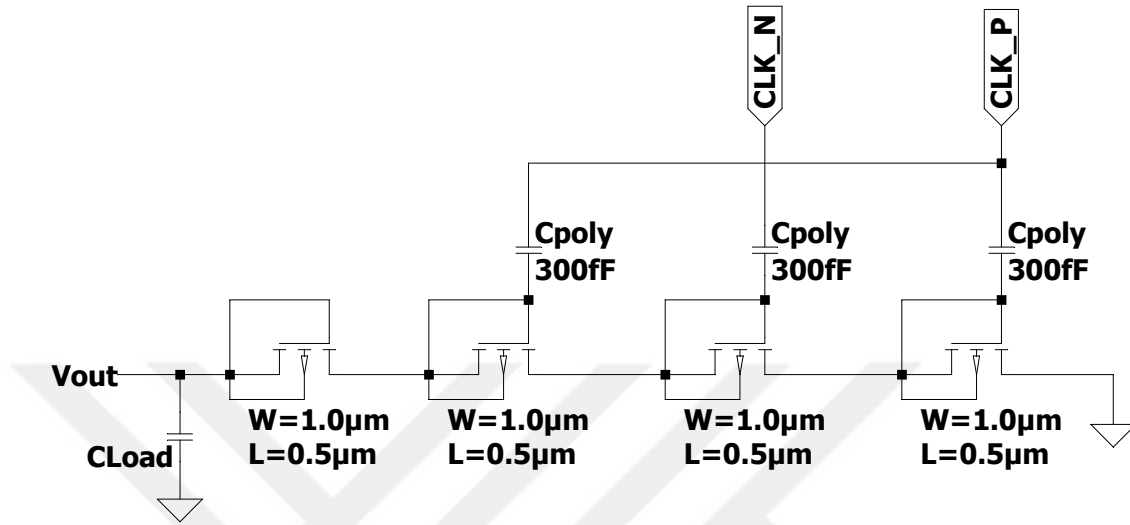


Figure 3.28: Three Stage Charge Pump Circuit

Layout of the three stage charge pump is shown in Figure 3.29. The layout dimensions are $100\mu\text{m} \times 75\mu\text{m}$. To provide a supply capacitance in order to reduce the conducted noise, a 800 fF DC supply capacitor was also placed inside the layout.

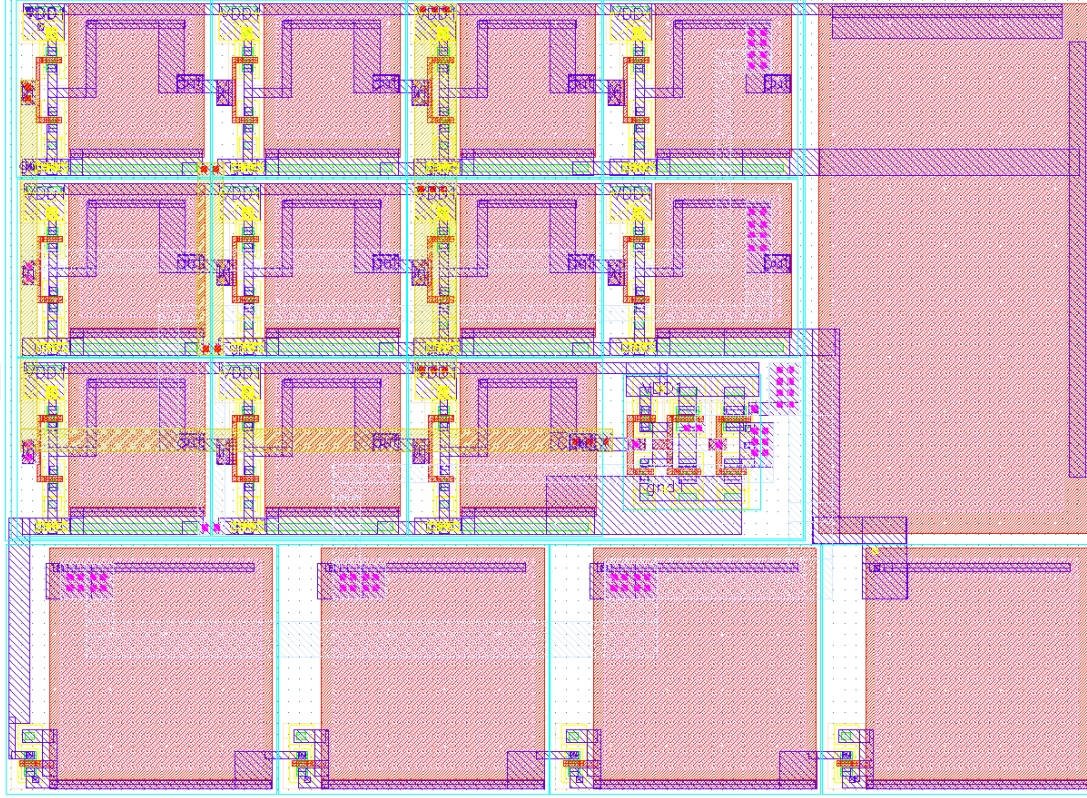


Figure 3.29: Three Stage Charge Pump Layout

Expected output voltage of an N stage charge pump can be calculated using the Equation 3.24 where V_{forward} is the diode forward voltage drop of each stage. This equation differs from what was explained in Section 3.2 due to the grounded input stage. The V_{forward} is calculated using Spectre in Subsection 3.3.2 to be around 0.8 Volts. Thus using Equation 3.24 and taking Vdd as 5 Volts, N as 3 the output voltage can be calculated as 11.8 Volts.

$$V_{\text{out}} = N \times V_{\text{dd}} - (N + 1) \times V_{\text{forward}} \quad (3.24)$$

Spectre transient simulation is carried out. The output load is selected to be a 1pF capacitor and the supply voltage is ramped up from 0 Volts to 5 Volts. The resulting output voltage waveform is shown in Figure 3.30.

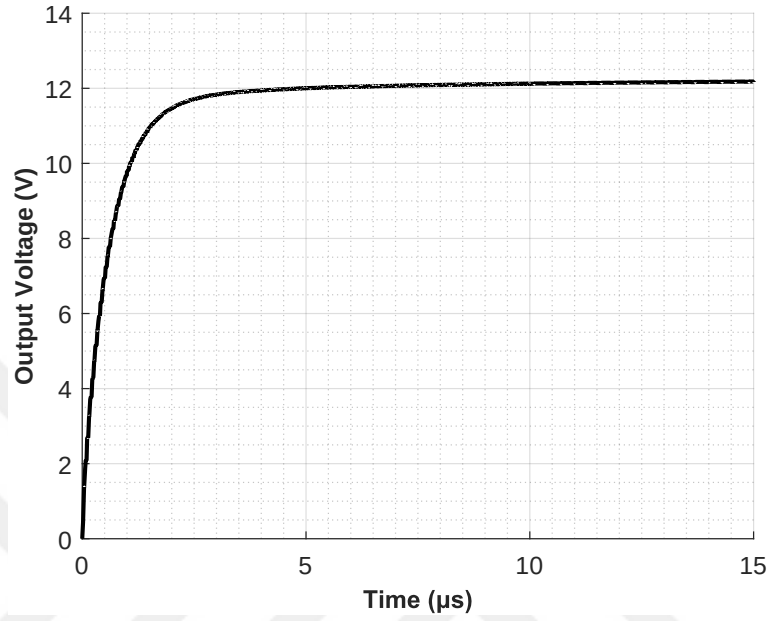


Figure 3.30: Threee Stage Charge Pump Transient Spice Simulation

3.4.3 Four Stage Charge Pump

A Four Stage charge pump circuit was designed using the charge pump blocks shown in Figure 3.10. The designed circuit is given in Figure 3.31. CLK_N and CLK_P signals are the driver clock signals which were generated using the ring oscillator circuit shown in Figure 3.23. Four stage charge pump provides the base of this thesis since the required output voltage levels around 15 Volts can be achieved with a Four Stage topology.

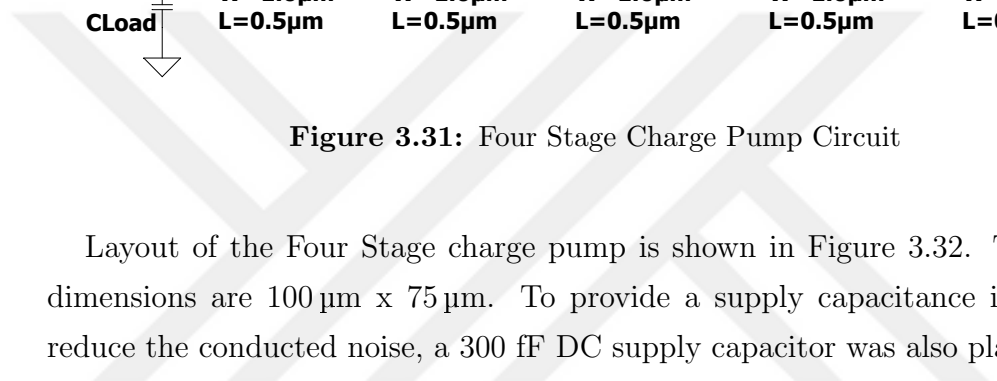


Figure 3.31: Four Stage Charge Pump Circuit

Layout of the Four Stage charge pump is shown in Figure 3.32. The layout dimensions are $100\mu\text{m} \times 75\mu\text{m}$. To provide a supply capacitance in order to reduce the conducted noise, a 300 fF DC supply capacitor was also placed inside the layout.

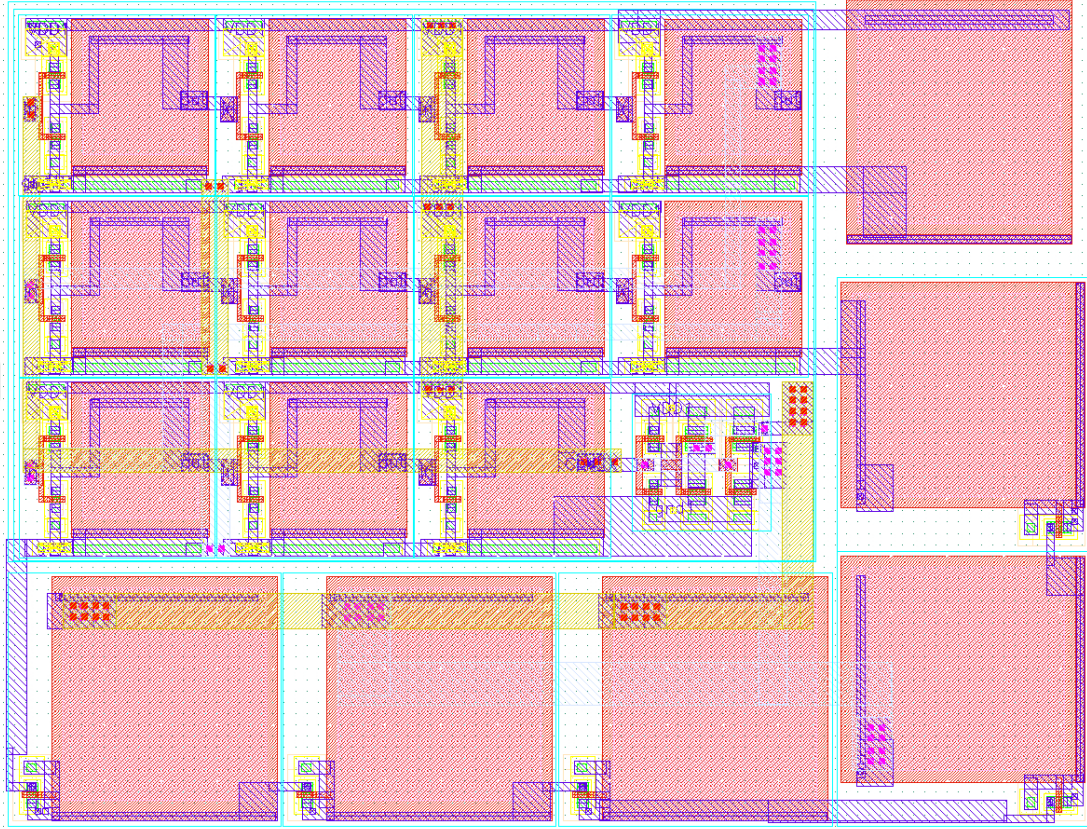


Figure 3.32: Four Stage Charge Pump Layout

Spectre simulation of the Four Stage Charge Pump is carried out. The output load is selected to be a 1pF capacitor and the supply voltage is ramped up from 0 Volts to 5 Volts. The resulting output voltage waveform is shown in Figure 3.33. The output voltage levels of 16 Volts is in agreement with the Equation 3.24.

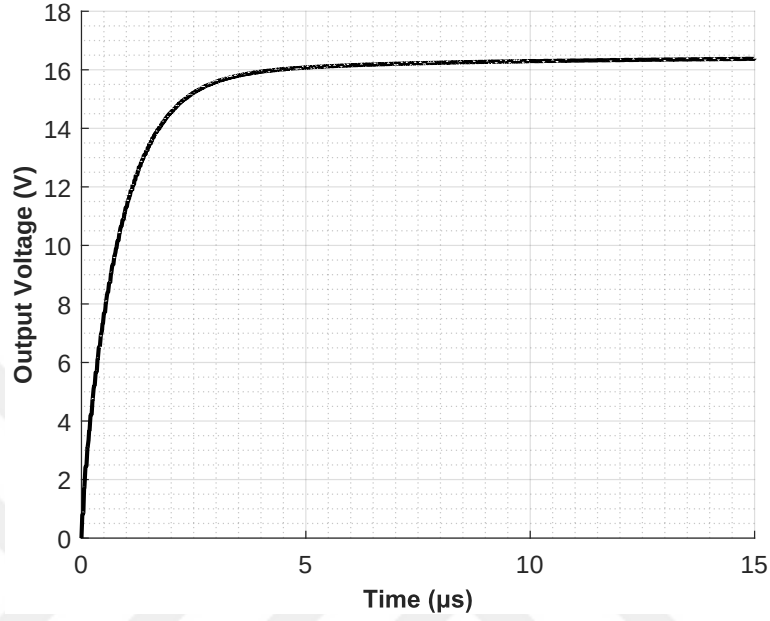


Figure 3.33: Four Stage Charge Pump Spice Simulation

As explained in the Section 3.1, there is a need to reduce the output voltage some time after settling around 15 Volts. This problem was approached using three different circuits which are explained in the following subsection.

3.4.3.1 Delayed Output Voltage Reduction

The main voltage reduction approach employed in this work is basically reducing the effective number of stages of the Four Stage charge pump circuit mid-operation. This is achieved by grounding the output of one of the first pump stage thus reducing the circuit into a Three Stage charge pump. In the general Dickson topology explained in the Section 3.2, this cannot be done because the input is connected to the power supply, thus any grounding of following stages would result in a shorting of the supply which is not desired.

Required grounding of the first stage is done with an NMOS transistor connected as shown in Figure 3.34. When the DELAY_CONTROL signal is LOW, the NMOS is OFF and the circuit acts as a Four Stage charge pump. However

when the control signal is asserted HIGH, the NMOS turns ON, shorting the first stage and reducing the effective number of stages by one.

This approach can be generalized to achieve different voltage levels and reduction or increase mechanisms. For instance if the default control signal is HIGH, and after a delay it becomes LOW, then the output voltage increases. Control NMOS transistor is objected to a voltage stress increasing as the number of stages it can bypass increases. In this work at startup the control signal was designed to be LOW, thus Four Stage pump operates to generate 15 Volts from 5 Volts supply. After a delay the control signal is asserted HIGH, reducing the topology to Three Stage Pump and reducing the output voltage to 12 Volts as required.

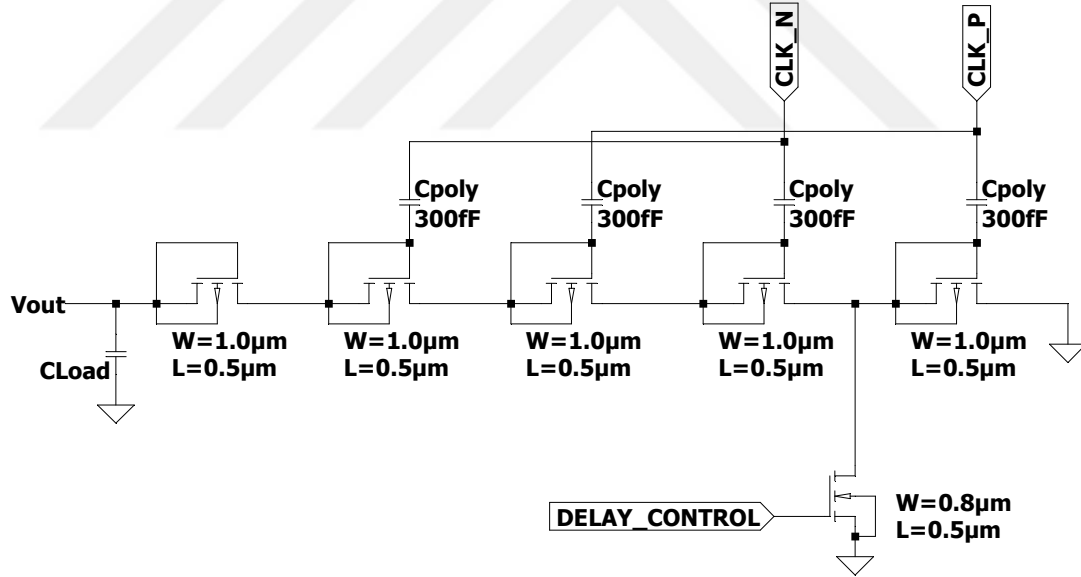


Figure 3.34: Output Voltage Reduction Control Circuit

The generation of the control signal DELAY_CONTROL is accomplished using three different time delay circuitry which are explained as follows.

3.4.3.1.1 Delayed Output Voltage Reduction Using an External Capacitor

First approach is based on the capacitive timer block explained in the subsection 3.3.3. The capacitive timer block is connected to a Four Stage Charge Pump as shown in Figure 3.35 where the Turn_On_Delay output of the delay block is used as the DELAY_CONTROL signal thus assuring a voltage reduction operation after a time delay.

The time delay expected by this topology can be calculated as shown in subsection 3.3.3 using Equation 3.22.

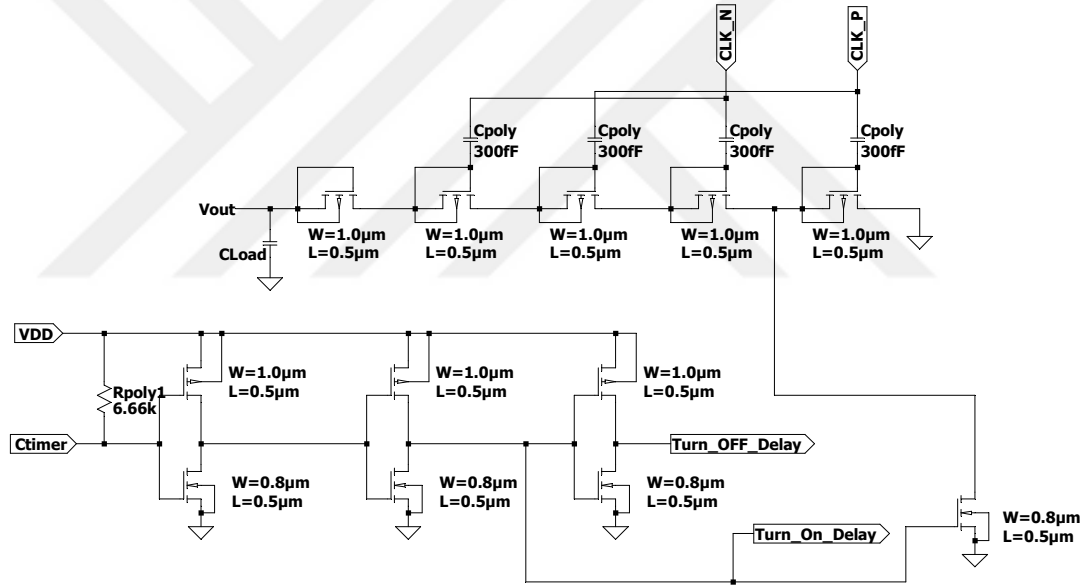


Figure 3.35: Four Stage Charge Pump Circuit with Capacitor Programmable Output Voltage Reduction

Layout of the Four Stage charge pump with capacitive timer delay control block is shown in Figure 3.36. The layout dimensions are $100\mu\text{m} \times 94.3\mu\text{m}$. To provide a supply capacitance in order to reduce the conducted noise, a 600 fF DC supply capacitor was also placed inside the layout.

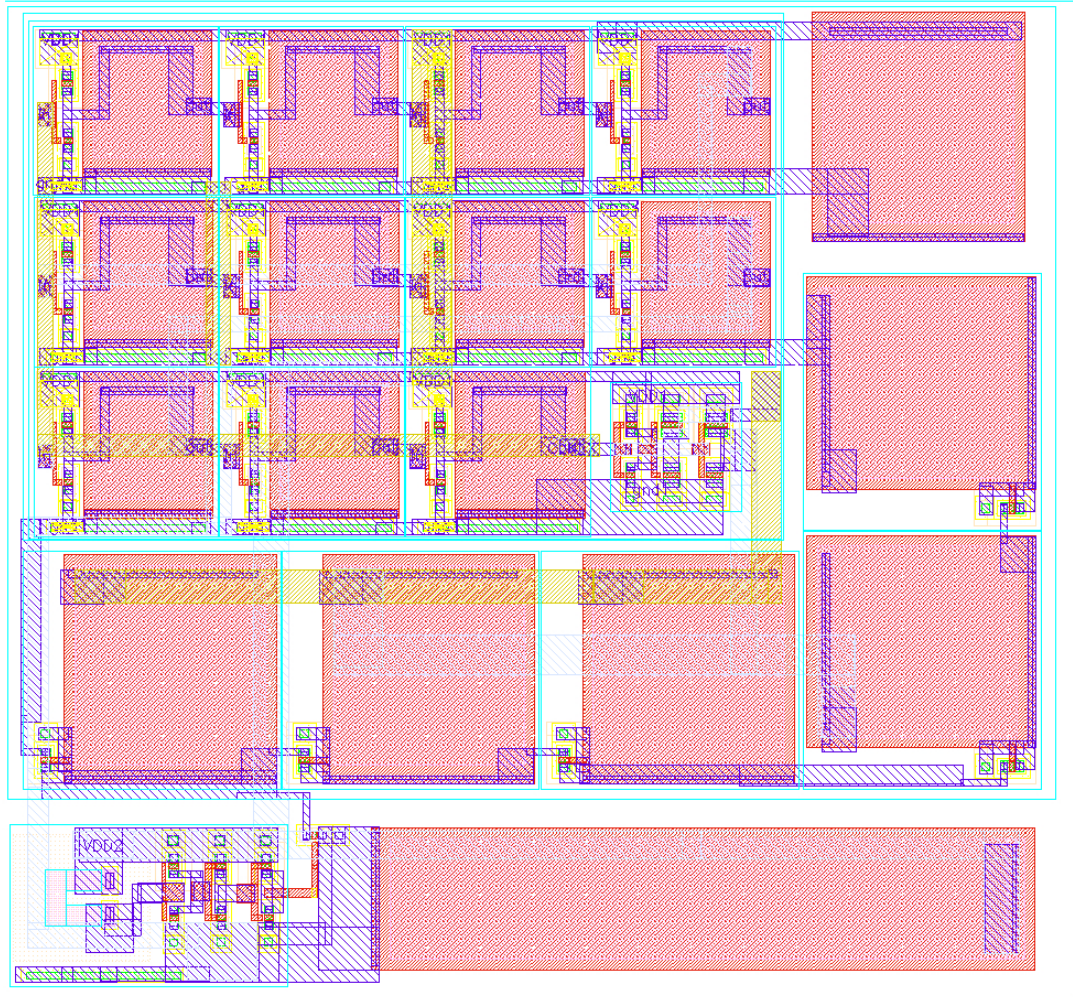


Figure 3.36: Four Stage Charge Pump Layout with Capacitor Programmable Output Voltage Reduction

Transient simulation of the Four Stage Charge Pump with capacitive timer block is carried out on Spectre. The output load is selected to be a 1pF capacitor and the supply voltage is ramped up from 0 Volts to 5 Volts. The resulting output voltage waveform is shown in Figure 3.37. The output voltage levels of 15 Volts and 12 Volts are in agreement with the Equation 3.24. 18 μ s delay was achieved using a 5nF external delay capacitor. This delay time can be increased or decreased using different values for the delay capacitor.

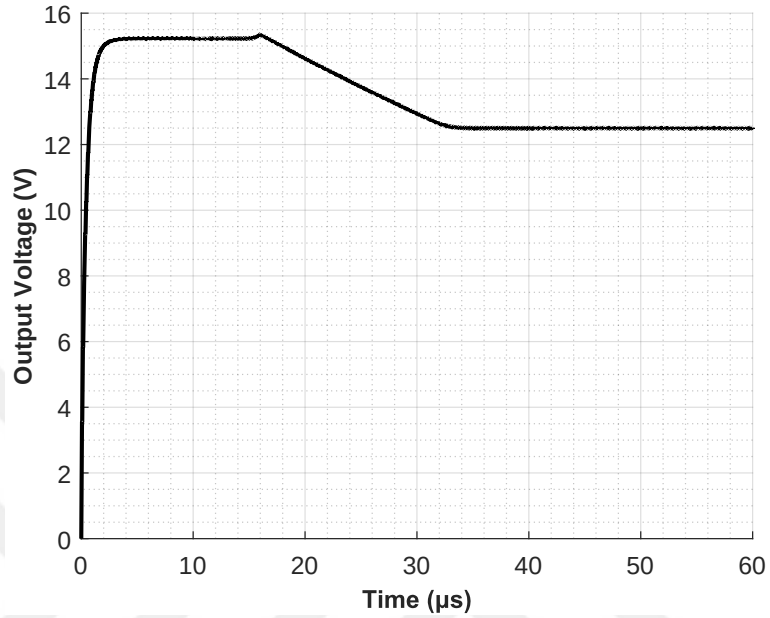


Figure 3.37: Four Stage Charge Pump Transient Simulation with 5nF External Delay Capacitor

3.4.3.1.2 Delayed Output Voltage Reduction Using an Surface Leakage Currents

Second approach used to generate the DELAY_CONTROL signal is based on surface leakage block which is explained in subsection 3.3.4. Similar to what is done with the capacitive delay block, the circuit is connected to the Four Stage Charge Pump as shown in Figure 3.38. Expected time delay is dependent in $R_{surface}$, C_{poly} and V_{IH} as it was explained previously. The Turn_On_Delay control signal is used to generate a voltage reduction after a time delay.

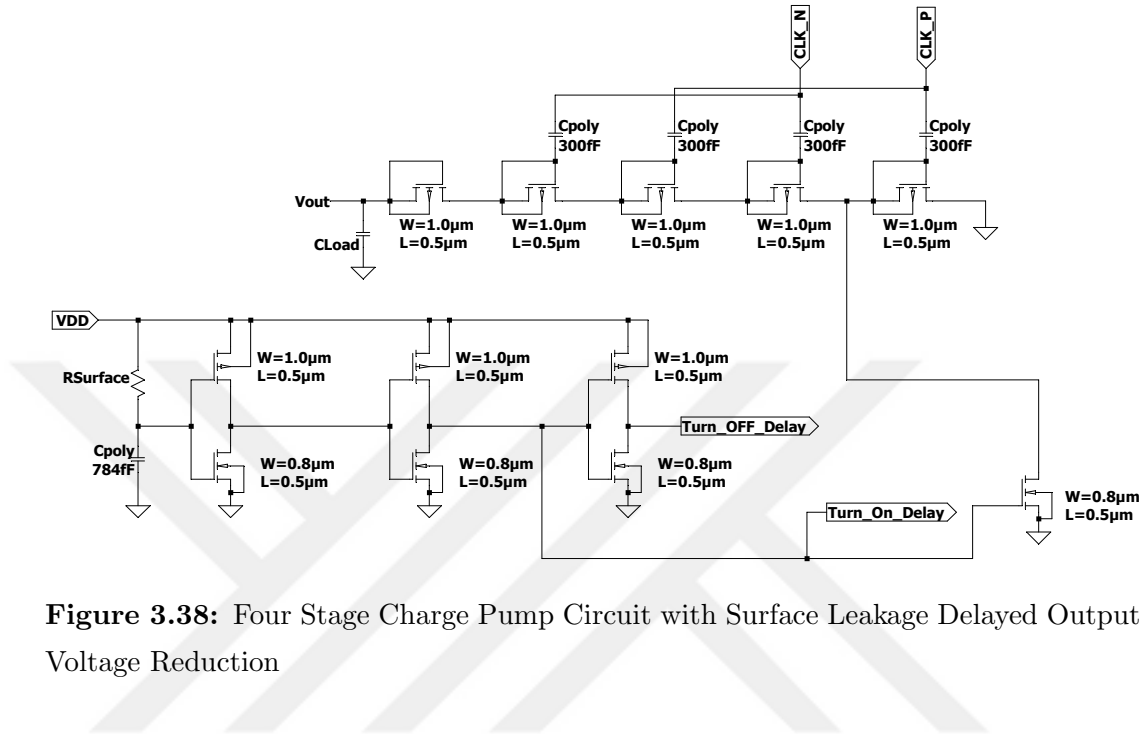


Figure 3.38: Four Stage Charge Pump Circuit with Surface Leakage Delayed Output Voltage Reduction

Layout of the Four Stage charge pump with surface leakage timer delay control block is shown in Figure 3.39. The layout dimensions are 102 μm x 115 μm . To provide a supply capacitance in order to reduce the conducted noise, a 600 fF DC supply capacitor was also placed inside the layout.

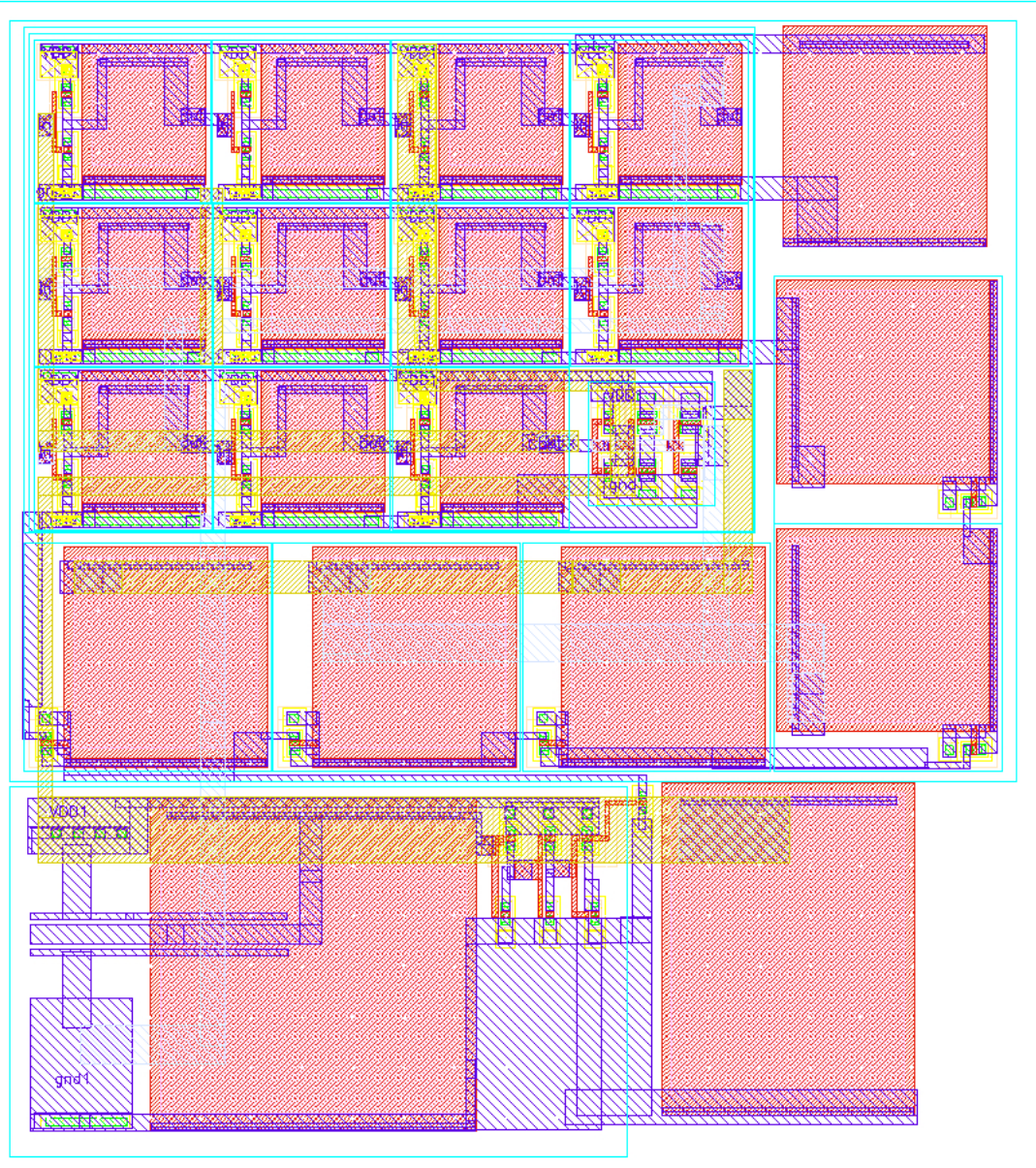


Figure 3.39: Four Stage Charge Pump Layout with Leakage Delayed Output Voltage Reduction

3.4.3.1.3 Delayed Output Voltage Reduction Using OFF PMOS Currents

Third and last approach used to generate the DELAY_CONTROL signal is

based on OFF-PMOS Delay block which is explained in subsection 3.3.5. The circuit is connected to the Four Stage Charge Pump as shown in Figure 3.40. The Turn_On_Delay control signal is connected to the DELAY_CONTROL pin to generate a voltage reduction after the time delay.

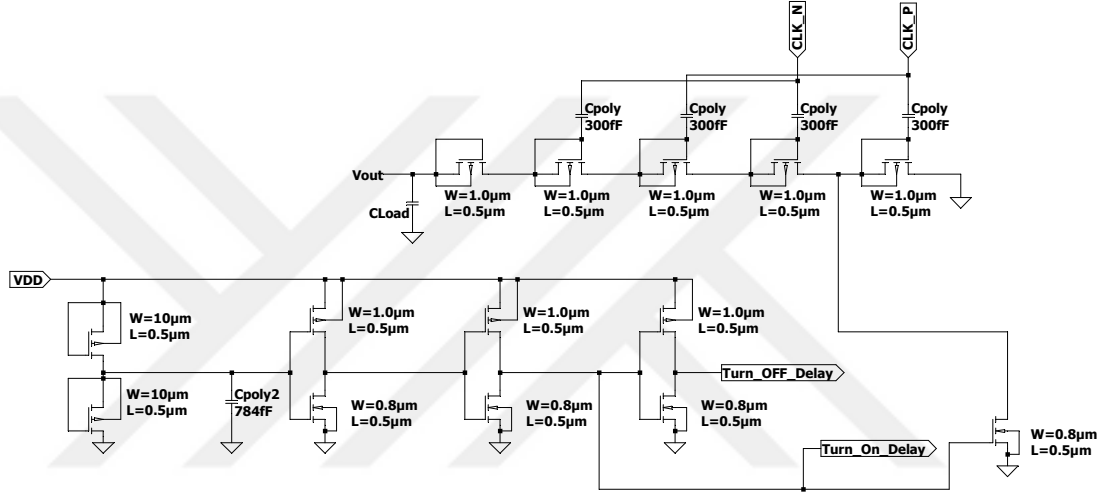


Figure 3.40: Four Stage Charge Pump Circuit with OFF PMOS Delayed Output Voltage Reduction

Layout of the Four Stage charge pump with OFF-PMOS timer delay control block is shown in Figure 3.41. The layout dimensions are $102\mu\text{m} \times 115\mu\text{m}$. To provide a supply capacitance in order to reduce the conducted noise, a 600 fF DC supply capacitor was also placed inside the layout.

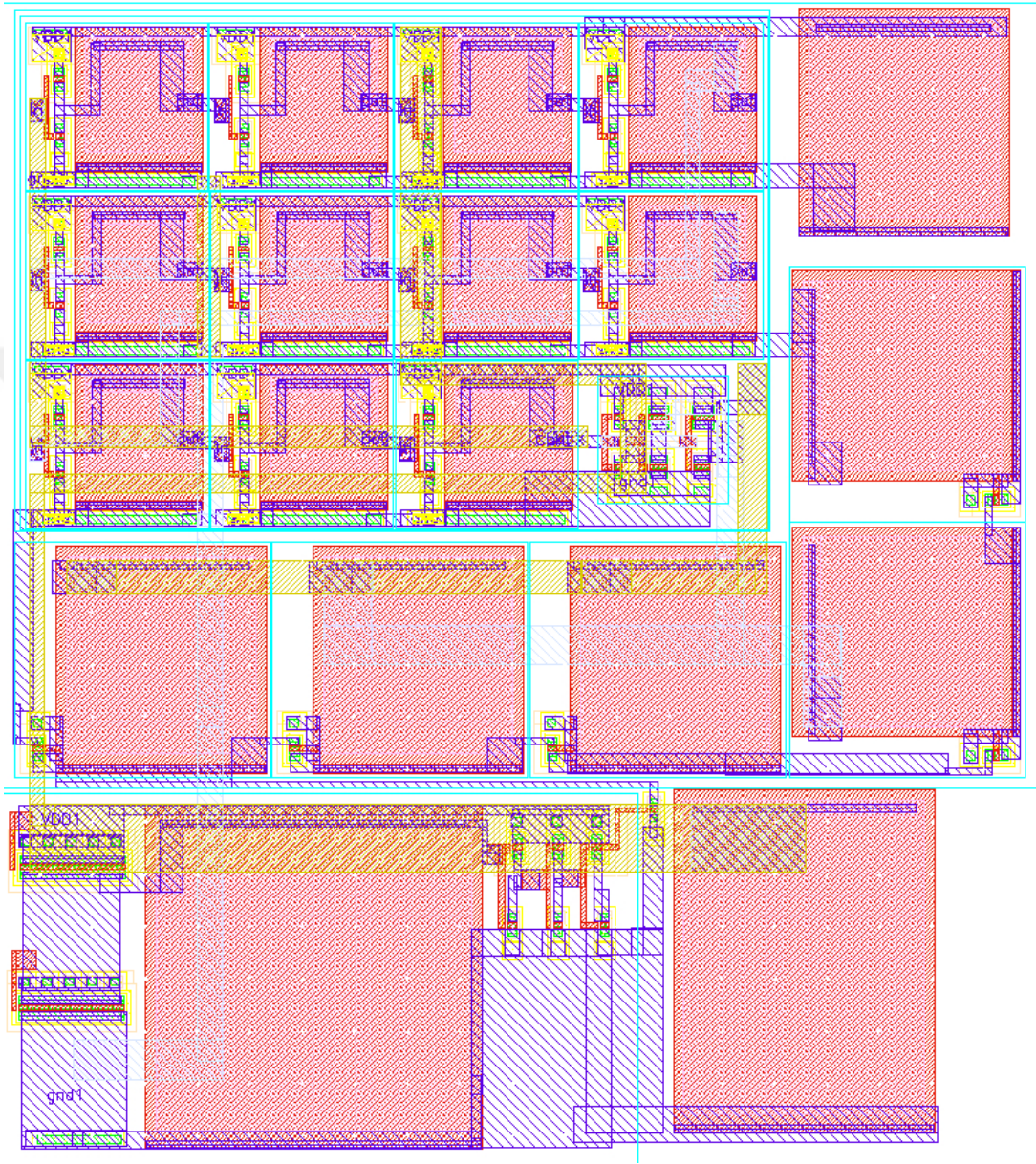


Figure 3.41: Four Stage Charge Pump Layout with OFF PMOS Delayed Output Voltage Reduction

3.5 Post-Layout Simulations and Layout Considerations

This section first provides the post-layout simulation results of the main circuit blocks then describes the final layout design considerations of the chip.

3.5.1 Post-Layout Simulations

Layout parasitics of the proposed main circuit blocks are extracted using Assura QRC tool in order to simulate the designed layout correctly with parasitics also taken into account.

Post-layout Spectre simulation with 1 M Ω load resistors at each output is carried out for 11 Stage Ring Oscillator with output stage using extracted parameters. Two out of phase clock outputs with 25 MHz oscillation are shown in Figure 3.42. It appears that the designed layout does not hinder the operation of the oscillator circuitry.

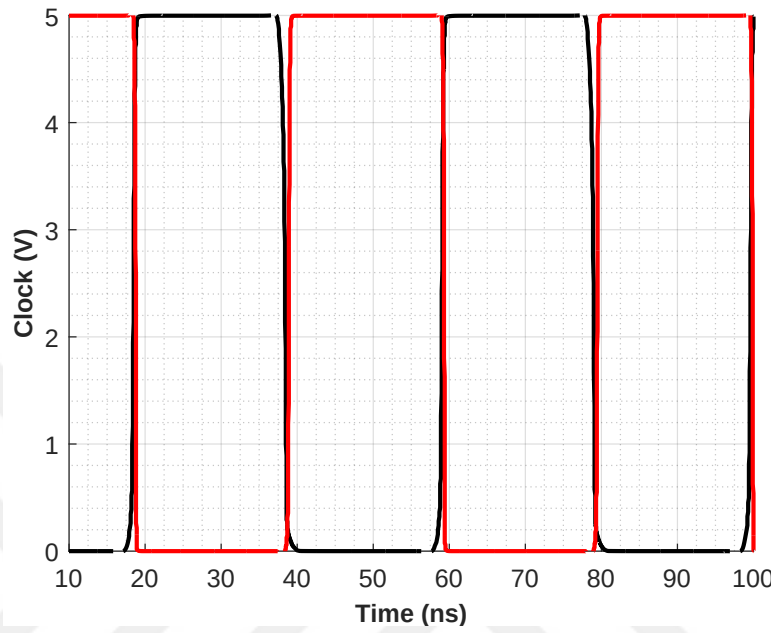


Figure 3.42: 11 Stage Ring Oscillator Post-Layout Simulation with Output Stage

Three Stage charge pump layout parameters are extracted and simulated with 1pF output capacitor while the supply voltage is ramped up from 0 Volts to 5 Volts. The resulting output voltage waveform is shown in Figure 3.43. The extracted capacitive parasitics showed around 70 pF sized stray capacitances to ground from each pumping node. This in return caused a reduction in the output voltage in accordance with the formula given in Equation 3.15.

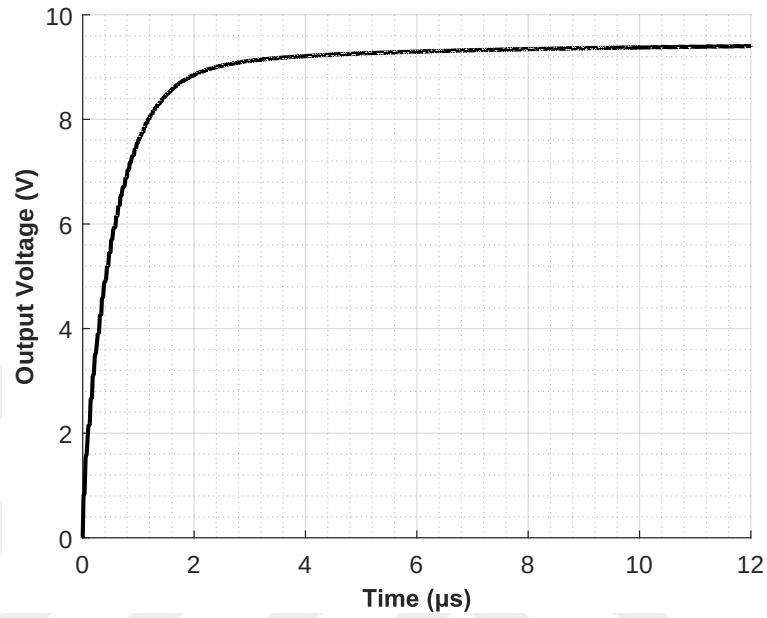


Figure 3.43: Three Stage Charge Pump Post-Layout Simulation

Four Stage charge pump layout parameters are extracted and simulated with 1pF output capacitor while the supply voltage is ramped up from 0 Volts to 5 Volts. The resulting output voltage waveform is shown in Figure 3.44. Since the layouts of Three Stage and Four Stage charge pumps have the same pumping stages, the extracted capacitive parasitics were also the same which were around 70 pF sized stray capacitances to ground from each pumping node. This again showed itself as a reduction in the output voltage in accordance with the previous discussions.

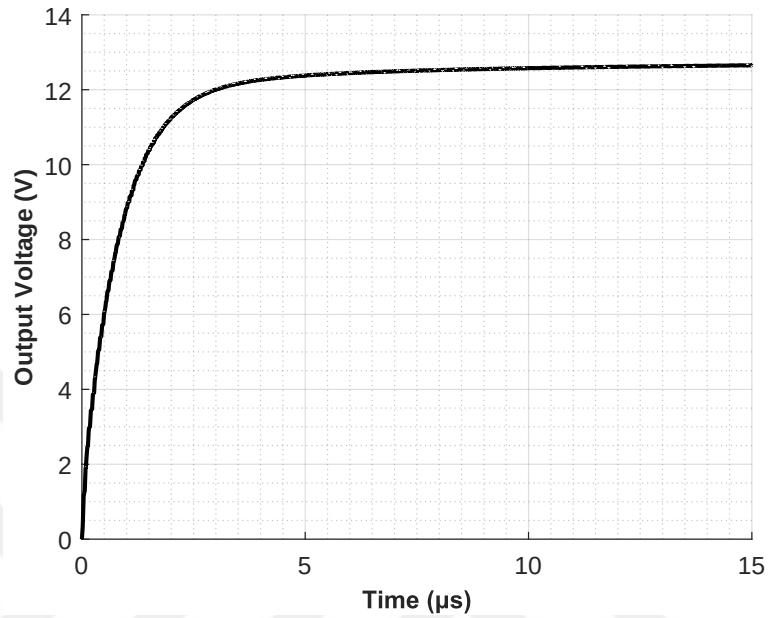


Figure 3.44: Four Stage Charge Pump Post-Layout Simulation

Post-layout simulation of the Four Stage Charge Pump with capacitive timer block is carried out. The output load is selected to be a 1pF capacitor and the supply voltage is ramped up from 0 Volts to 5 Volts. The resulting output voltage waveform is shown in Figure 3.45. Output voltage levels are smaller than those of the transient simulation results due to the parasitic stray capacitances. 18 μs delay was achieved using a 5nF external delay capacitor. This delay time is in accordance with the transient simulation results given in Figure 3.37. It was not affected by the layout properties since the 5 nF delay capacitor and 6.66 k Ω charging resistor values are too large to be affected by parasitics.

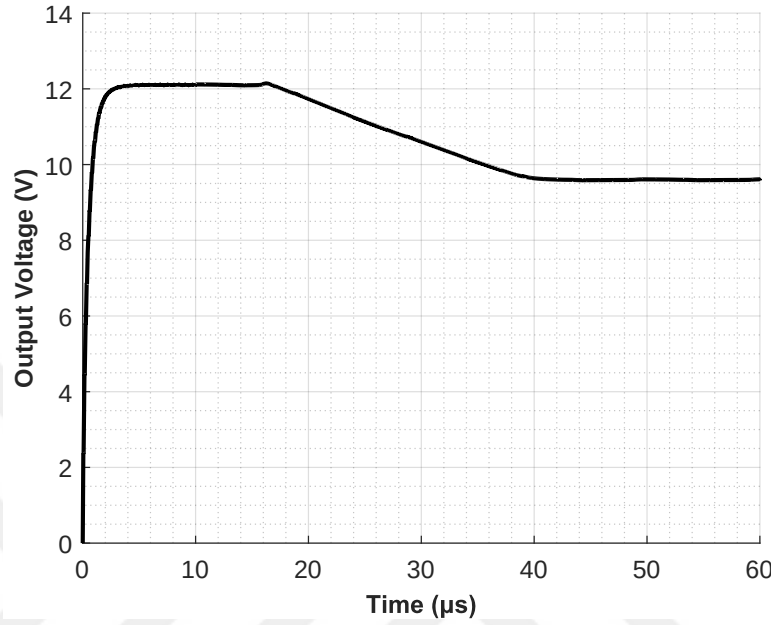


Figure 3.45: Four Stage Charge Pump Post-Layout Simulation with 5nF External Delay Capacitor

3.5.2 Final Layout Design

After finishing the layout designs of main circuit blocks, it is needed to bring separate designs together in a single chip for manufacturing. In this section, the step of collecting and putting circuit blocks with different functions together on the same chip in a way that it is possible to test the chip on a PCB is described.

3.5.2.1 PAD selection

It is required to have some kind of an interface blocks between our chip and the outside world in order to have a way to access and interact with our circuitry. That interface block is called a Pad, which provides a surface large enough for wire bonding to a PCB while connecting to the inner circuitry of the chip. Since a PAD is the point of the chip opening to the outside world, it is the most vulnerable location to external effects such as overvoltage conditions, reverse voltage conditions and electrostatic discharge also known as ESD. Therefore most

PADs include some protection circuitry against such disturbances to protect the chip from failing.

In this design three types of PADs were used: VDD PAD, GND PAD and Signal PAD. Simplified schematic of a VDD PAD is shown in Figure 3.46. The PAD has a large metal surface which is suitable for wire bonding. Two diodes shown in the schematic are protecting the inner circuitry from reverse polarity voltages at the power nets by clamping it to the ground. Furthermore, low level of ESD can be dissipated on these diodes assuming the dissipated energy does not exceed the limits of the diodes so that the breakdown is reversible. Of course for any serious ESD protection larger diodes with higher ratings should be used.

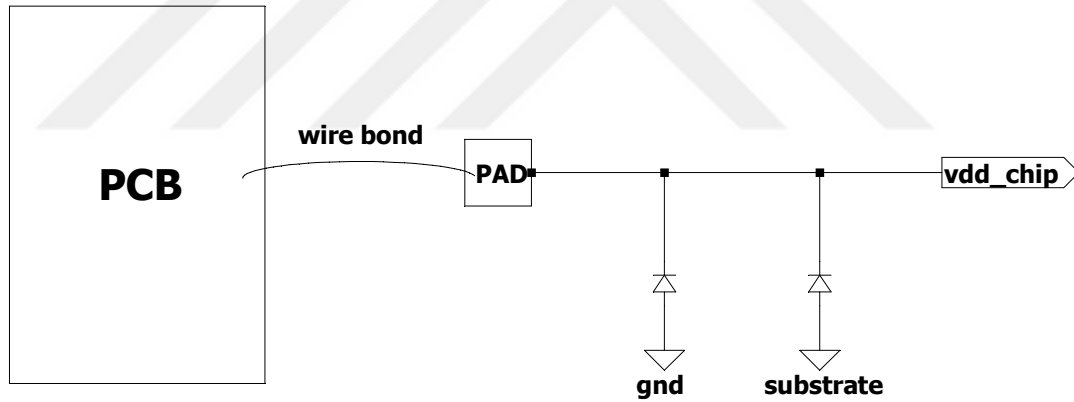


Figure 3.46: VDD PAD Schematic

The PAD used in this work is chosen from the manufacturer's library of available PADs. Each PAD has connections to GND and VDD strips so that each consecutive PAD will see the same ground and power potentials.

The schematic of the used ground PAD is given in Figure 3.47. This PAD provides ground reference connections to the substrate and circuits. It has a diode connecting to the power strip which clamps the ground voltage to a value lower than the supply voltage thus protecting circuits from reverse voltages.

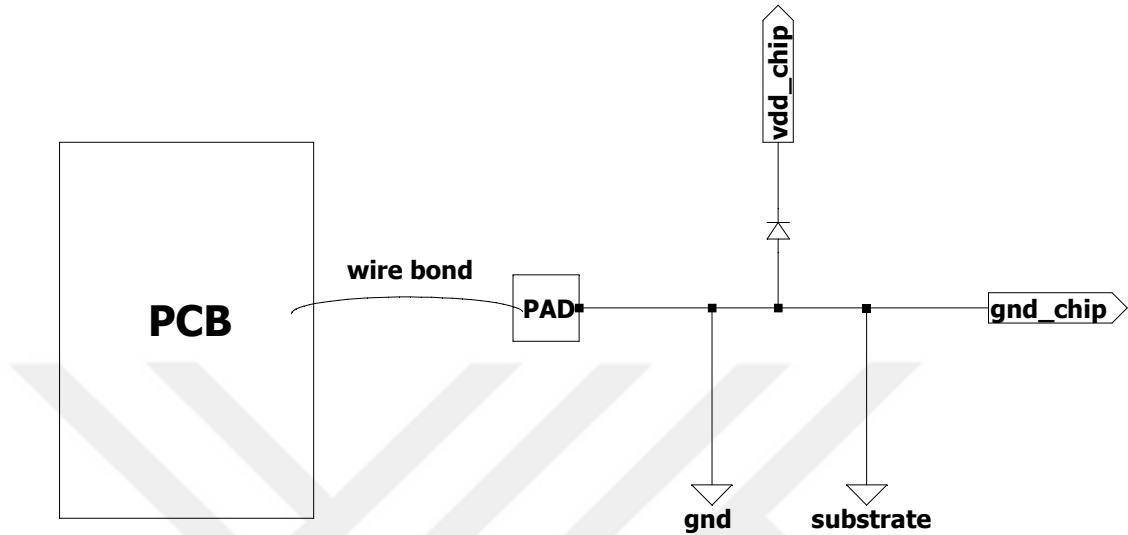


Figure 3.47: GND PAD Schematic

The GND PAD used in this work is chosen from the manufacturer's library of available PADs. Just like other PADs, this PAD also has connections to GND and VDD strips.

The schematic of the signal PAD is given in Figure 3.48. This PAD provides a connection to the inputs and outputs of inner circuits. It has protection diodes from ground and to the supply. Therefore any signal connected to this PAD can not exceed the supply voltage, nor can it take any value lower than the ground voltage level. Since the aim of our design is to generate higher voltages than that of the supply, 5 Volts, the outputs of the charge pumps can not be connected to signal PADs. Only delay capacitor charging signal, clock signals etc can be connected via a signal PAD. Charge pump outputs were connected to VDD PADs since those PADs do not limit the voltage on them. More details are explained below.

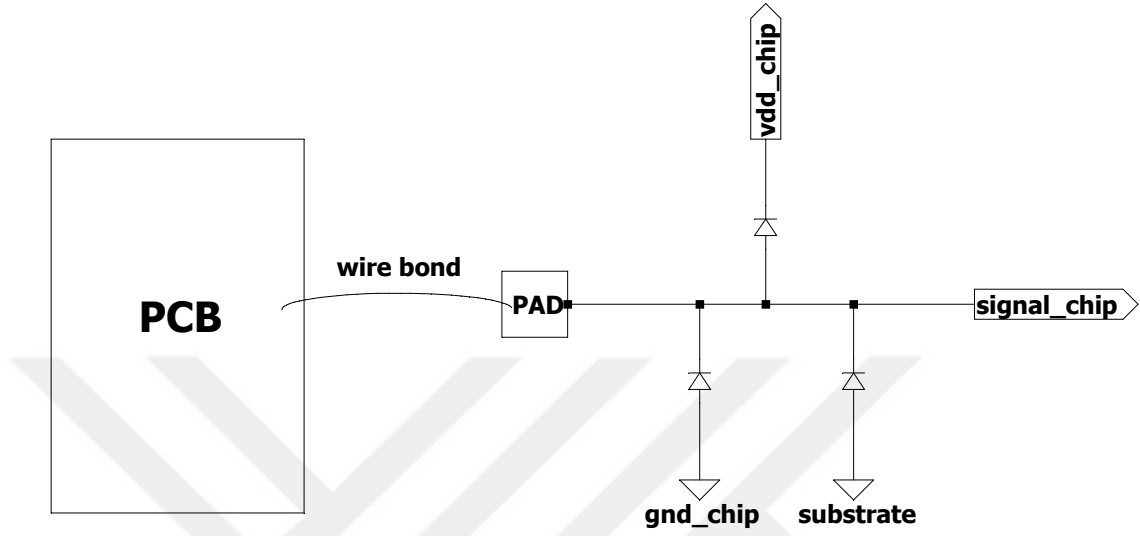


Figure 3.48: Signal PAD Schematic

The signal PAD used in this work is chosen from the manufacturer’s library of available PADs. Just like other PADs, this also has connections to GND and VDD strips. The protection diodes are connected to those strips for VDD and GND referencing.

3.5.2.2 Powercut Selection

It is briefly mentioned above that the charge pump outputs were connected to VDD PADs. This potentially creates another problem while solving the charge pump output access issue. Any PAD placed consecutive to this charge pump output PAD would see the charge pump output as its VDD reference since all the PADs placed next to one another share VDD and GND strips. This is undesired because the circuitry already has a VDD connection for the 5 Volts power supply. Any other VDD PAD would short the charge pump output to the 5 Volts supply.

This problem is solved if this PAD can be separated from the rest of the PADs on the layout. This is achieved in our design by using a structure called ”powercut”. The simplified schematic of the powercut is given in Figure 3.49. It separates the VDD strips of the PADs on its each side so that each side of the

powercut can see a different VDD potential at the power reference strip. Moreover it connects the grounds of both sides with a back-to-back diode configuration thus virtually making sure that these ground potentials can deviate from one another as most as a forward voltage drop of a single diode. Since in this work's design the charge pumps share the same ground as with the rest of the circuitry, an extra ground PAD was placed after each powercut and connected to the same ground nets to ensure the powercut does not cause any voltage difference whatsoever between two sides of itself.

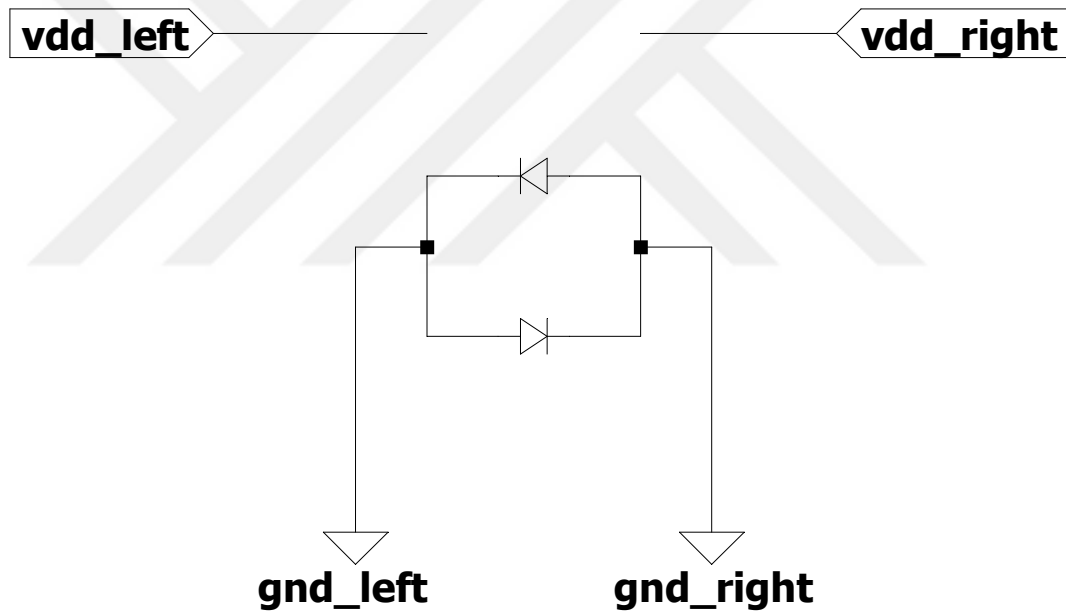


Figure 3.49: Powercut Schematic

There are also different types of powercut structures where they can short the supplies but cut the grounds or cut both ground and supply connections. Using powercuts enables IC designers to connect circuits with different supply voltages or different grounds together on a single line of consecutive PADs.

3.5.2.3 Finalized Layout

Finalized layout of the chip is given in Figure 3.50. The chip contains designs of different designers as well. The chip is a square with 2.5 mm side lengths. It is designed with AMS technologies C35B4C3 libraries and device definitions. This works' circuits are divided into two locations on the chip.

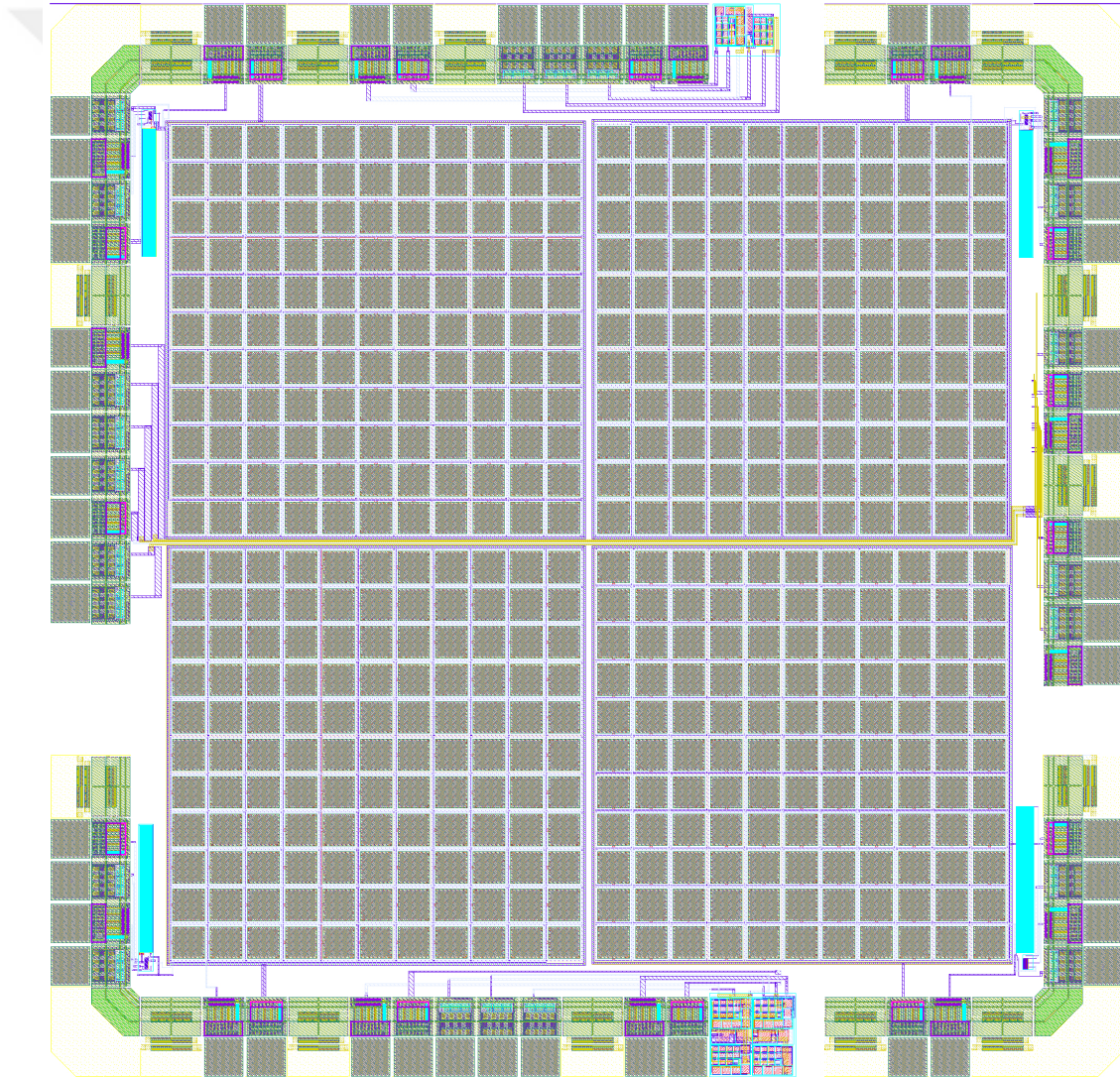


Figure 3.50: Chip Layout

On the top side of the chip there exists one block of our design which contains an 11-stage ring oscillator with buffered and inverted outputs, also a Four Stage

charge pump with capacitive timer delay connection. The layout is shown in Figure 3.51. The PADs are visible on the figure where the left most powercut separates this circuit block from other circuits on the chip. Then the two PADs after the left most powercut are placed one of which is a VDD PAD for charge pump output connection, and the other is a GND PAD for ground connection. Then another powercut separates the expected high charge pump output voltage from the low voltages of the clock outputs and capacitive charging output.

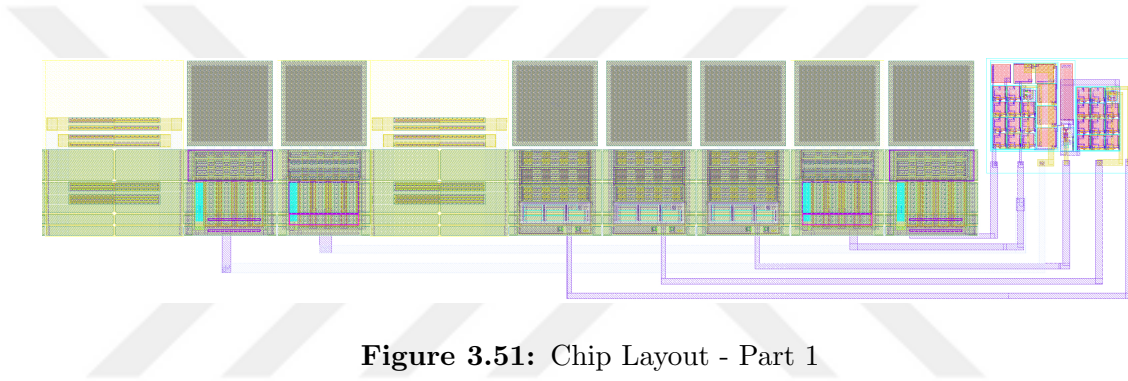


Figure 3.51: Chip Layout - Part 1

The second block of the design is placed on the bottom side of the chip which contains a Three Stage pump output, Four Stage pump output, leakage delayed Four Stage pump output and off-pmos delayed Four Stage pump output. The layout is shown in Figure 3.52. The PADs are visible on the figure where the left most powercut separates this circuit block from other circuits on the chip. Then the five PADs after the left most powercut are placed which are the charge pump outputs and a following GND PAD for ground connection. On this high voltage side of the PADs, the output of the Four Stage pump was connected to a VDD PAD and the rest of the pump outputs are connected to signal PADs since the highest voltage will be the one clamping the rest of the PAD voltages. After the high voltage side, another powercut separates the low voltage side which contains a 5 V supply PAD and a ground PAD.

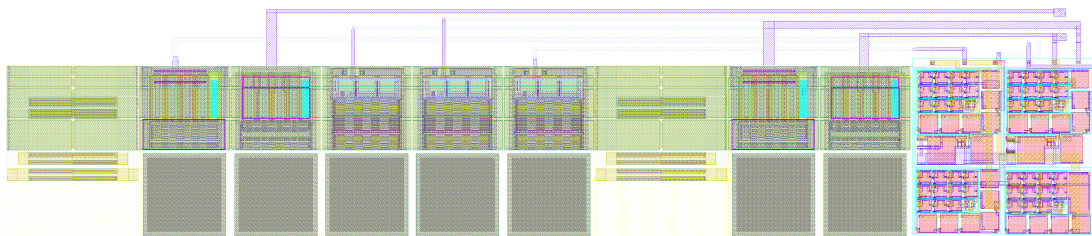


Figure 3.52: Chip Layout - Part 2



Chapter 4

Experimental Results

In this chapter the experimental results are given. These results are interpreted and a future better design is provided.

4.1 Test PCB Design

Testing a chip requires a setup which functions as an interface between the chip and the user. Commercial ICs come in prepackaged form such as SOIC, TSSOP, VSSOP etc. These packages all have a semiconductor IC chip inside which has connections bonded to the package's pins. These pins are large enough so that a designer can handle and solder ICs to boards. Our design was manufactured but was not packaged, therefore bonding the die to a structure was needed. There are standard DIP or SMD packages onto which the dies can be bonded. However in this work bonding the die directly onto a testing PCB with required connections is chosen for simplicity.

Test PCB was designed using Mentor Graphics PADS software. It is a two layered 35 micron copper coated FR4 board with ground layer poured on the bottom layer. Top layer is chosen to hold the chip and required SMD components such as 0603 packaged capacitors. Top layer of the manufactured PCB is shown

in Figure 4.1.

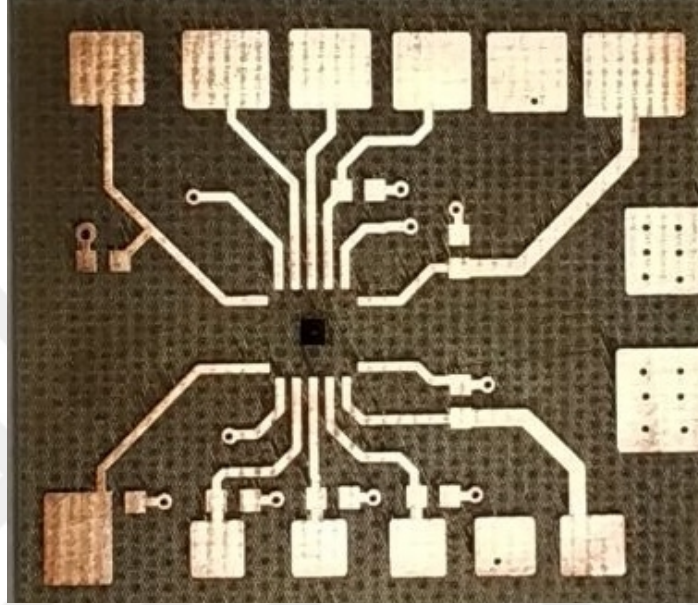


Figure 4.1: Test PCB for Bonding

The chip is glued onto the area on the designated area of the test PCB with epoxy glue. Circuit blocks described in Section 3.5.2 are bonded to the PCB under microscope. It is observed that grinding the surface of the PCB allowed better bonding by removing the oxide layer of the copper. Acetone, alcohol cleaning is also performed to remove any remaining oil or organic residues which might interfere with the bonding process. Final microscope photograph of the bonded chip is shown in Figure 4.2.

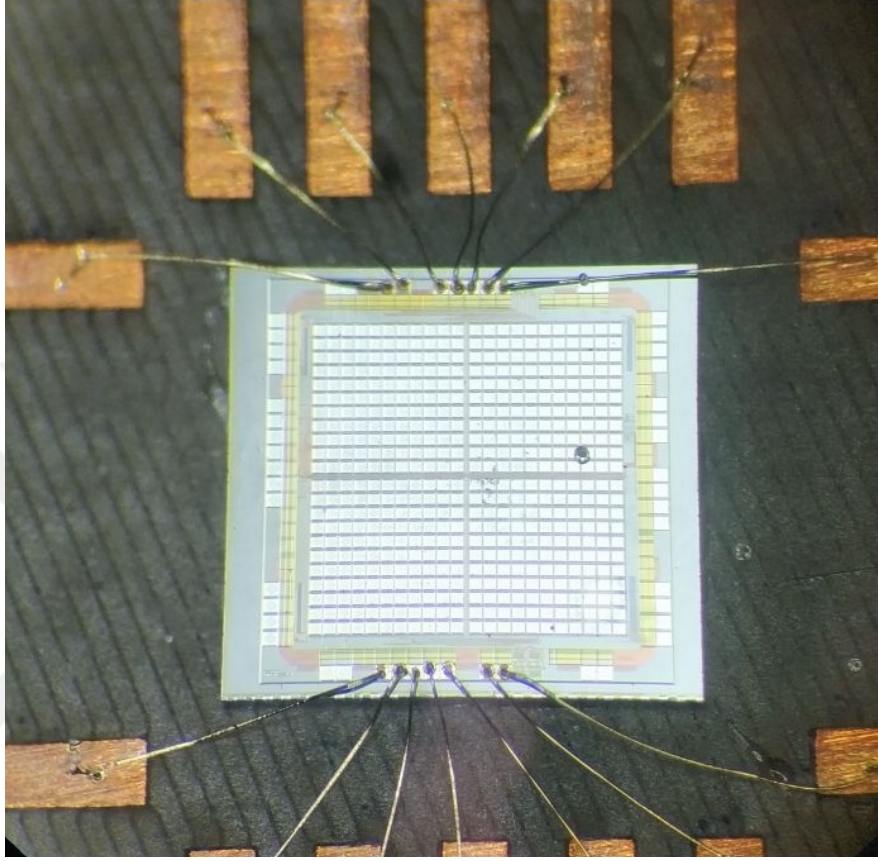


Figure 4.2: Bonded Chip Microscope Photo

4.2 Measurements

4.2.1 11 Stage Ring Oscillator Measurements

11 stage ring oscillator circuit's operation principles and design process was explained in Section 3.4.1. The placement of this circuit block on the final layout was described in Section 3.5.2.3. Although each charge pump block has its own ring oscillator inside, one separate ring oscillator was placed on the chip so it could be measured directly without any charge pump circuitry loading it. Thus a 11 stage ring oscillator is placed on the chip and its two out of phase buffered outputs are connected to signal PADs.

On the test PCB these two clocks are not loaded with any dedicated capacitors, they are just connected to a large copper area for probing. The oscillator is then powered up with 5 Volts supply then its outputs are measured with KEYSIGHT N2843A passive probes and DSOX3054T 500 MHz oscilloscope.

Measurements taken were seen to be triangle signals with some amount of DC offsets instead of the expected square wave signals. The measurement results are shown in Figure 4.3. These measurements suggest that there is oscillation of the desired frequency in the circuit however while routing it to the outside world the signals appear to be distorted.

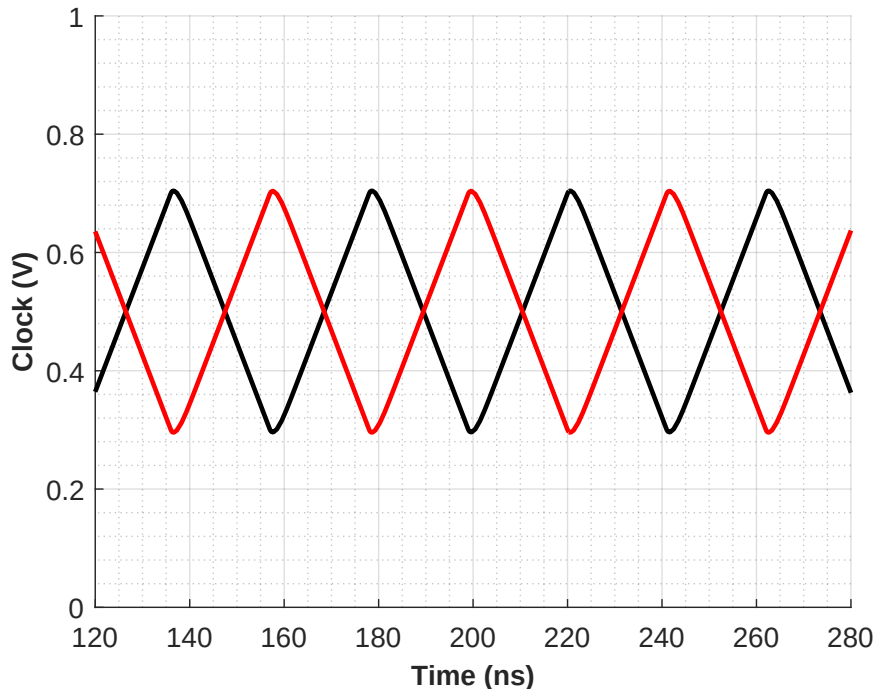


Figure 4.3: Ring Oscillator Measurement Results

More measurements of the clock outputs were performed at different supply voltages and results are shown in Table 4.1. As expected the oscillation frequency increases as the supply voltage increases due to faster charging of gate capacitances of consecutive inverter stages. Moreover the swing magnitudes are also increasing as is expected of an oscillator circuit with larger supply voltages.

Vsupply (V)	Oscillation Frequency (MHz)	Voffset (mV)	Vpp (mV)
3.5	15.7	300	310
4	18.5	368	350
4.5	20.7	438	390
5	22.8	550	450
5.5	24.6	620	470

Table 4.1: 11 Stage Ring Oscillator Measurement Results

In order to understand the cause of this problem the circuit is built on LtSpice and simulated. It is seen that any large capacitive loading at the output of the oscillator buffer disrupts the clock signals and creates similar triangle waves. This is due to the excessing of the output buffer's drive limits. Therefore initially it was theorized that this issue is caused by capacitive loading of the oscillator block. Since the N2843A oscilloscope probes have 11 pF input capacitance, it is possible that by measuring the circuit we are in fact disturbing it at the same time by loading the oscillator with 11 pF of capacitance which is a large capacitance compared to the size of our circuit.

Therefore it was needed to reduce the loading of the measurement probes' effect on the circuit. For this purpose the outputs of the clock signals were buffered with a high frequency bandwidth operational amplifier in a non-inverting topology. The amplifier used is selected as THS3120 from Texas Instruments which has 0.4 pF non-inverting input capacitance according to the datasheet [26]. The op-amp connection is shown in Figure 4.4

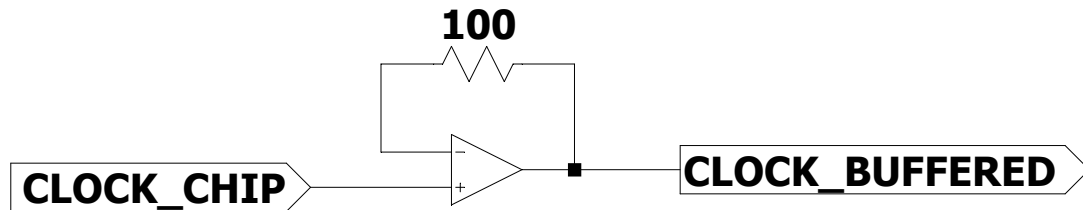


Figure 4.4: Ring Oscillator Buffer Connection

Buffering the clock output with a low capacitance op-amp worked as intended and the buffered clock output was measured to have 700mV offset with 1 Volt

peak to peak deviation at 22.8 MHz under 5 Volts supply. This peak to peak value is double the deviation of the previous measurements done directly by the oscilloscope probe. This observation proved that the ring oscillator's output stage lacked the ability to drive large capacitive loads. Moreover, despite using an external buffer with very low input capacitance, still the desired clock signal with 5 Volts amplitude is not observed. This suggested that there is another source of capacitive loading in between the PCB and the oscillator circuitry. Only structures in between the outside world and the circuit are the signal PADS used for wire bonding.

Layout extraction up to this point was done on the designed circuitry and the PADS were ignored. However these measurement results suggested that the PADS should not be ignored since they might also be disturbing the signals by loading them capacitively. In order to illuminate these suspicions a capacitive parasitic extraction of the PADS are carried out and it is observed that the PADS have around 1 pF capacitance loading the signals. This is enough to disturb the small output buffers of the ring oscillator block.

Realizing that the output buffer of the ring oscillators are too weak to drive almost any parasitic capacitive loads, the output buffer is updated to solve this issue. The original output stage is shown in Figure 3.22. Updated output stage has 10 times wider output MOSFETs to increase its ability to drive higher currents therefore higher capacitive loads as well. The updated layout of the output stage with $60\mu\text{m} \times 14\mu\text{m}$ size is shown in Figure 4.5.

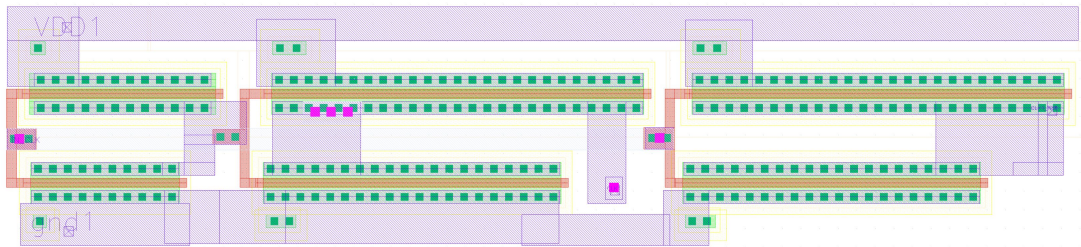


Figure 4.5: Ring Oscillator Updated Output Stage Layout

In order to verify the higher capacitive load ability of this updated circuit,

the layout is simulated using Spectre with 7 pF output capacitors connected to the clock outputs. The resulting waveforms are shown in Figure 4.6. Therefore it is proven that a bigger output buffer would have allowed us to observe the clock signals more correctly and for future works these oscillator buffers should be updated to have larger drivers.

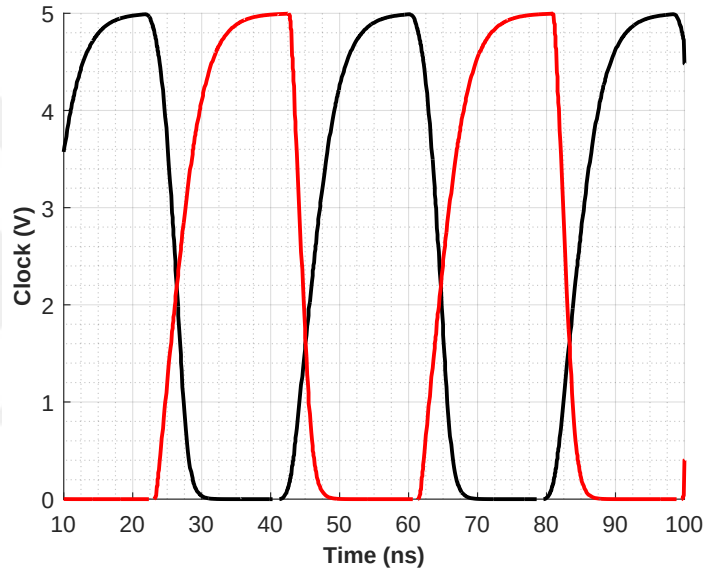


Figure 4.6: Ring Oscillator Updated Output Stage Simulation Result

In conclusion, the ring oscillator measurements has shown that some parasitics of the layout and measurement setup was ignored during the design process which caused high capacitive loading to the clock outputs. This disrupted the signals of interest. Reasons of this situation are explained and a solution design is provided for future works.

4.2.2 Four Stage Charge Pump with Capacitive Delay Measurements

Four Stage charge pump with a capacitive delay circuitry was placed in the same part of the chip with the 11 stage ring oscillator as explained in Section 3.5.2.

Vsupply (V)	VCtimer (V)	Vout (V)
4	4	3.5
5	5	4.5
5.5	5.5	5
6	6	5.42

Table 4.2: Four Stage Charge Pump with Capacitive Delay Measurement Results

of the charge pump still sees some amount of capacitive loading which in return reduces the effective pumping voltage amplitude. Second, the stray capacitances of the charge pump nodes are not small enough to be negligible. Although extracted parameter simulations of these circuits were carried out, still when the pumping capacitors are on the order of 300 fF, any smallest stray parasitics start to affect the pumping capabilities of the charge pump block by reducing the output voltage. Third, since the pump capacitors are not large, the current driving ability of the charge pump is not large either according to the formulations given in Section 3.2. Therefore slight shunt resistances at the output are able to overload the charge pump thus reducing the output voltage.

In fact, to prove this, a 1 M Ω resistor was connected to the output of the charge pump and it was observed that the output voltages did not exceed 200-300 mV levels. Therefore any leakage path in the chip, in the PCB or in the soldered components at the output can act in a way to reduce the output voltage levels. Since these circuits were designed to drive purely capacitive loads, the resistive load driving capabilities of them were overlooked.

Furthermore, the layout's parasitics are extracted again including the parasitic small resistances and small capacitances. The resulting netlist is simulated on Spectre with 5 M Ω output load and 10 pF output capacitances. Ctimer capacitance was not connected in order to reduce simulation duration. Simulation result is given in Figure 4.8. Resulting output voltage is calculated as 6.5 Volts. This level is still slightly larger than that of the measurements given in Table 4.2. However the general trend of the reduced output voltage value is the same therefore it is believed that the suspected reasons are really playing a role in these measurement results.

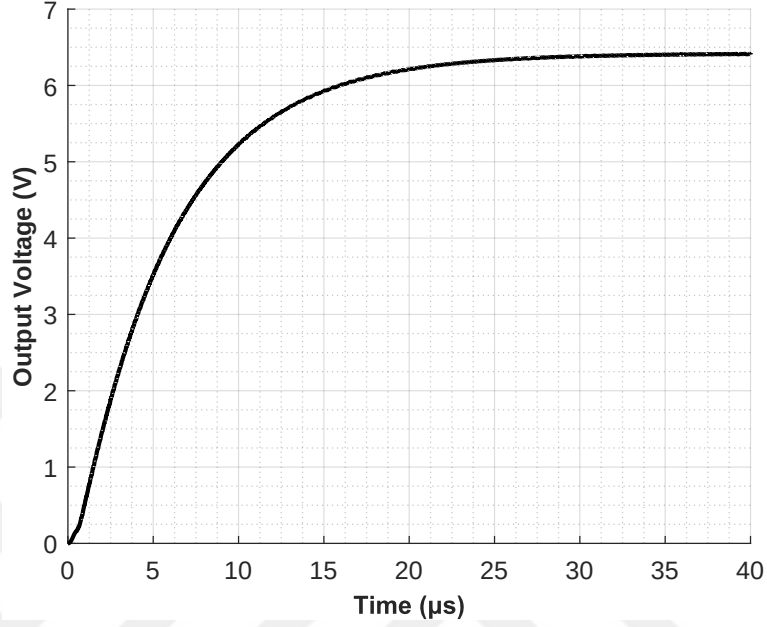


Figure 4.8: Four Stage Charge Pump with Capacitive Delay Post-Layout Simulation

In order to solve the issues regarding the designed circuit, several updates are proposed. First, instead of using 300 fF pump capacitors, larger pump capacitors should be used to reduce the stray capacitance effect and at the same time increasing the resistive load driving capabilities. Second, ring oscillator output which drives the pump stages should have larger buffer MOSFETs so that the clock voltages will be able to swing the whole supply range easily.

These proposed updates are implemented on the respective circuit blocks. Ring oscillator circuit is updated to the one which is proposed on Section 4.2.1. The pump stage's pump capacitance is increased to 5 pF which should be enough to counteract the effects of the stray capacitances. Of course this update comes at the cost of increased area. The finalized layout of a single charge pump stage is $80\text{ }\mu\text{m} \times 83\text{ }\mu\text{m}$.

A Four Stage charge pump layout is designed with the updated larger pump capacitors and clock buffer output. The new layout size is $250\text{ }\mu\text{m} \times 160\text{ }\mu\text{m}$.

Updated circuit is simulated including the stray capacitances and a 5 M Ω output resistor connected. The simulation result is shown in Figure 4.9. As

expected, the output voltage is almost doubled compared to the previous design. Therefore it is proven that if there is a need for more output drive capability and less sensitivity to unexpected parasitics, it is better to have larger clock drivers and pump capacitors.

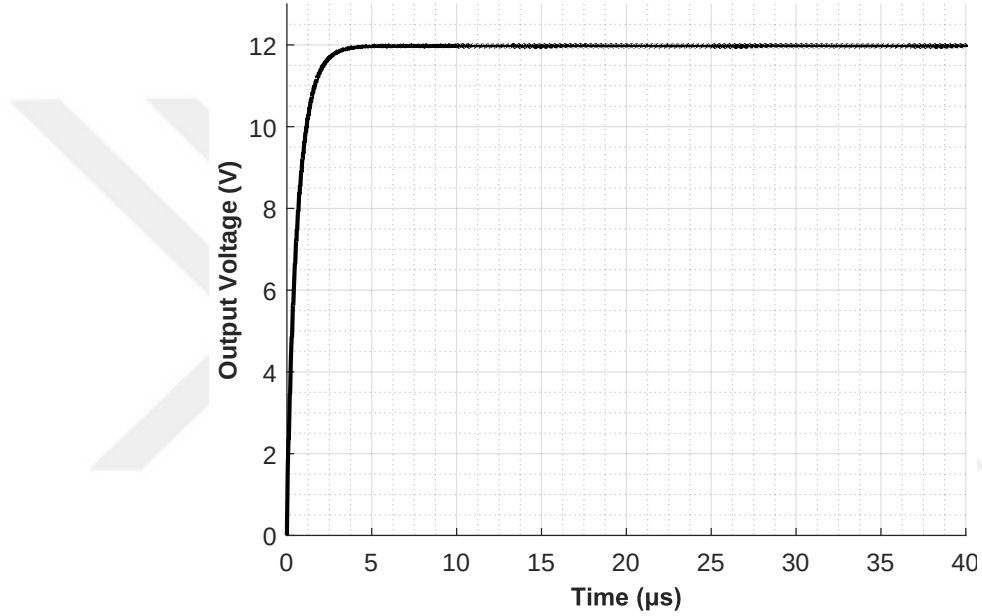


Figure 4.9: Updated Four Stage Charge Pump with Capacitive Delay Post-Layout Simulation

In conclusion, the Four Stage charge pump circuitry did not function as expected after testing the bonded chip. The reasons for the decreased performance were investigated and explained. An updated design is proposed and implemented on software. Simulated updated design showed good performance despite parasitics and good output drive capability compared to the previous design. In a future work, the steps laid out here can be followed to design an optimum charge pump for a given task.

4.2.3 Leakage Delay, Off PMOS Delay, Three Stage Pump, Four Stage Pump Measurements

In this section the measurement results of the second circuit block which consists of 4 different charge pumps are provided. The results of these circuits are given together since they are in the same collection of circuitry, they share their supply and ground and also their PADs are placed side by side.

Each four of the outputs are connected to 10 nF output capacitors. As it was described in the Section 3.5.2 the Four Stage Pump output is connected to a VDD PAD to provide the highest voltage on the block. PADs connected to this VDD PAD are the outputs of the remaining three pump circuits. Powercut structure is used to separate the signals with different expected voltage levels.

When the circuit is powered, it was observed that the output voltages of each pump stage had been clamped at around 0.7 Volts. Upon investigating the reason for this, it was realized that the output of the Four Stage pump was clamping other pump outputs to ground potential. This was unexpected since initially, during the design process, it was assumed that the Four Stage pump would achieve a higher output level than other pumps thus it would not clamp them. Each of the other pump outputs are connected to the output of the Four Stage pump through a diode as it was explained in the Section 3.5.2.

The design was depending on the assumption that the Four Stage pump would achieve the higher expected voltage potential before the other stages reached the same level. Yet the measurements showed this assumption to be false. Therefore in order to bias the VDD connections of the pump circuits, the Four Stage pump output was biased from outside the chip directly thus providing a high potential reference to the protection diodes inside other pump circuits. Measurement results are summarized in Table 4.3.

These measurements come with several important observations. First of all, none of the voltages in any case has exceeded the bias voltage which is expected. Furthermore, Three Stage Pump output voltage appears to be not affected by the

VDD (V)	Vbias (V)	Leakage Delay Circuit Output (V)	Off PMOS Delay Circuit Output (V)	Three Stage Pump Output (V)
3	3	1.10	2.15	1.72
3	6	2.32	2.20	1.85
4	4	1.33	2.96	1.80
5	5	1.60	3.62	2.11
5	5.5	1.60	3.62	2.11
6	6	1.85	4.23	2.53

Table 4.3: Charge Pump Circuits Output Measurements vs VDD & Vbias

bias voltage as long as the bias voltage is not clamping its output. General trend of increasing output voltage as the supply voltage increases is observed which is expected.

Off PMOS Delay circuit's output measurements suggest that the intended effect of voltage reduction due to delay control block triggering did not take place since the off pmos delay circuit's output voltages were measured to be larger than the Three Stage pump's output. If in fact the delay circuitry was triggered, then the off pmos delay circuit would have become a Three Stage pump thus having a similar output voltage as a regular Three Stage pump circuit.

Using the same reasoning, it is observed that the leakage delay circuitry was in some cases triggered for the leakage delay block thus providing a lower voltage than the off PMOS delay circuit. However in the measurement with 6 Volts bias and 3 Volts supply, the leakage delay circuitry appears to be not triggered since it gives almost the same voltage as the off PMOS delay circuit. However the overall observations suggest that the leakage based delay circuitry does not function as intended and gives out exceptionally low output voltages. This might be due to the unpredictable nature of the surface leakage currents present at the chip. The delay timing circuitry works by using a MOSFET as a switch to turn off one stage of the cascaded pumps. The leakage based circuitry might have settled at an operation point where the control MOSFETs are biased on saturation region instead of the desired triode region thus giving out peculiar results.

The small voltage levels in general can be explained as in the case of the previous section, due to parasitics, leakage paths and insufficient drive capabilities of ring oscillators. Thus, in conclusion, designed pump circuits in this work

rendered to be insufficient by the parasitics and loading effects. Therefore better and improved designs are proposed with larger pump capacitors and buffers. Moreover, it is observed that using the output voltage of a charge pump to provide VDD reference to outputs of other circuits is not usable. Instead, each charge pump's output should be separated from one another with either empty distance or powercut structures.

4.3 Layout Design Results and Notes for Future Studies

It is explained in the previous sections that layout design is of utmost importance in designing a functioning charge pump. It was observed that the designed pump circuits in this work measured to be giving output voltages less than the desired values. Solutions to this issue were proposed and improved designs were simulated and provided.

Apart from the layouts of the circuit blocks, also the layouts of the PADs are observed to be important. As it was seen in Section 3.5.2, each PAD has protection diodes to supply and from ground. Any voltage level on a PAD appears as a reverse voltage on these diodes. Especially in future works, after implementing the proposed updates, the output voltage levels of 12-15 Volts will appear on these diodes. Assuming that the same VDD PAD is used for routing these voltage outputs to the outside world, the diodes on the VDD PADs should have breakdown voltages significantly larger than the expected maximum output voltage.

Diode types and breakdown voltage levels are always provided by the chip manufacturer's design manuals. It is important to give extra attention to the parasitic diodes resulting from the junctions between differently doped regions and different MOSFET bodies.

Moreover, apart from the diodes, also the pump capacitors should be chosen to have a structure capable of not breaking down under the maximum output voltage

level. Initial stages of the charge pump topology would have less stress than the later stages. Therefore different types of capacitors could be used at different stages depending on their capacitance per unit area and breakdown voltages in order to optimize the layout area.

Furthermore, using larger pump capacitors as proposed by the results of this work's measurements would result in larger capacitive loading for the ring oscillator block. Thus it should not be overlooked that the output buffer of the ring oscillator should be able to drive the needed pump capacitances.

The design principle of safety margin should be implemented where the stray capacitances may be taken into account as at least 2-3 times the extracted values and leakage paths could be employed on the simulations. Sufficient safety margins would reduce the chances of a dysfunctioning chip. Drive capabilities should be designed as powerful as to drive 2-3 times heavier loads than expected.

Chapter 5

Conclusion

In this work the design steps of several variations of Dickson Charge Pump topology is explained in detail. Required circuit blocks are described and the designed circuits are provided. Each block is simulated before the layout, and also post-layout simulations are performed and provided in order to include parasitic effects.

Designed circuits can be divided into three types. First, ring oscillators are designed to provide two 180 degrees out of phase clock signals to each charge pump circuit in order to pump the charges towards the output. 11 stage ring oscillator are designed and the output signal is buffered through inverters to achieve two out of phase clocks. Oscillation frequencies around 25 MHz are aimed.

Second, Dickson pump stages are designed with 300 fF pump capacitors where the input stage is connected to the ground and switching elements are realized using diode connected PMOS transistors. Ring oscillators are connected to each designed charge pump to drive the pumping stages.

Third, a circuit block is designed which is capable of switching off the first stage of a Dickson pump strip. This is planned to be used for reducing the output voltage after a certain amount of time which is the desired bias voltage for this work's intended capacitive loads.

These main blocks are collected together to create several different circuit blocks. Simple three-four staged charge pump circuits are designed, furthermore 3 different types of delayed Four Stage pumps are designed. All these circuits are analyzed using Spice simulation tools. Layouts of these circuits are designed for 350 nm CMOS process and the resulting layouts are also simulated using extracted parasitics in order to ensure correct circuit operation. Approaches for layout design process are also provided.

Designed chip is manufactured then bonded on a test PCB in order to verify the circuit blocks on the chip. Results are provided and explained. It is observed that some parasitic effects are overlooked during the design process which caused diminished performance of the chip. Capacitive parasitics disrupted the signals of ring oscillator outputs and reduced the output voltages of the charge pump stages. Resistive parasitics also caused a reduction in the output voltages as well. From these observations several updated designs are proposed and they are verified using simulations.

These updates are strengthening the drive capabilities of the ring oscillators as well as charge pumps by reducing the circuits' sensitivity to parasitics. Of course this comes at the cost of increased chip area which is the main trade-off for increased load capabilities.

In conclusion, updates and design guidelines for future works are presented. These proposed updates are supported with simulations and layouts of several updated blocks are shown. This work lays the ground for future, more successful, higher load capable charge pump circuits for driving not only capacitive loads but also resistive loads.

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