A TRANSIMPEDANCE AMPLIFIER FOR CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR
THE DEGREE OF
MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

By
Yavuz KANSU
December, 2015

A TRANSIMPEDANCE AMPLIFIER FOR CAPACITIVE MICRO-MACHINED ULTRASONIC TRANSDUCERS
By Yavuz KANSU
December, 2015

We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Abdullah ATALAR(Advisor)

Prof. Dr. Hayrettin KÖYMEN

Assoc. Prof. Dr. Arif Sanlı ERGÜN

Approved for the Graduate School of Engineering and Science:

Prof. Dr. Levent Onural
Director of the Graduate School

ABSTRACT

A TRANSIMPEDANCE AMPLIFIER FOR CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS

Yavuz KANSU
M.S. in Electrical and Electronics Engineering
Advisor: Prof. Dr. Abdullah ATALAR
December, 2015

In this thesis a design of a CMOS transimpedance amplifier (TIA) for a capacitive micro-machined ultrasonic transducer (CMUT) is presented. CMUT's have a high electrical impedance when used as receivers. Any capacitance between the CMUT and a high impedance amplifier will degrade the frequency response. So, we need to amplify the current rather than the voltage. This approach requires a transimpedance amplifier.

The designed TIA has a 30 MHz bandwidth and 400 kΩ transimpedance gain. The total input referred current noise of the TIA is 270 fA/$\sqrt{\text{Hz}}$ at 10 MHz. The noise figure of the TIA is 2.7 dB at 10 MHz when connected to the CMUT with 200 kΩ source resistance. The power consumption of the TIA is 10.5 mW and the size of the TIA layout is 133μm x 45μm. The TIA chip will be fabricated in AMS C35B4C3 (0.35μm) process.

Keywords: CMUT, TIA, Transimpedance Amplifier, CMUT Receiver.

ÖZET

KAPASİTİF MİKROİŞLENMİŞ ULTRASONİK ÇEVİRİCİLER İÇİN TRANSEMPEDANS YÜKSELTECİ

Yavuz KANSU
Elektrik ve Elektronik Mühendisliği, Yüksek Lisans
Tez Danışmanı: Prof. Dr. Abdullah ATALAR
Aralık, 2015

Bu tezde kapasitif mikroişlenmiş ultrasonik çeviriciler (CMUT) için transempedans yükselteçi (TIA) tasarımı anlatılmaktadır. CMUT'lar almaç olarak kullanıldıklarında elektriksel olarak yüksek empedansa sahiptirler. CMUT ile yüksek empedanslı yükselteç arasındaki herhangi bir kapasitans, CMUT'ın frekans cevabını kötüleştirir. Bu nedenle CMUT'ın çıkış voltajı yerine CMUT'ın çıkış akımı yükseltilmelidir. Bu yöntem transempedans yükselteci kullanımını gerektirir.

Tasarlanmış olan TIA 30 MHz bantgenişliğine ve 400 kΩ transempedans kazancına sahiptir. TIA'nın 10 MHz'deki giriş akım gürültüsü 270 fA/$\sqrt{\text{Hz}}$'dir. TIA'ya, kaynak direnci 200 kΩ olan bir CMUT bağlandığında 10 MHz'deki gürültü işareti (NF) 2.7 dB olmaktadır. TIA'nın güç tüketimi 10.5 mW ve serim ölçüleri 133μm x 45μm'dir. Tasarlanan TIA çipi AMS C35B4C3 (0.35μm) prosesi ile üretilecektir.

Anahtar sözcükler: CMUT, TIA, Transimpedans.

Acknowledgement

I am deeply grateful to my supervisor Prof. Dr. Abdullah Atalar for his support and guidance through the advancement of this thesis.

I would like to express my gratitude to Prof. Dr. Hayrettin Köymen for giving me the chance to work in CMUT research group. I would also like to thank to Professor Hayrettin Köymen and Assoc. Prof. Dr. Arif Sanlı Ergün for reviewing and evaluating my thesis.

I am also thankful to my friends and colleagues; Yasin, Parisa, Mansoor, Elif, Aslı, Kağan and Oğuzhan. Additionally, special thanks to Burak Şahinbaş and Mehmet Zafer Akgül for editing my thesis.

I acknowledge that the financial support I received from TÜBİTAK BİDEB 2210 Program. Also, this work is carried out using the simulation infrastructure provided by the 213E031 project (TÜBİTAK).

Lastly, I would like to thank my father Hüseyin and my mother Zeyniye for their endless support and love.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Capacitive Micromachined Ultrasonic Transducer (CMUT) is a device which converts electrical signals to ultrasound signals as a transmitter and converts ultrasound signals to electrical signals as a receiver [2]. CMUT can be described as a parallel plate capacitor in which one of the plates is moveable and interfaces with the medium while the other one is fixed.

To operate the CMUT as a transmitter, an AC signal on top of a DC bias voltage should be applied, then the changing electrical field between the plates moves the front plate and generates the ultrasound signals. In order to operate CMUT as a receiver, DC bias voltage should be applied to the plates. When the ultrasound signals vibrate the front plate of the CMUT, its capacitance will change and a current will be generated.

To measure the generated current signal from the CMUT receiver, a transimpedance amplifier (TIA) is used. A TIA converts an input current to a voltage output. Since TIA's input impedance is very low, they are used as a pre-amplifier for high impedance sensors like photo diodes [3], MEMS accelerometers [4] and CMUT's [5].

CMUTs are fabricated with MEMS process given in [6]. Many CMUT cells can be fabricated on a single die to form a 2-dimensional array [7]. CMUTs have been

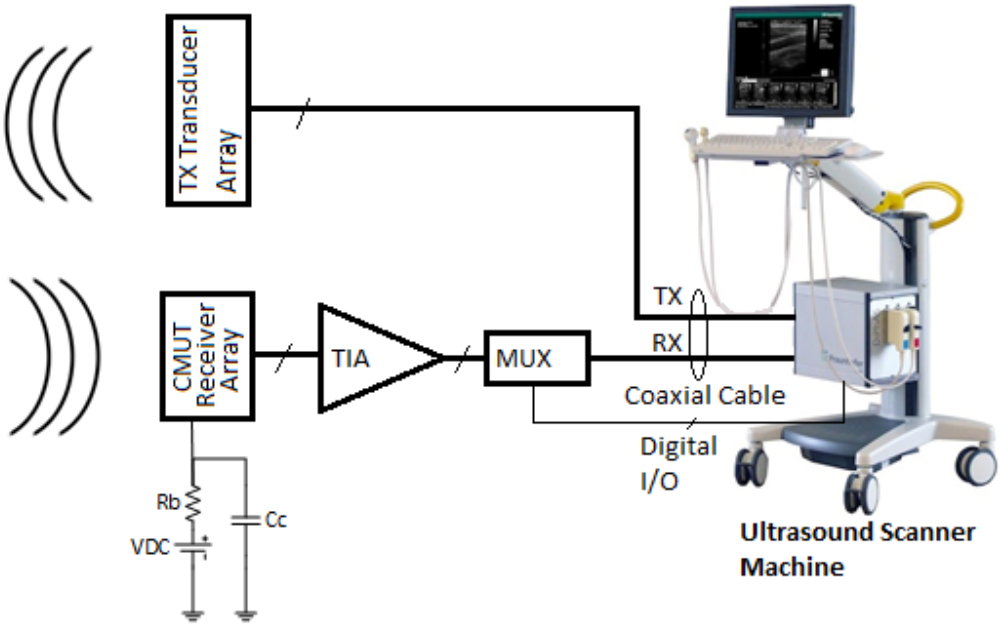

Figure 1.1: Block diagram of the ultrasound imaging system

found very attractive in medical imaging applications because of design flexibility and the ease of fabricating large arrays [8, 9]. For medical ultrasound imaging, the CMUT receiver array is connected to the ultrasound scanner machine through the TIA shown in Fig. (1.1). Since the impedance of the CMUT receiver is very high, the TIA should be placed near the CMUT array as close as possible [10]. A CMUT array with thousands of elements is needed for better image resolution [11]. In contrast, the state of the art ultrasound scanners have up to 256 receiving channels [12, 13]. As a solution, the CMUT array with thousands of elements can be connected to the scanner by multiplexing the TIA outputs.

As a CMUT pre-amplifier, a TIA should not degrade the performance of the sensor. Design of a wide bandwidth, a high gain and a low input referred noise TIA for a CMUT is presented.

Chapter 2

Transimpedance Amplifier

CMUT receivers produce current output when the acoustic waves hit the CMUT's plate. If the acoustic waves are small in amplitude, the output of the receiver becomes very weak. So, the generated current from the CMUT receiver should be amplified. For signal processing, analog signals should be converted to digital signals and this is done by analog to digital converters (ADC). Since most of the ADCs convert voltage signals [14], CMUT current signals must be converted to voltage signals. Hence, a transimpedance amplifier (TIA) is needed to make this conversion.

There are three important parameters for TIA design; transimpedance gain, bandwidth and input-referred current noise. The transimpedance gain is a ratio between the TIA output voltage to the TIA input current which is given as $R_T = \partial V_{out}/\partial I_{in}$. So, it determines how much output voltage for a given current is produced. For example, if the CMUT output is 1 mA and transimpedance gain is 1 kΩ then TIA output voltage will be 1 V.

The input-referred noise is a fictional parameter which is used for the comparison of the TIAs independent from their transimpedance gain. The input-referred current noise can be calculated by dividing the output voltage noise to the transimpedance and its unit is A/$\sqrt{\text{Hz}}$. It determines the minimum detectable current

of the TIA. Also, the input-referred current noise of the TIA can be used in the noise figure (NF) calculations as given Eq. (2.1)

$$\mathrm{dB}(NF) = \mathrm{dB}\left(\frac{\overline{I_{n,op}^2} + \overline{I_{n,cmut}^2}}{\overline{I_{n,cmut}^2}}\right) \Bigg| 290^{\circ}\mathrm{K} \tag{2.1}$$

where $\overline{I_{n,op}}$ is the input-referred current noise of the TIA and $\overline{I_{n,cmut}}$ is the CMUT current noise. NF is difference between signal to noise ratio (SNR) at the input and signal to noise ratio (SNR) at the output at 290° K. For low noise applications, NF should be lower than 3 dB. So, the input-referred current noise of the TIA should be lower than the CMUT current noise. For example, the CMUT cells in the 2D array have 200 kΩ resistance (R_{cmut}) and 100 fF capacitance (C_{cmut}) at the resonance. The CMUT current noise is

$$\overline{I_{n,cmut}} = \sqrt{\frac{4kT}{R_{cmut}}} \approx 0.3 \text{ pA}/\sqrt{\text{Hz}} \Bigg| 290^{\circ}\mathrm{K} \tag{2.2}$$

where k is the Boltzmann constant and T is the ambient temperature in Kelvin. As a result, $\overline{I_{n,op}}$ should be lower than 0.3 pA/$\sqrt{\text{Hz}}$.

Bandwidth (BW) is the operating frequency range of the amplifier. The TIA bandwidth should be wide enough such that information in the analog signal can be amplified without loss. So, TIA shouldn't limit the CMUT receiver BW. Since the CMUT cells in the 2D array have more than 30 MHz bandwidth, TIA is designed for a minimum of 30 MHz bandwidth.

To explore the benefits of different approaches, three types of TIA topologies are analysed; Resistive Termination, Common Gate Amplifier and Resistive Feedback Amplifier. Resistive termination and Common Gate Amplifier is analysed briefly because they are not good for low noise applications [15]. However, the resistive feedback amplifier as a CMUT front-end receiver has been reported in various papers [10, 16, 17, 18].

2.1 Resistive Termination

Probably the simplest approach for converting the CMUT output current to a voltage signal is to terminate the CMUT with a shunt load resistor R_L as given in Eq. (2.1). The bandwidth of the circuit can be calculated as

$$f_{3dB} = \frac{1}{2\pi(R_{cmut} \mid\mid R_L)(C_{cmut} + C_L)} \tag{2.3}$$

where C_L is a load capacitance which can be a parasitic capacitance or an input capacitance of the following stage. If the CMUT connected to a high input impedance voltage amplifier with $R_L \gg R_{cmut}$ and $C_L \gg C_{cmut}$ then Eq. (2.3) becomes

$$f_{3dB} = \frac{1}{2\pi R_{cmut} C_L}. \tag{2.4}$$

If $R_{cmut} = 200$ kΩ, $C_{cmut} = 100$ fF and $C_{amp} = 2$ pF, then the bandwidth is 380 kHz which is much lower than required 30 MHz bandwidth. As we can see, the bandwidth is limited because of R_{cmut} and C_L.

The noise figure NF of the circuit is

$$NF = \text{dB}\left(\frac{\overline{I^2_{n,cmut}} + \overline{I^2_{n,L}}}{\overline{I^2_{n,cmut}}}\right) = \text{dB}\left(1 + \frac{R_{cmut}}{R_L}\right). \tag{2.5}$$

From Eq. (2.3) and Eq. (2.5), both BW and NF are inversely proportional to R_L. As R_L increases, BW and NF drop, hence for high impedance sensors like small CMUTs, a wide band and low noise amplification is not simultaneously possible with resistive termination.

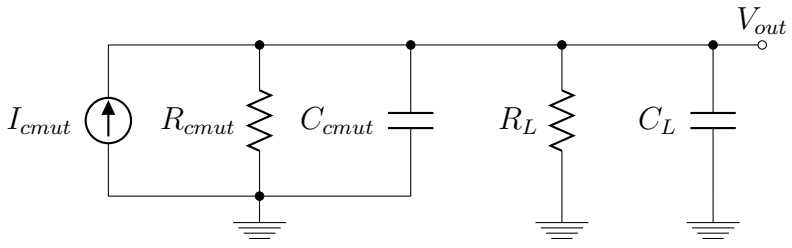

Figure 2.1: Resistive Termination

2.2 Common Gate Amplifier

Common gate amplifier (CGA) is an amplifier with a low input impedance which buffers the input current. It is generally used with large area photo-diodes to short out the photo-diode's large capacitance [15]. In this work, CMUT cells will be integrated to the front-end electronics via wire bonding technique. So, there will be a significant parasitic capacitance between the CMUT and the amplifier [19]. Since CGA input impedance is much lower than that of CMUTs, CMUTs receiving performance and bandwidth will not be effected by the parasitic capacitance.

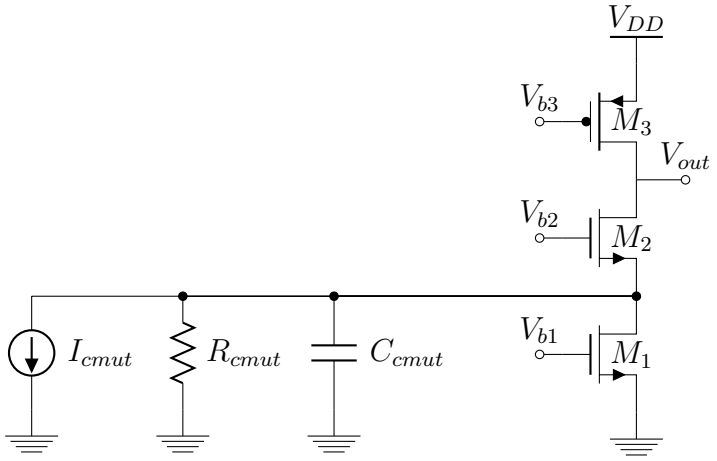

Figure 2.2: Common Gate Amplifier

The CGA given in Fig. (2.2) is designed with NMOS and PMOS current sources to achieve a higher gain and a low input impedance. M_1 is the NMOS current source and M_3 is the PMOS current source. M_2 is the NMOS common gate amplifier stage. V_{b1}, V_{b2} and V_{b3} are the bias voltages of the transistors. The detailed analysis of the CGA can be found in [15]. The transimpedance gain of CGA is given by:

$$R_T = \frac{r_{o1} r_{o3}((g_{m2} + g_{mb2}) r_{o2} + 1)}{r_{o1} + r_{o2} + r_{o3} + (g_{m2} + g_{mb2}) r_{o1} r_{o2}} \tag{2.6}$$

where g_{mi} is the transconductance of the transistor M_i, g_{mbi} is the body transconductance of the transistor M_i and r_{oi} is the output resistance of the transistor

M_i. It is reasonable to assume that $(g_{m2}+g_{mb2})r_{o2} \gg 1$ and $(g_{m2}+g_{mb2})r_{o2}r_{o1} \gg r_{o1}+r_{o2}+r_{o3}$. Thus,

$$R_T \approx r_{o3} \approx \frac{1}{\lambda I_D}. \tag{2.7}$$

The input impedance of the CGA is given:

$$R_{in} \approx \frac{1}{g_{m2}+g_{mb2}}. \tag{2.8}$$

$(g_{m2}+g_{mb2})$ can be as high as 20 mS. Thus, R_{in} can be 50 Ω.

The bandwidth of the CGA for a large input capacitance given as:

$$f_{3dB} = \frac{1}{2\pi(R_{cmut} \mid\mid R_{in})(C_{cmut}+C_{par})} \tag{2.9}$$

where C_{par} is the parasitic capacitance due to the interconnection between the CGA and CMUT. Generally C_{par} is on the order of 1 pF when wire bonding technique is used and it is larger than C_{cmut}. Also, R_{in} is much lower than R_{cmut}. Thus,

$$f_{3dB} = \frac{g_{m2}+g_{mb2}}{2\pi C_{par}}. \tag{2.10}$$

The input referred current noise of the CGA is given

$$\overline{I_{n,op}^2} = 4kT\gamma(g_{m1}+g_{m3}) \tag{2.11}$$

where γ is the MOS transistor noise coefficient. The transconductance of a transistor at saturation can be calculated as

$$g_m = \frac{2I_D}{|V_{GS}-V_{TH}|} = \frac{2I_D}{V_{OD}}, \tag{2.12}$$

where V_{GS} is the transistor gate to source voltage, V_{TH} is the transistor threshold voltage and V_{OD} is the transistor over drive voltage. Thus,

$$\overline{I_{n,op}^2} = \frac{8\gamma I_D kT}{V_{OD1}} + \frac{8\gamma I_D kT}{V_{OD3}}. \tag{2.13}$$

For a lower input current noise, V_{OD} of transistor should be increased or I_D should be decreased. V_{OD} can not be increased independently because transistors are in saturation region when $|V_{DS}| > V_{OD}$. Also, the sum of the over drive voltages of the transistors must be lower than the supply voltage (V_{DD}) as given

$$V_{OD1}+V_{OD2}+V_{OD3} < V_{DD}. \tag{2.14}$$

Additionally, the bias current I_D can not be decreased because this will limit the dynamic range of the CGA. Thus, $\overline{I_{n,op}^2}$ must be minimized according to Eq. (2.14). This limitation makes a low noise design impossible with a low supply voltage [15].

2.3 Resistive Feedback Transimpedance Amplifier

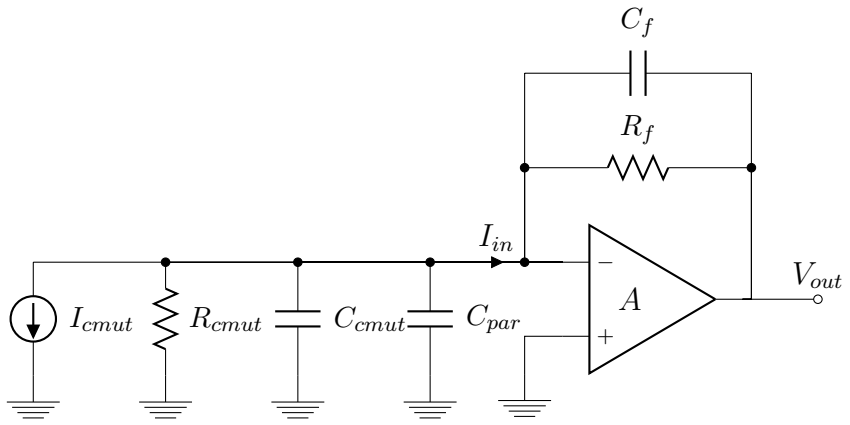

Figure 2.3: Resistive Feedback Transimpedance Amplifier

Resistive feedback TIA shown in Fig. (2.3) is commonly used in optoelectronics. The inverting amplifier senses its input and gives a proportional current over feedback resistor back to the input. Because of the Miller effect, input impedance of the amplifier is equal to the feedback resistor R_f divided by the amplifier open loop gain A_0, providing us with a low input impedance. As described by B.Razavi [15], the resistive feedback amplifier can be treated as a second order system. If $C_f = 0$ then transfer function of the amplifier is given by:

$$\frac{V_{out}}{I_{cmut}} = -\frac{\dfrac{A_0\omega_0}{C_{tot}}}{s^2 + \dfrac{R_f C_{tot} + 1/\omega_0}{R_f C_{tot}} s + \dfrac{(A_0+1)\omega_0}{R_f C_{tot}}}, \tag{2.15}$$

where C_{tot} is the total capacitance at the input of the amplifier and ω_0 is the open loop voltage gain corner frequency. Eq. (2.15) gives the transimpedance

gain of the topology and when $s = 0$ and $A_0 \gg 1$, it approaches R_f. In order to get a high transimpedance gain, the feedback resistor should be large. The denominator of the transfer function can be written as $s^2 + 2\zeta\omega_n + \omega_n^2$, where ω_n is the closed loop corner frequency and ζ is the damping factor. To get a well-behaving step response and a maximally flat frequency response, the damping factor of the system should be equal to $\sqrt{2}/2$. When the system of equations are solved, there appears a relation between ω_0 and ω_n which is given by:

$$\omega_0 = \sqrt{2}\omega_n \tag{2.16}$$

$$\omega_n \approx \frac{\sqrt{2}A_0}{R_f C_{tot}} \tag{2.17}$$

$$GBW = \frac{\omega_0 A_0}{2\pi} = \frac{\omega_n^2 R_f C_{tot}}{2\pi} \tag{2.18}$$

As seen in the Eq. (2.17), -3 dB bandwidth is improved by $\sqrt{2}A_0$ relative to the resistive termination. In our implementation, -3 dB bandwidth should be higher than 42 MHz and the voltage gain should be higher than two. Since the voltage gain of the amplifier is equal to $\frac{Rf}{R_{cmut}}$, we choose $R_f = 400$ kΩ. If we assume that the input capacitance of the amplifier is equal to 1.5 pF, then the core amplifier should have more than 42.4 MHz bandwidth and 22 dB open loop gain. So, the core amplifier should have more than 5.4 GHz gain bandwidth product (GBW). From the Eq. (2.18), if we increase the total input capacitance or the feedback resistor, we will need more gain bandwidth product for the same closed loop bandwidth. If C_f is not equal to zero than TIA BW becomes

$$\omega_n = \frac{1}{R_f C_f} \tag{2.19}$$

[20]. For a 30 MHz bandwidth and a 400 kΩ gain, C_f should be 13 fF.

Since the CMUT receiver generates a current output, the TIA input-refered current noise density is an important criterion for the noise analysis. The input current noise of the amplifier is analysed in [17] and it is given by:

$$\overline{I_{n,op}^2} = \omega^2 C_{tot}^2 \overline{V_{n,op}^2} + \frac{\overline{V_{n,op}^2}}{(R_{cmut} \mid\mid R_f)^2} + \frac{4kT}{R_f}, \tag{2.20}$$

where $\overline{V_{n,op}^2}$ is the input voltage noise of the core amplifier. As seen in Eq. (2.20), the dominant noise source is the feedback resistor at lower frequencies. However,

the core amplifier noise contribution becomes significant at higher frequencies because of the capacitances. To obtain a lower input current noise, the feedback resistor can be increased. On the other hand, increasing the feedback resistor may decrease the bandwidth and increase the polysilicon area. Thus, the parameters of the design are tightly bounded to one another and this fact should be taken into account during the design steps.

2.3.1 The Cascode Common Source Amplifier

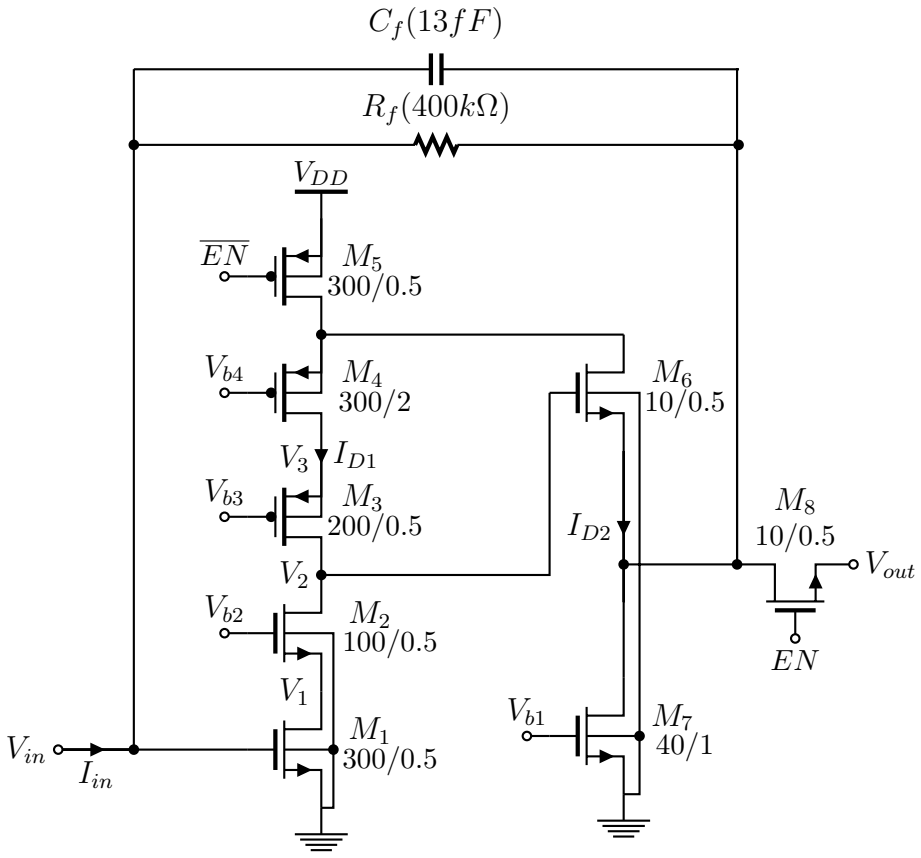

Figure 2.4: Cascode Common Source Amplifier

The core amplifier which consists of five NMOS transistors and three PMOS transistors is given in Fig. (2.4). M_1 and M_2 transistors are cascode connected transistors which give the main gain of the core amplifier. M_4 is the constant

current source transistor and M_3 transistor is cascode connected to them to boost the output impedance of M_4. To lower the output impedance of the cascode stage, a source follower amplifier is connected to the output of the first stage. M_6 is the source follower amplifier which is connected to M_7 current mirror transistor. R_f is the feedback transistor and C_f is the compensation capacitor. M_5 is the power shutdown switch and M_8 is the output switch. When the outputs of multiple TIAs are connected in parallel, M_8 transistors will form a multiplexer as given in Fig. (2.5).

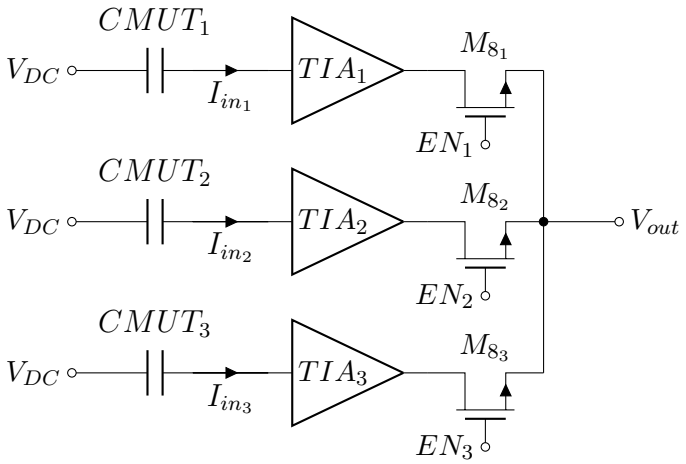

Figure 2.5: Connection diagram of multiple TIAs

2.3.1.1 Analysis

To simplify the analysis we will neglect the effect of the switches M_5, M_8 because their on resistance are very low. Since V_{SB3} is equal to zero than g_{mb3} is also equal to zero. The detailed analysis of the cascode amplifier can be found in [21]. The output impedance of the cascode PMOS current source R_{l3} is given as:

$$R_{l3} = r_{o3}(1 + g_{m3}r_{o4}) + r_{o4} \approx g_{m3}r_{o3}r_{o4} \tag{2.21}$$

As we can see, R_{l3} is equal to the output impedance of the M_4 multiplied by intrinsic gain $A_{i3} = g_{m3}r_{o3}$ of M_3. To increase r_{o4}, a longer channel length

is chosen for M_4. Also, to increase A_{i3}, L_3 is chosen minimum process length of 0.5μm and W_3 is chosen wider. To find the open loop gain of the cascode amplifier, we need to find gain from node V_1 to node V_2 which is the gain of M_2 written as

$$A_{v2} = \frac{V_2}{V_1} = \frac{1 + (g_{m2} + g_{mb2})r_{o2}}{r_{o2}}(r_{o2} \mid\mid R_{l3}) \approx (g_{m2} + g_{mb2})r_{o2}. \tag{2.22}$$

R_{l2} is the resistance seen from the drain of M_1. R_{l2} can be written as

$$R_{l2} = \frac{r_{o2} + R_{l3}}{1 + (g_{m2} + g_{mb2})r_{o2}} \approx \frac{g_{m3}r_{o3}r_{o4}}{(g_{m2} + g_{mb2})r_{o2}}. \tag{2.23}$$

Then we will write the gain from V_{in} to V_1. Since M_1 is the common source amplifier, its gain is given as

$$\begin{aligned} A_{v1} =& \frac{V_1}{V_{in}} = -g_{m1}(r_{o1} \mid\mid R_{l2}) \\ &= -g_{m1}r_{o1}\frac{g_{m3}r_{o3}r_{o4}}{g_{m3}r_{o3}r_{o4} + (g_{m2} + g_{mb2})r_{o2}r_{o1}} \end{aligned} \tag{2.24}$$

As the last step to find the gain from V_{in} to V_{out}, we need to find the source follower gain. The source follower gain is given as

$$A_{v3} = \frac{V_{out}}{V_2} \approx \frac{g_{m6}}{g_{m6} + g_{mb6}} \approx 0.8 \tag{2.25}$$

If we substitute Eq. (2.22), Eq. (2.24) and Eq. (2.25), the open loop gain of the cascode amplifier becomes Eq. (2.26)

$$A_v = A_{v1}A_{v2}A_{v3} \approx -0.8g_{m1}\frac{g_{m2}g_{m3}r_{o1}r_{o2}r_{o3}r_{o4}}{g_{m2}r_{o1}r_{o2} + g_{m3}r_{o3}r_{o4}} \tag{2.26}$$

If we assume that the core amplifier poles are far apart and the most dominant pole of the system is created from the node which has the highest impedance. This node is V_2, because of two cascoded transistors are connected. The impedance at the node V_2 is given as

$$\begin{aligned} R_{out1} &= [r_{o1} + r_{o2}(1 + (g_{m2} + g_{mb2})r_{o1})] \mid\mid [r_{o4} + r_{o3}(1 + g_{m3}r_{o4})] \\ &\approx \frac{g_{m2}g_{m3}r_{o1}r_{o2}r_{o3}r_{o4}}{g_{m2}r_{o1}r_{o2} + g_{m3}r_{o3}r_{o4}} \end{aligned} \tag{2.27}$$

The capacitance at the node V_2 is

$$C_{out1} = C_{DG2} + C_{DB2} + C_{DG3} + C_{DB3} + C_{GD6}. \tag{2.28}$$

The dominant pole can be written as

$$\begin{aligned}\omega_0 =& \frac{1}{2\pi R_{out1} C_{out1}} \\ \approx& \frac{g_{m2} r_{o1} r_{o2} + g_{m3} r_{o3} r_{o4}}{2\pi (C_{DG2} + C_{DB2} + C_{DG3} + C_{DB3} + C_{GD6})(g_{m2} g_{m3} r_{o1} r_{o2} r_{o3} r_{o4})}.\end{aligned} \tag{2.29}$$

Lastly, we need to find the unity gain bandwidth (GBW) of the core amplifier which is given

$$GBW = \frac{g_{m1}}{2\pi C_{out1}} \approx \frac{\sqrt{2 I_{D1} K_n (W/L)_1}}{2\pi C_{out1}} \tag{2.30}$$

where I_{D1} is the bias current of M_1, K_n is the NMOS transistors transconductance parameter, W is the width of the transistor and L is the channel length of the transistor. Eq. (2.30) shows that keeping C_{out1} lower is critical to achieve a high unity gain bandwidth for the given bias current I_{D1}. We optimized the size of M_2, M_3 and M_6 transistors to increase the GBW. Also, the size of M_1 transistor affects the input capacitance of the TIA as given in Eq. (2.43). To achieve a high unity gain bandwidth, we used a wider input transistor at the input. However, we used a narrow width transistor at the source follower to lower C_{out1}.

2.3.1.2 TIA Biasing

The TIA biasing circuit is given in Fig. (2.6). To get the maximum gain from the core amplifier, all transistors except switch transistors must operate in saturation region for all operation conditions. Since all transistors are connected each other, an incorrect biasing of the single transistor will cause a reduction in amplifier performance.

The basic idea of the bias circuit is to replicate a reference current I_{ref} for other transistor branches by current mirrors. For a good current matching, long channel transistors are used in current mirrors. For example, M_9/M_{10} and M_{12}/M_{15} are current mirror pairs. These transistors have longer channel length than the minimum process length of 0.5 μm and each pair has the same channel length. We have three current branches in our bias circuit which are I_{ref}, I_{D3} and I_{D4}. R_1 resistor is tied between V_{DD} and the gate of M_9 to generate the reference

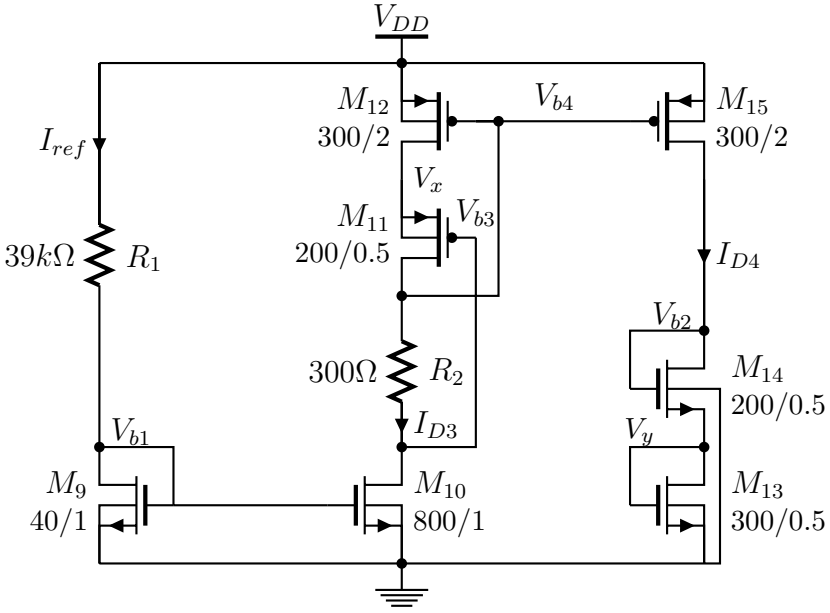

Figure 2.6: TIA Bias Circuit

current I_{ref}. Then I_{D3} is copied from I_{ref} by the current mirror transistor M_{10}. For analysis, we will ignore the channel length modulation and the body effect. The relation between I_{ref} and I_{D3} is given as:

$$I_{D3} = I_{ref}\frac{(W/L)_{10}}{(W/L)_9} = 20I_{ref} \tag{2.31}$$

I_{D4} is also replicated from I_{D3} by current mirror transistor M_{15}. Since M_{15} and M_{12} are the same, I_{D4} is equal to I_{D3}. Lastly, we will mirror I_{D3} to I_{D1} by connecting the gate of M_{11}, M_{12} and M_{14} to M_3, M_4 and M_2 to each other, respectively. To minimize the errors caused by the channel length modulation, the sizes of the current mirrors in the bias circuit and in the amplifier circuit are the same. So, I_{D1} is equal to I_{D3} and I_{D2} is equal to I_{ref}. In CMOS fabrication, the transistor parameters are prone to process variations. In the process file, statistically calculated variations of the transistor parameters are provided in terms of process corners. While designing the amplifier and the bias circuit, we should simulate the circuit for all process corners. In the amplifier circuit, we have two cascoded blocks and they consume a lot of voltage headroom. So, biasing of these transistors at the edge of the saturation region will increase the output

voltage swing. We designed a low voltage cascode current mirror by M_{11}, M_{12} and R_2 [22]. The condition to keep M_4 transistor in saturation region:

$$V_{SD4} > V_{SG4} - |V_{TP4}|$$
$$V_{DD} - V_3 > V_{DD} - V_{b4} - |V_{TP4}|$$
$$V_3 < V_{b4} + |V_{TP4}| \tag{2.32}$$
$$V_{b3} = V_3 - V_{SG3}$$
$$V_{b4} - V_{b3} > V_{SG3} - |V_{TP4}| \tag{2.33}$$

Eq. (2.33) shows that the voltage difference between V_{b4} and V_{b3} should be greater than $V_{SG3} - |V_{TP4}|$. In the bias circuit, gate of M_{12} is connected to drain of M_{11} and the gate of M_{11} is connected to its drain via resistor R_2. The voltage drop on R_2 should enforce the condition in Eq. (2.33) to hold. To match I_{D1} and I_{D3}, both M_{11} and M_{12} should be in saturation region.

$$I_{D3}R_2 = V_{b4} - V_{b3} \tag{2.34}$$
$$V_{SD11} > V_{SG11} - |V_{TP11}|$$
$$V_{b4} - V_{b3} < |V_{TP11}| \tag{2.35}$$

If we combine Eq. (2.34), Eq. (2.33) and Eq. (2.35), we get

$$V_{SG3} - |V_{TP4}| < I_{D3}R_2 < |V_{TP11}| + |V_{TP3}| \tag{2.36}$$

Since V_{SB3}, V_{SB4}, V_{SB11} and V_{SB12} are equal to 0, $V_{TP3} = V_{TP4} = V_{TP11} = V_{TP12}$. If we rewrite Eq. (2.36) we find

$$\sqrt{\frac{2I_{D1}}{K_p(W/L)_3}} < I_{D3}R_2 < 2|V_{TP3}| \tag{2.37}$$

$$\frac{I_{D1}}{2K_pV_{TP3}^2} < (W/L)_3. \tag{2.38}$$

To keep M_3, M_4, M_{11} and M_{12} in saturation, $(W/L)_3$ and R_2 should be in the range given by Eq. (2.37) and Eq. (2.38). In design steps, $(W/L)_3$ and R_2 values are found by parametric sweep simulations.

In the bias circuit, V_{b2} voltage is generated by M_{14} to bias M_2. The saturation condition for M_2 is given

$$\begin{gathered} V_{DS2} > V_{GS2} - V_{TN2} \\ V_2 + V_{TN2} > V_{b2} > V_{GS2} + V_{GS1} - V_{TN1} \\ V_2 = V_{GS1} + V_{GS6} \\ V_{GS1} + V_{GS6} + V_{TN2} > V_{b2} > V_{GS2} + V_{GS1} - V_{TN1} \end{gathered} \tag{2.39}$$

In the bias circuit, V_{b2} is equal to $V_{GS13} + V_{GS14}$. If $V_{GS13} + V_{GS14}$ is always less than $V_{GS1} + V_{GS6} + V_{TN2}$ and greater than $V_{GS2} + V_{GS1} - V_{TN1}$ then M_1 and M_2 will be in saturation. To satisfy these conditions, the size of M_{13} is made equal to M_1 and the size of the M_{14} is made equal to M_2. As a result, V_{GS13} is equal to V_{GS1} and V_{GS14} is equal to V_{GS2} because of $I_{D1} = I_{D3}$. Then M_1 and M_2 will be in saturation if

$$\begin{gathered} V_{GS6} > V_{GS2} - V_{TN2} \\ V_{TN6} + \sqrt{\frac{2I_{D2}}{K_n(W/L)_6}} > \sqrt{\frac{2I_{D1}}{K_n(W/L)_2}} \end{gathered} \tag{2.40}$$

M_7 transistor bias voltage V_{b1} is generated by M_9. There is no DC current flow over feedback resistor R_f and we can write that

$$V_{DS7} = V_{out} = V_{in} = V_{GS1} \tag{2.41}$$

By using Eq. (2.41), we can write bias condition for M_7

$$\begin{gathered} V_{GS1} > V_{b1} - V_{TN7} \\ V_{TN1} + \sqrt{\frac{2I_{D1}}{K_n(W/L)_1}} > \sqrt{\frac{2I_{D2}}{K_n(W/L)_7}} \end{gathered} \tag{2.42}$$

Size of M_1 and M_7 are chosen in terms of Eq. (2.42).

2.3.1.3 Input Capacitance of TIA

The main advantage of the cascode topology over a simple common source amplifier is that it lowers the Miller effect as given in Eq. (2.43) [21]. The input

capacitance of the cascode amplifier is given by:

$$C_{in,amp} = C_{GS1} + (1 - A_{v1})C_{GD1} \tag{2.43}$$

where C_{GS1} is the gate to source capacitance of M_1 and C_{GD1} is the gate to drain capacitance of M_1. A_{v1} is the Miller gain which is given in Eq. (2.24). C_{GS1} and C_{GD1} are given by:

$$C_{GS1} = W_1 C_{ov} + \frac{2W_1 L_1 C_{ox}}{3}, \quad C_{GD1} = W_1 C_{ov} \tag{2.44}$$

where W_1 is the width of the input transistor M_1, L_1 is the length of the input transistor M_1, C_{ov} is the overlap capacitance of the transistor and C_{ox} is the gate capacitance of the transistor. Eq.(2.43) can be rewritten as

$$C_{in,amp} = W_1\{(2 - A_{v1})C_{ov} + \frac{2L_1 C_{ox}}{3}\}. \tag{2.45}$$

To optimize $C_{in,amp}$, the size of the M_1 and the Miller gain A_{v1} should be minimized while conserving GBW. A_{v1} given in Eq. (2.24) can be approximated as $A_1 = g_{m1}r_{o1}$ which is the intrinsic gain of M_1.

2.3.1.4 Noise Analysis

As seen in Eq.(2.20), the voltage noise of the amplifier is an important factor to achieve a lower noise. For simplification, the noise contribution of the source follower is neglected. The input referred voltage noise of the cascode amplifier is given as:

$$\overline{V_{n,op}^2} = \frac{4kT\gamma}{g_{m1}} + \frac{4kT\gamma}{g_{m2}g_{m1}^2 r_{o1}^2} + \frac{4kT\gamma}{g_{m3}g_{m1}^2 r_{o4}^2} + \frac{4kT\gamma g_{m4}}{g_{m1}^2} \tag{2.46}$$

where r_o is the transistor output resistance. Typically, $g_{m1}r_{o1} \gg 1, g_{m1}r_{o4} \gg 1$ and $g_{m4}/g_{m1} \ll 1$, yielding

$$\overline{V_{n,op}^2} \approx \frac{4kT\gamma}{g_{m1}}. \tag{2.47}$$

From the Eq.(2.47), the voltage noise of the amplifier can be minimized by increasing the input transistor transconductance g_{m1}. If the transistor is in the saturation region, the g_{m1} can be written as

$$g_{m1} = \sqrt{2\mu_0 C_{ox} I_{D1} \frac{W_1}{L_1}} \tag{2.48}$$

where μ_0 is the mobility of the transistors and I_{D1} is the bias current or the drain current of the transistor. If Eq.(2.47) and Eq.(2.48) are combined together to get

$$\overline{V_{n,op}^2} \approx \frac{4kT\gamma}{\sqrt{2\mu_0 C_{ox}}}\sqrt{\frac{L_1}{I_{D1}W_1}} \tag{2.49}$$

As seen in Eq.(2.49), the voltage noise $\overline{V_{n,op}^2}$ is inversely proportional to the square root of I_{D1} and W_1.

To lower the input current noise given in Eq.(2.20), g_{m1} should be higher and $C_{in,amp}$ should be lower. Since the power budget is limited, g_{m1} can be increased only by making M_1 transistor wider. However, as M_1 gets wider, the input capacitance of the amplifier ($C_{in,amp}$) also increases. As a result, there is an optimal input transistor size for the smallest noise figure (NF) [23].

2.3.1.5 Optimal M_1 Size

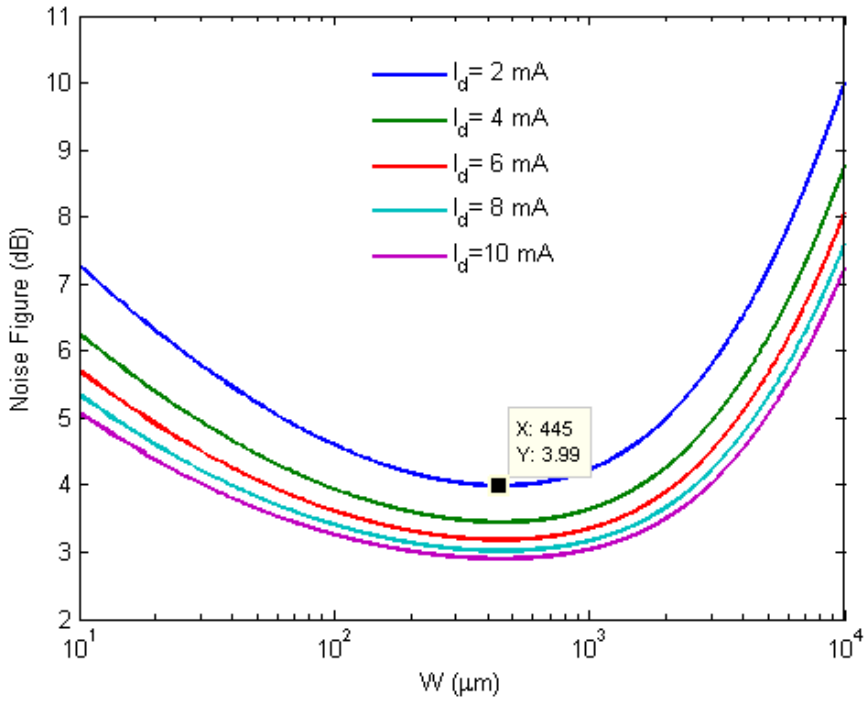

Figure 2.7: Optimal Noise Figure vs. Input Transistor Width

To find the optimum W_1, the MATLAB code given in Apendix A.1 is used. In the code, C_{par} is assumed to be 1.5 pF which is sum of the bonding pad capacitance [19] and the electrostatic discharge (ESD) protection circuit capacitance at the input. For simplification of the analysis A_{v1} taken as -8. NF is optimized for 20 MHz. The result from the MATLAB code is given in Figure 2.7.

As seen in Fig. (2.7), NF starts to decrease as W_1 increases until the optimum point because the amplifier voltage noise decreases. After the optimum point, NF increases gradually because the amplifier input capacitance becomes dominant. Additionally, the bias current I_{D1} and NF are directly proportional while the optimum transistor width does not depend on the bias current.

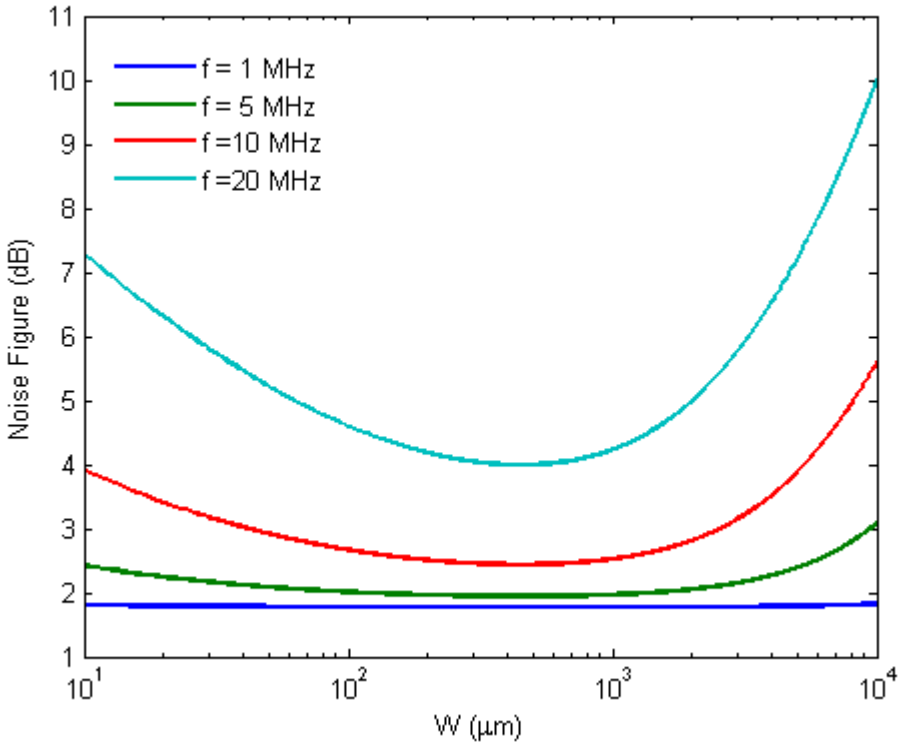

Figure 2.8: Optimum Input Transistor Width for Different Frequencies $I_D = 2mA$

In Fig. (2.8), the optimum input transistor width is analysed at different frequencies for the given bias current. The results indicate that the optimum input transistor width doesn't change for different frequencies. As a result of optimum transistor size analysis, we chose size of M_1 as $(300\mu m/0.5\mu m)$ and the bias current I_D as 2 mA.

2.3.1.6 Simulations

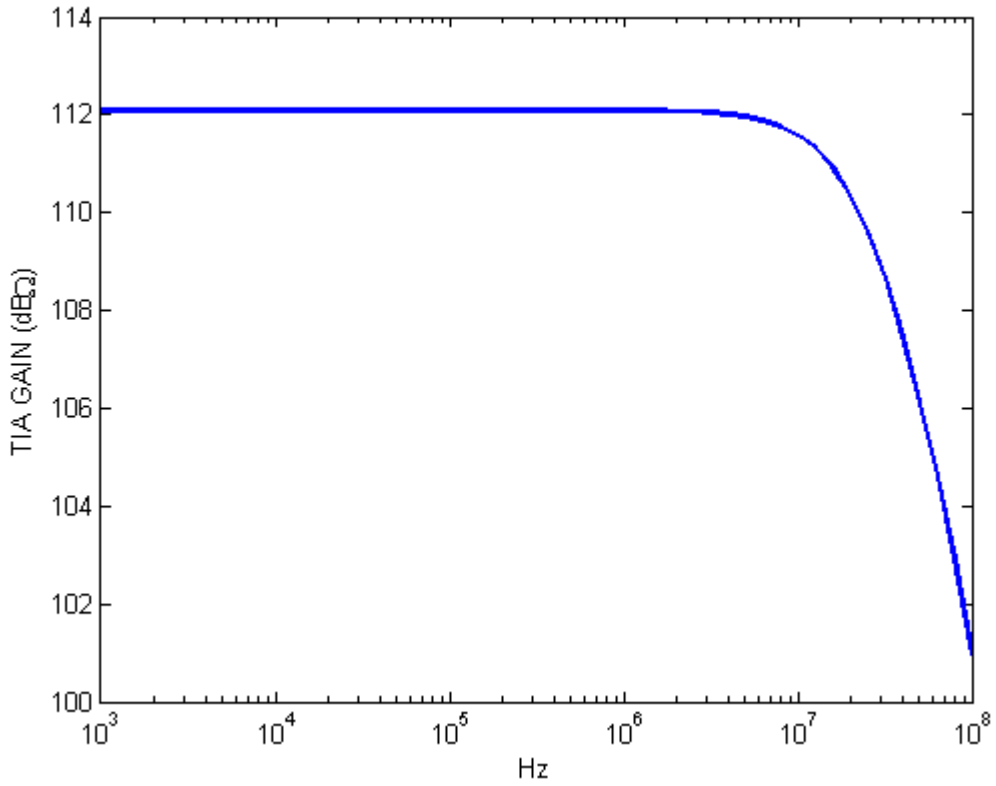

Figure 2.9: TIA Transimpedance Gain and Bandwidth

To find bandwidth and transimpedance gain of the implemented circuit, small-signal AC analysis is done with CADENCE Spectre simulator. As a result, simulated closed loop bandwidth of the TIA is 30 MHz and the transimpedance gain is 400 kΩ (112 dBΩ) as given in Fig. (2.9).

2.3.1.7 Noise

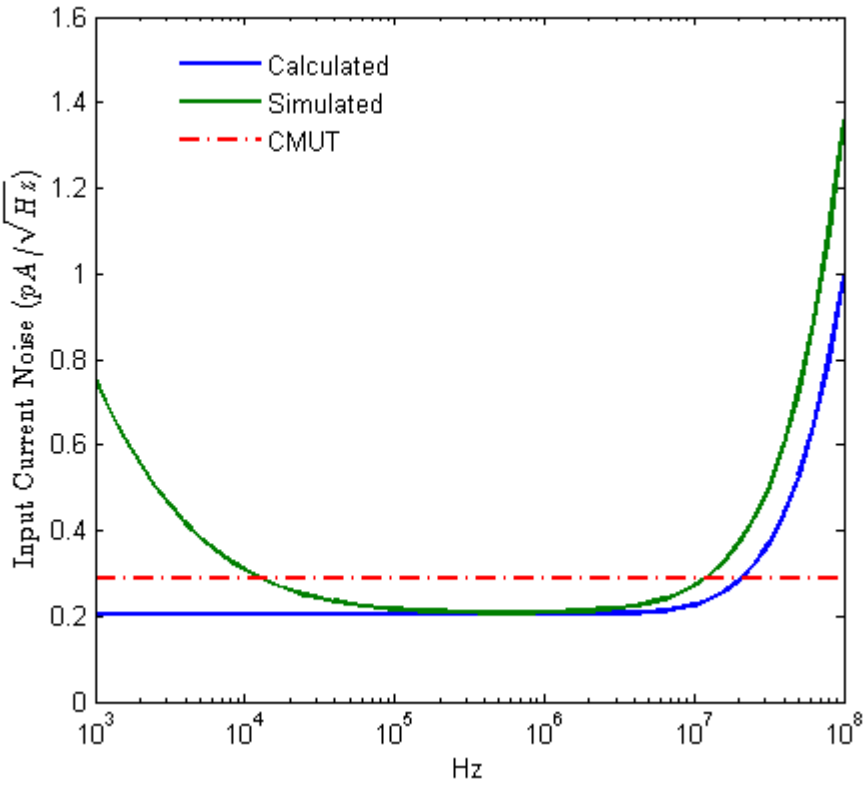

Figure 2.10: TIA Input Referred Current Noise

In Fig. (2.10), theoretically calculated and simulated TIA input referred current noise is given. As seen in Fig. (2.10), TIA input referred current noise is higher than CMUT current noise below 100 kHz because of transistors flicker noise which is neglected in the MATLAB calculation. TIA input current noise is approximately 0.2 pA/$\sqrt{\text{Hz}}$ at the interval (100 kHz - 10 MHz), which is equal to the current noise of 400 kΩ feedback resistor R_f. As seen, it is lower than CMUT current noise 0.3 pA/$\sqrt{\text{Hz}}$. Beyond 10 MHz, TIA input referred current noise starts to increase because of the total input capacitance Eq. (2.20). However, the noise increase at higher frequencies is not significant because additional low pass filters can be used at the input of an ultrasound scanner. Additionally, the simulated input referred current noise is always higher than that of the calculated one beyond 10 MHz. This shows that the calculated

TIA input capacitance given by Eq. (2.45) is lower than the simulated value.

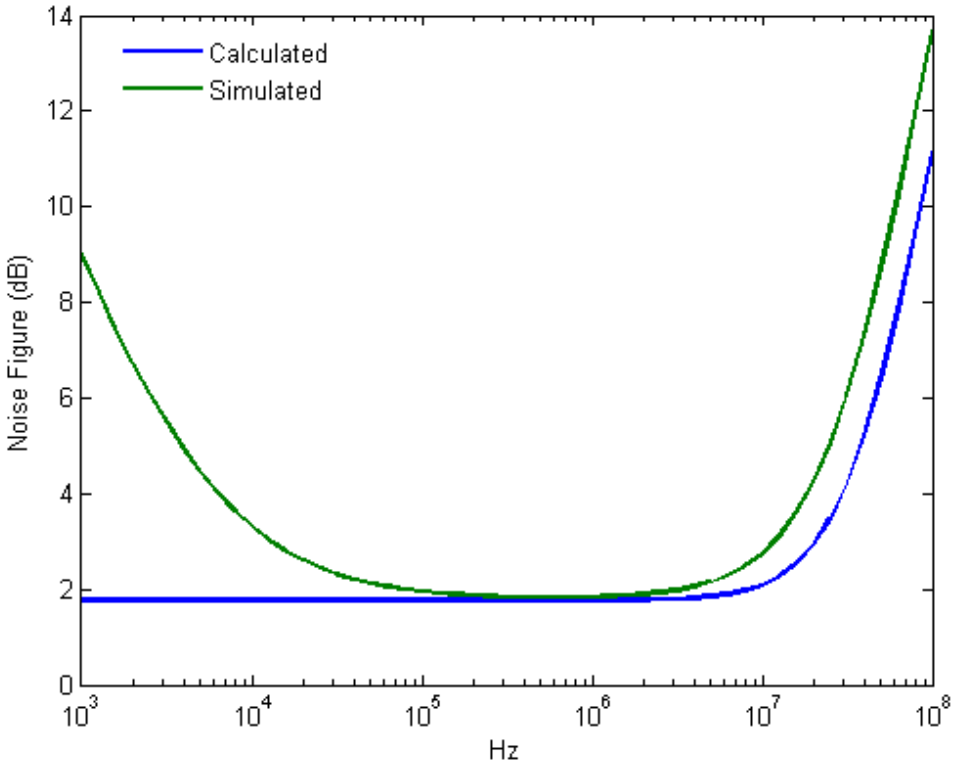

Figure 2.11: TIA Input Referred Current Noise

To obtain the noise figure presented in Fig. (2.11), we used the input current noise Eq. (2.20) and the CADENCE Spectre noise simulation result. As depicted above, the simulated NF is very high at the lower and higher frequencies. However, at the mid band which we are interested in, NF is equal to 1.8 dB. As a result, the input current noise of the amplifier is lower than current noise of the CMUT within the frequency range 20 kHz to 10 MHz.

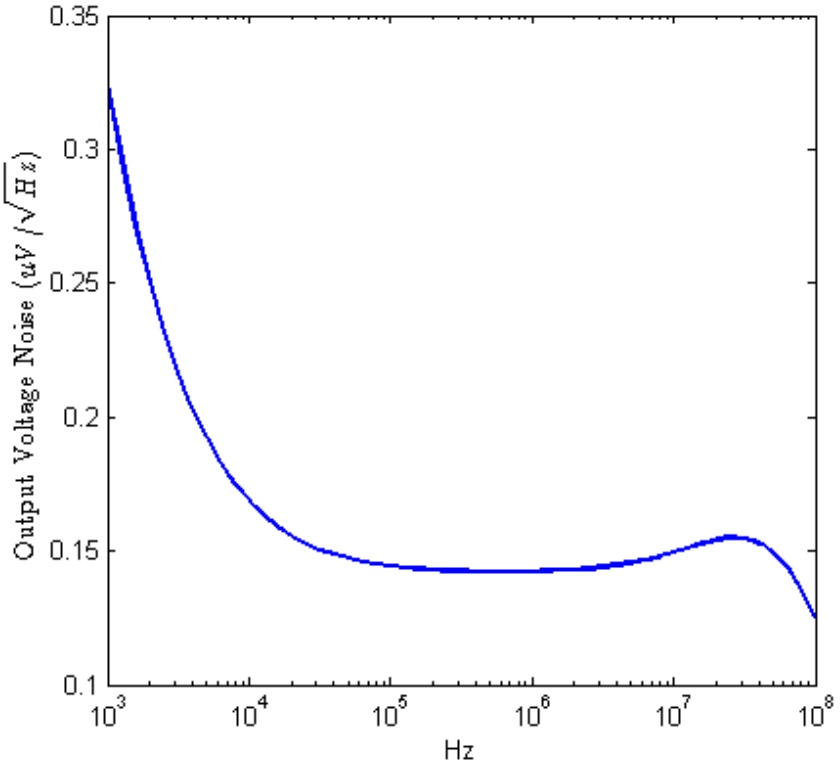

Figure 2.12: Total Output Voltage Noise Spectral Density

The total output voltage noise spectral density graphic which is simulated by CADENCE Spectre given in Fig. (2.12). The output voltage noise is approximately equal to 0.14 μV/$\sqrt{\text{Hz}}$ in frequency range (100 kHz to 10 MHz). Because of the feedback and input capacitances, the output noise voltage has a peak at 25 MHz and it is equal to 0.155 μV/$\sqrt{\text{Hz}}$.

2.3.1.8 Stability

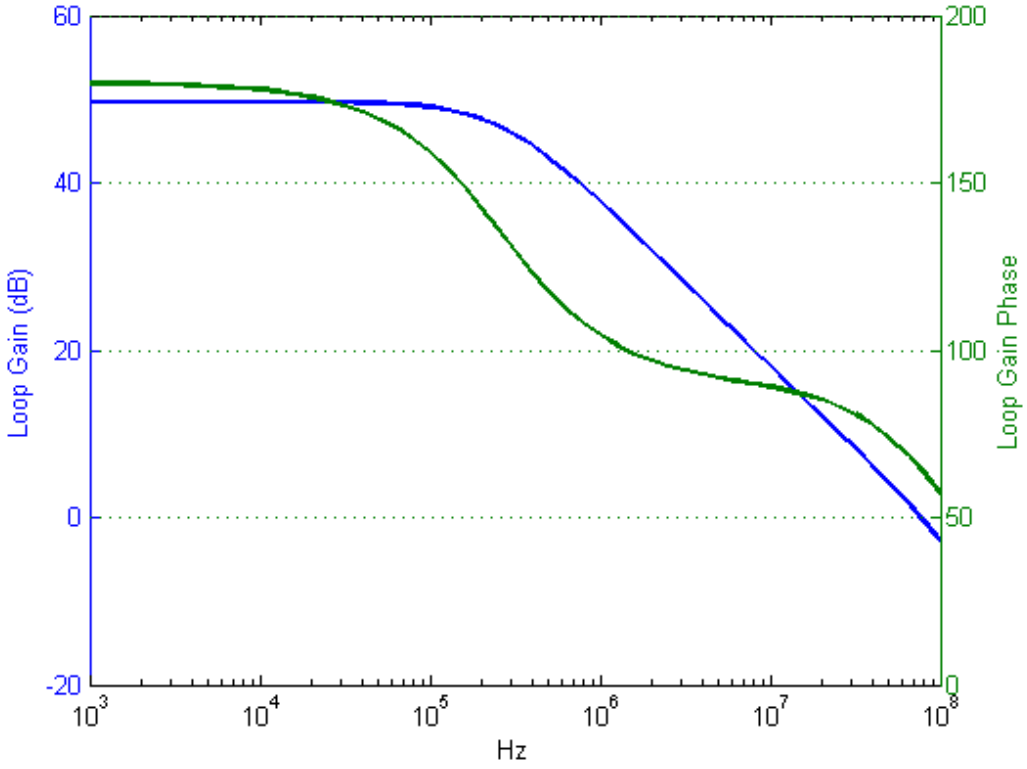

Figure 2.13: Loop Gain

The stability analysis of the TIA is done with CADENCE Spectre Stability simulation tool (STB). To determine the stability of the system, the loop gain of the system should be analysed. The best known method to find the loop gain of a closed system is breaking the feedback from the input while preserving the system DC operation point. However, STB can generate the loop gain by inserting an ampermeter into the feedback without breaking the loop. TIA loop gain and the loop gain phase is given in Fig. (2.13). When the loop gain is 0 dB at 77 MHz, phase of the loop gain is 65° degree. So, the phase margin of TIA is 65° degree, acceptable value.

2.4 Layout

After completing the schematic design and simulations, the next step is the layout design. The designed TIA will be fabricated by AMS C35B4C3 (0.35 μm) CMOS process. C35B4C3 process has two layers poly-silicon, four layers Metal, 3.3V / 5V MOSFET transistors and high resistive poly. C35B4C3 process features are summarized in Table 2.1. Additionally the cross section of the wafer given in Fig 2.14.

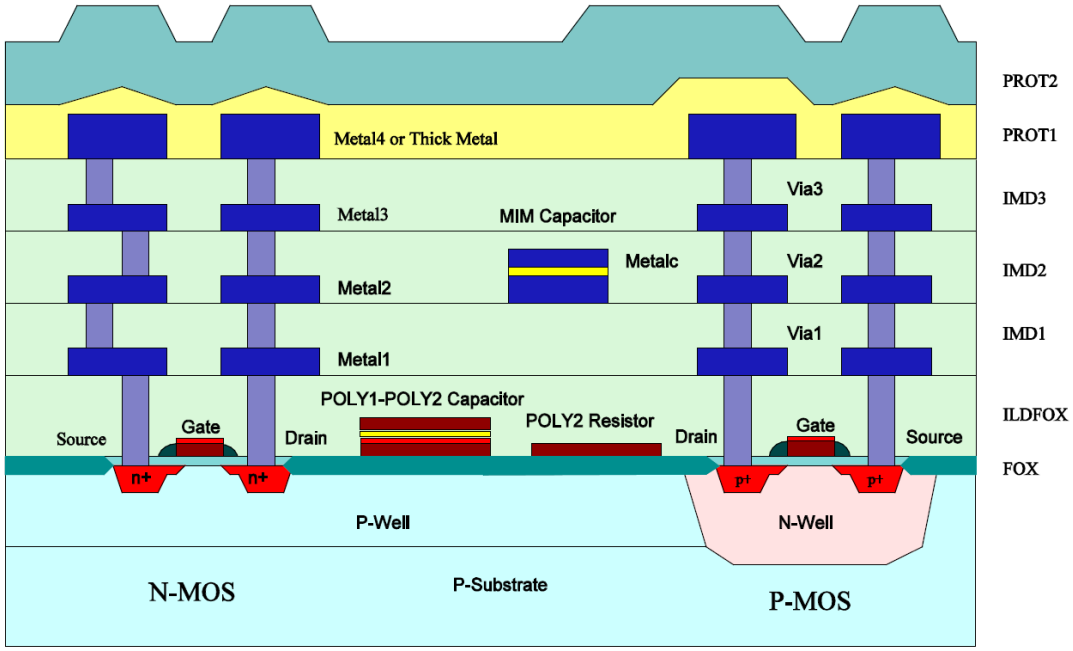

Figure 2.14: C35B4C3 Process Wafer Cross Section [1]

The amplifier layout is given in Fig. (2.15). The dimensions of the TIA layout is 133μm x 45μm. In the chip, 128 TIA cells will be placed in a one column to connect them to input pads easily. Additionally, left side of the layout is input port and the right side is output port of the TIA. The bias voltage ports are placed in rows and their connections reach from top to bottom side of the cell boundary. When TIA cells are put on top of each other, their bias and supply ports will be connected each other without any interconnections. We will use only one bias circuit to bias all TIA cells because all of them are the same. By this way

Table 2.1: C35B4C3 Features [1]

Process technology specifications	**Units**	**C35B4C3**
Drawn MOS Channel Length	μm	0.35
Operating Voltage	V	3.3 / 5
Number of Masks	#	20
Number of Masking layers	#	24
Number of Metal Layers	#	4
Number of Poly Layers	#	2
Substrate Type		p
Diffusion Pitch	μm	0.9
Metal1/2/3/4 Pitch	μm	0.95 / 1.1 / 1.1 / 1.2
Metal1/2/3/4 conacted Pitch	μm	1.05 / 1.2 / 1.2 / 1.3
Poly1 Pitch	μm	0.8
High Resistive Poly	k$\Omega/\square$	1.2
Poly1/Poly2 Precision Caps	fF/μm^2	0.9
N/PMOS Channel Length	μm	0.30 / 0.30
N/PMOS Saturation Current	μA/μm	520 / 240

we will save power and silicon space. Additionally, the bias voltages generated inside the chip will have output pads to control and adjust their voltages from the outside.

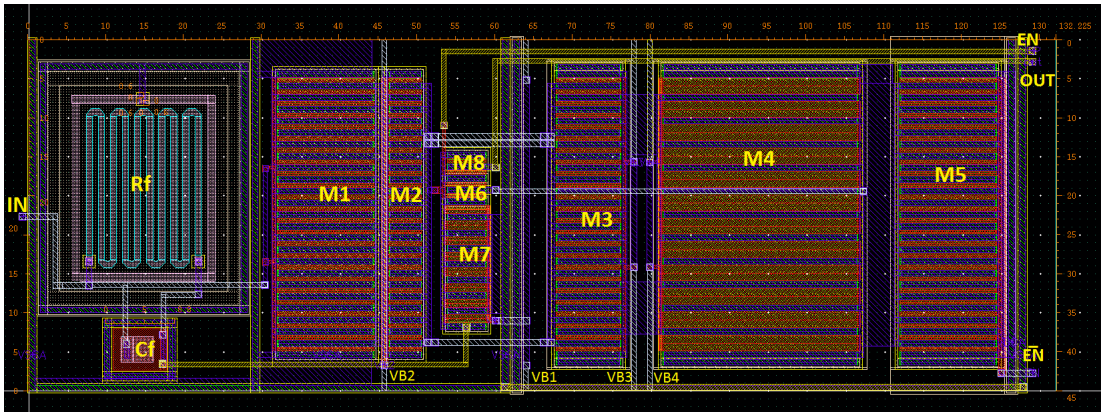

Figure 2.15: TIA Layout

In the layout design, the most critical part is parasitic capacitances between layers and routes. In our design, the most critical part of the amplifier is node V_2 in Fig. (2.4) because additional parasitic capacitances will limit GBW in Eq. (2.30).

So, in the layout we put transistors M_2, M_6 and M_3 at that node as close as possible. We divided the wide transistors to multiple gates to lower drain and source capacitances. M_1 transistor is placed as close as possible to the input port to decrease interconnection length and parasitics. Using the minimum width for interconnections decreases the metal to substrate parasitic capacitances. However, metal layers and vias have a current density limit. For example, METAL-1 layer can carry current up to 1mA/1μm width. The connection between M_2 and M_3 is sensitive to the parasitic capacitances, but this connection has to carry 2 mA current. So, the interconnection width between M_2 and M_3 is chosen in terms of current density limit. To prevent latch up, ntub and ptub guard rings are added between the PMOS and NMOS transistors. The ring will be completed when all the cells are put together.

Another critical part of the layout is the feedback resistor R_f. Since we need a high resistance at the feedback in a small area, we used "High Resistive Poly" module (RPOLYH) layer in layout. RPOLYH sheet resistance is 1.2k$\Omega/\square$ and the minimum allowed width is 0.8μm. RPOLYH layer has also parasitic capacitances to substrate and this capacitances cause ringing in the step response. Increasing the width of the R_f, increases the resistance precision however it also increases the parasitic capacitances. So, we chose the minimum width for R_f to minimize the parasitic capacitances. To get 400kΩ resistance, we used 267 μm length, 0.8μm width RPOLYH and we draw R_f like a meander to minimize the size. The feedback capacitor C_f is designed by using POLY1-POLY2 capacitor CPOLY which has 0.86fF/μm^2.

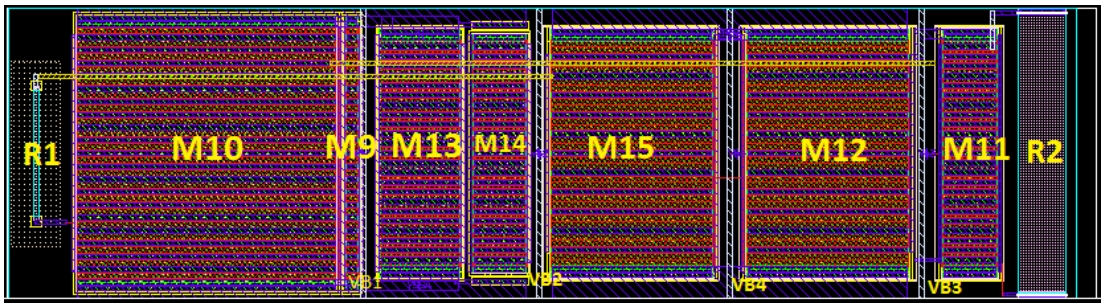

Figure 2.16: Bias Circuit Layout

The bias circuit layout is given in Fig. (2.16). The dimensions of the layout is 170μm x 45μm. Although R_1 is bigger than R_2, R_2 covers much more area than R_1 in the layout. Since R_2 is critical to keep transistors in saturation, we used high precision poly2 resistor (RPOLY2PH) which has the highest precision of %5 whereas RPOLYH precision is %20 . The sheet resistance of the RPOLY2 is 50$\Omega/\square$ which is much smaller than RPOLYH.

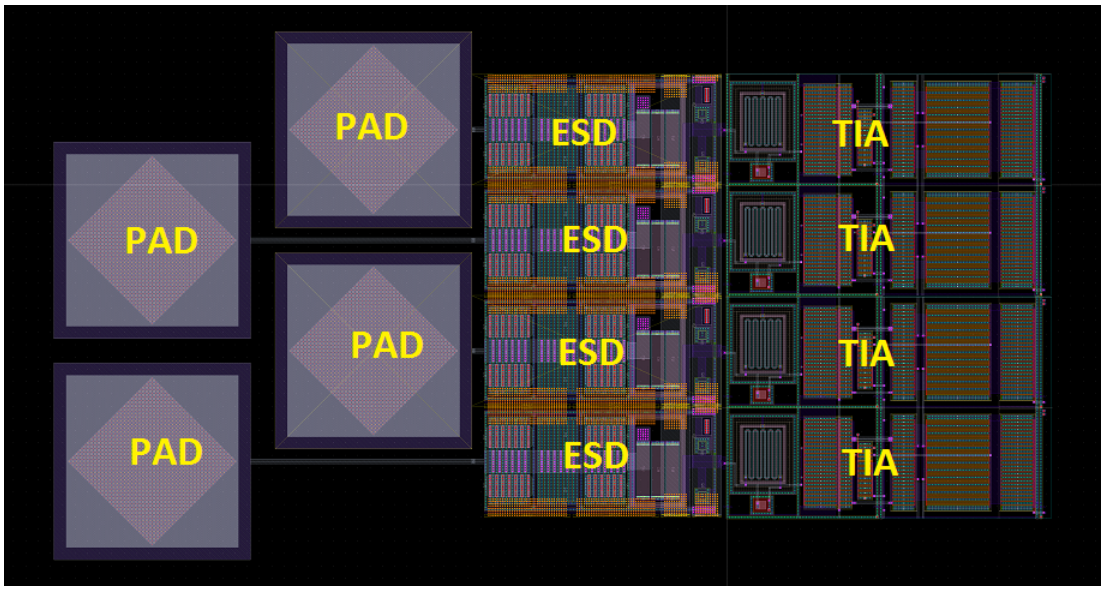

Figure 2.17: TIA Layout with I/O Pads

In Fig. (2.17) 4 TIA cells integrated to I/O Pads and electro static discharge (ESD) circuit. Size of the one I/O Pad is 85μm x 85μm. We placed the I/O PADS in 2 columns to keep aspect ratio of the die low. Also, we added ESD diodes to the input for protecting the amplifier input. In the die, we will have 128 input Pads and the pitch of the pads is 45μm. So, our die size is 5760μm x 1215μm and the total die area is 7mm^2.

2.4.1 Post-layout Simulations

After completing the layout design, we extracted parasitic capacitances from the layout by QRC simulation. Then we made a Monte Carlo simulation by using extracted schematic. In the Monte Carlo simulation we tested 48 different

conditions. We tested the circuit for temperatures 0° C, 27° C and 70°. As described before CMOS technology file has process corner. Both resistors and capacitors have worst case speed and worst case power corners. Transistors have four process corners which are cmosws, cmoswp, cmoswo and cmoswz. In cmosws, the transistors are slower and weaker than typical. In cmoswp, the transistors are faster and stronger than typical. In cmoswo, PMOS transistors are slower than typical and NMOS transistors are faster than typical. cmoswz is the opposite of the cmoswo. In these corners, we made AC small-signal analysis, stability analysis and transient analysis. In the AC analysis we measured the TIA bandwidth whereas in the stability analysis we measured the phase margin of the TIA. Lastly, in the transient simulation, we applied 100 nA current pulse at the input to measure overshoot at the TIA output. Monte Carlo simulation results are depicted in Table 2.2. Summarized parameters of the designed TIA is given in Table 2.3.

Table 2.2: Monte Carlo Simulation Results

	Minimum	Maximum
Bandwidth	28 MHz	80 MHz
TIA Gain	333 $k\Omega$	466 $k\Omega$
Phase Margin	53°	121°
Overshoot	%1	%33

Table 2.3: Results

Process	0.35μm
TIA Area	133μm x 45μm
Bias Area	170μm x 45μm
Bandwidth	30 MHz
TIA Gain	400 kΩ
Input Current Noise	270 fA/$\sqrt{\text{Hz}}$ @ 10 MHz
Power Supply	5 V
TIA Power Consumption	10.5 mW
Bias Power Consumption	20.5 mW

Chapter 3

Conclusion

For ultrasonic imaging with CMUTs, interfacing electronics is needed because impedance mismatch between the cable and CMUT receivers and to preserve the CMUT receiver sensitivity. For this reason, a CMOS transimpedance amplifier is designed for connecting the CMUT receivers to an ultrasonic imaging system. We evaluated different TIA topologies such that resistive termination, common gate amplifier and resistive feedback TIA. In the evaluation of the these topologies, we saw that resistive termination and CGA has limitations to achieve a low noise performance. However, a resistive feedback TIA can provide both low noise and wide bandwidth amplification.

To preserve the CMUT receiver's sensitivity, designing a low noise amplifier is very important. In the analysis of the resistive feedback TIA, we saw that capacitances at the input of the amplifier and the input voltage noise of the core amplifier have significant effect on noise performance of the amplifier. Additionally, we find out that there is a trade off between the input capacitance of the amplifier and the input voltage noise of the amplifier. To design a low noise amplifier, we write a MATLAB code to find the optimum size of the input transistor.

We implemented the schematic of TIA with Cadence and made simulations to

characterize the TIA. Designed TIA has 30 MHz bandwidth and 400 kΩ transimpedance gain. Total input referred current noise of the TIA is 270 fA/$\sqrt{\text{Hz}}$ at 10 MHz. The noise figure of the TIA is 2.7 dB at 10 MHz when connected to the CMUT with 200 kΩ source resistance. Power consumption of the TIA is 10.5 mW. These results shows that a low power, low noise and wide bandwidth TIA design is achieved. The design will be produced by Europractice multi-project wafer (MPW) service using AMS foundry [24].

Bibliography

[1] Austriamicrosystems, "Technology Processes and Runs in 2013." `http://cmp.imag.fr/aboutus/slides/Slides2014/02_AMS_2014.pdf`, 2014. [Online; accessed 28-Nov-2015].

[2] O. Oralkan, X. Jin, F. Degertekin, and B. Khuri-Yakub, "Simulation and experimental characterization of a 2-D capacitive micromachined ultrasonic transducer array element," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 46, pp. 1337–1340, Nov 1999.

[3] C. Harder, B. Van Zeghbroeck, H. Meier, W. Patrick, and P. Vettiger, "5.2-GHz bandwidth monolithic GaAs optoelectronic receiver," *Electron Device Letters, IEEE*, vol. 9, pp. 171–173, April 1988.

[4] Y. Zhao, J. Zhao, X. Wang, G. M. Xia, A. P. Qiu, Y. Su, and Y. P. Xu, "A sub-μg bias-instability MEMS oscillating accelerometer with an ultra-low-noise read-out circuit in CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 50, pp. 2113–2126, Sept 2015.

[5] A. Nikoozadeh, I. Wygant, D.-S. Lin, O. Oralkan, A. Ergun, D. Stephens, K. Thomenius, A. Dentinger, D. Wildes, G. Akopyan, K. Shivkumar, A. Mahajan, D. Sahn, and B. Khuri-Yakub, "Forward-looking intracardiac ultrasound imaging using a 1-D CMUT array integrated with custom front-end electronics," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 55, pp. 2651–2660, December 2008.

[6] X. Jin, I. Ladabaum, and B. Khuri-Yakub, "The microfabrication of capacitive ultrasonic transducers," *Microelectromechanical Systems, Journal of*, vol. 7, pp. 295–302, Sep 1998.

[7] O. Oralkan, A. Ergun, C.-H. Cheng, J. Johnson, M. Karaman, T. Lee, and B. Khuri-Yakub, "Volumetric ultrasound imaging using 2-D CMUT arrays," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 50, pp. 1581–1594, Nov 2003.

[8] X. Jin, B. Ehuri-Yakub, F. Degertekin, I. Ladabaum, and S. Calmes, "Micromachined capacitive ultrasonic immersion transducer for medical imaging," in *Engineering in Medicine and Biology Society, 1998. Proceedings of the 20th Annual International Conference of the IEEE*, vol. 2, pp. 779–782 vol.2, Oct 1998.

[9] O. Oralkan, A. Ergun, J. Johnson, M. Karaman, U. Demirci, K. Kaviani, T. Lee, and B. Khuri-Yakub, "Capacitive micromachined ultrasonic transducers: next-generation arrays for acoustic imaging?," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 49, pp. 1596–1610, Nov 2002.

[10] I. Wygant, X. Zhuang, D. Yeh, O. Oralkan, A. Ergun, M. Karaman, and B. Khuri-Yakub, "Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 55, pp. 327–342, February 2008.

[11] D. Lemmerhirt, X. Cheng, O. Kripfgans, M. Zhang, and J. Fowlkes, "A fully-populated 32x32 CMUT-in-CMOS array," in *Ultrasonics Symposium (IUS), 2010 IEEE*, pp. 559–562, Oct 2010.

[12] J. Woo, "A short history of the development of ultrasound in obstetrics and gynaecology," *See http://www. ob-ultrasound. net/history1. html (last checked 14 May 2011)*, 2002.

[13] F. IBMT, "Ultrasound Research Device DiPhAS." `http://www.ibmt.fraunhofer.de/content/dam/ibmt/en/documents/PDFs/ibmt-product-information-sheets/ibmt-ultrasound/US_ba_`

`Ultrasound-Research-Device-DiPhAS-2011.pdf`, 2015. [Online; accessed 28-Nov-2015].

[14] N. Gray, "ABCs of ADCs," *National Semiconductor Corporation, Aug*, vol. 4, 2003.

[15] B. Razavi, *Design of Integrated Circuits for Optical Communications*. McGraw-Hill Series in Electrical and Computer Engineering, McGraw-Hill, 2003.

[16] I. Wygant, N. Jamal, H. Lee, A. Nikoozadeh, O. Oralkan, M. Karaman, and B. Khuri-yakub, "An integrated circuit with transmit beamforming flip-chip bonded to a 2-D CMUT array for 3-D ultrasound imaging," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 56, pp. 2145–2156, October 2009.

[17] G. Gurun, P. Hasler, and F. Degertekin, "Front-end receiver electronics for high-frequency monolithic CMUT-on-CMOS imaging arrays," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 58, pp. 1658–1668, August 2011.

[18] K. Chen, H.-S. Lee, A. Chandrakasan, and C. Sodini, "Ultrasonic imaging transceiver design for CMUT: A three-level 30-Vpp pulse-shaping pulser with improved efficiency and a noise-optimized receiver," *Solid-State Circuits, IEEE Journal of*, vol. 48, pp. 2734–2745, Nov 2013.

[19] A. Sharma, M. Zaman, and F. Ayazi, "A 104-dB dynamic range transimpedance-based CMOS ASIC for tuning fork microgyroscopes," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 1790–1802, Aug 2007.

[20] W. Jung, *Op Amp Applications Handbook*. Analog Devices series, Newnes, 2005.

[21] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill higher education, Tata McGraw-Hill, 2002.

[22] E. Bruun and P. Shah, "Dynamic range of low-voltage cascode current mirrors," in *Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on*, vol. 2, pp. 1328–1331 vol.2, Apr 1995.

[23] A. Abidi, "On the choice of optimum FET size in wide-band transimpedance amplifiers," *Lightwave Technology, Journal of*, vol. 6, pp. 64–66, Jan 1988.

[24] Europractice-IC, "Multi Project Wafer Runs." `http://www.europractice-ic.com/prototyping.php`, 2015. [Online; accessed 28-Nov-2015].

Appendix A

Data

A.1 Optimum Width MATLAB Code

```
%% Initials
k=1.38E-23; % J/K
T=300; % K
Rf = 400e3; % ohm
Rs = 200e3;
Ccmut = 0.1e-12; % F
Cpar = 1.5e-12;
W = (10:1:10000)*1e-6; % m
L = 0.5e-6; % m
tox= 15.2e-9; % m
u0 = 564.3e-4; %m^2/(V.s)
er = 3.9;
e0 = 8.85e-12; % F/m
Vth = 0.76; %V
Cgdo = 1.08e-10; %F/m 5
Cox = er*e0/tox;
Cg = Cox*W*L;
Cov = Cgdo*W;
CGS = 2*Cg/3+Cov;
CGD = Cov;
```

```
miller = -8; % 1+gm1 /(gm2+gmb2)
Cin_op = CGS+(1-miller)*CGD;
%wx = (Ccmut+Cpar)/((miller)*Cgdo+2*L*Cox/3)*1e6
% Cin,amp = Ccmut+Cpar
%Id = 2e-3; % Bias Current
for i=(1:5)
    Id=i*2e-3;
%vop = 0.3e-9; % (nV/sqrt(Hz)
%gm = 15e-3; % S gm1
gm = 2/3*sqrt(2*u0*Cox*Id*W/L);
gm2= gm/miller;
$Ctot = Cin_op+Ccmut+Cpar;$
vop = sqrt(4*k*T./gm); % (nV/sqrt(Hz)
ix2 = (vop.*Ctot).^2;
%f = 10.^(0:0.01:8);
f=20e6;
w = 2*pi*f;
%% Input Noise
%inoise = w.^2.*ix2+(vop/(Rs*Rf/(Rs+Rf)))^2+4*k*T/Rf+4*k*T/Rs;
inoise = w.^2.*ix2 + (vop/(Rs*Rf/(Rs+Rf))).^2;
irf =4*k*T/Rf*ones(1,size(f,2));
% figure(1)
% tit = sprintf('Rf=%d,Rs=%d,Ctot=%d,Vop=%d',Rf,Rs,Ctot,vop);
% loglog(f,inoise,f,irf)
% title(tit)
% legend('Opamp Noise','Feedback Noise')
% xlabel('Hz'); ylabel('A^2/Hz');
%% Noise Figure
icmut = 4*k*T/Rs;
nf(i,:) = db((inoise+irf+icmut)/(icmut),'power');
%led = sprintf('Rf=%0.3g,Rs=%0.3g,Id=%0.3g,L=%0.3g, f=%0.3g',Rf,Rs,Id,L,f);
P(i) = Id*5/1e-3;
led{i} = sprintf('I_d=%2.0f mA',P(i)/5);
%legend(led);
Gm(i,:) = vop;
CCtot(i,:)=Ctot;
end
figure(1)
semilogx(W./1e-6,nf,'LineWidth',2)
%title('Noise Figure @ 20MHz')
```

```
xlabel('W ({\mu}m)'); ylabel('Noise Figure (dB)');
legend(led,'Location','best')
legend BOXOFF
```