LASER FABRICATION OF IN-CHIP MULTI-LAYER MICRO-CHANNELS

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By
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Laser fabrication of in-chip multi-layer micro-channels
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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

LASER FABRICATION OF IN-CHIP MULTI-LAYER MICRO-CHANNELS

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M.S. in MATERIALS SCIENCE AND NANOTECHNOLOGY
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For over half a century, the trend towards miniaturization resulted in great advances in electronic devices and computation. However, this is recently challenged by the emerging "heat-wall", a term indicating that the limitation in heat extraction capability precludes further increasing the clock rates of electronics and thus delays faster computation [1]. The challenge of heat extraction is a critical contributor to the recent stalling of Moore's Law. A potential solution for the heat-wall problem is to exploit microfluidic channels, in order to deliver controlled amounts of cooling fluid into relevant parts of the chip. Such an innovative approach is shown recently using integrated microfluidics [1]. However, such approaches constitute surface microchannels fabricated with conventional lithography techniques, involving expensive and complicated fabrication steps. Further, these strategies may not treat all hot spots over a chip, where microfluidic channels are challenged to have access to desired locations.

Here, we propose a laser-based micro-fabrication approach for creating multi-layered microchannels at any depth in the bulk of silicon. Further, the method ensures that the optical quality of top wafer surface remains preserved for potential integration of on-chip elements. Previously, proof-of-concept 3D laser-sculpting of silicon wafers have been demonstrated [2]. Here, we leverage this approach, and exploit a two-step method which involves nonlinear laser-writing deep inside Si, followed by selective chemical etching of modified areas. We demonstrate the first fully buried multi-layered arrays, curved geometries and advanced architecture control. We create in-chip microchannels with a high aspect ratio of 25. We investigate the scaling and feature size of structures and the flexibility in laser-writing modality; characterize selective etching rates; and achieve wafer surface protection exploiting photo-resist coatings [3]. We further present early results for

low channel-wall roughness (0.23 µm) using modulated beams, and fabricate vertical micro-channels, *i.e.*, "through-silicon vias". The created multi-layer channel architectures with unscathed wafer surfaces have significant potential for use in heat-engineering of integrated systems.

Keywords: laser micro-/nano-lithography, 3D laser writing, direct writing, nonlinear absorption, subtractive manufacturing, micro-channels, in-chip systems.

ÖZET

LAZER İLE YONGA-İÇİ ÇOK KATMANLI MİKRO-KANAL ÜRETİMİ

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Yarım yüzyıldan fazla bir süredir devam eden elektroniklerin boyutunun küçültülmesine dair yönelim, elektronik cihazlarda ve bilişimde büyük ilerlemelerle sonuçlanmıştır. Ancak bu ilerlemeler "ısı-duvarı" probleminin ortaya çıkışıyla kesintiye uğramıştır. Isı duvarı terimi, sistemden ısının uzaklaştırılması kapasitesindeki kısıtlamayı ifade etmektedir. Isı duvarı nedeniyle elektronik cihazların saat hızlarındaki artış oranı azalmış ve daha hızlı hesaplama seviyelerine ulaşım güçleşmiştir [1]. Soğutma problemi, günümüzde, teknolojinin Moore Yasası'nda öngörüldüğü gibi ilerleyememesinde kritik bir rol oynamaktadır. Isı-duvarı problemine olası bir çözüm, yongaların içindeki gerekli yerlere, kontrollü miktarlarda, soğutucu akışkan dağıtımı sağlayan mikro-akışkan kanalların kullanımıdır. Bu yenilikçi yaklaşım, entegre mikro-akışkanlar kullanımıyla yakın zamanda gösterilmiştir [1]. Ancak bu tür yaklaşımlar, pahalı ve karmaşık üretim yöntemleri içeren geleneksel litografi teknikleriyle üretilmiş yüzey mikro-kanalları içermektedir. Ayrıca bu yöntemler, mikro-akışkan kanalların erişiminin zor olacağı yongadaki tüm sıcak bölgelerin soğutulmasına etki etmeyebilir.

Bu çalışmada, silisyumun içerisinde, istenilen derinlikte, çok katmanlı mikro kanallar oluşturulması için lazer tabanlı bir mikro üretim yaklaşımı öneriyoruz. Ayrıca bu yöntem, yonga üstü elemanların entegrasyonu için yonga üst yüzeyinin optik kalitesinin korunmasını da sağlamaktadır. Silisyum yongalarının lazerle üç boyutlu şekillendirme konseptinin kanıtı daha önce gösterilmiştir [2]. Burada bu yaklaşımdan yararlanıyoruz ve silisyumun derinliklerinde doğrusal olmayan lazer yazımını ve yazılmış bölgelerin seçici kimyasal aşındırılmasını içeren iki aşamalı bir yöntem kullanmaktayız. Şu ana kadar ilk kez üretilmiş, yongaya tamamen gömülü ve çok katmanlı mikro-kanal serilerini, kavisli geometrileri ve gelişmiş mimari kontrolünü sunmaktayız. Yonga-içi mikro-kanalları 25'e varan yüksek bir

en-boy oranı ile üretmekteyiz. Yapıların ölçeklendirilebilirliğini, üretilen yapıların boyutlarını ve kullanılan lazer yazım modalitesindeki değişebilirliği inceliyoruz; seçici aşındırma oranlarını karakterize ediyoruz ve foto-dirençli kaplamalardan yararlanarak yonga yüzeyinin korumasını sağlıyoruz [3]. Desenlendirilmiş ışık demetleri kullanarak düşük duvar pürüzlülüğü (0.23 µm) hakkındaki ilk sonuçlarımızı sunuyoruz ve dikey mikro kanallar, yani "silisyum boyu kanallar" üretimini gösteriyoruz. Yonga yüzeyi hasar görmemiş olarak üretilen bu çok katmanlı kanal mimarisi, entegre sistemlerin ısı yönetimi için kullanımı açısından önemli bir potansiyele sahiptir.

Anahtar sözcükler: lazer mikro/nano litografi, 3B lazer yazım, doğrudan yazım, doğrusal olmayan soğrulma, çıkarmalı üretim, mikro-kanallar, yonga-içi sistemler.

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Chapter 1

Introduction

Due to their numerous applications, microchannels have been attracting the interest of scientists and engineers for more than two decades [1, 5–11]. The applications of the field cover a broad spectrum, such as medical devices [12, 13], microfluidic and optofluidic systems [9], as well as advanced integration involving photonics [14] and electronics [1, 15]. Microfluidic technologies are commonly employed in medical applications, such as cell sorting/mixing [16], cancer studies [17], electrolyte flow [18], DNA analysis [19], and lab-chip systems [20]. Fabrication techniques of micro-channels are generally based on lithography or 3D printing methods. An important fabrication direction is based on direct-laser micro-structuring approaches [2, 21–23]. In such methods, a transparent material is first irradiated with a laser, followed by selective chemical removal of the modified sections. The microchannels may need to be on the surface and/or sub-surface (that is buried in the bulk of the material) [22]. Due to such diverse requirements of different systems, novel multi-dimensional fabrication techniques are highly desired, and unique solutions are emerging (*e.g.*, Kotz *et al.*, Nature, 544, 337, 2017) [24].

While fabrication methods exist for microchannels in various scientifically and technologically critical materials such as glass [22], there has been no demonstration of buried microchannels inside the bulk of silicon with full control. *In*

this thesis, we will introduce such a method, enabling multi-layered fabrication of microchannels in Si, while preserving the wafer surface. Such channels may provide a potential solution for the notorious heat removal problem of electronics and other integrated systems, among other applications [3].

We will begin by discussing the main motivation behind our work. This will be followed by a detailed literature review of microchannel fabrication techniques, including a discussion of their limitations. The emphasis will be on the lithography techniques for transparent materials. We will review the state-of-the-art fabrication techniques for Si. Then, we will introduce our method to overcome the lithographic limitations of the previously developed techniques, enabling microchannels created in *different 3D sizes, geometries, and architectures.* Notably, we will show that the surface of the wafer is unaltered after the process, thus potentially allowing a CMOS-compatible method, constituting a powerful basis for future integration of on-chip and in-chip systems.

1.1 Motivation

Semiconductors have > \$500 billion/year market share, without even considering their various applications, such as online trade. Thus, silicon is one of the most critical elements for technology, if not the most critical. As a material, it is abundant in nature and therefore it is a low-cost semiconductor. Unlike other materials such as fused silica or yttrium aluminum garnet (YAG), Si is compatible with the CMOS (complementary metal oxide semiconductor) process, which is the established fabrication process used in the electronics industry. These constitute an ideal material with diverse applications, manageable costs and significant opportunities for further integration with other technologies, such as photonics and microfluidics.

An exciting recent advance illustrates the potential of integration between microfluidics and electronics. Erp *et al.*, exploited microchannels on silicon surface

using conventional lithography techniques and integrated them to a gallium nitride (GaN) power-electronics system [1]. In essence, a cooling fluid is passed through the microchannels created on the surface of Si, which in turn removes the heat generated at the GaN layer, in particular at the hot spots (*Nature*, 2020). Their results reveal that liquid-cooled systems can be far more efficient than air-cooled systems. This allows to reach much higher powers, to a regime that would not have been possible due to the heat removal problem.

In the future, one may imagine an analogous technology created purely for CMOS-based Si-electronics. While the preceding approach may be applicable for Si chips, a much more direct approach would present itself, if the channels could be created directly at the desired locations within the chip, without altering the wafer surface. *However, to date, the capability of fabricating fully-buried microchannels inside silicon with high control does not exist.*

The focus of this Thesis is to establish a laser-based fabrication method for creating such in-chip microchannels, with high control, rich geometries and in various architectures. We envision that our work will be an enabling technology, leading to exciting applications in multiple fields. Once the channels are available, it is a direct logical extension to integrate surface systems (on-chip) with subsurface networks (in-chip). Thus, an exciting future goal would be to exploit in-chip microfluidics integrated to on-chip Si-based electronics, geared towards efficient chip cooling [1, 2, 25].

1.2 Fabrication methods of micro-channels - an overview

In this section, we will overview previous fabrication techniques and their limitations.

1.2.1 Conventional microchannel fabrication approaches (including in other materials)

In order to fabricate microchannels, conventional lithography or laser exposure-based ablation have been employed.

Conventional lithography was broadly used in three distinctive approaches in order to fabricate microchannels, (i) photolithography, (ii) deep reactive ion etching, and (iii) focused ion beam milling. Photolithography is a frequently used technique where material is coated with a photo-sensitive resist, followed by patterning with light exposure. A mask is used to pattern the resist. The resist helps in the directional etching of material to fabricate channels on the sample's surface. However, photolithography results in non-uniform etching at the vertical walls when fabricating high-aspect-ratio trenches. A mask-less photolithography technique was also introduced to simplify the process [26]. The second approach is deep reactive ion etching (DRIE) or the Bosch process [27]. This is an anisotropic dry etching method where a time-multiplex alternative protective coating is applied to the trench walls for fabricating smooth and vertical high aspect ratio trenches. Similarly, a focused ion beam is another approach, which can create high aspect ratio trenches with a nanometric resolution at the cross-section [28]. Despite the capability, all of these conventional lithography techniques are hard-to-implement, extremely time-consuming, and expensive [1, 29].

In contrast, direct-laser writing based ablation is a single step method [30–32]. It does not require complex and inefficient steps of designing and aligning a photoresist mask. Instead, it uses a pulsed laser to directly ablate the material at the focal point. As a result, the ablation of material with a pulsed laser is a viable option for addressing the drawbacks of traditional lithography techniques.

Nevertheless, conventional lithography techniques and ablation via direct laser exposure are not capable of penetrating the sub-surface and are strictly limited to fabricating surface microchannels. Large volume coverage is another significant challenge for these methods.

On the other hand, various techniques have been employed in literature to successfully demonstrate the fabrication of microchannels buried inside transparent materials, such as glass [24, 33–35]. A recent novel technique creates microchannels in fused silica by using a sacrificial template submerged in amorphous silicon-dioxide nanocomposites. Next, a combination of thermal debinding and sintering causes the polymerization of glass nanocomposites, turning them into a crystalline glass. During the process, the sacrificial template escapes in the form of gas to give arbitrary 3D smooth-walled microchannels inside fused silica [24].

However, the aforementioned techniques are either restricted to surface fabrication or are material specific. They cannot be directly implemented for subsurface channel fabrication in Si.

1.2.2 Laser fabrication of micro-channels inside transparent materials

An exciting direction for this aim is to exploit direct laser writing of transparent materials, in particular using laser-assisted chemical etching [36]. This has been successfully implemented in other materials. For instance, a femtosecond laser-assisted selective chemical etching of transparent materials, such as glass, yttrium aluminum garnet (YAG), and sapphire, is a well-known technique for its capability to create any 3D structure [36–39]. The advent of subsurface laser modifications in transparent materials to create sub-surface waveguides became a stepping stone in fabricating microchannels [40]. Y. Bellouard et al. demonstrated that laser-modified regions are susceptible to having a higher etching rate, leading to the development of sub-surface microchannels in glass [39]. These channels were used as micromixers in various biological and chemical applications. Consequently, He. S. et al. demonstrated the fabrication of arbitrary long and uniform 3D microchannels in the bulk of fused silica [41]. This was achieved by introducing excess ports for the etchant. In order to make these channels uniform, the laser power was varied (low power near the ports and vice versa). To date, numerous studies have been directed towards understanding and improving

this technique [42]. By modifying the laser writing parameters and/or optimizing the etchant recipe, the selectivity of this method was significantly improved [43]. For instance, temporal beam shaping [44], modulating pulse energy and duration, controlling polarization [45], employing two-pulse bursts [46, 47] and using KOH instead of HF as the etchant, have all proven successful [45].

Similarly, a recent effort demonstrated exceptionally high selective etching of laser-written structures in order to build high-quality nanoscale channels in YAG and sapphire [48]. The significant selectivity value, which is close to 5 orders of magnitude higher than any previously recorded selectivity value in any material, was an enabling factor.

While ultrafast laser-assisted chemical etching has been successful in creating such channels in the bulk of glass materials, highly-controlled microchannel fabrication in Si will likely enable new applications due to semiconductor properties of silicon.

1.2.3 State-of-the-art laser-written microchannels on the silicon surface

As discussed earlier, conventional lithography techniques and ablation with pulsed lasers are possible for creating Si surface channels. Subsequently, attempts to create sub-surface modifications inside Si, similar to those created in glass, were unsuccessful until a few years ago. Tokel *et al.* introduced a novel fabrication approach enabling in-chip microstructures leading to unique applications including gratings, lenses, waveguides, holograms, and optical data storage [2]. This state-of-the-art laser lithography technique achieved 3D microstructures with high-aspect-ratio buried in the bulk of silicon. In essence, a non-linear feedback mechanism enabled in-chip laser-sculpting. This was achieved by focusing the Gaussian beam and reflecting it from the back surface of the sample. This initiates a feedback mechanism between self-focusing and plasma shielding. The resulting subsurface structures had unique material properties and refractive index, which

can be used as building blocks for 3D functionalities.

As an optional second step, a selective chemical etching recipe was introduced, enabling the creation of unique structures [2]. The current work is based on such an approach, where laser-sculpting in conjunction with chemical etching is used in order to fabricate multi-layered sub-surface microchannels deep inside silicon, without altering the wafer surface. We believe this unique capability will be the basis for future applications, including thermal management of chips.

1.3 Understanding light-material interaction

Light-material interaction on the surface of a material differs from the interaction inside its bulk [49]. The basic concept behind laser-writing inside materials is to take advantage of the laser's non-linear interactions within the material. Such nonlinear interactions induce localized modification at the focus of laser. Since these crystal modifications have distinct optical properties, such as refractive index, they can later be used in the fabrication of optical devices.

A material's transparency window is determined by its electronic bandgap. When light with a specific wavelength is incident on a material, the absorption of a photon causes electronic excitations. If the photon has less energy than the electronic bandgap of the material, no optical absorption occurs, and the material is said to be transparent at that wavelength. In order to absorb photons and create modifications, non-linear interactions are required, which can only be achieved at higher intensities and tight focusing conditions [49]. At high intensities, non-linear phenomena such as two-photon absorption and/or multi-photon absorption become available. Other relevant phenomena are resulting thermal accumulation and avalanche ionization. A single laser pulse may not be enough to create modifications, but a high repetition-rate laser can cause local heat accumulation with beam collapse, resulting in permanent material modification.

At the same time, plasma formation results in delocalization of the focused light, which may even block modification at the focus. Despite delocalization due to plasma formation, self-focusing may overcome this effect at high intensities, inducing subsurface modifications [50, 51]. All the complex phenomena occur concurrently, critically depending on laser and focusing conditions, including wavelength, energy and repetition rate. At a specific regime, one can achieve crystal disruptions with refractive index change, enabling localized subsurface control of material properties.

Studies indicate that silicon has a transparent window, from a wavelength $>$ 1.2 µm, ideally in the infrared regime [49]. Thus, we will use a laser at 1.5 µm, with low losses due to absorption, and ideal non-linear response at the given wavelength.

In the next section we will introduce and exploit the *laser-sculpting fabrication technique* for creating, to the best of our knowledge, the first fully buried microchannel inside silicon sample. This technique, along with *passivation steps*, will ensure that the optical quality of the sample's surface is preserved for future integration of on-chip elements.

Chapter 2

Methodology

In this thesis, we are proposing a fabrication method to create *fully buried* microchannels in the bulk of silicon while preserving the device-level quality of top wafer surface. For this purpose, we will leverage state-of-the-art laser-sculpting technique that resulted in the formation of surface microchannels. By overcoming current limitations, we will create, for the first time, sub-surface microchannels in silicon. Further, we will fabricate through-silicon vias (TSVs), from the top to the bottom surface of the wafer, without requiring any additional steps, such as polishing.

2.1 Two-step fabrication approach for subsurface microchannels

We employ a two-step fabrication method. Step one entails non-linear laser writing process to induce subsurface permanent modifications deep inside silicon. This is followed by the second step, which involves selective etching of the laser-written structures with a chemical etchant. Figure 2.1 shows the schematic of the entire process. This approach enables us to demonstrate the first sub-surface microchannels in Si, with the capability of controlling their depth, cross-sectional

geometry, and aspect ratio. The inner channel walls will also be of high quality.

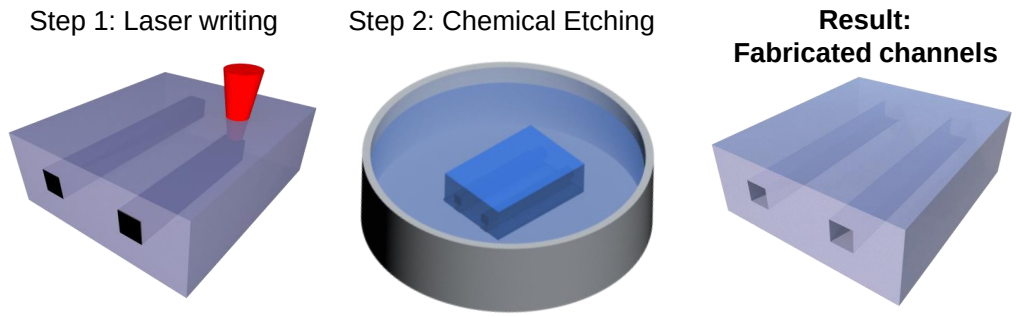

Figure 2.1: The concept of in-chip microchannel fabrication approach. The process involves two steps, (i) laser writing of permanent modifications deep inside Si wafer, and (ii) selective chemical etching in order to create the fully buried channels.

2.1.1 Step 1: Laser writing inside silicon

The laser setup for writing sub-surface modifications in the bulk of silicon is shown in Figure 2.2. The light source in our setup is a master oscillator power amplifier system (MOPA) that operates in the transparency window of Si. It is a custom-built nanosecond laser operating at a wavelength at 1550 nm, a repetition rate of 150 kHz, and a pulse duration of 10 ns [2]. The laser is capable of producing a maximum output of 6 W. The beam output has a profile of a gaussian beam.

The output from the laser is passed through a quarter-wave plate (QWP) and half-wave plate (HWP) to control its power. This is followed by a polarized beam splitter to transmit only the p-polarized light. In our setup, we have a spatial light modulator (SLM) to control and modulate the shape or the phase profile of the beam. Before the beam is projected onto the SLM, it is passed through a pair of lenses, serving as a telescope, to collimate and expand the beam. The lenses L1 and L2 have focal lengths of f1 = 15 mm and f2 = 35 mm. The beam is then projected and reflected through the liquid crystal on the silicon SLM with 792 $\times$ 600 pixels and 20 µm pixel size. The SLM modulates the phase profile

of the beam. For most of the work, we use a Gaussian beam for laser writing. Therefore, SLM only works as a mirror mainly, however we will show some early results from the use of SLM in the later chapters, in particular for controlling channel aspect ratios.

Before the beam is passed through the last focusing lens, its diameter needs to be adjusted according to the aperture of the aspheric focusing lens. Therefore, a 4f system is used to de-magnify the beam (f3 =125 mm, f4 = 100 mm). The focusing aspheric lens (AFL) has a focal length of 4.5 mm. The AFL directly focuses the beam into the bulk of the Si sample, where it induces a highly non-linear effect at the focal point, resulting in the localized material change. This is because the modifications cause stress/strain effects, deforming the crystal structure of Si. The beam width at the focal point is 3 µm at $1/e^2$ of maximum .

In order to scan the sample with respect to the laser, it is mounted on a precise 3D positioning stage (Aerotech), with a resolution on the order of nanometers. The stage is controlled with a computer code, which is capable of creating almost any complex 3D shape, and consequently laser-written structures.

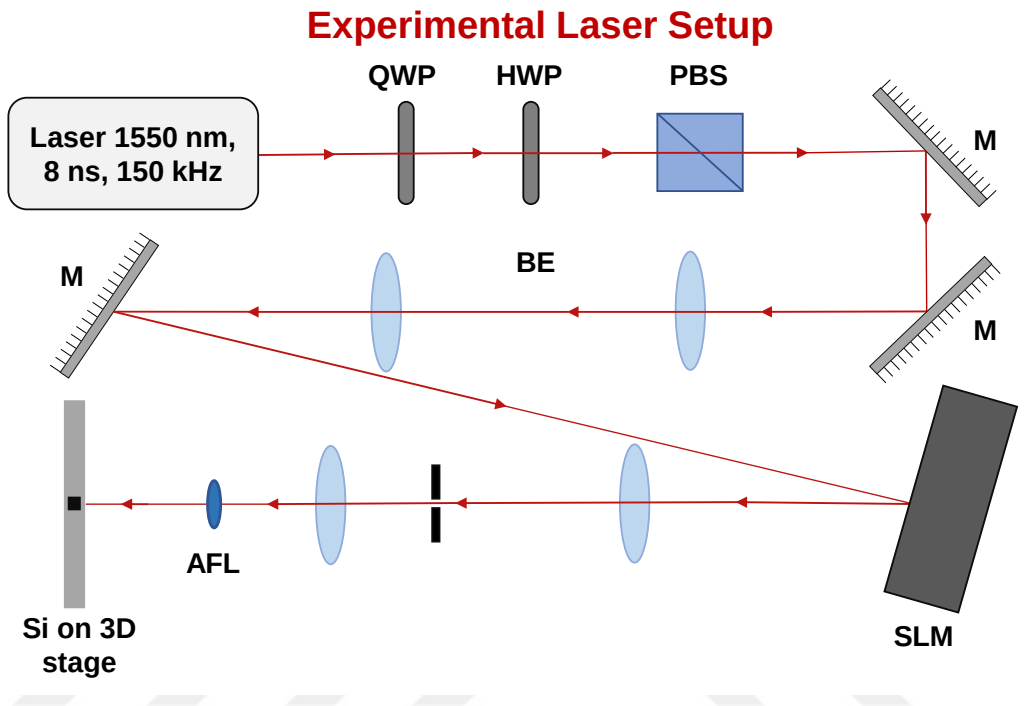

Figure 2.2: Schematic of the experimental setup for laser writing in silicon.

Writing modality: Conventionally there are two modes for three-dimensional laser writing; transverse writing modality and longitudinal writing modality. In the transverse mode, the laser scanning direction is perpendicular to its propagation direction. In the longitudinal mode, laser is scanned parallel to its propagation direction. Figure 2.3 illustrates these, where the z-axis is chosen as the laser propagation direction.

Each mode has its benefits and drawbacks. For instance, while the transverse mode allows writing structures of any arbitrary lengths simply by scanning, the longitudinal mode affords better control on cross-sectional geometry and cross-sectional dimension. However, in longitudinal writing, the length of subsurface structures is limited by the focal length of the aspheric focusing lens.

We will further discuss the use of these modes in the Results section. The written parts will then be used as building blocks for numerous microchannel architectures.

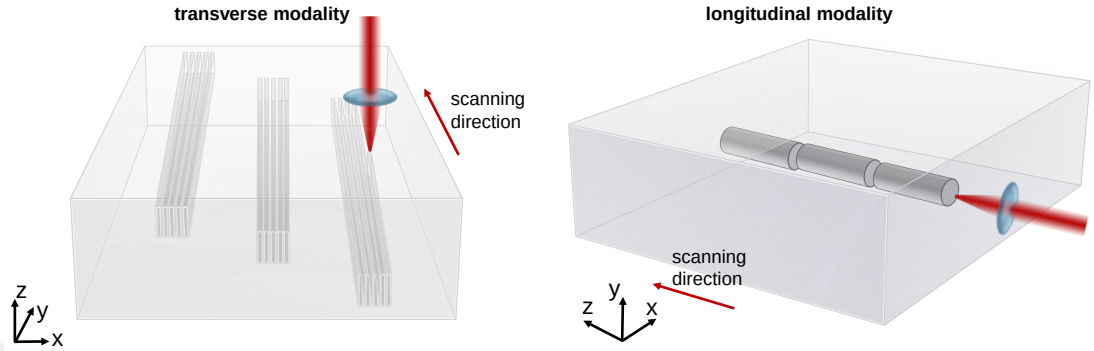

Figure 2.3: A schematic representing the two laser-writing modalities: (a) Transverse writing modality where the laser scans perpendicular to the propagation direction. (b) Longitudinal writing modality in which the laser propagation is parallel to laser scanning direction.

2.1.2 Step 2: Selective etching of laser modified regions inside Si

Once we create the laser-written modifications inside Si, the next step is to selectively remove them, in order to create a fully-buried microchannel or a TSV. As mentioned in the light-material interaction section, areas exposed to multi-photon absorption experience a crystal disruption. Hence, an ideal etchant in our case would be the one that selectively attacks only disrupted regions and leave the crystalline silicon unaffected. Such a selective chemical etchant recipe was previously devised by our group [2]. It includes a combination of chemicals that simultaneously work together in order to perform the desired etching task. Tokel *et al.* previously used this process to reveal laser-written architectures in Si, that are exposed to the surface with polishing.

The etchant composes of a mixture of the chemicals below and their compositions in the following sequence: copper II nitrate ($Cu(NO_3)_2$): 0.05 M (3 gr.), hydrofluoric acid (HF): 10 M (36 ml.), nitric acid (HNO_3): 4 M (25 ml.), and acetic acid (CH_3COOH): 3.5 M (24 ml.).The process of etching involves oxidizing

and subsequently dissolving the laser-irradiated regions. Each chemical performs a certain function. For instance, HNO_3 is used as an oxidizing agent, HF removes the oxidized areas, $Cu(NO_3)_2$ reduces the activation energy of the process, thereby increasing the selectivity, and CH_3COOH is used as a diluting agent. We provide the details of the etching protocol in Appendix A.

The mixture is carefully prepared in the cleanroom on a wet bench, designated for this purpose. While preparing the etchant, all safety precautions are taken with respect to the material safety data sheet (MSDS) of each chemical used in the process.

2.2 Sample preparation

Before conducting an experiment or analyzing a sample, we follow the following protocols and techniques to prepare the sample for imaging and to protect the sample quality through passivation.

2.2.1 Sample type

Mainly, two different types of samples were employed with a difference in their crystallographic orientation and resistivity. A 1-mm thick p-doped <100> type silicon sample with a resistivity of 1-10 Ω.cm and a 1-mm thick p-doped <111> type Si sample with a resistivity of 1-10 Ω.cm. For Gaussian beam and transverse writing modality experiments, p <111> samples were mostly employed. Similarly, for longitudinal modality, Bessel written structures, p <100> side-polished samples were used. The selection of sample type for any experiment was based on input from previous work. We observed no discernible difference in the results between the two types of samples. Similarly, the thickness of the sample is not strictly limited to 1 mm for our technique.

2.2.2 Sample preparation before etching: Dicing

The sub-surface laser modifications are fully buried in three-dimensions. It is a simple yet crucial step to expose these modifications from the sides to make way for the etchant. For this purpose, DISCO DAD3220 dicing machine is used to dice and open the two end ports of the microchannel before it is dipped into the chemical etchant. Similarly, dicing is further employed for cutting a Si wafer into smaller chips to fit on the 3D stage for laser writing.

After dicing, samples are carefully cleaned to remove any organic or inorganic impurities that may have been deposited over the sample. We used Acetone, Isopropanol, and de-ionized water in sequence and washed the sample in an ultrasonic bath for a total of 15 minutes. The sample is then dried with nitrogen gas. This cleaning procedure is strictly followed before laser-writing and chemical etching steps to avoid any contamination.

2.2.3 Sample preparation before etching: Photo-resist passivation

The aim of fabricating state-of-the-art in-chip microchannels requires the top wafer surface to remain unaltered for future integration of on-chip systems. Therefore, in order to avoid any damage to the sample surface, a systematic study of different photoresist (PR) coating was conducted. A pipette was used to coat the photoresist, to allow a thick protective layer to be deposited. Then PR was hard baked at 120°C for 5 minutes. The PR was successful in preserving the sample surface for at least 75 minutes. In order to fabricate microchannels that require longer etching periods, a time-multiplexed alternative process of coating and etching was employed [52]. The sample was etched with photoresist for 75 mins, after which it removed from the etchant and then coated again before dipping it into the etchant again. These steps are followed recursively for protection of samples which require longer etching time.

2.2.4 Sample preparation before imaging: Polishing

Polishing plays an important role in the imaging of in-chip, curved structures as it is technically impossible to image a buried and curved channel with dicing. Hence, we perform chemical mechanical polishing (CMP) to polish the top surface of the sample. We used an Allied-Multiprep polisher along with a combination of diamond polishing lapping, with different grid sizes.

A polishing protocol was used, which provided an optimized speed and the amount of material to be removed by each lapping in the sequence summarized in Table 2.1. For instance, if only smooth polishing is required, then the last few lapping with smaller grid sizes are used. The number of lappings to be used is decided in reverse order, from bottom to top, depending on the amount of material needed to be removed. Other parameters, such as time and pressure on the sample are adjusted according to the required depth and quality of polishing.

Initially, the sample is mounted to a metal plate with glue that melts on heating. The metal plate is attached in an upside-down manner to the holder above the rotating disk. The sample is then slowly moved closer to the rotating disk on which the lapping is placed. The water is kept running throughout the process and the change in sample thickness is recorded after each major step. We start with larger grid lappings for hard polishing and follow the protocol to reach smaller grid lappings for finer polishing. For extra-fine polishing silica-colloidal particles are used as the last step. The CMP may take up to a few hours, depending on the amount of polishing required. Therefore, channel architecture and design is carefully considered to minimize the polishing time.

2.3 Imaging and characterization methods

We use various 3D imaging methods for surface and sub-surface characterization. For sub-surface laser-written modifications, we use an infrared transmission

Lapping grid size (µm)	Speed (RPM)	Material to be removed (µm)
50	200	100 or above
15	150	90
6	100	45
3	50	18
1	30	9

Table 2.1: Parameters for performing chemical mechanical polishing.

microscope (ITM) to characterize their quality and dimensions. For surface measurements, such as imaging the cross-section of microchannel, a scanning electron microscope (SEM) is used. Similarly, to characterize the overall surface morphology of the microchannel inner wall, as well as the wafer surface quality of Si after fabrication, optical profilometer device (OPD), Scanning laser microscope (SLM), and Energy dispersive x-ray spectroscopy (EDXS) are employed. In the next part, we summarize the use of these techniques in our experiments.

2.3.1 Infrared transmission microscopy

Since laser-written structures are positioned such as to be completely buried inside the wafer, we use a transmission mode home-made infrared light microscope to characterize them. The sample is placed under a halogen tungsten lamp, providing infrared light. The transmitted near-infrared light is then collected with an objective lens, which is sent to a highly-sensitive CMOS camera (Thorlabs). The final data is transmitted to a computer, where it is recorded and analyzed.

Depending on the size of structures, 20 X and 50 X objectives were used interchangeably providing different magnifications. The position of sample is controlled with a two-dimensional translation stage and the focus of the sample is adjusted manually with a 1-D translation stage. The recorded images are used to evaluate the quality of structures, dimensions of the microchannels, and any discontinuities or discrepancies in their fabrication.

The infrared transmission microscope image in Figure 2.4 shows thin planes of modifications stacked together to make up a microchannel. Such images prove to be crucial in optimizing laser parameters for the fabrication of uniform and structurally stable microchannels. Further, the infrared transmission microscope is used for analyzing the chemical etching rates (Section 3.2).

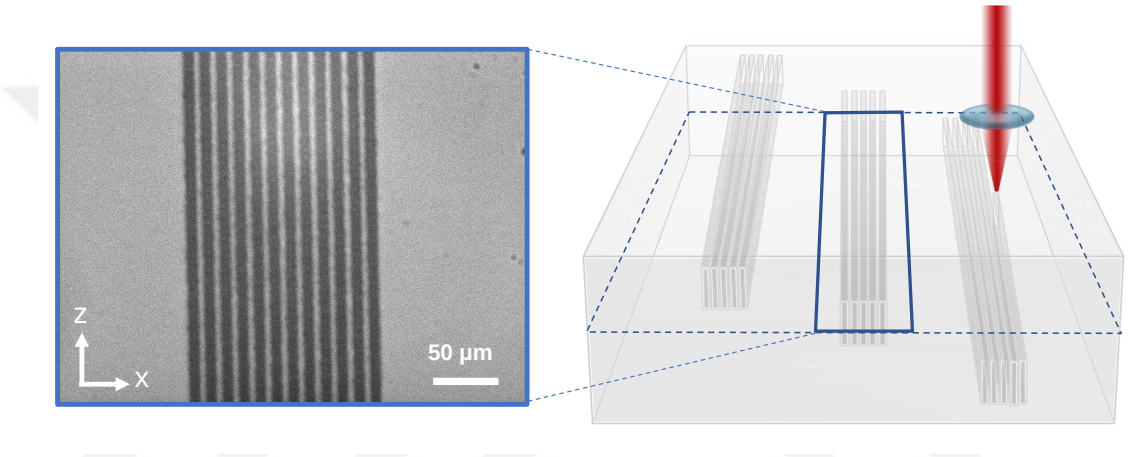

Figure 2.4: Infrared transmission microscope image of a laser-written microchannel is shown on the left. The schematic on the right illustrates the 3D geometry. These subsurface thin planes are used as building blocks for numerous types of in-chip microchannels.

2.3.2 Scanning electron microscopy

For surface imaging and analysis of the fabricated microchannels, a scanning electron microscope (SEM) is used. SEM uses electrons reflected from the surface to create an image of the surface. The method was instrumental in characterizing the channels and provided essential input for optimizations. For instance, Figure 2.5 shows an SEM image of an unsuccessful attempt to fabricate a sub-surface, end-to-end opened microchannel, imaged at the cross-section of a 1mm thick Si sample. The image also gives information regarding the shape and dimensions of the cross-section. In addition, to visualize the curved structures fabricated in Si, the top surface of the sample is polished until the structures are reached. Then SEM is used to show the curved geometry of the channel, along its length.

Overall, due to its high resolution and sensitivity, SEM is the preferred technique for surface imaging of laser-written architectures.

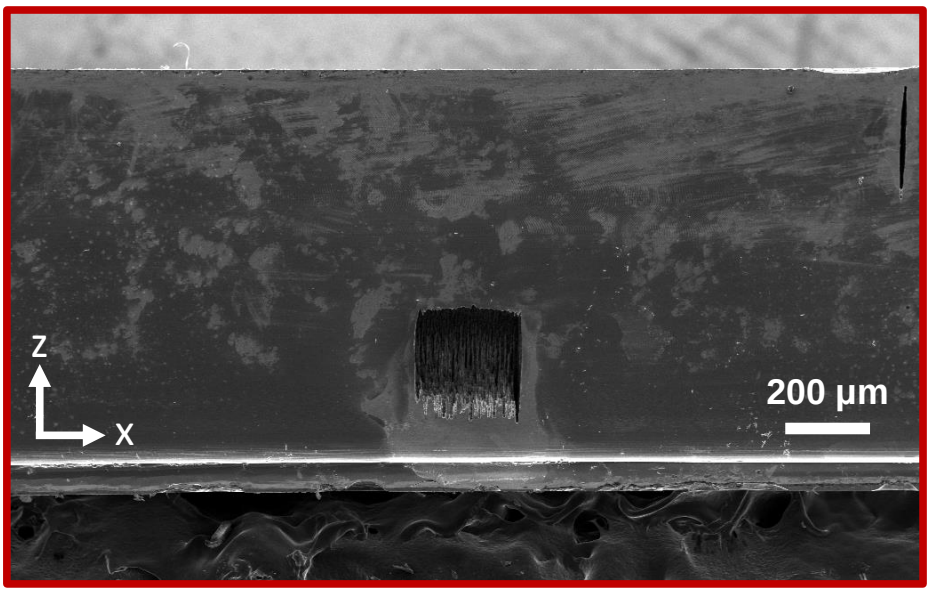

Figure 2.5: SEM image of a cross-section of a microchannel fabricated in 1-mm thick Si sample.

2.3.3 Confocal laser scanning microscopy

We found that the roughness of the microchannel's inner walls is on the order of micrometers. An appropriate method to analyze such structures is found to be confocal laser scanning microscopy (CLSM). The microscope measures surface structures > 5 nm in the axial direction. It uses stepwise signal collection at the focal volume, rejecting out-of-focus light, and then reconstructs a 3D image by joining these signals at each focal volume. This allows us to have a precise 3D image of deep trenches, valleys, or peaks on inner channel surface.

We employ Keyence VKX 100 CLSM for measuring the channel inner wall profile. Figure 2.6 shows a 3D color map of the inner walls of a sample microchannel. Different channel roughness values may be required for different applications, and

CLSM is critical for such optimizations.

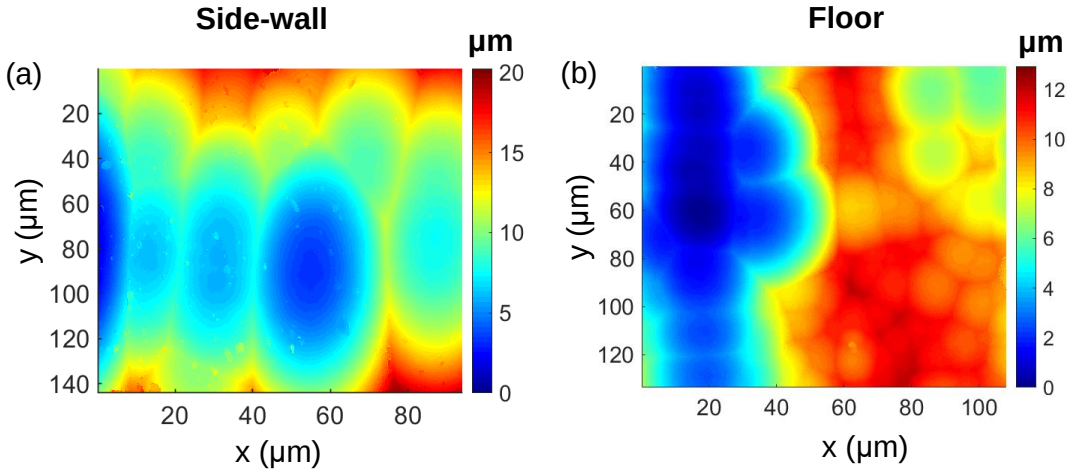

Figure 2.6: Representative laser scanning microscopy images of inner walls of in-chip microchannels. The roughness pattern on the (a) side wall varies from the (b) top and bottom surfaces due to the different orientations of laser written structures in the two dimensions.

2.3.4 Optical profilometer

After fabrication is complete, we evaluate the wafer surface damage, if any, due to the developed fabrication method. For this purpose, we use Zygo NewView™ 7000 optical profilometer device (OPD) to characterize the top wafer surface quality. OPD is a non-contact optical device for the measurement of surface profiles at high precision. It measures the elevation with an axial precision as high as < 1 nm. The final image provides a topography of the surface with the lateral area and lateral resolution depending on the objective lens, available between 5 X to 100 X.

In order to check the sensitivity and calibration of the device, we image pristine Si where the roughness measurement turned out to be reasonable. The tool allows us to evaluate any potential; surface alteration after each step of fabrication i.e., after laser writing and chemical etching steps. For instance, the profile

measurement of a damaged surface is shown in Figure 2.7. With input from such data, one can develop strategies for improved surface quality.

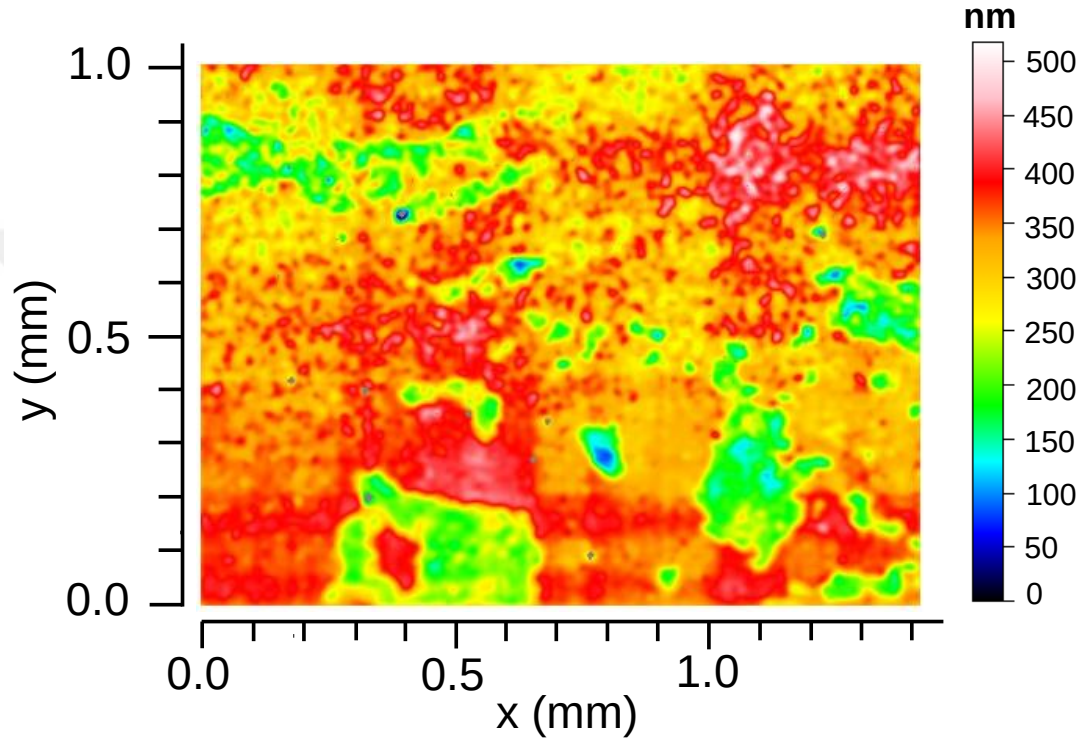

Figure 2.7: The use of optical profilometer for evaluating any surface damage after etching. An undamaged surface would have been within a few nm range (blue color range in the side bar).

2.3.5 Energy dispersive x-ray spectroscopy

In order to better evaluate the chemical structure of sample surface, energy dispersive x-ray spectroscopy (EDXS) is exploited. EDXS requires scanning the sample under a focused beam of electrons in vacuum, and uses the available SEM vacuum chamber. EDXS measures the X-ray response of material under an electron beam, to distinguish the chemical elements on the surface. This helps in measuring the change in the chemical morphology of the sample after fabrication.

We test the sensitivity of the device by recording EDAX measurements of

pristine Si and a Si sample coated with a 10 nm thin layer of gold (Figure 2.8). Even 10-nm thin Au coating is clearly visible, thus any potential contaminants from coatings/etchants is also expected to be measurable.

Thus, EDAX is considered to be a strong tool for surface structure evaluation measurements.

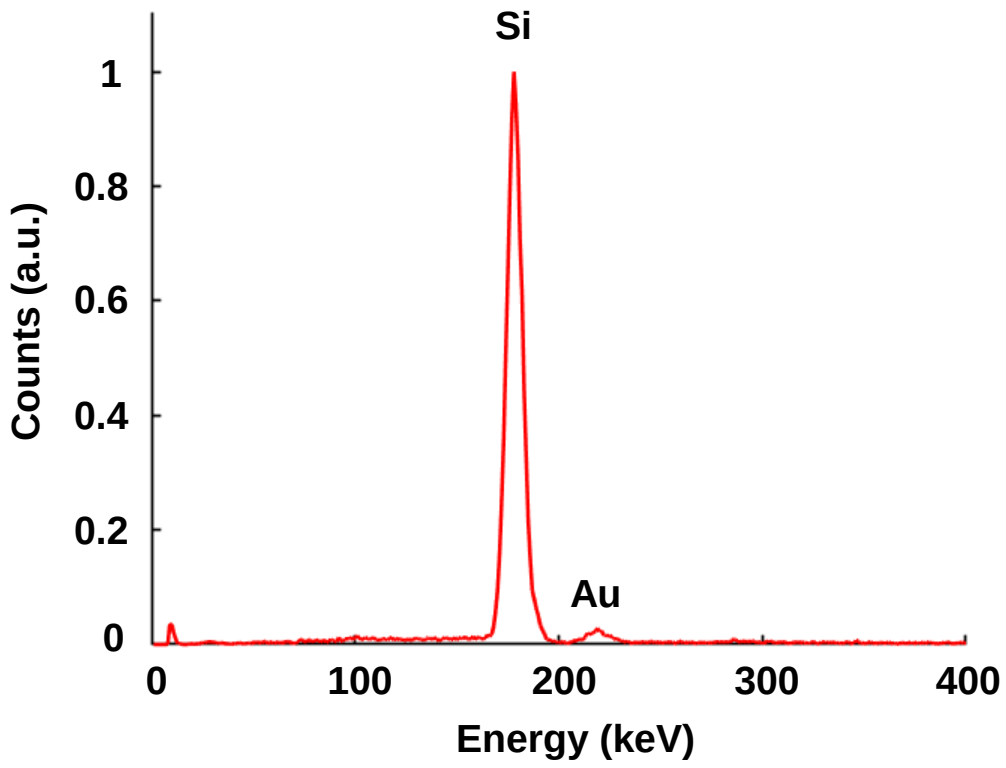

Figure 2.8: Energy dispersive x-ray spectroscopy of Si test sample, coated with 10-nm gold. The measurement establishes the sensitivity of the device, as the thin Au coating is clearly visible.

In order to ensure that the preceding imaging techniques are accurate we performed controlled experiments before taking measurements, and confirmed their reproducibility. In the next section, we start providing our results based on the methods described here.

Chapter 3

Results and Discussion

Here we examine the fabrication of in-chip microchannels and provide detailed experimental parameters for creating various 2D and 2.5D channel architectures, while preserving the optical quality of the top wafer surface. We follow the methodology given in Chapter 2.

We begin by exploring the use of Gaussian-type laser beams for creating subsurface channels and outlining the main challenges faced during microchannel fabrication. The challenges are overcome by systematic controlled experiments, which include optimizing etching rates for creating regular and reproducible arrays, as well as optimizing the laser-writing parameters for best inner channel wall roughness and wafer top surface quality. The approach enables the creation of multi-layer channels and high-quality through-silicon vias (TSVs). We further show preliminary data for creating high-aspect-ratio microchannels by using spatially-modulated laser beams.

3.1 In-chip microchannels written with a pulsed Gaussian laser beam

Here, we demonstrate a fully-buried microchannel with depth control for the first time in Si. The laser-written modifications are etched with selective chemical etching to reveal the channels. Figure 3.1a provides an infrared transmission microscope (ITM) image of a laser-written microchannel (top-view). After the chemical etching step, the channel is revealed from both ends. Figure 3.1b shows the SEM data for such a microchannel, imaged from its cross-sectional plane.

In the laser-writing step, we used a p-polarized Gaussian beam in transverse-writing mode, with a pulse energy (E_p) = 4.3 µJ. The channel was formed by laterally aligning thin laser-written planes with a separation of $\Lambda = 11$ µm (Figure 3.1a). The number of successive planes was chosen as 20, but can easily be increased affording strong size control. The sample was then etched for $\approx$ 2 hours to remove laser-modified regions. In this approach, crystal parts in between the planes are partly etched, and the remaining parts simply fall, increasing the effective (total) etching rate for the entire channel.

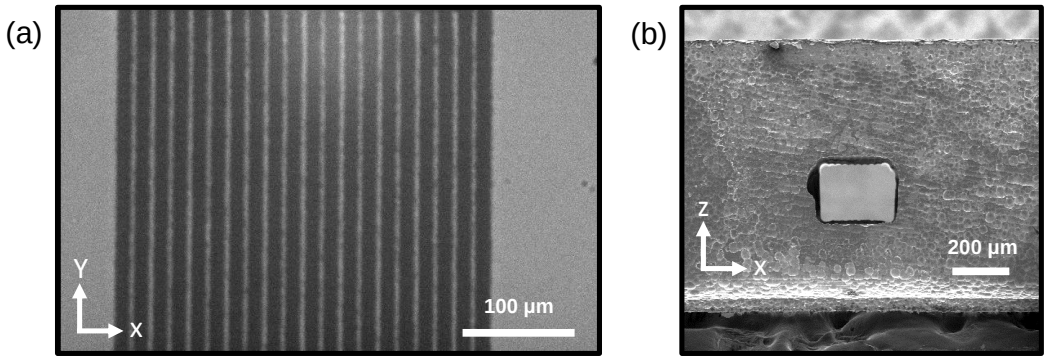

Figure 3.1: Fabrication of in-chip microchannels. (a) An infrared transmission microscope image from the x-y plane buried of planar arrays (y-z plane). The dark sections indicate modifications, the bright parts correspond to Si crystal. (b) SEM image of the first sub-surface microchannel in Si with depth control, created after chemical etching of the structure given in (a).

An important challenge for uniform channel fabrication was the observation of unwanted structural instabilities or cracks (Fig. 3.2). The cracks can propagate all the way from the channel edge to wafer surface. They occur due to two related forms of stress accumulation. The first one is due to pressure accumulation due to laser modification in a large bulk volume. The second is more related to channel geometry. In order to confirm the former, in-chip planes were created with 3 µm inter-wall separation ($\Lambda = 3\,\mu m$). ITM image confirms that the planes can be written extremely close (Figure 3.2a). However, after etching, SEM image shows that structural deformations emerge and extend to both wafer surfaces (Figure 3.2b). We found that the effect may be removed simply by increasing inter-wall separation (from $\Lambda = 3\,\mu m$ to $\Lambda = 10\,\mu m$, at $E_p = 4\,\mu J$ and p-polarized light), decreasing stored energy due to stress between modified sections (figure 3.2c).

The second form of instability is similar to the former, but related to geometry. We performed a series of experiments changing Λ from 3 µm to 12 µm, with $E_p = 4\,\mu J$. When $\Lambda = 10\,\mu m$, although the modifications are well separated from each other (Figure 3.2c); we still observe a crack after etching (Figure 3.2d). After carefully repeating similar experiments we observed that location of the crack always coincides with the first laser-written plane (at a specific energy range). This is ascribed to the stress induced between the first plane which forms the corner of the channel and the bulk of Si. We refer to this as the "inverse seeding effect", as each new laser-written modification induces pressure on previously created modification planes, in particular to the first.

We observed that increasing the number of planes increases the inverse seeding effect, which is ascribed to higher stress accumulation at the first plane due to creation of later planes.

This type of crack formation seems analogous to early problems in fabricating square windows for planes [53]. Plane fuselage have stress due to pressure difference between the cabin and outside atmosphere. The smooth flow of stress in a plane body is disrupted due to obstacles, such as windows. This results in stress concentrations at the window and cabin interface, mainly at the edges. This causes structural instabilities such as fatigue cracks, which had even caused

plane crashes back in 1950s [53].

The two stress challenges (planes windows and in-chip channels) can be solved in analogous ways; by either reducing the stress in general, or by allowing smooth flow of the same amount of stress and avoiding it from concentrating at sharp corners. In the case of a plane, the cabin pressure cannot be modulated much, so as to provide a livable environment for passengers. Hence, the issue was resolved by avoiding excessive stress concentration at sharp corners of windows by replacing them with oval windows. The change in shape allows the stress to smoothly flow at the interface [53].

In our case, we could have followed this path, but there might be some future application requiring rectangular or square channels, so we aimed to reduce the total stress. We achieved this by further increasing the inter-wall separation between modifications (from $\Lambda = 10\,\mu m$ to $\Lambda = 11\,\mu m$, at $E_p = 4\,\mu J$). This allows us to reduce the effect of stress concentration at the edges, providing a uniform rectangular cross-section (Figure 3.1a). This also allows an increase in the effective etching rate.

We note that increasing Λ indefinitely is not an option, as it would not be practical for very large values. As in any engineering problem, this is design criterion involving desired channel opening size and cross-sectional shape. For instance, increasing Λ above $10\,\mu m$ is illustrated in Fig. 3.3. Etching crystal Si between modifications leads to high roughness at the top and bottom walls of the channels. This is due to a considerable gap in the successive modifications, leaving the un-modified areas partially unetched. Hence, for an E_p range of 4 ± 0.5 µJ, the optimized Λ is $11\,\mu m$.

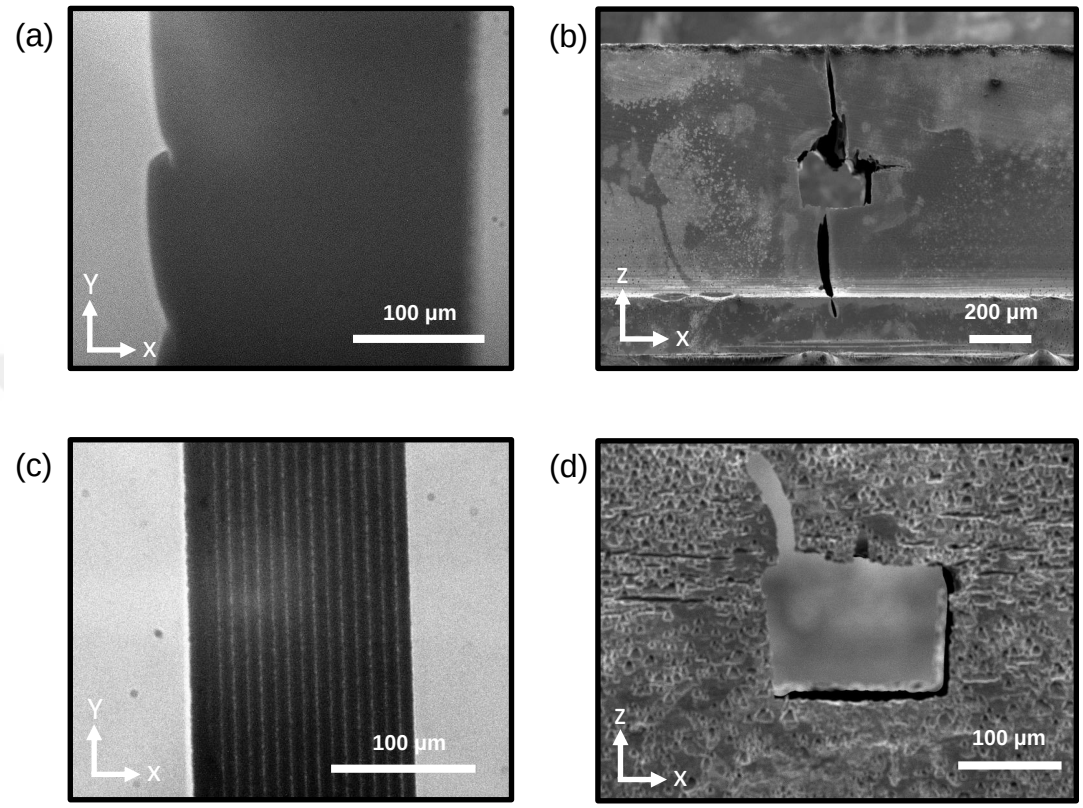

Figure 3.2: Unwanted structural instability and crack formation, propagating from the channel edge to sample surface. (a) ITM image of overlapped laser modifications in Si ($\Lambda = 3\,\mu m$). The dark modified part on the left show unevenness due to release of stress accumulation. (b) SEM image of the etched microchannel, laser written in (a). (c) ITM image of a microchannel with $\Lambda = 10\,\mu m$. The planes are well separated from each other; and do not show any unevenness between dark modified regions and crystal Si. (d) SEM image shows a crack in the microchannel near the first plane modification and the Si crystal interface, after etching the sample in (c). This crack is an indication of the presence of inverse seeding effect, where each successive modification non-locally induces a stress to the previously written modification. For the set of experiments, a p-polarized light and a E_p of $4\,\mu J$ was fixed.

We also note that pulse energy, E_p, has an effect on the thickness of modification planes. Therefore, a change in E_p has a small but noticeable effect on the

range of optimized Λ values. For instance, when Λ is 12 µm, the E_p is optimized for 3.5 – 4.5 µJ, however, for $\Lambda = 11$ µm, the pulse energy has an optimum range between 2.6 – 4 µJ. From experimental observations, we can safely conclude that for a specific Λ value, as long as the pulse energy is in the broad acceptable range, the microchannel will not experience a crack or high channel wall roughness.

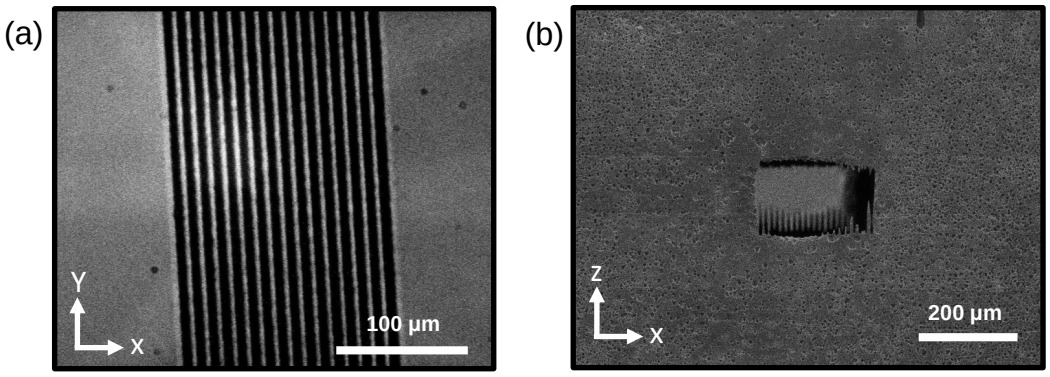

Figure 3.3: High roughness at the inner walls of a microchannel (a) An ITM of a microchannel with $\Lambda = 12$ µm and $E_p = 4$ µJ. (b) High inner wall roughness was observed in SEM image, after etching due to the modifications being at a distance.

After optimizing the laser parameters for uniformity of microchannels, we aimed depth control. We created straight microchannels at various depths in Si using the preceding parameters. The depth of the laser-written structures in Si can be estimated from the multiplication of the refractive index of Si ($n = 3.48$) and the translation of the laser in the air. Thus, a calculated translation of the laser focus allows us to place the structures at desired levels in Si. We created an array of 3 microchannels varied in depth (Figure 3.4). For these channels, the depth in Si was set as 220, 500, and 780 µm from left to right, respectively.

In the next section, we focus on increasing etching rates for increased through put.

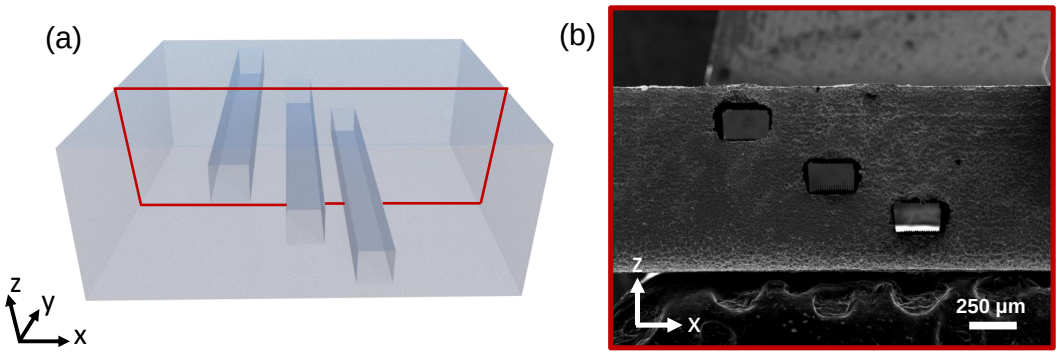

Figure 3.4: Depth control of channel arrays inside Si. (a) Schematic of multi-level microchannels (b) SEM image of the multi-level channel array. The laser writing parameters are as follows: $\Lambda = 12\,\mu m$ and $E_p = 4.3\,\mu J$.

3.2 Etching-rate analysis with respect to pulse energy and cross-sectional area

So far, we have demonstrated the fabrication of in-chip and multi-depth microchannels in Si. Another important parameter is fabrication throughput, which depends on etching rate. To achieve higher rates, we optimized it as a function of laser pulse energy and channel cross-sectional area.

We found that etching rate for a Gaussian-beam-written single-plane modification is 189 µm/h. However, a microchannel is different from a single plane, as it consists of multiple modification planes stacked (Fig. 3.2c), with un-modified crystal sections in between. Therefore, etching rate for a single line does not reflect the etching rate of a microchannel. Hence, we defined the "effective etching rate" of a microchannel as the length of a microchannel opened per unit time (µm/h).

We used infrared transmission microscopy to measure the effective etching rate. Fig. 3.5 illustrates this parameter as a function of pulse energy, obtained by opening channels from single side. All other operational parameters were kept

constant during the analysis as follows: $\Lambda = 11\,\mu m$, number of planes = 16, and etching time = 1.5 hours. From Fig. 3.5, we observed a linear increase in effective etching rate with increasing pulse energy. However, when we increase the pulse energy beyond a certain value, the stress-accumulation causes structural instability and cracks. This exact cut-off value for pulse energy depends on the separation between modifications (Λ).

In the sample case for $\Lambda = 11\,\mu m$, the cut-off pulse energy is around $4.3\,\mu J$, providing an effective etching rate as high as 680 µm/h.

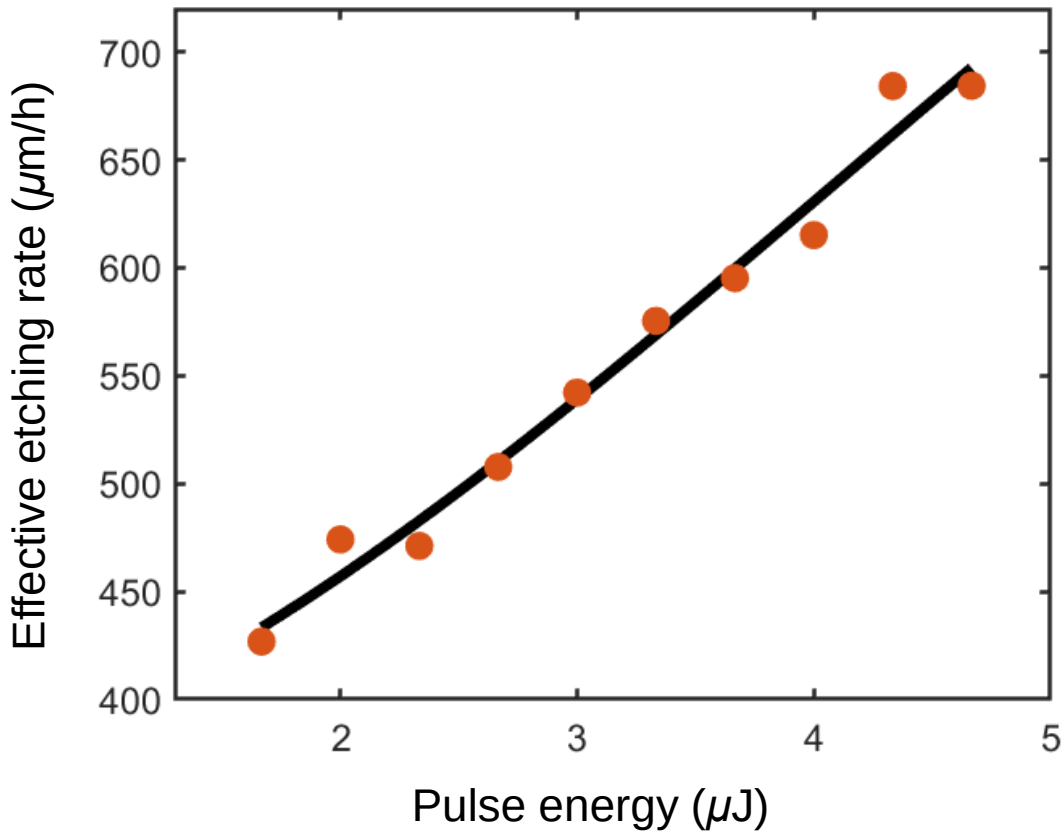

Figure 3.5: Effective etching rate as a function of pulse energy. For $\Lambda = 11\,\mu m$ and number of modification planes = 16, the cut-off pulse energy is $4.3\,\mu J$, beyond which is the structural instability regime. The black line is a linear fit to the experimental data which is represented by orange data points. All etching experiments are performed for 1.5 hours.

Another parameter to improve the effective etching rate depends on the cross-sectional area of a microchannel. This is expected as larger cross-sectional area provides higher accessibility and interaction surface area for the chemical etchant. We performed a systematic analysis exploring this effect (Fig. 3.6). The cross-sectional area can be controlled simply by changing the number of successive planes forming the channel. Thus, we fabricated microchannels with number of planes ranging from 2 to 16. All other parameters, including the pulse energy ($E_p = 4.3\,\mu J$), were kept constant.

The results shown in Fig. 3.6 give a linear trend, which indicates that etching rates can be increased simply by increasing the cross-sectional area, for almost any shape or type of microchannels.

For a smooth-walled microchannel with $\Lambda = 11\,\mu m$, $E_p = 4.3\,\mu J$ and number of planes modification = 20, the effective etching rate was as high as 750 µm/h. This etching rate is higher than the highest recorded etching rate in glass, 363 µm/h [45]. In our experiments, the crystal silicon planes in between the successive modifications fall off during etching, providing a higher *effective* etching rate, compared to the etching rate of single line modification.

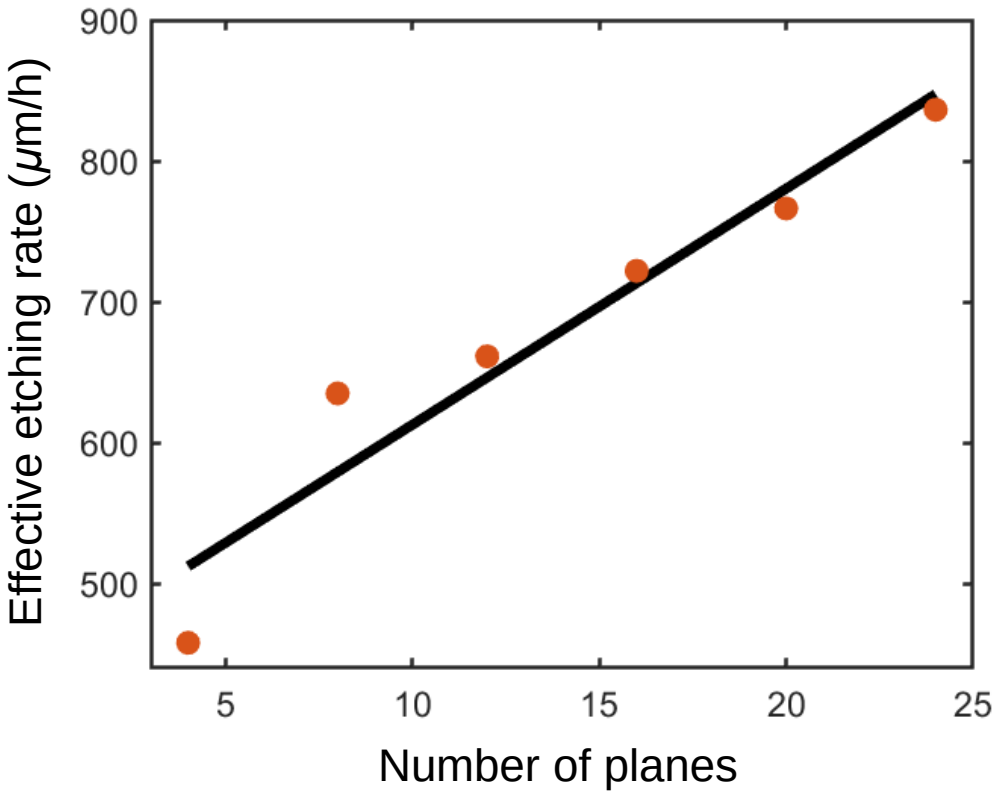

Figure 3.6: Effective etching rate as a function of modified planes. The number of planes directly define channel cross-sectional area. The black line is a linear fit to experimental data represented by orange data points.

3.3 Preserving the wafer surface during channel fabrication

Now that we have control over in-chip microchannel fabrication and etching rates, the next step is to ensure that the top wafer surface is preserved during fabrication. This would be critical for future applications, such as on-chip integration with electronics. Thus, we performed systematic experiments in order to find the most suitable surface passivation.

The first attempt was simply using a carbon tape on the surface top. The

carbon tape reacted strongly with the etchant and eventually destroyed the sample. Next, we tested Kapton tape for passivation, commonly used for its stability at a wide range of temperatures. From experimental observation, we found out that Kapton tape resulted in very slow etching of the microchannels, hence it was deemed not feasible.

Subsequently, we explored two types of photoresists (PR), AZ-5214E and AZ-4562, with different hard-baking times. For coating the PR over the sample surface, we used two approaches, i.e., spin coating and manually coating with a pipette. For both PRs, spin coating resulted in extremely thin coating, which was stripped off during etching. Thus, we decided to continue with pipette coating. Similarly, AZ-4562 PR started to trap air bubbles during hard-bake. This is due to the high viscosity of AZ-4562 PR resulting in an uneven coat. Hence, we decided to continue with the hand coating approach of AZ-5214E PR.

Table 3.1 shows the detailed methodology and the results of our experimental investigation in applying coatings with variable baking and resting times.

Serial No.	Method	AZ-5214E results
1.	Coated sample with a pipette, baked for 10 mins at 110°C, let it cool for 3 mins and coated another layer to provide thicker covering and then hard-baked.	Unsuccessful (It started to form bubbles while hard baking)
2.	Coated sample with a pipette, a slightly thicker layer, baked 40 s at 110°C, let it rest for 10 mins, baked again for 5 mins at 120°C.	Unsuccessful (It started to form bubbles while hard baking)
3.	A coated thin layer with a pipette, baked 40 s at 110°C, let it rest for 2 h, baked again for 5 mins at 120°C.	Successful, but requires 2 baking steps
4.	A coated thin layer with a pipette, baked for 5 mins at 120°C (no resting time).	Unsuccessful
5.	A coated thin layer with a pipette, baked for 5 mins at 120°C, and let it rest for 2 hr.	Successful

Table 3.1: Coating methods for AZ-5214E photoresist and their results. A thin coat with a pipette and giving rest is essential for successfully protecting the sample.

From the results, we hypothesize that a thicker layer of PR traps air bubbles and forms a non-uniform layer, even if we stack thin layers, one by one on top of each other. Secondly, resting time for the PR is essential, as it allows the residue liquid to evaporate, leaving a solid strong layer, crucial for protecting the surface.

While two methods, no. 3 and no. 5 successfully preserved the sample for 75 mins; method no. 5 is preferred as it requires baking the sample only once, compared to method no. 3, which requires two baking steps. For microchannels which require longer etching periods, we used alternative passivation and etching steps (section 2.2.3).

In order to confirm that the wafer surface is protected after chemical etching, the first step is to strip off the photoresist layer from the top surface using the following protocol:

1. wash the sample with acetone for 5 mins in an ultra-sonic bath (twice)

2. wash the sample with isopropanol for 5 mins in an ultra-sonic bath

3. wash the sample with distilled water

4. dry the sample with Nitrogen gas

This protocol allows us to get rid of any organic or inorganic leftover residues from the PR layer. We imaged the sample surface with SEM to observe the morphology (Figure 3.7). At the central parts the wafer seemed well-preserved (see Appendix B for a discussion on edge effects).

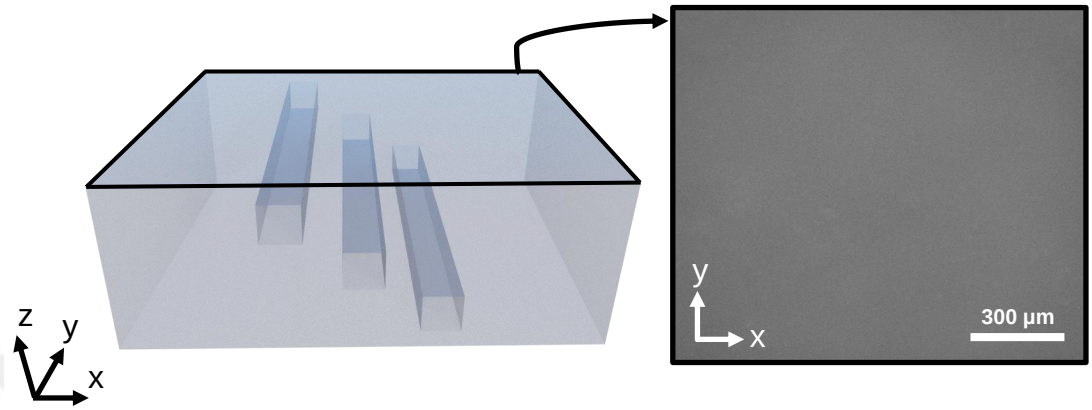

Figure 3.7: Schematic and an SEM image of the silicon surface after channel fabrication.

Then, we measured the surface roughness of the top wafer sample using an optical profilometer device OPD (Figure 3.8). *The average roughness of the sample after channel fabrication was measured as 2.2 nm, which is similar to that of pristine silicon (2.0 nm).*

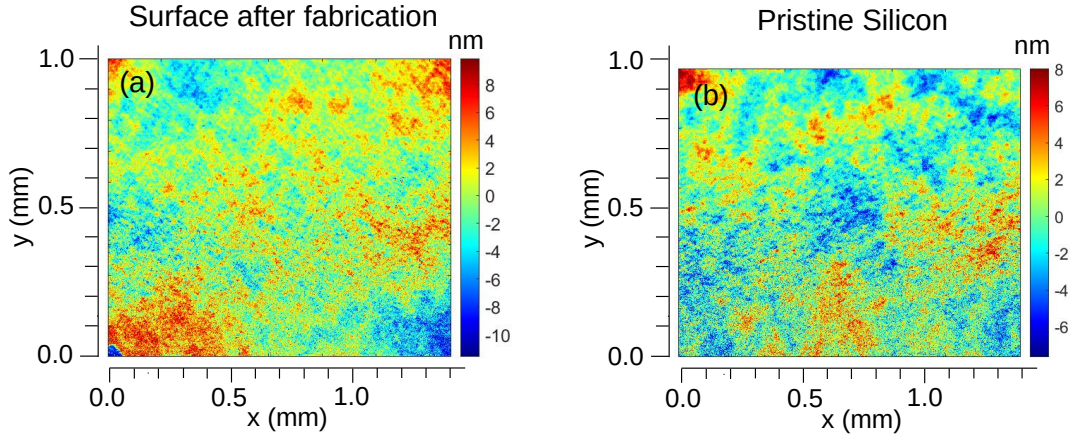

Figure 3.8: Surface quality control after channel fabrication. (a) Optical profilometer device (OPD) image of the surface after channel fabrication. The average roughness (Ra) is measured as 2.2 nm. (b) OPD image of a control pristine Si surface, with a surface roughness 2.0 nm. This confirms that the morphology of the surface does not change during fabrication.

Another important characterization is to test the chemical structure of the surface after fabrication. We performed EDXS analysis, which confirmed that no impurities are introduced to the surface (Fig. 3.9). *Thus, we were able to protect the sample's top surface from any physical or chemical impurities during microchannel fabrication.*

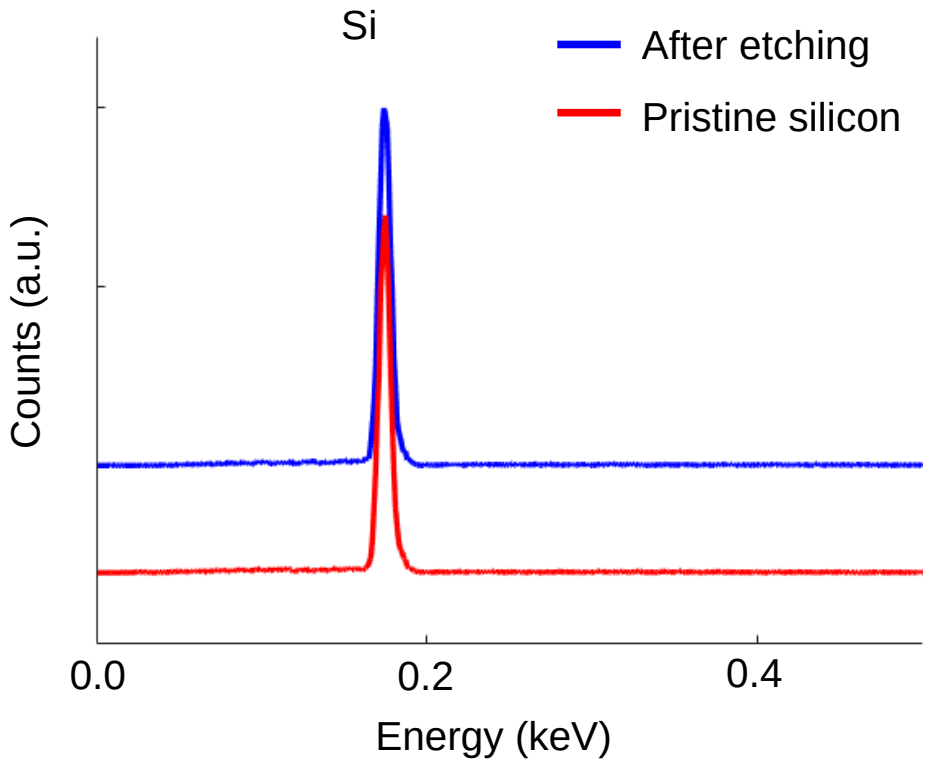

Figure 3.9: EDXS measurement of the pristine silicon and the surface after fabrication. The y-axis is *shifted* for the graphs for better visual representation, as they are almost identical. The peaks confirm that the surface is purely Si and there is no adsorption of chemical impurities. The control of this experiment was performed by nano-coating of metal on metal surface (see figure 2.8).

3.4 Analysis of inner-wall roughness

In-chip microchannels may find applications for various chemical mixing [41, 54] and biological applications [20]. One significant characteristic of such applications is the inner-wall roughness of the in-chip channels [55, 56]. In this section, we will quantify the roughness of inner-wall surfaces of our microchannels using a confocal laser scanning microscope (CLSM).

After fabricating representative channels, we diced the sample to measure side-walls and the floor of the microchannel. The data from CLSM was exported and used in Matlab^{TM} for better plotting capability (Fig. 3.10). For the transverse-mode laser-written microchannel, the average roughness (Ra) for the side-wall is found as 10.8 µm, while Ra for the channel floor is 9.3 µm.

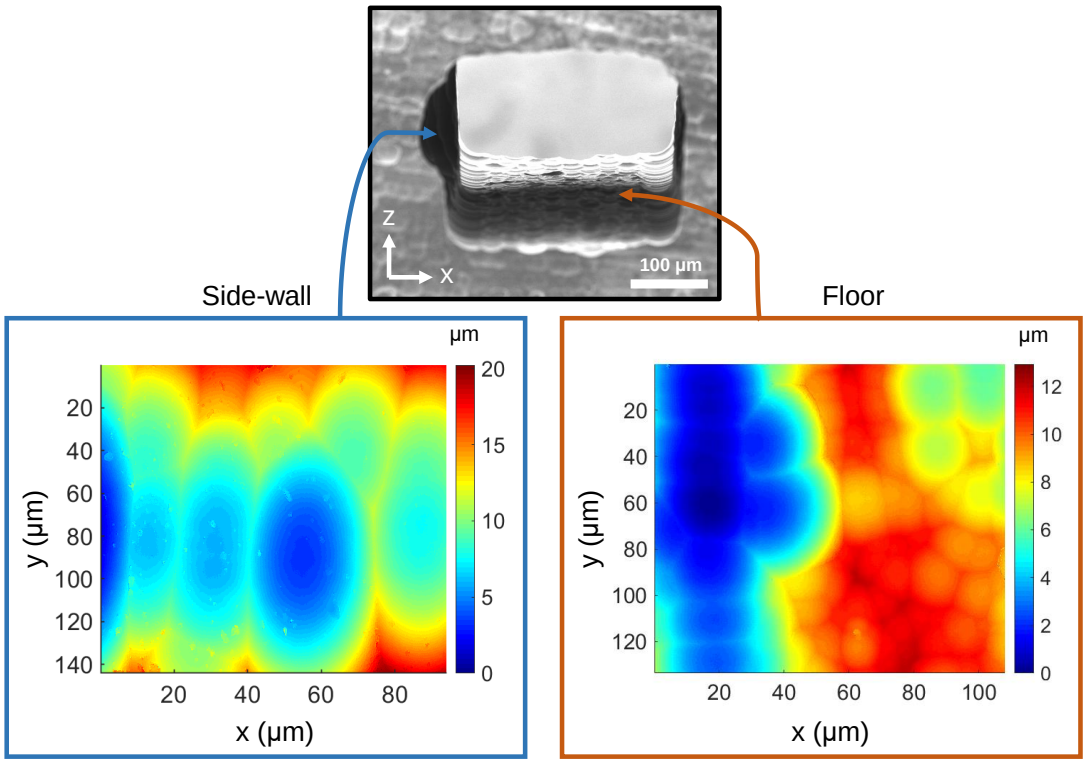

Figure 3.10: CLSM images of the side-wall and floor of a microchannel, imported and plotted in Matlab. The Ra values for side-wall and floor are calculated as 10.8 µm and 9.3 µm, respectively.

3.5 Controlling the dimension, architecture, and geometry

So far, we have demonstrated the fabrication of a Gaussian beam written in-chip and multi-depth microchannels in Si while preserving the device level quality of the sample surface. This section will further show control over the fabrication technique. We will look deeper into fabricating microchannels with different *architectures, geometries, and cross-sectional dimensions*.

We begin by showing cross-sectional dimension control. This was simply achieved by changing the number of the modification planes stacked in the x-dimension. For control, the length of all microchannels was kept constant *i.e.*, approximately 1.7 mm. By reducing the cross-sectional dimension (from 20 to 10 planes), we achieved a higher aspect ratio up to 17. (Fig. 3.11). This may be further improved by increasing the length of the microchannel. The longest channel opened has a length of 5 mm.

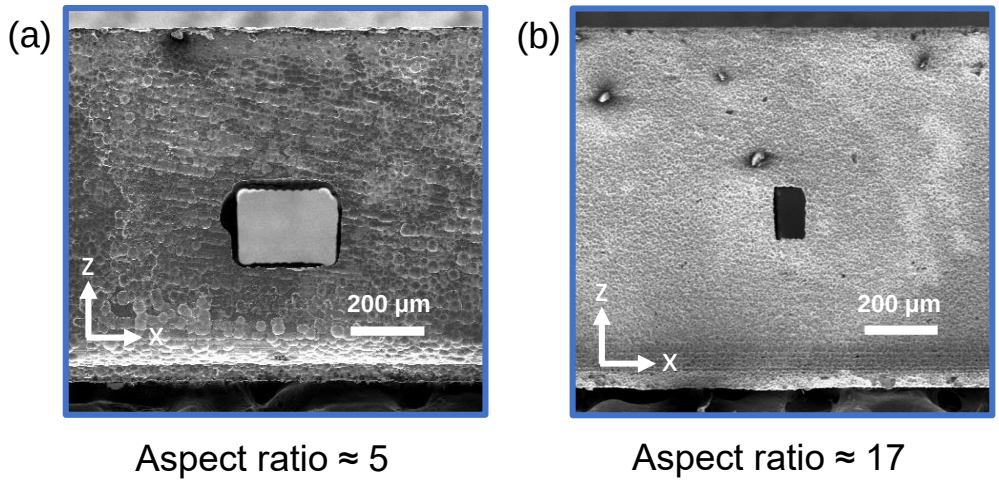

Figure 3.11: Cross-sectional dimension control experiment. (a) SEM image of a microchannel with modification planes = 20 and an aspect ratio = 5. (b) SEM image of a microchannel with modification planes = 10 and an aspect ratio of 17.

Now that we have control over the depth and cross-sectional area of the microchannel, we showcase the capability of fabricating the state-of-the-art 3×3 array of multi-level microchannels in a 1 mm thick silicon sample. These microchannels were written one-by-one starting from the bottom to the top level of the sample and then etched together. The laser parameters for each microchannel are as follows: $E_p = 2.9\,\mu J$, $\Lambda = 10\,\mu m$, and planes = 14.

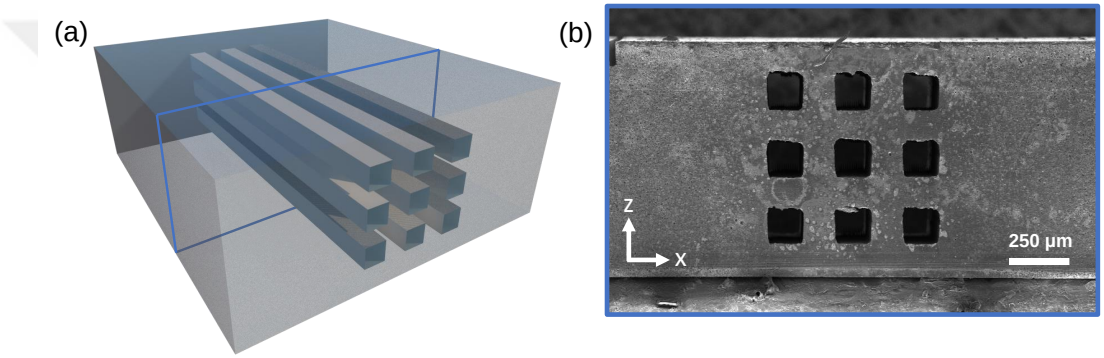

Figure 3.12: Multi-level microchannel array. (a) Schematic of the a 3×3 array of microchannels in a 1-mm thick silicon sample. (b) SEM image of a multi-level system of microchannels fabricated inside silicon.

Next, we fabricated a proof-of-concept curved geometry in Si (Fig. 3.13). We inscribed curved structures in the bulk using a precise 3D stage controlled with a computer-generated code. The sample is translated with respect to the laser such as to create desired shapes and architectures. We first performed ITM before etching (Fig. 3.13a) to confirm the laser writing step. Then, we revealed the curved channel through CMP followed by SEM imaging (Fig. 3.14). With such control, we can form virtually any lateral shape, or even connected sets of channels, depending on the requirements of the application.

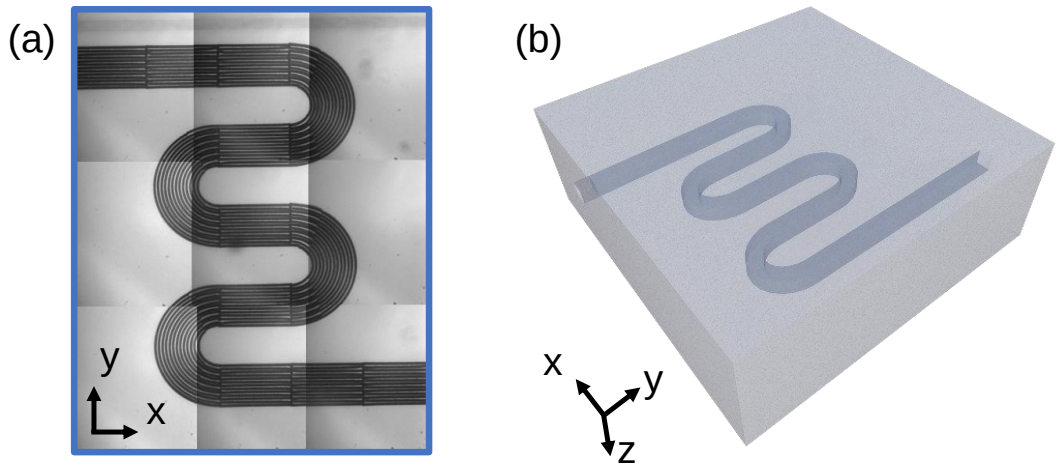

Figure 3.13: Proof-of-concept laser-written curved structures in the bulk of Si. (a) ITM image of the curved structure before etching. (b) Schematic of the buried 2.5D curved microchannel before etching. The parameters of laser-writing are as follows: $E_p = 3.6\,\mu J$ and $\Lambda = 12\,\mu m$.

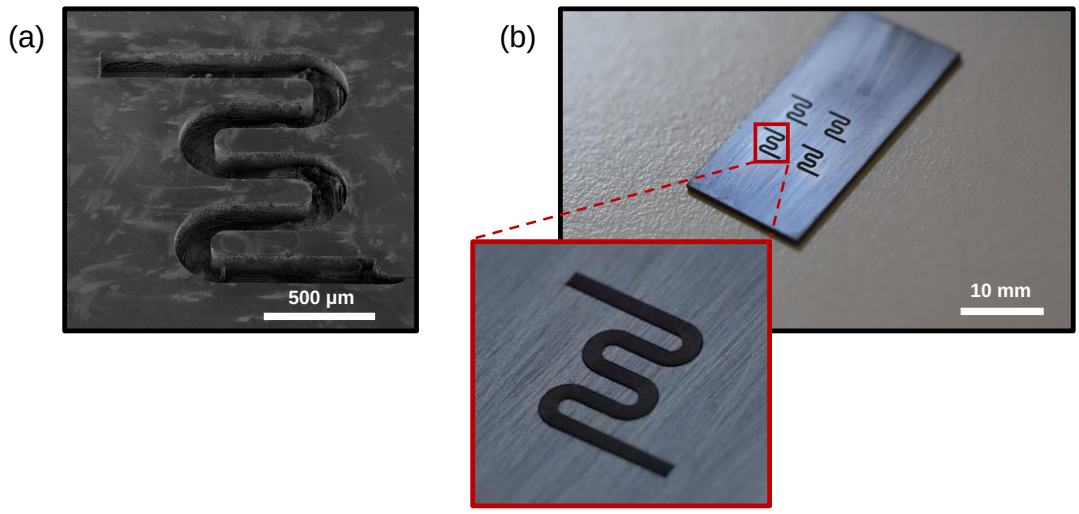

Figure 3.14: Curved microchannels after etching and polishing. (a) SEM image of the curved geometry revealed through CMP. (b) High definition DLSR camera image of a set of 4 curved microchannels. The inset in red is a zoomed in version to show high control over the edges.

3.6 Higher-aspect-ratio microchannels with spatially modulated beams

In this section, we provide some preliminary data indicating the future potential of our method, if used with emerging laser-writing approaches. Here we use a spatially modulated beam to fabricate higher-aspect-ratio channels. In particular, we generate a Bessel beam using phase modulation of a Gaussian beam. An Axicon is an optical element required to perform this job (Fig. 3.15a). The phase profile applied by the axicon angle of θ on the incident beam is as follows:

$$\phi_{\text{Axicon}}(r) = e^{\pm\left(2\pi r \frac{2\tan(\frac{\theta}{2})}{\lambda}\right)}$$

Similarly, a Bessel beam can also be generated using an SLM. In order to generate a Bessel beam using an SLM, a computer-generated hologram is applied to the SLM screen. The hologram can be depicted as a virtual axicon that converts a Gaussian incident beam into a spatially modulated Bessel beam (Fig. 3.15b inset). The Phase profile applied by the hologram is as follows:

$$\phi_{\text{SLM}}(r) = e^{\pm\left(2\pi \frac{r}{r_0}\right)}, r_0 = \frac{\lambda}{2\tan\left(\frac{\theta}{2}\right)}$$

The phase profile of the generated beam depends on the r_0 parameter, which is related to the cone angle of axicon (180° - 2θ). The r_0 values are chosen based on the pixel numbers. For instance, a hologram with r_0 = 7 pixels (pixel size in our SLM is 20 µm) corresponds to an angle of 0.61° on a physical axicon. In this way, we had freedom to generate different Bessel beams. The intensity profile of the Bessel zone and its cross-section is experimentally characterized for r_0 =10 and demonstrated in Fig. 3.16 [4].

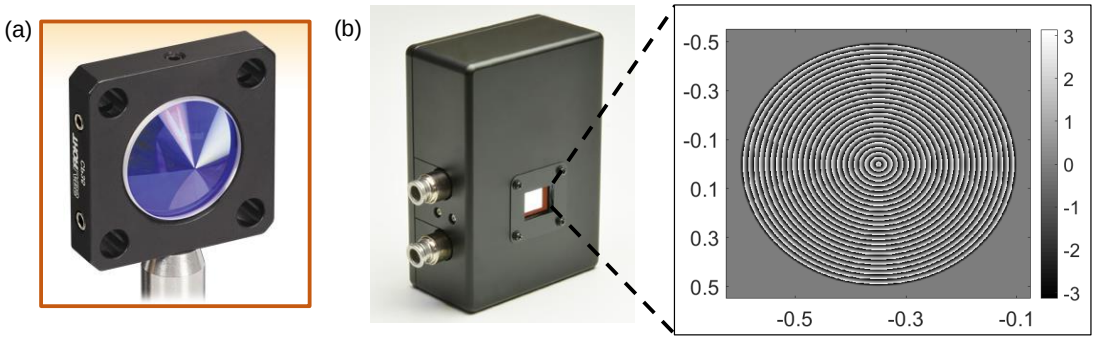

Figure 3.15: Optical elements to generate Bessel beam. (a) Physical element: axicon. (b) HAMAMATSU X10468 LCOS-SLM with 792 × 600 pixels and 20 µm pixel size. The hologram shows a phase pattern for generation of $r_0 = 10$ Bessel beam (inset in b) [4].

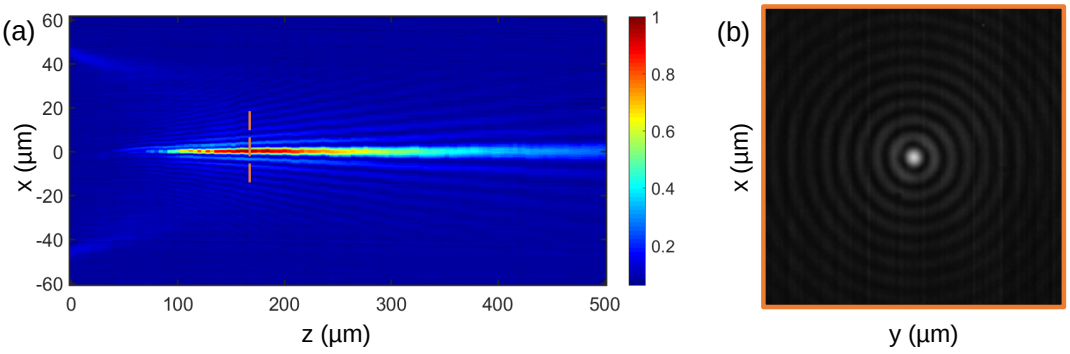

Figure 3.16: (a) The intensity profile of the Bessel zone along the beam propagation direction (x-z plane) measured with an InGaAs camera. (b) The cross-section intensity image in the x-y plane, at the point where the intensity is the highest along the propagation.

Previously, we created microchannels with Gaussian beams operating in transverse mode (Fig. 2.3a). On the other hand, Bessel beams are highly localized in two dimensions and extend longer in the axial direction. Therefore, we employ a Bessel beam in the longitudinal-writing modality (Fig. 2.3b). This will ensure a smaller cross-section and higher-aspect-ratio microchannel. Further, the longitudinal writing modality allows us to have control over the cross-sectional shape

of the microchannel. In this manner, we fabricated a set of three microchannels with different shapes at cross-section (Fig. 3.17), with an aspect ratio of 25.

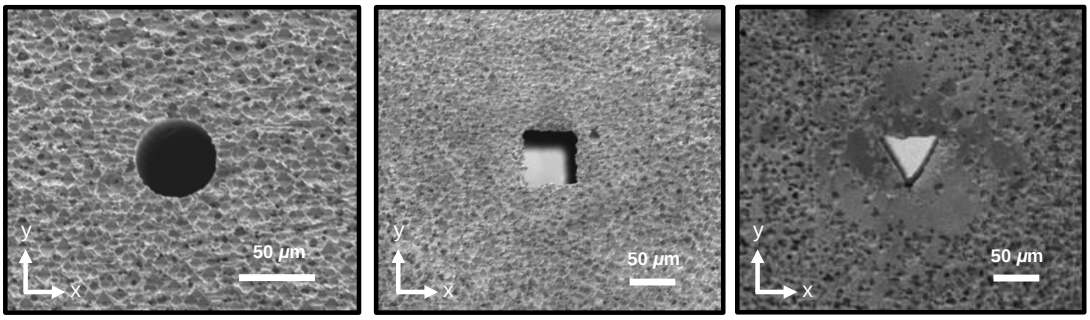

Figure 3.17: SEM images of high aspect ratio circular, square and triangular cross-sectional microchannels fabricated with highly localized Bessel beam. The laser parameters are as follows: $E_p = 6.7\,\mu J$, $\Lambda = 0.8\,\mu m$, $r_0 = 7$ and p-polarized light.

We then measured the inner-wall roughness of a Bessel-written microchannel (Fig. 3.18). Since the structures created by Bessel beams, which are building blocks of the microchannels, are thinner and have higher spatialization, we observe smoother surfaces with a Ra value of $0.23\,\mu m$.

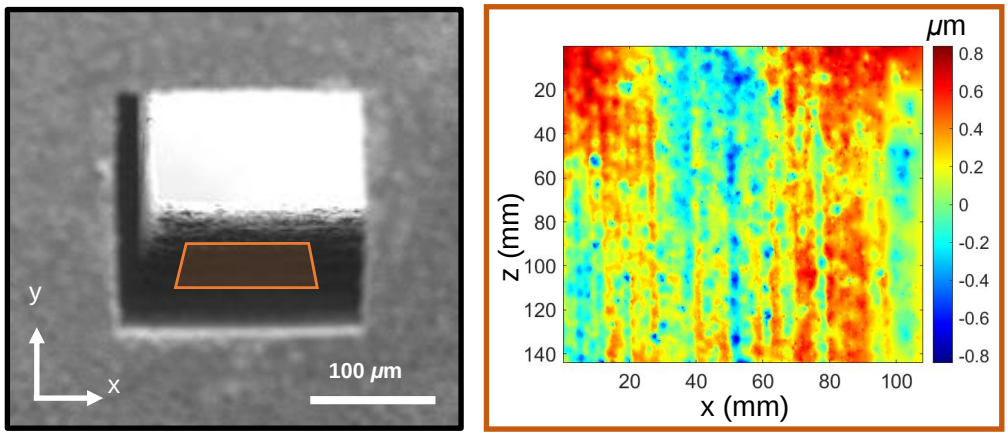

Figure 3.18: CLSM measurement for characterization of the inner-wall roughness of a Bessel-written microchannel. Ra = $0.23\,\mu m$, almost 2.3% of the roughness measured with a Gaussian-written microchannel.

3.7 Laser-written through-silicon vias (TSVs)

Until this point, we have established the fabrication of in-chip microchannels which are aligned horizontally with respect to the wafer surfaces (Fig. 3.12). Another type is vertical channels, elongating from the top to the bottom wafer surface, also known as, through-silicon vias (TSVs). TSV has unique and novel applications in the field of electronics, such as vertical electrical connections or interconnections between electronic chips for 3D integrated circuits.

Fabrication of TSVs with laser-lithography has been previously demonstrated by Tokel et al. However, the method requires polishing the sample from both ends to reach the in-chip modifications [2]. Here, we demonstrate the creation of TSVs directly, by eliminating the tedious polishing steps, preserving the full sample thickness.

The laser-written structures were written end to end using Bessel beam in longitudinal writing modality (Fig. 3.19), and the sample was etched without polishing. We created square and circular cross-sectional TSVs with the help of computer-generated code (Fig. 3.20). In order form a circular cross-section, concentric circles of modifications were written in the x-y plane with a stepwise shift of laser in the z-direction (Fig. 3.14). *Thus, we showed the capability to create TSVs all the way from the top to the bottom surface of the 1mm thick* $p\langle 111\rangle$ *type silicon wafer with laser writing and selective chemical etching.*

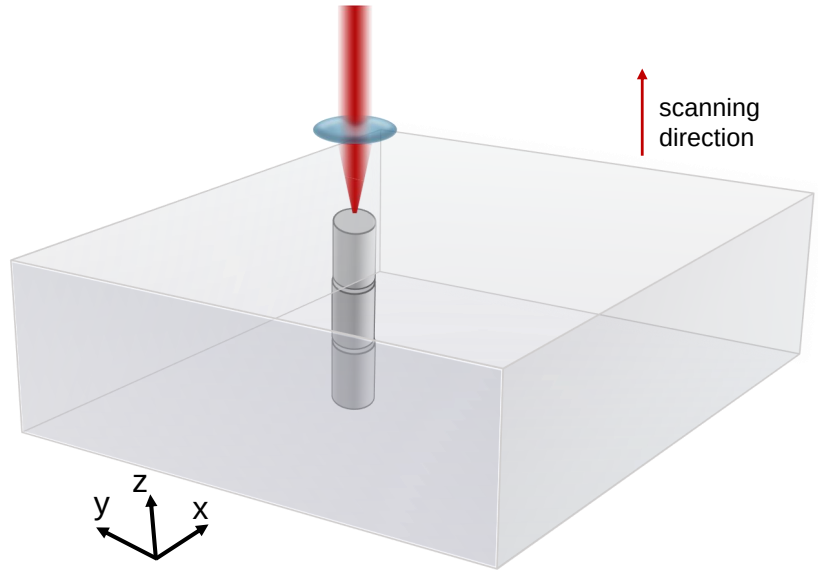

Figure 3.19: Schematic of longitudinal laser-writing of a circular cross-sectional TSVs.

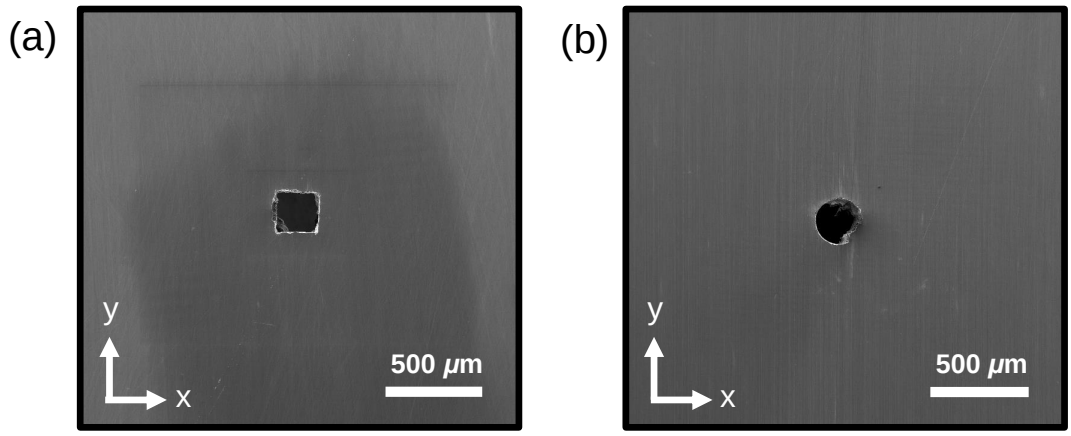

Figure 3.20: SEM images of (a) square and, (b) circular cross-sectional TSVs, created with our two-step laser-based fabrication technique. The laser parameters are as follows: $E_p = 6.7\,\mu J$, $\Lambda = 0.8\,\mu m$, $r_0 = 7$ and p-polarized light.

Hence, we were able to fabricate highly-controlled Gaussian-beam-written, multi-layer in-chip channel arrays; as well as proof-of-concept high-aspect-ratio microchannels with smoother walls and complete control on the cross-sectional

geometry, using highly localized Bessel beams.

In the next chapter, we will look at some of the potential applications for our state-of-the-art subsurface microchannels in Si.

Chapter 4

Conclusion

In this Thesis, we introduce a novel approach which enables creation of state-of-the-art subsurface microchannels deep inside Si. This corresponds to a mask-less laser-based fabrication approach, that can create a plethora of architectures and geometries. In contrast to previously-developed complex conventional lithography approaches used for surface fabrication, the channels can be positioned entirely within the wafer, and can be revealed without polishing.

The two-step laser-lithography method comprises of non-linear laser writing, followed by selective chemical etching. The laser parameters for the experimental setup are; wavelength = 1550 nm, pulse duration = 10 ns, and repetition rate = 150 kHz. For most experiments, we use a Gaussian beam in transverse writing modality. After inscribing in-chip modifications, the second step is to use a specialized mixture of chemical etchants, for selective removal of laser-written modifications in order to get a subsurface microchannel in Si.

We used multiple imaging techniques for the characterization and analysis of our developed in-chip microchannels. Infrared transmission microscope (ITM) for imaging buried laser-scribed structures; scanning electron microscope (SEM) for imaging and measuring cross-sectional dimensions of a fabricated microchannel; laser scanning microscope (LSM) and optical profilometer device (OPD) for

measuring inner-wall roughness and characterizing the top wafer surface of the sample.

The experimental results demonstrated that we can fabricate a fully-buried microchannel at any depth in the bulk of Si. The initial challenge was to avoid cracks and fabricate a microchannel with smooth inner-walls. We observed two types of cracks *i.e.*, cracks due to stress release because of the modifications being extreme close; and cracks due to stress concentration at the modified and crystal silicon interface. This structural instability problem was solved by increasing the spacing between successive modifications planes to reduce the effect of stress concentration at the edges of the microchannel, and to achieve smooth-walled microchannels.

Conversely, at very large Λ values, uneven channel walls were observed because of the thick unmodified region in-between modifications. Hence, we concluded that for each Λ value, there is a specific range of E_p that corresponds to a smooth surface crack-free microchannel (*e.g.*, when Λ is set as 12 µm, E_p has an optimum range of 4 ± 0.5 µJ).

Next, in order to increase the throughput of the fabrication process, we aimed at increasing the etching rates. We performed two systematic studies on "effective etching rates" of a microchannel. The effective etching rates as a function of E_p; and effective etching rates as a function of number of modification planes. Thus, the highest effective etching rate with smooth channel walls was measured as 750 µm/h, higher than the recorded etching rates of any type of glass.

Moreover, to reserve the wafer surface for on-chip integration in future, the challenge was to control the sample surface from damage during etching. Therefore, the sample was protected with AZ-5214E photoresist. To validate the control of the surface, we characterize the surface roughness and chemical morphology, and used SEM imaging. The results validate that the properties of the surface are similar to that of a pristine silicon.

We further analyzed the average inner-wall roughness of a Gaussian written

channel, measured as 10.8 µm for the side-wall, and 9.3 µm for the floor. This can be a significant characteristic for many medical and chemical mixing applications.

Next, we fabricated microchannels with aspect ratio, up to 17. The longest channel opened was up to 5 mm in length. Furthermore, we extended this approach to create state-of-the art 3×3 array of multi-level channels and proof-of-concept curved microchannels in the bulk of silicon. This proves that we can create any shape or kind of microchannel with the same level of control.

Furthermore, we demonstrated preliminary results of fabricating higher aspect ratio smooth-walled microchannels by using spatially modulated beams. We fabricated microchannels with an aspect ratio of 25 and inner-wall roughness, as low as, 0.23 µm. Additionally, longitudinal writing modality provided an extra degree of freedom to create microchannels with any cross-sectional shape.

Another important implication of our fabrication technique is the creation of vertical channel, known as through-silicon via (TSV). We fabricated square and circular cross-sectional TSV without any additional pre-etching polishing steps.

Now, we will look at some of the potential applications of our fully-buried microchannels and TSVs.

An exciting implication would be to integrate in-chip microfluidic channels for cooling of on-chip Si based electronics. Over the past decade, the miniaturization of electronics is challenged by the excessive heat generation, preventing the devices to work at their full potential and thus, jeopardizing the efficiency of the system. One potential solution is to exploit microfluidic channels to pass controlled amounts of liquid coolant across the Si chip. Such efforts made by Erp *et al.* have demonstrated that liquid-cooled systems are better heat extractors, compared to air-cooled systems. While these surface channels on Si are successful in heat extraction of GaN electronics, we believe that a subsurface channel will provide a more efficient thermal management platform, by providing a closer contact of the fluid to the immediate hot spots of the chip (Fig. 4.1). Furthermore, high control of the top surface of the wafer allows us to use silicon as an electronically

active layer in CMOS compatible electronics. Integrating in-chip microchannels to the electronics is an ongoing research as a part of another project.

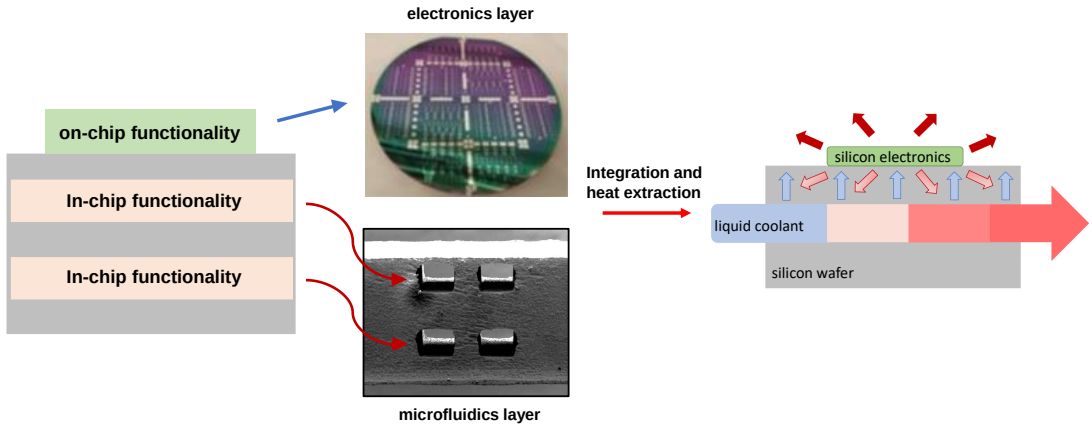

Figure 4.1: Concept of integrating on-chip functional electronics elements to in-chip microfluidics for heat management of Si based electronic devices (Image courtesy: Dr. Sueda Saylan).

On the other hand, a significant application of TSV is the multi-level stacking of Si chips for three-dimensional electronic devices. The electronics industry is shifting to 3D stacking of silicon ICs, to satisfy the ever-increasing demand for compact electronic devices while maintaining their performance [57, 58]. An example of such 3D electronics is Intel's Foveros stacking technology that uses TSV, created with conventional lithography techniques [59]. The benefits of such 3D integration include heterogeneous functionalities of the device, improved power consumption and cost effectiveness [58]. While the technology to fabricate TSV already exists, we believe that the use of mask-free laser lithography technique has the potential to replace complex conventional lithography processes in future.

In summary, we achieved state-of-the-art high aspect ratio in-chip array of microchannels at various depths in Si with Gaussian beam pulses. We increased throughput and controlled the quality of top surface of the wafer. We further achieved fabrication of TSV; and showed preliminary results of higher aspect ratio smooth microchannels by incorporating spatially modulated beams. Finally, we talked about some of the exciting opportunities for thermal management of

electronics and 3D stacking of electronic chips.

In future, the laser-sculpting technique has the potential to upgrade the fabricate novel subsurface nanochannels. This will provide exciting opportunities not only in nano-fluidics but also in the field of nano-optics and nano-photonic.

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Appendix A

Etching Protocol

The etching process is conducted in the designated areas inside the clean room. When entering the clean room, it is to be ensured that all protocols relating to cleanroom suits are strictly followed.

Before preparing the etchant, the solvent wet-bench is used to clean the sample in the following sequence:

1. wash the sample with acetone for 5 mins in an ultra-sonic bath (Figure A.1)

2. thoroughly wash the sample with de-ionized (DI) water

3. dry the sample with nitrogen gas

Figure A.1: Silicon sample placed in a petri dish filled with acetone. The sample is cleaned for 5 minutes in an ultra-sonic bath.

On the same solvent workbench, weighing scale is used to measure the required mass of copper II nitrate ($Cu(NO_3)_2$) in a glass petri dish (Figure A.2).

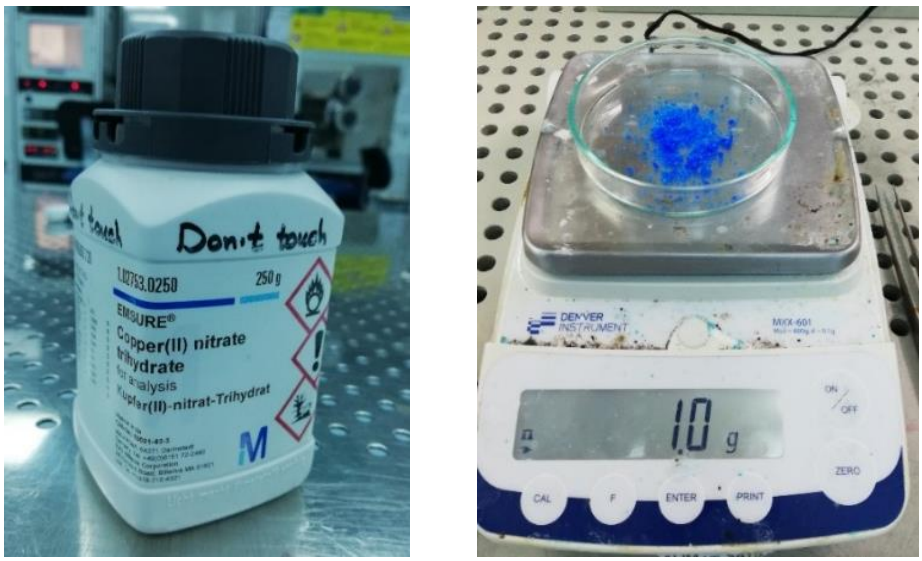

Figure A.2: Image demonstrating a petri dish filled with copper II nitrate placed on a weighing scale.

It is mandatory to wear an extra protection kit while working on an acid workbench to avoid inhaling fumes and to avoid any physical contact with acid in case of splashing or spilling. The kit includes acid-resistant gloves, an N-95 mask, a glass helmet, and a green gown to be worn over the cleanroom suit (Figure A.3). Ensure the gloves are clean, dry, and do not have any wear or holes. These acids are hazardous, and being careless about them can be life-threatening.


Figure A.3: Images of an N-95 mask; the gown and helmet; and the acid-resistant gloves used for personal protection during the etching process

We need the following equipment to perform etching:

1. acid/base compatible measuring cylinder
2. acid/base compatible funnel
3. Teflon container
4. acid/base compatible tweezers
5. A stopwatch

To prepare the etchant, we use the following steps in sequence:

1. Measure the required amount of water using a funnel and measuring cylinder and pour it in the Teflon container.

2. Pour the powdered $Cu(NO_3)_2$ inside and shake it cautiously until it completely dissolves (Figure A.4).

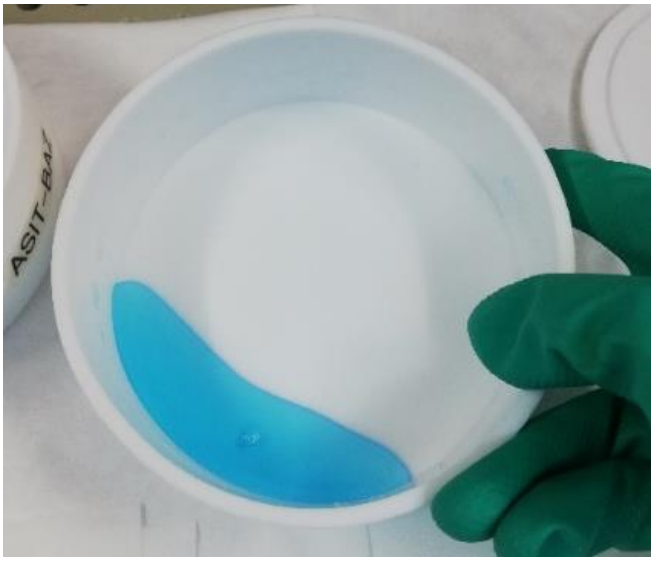

Figure A.4: Image of $Cu(NO_3)_2$ dissolved in water

The following steps are to be followed repeatedly for each liquid etchant (HF, HNO_3, and CH_3COOH):

3. Rinse the measuring cylinder and funnel with water and dry it.

4. Measure the required amount of acid (shown in Figure A.5) using a funnel and measuring cylinder and attentively pour it in the mixture.

5. Cover the container with the lid.

Figure A.5: Images of hydrofluoric acid, nitric acid, and acetic acid used in steps 3-5.

Follow the last three steps for each acid to prepare the etchant. The sample can be placed and removed from the etchant using tweezers. Measure the etching time using a stopwatch and once the sample is etched, remove the sample from the etching solution and wash it with DI water, and then dry it with nitrogen gas.

Figure A.6: Image of a sample placed inside the chemical etchant

After the etching process is over, the etchant must be discarded in an environmentally-friendly manner. Use the waste bottle designated for our etchant (Figure A.7). Fill the bottle with at least 20% water (to make it diluted), then discard the etchant with the help of a funnel into the bottle. Wash all the equipment thoroughly with DI water.

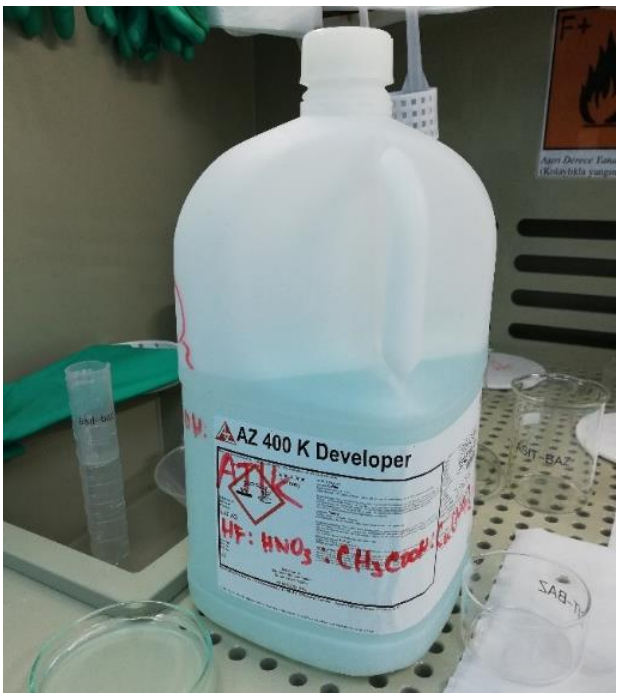

Figure A.7: Waste bottle for discarding the etchant in an environmentally-friendly manner

Appendix B

Wafer surface preservation and the edge effects

While the central part of the wafer surface was well-protected from all kinds of physical and chemical damage (refer to Fig. 3.7 - 3.9), we observed that the edges of the sample were affected. This type of damage, where the etchant seeps under the photoresist through edges, is commonly known as the "undercut effect". Figure B.1 shows the damaged sides of the top surface of the sample.

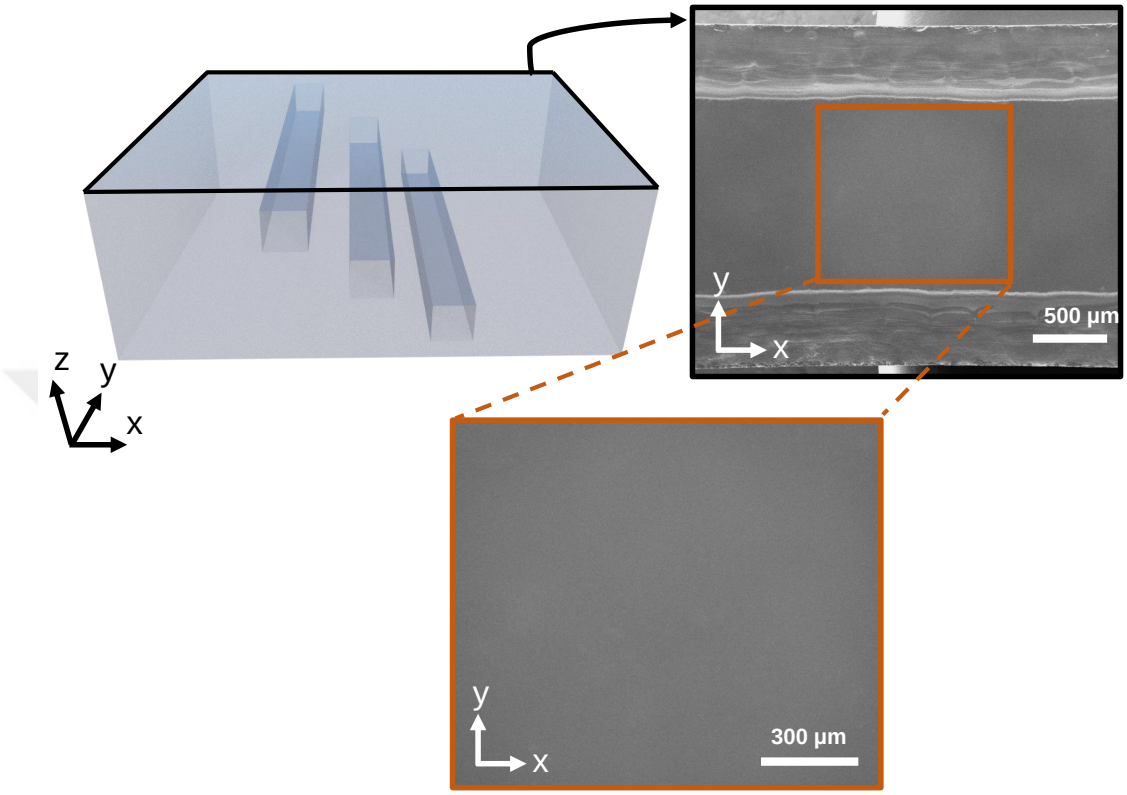

Figure B.1: SEM images showing that the central parts of the surface are fully-preserved while the edges observe an undercut effect.