

LOW POWER SMALL SIZE MAGNETIC RESONANCE IMAGING SIGNAL ACQUISITION SYSTEM WITH OPTICAL CONNECTIONS

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By
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We certify that we have read this thesis and that in our opinion it is fully adequate,
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ABSTRACT

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In Magnetic Resonance Imaging (MRI) systems echo signals received by a coil are sampled and subjected to digital signal processing. The physical link between the sampling system and the signal processor is coaxial cables in conventional applications. However, coaxial cables possess risks and limitations when placed in gradient and radio frequency fields, both of which are present in an MRI system. The complexity of issues related to coaxial cables increases rapidly as the number of channels scales up in parallel imaging applications. To overcome the drawbacks of coaxial cables, systems that employ fiber optic cables for the transmission of the analog signal have been proposed.

In this work, we designed a system which transmits sampled and digitized analog signal through fiber optic cables, while the power required to perform acquisition and conversion operations is also delivered to the module using an optical link. To increase the number of channels that can be placed in a typical birdcage compartment, dimensions of the module are kept as small as possible. The module is designed to be used in a project with a 10.5 Tesla MRI system operating at 447 MHz which is currently available only at the University of Minnesota. The circuit design for one of the proposed approaches is completed at both the schematic and the layout levels to perform feasibility analysis. Theoretical estimations show that the power consumption is 263 mW and occupied cross-sectional area is 900 mm² per channel while attaining more than 95 dBFS SNR figure using 65 MSPS sampling rate.

Keywords: Magnetic Resonance Imaging, Fiber Optics, Low Power, Small Size.

ÖZET

MANYETİK REZONANS GÖRÜNTÜLEME İÇİN DÜŞÜK GÜÇ TÜKETİMLİ VE KÜÇÜK BOYUTLU OPTİK BAĞLANTILI İŞARET ALMA SİSTEMİ

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Manyetik Rezonans Görüntüleme (MRG) sistemlerinde yankı işaretleri bir bobin tarafından yakalandıktan sonra örneklenir ve sayısal sinyal işlemeye tabi tutulur. Geleneksel uygulamalarda örnekleme sistemi ile sinyal işleme birimi arasındaki fiziksel bağlantı eş eksenel iletim kabloları ile sağlanır. Ne var ki, eş eksenel kablolar değişen ve radyo frekansı alanlarının içine yerleştirildiklerinde riskler ve sınırlandırmalar barındırırlar. Bir MRG sisteminde bu alanların ikisi de mevcuttur. Eş eksenel kablo kullanımına bağlı sorunların güçlüğü, paralel görüntüleme uygulamalarında kanal sayısının çoğalması ile hızla artar. Eş eksenel kabloların dezavantajlarını gidermek etmek amacıyla, analog işaretlerin taşınması için optik kabloların kullanıldığı sistemler önerilmiştir.

Bu çalışmada örneklenmiş ve sayısallaştırılmış analog işaretin taşınması için fiber optik kabloların kullanılmasının yanı sıra yakalama ve dönüştürme işlevlerinin yerine getirebilmesi için birime gereken gücün optik bağlantı ile iletildiği bir sistem tasarlanmıştır. Tipik bir kafes bölümüne sığabilecek kanal sayısını artırmak için birimin boyutları olabildiğince küçük tutulmuştur. Birim şu anda yalnızca Minnesota Üniversitesi'nde bulunan ve 447 MHz 'de çalışan 10.5 Tesla MRG sistemi için yürütülmekte olan bir projede kullanılmak üzere tasarlanmıştır. Yapılabilirlik analizi amacıyla, önerilen yaklaşımlardan birinin devre tasarımı şema ve serim seviyesinde tamamlanmıştır. Teorik değerlendirmelere göre kanal başına güç tüketimi 263 mW ve kullanılan kesit alanı 900 mm² iken 65 MSPS örnekleme sıklığı kullanılarak 95 dBFS'ten daha fazla SNR değeri elde edileceği görülmüştür.

Anahtar sözcükler: Manyetik Rezonans Görüntüleme, Fiber Optik, Düşük Güç

Tüketimi, Küçük Boyut.



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To our martyrs and veterans...

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Chapter 1

Introduction

Magnetic Resonance Imaging is a commonly used technique in medical practices. Improvements in image quality provide a more accurate diagnosis, which is preferable. One way to enhance the image quality is to use multiple number of channels as much as possible. However, in addition to physical limitations, increasing the number of channels also introduces issues which may not be a problem with systems equipped with less channels.

As MRI systems interact with living creatures, patient safety is of the utmost importance and is regulated by international standards. One of the design considerations that require attention is due to radio frequency (RF) heating. This phenomenon occurs when a conductor material, e.g. copper, is placed in an RF field [1]. It causes material to heat up and can cause discomfort or even burns if the tissue is close by for external coil applications. It is even more problematic in interventional applications as there is a physical contact. Furthermore, the increase in the temperature in the surrounding environment can degrade the performance of the system or even worse result in failure.

Another problem associated with the use of a large number of channels is due to interference of the information cables with each other. In conventional MRI devices, signals captured by a coil are transmitted to the signal processor using

coaxial cables. Systems with 96 or less channels have been implemented using coaxial cables; however, issues related to coaxial cables are also acknowledged in these works as well [2, 3].

Instead of using coaxial cables to transmit the MRI signal to the signal processor, fiber optic cables can be used to achieve the same goal. In addition, because they are made of electrically insulating material, fiber optical cables do not have the problems associated with coaxial cables. Since fiber optic cables do not carry electric current, they are inherently immune to electrical interference and electrical noise coupling from each other and from other parts of the system as well. For these advantageous reasons, systems that use fiber optic cables have been proposed for MRI signal transmission [4, 5]. Although the use of fiber optic cables eliminates the problems associated with coaxial cables, it also introduces new issues related to optical transmission. With coaxial cables, received signals are transmitted as electrical signals without changing form. On the other hand, in the optical transmission approach, MRI signals are converted from electrical to optical form and then sent through fiber optic cables. The transducer used to perform the conversion in [5] is a laser diode, and in [4] it is a modulator. These additional blocks in the transmission channel introduce their own noise contribution to the system, which degrades the Signal-to-Noise Ratio performance at the analog front-end output.

Furthermore, the power required for the accompanying circuitry is another aspect that should also be taken into consideration. In [5], a battery is used to supply power to active components, which includes a low-noise amplifier (LNA), the laser diode itself, and the requisite control circuitry in the module. Although the power consumption of the module is low enough to allow a long service life, this approach requires periodic maintenance. Using a combination of coaxial and optical cables is not preferable, as it would introduce disadvantages of both mediums into the system.

1.1 Motivation

In this work, we propose a system that uses optical connections for both the data transfer and the required power. With this approach, module interconnects become completely immune to field interactions; therefore, risks and limitations of systems that use coaxial cabling are no longer a problem for this system. Furthermore, in this system, the analog MRI signal is not sent to the processing system to be sampled as in [5], instead it is sampled and digitized in the module, and the digital MRI signal is sent out to the processor. By doing so, the noise contribution due to the electrical-optical-electrical conversion and the channel itself are also eliminated; therefore, the SNR level delivered to the processor remains unaffected from transmission stage. Since digitization is performed within the module, the power consumed by the requisite circuitry contributes to the total power consumption. At the same time, the power that can be delivered to the module is limited by the performance of the optical power infrastructure and size constraints.

The circuitry required to perform sampling and digital conversion is planned to be placed to the receiving coil as closely as possible. Given that the receiver coils are placed in a birdcage-like structure that is positioned around the patient's head, the surface area reserved for a single channel must be small enough to fit multiple channels in such a compartment. For this work, the total number of coils in the array is assumed to be 512 units; to accommodate enough space for each channel, a cross-sectional area of $30\text{ mm} \times 30\text{ mm}$ is allocated per channel. Although the height of the module is not restricted as strictly as its area, it is also kept as small as possible. For the final design, complete circuitry of a module can be divided into multi-layered structure where a layer is reserved for RF analog front-end, digital conversation and power/interconnect blocks.

The size restriction also introduces a need for thermal management. Although low-power components tend to be more efficient than regular products, when enclosed in a small volume without active cooling, a small temperature increase may trigger a positive feedback mechanism.

1.2 Thesis Outline

In this thesis, design considerations for a low-power, small-size MRI signal acquisition system with optical connections are described. The design parameters are adjusted according to a 10.5 Tesla MRI system operating at 447 MHz . Currently, such an MRI system is only available at the University of Minnesota. The bandwidth of the target signal is assumed to be 1 MHz . The main objective of this work is to attain a SNR level as high as possible while consuming low power and size using off-the-shelf components.

To achieve this goal, various circuit topologies are investigated at the initial design stage and these topologies are discussed in Chapter 2. Once the topology is determined, the actual design of the module is established reviewing currently available, state-of-the-art, off-the-shelf components. In Chapter 3 circuit schematics are explained in detail. Chapter 4 presents the considerations on the layout and elaborates on Printed Circuit Board (PCB) placement. A discussion of further performance improvements is given in Chapter 5. Finally, in Chapter 6 theoretical estimations are reviewed, and future improvements are discussed.

The appendix contains drawings of each layer of the designed PCB.

Chapter 2

Considered Circuit Topologies

2.1 Bandpass Sampling

The *sampling theorem* states that, a continuous time band-limited signal $x(t)$ with zero frequency content for $|\omega| > \omega_M$, is perfectly reconstructed, i.e. without distortion, from its samples $x(nT)$, $n = 0, \pm 1, \pm 2, \dots$, if the sampling frequency ω_s satisfies [6]

$$\omega_s > 2\omega_M \quad (2.1)$$

The above condition can be rephrased as a signal must be sampled with a sampling frequency more than twice the highest frequency component present in its spectral content for unambiguous recovery. This limiting frequency, $2\omega_M$ is called as the Nyquist rate and half of it is referred as the Nyquist frequency. The region covered in the corresponding frequency spectrum, starting from DC up to the Nyquist frequency, is denoted as the 1st Nyquist zone. Higher order Nyquist zones are placed ω_M apart in the frequency spectrum.

Although this condition guarantees alias-free sampling, if certain information about the signal is known a priori or has no interest for the application; then, restrictions imposed by the sampling theorem can be relaxed to some extent. For

this work, since the excitation frequency is controlled precisely and, therefore, is well known, the center frequency of the target signal carries no additional information. Hence, a potential candidate for the signal to be processed is the aliased replica of the original signal that is folded back to the baseband due to the lowered sampling rate with respect to the Nyquist rate.

The folding back effect should be precisely controlled so that aliased replicas do not overlap and distort the spectral content that is of interest. A continuous-time bandpass signal with lowest frequency component of F_L , highest frequency component of F_H and center frequency F_C , has bandwidth B given by,

$$B = F_H - F_L \quad (2.2)$$

Then, the non-overlapping condition for a uniform sampling frequency F_s is satisfied if there exists an integer k such that [7],

$$\begin{aligned} \frac{2F_H}{k} \leq F_s \leq \frac{2F_L}{k-1} \\ 1 \leq k \leq \left\lfloor \frac{F_H}{B} \right\rfloor \end{aligned} \quad (2.3)$$

For $k = 1$, above condition reduces to the sampling theorem given in Equation 2.1 and for higher values of k , the sampling system can become vulnerable to variations of the sampling rate or the center frequency depending on how critically k is chosen, which leads to distortion of the content stored in the bandwidth B . A higher sampling rate increases the system's immunity to these fluctuations by expanding the original signal bandwidth to a higher value of $B' = B + \Delta B_L + \Delta B_H$ which corresponds to lower $F'_L = F_L - \Delta B_L$ and higher $F'_H = F_H + \Delta B_H$ frequency end points. With these new end points, the conditions given in Equation 2.3 are modified to be:

$$\frac{2F'_H}{k'} \leq F_s \leq \frac{2F'_L}{k'-1} \text{ where } k' = \left\lfloor \frac{F'_H}{B'} \right\rfloor \quad (2.4)$$

Then for a sampling system with,

$$\begin{aligned} F_c &= 447 \text{ MHz} \\ B &= 1 \text{ MHz} \\ \Delta B_L &= \Delta B_H = 225 \text{ kHz} \end{aligned} \quad (2.5)$$

the range of acceptable sampling frequencies is:

$$2907.306kHz \leq F_s \leq 2907.328kHz \quad (2.6)$$

Although the bandpass sampling approach enables using much lower sampling rates compared to the rates imposed by the Nyquist criteria, careful selection of the sampling frequency is not the only critical parameter which needs to be precisely controlled when it comes to other concerns associated with sampling, such as the signal-to-noise ratio (SNR) and associated effective number of bits (ENOB) of the Analog-to-Digital Converter (ADC) used in the sampling system. The theoretical signal-to-noise ratio due to errors introduced while quantizing the sampled signal is given by the celebrated equation [8]:

$$SNR = 6.02N + 1.76dB \quad (2.7)$$

for full-scale sinewave input, where N is the number of bits used by the converter to represent the signal. The SNR value calculated using this equation is due to quantization noise only and is measured over the Nyquist bandwidth, which is from DC to $F_s/2$ for sampled lowpass signals. If the actual bandwidth B occupied by the signal is less than the Nyquist frequency, then using digital filtering, the SNR can be improved, and this effect is called the process gain and given as:

$$SNR = 6.02N + 1.76dB + 10 \log_{10} \left(\frac{F_s}{2B} \right) \quad (2.8)$$

Then, for a lowpass signal with $B = 1 \text{ MHz}$ sampled using 14-bit ADC with 125-MSPS, theoretical SNR can be as high as:

$$SNR = 6.02 * 14 + 1.76dB + 10 \log_{10} \left(\frac{125}{2 * 1} \right) \cong 104dB \quad (2.9)$$

ADC3664 is a state-of-the-art 14-bit 125-MSPS ADC offered by Texas Instruments and has specified typical SNR of 77.5 dBFS , for a -1 dBFS input signal of 5 MHz [9]. Compared to the 86 dB theoretical value, specified SNR value is lower due to other imperfections such as noise, timing jitters, etc. For bandpass sampling with very high input signal frequencies, the SNR becomes limited by the jitter-noise level rather than the quantization errors [10]. The main contributors to jitter are aperture jitter and sampling clock jitter, which includes inherent

jitter of the clock source, jitter introduced by the components on the clock path such as synthesizers, buffers, etc. and the circuitry itself. The total rms clock jitter is then calculated by summing these contributors in root-sum square fashion, and the SNR for an infinite resolution ADC limited only by the timing jitter is given by [11]:

$$SNR = 20 \log_{10} \left(\frac{1}{2\pi f_{in} t_j} \right) \text{ dB} \quad (2.10)$$

where f_{in} is the input signal frequency that is to be bandpass sampled and t_j is the total rms clock jitter.

For an ideal ADC, the relationship between the number of bits used to represent the sampled signal and the SNR is given by Equation 2.7; however, real-life ADCs have specified ENOB lower than N due to imperfections introduced by noise, jitter, etc. A more accurate measure of dynamic performance for an ADC is specified using the Signal-to-Noise-and-Distortion Ratio (SINAD) rather than the SNR. SINAD is specified by not only taking other noise components than the quantization noise into consideration, but also distortion due to harmonics, except DC, is also included. Using SINAD, ENOB is calculated from Equation 2.7 but in the place of SNR, SINAD figure is used as:

$$ENOB = \frac{SINAD - 1.76 \text{ dB}}{6.02} \quad (2.11)$$

Then, using Equation 2.10 combined with Equation 2.11, the theoretical value of ENOB can be approximated as a function of the input frequency. From [9] using specified ENOB values for different input frequency signals, it is deduced that the test environment which is used to characterize the ADC had approximately 1 ps total rms jitter and with this value ENOB for frequencies higher than the specified range is extrapolated in Fig. 2.1.

At low frequencies, degradation in SINAD is dominated by quantization noise and non-linearities of the encoder; therefore, timing jitter effects are not apparent in this region. However, as the input signal frequency increases, it becomes the limiting factor of the ADC performance and eventually renders the ADC impractical for the application due to dynamic range requirements.

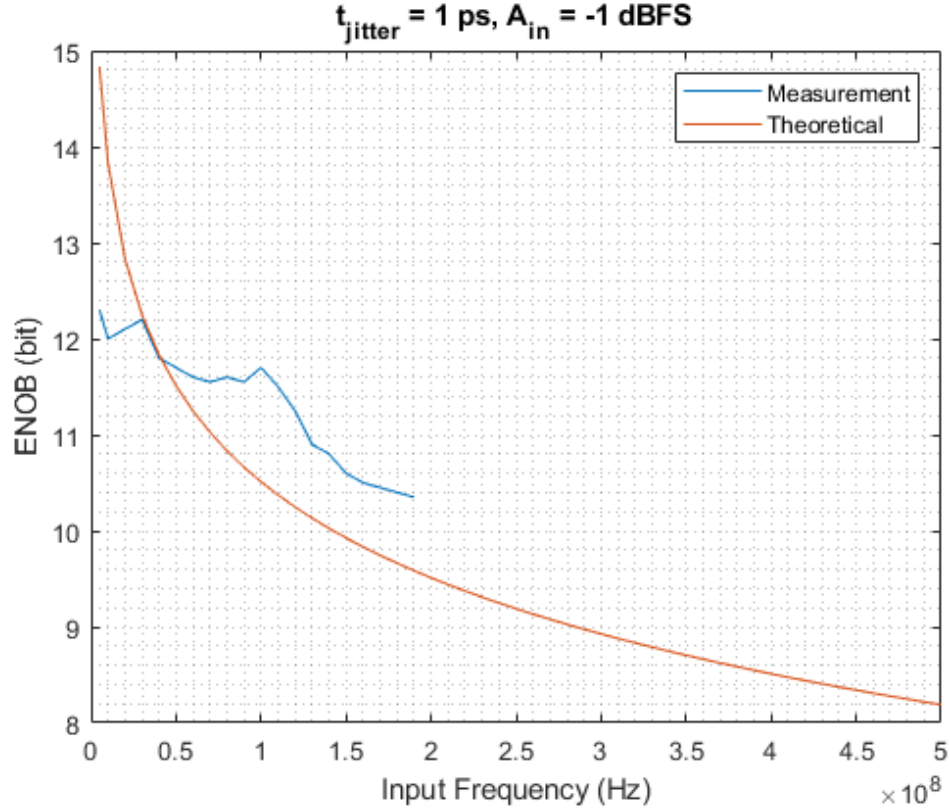


Figure 2.1: ENOB vs Input Frequency for ADC3664

A block diagram for the bandpass sampling approach is given in Fig. 2.2. The incoming signal is conditioned according to the ADC's input requirements using a differential amplifier, and then filtered to reject out-of-band frequency components before being fed into the converter. For the sampling clock source, an oscillator is used and its output is distributed to the target components using a clock distribution device. To configure and control these components, a microcontroller is included in the design. The ADC output is transmitted to the data collection system through an optical link, and control signals are also received through an optical link. Conversation between optical and electrical signals is accomplished using optical receiver and transmitter modules. Finally, the power required to run all of these components is also derived through an optical channel and converted to electrical power using a photovoltaic power converter whose output is regulated by a DC/DC converter and scaled required voltage levels using low-dropout regulators.

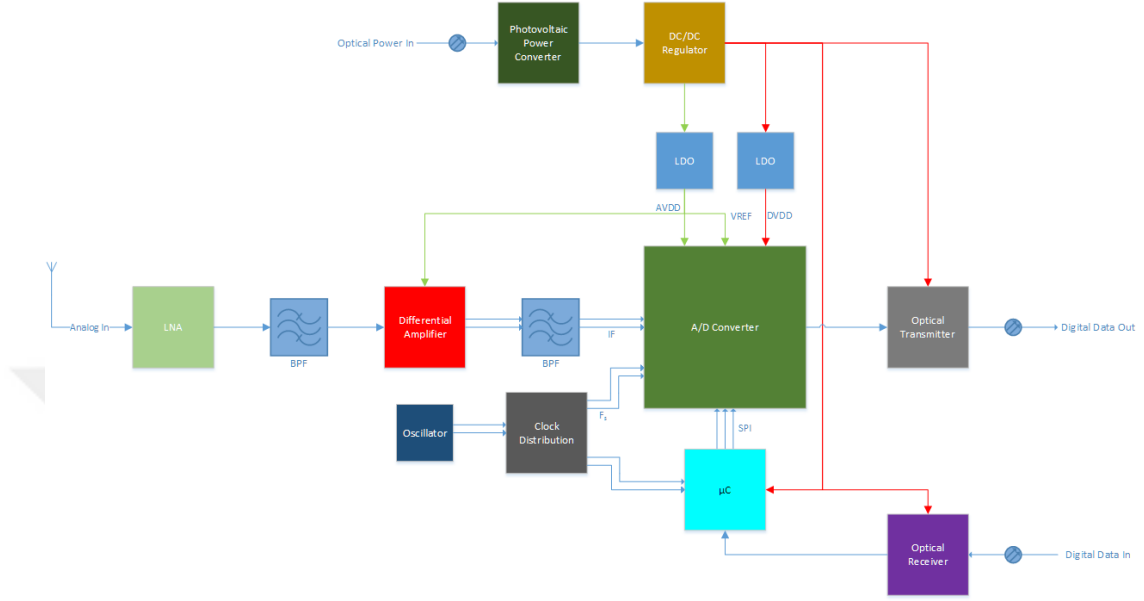


Figure 2.2: Block Diagram of Bandpass Sampling Approach

ADC that is going to be used for bandpass sampling applications should have a wide analog input bandwidth in order to capture signals without attenuation. Furthermore, to satisfy dynamic range requirements, it should have high SFDR and correspondingly high ENOB. For this application, it should consume as low power as possible and also occupy a small surface area. Although in the market there are very advanced ADCs that have very high analog input bandwidth, sampling rate, and SFDR for radar applications, communication systems, etc. they are power hungry and have a large physical package, since these criteria are out of the concern for these applications. Regarding the restrictions mentioned above, the outstanding ADCs from major integrated circuit (IC) manufacturers are compared in Table 2.1.

Manufacturer	Part Number	Resolution (Bits)	Sampling Rate (MSPS)	SNR (dBFS)	SFDR (dBFS)	ENOB (Bits)	Input Bandwidth (MHz)	Power Consumption (mW/Channel)	Surface Area (mm ²)
Analog Devices	LTC2256-14	14	25	72.9	90	11.8	800	37	36
Analog Devices	LTC2257-14	14	40	73.4	90	11.87	800	49	36
Analog Devices	LTC2258-14	14	65	74	90	11.97	800	49	36
Texas Instruments	ADC3541	14	10	79	95	12.8	400	36	25
Texas Instruments	ADC3542	14	25	79	95	12.8	400	45	25
Texas Instruments	ADC3543	14	65	79	95	12.8	400	79	25
Texas Instruments	ADC3561	16	10	82	90	13.3	900	76	25
Texas Instruments	ADC3562	16	25	82	90	13.3	900	83	25
Texas Instruments	ADC3563	16	65	82	90	13	900	122	25
Texas Instruments	ADC3581	18	10	84.5	90	13.7	900	76	25
Texas Instruments	ADC3582	18	25	84.5	90	13.7	900	83	25
Texas Instruments	ADC3583	18	65	83.8	89	13.6	900	122	25
Texas Instruments	ADC3660	16	65	81.9	88	13.3	900	71	25
Texas Instruments	ADC3661	16	10	82	90	13.3	900	50	25
Texas Instruments	ADC3662	16	25	82	90	13.3	900	55	25
Texas Instruments	ADC3663	16	65	82	89	13	900	94	25
Texas Instruments	ADC3664	14	125	77.5	92	12.6	1400	100	25
Texas Instruments	ADC3681	18	10	84.5	90	13.7	900	50	25
Texas Instruments	ADC3682	18	25	84.5	90	13.7	900	55	25
Texas Instruments	ADC3683	18	65	83.8	89	13.6	900	94	25

Table 2.1: Comparison of Wide Analog Input Bandwidth ADCs for Bandpass Sampling ($f_{in} = 5 \text{ MHz}$)

The dynamic characteristics quoted in Table 2.1 are specified for a 5 *MHz* input signal. Even though it resides in the first Nyquist zone for all of the ADCs, reported ENOBs are less than specified resolution and it decreases even further as the input frequency increases. Among these ADCs, ADC3664 is the most suitable one for this work but even it cannot satisfy the dynamic range requirements for the 447 *MHz* input frequency without an ultra-clean clock source.

Although the bandpass sampling approach enables digitizing the incoming signal using only an ADC and the requisite components, such as low-noise amplifier (LNA), filters, and drivers, thus it may offer a reduced bill of materials, surface area, and power consumption, it also requires a very clean clock source if the input frequency is considerably higher than the Nyquist frequency, and satisfying this requirement may defeat all the aforementioned advantages. For this reason, it is not the opted approach for this work; rather, the conventional way which uses a mixer to down-convert the incoming high-frequency signal to a baseband signal is chosen, and different circuit topologies to implement this conversation are investigated next.

2.2 Baseband Sampling

A common practice in radar and communication applications to digitize a received RF signal is downconversion through analog mixing where the high frequency input signal is shifted to a lower frequency using a mixer [12]. When the RF signal $S = \sin \omega_c t$ is multiplied with a fixed frequency signal, called as the local oscillator (LO), $LO = \sin \Omega t$ sum and difference of these frequencies appear at the mixer output as [13],

$$S \times LO = \frac{1}{2} [\cos((\omega_c - \Omega)t) - \cos((\omega_c + \Omega)t)] \quad (2.12)$$

The low frequency component, which has suitable frequency spectrum for baseband sampling, is called as the lower sideband, and the high frequency component, which will be filtered out using a low pass filter, is called as the upper sideband. The lower and upper sidebands are separated by $2 \times \Omega$ and since Ω is a high

frequency signal to achieve baseband conversion for a high frequency RF signal, filtering of the upper sideband can be performed with a high level of attenuation.

The analog multiplier element, the mixer, essentially utilizes saturated diodes to perform the multiplication action. To drive the diodes to saturation, the LO signal is required to have a very high amplitude compared to the RF signal. This requirement on the amplitude is usually accomplished by amplifying the LO signal prior to feeding it to the mixer if the source of the LO signal does not have high output level; however, some mixers have a built-in buffer, which greatly reduces amplitude requirements. Moreover, while performing the frequency conversion passive mixers introduce loss, referred as the conversion loss, contrary to active mixers that include amplifiers to achieve conversion gain [14]. Therefore, if output of the passive mixer does not attain required power levels for following stages due to conversion loss, an additional amplifier circuitry may become necessary to recondition this signal. On the other hand, the gain provided by the active mixer might be enough together with the gain introduced in the previous stages to be directly fed into later stages. Next, two different circuit topologies that use these two different mixer types are investigated.

2.2.1 Downconversion using a Passive Mixer

Passive mixers do not require supply input, since they do not include amplifier circuits to enhance the level of the output signal (IF) and commonly do not include LO buffers to be able to accept low LO levels. Instead, they have a specified range for the LO level to operate. If this level is not satisfied, depending on the deficiency in the LO signal level, they fail to provide the stated performance characteristics or may even become inoperative. For this reason, an amplifier circuitry is incorporated into the LO signal chain as output of the LO signal source, which can be a crystal, usually does not have the required output level to be directly fed into the mixer. A modified version of the topology given in Fig. 2.2 for baseband sampling in which a passive mixer is used for downconversion is given in Fig. 2.3.

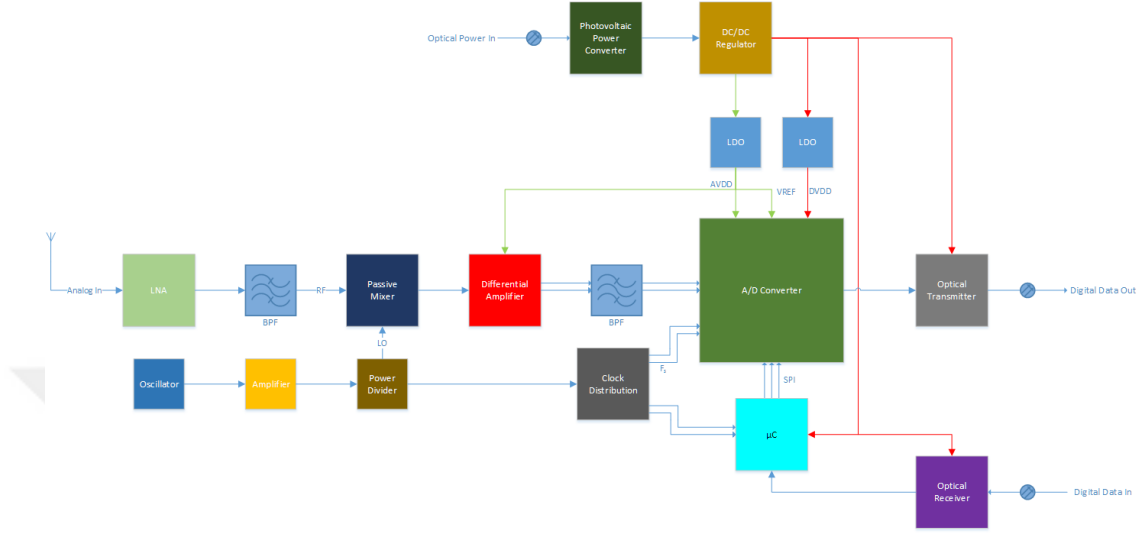


Figure 2.3: Block Diagram of the Baseband Sampling Approach: Using a Passive Mixer for Downconversion

Since with this approach, an additional circuit element, namely an amplifier, is required to be included in the design, in the best scenario, a portion of the valuable total surface would be sacrificed. Furthermore, depending on the characteristics and design of the amplifier circuitry, power consumption can become disadvantageous compared to active mixers. For these reasons, the method of using a passive mixer for downconversion is not opted for this work.

2.2.2 Downconversion using an Active Mixer

For downconversion of the incoming RF signal, active mixers are preferred over passive mixers in this work, as they are able to provide conversation gain while performing frequency shift as opposed to introducing loss like passive mixers. Furthermore, being able to accept lower LO signal levels compared to passive mixers is another advantage. The comparison of several active and passive mixers considered for this work is given in Table 2.2.

Manufacturer	Part Number	RF Freq. (Min-Max) (GHz)	LO Freq. (Min-Max) (GHz)	IF Freq. (Min-Max) (GHz)	LO Level (dBm)	Conversion Loss (dB)	Input IP3 (dBm)	P1dB (dBm)	Power Consumption (mW)	Surface Area (mm ²)
Analog Devices	LT5526	.0001-2.5	.0001-2.5	0-1	-5	-0.4	14	1	140	16
Analog Devices	LT5557	.4-3.8	.38-3.5	.0001-0.6	-3	-2.9	25.6	8.8	270	16
Analog Devices	LT5560	0-4	0-4	0-4	-2	-2.7	10.1	-0.8	30	9
Macom	MAMX-009239	.01-2.5	.01-2.5	.01-2.5	+17	5.5	25	13	-	45
Marki Microwave	T3-07	.001-7	.001-7	.001-4	+15	8.0	27	13	-	80
Mini-Circuits	RMS-5L+	.4-1.4	.4-1.4	0-8	+3	7	9	-3	-	50
Mini-Circuits	ADEX-10L+	.01-1	.01-1	0-8	+4	7.2	16	1	-	50
Mini-Circuits	ADE-1ASK+	.002-.6	.002-.6	0-.6	+7	5.3	16	1	-	50

Table 2.2: Comparison of Active and Passive Mixers for Downconversion (Typical Values)

The listed passive mixers require an LO signal level as much as 17 dBm while introducing a conversion loss as high as 8 dBm . On the contrary, active mixers can operate with an LO signal level as low as -5 dBm while providing a conversion gain of 2.7 dBm .

Once the topology for the downconversion is chosen, the next step is to determine the source of the LO signal. One option is to use a high frequency oscillator; another way is to utilize a frequency synthesizer; both options are reviewed in the following section.

2.2.2.1 High Frequency Oscillator as the LO Signal Source

A high frequency oscillator can be used as the LO signal source in a mixer application if there is one with the desired frequency. A block diagram of this topology is given in Fig. 2.4.

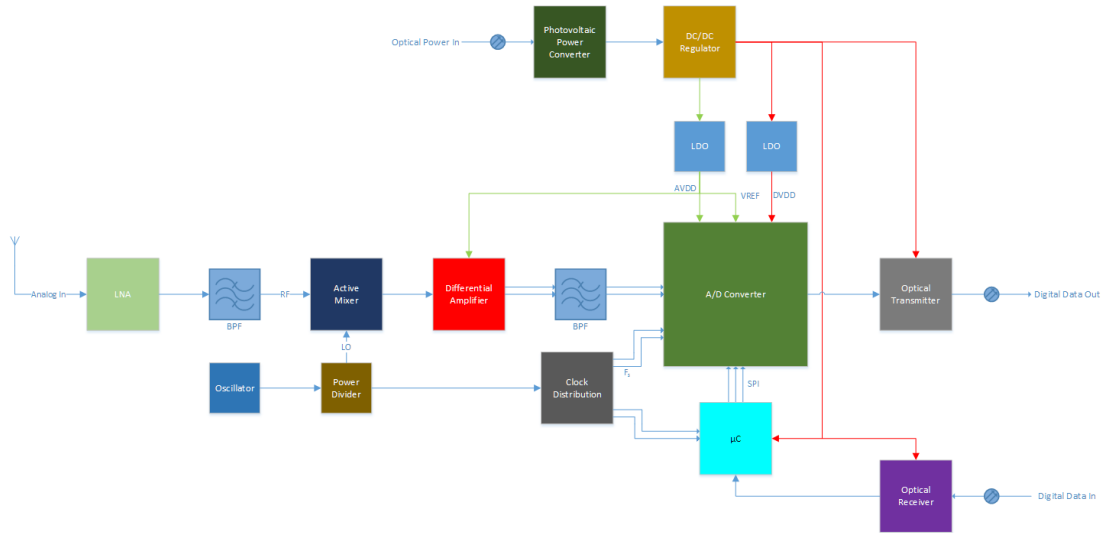


Figure 2.4: Block Diagram of the Baseband Sampling Approach: Using an Active Mixer with High Frequency Oscillator as the LO Source for Downconversion

Depending on the application, the required frequency of oscillation may not be a commonly encountered value on the market. Although for radar, communication and signal processing applications oscillators with many different output

frequencies are produced by various manufacturers, niche frequencies, such as 447 MHz required for this work, are not mass produced. Furthermore, although the requirement on the output frequency is the utmost critical, power consumption and surface area restrictions must be met at the same time. Finally, frequency stability of the source is another parameter which should be considered carefully, since temperature variations in the system may shift the output frequency of the source to a point where the resultant signal at the mixer output no longer resides in the reserved spectrum region.

Oscillators with different resonating elements, such as quartz crystals and surface acoustic wave (SAW) devices, are considered possible candidates as LO sources. In Table 2.3 different oscillators from various manufacturers are compared.

Manufacturer	Part Number / Series	Technology	Output Type	Output Frequency (MHz)	Frequency Stability (ppm)	Phase Noise (@10 kHz Offset) (dBc/Hz)	Jitter* (ps)	Power Consumption (mW)	Surface Area (mm ²)
Crystek	CCS575S	SAW	Sine Wave	433.92	± 150	-137	1	66	37.5
NEL	SR-A2A70	Crystal	Differential Sine Wave	250-700	± 100	-130	0.3	462	132
RFMI	SC3048B	SAW	Differential Sine Wave	444	± 200	-130	5.3	66	132
Skyworks	SI570	Crystal	LVDS	.01-1417	± 20	-132	0.36	330	35

Table 2.3: Comparison of the High Frequency Oscillators (* 12 kHz to 20 MHz)

Since the oscillators from NEL and Skyworks include active control elements and differential drive circuits, their power consumptions are considerably higher than those of the other parts. SAW based oscillators offered by Crystek and RFMI suffer from low frequency stability because of the highly physical geometry dependent nature of the underlying working principle. Due to the vulnerability to temperature variations in the system, these types of oscillators are not preferred for this work.

2.2.2.2 Frequency Synthesizer as the LO Signal Source

Instead of using a high frequency oscillator whose output frequency can be used directly as the LO signal, a lower-frequency oscillator which has robustness against temperature changes is chosen for this work. Such oscillators are referred to as

Temperature Compensated Crystal Oscillator (TCXO) and, as the name implies, they include correction mechanisms for output frequency against changes in temperature. This compensation action is achieved by changing the load capacitance seen by the crystal with respect to temperature variations [15]. Although TCXOs with high frequency output exist in the market, they are not preferred for this work either. The reason is to implement a high frequency output TCXO, the required circuitry, which includes a tailored Phase Locked Loop (PLL), necessarily increases the component size and also power consumption. OE-XBF series form NEL FC is such a TCXO with an output frequency range from 30 MHz to 2 GHz but occupies 972 mm^2 of surface area and consumes 330 mW of power.

Rather than using the output of a high frequency TCXO directly as the LO signal, a low frequency but small footprint and low power TCXO can be used as the reference signal for a frequency synthesizer whose output will then be fed into the mixer. A block diagram of this method is given in Fig. 2.5

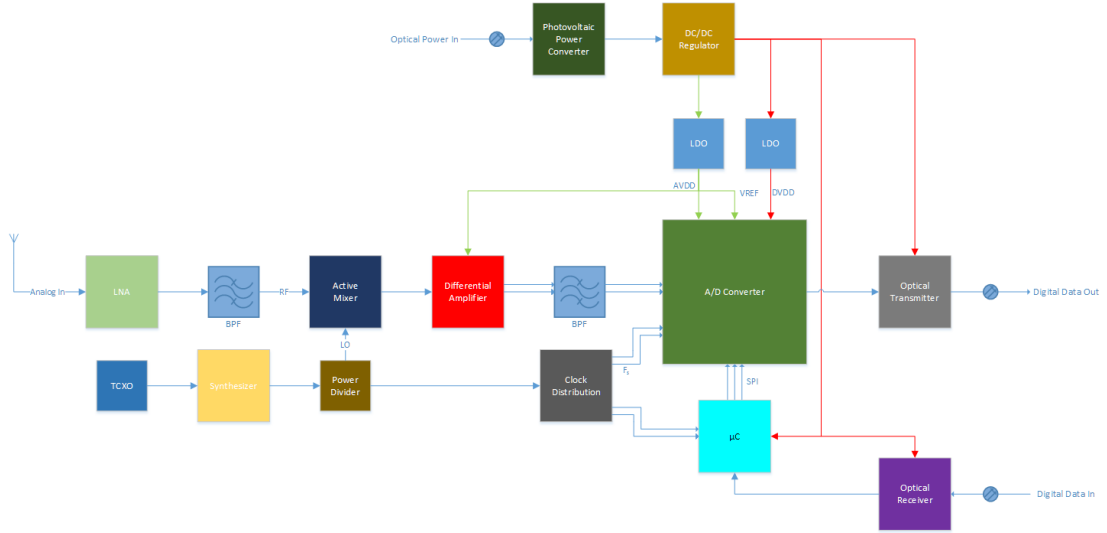


Figure 2.5: Block Diagram of the Baseband Sampling Approach: Using an Active Mixer with a Frequency Synthesizer as the LO Source for Downconversion

This topology not only offers reduction in surface area and power consumption but also enables the output frequency to be modified on the fly according to the changes in the system or in the application. Thanks to these benefits, this topology is chosen for this work but it is modified according to imposed necessities.

Chapter 3

Circuit Design

As discussed in the previous chapter, baseband sampling using an active mixer with a frequency synthesizer as the LO signal source is considered to be the optimal topology for this work. With this approach, the circuitry that is needed to perform digitization and transmission of the incoming RF signal can be realized with low power consumption and in a small surface area. Although the block diagram given in Fig. 2.5 represents the underlying principle to be used, it has been modified to further reduce the power consumption per input channel. Reasons for these modifications will become apparent as choices for components to perform a specific task are discussed in the remaining part of this chapter.

For schematic design, PADS Logic VX.1.1 from Mentor Graphics is used.

3.1 LO and Clock Signal Generation

The reasons for using a TCXO as the LO signal source are investigated in Section 2.2.2.2. Having selected the oscillator type, other criteria to consider while choosing a TCXO for an application are: output frequency, output type, frequency stability, phase noise, operating voltage, and for this work specifically power consumption and surface are other critical parameters to pay attention.

For the output frequency, 100 MHz is chosen because oscillators with this frequency are abundant on the market and, since they are used in many other applications, they have more refined characteristics than specific frequencies developed for specific tasks. A number of different TCXO candidates from various manufacturers are compared in Table 3.1.

Manufacturer	Part Number / Series	Technology	Output Type	Frequency Stability (ppm)	Phase Noise (@10 kHz Offset) (dBc/Hz)	Jitter (ps)	Power Consumption (mW)	Surface Area (mm ²)
ECS	ETXO-L3	Crystal	LVDS	± 2.5	-120	0.8	82.5	8
Mercury	QMQF326	Crystal	LVDS	± 2	-122	1.1	79.2	8
NEL	AA-AAD	Crystal	LVDS	± 1	-140	0.2	132	39
SiTime	SiT5021	MEMS	LVDS	± 5	-132	0.6	155	8

Table 3.1: Comparison of 100 MHz TCXOs (typical values)

Because the QMQF326 series from Mercury has the lowest power consumption while providing similar or comparable performance figures, it has been chosen as the reference signal source for the frequency synthesizer [16].

To generate the LO signal for downconversion from the 100 MHz oscillator, a frequency synthesizer is employed. This approach not only enables the system to be tolerant against variations during operation, such as temperature change, or long-term effects such as aging, but also makes it possible to be used in different operation frequencies. For example, if the operation frequency is halved, then the same baseband signal can be generated by changing the synthesized frequency at the output. This agility does not require any hardware changes but is only implemented through software update. The sole restriction on the input RF signal to be downconverted is imposed by the allowed output frequency range of the synthesizer.

Furthermore, since an oscillator is already incorporated into the design, it can also be used for clock generation, which is required for the ADC(s). Combining similar functioning blocks together, the power consumption per channel is reduced. Although the output of the TCXO can be divided into two using resistive division, which can be used in the synthesizer and ADC clock generation, characteristics of the oscillator input of the synthesizer have direct impact on system phase noise and spurs produced at the output. For this reason, the output of the TCXO is not distributed to any other branch, instead it is fed to

the oscillator input of the synthesizer with the highest slew rate possible. This decision necessitates two outputs to be generated in the synthesizer: one for the downconversion and the other one for ADC clock generation. The LO frequency synthesized at the output cannot also be used for the generation of ADC clocks because its frequency is too high. On the market, there are few frequency synthesizers with integrated Voltage Controlled Oscillator (VCO) which can output two different frequencies while consuming low power. Using a synthesizer with an integrated VCO has the advantage of occupying less surface area and low power consumption compared to using a synthesizer with an external VCO. Synthesizers which completely or partially meet the mentioned requirements from various manufacturers are compared in Table 3.2.

Manufacturer	Part Number	Output Frequency (GHz)	Output Power (Min / Max) (dBm)	Normalized Phase Noise Floor (dBc/Hz)	Normalized 1/f Noise (dBc/Hz)	Phase Noise (@100 kHz Offset /w 100 MHz Carrier) (dBc/Hz)	RMS Jitter ($f_{out} = 2111 \text{ MHz}$) (fs)	Power Consumption (mW)	Surface Area (mm ²)
Analog Devices	ADF4351	.035-4.4	-4 / +5	-220	-116	-135	270	478	26
Renesas	8V97051L	.034-4.4	-4 / +7	-231	-122.8	-134	245	661	25
ST	STW81200	.046-6	-1 / +7	-227	Not Specified	-144	Not Specified	612	36
TI	LMX2572	.012-6.4	-10 / +9	-232	-123.5	-142	91	255	36

Table 3.2: Comparison of the Frequency Synthesizers (typical values)

LMX2572 from Texas Instruments has good noise performance and, by a wide margin, has the lowest power consumption [17]. Although it is not the smallest footprint synthesizer, due to its exceptionally low power consumption, it is the chosen frequency synthesizer for this work. Even though it has the lowest power consumption among other candidates, 255 *mW* power consumption only to generate the LO signal and the reference for the ADC clock signal does not fit into the total power budget spared for a single channel. Since the LO frequency is the same for every channel in the system, it is not required to be synthesized for each channel; instead, a generated one can be used for multiple channels. By doing so, the power consumption of the synthesizer per input channel is scaled down linearly according to the number of channels to which its output is distributed and this number is determined as the result of the ADC architecture used in the system discussed in Section 3.5.

The circuit design for the synthesizer together with the reference oscillator is given in Fig. 3.1.

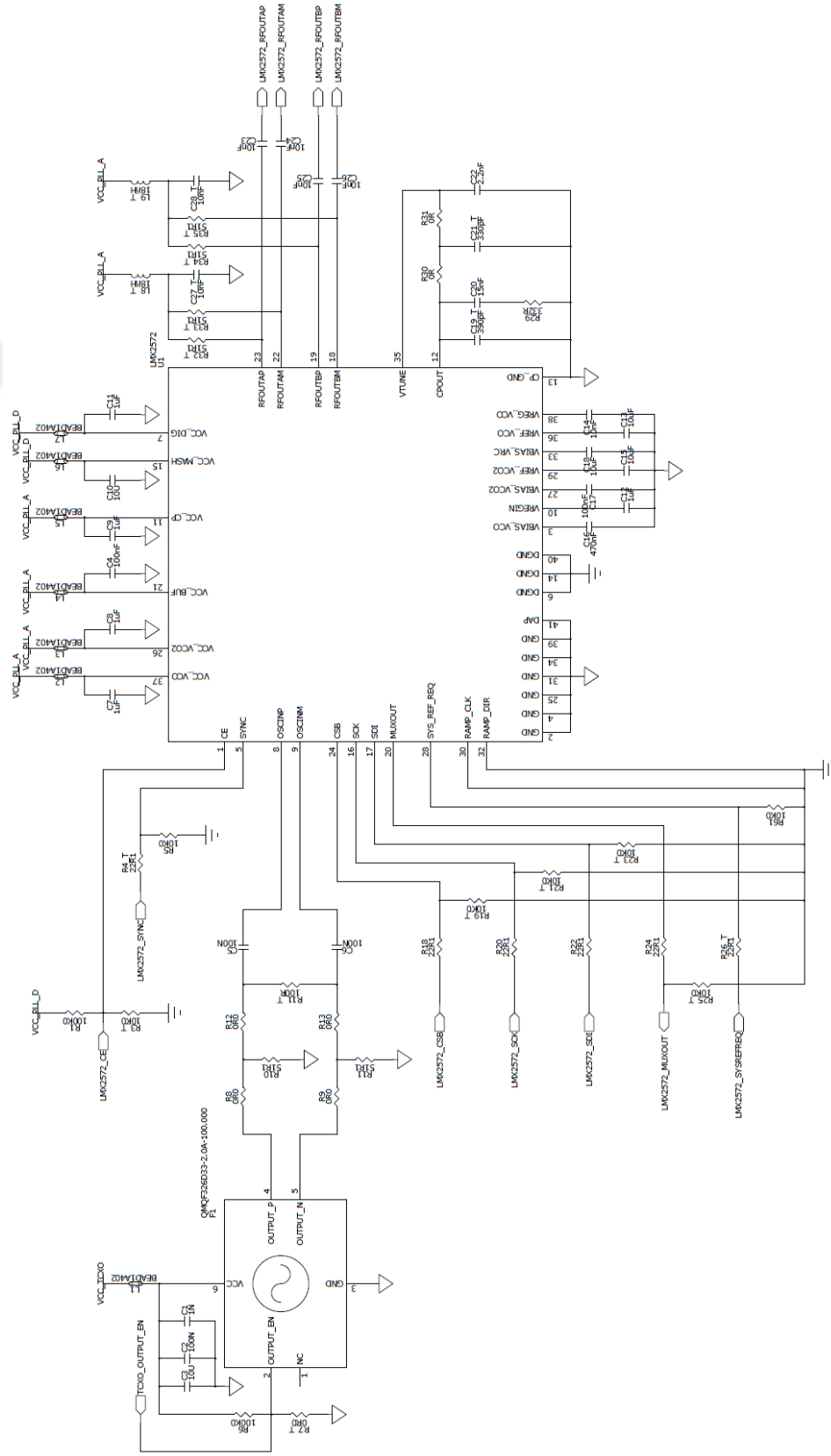


Figure 3.1: Reference Clock and Frequency Synthesizer Circuit

In the schematics, components whose names end with ”_T” denote parts which will not be placed during assembly; they are included in the schematics for debugging purposes or to provide flexibility in case needed.

For all active components in the design, a number of different value decoupling capacitors are placed at each of the power supply pins of the integrated circuits. While small-valued capacitors are included to suppress high frequency noise in power supply rails, large-value bulk capacitors are added to address demand for high currents.

Furthermore, power for each active component is supplied through a ferrite bead to filter high frequency noise, attenuate power supply cross talk, and provide an easy way to power off a specific component for debugging in case required.

Instead of supplying the power of the synthesizer through a single ferrite bead, in order to increase the fractional spur performance, a ferrite bead is placed at each of the power supply pins together with the mandatory decoupling capacitors.

TCXO output can be enabled or disabled by the microcontroller (MCU) on board for debugging; by default it is enabled via *R6*. As the output of the QMQF326 is of LVDS type, the differential clock input topology is used at the oscillator input pins. These input pins are internally biased; therefore, the TCXO output is AC-coupled through *C5* and *C6*.

Series resistors placed on digital Input-Output (IO) pins, coming from or going to the MCU, are to damp ringing, which may occur at high Serial Peripheral Interface (SPI) speeds. Together with the series resistors, the shunt resistors form a voltage divider, which will be used if the MCU output voltage levels are shifted to higher values.

With LMX2572, VCO bias, reference, varactor and regulator voltages; input reference path regulator voltage are generated internally. The maximum voltage level that is generated inside is not specified by the manufacturer. For this reason, bypass capacitors placed at these pins are selected so that they have equivalent or better voltage ratings than those used in the evaluation board of the synthesizer.

Texas Instruments recommends using *PLLatinum Sim* software to design the required external loop filter. This tool allows at most 4th order filters to be designed. To be able to implement the highest order filter, required circuit elements are included in the schematic. An example design generated by *PLLatinum Sim* is given in Fig. 3.2.

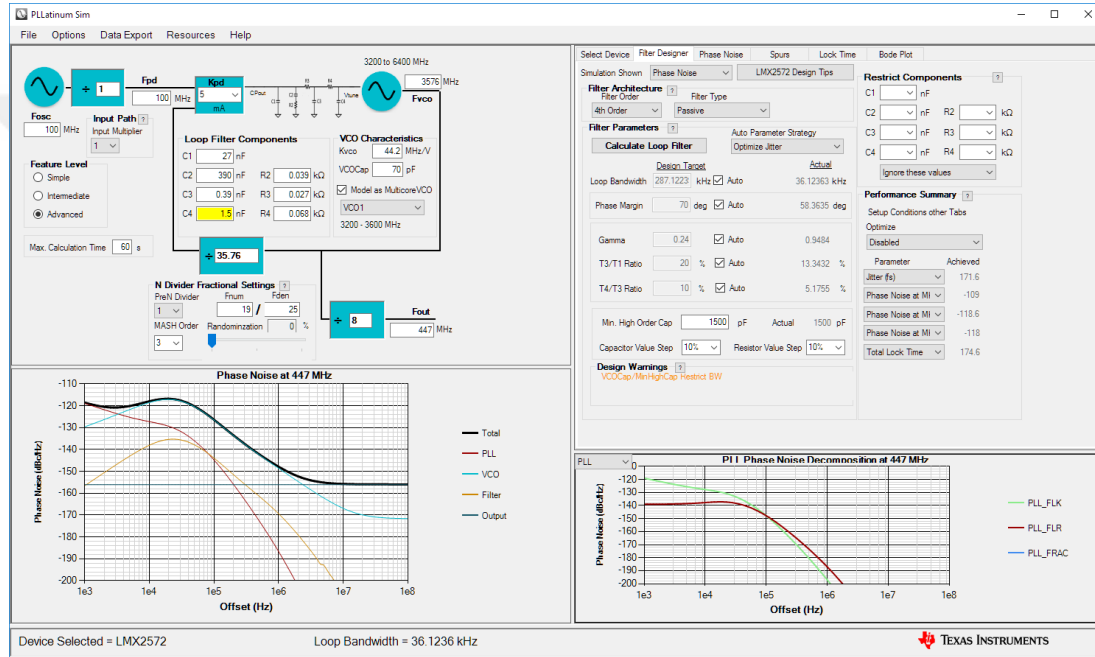


Figure 3.2: An Example 4th Order Loop Filter Design using PLLatinum Sim

The output pins are driven by low-impedance differential push-pull buffers and AC-coupled to drive the following devices. Since the output that is going to be used as the LO signal is of single-ended type, the unused pin is terminated while the used pin output is first filtered using a ceramic Low Pass Filter (LPF), LFCN-490+ from Mini-Circuits, and then fed into the power divider as in Fig. 3.3. The LPF is placed at the output of the synthesizer to attenuate high frequency signals above the desired frequency. LFCN-490+ has cut-off frequency of 650 MHz and attenuates signals in the frequency range 880 – 2500 MHz, in which the second harmonic of a 447 MHz signal would reside, by 40 dB [18].

The second output of the synthesizer is connected to CDCE6214, an ultra-low power clock generator with four differential outputs from Texas Instruments [19]. CDCE6214 is used to generate the required clock signals for the ADCs, and optionally it can be used to generate the MCU clock so that every time-dependent device is referenced to the same clock source.

Because differential signal is used for the primary reference input for increased signal integrity compared to a single-ended input, and since biasing of these input pins are performed internally, the primary reference signal is AC-coupled. A split termination network formed by $R103$, $R104$ and $C101$ is placed at these input pins.

For debugging purposes, a second reference source is also included in the design. It is a 25 MHz, fundamental order crystal unit with a drive level of 10 μW from NDK [20]. With this second reference, the ADC clock domain can be separated from the analog front-end, and sampling system characterization can be performed independently of the other blocks.

The clock generator can be configured to work with different power domains by supplying different voltage levels to the power supply pins. To enable modification of the system without altering the Printed Circuit Board (PCB), connections to these power pins are supplied through beads. By populating corresponding bead element, power domains are controlled for specific outputs. By default, internal functioning blocks and all outputs of the clock generator are powered from 1.8 V to reduce power consumption; however, they can be powered from 3.3 V to increase the slew rate of output signals, which would have an impact on ADC SNR performance. Moreover, power supply pins are isolated from each other using a separate bead for each one.

CDCE6214 is configured using the Inter-Integrated Circuit (I2C) interface, which requires data and clock lines to be pulled to VDD_REF . In addition to the I2C interface, there are also General Purpose Input-Output (GPIO) pins that can be used to monitor the lock status of the Phase-Locked Loop (PLL) or to enable or disable the outputs. Furthermore, it also includes a *Pin Mode* control, which

selects the power-up mode according to the voltage level applied to certain pins. For this reason, the *REFSEL* and *HW_SW_CT* pins include pull-up or pull-down resistors to be installed in case required.

The power-on-reset characteristics of CDCE6214 require the supply rails to reach their final value within the supply ramp time specification in a monotonic manner. If this condition is not guaranteed, then the *PDN* pin should be held low until the supply voltage reaches 95% of its final value. To ensure proper start-up, *C115* is placed on the *PDN* pin to delay the release of the reset signal.

3.2 Low Noise Amplifier

To keep the Signal-to-Noise Ratio of the system as high as possible, the first circuit element that the incoming RF signal encounters must be a Low Noise Amplifier (LNA). This requisite condition is a consequence of Friis' equation for the noise factor in cascaded systems, which is [21]:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_{n-1}} \quad (3.1)$$

where F_n is the noise factor for the n -th stage which has the power gain of G_n . Then, the first component, whose noise factor is directly added to the total noise factor, should be a low noise device, and since the contribution due to the second stage is weakened by the factor of G_n , the first device should have a high gain; hence the name Low Noise Amplifier.

A number of suitable LNA candidates for this work from various manufacturers are compared in Table 3.3.

Manufacturer	Part Number	Operating Frequency (MHz)	Gain (dB)	Noise Figure (dB)	Output P1dB (dBm)	Output IP3 (dBm)	Power Consumption (mW)	Surface Area (mm ²)
Infineon	BGA729N6	70-1000	16.3	1.25	Not Specified	Not Specified	17.65	0.77
Infineon	BGB719N7	10-1000	13.5	1.2	Not Specified	Not Specified	8.4	1.764
Macom	MAAL-011136	45-1218	20.3	1.1	16.5	32	159	18
Mini-Circuits	TSY-13LNB+	30-1000	14.7	1.2	17.1	26.4	21	4
NXP	BGA3018	5-1006	18	2.2	18	36	375	18
Skyworks	SKY67150-396LF	300-2200	23	0.45	19	36	410	4

Table 3.3: Comparison of Low Noise Amplifiers ($f_{in} \approx 500$ MHz, typical values)

While *SKY67150-396LF* from Skyworks has the lowest noise figure of 0.45 dB, it also has a dramatically high power consumption due to its wideband topology [22]. The solution offered by NXP has the highest noise figure and the second highest power consumption [23], while the Macom's has the third highest power consumption [24]. From a power consumption perspective, these three products are not preferred for this work. Both of the LNA solutions offered by Infineon have favorable noise and power consumption performance; but they are not fully characterized [25, 26]. TSY-13LNB+ from Mini-Circuits has a similar operating frequency range, gain, noise figure and comparable power consumption to those from Infineon while being fully characterized [27]. For these reasons, TSY-13LNB+ is used as the LNA in this design, and the circuit schematic for the LNA sections of a channel is given in Fig. 3.4.

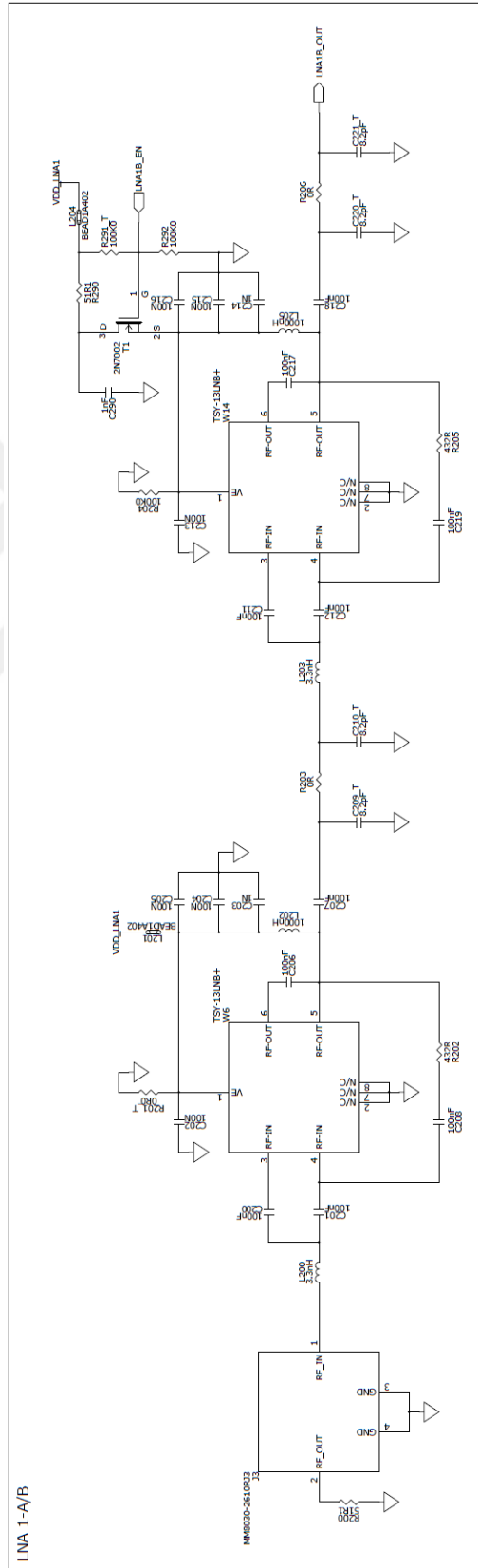


Figure 3.4: Low Noise Amplifier Circuitry

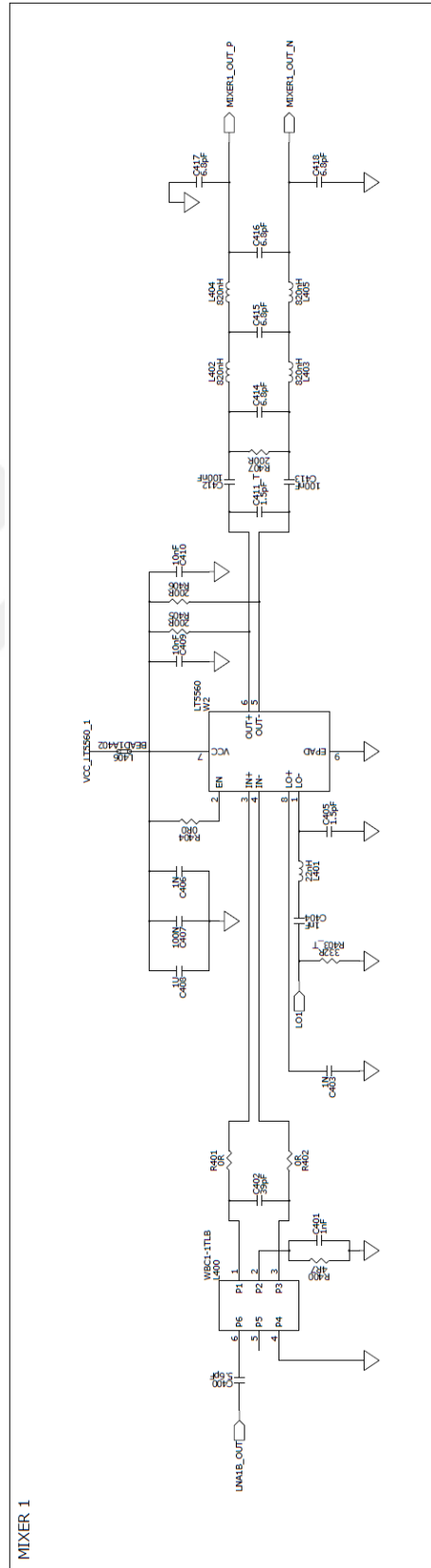
RF input to the system is supplied through a microwave coaxial connector, MM8030-2610 from Murata Electronics, which then goes into the LNA through DC blocking capacitors $C300$ and $C301$. The amplifier is biased using $L302$ and the supply line is filtered using multiple bypass capacitors and a ferrite bead. The LNA output also includes a DC blocking capacitor, $C307$.

In order to introduce system flexibility in terms of gain, a second LNA is included in the input signal chain. Contrary to the first LNA, which is configured to be always enabled by connecting its *Voltage Enable* (Ve) pin to V_{DD} , the second LNA can be enabled or bypassed over the MCU to implement an Active Gain Control (AGC) mechanism. The first LNA can also be bypassed manually by removing the ferrite bead at its supply and populating $R301_T$ if needed. If the noise due to a bypassed LNA, 0.8 dB, becomes a big concern, then the corresponding LNA can be removed from the circuit and the signal chain can be completed by replacing feedback components for that LNA, such as $C308$ and $R302$, with 0 Ω jumpers.

A π -attenuator network is placed at the output of each LNA for debugging, but is bypassed using 0 Ω jumpers by default.

3.3 Mixer

The amplified RF signal is downconverted using an active mixer, LT5560 from Analog Devices. Reasons for using an active mixer are discussed in Section 2.2.2 in depth, together with a comparison of mixers given in Table 2.2. Among active mixers, the LT5560 has the lowest power consumption with an acceptable required LO level and, thanks to these benefits, it is the chosen one for this work [28]. The circuit topology of the mixer section for a channel is given in Fig. 3.5.



The single-ended output of the LNA section is converted to a differential signal using a wideband transformer, WBC1-1TL from Coilcraft. It is the smallest footprint transformer with a surface area of 4 mm^2 and has a specified bandwidth ranging from 250 kHz to 750 MHz , which covers most of the operating frequency range of the LNA [29].

Although for an input signal with $f = 450 \text{ MHz}$ coming from a 50Ω source, which is the LNA in this case, is not required, an impedance matching network formed by $C400$, $C402$, $R401$ and 402 is included at the input pins. In case of need, 0402 package inductors of appropriate value should be populated in the 0 Ω jumper locations.

The supply current of the mixer is controlled through the resistor at the center tap of the input transformer, $R400$. An increase in this resistance value decreases the supply current at the cost of reduced linearity. As the supply current is lowered, Input 3rd-order Intercept Point IIP_3 and the gain decreases. A bypass capacitor, $C401$, is placed in parallel with the current-controlling resistor to minimize the effect on the noise figure.

The LT5560 is characterized using a single-ended LO drive, and the LO signal generated by the frequency synthesizer is also assumed to be single-ended. For this reason, the differential LO input capability of the mixer is not utilized; instead, the unused input is grounded using a capacitor, $C403$. The LO signal is fed to the remaining LO pin through a DC blocking capacitor, $C423$, as these pins are biased internally. Furthermore, a reactive matching network is also included on this pin, formed by 401 and $C424$, which has $390 - 605 \text{ MHz}$ matching bandwidth using the specified values.

The output pins are sourced from collectors of the mixer transistors, which require biasing. Since the Intermediate Frequency (IF) at the output is low, biasing is provided using pull-up resistors connected to the supply voltage, $R405$ and $R406$. To avoid disturbing this biasing, the output is coupled to the following section using blocking capacitors, $C412$ and $C413$.

A 5th order differential low-pass filter is placed at the mixer output to reject out-of-band frequency components that may appear as a result of mixing operation. Although the schematic includes symbols for the filter elements, the exact component values are left to be determined after assembly by observing the actual mixer output. To reduce the inductor count in the filter and eliminate the tuning and debugging difficulties introduced by serial capacitors, inductors are used as series elements [30].

Finally, a shunt capacitor is added to both outputs of the filter so that the source impedance seen by the following section, which is an ADC driver for this application, converges to zero at high frequencies.

3.4 Fully Differential Amplifier

Output of the mixer, which is the downconverted RF signal, is reconditioned before going into the ADC using a Full Differential Amplifier (FDA), THS4551 from Texas Instruments. In order to utilize full dynamic range of the ADC, the input signal should be adjusted according to the full-scale voltage. Furthermore, the insertion losses of the networks placed in between the driving circuit, which is the FDA in this case, and the ADC should be taken into consideration during scaling. The circuitry designed to accomplish the aforementioned functions is given in Fig. 3.6.

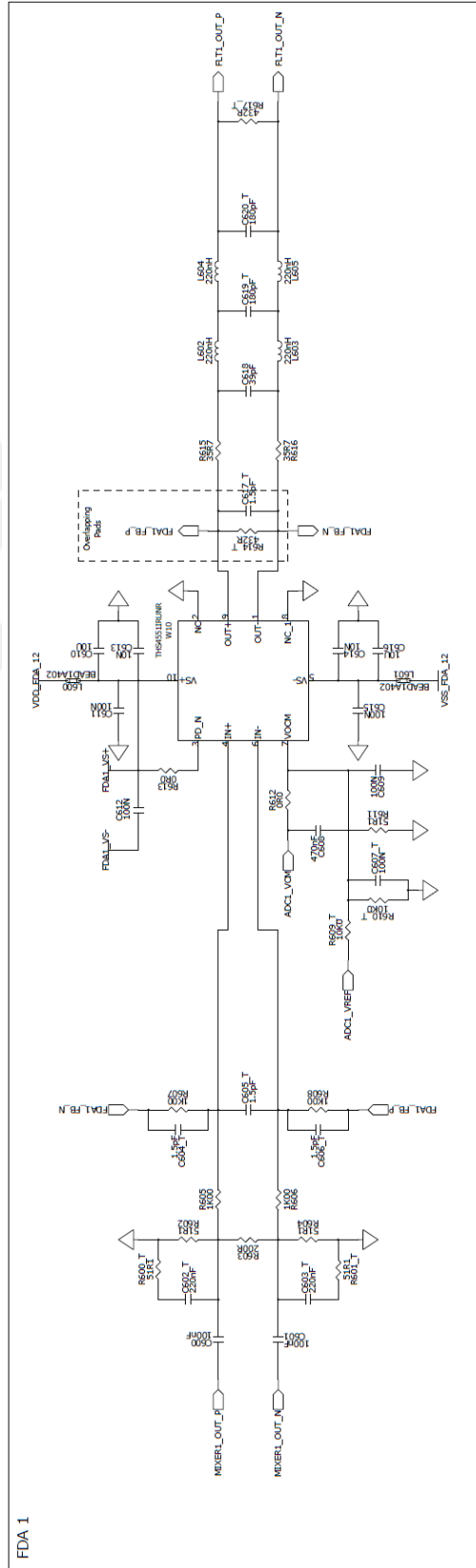


Figure 3.6: ADC Driver Circuitry

The output of the mixer stage is presented to the FDA through blocking capacitors, $C600$ and $C601$, followed by impedance matching circuitry to be used in case needed. Contrary to unpopulated elements in the matching circuitry, the input differential termination resistor $R603$ is included in the design by default, to allow usage of higher value gain setting resistors, $R605$ and $R606$ in this case, while providing low differential input impedance to the source [31].

FDA can be configured as an amplifier or attenuator, depending on the input signal level resulting from the previous sections. Since the exact values of filter elements at the mixer output is left to be studied, gain configuration for the FDA is to be determined afterwards. The resistor values in the feedback path, $R607$ and $R608$, are specified to provide unity gain by default. To implement a negative feedback topology, inverting output is fed to non-inverting input, and vice versa.

The output common mode voltage is configured to be supplied from the ADC; but it can be switched to be sourced from the reference voltage provided to the ADC as well.

The output of THS4551 can swing between 200 mV above and 200 mV below its negative and positive supply rails, respectively. However, with a single-supply operation, full-scale voltage swing at the ADC input pins may not be guaranteed. For this reason, a negative supply rail below the ground potential is provided to the FDA in addition to the requisite positive supply. A decoupling capacitor between negative and positive supply is also included in the design to improve the 2nd harmonic distortion performance [32].

The output of the FDA is filtered by a 5th order differential low-pass filter whose values are left to be determined once the gain is decided, and sent to ADC's input circuitry.

3.5 Analog-to-Digital Converter

As discussed in Section 2.2, baseband sampling of the downconverted RF signal approach is opted for this work. Since the downconverted signal has a low bandwidth, $BW \approx 1\text{ MHz}$, according to the sampling theorem of low-pass signals, an ADC with 2 Mega Samples per Second (MSPS) is sufficient for digitization. A comparison of the reviewed ADCs is given in Table 3.4.

Manufacturer	Part Number	Number of Channels	Resolution (Bits)	Sampling Rate (MSPS)	SNR (dBFS)	SFDR (dBFS)	ENOB (Bits)	Input Bandwidth (MHz)	Power Consumption (mW/Channel)	Surface Area (mm ²)
Analog Devices	AD4001	1	16	2	90.3 ¹	94 ¹	14.2 ¹	10	16	9
Analog Devices	AD4003	1	18	2	91.5 ¹	94 ¹	14.6 ¹	10	16	9
Analog Devices	AD4630-24	2	24	2	105.6 ²	Not Specified	17.04 ²	74	15	49
Analog Devices	AD7380	2	16	4	89 ²	Not Specified	14.47 ²	25	42	9
Analog Devices	AD7380-4	4	16	4	89.2 ²	Not Specified	14.47 ²	26.8	41	16
Analog Devices	LTC2269	1	16	20	84.1 ³	99 ³	13.64 ³	200	88	49
Analog Devices	LTC2271	2	16	20	84.1 ³	99 ³	13.64 ³	200	92	56
Analog Devices	AD9653	4	16	125	80 ⁴	94 ⁴	13 ⁴	650	168	49
Texas Instruments	ADS9110	1	18	2	89.3 ¹	106 ¹	14.45 ¹	88.5	15	16
Texas Instruments	ADS9120	1	16	2.5	84 ¹	106 ¹	13.65 ¹	88.5	15.5	16
Texas Instruments	ADS9224R	2	16	3	90.1 ¹	100 ¹	14.47 ¹	52	70	25
Texas Instruments	ADS5263	4	16	100	84.6 ⁴	80 ⁴	12.58 ⁴	700	355	81
Texas Instruments	ADC3581	1	18	10	84.5 ³	90 ³	13.7 ³	900	76	25
Texas Instruments	ADC3583	1	18	65	83.8 ³	89 ³	13.6 ³	900	122	25
Texas Instruments	ADC3664	2	14	125	77.5 ³	92 ³	12.6 ³	1400	100	25
Texas Instruments	ADC3681	2	18	10	84.5 ¹	90 ¹	13.7 ³	900	50	25
Texas Instruments	ADC3683	2	18	65	83.8 ³	89 ³	13.6 ³	900	94	25

Table 3.4: Comparison of ADCs (¹ $f_{in} = 0.5 \text{ MHz}$, ² $f_{in} = 0.1 \text{ MHz}$, ³ $f_{in} = 1 \text{ MHz}$, ⁴ $f_{in} = 10 \text{ MHz}$)

Although ADS9110 offers the best power consumption performance per SNR figure, its dynamic performance gradually decreases as the input frequency increases [33]. It has no margin left for imperfections that may occur in the real system. This is the case for most of the ADCs given in the table. However, ADC3683 offers the optimum performance in terms of power consumption and dynamic performance, given that it is a 65-MSPS ADC that can benefit from the process gain as described in Equation 2.8 [34]. For this reason, ADC3683 is used in this work as the sampling ADC.

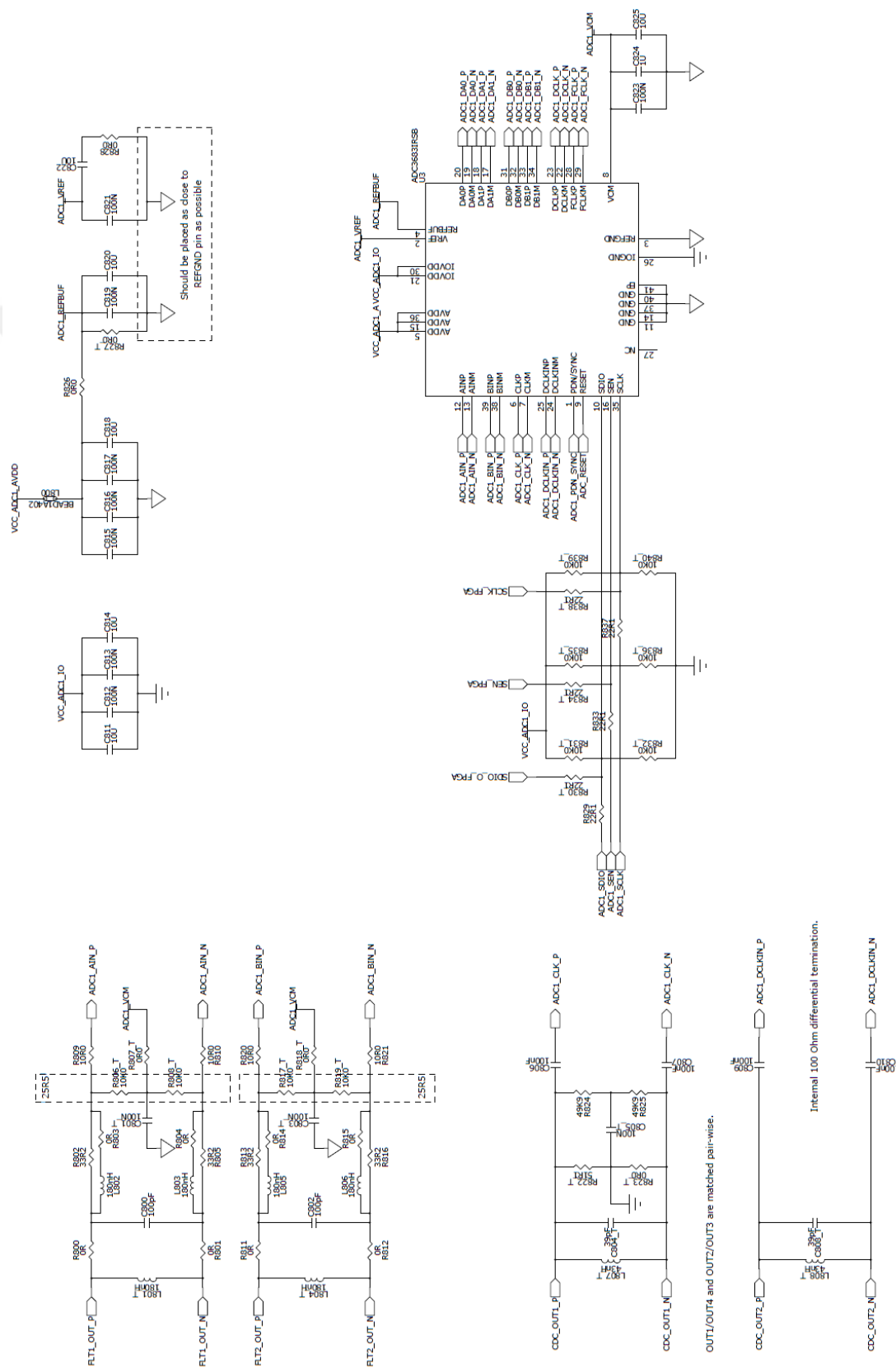
ADC3683 is a dual-channel ADC that can perform sampling on two different channels at the same time, in the same package. This feature of it leads to one of the major design decisions on the overall system. As discussed in Section 3.1, considerable amount of power budgeted is spared for the generation of the LO signal and the power consumption per channel is to be lowered by reusing the same LO signal in different channels. This number of channels is decided according to the number of input channels of the ADC. Using only one ADC with dual input channels in a subsystem does not meet the estimated power budgeted. Using two ADCs with a total of four input channels divides the total power consumption of the frequency synthesizer to four and offers a symmetrical module design where each input is placed at four corners of the PCB. Increasing the number of ADCs to three introduces asymmetry in placement, and four ADCs with eight channels or eight ADCs with sixteen channels increases the system complexity. Therefore, it was decided that the use of two ADC3683 with a total of four input channels offers optimum design reuse, power consumption and complexity.

Another advantage of using two ADCs in a module is that four outputs of the clock generator can be utilized. ADC3683 requires two input clocks: *CLK* and *DCLKIN*, the former one is for sampling and the latter one is used for data outputting. These clocks must be frequency locked, but do not need to be in phase since the phase difference is corrected internally [35]. The clock generator uses the same reference signal to generate all of its outputs; therefore, they are all synchronous.

By using two ADCs, not only all of the outputs of the clock generator utilized,

but the total number of signals that are going out of the module is also reduced. ADC3683 outputs two clocks: *DCLK* and *FCLK* along with data to make it possible for the receiving system to capture the data at the correct time instances. Normally, for a system with two independent ADCs, these two clocks must be delivered to the receiving system for proper functioning; however, in this case, since *DCLKIN* for both ADCs are also synchronous, only one pair of *DCLK* and *FCLK* transmission is sufficient for correct operation.

Regarding these design considerations, the schematic for one ADC is given in Fig. 3.7.



Because OUT1/OUT4 and OUT2/OUT3 of the clock generator are matched pairwise within 100 *ps* skew, to be able to use a single pair of *DCLK* and *FCLK* at the receiving system, OUT1 and OUT2 are used as the *CLK* and *DCLKIN* respectively with the first ADC, while OUT3 and OUT4 are used with the second ADC. Since for *DCLKIN* inputs, internal termination is provided by the ADC, no external termination is placed on these lines, unlike the *CLK* inputs, which include external termination.

Being an unbuffered ADC, meaning that the input pins do not include the requisite circuitry to absorb the transient charging spikes of the following sampling circuitry, ADC3683 requires a glitch filter at its input pins. It is formed by *C800*, *R802*, *R803*, *R804*, *R805*, *R809*, *R810*, *L802* and *L803* for channel A. Since the output of the FDA is DC-coupled to the input of the ADC and the DC bias is provided according to *VCM* by the FDA, the bias network elements in the glitch filter are not populated.

ADC3683 is able to generate the voltage reference internally; however, it can be supplied externally as well. Independent of the source, bypass capacitors at the *VREF* pin are recommended by the manufacturer and included in the design as *C821* and *822*. The reference voltage source is selected according to the voltage level at *REFBUF* pin during power-up by default. To select the external reference option, it is pulled up to *AVDD* through *R826*.

3.5.1 ADC Supplementary Circuits

Instead of using an internally generated voltage reference for ADCs, an external source is used for better accuracy and improved temperature drift [36]. REF3318 is a low-power and low-dropout voltage reference from Texas Instruments [37]. Its output is fixed 1.8 *V*, whereas ADC3683 expects 1.6 *V*; therefore, it should be scaled accordingly. Furthermore, the ADC draws about 1 *mA* load current from the reference. Although REF3318 is specified for ∓ 5 *mA* output current, to keep the dropout voltage as low as possible, its output is buffered using an opamp, OPA837 from Texas Instruments. This circuit is shown in Fig. 3.8.

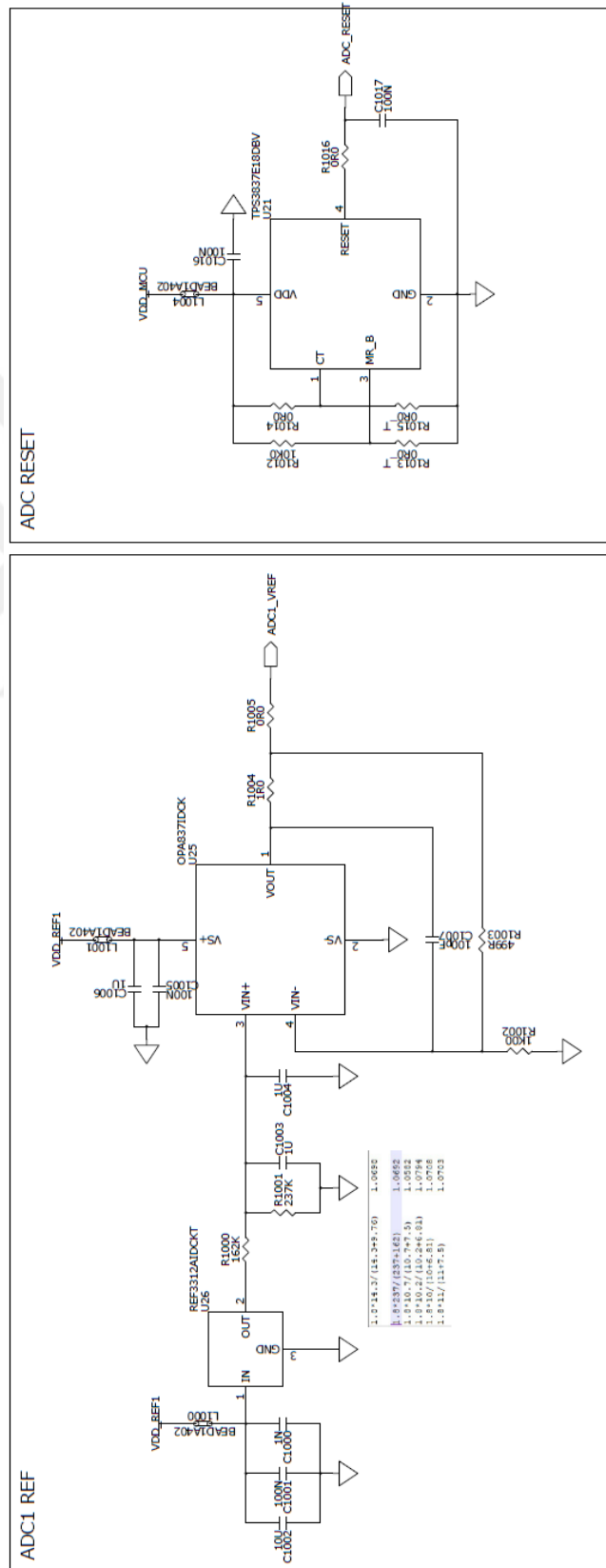


Figure 3.8: ADC Auxiliary Circuitry

ADC3683 requires a tailored power-up sequence for proper initialization. 2 *ms* after power is supplied to the *VDD* pins, a reset signal with at least 1 μs high duration must be applied to the *RESET* pin in order to initialize internal registers to their default values. This reset signal is generated from a supervisory circuit, TPS3837 from Texas Instruments. It has a selectable reset delay, configured using the *CT* pin, which is set to 200 *ms* through *R1014* [38].

3.6 Electrical-to-Optical Conversation

ADC data is transmitted to the processing system through an optical link. The electrical outputs of the ADCs are converted to optical signals using fiber optic transmitters. Similarly, control signals coming to the module through an optical link are converted to electrical signals using a fiber optic receiver. Some of the fiber optic transmitter, receiver and transceiver products offered by Broadcom are compared in Table 3.5.

Part Number	Function	Data Rate (MBd)	Wavelength (nm)	Power Consumption (mW)	Surface Area (mm ²)
AFBR-5972Z	Transceiver	250	650	300	342
AFBR-1624Z	Transmitter	50	650	70	195
AFBR-2624Z	Receiver	50	650	66	195
HFBR-1527ETZ	Transmitter	125	650	300	190
HFBR-2526ETZ	Receiver	125	650	75	190
HFBR-1424Z	Transmitter	160	820	500	250
HFBR-2426Z	Receiver	160	820	50	250
HFBR-1312TZ	Transmitter	155	1300	500	405
HFBR-2316TZ	Receiver	155	1200	50	405

Table 3.5: Comparison of Fiber Optic Transmitters, Receivers and Transceivers from Broadcom

For a unidirectional unit, as the wavelength increases, the size of the module tends to increase as well. Among these optical transceivers, the AFBR-x624Z series offers the lowest power consumption in a feasible surface area; however, it has a limited data rate. To overcome this issue, the internal functions of the ADC are utilized. Although output data rate of the ADC can be as high as 1000 *Mbps* for a given sampling rate, serial interface and output formatting configuration,

sending out such a signal through an optical link while consuming low power is not possible according to the power consumption values reported in the table. However, since the bandwidth of the target signal is low, the internal decimation filter feature of the ADC can be used to reduce the data rate and effectively the power consumption. For example, using sampling frequency $F_s = 65 \text{ MSPS}$, a complex decimation by 32 would result in a 2.03125 MSPS complex output data rate while allowing an output bandwidth of 1.625 MHz , which is sufficient for this work. Furthermore, output interface can be implemented as 1/2-Wire, 1-Wire or 2-Wire; while output resolution can be chosen as 14-bits, 16-bits, 18-bits or 20-bits. These settings determine the serialization factor at the output data pins, and can be as high as $40x$. Even though using lower output resolution decreases the required optical bandwidth, it corresponds to truncation of LSBs, which also decreases fidelity as well. Decimation filter operations are performed using 20-bit resolution, so that the SNR is not degraded due to quantization noise. Decimation filtering is one of the enabling features of the ADC that makes it possible to implement the overall function of the system in a low power budget.

Since the output of the ADC is differential and the AFBR series accepts single-ended input, a differential line receiver, SN65LVDT386 from Texas Instruments, is placed between the ADC and the optical transmitters. Unlike some differential receivers, SN65LVDT386 has integrated line termination resistors, which eliminates the need for external resistors.

The schematics for the optical receiver and transmitter circuitry together with the single-ended to differential converter section are given in Fig. 3.9.

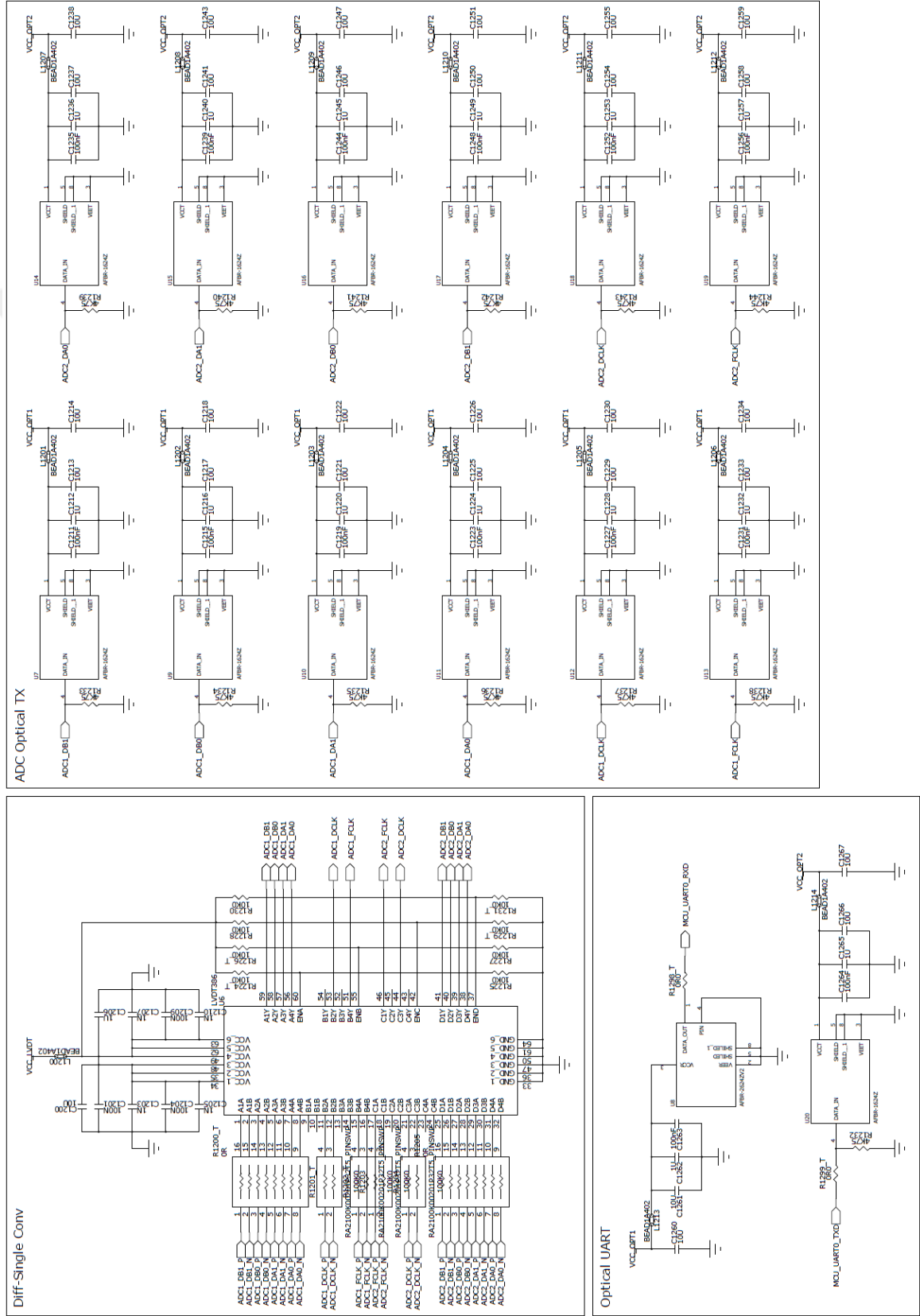


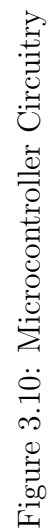
Figure 3.9: Optical Interface Circuitry

In addition to twelve optical transmitters, a transmitter and a receiver module are included in the design to implement the control interface. Electrical connections of these modules are connected to the microcontroller, and the Universal Asynchronous Receiver-Transmitter (UART) protocol is to be implemented between the module and the control station.

3.7 Microcontroller

In order to configure and control the components in the module, a microcontroller unit (MCU), ADuCM3029 from Analog Devices, is used. It is an ultra-low power Arm Cortex-M3 MCU that consumes $30\mu A/MHz$ dynamic current in active mode [39]. For the digital periphery, it has 3 SPI, 1 I²C and 1 UART interface. For clocking, 26 *MHz* and 32 *kHz* oscillators are provided on the chip; however, if required, the clock can be supplied externally for synchronous operation with the rest of the system.

MCU pin connections together with the mode selection and reset circuitry is given in Fig. 3.10. The reset signal can be asserted by the ADC supervisor circuit during start-up; however, by default, it is left to be governed by the external debug and programming circuitry.



3.8 Debug Interface

For easy and fast debugging or characterization purposes, a debug interface is also included in the design. With this interface, optical connections can be isolated from rest of the system, and ADC output can be analyzed on a computer.

Texas Instruments offers a data capture board, namely TSW1400EVM, which is capable of connecting ADC3683's evaluation module, ADC3683EVM, through a high-speed connector. The same terminal used in the ADC3683EVM is also used in this design with the same connections to the same pins to enable seamless integration with the data capture board. This electrical debug interface for the ADC output, together with the JTAG interface for MCU programming and debugging is shown in Fig. 3.11.

Series resistors at the ADC output lines are used to steer ADC signals either to optical interface or to debug interface. Depending on the populated resistor array, the destination of the ADC signals is determined, and by default, the ADC1 output is connected to the debug interface, while the ADC2 output is connected to the optical interface.

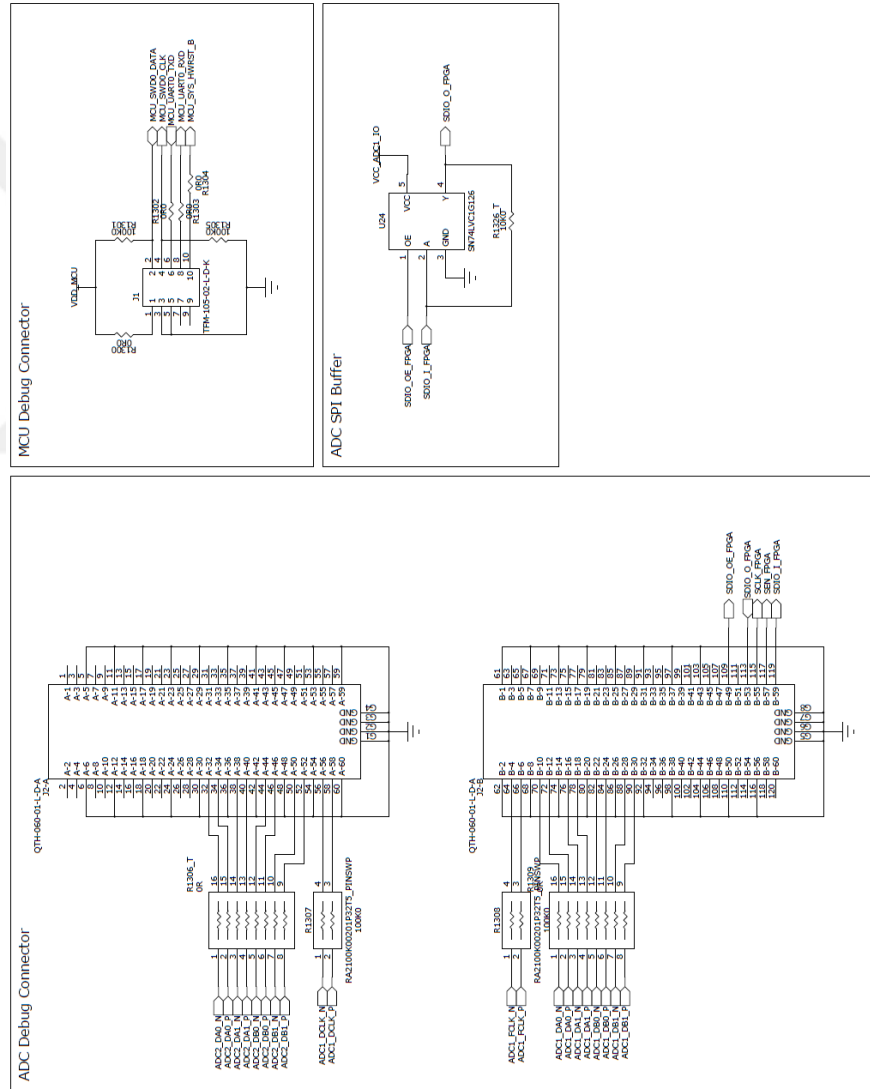


Figure 3.11: Debug Interface

3.9 Power Supplies

Similar to the interconnections of the digital interface, the power required for the module is also assumed to be delivered by optical connections. Unfortunately, the readily available photovoltaic power converter (PPC) modules on the market do not satisfy the size and material requirements of this work. Because the efficiency figures for these modules are on the order of 30%, they are prone to heating [40]. To help this problem, manufacturers use bulky heat-dissipative metal housings, which violates the design requirements. We have contacted MH GoPower and Lumentum to assess the feasibility of the development of MRI-compatible PPCs. At the end of the discussion, it is concluded that although it is technically possible to develop PPCs without ferromagnetic metals, because of the development costs, it is left for future studies.

For rapid prototyping, two electrical terminals are used as the power input to the module. The power supply circuitry is then divided into multiple domains using a DC/DC converter for each domain. By doing so, components that belong to one domain are isolated from the rest of the circuitry, and the voltage level for that domain can be individually adjusted. To enable tuning of the voltage of a domain, instead of using fixed output voltage converters, adjustable output voltage converters are used in each of the branches. To generate positive rails, TPS62150s from Texas Instruments are used, and for negative rails, it is TPS63710. A portion of the power supply circuitry is given in Fig. 3.12

To be able to bypass the DC/DC converters and supply power directly from an external source for debugging purposes, ferrite beads are placed between the input and output pins of each converter.

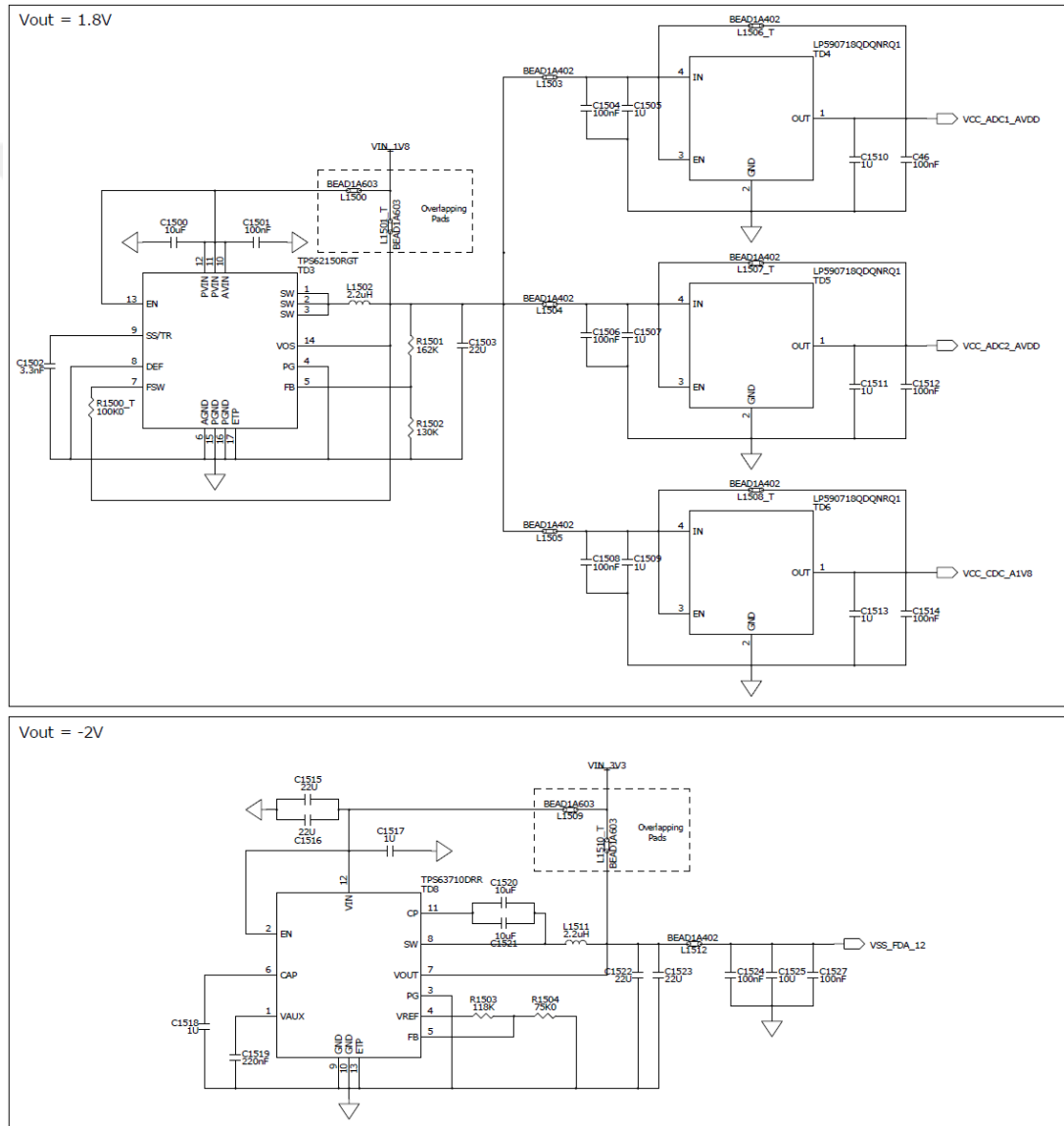


Figure 3.12: Part of the Power Supply Circuitry

Chapter 4

PCB Design

Layout of the schematics discussed in Chapter 3 determines the cross-sectional area of the design. Since the use of the cross-sectional area is one of the design criteria, the layout step is performed with diligence. The design of the PCB starts with determination of the stack-up and the trace properties are adjusted accordingly. Finally, circuit components are placed on the board in a precise manner with respect to design and performance requirements. Each of these design steps are reviewed in detail in the following sections.

PADS Layout VX.1.1 from Mentor Graphics is used to design the PCB and HyperLynx v9.2 is used for stack-up & trace characteristics analysis.

4.1 Stack-Up Design

Stack-up of the PCB is carefully determined to allow the placement of the circuit to be as compact as possible while taking the manufacturing costs into account. Although increasing the number of layers eases the layout process, it also dramatically increases the cost. As a moderately dense board, it was decided that a 12-layer PCB is adequate to implement the design. After completing the layout, we have seen that a 10-layer PCB would not be sufficient. Furthermore, for signal

integrity and power delivery, the module might benefit from a 14-layer PCB.

For optimal RF performance, a low-loss dielectric material, Rogers RO3450B, is used for the outer layers onto which the components are soldered. To enhance robustness against an increase in temperature, high T_g FR4 material is used for the inner layers.

The pin pitch of the MCU is 0.35 mm [39]. Even using state-of-the-art manufacturing processes, with 0.1 mm drill size, $75\text{ }\mu\text{m}$ annular ring width and $75\text{ }\mu\text{m}$ spacing, it is not possible to fan-out all I/Os in the package using via-in-pad [41]. Since the drill size is another important factor in the production cost, instead of using 0.1 mm as the diameter length, vias with 0.15 mm drill size are used for signal routing and 0.3 mm for power carrying throughout the board. With these drill sizes, to reduce the aspect ratio and therefore the cost of the PCB as much as possible, the total thickness of the board is kept below 1.6 mm by using thin core materials. With regard to these design considerations, stack-up of the PCB is determined to be as in Fig. 4.1

	Visible	Color	Pour Draw Style	Layer Name	Type	Usage	Thickness μm	Technology	Er	Metal	Bulk R ohm-m	T coef 1/°C	Loss Tangent
1					Dielectric	Solder Mask	12.7		3.3				0.02
2					Metal	Plating	2		3.3	Gold	2.439e-008	0.00396	0
3					Metal	Plating	17		3.3	Copper	1.724e-008	0.00393	0.02
4	✓	Red	Hatched	Top	Metal	Signal	18		3.3	Copper	1.724e-008	0.00393	0.02
5				Substrate	Dielectric	Substrate	101	Prepreg	3.66				0.002
6	✓	Yellow	Solid	GND1	Metal	Plane	18		3.2	Copper	1.724e-008	0.00393	0.002
7				Substrate	Dielectric	Substrate	100	Core	3.7				0.002
8	✓	Magenta	Hatched	S1	Metal	Signal	18		3.2	Copper	1.724e-008	0.00393	0.002
9				Substrate	Dielectric	Substrate	106	Prepreg	3.65				0.002
10	✓	Blue	Solid	GND2	Metal	Plane	18		3.2	Copper	1.724e-008	0.00393	0.002
11				Substrate	Dielectric	Substrate	100	Core	3.7				0.002
12	✓	Orange	Hatched	S2	Metal	Signal	18		3.2	Copper	1.724e-008	0.00393	0.002
13				Substrate	Dielectric	Substrate	188	Prepreg	3.65				0.002
14	✓	Cyan	Hatched	PWR1	Metal	Plane	18		3.2	Copper	1.724e-008	0.00393	0.002
15				Substrate	Dielectric	Substrate	100	Core	3.7				0.002
16	✓	Dark Red	Hatched	PWR2	Metal	Plane	18		3.2	Copper	1.724e-008	0.00393	0.002
17				Substrate	Dielectric	Substrate	188	Prepreg	3.65				0.002
18	✓	Green	Hatched	S3	Metal	Signal	18		3.2	Copper	1.724e-008	0.00393	0.002
19				Substrate	Dielectric	Substrate	100	Core	3.7				0.002
20	✓	Purple	Solid	GND3	Metal	Plane	18		3.2	Copper	1.724e-008	0.00393	0.002
21				Substrate	Dielectric	Substrate	106	Prepreg	3.65				0.002
22	✓	Teal	Hatched	S4	Metal	Signal	18		3.2	Copper	1.724e-008	0.00393	0.002
23				Substrate	Dielectric	Substrate	100	Core	3.7				0.002
24	✓	Dark Blue	Solid	GND4	Metal	Plane	18		3.2	Copper	1.724e-008	0.00393	0.002
25				Substrate	Dielectric	Substrate	101	Prepreg	3.66				0.002
26	✓	Dark Green	Hatched	Bottom	Metal	Signal	18		3.3	Copper	1.724e-008	0.00393	0.02
27					Metal	Plating	35		3.3	Copper	1.724e-008	0.00393	0.02
28					Metal	Plating	2		3.3	Gold	2.439e-008	0.00396	0
29					Dielectric	Solder Mask	12.7		3.3				0.02

Figure 4.1: Stack-Up of the PCB

The cross-section of this stack-up is visualized in Fig. 4.2 in which each layer is drawn proportionally with respect to its thickness.

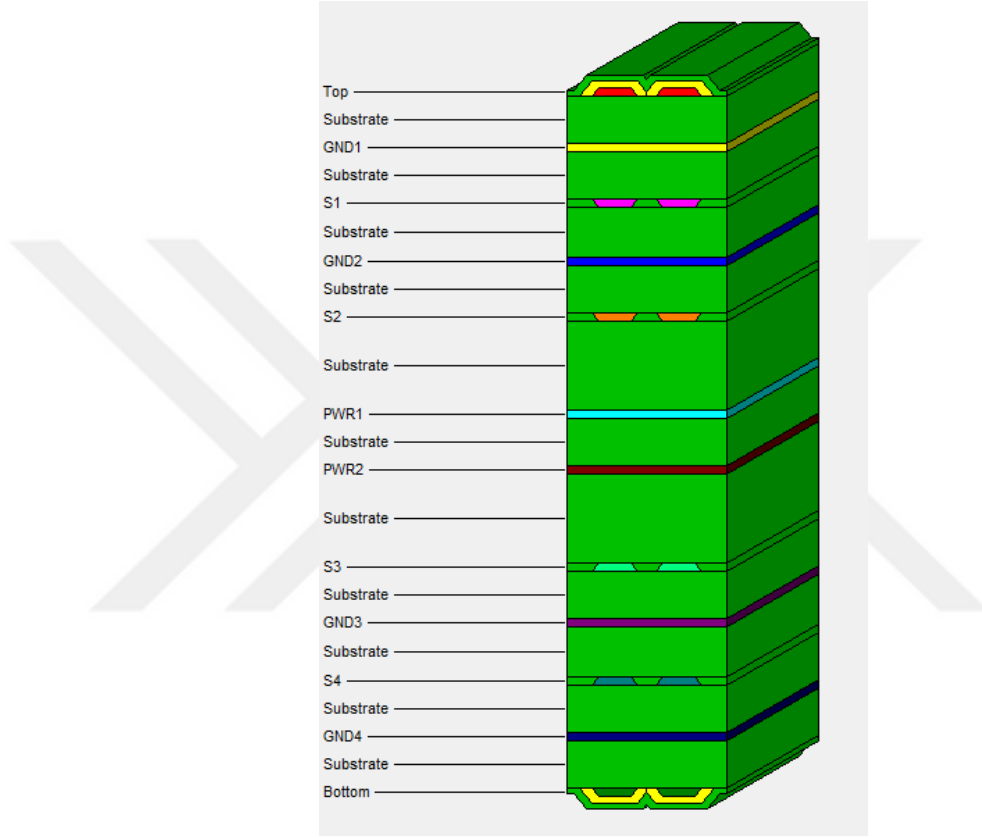


Figure 4.2: Cross-Section of the Stack-Up

As can be seen in the figure above, the power layers ($PWR1$ and $PWR2$) are further separated from the signal layers by using thicker substrates in between so that the reference layers for the signal layers $S2$ and $S3$ are $GND2$ and $GND3$ ground planes, respectively; instead of noisy and fragmented power layers.

4.1.1 Trace Properties

In order to achieve $50\ \Omega$ impedance for single-ended traces and $100\ \Omega$ impedance for differential traces, the width and spacing configurations are determined to be as in Fig. 4.3. Calculations for ground and power planes should be ignored, as no traces are routed on them.

	Visible	Color	Pour Draw Style	Layer Name	Test Width μm	Z0 ohm	Diff Z0 ohm	Width μm	Gap μm
1									
2									
3									
4	☒	Red	Hatched	Top	175	51.6	100	80	71.85
5				Substrate					
6	☒	Yellow	Solid	GND1	100	79	100	100	79.223
7				Substrate					
8	☒	Magenta	Hatched	S1	95	50.1	100	80	123.455
9				Substrate					
10	☒	Blue	Solid	GND2	100	71.6	100	100	85.296
11				Substrate					
12	☒	Orange	Hatched	S2	120	50.4	100	80	93.058
13				Substrate					
14	☒	Cyan	Hatched	PWR1	100	57.3	100	100	130.847
15				Substrate					
16	☒	Dark Red	Hatched	PWR2	100	57.3	100	100	130.847
17				Substrate					
18	☒	Green	Hatched	S3	120	50.4	100.5	80	95.036
19				Substrate					
20	☒	Purple	Solid	GND3	100	71.6	100	100	85.296
21				Substrate					
22	☒	Teal	Hatched	S4	95	50.1	100.2	80	125.063
23				Substrate					
24	☒	Dark Blue	Solid	GND4	100	79	100	100	79.223
25				Substrate					
26	☒	Dark Green	Hatched	Bottom	175	50.1	99.6	80	92.408
27									
28									
29									

Figure 4.3: Stack-Up of the PCB

For differential traces, it is possible to use different width and spacing pairs while attaining the same $100\ \Omega$ differential impedance given the layer thicknesses. Moreover, the thickness of the trace has an impact on signal attenuation, and the trade-off between these parameters should also be taken into account. The loss versus frequency for the above configuration is plotted in Fig. 4.4 and for the signals of interest these levels are in moderate order considering that the routing distances are short within the design.

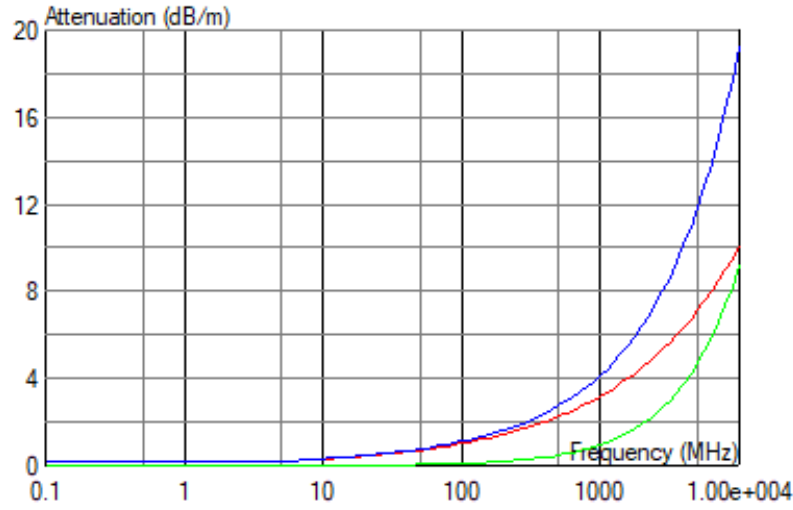


Figure 4.4: Loss vs Frequency Graph (Blue: Total, Red: Resistive, Green: Dielectric)

4.2 Circuit Placement

As discussed in Chapter 3, a varying number of decoupling capacitors are placed at the power pins of the integrated circuits. Small-size, high-frequency coupling capacitors are placed as close to power pins in the layout, whereas higher-value capacitors are placed around the vicinity of the IC.

Via sharing is omitted as much as possible; hence, almost for every power and ground connection, at least one via is placed at the component's pin. Furthermore, for low-inductance connections, multiple stitching vias are preferred whenever possible.

For every active component with an exposed thermal pad in the design, the maximum number of full-through vias are used for connection to the solid ground planes in order to increase thermal conductance.

The pads of the power steering ferrite beads are placed such that they overlap with each other to prevent connection to two different voltage levels at the same time and to save valuable board area.

The circuit components related to the incoming high-frequency MRI signal are placed only on one side of the board, the bottom layer, so that the RF signal is routed only on this layer without going through vias. Furthermore, the RF signal is delivered to the input pins of the mixer using short traces as much as possible while the total path length is mostly attained by the passive components. Lastly, to direct the RF signal, instead of using bent traces, a direction change is performed at the passive component pins.

Since the input and output pins of the FDA are sensitive to capacitive effects, both the ground and power planes on all layers are opened up around these pins. Instead of *201* package resistors, *402* ones are chosen to reduce the trace length in the feedback path [31].

The external component placement for the ADC input pins are kept symmetrical for both inputs. The corresponding traces across the ADCs are routed using the tolerance of 0.1 mm length difference. First, the longest path is determined for a signal group, and the remaining signals within that group are length-matched to this trace using meandering. This length matching is not only applied to ADC signals, but is also practiced for rest of the delivery time critical signals to keep phase of each channel equal.

Taking these design details into account, the PCB layout is finalized as in Fig. 4.5.

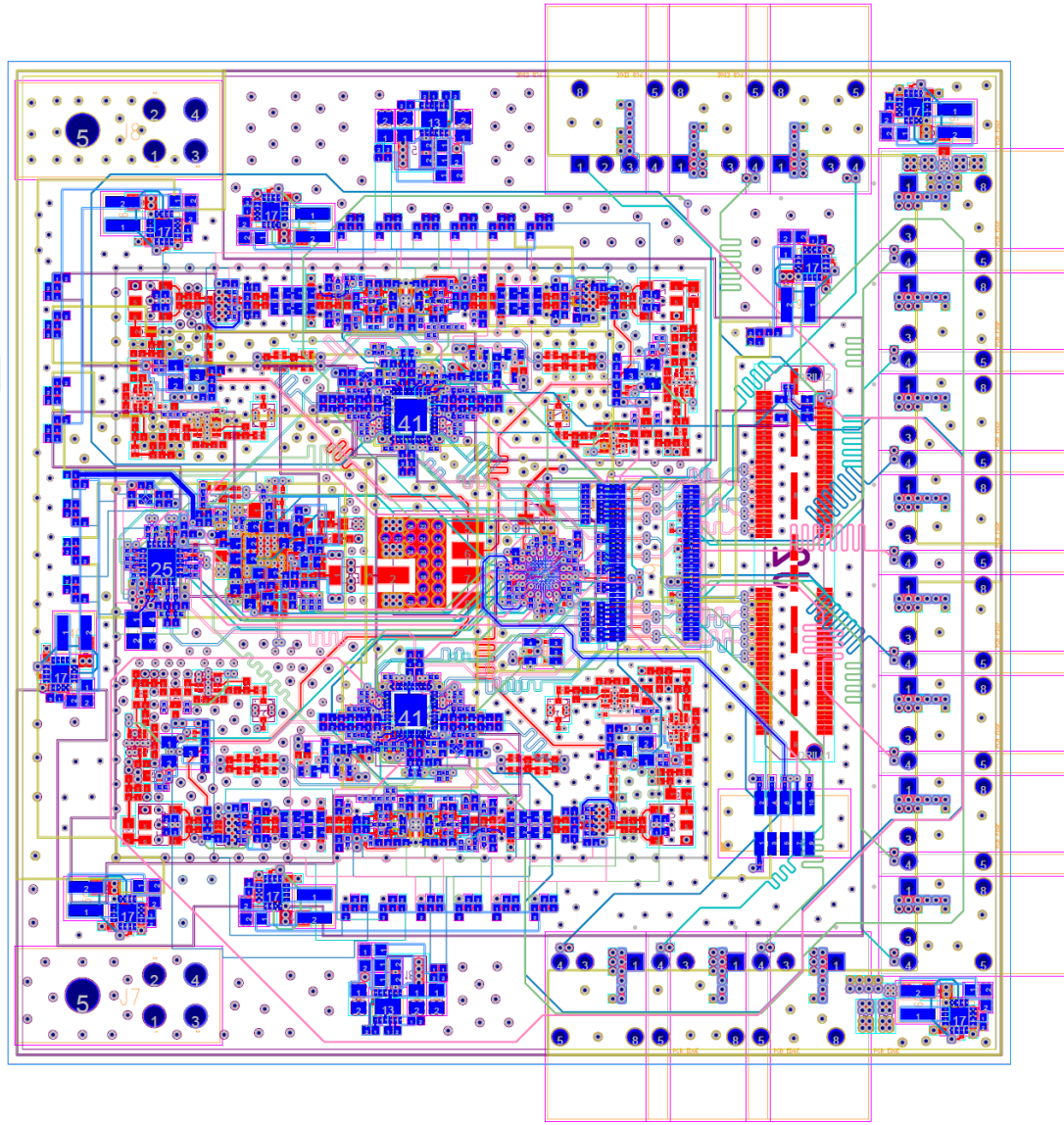


Figure 4.5: Final Design of the PCB

The corresponding 3D visualization for the top and bottom sides of the board is shown in Fig. 4.6 and Fig. 4.7, respectively.

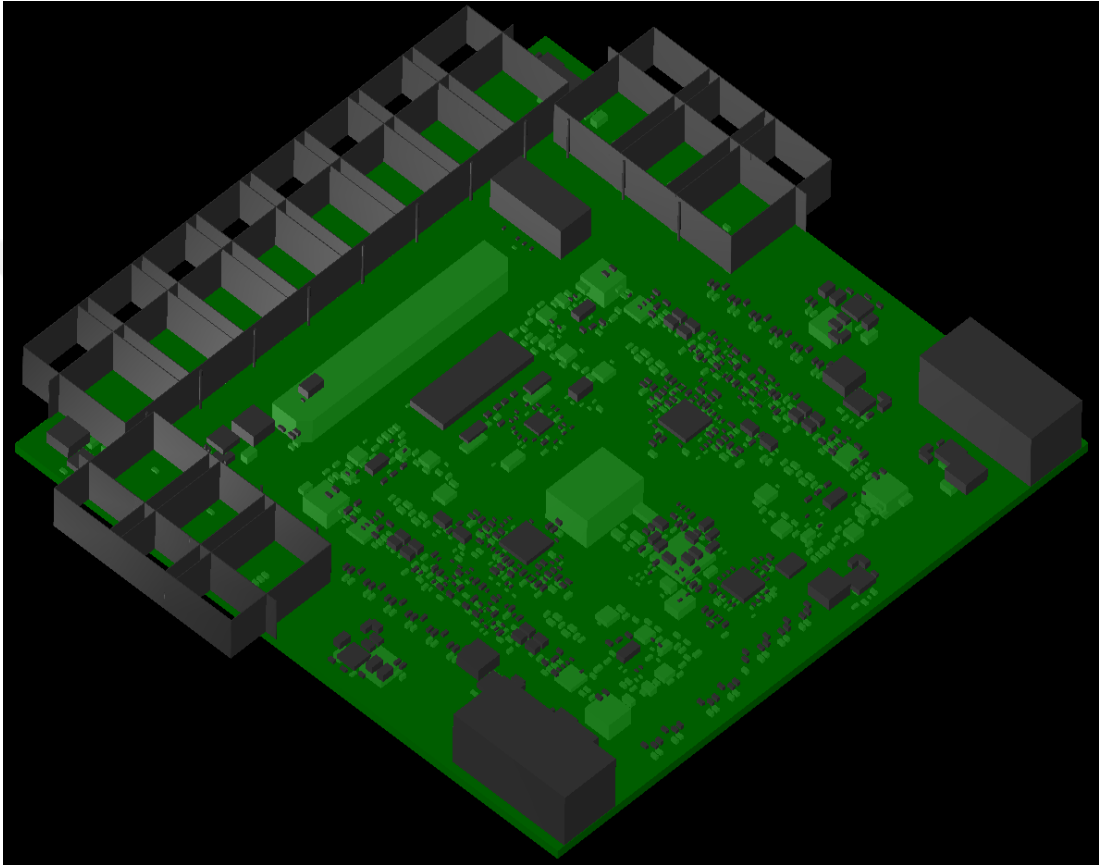


Figure 4.6: 3D Visualization of the Top Side

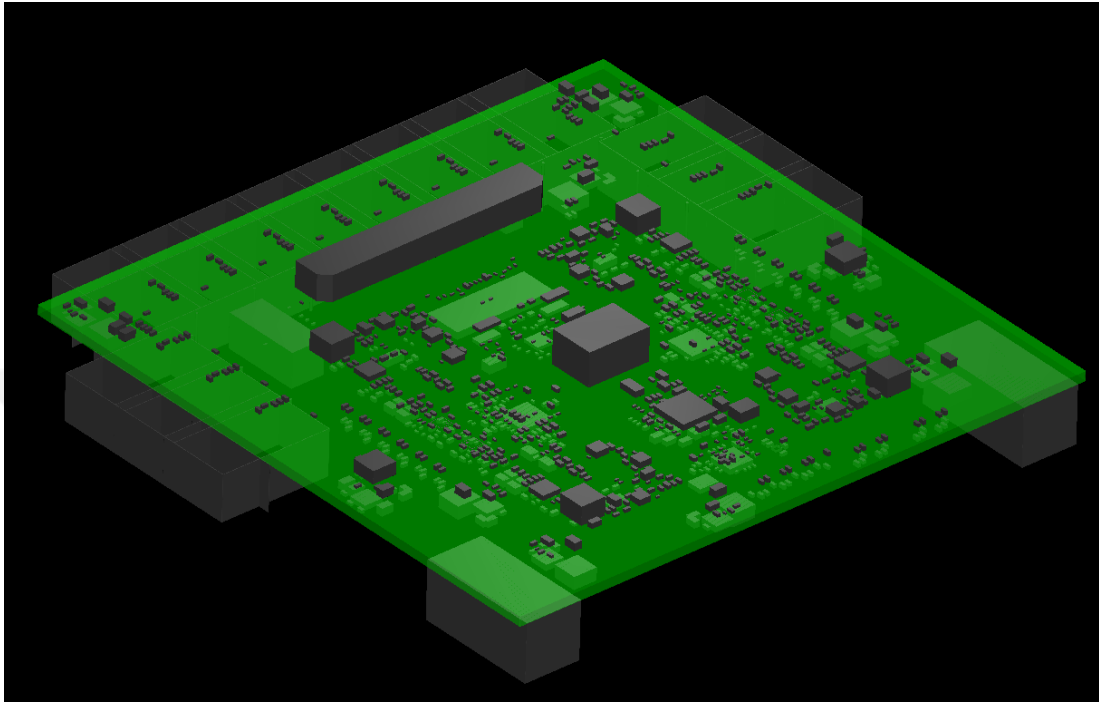


Figure 4.7: 3D Visualization of the Bottom Side

Finally, as mentioned in previous sections, the design includes many debugging components and redundant components for alternative implementations. In Table 4.1 breakdown of passive components in the design is given.

Package	Dimensions L x W (mm)	Courtyard L x W (mm)	Part Type	Number of Populated Components (per module)	Populated Components Total Surface Area (mm ²)	Number of Unpopulated Components (per module)	Unpopulated Components Total Surface Area (mm ²)
0201	0.6 x 0.3	1.4 x 0.8	Resistor	89	99.68	91	101.92
			Capacitor	134	150.08	12	13.44
0402	1.0 x 0.5	1.8 x 0.9	Resistor	133	215.46	17	27.54
			Capacitor	156	252.72	59	95.58
			Inductor	75	121.5	11	17.82
0603	1.6 x 0.8	3.1 x 1.5	Capacitor	15	69.75	2	19.22
			Inductor	24	111.6	2	19.22
0805	2.0 x 1.25	3.5 x 2.0	Capacitor	1	7	-	-
-	3.2 x 1.6	4.9 x 3.7	Ceramic LPF	1	18.13	-	-
-	4.0 x 4.0	5.0 x 5.0	Transformer	4	100	-	-
-	2.0 x 2.0	2.8 x 2.8	Connector	4	31.36	-	-
-	10 x 9.7	11.3 x 11.2	Power Splitter	1	126.56	-	-

Table 4.1: Breakdown of the Passive Components

There are a total of 194 passive components that are marked as not to be populated during assembly. The corresponding surface area spared for these components sums up to 295 mm^2 . Once the development of the board is complete, these components can be removed from the design in future revisions to allow smaller size board.

Chapter 5

Improvements on the Designed Circuit

Although, discussed and designed circuit in the previous sections offers less power and area consumption over conventional systems, these features can be further improved by using one optical line to send digital data out of the module instead of ten. This not only improves power consumption and PCB area usage by using less number of optical transceivers but also makes physical routing of optical lines between the sampling systems and the signal processor more feasible. To achieve such reduction in physical transmission layer while keeping bandwidth of the optical channel low in order not to consume excess power, the digital data that are being sent out should be compressed. However, the only intelligent component on the board, the MCU, is not capable of performing a compression operation on the ADC data due to its limited resources. Instead, a more powerful digital signal processing platform which has both logical processing elements and I/O resources is required. An Application Specific Integrated Circuit (ASIC) tailored for this implementation would be the best solution in terms of power and surface area consumption, but at the research and development stage a Field Programmable Gate Array (FPGA) is a more advantageous solution as it offers modifiable hardware architecture, and a variety of products with different resources for different applications are readily available from various manufacturers as an off-the-shelf

product for a much lower price compared to an ASIC. For the aforementioned reasons, the effects of using an FPGA in the design are also investigated in this work.

5.1 FPGA Selection

As for all designs, the selection of the FPGA is based on the function that is to be performed by the device and the resources required for the target application. In this work, the FPGA is used to capture the digital data coming from both of the ADCs, perform a compression operation on it, and finally feed this compressed data to the optical transceiver for optical transmission to the signal processor. At the same time, because the MCU is eliminated from the design to reduce resource usage, configuration and control operations are to be performed by the FPGA as well. Since the digital outputs of the ADCs are differential signals, the FPGA is required to accept differential inputs. Furthermore, the number of inputs and outputs (I/O) on the device must be sufficiently high to accommodate all of the signals, and the allowed voltage level for these pins must be compatible with other components. Breakdown of the digital signals required by the components in the design is given in Table 5.1. According to this table, there are a total of 89 digital signals that can be connected to the FPGA. 3 of these signals are not required for this application, 53 of them could be connected for extended control over components, 19 single-ended and 12 differential pairs must be routed for correct operation. Therefore, counting in the incoming and outgoing data, an FPGA with at least 45 I/O pins is required for this work.

Component	Number of Components (per module)	Signal	Utilization	Direction	Type	Level (V)
TCXO	1	OUTPUT_EN	Mandatory	In	CMOS	3.3
Synthesizer	1	CE	Optional	In		1.8 to 3.3
		SPI_CSB	Mandatory	In		
		SPI_SCK	Mandatory	In		
		SPI_SDI	Mandatory	In		
		MUXout	Mandatory	Out		
		RampClk	Not Required	In		
		RampDir	Not Required	In		
		SYNC	Optional	In		
		SysRefReq	Not Required	In		
Clock Generator	1	HW_SW_CT_RL	Optional	In		1.8
		REFSEL	Optional	In		
		GPIO1	Optional	In/Out		
		GPIO4	Optional	In/Out		
		PDN	Optional	In		
		I2C_SDA	Mandatory	In/Out		
		I2C_SCL	Mandatory	In		
LNA	4	Enable	Mandatory	In		-1
FDA	4	PD_N	Optional	In		
ADC	2	PDN/SYNC	Optional	In	LVDS	1.8
		RESET	Mandatory	In		
		SPI_SEN	Mandatory	In		
		SPI_SCLK	Mandatory	In		
		SPI_SDIO	Mandatory	In/Out		
		DA0P	Mandatory	Out		
		DA0M	Mandatory	Out		
		DA1P	Mandatory	Out		
		DA1M	Mandatory	Out		
		DB0P	Mandatory	Out		
		DB0M	Mandatory	Out		
		DB1P	Mandatory	Out		
		DB1M	Mandatory	Out		
		DCLKP	Mandatory	Out		
		DCLKM	Mandatory	Out		
		FCLKP	Mandatory	Out		
		FCLKM	Mandatory	Out		
Pos. DC/DC Converter	8	EN	Optional	In	CMOS	
		PG	Optional	Out		
		FSW	Optional	In		
		DEF	Optional	In		
Neg. DC/DC Converter	2	EN	Optional	In		
		PG	Optional	Out		

Table 5.1: Breakdown of Signals within the Design

As discussed in Section 3.6, depending on the configuration, the output data rate of the ADC can be as high as 1000 *Mbps*; however, using the internal decimation filter within the ADC, this rate can be lowered to 40 *Mbps* per output channel for signals that are of interest in this work. Such a low input data rate is supported by most modern FPGAs. Once the sampled and digitized data coming from all four channels are captured by the FPGA, it is subjected to compression and concatenation to allow transmission over only one optical channel. The compression algorithm can be as simple as a difference or logarithm operation, or more advanced encoding schemes can be deployed. Since the discussion of compression level is out of the scope of this work, the requirement on the output pin of the FPGA for compressed ADC data transmission is determined to allow tolerance. Even with decimation filtering and compression, the output data rate can be higher than the capability of a generic output pin in an FPGA, since the serial data output of the ADCs with a total of four channels are further serialized as a result of concatenation by a factor of 1 : 4. This serialization requires dedicated hardware within the FPGA and is commonly referred to as *SERDES* or *Transceiver* blocks. In addition to the power and surface area consumption requirements, in order to leave a margin at the output data rate, FPGAs with such dedicated resources are investigated in this work. In Table 5.2 FPGAs from major manufacturers complying with these restrictions are compared.

Manufacturer	Part Number	Process Technology (nm)	Package	Logic Elements	Block RAM (Kb)	Single-Ended I/O	Differential I/O	Transceiver	Surface Area (mm ²)
Intel	10CX085	20	U484	85000	5820	188	70	6	361
Lattice	LFE5UM-25	40	csfBGA	24000	1008	118	54	2	100
Microchip	M2GL025	65	FCS325	28000	558	180	58	2	121
Microchip	MPF050T	28	FCSG325	48000	450	164	42	4	121
Xilinx	XC7A15T	28	CPG236	16640	900	106	48	2	100

Table 5.2: Comparison of FPGAs

Although Intel's FPGA is fabricated using the lowest process technology, due to the offered package, surface area consumption is roughly three times higher than other products, and for this reason it is eliminated from the candidate list. For the remaining products, a power consumption analysis is performed in the next section.

5.2 FPGA Power Consumption Analysis

Power consumption figures are estimated using the manufacturer’s power estimator tools: *Power Calculator* for Lattice FPGAs, *Microsemi Power Estimator* for Microchip FPGAs and *Xilinx Power Estimator* for Xilinx FPGAs [42, 43, 44]. In all power estimator tools, the main system clock is assumed to be a 100 *MHz* reference. Logic element utilization is set to 70% for *XC7A15T* since it has the least number of blocks among the other candidates and for the remaining parts, the same number is used with a toggle rate of 12.5%. Similarly, for the block RAM utilization 50% of *XC7A15T*’s resources are used, and it is scaled for other candidates. All of the mandatory signals listed in Table 5.1 are entered into calculators with associated type, direction and toggle rate. For the ADC output signals in particular, differential type with internal termination, 400 *MHz* clock speed and 50% toggle rate is chosen. Finally, for the outgoing ADC data, a transceiver lane with 2 *Gbps* is enabled to represent the worst-case scenario. For the Lattice FPGA, because with a free license, the power consumption of the *SERDES* logic cannot be analyzed, the average power consumption due to this function obtained from the remaining parts is used. With these settings, the static and dynamic power consumption figures are estimated and given in Table 5.3. The total power consumption values are consistent within a range of 180 *mW* to 350 *mW*. Since these estimations are prone to change during the actual implementation stage, an average value of 250 *mW* is assigned to the power budget spared for the FPGA for the following discussions.

Manufacturer	Part Number	Supply Voltage (V)	Static Power Consumption (mW)	Dynamic Power Consumption (mW)	Total Power Consumption (mW)
Lattice	LFE5UM-25	1.1	85	166	251
Microchip	M2GL025	1.2	80	275	355
Microchip	MPF050T	1	32	153	185
Xilinx	XC7A15T	0.95	40	250	290

Table 5.3: Power Consumption of FPGAs

The breakdown of power consumption with respect to functionality within the FPGA is given in Table 5.4 where all numbers are in *mW* units.

Resource		LFE5UM-25	M2GL025	MPF050T	XC7A15T
Core Static		27	12	33	39
Core Dynamic	Clock	33	75	29	37
	Logic	48	115	42	40
	RAMs	43	37	13	22
I/O		51	70	38	66
Transceiver		- ¹	46	31	83

Table 5.4: FPGA Power Breakdown (¹ cannot be estimated with a free license)

5.3 Modified Circuit Topology

With inclusion of the FPGA in the design, the circuit topology given in Fig. 2.5 is modified as in Fig. 5.1.

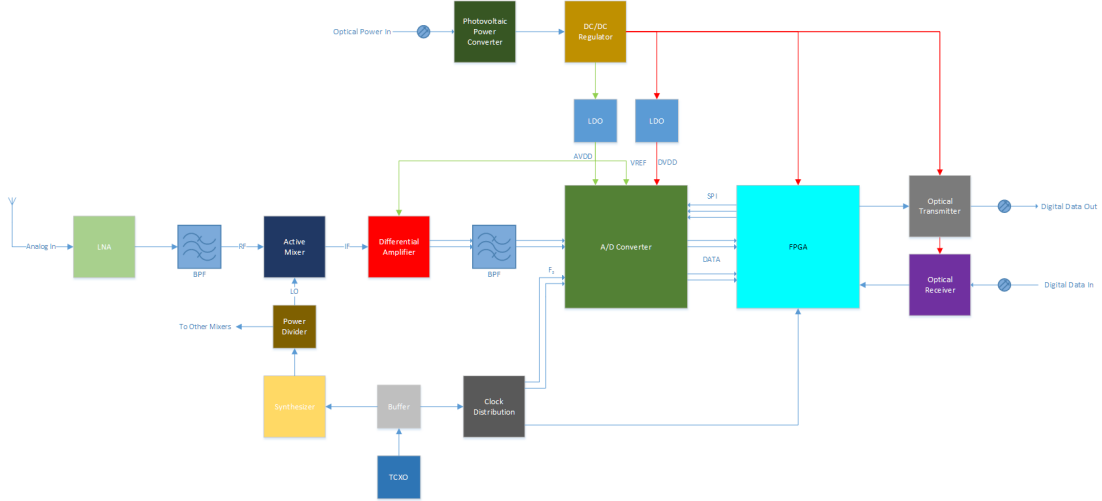


Figure 5.1: Block Diagram of the Design with an FPGA

Compared to the previous design, this design with an FPGA eliminates the need for an LVDS receiver to convert differential ADC outputs to optical transceiver compatible single-ended signals. Therefore, by combining functionality of MCU and LVDS receiver in a single component, the design with an FPGA enables further improvement on both power and surface area consumption in addition to reduction in number of optical transceivers.

Chapter 6

Conclusion

In this work, various topologies for an MRI signal acquisition system are discussed. Throughout the evaluation process, some of these topologies have been proven to be impractical or inefficient given the requirements. Initially, the topology that uses an active mixer with a frequency synthesizer as the LO source for downconversion is considered as the most suitable approach; therefore, circuit design and placement is performed for this approach. However, a deeper analysis regarding power consumption aspect has revealed that with inclusion of an FPGA into the design, both power and surface area consumption can be improved by compressing the outgoing ADC data, which eventually reduces the number of optical transmitters in the design, without degrading the SNR performance. The power consumption figure of the module can be further reduced by using a SAW oscillator for LO signal generation; however, as discussed in Section 2.2.2.1, with this method there is a trade-off between temperature stability and power consumption. The temperature stability problem can be solved by characterization, calibration and compensation. Therefore, for the lowest power consumption, a SAW oscillator should be used instead of a synthesizer. These different circuit topologies are compared in Table 6.1 with respect to power consumption.

Part Number	Function	Power Consumption per IC (mW)	Synthesizer Approach		SAW Oscillator Approach		FPGA Approach	
			Quantity per Board	Total Power Consumption (mW)	Quantity per Board	Total Power Consumption (mW)	Quantity per Board	Total Power Consumption (mW)
QMQF326	TCXO	82.5	1	82.5	1	82.5	1	82.5
CCS575S	SAW Oscillator	66	0	0	1	66	1	66
LMK1D1204P	Clock Buffer	81	1	81	0	0	0	0
LMX2572	Synthesizer	255	1	255	0	0	0	0
CDCE6214	Clock Generator	99	1	99	1	99	1	99
TSY-13LB+	LNA	21	8	84 ¹	8	84 ¹	8	84 ¹
LT5560	Mixer	12	4	48	4	48	4	48
THS4551	FDA	6.5	4	22	4	22	4	22
ADC3683	ADC	160	2	320	2	320	2	320
REF3318	Voltage Reference	.015	2	.03	2	.03	2	.03
OPA837	OPAMP	1.8	2	3.6	2	3.6	2	3.6
ADuCM3029	MCU	1.4	1	1.4	1	1.4	0	0
MPF050T	FPGA	250	0	0	0	0	1	250
SN65LVDT	LVDS Receiver	198	1	198	1	198	0	0
AFBR-2624Z	Optical Receiver	20	1	20	1	20	1	20
ADBR-1624Z	Optical Transmitter	51	11	561	11	561	1	51

Table 6.1: Comparison of Topologies (¹ Only four of them are ON by default)

In Table 6.1, *Synthesizer Approach* corresponds to the designed and laid-out topology discussed in Chapters 3 and 4. In *SAW Oscillator Approach*, the synthesizer is replaced with a SAW oscillator to generate the LO signal. Finally, with *FPGA Approach* an FPGA is integrated into the *SAW Oscillator Approach* and the block diagram of this topology is shown in Fig. 6.1.

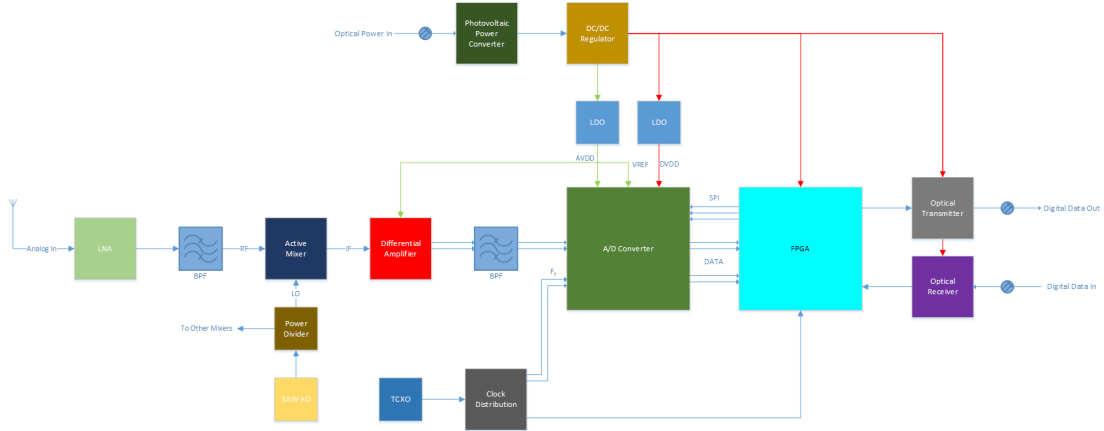


Figure 6.1: Block Diagram of the Design with SAW Oscillator and FPGA

PCB layout for the synthesizer approach is finalized while using 900 mm^2 cross-sectional area per channel, and one module accommodates four channels on the board. Although the total PCB area is slightly larger than the final module size, it includes many redundant components for debugging and prototyping that can be removed from the design to save surface area in future revisions. Moreover, the analog and digital circuitry on the board are separated from each other as much as possible to keep the SNR as high as possible by reducing the coupling between these domains. For future work, a multi-board structure is suggested to lower the cross-sectional area of the module by using smaller but stacked PCBs. With such a physical structure, the separation between the noise-sensitive analog circuitry and digital circuitry can be achieved inherently by design. Considering a stacked design with three boards, a board with analog circuitry close to the coil, a board for sampling and clock generation, and a board with the interface circuitry would lead to implicitly decoupled design. This approach not only reduces cross-sectional area by utilizing the volume in vertical axis, but together with exploitation of advanced manufacturing processes, e.g. partial or buried via, it also enables a more compact and closely placed physical placement since the components on each board are now in the same domain. On the contrary, for the designed PCB discussed in Chapter 4, the backsides of the analog and digital circuits were almost unutilized due to the reasons mentioned earlier.

Inclusion of the FPGA into the design would not dramatically affect the exercised PCB layout, as it would fit the area spared for the MCU and LVDS receiver. Furthermore, since the FPGA enables employment of fewer optical transceivers, the PCB area can be greatly reduced in future iterations. Similarly, for the SAW oscillator that can be used for the LO signal generation, the surface area spared for the synthesizer can be reused.

To conclude, in this work, an MRI data acquisition system is designed focusing on three main criteria that are implications of the application. The module surface area is kept as small as possible to allow placement of as many channels as possible in a birdcage compartment to take advantage of multiple-channel imaging. At the same time, to keep the SNR as high as possible, instead of transmitting the analog MRI signal, the sampled and digitized signal is sent out

of the module. Finally, to eliminate issues with the usage of the coaxial cable, the power delivered to the module should be delivered optically; however, due to the lack of capability of power carrying with optics, the module is designed to consume as low power as possible.

The optical power converters available on the market as an off-the-shelf solution at the time this study was conducted were not suitable for the application because of their size and housing material, which were of the ferromagnetic type and unsafe for MRI applications. For this reason, the optical power delivery to the module is left as a future work.

The topology with a SAW oscillator and an FPGA has the lowest power consumption among other approaches, and the power consumption per channel is estimated to be 263 mW according to the typical values given in the component data sheets. For this reason, this approach is suggested for future revisions. Furthermore, after performing digital signal processing at the processor, SNR of the system is expected to be more than 95 dBFS.

As a critical equipment for healthcare practices, advancements in MRI systems are desirable. The proposed approach and designed module offers many benefits over conventional systems. Theoretical estimations show that, for emerging needs of MRI applications the proposed system has a lot to offer.

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Appendix A

PCB Drawings

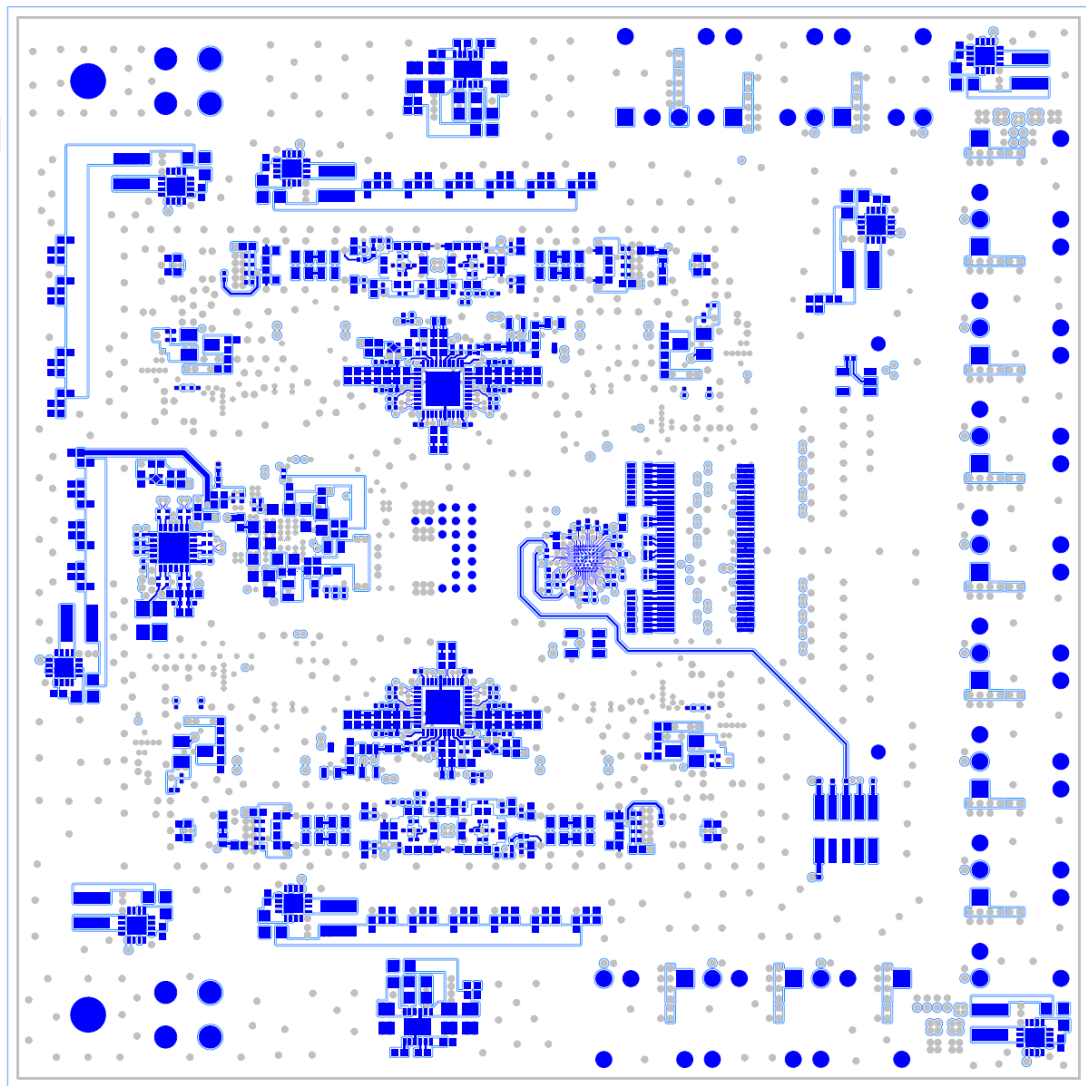


Figure A.1: Layer 1: Top

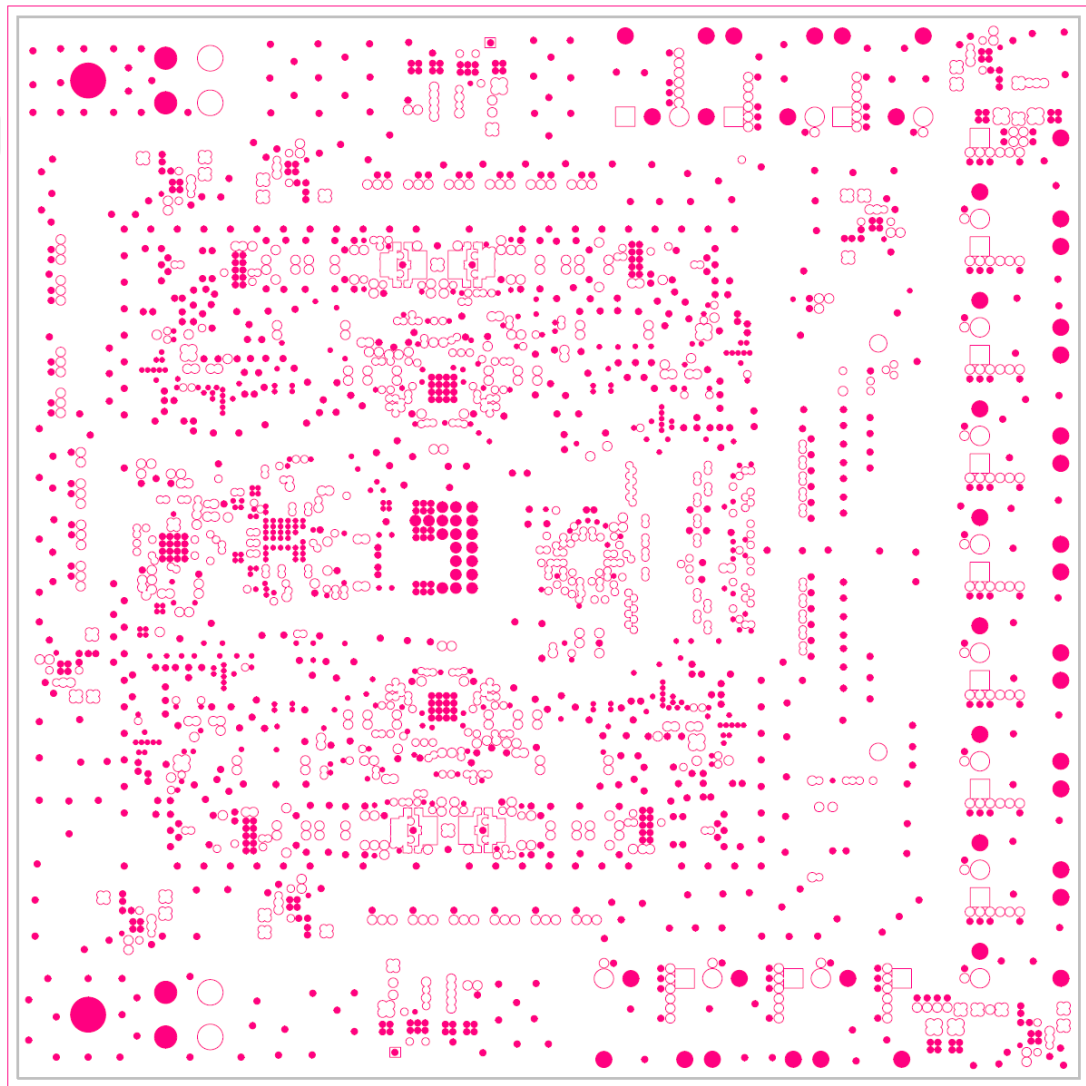


Figure A.2: Layer 2: Ground 1

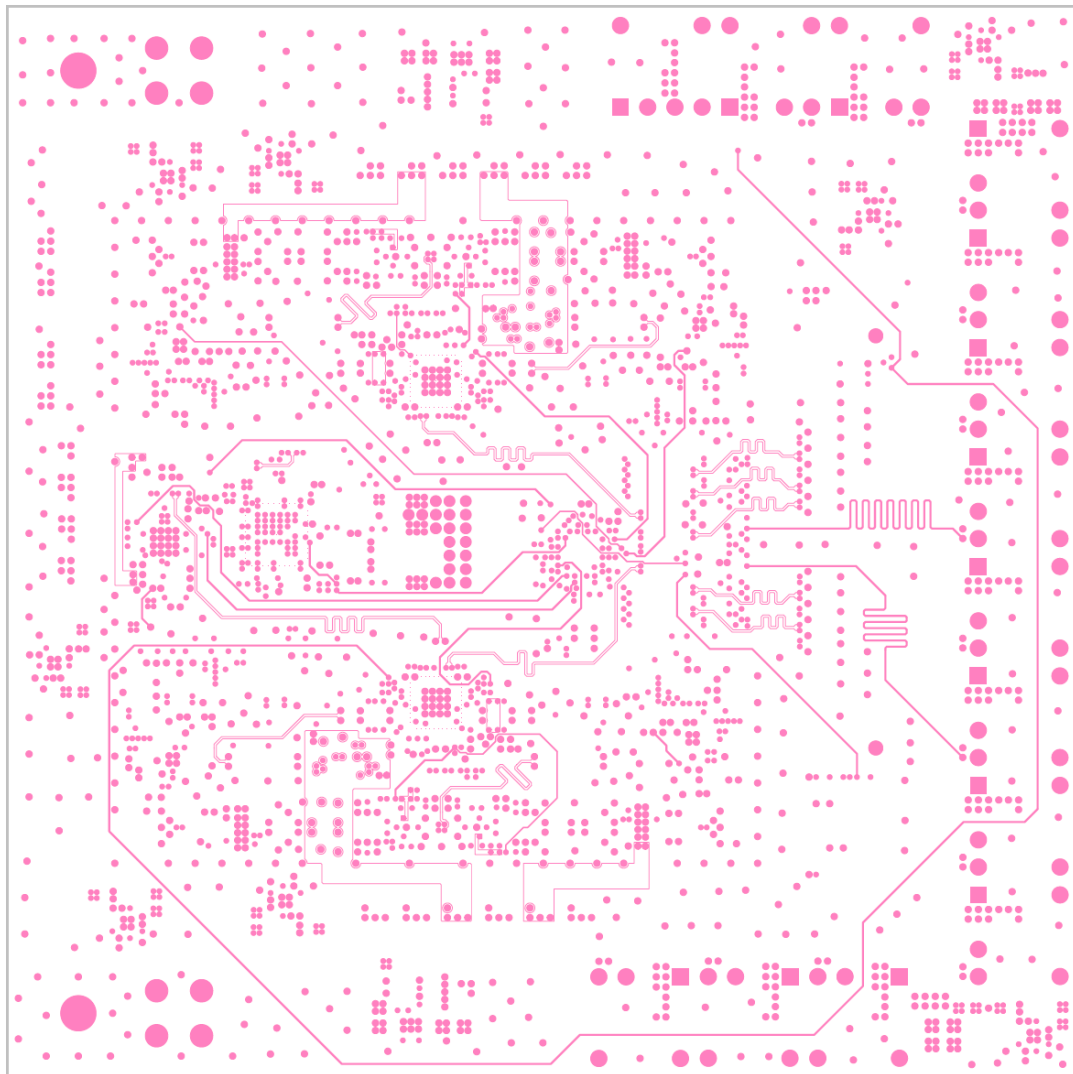


Figure A.3: Layer 3: Signal 1

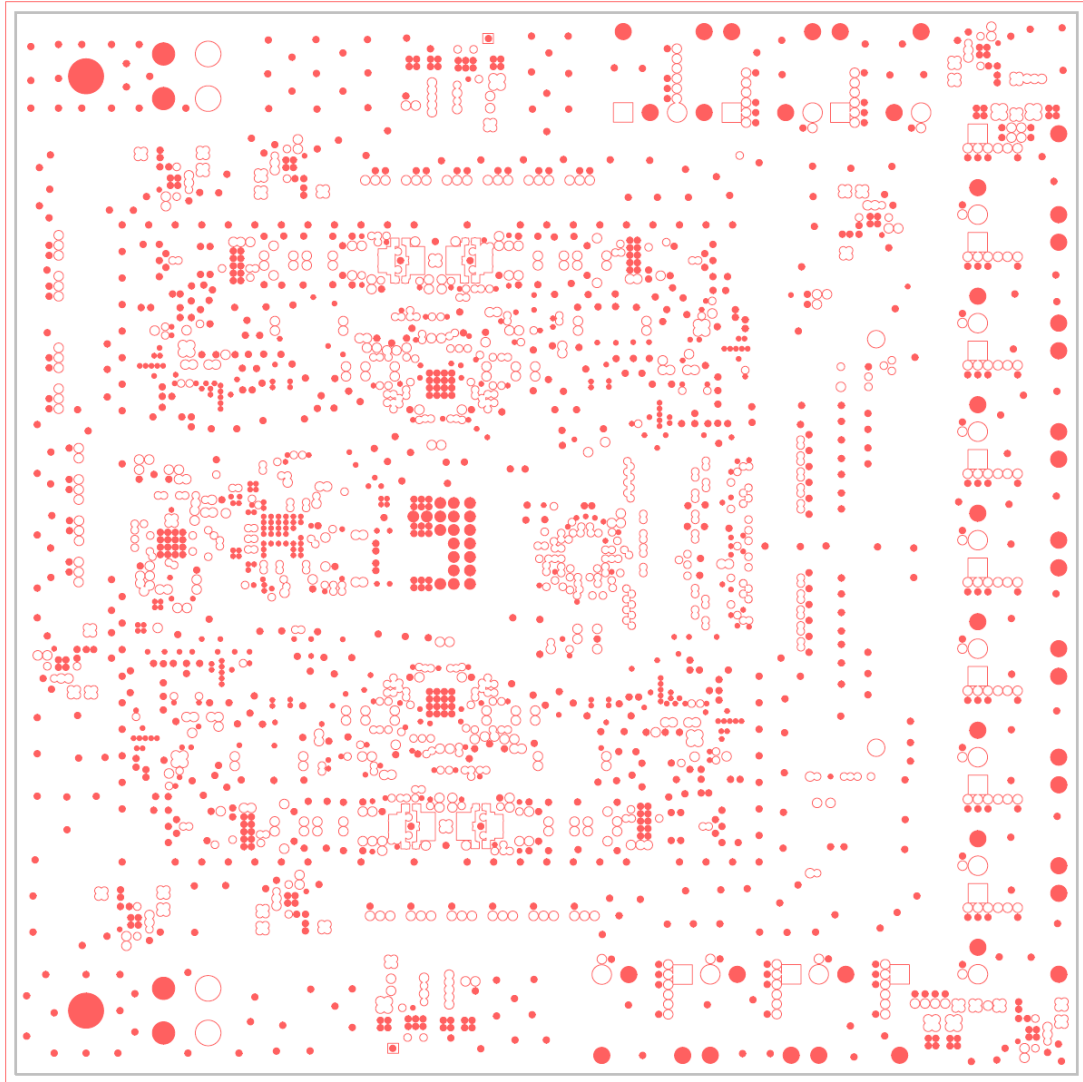


Figure A.4: Layer 4: Ground 2

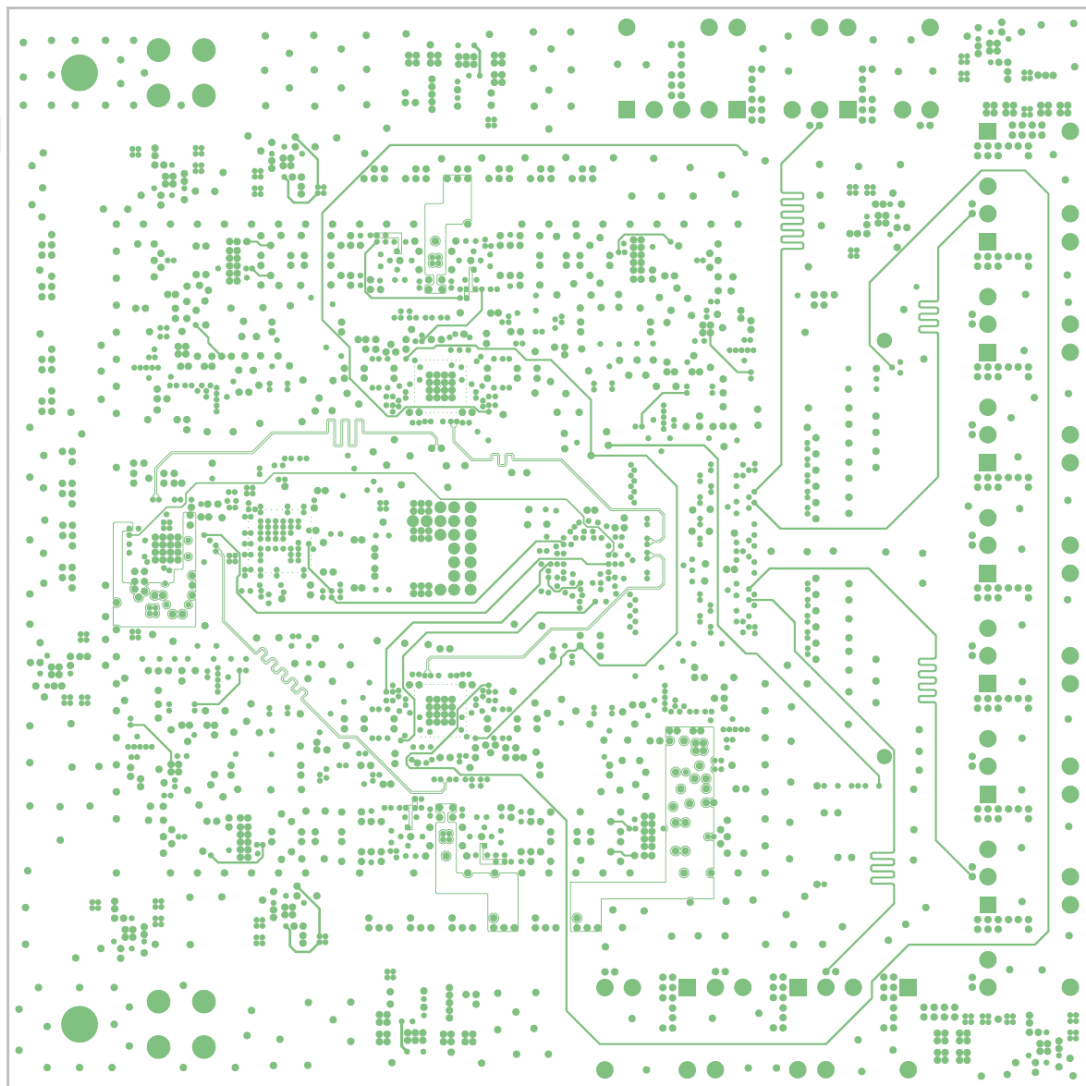


Figure A.5: Layer 5: Signal 2

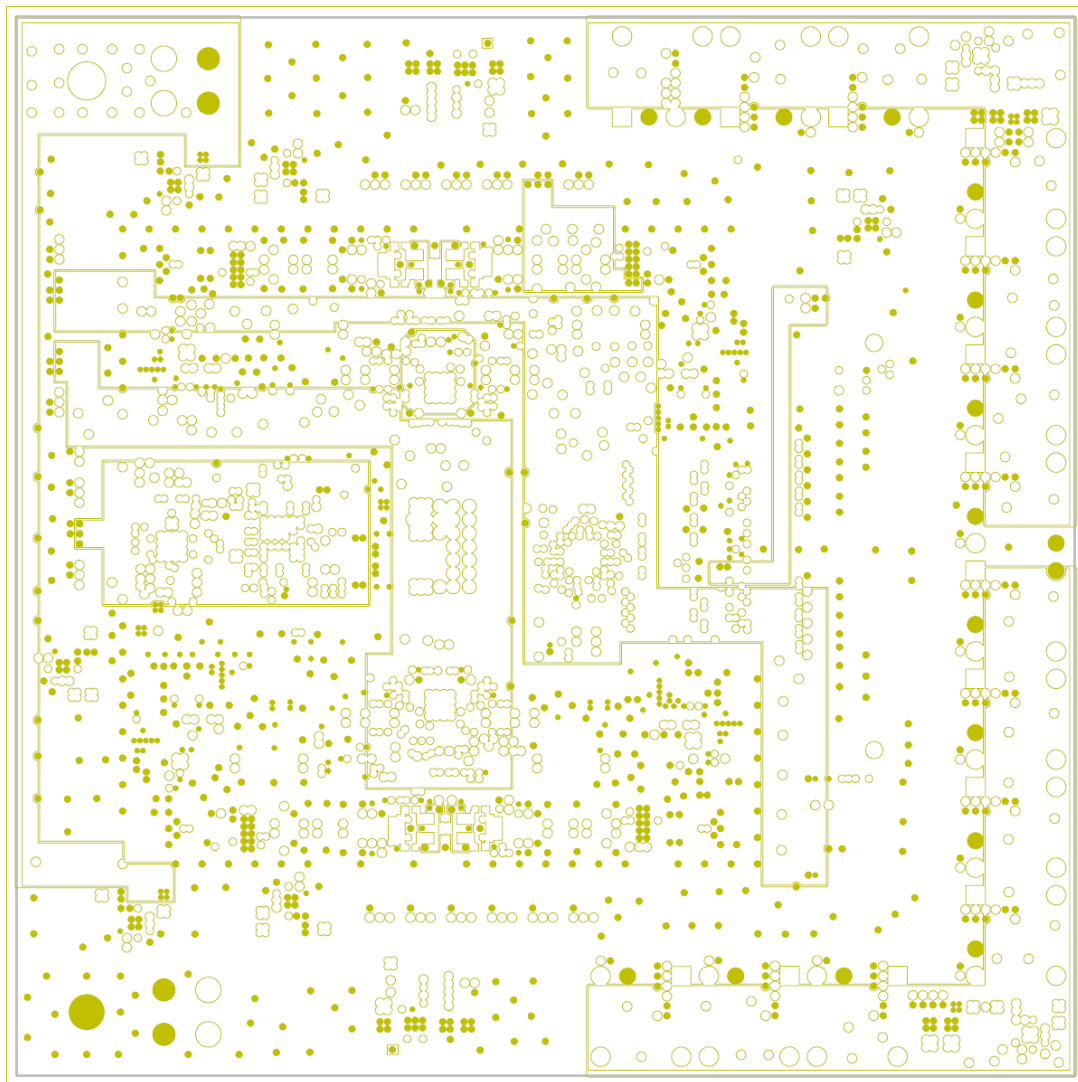


Figure A.6: Layer 6: Power 1

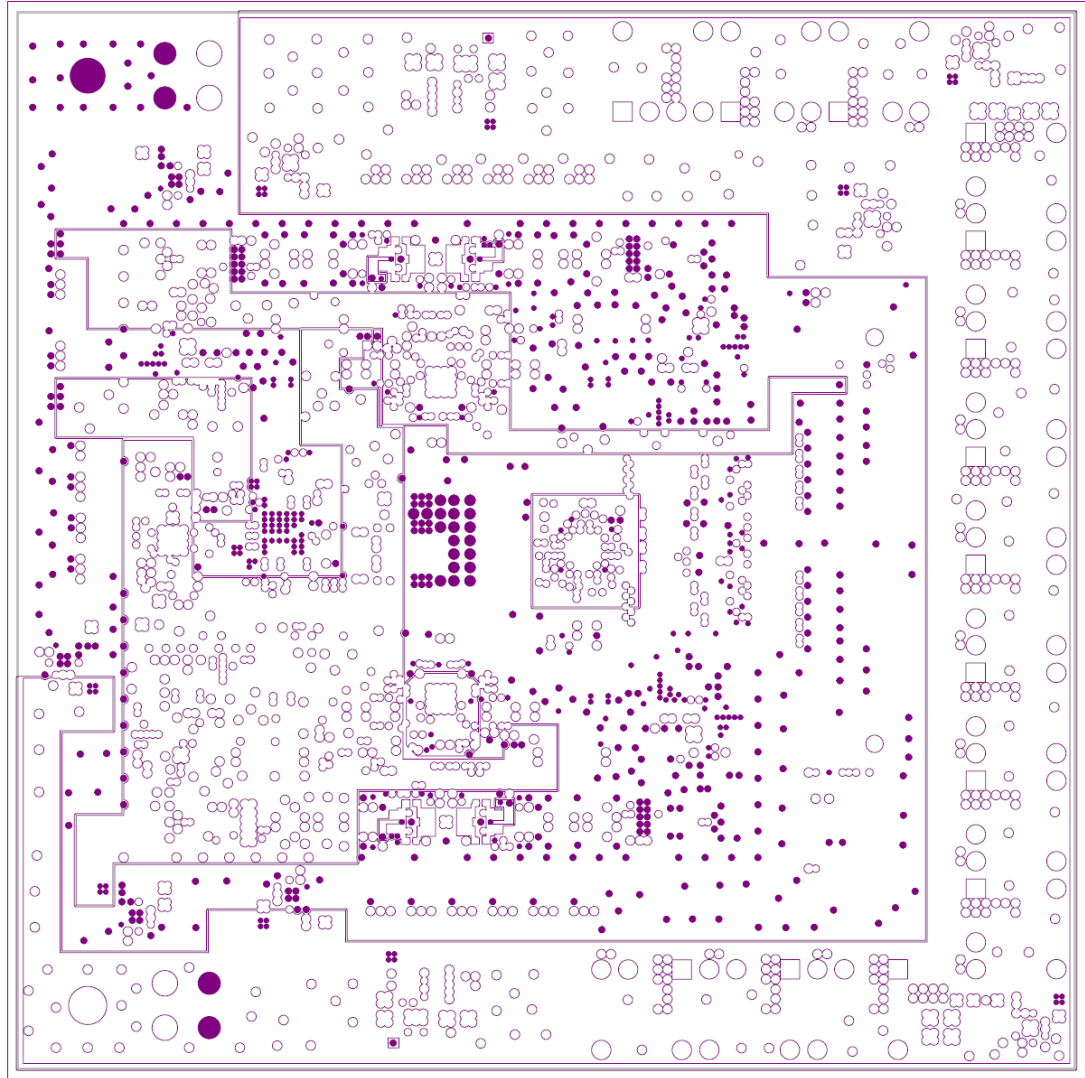


Figure A.7: Layer 7: Power 2

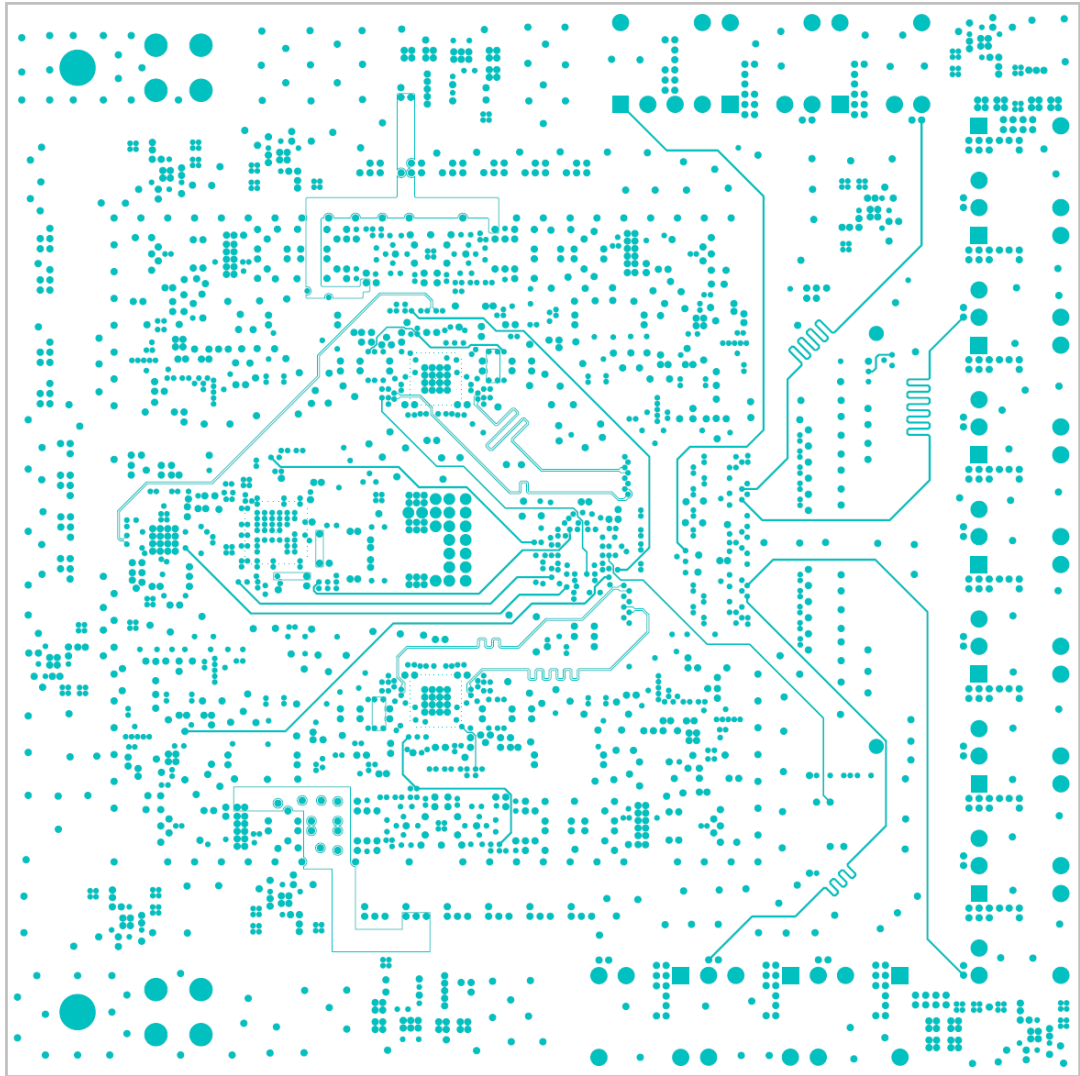


Figure A.8: Layer 8: Signal 3

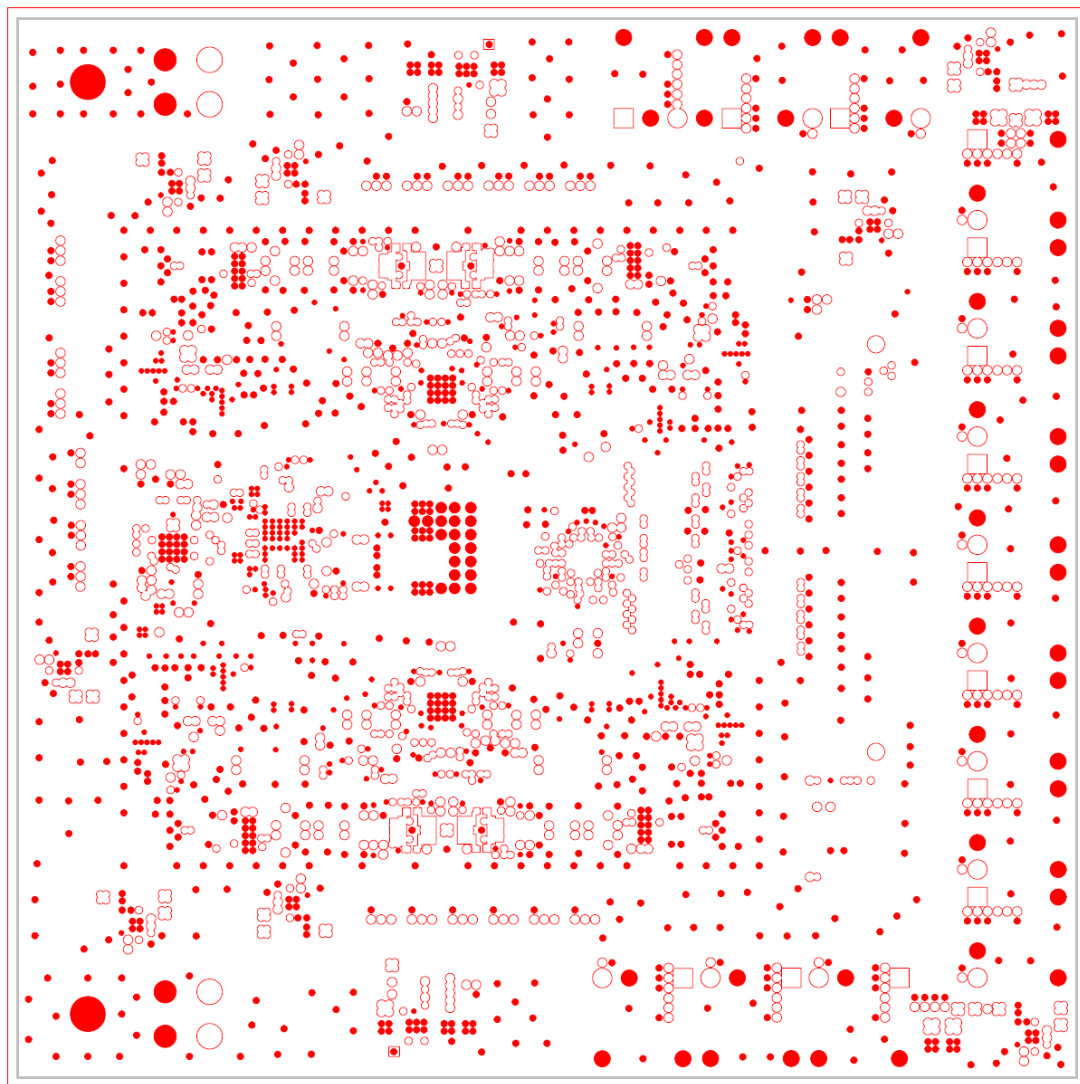


Figure A.9: Layer 9: Ground 3

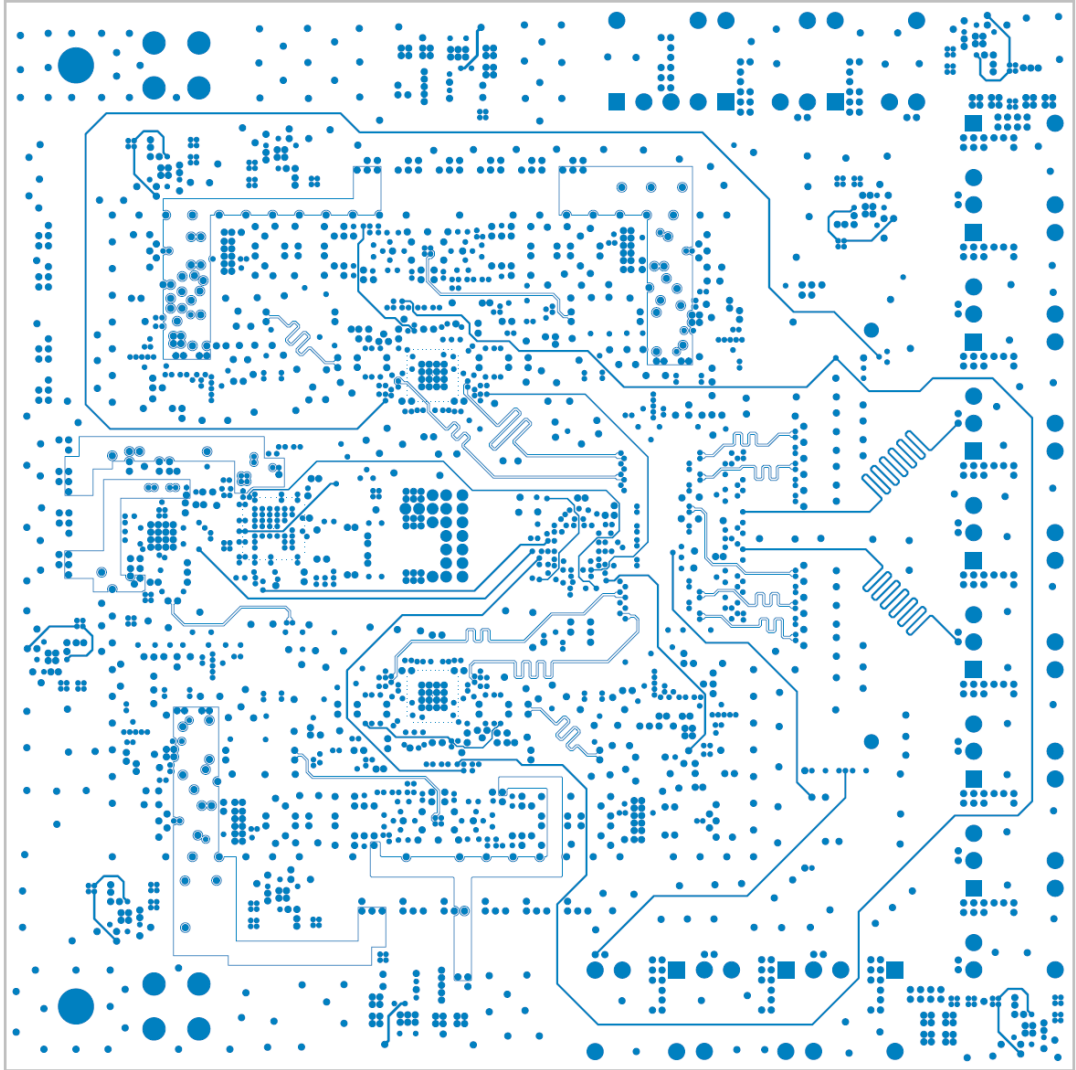


Figure A.10: Layer 10: Signal 4

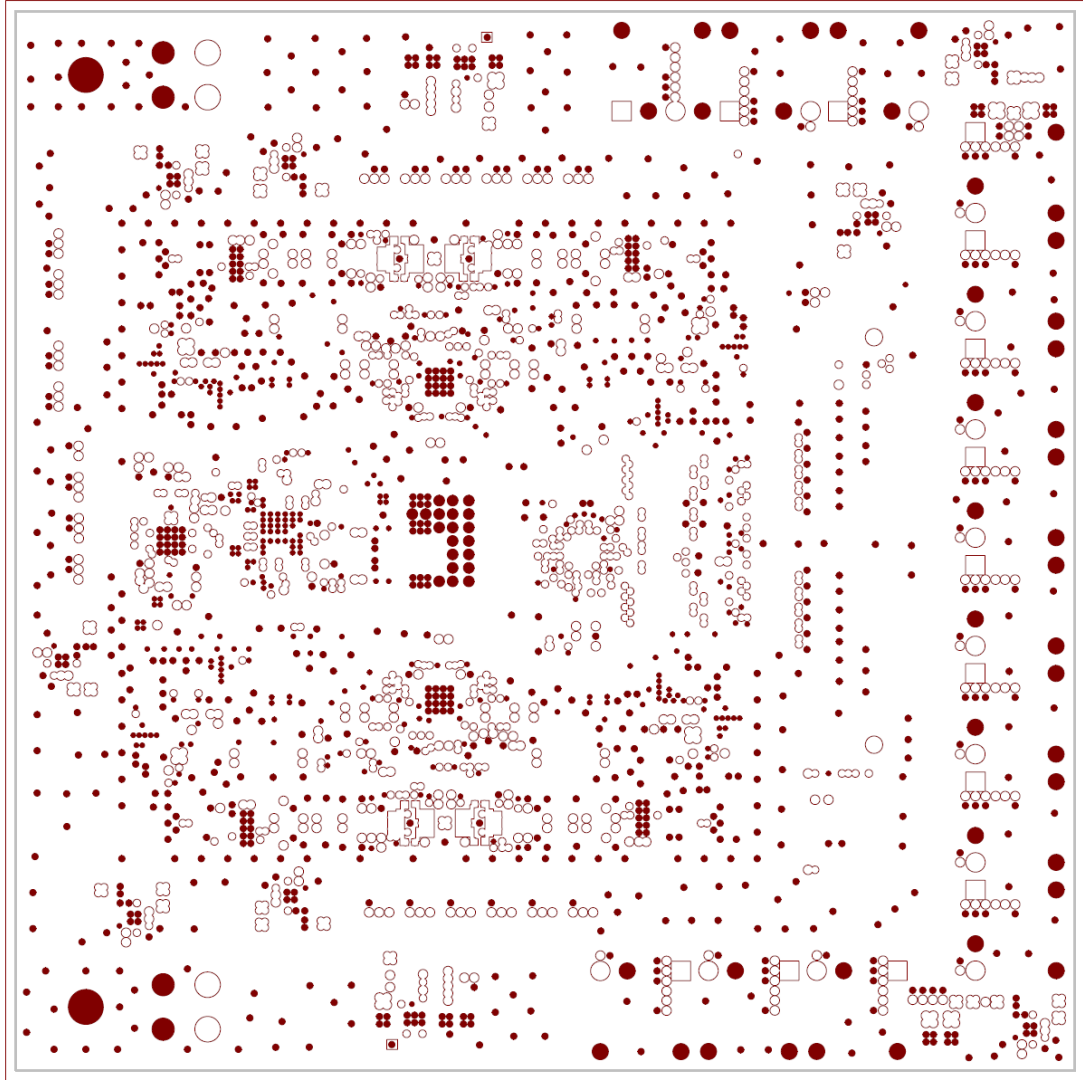


Figure A.11: Layer 11: Ground 4

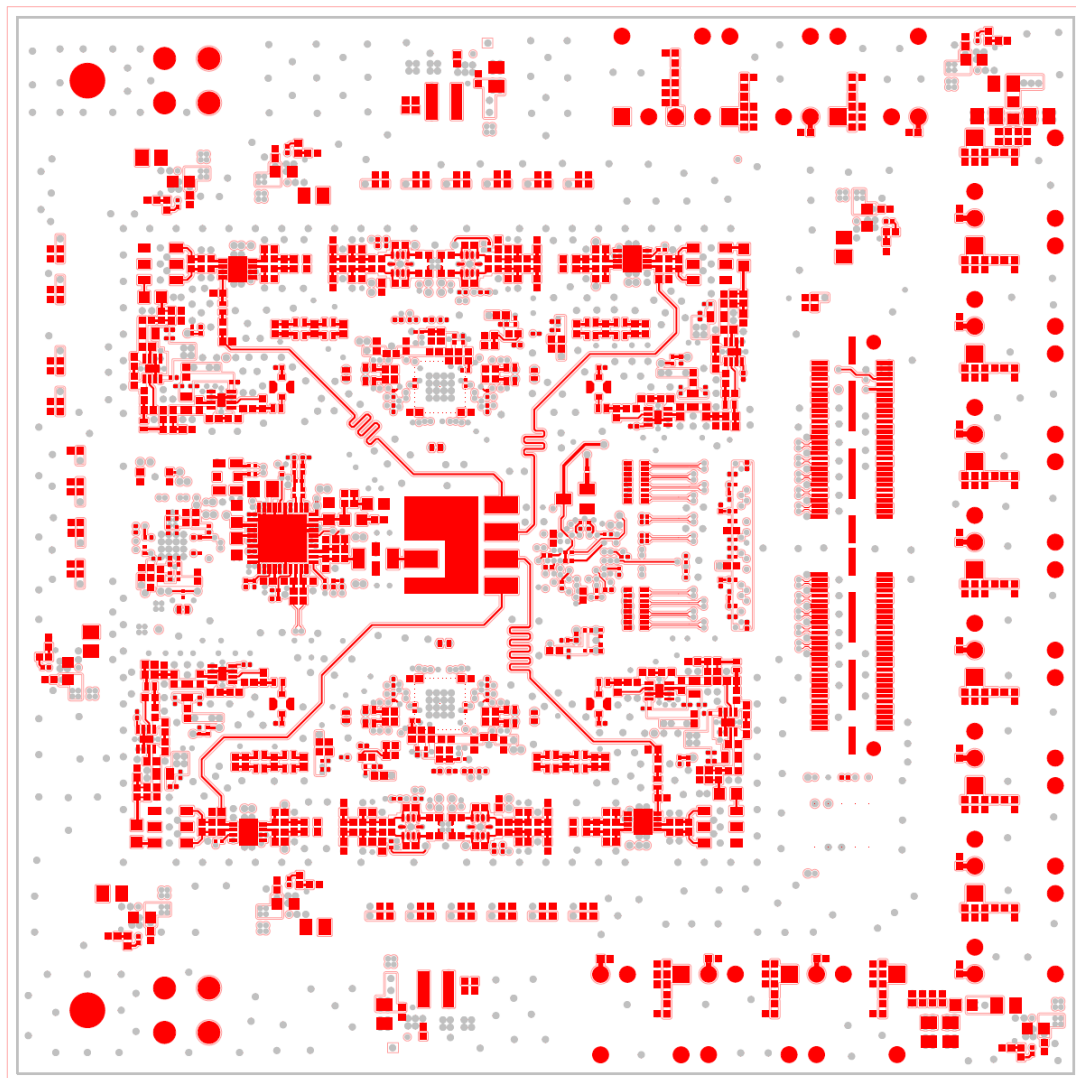


Figure A.12: Layer 12: Bottom

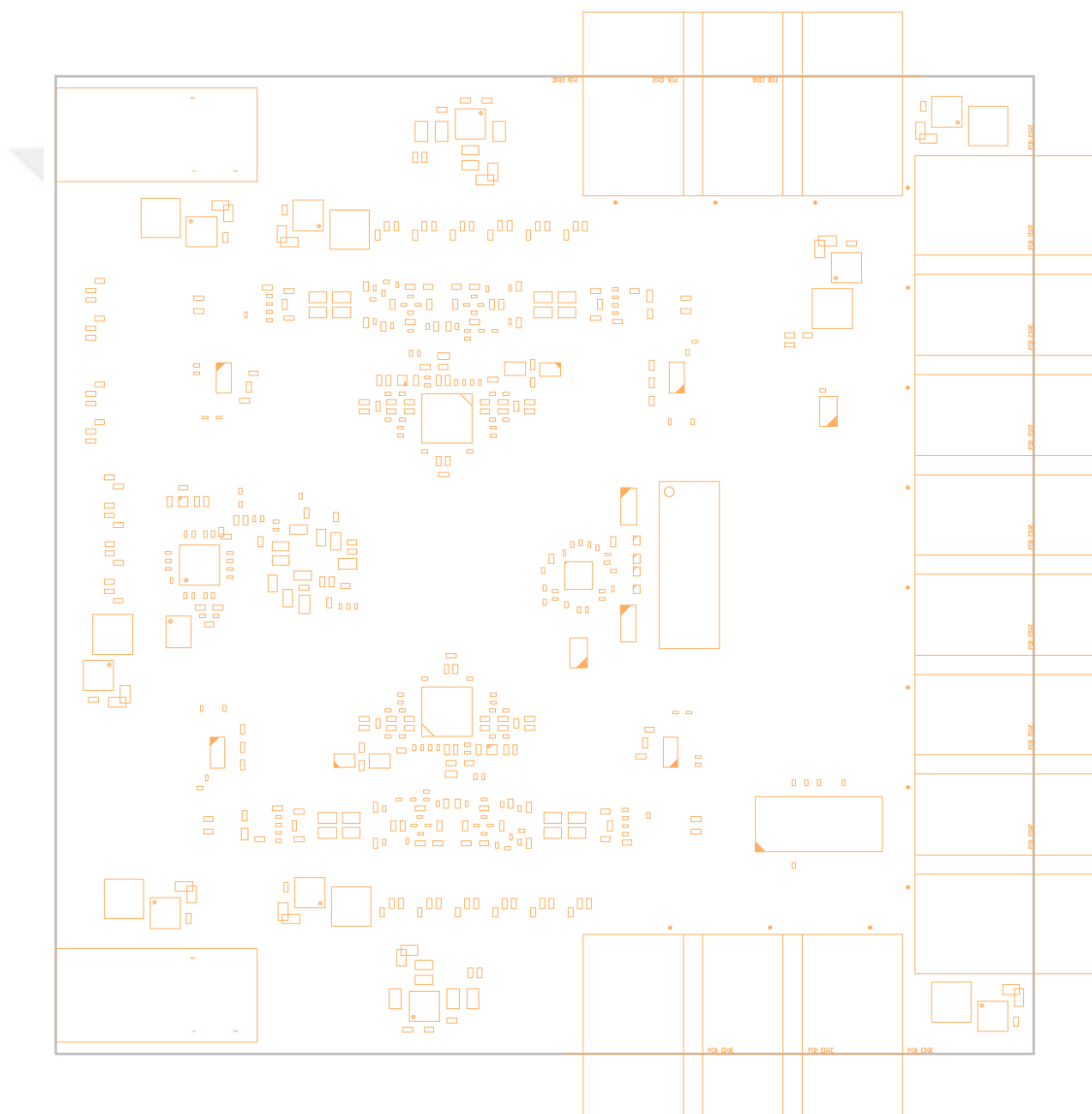


Figure A.13: Layer 13: Assembly Top

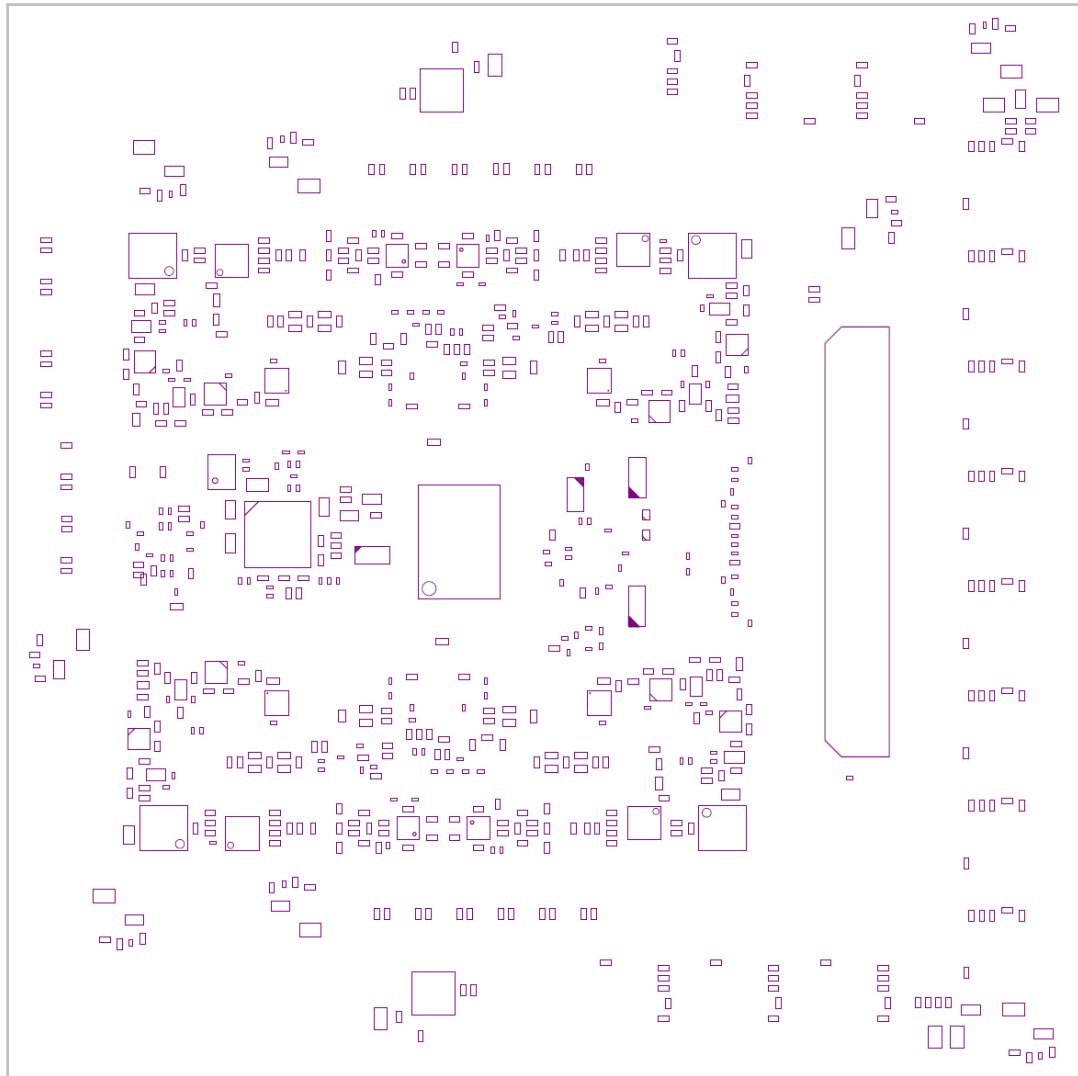


Figure A.14: Layer 14: Assembly Bottom