

DEVELOPMENT AND CHARACTERIZATION OF A MEGAPIXEL SWIR IMAGING SYSTEM

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR
THE DEGREE OF
MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

By
Mustafa Erdoğan
January 2022

Development and Characterization of a Megapixel SWIR Imaging
System

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January 2022

We certify that we have read this thesis and that in our opinion it is fully adequate,
in scope and in quality, as a thesis for the degree of Master of Science.

Ekmel Özbay(Advisor)

Vakur Behçet Ertürk

Haluk Külâh

Approved for the Graduate School of Engineering and Science:

Ezhan Karâşan
Director of the Graduate School

ABSTRACT

DEVELOPMENT AND CHARACTERIZATION OF A MEGAPIXEL SWIR IMAGING SYSTEM

Mustafa Erdoğan

M.S. in Electrical and Electronics Engineering

Advisor: Ekmel Özbay

January 2022

This thesis aims to develop a megapixel SWIR camera electronics and share the knowledge that has been acquired during the design phase as a detailed document that explains the theory and design steps to stand as a reference for academic researchers and engineers who work in this field. Valuable information from many different resources including books, presentations, technical articles, theses, etc. has been compiled and presented in this thesis following the design order. This thesis reviews the nature of light and its detection mechanisms and then concentrates on the idea of developing a product to detect light in the SWIR band.

The sensors to detect light in the SWIR band are designed and manufactured in NANOTAM. There is a need to develop both hardware and software to process the sensor outputs which carry information about the captured image to generate a meaningful and useful set of data to be displayed.

The objective is to come up with an imaging system that uses the in-house manufactured sensors and digitally visualizes the SWIR band with the best performance possible.

The components that will make up the imaging system are examined thoroughly to be able to inherit correct design procedures and go for the best performance while preventing costly over-design. Different image sensor types such as CCD, CMOS, InGaAs, etc., and their characteristics and requirements are studied in detail. Analog Front End electronics are designed to add the lowest possible noise and thus degrading the sensor performance minimally. Other electronic circuits such as Thermoelectric Cooler controller, power regulation, FPGA

electronics, etc. are designed to meet required operations without causing disturbance to Analog Front End electronics. Designs are carried out by abiding by correct PCB design practices which are addressed in this thesis. This way, it is made sure that the sensor performance, which is the limiting factor, is not degraded by the external electronics.



Keywords: SWIR, Infrared Imaging, InGaAs, Camera Electronics.

ÖZET

MEGAPİKSEL SWIR GÖRÜNTÜLEME SİSTEMİ GELİŞTİRİLMESİ VE KARAKTERİZE EDİLMESİ

Mustafa Erdoğan
Elektrik ve Elektronik Mühendisliği, Yüksek Lisans
Tez Danışmanı: Ekmel Özbay
Ocak 2022

Bu tez bir megapiksel SWIR kamera geliştirmeyi ve tasarım sürecinde elde edilen bilgileri detaylı bir doküman halinde bu konuda çalışan akademisyenler ve mühendislere referans olacak biçimde paylaşmayı amaçlamaktadır. Bu tezde, kitaplar, sunumlar, teknik yazılar, tezler vb. gibi kaynaklardan elde edilen bilgiler tasarım sürecine göre derlenmiş ve sunulmuştur. Bu tez ilk olarak ışığın doğasını ve algılama sürecini incelemekte ve sonrasında SWIR frekans bandını algılamak için bir ürün geliştirmeye odaklanmaktadır.

SWIR frekans bandını algılamak için kullanılacak sensörler NANOTAM'da tasarlanmakta ve üretilmektedir. Yakalanan görselle ilgili bilgiyi taşıyan sensör çıktılarını görselleştirebilecek şekilde anlamlı ve faydalı veri grubu oluşturacak şekilde işlemek amacıyla hem donanıma hem de yazılıma ihtiyaç bulunmaktadır.

Bu tezin amacı NANOTAM içinde üretilen sensörleri kullanan SWIR frekans bandını olabilecek en iyi performansla sayısal olarak görselleştirecek bir görüntüleme sistemi sunmaktır.

Görüntüleme sistemini oluşturacak parçalar doğru tasarım yöntemini kullanarak en iyi performansa ulaşırken maliyeti arttıracak aşırı tasarımdan kaçınmak amacıyla detaylı olarak incelenmiştir. CCD, CMOS, InGaAs vb. gibi farklı görüntü sensörleri ve özellikleriyle gereksinimleri detaylı olarak incelenmiştir. Analog ön yüz elektroniği mümkün olan en az gürültüyü ekleyerek sensör performansını asgari derecede azaltacak şekilde tasarlanmıştır. Termoelektrik soğutma kontrolörü, güç regülasyon ve FPGA elektroniği gibi diğer elektronik devreler gerekli işlemlere cevap verebilecek ve analog ön yüz elektroniğinde bozulmaya sebep olmayacak şekilde tasarlanmıştır. Tasarımlar bu tezde anlatılan doğru

PCB tasarım yöntemleri gözetilerek tamamlanmıştır. Bu sayede sistemin kısıtı olan sensör permansının harici elektronik devreler tarafından kötü yönde etkilenmeyeceğinden emin olunmuştur.



Acknowledgement

I would like to express my highest gratitude to my advisor and role model Prof. Ekmel Özbay. It was an honor for me to work under his supervision and guidance. I started working with him as a newly graduated junior engineer. Through the years we worked together I learned a lot from him in the road of becoming a senior engineer. It was his trust and guidance that made this thesis possible.

I also would like to extend my regards to Prof. Abdullah Atalar. During the courses he taught, his wisdom and knowledge shined light to my way. His continuous energy and desire to teach his students kept me motivated during my graduate student period.

Working in a multidisciplinary project requires more than being colleagues. In NANOTAM, we became a team and did our best to successfully accomplish megapixel SWIR camera project. With my teammates Can Kanbak and Yusuf Ziya Köksal we did a great job by producing a SWIR camera with completely in-house design. Also, the state of the art sensors developed by Halit Dolaş, Okan Ateşal and Özlem Arslan made our project invaluable.

During the Master's, I spent a lot of time in the office and laboratories of NANOTAM. My colleagues became my life-time friends. I want to express my special thanks to Büşra Gürdal, Faruk Uyar, Okan Özdemir, Canberk Ünal, Kaan Balkan, Sevda Ünal Apaydın and Diğdem Kazan due to the friendly environment they created, their help and motivation.

I would like to express my special thanks to my family members; my mother Elmas, my father Kamil, my sisters Şule and Betül and my brother Fatih. It is thanks to them; where I am and what I have.

Last but the most important, I want to show my thankfulness to the founder of Republic of Turkey, Mustafa Kemal ATATÜRK. He is the leader who praised science by his words; “If one day, my words are against science, choose science.”

and who marked the importance of peace by saying “Peace at home, peace at world.” His vision will always be on me and on everyone who understands him truly.



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Chapter 1

Introduction

Human beings have five senses which are sight, hearing, taste, smell and touch. Undoubtedly, people value sight as the most important sense among the five senses. This is because of the fact that the information gathered by sight outweighs others. People interact with their surroundings, keep themselves safe and avoid danger with the help of the information that is available thanks to being able to see. However, as human beings, our eyes can't sense all of the available information around us since our eyes are sensitive to only a small part of electromagnetic spectrum. This part of electromagnetic spectrum is known as the visible spectrum. A fragment of electromagnetic spectrum that cannot be detected by human eye is infrared spectrum, which lies between visible and microwave spectrum. People are not able to see light that is in infrared spectrum but still value the information in this band. Humankind first discovered infrared light and then looked for ways to gather information that is hidden in infrared region and came up with infrared detectors[1].

It has been made obvious by previous works that blackbody radiation's maximum output power is in the 8 to 12 μm region that corresponds to skin temperature between 30 to 34°C [2] and some part of the infrared spectrum has the ability to penetrate through dust[3]. Such properties of infrared light give it special uses in many different applications in space, military, security, scientific,

medical, industrial etc.

The main goal of this thesis is to review and collect information about infrared imaging technologies, apply core information that has been acquired in the development phase of a Megapixel SWIR Imaging System. The major consideration of this thesis is developing camera electronics for image acquisition in SWIR band. Moreover, it also touches on some of the image processing algorithms that are used and prevalent in infrared imaging systems.

1.1 Work Motivation

Beginning from the mid of the past century there has been a great growth in semiconductor industry and semiconductors started to be used widely. One of the important areas that benefits from solid-state materials is imaging technology. The first image sensor was invented by Morrison in 1963 [4] and after that, other scientists followed him to develop different types of image sensors to detect various parts of electromagnetic spectrum from UV to THz.

Infrared imaging emerged to detect the electromagnetic waves that are in the infrared region, as the name implies. Infrared spectrum can be divided into sub-regions which are Near Infrared Region (NIR) ($0.7\ \mu\text{m}$ - $0.9\ \mu\text{m}$), Short Wave Infrared (SWIR) ($0.9\ \mu\text{m}$ - $2.4\ \mu\text{m}$), Mid Wave Infrared (MWIR) ($3\ \mu\text{m}$ - $5\ \mu\text{m}$) and Long Wave Infrared (LWIR) ($7\ \mu\text{m}$ - $14\ \mu\text{m}$)[5]. In the scope of thesis, the focus is on SWIR region due to the unique properties it has. Detailed information about unique advantages that SWIR holds is given in the next chapter.

It is no doubt that semiconductor technology keeps improving, which then boosts the demand for advanced infrared imaging systems. Technology trends and industrial demand push infrared systems to have more pixels with a smaller pitch, higher frame rates and better image quality[5]. The aim of this thesis is to show a method of developing a SWIR imaging system which can meet the demands of industry by reviewing theoretical background of infrared imaging and

electronics and applying the acquired core knowledge.

1.2 System Architecture

As stated in the previous section, technology trend pushes for better performance in imaging systems. To handle possible challenges in the way, it is best to define units in the overall system in a coherent scheme. A general system architecture can be seen in figure 1.1 and 1.2 for different imaging applications of interest.

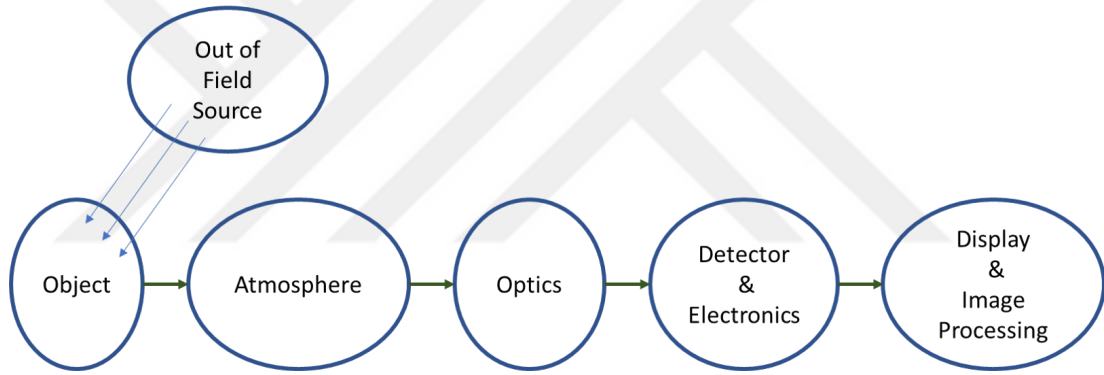


Figure 1.1: General purpose imaging system

[8]

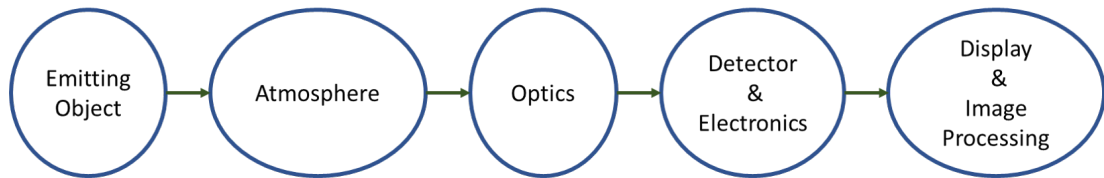


Figure 1.2: General purpose imaging system when object is a source

The most important piece in the system is certainly the light source. Detector should be chosen according to the properties of the targeted light source. The rest of the system should be designed to convert the output of the selected detector to a meaningful set of data; image. One should understand the nature and physics of light so as to design a high performance camera electronics. Literature review is carried out in chapter 2.

1.3 Objectives and Author Contribution

The main object of this thesis is to design a megapixel SWIR camera with highest performance possible. For successful accomplishment of this object, it is aimed to study the theoretical background for every unit. The measurable and clearly defined goals of this thesis are given as follows:

1. The imaging system should be able to monitor light in SWIR band of infrared region.
2. The resolution of the imaging system should be 1.3MP(1024x1280).
3. The maximum percentage of the dead pixels in the detector should be less than % 1.
4. The system should include a solution to eliminate the effects of dead pixels.
5. The dynamic range of the system should be more than 1000.
6. The detector temperature should be kept stable and under 20°C.
7. The system should carry out on-board Non Uniformity Correction.
8. The system should adjust itself according to intensity of light to achieve a good image of the scene in all light conditions.
9. The system should be watertight and airtight to be durable in all weather conditions.
10. The image flow rate should be greater than 25 FPS.
11. Image streaming to PC GUI and message flow for system controls should be done via Ethernet line.
12. The system should be powered by a single DC source with 12V.

The main contribution of the author of this thesis is reviewing theoretical background of imaging systems, designing camera electronics, testing manufactured

hardware and taking part in the integration of the overall system. Required software and mechanical hardware were designed by other members of Electro Optic Systems Division of NANOTAM. Design of mechanical hardware, camera software and image processing algorithms are beyond the scope of this thesis. However, some of the image processing algorithms and their advantages will be described to some extent.

1.4 Thesis Organization

This thesis is composed of 6 chapters. Chapter 2 is based on literature review for physics of light, basics of imaging and commonly used image sensor types. In this chapter, the required core information of imaging is acquired and summarized.

Chapter 3 concentrates on the design of the camera electronics. Details from detector selection to analog front end design are addressed. Necessary information to realize camera electronics correctly is studied and summarized.

Chapter 4 gives brief explanation for the need and methods for proper hardware design and then shows the designed PCBs that house designed electronic circuits.

Chapter 5 presents the test results carried out to evaluate the system performance. It also gives information about image correction techniques that are used in our system. Some of the images acquired by the system is demonstrated in this chapter.

In Chapter 6, test results and system performance are appraised. The difficulties that are faced during development process are mentioned. Possible solutions and future works are proposed.

Chapter 2

Literature Review

In this chapter, properties of light and approaches for detecting it are studied. In Section 2.1, historical evolution of understanding of light is given. Information about infrared spectrum and propagation of light in atmosphere is also provided in this section. Section 2.2 focuses on the basics of imaging technologies. In this section, the mechanism of light detection and basics of semiconductors are explored. Finally, in Section 2.3 commonly use image sensors are studied in detail.

2.1 Nature of Light

2.1.1 What is Light?

The history of optical technology can be traced back to antiquity. The Greek philosophers Pythagoras, Democritus, Empedocles, Plato, Aristotle, and many others came up with theories about the nature of light. They and countless more carried out experiments with accessories that can be used as mirrors and lenses to explore the nature of light. Leonardo da Vinci described the *camera obscura* which reveals that the passion for optics and light was continuing in the 15th and 16th centuries. On the way to modern optics, many scientists contributed

by discovering various optic phenomena such as diffraction, refraction, total internal reflection, interference and so on. These discoveries illuminated the way to understand the nature of light. Beside the progress taking place in optics, quite independently, the study of electricity and magnetism was prospering. In 1845, Michael Faraday observed that a strong magnetic field applied to the medium could change the polarization direction of a beam. With this knowledge, he established a link between electromagnetism and light. In a single set of mathematical equations, James Clerk Maxwell summarized and extended all empirical information on the subject. Maxwell arrived at the expression given in equation 2.1 in terms of electric and magnetic properties of the medium in which light was traveling when he solved for the speed of the wave.

$$c = \frac{1}{\sqrt{\epsilon_0 \mu_0}} \quad (2.1)$$

After substituting known, empirically determined values for the quantities in the expression, he obtained a numerical result equal to the measured speed of light. According to the conclusion he reached, light was an electromagnetic disturbance in the form of waves propagated through the medium. Heinrich Rudolf Hertz proved the existence of long electromagnetic waves in a series of experiments in which he generated and detected them. He confirmed Maxwell's conclusion and published it in 1888. On October 19, 1900, Max Planck presented a paper to the German Physical Society in which he described the origins of Quantum Mechanics, a theory that encompasses submicroscopic events. Einstein presented a new type of corpuscular theory in 1905, based on these notions, in which he claimed that light was made up of globs or "particles" of energy. Each such particle of luminous energy is called *photon*. Each photon has energy proportional to its frequency and the relation is shown in equation 2.2[6].

$$E = hf \quad (2.2)$$

In summary, light can be represented as both an electromagnetic wave and a particle.

2.1.2 Atmosphere, Its Windows and Propagation of Light

The atmosphere is the structure that surrounds and protects the earth, acting as a shield against damaging radiation and meteorites. The vast majority of imaging systems interact with the atmosphere. The quality of the images acquired by these devices is largely determined by atmospheric factors. The electromagnetic spectrum is subjected to some degree of absorption of electromagnetic energy by atmospheric gases and attenuation by atmospheric aerosols during its propagation throughout the atmosphere. Before the radiation or reflection from objects reaches the optical sensor, the radiant flux emitted by the target is selectively absorbed by many gases that make up the atmosphere, dispersed by small particles suspended in the environment, and modulated by abrupt changes in atmospheric quality. Optical propagation in this medium has many important characteristics and consequences for remote sensing, electro-optical system performance etc.[20][13][8].

The atmosphere is made up of gases and suspended particles at varied temperatures and pressures as a function of altitude and azimuth. The troposphere, stratosphere, mesosphere, ionosphere, thermosphere, and exosphere are the six main horizontal layers that make up the atmosphere. The first layer, which stretches from the ground to approximately 11 km height, contains the majority of the key atmospheric attenuators such as H_2O , CO_2 , clouds, fogs, aerosols, etc. Because of the high pressure and density in this layer, the maximum level of molecular scattering occurs here[13][21]. We are mostly concerned with the first layer and the atmospheric attenuators it has, when designing and using our imaging systems.

The term extinction is used to describe the combination of absorption and scattering. Beer's law, given in equation 2.3, states that extinction causes a decrease in the flux of radiation through the atmosphere. This is stated in terms of

an exponential coefficient that is the sum of the coefficients of the total absorption and the total scattering. These coefficients are proportional to the density and molecular composition of the atmosphere, as well as the number, compositions, and size distributions of aerosols[22][13].

$$\tau = e^{-\mu R} \quad (2.3)$$

Where;

τ : Transmittance of a path length R through the atmosphere,

μ : Extinction coefficient.

Absorption is more important than scattering in the infrared region of the electromagnetic spectrum. Water vapor, carbon dioxide, ozone, and oxygen absorb the most infrared light in the atmosphere[8]. The earth's atmosphere is opaque to vast sections of the electromagnetic spectrum as a result of such atmospheric effects. In figure 2.1 spectral transmission of the atmosphere is shown. The atmosphere absorbs and re-emits the radiation reaching the viewer at these wavelengths, and thus contains no information about the object to be observed. The atmosphere is transparent in some discrete sections of the spectrum. These spectral segments, which are known as "atmospheric windows" or just "windows", are defined by molecular absorption of mostly water vapor and carbon dioxide, and they're separated by extremely absorptive zones with essentially no transmission[13].

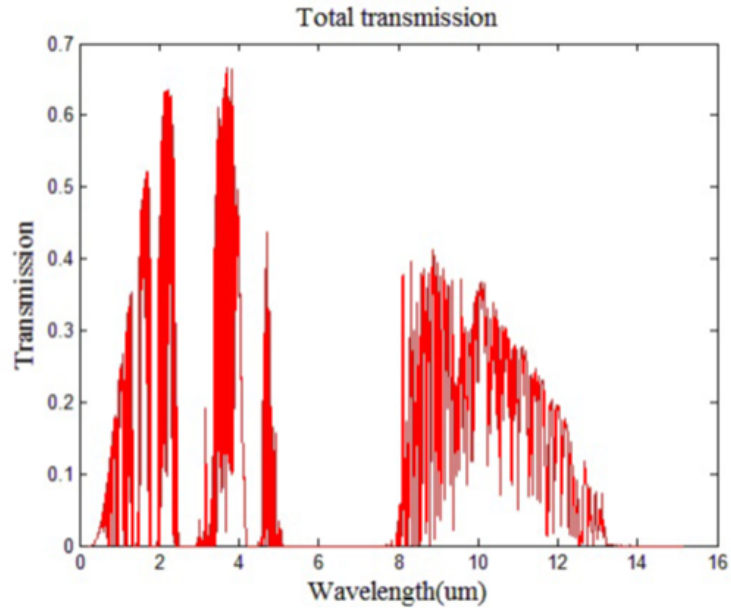


Figure 2.1: Total spectral transmission of atmosphere at 5 km range and 90 degree zenith angle[8]

Figure 2.2 shows the transmission levels in infrared spectrum and resulting atmospheric windows. The windows are visible and near infrared(VIS-NIR), short wave infrared(SWIR), mid wave infrared(MWIR) and long wave infrared(LWIR). The distinct properties these windows have are studied in detail in section 2.1.3 and 2.1.4.

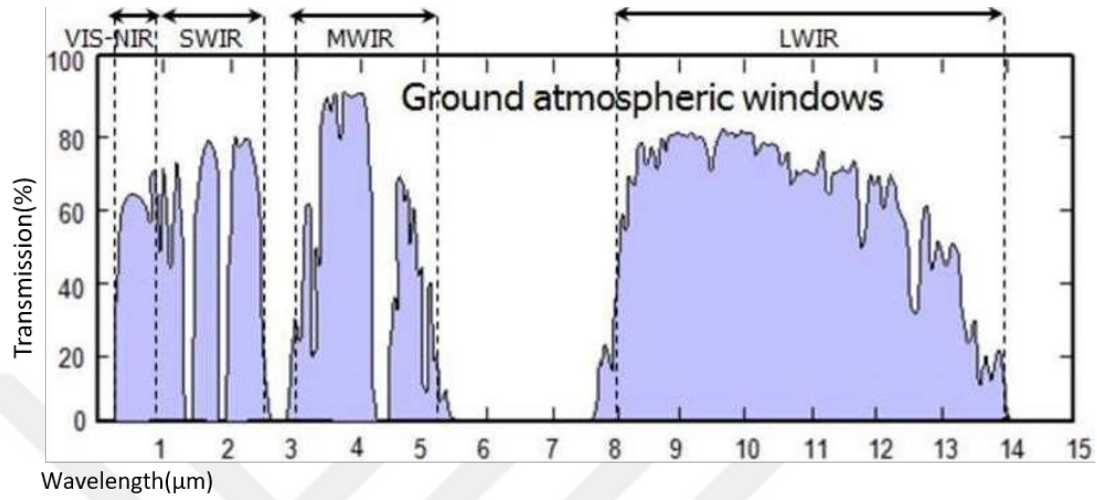


Figure 2.2: Range of the transmission of the IR spectra ground atmospheric windows[23]

2.1.3 Infrared Spectrum

Electromagnetic waves span from low frequencies which are called radio waves to high frequencies that we generally perceive as light. Even high energy particles fall into electromagnetic spectrum. The human eye can only see a small portion of the electromagnetic spectrum that is named as the visible light region. Visible region lies between the wavelengths of 400 nm to 700 nm. The longest wavelength is known as red light and the shortest wavelength is known as the violet. The region that contains light with smaller wavelengths than violet is called ultraviolet region whereas the region that holds light with larger wavelengths than red is named as infrared region. The complete electromagnetic spectrum including the spectral subdivisions is given in figure 2.3.

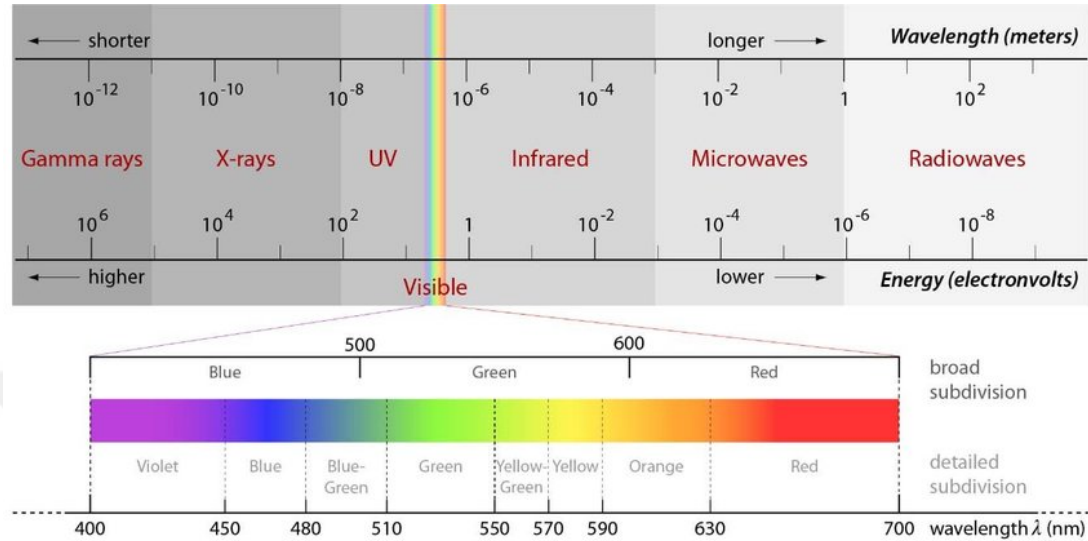


Figure 2.3: The complete electromagnetic spectrum with the spectral subdivisions of the visible waveband [10]

Infrared region lies between the wavelengths of around $0.7 \mu\text{m}$ and $1000 \mu\text{m}$ and infrared light possesses unique characteristics. For instance, the refraction properties of infrared light in some certain materials are different than that of visible light. As a result of these different properties, materials that are visible or opaque in visible light may be transparent or invisible under infrared illumination. Moreover, any material above the absolute zero (0 Kelvin) radiates in the infrared range of the electromagnetic spectrum. An important portion of aforementioned thermal radiation, occurs in infrared region. Therefore, any object can be seen by sensing the infrared radiation. Infrared imaging systems that possess infrared detectors are used in order to sense the infrared radiation.

Such properties of infrared light can be utilized in a wide variety of areas. For instance, dust particles which obstruct the visibility in space observations are invisible to infrared light and infrared imaging stands as a solution in such cases. Weather satellites can see through some cloud types and hence distinguish between different kinds of clouds thanks to the different refraction infrared light faces at different cloud types. Because objects thermally radiate by themselves, this thermal radiation can be employed in night vision applications without any

external light source. What is more, thermal vision helps in fault finding in circuits, detection of some health problems in humans, and automated target tracking in military applications [7][9].

Infrared spectrum can be divided into sub regions. The idea behind these sub regions are covered in section 2.1.2. These regions are shown in table 2.1 and figure 2.4.

Infrared Region	Waveband (μm)
Near Infrared (NIR)	0.75-0.9
Shortwave Infrared (SWIR)	0.9-2.4
Midwave Infrared (MWIR)	3-5
Longwave Infrared (LWIR)	7-14
Very Longwave Infrared	14-30

Table 2.1: Sub regions of infrared spectrum[8]

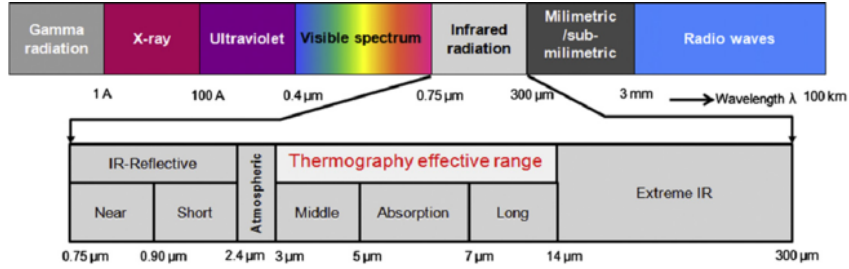


Figure 2.4: Infrared band with the spectral subdivisions [11]

All objects with a temperature above absolute 0 Kelvin emits infrared rays what we know as black-body radiation. For room temperature (300 K), black-body radiation is centered on 8 μm -12 μm band which falls into LWIR band. For that reason, LWIR band can be utilized in applications where human surveillance is the main concern. When it comes to higher temperature objects such as missile and aircraft plume, their detection is achievable at MWIR band. Because of the black body radiation, target objects produce infrared light in the MWIR and LWIR bands passively. As a result, no external light source is required for LWIR

and MWIR. However, if there is not a sufficient temperature difference between the object to be viewed and the background environment, detection of that object becomes impossible. Shortly, MWIR and LWIR sensors can't detect significant details unless there is enough temperature contrast between the object and the background[12][13].

Despite the fact that light in the SWIR region is invisible to the human eye, it interacts with objects in a similar way as light in visible region do. The image is formed with the reflected light just like it is formed in the visible range. Because of this, active illumination from sun or moon or an external SWIR source is needed for detection in SWIR. Considerable details of objects can be seen in SWIR imaging and hence target recognition becomes possible as it is in visible imaging since reflected light is used in both of the regions and there is not a requirement for large temperature differences between objects and their background. Moreover, because Rayleigh scattering of light at longer wavelengths is less, infrared light can travel through haze, fog, dust and high humidity without being scattered. This results in an advantage for SWIR cameras that they see better in various weather conditions than visible cameras. Also, since the image formation mechanism for SWIR is the same as it is in visible light, SWIR images seem much more natural to viewers than images taken in MWIR and LWIR in which emitted light is used for image formation[12][13][14]. In this thesis, the focus is SWIR imaging. The areas that SWIR imaging is used and the advantages it brings are represented in detail in section 2.1.4

2.1.4 Use of SWIR Band and Advantages

SWIR imaging technology has unique properties and thanks to them SWIR holds major advantages over both visible(VIS) imaging and thermal imaging in MWIR and LWIR bands. Visible and thermal cameras may be ineffective in some certain situations. In such situations, SWIR imaging becomes useful with its properties [19]. In this section, the virtues that SWIR imaging offers over visible and thermal imaging are discussed separately.

In adverse weather conditions visible imaging suffers from limited view. Similarly, when there is not enough temperature difference between the object to be imaged and the background, thermal imaging becomes impractical. SWIR cameras can present clearer images than visible cameras with their ability to see through haze, fog, smoke, dust. Also, without any temperature difference constraint, SWIR cameras can capture greater details than thermal cameras. Apart from imaging in harsh weather, long distance imaging through the atmosphere in SWIR is better in quality due to the reduced Rayleigh Scattering at longer wavelengths in which SWIR resides in[13][19].

Below is a list for comparison of SWIR with VIS and NIR[8]:

- The background radiation is weaker and the transmission through the atmosphere is higher in SWIR than it is in VIS and NIR. As a result of this, higher SNR values can be reached and hence better image quality is achieved in SWIR when compared to VIS and NIR band.
- Less exposure time is required in SWIR than VIS and NIR. So, stabilization is easier to achieve in comparison with VIS and NIR band.
- Because SWIR has a longer wavelength than VIS and NIR, atmospheric turbulence and dispersion are less effective.
- Thanks to the reduced Rayleigh Scatter of light at longer wavelengths, SWIR cameras can see through particles in the air such as dust, fog, and haze, better than visible cameras as shown in the figures 2.5 and 2.6[14].
- Military laser range finders and designators operate at 0.85, 1.06 and 1.55 μm . These wavelengths are often beyond the cutoff wavelength of VIS and NIR sensors, making them difficult to detect with these sensors. SWIR sensors are able to detect all of these wavelengths without any difficulty.
- Because SWIR light can travel through ordinary glass, it can be used with lower-cost optics.

- Because the wavelength of SWIR is longer than the wavelengths of VIS and NIR, the manufacture and alignment tolerances of lenses in SWIR optics are better.
- SWIR cameras passively image well under natural ‘nightglow’ illumination, and produce excellent imagery with active illumination from sources completely that cannot be seen by night vision goggles.



Figure 2.5: Visible imaging vs SWIR imaging in smoke[17]



Figure 2.6: Visible imaging vs SWIR imaging in haze[17]

Comparison with MWIR and LWIR[8]:

SWIR band is usually thought of as a complement to MWIR and LWIR bands. For this reason, a direct comparison is not appropriate between these wavebands,

although the following are the key advantages of SWIR over MWIR and LWIR:

- SWIR images are mostly formed by reflected broadband light sources, just like visible cameras. So, SWIR images seem much more natural[18].
- The dark current values in InGaAs FPAs, the most prevalent detector type used in SWIR cameras, have reduced significantly in recent years, allowing for the development of compact and low-power uncooled SWIR cameras[14]. Because cryogenic cooling for SWIR detectors is not necessary, the size, weight and power requirements are much reasonable than they are in MWIR and LWIR.
- In MWIR and LWIR applications expensive and peculiar materials are needed. This increases the overall cost. On the other hand, conventional glasses and coating materials that are used in visible imaging systems can be utilized in SWIR, allowing for low cost imaging systems.
- SWIR imaging uses shorter wavelengths than MWIR and LWIR imaging. Thanks to this, pixels with smaller sizes can be employed in SWIR detectors. Hence, SWIR FPAs that are more compact and have a greater resolution can be made without any limitation that can be caused by the optical diffraction[14].
- Thermal imagers, that are mostly used in MWIR and LWIR bands, basically detect the photoemission of objects and surfaces due to the black body radiation related with their temperatures. As an advantage of this detection mechanism, thermal cameras outdo at detecting temperature differences, if there is any, in a scene. This ability makes thermal cameras useful for imaging people and animals, especially for night-time surveillance. However, resolution is limited because of the long wavelengths associated with LWIR and MWIR. Unnatural image appearances occur due to the low resolution, making it difficult for thermal camera users to distinguish between people and vehicles under surveillance. As a solution to this problem, SWIR imaging and thermal imaging can be used together within a system

in which thermal imagers detect any black body radiating object and then SWIR imagers identify the detected object[18].

With the exclusive characteristics attributed to SWIR imaging, it finds numerous usage and application areas. We can separate the application areas into subcategories on the basis of operations they are used in.

Military Applications are as follows[18]:

- In battlefield, located targets can be visualized and seeking targets which are marked by eye-safe lasers is possible. For such purposes, SWIR imaging can be used for target acquisition and tracking.
- SWIR imaging can be used in surveillance and passive imaging by utilizing the atmospheric night glow to illuminate scenes on moonless nights.
- Especially at night-time, detection of muzzle flare and target strikes with a SWIR camera helps in sniper detection and spotting. An example is shown in figure 2.7.
- Identification of natural and man-made materials with SWIR, camouflage detection becomes possible with SWIR imaging.
- With the ability of recognition of unique wavelengths of battlefield light sources, SWIR helps greatly in identification of friend or foe.
- Imaging through fog, haze and dust helps in battlefield.
- With spectral identification of materials explosive materials can be detected by SWIR imaging.



Figure 2.7: Muzzle flare detected by SWIR[18]

Industrial Usage:

- Line scan SWIR cameras for continuous processes or area cameras for moving objects are utilized in production lines for inspection and sorting purposes.
- Different types of plastic respond differently under SWIR illumination. This property helps in recycling operations by helping in plastic type identification.
- Failure analysis or inspection through silicon structures like integrated circuits or nano-structures is carried out with SWIR cameras. Therefore, SWIR imaging is also utilized in semiconductor industry.
- NIR Spectroscopy can detect and monitor moisture, lipids, proteins, soil types, pharmaceutical chemical and coatings to be used in quality control processes[18].
- SWIR cameras can be used to see the invisible laser light for beam profiles, which helps in alignment of telecommunications fibers and sources and engineering and inspecting optical waveguides at wavelengths of $1.31\mu\text{m}$ and $1.55\mu\text{m}$ which are utilized in fiber optic communications [19].

Clinical and Biomedical Applications:

- Wavelength dependent scattering that occurs with the particles in the air is also the case in biological tissue as well as in industrial coatings, semiconductors and fiberglass circuit boards. As a result of wavelength dependent scattering, longer wavelengths are able to penetrate deeper into the biological tissue than shorter wavelengths. A relatively new method named as optical coherence tomography (OCT), utilizes SWIR wavelengths for increased penetration depth[19].
- Structures that reside deep within biological tissue are hard to visualize and detecting them becomes a major difficulty to overcome in biomedical imaging. SWIR cameras make imaging of those structures possible with high resolution, high sensitivity, and sufficient penetration depth to noninvasively interrogate sub-surface tissue features[15].
- Another biomedical application that makes use of NIR/SWIR cameras is vein location for administering intravenous medicine or blood transfusions. Even though medical officials are able to locate veins generally by feel with the help of their experience, in some cases such as in elderly or infant patients or under battlefield conditions, vein location may pose a big problem. Figure 2.8 shows an image, demonstrating the potential of using SWIR imaging for vein locating[19].



Figure 2.8: Finding vein location with SWIR camera [19]

Navigational Purposes:

- As stated before, SWIR wavelengths span from 1 to $3\mu\text{m}$. Astronomers have defined bands within the SWIR spectrum suitable for astronomy because of the high transmittance through the atmosphere.
- Most star tracking systems operate in space, either on spacecraft or satellites. As long as the star tracker is not pointing directly at the sun, the background light is limited. Therefore, in most space-based systems a Charged Coupled Device (CCD) sensor is used, operating in the visual spectrum at about $0.4 - 0.8\mu\text{m}$. CCD sensors are also often the selected sensor in lunar rover applications. When investigating the use of star trackers on earth however, the background light from the sun and the moon becomes significant. The atmospheric transmittance must also be taken into account, which affects the choice of sensor and wavelength filters. In summary, navigational systems, especially on earth, is an area in which SWIR cameras can be utilized [16].

2.2 Infrared Imaging Basics

Semiconductor technology has changed the world as no other invention did. It gave humankind a power that was not imaginable. Calculations have shifted from paper to billions of operations in seconds. We can communicate from any point on earth, even among planets. The hero of that achievement is silicon, a semiconductor[24]. Semiconductor industry also gave rise to imaging technologies. In this section, basics of imaging, specifically infrared imaging is covered.

2.2.1 Historical Background in Infrared Imaging

Sir William Herschel discovered the radiant energy that is beyond the visible spectrum in 1800, while he was trying to spread sunlight into its component colors, in other words wavelengths, using a prism. After seeing different colors, he tried to measure temperature of those colors that correspond to different portions of visible spectrum using a thermometer. He saw that the thermometer showed a significant heating effect even at places where he didn't see any color. Since then, the detectors were designed and optimized to with an aim to come up with sensitive thermometers[25]. Herschel's experiment was described by Hudson in 1969 and an illustration for Herschel's experiment is shown in figure 2.9. Of course, we know that not all infrared sensors use heating effect for infrared detection. Those will be covered in detail in the following sections.

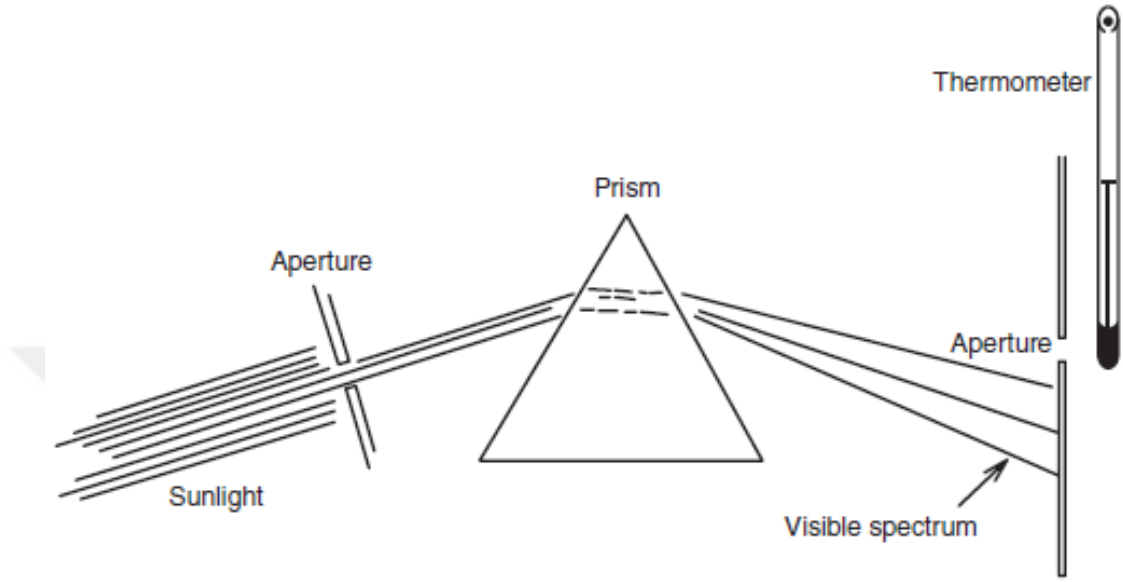


Figure 2.9: Herschell's IR detector[25]

From the middle of the past century, semiconductor technology has become prevalent and various areas have begun to utilize semiconductors within their applications. One notable area that makes use of semiconductors is imaging technology. In 1963, Morrison marked the beginning of an era by inventing the first image sensor[4] and other works together with inventions continued in the field leading image sensors to be adopted extensively. Thenceforward, image sensors with various types have been developed in order to sense separate regions of electromagnetic spectrum from UV to THz[5].

2.2.2 Infrared Detectors

An infrared detector detects infrared light and converts it into electrical signals, which are subsequently processed to create an image. IR radiation can be detected using a few detection techniques[1]. IR detectors are separated into sub categories on the basis of the detection mechanisms they utilize.

Detection mechanisms of infrared radiation fall into three categories that are

photon detection, wave interaction detection, and thermal detection. Table 2.2 gives the classification of infrared detectors [26].

Photon	Wave Interaction	Thermal
Photoconductivity(PC)	Optical Heterodyne	Bolometer
Photovoltaic(PV)	Photon-assisted tunneling	Thermocouple/thermopile
Photoelectromagnetic	Optical parametric	Pyroelectric
Phototransistor	Schottky barrier mixer	Golay cell microphone
Photon drag	Metal-oxide-metal	Absorption edge
Photoemissive		Pyromagnetic
Quantum counter		Liquid crystal
		Thermomechanical

Table 2.2: Classes of infrared detectors[26]

The most common infrared detection mechanisms are photon and thermal detection, which depend on the intensity of the incident electromagnetic radiation. On the other hand, wave interaction effects depend on the magnitude of the incident electric field vector, and none of the efforts that have been made to apply this technology to the detection of infrared radiation has proven to be practical[26]. For this reason, throughout this section the main focus will be on the theory and the working principle of thermal and photon detectors.

2.2.2.1 Band Structures of Semiconductors

To figure out the working principle of detectors, one needs to have an understanding of band structures of semiconductors, which are utilized as detector materials. Band structures of semiconductors is a highly complex topic and it is not possible to cover it entirely in this thesis. But still, gaining a basic understanding of this topic is extremely critical for comprehension of detectors' operation and in the selection phase of a detector for a specific application.

There are two very important models or visualization aids that are used extensively in the analysis of semiconductor devices. They are bonding model and energy band model[34].

Since we are focused on detectors and more interested in energy related aspects of the events that happen within a semiconductor, energy band model is the primary visualization aid[34].

For an isolated atom, the electrons can have discrete energy levels. The unit of the energy is eV and it corresponds to the energy gained by an electron when its potential is increased by one volt. If two identical atoms are placed far apart from each other the allowed energy levels for a given principal quantum number (e.g., $n = 1$) consist of one doubly degenerate level; that is, both atoms have exactly the same energy. When they are brought closer, the doubly degenerate energy levels will split into two levels by the interaction between the atoms. The split occurs due to the Pauli exclusion principle, which states that no more than two electrons in a given system can reside in the same energy state at the same time. To form a solid, a number of, let's call it N , isolated atoms are accumulated together. The orbits that house the outer electrons of N different atoms overlap and begin interacting with one another. It is known that in the case of two interacting atoms, a shift in energy levels occur. Similarly, a shift in the energy levels also occurs in the case of interaction of N different atoms, including the forces of attraction and repulsion between them, creating N separate but closely spaced energy levels. If the number N becomes very large, this yields continuous band of energy. The band that is formed can extend over a few eV at the inter-atomic distance of the crystal. The electrons can no longer be treated as belonging to their parent atoms. They belong to the crystal as a whole. In figure 2.10, this phenomenon is shown. In the figure, a stands for the inter-atomic distance of the crystal[33].

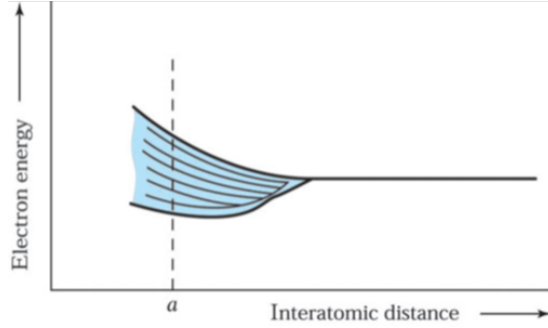


Figure 2.10: The splitting of a degenerate state into a band of allowed energies[33]

When temperature is absolute zero (0K), electrons occupy the lowest energy states. This causes all states that are in the lower band, also known as the valence band, to be full and all states that are in the upper band, also known as the conduction band, to be empty. The bottom of the conduction band is labeled as E_C and the top of the valence band is named as E_V . The bandgap energy E_g is defined as the energy difference between E_C and E_V and it is given with the relation $E_g = E_C - E_V$. E_g is also shown at the far left of the figure 2.11 marking the width of the forbidden energy gap. E_g is the required amount of energy to break a bond in the semiconductor to free an electron to the conduction band and leave a hole in the valence band.

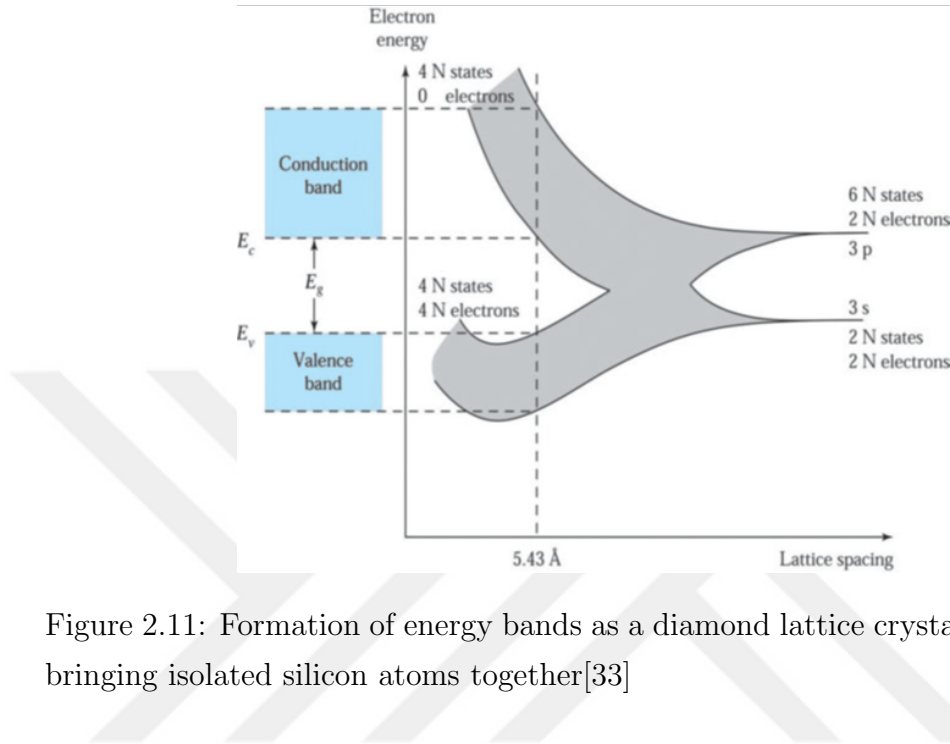


Figure 2.11: Formation of energy bands as a diamond lattice crystal is formed by bringing isolated silicon atoms together[33]

Energy-momentum diagrams can be generated using effective-mass concept for electrons. The effective-mass concept is extremely beneficial since it allows us to regard electrons and holes as classical charged particles and gain a better understanding of them. The theory behind effective-mass concept is beyond the scope of this thesis and no further information about it is given in this thesis.

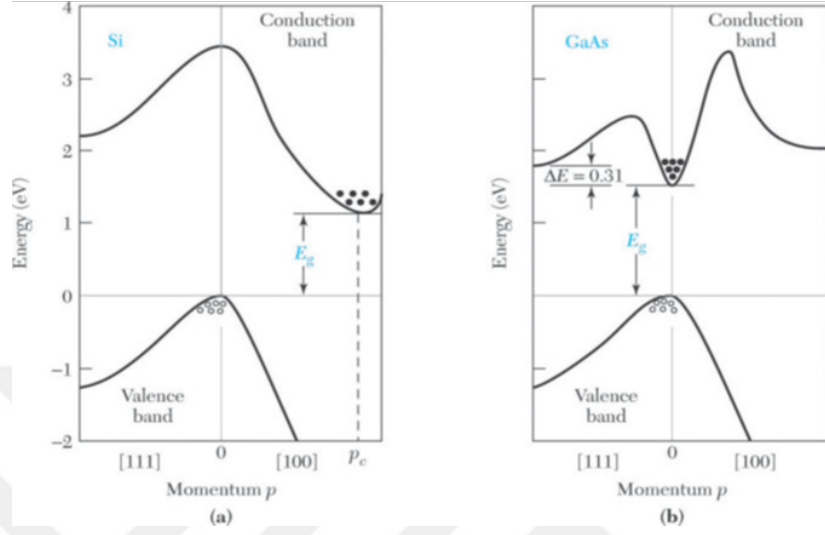


Figure 2.12: Energy band structures of (a) Si and (b) GaAs. Circles ($\circ$) indicate holes in the valence band and dots ($\bullet$) indicate electrons in the conduction bands[33].

The bandgap, E_g , lies between the bottom of the conduction band and the top of the valence band. The energy-momentum, E - p , curves are generally parabolic near the minimum of the conduction band or the maximum of the valence band. For silicon, the maximum in the valence band is reached at $p = 0$ whereas the minimum in the conduction band occurs along the 100 direction at $p = P_c$ as illustrated in fig. 2.12 a. For this reason, when an electron makes transition from lower band to upper band an energy change of ($\geq E_g$) is not enough. Some amount of momentum change at around ($\geq E_g$) is also necessary. Silicon is called an *indirect semiconductor* since a transition requires not only the bandgap energy but also some amount of momentum change. On the other hand, for gallium arsenide, the maximum in the valence band and the minimum in the conduction band occur at the same momentum, at ($p = 0$) as shown in figure 2.12b. For this reason, an electron that makes transition from the valence band to the conduction band doesn't require any change in its momentum. Therefore, gallium arsenide is called a *direct semiconductor*[33].

Being direct or indirect of a semiconductor has a primary effect on electron hole pair creation and it is an important property for a semiconductor which is

used as a detector.

2.2.2.2 Photon Detectors

According to the Planck's law, photons have an energy with the relation $E=hf$, where h is the Planck's constant and f is the frequency of the incident light. Direct bandgap semiconductors can absorb photons provided that the incoming photon's energy is higher than the bandgap energy of the semiconductor. In the case of an incident photon with a higher energy than a direct semiconductor's bandgap, photon interacts with an electron in the valence band and moves it into the conduction band leading to formation of an electron-hole (E-H) pair. Yet, if the semiconductor is indirect bandgap type, incident photons may not provide required momentum change for the electron excitation to the conduction band and hence may not create an electron-hole pair[12].

Photon detectors utilize low bandgap semiconductors and these detectors generally use a photodiode as a photo detector. Photodiode is a reverse biased p-n junction device which generates electron hole pairs if there are incident photons. Figure 2.13 shows that absorbed incident light creates electron-hole pairs, explaining the photocurrent generation. These E-H pairs need to be separated and this is achieved with the help of an electric field. The required electric field can be generated by either applying a bias externally or creating a built-in electrical potential. The amount of the photo-generated current is proportional to the number of incoming photons. This can also be defined as the intensity of light. In the case of an incident light, photo-excited electrons are accumulated in capacitors that are placed in the ROIC(Read Out Integrated Circuit). Analog to digital converters convert the electrical potential formed on these capacitors into digital signals, which can then be used to form the image an object[1][12][27][30].

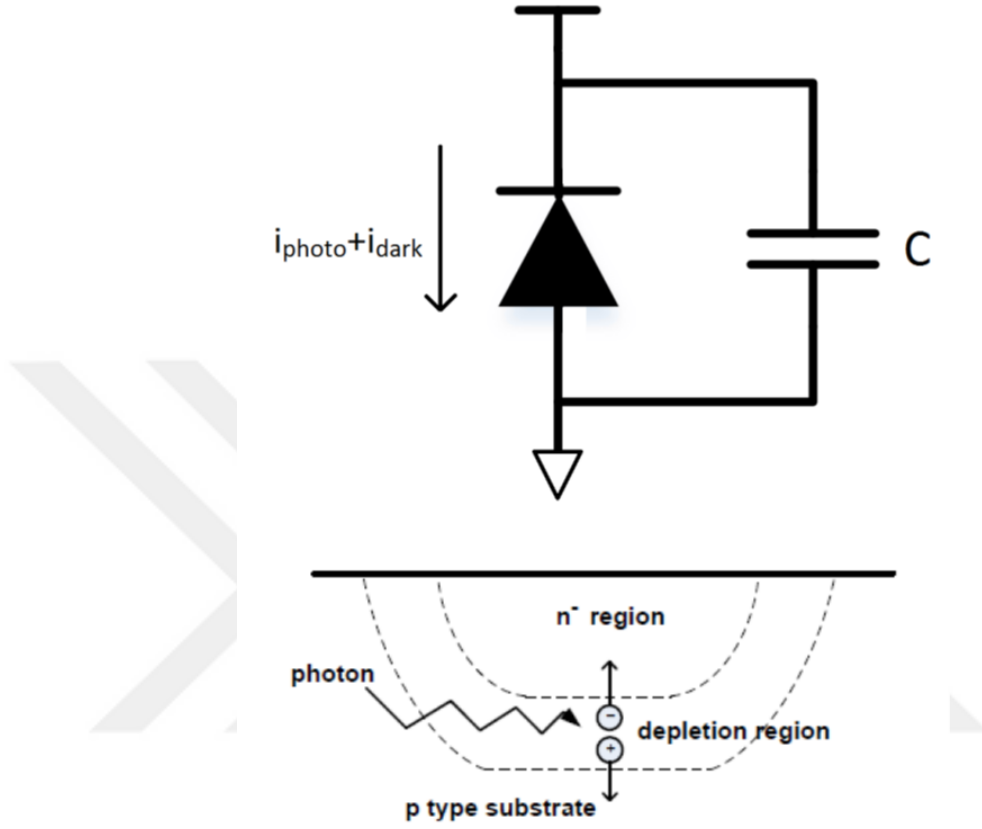


Figure 2.13: Photodiode model and electron hole pair generation mechanism[4].

The photo-generated current is quite small in comparison with the bias currents of analog circuits. For this reason, electrons are collected during an integration period. This integration period should be chosen in such a way that sufficient amount of electrons accumulate for a successful readout operation.

$$Q_{\text{collected}} = I_{\text{photo}} \times T_{\text{integration}} \quad (2.4)$$

Equation 2.4 shows the direct relation between collected charge ($Q_{\text{collected}}$), photogenerated current (I_{photo}) and integration period ($T_{\text{integration}}$). It is obvious that, selecting a longer integration period helps collecting more charges induced by incident photons. Collected or integrated charge in other words, is stored inside pixel capacitors. Junction capacitor of the reverse biased photodiode can be

utilized for charge storage purpose. Other alternatives to realize the charge storage capacitor make use of CMOS process layers, such as MOS gate capacitance and MIM capacitor. Selection between these alternatives is made with an aim to reach sufficient Full Well Capacity for the targeted application[12].

In addition to photonic excitation, thermal excitation is another E-H pair generating mechanism in photon detectors. Because of these extra sources of E-H pair generators, detecting IR radiation by photon detectors has several challenges. Because the energy of IR radiation in the MWIR and LWIR bands is comparable to the phonon energy of materials at room temperature, infrared photonic detectors must be cooled to cryogenic temperatures ($\approx 77\text{K}$), with the exception of those utilized in the near infrared range, in order to suppress the unwanted thermal generation which contributes to the total photo generated current as noise. However, cryogenic cooling increases the system's cost and overall power dissipation, and also makes it bulkier and more sophisticated. Some examples of photon detectors are Mercury Cadmium Telluride (MCT), Indium Antimonide (InSb), Quantum Well Infrared Photodetector (QWIP), and Supper Lattice Detectors[1][27][30].

2.2.2.3 Thermal Detectors

Thermal detectors make use of the heat power that is introduced by IR radiation. When IR radiation is absorbed by a material, it heats the material up and the material's temperature rises. The rise in the temperature produces a change in the active material's electrical properties, which are then transformed into meaningful electrical signals to create an image. For example, the main working principle of a bolometer, which is the most common thermal detector type used in thermal imaging systems, is conductivity change due to IR light absorption[28][1].

Different from photon detectors, thermal detectors can operate at room temperature and do not need to be cooled down to cryogenic temperatures. For this reason, they are also called uncooled infrared detectors. In spite of their lower performance, uncooled infrared detectors have a wide application area thanks to

their advantages such as low cost, low power dissipation, and small size, making them suitable for large volume commercial applications[9]. The output of a thermal detector is directly dependent on the amount of the absorbed power. The surface of the detector is blackened in order to reach maximum possible absorbance. If all of the incoming energy is absorbed by the detector, then the output of the thermal detector becomes directly proportional to and only dependent on the absorbed power. As a result of this, the responsivity is independent of wavelength and it is given with the unit volts/watts. For photon detectors, responsivity is affected by the wavelength of the incident light and it increases linearly with wavelength [25]. Some examples of thermal detectors are bolometers, thermocouples, thermopiles and pneumatic detectors.

When compared with each other, photon detectors are known for their superior performance over thermal ones on the basis of detector response time, NETD and multispectral operation. However, imaging systems that employ photon detectors are generally bulkier and more expensive when compared to imaging systems with thermal detectors. These are the trade-offs and selection between them is made considering the targeted application. For example, in applications where performance is the key criteria and other parameters such as size weight and cost are not limiting factors, photon detector based imagers are used. However, if size, weight, and cost considerations are more important, then cameras with thermal detectors are preferred[29].

2.3 Common Image Sensors

Visible and thermal image sensors are realized and utilized in different forms. In this section some of the commonly used image sensors are covered. Information about their working principle, physical structure, advantages and disadvantages is given.

2.3.1 CCD (Charge Coupled Devices)

The charge-coupled device (CCD) was invented in 1969 by scientists at Bell Labs in New Jersey, USA. For years, it has dominated the imaging technology and it has been used in applications from digital astrophotography to machine vision inspection. The CCD sensor is a silicon chip that is composed of an array of photosensitive sites. Figure 2.16 shows the block diagram of a CCD. The term charge-coupled device refers to the method of sensor's operation. CCDs operate in a manner that charge packets are carried around on the chip from the photosites to readout. This operation is also similar to an analog shift register, and it can also be explained by analogy with a bucket brigade shown in figure 2.14[35].

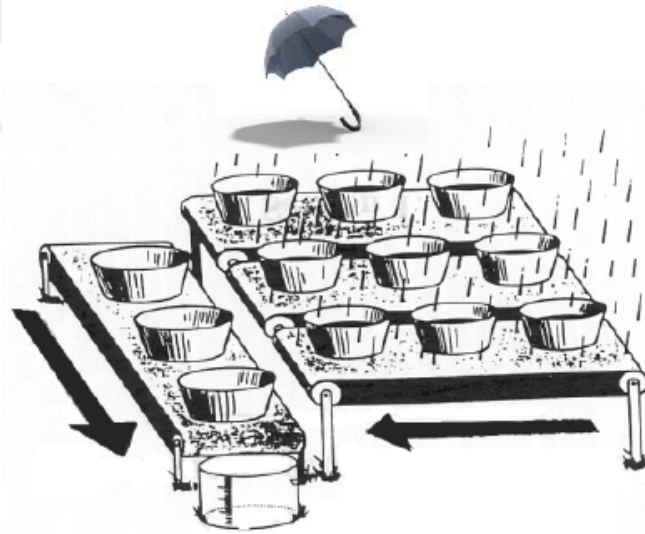


Figure 2.14: An illustration of a bucket brigade[36]

The working principle of image-sensing CCDs is the combination of the photosensitive nature of a semiconductor with their behavior as analog shift registers. As photons strike the surface of a semiconductor, they produce electron-hole pairs. This is a similar mechanism with what other silicon photo detectors have. But, instead of supplying a DC current that is proportional to the amount of incident light, each CCD photosite collects and traps these electrons into a charge packet. The array of charge packets records the spatial differences in luminous

intensity of the picture focused onto the sensor by integrating the electrons over time[37].

After the collection of charges in the photosites, clock pulses create potential wells as seen in figure 2.15, and the signal charge packed in this potential well is subsequently transported via the semiconductor to the output section. This is why CCD is also known as an analog shift register. Carried charges stored in a capacitor and gets converted to voltage just before readout amplifier. Digitization of this voltage can be carried out both internally and externally according to demands of application[38][37].

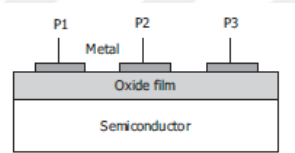


Figure 2.15: CCD basic structure and potential well[35]

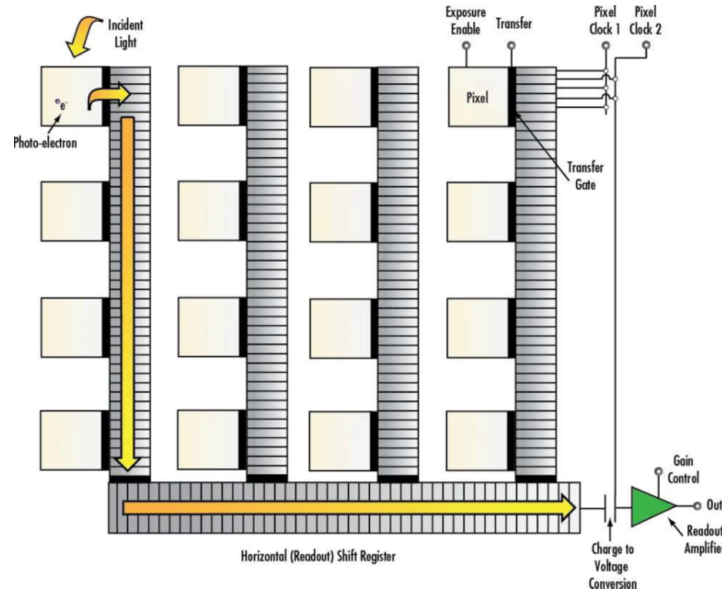


Figure 2.16: Block diagram of a Charge-Coupled Device[35]

The charge packets are limited to the speed at which they can be transferred. This is the main limiting factor for the CCD speed. However, CCDs have high

sensitivity and pixel to pixel consistency. Moreover, because each charge sees the same voltage conversion, uniformity across photosensitive areas is quite high.

Another drawback of CCD image sensors is blooming. Due to finite well depth or limited charge holding capacity, charge from one photosensitive site overflows over to nearby sites, causing blooming which can be seen in figure 2.17. This is a limitation factor for the dynamic range of CCDs. When charge is transferred vertically, the same effect reveals itself as smearing out of bright spots as seen in figure 2.18 [35].

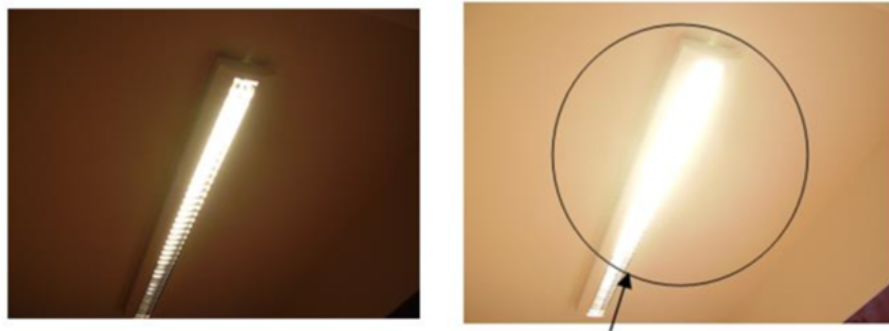


Figure 2.17: Example of an image suffering from blooming[46]

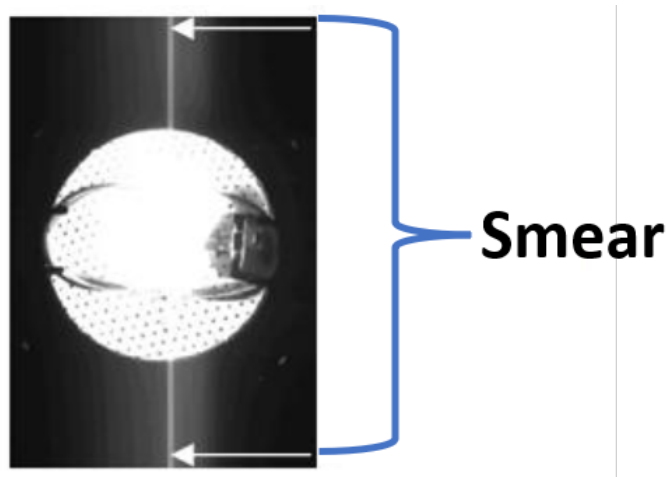
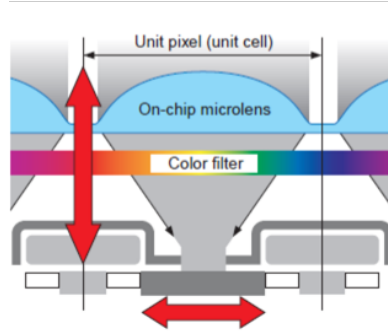
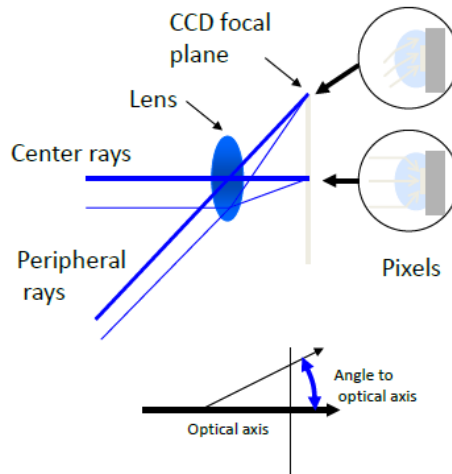


Figure 2.18: Example of an image suffering from smearing[46]

In order to overcome the negative effects of low well depth in CCD sensors,



(a) Microlens structure of Super HAD CCD from Sony[46]



(b) Angular sensitivity problem Introduced by microlens[36]

Figure 2.19: Microlens a) structure and b) angular sensitivity problem

microlenses whose structure is illustrated in 2.19a are utilized. Microlenses increase the fill factor or the effective photosensitive area. This method improves efficiency of the pixels but increases the angular sensitivity for incoming rays. This angular sensitivity requires the incoming rays to hit the sensor near normal as shown in figure 2.19b[35].

2.3.2 CMOS Image Sensors

CMOS stands for Complimentary Metal-Oxide Semiconductor. In a CMOS sensor, the signal is multiplexed by row and column once the charge from the photosensitive pixel is transformed to a voltage at the pixel location. Each site is made up of a photodiode and three transistors that perform activities such as pixel resetting or activation, amplification and charge conversion, and selection or multiplexing. A general system diagram is shown in figure 2.20. This structure enables CMOS sensors to reach high speed. On the other hand, it accounts for the low sensitivity and significant fixed-pattern noise caused by the inequalities of the fabrication of multiple charge to voltage conversion circuits[35].

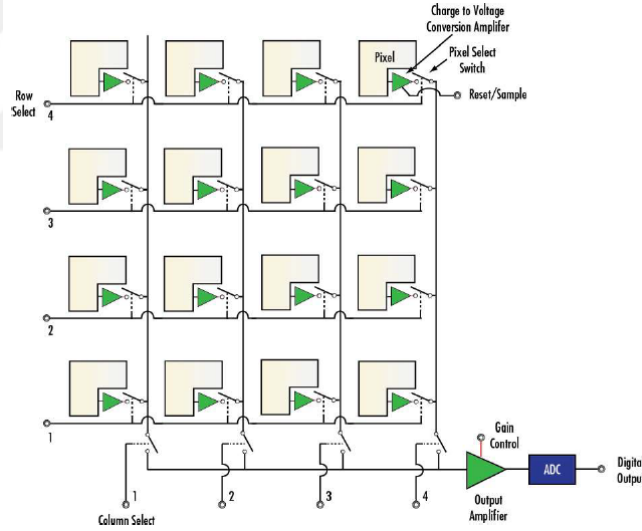


Figure 2.20: Block diagram of a Complementary Metal Oxide Semiconductor (CMOS)[35]

The multiplexing configuration of a CMOS sensor is generally accompanied by an electronic rolling shutter. CMOS image sensors account for lower consumption and dissipation of power than an equivalent CCD sensor. The main reason for this reality is that there is less flow of charge, or current in CMOS image sensors. Moreover, CMOS image sensors are able to handle high light levels without blooming. With the advantage acquired by this property, they can be employed in high dynamic-range cameras that can image welding seams or light filaments, for

example. In addition, CMOS cameras are typically smaller and lighter than their digital CCD equivalents, because of the fact that digital CCD cameras need additional off-chip ADC circuitry whereas ADCs can be implemented within CMOS image sensors.

The multilayer MOS fabrication process of a CMOS sensor does not allow the use of microlenses on the chip. This results in reduced efficiency or fill factor of the sensor when compared to CCD equivalent. Low efficiency and pixel-to-pixel inconsistency of CMOS image sensor lead to a lower signal-to-noise ratio and lower overall image quality than CCD sensors exhibit[35].

2.3.3 InGaAs Sensors

Silicon based detectors, CCDs and CMOS detectors, are generally used in high performance imaging applications, that includes detecting wavelengths from soft x-ray to near infrared. Typically, the quantum efficiency (QE) of the silicon based detectors decreases rapidly as the detection wavelength reaches the near infrared region. Silicon is transparent to light with wavelengths above 1100nm and it cannot be used to detect light in these wavelengths. However, there are many other materials that have photon sensitivity at these wavelengths and even at longer wavelengths. Some examples of such materials are Indium Gallium Arsenide-InGaAs-(400nm - $2.6\mu\text{m}$), Germanium-Ge-(800nm - $1.8\mu\text{m}$), Indium Antimonide-InSb-($1\mu\text{m}$ - $5\mu\text{m}$) and Mercury Cadmium Telluride-HgCdTe-($1.5\mu\text{m}$ - $12\mu\text{m}$)[39].

Each material type has their own advantages and is used as detector for sensing light in different sub regions of electromagnetic spectrum. The main goal in this thesis is to develop a SWIR camera. For this reason, the concentration is on InGaAs detectors which are sensitive between 400nm and $1.7\mu\text{m}$.

2.3.3.1 Detector Structure

InGaAs is a semiconductor material which is an alloy of Indium Arsenide (InAs) and Gallium Arsenide (GaAs). The doped InP substrate and InGaAs layer are used to construct a photodiode array (PDA) which delivers photosensitivity, typically for wavelengths between 400nm and $1.7\mu\text{m}$. The photodiode array is then indium bump bonded to a CMOS ROIC (ReadOut Integrated Circuit), which is used to perform the charge to voltage conversion, and transfer data from sensor either in analog or digital[39].

Indium bumps provide the required electrical connection between InGaAs photodiode array and the ROIC. Young's modulus, a mechanical property that measures the tensile or compressive stiffness of a solid material, of indium is lower than that of gold, copper and aluminum and indium has a melting point of 157°C . This means that any distortion that may be caused by heat, can be suppressed by indium. As a result, indium is suitable for connecting metals and semiconductors with different thermal expansion coefficients.

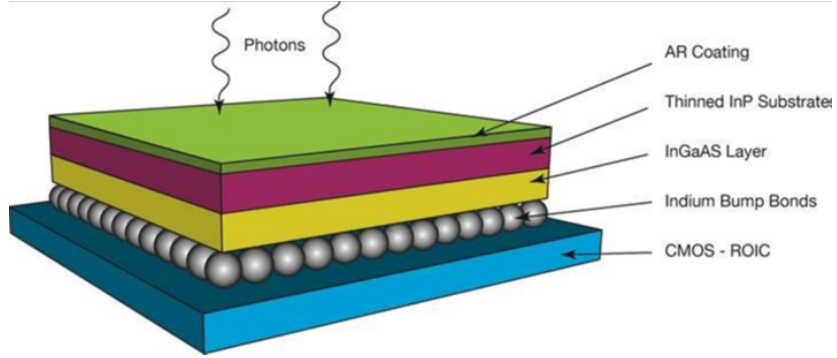


Figure 2.21: Schematic representation of the main components used in the construction of a VIS-SWIR InGaAs detector array[39]

The hybridized sensor structure that is shown in figure 2.21 is assumed to be illuminated through the substrate layer just as shown in the figure. Resulting quantum efficiency (QE) curve is shown in figure 2.22. The InP substrate layer, prevents wavelengths $\leq 900\text{nm}$ from reaching the InGaAs layer, causing the lack of visible response observed on many InGaAs detectors. However, if the bulk of

this InP substrate layer is removed, in other words thinned away, it produces a detector which has high responsivity across visible, NIR and SWIR regions. A broadband AR coating is also applied to the thinned PDA, producing a detector array which has excellent QE across the SWIR and NIR regions and good QE extending into the visible region[39].

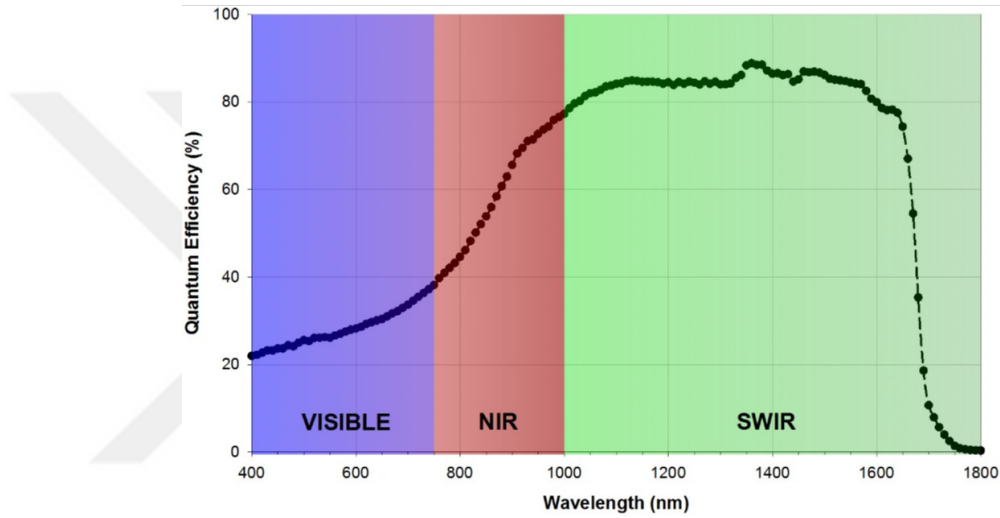


Figure 2.22: Typical QE curve for a InP thinned, AR-coated, VIS-SWIR InGaAs detector array[39]

Figure 2.23 shows another representation of QE spectral response difference between InGaAs detector with InP substrate and InGaAs detector with thinned InP layer.

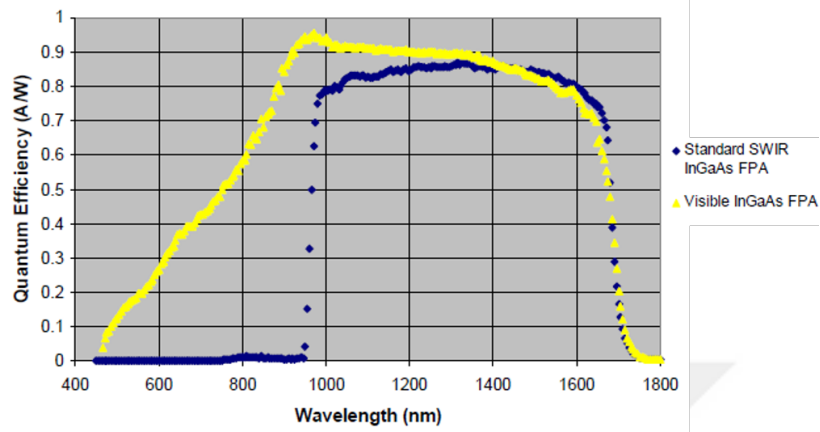


Figure 2.23: QE Curves for standard InGaAs FPA with InP (Blue curve) and InGaAs FPA with thinned InP layer (Yellow curve)[40]

The long wavelength cut-off is dependent on the InGaAs material and can be extended out to as far as $2.6\mu\text{m}$ by increasing the fraction of InAs within the alloy. The data presented in figure 2.22 and figure 2.23 show sensors with a long wavelength cut-off at around $1.7\mu\text{m}$.

2.3.3.2 ROIC

ROICs (Read Out Integrated Circuits) are used to gather the photo generated charges by the detector. ROICs convert charge to voltage by accumulating them into a capacitor over a period of time. This period of time is the integration time and the capacitor in which the charge is stored is called the integration capacitor.

The gain of the ROIC is adjusted by switching between integration capacitors which have different values from each other. When integration capacitor is low valued, then the ROIC gain is high. And conversely, when integration capacitor is high valued, then the ROIC gain is low. This can also be inferred from the relation between charge stored in a capacitor and the voltage across it, shown in equation 2.5.

$$Q = C \times V \quad (2.5)$$

Charge and voltage relation of a capacitor. Q : charge in coulombs, C : capacitance in farads, V : voltage in volts

2.3.3.3 Detector Performance Parameters

2.3.3.3.1 Non-uniformity

InGaAs area image sensors are composed lots of, in some applications even more than a million, different InGaAs photodiode elements arranged in an order to form an area image sensor. The sensitivity of each photodiode is different from each other. This may result from crystal defects in the InGaAs substrate, process variations during manufacturing of InGaAs detector or inconsistencies in pixel amplifiers of the ROIC. Because of this fact, some level of non-uniformity is present in the images that are acquired with InGaAs detectors[41].

This undesired effect can be overcome by applying signal processing to the acquired image. Each photodiode's responsivity is recorded, and after the acquisition of an image, correction factors are applied to each pixel value to make all of the photodiodes' responses to look uniform.

2.3.3.3.2 Dark Current

The dark current is the current that is generated even when there is no source of illumination. The total output is the sum of diffusion current, recombination current and surface leakage current of the photodiode.

High dark current both reduces dynamic range and makes it difficult to detect low level of light sources. Keeping in mind that the video signal is a combination of the output generated by incident light and dark current, image processing algorithms to subtract the dark current can increase overall image quality.

Equation 2.6 gives the total dark noise [41]. Where;

V_d : Dark output (V)

I_D : Dark current(pA)

T_s : Integration time(s)

C_f : Integration capacitance

V_{off} : ROIC offset voltage

$$V_d = I_D \times \frac{T_s}{C_f} + V_{off} \quad (2.6)$$

The small bandgap of InGaAs (approximately 0.75eV at room temperature) means that it is much easier to thermally excite electrons from the valance band into the conduction band, compared to other semiconductors, silicon for example. Due to this, in general, significantly higher dark currents are reported for InGaAs detectors when compared to silicon based detectors with same pixel sizes[39].

As the sensor is cooled, the bandgap of the detector material widens, decreasing the number of carriers thermally excited into the valence band from conduction band, which is the main contributor of dark current. This phenomenon reduces amount of dark current exponentially. For this reason for applications where low dark current and high performance are required, InGaAs sensors need to be cooled[41].

2.3.3.3.3 Noise

InGaAs image sensors' noise can be divided into two categories; fixed pattern noise and random noise. Fixed pattern noise is mostly made up of ROIC DC offset and photodiode dark current and can be eliminated with image processing. However, random noise results from fluctuations in voltage, current or charge. After fixed pattern noise is eliminated, random noise becomes the limiting factor for an InGaAs detector. Random noise is composed of the following noise contributors;

- Dark current shot noise (N_d)
- Signal current shot noise, under illumination(N_s)
- Charge amplifier reset noise (N_r)
- ROIC readout noise(N_R)

The total noise is expressed in equation 2.7[41].

$$N(V_{rms}) = \sqrt{N_d^2 + N_s^2 + N_r^2 + N_R^2} \quad (2.7)$$

2.3.4 Microbolometers

A microbolometer is a thermal type of infrared detector whose dimensions are in micrometer range. This type of detector's electrical characteristic, usually resistance, changes as the sensor temperature changes due to heat absorption from infrared radiation. The amount of resistance change is proportional to the absorbed heat. The majority of bolometers are resistive, however diode-type microbolometers are also available. The resistance change of the sensitive resistor on the detector is measured in resistive-type microbolometers. Diode-type microbolometers, on the other hand, detect the voltage change of a forward biased diode[42].

Both surface micromachining and bulk micromachining can be used for the fabrication of a microbolometer pixel. Figure 2.24 shows a general structure of a surface micromachined pixel, and figure 2.25 shows a classic bulk micromachined pixel structure. Both types of the pixel structures have an absorber and support arms which also serve as a carrier to the interconnect layer. Moreover, they are also compatible with CMOS technology[42][44].

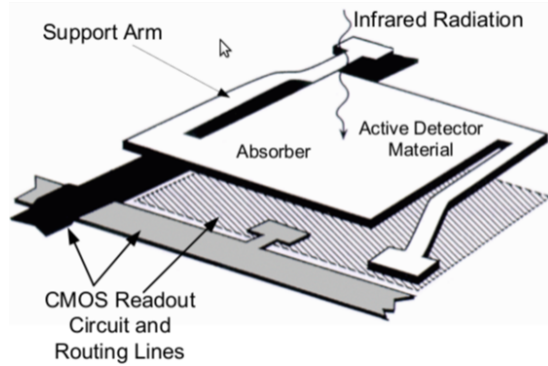


Figure 2.24: Surface micromachined microbolometer pixel structure[32]

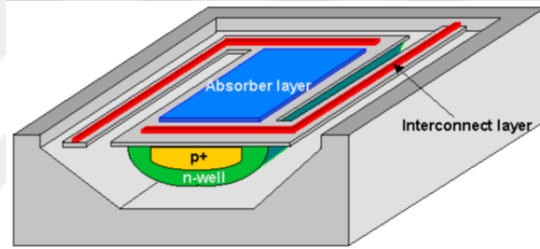


Figure 2.25: Bulk micromachined microbolometer pixel structure[43]

The absorber layer is designed and manufactured in such a way that it provides high level of infrared absorption. Increasing the absorber area helps reaching high absorption coefficient in the absorber region, in turn increasing the amount of absorbed radiation. Thanks to these improvements in the absorber, the detector gives a higher response to the same level of radiation. In addition to making an electrical connection, the interconnect layer's functions include mechanically supporting the pixel and providing effective thermal insulation of the pixel from the bulk. Thinner and longer support arms are generally desired in order to achieve better thermal isolation between the absorber and the rest of the detector. In the case of an infrared radiation that falls on a microbolometer, a measurable heat change occurs with the help of the thermal isolation. Thermal isolation is the key factor for achieving a measurable heat change since radiation should not leak into the substrate. Therefore, thermal isolation is a critical property for thermal detectors. Typically, the received power from infrared radiation of a pixel lies in the order of nanowatts. This shows the importance of thermal isolation since it

is necessary for the pixel to heat up by absorbing that small amount of power without losing any incident radiant power[42][1].

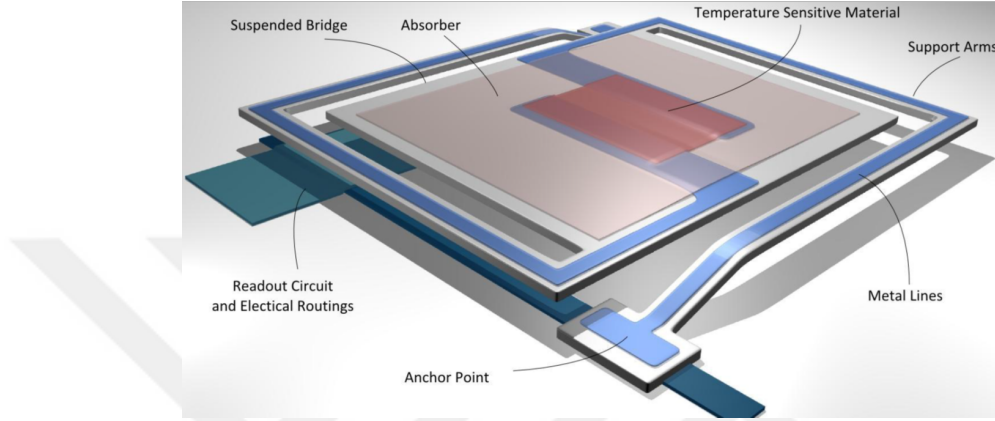


Figure 2.26: Resistive type microbolometer pixel structure[29]

2.3.4.1 Main Performance Parameters of Microbolometers

2.3.4.1.1 Responsivity

The ratio of the detector's signal change to the incident power on it, is known as responsivity. It is given in equation 2.8, where ΔV_0 is the change in the output voltage and P_i is the incident IR power on the detector[42].

$$\mathfrak{R} = \frac{\Delta V_0}{P_i} \quad (2.8)$$

Under the same intensity of incident radiation, more responsivity yields a larger change in the output signal. Higher responsivity, which can be obtained with higher absorbance and lower thermal conductance, makes it easier to read very small amount of infrared radiations[42].

2.3.4.1.2 Noise

Resistive type microbolometer structures consist of two main group of elements. First are resistances that are processed by MEMS technology and second are circuits which are fabricated using the silicon CMOS production. Both of these parts in the structure have some effect on the noise level of the microbolometers. Deviations in infrared images and temperature inaccuracies in the target are primarily caused by noise in the microbolometers. As a result, noise is a critical performance metric for microbolometers.[44].

The detectors' noise contribution to the microbolometer structure can be divided into four categories:

- Thermal (Johnson) Noise $V_{n,johnson}^2$
- Filcker(1/f) Noise $V_{n,1/f}^2$
- Temperature Fluctuation Noise $V_{n,tf}^2$
- Background Fluctuation Noise $V_{n,bf}^2$

Overall noise can be represented as shown in equation 2.9.

$$V_n(V_{rms}) = \sqrt{V_{n,johnson}^2 + V_{n,1/f}^2 + V_{n,tf}^2 + V_{n,bf}^2} \quad (2.9)$$

When compared to each other, thermal noise and flicker noise dominate the total noise[44].

2.3.4.1.3 NETD (Noise Equivalent Temperature Difference)

NETD or noise equivalent temperature difference is another widely used performance parameter. It is defined as the change in the temperature of a blackbody that causes the detector output signal to have a signal to noise ratio of one. In other words, the minimum observable temperature difference by the microbolometer is referred to NETD[45].

NETD is one of the most essential microbolometer performance metrics, as it includes practically all other microbolometer performance parameters such as noise, detector area, and responsivity. It is also effected by the optics used in the system[44].



Chapter 3

System Design

This chapter concentrates on the design of the camera electronics. Details from detector selection to analog front end design are addressed. Necessary information to realize camera electronics properly is studied and summarized before designs. The concluded designs and their performance characteristics are mentioned within this chapter.

In figure 3.1, an architectural system diagram which is required for operation of the targeted infrared imaging system is shown.

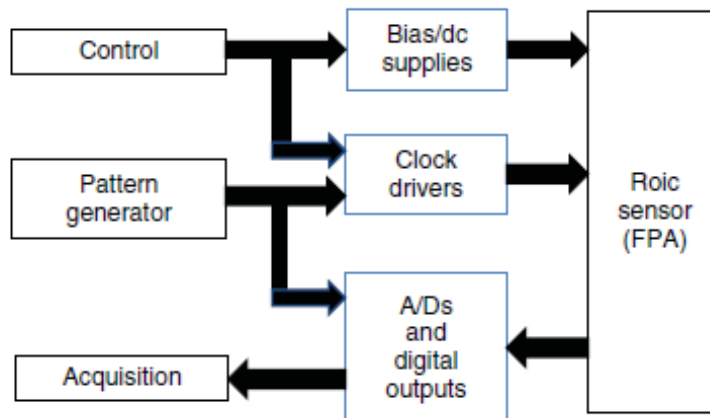


Figure 3.1: Typical imaging system architecture for an infrared imaging system [25]

In this chapter, analysis and design of required blocks for successful operation of an imaging system is reviewed step by step. Image sensor design is the starting point since it is the most critical component in the overall system. Other blocks and their internal electronics are either designed or selected to feature the state of the art performance of NANOTAM InGaAs SWIR detector.

3.1 Image Sensor Design

In this thesis, image sensor refers to the hybridized structure of infrared detector and its ROIC (Read Out Integrated Circuit). The infrared detector was designed and manufactured using InGaAs and in 1280 x 1024 format by Infrared Photonic Detectors Group, at NANOTAM. A ROIC, which is compatible with the manufactured InGaAs detector was selected after careful research and comparison.

3.1.1 InGaAs Detector

A variety of detectors such as Germanium (Ge), Indium Gallium Arsenide (InGaAs), Indium Antimonide (InSb), and Mercury Cadmium Telluride (MCT or HgCdTe) can be utilized in SWIR imaging applications. Out of these, InGaAs array detectors are seen as the most practical one for imaging technologies thanks to their high quantum efficiency throughout the corresponding band and low level of dark current even at room temperature, especially for lattice matched InGaAs/InP detector structures that operate in the 0.9 to 1.7 μm wavelength range[19].

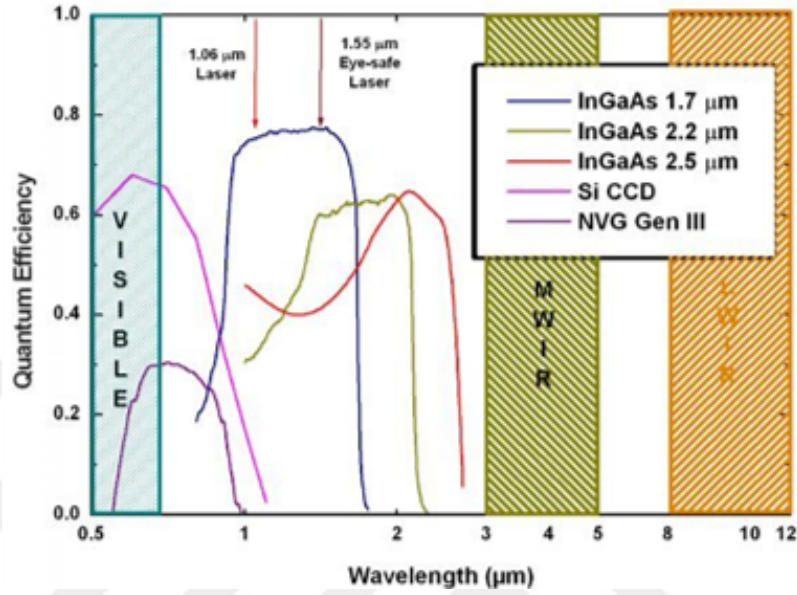


Figure 3.2: Quantum efficiency of InGaAs [18]

Figure 3.2 shows that the spectral sensitivity range of the semiconductor compound InGaAs corresponds to the SWIR band. InGaAs also gives the ability to modify quantum efficiency curve by adjusting the proportions of the compound's main components. This way, the long wavelength boundary of the sensitivity range can be adjusted as seen in figure 3.3. When the compound ratio results in a crystal structure that matches that of the substrate, the detectors have the lowest dark current and thus the best performance. This is known as lattice matched InGaAs, which has a spectral range that cuts off at 1.7 μm . Detectors which are manufactured lattice matched have low noise and high sensitivity even at room temperature. This enables to produce solid-state cameras without the need of cryogenic cooling elements. Though several thermal detectors can be employed in the SWIR, lattice matched InGaAs detectors are the smallest and have the lowest cost both in the beginning and during its lifetime[18].

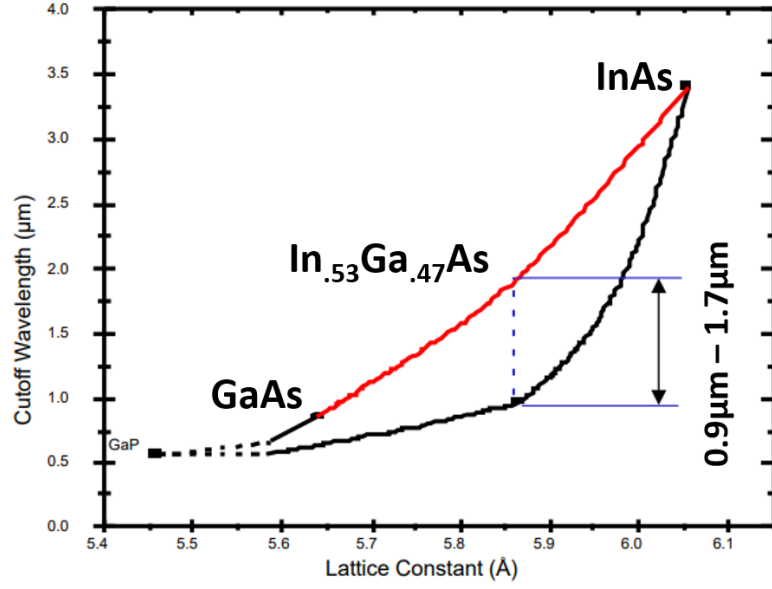


Figure 3.3: GaAs and InAs ratio and long wavelength cutoff [49]

3.1.1.1 NANOTAM InGaAs Detector

A megapixel, low dark current, diffusion limited, planar type and 1280x1024 format InGaAs photodetector was manufactured and tested at NANOTAM. The fabrication methodology and performance parameters are presented in the article given in bibliography[47]. The epilayer design and mask layout of the detector is shown in figure 3.4 and figure 3.5 respectively.

InGaAs Cap Layer
1 μm p-InP (locally doped)
2.5 μm n-InGaAs Absorber
0.3 μm n-InP

Figure 3.4: Epilayer design of the detector [47]

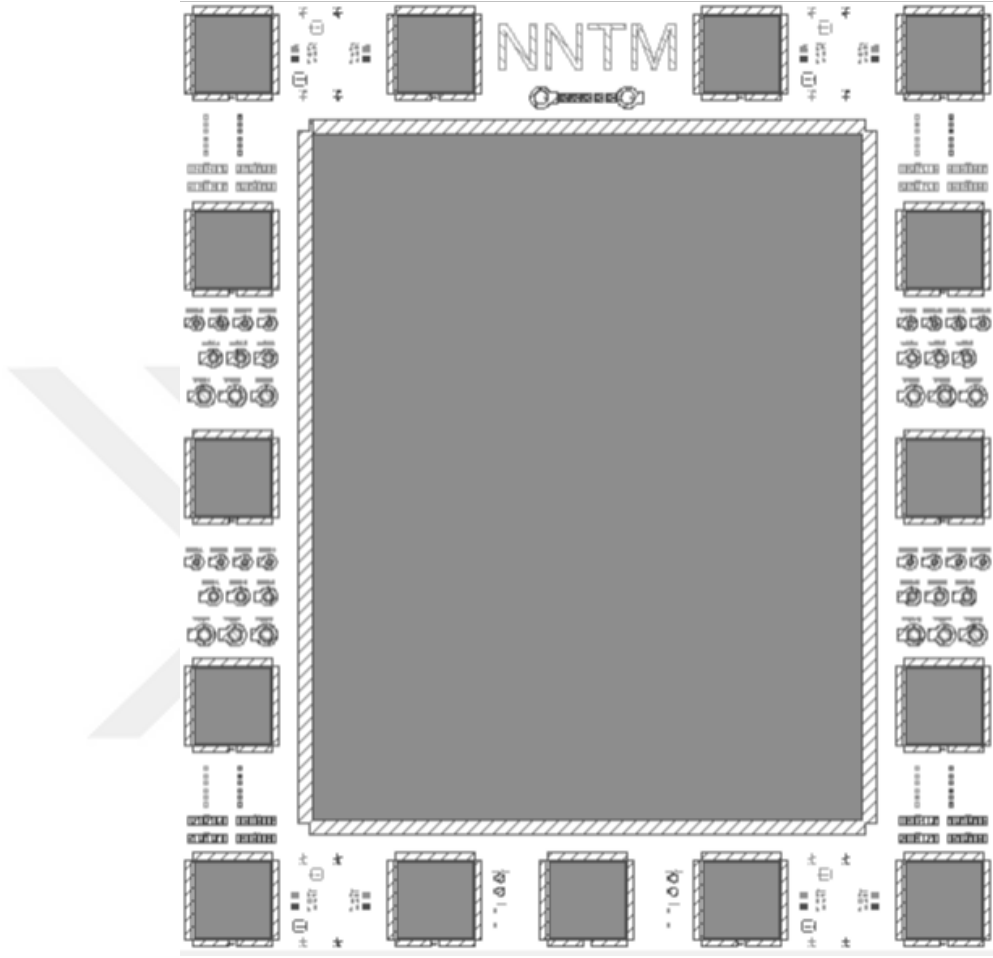


Figure 3.5: Mask layout of the detector [47]

Some of the key performance parameters which are also available in [47] are as follows;

- Dark current : 10fA
- Responsivity: 1.08 A/W
- Quantum Efficiency: % 86 at $1.55 \mu\text{m}$

In figure 3.6 the measurements which are used to calculate key performance parameters are shown.

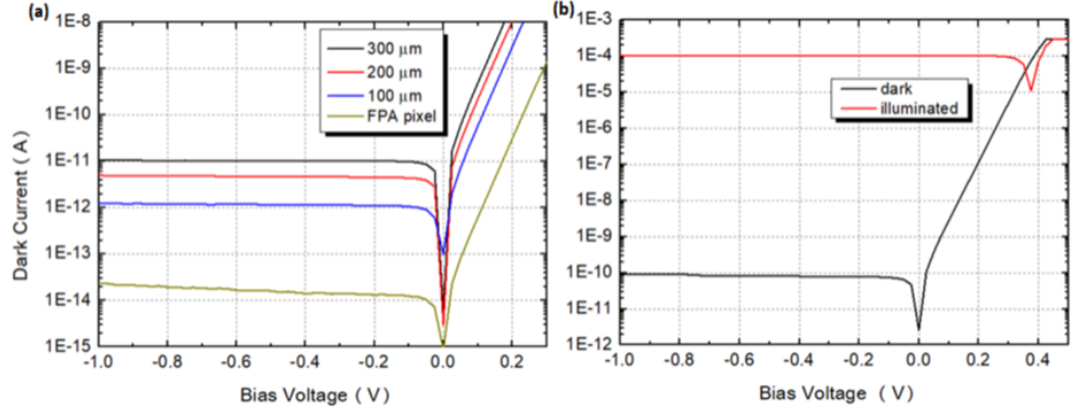


Figure 3.6: a) Dark current measurements of differently sized pixels b) Photo current measurement [47]

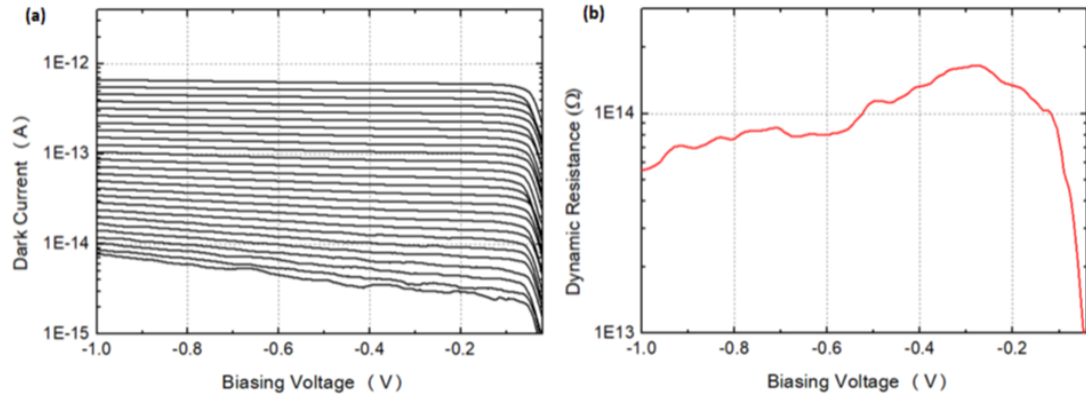


Figure 3.7: a) Temperature dependent IV characteristics of FPA pixel b) Room temperature dynamic resistance curve [47]

In figure 3.7, it is seen that, the dark current increases with temperature. In order to reach a superior performance, cooling of this sensor plays a critical role. Moreover, biasing voltage has important effect in both dark current value and dynamic resistance. This is taken into consideration to go for bias point optimization in further calibration steps.

3.1.2 ROIC for InGaAs Detector

A ROIC, in the targeted imaging system, which is compatible with the manufactured InGaAs detector is needed to convert the photocurrent generated in the InGaAs detector to analog signals and output them in a multiplexing manner to handle large number of detector pixel sensor elements to form an image. Visible imagers may combine detector and ROIC in a single chip and they are also known as CMOS image sensors.

For InGaAs sensors, detector and ROIC need to be manufactured using different fabrication techniques. Because of this, they are hybridized to form a sensor chip assembly, also known as SCA. Figure 3.8 shows an image of a sensor chip assembly with all details. The detector array is connected to the ROIC's preamplifier unit cell structure with indium bumps. The input and output pads are ready to be wire-bonded to a packaging structure or a fan-out printed circuit board.

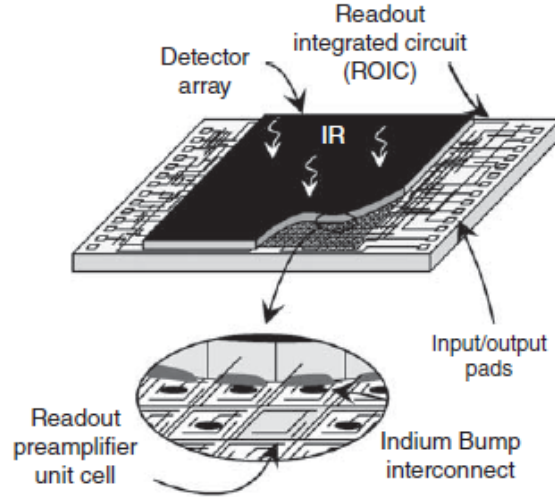


Figure 3.8: The sensor chip assembly (SCA) comprises a detector array that is hybridized to the readout integrated circuit (ROIC)[25]

Figure 3.9 shows the signal path followed by incident light. Incoming photons create a current, which then is integrated for a period of time to be converted to

voltage. The voltage values for each pixel are stored for a while and multiplexed to output in a data stream. As requirements from modern image sensors increase, some additional functions such as band limiting, gain and integration control, self-timing and biasing are also implemented by ROICs. Some ROICs even carry out analog to digital conversion on-chip and have digital output.

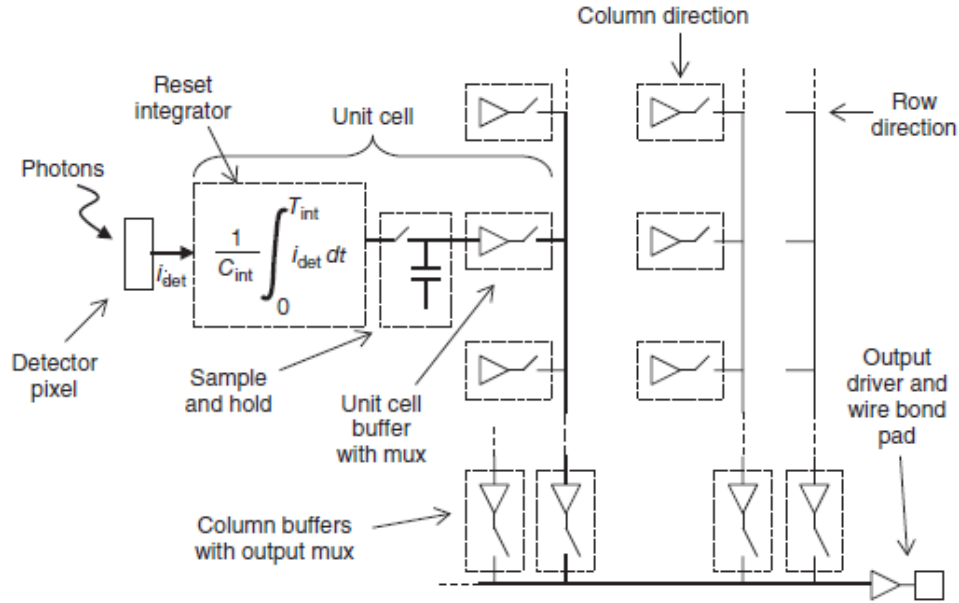


Figure 3.9: A photon's travel path from detector pixel to ROIC output[25]

3.1.2.1 Visible and Infrared ROIC Architectures

There are a few distinct ROIC architectures. Some of these architectures have a detector built into the ROIC's unit cell amplifier, while others have the detector as a separate material hybridized or coupled to the ROIC's unit cell preamplifiers[25].

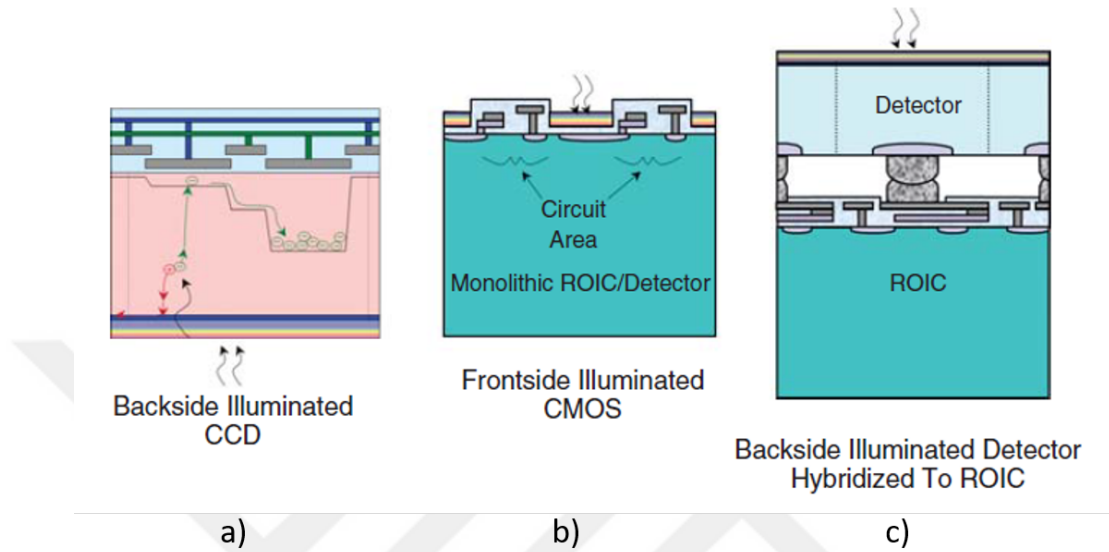


Figure 3.10: 3 different ROIC architectures: a) Backside Illuminated CCD b) Frontside Illuminated CMOS c) Backside Illuminated Detector hybridized to ROIC[25]

A visible CCD imager uses the photovoltaic nature of silicon and employs a charge to voltage converter along with a buffer. This is also known as a transimpedance amplifier placed just before the output driver. The transimpedance amplifier also gives the ability to use current from an external infrared detector material, that is hybridized to CCD through electrical connections, as a charge source. This allows a CCD to be utilized as a ROIC element for an infrared detector material.

CMOS visible imagers have the detector embedded within the ROIC as a single chip. As photovoltaic generators, p-n junctions or pinned gate devices are the most commonly used structures. The surface area is not completely allocated for photosensitive elements and there needs to be some place reserved for some circuitry to buffer and multiplex the generated signal.

There are also CMOS ROICs which are designed and dedicated to be used specifically with infrared detectors. Overall sensor is achieved by hybridization of

detector and ROIC. Since detector and ROIC element are designed and manufactured separately, they can be optimized for their special purposes and therefore offers superior performance.

3.1.2.2 Functions and Internal Elements of ROICs

ROICs do not only process and shape the image signal but also provides electrical interface to the detector, controls the required timing for controlling events, biases and references to control amplifiers, drivers and the detector. Some advanced ROICs even handle analog to digital conversion within the ROIC.

3.1.2.2.1 Signal Preamplification and Detector Biasing

Electrical interface to the detector, buffering of the signal, charge to voltage conversion and application of gain are the functions that are performed in the unit cell. So, signal preamplification and detector biasing are executed within the unit cell.

Detector's impedance is highly significant when selecting the ROIC unit cell structure. For this reason, detectors are generally classified as high-impedance and low-impedance detectors. Photovoltaic and photoconductive sensors are high-impedance detectors whereas bolometers are low-impedance detectors.

Most ROIC circuits hold the detector at a relatively constant voltage, and then charge that results from the detector's exposure to light, is accumulated. These are generally high-impedance photovoltaic detectors such as HgCdTe, InGaAs, InSb and Si. Among these, there are some detectors which are very sensitive to biasing level. For instance, for HgCdTe detector, which is used in LWIR imaging, it is very critical to hold the bias voltage constant and independent of the image input signal. But, for other detector types like InGaAs and visible detectors, having a large bias range doesn't pose a catastrophic problem.

Low-impedance detectors like bolometers operate better when they are biased

with constant current. These detectors mostly change their resistances in the case of incident light source. Constant current biasing enables detection of any change in resistance that is caused by incoming light.

3.1.2.2.2 Integration and Voltage Sampling

There are two types of image sampling that is completed inside the unit cell. First type is based on the integration of the signal for a period of time before sampling and the second type adopts the idea of sampling detector voltage or current instantaneously.

3.1.2.2.2.1 Integration

Most of the available ROICs integrate the signal from the detector for a period of time, named as integration time. Random noise tends to get filtered or averaged over this integration time. As a result, the noise bandwidth of the circuit and therefore the inherent noise of the detector decreases. A capacitor is used as the integration element. The change in the output voltage in terms of other mentioned parameters is given in equation 3.1 [25].

$$dV_{out} = q \times QE \times dE_p \times \frac{A_{det} t_{int}}{C_{int}} \quad (3.1)$$

In equation 3.1, q is the charge of the electron, QE is the quantum efficiency of the detector, E_p is the photon irradiance on the detector, A_{det} is the effective optical area of the detector, t_{int} is the integration period, and C_{int} is the capacitor on which the photon charge is integrated. The gain of the integrator can be adjusted by changing the value of the integration capacitor.

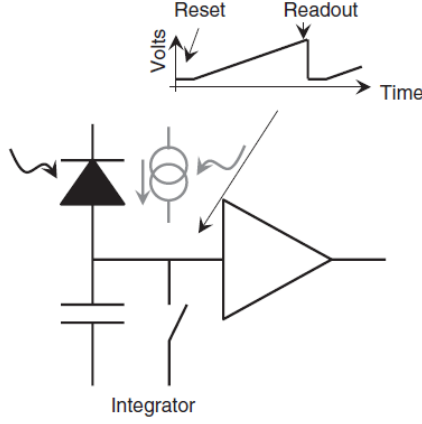


Figure 3.11: After reset, charge generated by the detector is accumulated in the capacitor and voltage across the capacitor ramps up[25]

3.1.2.2.2 Voltage Sampling

In voltage sampling method, the amplifier reads the instantaneous voltage of the detector and gives it to the following stage where it may be amplified further. With this type of amplifier, there is no circuitry for an integration and device complexity is lower. However, because there is no averaging, random noise is not reduced. This method gives a relatively noisy result and only acceptable in high-signal environments.

This method is used in bolometers and detectors that are not constantly biased. Instead, with the help of multiplexing, targeted pixel is reached, biased and resulting voltage is sampled instantaneously. The change in the output voltage in terms of other mentioned parameters is given in equation 3.2 [25].

$$dV_{out} = I_{bias} \times \left(\frac{dR}{dE} \right) \times dE \quad (3.2)$$

In equation 3.1, I_{bias} is the bias current flowing through the detector, and dR/dE is the change in the resistance for a given variation in the irradiance on the detector. The gain can be adjusted by changing the bias current. But, that may

not be desirable since different bias regions can result in decreased performance of the detector due to increased noise, image latency etc.

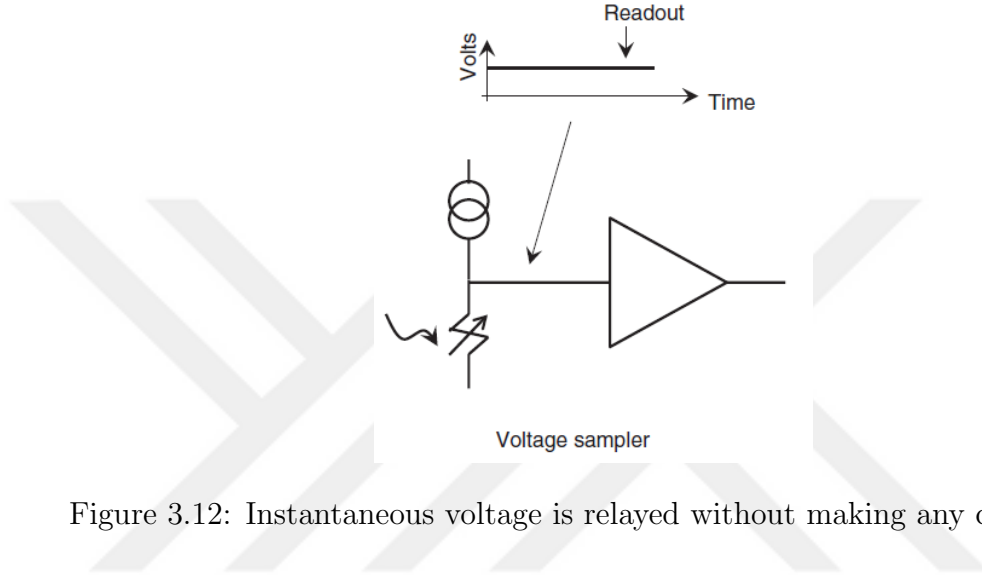


Figure 3.12: Instantaneous voltage is relayed without making any change[25]

3.1.2.2.3 Signal Multiplexing

Signals collected at the unit cell have the information about the acquired image frame, and they must be sent to the column amplifier or output buffer that is outside the image region of the ROIC. This process should be finished until the data of next frame is available.

There are two multiplexers in the ROIC, the row multiplexer (slow multiplexer) and the column multiplexer (fast multiplexer). The row multiplexer connects each row sequentially to the column buffers, whereas column multiplexer takes the output column buffers and feeds them to output buffer. The operation is shown in figure 3.13.

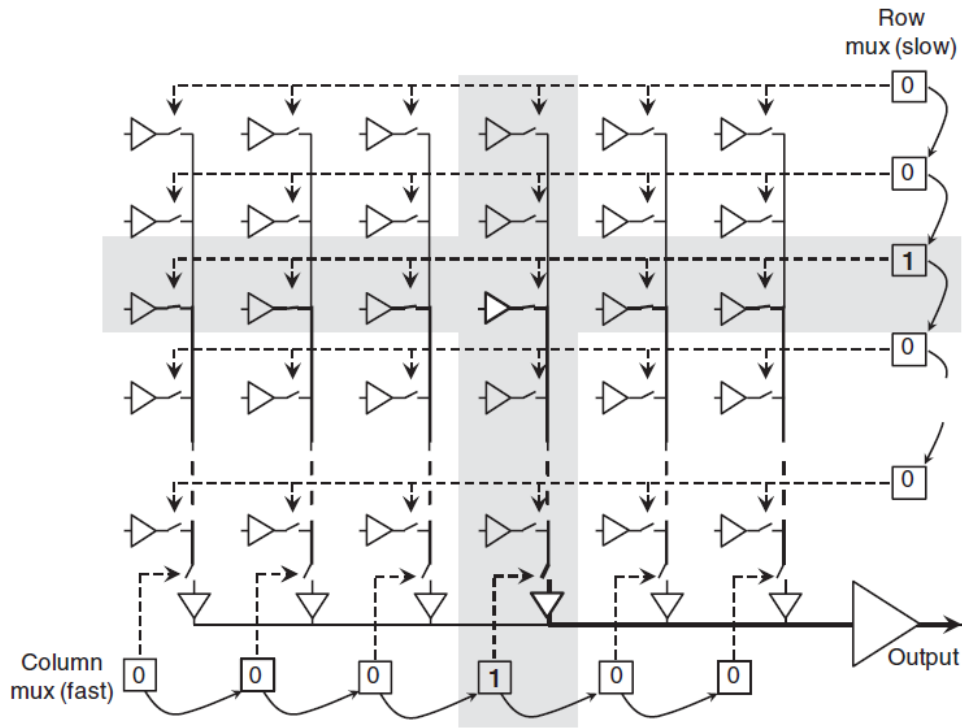


Figure 3.13: Data transmission from unit cell to output buffer by enabling row and column scanning multiplexers[25]

There are two methods of getting the signal from unit cell and transferring it to the column buffer.

3.1.2.2.3.1 Voltage Mode Transfer

Most of the ROICs use this method because their unit cells are transimpedance amplifiers. Buffering the signal from unit cell reduces the susceptibility to noise. Even though this method requires additional power in the unit cell to drive the column, low power and low noise column amplifiers can be used because the signal is already in voltage domain. This signal transfer method is generally used in medium and low flux imagers.

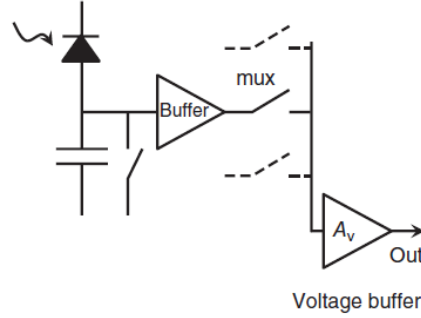


Figure 3.14: Voltage mode signal transfer[25]

3.1.2.2.3.2 Charge Mode Transfer

In this transfer method, the photon charge is stored in unit cell. This charge is transferred to output buffers directly. For this reason, there is no extra circuitry in the unit cell, allowing very low power consumption and small unit cell area. On the other hand, during transmission to output buffer crosstalk and noise may deteriorate the signal. Moreover, a very high speed charge to voltage transimpedance amplifier should be used at the output buffer which in turn increases the total power consumption. This transfer method is generally used in high flux and small pixel imagers.

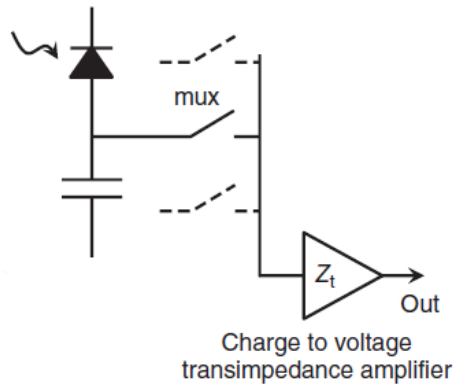


Figure 3.15: Charge mode signal transfer[25]

3.1.2.2.4 Integration Methods

Imaging systems with a staring array generally use one of the two following methods; snapshot integration or rolling integration. In snapshot integration, all pixels integrate the signal at the same time. In rolling integration method; a row is read out, reset and ready to start imaging again and then the next row is read out. This process continues until the entire array is read out.

3.1.2.2.4.1 Snapshot Integrate Then Read

This method is very important in cases where there is an important motion or temporal information to be imaged. ROICs using this method have a global electronic shutter to start and stop the integration in unit cells at the same time. The process of storing the charge from the unit cell and then reading it out is finished until the capture of the next frame. After the integration is terminated by the global shutter, detector is disconnected from the unit cell to prevent extra charge flow. This method is called *Snapshot Integrate Then Read*. In this method fewer photons can be collected since detector is disconnected from the unit cell during readout operation.

3.1.2.2.4.2 Snapshot Integrate While Read

In order to increase the amount of photon collection in the ITR method, an additional storage capacitor in the unit cell is placed. This additional storage element is also known as a frame store. This allows the system to continue collecting photons while the signals of the previous frame are being readout. This method is also called IWR.

3.1.2.2.4.3 Rolling Integrate While Read

This method is shown with an illustration in figure 3.16. The process goes as follows:

- Data from row-1 is read out to the column amplifier,
- Image in row-1 is reset,
- Integration in row-1 starts immediately after reset, to be ready for the next frame,
- The procedure is repeated until the last row.

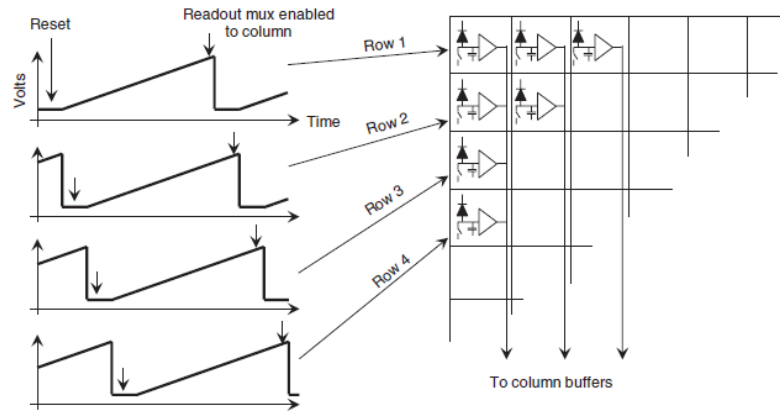


Figure 3.16: Illustration of Rolling Integrate While Read method[25]

This method requires less chip area since there is no need for a frame store to hold the signal. This method may increase the integration efficiency up to %100. But, due to the staggered integration timings of each row, any movement in the picture looks to be delayed.

3.1.2.2.5 Integrated Signal Sampling Methods

The easiest method of sampling the integrated signal is sampling the signal at the end of the integration time by assuming it's the final value. There are more complex methods used in ROICs to decrease the noise, thus achieving a higher signal to noise ratio. Some of these complex methods are correlated double sampling (CDS), fowler sampling and sample up the ramp.

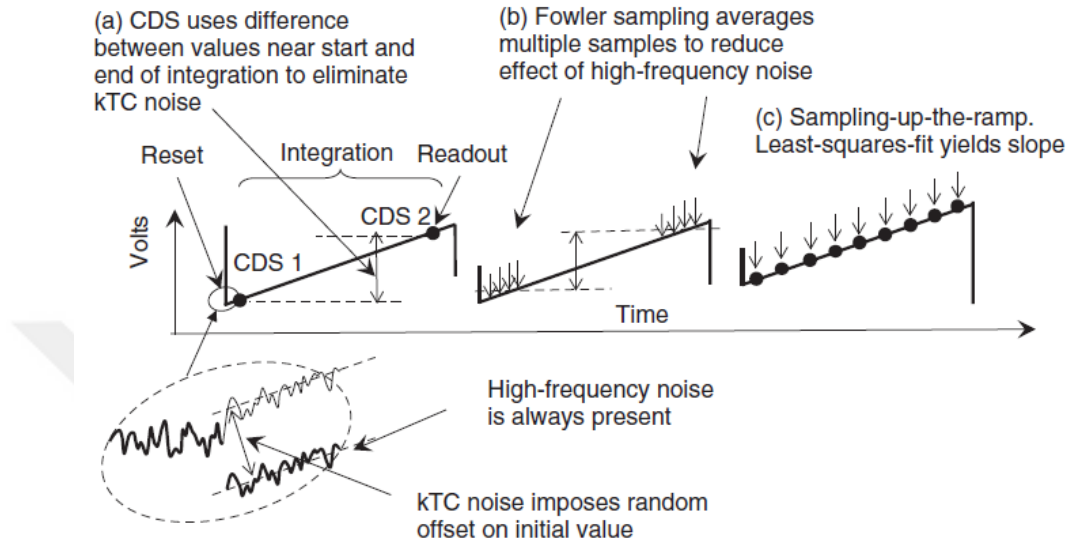


Figure 3.17: Sampling methods to reduce or eliminate noise in the output. (a) Correlated double sampling (CDS) (b) Fowler sampling (c) Sampling up the ramp[25]

3.1.2.2.5.1 Correlated Double Sampling

The active elements used in the ROICs are MOSFETs. The voltage level at any point for a signal also includes the offset introduced by MOSFETs. The properties of MOSFETs within the ROIC are not uniform and they may also face drift in time. Another offset source is due to the process of resetting capacitors along the signal path. After each reset, voltage across capacitors never become zero resulting in kTC noise. If the mentioned noise and/or non uniformity sources are the primary contributors of the overall noise, CDS is used to overcome this problem.

In figure 3.17a, an illustration of CDS is shown. In CDS, the difference between two different samples in time is used to eliminate any source of offset that is same in both samples. In imaging systems where the photocurrent is integrated over a period of time, first sample is taken right after the integration starts named as CDS1 and the second sample is taken just before the end of the integration

named as CDS2. The signal processed is the difference between CDS2 and CDS1.

3.1.2.2.5.2 Fowler Sampling

Fowler sampling is an extension of CDS. In fowler sampling, the output is sampled many times after the beginning and before the end of integration instead of using two separate sampling points like in CDS. As shown in figure 3.17b, these two different sets of samples are averaged within the groups yielding two sampling points. This method helps eliminating most of the high frequency noise. Fowler sampling is generally used in astronomy applications where integration times are longer, from many seconds to many minutes, because there is enough time to collect many samples.

3.1.2.2.5.3 Sample up the Ramp

In this method, many samples are taken with equal time intervals between them as shown in figure 3.17c. These sampled data points can then be processed (using least-squares fit is an option) to find a perfect slope value rather than relying on two data points as done in CDS. However, this is not an easy task to do on chip, and the data points need to be outputted requiring operation at very high data rates.

3.1.2.2.6 Windowing

Windowing is a method for only outputting just a targeted subset of the entire pixel array. This is achieved by special multiplexing. This allows ROICs to reach higher data rates by lowering readout time but sacrificing the resolution.

3.1.2.2.7 Analog to Digital Conversion

All modern imaging systems require the conversion of analog data to digital for easier transmission, storage and processing purposes.

Most applications carry out analog to digital conversion and send out digital signals that carry the information about the captured image. Having ADCs on chip brings many advantages. Digital signals are less susceptible to noise, the system is compact requiring few external components, overall system size and power requirements are reduced.

For ROICs, which provide on chip analog to digital conversion, there are three places that ADC blocks can be located. First place is within the unit cell. All unit cells output digitized data. This necessitates number of ADC blocks that is equal to number of pixels in the ROIC. Second place is in the column. After analog signals are multiplexed from unit cells A/D conversion takes place at the column. Third and final place is right before the output of the ROIC.

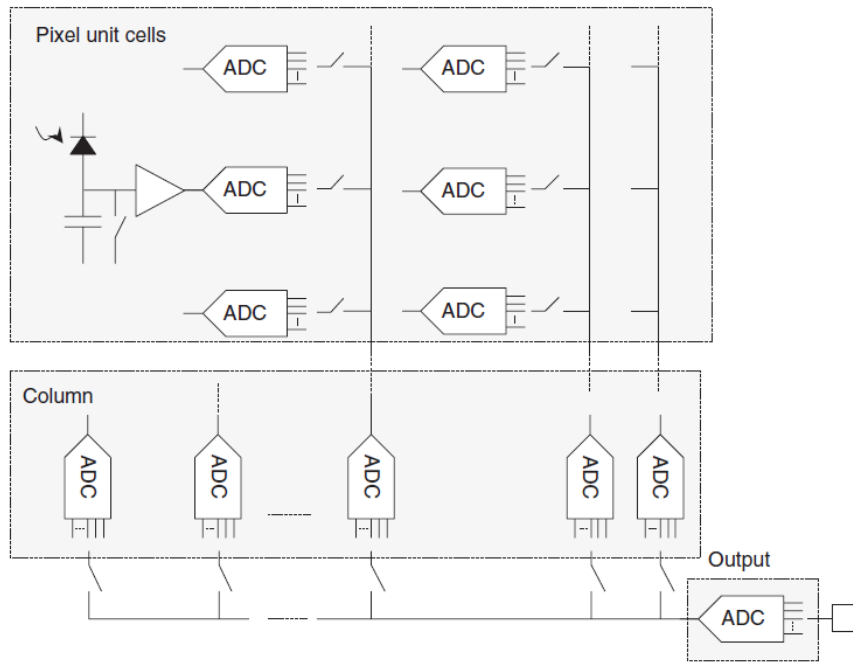


Figure 3.18: Analog-to-digital conversion is commonly done in one of three places: within the unit cell, at the column, at the output [25]

Another chance for A/D conversion is taking analog signal from ROIC and using an external ADC chip.

They all have their own advantages and disadvantages. Designers need to know all possibilities and application requirements to decide between these possible options.

3.1.2.2.8 Output Driving

There are two types of output drivers; analog and digital. Digital drivers are mostly known for their complex design nature, but they offer the ability to on-chip or near-chip digital processing. Analog drivers are used in certain areas, for example astronomy and similar applications where low-level signals, low frame rates and operating temperatures are common.

3.1.2.3 Unit Cell Preamplifier Families

For monolithic sensors, the unit cell section of a ROIC is located within the detector pixel, but for hybridized sensors, it is directly under the detector pixel in a distinct integrated circuit. The unit cell executes several functions that have been mentioned earlier. Some functions may be omitted or changed in type for different application purposes. Most important duty of a unit cell is to provide a low-noise gain or buffering of the detector signal to minimize the effect on the downstream noise sources.

A photovoltaic detector is often modeled as a current source which produces one electron-hole pair for each absorbed photon. The circuit model also has detector's self capacitance and a parallel resistance. The preamplifier families have been developed to integrate the charge coming from the detector and offer different qualities required by different applications.

3.1.2.3.1 Self-Integration Unit Cell

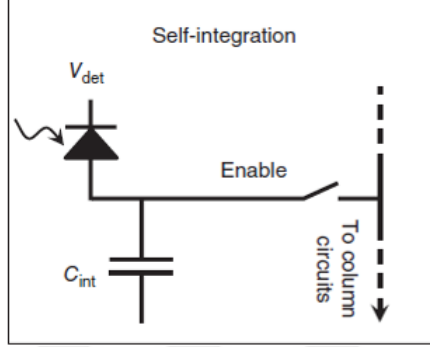


Figure 3.19: Self-Integration unit cell structure [25]

The structure of self-integration is shown in figure 3.19. It is also called as direct integration cell. It doesn't contain a buffer nor an amplifier. Charge to voltage conversion takes place in the column amplifier. The circuit doesn't need to include an extra capacitor, the detector's self-capacitance for charge storage. In some applications this capacitance is seen adequate.

As for the advantages, the circuit requires very small area and the circuit's power consumption is very low. But negatively, the circuit tends to be noisy and exhibits significant non-linearity.

3.1.2.3.2 Direct Injection Unit Cell

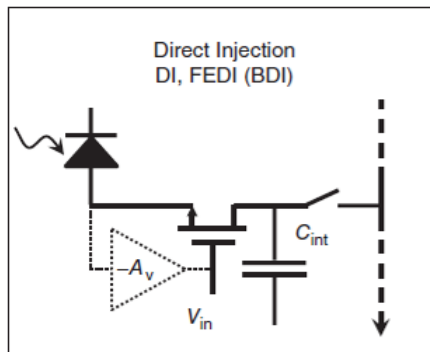


Figure 3.20: Direct Injection unit cell structure [25]

The direct injection unit cell structure, shown in figure 3.20, has three circuit components in addition to the detector. After the signal is read out to the column, integration capacitor is reset to a low voltage. The input transistor, in a common gate configuration, keeps the detector bias at one MOSFET threshold drop above the bias V_{in} . V_{in} is set to a value so that the detector is reverse biased. This circuit provides a stable bias to the detector while accumulating the charge from detector to integration capacitor.

3.1.2.3.3 Source Follower Per Detector

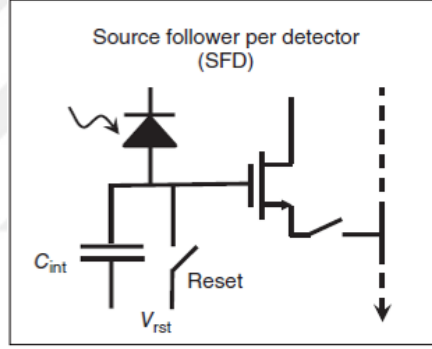


Figure 3.21: Source follower per detector unit cell structure [25]

The circuit of the source follower per detector unit cell structure is shown in figure 3.21. It has a voltage buffer which introduces almost unity gain and drives the pixel signal to the column circuitry. This configuration provides active current source load for the amplifier in the unit cell. This results in an operation where only the unit cell that is enabled actually draws current. With this type of operation, no power is dissipated during integration time lowering the overall power consumption.

3.1.2.3.4 Capacitive Transimpedance Amplifier

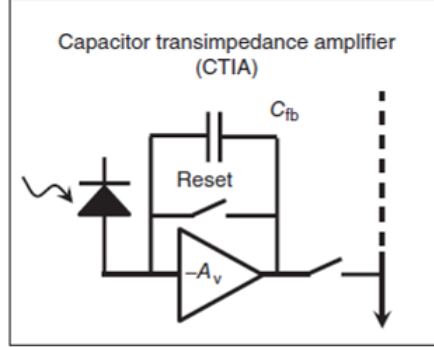


Figure 3.22: Capacitive transimpedance amplifier unit cell structure [25]

CTIA type unit cell configuration is shown in figure 3.22. By using the integration capacitor as a feedback element around a high gain amplifier, it achieves exceptional control over the detector node bias while offering a highly linear, low noise dynamic range. The charge generated by the detector is stored in the feedback capacitor as shown in figure 3.23. The output voltage of the amplifier is kept constant until it is read out.

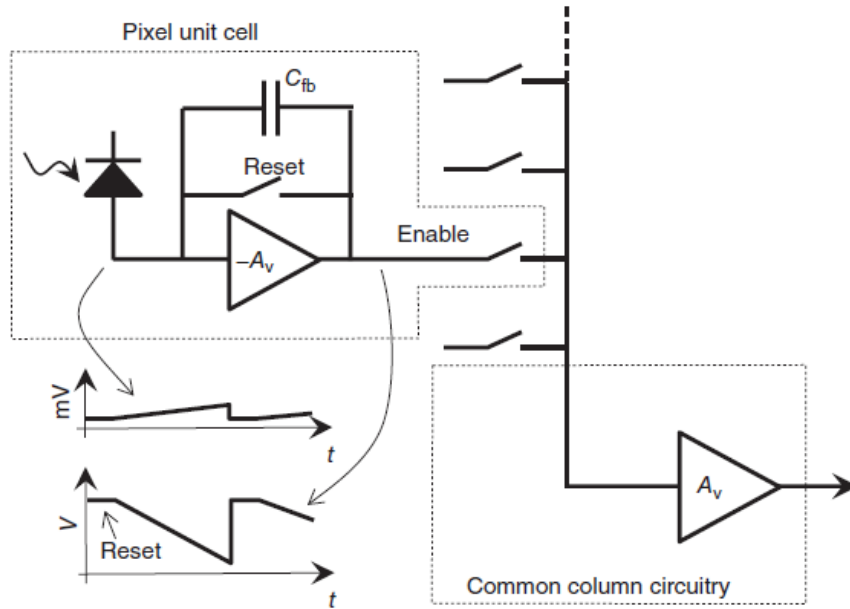


Figure 3.23: Capacitive transimpedance amplifier operation [25]

The gain of CTIA can be adjusted by using different valued integration capacitors. Since capacitors in the ROIC can be designed to present excellent linearity over voltage, the overall linearity of CTIA can be really good. The CTIA type unit cell circuit can also keep detector bias at a fixed value throughout the linear dynamic range, once it's set.

The CTIA provides wide dynamic range, high linearity and low noise. But required circuit area is large and power requirement is high.

3.1.2.4 ROIC Noise

ROIC noise can be predicted from circuit models and generally MOSFET 1/f noise or capacitor reset noise (also known as the “kTC” noise) dominates.

kTC noise refers to the thermal noise associated with capacitors. Normally capacitor is a noise-free circuit element, but the action of resetting of a capacitor introduces a noise and this noise is named as the “kTC” noise. The main reason of this noise is the uncertainty or random variation on the capacitor voltage each time the capacitor is reset.

kTC noise is the main noise source for a ROIC. The expression for the variance of the voltage is given in equation 3.3.

$$v_n^2 = \frac{kT}{C} \quad (3.3)$$

This noise is also expressed in terms of the electrical charge variance in equation 3.4 and the equivalent variance of the number of the carriers on the capacitor in equation 3.5.

$$q_n^2 = kTC = (v_n C) \quad (3.4)$$

$$N_n^2 = \left(\frac{q_n}{e^-} \right)^2 \quad (3.5a)$$

$$N_n = \frac{\sqrt{kTC}}{e^-} \quad (3.5b)$$

kTC noise can be eliminated with sampling methods such as CDS, fowler sampling and SUP. ROIC noise is generally reported as the equivalent number of “rms noise electrons” by ROIC manufacturers and designers. This can be converted to voltage noise using the Full Well Capacity and output voltage range.

3.1.3 ROIC in NANOTAM SWIR Sensor: MT12815CA-3G

Most parameters and characteristics to be knowledgeable about ROICs are covered under 3.1.2. After careful investigation and research of commercially available ROICs, “MT12815CA-3G” is selected to be used in the targeted imaging system. It is stated by the designer company that MT12815CA-3G is suitable for megapixel InGaAs detectors in low light imaging applications. Moreover, MT12815CA-3G has a system-on-chip architecture which generates all the timing and biasing signals on-chip, reducing the need of external electronics to a great extent. The required configurations for biases and timings are carried out with the help of a 3-wire serial communication, which eases the use of the ROIC.

This ROIC has a format of 1280 x 1024 and pixel pitch of $15\mu\text{m}$. The ROIC is suitable for both p-on-n and n-on p detector arrays and provides on chip detector bias that can be programmed in 0.7mV steps. Integration time and full well capacity of the CTIA type pixel input circuitry is also programmable, making the gain adjustable, with three different options. At different gain modes, the full well capacity values and readout noise values in those modes are given in table 3.1.

Mode	Full Well Capacity	Readout Noise
Very High Gain: VHG	10000 e-	< 5 e-
High Gain: HG	20000 e-	< 9 e-
Low Gain: LG	350000 e-	< 110 e-

Table 3.1: Full well capacity and readout noise values in different gain modes[26]

MT12815CA-3G performs snapshot operation using Integrate Then Read (ITR) and Integrate While Read (IWR) modes. MT12815CA-3G gives signals with analog outputs. Output swing is $\leq 2V$ and programmable to be given offset. Number of analog outputs can be programmed in 8, 4 and 2 channel output modes. There are also two reference outputs for pseudo-differential operation. The ROIC also outputs a reference clock, allowing users to take it as a reference for sampling analog signals and hence achieving proper settling at the analog outputs. The pixel data rate for one channel is 10 MHz and can be raised up to 12.5 MHz.

Scanning direction of the pixels can be adjusted in horizontal and vertical directions. The on-chip processing capabilities enables windowing, which implements imaging of only a portion of the full view at maximum possible resolution, with programmable location and size. Another feature of this ROIC is that it can support sub-sampling, which assumes 4 adjoining unit cells as a joined unit cell with equivalent pitch of $30 \mu m$ and image size of 640×512 . Here, full view is kept at the expense of reduced resolution. Finally, the ROIC has an on-chip temperature sensor with $1mV/K$ sensitivity.

3.1.3.1 MT12815CA-3G ROIC Architecture

Figure 3.24 shows the architecture of the signal chain in MT12815CA-3G ROIC. The CTIA type pixel input circuitry is the interface point to the detector and performs the current to voltage conversion within the pixel. Since the ROIC operates in snapshot mode, either ITR or IWR, all the pixels are integrated and

reset in parallel at the same instant.

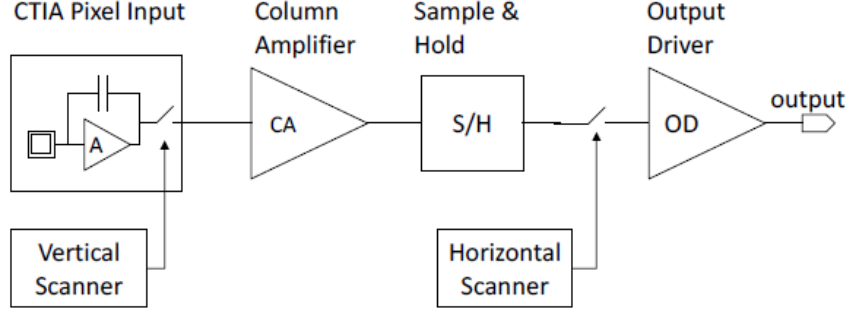


Figure 3.24: Simplified architecture of the signal chain in MT12815CA-3G ROIC[25]

After the integration, all of the pixel circuits hold charges in their integration capacitors. After that, the readout process takes place in a sequential manner, reaching each pixel. During the readout process, at first, vertical scanner connects the CTIA pixel input to column amplifier and sample and hold circuit. At this time, all pixels in a column are amplified by the column amplifier and fed into sample and hold circuit. Following, each pixel is multiplexed to output driver one after another at each clock cycle. When reading of one column is finished next column is readout in the same way. This process continues until the whole image is read out and repeats itself for every frame.

MT12815CA-3G ROIC holds an on-chip bias generator to be used for detector biasing. This bias generator is programmable and gives user the freedom to adjust the biasing level of the detector. Sometimes users may want to adjust biasing level to different values to find an optimum biasing point in terms of noise and image quality. On-chip programmable biasing eases this approach.

MT12815CA-3G ROIC also houses a digital control circuit that is capable of generating timing signals and responsible for controlling other functions. The digital control circuitry can control all required signaling for multiplexing operations along with timing in the pixel array and column readout. Also there is a 3-wire SPI communication module that establishes the connection with external

electronics for configuration. The digital control circuit works in such a way that when there is a configuration update, it is activated only between frames. This way, any frame synchronization problems that might occur are avoided[25].

3.1.4 Hybridization of Detector and ROIC

The infrared detector (InGaAs) and its readout circuit (ROIC) are manufactured separately using different fabrication techniques and technologies. In order to form the image sensor, the detector and the ROIC need to be hybridized. The process of hybridization is called flip chip bonding (FCB).

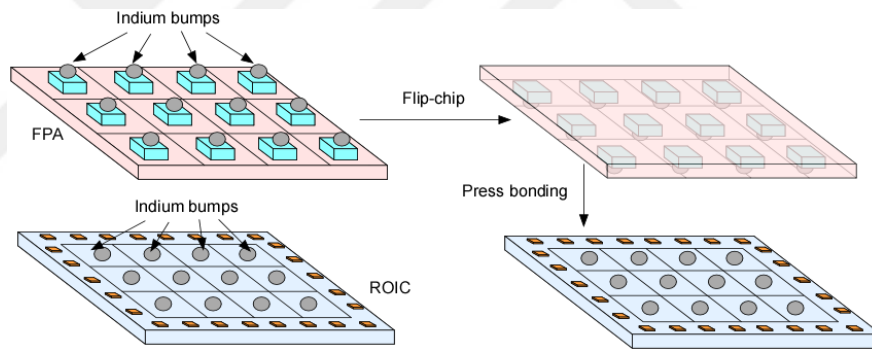


Figure 3.25: Illustration of flip chip bonding process [55]

The InGaAs sensors and silicon CMOS ROIC are fabricated separately. Then, indium solder bumps are deposited in each pixel of both arrays. The hybridization is completed after both arrays are combined with flip-chip bonding .

Before bonding, the FPA and ROIC chips to each other, reflow process is applied as shown in figure 3.26 which shows the SEM images of indium bumps on test samples before and after the reflow process.

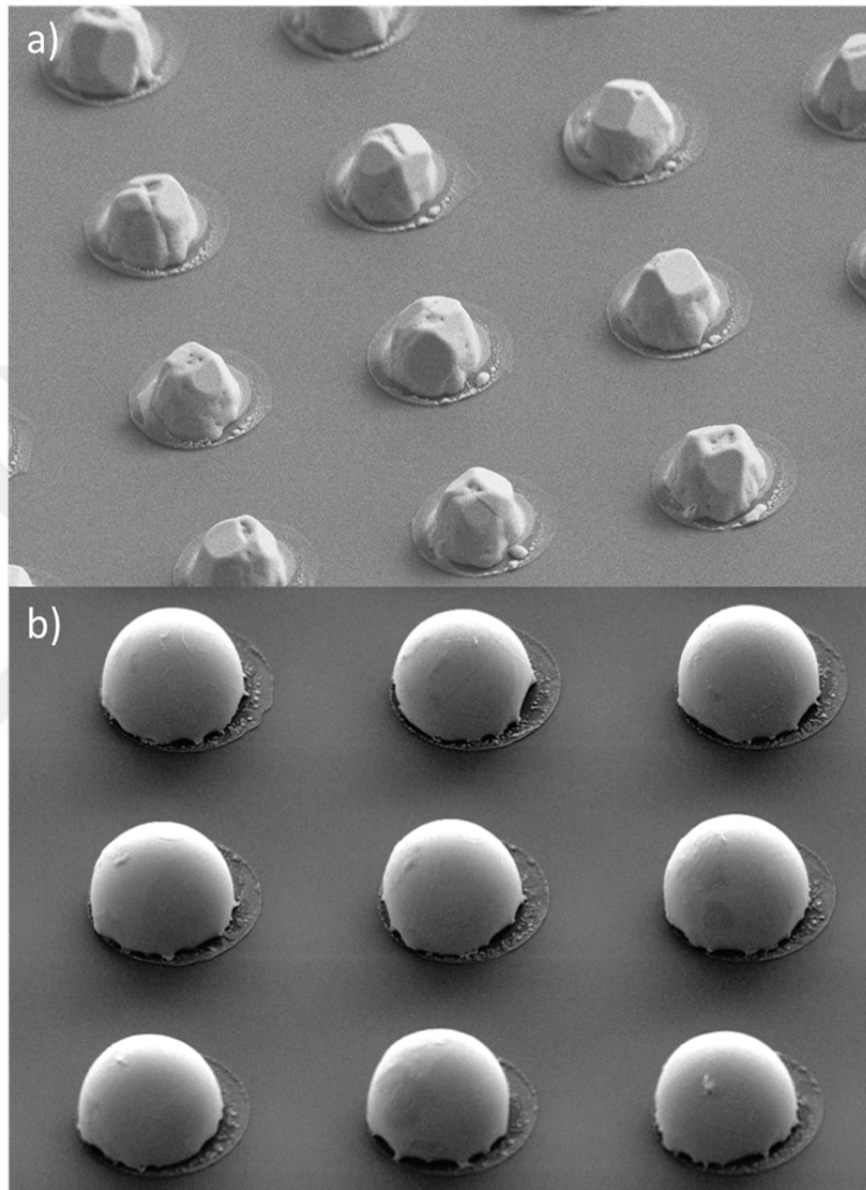


Figure 3.26: Indium bumps on test samples a) before and b) after the reflow process[56]

FPA and ROIC chips are loaded to the FCB system as the surfaces with indium bumps facing each other after the calibration of the FCB system. FPA and ROIC chips are aligned to each other with the help of a special microscope system that is able to monitor surfaces of both chips together. In parallelism alignment stage, surfaces of both FPA and ROIC chips are paralleled to each other with auto

collimation which is simply, matching the images of the alignment marks that are optically reflected from both chips' surfaces. After finishing the alignment step, chip bonding procedure is applied with optimized bonding cycle. The result of FCB process is shown in figure 3.27 [56].

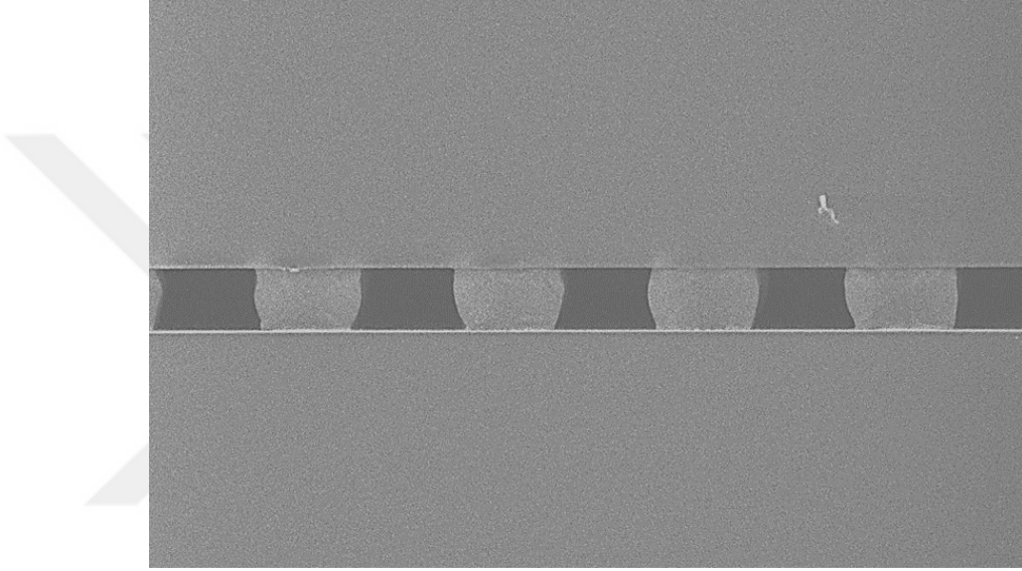


Figure 3.27: Fused indium bumps after FCB process [56]

The image sensor is complete with the hybridization of ROIC and FPA (detector). After this point, external electronics for proper operation of the image sensor are needed.

3.2 Analog Front End Design

The output of analog output ROICs rarely matches the system level ADCs' input range. The electronics to run a ROIC with analog outputs needs to provide DC offset and gain, an analog front end circuit in other words, to match the ADC's input requirements. ROIC analog outputs also need buffering because ROIC outputs generally are not designed to drive very large loads[25].

3.2.1 Design Considerations of Analog Front End

For proper operation of overall imaging system, there are a few important design considerations in Analog Front End design to place emphasis on.

3.2.1.1 Noise

Noise is any unwanted signal that distorts the signal in the system. Especially in imaging systems, noise becomes more distinguishable with the visual discomfort it creates. Figure 3.28 shows the same image with noisy and noiseless options and marks the importance of having a noise-free system.

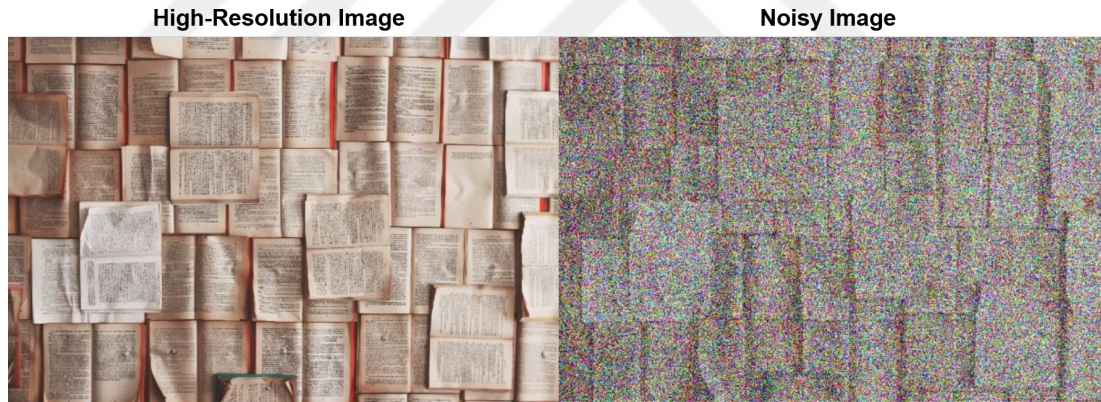


Figure 3.28: The same image with and without noise[66]

Noise is a central topic in analog circuit design because it directly affects how much information can be extracted from a measurement. In order to achieve best performance from a signal conditioning circuitry, the main goal is to attain the lowest possible noise floor. To achieve this goal, one must understand that every sensor has its own noise, characteristics, and requirements. So, selecting the lowest noise component that is available is not always the solution to signal conditioning noise issues. For this reason, it's very critical to understand component level noise sources' characteristics and account for them in an analog signal conditioning circuitry to obtain best performance while avoiding costly overdesign and inefficient use of resources [50][52].

There are mainly two distinct categories of noise that degrade circuit performance, extrinsic and intrinsic noise.

Electrical and magnetic noise are forms of extrinsic noise. Extrinsic noise can appear as spikes, steps, sine waves or random noise. They are not inherent to the circuit and they are disturbances coming from surrounding environment. Interference can come from anywhere; machinery, nearby power lines, RF transmitters or receivers etc. Designers can reduce the effects of extrinsic noise in a number of ways, such as shielding, filtering, applying good design/layout techniques etc.[50][51].

Intrinsic noise is a random process that occurs as a result of quantum fluctuations in all resistors and semiconductor devices (PN junctions) that produce voltages and currents in any application. It is not possible to get rid of noise completely, instead the degradation it causes can be minimized by applying core knowledge about noise and employing correct design techniques[50]. Types of intrinsic noise is described in detail in 3.2.1.1.1.

Noise is mostly specified as peak-to-peak (p-p), rms (root mean squared) or spectral density ($\text{nV}/\sqrt{\text{Hz}}$). It is graphically shown as peak-to-peak voltage in time as shown in figure 3.29b, or as $\text{nV}/\sqrt{\text{Hz}}$ in a specified spectral band as shown in figure 3.29a. When it comes to rms noise, it is the rms value over a given bandwidth. There is a conversion method between p-p noise and rms noise values. Noise is random and there is always possibility that the noise voltage could exceed the peak-to-peak value. Multiplying rms noise by 6.6 gives a peak to peak value, with a % 99.97 confidence, that will not be exceeded[50].

In ac signals, power is concentrated at a fixed frequency. Whereas in noise, power is spread out over a specified frequency spectrum. Noise values may not be known exactly, but they can be predicted in terms of probability. Most noise, those with spectral content to the infinity, has a Gaussian distribution.

Peak-to-peak noise graphs are not very handy since it's difficult to read values accurately and consistently. On the other hand, noise spectral density vs.

frequency plots are more helpful for analysis. It provides a visual indication of how noise power is distributed over frequency as shown in figure 3.29a. For hand calculation and comparison purposes, using rms noise values is a better approach. The reason is that, noise spectral density is dependent on frequency, and in an analog signal chain, bandwidth of each component may be different from each other. This may cause miscalculations and wrong results leading to incorrect decisions. In this thesis, rms noise values are used in signal chain analysis. If noise of signal chain components are represented in different forms in their datasheets, necessary conversions to rms are carried out.

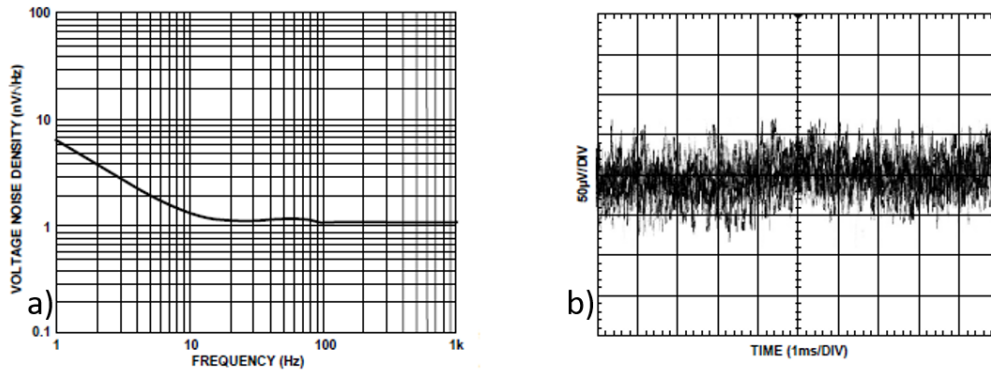


Figure 3.29: Representation of a) noise spectral density b) peak-to-peak noise voltage[50]

3.2.1.1.1 Noise Types

3.2.1.1.1.1 White Noise

White noise, also known as broadband noise, is the flat part of the spectral noise density graphs. In figure 3.30, the dashed lines show the white noise. White noise is defined over a frequency where noise is spread evenly in the frequency domain. Generally, in electronic circuits, white noise is dominant at frequencies that are greater than a few kHz. Because of this, it is the noise floor of the systems and limiting factor for the system resolution in most of the electronic circuits.

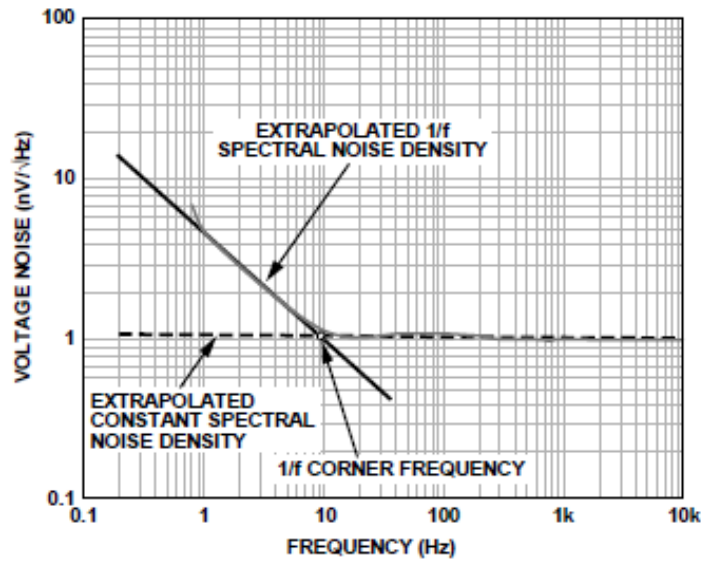


Figure 3.30: Spectral Noise Density; at lower frequencies flicker noise dominates whereas at higher frequencies white noise dominates [51]

Figure 3.31a shows the time domain measurement of a white noise. It is a composition of signals with different amplitudes and frequencies. In figure 3.31b, statistical distribution of white noise is shown. The distribution is Gaussian with a mean value of 0V. This distribution property is utilized in noise measurements and calculations and helps greatly in noise optimization of analog circuits.

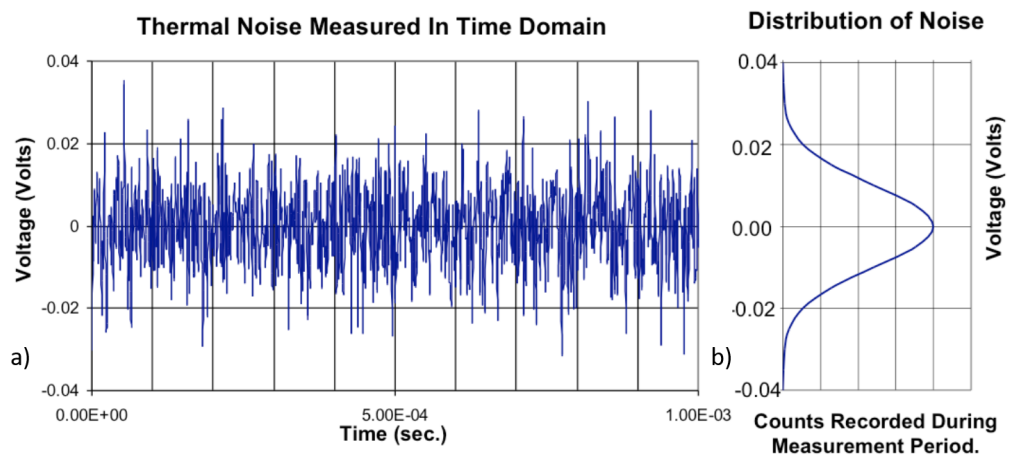


Figure 3.31: White noise a) in time domain b) statistical distribution [62]

3.2.1.1.1.2 Shot Noise

Shot noise generally occurs when a current passes through a PN junction. This barrier crossing happens totally randomly, the resulting dc current is the sum of many random elementary current pulses. Shot noise is constant over all frequencies. It is a current noise which has a uniform power spectral density, and becomes part of the white noise.

3.2.1.1.1.3 Flicker(1/f) Noise

As seen in figure 3.30, noise goes up inversely proportional to frequency. This is due to the flicker noise, or with another naming, 1/f noise. The main reason for flicker noise is the random capture and release of charges in semiconductors. In electronic circuits, flicker noise is dominant at frequencies up to a few kHz. For this reason, it is not the main limiting factor for applications which have bandwidth of a few MHz. However, it is better to select a component with a lower corner frequency, which is the frequency white noise starts to be dominant.

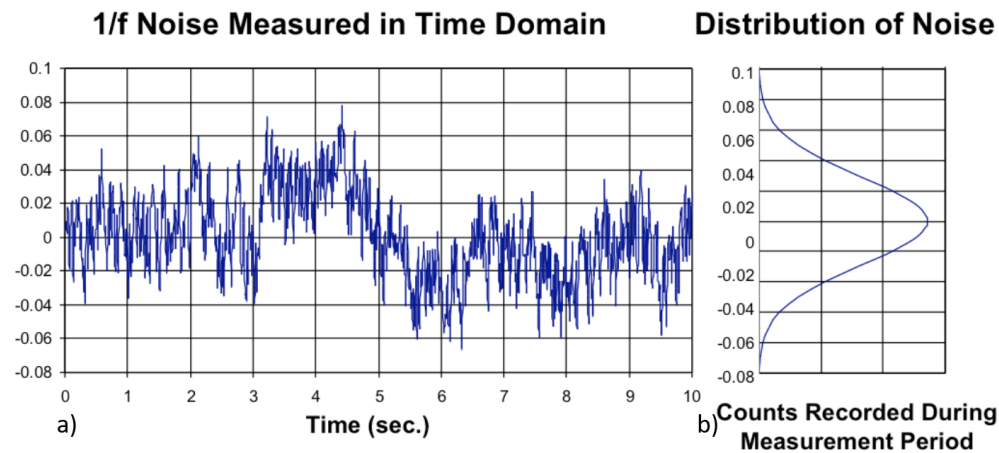


Figure 3.32: Flicker Noise a) in time domain b) statistical distribution [62]

3.2.1.1.1.4 Resistor Thermal Noise

A noise is generated by the random motion of the charges within the resistor.

Total rms noise produced by a resistor is given in equation 3.6, where T is the temperature in Kelvin, R is the resistance in Ω , Δf is the frequency band and k is the Stefan Boltzmann constant. Another approach of expressing resistor noise is noise spectral density given in equation 3.7 with a unit of $\text{nV}/\sqrt{\text{Hz}}$.

$$e_n = \sqrt{4kTR\Delta f} \quad (3.6)$$

$$e_{\text{density}} = \sqrt{4kTR} \quad (3.7)$$

Resistor noise is constant at all frequencies and adds up on to white noise. Since resistors are widely used in electronic circuits, the noise generated by them must be taken into consideration in the overall noise analysis.

3.2.1.2 Linearity and Distortion

The designed circuit should perform a linear operation within the range of image sensor output. Each stage and its components need to be selected and analyzed carefully, making sure that none of them operates in a nonlinear region.

Operation in nonlinear region results in distortion of signals. Distortion may lead to degradation of the quality of the sensor information, which is an image data in this thesis, or miss of a range of signal range which carries valuable sensor data.

3.2.1.3 Bandwidth

Bandwidth is a property of certain types of electronic circuits that determines the frequency range that can be passed from input to output[57].

When designing the analog front end, bandwidth is an important point to pay

attention to. The designed circuit should be able to operate as desired, without any unwanted distortion, phase change, and with the appropriate amplification within the required bandwidth of interest. Analysis of circuits' bandwidths is carried out and results are shown for the proper operation in the desired bandwidth.

3.2.1.4 Stability

Analog Front End circuitry is comprised of operational amplifiers and fully differential amplifiers which are closed loop systems with feedback. Systems with feedback need to be designed and characterized carefully because they are potentially unstable and they may oscillate.

$$\frac{Y}{X}(s) = \frac{H(s)}{1 + \beta H(s)} \quad (3.8)$$

The closed loop transfer function of the system in figure 3.33 is given in equation 3.8. If $\beta H(s) = -1$ the closed loop gain becomes infinite. The circuit can amplify its own noise until eventually it begins to oscillate. $\beta H(s)$ is -1 when β is 1 and 180° of phase shift between the input and the output is present. To ensure stability of a closed loop negative feedback system, maximum phase shift value to be introduced is 180° when the gain is equal to unity.

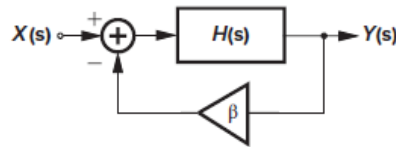


Figure 3.33: Basic negative feedback system [53]

After considering other important issues such as noise, stability is a point that should not be skipped in the design of the analog front end. In the case

of instability, techniques of compensation can be employed to make the circuit stable.

3.2.2 Analog Front End Components

The analog front end for each channel of ROIC's output consists of three main components; an operational amplifier (op amp) to drive analog output and reference output, a fully differential amplifier for pseudo differential to fully differential signal conversion and ADC driving, and an ADC for digitizing the analog signals. There are maximum of 8 channels that can be used with the selected ROIC. The analog front end should be repeated for each channel.

3.2.2.1 Operational Amplifier

Operational amplifiers (op amps) are generally considered as the essential building block of various analog and mixed-signal systems. Until a few decades ago, engineers were trying hard to design op amps to serve as general purpose circuit elements. With this point of view, the focus was on designing op amps that could be used in many different applications. For this reason, all of the efforts were concentrated on coming up with a design that approximates the ideal op amp parameters as much as possible. Conversely, in today's world, designers work with the recognition that there are trade-offs between op amp parameters and trying to make each single parameter better makes no sense. Hence, knowing the adequate value that needs to be achieved for each parameter and designing specifically for a targeted application is a way better approach[53]. For this reason, key parameters of the op amps are studied with an aim to choose the best option for achieving high performance in the targeted imaging system.

The ROIC's analog output has limited drive capability[14]. For this reason, it is not possible for the ROIC's output to establish a healthy connection with the external electronics. In order to overcome this issue, buffering of the outputs is inevitable. As buffer elements, unity gain configured op amps need to be used.

The op amp to be used in this configuration should be selected accordingly. Following op amp parameters are reviewed on the basis of the unity gain op amp configuration and ROIC's output properties.

3.2.2.1.1 Input and Output Voltage Range

There is a voltage range for the inputs of the op amp in which the input stage functions properly with all transistors are in the active region. This is either called input voltage range or specified in component datasheets as the input common mode range. Here, common mode voltage is calculated as $\frac{v_p + v_n}{2}$.

Similar to the input common mode range, there is a maximum and minimum output voltage value that an op amp can have. Between these values, output stage of the op amp functions properly. That is named as output voltage swing in component datasheets[61].

Since the op amps will be used as voltage buffers, they will be configured as unity gain amplifiers. In the case of unity gain configuration, input voltage supplied by the ROIC output is equal to the input common mode voltage which will also be equal to the output voltage. While selecting the operational amplifier this should be kept in mind that, the sensor output extreme points should stay well within the range of input common mode voltage and the output voltage swing.

3.2.2.1.2 Input Offset Voltage and Offset Current

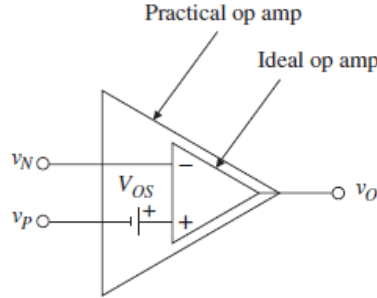


Figure 3.34: Op amp with input offset voltage [61]

Ideally, shorting the inputs of an op amp give $v_o = 0V$ at the output. However, this is not the case for real world applications. Because of the inherent mismatches between the inputs of the op amp, a practical op amp gives $v_o \neq 0V$. There is a need to apply some correction voltage that forces $v_o = 0V$. The correction voltage value is called the offset voltage. In our imaging system, offset voltage can easily be corrected digitally with the help of offset-correction technique.

However, some operational amplifiers have such an input topology that have different offset values for different input voltages. Such topologies give the designer ability to use the full input range from positive supply rail to negative supply rail. Those op amps are called rail-to-rail op amps. In our imaging system, having different offset values for different input voltages causes a problem in the offset correction process. While selecting the buffer op-amp, it should be made sure that the offset voltage value stays constant for all possible input values.

In ideal op amps, no current flows through the input pins. But, in real life some amount of current flows due to the internal structure of the input stage and ESD protection elements placed at the inputs. That flowing current for each input is called input bias current, the mismatch between input bias currents is called input offset current. Input offset and input bias currents lead to unwanted effects on the output signal. For this reason, selecting an op amp with the lowest input bias and offset current values enhance the performance of the targeted imaging

system.

3.2.2.1.3 Open Loop Gain and Bandwidth

Open loop gain or A_{ol} can be defined as the gain applied to the voltage difference between the input terminals when there is no feedback. In an ideal op amp, A_{ol} is infinite. Modern real-world op amps have open loop gains around 120dB. Open loop gain of an op amp has a low-frequency dominant pole like an RC filter as shown in figure 3.35.

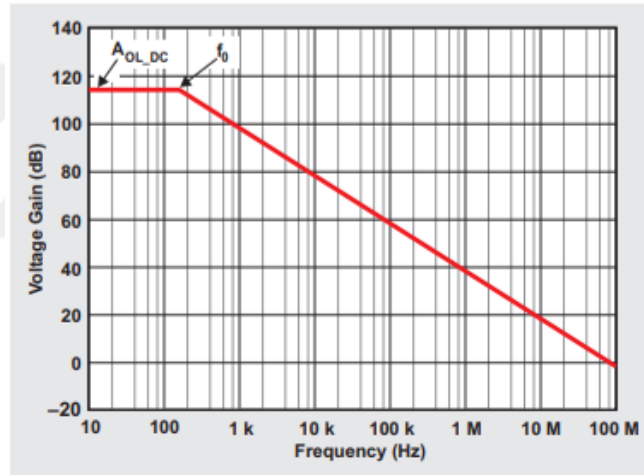


Figure 3.35: Op amp open loop curve[84]

Op amps without a feedback or in open loop configuration have limited use. The loop should be closed with a feedback which creates a closed loop gain A_{cl} . A_{ol} and A_{cl} can both be plotted on the same curve to detect the bandwidth of an op amp circuit as shown in figure 3.36. The crossing point of the A_{ol} and A_{cl} shows the bandwidth of the op amp circuit whose gain is adjusted by designer. Another method of finding the bandwidth of the circuit is using the op amp parameter gain bandwidth product, also known as GBW. It is a component parameter specified in datasheets and it gives the bandwidth of the circuit for a specific gain value with $BW = \frac{GBW}{Gain}$. But, this relation is valid provided that the slope of the A_{ol} curve is -20dB/decade.

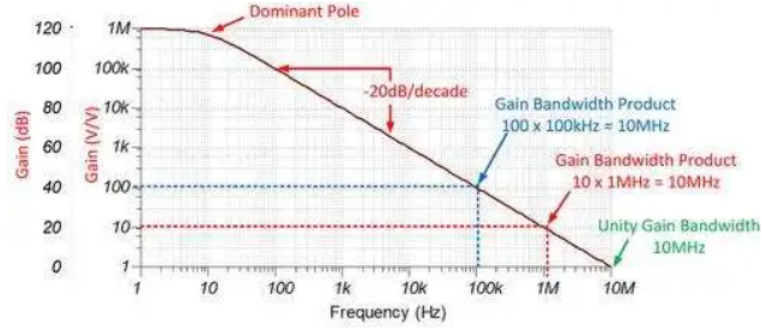


Figure 3.36: Op amp open loop and closed loop curves[85]

In our targeted analog front end circuit, op amps have unity gain and the selected op amp should have enough bandwidth for the gain of one.

3.2.2.1.4 Stability

Every circuit with a feedback has a potential to be unstable as mentioned in 3.2.1.4. Op amp circuits may have poles and zeros and each of them introduce a phase shift. For a circuit to be stable, total phase shift that is introduced to the system should be less than 180° at the point where gain is unity. For this reason, op amps in the unity gain configuration are the most potentially unstable circuits and need special care while selecting them for this specific purpose.

3.2.2.1.5 Slew Rate

Slew rate is defined as the maximum rate of change of an op amp's output voltage and it is given with the units of volts per microsecond. It is a large signal characteristic and measured by applying a large signal step like 1V and observing the necessary time for the output to go from %10 to %90 for a specific load as shown in figure 3.37. This parameter is related with how fast an op amp source or sink current for a specific loading condition. For the example shown in figure

$$3.37, \text{ Slew Rate} = \frac{\Delta V_o}{\Delta Time} = \frac{8V}{0.25\mu s} = 29 \frac{V}{\mu s}.$$

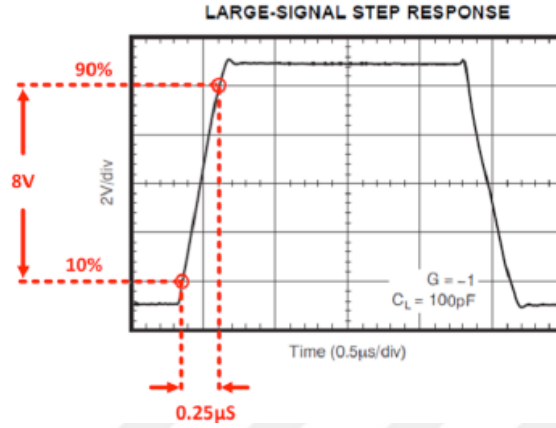


Figure 3.37: Op amp slew rate measurement[86]

For the targeted imaging system, the buffer op amp needs to have such a slew rate that it can track the ROIC output for the worst case scenario. The worst case scenario is, going from the ROIC's minimum output value to maximum value in one multiplexing time. So, minimum slew rate should be $\frac{\text{voltage swing}}{\text{clock period}} = \frac{2V}{100ns} = 20 \frac{V}{\mu s}$.

3.2.2.1.6 Common Mode Rejection and Power Supply Rejection

An op amp should only respond to the voltage differences between its input terminals in ideal situations. However, in real life, op amps may be sensitive to the signals that is common to both inputs and that is not desirable. CMRR, or common mode rejection ratio in other words, shows the level of op amp's is insensitivity to the common mode signals.

Similarly, a change in the power supply rail should have no effect on op amp's output voltage. The rate of not passing on power supply changes to the output is called PSRR or power supply rejection ratio.

CMRR and PSRR for an op amp should be as high as possible provided that they don't lead to costly overdesign. Moreover, PSSR and CMRR values vary over frequency. They should be high for specific frequencies such as at a switched-mode

power supply's switching frequency or a clock source frequency in the system.

3.2.2.1.7 Noise

It is mentioned in 3.2.1.1 that there are two type of noise sources which are extrinsic and intrinsic noise sources. Extrinsic noise effects can be minimized with the adoption of good design methodologies such as shielding, application of good layout techniques etc. Intrinsic noise are due to electronic components and they cannot be eliminated completely. Intrinsic noise types are also reviewed in 3.2.1.1.

When designing a signal chain, every element of the signal chain contributes to the overall noise of the system. For this reason, every element's noise properties should be analyzed thoroughly. Then, best option for the signal chain should be selected, which is the option that degrades the sensor performance at a minimal level. While selecting for the best option, having a detailed information about op amp noise types and their effects on the performance helps greatly.

For better noise analysis of any signal chain, noise sources are modeled. A voltage source at the non-inverting input representing voltage noise and two uncorrelated current sources at both inputs representing current noise with an ideal noiseless op amp constitutes op amp noise model as in figure 3.38. The two uncorrelated current noise sources can also be summed in rss (root sums of squares) fashion and represented as one current source. Current noise becomes noticeable only when there is a large source resistance.

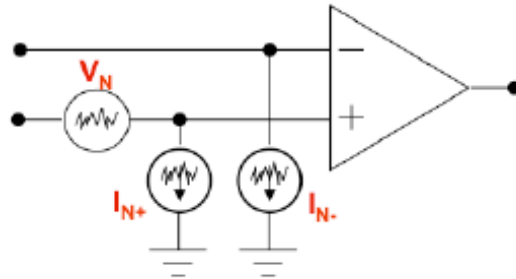


Figure 3.38: Op amp noise model

While selecting an operational amplifier as a voltage buffer at the ROIC output, noise of op amp should have such a value that it doesn't add so much on the readout noise of the ROIC. Since uncorrelated noise sources are summed in rss method, there is a general rule of thumb stating that the additional noise from external circuitry shouldn't exceed one tenth of sensor's, ROIC's readout rms, noise. This way total noise is only % 0.5 more than ROIC's readout noise and can be neglected. Op amp noise parameters for selection need to be considered on the basis of this approach along with other signal chain elements.

After careful investigation, an op amp whose core characteristics are given in table 3.2 is selected. The parameters are given specifically for the targeted operating conditions.

Parameter	Typical Value	Unit
Input Offset Voltage	0.2	mV
Input Bias Current	± 3	fA
Common Mode Rejection Ratio	90	dB
Power Supply Rejection Ratio	95	dB
Bandwidth(Unity Gain)	350	MHz
Slew Rate (Rising)	400	V/ μ s
Slew Rate (Falling)	260	V/ μ s
Input Common Mode Voltage Range	$V_+ + (0.5) - V_- - (0.4)$	V
Output Voltage Swing	$V_+ + (0.1) - V_- - (0.2)$	V
Noise Spectral Density	4.1	nV/ $\sqrt{Hz}$

Table 3.2: Selected op amp's key parameters

This op amp is suitable for our imaging system's analog front end circuit. It has a very high input impedance which enables the ROIC's output to drive it. Both rising and falling slew rates are well over the critical slew rate value of 20V/ μ s. Offset value is constant in the operation range and can be eliminated with calibration. Noise spectral density value yields a much lower rms noise value than the ROIC's readout noise in the targeted bandwidth leaving some margin for

other signal chain components. Detailed calculations are carried out in 3.2.2.4.5.

3.2.2.2 Programmable Gain Amplifier –*Fully Differential Amplifier*–

The selected ROIC outputs video signals in a pseudo differential method. In this method, there is one reference signal shared by four video signals. Modern ADCs accept fully differential signals for superior performance. In order to implement pseudo differential to fully differential conversion of the ROIC signals, a fully differential amplifier is utilized.

3.2.2.2.1 Fully Differential Signaling

Fully differential signals consist of two complementary single-ended signals with respect to a dc common mode and they are 180° out of phase. The final differential signal is obtained by taking the difference between the two single-ended signals. The resulting signal therefore, has twice the magnitude of each single-ended signal. An illustration for a pair of differential signal is given in figure 3.39.

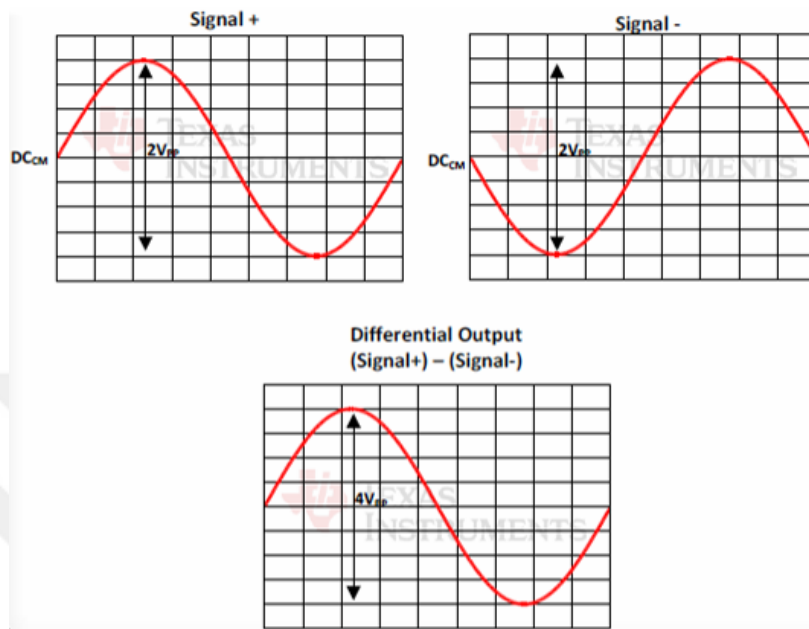


Figure 3.39: Differential signals[63]

Fully differential signaling has the following advantages, and therefore they are commonly used.

- Common mode signals are better rejected, noise and interference that are common to both signals are eliminated,
- Even order harmonics are canceled,
- Dynamic range is doubled without the need of using higher voltage levels.

3.2.2.2.2 FDA Structure

A simple structure of FDA is shown in figure 3.40. There are three operational amplifiers one of which determines the common mode dc value. Other two operational amplifiers are configured in inverting amplifier configuration with an ability of introducing gain with external resistors. This structure offers low noise and highly balanced differential signals around a desired dc common mode voltage.

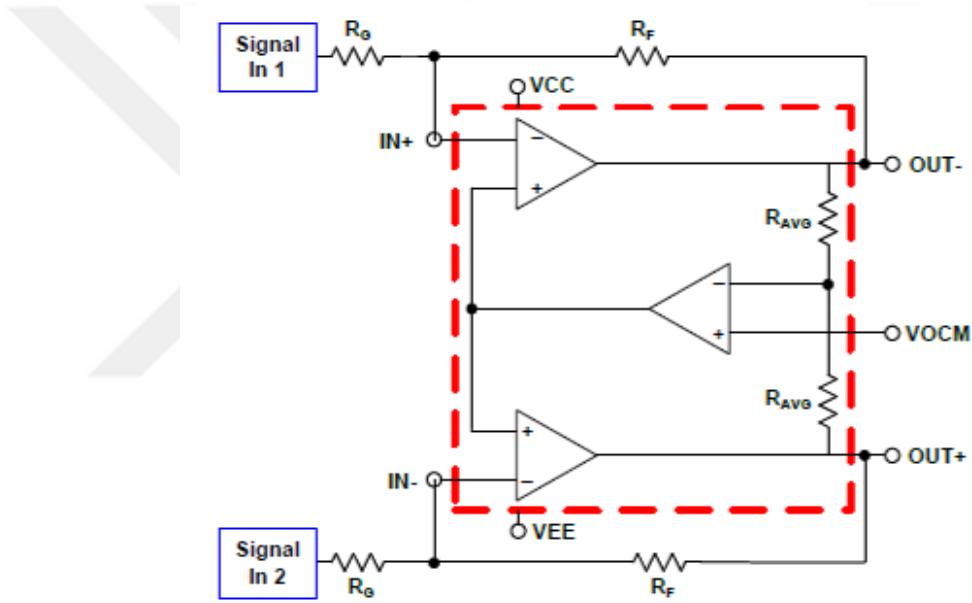


Figure 3.40: Fully differential amplifier structure is shown in red dashed lines[63]

Nodal analysis of this structure can be made applying core knowledge about op amps. IN+ and IN- nodes track each other exactly. OUT+ and OUT- signals are 180 ° out of phase and complementary of each other around V_OCM dc value. The signal gain introduced by the FDA is given with $\frac{R_F}{R_G}$.

3.2.2.2.3 Noise

The noise model of an FDA is shown in figure 3.41 with a differential voltage noise and two uncorrelated current noise sources equal in value. Also, noise sources from external resistors are included in the system. Noise gain, is given as

$1 + \frac{R_F}{R_G}$, different from the signal gain.

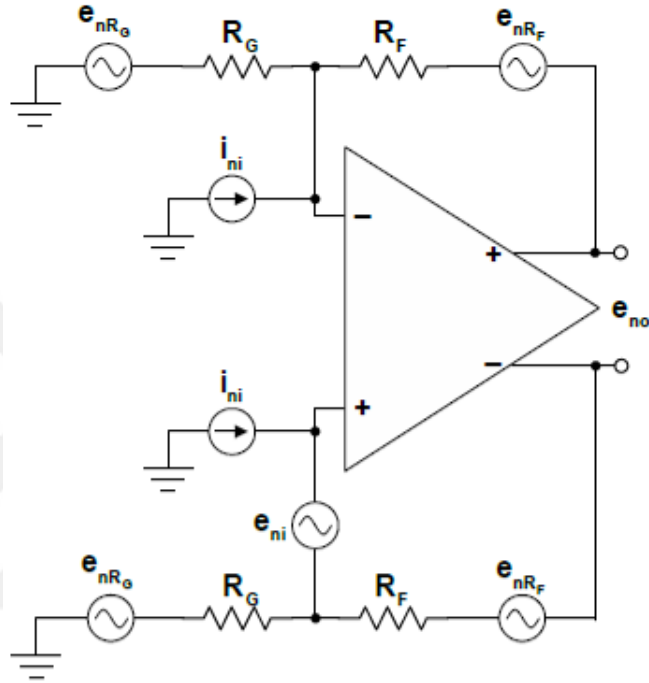


Figure 3.41: Fully differential amplifier noise model[64]

After careful investigation, an FDA whose core characteristics are given in table 3.3 is selected. The parameters are given specifically for the targeted operating conditions.

Parameter	Typical Value	Unit
Differential Offset Voltage (Input Referred)	± 0.3	mV
Input Bias Current	± 60	μA
Common Mode Rejection Ratio	90	dB
Power Supply Rejection Ratio	85	dB
Bandwidth(Unity Gain)	2	GHz
Slew Rate +OUT Rising (-OUT Falling)	1720	$\text{V}/\mu\text{s}$
Slew Rate +OUT Falling (-OUT Rising)	1580	$\text{V}/\mu\text{s}$
Differential Input Noise Voltage Density	1.1	$\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current Density	8.8	$\text{pA}/\sqrt{\text{Hz}}$
Settling Time	1.9	ns

Table 3.3: Selected FDA's key parameters

This FDA is convenient for our imaging system's analog front end circuit. Both rising and falling slew rates can track buffer op amp's output. Offset value is constant in the operation range and can be eliminated with calibration just as it is for the selected op amp. Noise spectral density value gives a lower rms noise value than the op amp's output and hence ROIC's readout noise in the targeted bandwidth. It has enough bandwidth and low settling time to drive the selected ADC. Detailed calculations are carried out in 3.2.2.4.5.

3.2.2.3 Analog to Digital Converter ADC

An imaging system needs an ADC to convert analog image signals to a set of digital numbers which can be transmitted, manipulated, and/or stored. Since the ROIC selected for the aimed imaging system doesn't have on-chip ADCs, external ADC is needed. There are plenty of ADC architectures and performance metrics related with data converters. These demand gaining knowledge about them and going for the best option for the targeted imaging system.

3.2.2.3.1 Architecture Comparison

The three most common ADC architectures used in imaging systems are successive approximation register, ramp/counter, and sigma-delta.

3.2.2.3.1.1 Ramp ADC

The simplest and most often used ADC architecture in imaging systems is the ramp ADC. It is generally implemented within the ROICs, thanks to its easy-to-implement structure and small die area. The operation principle is based on comparing analog sampled input signal to on-chip produced ramp at each clock edge. The counter circuit is incremented at each clock concurrently with the ramp signal. The comparator is triggered when the ramp signal passes the sampled input signal. At this instant, the counter value is latched to the memory, giving the digitized equivalent of the input signal[5].

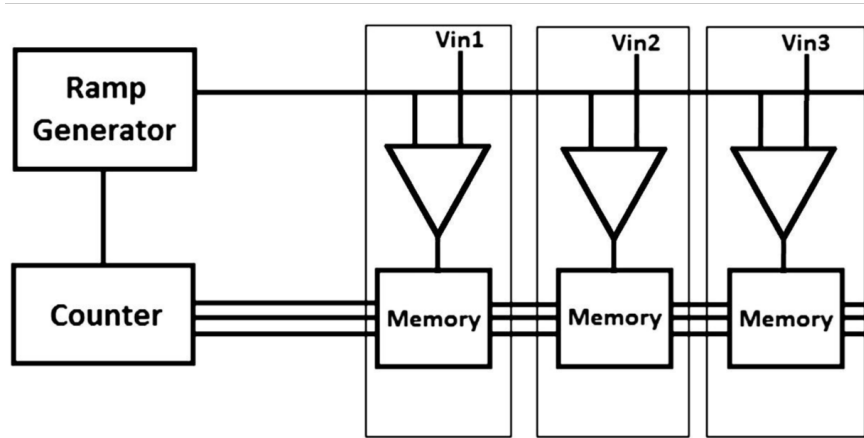


Figure 3.42: Blocks of a ramp ADC[5]

Conversion speed is the limiting factor in this architecture. Consequently, this architecture is not suitable for applications requiring great resolution and speed.

3.2.2.3.1.2 Sigma Delta ADC

Thanks to the oversampling and noise shaping characteristics, Sigma Delta ADCs are remarked for their high resolution conversion. Under a negative feedback loop, the input voltage is sampled and modulated multiple times. The comparator compares the modulated output to the reference value and provides feedback to the DAC, in order to influence the modulator's input. Digital decimation filters filter the comparator's digital output. This operation of modulation and demodulation reduces noise to a great extent[5].

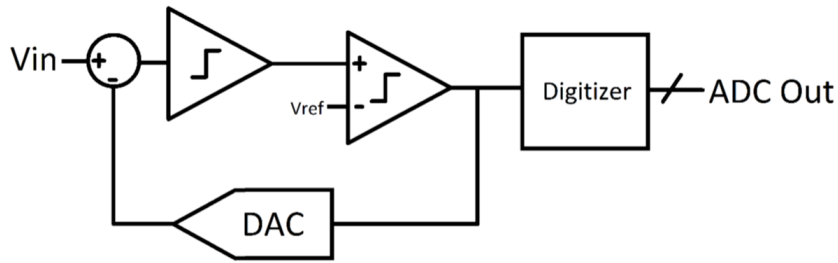


Figure 3.43: Block diagram of a sigma delta ADC[5]

Sigma delta ADCs are generally used for low speed conversion purposes. Even though they are low-noise due to noise shaping, they are not good selection for high speed imaging purposes because they average signal over a time interval and that is not desired in digitizing multiplexed DC signals.

3.2.2.3.1.3 SAR (Successive Approximation Register) ADC

SAR ADCs are widely used for their high speed operation ability and efficiency. Analog signal at the input is stored in sampling capacitor. The stored signal is then compared with the output of a digital to analog converter (DAC). At every clock cycle, DAC adjusts its analog output according to comparator output. Analog signal is approximated until the difference between the input signal and the DAC output is less than $1/2$ LSB. Final value is the digitized equivalent of the input signal.

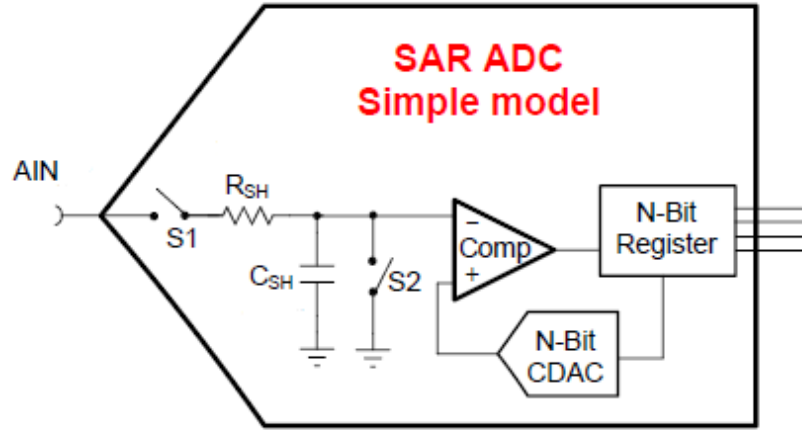


Figure 3.44: SAR ADC model[65]

SAR ADCs require n clock cycles for n bit conversion. They are low power, low-latency, suitable for high data rates and there are many commercially available products. Moreover, their snapshot operating feature makes them very convenient for conversion of multiplexed DC signal values. For this reason, SAR ADC architecture is the most favorable option in the targeted imaging system. For the mentioned reasons, SAR ADC architecture is selected to be used in our imaging system.

3.2.2.3.2 SAR ADC Working Principle

When a signal is applied to the input of the ADC, it is first acquired in the acquisition phase. The input signal is stored in the sample and hold capacitor with the internal switches are at the places shown in figure 3.45a. Since this is an RC circuit, the input signal charges the capacitor at an exponential rate. Duration of the acquisition phase is determined according to sampling rate of the ADC.

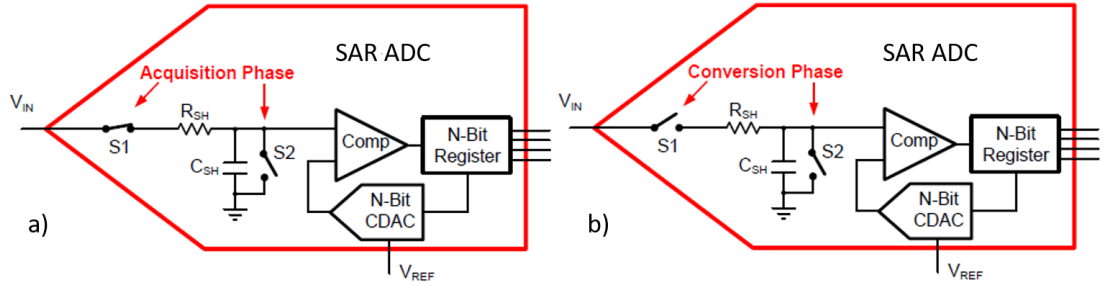


Figure 3.45: SAR ADC in a) acquisition phase b) conversion phase[65]

After the acquisition phase, internal switches are adjusted in places as shown in 3.45b. This indicates the start of conversion phase. Output of the CDAC is adjusted in a such a manner that it tries to match its output with the signal stored in the sample and hold capacitor. The conversion takes n cycles, where n is the resolution of both CDAC and the overall SAR ADC.

Figure 3.46 shows the operation during the conversion cycle of a five bit converter. DAC output starts comparison with the input signal by making MSB 1. Since the resulting DAC output doesn't exceed analog input, MSB is kept as 1. In the next test MSB-1 is made 1, it is seen that DAC output exceeds analog input, MSB-1 is switched to 0 and it is time for testing MSB-2. MSB-2 is made 1, DAC output is smaller than analog input and it is kept as 1. For both MSB-3 and LSB output of DAC exceeds analog input and they are switched back to 0 indicating the end of conversion cycle with the digitized value.

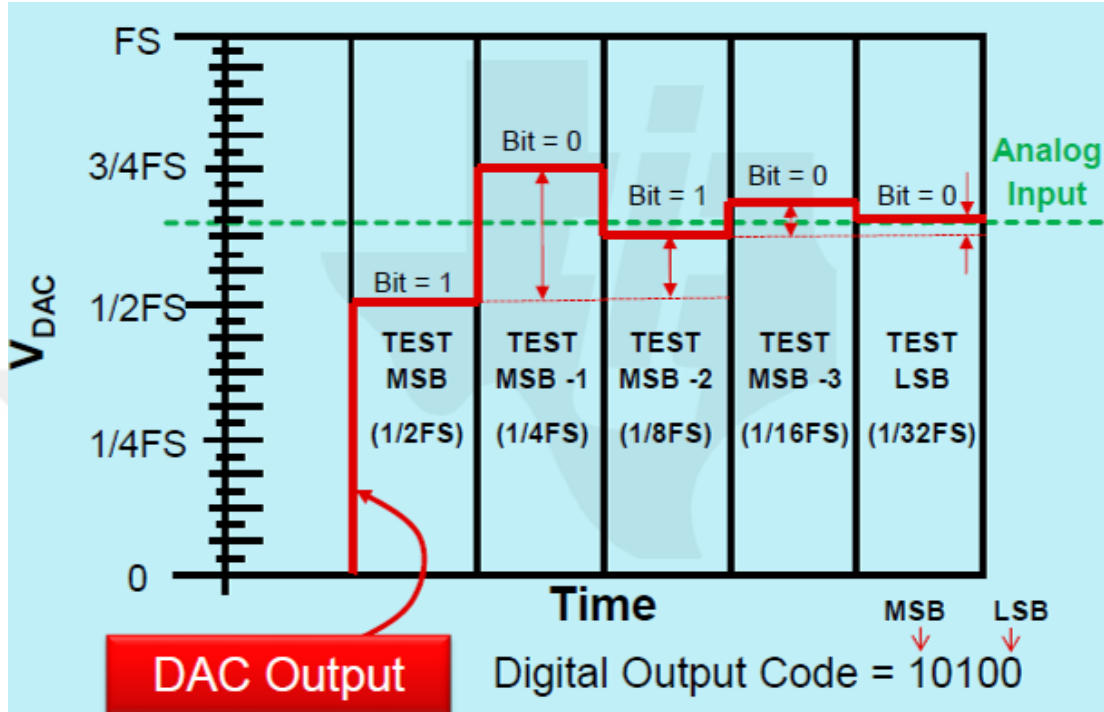


Figure 3.46: SAR ADC conversion cycle[65]

3.2.2.3.3 Performance Metrics

When selecting an ADC, the performance parameters supplied by the manufacturer is the main source to resort to. To understand if an option is suitable for an aimed application, the performance parameters must be understood very well.

3.2.2.3.3.1 INL(Integral Non-linearity) and DNL(Differential Non-linearity) and NMC(No Missing Code)

In ideal cases, an ADC is expected to have a transfer function which is like the the one shown in figure 3.47.

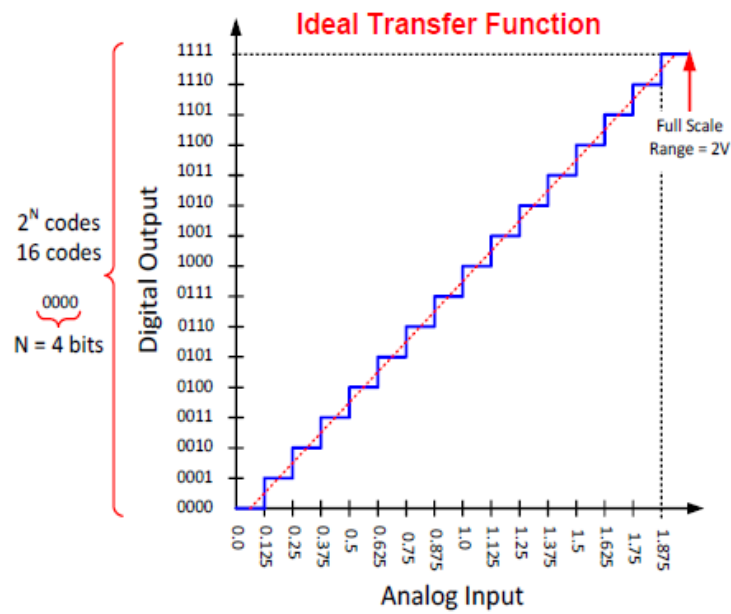


Figure 3.47: Ideal transfer function of a 4-bit ADC[66]

But in real life applications, it is almost impossible to come up with such an ADC. Not all the code widths are equal to each other and have the ideal code width. The deviation from the ideal code width creates DNL error. Transfer function of a 4-bit ADC with some DNL error is shown in figure3.48.

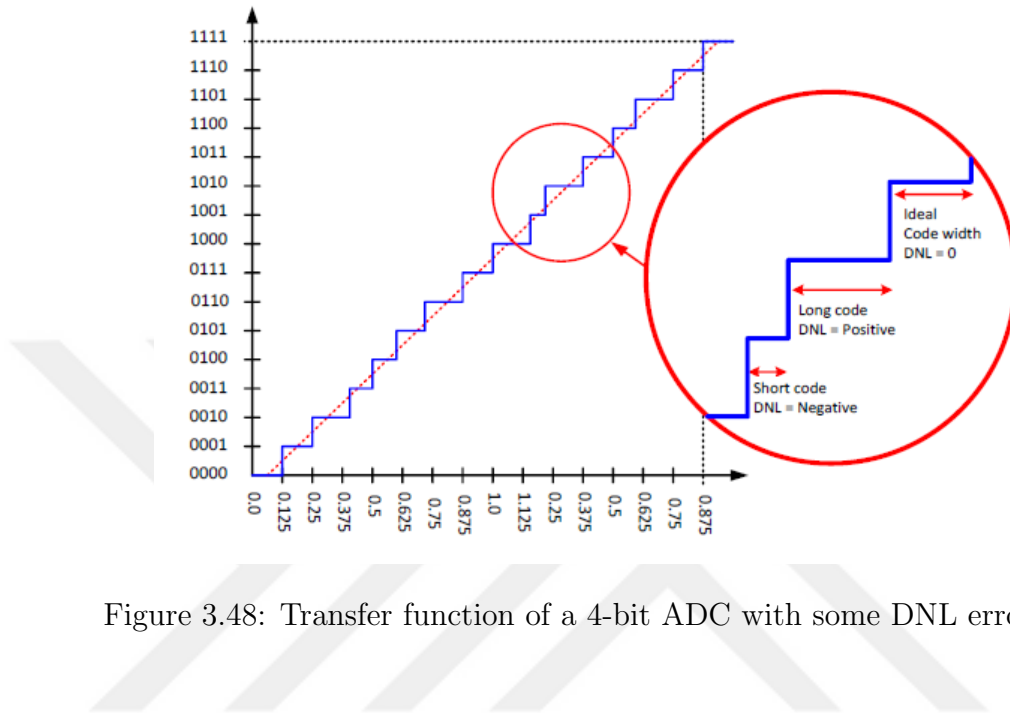


Figure 3.48: Transfer function of a 4-bit ADC with some DNL error[66]

Another non-ideality reason is linear end point fit's deviation from the ideal fit. Transfer function of a 4-bit ADC with some INL error is shown in figure 3.49

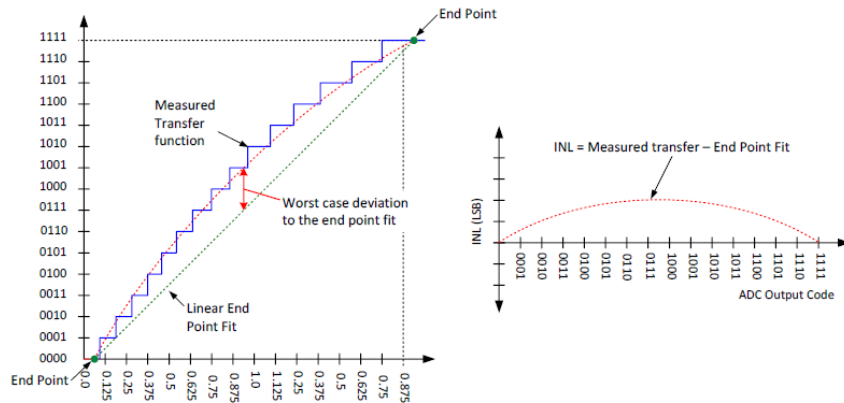


Figure 3.49: Transfer function of a 4-bit ADC with some INL error[66]

In some ADCs, a digital output code which corresponds to an analog input value is completely skipped. No analog input value gives that specific output code. The skipped output code is named as missing code, and shown in figure 3.50.

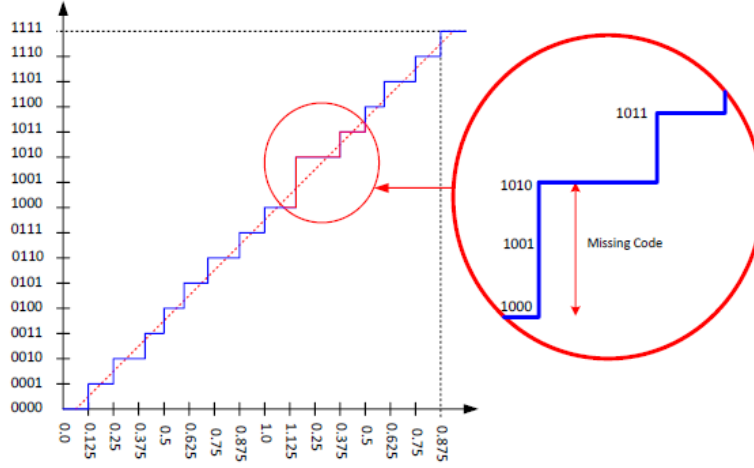


Figure 3.50: Transfer function of a 4-bit ADC with a missing code[66]

INL, DNL and NMC are the main DC specifications of an ADC that give information about the DC performance of the ADC. For sensitive imaging systems, they should be kept as low as possible. In some systems oversampling and averaging can be used to smooth out the DNL errors. For our systems averaging can't be used and low-DNL ADC selection becomes important.

3.2.2.3.3.2 Common Mode Rejection Ratio(CMRR) and Power Supply Rejection Ratio(PSRR)

CMRR is calculated using the ratio of the error created by a signal that is common to both inputs to the common mode signal as shown in equation 3.9.

$$CMRR(dB) = 20 \log \left(\frac{\Delta V_{CMerror}}{\Delta V_{CM}} \right) \quad (3.9)$$

PSRR, in a similar manner is calculated using the ratio of the error created by a disturbance in the power supply rail to the power supply disturbance amplitude as shown in equation 3.10.

$$PSRR(dB) = 20 \log \left(\frac{\Delta V_{PError}}{\Delta V_{PS}} \right) \quad (3.10)$$

High values of both PSRR and CMRR are desired. Especially noisy environments and systems with a noisy power supply require high PSRR and CMRR ratings.

3.2.2.3.3.3 SNR (Signal to Noise Ratio) and THD (Total Harmonic Distortion)

SNR, signal to noise ratio, an AC performance metric that can be defined as the ratio of the fundamental signal to the total noise within the interested frequency band. For this measurement, ADC is excited with a pure sinusoidal. SNR is calculated with the measured data with the equation 3.11 after visualizing the signal in the frequency domain as shown in figure 3.51. An ideal ADC has a maximum SNR of $6.02 \times N + 1.76$ where N is the number of bits. This limitation is caused by the quantization noise which is covered in more detail in 3.2.2.3.4.

$$SNR(dB) = 20 \log \left(\frac{V_{signal}}{V_{totalrmsnoise}} \right) \quad (3.11)$$

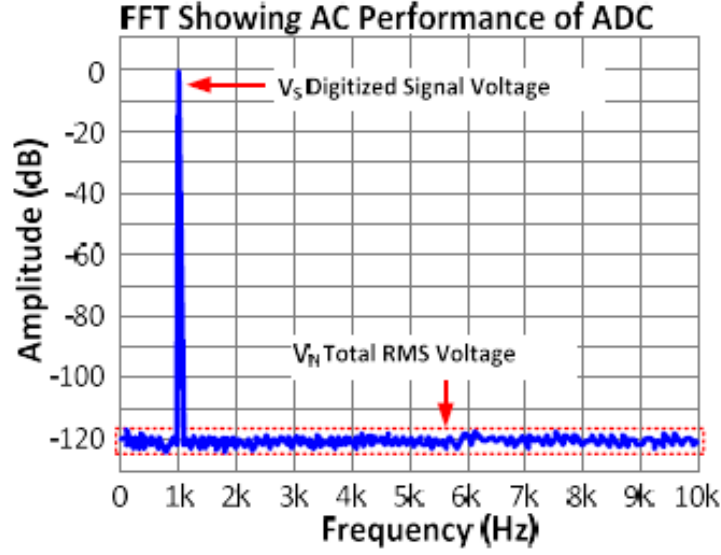


Figure 3.51: Fundamental signal and noise floor in frequency domain[66]

THD, total harmonic distortion, is an AC performance metric which mainly focuses on the linearity of the ADC. In figure 3.52b it is seen that ADC has a nonlinear response while digitizing the applied signed. This non-linearity causes the harmonics shown in figure 3.52a. Total harmonic distortion is the ratio of the fundamental signal to the harmonic signals and it is calculated with the equation 3.12. Harmonics are included up to tenth harmonic according to IEEE standards. Low values of THD yield highly linear ADCs.

$$THD(dB) = 20 \log \left(\sqrt{\frac{\sum_{i=2}^{10} V_i^2}{V_s^2}} \right) \quad (3.12)$$

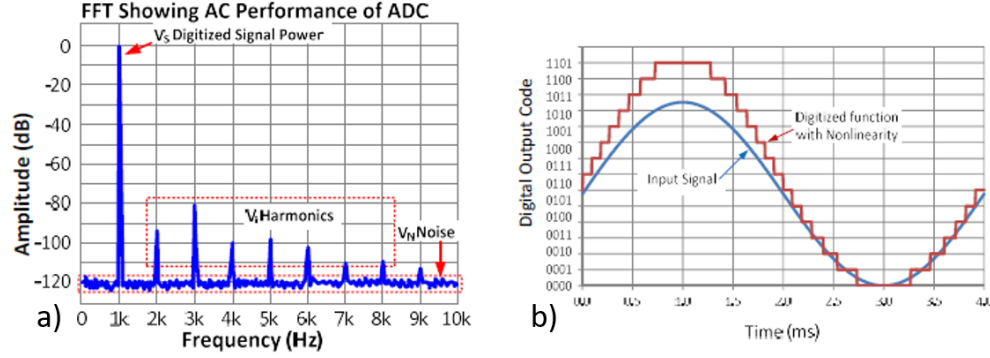


Figure 3.52: a) Fundamental signal and its harmonic frequency domain b) Non-linear response of the ADC in time domain[66]

(THD + N) is another metric which considers both noise and harmonics and it is calculated with the equation 3.13. SINAD (signal to noise and distortion ratio) is the reciprocal of (THD+N) and it is calculated with the equation 3.14.

$$(THD + N)(dB) = 20 \log \left(\sqrt{\frac{\sum_{i=2}^{10} V_i^2 + V_N^2}{V_s^2}} \right) \quad (3.13)$$

$$SINAD(dB) = 20 \log \left(\sqrt{\frac{V_s^2}{\sum_{i=2}^{10} V_i^2 + V_N^2}} \right) \quad (3.14)$$

ENOB (equivalent number of bits) is another AC performance metric and it is derived from SINAD, given with equation 3.15.

$$ENOB = \frac{SINAD - 1.76dB}{6.02} \quad (3.15)$$

SNR, THD, ENOB and SINAD are AC performance parameters. They are measured with the excitation of an pure sinusoidal signal. In the targeted imaging system, ROIC outputs DC signals with the programmed multiplexing rate. These AC performance metrics cannot directly be related with the performance of the imaging system. But they generally give a clue about the ADC performance[66].

3.2.2.3.3.4 Noise Free Code Resolution and Effective Resolution

The noise-free code resolution of an ADC is the number of bits of resolution beyond which it is impossible to distinctly resolve individual codes. This limitation is caused by the effective input noise, also defined as the input-referred noise, associated with all ADCs due to kT/C and thermal noise. Input referred noise is usually expressed as an rms quantity with the units of LSBs rms. To use in necessary calculations, there may be a need for conversion between rms and peak to peak values. Rms noise value is converted to peak to peak noise by multiplying it by 6.6[67]. Noise-free counts is calculated as in equation 3.16 to be used in noise-free code resolution calculation in equation 3.17. Some manufacturers specify effective resolution instead of noise-free code resolution that is given in equation 3.18. N is the number of bits of the ADC.

$$Noise - free Counts = \frac{2^N}{peak - to - peak input noise(LSB)} [67] \quad (3.16)$$

$$Noise - free Code Resolution = \log_2 (Noise - free Counts) [67] \quad (3.17)$$

$$Effective Resolution = \log_2 \left(\frac{2^N}{input rms noise(LSB)} \right) [67] \quad (3.18)$$

Noise-free Counts and Effective Resolution are DC performance parameters. They may be given in supplier datasheet or they can be inferred using other parameters such as input referred or code transition noise.

3.2.2.3.4 Noise

Noise in an ADC system comes from many places. The ADC itself has thermal noise and quantization noise. External analog circuitry has its own noise and it

adds up on to the ADC noise. Moreover, other elements such as voltage reference, power supply and clock jitter also contribute to overall noise.

There is a misconception about signal resolution in ADC systems. ADC resolution cannot improve the system resolution if the system has high level of noise. So, gathering information about all the noise contributors of the system including ADC noise plays a critical role in the system.

3.2.2.3.4.1 Quantization Noise

Due to quantized nature of ADCs, it is not possible to have a corresponding digital code for every analog input value. As seen in figure 3.53, there is always an inevitable error. This error is reflected to frequency domain as a broadband noise and named as quantization noise. All ADCs have this noise and this is the limiting factor for SNR value for an ideal ADC.

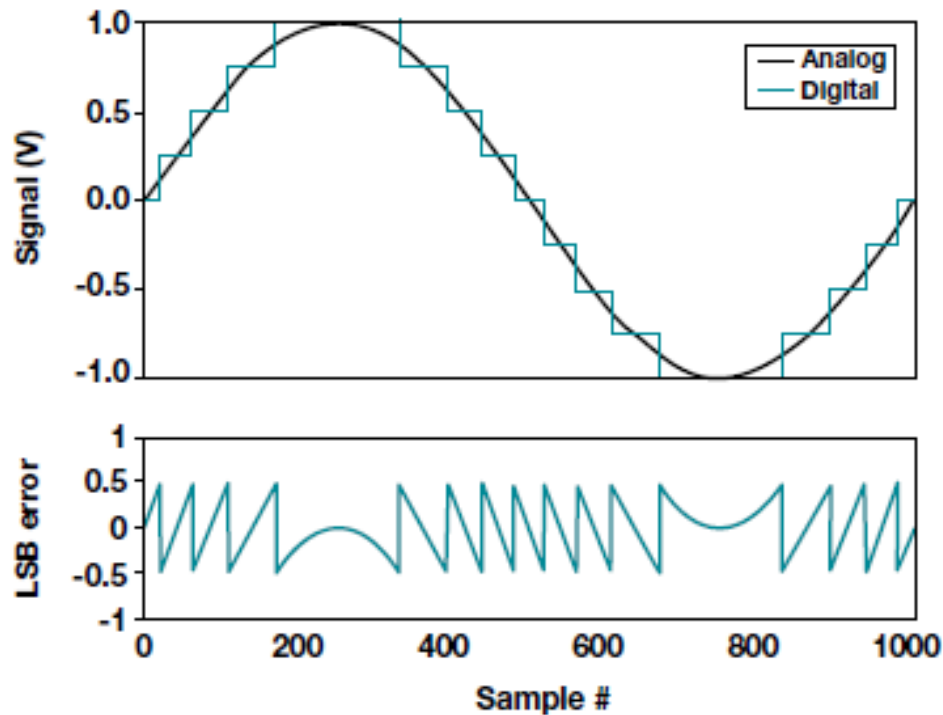


Figure 3.53: Error from quantized nature of ADCs[82]

3.2.2.3.4.2 Thermal Noise

Thermal noise in ADCs can be defined as combination of all noise sources other than quantization noise such as resistor noise and kT/C noise. Thermal noise is summed with quantization noise using root-sum-squares method since they are uncorrelated. Thermal noise can be observed both in time domain and in histogram as shown in figure 3.54. In figure 3.54a, expected time domain signal and resulting histogram for a fixed analog input is shown. But in real life, what we see is shown in figure 3.54b both in time domain and in histogram distribution. This is the thermal noise, showing Gaussian distribution in histogram and random values in time domain.

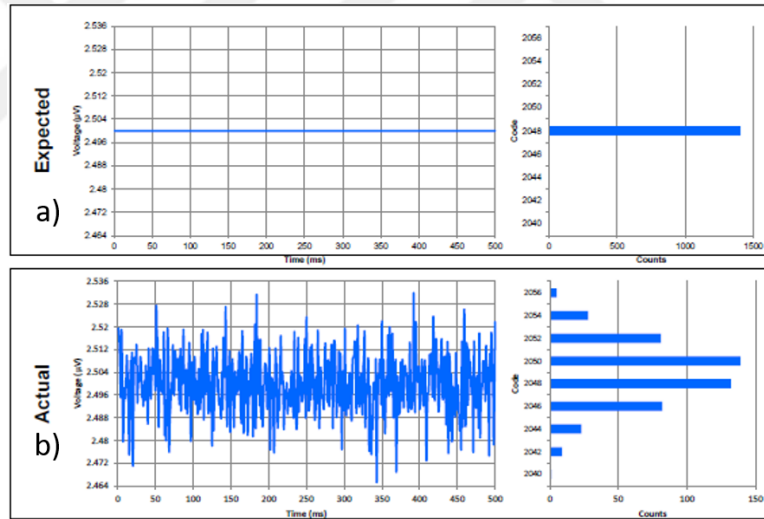


Figure 3.54: ADC output a) expected b) actual[83]

Another representation of this noise is shown in figure 3.55. For an ideal ADC, the level of code transition noise is zero, and hence its transfer function's transition region width is also zero. However in real life, ADC has some code transition noise, and because of that it has a finite transition region width. Code transition noise is generally known as input referred noise. To determine the equivalent rms input referred noise, analog inputs should either be grounded or connected to a voltage source which is heavily decoupled and free of noise[67]. Resulting histogram is like the one shown in figure 3.54b. Rms noise is the

standard deviation (σ) of the resulting histogram with units of LSB. LSB voltage equivalent can be used to find the input referred noise with units of V_{rms} and peak to peak noise voltage can be calculated by multiplying rms noise voltage by 6.6. This helps with the overall noise analysis when other electronic components are also in the noise equation.

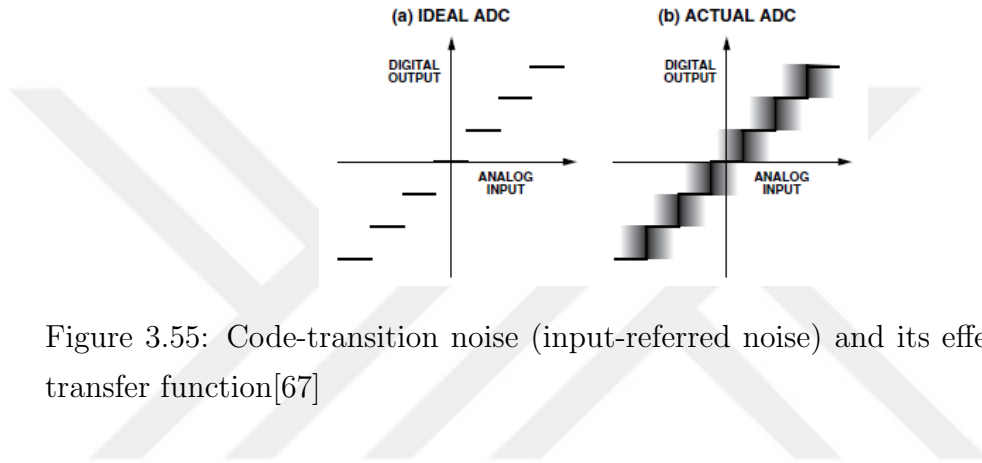


Figure 3.55: Code-transition noise (input-referred noise) and its effect on ADC transfer function[67]

If the standard deviation (σ) of the resulting histogram differs with different values of input voltage levels, averaging them gives a reasonable value to be used in further analysis. Normally that should not be the case provided that DNL value is acceptably low[67].

Another possibility is that, the resulting histogram doesn't look like a Gaussian. This means that the ADC is not designed properly or bad printed circuit board layout techniques are employed like poor grounding and/or decoupling[67].

3.2.2.3.4.3 Kickback Noise

Kickback noise arises due to switching and movement of charges during the switches between acquisition and conversion phases. When conversion time is over, sample and hold capacitor resets. The sample and hold capacitor needs to be replenished so that its voltage is equal to that of the ADC input. This charge transfer should be finished and the voltage across the sample and hold capacitor needs to be settled at the end of acquisition phase. According to the rule of

thumb, the voltage across the sample and hold capacitor should be within the range of $V_{ADCIN} \pm 1/2 \text{ LSB}$.

This noise can be eliminated or minimized by employing a charge bucket circuitry at the input. This is covered in detail in 3.2.2.3.5.

3.2.2.3.5 ADC Input Model and Driving the ADC

Figure 3.56 shows a typical input model of a SAR ADC. During the acquisition phase the voltage at the input should charge the sample and hold capacitor C_{SH} . Since the input is an RC circuit charging has an exponential curve. At the end of the acquisition phase C_{SH} should be charged to the value of the input with a maximum error of $1/2 \text{ LSB}$. In order to fulfill this requirement an ADC driver with enough bandwidth along with a charge bucket circuit should be placed at the input of the ADC. Otherwise, kickback noise becomes prominent by degrading circuit performance.

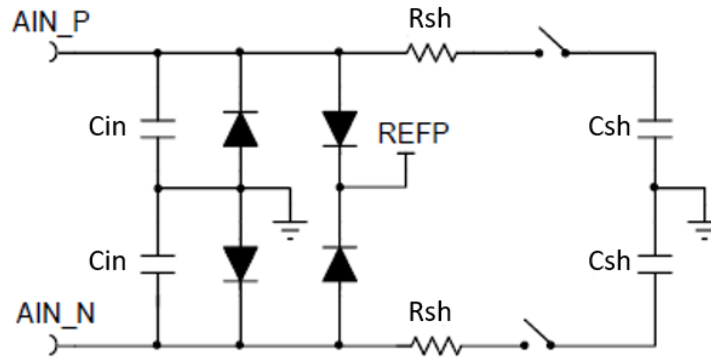


Figure 3.56: Input model of a typical SAR ADC

After conducting meticulous survey, an ADC with SAR architecture whose core characteristics are given in table 3.4 is selected. The parameters are given specifically for the targeted operating conditions.

Parameter	Typical Value	Unit
Resolution	14	bits
Input Voltage Range	1 or 2 (Selectable)	V_{p-p}
SNR	73.4	dBFS
Code Transition Noise(Input Referred Noise)	1.2	LSB(rms)
Common Mode Rejection Ratio	80	dB
Power Supply Rejection Ratio	85	dB
Missing Codes	0 (No Missing Codes)	
Sampling Rate	10/20/40 (Selectable)	MSps
Configuration Interface	SPI	
Digital Data Output Format	LVDS	

Table 3.4: Selected ADC's key parameters

The selected ADC is compatible with our system requirements. It has eight simultaneous sampling ADCs that are integrated on single chip. The sampling rates it supports are convenient for the output rate of the ROIC. Its input referred noise is low enough not to degrade system performance greatly. Detailed calculations are carried out in 3.2.2.4.5.

3.2.2.4 Overall Analog Front End Circuit

The components of the analog front end circuit are chosen. They need to be integrated to come up with the correct overall analog front end circuit.

3.2.2.4.1 Overall System

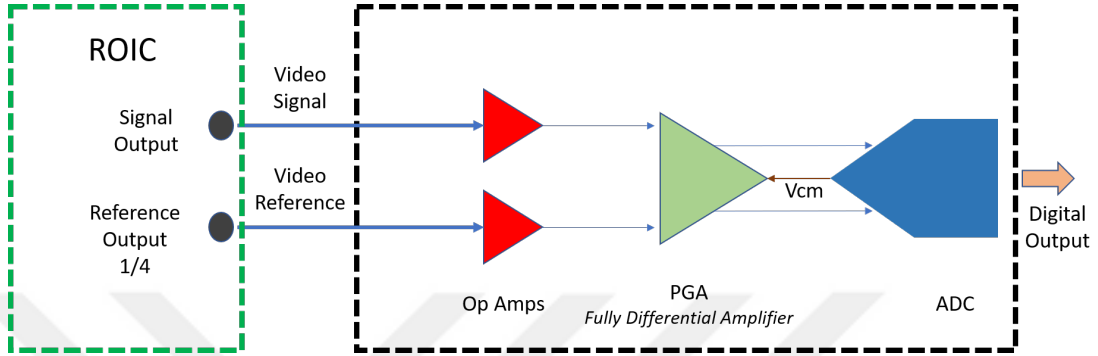


Figure 3.57: Overall analog front end circuit

In the overall system, ROIC sends video signals with eight different analog signals and there are two reference signals for these eight channels. In figure 3.57, only one channel is shown. Both video and reference signals are buffered with unity-gain configured op amps. This is required because ROIC's output buffers' drive capability is very low. Then, the buffered signals are fed into a FDA (Fully Differential Amplifier) to convert pseudo differential signals to fully differential signals. The FDA drives the ADC with fully differential signals. ADC outputs its common mode voltage and this common mode voltage is connected to the common mode pin of the FDA to make sure the differential signals at the input of the ADC have the same common mode as the ADC. There are other passive components that are used for filtering, compensation, gain adjustment and charge bucket circuitry, but they are not shown in this overall diagram for the sake of simplicity. Finally, digitized image data are sent to the digital controller of the system for further processes.

3.2.2.4.2 Integrated Noise Models and Calculations

For analysis of the overall noise of the system, all noise sources from noise models of components are integrated together. Some noise sources such as current noise of op amps are neglected because their effect is minimal. Figure 3.58 shows the system with all the noise sources to be considered.

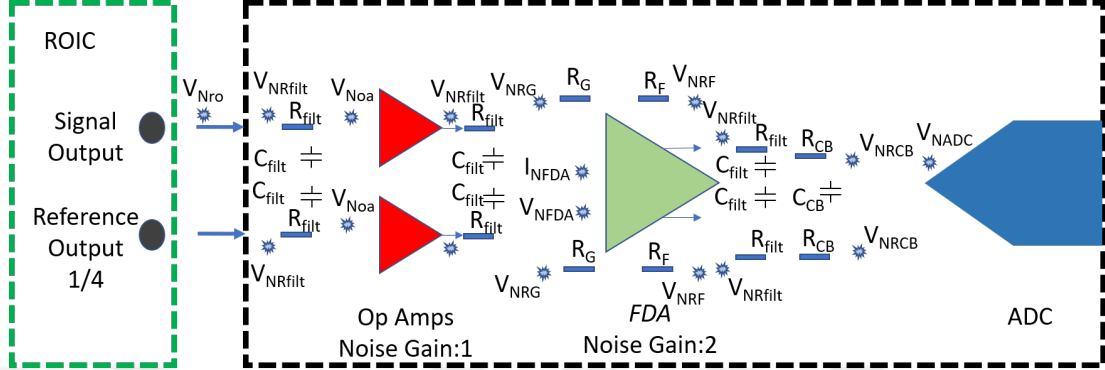


Figure 3.58: AFE with all noise sources integrated

Abbreviated noise sources' descriptions are as follows;

- V_{Nro} : Readout noise of the ROIC,
- V_{NRfilt} and V_{NRCB} : Thermal noise of filter and charge bucket resistors,
- V_{Noa} : Input referred noise of op amp,
- V_{NRG} and V_{NRF} : Thermal noise of the FDA gain resistors,
- V_{NFDA} and I_{NFDA} : Current and voltage noise of the FDA,
- V_{NADC} : Input referred noise of the ADC.

To make the noise calculations, first it is better to state that all noise sources are considered as rms voltage sources and they are going to be added with root-sums-squares. All of the noise sources are considered to be totally uncorrelated. Noise gain of the FDA is 2 even though the signal gain is 1. All noise sources are added at the adc input, yielding the resulting overall noise at the input of the ADC.

$$N_{overall} = \sqrt{(2 \cdot V_{NFDA})^2 + 2 (I_{NFDA} \cdot R_F)^2 + 2 (V_{NRF})^2 + 2 (2 \cdot V_{NRG})^2 + 2 (2 \cdot V_{Noa})^2 + 4 (2 \cdot V_{NRfilt})^2 + 2 (V_{NRCB})^2 + 2 (V_{NRfilt})^2 + V_{NADC}^2} \quad (3.19)$$

This is a very complicated equation and each of the noise source should be calculated with their noise effective bandwidth. Having multiple pole and zero points make it almost impossible to correctly determine the effective noise bandwidth. Instead of hand calculation, using a spice simulator is a way better option. But, knowing the noise contributors and the level they affect the total noise gives designer the confidence to detect the problem and correct it. With this point of view, equation 3.19 becomes useful.

3.2.2.4.3 ROIC Output Loading Equalization

As mentioned previously, the selected ROIC has one reference output shared by four signal outputs. At this point, a problem arises. The loading that output of the ROIC reference sees is different from that of signal outputs see. In order to eliminate or minimize this problem, RC filters that are placed between ROIC outputs and buffer op amps should be adjusted. The adjustment needs to be done in such a way that both the loading and the resulting bandwidth of four signal outputs and one reference output are the same. This can be achieved by manipulating the resistor and capacitor values of the RC network. This manipulation can also be verified by spice analysis.

The simulation results in figure 3.59 and 3.60 show that both reference and signal output sees the same loading and have the same AC response.

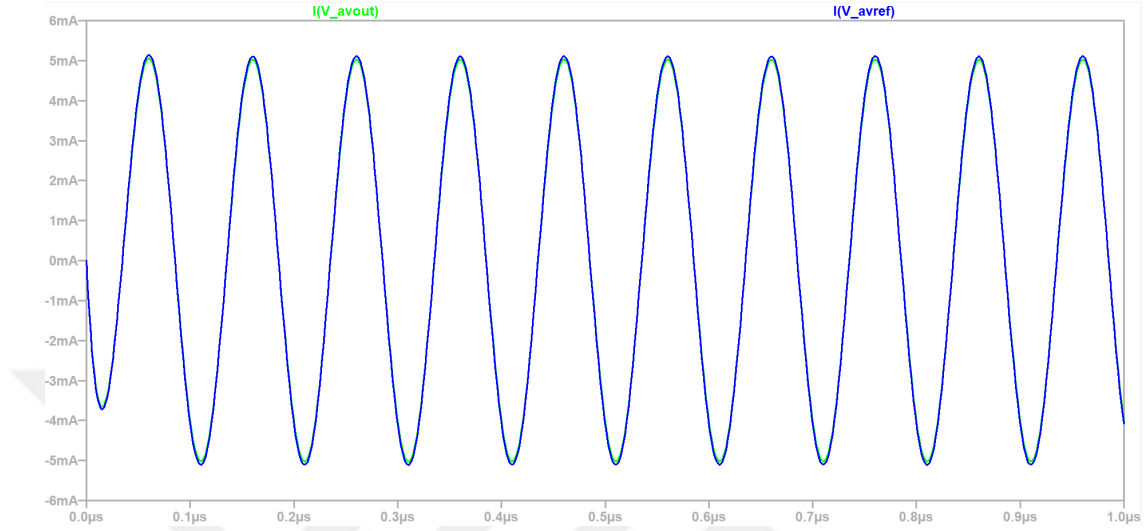


Figure 3.59: The current drawn from signal and reference output

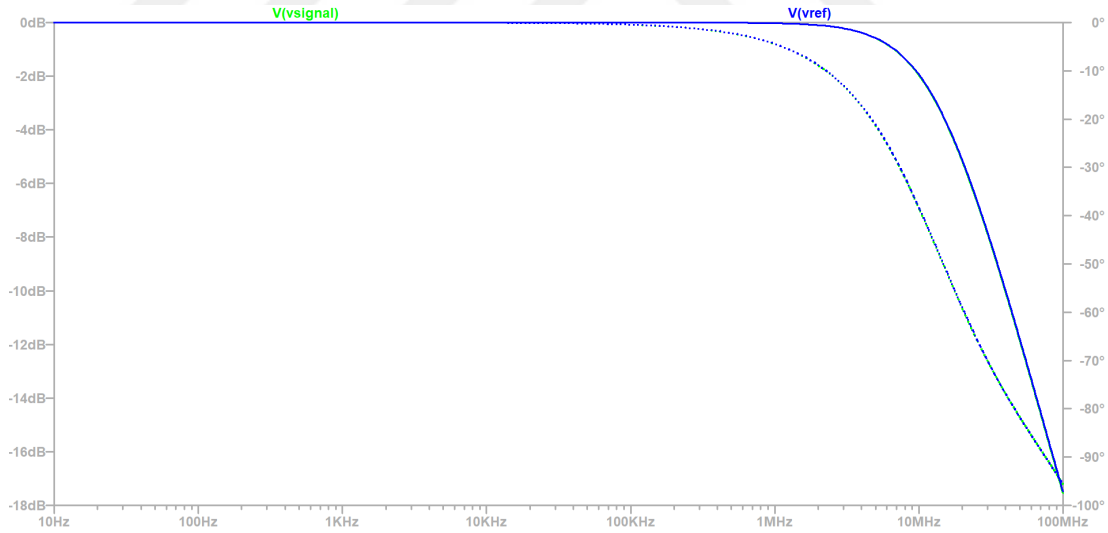


Figure 3.60: AC response of signal and reference output

3.2.2.4.4 ADC Driving

3.2.2.4.4.1 Charge Bucket Design

In order to design a charge bucket circuit, input model of the selected ADC needs to be created. Figure 3.61 shows the created ADC analog input model

with input resistor and capacitor values given in the datasheet. The timing of the acquisition and conversion phases are also generated using datasheet timing diagrams to simulate the input model correctly.

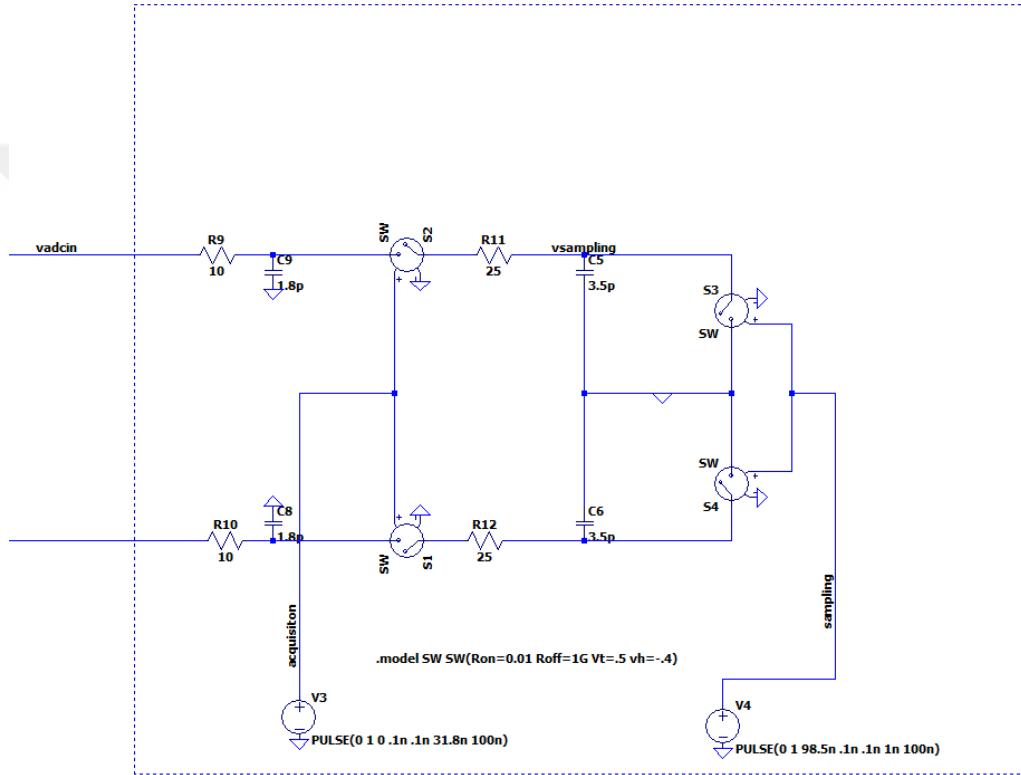


Figure 3.61: Selected SAR ADC's analog input model

Here, charge bucket RC circuit should be implemented in such a way that it should have enough bandwidth to replenish sample and hold capacitor and settle before next conversion phase. However, larger bandwidth yields higher noise. For this reason, with iterative processes, the circuit given in figure 3.62 is designed with enough bandwidth for settling and limiting as much noise as possible.

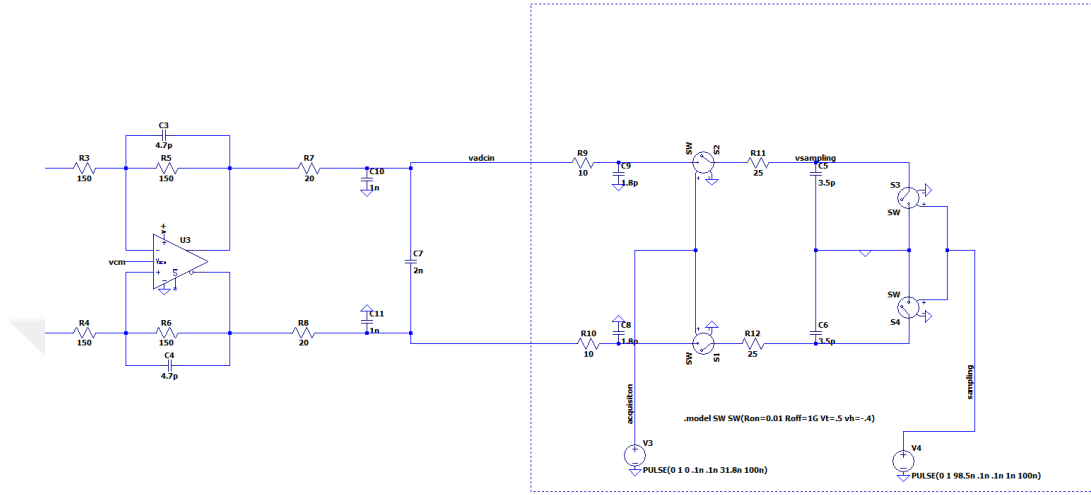


Figure 3.62: ADC input model and driver circuit

The amount of error right before the next conversion phase is around 140nV which is much lower than the $1/2$ LSB value of $61\mu\text{V}$. The simulation result is given in figure 3.63

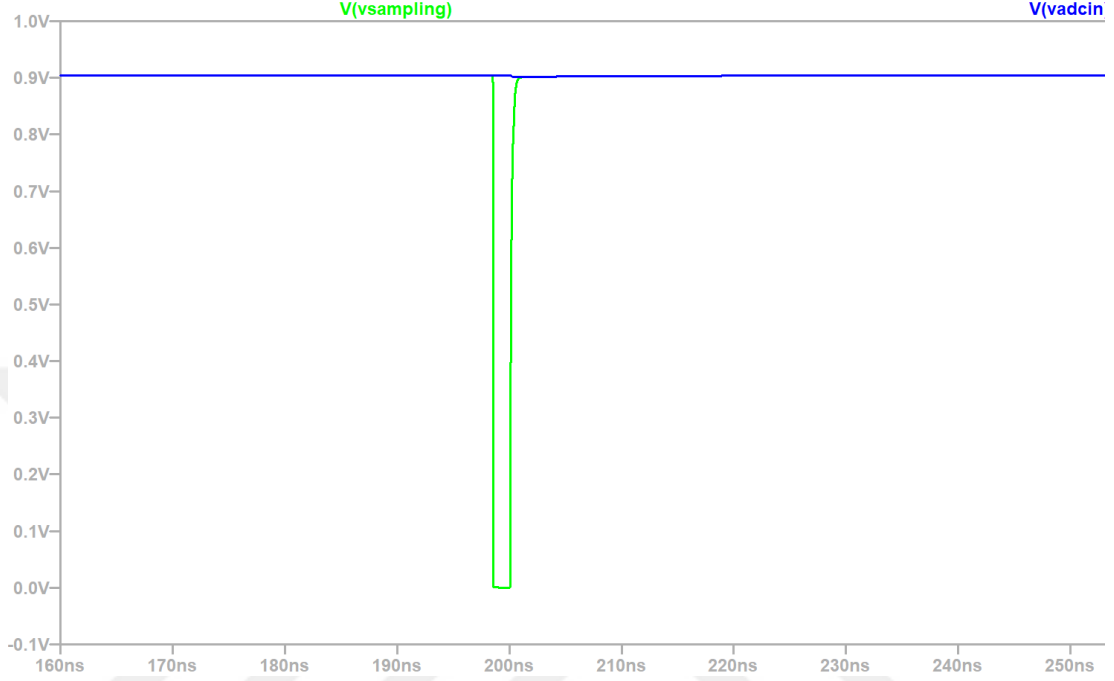


Figure 3.63: ADC input settling error simulation result

3.2.2.4.5 Overall Noise Analysis

In 3.2.2.4.2 the overall noise contributors of the system is shown. To understand how much degradation of SNR is introduced to sensor by the external electronics is calculated as follows;

- Sensor SNR value is calculated as $20 \log\left(\frac{FullWellCapacity}{ReadoutNoise}\right)$ which is equal to $20 \log\left(\frac{350000e-}{110e-}\right) = 70.05$ dB. This is the highest SNR that can be reached or limiting factor for the system in other words.
- Sensor readout noise is converted μV_{rms} value using peak-to-peak sensor output voltage $2V \times \frac{110e-}{350000e-} = 628 \mu V_{rms}$.
- The analog front end circuit is seen as a black box. ADC input referred noise and other electronics' noise contribution at the ADC input is calculated and accepted as the total noise of the black box. Dividing it by the gain gives

the rms input referred noise of the black box then which can be summed with sensor readout rms noise.

- ADC input noise contributor kickback noise assumed to be reduced so much that it can be neglected. This leaves only thermal and quantization noise of the ADC, together they can be named and analyzed as ADC input referred noise. ADC input referred noise can be calculated in two ways. First, datasheet gives a parameter as code-transition (or input referred) noise with a unit of LSB rms. For our 14-bit ADC code-transition noise is given as 1.2 LSB rms which yields to $\frac{2V}{2^{14}} \times 1.2 = 146 \mu\text{Vrms}$. Another formula to calculate input referred noise is using the SNR value which is given in the ADC datasheet in the equation 3.20. Using this equation gives $151 \mu\text{Vrms}$ which is close to the calculated value with the code transition noise.

$$\text{input referred noise}_{ADC} = \frac{(\text{full scale voltage})}{2\sqrt{2} \cdot 10^{\frac{SNR}{20}}} [68] \quad (3.20)$$

- At the ADC input node, op amps and FDA along with resistors contribute to ADC input referred noise with the equation 3.19. The contributor's noise values are given as noise spectral density values in their datasheets. For rms noise effective noise bandwidth values need to be calculated separately which can be challenging with multiple poles and zeros. Instead, carrying out noise simulation in spice gives the total rms noise at the ADC input. This step is done after charge bucket design and ROIC output load equalization steps since they lead to change in system bandwidth. Figure 3.64 shows the simulated rms noise.

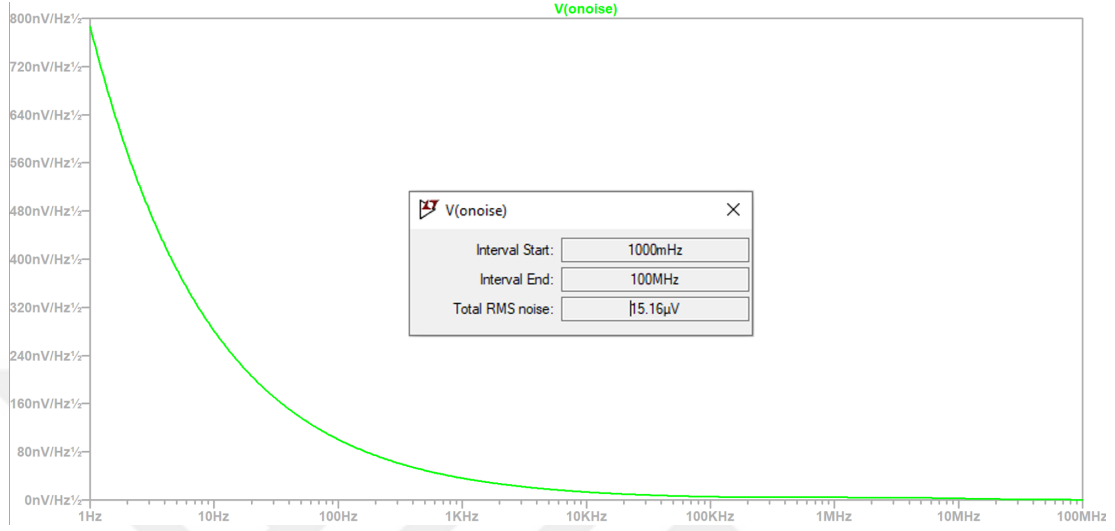


Figure 3.64: System noise in rms

- Total ADC input noise is calculated as $\text{adc input rms noise} = \sqrt{15^2 + 146^2} \approx 147 \mu\text{Vrms}$. Total AFE input referred noise is also $147 \mu\text{Vrms}$, since the system gain is equal to 1.
- The noise at the sensor output becomes $\sqrt{147^2 + 628^2} = 645 \mu\text{Vrms}$. New SNR is $20 \log \left(\frac{2V}{645 \mu V} \right) = 69.83\text{dB}$. The degradation caused by the electronics is 0.22 dB.

3.2.2.4.6 Overall AC Analysis

With the design considerations to minimize noise some precautions need to be taken to make the system stable. Compensation capacitors are placed in parallel with FDA gain resistors. After AC analysis of the system it's seen that the phase margin is more than 50° which means the system is safely stable as shown in figure 3.65 that gives the AC analysis of the overall circuit.

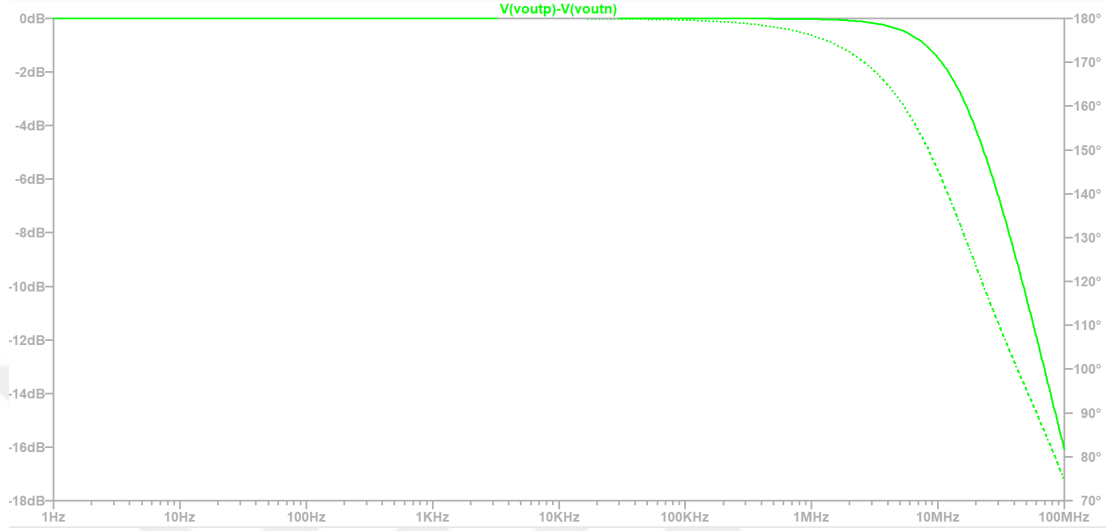


Figure 3.65: Overall analog front end AC analysis

3.3 FPGA Board

After the ROIC signals are digitized, they need to be received by a digital controller to arrange them in such a way that they can be received by the micro-controller (Detailed description of this micro-controller is given in 3.4) to send an outside PC GUI to be displayed. There are a few options to be used for this purpose, FPGAs (Field Programmable Gate Arrays), CPLDs (Complex Programmable Logic Devices), ASICs (Application Specific Integrated Circuits) with custom design or commercially available micro-controllers. Out of these, an FPGA is the most convenient solution for our system. FPGA's programmable logic feature makes it convenient for research and development applications because any custom logic can be implemented whereas in micro-controllers, users are restricted with what is offered by the manufacturer. They have superior power than CPLDs, and overall design cycle is much less costly than ASICs'. Moreover, soft-core processors can be synthesized within FPGAs which make them a great, flexible option.

Selecting an FPGA for a specific purpose demands detailed analysis of the

system requirements. After the system requirements are clear, FPGA families and specific FPGA products are analyzed to determine the FPGA product to be used.

The tasks that the FPGA in the system is required to perform and the restrictions are as follows;

- Having standard communication interfaces such as SPI, I2C and UART to configure or read data from integrated circuits in the system,
- Receiving differential data from the ADC of the system,
- Carrying out non-uniformity correction algorithm for the acquired image,
- Interfacing with an external memory element during non-uniformity correction process,
- Wrapping up the acquired and non-uniformity corrected data and sending the image data with CSI interface to the micro-controller (Detailed description of this micro-controller is given in 3.4),
- Consuming moderate amount of power and occupying small board space.

3.3.1 FPGA

Field-programmable gate array (FPGA) is a logic device that can implement user desired logics by programming logic functions. Figure 3.66 shows the structure of a typical island-style FPGA. The basic components of an FPGA can be split into three categories. The first one consists of the logic elements (the logic block: LB) that realize logic circuits. The second is the input/output elements (the input/output block, IOB) which input and output signals to and from outside. The third is the wiring elements (the switch block, SB, and the connection block, CB) connecting LBs and IOBs. Apart from these three components, there are a clock network, a configuration/scan chain, and a test circuit. Specific function

circuits, including soft or hard core processors, block memory, and multipliers, are also included in commercial FPGAs[80].

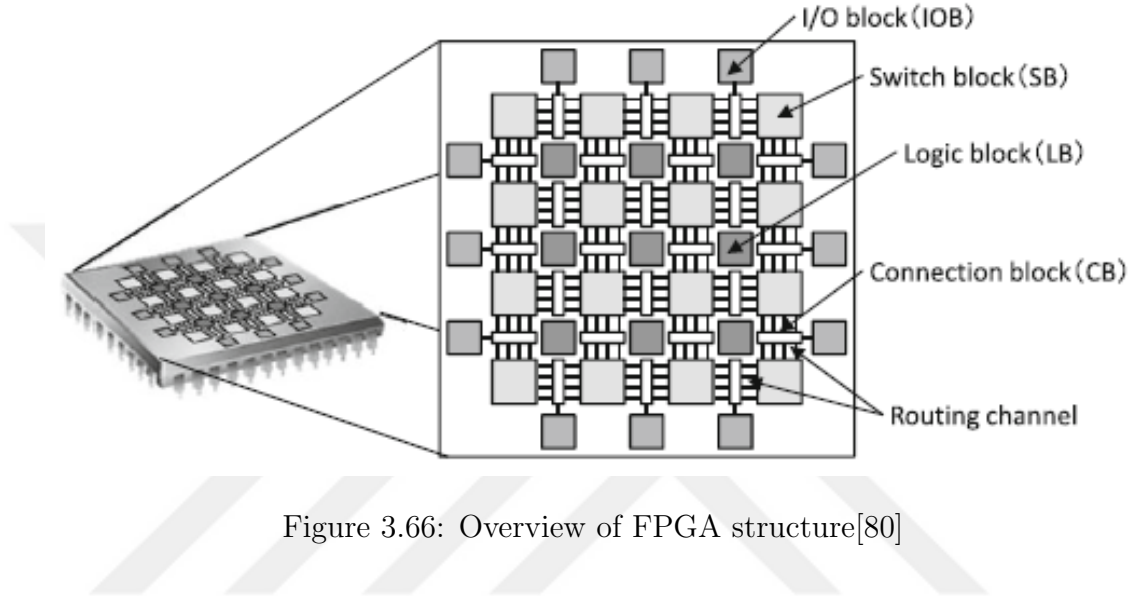


Figure 3.66: Overview of FPGA structure[80]

An FPGA's capabilities can be inferred by looking at the resources such as logic, memory, clock, I/O and embedded hard IP resources. By looking at the availability of these resources, it is easy to understand whether or not the selected FPGA can get through the required tasks.

After careful research, a commercially available FPGA with the core characteristics that are important in our application given in table 3.5 is selected to be used in the system.

Resource	Availability
Logic Cells	101440
Slices	15850
CLB Flip Flops	126800
Maximum Distributed RAM(Kb)	1188
Block RAM/FIFO w/ ECC (36 Kb each)	135
Total Block RAM (Kb)	4860
Clock Management Tiles (1 MMCM + 1 PLL)	6
Maximum Single Ended I/O	300
Maximum Differential I/O Pairs	144
DSP Slices	240
Parameter	Value
Dimension	15mm X 15mm
Ball Pitch	0.5mm

Table 3.5: Selected FPGA's resources and parameters

The selected FPGA safely meets system requirements with all the resources it has and the small space area it consumes with a reasonable ball pitch. It can also deploy embedded processing with a soft-core processor supplied by the device vendor. Moreover, it supports DDR3 interface with a data rate up to 866Mb/s.

The vendor of the selected FPGA has footprint compatible, lower cost options that can replace the selected FPGA. Considering this, after research and development phase, lower-cost options can be integrated to the system without the need of redesigning a PCB.

3.3.2 Memory

The memory that the FPGA has is volatile and when it is powered down, the configuration becomes lost. For this reason, a non-volatile memory element that

holds the configuration file is needed. In our system, this non-volatile memory is also responsible for keeping calibration data for non-uniformity correction. However, there is a drawback for non-volatile memories which is low data transfer rate. This is where dynamic random access memories come into play. They are also volatile memory elements but they can reach high data rates.

The solution is as follows; a flash memory, which is a non-volatile memory, holds both FPGA configuration file and non-uniformity correction calibration data. At the power-up FPGA is configured with the configuration file. After that, FPGA reads the non-uniformity correction calibration data and writes them to a DDR3 RAM. During non-uniformity correction process, FPGA reads related data from DDR3 RAM at a fast rate that non-uniformity correction is carried out successfully.

As memory elements, a flash memory with SPI interface and a DDR3 RAM with a parallel interface is selected.

3.3.3 Clocking

The selected FPGA's clocking resources manage complex and simple clocking requirements with dedicated global and regional I/O and clocking resources. The clock management tiles (CMT) enable clock frequency synthesis, deskew, and jitter filtering functionality. Clocking of synchronous elements across the device is possible thanks to global clock trees[81].

Most of the required clocking functions are carried out by the FPGA. But, it must be supplied with an appropriate external clock source. Since FPGA can synthesize a wide variety of clock sources with different frequencies, having a low-jitter fixed frequency oscillator is a good choice. Keeping these in mind a clock source with the following properties is chosen;

- Low-jitter,

- Long-term reliable with very low temperature and aging drift,
- Available with footprint compatible different fixed-frequency alternatives.

In order to meet aforementioned requirements with a stable and reliable solution, the general block diagram for the FPGA system along with other elements is shown in figure 3.67.

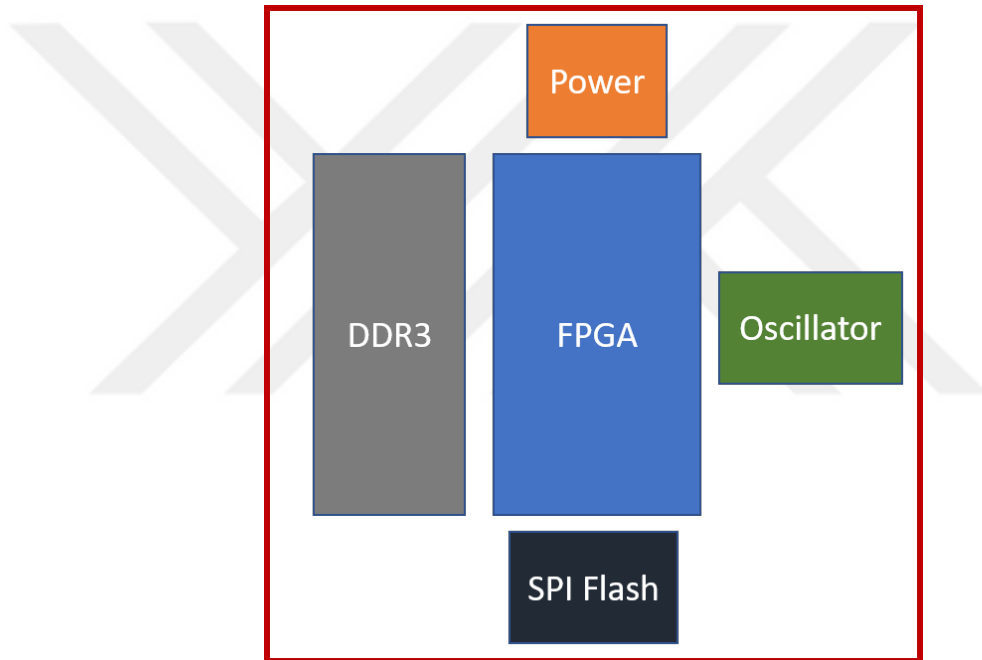


Figure 3.67: Block diagram solution for FPGA with accompanying elements

3.4 Micro-controller Board and its Carrier

FPGA sends the data of the acquired images via a standard called camera parallel interface (CPI) or CSI. Further image processing, compression and data transfer to the PC GUI along with system controls are carried out by a micro-controller. This micro-controller is available as a PCB module. This micro-controller module has some requirements for desired operations, such as Ethernet line driving, memory and powering. To meet those requirements, a carrier board is necessary. The elements of the carrier is shown in figure 3.68.

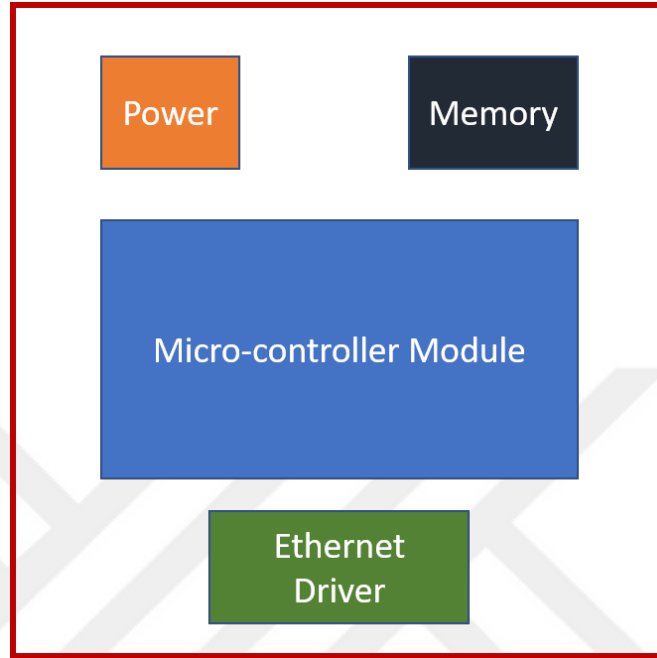


Figure 3.68: Micro-controller baseboard system diagram

3.4.1 Memory

The selected micro-controller runs a Linux based operating system. For booting purpose, it needs a compiled boot file. For user convenience, an SD card slot with appropriate connections to the micro-controller is placed on the baseboard. Some other non-volatile memory elements are also placed for further storage purposes.

3.4.2 Ethernet

A gigabit Ethernet connection is used for both transferring the acquired image data and system control. Gigabit Ethernet is chosen because of its speed, reliability, ease of usage and security.

A generic 7-Layer OSI Model is universally used to designate the frame structure of all communication protocols and Ethernet. As defined by the IEEE802.3

standard, it combines some of the OSI Model layers and the result is just four layers. Design of the physical layer is what hardware designers are interested and in the scope of this thesis[73]. The data flow in our system is shown in figure 3.69.



Figure 3.69: Ethernet data flow diagram

Both MCU and PHY IC are placed on the micro-controller PCB module. RJ-45 connector and magnetics need to be included in the system.

3.4.3 RJ-45 Connector and Magnetics

According to requirements stated in IEEE 802.3 Ethernet standard, Ethernet PHY must be galvanically isolated from the transmission medium. There are two main causes behind this isolation requirement. First, it is possible that there is ground offset between devices that are located with great distances from each other. Second is that, line failures such as a short to a high-voltage rail, a surge-spike, or an ESD strike may damage the system severely. For this reason, the system needs a decent way of protection[73]. To fulfill this requirement, transformers are used because of the advantages they have over optoisolators;

- Transformers do not require external supply,
- They can operate at high speeds whereas optoisolators may fail at rates over 10Mbps,
- They have high common mode rejection ratio and they are very good at differential signaling,
- Transformers offer high isolation voltage protection and this ensures the safety of the PHY IC in the presence of an ESD strike.

The RJ-45 connector is selected according to mechanical and environmental requirements. Required cabling between transformers and the RJ-45 connector is planned carefully.

3.5 TEC Driver

The system requires to stabilize the temperature of the InGaAs detector. This helps in two ways; first, calibration data for non-uniformity correction is taken for different temperatures to be used in those specified temperature ranges and second, lowering the temperature of the InGaAs detector reduces the dark current and gives higher performance. For the realization of the aforementioned purposes, a peltier element is used. The simplified diagram of the thermo-electric cooling system is shown in figure 3.70.

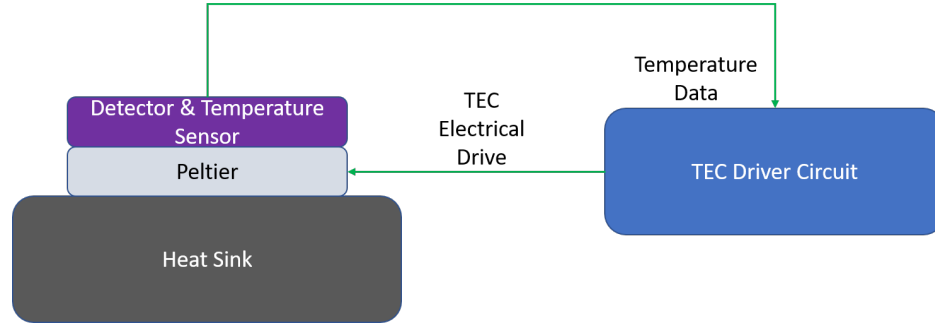


Figure 3.70: Simplified system schematic of the thermo-electric cooling system

3.5.1 Peltier Element and Working Principle

Jean Peltier discovered that, if an electrical current is applied between two conductors, that have distinct properties from each other, heat grows at one junction and gets absorbed by the other. Simply, when an electric current flows through a circuit that is composed of two conductors, a junction will see an increase in its temperature and the other junction will have a cooling effect. This phenomenon is known as the Peltier effect, named after the person who discovered it[69]. With

this nature, peltier elements are widely used in thermo-electric cooling systems.

General structure of a peltier is shown in figure 3.71. A typical thermoelectric module is made up of an array of Bismuth Telluride semiconductor pellets. These pellets are doped, and hence one type of charge carrier, either positive or negative, is responsible for the majority of the current. The pairs of P/N pellets are configured in such a way that they are connected electrically in series, but thermally in parallel. Metalized ceramic substrates stand as the platform for both the pellets and the small conductive tabs that connect them[70].

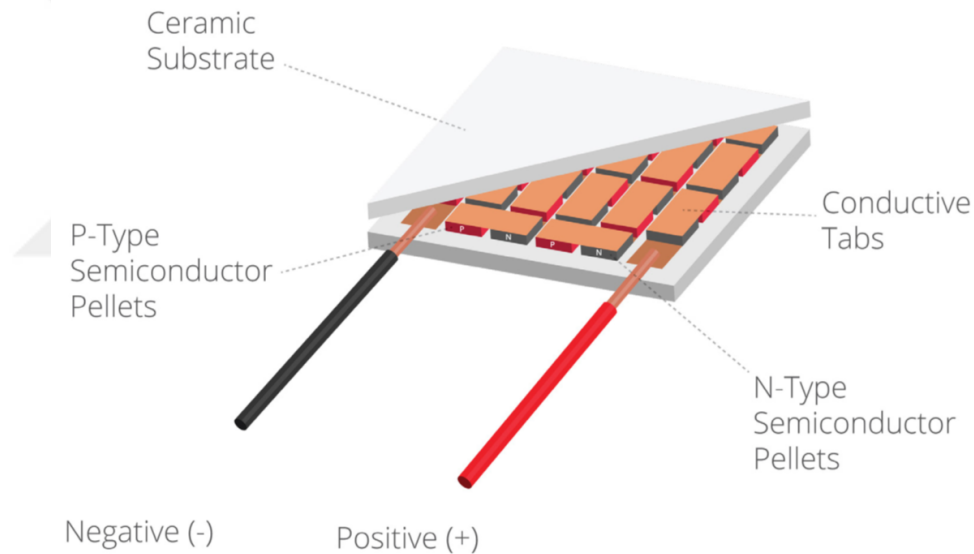


Figure 3.71: General structure of a peltier[70]

To sum up, when a current flows in the proper direction, the electron carriers in the n material and the hole carriers in the p material move thermal energy together with their movement. This action in turn, creates a hot side and a cold side as seen in figure 3.72, making it possible to be used in both cooling and heating systems[71].

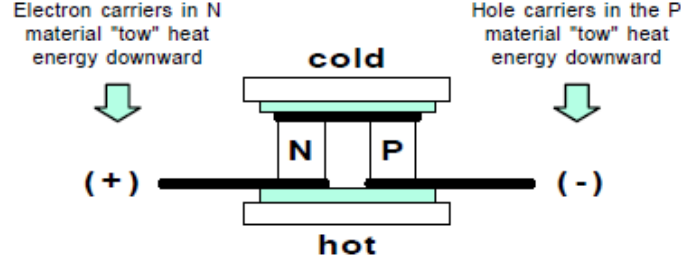


Figure 3.72: Current applied to peltier to create cold and hot plates[71]

3.5.2 Thermal System and Thermo-electric Cooler Driving

Typical schematic of a thermo-electric cooling system is shown in figure 3.73. Here, object is the detector, cooler is peltier element and heat sink is the case of the camera. The aimed temperature of the detector is given as T_1 . Thermal analysis of the overall system is out of the scope of this thesis. But a designer must fully understand that thermo-electric cooling system has thermal resistances and other effects. For this reason, its thermal response must be considered while designing a closed-loop thermo-electric cooler driver.

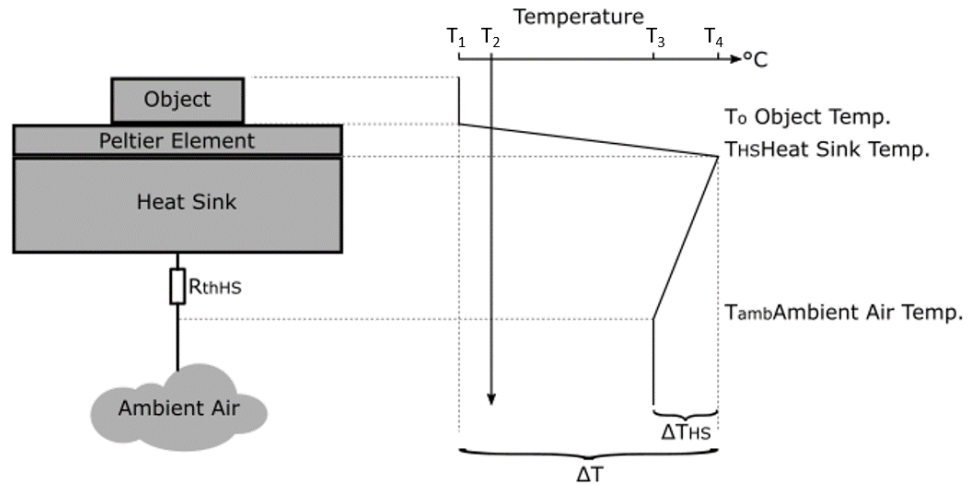


Figure 3.73: Thermal schematic of a typical thermo-electric cooling system[72]

Taking the total thermal schematic into consideration, a commercially available thermo-electric cooler driver IC is selected and the system shown in figure 3.74 is designed. In the system, a temperature sensor is available in the ROIC and thus the image sensor gives feedback about the detector and peltier. This temperature sensor signal is compared with the DAC's output, which is set externally by the user. The difference between two signal is fed into a PID circuit. PID circuit evaluates the difference between feedback signal and set signal (DAC output), generating an output for drive control circuitry. Drive control circuitry generates required voltage across peltier's connections to either heat or cool the detector. Ultimate goal of the system is to make the temperature signal from the detector equal to DAC output. So, different output values of the DAC correspond to different temperature values. Setting DAC output to those values, determines the final sensor temperature.

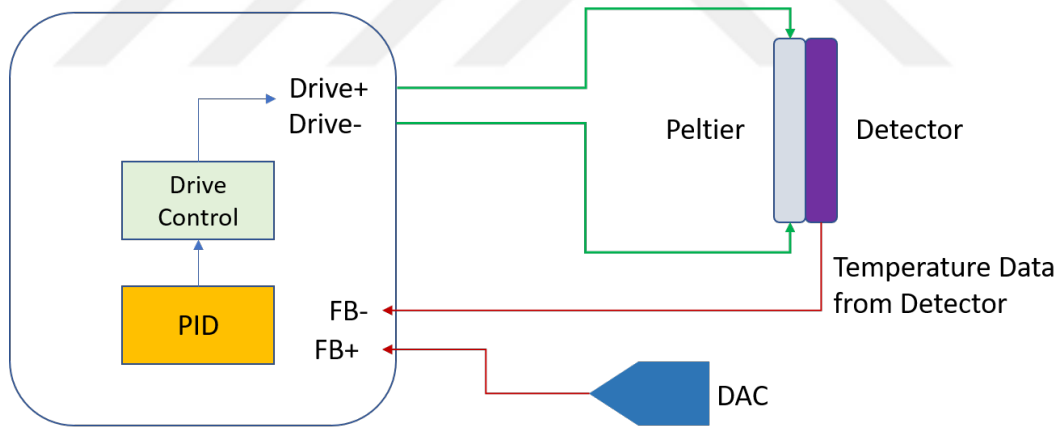


Figure 3.74: Designed thermo-electric cooling system

3.5.3 Thermal Response and Compensation

Once DAC output is set to a value which corresponds to a different temperature from sensor temperature, system adjusts peltier current. This means that the detector temperature is set by the DAC output. The behavior of the system during the temperature adjustment is called thermal response. Thermal response shows how fast or slow the system cools the detector along with how much overshoot

can happen at the detector temperature. Ideally, a fast thermal response without any overshoot is desired.

Thermal response of the system depends on the thermal schematic, temperature sensor, driver circuitry and the PID circuit. Out of them, PID circuit is the one, we can make adjustments to stabilize the system response. This is because other elements are hard to manipulate and changing their properties is both costly and time consuming.

Using DAC, step input with different frequencies within desired range is applied and temperature data from detector is observed and noted. PID parameters are changed until there is no overshoot and the system is fast enough for both cooling and heating. In figures 3.75 and 3.76 , orange curves show the TEC temperature and blue curves show the temperature value step input of adjusted by DAC. In figure 3.75, there is an overshoot that is not desired. After compensating the control loop the curve in figure 3.76 is reached. There is no overshoot and thermal response is slower but still it is fast enough to meet requirements.

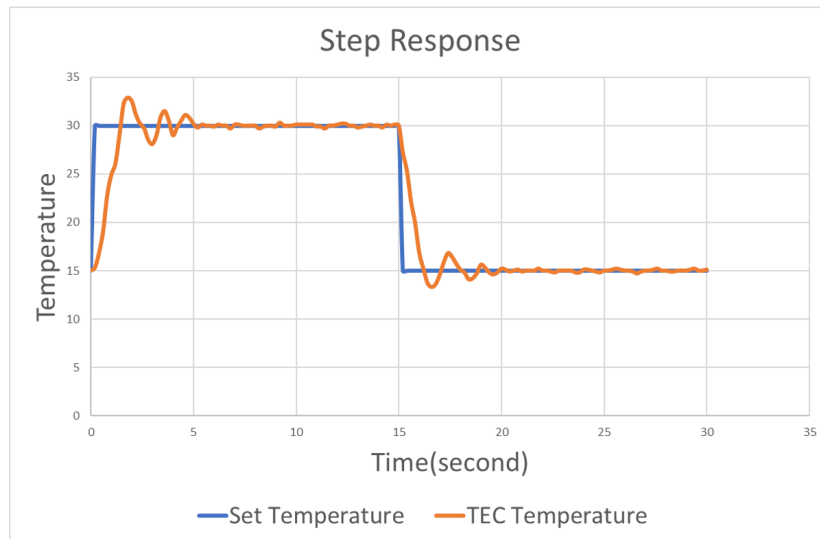


Figure 3.75: Step response of the thermal system before compensation

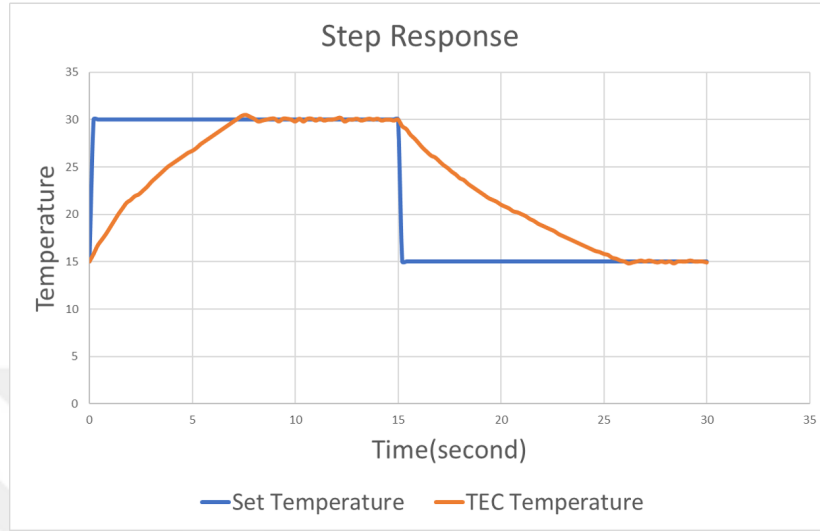


Figure 3.76: Step response of the thermal system after compensation

Other techniques can be employed for analysis and compensation of the thermal loop based on the IC being used. For the sake of simplicity, and to maintain system integrity this experimental method is quite useful and easy-to-implement.

3.6 Powering The System

The camera is required to work with a single 12V DC input. Keeping in mind that the system consists of many different elements with the special functions they take care of, they also need special care with powering. Each part has sub-elements with different working voltage and current demand. This reality brings up a new problem to be solved. Each part should be supplied properly according to their operating voltage and current demands using a single main power supply.

3.6.1 Voltage Regulators

There are mainly two type of regulators, linear regulators and switching regulators. It is very critical to understand each type's properties to satisfy system

requirements and achieve the highest possible system performance.

3.6.1.1 Linear Regulators

Linear regulator is the simplest type of regulator to regulate and control an output voltage that is delivered from a higher input voltage supply. They are used extensively in a wide variety of electronic applications across many different industries. They have both advantages and disadvantages, and the decision to use them in a system requires detailed knowledge about both properties of linear regulators and powering sensitivity of the targeted system.

Linear regulators work with an idea of voltage divider with a dynamic resistance to keep the output voltage at the desired value. Figure 3.77 shows the basic structure of a linear regulator. The feedback loop adjusts R1 in such a way that, VCC is always 3.3V no matter what the value of the load is.

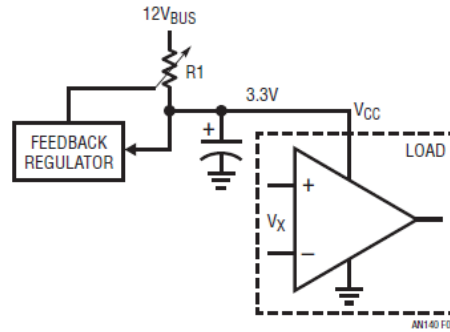


Figure 3.77: Feedback loop adjusts series resistor R1 value to regulate 3.3V [74]

Internal structure of a linear regulator is shown in figure 3.78. Instead of the resistor shown as R1 in figure 3.77, a transistor is used. The transistor works as a variable resistor in series with the output load. An error amplifier is used to sense the DC output voltage via a voltage divider resistor network, R_A and R_B. The divided portion of the output voltage, called the feedback voltage V_{FB} , is then compared with a reference voltage V_{REF} . The error amplifier's output, which is proportional to the difference between V_{FB} and V_{REF} determines

how much to drive the base of the series power transistor with the help of a current amplifier. In the case of a decrease in either the input V_{BUS} voltage or in the load current, the output voltage, V_{CC} , also decreases. The feedback voltage, V_{FB} , decreases as a consequence of the drop in the V_{CC} . Subsequently, the error amplifier's output increases causing the current amplifier to generate more current into the base of the power transistor Q1. The voltage drop V_{CE} is reduced and hence V_{CC} is brought back to be the output voltage, until V_{FB} equals V_{REF} . Conversely, if the V_{CC} output voltage goes up, in a similar way, the negative feedback circuit increases V_{CE} to establish the accurate regulation of the 3.3V output. In summary, any variation of V_O is detected and compensated by a feedback loop. Therefore, the output voltage V_{CC} always stays constant and regulated[74].

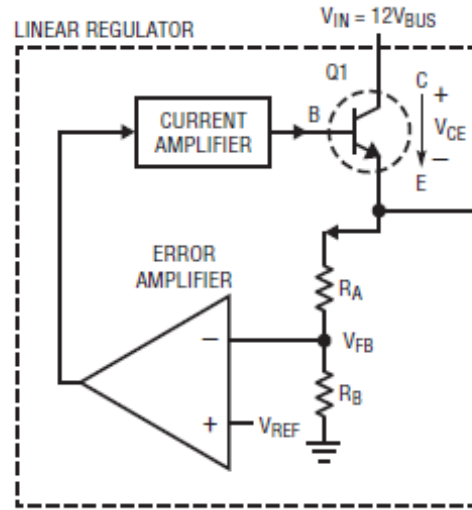


Figure 3.78: Internal structure of a linear regulator [74]

Nowadays LDO (Low Drop-out) is used as a synonym for linear regulators. But the reality is that, LDO regulators are special type linear voltage regulators with drop-out voltage (the differential between the input-to-output voltages needed to maintain regulation) typically below 600mV[75].

3.6.1.1.1 LDO Key Performance Parameters

3.6.1.1.1.1 Dropout Voltage

Dropout voltage is defined as the minimum input to output differential voltage which is required to maintain the output voltage within a small range, generally $\pm 100\text{mV}$ of the nominal value. In the dropout condition, the pass element operates in the linear region and behaves like a resistor. For the modern LDO, PMOS or NMOS FETs are used as the pass element, enabling the regulator to have a dropout voltage as low as 30mV to 500mV . Dropout voltage directly translates to efficiency of the regulator[76][77].

3.6.1.1.1.2 Power Supply Rejection Ratio (PSRR)

PSRR is a measure of the LDO's capability to smooth out and/or suppress input voltage fluctuations in the output voltage, as expressed in equation 3.21. PSRR must be taken into account throughout a broad frequency range because it is a frequency dependent performance metric[76]. When selecting an LDO, paying attention to specific frequencies of interest is critical. This is because of the fact that, the main aim may be to suppress a specific ripple or noise source.

$$PSRR = 20 \log \frac{V_{in}}{V_{out}} \quad (3.21)$$

Figure 3.79 shows a typical usage of LDO, ripple suppression of a switching DC-DC converter. Figure 3.79 also has an example PSRR plot vs frequency.

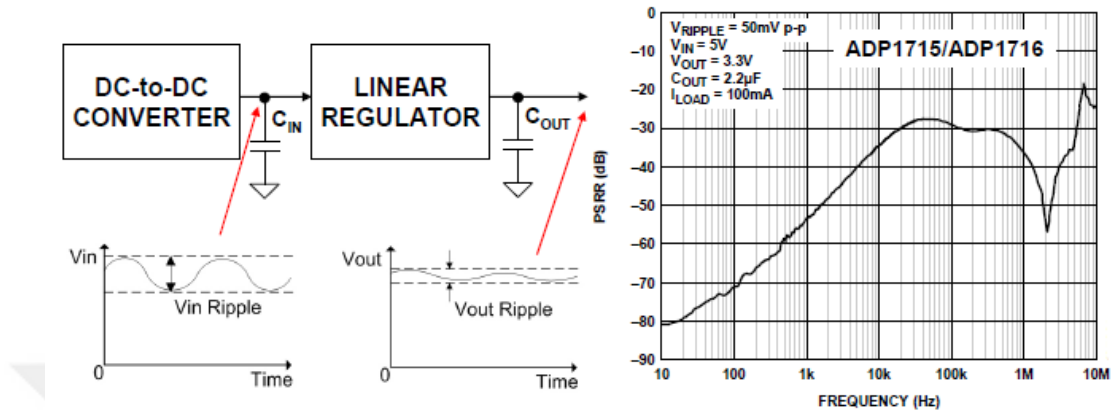


Figure 3.79: Input and output of an LDO regulator and an example PSRR vs frequency plot [77]

3.6.1.1.1.3 Noise

This parameter usually relates to the noise generated by the LDO itself on the output voltage, which is an intrinsic feature of the bandgap voltage reference within the LDO[76]. Noise directly affects the system that is powered by the regulator. Considering the PSRR of the system that is being powered within a specified range and the total noise within that range is a good starting point for regulator selection. Figure 3.80 shows an example noise plot for an LDO. It shows the total rms noise for a given band and its change with the output capacitor value.

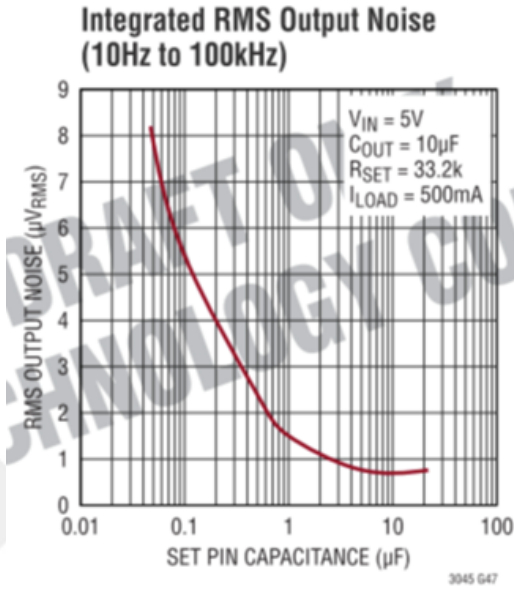


Figure 3.80: Output noise performance [75]

3.6.1.1.1.4 Quiescent Current

The quiescent current, also known as the ground current, of an LDO is composed of the bias current and drive current of the pass element, which are required to keep an LDO working. Normally, it is kept as low as possible because it is directly related with efficiency of the LDO. It is generally affected by the load but, when the pass element is either PMOS or NMOS FETs, amount of load current does not affect the quiescent current significantly[76][77].

Advantages	Disadvantages
Simple and easy to implement, Requires less external components, Generates low noise.	Efficiency is low, Generates heat, Output voltage should be lower than input.

Table 3.6: Advantages and Disadvantages of Linear Regulator [74][75][76] [77]

Considering the advantages and disadvantages, linear regulators are best when they are used in systems where;

- Drop-out voltage is small,
- Noise sensitive systems are powered,
- Current demand of the system is not high.

3.6.1.2 Switching Regulators

Switching regulators transfer energy from input to output via an inductor that has the voltage polarity across it switching at a fixed frequency. If the circuit elements are ideal, the input power equals the output power, and the converter is 100 % efficient[77]. Switching regulators can be named on the basis of their operation. Three most common switching regulators are buck converters, boost converters and buck-boost converters. Buck converter generates a voltage that is lower than its input whereas boost converter generates a voltage that is higher than its input. Buck-boost converter can generate output voltage that is both higher and lower than its input voltage. In the scope of this thesis, main concern is to reduce the input voltage and power sub-systems. So, the focus is on buck converters. Figure 3.81 illustrates the working of a buck converter.

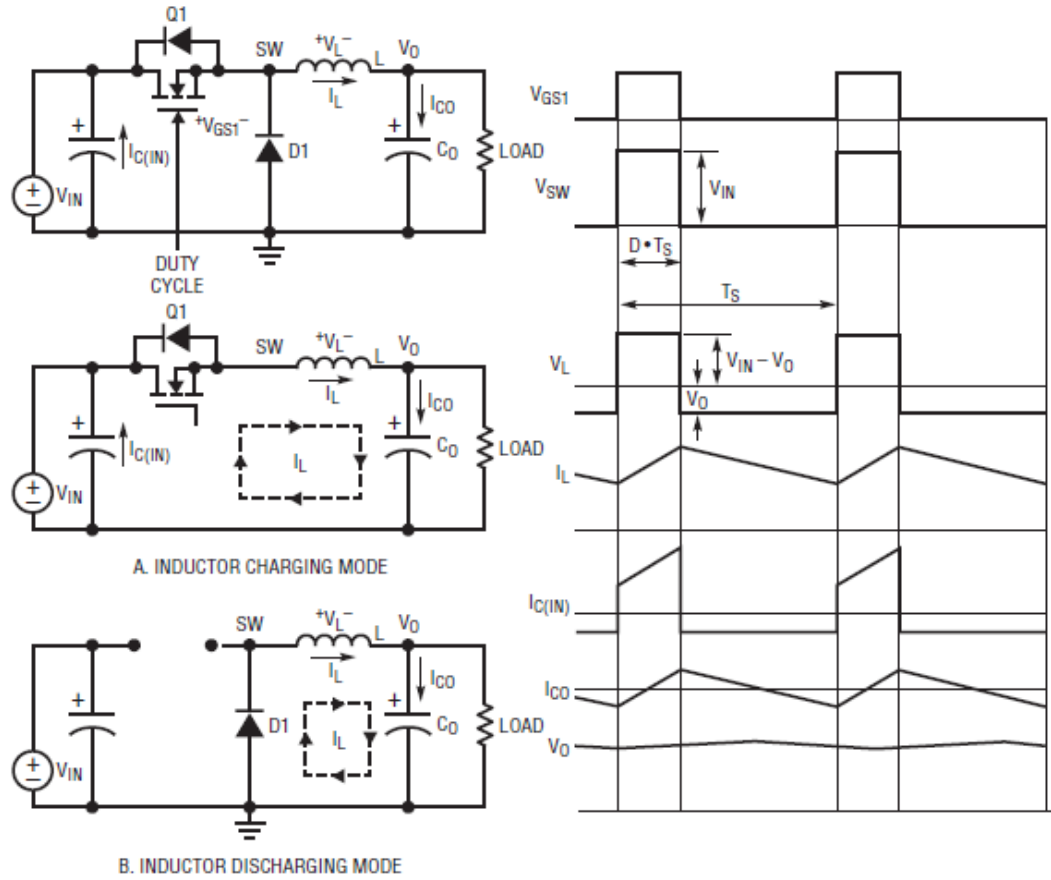


Figure 3.81: Buck converter operation [74]

The upmost figure shows the main components of a buck converter; a switch (a MOSFET), a diode and an inductor. There are capacitors both at the input and the output for storing charge and proper operation. When switch (transistor) Q1 is turned on, the switching node voltage $V_{SW} = V_{IN}$ and inductor current i_L ramps up with a rate proportional to $V_{IN} - V_O$. When switch Q1 is turned off, inductor current goes through the freewheeling diode D1, as shown in the figure at the bottom. The switching node voltage $V_{SW} = 0V$ and inductor current i_L ramps down with a rate proportional to V_O . Since the ideal inductor cannot have DC voltage in the steady state, the average output voltage V_O can be given as:

$$V_O = \frac{T_{ON}}{T_S} \times V_{IN} \quad (3.22)$$

Where T_{ON} is the duration switch is conducting and T_S is the period of switching.

Switching regulators are complex to design and require special care. Ideally they are 100 %, however, in real life applications that is not the case. Non-idealities of the switch, inductor, diode and input/output capacitors reduces the percentage of efficiency. They are good at supplying large amount currents, but since they generate a lot of ripple, they are not favored in noise sensitive applications. A solution to this is using a linear regulator as an active filter at the output of a switching regulator as shown in figure 3.82.



Figure 3.82: A linear regulator as an active filter at the output of a switching regulator [79]

Advantages	Disadvantages
Used for voltage increase, decrease and inversion, Highly efficient, Dissipates lower power and generates less heat.	Complex and costly design, Generates noisy output, More components needed.

Table 3.7: Advantages and disadvantages of switching regulators

Switching regulators also have both cons and pros. They are best when they are used for systems where;

- Drop-out voltage is large,
- Efficiency and heat generation is a concern,

- Large amount of current is needed,
- Cost and area is not a concern.

3.6.2 Voltage Regulation Planning

After review and study of linear and switching regulators, the best solution is designing a voltage regulation system with a hybrid structure, where both linear and switching regulators are used for their purposes. The ultimate voltage regulation plan is shown in figure 3.83.

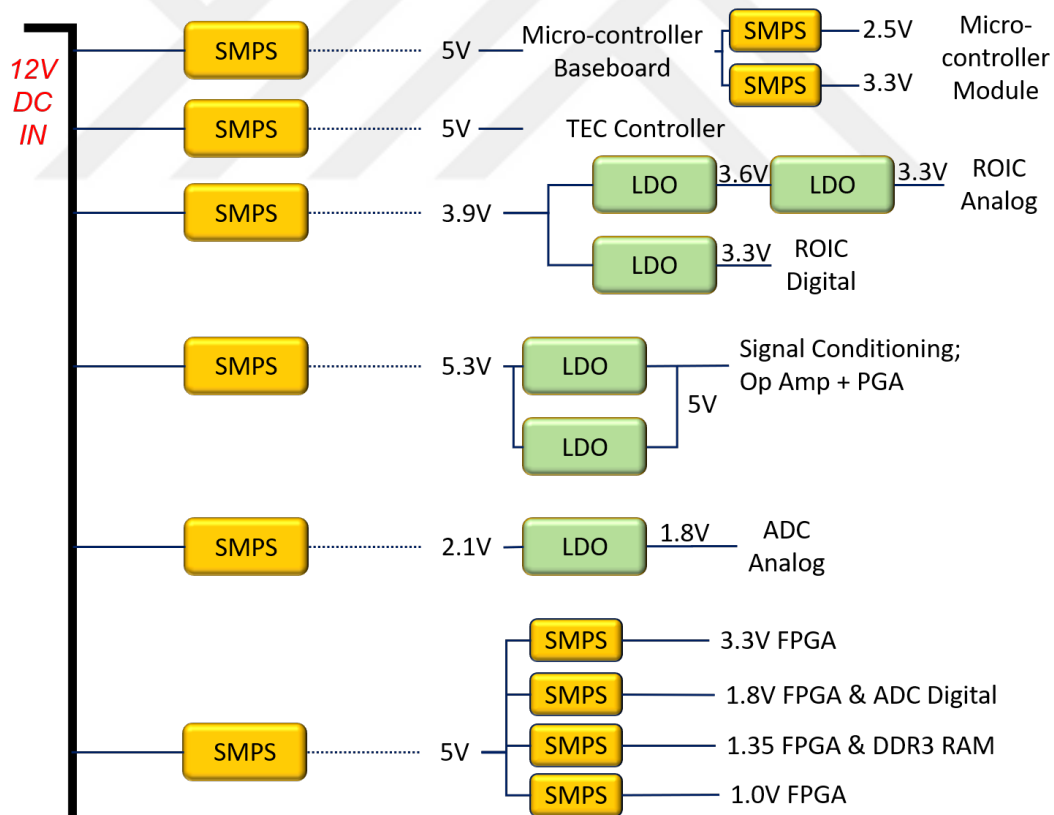


Figure 3.83: Voltage regulation schematic for powering the camera

SMPS stands for *Switch Mode Power Supply* whereas LDO is used for *Low Dropout* linear regulators. Switching regulators are used for large dropout voltage

conversions. If the part to be supplied is not a noise sensitive part and requires large amount of current, SMPS directly supplies them. But for noise sensitive parts, large dropout conversions are carried out with SMPS whose output is then filtered actively with an LDO regulator. In some parts, LDOs are used in cascade for increased filtering. Moreover, paralleling of LDOs is also practiced with an aim to provide more current and lower noise. Paralleling LDOs also helps in spreading heat [75].



Chapter 4

Hardware Implementation

In chapter 3, the electronics that are required to make the camera work is reviewed. Required electronic circuits are designed and simulated, system solutions are proposed.

In this chapter the main concentration is on realizing those electronic circuits and solutions on PCBs (Printed Circuit Boards). Detailed study of PCB design procedures are carried out to learn the ropes of the subject. Finally fabricated PCBs are demonstrated.

4.1 PCB Design Core Knowledge

PCBs are very critical instruments to bring electronic circuits to life. Very carefully designed analog or digital circuits may fail, if the PCB is not designed properly. PCB design concept is surely much more than bringing integrated circuits closer and connect related pins with copper traces. This can be summarized with a quote from Dr. Eric Bogatin, not exactly but with a meaning “Everything in schematic is perfect, the way layout is implemented deteriorates performance. Best layout practice is aiming for as less deterioration as possible.”.

In high-speed products, both physical and mechanical design have impact on the performance of the system. To specify a product as high-speed, looking at the highest clock frequency and deciding accordingly is not a good approach. Rise time and fall time of the output of the integrated circuits play a more critical role. Even though the highest clock frequency in a system is in the order of kHz, rise and fall times at the order of nanoseconds may cause it to be called a high-speed system. Rise and fall times of a specific IC may be updated in years. As transistor sizes continue to shrink and IC vendors try to put more dies on a single wafer to reduce overall cost, rise and fall times continue to shrink too. This may result in a situation where the same IC does not work properly with the same hardware design it used to [87]. For this reason, caring every design as if it is a high-speed product is a nice approach for a decent and unproblematic hardware design.

If a system is designed without good care, lots of problems arise due to interconnects within a PCB. All of the problems can be categorized under three main concepts each of which have considerable overlap with two others;

- **Signal Integrity(SI)** considers distortion of the signals,
- **Power Integrity(PI)** concentrates on the noise on the interconnects and any associated components delivering power to the active devices,
- **Electromagnetic compatibility(EMC)** can be described as the contribution to radiated emissions or susceptibility to electromagnetic interference from fields that are caused by external products.

Throughout the design process, all the three aforementioned performance issues need to be taken into account for a successful hardware product [87].

As a summary, designing for EMC includes good SI and PI design practices along with additional concepts such as cabling, shielding and connectors. PI is mainly about problems associated with power distribution network (PDN) which encompasses all connections (including vias, planes, wirebonds, die pads,

PCB pads and IC packages) and components from voltage regulator modules (VRMs) to power rail on a chip die. Signal integrity signifies the signal's ability to propagate without distortion. Signal integrity is nothing but the quality of the signal passing through a transmission line[87][88].

4.1.1 Common SI/PI/EMC Problems

There are lots of problems related caused by poor design practices. They can be categorized under six unique families.

4.1.1.1 Signal Distortion on One Net

Reflection is solely caused by a change in the impedance seen by the signal. A signal propagates from the driver to load being affected by the impedance on the net. If there is a discontinuity of impedance in the net, signal is reflected causing the distortion. Some of the reasons of discontinuity are as follows; unterminated end of interconnect, abrupt change in trace width causing a change in the impedance, a layer change with a via, a gap in a return plane, a connector and routing topologies like branching, tee and stub.

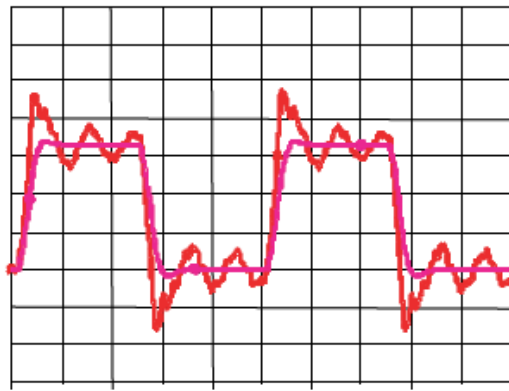


Figure 4.1: Ringing due to an unterminated line and signal with good quality with proper termination [87]

There are also timing problems caused by the signal propagation. The time delay between two signal paths is called skew. If a signal and a synchronized clock have skew different than expected, false triggering and errors can happen. Especially if there is a skew between differential signals, some of the differential signal is converted into common mode signal causing a distortion[87].

4.1.1.2 Crosstalk

A signal on one net may couple into an adjacent signal net because of a few reasons. Even though the signal quality in the first net, which is called aggressor, is perfect, the coupled portion of the signal may appear as noise in the second, victim signal. One reason is that two signals' return current paths overlap with each other to some extent. That is generally referred as the mutual inductance. The higher the mutual inductance two nets have, the bigger the rate of crosstalk becomes[87].

4.1.1.3 Ground and Power Bounce

Ground and power bounce is a special case for crosstalk. Supply and ground bounce are the shifts in the supply and ground rails on the integrated circuit (IC) die with respect to their respective levels on the planes of the PCB. Any noise that is injected into the supply and ground path can appear at the logic inputs and outputs[89].

4.1.1.4 Loss

Loss at high frequencies is also referred as frequency dependent loss. This is caused by the dielectric's frequency dependent property. In such cases, high frequency components of a signal is attenuated more than the low-frequency components yielding a distorted signal. That is a special case for signal distortion on one net[87].

4.1.1.5 Rail Collapse, Voltage Droop, Power Supply Noise

Noise is not a problem for only signal paths. In power and ground distribution networks which feed each chip, it becomes more important and it can even lead to disastrous results.

Power distribution network (PDN) is a reason for jitter. The propagation delay for the turn-on of a gate is directly related with the voltage between source and drain. Bringing voltage to the gate slower causes a delay and accounts for the main source of jitter.

Reactive elements in PDN, especially along with parallel resonances cause high voltage spikes due to switching power currents. This results in enhanced jitter which then leads to bit errors and false triggering.

Poorly designed PCBs have unevenly distributed high impedance PDN profile, which produces voltage drops across it when current flows.

All of the problems that are mentioned contribute to power supply noise and they are sources of performance degradation [87].

4.1.1.6 EMI

With board-level clock frequencies in the 100-MHz to 500-MHz range, the first few harmonics are within the common communications bands of TV, FM radio, cell phone, and personal communications services. This means that there is a very real possibility of electronic products interfering with communications, unless their electromagnetic emissions are kept below acceptable levels.

There are three things that combine and create an EMI problem; a noise source, a pathway to radiator and an antenna that serves as radiator.

Every problem that is related with SI and PI generally becomes a source for EMI problem. However, sometimes noise levels can be so low to meet SI and PI

criteria but still can cause EMI problems. That is the most challenging nature of EMI problems.

The two most common sources of EMI are the conversion of some differential signal into a common signal, which eventually gets out on an external twisted-pair cable, and ground bounce on a circuit board generating common currents on external single-ended shielded cables, which are also signs of having SI and PI problems. Additional noise can also come from internally generated radiation leaking out of the enclosure[87].

4.1.2 Good PCB Design Practices

Before learning how to apply good PCB design practices, fundamental concepts about signals and their propagation should be understood thoroughly. Once they are learned properly, the proposed techniques make more sense and become more applicable.

First of all, energy in a PCB is neither in the voltage nor in the current. Energy is entirely in fields, either electric or magnetic. The fields are located in the space between the traces and their references, in the dielectric. In other words, energy in a PCB travels in the fiberglass material. We call this energy, in a transmission event, as called electromagnetic wave. The copper traces that are routed are used to steer the electromagnetic wave from one point to another. For this reason, these copper elements can be perceived as wave guides[87][90].

Transmission lines are wave guides, composed of a pair of conductors or wires to move energy from one point to another by steering the electromagnetic waves. There are lots of ways of realizing transmission lines on a PCB. The most commonly used ones are stripline shown in figure 4.2 and microstrip in figure 4.3.

Stripline (Inner layer trace and return planes) -

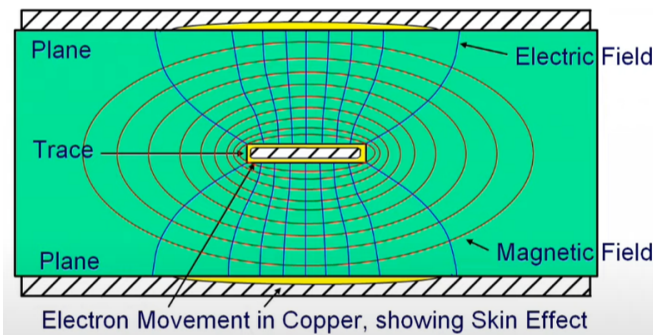


Figure 4.2: Stripline transmission line with electric and magnetic fields coupled to reference planes [90]

Microstrip Line (Outer layer trace and return plane) -

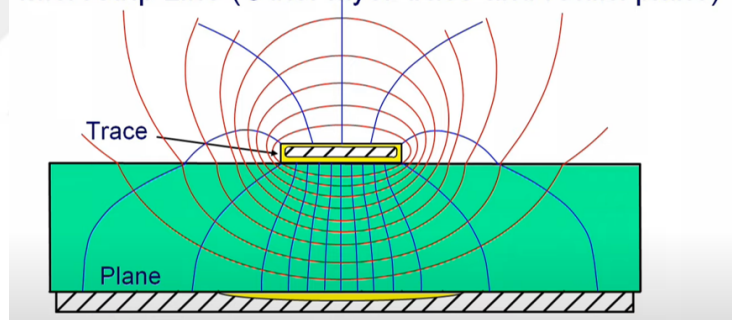


Figure 4.3: Microstrip transmission line with electric and magnetic fields coupled to reference plane [90]

Figure 4.4 illustrates a signal and its return. According to Kirchhoff's Law, all currents return to their sources using the path of least impedance. For DC currents this is the shortest path, but for higher frequencies ($>10\text{kHz}$) return current path is directly under the trace (Return currents of high frequency signals are illustrated in figures 4.2 and 4.3 with yellow in reference planes). This is due to the fact that, inductance dominates over resistance at higher frequencies.

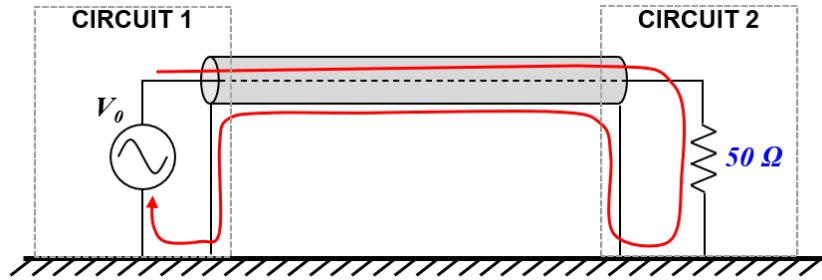


Figure 4.4: A signal traveling to the load and returning using the least impedance path [91]

4.1.2.1 PDN Engineering

A PDN consists of all the interconnects in the power supply path from the voltage regulator modules (VRMs) to the circuits on the die. These interconnects mostly include the power and ground planes in the boards, cables, connectors, and all the capacitors that are related with the power supply [98].

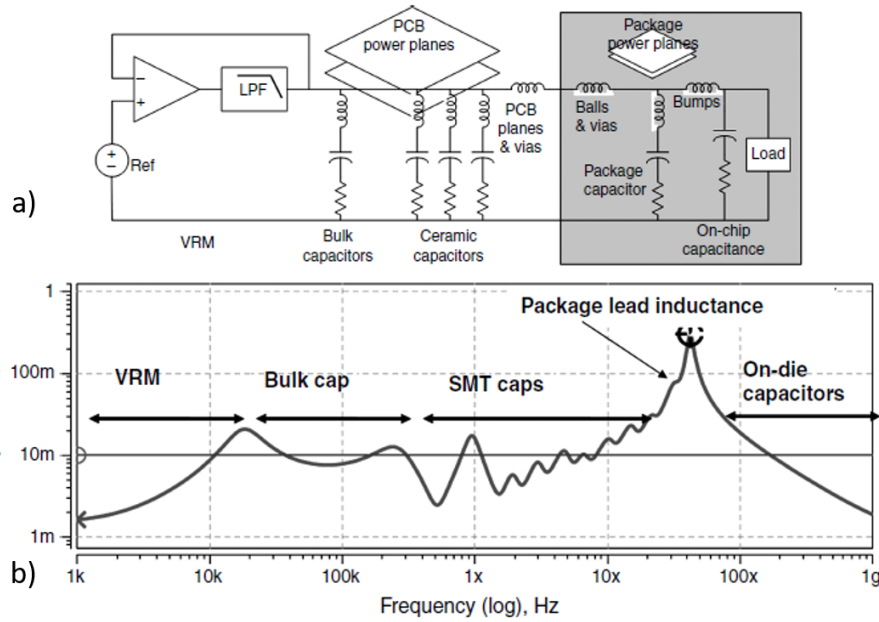


Figure 4.5: a) Simplified schematic of the PDN ecology showing the main elements
b) Resulting impedance profile identifying how specific design features contribute to specific impedance features (X stands for MHz) [98]

The non-idealities of the interconnects, capacitors and voltage regulator modules create extra parasitic elements as shown in figure 4.5. This overall creates an impedance profile from the supply to the power pads of the IC die. High impedance values are not desired since they cause high voltage drops when large amounts of current is supplied. Setting a specific target impedance and designing to have a lower impedance than the target is called PDN engineering.

4.1.2.1.1 Decoupling Capacitors

In real life, capacitors have some resistance and some inductance due to packaging and PCB pads. Because of this non-ideality, they begin to behave like inductors after a certain frequency, called resonance frequency as shown in figure 4.6 for different valued of capacitors.

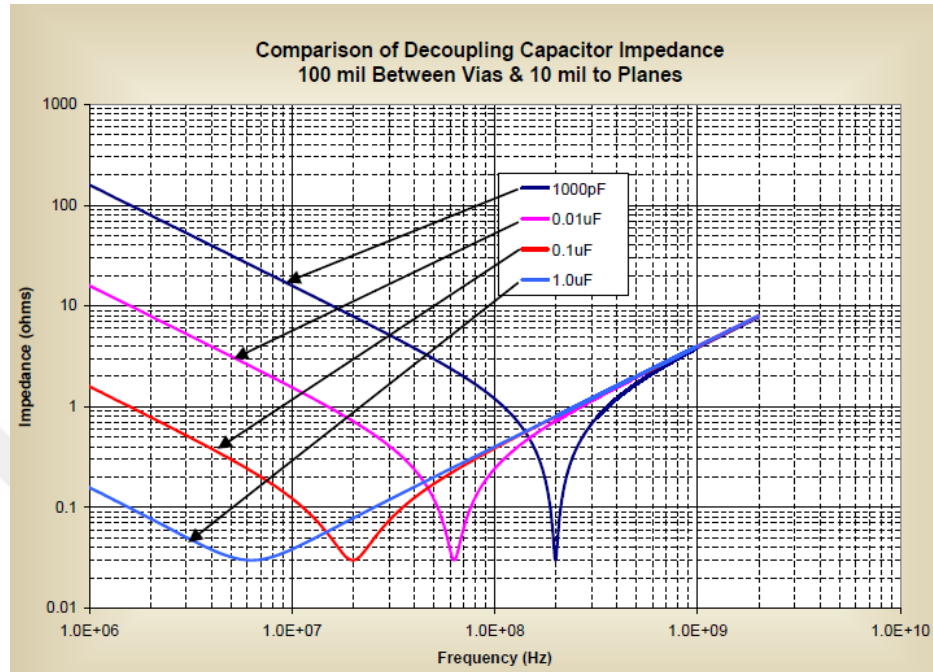


Figure 4.6: Impedance profile of different valued capacitors [95]

Using all of the capacitors whose impedance profiles plotted separately in figure 4.6, yields a wide band low impedance profile as shown in figure 4.7. This is a commonly used method for PDN engineering.

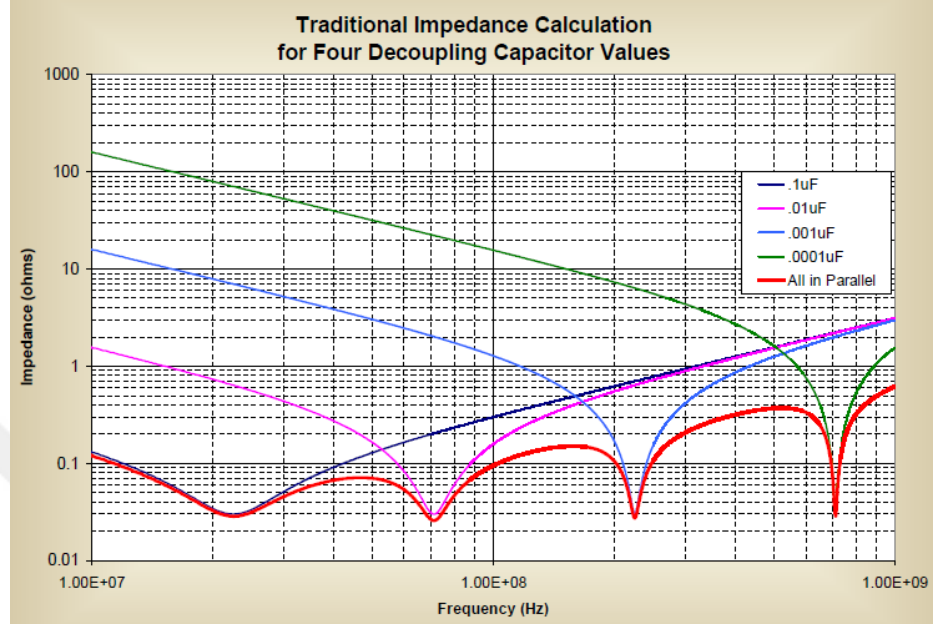


Figure 4.7: Impedance profile of different valued capacitors and their parallel combination [95]

The main target using decoupling capacitors is lowering the resulting inductance. So, their placement also plays a critical role. Placing capacitors directly under the IC may result in a bigger loop, which then causes a bigger inductance as shown in figure 4.8. For this reason, it is better to analyze how to minimize loop inductance for a good design.

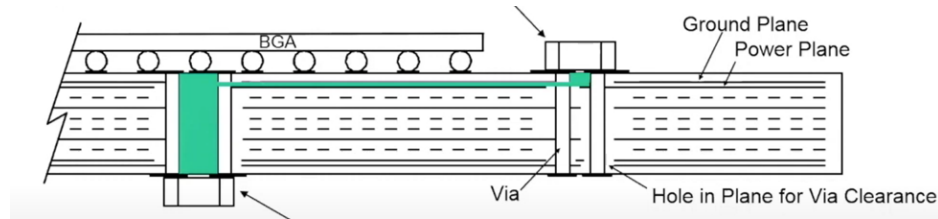


Figure 4.8: Capacitor placement and resulting loop inductance; overall loop area is shown in green for two different capacitor placement [99]

Moreover, while connecting decoupling capacitors' pins to ground and power planes, using multiple vias reduces overall inductance. However, location of vias also affects performance. In figure 4.9b, a better via placement is conducted since

vias of power and ground lines are closer to each other reducing the overall loop inductance.

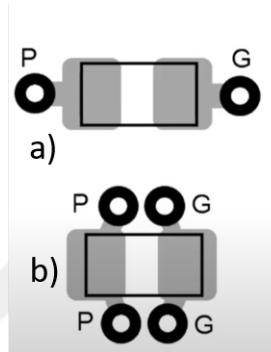


Figure 4.9: Via placement for decoupling capacitor. Configuration in a) yields higher inductance than the configuration in b)[99]

Another method that is used for engineering the PDN is the interplane capacitance. Interplane capacitance is formed by power and ground layers closely spaced with the PCB dielectric substrate. The closer the power and ground layers are, the higher the interplane capacitance gets. Interplane capacitance generally has a much lower capacitance than decoupling chip capacitors. But they have lower resistance and inductance as well. This property makes them very useful to be used with ICs that are switching at very high frequencies. Using partial planes on different layers to increase overall area also increases the resulting interplane capacitance.

4.1.2.2 Transmission Lines

While designing transmission lines, the most critical design concept is keeping their impedance fixed from the driver (source) to load. This avoids reflection and distortion to a great extent. Ensuring the coupling of fields to reference plane and splitting signals from each other reduces the risk of crosstalk.

There can be signal groups that need to be synchronized. The synchronization can be achieved by matching the propagation delay between nets.

4.1.2.3 Vias

Vias are used to change trace's layers in PCBs. Vias should be treated in such a way that they maintain the integrity of the transmission line. In figure 4.10, a signal goes from layer one to layer four. Layer two and layer three are reference planes. Normally the energy is in the dielectrics between layer 1 and 2, and 3 and 4. The via needs to have a reference to keep the energy. Placing a ground via near the signal via solves this problem. Otherwise, the energy spreads within the dielectric interacting with other signals' fields and thus causes distortion.

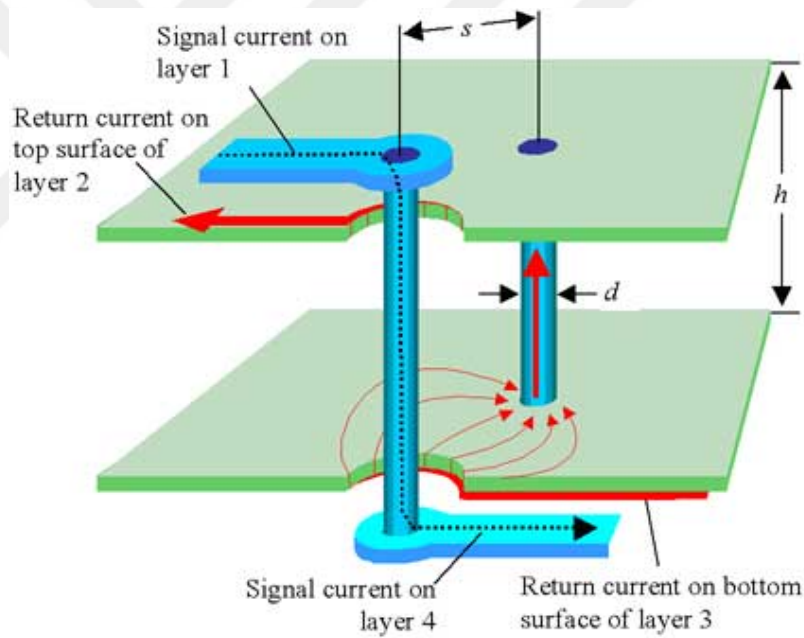


Figure 4.10: Signal currents with their return currents [92]

Another problem with the vias is that, while changing layers there may be unused parts of vias that distort the signal by acting like a stub as shown in figure 4.11. There are a few solutions for this situation. Blind and buried vias, in which there are no unused parts can be used. But, production of these vias are complicated and including them in the PCB increases the production cost. Another method is named as backdrilling. In this method, the excess metallization of the via is removed by a drill as shown in figure 4.12. This is a cheaper method,

but designer needs to be aware of the manufacturer's capabilities.

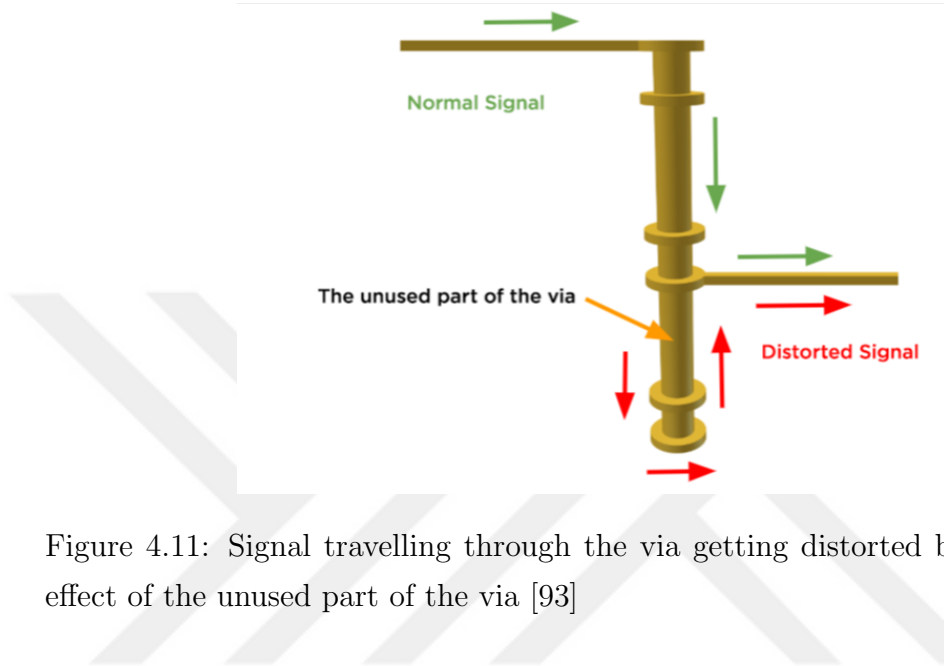


Figure 4.11: Signal travelling through the via getting distorted by the sub-like effect of the unused part of the via [93]

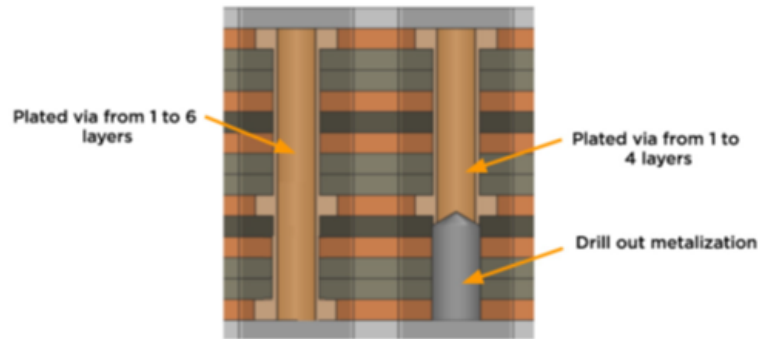


Figure 4.12: The excess part from layer 4 to 6 is drilled out to get rid of stub [93]

4.1.2.4 Mixed Signal PCB Design Considerations

Mixed-signal PCBs house both noisy digital signals and sensitive analog components together. This reality brings a responsibility to design carefully. The most important step is partitioning the board correctly for digital and analog parts. The PCB should have a single, unbroken ground plane as return path for both analog and digital components. Splitting planes and allocating them for digital

and analog parts separately is not a good design approach. However, analog and digital parts should be separated as shown in figure 4.13. Everything analog should be kept in analog section, and similarly, everything digital should be kept in digital section. Analog and digital sections should be separated from each other with at least $20H$ distance, where H is the thickness of dielectric between signals and their reference plane. Such practice keeps return paths of analog and digital signals away from each other, avoiding crosstalk.

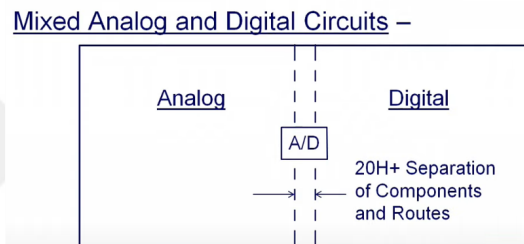


Figure 4.13: Floor-planning of mixed signal boards [90]

Digital and analog components should be supplied from different power supplies placed on their targeted sections. This prevents switching noise of digital components from coupling to analog signals.

4.1.2.5 Stack-up Design

Stack-up design is the beginning of a PCB design. After careful planning and analysis, number of layers to be used needs to be determined. Following that, each layer should be assigned to specific signals and planes to realize targeted impedance values and design practices. Most manufacturers have custom stack-ups to be used. They are generally cheaper and since the manufacturer optimized its production, there is less possibility of failure due to PCB manufacturing. Custom stack-ups can also be used for better performance if the need arises. Figure 4.14 shows how the signal traces and reference planes are allocated at different layers. For a good stack-up planning, all signals and power planes should be put on layers where can directly reference to ground planes.

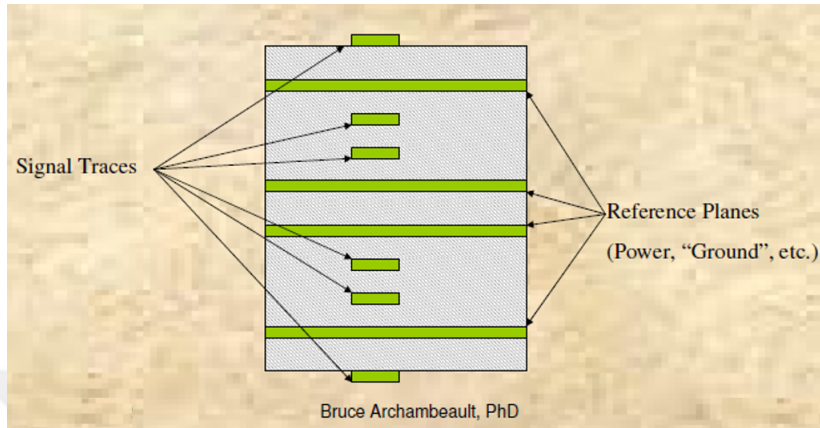


Figure 4.14: Stack-up planning with traces and reference planes in a multi-layer PCB [94]

4.1.2.6 Dielectric Substrate Selection

PCBs are mainly composed of copper conductors and dielectrics between them. Dielectric material is very important, because that is the medium where electromagnetic wave propagates. Typical PCB dielectric (core/prepreg) substrates are constructed from various woven fiberglass fabrics strengthened and bound together with epoxy resin. Figure 4.15 shows different types of fiber weaves that are used in lamination to constitute the dielectric substrate. The numbers next to each diagram identify the glass fabric style based on the fiberglass thickness, pitch, warp yarn, fill yarn, and the number of glass fiber strands used[96].

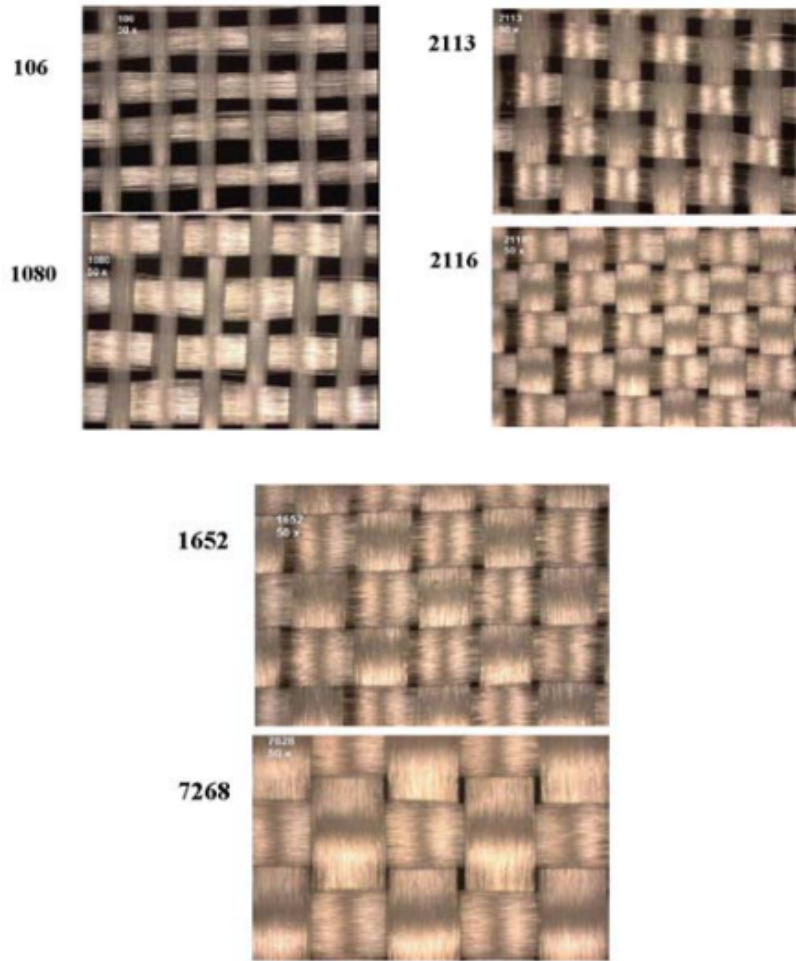


Figure 4.15: Different types of fiber weaves [96]

Figure 4.16 shows a differential line on a specific type fiber weave. The problem here is that, the effective dielectric constant seen by each pair is different from each other. For different signals which need to be synchronized, this can cause problems since each of them have a different propagation delay. To overcome this problem either the 7268 type, which has a uniform effective dielectric constant, can be selected or different types of routing, for example diagonal routing to equalize effective dielectric constant can be implemented.

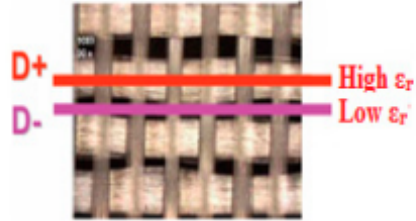


Figure 4.16: Differential pair on a specific fiber weave [97]

4.2 Designed PCBs

In 4.1 and 4.1.2 theoretical background about PCB design, common problems associated with PCB design and good PCB design practices are reviewed. PCBs that hold the required circuits for system operation are designed in the light of information gathered in 4.1.

4.2.1 Image Sensor Carrier PCB

This PCB is designed to make a connection between the image sensor and the rest of the system. The pads of the ROIC is connected to this PCB via wirebonds. Wirebonds are made on the gold finished openings on the PCB. The designed PCB and its stack-up plan are shown in figure 4.17.

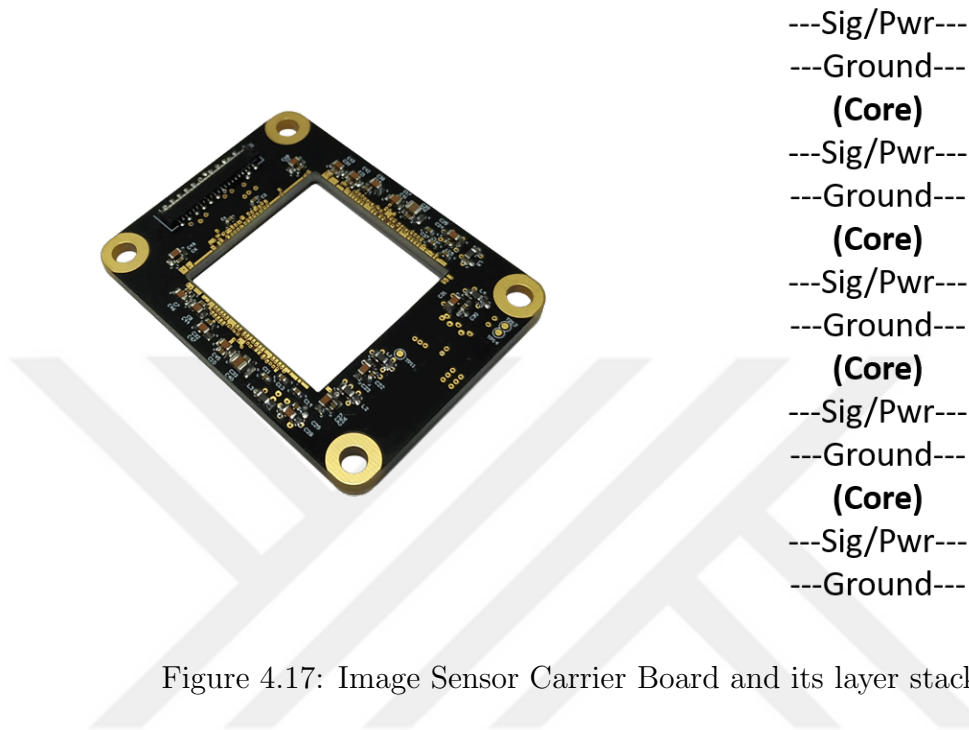


Figure 4.17: Image Sensor Carrier Board and its layer stack-up

4.2.2 Analog Signal Conditioning Board

This PCB is designed to hold the op amps and FDAs of the analog front end circuitry. Layout is optimized carefully by employing analog layout techniques. Analog Signal Conditioning Board and its stack-up plan are shown in figure 4.18

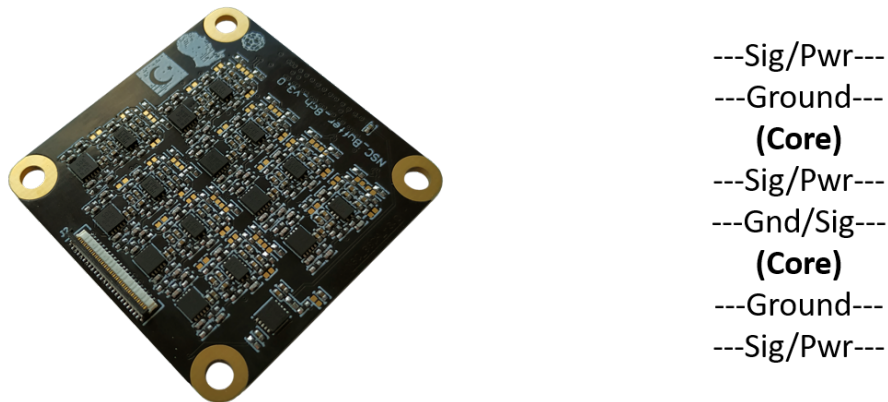


Figure 4.18: Analog Signal Conditioning Board and its layer stack-up

4.2.3 FPGA Board

This PCB is designed to house ADC of the analog front end circuitry and FPGA along with other digital ICs such as DDR3 and flash memory. Analog signals from the Analog Signal Conditioning Board are fed into the ADC via a flat-flexible cable. FPGA Board is shown in figure 4.19 and its stack-up plan is shown in figure 4.20.

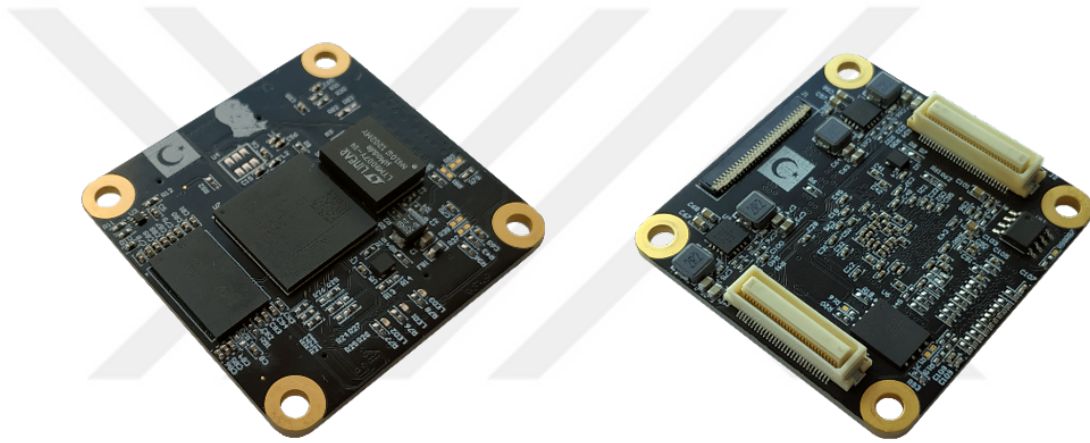


Figure 4.19: FPGA Board

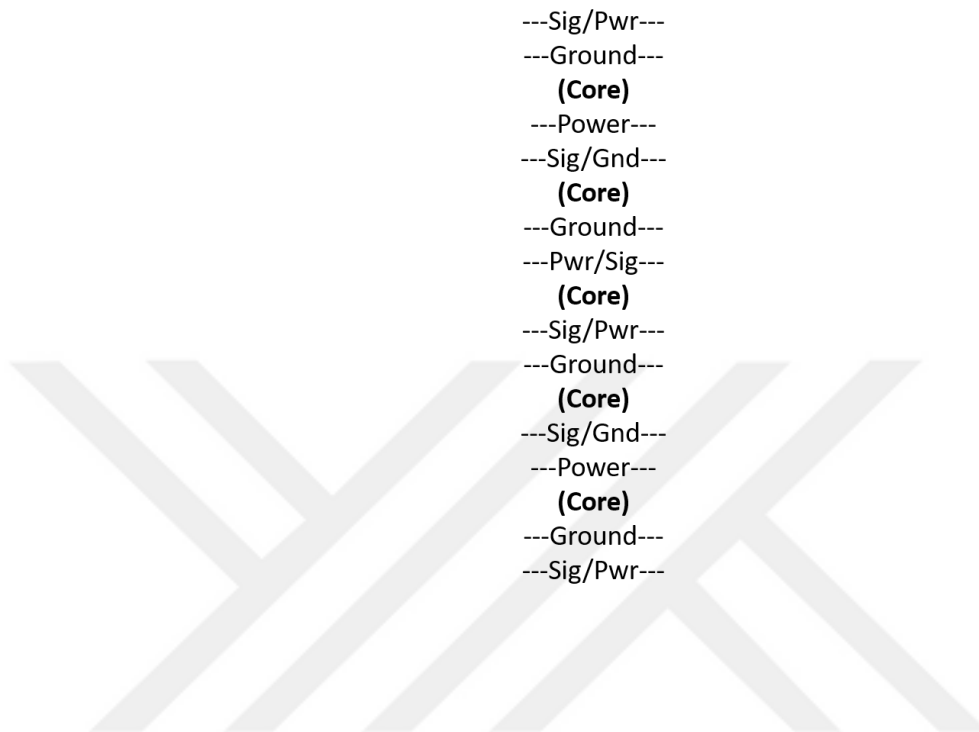


Figure 4.20: Stack-up for FPGA Board

4.2.4 Power and Thermal Regulation Board

This PCB has the voltage regulators for the targeted voltage regulation plan and the thermoelectric cooler control circuitry. The PCB and its stack-up are shown in figure 4.21

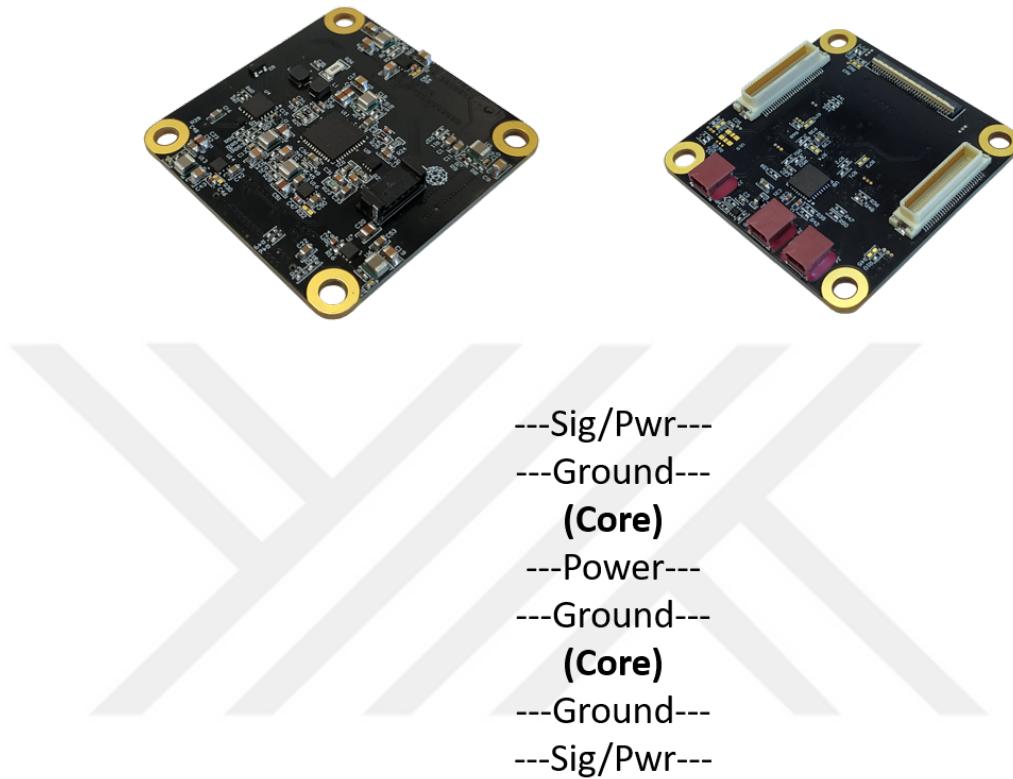


Figure 4.21: Power and Thermal Regulation Board and its layer stack-up

Connections to power supply and peltier element are established with the help of durable surface-mount connectors.

4.2.5 Micro-controller Baseboard

Micro-controller Baseboard supplies selected micro-controller module with power, holds memory elements for booting and storage purposes and transformers for Ethernet line driving. The PCB and its stack-up are shown in figure 4.21



---Signal---
 ---Ground---
(Core)
 ---Sig/Pwr---
 ---Ground---
(Core)
 ---Sig/Pwr---
 ---Ground---
(Core)
 ---Signal---
 ---Ground---

Figure 4.22: Micro-controller Baseboard and its layer stack-up

4.3 Mechanic Design

The mechanic design is finished to hold all the PCBs together. The mechanic itself is also heat sink for all PCBs. The robust structure protects the electronic circuits from environmental effects such as humidity, water, shock and vibration. Mechanical design with the PCBs is shown in figure 4.23 and the manufactured overall camera is shown in figure 4.24.

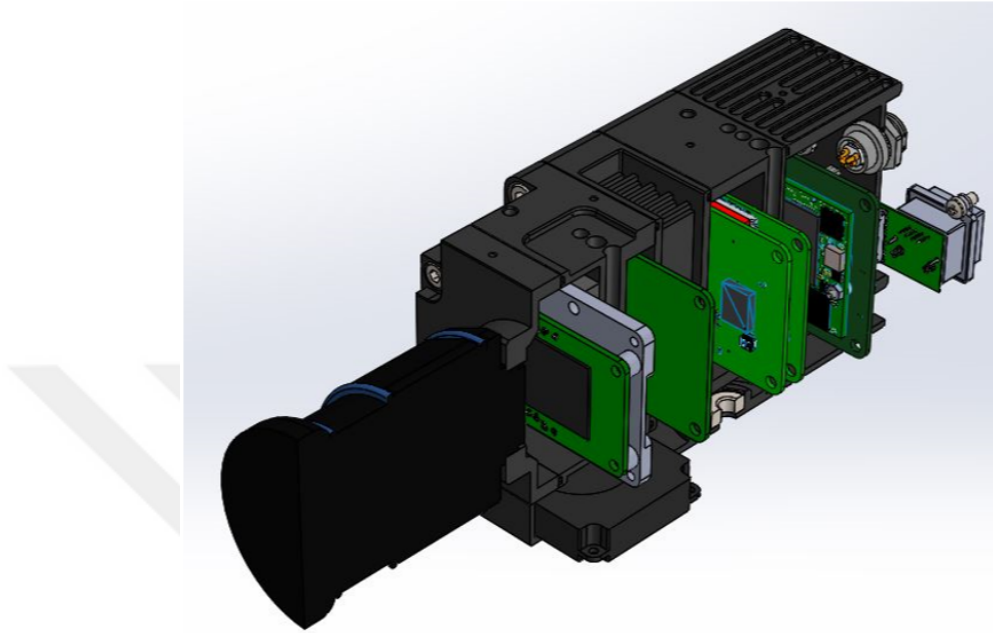


Figure 4.23: Mechanical design to house PCBs



Figure 4.24: Manufactured mechanic with working PCBs inside

Chapter 5

System Characterization

After the completion of hardware development, its characterization needs to be done. In order to characterize the system, a user-friendly PC GUI is used.

In this chapter, brief explanation of the PC GUI and image correction methods is given. After that, test setups and test results are demonstrated to show that the design requirements are met.

5.1 PC GUI

A PC GUI is used to display the acquired image and manage the controls of the system. The main screen of the PC GUI is shown in figure 5.1

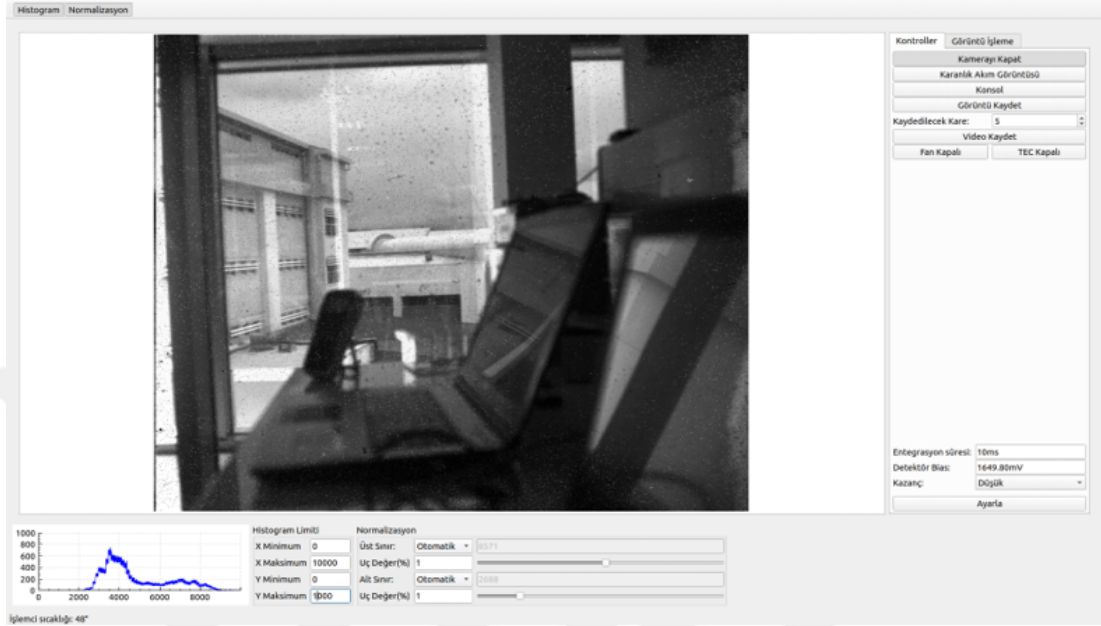


Figure 5.1: PC GUI main screen

On the bottom left of the main screen, a histogram of the acquired image is given and updated at every second. On the right hand side, there are control buttons for detector bias and integration time adjustment, detector temperature setting and acquiring calibration data.

PC GUI has paramount importance with the convenience it brings during characterization of the camera thanks to special functions it has.

5.2 Image Correction Techniques

5.2.1 Defective Pixel Correction

The detector array that is manufactured at NANOTAM has about 1.3 million pixels. It is impossible for all of them to function perfectly. It is inevitable that all of the pixels do not respond to incident light as they are supposed to. Location of the defective pixels are detected by acquiring dark and light images.

The data to be displayed at the location of the defective pixels are always updated by a corrected pixel value instead of the defective pixel value. There are options that offer different methods of correction such as median filtering, averaging of the neighboring pixel values or using the neighboring pixel values directly. The method to be used is adjusted according to application or properties of the manufactured detector. In figure 5.2 an image area with defective pixel and its corrected versions are shown.

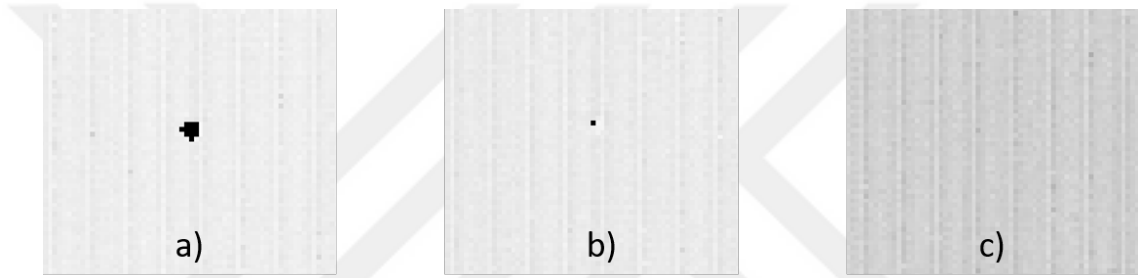


Figure 5.2: Dead pixel correction; a) no correction b) 3x3 pixel square corrected c) 3x3 pixel square corrected

5.2.2 Non-Uniformity Correction(NUC)

As mentioned, the detector has about 1.3 million pixels and all of them do not respond to incident light equally. That reality is called as non-uniformity and can be overcome by applying non-uniformity correction.

To implement non-uniformity correction, light (When there is full illumination) and dark (When there is no illumination) images are acquired under different temperature and exposure conditions. Behavior of each pixel, an offset value and a gain value they have, are detected. Each pixel is corrected with the equation given in equation 5.1 and corrected output is sent out to be displayed. In the equation, p_i is the raw pixel value to be corrected, d_i the value of the dark pixel, l_i is the value of the light pixel, g is the adjustable gain value and $\bar{p}_i$ is the corrected pixel value to be displayed.

$$\bar{p}_i = \frac{(p_i - d_i) \times g}{(l_i - d_i)} \quad (5.1)$$

Figure 5.3 shows an indoor scene that was captured by NANOTAM SWIR Camera without NUC and figure 5.4 shows the same screen with NUC. Also in figure 5.5 defective pixel correction methods were employed after NUC.

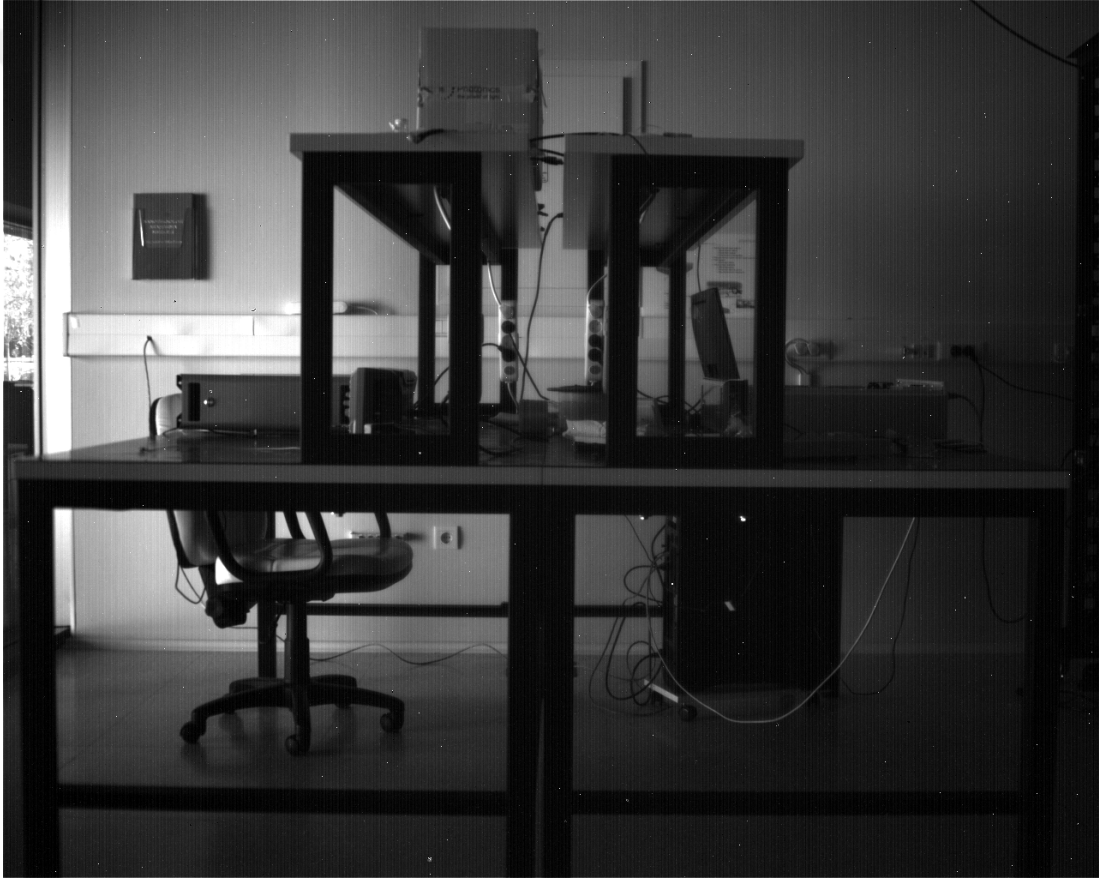


Figure 5.3: An indoor scene captured with NANOTAM SWIR Camera without NUC

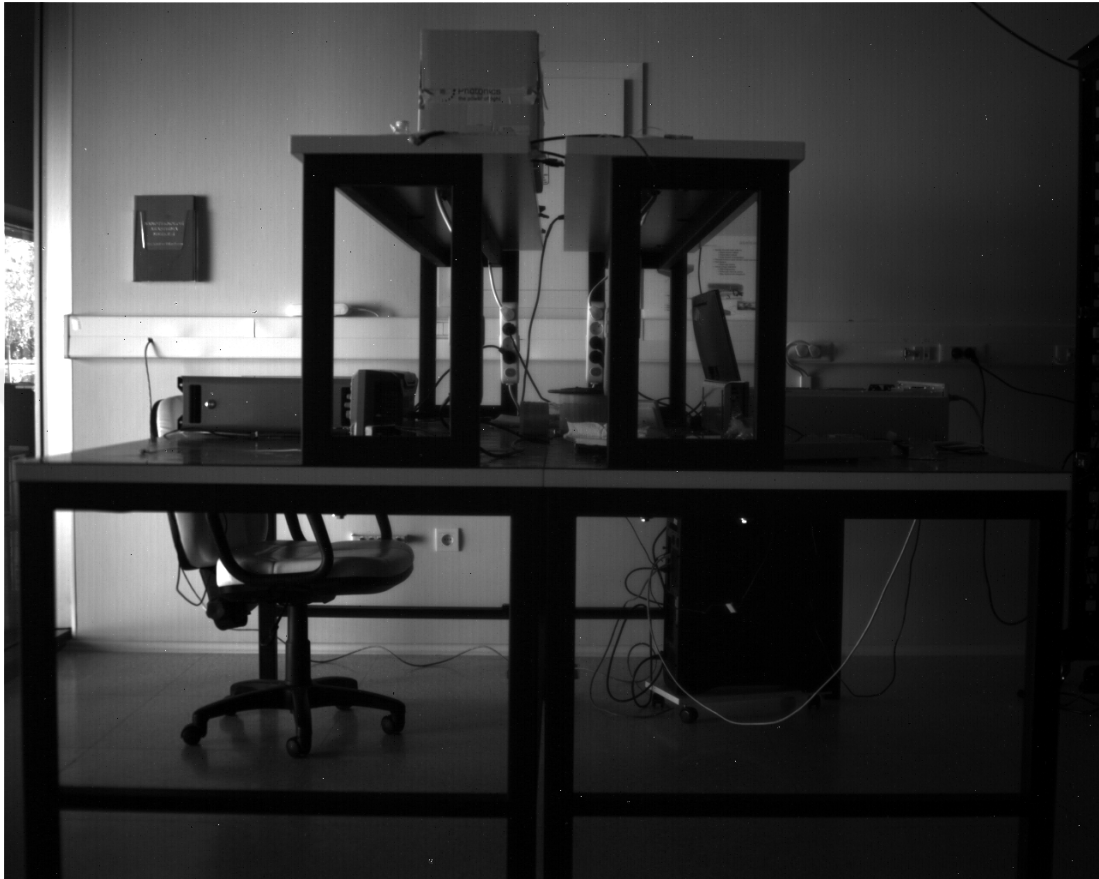


Figure 5.4: An indoor scene captured with NANOTAM SWIR Camera with NUC

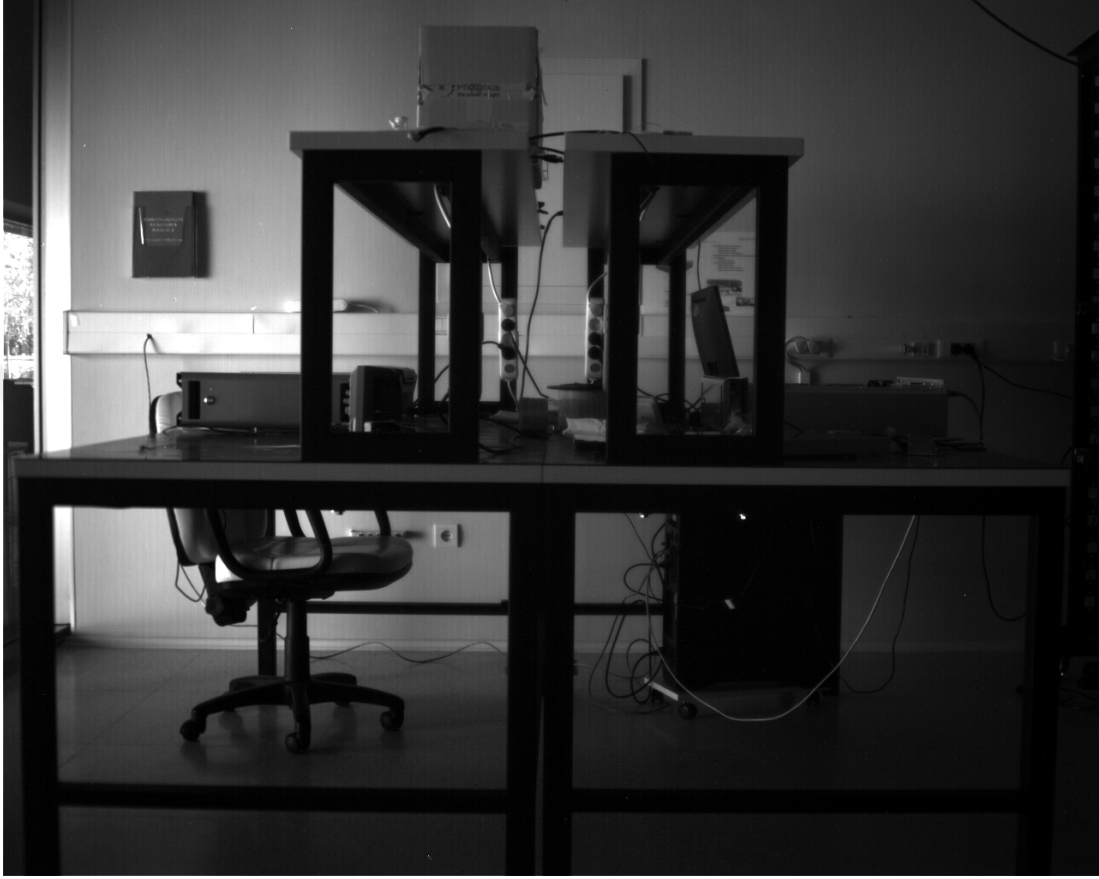


Figure 5.5: An indoor scene captured with NANOTAM SWIR Camera with NUC and defective/dead pixel correction

It is clearly seen that NUC reduces non-idealities and fixed pattern noise greatly. Dead pixel correction maximizes the image quality.

5.2.3 Auto Exposure

Exposure can be defined as the integration period in our system. With the amount of the incident light this integration time needs to be adjusted dynamically to make use of the dynamic range of the ADC at a better degree. To realize this, automatic adjustment mean of the histogram is always observed. The mean of the histogram is tried to be set in the middle of the ADC dynamic range with the

help of a control loop that sets integration time by observing histogram mean.

5.3 Characterization

5.3.1 Dead Pixel Analysis

The detector is required to have dead pixel percentage of less than % 1.

5.3.2 Test Setup and Procedure

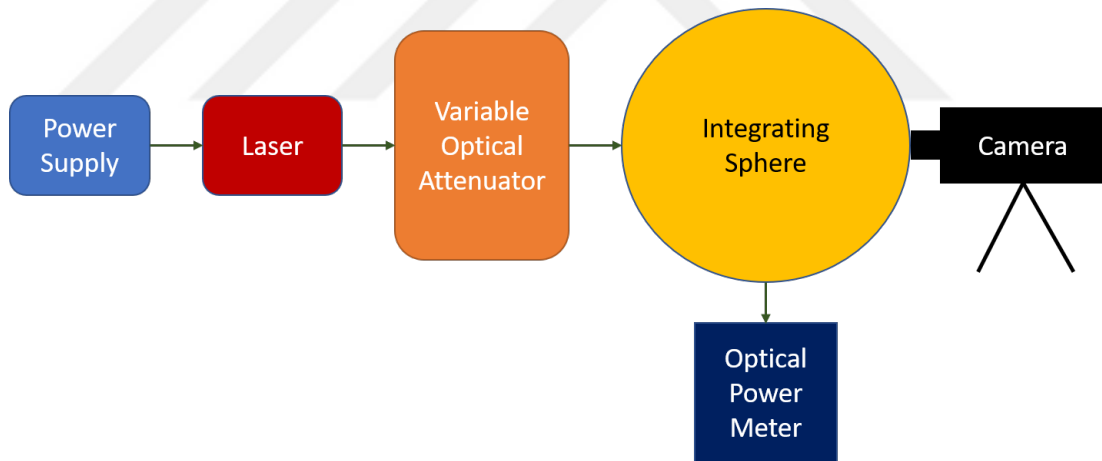


Figure 5.6: Test setup for dead pixel analysis and dynamic range analysis

The camera is placed at its place near the integrating sphere as shown in figure 5.6. Laser is supplied with the power supply and the variable optical attenuator is adjusted so that there is no optical power, this is verified by looking at the optical power meter. At this moment, dark image is acquired with the help of PC GUI. After that, variable optical attenuator is adjusted in such a way that the detector is at the edge of saturation. This is verified by looking at the optical power meter and the histogram panel in the PC GUI. At this moment, light image is acquired with the help of PC GUI. Every pixel is checked using the formula

shown in equation 5.2. In this equation, l_i is the pixel's light image value, d_i is the pixel's dark image value, $\bar{l}$ is the average value of pixels in light image and $\bar{d}$ is the average value of pixels in dark image. The pixels that have responsivity less than % 30 of average responsivity are assumed to be dead/defective pixels.

$$\frac{l_i - d_i}{\bar{l} - \bar{d}} > 0.3 \quad (5.2)$$

5.3.3 Test Results

Number of Dead Pixels	Total Pixel Number	% of Dead Pixels	Test Result
1742	1310720	% 0.133	Passed

Table 5.1: Dead pixel analysis test results

5.3.4 Dynamic Range Analysis

The camera is required to have dynamic range of at least 1000. This can be described as the ratio of maximum detectable optical power to minimum detectable optical power.

5.3.4.1 Test Setup and Procedure

The camera is placed at its place near the integrating sphere as shown in figure 5.6. Laser is supplied with the power supply and the variable optical attenuator is adjusted so that there is no optical power, this is verified by looking at the optical power meter. Integration time is adjusted to $500\mu s$. After that, optical power is increased gradually by checking the mean of the histogram. The optical power at which mean of the histogram begins to increase is noted as the *Low Power*. And then, integration time is adjusted to 200ms. Optical power is increased slowly

by checking the mean of the histogram. The optical power at which mean of the histogram no longer increases, detector reaches saturation, is noted as the *High Power*. The ratio of *High Power* to *Low Power* gives dynamic range as shown in equation 5.3.

$$DynamicRange = \frac{High\ Power(W/cm^2)}{Low\ Power(W/cm^2)} \quad (5.3)$$

5.3.4.2 Test Results

<i>High Power</i> (mW/cm ²)	<i>Low Power</i> (μW/cm ²)	Dynamic Range	Test Result
224	31	7226	Passed

Table 5.2: Dynamic range analysis test results

Following are the images that were captured using the camera designed and manufactured at NANOTAM with a cooperation of Electro-Optics System Group and Infrared Photonic Detectors Group; also named as NANOTAM SWIR Camera. Figure 5.7 shows an image which marks NANOTAM SWIR Camera's ability to see through haze. Figure 5.8 seals the excellent imaging quality of NANOTAM SWIR Camera with employed image correction techniques.



Figure 5.7: SWIR image acquired with NANOTAM SWIR Camera vs visible image captured with a smart phone camera



Figure 5.8: SWIR image acquired with NANOTAM SWIR Camera

It is seen that all other system requirements are met without the need of a test. On PC GUI main screen, it is seen that image flow rate is always more than 25 FPS, detector temperature is kept stable at 15°C, auto exposure is employed, on board Non Uniformity Correction and dead pixel correction is carried out. All data flow is performed via Ethernet line. System is supplied with a single 12V DC source and the camera mechanic is both watertight and airtight.



Chapter 6

Conclusion and Future Work

SWIR cameras are utilized in various areas from military applications to navigational systems. SWIR cameras' ability see through haze, fog and smoke make them very special. Moreover, SWIR cameras detect reflected light as visual cameras do and as a result of this, the images captured by SWIR cameras seem much more natural to human eye than other infrared cameras.

In this thesis, the main focus is on learning the basics of how to design an end product for a sensor based system; in our case an imaging system. Imaging systems and their detection mechanisms, image sensors, analog circuits for image sensors and development of other electronics have been reviewed in detail. All of the required electronics have been designed and characterized. Finally, it is seen that the designed imaging system meet all of the requirements.

Chapter 1 states the work motivation to design a SWIR Imaging system as well as showing the possible system architectures, performance criteria and authors' contribution to the system.

Chapter 2 starts with reviewing the nature of light. Duality of light; being wave and particle, properties of atmosphere and formation of bands are addressed. Also, infrared spectrum and reasons to benefit from SWIR band are mentioned. Detection mechanism of infrared light and common image sensors are presented

in this chapter as well.

The design of the camera electronics is summarized in chapter 3. At first, brief information about the detector that was manufactured at NANOTAM is given. And then, detailed knowledge about ROICs that can be used with NANOTAM InGaAs detector is reviewed. It is indicated that, acquired knowledge about ROICs was utilized in the ROIC selection phase. After the evaluation of the selected ROIC's properties and functions, hybridization process of the detector and the selected ROIC is addressed. After that, both the units to be included and importance of the analog front end electronics are stated. Design considerations for a successful analog front end design is discussed. What parameters are needed to be paid attention are clarified and selected components together with their datasheet parameters are given. Finally, the designed analog front end is analyzed. It is seen that the designed analog front end meets all the requirements. As the most important analysis, noise analysis shows that the analog front end causes a 0.22dB of SNR degradation, which is quite small and stays in the acceptable range. Design steps of all other electronics such as power regulation, FPGA board, micro-controller board and TEC driver circuit are also shared in this chapter. Theory behind the design and component selection of these circuits are also revealed.

All electronic circuits that are designed and simulated, needed to be realized with real components on PCBs. Chapter 4 starts with the possible problems that may arise due to poorly designed PCBs and correct design techniques that should be followed to avoid those problems while designing the PCBs. Following that, designed PCBs are demonstrated signifying the end of the camera design.

Chapter 5 focuses on the system characterization. In this chapter, test results are exhibited validating that all the requirements are met successfully. Brief information about the PC GUI that was used in the tests and image correction techniques is also given in this chapter. The images that were acquired with NANOTAM SWIR Camera are shown in this chapter. The quality of the demonstrated images stands as a confirmation for the design process and the designed electronics along with software, mechanics and the state-of-the art InGaAs SWIR

detectors.

As a result, a megapixel SWIR imaging system including camera electronics, software and mechanics with completely in-house design has been developed and tested successfully. It passed all the tests showing that it met all of the requirements that were stated at the beginning.

As a future enhancement, designing a ROIC which also houses the analog front end circuitry and gives digital output can be an improvement by reducing design complexity and the overall size of the overall camera. Another approach for reducing design complexity and enhancing performance is designing a mixed-signal ASIC which integrates all of the analog front end components on a single chip. All components' being integrated on a single chip reduces effects of external noise and helps to have a less complex design with a smaller camera. Author of this thesis holds personal passion to be included in such challenging projects.

Through the camera development process we faced a lot of difficulties and had countless failures. The biggest reason for such difficulties and failures was lack of knowledge in the area. As a designer, being aware of the theory and/or working mechanism of what I have been working on helped a lot during design and debug processes. Gaining knowledge about theory and working mechanisms was not easy, it required diving deep into different resources from YouTube tutorials to books and technical articles. This thesis compiled the information that I collected so far and can be a great reference to both researchers and engineers who work in the field.

Moreover, this thesis also stands as a reference for the author too. Taking this thesis as a starting point, it is a motivation for the author of this thesis for authoring books about camera design and/or hardware development methodologies for different types of sensor based systems.

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