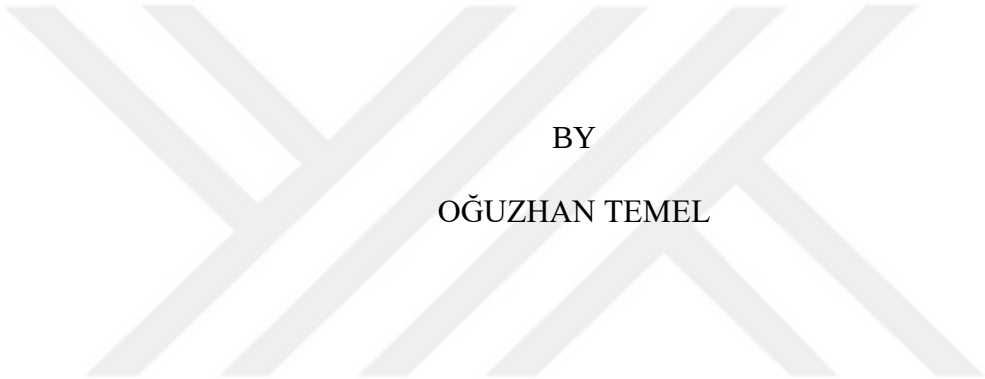


INVESTIGATION OF SOLDER MATERIALS AND BOND FORMATION FOR
WAFER LEVEL PACKAGING OF MEMS DEVICES

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ABSTRACT

INVESTIGATION OF SOLDER MATERIALS AND BOND FORMATION FOR WAFER LEVEL PACKAGING OF MEMS DEVICES

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The packaging of MEMS devices is one of the most challenging parts of MEMS commercialization. The die-level packaging of the MEMS devices is an expensive approach in which the packaging process should be applied to each device independently. On the other hand, the use of wafer-level-packaging (WLP) processes enables the packaging of the devices with a single bonding process before the fabricated device wafer is diced to have individual devices.

Metallic solder materials have a high potential to provide strong and hermetic bonding methods for MEMS packaging. Metallic materials and alloys can provide various bonding temperature and processing options. In this thesis work, Aluminum-Germanium (Al-Ge) eutectic alloy, Gold-Indium (Au-In) alloy, and Gold-Tin (Au-Sn) alloy have been investigated in terms of chemical, structural, thermal properties, and capabilities of forming a reliable bond and integrability. The bonding materials and processes have been developed for eutectic and TLP bonding methods to obtain mechanically robust, hermetic bonding processes that are compatible with MEMS device fabrication processes.

Al-Ge eutectic alloy (51 wt. % Ge) was investigated to form a eutectic bond between the substrate and the cap wafers. Al-Ge eutectic liquid wets and forms a strong bond

on Si_3N_4 surfaces. Al-Ge eutectic material is a promising material for the bond configurations in which the bond rings are formed only on one of the wafers, and the other wafer has Si_3N_4 as the bond surface. The bonds with a shear strength value up to 97 MPa have been obtained with Al-Ge eutectic bonding. However, the Al-Ge material system is very susceptible to oxidation. Therefore, the metal bond rings need to be treated properly before the bonding process. Hermetic bonds could not be obtained with this material system due to the oxidation problem, and poor de-oxidation process resulting in little interaction in the bond ring region.

Au-In material system enables to perform wafer-level TLP bonding and it is promising in terms of low bonding temperature thanks to the low melting point of indium. The material system also provides high-temperature resistance of the formed bond thanks to the high melting temperature of intermetallic phases formed during bonding. The minimum shear strength obtained with the wafer level Au-In TLP bonding method is 50 MPa. The higher values could not be measured due to equipment limitations. The bonds formed with the Au-In TLP method were tested hermetic via He-Leak tests performed according to MIL-STD 883. The re-melting temperature of the bonds is expected to be around 490 °C. He-leak values as low as $1 \times 10^{-8} \text{ atm. cc/sec}$ were obtained with the method for 6 inches wafer bonding with 200 nm topography.

Au-Sn material system was demonstrated with two different approaches to implement very thin solder metal layers ($< 2 \text{ }\mu\text{m}$) for wafer-level Au-Sn TLP bonding. The eutectic liquid was employed as the liquid layer in one approach. TLP bonding using the eutectic liquid approach provided strong bonds with 35-40 MPa shear strength. The packages formed by the method were hermetic with a He-leak value lower than $0.9 \times 10^{-9} \text{ atm. cc/sec}$. This approach is integrated into CMOS based MEMS μ bolometer fabrication process which is a commercially available process. A non-compatibility of the adhesion layer has been observed with the CMOS wafers. The second approach employed a thin barrier layer to make Au-Sn TLP bonding with thin layers possible. The symmetric and asymmetric versions of

this approach are demonstrated. While the symmetric approach provides good bond formation, the asymmetric approach could not be achieved with strong enough bonds.

Keywords: Wafer-Level Packaging, TLP Bonding, SLID Bonding, MEMS Packaging



ÖZ

MEMS AYGITLARININ DİSK SEVİYESİNDE PAKETLEME İŞLEMİ İÇİN BAĞ MALZEMELERİNİN VE BAĞ OLUŞUMUNUN İNCELENMESİ

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Paketleme işlemleri MEMS cihazların ticari ürüne dönüşmesindeki en zorlu süreçlerdendir. Bunun yanında bu cihazların ucuz ve minyatür bir şekilde üretilebilmeleri disk seviyesinde paketleme yöntemleri ile mümkün olabilmektedir. Bu yöntemler, disk üzerindeki her aygıtın aynı anda tek bir işlem ile mikro-üretim sürecinin son aşamasında paketlenmesini sağlar.

Metallik lehim malzemeleri MEMS paketleri için güçlü ve sızdırmaz bağlar oluşturma konusunda potansiyeli yüksek malzemelerdir. Farklı sıcaklıklarda ve özelliklerde bağlar bu malzemelerle elde edilebilir. Bu çalışmada Alüminyum-Germanyum (Al-Ge) , Altın-İndiyum (Au-In) ve Altın-Kalay (Au-Sn) malzeme sistemleriyle disk seviyesinde MEMS cihazlarına uygun bağlama yöntemleri geliştirilmiş ve incelenmiştir. Al-Ge ötektik bağlama yöntemi, Au-In ve Au-Sn ise geçici sıvı faz (TLP) bağlama yöntemi için uygulanmış ve incelenmiştir.

Al-Ge ötektik alaşımı aygıt ve kapak diskleri arasında ötektik bağ oluşturacak şekilde uygulanmıştır. Al-Ge ötektik sıvısı Si_3N_4 ve Al_2O_3 yüzeylerini iyi bir şekilde ıslatır ve güçlü bağ kurar. Tek bir diskte ötektik yapının bulunduğu paketleme konfigürasyonu Si_3N_4 yüzeyine 440 °C’de bağlanacak şekilde uygulanmıştır.

Oluşturulan bağların kesme dayanımı 97 MPa kadar yüksek çıkmıştır. Yüksek bağ gücüne rağmen Al-Ge malzemesinin oksitlenme yatkınlığı ve bunun temizliğinin zorluğu nedeniyle hermetik bağ yapıları elde edilememiştir.

Au-In malzeme sistemi TLP bağlama için potansiyeli yüksek bir malzeme sistemidir. İndiyum sayesinde düşük bağlama sıcaklığı sağlarken, yüksek erime noktasına sahip bileşikleri sayesinde yüksek sıcaklık dayanımları sağlayabilmektedir. Bu malzeme sistemiyle en düşük 50 MPa kesme dayancına sahip bağlar gözlenmiştir. Malzeme sistemiyle 6 inç boyutta 200 nm yüzey çıkıntısı olan disklerle elde edilen bağlar, MIL-STD 883 standardına göre uygulanmış He-kaçak testi verilerine göre hermetik özellikte olmuştur ve $1 \times 10^{-8} \text{ atm.cc/sn}$ kadar düşük helyum kaçak seviyeleri ölçülmüştür.

Au-Sn malzeme sistemi iki farklı yaklaşım için kullanılmıştır. Bu yaklaşımlar 2 µm altı kalınlıklara sahip bağ metali katmanlarıyla TLP bağlama sağlanacak şekilde tasarlanmıştır. Bir yaklaşım ötektik Au-Sn sıvısının TLP bağlama yönteminde sıvı faz olarak kullanılmaktadır. Bu yöntemle 35-40 MPa kesme dayancına sahip bağlar 320 °C'de elde edilebilmiştir. Bağların tekrar erime sıcaklıkları 500 °C'nin üstündedir. Oluşturulan bağların helyum sızdırmazlık değerleri $0.1 \times 10^{-9} \text{ atm.cc/sn}$ 'den daha düşük ölçülmüştür. Bu yöntem CMOS tabanlı MEMS mikro bolometre aygıtlarının ticari olarak da kullanılan üretim sürecine entegre edilmiştir. Fakat CMOS diski yüzeyiyle oluşan bir uyumsuzluk gözlemlenmiştir. Diğer yöntemde ise Sn katmanıyla Au katmanı arasına bir bariyer katmanı entegre edilmiş ve böylelikle düşük kalınlıklarda Au-Sn TLP bağlama mümkün kılınmıştır. Simetrik ve asimetrik konfigürasyonlarda uygulanan bu yöntem ile, güçlü bağlar sadece simetrik konfigürasyonda elde edilebilmiştir. Asimetrik konfigürasyonda bariyer katmanının oksitlenme probleminden kaynaklanabileceği düşünülen zayıf bağ oluşturma durumuyla karşılaşmıştır.

Anahtar Kelimeler: Disk Seviyesi Paketleme, TLP bağlama, SLID bağlama, MEMS paketleme.



To My Beloved Wife

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CHAPTER 1

INTRODUCTION

1.1 Overview

Micro-Electro-Mechanical Systems (MEMS) integrate the mechanical structures and electronic components to interact with the outside world's physical and chemical aspects such as acceleration, radiation, oxidization. MEMS devices are microscale systems that are fabricated using microfabrication techniques. MEMS systems suggest many different functional devices for both military applications and consumer products. Also, the market of MEMS devices is huge, and it is expanding due to the stimulation by the growing potential of Internet-of-Things (IoT), which enables smart systems in everyday life such as autonomous vehicles, smart buildings [1].

The packaging of MEMS devices is one of the most challenging parts of MEMS commercialization. The packaging of MEMS devices has a crucial role in the operation of each MEMS device. Each type of MEMS device may need a special operation environment such as vacuum, inert atmosphere, or controlled gas atmosphere, etc. The vacuum levels required by some MEMS devices can be seen in Table 1.1.

Table 1.1: Vacuum requirements of MEMS devices [7]

Sensor	Working Pressure
Accelerometer	300-700 mbar
Resonator	10^{-1} - 10^{-4} mbar
Gyroscope	10^{-1} - 10^{-4} mbar
RF switch	10^{-1} - 10^{-4} mbar
Microbolometers	$<10^{-4}$ mbar

Therefore, the packaging of MEMS devices must provide the required hermeticity to keep the special environment throughout the device's lifetime. Some devices may not need a special environment; however, it is also important to protect the devices from dust, moisture, and mechanical effects to provide a long lifetime.

Another aspect of the development of MEMS devices is the miniaturization of the devices. Miniaturization will provide the use of MEMS devices in more applications such as consumer products and mobile systems. Miniaturization will also decrease the cost of the devices, increasing the number of devices per batch of fabrication. Therefore, it is crucial to have the smallest possible dimensions for the packaged MEMS devices. Together with miniaturization, lower production cost enables to use of MEMS devices in a wide range of applications. It will be easier to implement these devices to consumer products and mobile systems. The die-level packaging of MEMS devices is a costly process, and it is the main part of the device cost. The use of wafer-level-packaging (WLP) processes enables the packaging of the devices with a single packaging process before the device wafer is separated into individual devices. A single packaging process at the end of the production line can yield tens or hundreds of packaged devices depending on the dimensions of the devices and the size of the process wafers.

To sum up, it is essential to have a WLP process that is suitable for the specific device process and the device requirements in terms of performance, cost, and application area.

1.2 Wafer-Level Vacuum Packaging Methods

There are two main approaches for wafer-level packaging of the MEMS devices. One of them is the thin-film encapsulation technique, and the other is packaging using cap wafer bonding. In the thin-film encapsulation method, a vacuum cavity is formed using thin-film fabrication methods implementing sacrificial layer use. The schematic process steps of the thin-film encapsulation technique are given in Figure 1.1. A thin film layer is deposited on a sacrificial layer, and then forming a hole to remove the sacrificial layer is performed. After the sacrificial layer removal, the open hole is closed using physical vacuum deposition techniques to have an enclosed vacuum cavity.

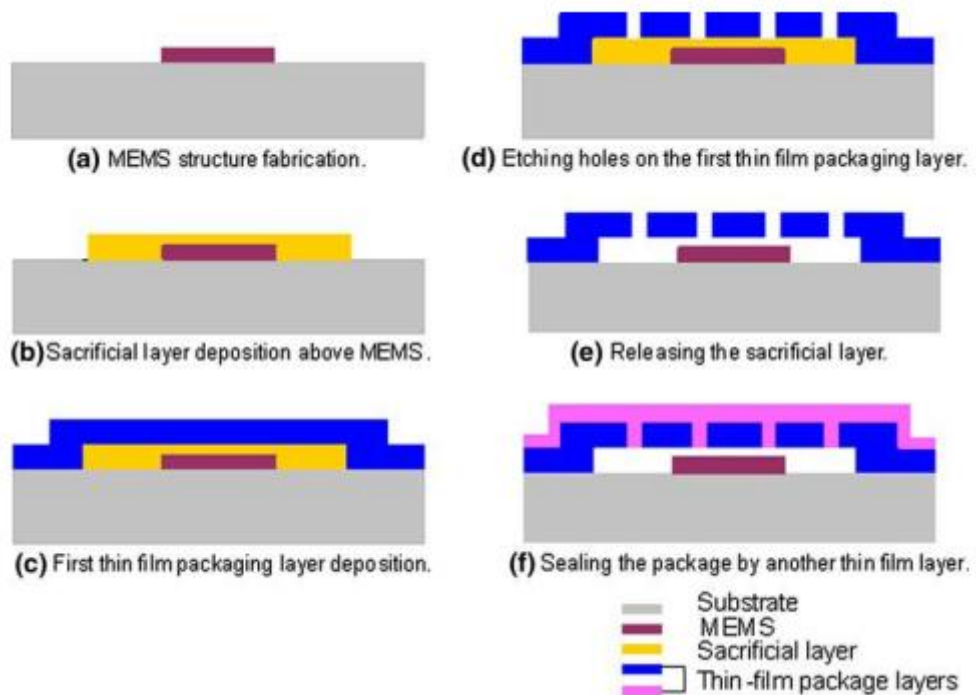


Figure 1.1: Schematic process flow of thin-film encapsulation technique for MEMS packaging [2].

The thin-film encapsulation method has the advantage of enabling device miniaturization because of no need for sealing rings. It also does not need extra bonding equipment; therefore, the cost reduction for these processes can be significant. However, there are also some problems regarding this technique. The getter integration is problematic in this method. The mechanical endurance of the package is another problem. Moreover, the thermal expansion coefficient difference between the substrate material and the thin film materials may cause crack initiations during the operation.

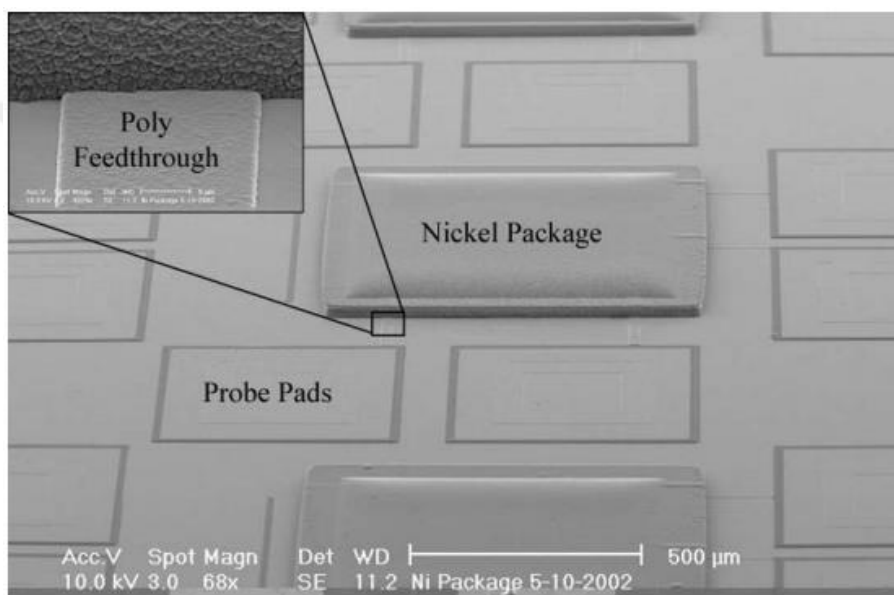


Figure 1.2: SEM image of a thin film encapsulated MEMS sensor. In this process, the Ni cover has formed with electroplating, and the hole is closed with PVD [3].

As mentioned before, another approach for the packaging of MEMS devices is cap wafer bonding. In this approach, a cap wafer with a cavity is bonded with a device wafer. Interfacial reactions between the two wafers form a bond. The interfacial reaction may take place between the substrate materials directly, or an intermediate material may be used for the bond formation. There are different bonding techniques for the packaging of MEMS devices using cap wafer bonding. These processes can be listed as following [4],

- Direct Bonding
- Anodic Bonding

- Glass frit Bonding
- Polymer Adhesive Bonding
- Metal Thermo-compression bonding
- Solder/Eutectic Bonding

In direct bonding and anodic bonding, the bonding reaction takes place between the substrate materials themselves. However, an intermediate bonding material provides the formation of the bond in other listed bonding methods.

1.2.1 Direct Bonding

In the direct bonding method, two different wafer surfaces are bonded with applied force and high temperature. The wafer surfaces need to be activated using wet or dry methods to enhance bond formation. Various couples of surfaces can be implemented in this bonding method, including silicon (Si) -silicon, Si-Silicon Dioxide (SiO_2), Si-Silicon Nitride (Si_3N_4), Si-Gallium Arsenide (GaAs), and Si-Sapphire (Al_2O_3) [5]. Process temperatures for direct bonding processes vary from 600 °C- 1200 °C. However, these temperatures may be decreased using surface activated direct bonding (SAB) method. In this method, the wafer surfaces are treated using plasma methods to increase the reactivity of the surfaces. Therefore, the process temperatures varying from room temperature to 400 °C can be obtained [6]. The direct bonding method needs ultra-clean surfaces, and it is very sensitive to surface roughness.

1.2.2 Anodic Bonding

Anodic bonding can be used to bond Si and Sodium (Na) doped glass substrates. Anodic bonding forms very strong and reliable bonds. However, its surface roughness tolerance is also low. The surface roughness for successful anodic bonding

must be on the nanometer scale. A schematic drawing of the Anodic bonding process can be seen in Figure 1.3.

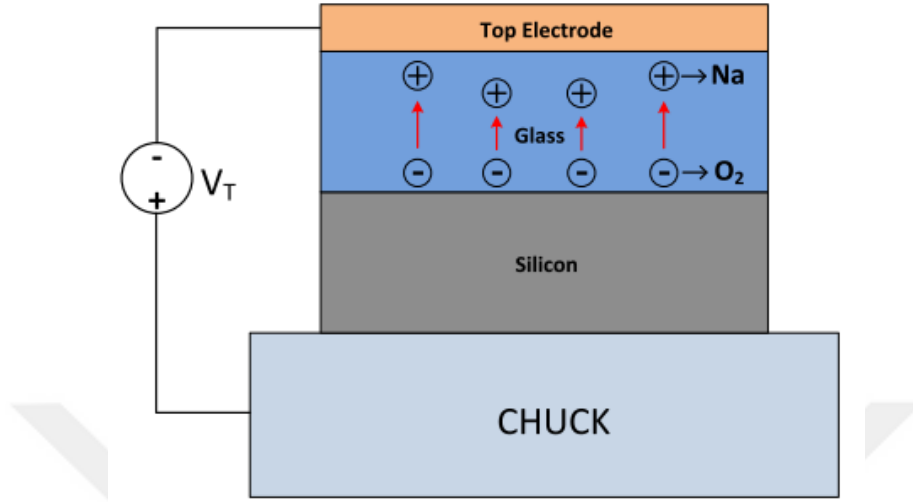


Figure 1.3: Schematic drawing of the Anodic bonding process [7].

Applied voltage and temperature result in Na ions to migrate from the Si-Glass interface leaving unbonded oxygen ions. The oxygen ions react with the Si atoms and form SiO_2 at the interface. Very strong and hermetic bonding can be obtained using the anodic bonding method. Oxygen releasing during the process may lead to a low vacuum. Therefore, getter integration is needed for the devices demanding a vacuum environment.

1.2.3 Glass-Frit Bonding

Glass-frit bonding is a commercially important bonding process. It can provide a reliable high-yield bonding process, and it can be applied for many different substrate materials. An intermediate glass making paste is deposited using the screen-printing method. High bonding temperatures ($>400\text{ }^{\circ}\text{C}$) enables liquid glass formation. The solidified glass layer between the substrates provides very strong bond formation. Out-gassing of organic residue in the glass frit takes place during the glass formation process. Getter must be integrated into the package to have high vacuum levels in the package [8]. Glass-frit bonding can tolerate the topography of

the substrate up to 2 μm . The insulating glass material can be applied with electrical feed-throughs. However, this process needs a relatively high temperature above 400 °C, and the screen-printing method cannot provide a small sealing ring width. Therefore, miniaturization with this method can be challenging. Another issue with this method is that most of the glass making pastes utilize Lead (Pb) as the component. The use of Pb containing materials has been restricted by The Restriction of Hazardous Substances Directive (RoHS).

1.2.4 Polymer Adhesive Bonding

Polymer adhesive bonding utilizes organic compounds to form bonding between the wafers. Low-temperature bonding can be obtained using polymer bonding; however, organic compounds may have a certain degree of permeability for gases; therefore, this type of bonding does not provide hermetic sealing and vacuum environment [9]. Benzo-cyclobutene (BCB), polyimide (PI) are some organic compounds that can be applied as polymer adhesive bonding material.

1.2.5 Metal Thermo-compression Bonding

Metal thermo-compression bonding, or diffusion bonding, is another bonding method. Metals such as gold (Au), Aluminum (Al), and Copper (Cu), which are frequently used in microelectronic processing, can be implemented for thermo-compression bonding processes [4]. Metal deposited wafers are brought together to form the bond; heat and force are applied to start solid-state diffusion between metals. Vacuum packages can be obtained using the metal thermo-compression method [10]. This method cannot tolerate surface topography.

1.2.6 Solder/Eutectic Bonding

Wafer bonding with solder materials implements metallic layers as an intermediate bonding material between the wafers to be bonded. Solder materials form liquid metal and form very strong and tough bond. Implementation of metals and metallic alloys allows performing different bonding processes with many varying properties such as bonding temperature, mechanical strength, and hermeticity. Solder bonding enables to form of hermetic packages, and liquid metal allows tolerating roughness and topography on the substrates. Moreover, metals allow electrical conduction; therefore, bonding materials may also be employed as feedthrough material for MEMS devices.

Any metal which melts between the substrate and the cap wafer can be used as solder material if it affords the requirements such as wetting, temperature requirement, and mechanical strength. It is important to have a bonding temperature compatible with the device, high mechanical strength, and high-temperature stability of the formed bond. These properties may be required one by one or all together for a designed bonding process and the bond formed.

Some types of solder bonding are defined as eutectic bonding. The eutectic bonding is a special case of the solder bonding in which the liquid metal formed between the wafers is a eutectic alloy of the metals. Eutectic alloy and the eutectic reaction of the metallic material systems allow phase transformation from liquid to solid at a lower temperature than the melting temperature of the components. One of the well-known solder materials is lead-tin eutectic alloy. The phase diagram of the lead-tin system with a eutectic reaction at 183 °C and 61.9 wt. % Sn is given in Figure 1.4.

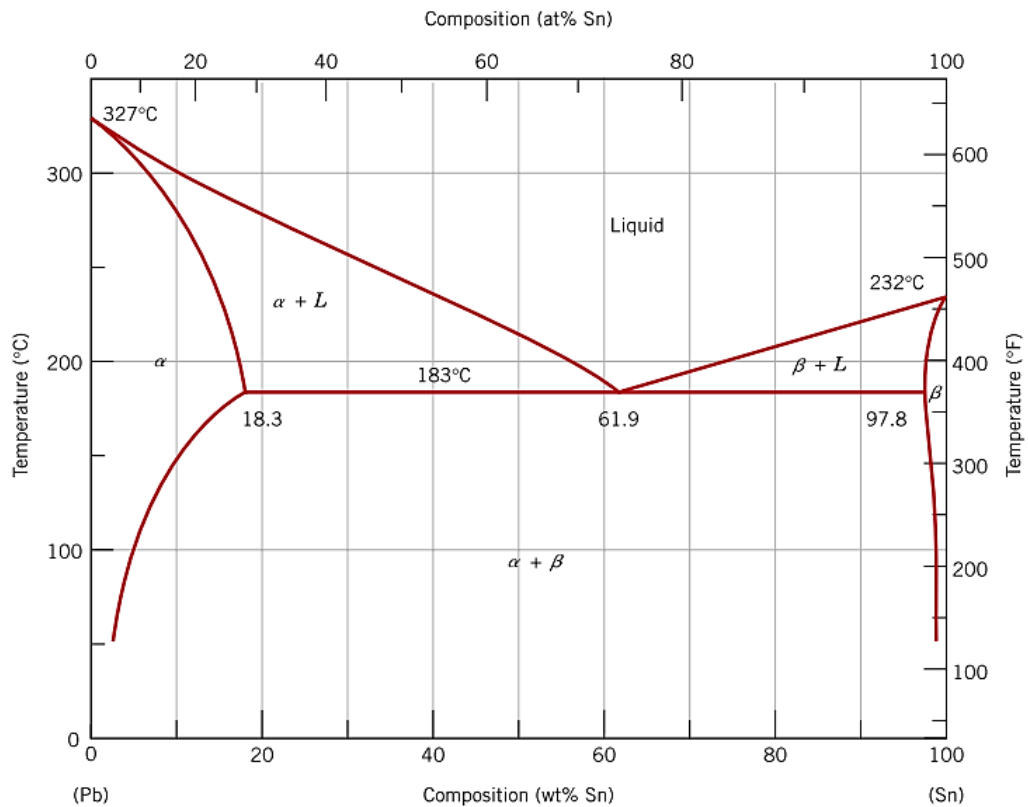


Figure 1.4: Lead-tin phase diagram with the eutectic reaction at 183 °C and composition of 61.9 wt. % Sn [12].

Very stable hermetic vacuum packages can be formed using the eutectic bonding method [11]. Many metallic systems allow eutectic bonding, and some of these systems are provided in Table 1.2.

Table 1.2: Selected metallic systems which provide eutectic reaction.

Material System	Eutectic Reaction Temperature
Au:Sn	280 ° C
Au:Si	380 ° C
Au:Ge	380 ° C
Al:Ge	440 ° C
Au:In	510 ° C

Another special method that utilizes metallic materials as intermediate bonding material is the transient liquid phase (TLP) bonding. It is also called Solid-Liquid inter-diffusion (SLID) bonding. This method uses an intermediate metallic liquid phase between other solid metallic layers. Inter-diffusion takes place between liquid and solid phases, and intermetallic compounds (IMC) are formed at the end of the diffusion process. The IMCs are usually the phases with high strength and high melting point. Therefore, it is possible to obtain bonds that have a high melting temperature than the joining temperature by utilizing the TLP bonding method [13].

Many different material systems enable TLP bonding. The material system must allow the low-temperature liquid formation and the formation of the solid phase, which has a high melting point. Some material systems which provide the TLP bonding method are given in Table 1.3.

Table 1.3: Materials that can be implemented for the TLP bonding method [14].

Material System	Process Time and Temp.	Re-melt Temp.
Copper-Indium	4 min at 180 °C	> 307 °C
Copper-Tin	4 min at 280 °C	> 415 °C
Silver-Tin	60 min at 250 °C	> 600 °C
Silver-Indium	120 min at 175 °C	> 880 °C
Gold-Tin	15 min at 260 °C	> 278 °C
Gold-Indium	0.5 min at 200 °C	> 495 °C
Nickel-Tin	6 min at 300 °C	> 400 °C

The TLP bonding process can be challenging due to the high inter-diffusion velocities of metals. Very high heating rates are needed to reach to melting temperature of the transient layer to transform into liquid phase before all layer is mixed up in solid-state. The bonding equipment dictates heating rates during the process. Therefore, this method can be equipment limited. A TLP bonding process is represented schematically in Figure 1.5 with the heating profile during the bonding process.

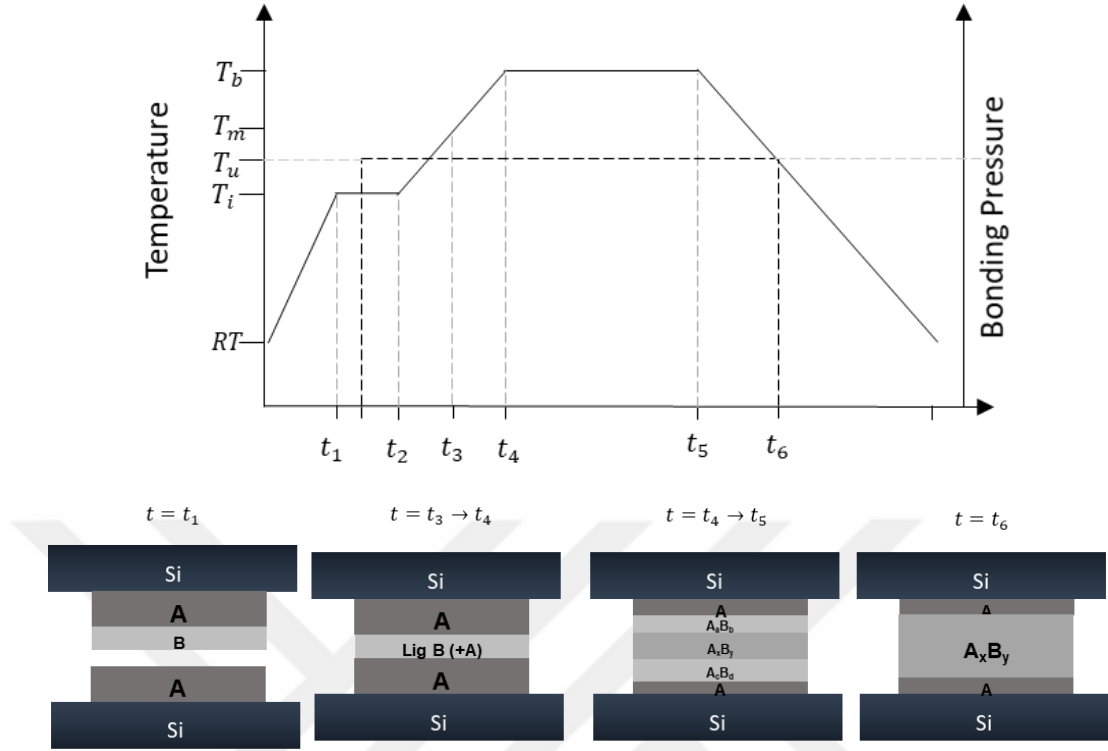


Figure 1.5: Schematic representation of TLP bonding with critical temperature steps.

In Figure 1.5, the heating starts, and the wafers are brought into contact at a lower temperature than the melting temperature of interlayer B between t_1 - t_2 . The interlayer starts to melt after t_3 , and liquid-solid interaction takes place between liquid B and solid A. The formation of A_xB_y intermetallic phases starts to form. The bonding continues between t_4 and t_5 at the bonding temperature T_b with the applied bonding pressure.

The interlayer B may be consumed by diffusion entirely before reaching the melting temperature if the thickness of the layer is lower than a critical thickness to ensure that the liquid phase obtained before all the interlayer material is consumed. Using the formula from Bosco et al. for a diffusion limiting process, the critical interlayer thickness h_c can be calculated [15],

$$h_c = 2h_\delta C_\delta \left(\frac{\rho_{\text{alloy}}}{\rho_M} \right)^2 \quad (1.1)$$

where $2h_\delta$ is the total thickness of the forming alloy or IMC by solid-state diffusion when the melting temperature of Sn is reached. C_δ is the mass fraction of Sn in the targeted alloy or IMC, ρ_{alloy} and ρ_M are the mass densities of the alloy or IMC and metal, respectively. The minimum metal thickness, h_c , corresponds to the thickness, which is needed to guarantee that enough liquid metal is available to wet both parent metals after reaching the melting temperature. Moreover, intermetallic growth from both sides can cause void formation at the interface as shown in Figure 1.6 [14-15].

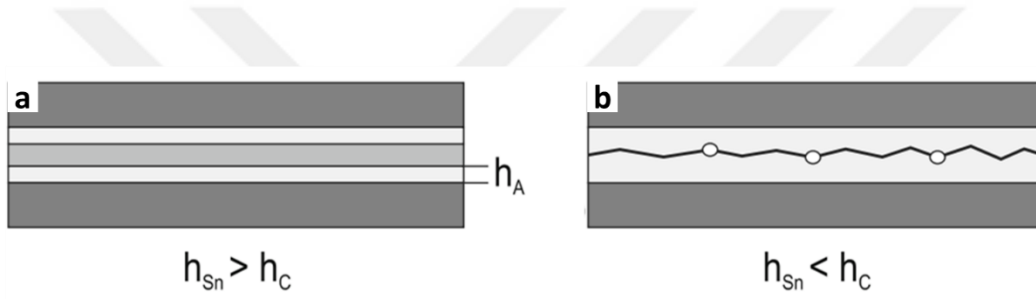


Figure 1.6: Illustration of the bond interface in the case of the interlayer metal thickness is (a) thicker and (b) lower than the critical thickness [15].

Finally, the summary of the selected bonding techniques that use metallic materials for wafer-level packaging of micro-devices is given in Table 1.4. The advantages and disadvantages can be seen in the table.

Table 1.4: Summary of the selected bonding techniques with metallic materials [29].

Bonding Type	Material	Bonding Temperature (°C)	Primary Advantages	Primary Disadvantages
Eutectic	Au _{0.8} Sn _{0.2}	>280	- Relative maturity - Fluxless bonding - Deposition options	- Steep eutectic liquidus lines - Challenging under-seal metal (USM) integration
	Au _{0.82} Si _{0.18}	>363	Ease of deposition	- Complex diffusion barrier - Challenging USM integration
	Al _{0.72} Ge _{0.28}	>423	- Compatibility of seal materials with legacy complementary metal-oxide semiconductor (CMOS) processes - Production process available in CMOS foundries	- Bonding temperatures at or near CMOS limits - Difficulty in removing native oxide
Solid-liquid diffusion (SLID)	Cu-Sn	>232	Relative maturity	Stiffness of final bonding materials
	Au-Sn	>280	Low modulus bonding materials and high remelting temperature (good candidate for devices with high operating temperatures)	- Complex phase diagram - USM integration challenging due to high rate of Au consumption
	Au-In	>156	Low bonding temperature	- Complex phase diagram - Premature mixing of bond materials
Metal-to-Metal	Al	>400	Standard CMOS pad material	- Difficulty in removing native oxide - High bonding temperature - Sensitivity to particles and topography
	Cu	>350	- Relative maturity - Simplicity	Sensitivity to particles and topography
	Au	>260	- No native oxide - Relative maturity - Simplicity	Sensitivity to particles and topography

1.2.7 Getter Integration

The getter integration is a necessary step to form a reliable vacuum environment in the package cavity. Getters are implemented in the cavity as a thin-film. The getter materials are selected as chemically active materials. When the getter material is heated, it reacts with the gas molecules to bind them in the cavity and help to reduce vacuum inside the cavity acting as a chemical vacuum pump. The getter must fulfill the requirements such as chemical stability, mechanical stability, absence of contaminating particles, low gas emission, easy activation. To activate the getter, it must be heated up. Therefore, the activation temperature should low enough not to

deteriorate the bond. Some of the common getter materials are titanium, tantalum, zirconium, and yttrium.

1.2.8 Difficulties in Solder Bonding Techniques

There are some difficulties in performing solder bonding techniques in practice. They can be listed as follows,

- The metals have high surface energy in the pure state. Their wetting and adhesion can be problematic. Flux used for adhesion can deteriorate the vacuum properties of the package. Therefore, the bonding method must be flux-less. The under-seal metallization (USM) for the adhesion/wetting and barrier functions must be selected carefully.
- The eutectic bonding method needs a precise composition of the alloy. Therefore, tuning the composition precisely for eutectic composition can be challenging, especially with the physical vapor deposition (PVD) methods.
- Oxidation of metals occurs easily. The native oxide layers on bonding materials can cause the failure of the bond formation or weak bonds. For some material systems, a thin oxidation protection layer can help while it may also cause negative effects in liquid formation. Therefore, proper de-oxidation processes may be needed for some material systems. These methods can be wet or dry treatments. These treatments may need some complicated equipment and can make the fabrication more complicated and expensive.
- TLP methods depend on the diffusion process of the metallic films. It usually utilizes thick ($\geq 5\mu\text{m}$) electrodeposited metal layers in the processes. The uniformity of electroplated metals on 6 inches or 8 inches wafers may not be

good enough. The deposited layers may need some surface planarization steps such as the chemical mechanical polishing (CMP) process, which makes the process complicated and expensive. Moreover, electrodeposition on complementary metal-oxide-semiconductor (CMOS) wafers may not be preferred due to applied voltage. Utilizing vacuum deposition methods such as DC sputtering and evaporation can be challenging for TLP bonding process development due to their deposition rates and source material consumptions.

- Getter integration and activation can be problematic for low-temperature bondings. The getter activation temperatures for conventional getter materials are above 400 °C. Therefore, getter material selection or development is another critical issue. The development of getter materials with low activation temperature, the activation by localized heating, and TLP bonding method can be a solution for this problem.

1.3 Literature Review

In this section, a literature review for wafer-level Al-Ge eutectic bonding, wafer-level TLP bonding for Au-In, and Au-Sn material systems will be presented, focusing on the application for MEMS device encapsulations.

Al-Ge Eutectic Bonding

The soldering or solder bonding techniques are very old methods to bond the dissimilar metals. In the electronic industry, soldering is implemented both for interconnection formation and encapsulation of certain devices or circuits [17-21]. Eutectic alloys are promising candidates for high strength bond formation at low temperatures. The encapsulation of the MEMS devices in a ceramic or metal package does not require strict restrictions for encapsulation material and process. On the other hand, wafer-level encapsulation of MEMS devices, especially for the devices

integrated with CMOS technology, needs encapsulation materials that are compatible with CMOS technology and devices processes. Al and Ge are fab-friendly materials that can be implemented in CMOS/MEMS manufacturing facilities; therefore, the Al-Ge material system is a good candidate to implement to wafer-level CMOS/MEMS devices encapsulation processes [22]. Vu et al. have demonstrated Al-Ge eutectic bonding using 1 μm Al and 0.573 μm Ge on the SiO_2 passivation layer. They bonded two sets of samples with 1 μm Al-0.573 μm Ge and 2 μm Al-1 μm Ge. They obtained hermetic seals with the thicker material stacks at 525 $^\circ\text{C}$ in their bond set up [23]. Park et al. performed Al-Ge eutectic bonding with the layer thicknesses of 1 μm Al and 0.2 μm Ge. Ge was deposited on SiO_2 /poly-Si layers, and Al was deposited on SiO_2 [24]. The Al-Ge material configurations they suggested for MEMS device encapsulation are given in Figure 1.7.

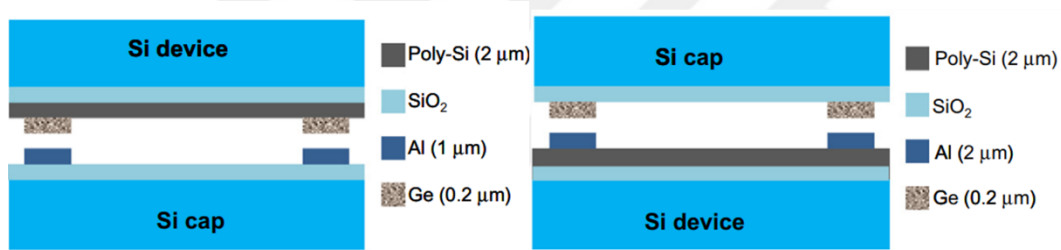


Figure 1.7: The material configurations of Al-Ge Eutectic bonding suggested MEMS devices by Park et al. [24].

Chidambaram et al. applied a diffusion bonding using the Al-Ge material system. This approach aims to lower the relatively high-temperature requirements of Al-Ge eutectic bonding, which is higher than 420 $^\circ\text{C}$. They applied a pre-treatment with Ar plasma etching for Aluminum oxide (Al_2O_3) formed on the Al surface before the bonding process. They used in-situ formic acid treatment during bonding to reduce the native oxide of the Ge layer. The shear strength values of their diffusion bonded samples were around 20 MPa, approximately half of the eutectic bonded samples as given in Figure 1.8. Furthermore, the He-leak test results of the samples were one order of magnitude lower than the eutectic bonded ones [25]. The work by Geng et.al

also showed that the surface treatment of the Al-Ge material system is important to obtain a significant interaction between the bond layers [27].

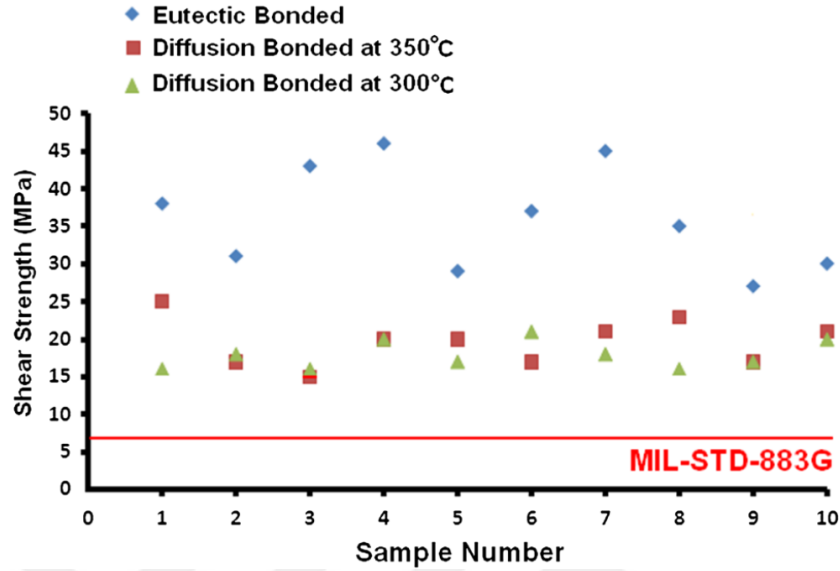


Figure 1.8: Shear strength comparison of Al-Ge eutectic bonded and diffusion bonded samples [25].

Another work for 3D IC integration by Crnogorac et al. uses Al-Ge eutectic bonding for structure transfer from one wafer to another [28]. The configuration they used for bonding can be seen in Figure 1.9(a)(b). They implemented 300 nm Al and 175 nm Ge layer for eutectic composition. The eutectic alloy and its structure in the SEM image can be seen in Figure 1.9(c). It should be noted that they implemented Al-Ge bond material only one side, and the bond surface on the other wafer is Si_3N_4 . The bonding temperature was 430 °C for 30 minutes. Although they did not provide mechanical strength data for the bonding, the transfer with the bonding was successful with a 90 % yield.

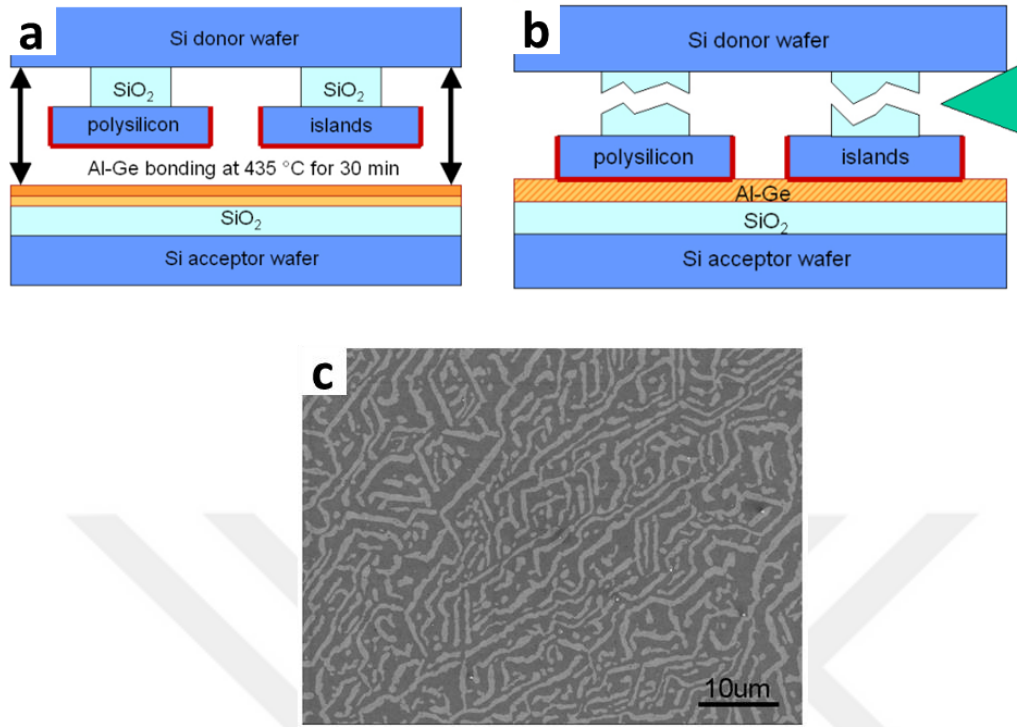


Figure 1.9: (a)(b) The structure transfer using Al-Ge bonding on Si₃N₄ surface, (c) the plan view SEM image of the Al-Ge eutectic bond region [28].

Au-In TLP Bonding

Au-In material system is a promising bond material providing a low-temperature process for temperature-sensitive devices. The melting temperature of Indium is 156 °C, therefore 180-200°C bonding temperatures can be realized by implementing the pure metal indium as the liquid forming component. Although, Au-In bonding is implemented for the systems such as wide-bandgap materials, image sensors, chip stacking applications [30-35], the method has also been demonstrated in WLP of MEMS and sensor applications.

Yoon-Chul et al. [36] implemented Au-In TLP bonding in wafer-level applying two different bonding temperatures to the wafers with the material stacks as given in Table 1.5. They performed Au-In TLP type-1 bonding at 210 °C with 0.04 MPa bonding pressure for 10 minutes and type-2 bonding at 180 °C with 0.02 MPa for

30 minutes. They assumed to have AuIn_2 , AuIn , and Au_7In_3 intermetallic phases according to energy-dispersive x-ray spectroscopy (EDS) results. The shear strength values for type-1 and type-2 samples were 40 MPa and 20 MPa, respectively. They obtained a re-melting temperature around 470 °C.

Table 1.5: Materials implemented for Au-In TLP bonding by Yoon-Chul et al.[36].

	Type 1	Type 2
Cap wafer	Glass (4 inches)	Glass (4 inches)
metallization	Ti/Ni/Au/In/Au 500/2000/500/25000/ 500 (Å)	Ti/Ni/Au/In/Au 500/2000/500/2 5000/500 (Å)
Bottom wafer	Glass	Si
metallization	Ti/Ni/Au 500/1000/20000 (Å)	Cr/Au 400/20000 (Å)

Welch et al. has used Au-In TLP bonding for wafer-level packaging of Pirani gauge structures implementing getter onto the cap wafer. The bonding configuration they realized can be seen in Figure 1.10. They formed the gold layers by electroplating and the indium layer by evaporation. The bond formed at 200 °C for 1 hour, then getter activation annealing was done at 400 °C for 40 minutes. The measured package pressures after bonding were ranged between 200 mTorr - 5 Torr. The calculated leak rate was as low as $1 \times 10^{-16} \text{ atm.cc/sec}$.

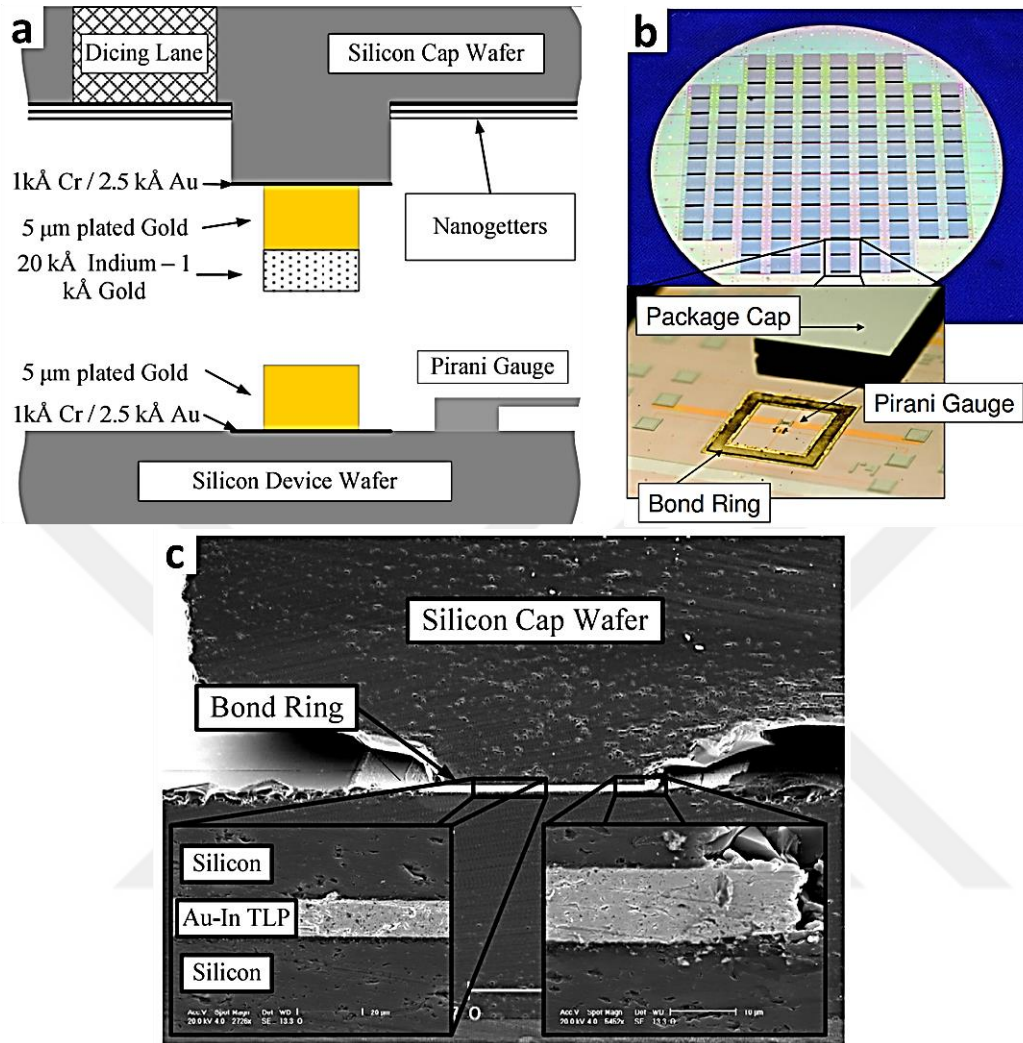


Figure 1.10: (a) The schematic representation of the wafers before bonding, (b) the de-capped Pirani gauge, and (c) SEM cross-section of the bond region after bonding [37].

Chidambaram et al. performed different Au-In bonding trials employing Au-In materials stacks with/without gold protective layer on the indium layer and Ti/Ni/Pt barrier layers between Au and In. The layer thicknesses of Au and In in the bond experiments were relatively low, 1 μm and 1.28 μm, respectively. They implemented both wafer-level bonding with 200 mm wafers and chip-level bonding with 16x16mm² dies. They investigated the heating rate effect realizing the chip-level bonding using a flip-chip bonding device. The wafer-level bonding system lacks a

high heating rate due to practical limitations; however, they were able to apply a high heating rate, as high as 100 °C/min, via a chip-level bonding system. The results of lower heating rates than 100 °C/min were leaky in the C-SAM investigations of the samples as given in Figure 1.11.

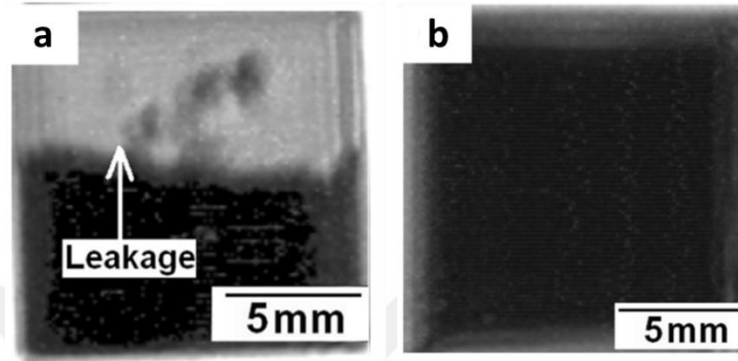


Figure 1.11: The C-SAM images of chip-level Au-In TLP bonded samples with (a) 75 °C/min and (b) 100 °C/min [38].

The effect of the protective Au layer on In was observed in wafer-level using a 45 °C/min heating rate with commercially available wafer-level bonder. Their C-SAM investigation showed that the samples without a protective Au layer need higher bonding pressure to obtain a leak-free bonding. Higher bond pressure allows breaking the indium oxide; on the other hand, the samples with a protective Au layer provided leak-free bonds with lower bond pressures.

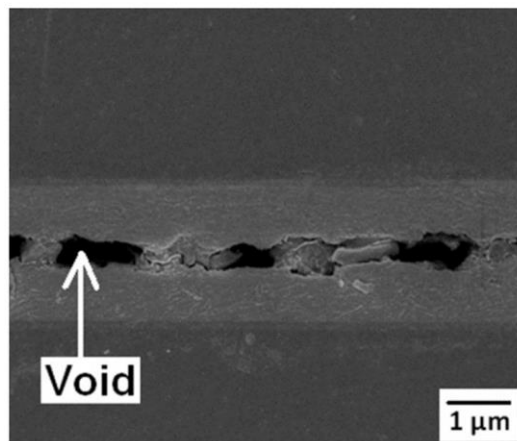


Figure 1.12: The cross-sectional SEM image of the Au-In TLP bond interface was performed without a barrier [38].

Another important observation from their work is the effect of the barrier layer. With the samples without a barrier layer, they could not achieve bonding when Au and In layers on the cap and substrate wafers are in contact before bonding. The bond interface had a structure with voids as shown in Figure 1.12. The best barrier thickness and material is determined as 20 nm Ni in their work. The He-leak test results for Au-In TLP bonded samples in the work are summarized in Table 1.6.

Table 1.6: He-Leak test results of the Au-In TLP bonded samples with and without barriers [38].

S. no.	Without diffusion barriers		With diffusion barriers		
	Without Au protective coverage layer (atm cc/s)	With Au protective coverage layer (atm cc/s)	Ti (atm cc/s)	Pt (atm cc/s)	Ni (atm cc/s)
1.	0.2×10^{-5}	0.1×10^{-7}	0.2×10^{-7}	4.8×10^{-7}	0.5×10^{-7}
2.	1.3×10^{-5}	0.2×10^{-8}	1.3×10^{-6}	0.2×10^{-8}	0.3×10^{-8}
3.	0.8×10^{-6}	0.5×10^{-8}	1.0×10^{-5}	2.5×10^{-7}	0.3×10^{-8}
4.	0.4×10^{-7}	2.2×10^{-6}	1.0×10^{-5}	1.6×10^{-7}	0.6×10^{-8}
5.	0.2×10^{-6}	0.7×10^{-8}	0.2×10^{-7}	3.2×10^{-7}	5.5×10^{-7}

Au-Sn TLP Bonding

Au-Sn material system, especially Au₈₀Sn₂₀ eutectic composition, is one of the most widespread material systems in the microelectronic industry in soldering and joining applications [39-40]. The Au-Sn material system provides flux-less bonding thanks to its oxidation resistive nature. Moreover, its high strength, creep resistance, fatigue resistance, and inertness make the material suitable for many applications [39-40]. Au-Sn material has been implemented in flip-chip bonding and die attachment processes as flux-less solder joint as both Au₈₀Sn₂₀ eutectic alloy and Sn-rich eutectic alloy [41-42]. Note that Au-rich Au-Sn eutectic provides bonding at 280 °C while Sn-rich Au-Sn eutectic provides bonding at 220 °C. However, Sn-rich solder can be more prone to oxidation due to high Sn content.

In addition to its fluxless soldering application, the Au-Sn system has a wide range of applications in hermetic packaging [43-44]. The Au-Sn bond rings are demonstrated as both solder pre-forms and electroplated layers for hermetic packaging applications [44-45]. The bond metal thicknesses are 10 µm for Au,

12.5 μm for AuSn in the pre-form case while 15 μm for Au, 5 μm for Sn in the electroplated case. The schematic drawing of Au-Sn bonding applied to ceramic packages with Ni/Au metallization can be seen in Figure 1.13 both for the solder pre-form and the electroplated layer application.

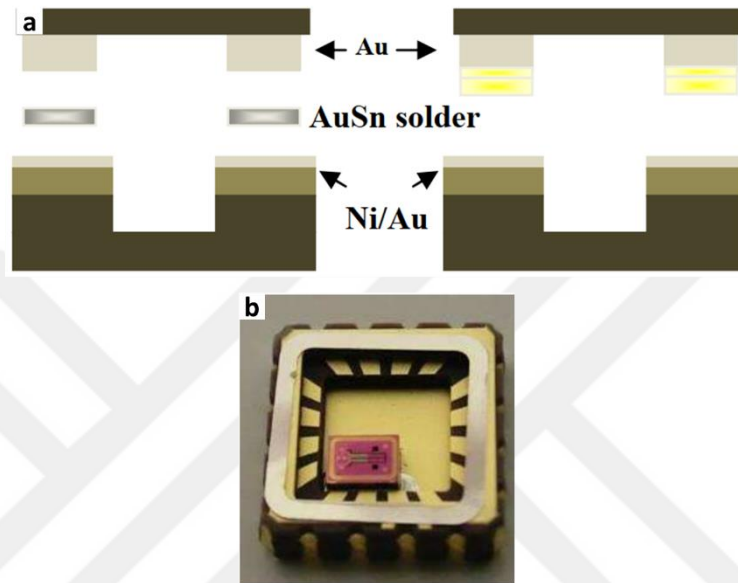


Figure 1.13: (a) Schematic drawing of Au-Sn TLP bonding applied for hermetic ceramic packages with AuSn solder pre-form and electroplated layers on the lid and (b) LCC ceramic package with AuSn solder pre-form [44].

Although there are studies on Sn-rich Au-Sn bonding for the wafer-level process [46], most of the wafer-level packaging studies are concentrated on gold-rich TLP or $\text{Au}_{80}\text{Sn}_{20}$ eutectic bonding [29]. Xu et al. have demonstrated a wafer-level Au-Sn TLP bonding on 6 inches wafers. They used the bond configurations given in Figure 1.14. There are two different Au-Sn material structures. In one approach, they used a symmetric configuration, which was bonded at 320 °C. In the second approach, they used an asymmetric configuration, which was bonded at 350 °C. In the latter, the total Sn thickness is higher. They observed low mechanical strength at the IMC and TiW adhesion layer interface, and they suggested that to have an unreacted Au layer at the contact point with the adhesion layer. They proposed to increase the Au layer thickness to have an unreacted gold layer. In the asymmetric

bond material configuration, they observed voids in the bond interface, as shown in Figure 1.14(b).

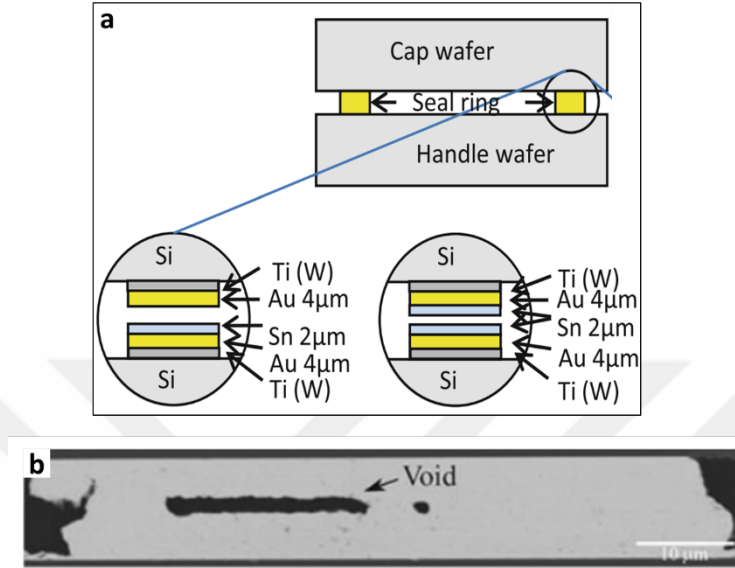


Figure 1.14: The Au-Sn bond ring material configuration applied by Xu et al., and the voids observed in the bond interface of asymmetric material configuration [47].

Maruska et al. have performed Au-Sn TLP bonding experiments for relatively low bonding temperature with 6 inches sized wafers [48]. They calculated the minimum Sn thickness for enough amount of the liquid-Sn during the bonding process and the void-free bond interface using the model proposed by Bosco et al. [15]. Their calculated Sn thickness was 1.4 μm, with a heating rate of 30 K/min. The thicknesses used are 2 μm Sn thickness between 3.2 μm gold layers targeting the 8 wt. % Sn as the final alloy composition. They aimed at bonding processes between 240 °C - 280 °C. They observed the unreacted residual Sn layer at the bond interface for the bonding experiments performed at 240 °C, Figure 1.15(b). They obtained a fully reacted bond structure with 280 °C bonding temperature as shown in Figure 1.15(a). The bond strength values were around 100 MPa.

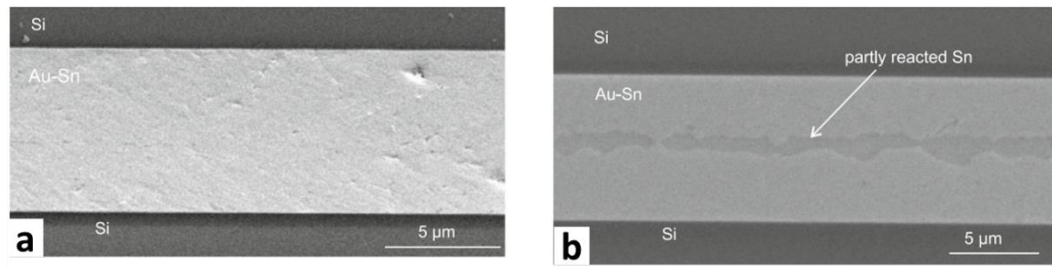


Figure 1.15: Cross-sectional SEM images of Au-Sn TLP bonds at (a) 280 °C and (b) 240 °C [48].

Another Au-Sn TLP bonding with 6 inches wafers has been demonstrated by Rautiainen et.al. The bond ring structures employed in their work are provided in Figure 1.16. The bonding pressures of the samples were 2.4 MPa for TiW adhesion layers and 14.4 MPa for TiW/Ni adhesion layers. The bonding processes for samples with only TiW and TiW/Ni adhesion layers were performed at 320 °C and 350 °C, respectively. The shear strength and tensile strength of the bonds can be seen in Figure 1.16(b). The samples with TiW/Ni adhesion layer have significantly higher strength values.

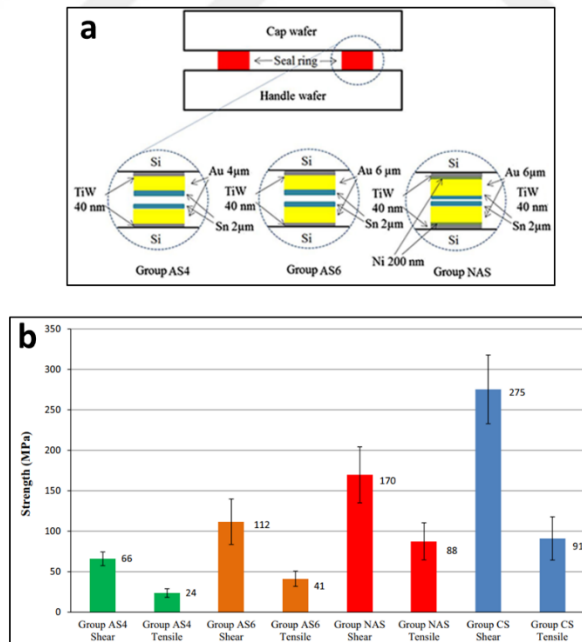


Figure 1.16: The Au-Sn bond ring material configuration applied by Rautiainen et al., and the mechanical strength values of the bonded samples [49].

In another study, Rautiainen et al. aimed to develop an Au-Sn TLP bonding that is more suitable to implement the bonding process for CMOS based devices. They have designed the bonding material to be placed on only a cap wafer and aimed to have another adhesion/barrier layer stack on the device wafer, as can be seen in Figure 1.17. The bonding achieved a high strength bond (higher than 40 MPa) at 320 °C and with 3 MPa bonding pressure. They observed that the Pt thickness higher than 100 nm provides stronger bonds with cohesive (bulk) failure of the bond instead of interfacial failure.

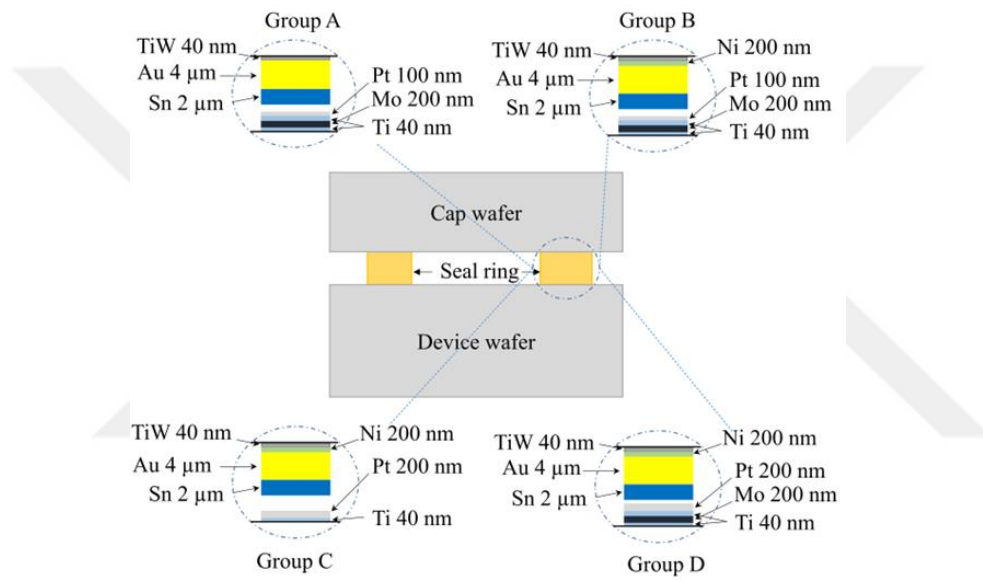


Figure 1.17: The material configuration studied by Rautiainen et al. to have a flexible Au-Sn TLP Bonding process for better process integration [50].

1.4 Motivation and the outline of the thesis

This work aims to investigate the metallic material systems for wafer bonding methods, which can be integrated into MEMS device fabrication flow as the final packaging method utilizing solder bonding in the wafer-level. The packaging is the final step of the MEMS process flow; therefore, these methods have crucial importance in obtaining commercialized MEMS products.

Solder bonding techniques provide a flexible and reliable encapsulation method, as presented in previous sections. TLP bonding is the up-and-coming solder bonding technique in terms of low bonding temperature, high thermal stability, high mechanical strength, and hermeticity. The wafer-level TLP bonding methods usually utilize relatively thick metallic layers (8-10 μm), as reported in the literature review part of this text. The high layer thickness makes the electrodeposition method the best choice for the metal deposition steps. The wafer-level electrodeposition of metals can lack uniformity. Therefore, a planarization step, such as CMP, must be implemented in the process flow. The planarization step can be costly and time-consuming. Furthermore, the applied voltage during plating may be harmful to some CMOS based devices, as mentioned before.

This thesis work aims to develop solder bonding methods that are promising in terms of hermeticity, mechanical strength, thermal stability, and potential to be integrated easily into the device fabrication processes. Wafer-level packaging process integration into CMOS-based devices processes can be challenging due to restrictions of CMOS devices such as temperature limits, chemical compatibility, and pressure sensitivity. In this work, the TLP bonding method was implemented with the Au-In and Au-Sn material systems, and the eutectic bonding method was implemented with the Al-Ge material system. The work focuses on the bonding processes with relatively thin metallic films whose thicknesses are below 5 μm for Au-In TLP bonding and below 2.5 μm for Au-Sn TLP bonding. Such bonding processes are challenging, especially for TLP bonding. The thin films with low thicknesses in this work can be deposited by PVD methods such as thermal evaporation and DC sputtering, which can provide uniform metal films in wafer-level. The TLP bonding methods in this work aims the bonding temperatures as low as possible, and high re-melting temperatures to compensate for getter activation heating. The bonding methods have been designed and examined for both the required physical properties and the process integration aspects.

The material systems Au-In, Au-Sn, and Al-Ge are introduced, and the design considerations of the alloys are mentioned in Section 2.1, then the methods, process flows, and equipment are explained in Section 2.2. Finally, the results are presented and discussed in Section 3. The study is concluded, and the future works are mentioned in Section 4.



CHAPTER 2

EXPERIMENTAL

2.1 Materials

2.1.1 Overview

In this work, materials systems have been chosen for both eutectic and TLP bonding methods. The eutectic bonding method has been utilized using the Al-Ge material system. The TLP bonding method has been utilized using Au-In and Au-Sn material systems. The material selection and design have been performed according to the design rules listed in the following section.

2.1.1.1 Design Rules for Material Design and Selection

Under Solder Metallization Layer Selection

Under solder metallization (USM) layers and their thickness is crucial. They provide adhesion of bond metals to the substrate surface and act as a barrier layer between the bond metal and the substrate surface. Liquid metal must wet the USM layer for good adhesion. The reaction between the USM layer and liquid metal should be minimum not to affect the composition and properties of the bond metal, and the USM layer should act as a barrier between the solder and the substrate.

Bonding Temperature

The bonding temperature is desired to be kept as low as possible. Low bonding temperature decreases the heat load to devices wafers. The less heat load provides

lower thermal stress on the structures and materials. CMOS based device wafers are limited with the thermal limit of the CMOS structures if the device does not own a lower limit. The temperature limit dictated by standard CMOS structures is 450 °C. However, it has been reported that CMOS wafers with Al interconnects and Tungsten (W) plugs can withstand temperatures as high as 525 °C. In this work, the CMOS limit has been considered as 450 °C.

Re-melting Temperature and Getter Integration

The device packages may need to expose to high temperatures after fabrication. The cause of the high temperature may be a working environment or a post-processing step after fabrication. Getter activation is one of the most common processes that require high-temperature processing after packaging. The getter activation temperature must be above 400 °C to activate Ti thin-film getter, which is a widespread thin-film getter material. Therefore, the bonding process must allow getter activation during the bonding or later. To enable the getter activation, especially after the bonding, the formed bond must withstand the getter activation temperatures. This requirement can be satisfied with the TLP bonding method having high-temperature resistance after the bonding process thanks to its phases and IMCs with a high melting temperature. In the eutectic bonding method, the bonding and the re-melting temperatures will be the same. So, the getter activation can take place in eutectic method only if the bond formation temperature is close to the activation temperature.

Flux-less Bonding and Oxide Treatment

Oxide formation and the needs of surface treatment can affect the bonding process in terms of bond quality and practicality of the bonding process. Flux used for vacuum packaging is not desired due to outgassing issues. Therefore, materials implemented for the wafer-level bonding should allow flux-less bonding design, and the materials should have easy surface treatment requirements.

Composition and Thickness Selection

Eutectic bonding methods employ the eutectic composition of the selected material system. Material systems with a complicated phase diagram may have more than one eutectic reaction. The design considerations mentioned above lead to the selection of the proper eutectic composition of the material system.

TLP bonding methods usually use pure metals as liquid phase; therefore, these methods aim a specific final composition at the end of the process. The target composition should be selected according to desired bond properties such as mechanical and thermal properties. According to the target composition, the amount and the type of intermetallic phases in the structure change and result in different properties.

Both for TLP and eutectic bonding method, the composition must be adjusted with deposition thicknesses of the metal thin-films. The target thickness ratio for a specific composition can be calculated using Equation 2.1,

$$\frac{t_A}{t_B} = \frac{wt\%A \times \rho_B}{wt\%B \times \rho_A} \quad (2.1)$$

where t_A and t_B thicknesses of the layers, $wt\%A$ and $wt\%B$ weight percentages of metals in the desire composition, ρ_B and ρ_A density values of the pure metals. The eutectic method needs a precise composition adjustment. In contrast, TLP methods can be more flexible about the final composition. However, as mentioned in Section 1.2.6, the interlayer thickness should be selected carefully. It must be higher than the critical layer thickness. This thickness is dependent parameters such as diffusion and intermetallic growth rate, process temperature, the composition of intermetallic, and heating rate. The material system defines all these parameters; the bonding equipment dictates only the heating rate. The critical thickness for a material system can be calculated using following equation

$$h_c = 2h_\delta C_\delta \left(\frac{\rho_{alloy}}{\rho_M} \right)^2 \quad (2.2)$$

Here ρ_{alloy} is the density of the alloy, ρ_M is the density of the metal, C_δ is the weight fraction of the metal in the intermetallic phase and h_δ is the formed thickness of the intermetallic phase until the melting temperature of the metal is reached. h_δ can be estimated using the following equation.

$$h_\delta = \sqrt{k_0 \left(\frac{\Delta T}{\dot{t}} \right) e^{-\left(\frac{E}{k_b T} \right)}} \quad (2.3)$$

Here k_0 is the growth constant, $\dot{t}$ is the heating rate, ΔT is the temperature difference between the initial temperature and the melting temperature, E is the activation energy, k_b is the Boltzmann Constant. The critical thickness versus heating rate plot for Au-Sn and Au-In is provided in Figure 2.1.

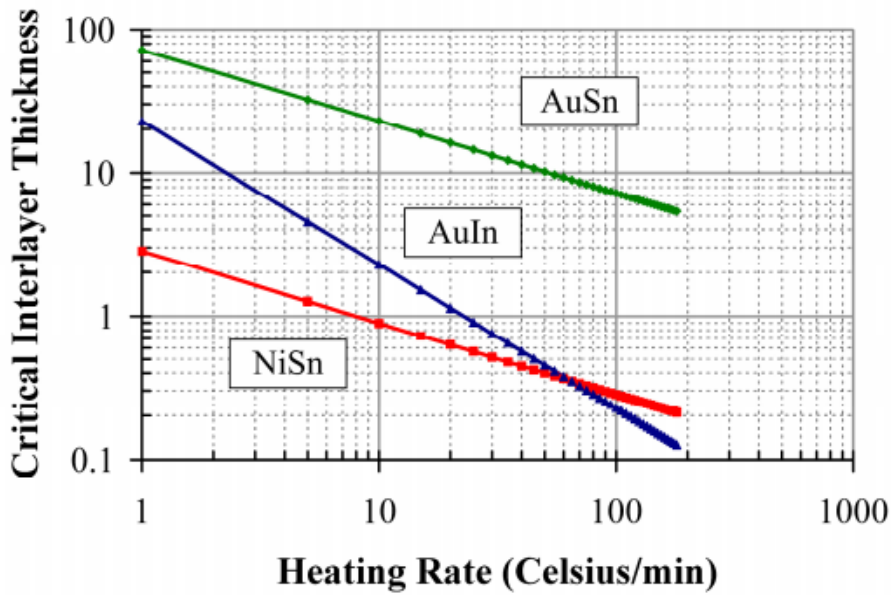


Figure 2.1: The critical thickness vs. heating rate plots of Au-In and Au-Sn [52].

2.1.2 Au-Sn Material System for TLP bonding

Au-Sn material system has a complicated phase diagram with many different intermetallic phases. The phase diagram is given in Figure 2.2. There are two eutectic reaction points in the Au-Sn binary phase diagram. One of them is Au-rich eutectic

point at 280 °C and 20 wt. % Sn, the other eutectic point is the Sn-rich eutectic point at 217 °C and 90 wt. % Sn. Au-rich and Sn-rich eutectic points are marked with yellow and green dashed lines, respectively, in Figure 2.2.

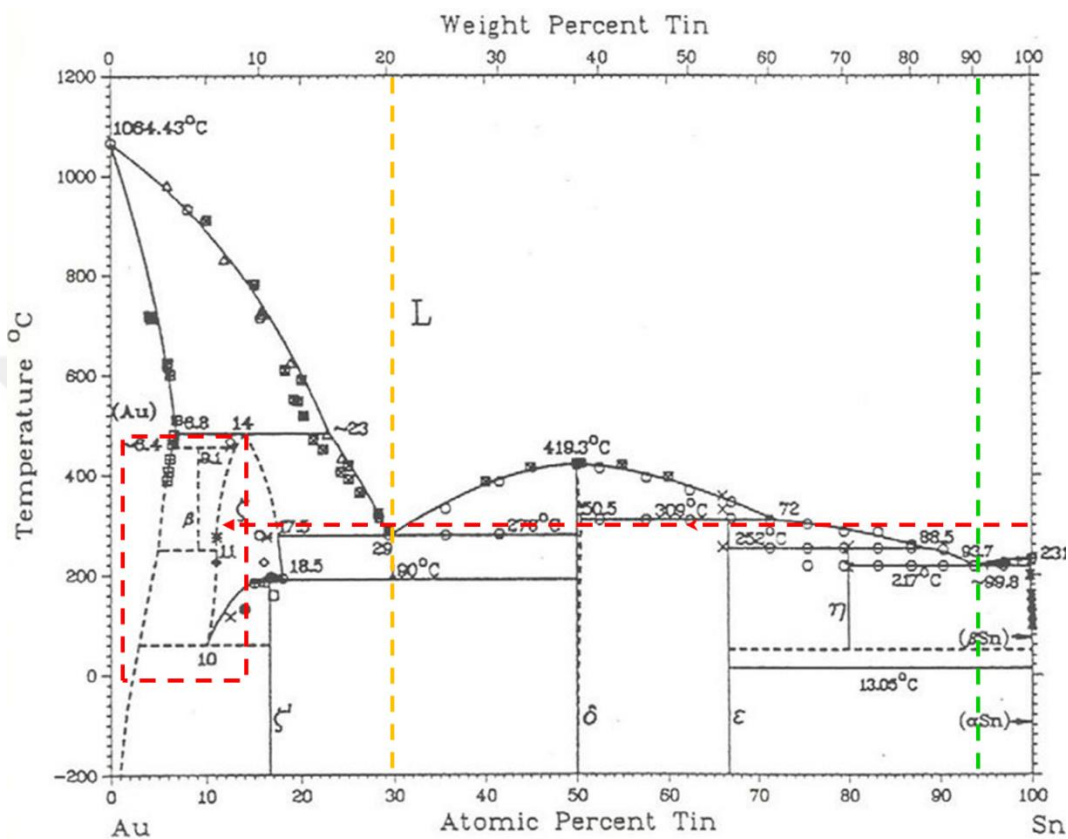


Figure 2.2: Gold-Tin phase diagram [53] two eutectic points are marked with yellow and green dashed lines, and the red dashed line shows the TLP bonding process.

Phase transformation during a TLP process starting from the liquid Sn phase is shown by the red dashed line in Figure 2.2. Initial heating provides liquefaction of Sn, and the diffusion process starts at that specific temperature increasing the gold content of the alloy following the dashed red line. When the cooling starts, the alloy is gold-rich, preferentially in the region drawn by the dashed red line, and the room temperature structure contains Au-Sn IMCs or gold-rich solid-solution depending on the final target composition. The re-melting point of the final composition in that region is higher than 500 °C.

There are significant problems in obtaining the liquid phase in the Au-Sn material system. The diffusion of Au into Sn is very rapid, and there is limited time for Sn to reach melting temperature and get melted. The critical thickness of the Au-Sn layer is very high for practical heating rates (45 °C/min for this thesis work). Using PVD deposition methods, it is exceptionally challenging and expensive to fabricate bonding metal for the TLP bonding method. As a solution for wafer-level packaging of MEMS devices using the TLP bonding method with ultra-thin metal layers that can be fabricated using PVD methods, the Au-Sn material system has been investigated with two different approaches. Both approaches utilize TLP bonding using different material designs and bonding process. In one approach, the Au-Sn material system has been used to have a TLP bonding, which implements the eutectic liquid as the liquid phase. In the other approach, the liquid phase obtained using elemental Sn applying an intermediate barrier layer between Sn and Au layers aiming to retard the interdiffusion between layers so that the Sn layer can have time to transform into liquid.

2.1.2.1 Au-Sn TLP Bonding with Eutectic Liquid

As reported in the literature review section, Au-Sn TLP bonding for wafer-level encapsulation of microelectronic devices is being performed with Sn as liquid phase, and with the relatively thick layers of metals (>8-10 μm in total). In TLP bonding with the eutectic liquid approach, the total thickness of the metals has been kept around 2 μm . The bond metal layers have been designed to have the eutectic liquid ($\text{Au}_{80}\text{Sn}_{20}$) as the liquid phase during the bonding process. It aimed to have the eutectic phase on the one wafer, and to increase the Au content of the alloy with an Au layer is deposited on the other wafer. Only gold deposition and patterning on the device wafer can be easier to integrate into the process flow. Thus, this configuration gives more flexibility for the device process integration. A schematic drawing of the bond metal configuration is provided in Figure 2.3.

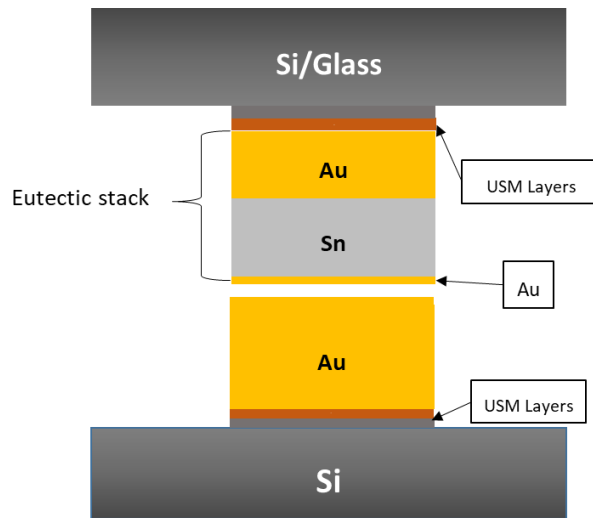


Figure 2.3: The schematic representation of the bond metal structure proposed for Au-Sn TLP bonding using eutectic liquid.

A very thin Au layer is deposited on the Sn layer to avoid the oxidation of Sn. The eutectic phase on the wafer is aimed to be formed using Au and Sn thin-film layers. Upon heating, the interdiffusion in solid-state will be completed to form the eutectic alloy with the composition of 20 wt. % Sn. When the eutectic temperature is reached, the phase transformation from solid to liquid takes place. The bond formation between the eutectic liquid and the solid Au layer occurs, and the Au-rich final alloy is obtained with a composition around 8 wt. % Sn. The final microstructure consists of Au-Sn IMCs at room temperature. The properties of the final phases determine the properties of the formed bond. The mechanical and thermal properties of the selected phases of the Au-Sn material system are given in Table 2.1.

Table 2.1: Properties of Selected Au-Sn IMCs.

Phase	Elastic Modulus (GPa)	CTE (ppm K ⁻¹)	T _{melting} (°C)
Au	77.2	14.4	1064
Sn	41	23	232
AuSn (δ)	70-101	14	419
Eutectic AuSn (δ - ζ' mix)	69-74	16	278
Au ₅ Sn (ζ')	62-76	18	190
AuSn _{0.18-0.10} (ζ)	58	20	519
Au ₁₀ Sn (β)	88	N/A	532

At the final target composition, the consistent phases are Au-Au₅Sn (ζ/ζ') at room temperature. Upon heating the final alloy, the whole structure turns to ζ -phase, having a melting temperature at 519 °C. The part of the phase diagram, including the final composition of the alloy, is given in Figure 2.4. The green dashed line corresponds to the heating of the final alloy.

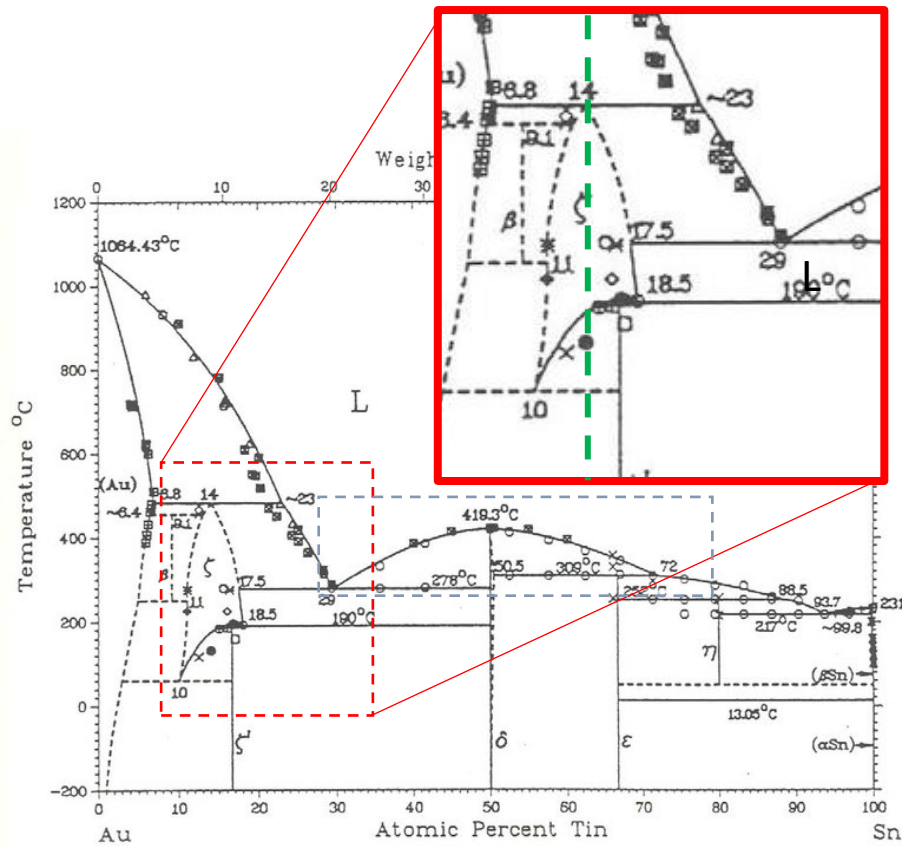


Figure 2.4: The part of the phase diagram aimed to have the final composition after TLP bonding with eutectic liquid. The dashed green line corresponds to the target final composition.

The eutectic stack of this material design consists of Au and Sn thin-films. The eutectic composition must be tuned carefully using the proper thicknesses. The required metal thicknesses can be calculated using Equation 2.1. According to calculations using Equation 2.1, the thickness ratio of Au/Sn layers needs to be 3/2.

Ti/Ni USM layers have been implemented for Au-Sn TLP bonding to provide good adhesion and barrier properties. Ti/Ni USM layers work well with this material system [54-56]. The tuning of the eutectic composition has been performed with three different Au/Sn stacks, which are 520nm/520nm, 520nm/500nm, and 520/490 nm.

2.1.2.2 TLP Bonding with Intermediate Barrier Layer

The other approach proposed in this work to enable Au-Sn TLP bonding in wafer-level employing ultra-thin metal layers is Au-Sn TLP bonding with an intermediate barrier layer. The design includes a thin intermediate barrier layer between the Au and Sn layers. The intermediate thin barrier layer aims to retard the inter-diffusion between Au and Sn. Therefore, during the heating in the bonding chamber, Sn will have more time to reach melting temperature before Au diffuses into Sn or vice versa and forms a high melting temperature alloy. The initial design of this approach implemented the eutectic stack on the barrier layer. Then the design has changed to have only the Sn layer on the barrier layer. This design aims at a bonding temperature close to the melting temperature of Sn. The design of the barrier layer and the bond ring can be seen schematically in Figure 2.5.

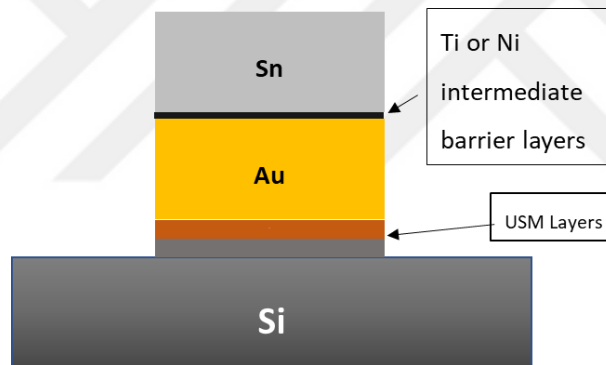


Figure 2.5: The schematic drawing of Intermediate barrier layer design in Au-Sn TLP bonding material stack.

In this design, the barrier layer should be chosen carefully. Ti and Ni are chosen as the intermediate barrier layers. Ni is known as an excellent barrier material, while Ti is not known for its barrier properties [56]. However, in this application, it is required that the material should retard the diffusion and also should allow the interaction with the underlying gold layer. The excess amount of barrier material will not allow the liquid Sn to interact with the Au layer, and a small amount of barrier material may not be able to act as a barrier. Different thicknesses of Ti and Ni layers have

been applied as a barrier material to optimize the barrier material. The thicknesses applied for the intermediate barrier layer are 20 nm Ni, 20 nm Ti, and 10 nm Ti. In this method, the USM layer does not contact with a liquid phase; therefore, the USM layer in this approach is less tricky than the eutectic liquid approach. The final composition is also aimed to be lesser than 10 wt. % Sn to have a re-melting temperature higher than 500 °C. The thickness of the layers in this method is not as critical as the eutectic liquid approach. However, the Sn layer thickness should be high enough to obtain liquefaction with the help of the barrier layer. As Sn thickness increases, Au layer thickness also must increase to keep the overall composition in the target range.

2.1.3 Al-Ge Material System for Eutectic Bonding

Al-Ge eutectic material is an auspicious material for MEMS packaging applications. It is a CMOS-compatible material due to its aluminum bond ring, which is already implemented in CMOS processing. Another importance of Al-Ge eutectic alloy is its potential to form bonds directly onto the insulating layers like SiO₂, SiN_x, and Al₂O₃[28, 57-58]. In this work eutectic composition of the Al-Ge material system has been implemented to have a bond directly to Si₃N₄ and Al₂O₃ surfaces. This bonding approach gives perfect flexibility for process integration, and it enables the integration of this method into a very high number of types of MEMS devices.

The Al-Ge binary phase diagram, which is not a complicated one with a single eutectic point, is provided in Figure 2.6. Al and Ge form a eutectic alloy at 51.6 wt. % Ge. The melting point of the eutectic alloy is 420 °C. Note that the solubility Ge and Al in each other is very low. The solubility limit of Ge in Al is 2.4 at. % and Al in Ge is 1.1 at. %. In eutectic composition at room temperature, the structure consists of Al and Ge composite structure.

In this work, Al-Ge eutectic alloy was fabricated using DC sputtering deposition method. The layer-by-layer deposition method has been implemented. The layer

thicknesses were initially calculated using Equation 2.1 and the bulk properties of Al and Ge. The calculated t_{Al}/t_{Ge} is 1.7. The layer thicknesses were optimized for exact eutectic composition. In the layer-layer deposition approach, the top layer is designed as Ge. The native oxide of Ge is less stable than the native oxide of Al. Ge layer is used as the cap layer on the material stack to have a more straightforward surface treatment. Note that Al-Ge eutectic alloy wets the SiO_2 surface, and it does not need a USM layer on the SiO_2 layer. Therefore, the layers are directly deposited on the SiO_2 layer. The Al/Ge layer combinations used for eutectic composition determination given in Table 2.2.

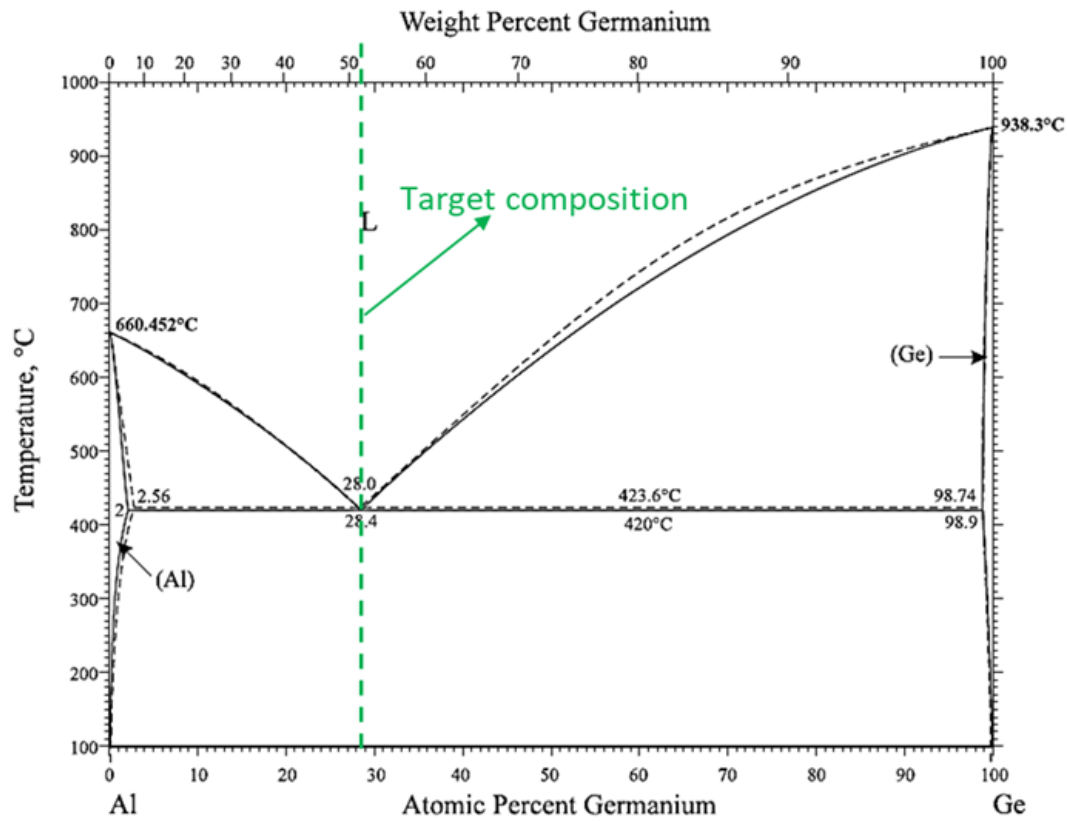


Figure 2.6: Al-Ge Binary Phase diagram and the eutectic composition marked with a green dashed line [59].

Table 2.2: Al-Ge layer combinations for eutectic composition optimization.

		Al	Ge	t_{Al}/t_{Ge}
	Stack 1	500 nm	300 nm	1.7
	Stack 2	500 nm	380 nm	1.3
	Stack 3	500 nm	400 nm	1.25

2.1.4 Au-In Material System

The Gold-Indium material system has a complicated phase diagram with many intermetallic phase formations. The material system has a eutectic point; however, the eutectic temperature of the system is 495 °C, which is a relatively high temperature for MEMS applications, especially for the CMOS-based MEMS devices. The low-temperature liquid formation can be obtained, having the melted indium as the liquid phase.

Thanks to indium's low melting temperature and high melting temperatures of IMCs in the Au-In system, the material system is a promising one for the low-temperature TLP bonding method. The phase diagram of the Au-In system is given in Figure 2.7(a). In the phase diagram, the region between AuIn and AuIn₂ intermetallics, marked in Figure 2.7(a), is very suitable for TLP applications. In this region, the re-melting temperature is 495 °C for a wide range of compositions. Therefore, minor composition variations do not affect the re-melting temperature of the final bond. Toleration of composition means that non-uniformity in the layer thicknesses can also be compensated. The variations in the composition will affect the AuIn and AuIn₂ amounts in the final structure.

The non-uniformity on larger wafers is usual. Therefore, this method may increase the yield of the packaging process on the larger wafers. In this work, the Au-In TLP

bonding was implemented on 6 inches wafers with a surface topography to investigate the surface topography compensation capability of the bonding method.

The USM layer of Ti/Ni was also applied for Au-In TLP bonding materials. Note that the USM layer does not contact with the liquid phase in this method. Also, the surface treatment was not applied for this material system.

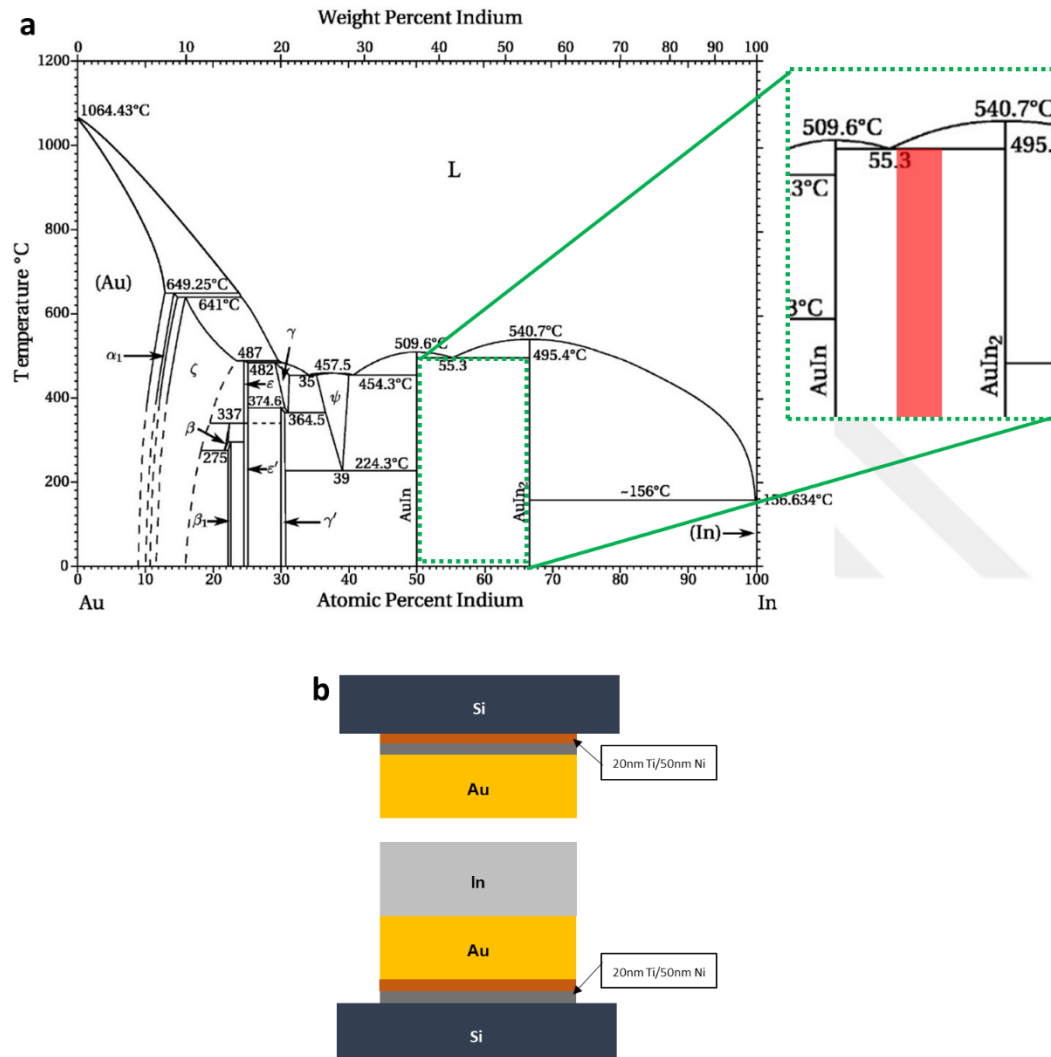


Figure 2.7: (a) Au-In phase diagram and (b) the bond material configuration.

2.2 Methods

2.2.1 Overview

Single side polished 4 and 6 inches Si wafers are used for bonding experiments for the development processes. The bond ring and cavity structures have been fabricated using microfabrication techniques. The integration of the developed bonding process into the device process requires extra steps. In this work, the integration of the developed process has been planned for CMOS based μ bolometer wafers. The flow of the bonding process integrated into μ bolometer wafers are presented in Figure 2.13

After the fabrication steps, the formed bonds have been characterized for their structural, mechanical properties. The dies with cavity have been tested for the hermeticity by He-leak test, the bonded wafers with cavity have been tested with the cap deflection method to observe the vacuum inside the cavity.

2.2.2 Microfabrication

Passivation Depositions

The fabrication of MEMS devices uses passivation layers as the surface finish. Thus, the bond materials should be optimized and deposited on passivation layers. SiO_2 or Si_3N_4 layers were deposited on the wafers by the PECVD system. 100-200 nm passivation layer was deposited onto wafers as the first step of the process. Passivation deposition has been performed with the STS PECVD system. Al_2O_3 layers for Al-Ge bonding were deposited using Atomic Layer Deposition (ALD) method. ALD system from Okyay Enerji A.Ş. was used for the depositions.

UV Lithography

The lithography step is the pattern generation step on the wafer. Photoresist polymers (PR) are exposed to ultra-violet (UV) light using the pattern mask in the contact mask

aligner and exposer system. Mask alignment and UV exposure have been realized with EVG 620 and EVG 6200 contact mask aligner and exposer systems. UV expose step of PI opening lithography of CMOS μ bolometer wafer was performed using ASML PAS5500 Stepper System. The pictures of the UV expose equipment can be seen in Figure 2.8. Lithography of the samples have been performed with the following steps,

- De-hydration baking at 110 °C in N₂ environment
- HDMS primer spinning coating
- Spin coating of photoresist (PR)
- Soft-bake on hotplate
- UV expose
- Development (etching of UV exposed PR in development solution)

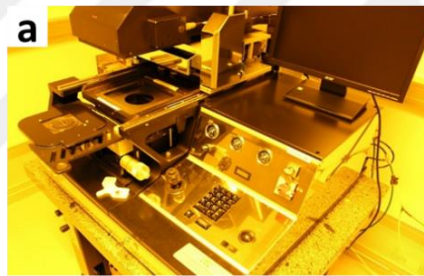


Figure 2.8: (a) EVG 620 Mask Aligner and (b) ASML PAS 5500 Stepper Lithography Equipment.

Metal Depositions and Lift-off

Metal depositions for the bond-ring formation have been realized with thermal evaporation and DC sputtering. Sn layers and thin (20 nm) gold layers were deposited in the Varian 3119 thermal evaporator system, and Indium layers were deposited in the Varian 3119 E-beam evaporation system. Thick gold depositions and USM layer depositions were employed in the AJA DC sputter system. For thermal evaporations of Sn layers, 5 Å/sec deposition rate was not exceeded. E-beam evaporation rate of In was kept around 20-25 Å/sec. Varian 3119 systems are 3 inches compatible systems, and they have been modified to use with wafer size up to 6 inches. Therefore, a non-uniformity is not an unexpected result for those depositions. The USM layers and Au layers under Sn and In layers are deposited using DC sputtering, and then the wafers are transferred for thermal and e-beam evaporation steps. The pictures of the sputtering and the thermal evaporation metal deposition equipments are given in Figure 2.9.

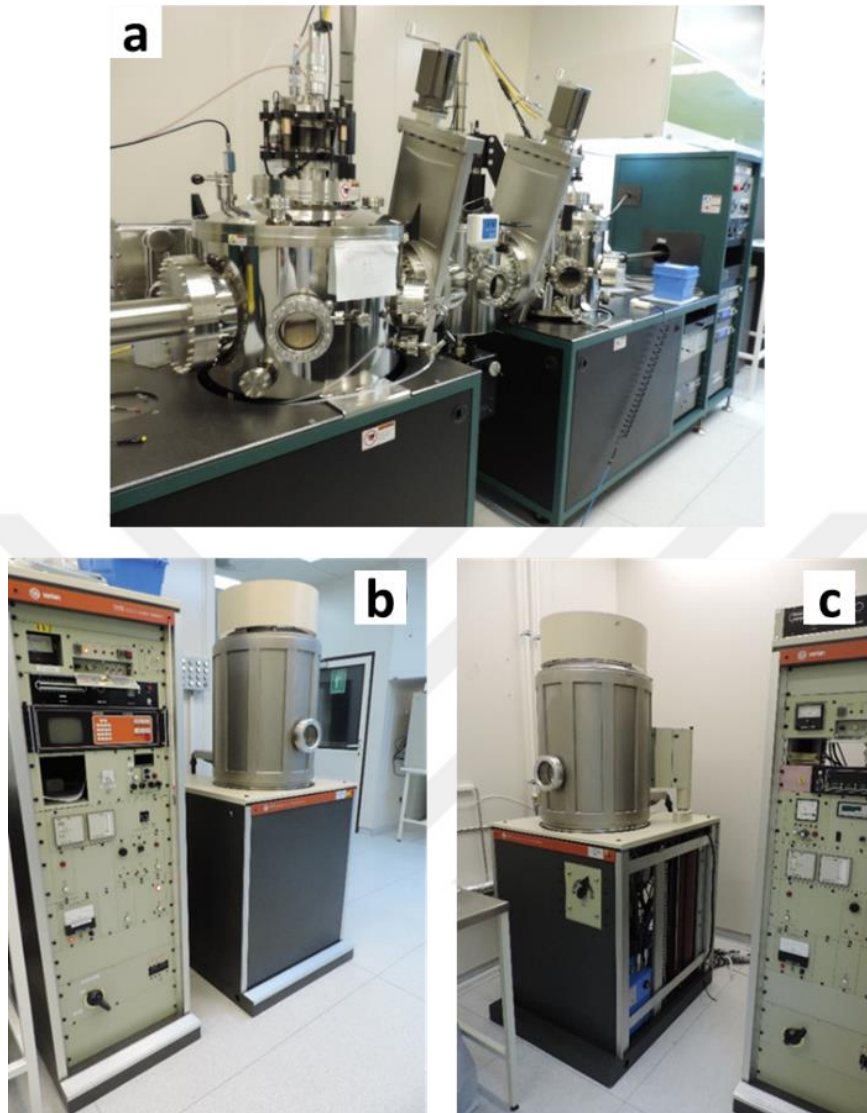


Figure 2.9: (a) AJA DC sputter system and Varian (b) e-beam and (c) thermal evaporators.

All metal patterning processes have been performed with the lift-off method in which the metal layer was deposited on the patterned PR layer. Then, the metal on PR layer was stripped in acetone, leaving the metal layers in the PR openings. A schematic drawing of photolithography steps and metal patterning lift-off is presented in Figure 2.10.

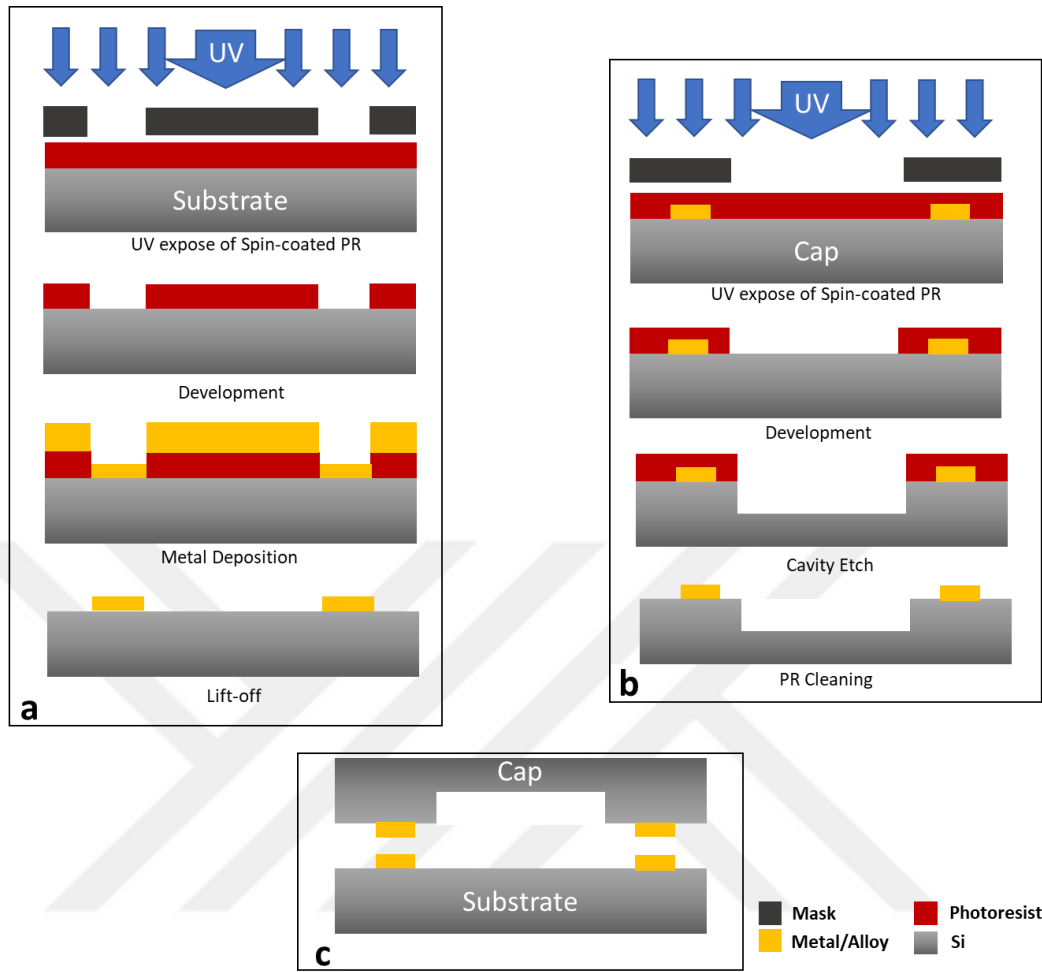


Figure 2.10: Representation of the process flow of (a) substrate and (b) wafer fabrication.

Cap Cavity Formation

Cap cavity formation of Si cap wafers was performed using the STS Pegasus DRIE system, Figure 2.11, with process gases of C_4F_8 and SF_6 . PR has been used as the mask layer during the DRIE process and was patterned with UV lithography. 100 μm deep cavities have been fabricated on cap wafers to obtain a vacuum cavity after the bonding. The cavity formation step starts just after the metal lift-off is performed. The PR layer has protected the metal layers during the cavity etching.



Figure 2.11: STS Pegasus DRIE system.

Cap Thinning

The observation of the vacuum inside the cavity of the bonded wafers has been realized using the cap thinning method. After the bonding process, the cap wafers were thinned using DRIE. STS Pegasus DRIE system was used for this thinning process. The DRIE process was performed without any protective layer on the wafers. The cap wafer was etched until the cap thickness is below 50 μm . The thinning must be performed in a controlled manner to stop at the desired thickness. Moreover, the excess heating during the process may cause the braking of the thinned cap wafer. So, a slow and controlled etching is crucial for this step.

Pre-Bonding Surface Preparation

This preparation step includes the oxide removal step for Al-Ge and Au-Sn material systems. Both wet and dry oxide removal processes have been applied for Al-Ge materials. Wet treatment was applied using BHF (1:7), Dilute-HF, NH_4F , and Dilute-HF: NH_4F solutions. The dry oxide removal process for both material systems

was performed by the Ar^+ reverse sputtering method. The oxide treatment steps were applied just before the bonding process. The die level sample surfaces were treated in SET FC150 Flip-Chip Bonder to observe the oxide reduction capability of formic acid (CH_2O_2) for the Al-Ge material system. Note that after the oxide treatment process, the metal surfaces were exposed to the atmosphere until they were placed in the bonding chamber.

Wafer Bonding & Dicing

The prepared wafers were aligned with each other using the EVG 6200 Bond Alignment System. After pre-bonding surface treatment, the alignment duration must be kept as short as possible to limit the exposure of the treated metal surface to the atmosphere. After the alignment, the wafers were placed into the bond chamber, and the bonding process was started with the determined temperature, force, and process environment parameters. Wafers were not at contact after the alignment process; a thin metal separator is inserted to avoid the contact of the wafers both before the evacuation for vacuum and reaching the bonding temperature. All the bonding processes were started from room temperature. The initial heating was applied in an inert gas atmosphere (instead of a vacuum environment), which is forming gas (5 % H_2 , 95 % N_2). The gas atmosphere provides effective heating thanks to convection in the chamber. TLP bonding methods are extremely heating rate dependent. Therefore, the equipment capability is very critical for the TLP bonding method. The maximum heating rate that can be applied by EVG 520 Wafer Bonder is 45 °C/min. EVG 520 wafer bonder system and a bonding profile applied during bonding can be seen in Figure 2.12.

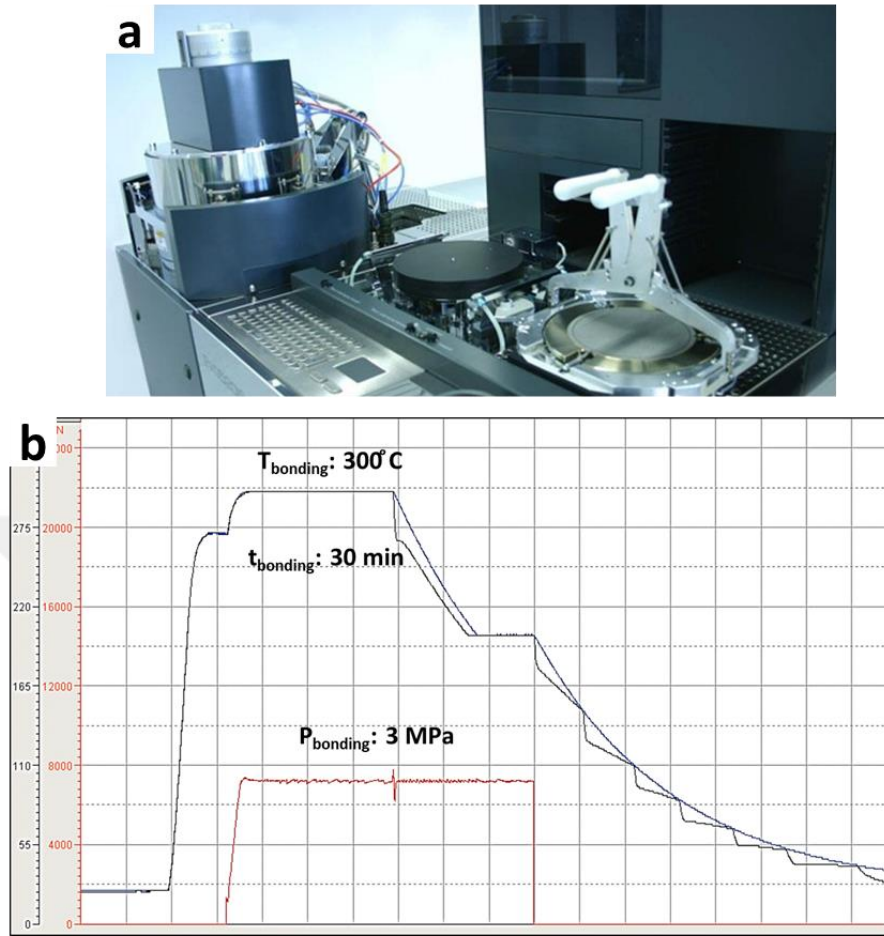


Figure 2.12: (a) EVG 520 Wafer bonder and (a) example bonding profile.

Integration of Bonding Processes into μ Bolometer Process

The integration of TLP bonding methods into μ Bolometer processes needs bond ring formation on the CMOS wafer, which has μ bolometer structures on it. Note that at the final step of the μ bolometer fabrication, the μ bolometer structure has suspended microstructures. These structures are extremely fragile. After the fabrication of μ bolometer structures finished, the structures could not withstand any further processing step, especially the wet processes are extremely hard to apply. Therefore, the bond ring formation step must be integrated before the fabrication is completed. Early deposition of the metals can result in defected bond ring metals due to the following device process steps. Therefore, the best step to integrate the bond ring

fabrication is just before the μ bolometer releasing step. The wafer surface has a polyimide (PI) layer at the final stage, and the structures are safe both mechanically and chemically. The PI layer was opened by lithography and O_2 plasma etching process to obtain a large opening for metal patterning. Then, the bond ring metal was patterned with lithography, deposition, and lift-off steps, as described in the Metal Deposition and Lift-off part of this section. The schematic process flow for the bond ring integration onto CMOS based μ bolometer wafer can be seen in Figure 2.13.

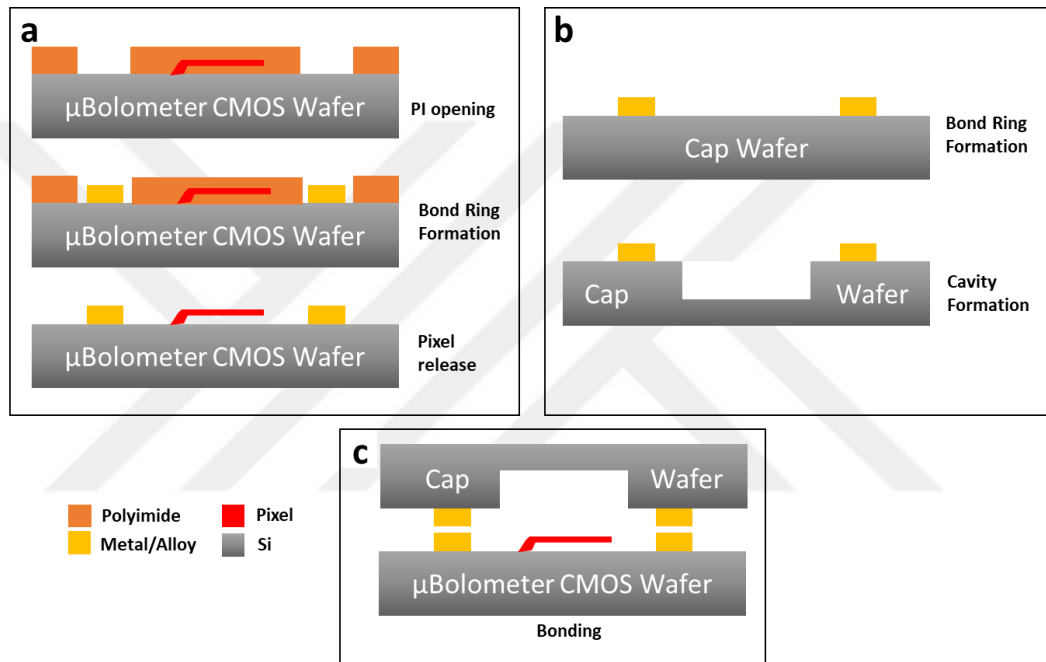


Figure 2.13: Process flow for the integration of bond ring on CMOS MEMS μ bolometer wafer.

2.2.3 Characterization

Thin Film Metal/Alloy Characterization

The metal layers have been characterized in terms of structural, chemical, and thermal properties. Structural and morphological properties of thin films were investigated with both optical microscope (OM), Veeco NT1000 optical surface profiler (OSP), JEOL 7500, FEI NOVA NanoSEM, and Hitachi Regulus 8230

scanning electron microscopes (SEM), Figure 2.14. Elemental analysis of the thin-films has been performed with energy-dispersive X-ray spectroscopy (EDS).



Figure 2.14: Hitachi Regulus 8230 SEM.

Thermal analysis of the thin films was performed using the differential scanning calorimetry (DSC) method. SEIKO SII X-DSC 7000 instrument, shown in Figure 2.15, was used for DSC characterizations. DSC characterizations were performed using 3mm x 3mm sized samples. The heating rate applied during the characterizations was 45°C/min to simulate the heating of EVG 520 Wafer Bonder.



Figure 2.15: SEIKO SII X-DSC 7000.

Structural and Mechanical Characterization of Bonds

After the bonding experiments, the bonds are tested both in wafer-level and die-level. The wafer-level structural test was performed with PVA TePLA SAM 301 HD² scanning acoustic microscope system (SAM), Figure 2.16(c). C-SAM imaging mode enables non-destructive investigation of the bond interface utilizing scanning of the sample by acoustic waves in water (DIW). C-SAM characterization reveals delamination at the bond interface. The minimum resolution with 200 MHz transducers is approximately 5-10 μm .

The mechanical characterization of the bonds was characterized by DAGE Nordson 4000 Bond Tester, Figure 2.16(a). The shear strength of the bonds was tested in die-level using 20 $\mu\text{m}/\text{sec}$ travel speed during the test. The maximum load that can be applied with this equipment is 1000 N. Shear strength for the microelectronic packages must have a minimum of 6 MPa Shear strength according to military standard MIL-STD 883 [51].

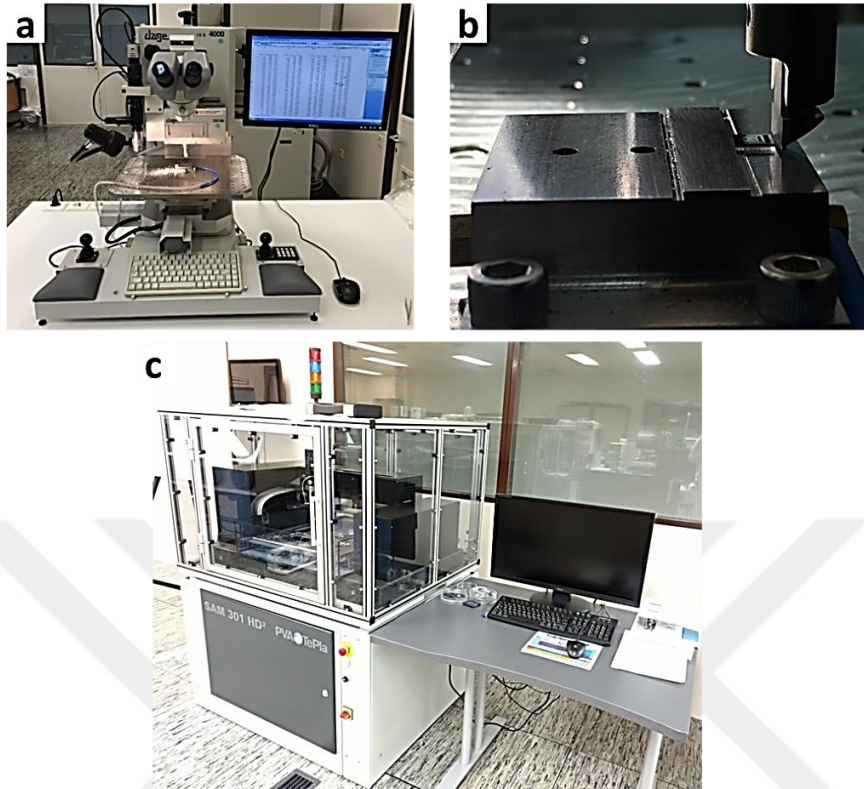


Figure 2.16: (a) (b) Dage Nordson 4000 Bond Tester and (c) PVA TePLA SAM 301 HD².

Hermeticity Characterization

The hermeticity characterizations in this work have been performed with the He-leak test and cap deflection method. Gross leaks were also observed during the SAM investigations. The dies with poor bond leaks DIW into the package during the SAM characterization.

He-leak test was performed according to MIL-STD 883 Method [51]. In this test, packages are bombed by He atoms in a pressure vessel during the specified bombing time. After the bombing time, the packages must be transferred into He-leak test chamber in allowed dwell time. In the chamber, He leaks from the package is measured by the leak detector. According to MIL-STD 883 standard, the tests must be performed with the parameters given in Table 2.3. The equipment used for the He-leak test is shown in Figure 2.17. The He-bombardment was applied in the

pressure vessel shown in Figure 2.17(a) at 75 psi for 16 hours. Then, the samples were placed in the test chamber shown in Figure 2.17(b) in a few minutes dwell time, and the chamber was pumped down for the He-leak test. The background reading of the test detector is $0.1 \times 10^{-9} \text{ atm. cc/sec}$.

Table 2.3: MIL-STD 883 He-Leak Test parameters [51].

Volume of package (V) in cm^3	Bomb condition			R ₁ Reject limit (atm cc/s He)
	Psia ± 2	Minimum exposure time hours (t_1)	Maximum dwell hours (t_2)	
<0.05	75	2	1	5×10^{-8}
≥ 0.05 - <0.5	75	4	1	5×10^{-8}
≥ 0.5 - <1.0	45	2	1	1×10^{-7}
≥ 1.0 - <10.0	45	5	1	5×10^{-8}
≥ 10.0 - <20.0	45	10	1	5×10^{-8}

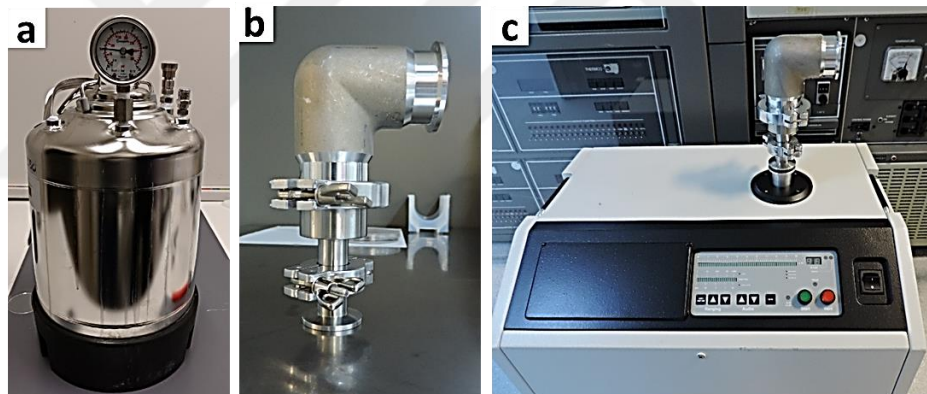


Figure 2.17: (a) The pressure vessel for He bombardment, (b) test chamber, and (c) He-leak detector.

Table 2.4: He-Leak Test conditions.

He Bombardment Pressure	75 psi
Bombardment Tim	16 h
Dwell Time	1-5 min
Package Volume	0,006 cc

CHAPTER 3

RESULTS AND DISCUSSIONS

3.1 Al-Ge Eutectic Bonding

Adjustment of Eutectic Composition

The composition adjustment for the Al-Ge eutectic bonding was performed using the material thicknesses given in Table 3.1. These wafers were fabricated using DC sputtering, and annealing was performed in the bonder chamber at 440 °C for 1 h. The samples were investigated using SEM and EDS analysis after the annealing. The SEM images and the EDS results of the samples are provided in Figure 3.1. The results of the annealing and characterization are summarized in Table 3.1.

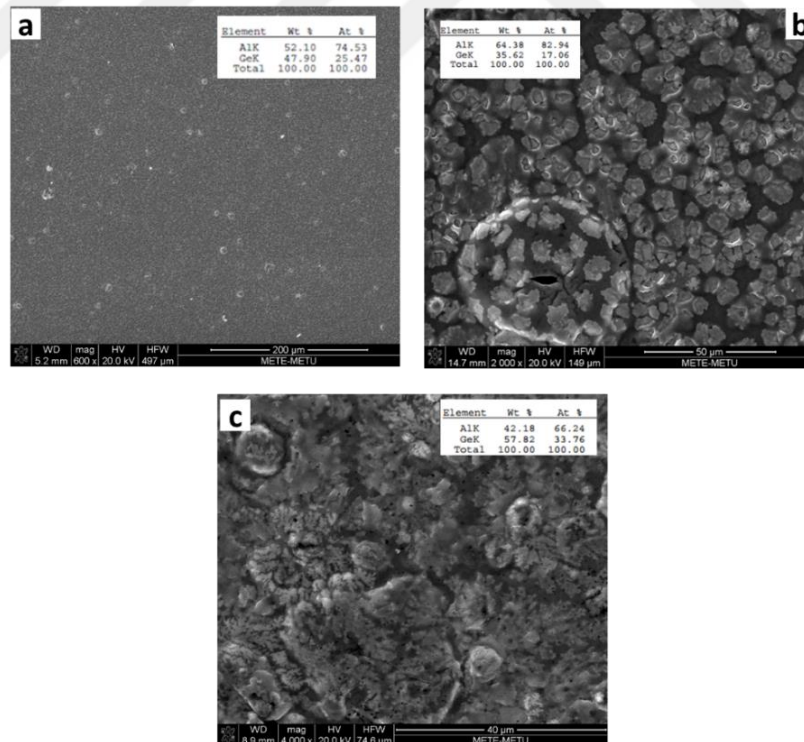


Figure 3.1: SEM images of (a) Stack 1, (b) Stack 2 and (c) Stack 3 after annealing.

Table 3.1: The Al-Ge layer combinations and results for eutectic composition optimization.

	Al	Ge	Annealing	EDS wt.%Ge
Stack 1	500 nm	300 nm	440 °C -1h	35
Stack 2	500 nm	380 nm	440 °C -1h	48
Stack 3	500 nm	400 nm	440 °C -1h	57



According to the EDS results the Stack 3 is chosen as the bond material stack for bonding experiments.

Bonding Experiments without Surface Treatment

Stack 3 has been implemented in the wafer bonding experiments. The initial bonding experiments were performed without any surface treatment. It has been aimed to have the oxide layers to be broken by the pressure during the bonding process. Two wafers with eutectic stack were bonded to wafers with top surface is SiN_x and Al_2O_3 . The bonding was performed with 3 MPa bonding pressure at 440 °C for 30 minutes. The first samples were tested with the cleaving method by hand. The images of broken samples of Al-Ge bonding to Si_3N_4 and Al_2O_3 can be seen in Figure 3.2 and Figure 3.3, respectively.

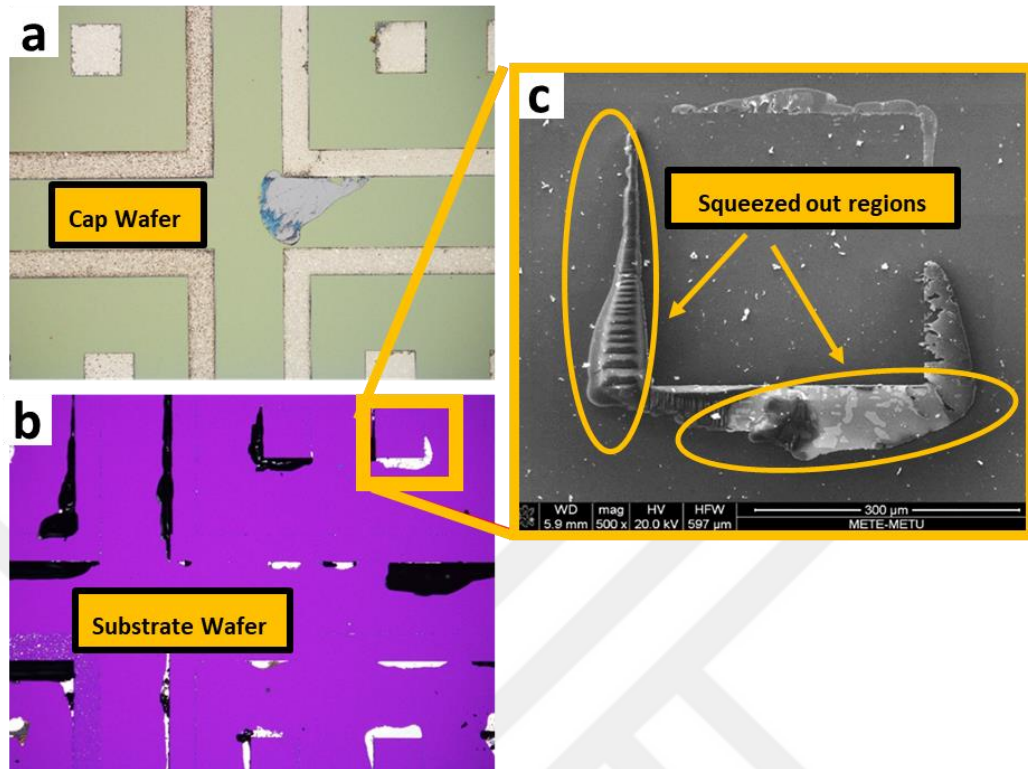


Figure 3.2: Al-Ge bonding on Si_3N_4 after cleavage (a) Cap wafer, (b) Substrate wafer, and (c) SEM image of the squeezed-out metal.

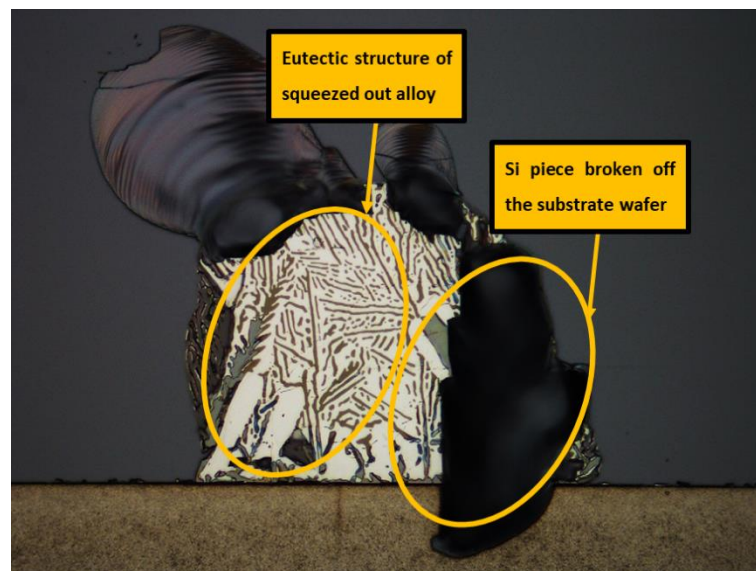


Figure 3.3: Al-Ge bonding on the Al_2O_3 surface after cleavage.

As can be seen in Figure 3.2 and Figure 3.3, the bond ring regions of the Al-Ge material did not interact with the substrate surface. However, the squeezed-out liquid metal was bonded to the substrate surface strongly. The Si pieces from the substrate surface were also broken off during the cleavage. Squeezed-out Al-Ge eutectic liquid strongly bonded to both Si_3N_4 and Al_2O_3 surfaces.

Surface Treatments of Al-Ge Eutectic Stack

The lack of interaction of Al-Ge material with the substrate surfaces on the bond ring region has been attributed to surface oxides on the bond material. The XPS measurement was performed for the oxide layers on the bond ring material after deposition. The XPS data in Figure 3.4 shows that there is Ge oxide for a sputtering depth of 10 nm, which corresponds to a native Ge oxide thickness of approximately 10 nm.

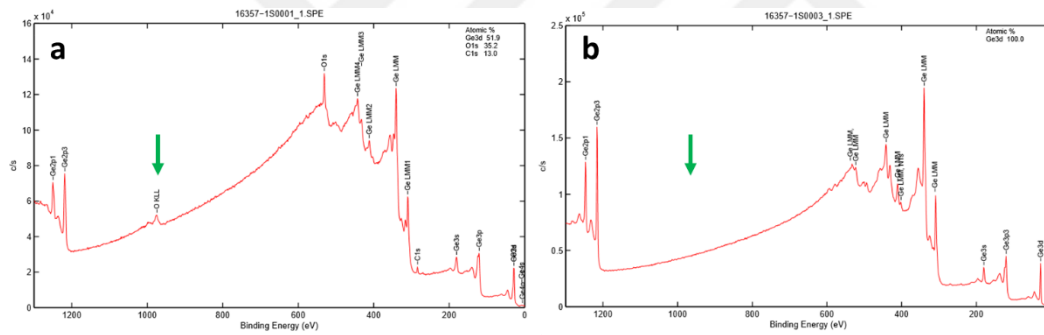


Figure 3.4: XPS data obtained from the Al-Ge as-deposited sample (a) as-deposited surface (b) after 10 nm sputtering.

The wet treatments were applied with the following chemicals, given in Table 3.2, to avoid the oxide layer before bonding.

Table 3.2: Wet treatments applied for Al-Ge oxide removal.

No	Solution	Duration
1	dilute HF (50:1)	10 sec
2	BHF (1:7)	1 min
3	NH ₄ F	1 min
4	HF-NH ₄ F	10 sec

After each wet treatment given in Table 3.2, samples were immediately transferred into the bond chamber to be annealed at 460 °C for 15 minutes in a vacuum environment. The optical microscope images of surface conditions after the annealing is provided in Figure 3.5.

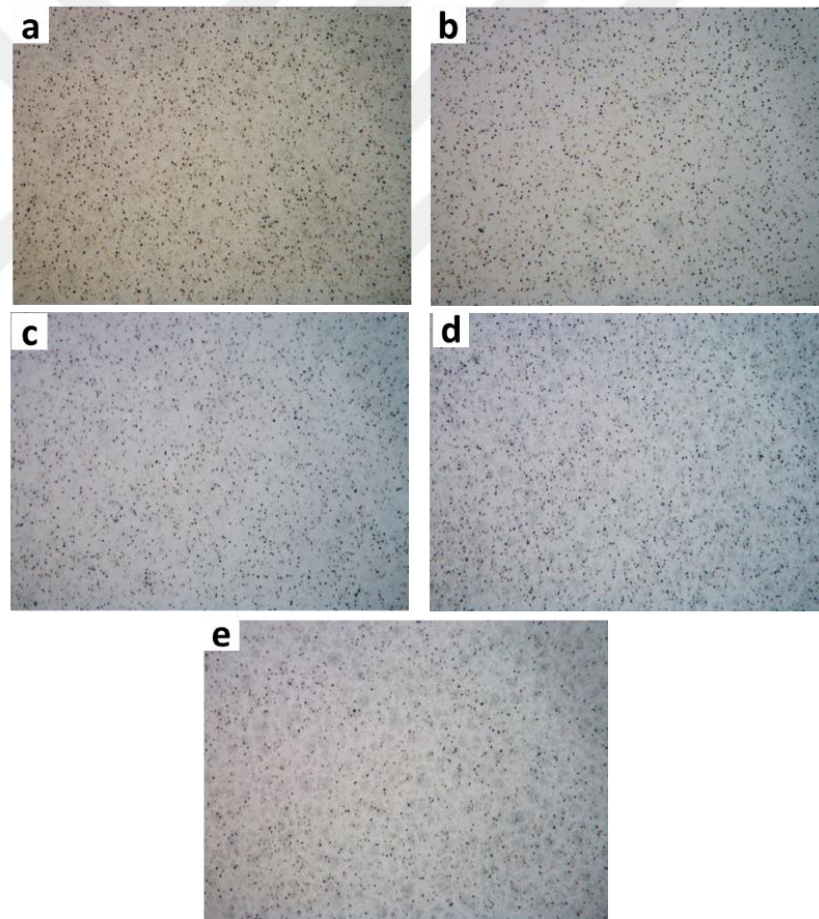


Figure 3.5: Al-Ge Eutectic samples annealed at 460 °C for 15 minutes in vacuum environment, (a) As deposited sample and after treatment of (b) dilute HF (50:1) for 10 sec, (c) NH₄F for 1 minute (d) HF-NH₄F for 10 sec (e) BHF (1:7) for 1 minute.

After wet surface treatments, a clear two-phase structure of the Al-Ge eutectic could not be obtained. The BHF treatment provided a surface closest to a two-phase structured surface. The SEM image of the BHF treated sample is provided in Figure 3.6.

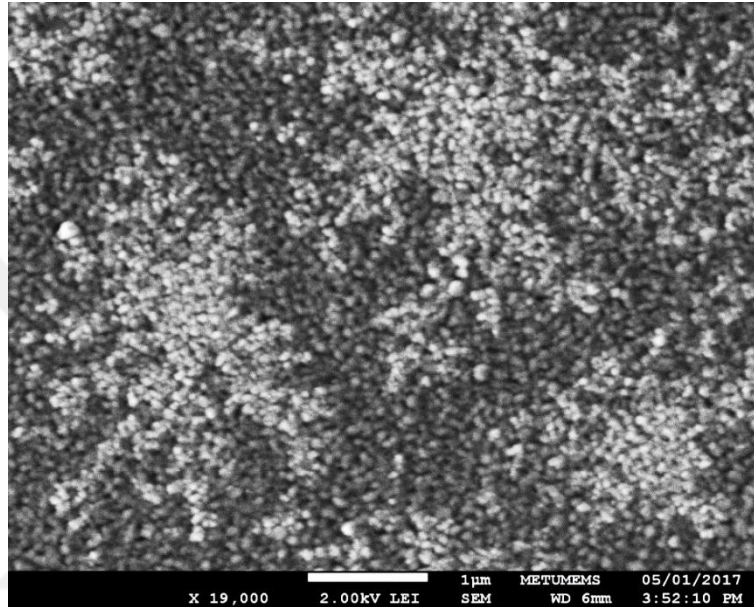


Figure 3.6: The SEM image of BHF treated Al-Ge eutectic material after annealing at 460 °C for 15 minutes in a vacuum environment.

After wet treatments, Ar^+ reverse sputter has been applied as the native oxide removal method. The metal surface was cleaned with sputtering using Ar^+ plasma with 300 W power and 3.5 sccm Ar flow for 60 sec. The cleaned sample was annealed at 460 °C for 15 minutes. The SEM images of the as-deposited and after cleaned is given in Figure 3.7.

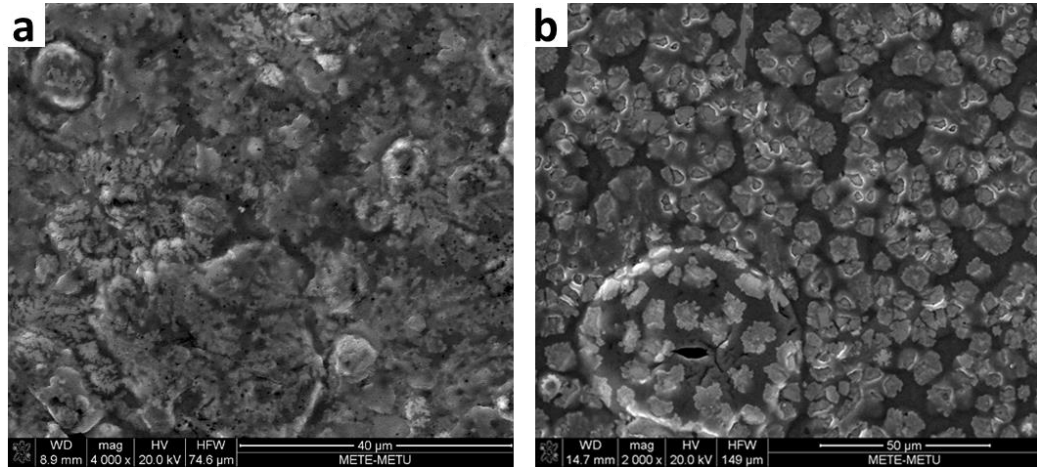


Figure 3.7: Al-Ge Eutectic material samples after annealing at 460 °C for 15 minutes (a) as-deposited and (b) cleaned sample with 60 sec Ar reverse sputtering.

The cleaning with Ar reverse sputtering has provided a better result than the wet treatments. The two-phase structure was more apparent than the as-deposited sample after the annealing process. However, note that the sample must expose the atmosphere until the bond alignment and transfer into the bond chamber is realized.

As another dry oxide treatment method, a die level sample was annealed in a formic acid environment at 460 °C for 5 minutes. The SEM image of the alloy after the annealing is provided in Figure 3.8. The eutectic structure can be seen clearly in the figure. The formic acid treatment can be the right choice for the oxide treatment of the Al-Ge alloy. Although there are commercially available bonder systems that allow formic acid treatment in the bond chamber, the system used in this work does not have a formic acid treatment option.

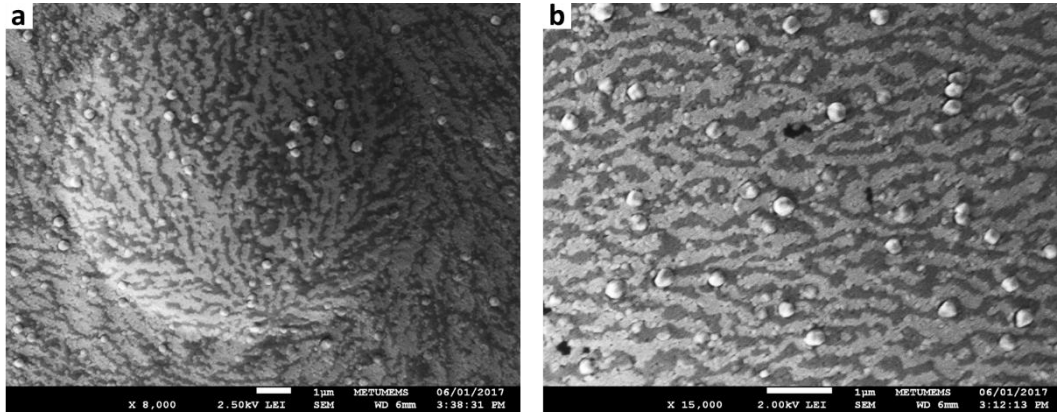


Figure 3.8: SEM images of Al-Ge alloy annealed in a formic acid environment at 460 °C for 5 minutes.

Bonding Experiments with Surface Treatment

The bonding experiments with the Ar^+ reverse sputter cleaning have been performed using the bond configuration given in Figure 3.9. The bond ring material was patterned with the lift-off method. The bonding process was performed in a vacuum environment at 440 °C for 30 minutes, with 3 MPa bonding pressure.

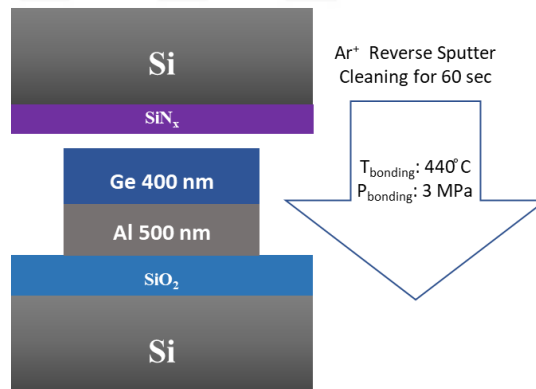


Figure 3.9: Al-Ge Eutectic bonding configuration applied with Ar^+ reverse sputter cleaning.

The bonded wafers were characterized by SAM just after the bonding experiments. The SAM image of the bonded wafers is provided in Figure 3.10. The SAM image has revealed some defected regions near to the edge of the wafers. These defected regions may have resulted during the fabrication. The inset in Figure 3.10 shows that

there are some squeezed-out metals around the bond rings. The squeezed-out metals are the sign of the liquid metal that had been obtained during the bonding.

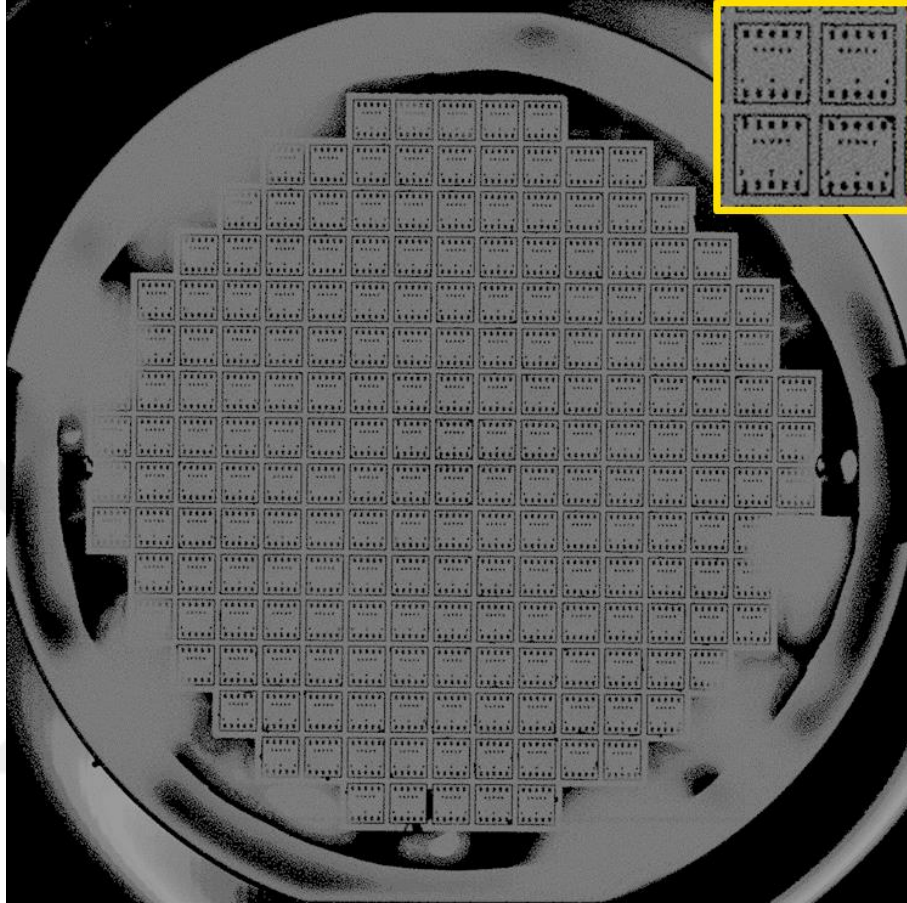


Figure 3.10: SAM image of Al-Ge eutectic bonding performed with Ar^+ reverse sputter cleaning before bonding.

Note that Ar^+ reverse sputter cleaning was performed in the sputtering system, and the wafers are transferred in atmospheric conditions for bond alignment. There is a duration in which wafers are exposed to air after the cleaning. The same bonding was performed with the identical layers and parameters shown in Figure 3.8, aiming to keep the air exposure duration as short as possible. The SAM image of the bonded wafers is given in Figure 3.11.

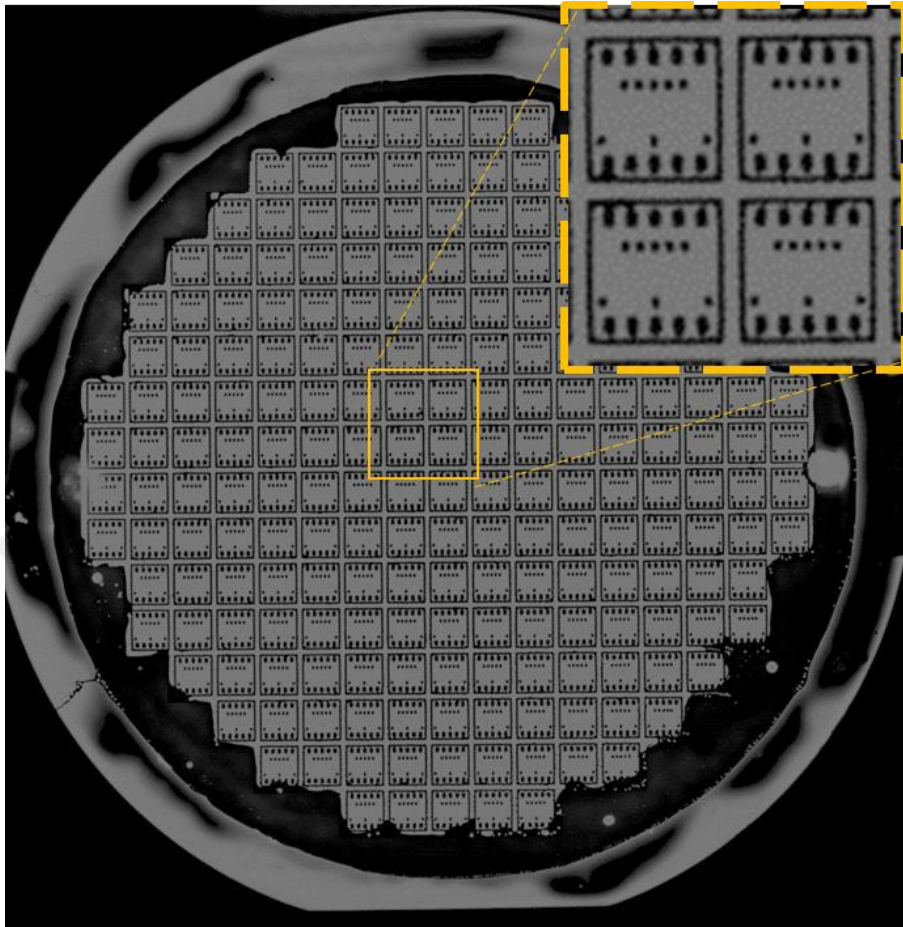
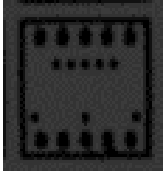
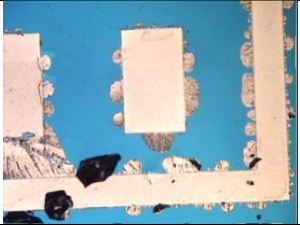
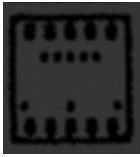
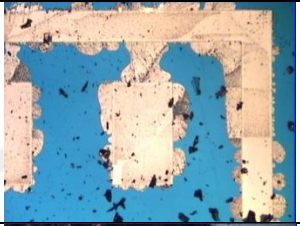
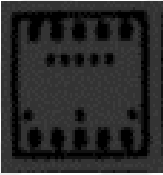
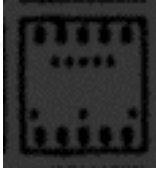
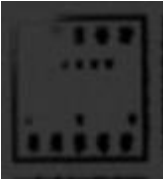
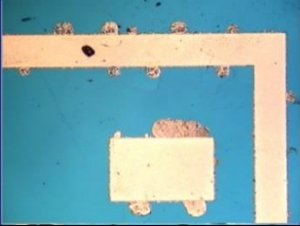


Figure 3.11: SAM image of repeated Al-Ge eutectic bonding performed with Ar⁺ reverse sputter cleaning before bonding.

The SAM image of the repeated bonding does not have defected regions. The squeezed-out metal amount in this bonding experiment is more than the previous bonding experiment. These results are attributed to shorter air exposure of the wafer between the cleaning and bonding steps of the fabrication. The wafer has been diced to perform the shear tests of the dies. During the dicing, all of the dies were kept bonded, which is the initial sign of a strong bond. The shear test results of selected dies and their optical microscope images are presented in Table 3.3.

Table 3.3: Shear Test Results of Al-Ge Eutectic Bonded samples

Position	SAM Image	Shear Strength	Optic Microscope Image
1		75 MPa	
2		97 MPa	
3		97 MPa	
4		96 MPa	
5		16 MPa	

As can be seen in Table 3.3, the shear strength of the dies is much higher than the requirement of MIL-STD 883, which is 6 MPa. Die number 5 in Table 3.3 has a lower shear strength value than the others. However, the SAM image of the die also has some defected region at the die corner. The low shear strength of this die has been claimed to be caused due to the defect. The SEM images after the shear test are provided in Figure 3.12. It can be easily seen that the bond material could not interact

with the Si_3N_4 surface of the substrate on the bond ring region, and the bond metal has been kept on the cap wafer completely. However, there are large Si substrate pieces broken from the cap or substrate wafers. The squeezed-out liquid metal probably bonded onto the Si_3N_4 surface very strongly and broke off the Si substrate during the shear test. The high shear strength values in Table 3.3 are likely due to this strong bond of squeezed-out metal.

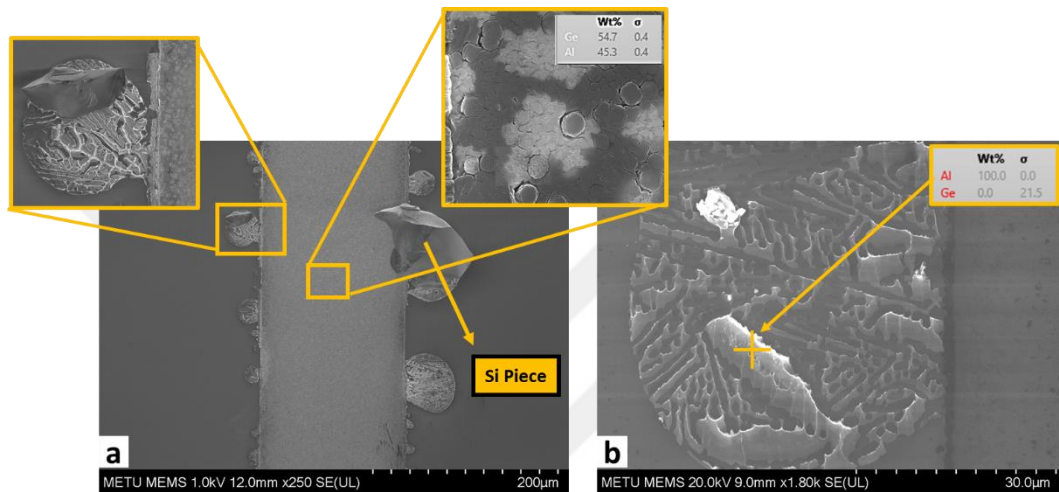


Figure 3.12: The shear surface of the dies after the shear strength test, (a) the bond surface of the cap die with bond ring material and (b) The bond surface of the substrate die.

The EDS measurement from the bond material on the cap wafer yielded 54.7 wt. % Ge which is very close to the aimed final composition. The EDS result of the squeezed-out eutectic metal with dendritic structure yielded higher Ge content than the eutectic composition. When the substrate wafer has been investigated, it was observed that some squeezed-out and bonded metals are present on the surface. The EDS result of the bonded metals yields 100 % Aluminum. It can be concluded that the Al-rich part of eutectic alloy bonds more strongly to the Si_3N_4 surface. The reason for the shift from the eutectic composition of the squeezed-out metal has been attributed to Al content that has been kept on the substrate surface during the shear test.

To sum up, Al-Ge eutectic liquid forms a strong bond with the widespread passivation layers implemented on MEMS devices such as Si_3N_4 and Al_2O_3 . The oxide treatment requirement makes it challenging to apply to wafer-level processes. In-situ treatment methods like reverse sputter Ar^+ plasma cleaning and formic acid treatment can be an effective solution for this method.

3.2 Au-In TLP Bonding

Defining the Bonding Configuration

Au-In TLP bonding experiments are designed to have a strong bond with 6 inches wafers, which have surface topography on it. Note that this bonding method does not require fine-tuning of the metal layers, as described in Section 2.1.4. There is not a specific target composition; there is a target composition range for this material. So the thickness calculation according to Equation 2.1 should be enough. The designed asymmetric bond configuration is given in section 2.1.4. The bond configuration with the designed thicknesses is shown in Figure 3.13.

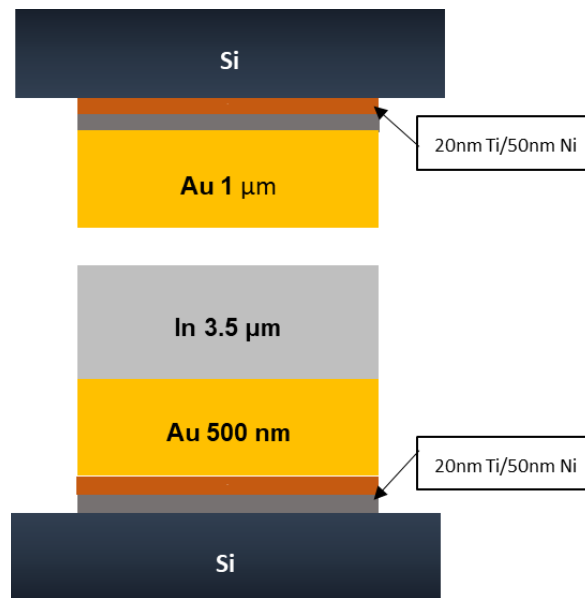


Figure 3.13: The asymmetric bond configuration applied for the Au-In TLP bonding.

Application of Surface Topography to Simulate Device Wafer

The surface topography of the wafers was fabricated with RIE etching of 200 nm Si_3N_4 layers. The optical microscope of surface topography with the gold layer on it can be seen in Figure 3.14.

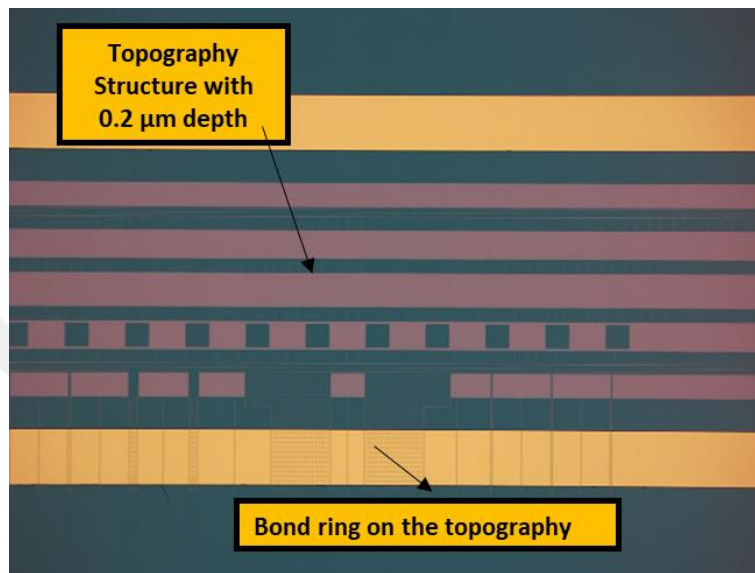


Figure 3.14: The topography formed on the 6 inches wafer with a gold bond ring on it.

Formation of Bond Ring Metals

After the formation of the topography and gold layer, the wafer was transferred to the e-beam evaporator to deposit the indium layer. E-beam evaporator provides high deposition rates; however, the high deposition rates result in porous material structures. The SEM image of the deposited indium layer on the topography and gold layer is shown in Figure 3.15(a)(b). The porous structure of indium can be seen in Figure 3.15(b). The optical profiler measurement given in Figure 3.15(c) shows the 3D measured model of the bond ring, and the 2D measurement shows the deposition thicknesses, which is 3.3 μm .

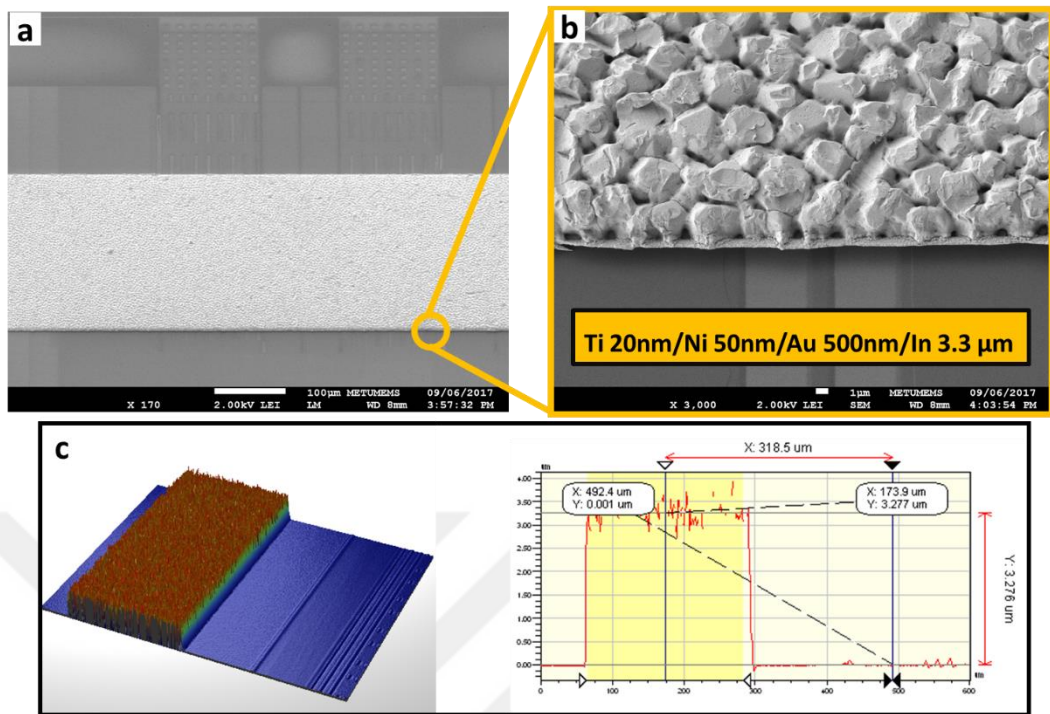


Figure 3.15: (a) SEM images of the Indium layer deposited on the topography formed on Si_3N_4 and (b) optical profiler measurement of deposited indium layer.

Process Integration Development for Suspended MEMS structure

In terms of process integration point of view, the Au layer on other wafer was fabricated, developing a dummy PI opening process. PI opening and metal deposition processes have been developed for the integration of process into MEMS devices processes that use PI as the sacrificial layer. 2 µm PI layer was spin-coated on the wafer. It has been opened with the lithography and RIE etching steps. After the PI opening, the Au layer was patterned by the lift-off process in the opening. The schematic presentation of the process was given in Figure 3.16(a). The patterned Au layer in the PI opening can be seen in Figure 3.16. Wafer with PI opening and deposited gold layer can be seen in Figure 3.16(b) and 3.16(d), and their microscope images can be seen in Figure 3.16(c) and 3.16(e), respectively.

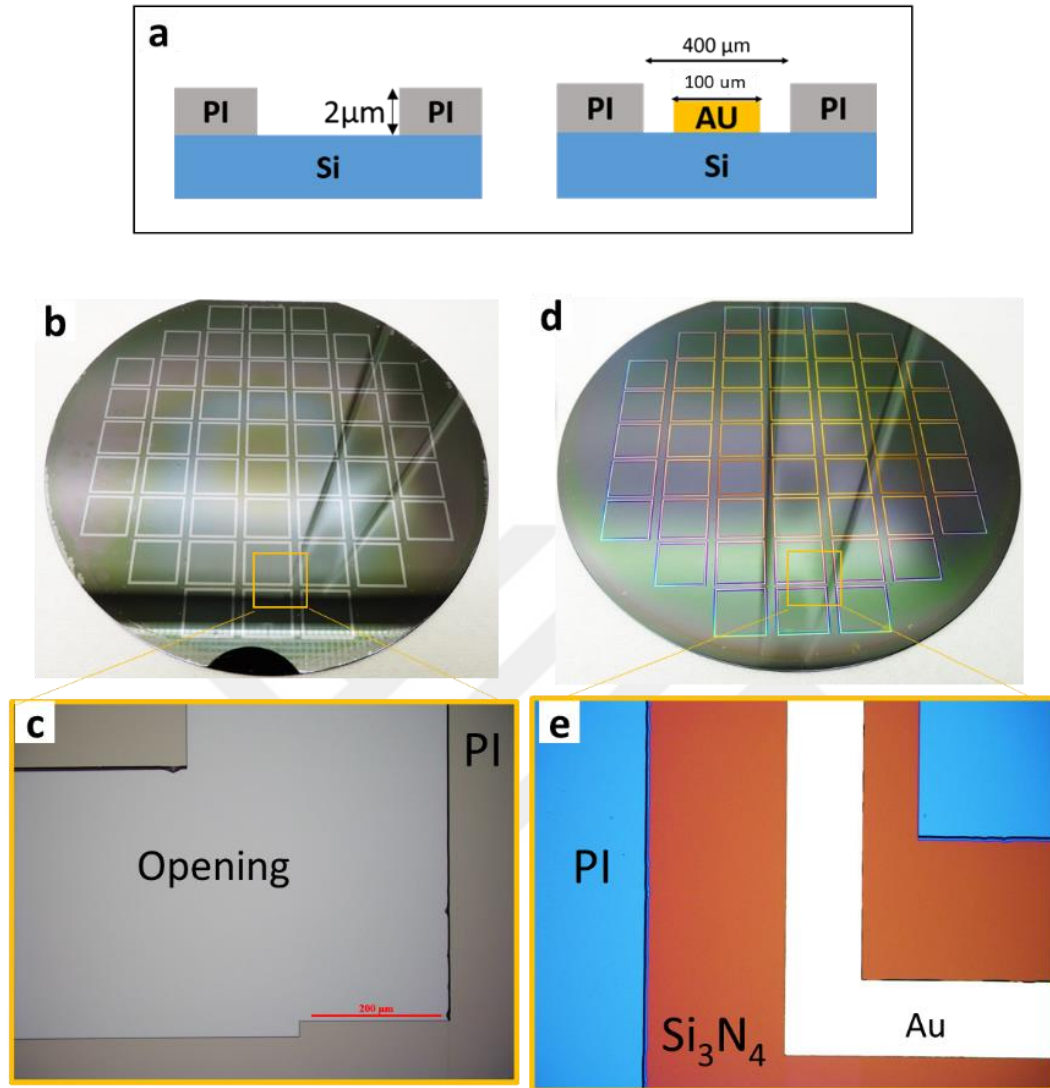


Figure 3.16: The PI opening and bond ring formation on 6 inches wafer for the integration step of metal bonding for suspended MEMS device wafers. (a) Schematic representation of the process, (b) PI opened wafer, (c) OM image of the opening, (d) Au deposited wafer, and (e) OM image of the Au deposited into the opening.

Bonding Process and Characterization of Bonded Wafers

The bonding of the fabricated wafers was performed at 200 °C with 3 MPa bonding pressure. The surface treatment for the bond metals was not applied for these materials and note that the e-beam evaporator does not allow to deposit a thin Au cap layer to protect the indium from oxidation. The SAM investigation of the bonds

has been performed at the die level. The SAM image of a die from the wafer center is provided in Figure 3.17.

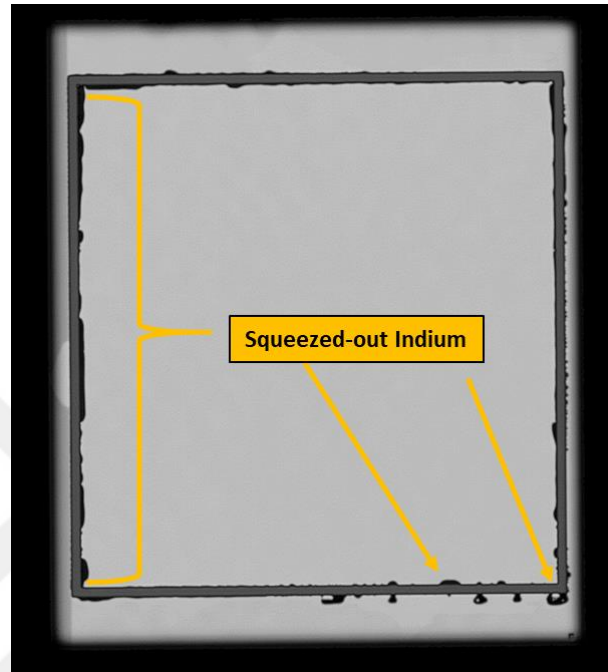


Figure 3.17: SAM image of a die from the wafers bonded with the Au-In TLP bonding method.

There is no delamination in the bond ring in the SAM image. Some squeezed-out metal is present around the bond ring material. 3 MPa bonding pressure is suitable for this bonding configuration in terms of squeezing of liquid metal. The diced dies were tested for the shear strength. Most of the tested dies could not be broken by the shear tester, which is capable of applying 1000 N. There were a few dies that are broken at an applied force of 800-980 N, which corresponds to a shear strength value of 40-50 MPa. The SEM top-view image of the shear surface of a broken die is provided in Figure 3.18.

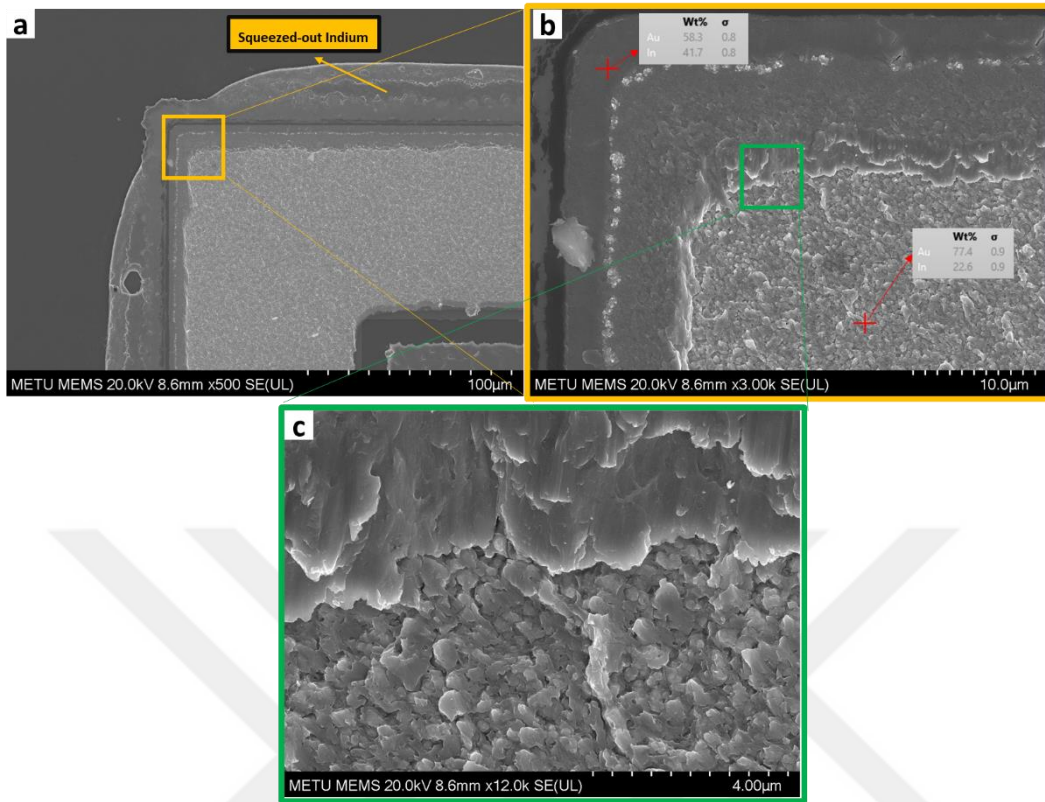


Figure 3.18: SEM images of the shear surface of Au-In TLP bonding.

The squeezed-out indium can be seen clearly in Figure 3.18(a). There is a very narrow, a few micrometers broad, region on the shear surface. There is a highly deformed region at the rest of the bond ring. The deformation seems more like a ductile fracture with dimples and cones. The EDS measurement from the narrow region, which has bulk bonding material, yielded 42 wt. % In. The measured value is very close to the aimed composition for the total. The EDS measurement from the deformation region yielded 77.4 wt. % Au. The failure of the bond has likely occurred from the AuIn intermetallic.

The Hermeticity of the dies was tested with the He-leak test method. The measured He-leak test of the dies was $1 \times 10^{-8} \text{ atm. cc/sec}$. This value is lower than the limit of MIL-STD 883 standard, as given in Table 2.3.

As a summary, the Au-In material system is a promising one for the low-temperature TLP bonding. The bond is strong enough and hermetic. The asymmetric bond

material configuration makes the method suitable for the integration into device processes. However, the thick indium layer in the material configuration makes it relatively a costly method.

3.3 Au-Sn

As described in Section 2.1.2, the Au-Sn material system has been implemented for two different TLP bonding designs, Au-Sn TLP bonding with eutectic liquid and Au-Sn TLP Bonding with Intermediate Barrier Layer.

3.3.1 Au-Sn TLP Bonding with Eutectic Liquid

Eutectic stack thickness and composition optimization

The thicknesses of Sn and Au to obtain eutectic composition can be calculated using Equation 2.1 given in Section 2. The equation uses the bulk material densities for the calculation. The calculated thickness ratio t_{Au}/t_{Sn} is 3/2. However, the PVD thin film deposition methods like sputtering and thermal evaporation can grow in different modes according to the deposition and surface conditions (such as surface temperature, roughness, and shadowing) [60]. The structure of the thin film can vary, and it is not an unexpected situation to have lower densities than the bulk material. The cross-sectional and top-view SEM image of the as-deposited Sn layer is given in Figure 3.19. The layer is rough with its granular structure. Therefore, the calculated film thicknesses may not yield the desired composition. The three different material stacks with varying t_{Au}/t_{Sn} which were given in Table 3.4 have been deposited for the eutectic composition adjustment. The SEM images and corresponding EDS results of the microstructure of each stack after annealing at 300 °C for 30 minutes is provided in Figure 3.20.

Table 3.4: The Au/Sn stacks used in the Au-Sn eutectic composition optimization.

	Au/Sn Stack 1	Au/Sn Stack 2	Au/Sn Stack 3
Sn Thickness	520 nm	450 nm	490 nm
Au Thickness	520 nm	520 nm	520 nm
Au:Sn Ratio	1	1.2	1.1
Annealing Condition	300 °C -30 min	300 °C -30 min	300 °C -30 min

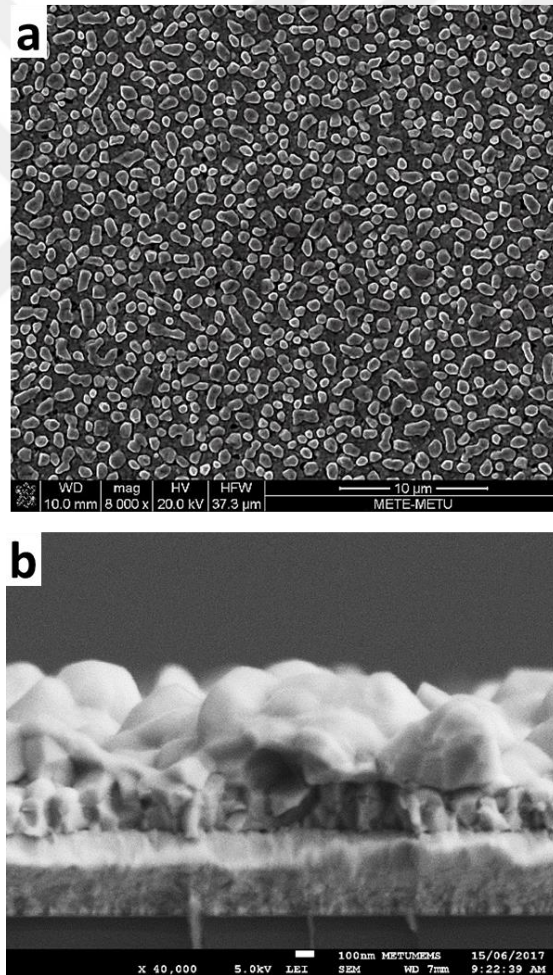


Figure 3.19: As deposited Sn layers (a) top-view and (b) cross-sectional view.

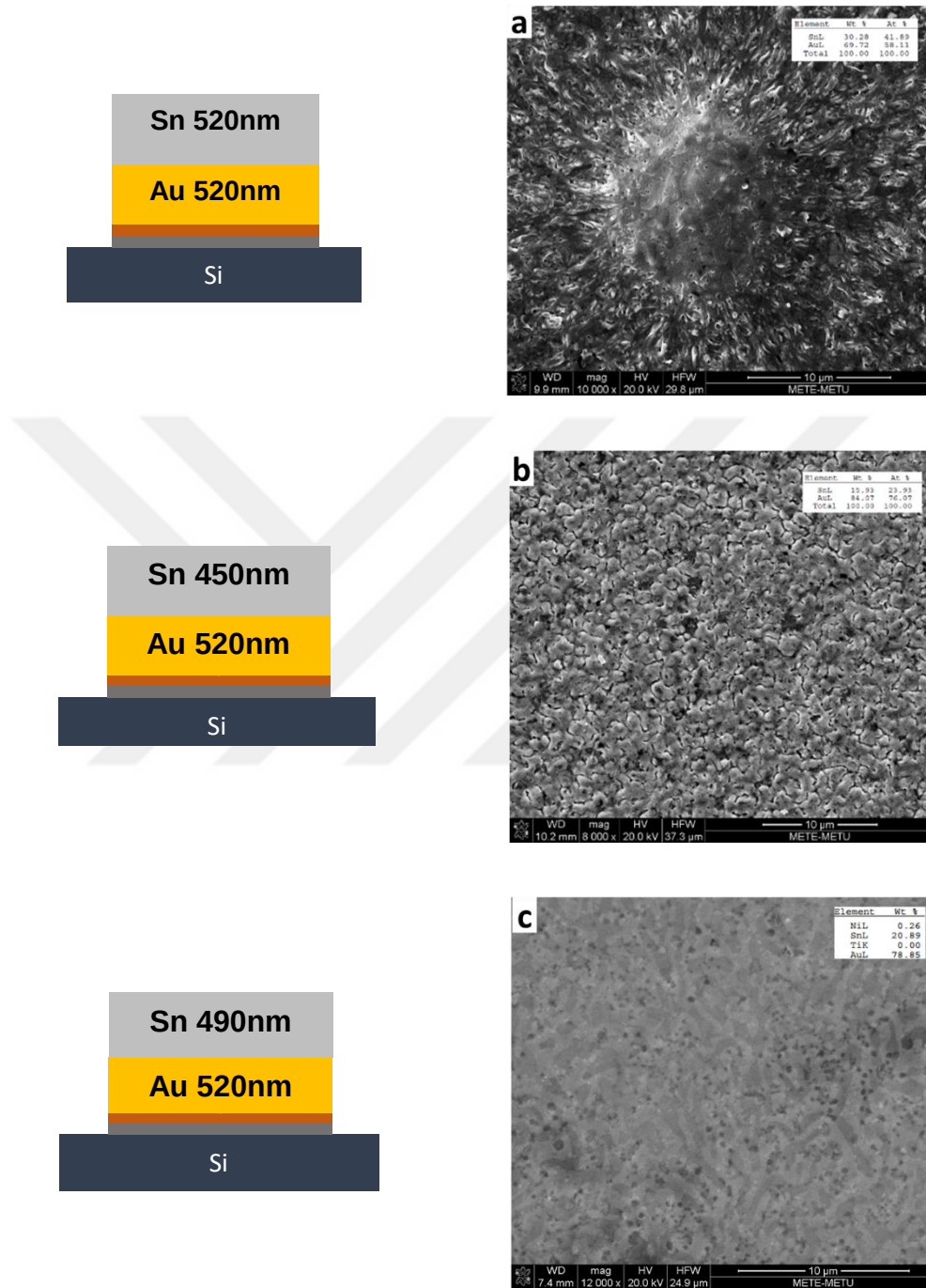


Figure 3.20: The SEM images of (a) as-deposited Sn thin-film and annealed (b) Au/Sn Stack 1, (b) Au/Sn Stack 2, and (c) Au/Sn Stack 3.

As can be seen in Figure 3.20(c), Stack 3, with a thickness ratio of 1.1, has a two-phase eutectic microstructure. The dark phase in the microstructure is AuSn (δ), and the light gray phase is Au₅Sn (ζ'). Eutectic liquid wets the USM layer as a continuous uniform layer, and the composition measured by EDS yielded 21 wt. % Sn which very close to the value expected as the theoretical eutectic composition value, which is 20 wt. % Sn. Using experimentally obtained composition value, the porosity value, and the density of the Sn deposited using the METU-MEMS evaporator can be estimated. The gold layer can be assumed to have its bulk value. It has a mirror-like metallic surface, which is the sign of being deposited similar to bulk properties. The density of Sn thin film is calculated as 5.6 g/cm³ using Equation 2.1 and the experimental composition and thicknesses. The density value has been resulted due to 30 % porosity determined by the experimental data.

TLP Bonding with Eutectic stack

TLP bonding has been performed using the eutectic stack on one wafer and the Au layer on the other wafer. This asymmetric configuration also helps to have a process integration-friendly bonding method, as mentioned in Section 3.2. A schematic drawing of the bonding configuration applied for this method showing implemented layers is provided in Figure 3.21.

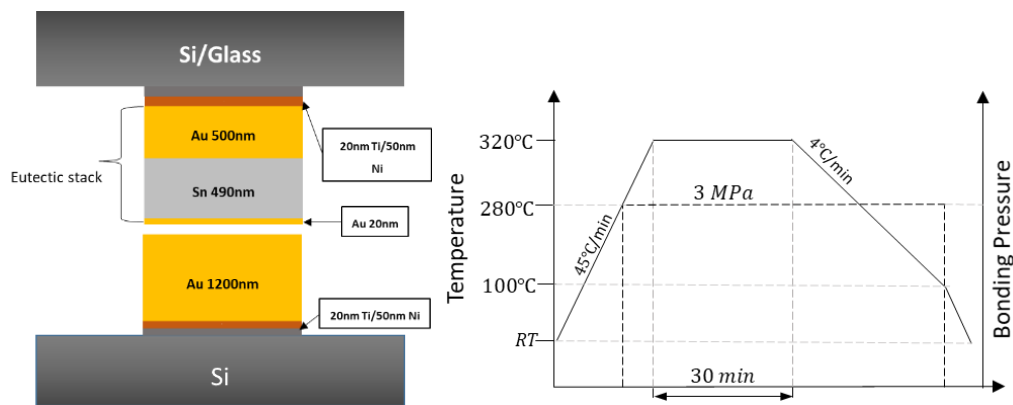


Figure 3.21: The bond material configuration and the bonding profile applied for the Au-Sn TLP bonding with the eutectic stack.

The bonding process aims first to obtain the eutectic liquid at T_{eutectic} , 278 °C, before both wafers are getting into contact. The composition change of the material system obtaining eutectic composition (dashed green line) has been shown in Figure 3.22(a). The interdiffusion between Au-Sn starts even at room temperature, and the diffusion of Au into Sn is faster than the reverse. Therefore, the first intermetallic formation takes place at the Sn rich part of the phase diagram. The IMC formation starts at solid-state, consuming the pure Sn and gets faster as the temperature increases. The first IMC forms at the interface are AuSn_4 (η), then the formation of other phases AuSn_2 (ϵ), and AuSn (δ) takes place, according to the phase diagram. As the diffusion takes place, the IMC formation and dissolution take place until the final eutectic composition (20 wt. % Sn) is reached. Maintaining temperatures high enough throughout the composition change to obtain the liquid phase makes the dissolution of pre-formed IMCs easier. Note that any temperature below 309 °C (the red arrow in Figure 3.22(a)) causes that the phase transformation takes place at solid-state in $\delta + \epsilon$ region (50-66 wt. % Sn). This situation can affect obtaining eutectic liquid adversely in a manner of limited process time. A process temperature above 309 °C (the green arrow in Figure 3.22(a)) ensures solid and liquid phase mixture in the $\delta + \epsilon$ region (green area in Figure 3.22(a)), which makes the dissolution of the ϵ phase easier. It helps to have eutectic liquid easier in the limited process time.

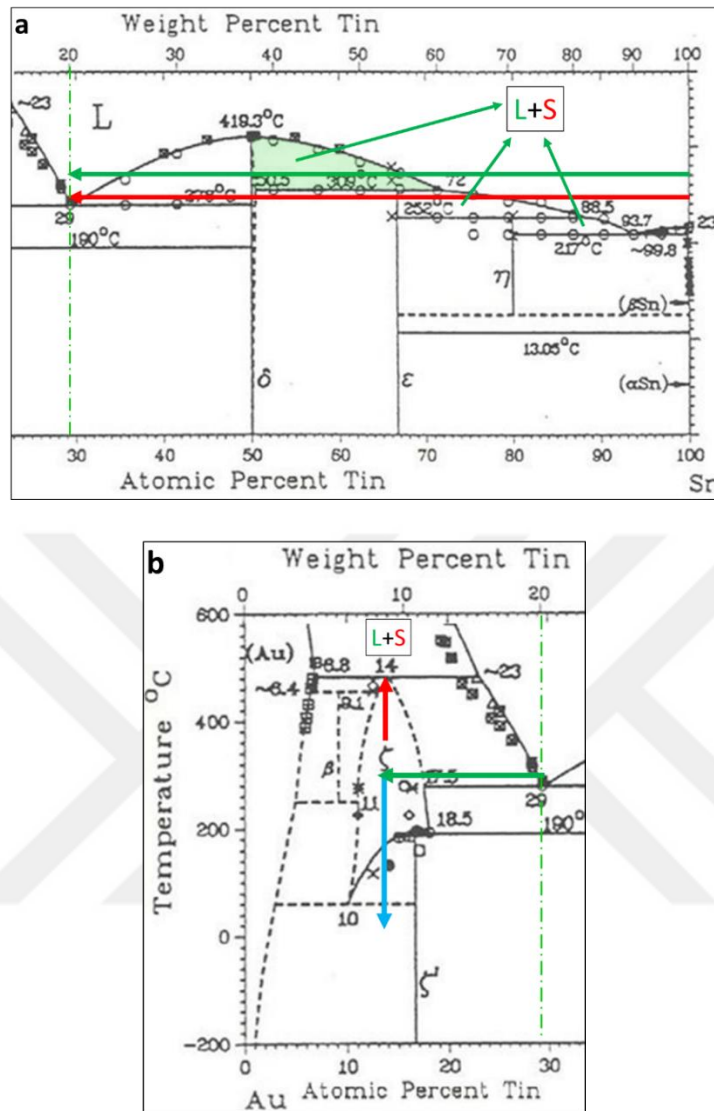


Figure 3.22: The composition changes of the eutectic stack upon heating and the composition change after the eutectic liquid and Au layer is contacted.

After the eutectic liquid is obtained on one side, the wafers are brought to contact, and the bonding process starts with the interdiffusion between the solid gold layer and eutectic liquid. Figure 3.22(b) focuses on the composition change during the process after two wafers got contacted. As the target composition, 8 wt. % Sn, is reached, solidification occurs, and the bond is formed between two wafers. The cross-sectional SEM image and EDS measurements of the formed bond are given in Figure 3.23. The yellow line corresponds to the line EDS measurement, whose result

is in Figure 3.23(b). The bond area is uniform in terms of both structural and chemical profiles. There is a small downward peak in Au data of the line EDS; it is thought that it could be caused by the step around that region on the cross-sectional SEM image. The step might affect the measurement adversely in that region. Figure 3.23c corresponds to the EDS result of the measurement from the region defined by the dashed yellow box in the cross-sectional SEM image. The measurement yielded 7.5 wt. % Sn, which is very close to the designed value. Note that any percentage lower than 10 wt. % Sn is desired for a bond structure thermally stable above 500 °C.

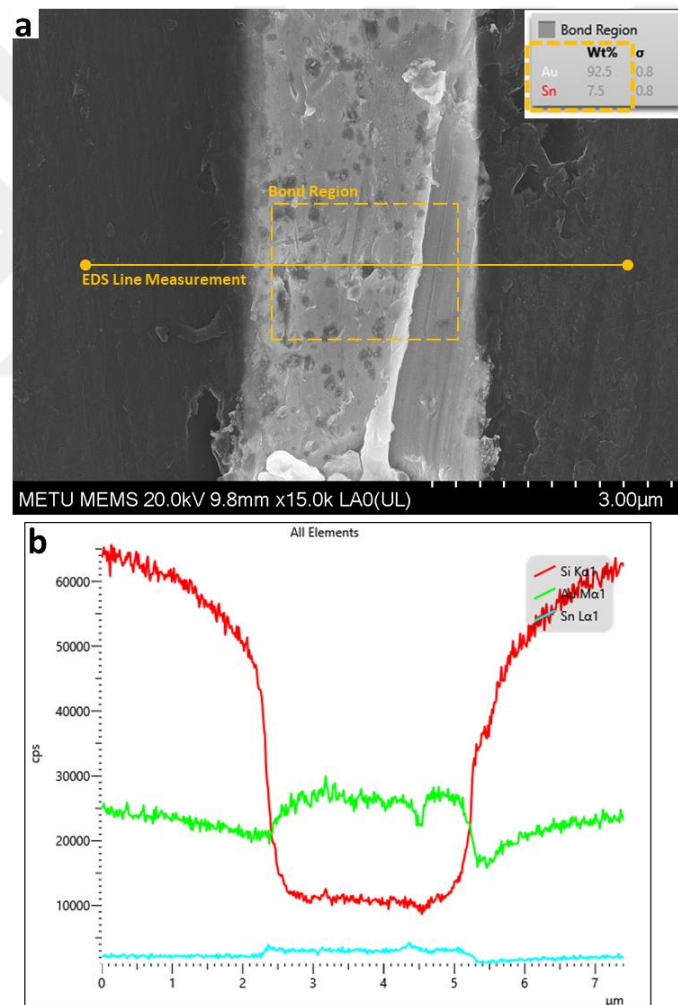


Figure 3.23: (a) Cross-sectional SEM image of Au-Sn TLP bond formed with Au₈₀Sn₂₀ eutectic liquid and Au layer, (b) Line EDS result.

Figure 3.24 shows the SAM image of a bonded wafers using TLP bonding with the eutectic stack. In the SAM image, the dark colors are the sign of continuous penetration of ultrasound waves. The bond-ring regions are in dark gray color, which is the sign of a continuous material structure in the bond-ring region. The leaked water in the streets between dies can be seen in the image as a light gray color. The water was observed even in the center of the layout. The leakage also can be observed in the dies with weak bonds. A die with leakage and another die without leakage is provided in the inset of Figure 3.24(a). In Figure 3.24(b), a larger image of a die with the leakage is shown. The die has a deformed bond-ring structure with white regions, which is the cause of the water leakage. As observed in the SAM investigation, the most dies of the outer circle of the layout have failed with a gross leak. The deformed bond-ring structure of these dies is attributed to the non-uniformity caused by the processing.

Optimization of Bonding Pressure

The bonding pressure is crucial to obtain a strong and reliable bond formation. The bonding pressure must ensure the optimum material contact while providing a minimum amount of liquid loss caused by the squeeze-out during the application of pressure. It is not an unexpected result that the liquid bond material can be lost with excessive pressure, and mechanically weak and non-hermetic bond structures might be obtained. Three different bonding pressures were investigated to optimize the bond pressure. Three bonding processes with the same bond material configuration have been performed with the bonding pressures of 3 MPa, 5 MPa, and 8 MPa.

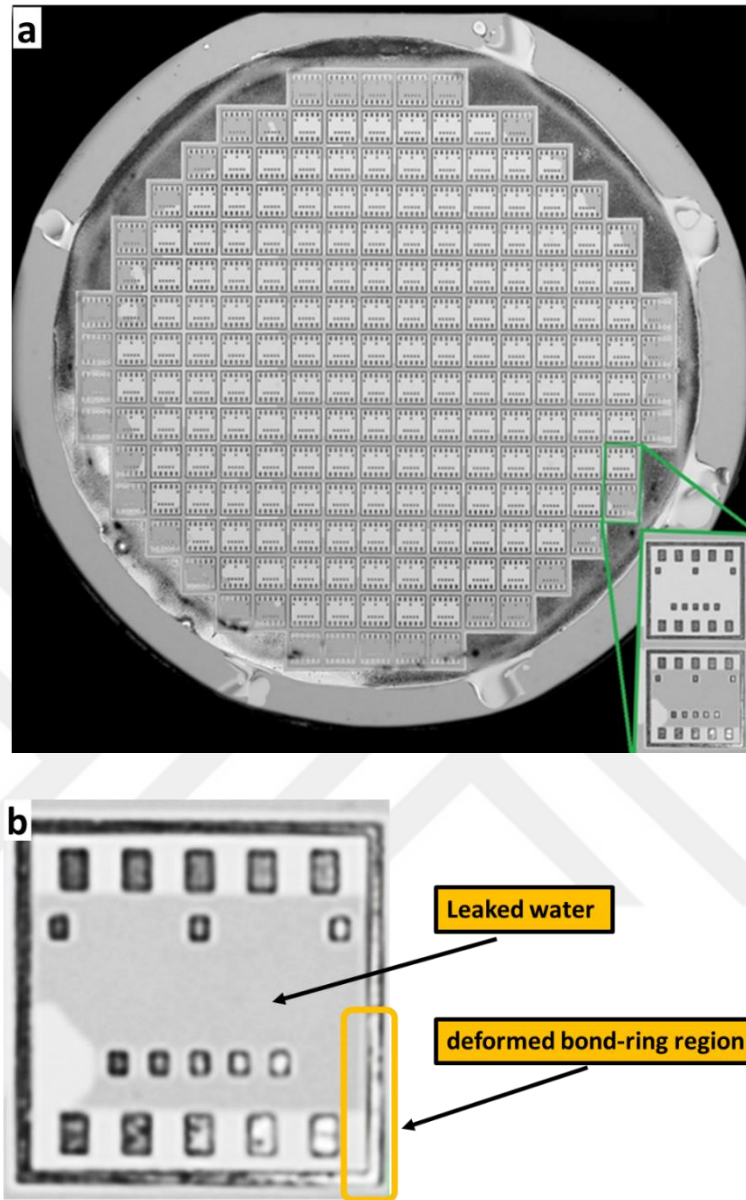


Figure 3.24: (a) Wafer-level and (b) die-level SAM images of the samples bonded using the Au-Sn TLP bonding with eutectic liquid.

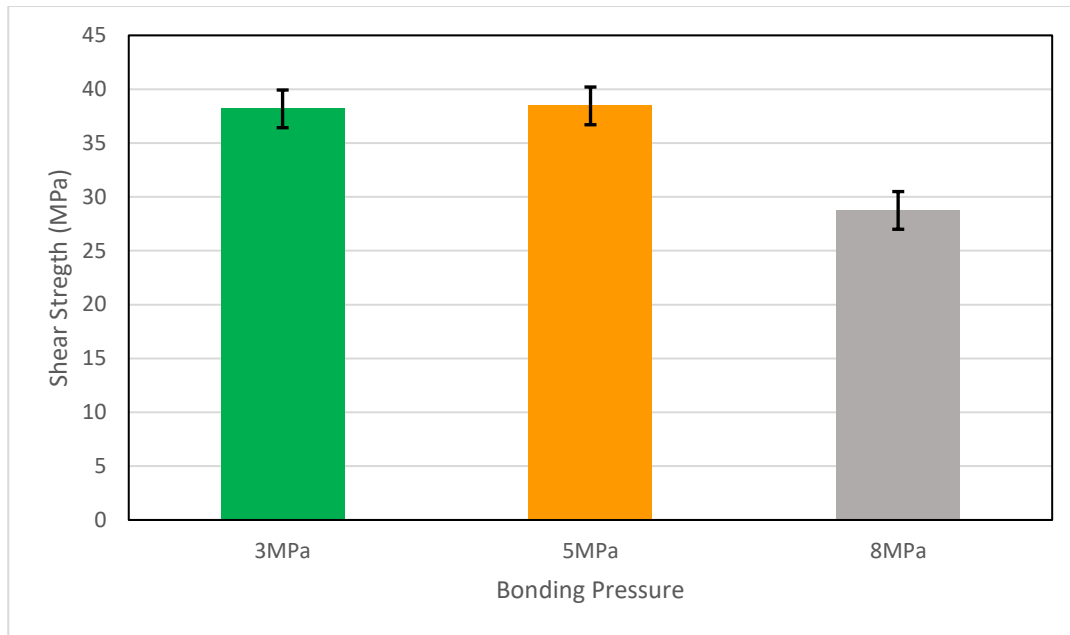


Figure 3.25: The mean shear strength values of samples bonded with Au-Sn TLP using Eutectic liquid with different bonding pressures.

The samples from wafers bonded using 3 MPa and 5 MPa bonding pressures have very similar mean shear strength values, which are 38.2 ± 1.8 MPa and 38.5 ± 1.9 MPa as shown in Figure 3.25. Samples from the wafer bonded with 8 MPa bonding pressure yielded approximately 26 % lower mean shear strength value, which is 28.7 ± 1.6 MPa. The shear strength values, according to positions on a wafer, have been provided in Figure 3.26. The position of each sample number is given in Figure 3.26(a). The shear strength value of each sample has a value greater than the 6 MPa limit value required by MIL-STD 883 standard. However, samples with 5 MPa and 8 MPa bonding pressures have more scattered shear strength distributions along with the position. On the other hand, the shear strength distribution of 3 MPa bonding is more uniform compared to the other bonding. It can be discussed that 3 MPa bond pressure is optimal for this bonding configuration.

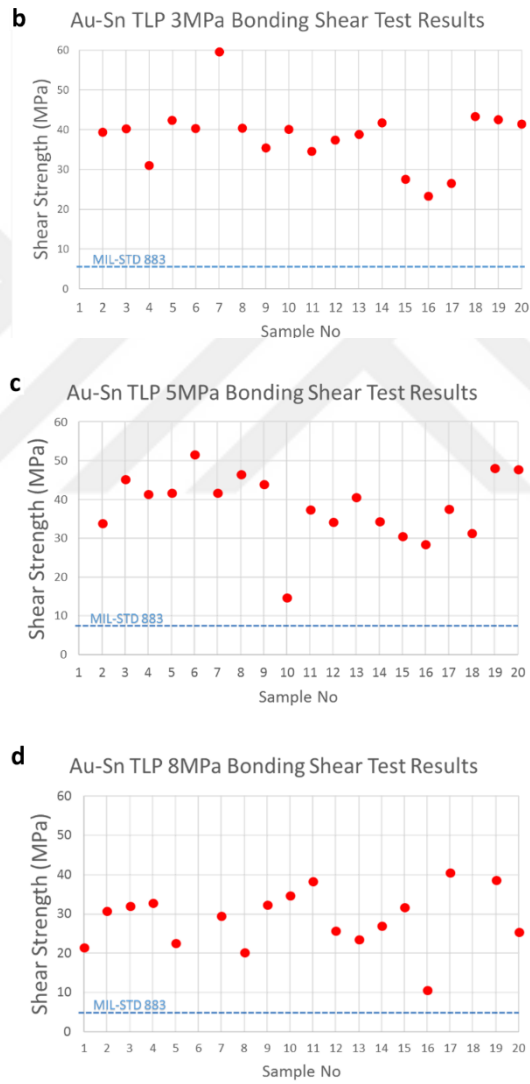
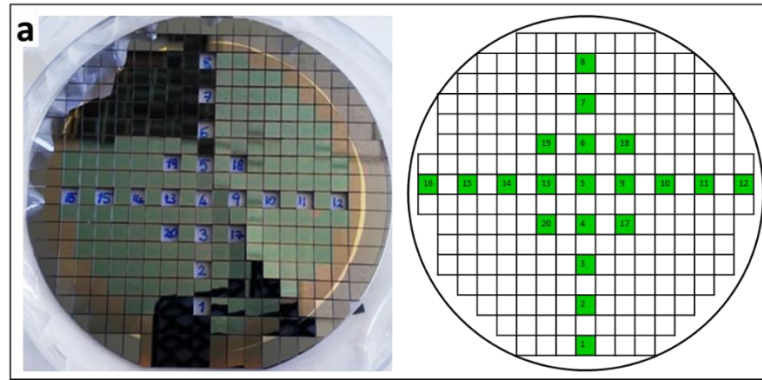


Figure 3.26: (a) The diced wafer for shear strength test and schematic representation of die positions on the wafer and the shear strength results with varying positions of dies from wafers bonded with (b) 3 MPa, (c) 5MPa, and (d) 8MPa bonding pressures.

The Shear Surface and Failure Mode Analysis

The failure of samples bonded with Au-Sn TLP bonding with eutectic liquid has occurred in three different modes. The schematic representation of the failure modes is given in Figure 3.27.

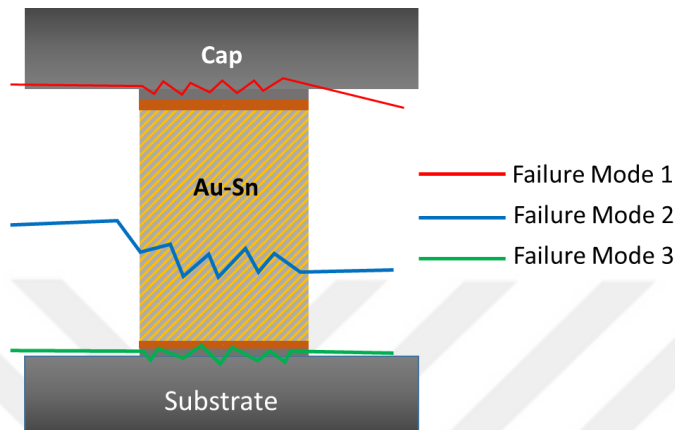


Figure 3.27: The failure modes observed in shear strength tests of Au-Sn TLP bonding with eutectic liquid.

Three different modes are shown in Figure 3.27. Mode 1 is the failure that occurs between the adhesion layer and the cap wafer. Mode 2 is the failure of the Au-Sn bond alloy itself. The SEM investigations of the shear surfaces reveal these failure modes. Figure 3.28 shows the shear surface of a sample, which has a relatively low shear strength. The image shows all three modes. The region defined as Mode 1 was separated from the adhesion/cap interface. The region defined as Mode 2 was broken from the Au-Sn alloy. The region defined as Mode 3 was separated from the adhesion/substrate interface.

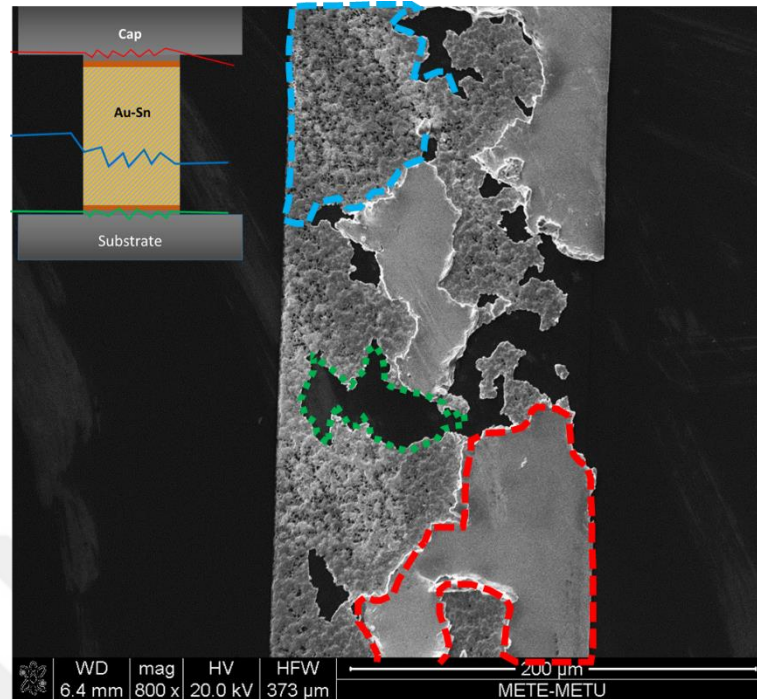


Figure 3.28: The failure modes observed in the shear surface of a sample bonded with Au-Sn TLP with the eutectic stack.

The failure analysis of the samples has revealed that Mode 1 failure is more dominant in the relatively weak samples. On the other hand, the shear surface of relatively strong samples extensively has Mode 2 and Mode 3 failures modes. The least dominant failure mode in all samples is Mode 3. The SEM images of relatively weak (23 MPa shear strength) and relatively strong sample (42 MPa shear strength) are provided in Figure 3.29. The distribution of the failure modes can be seen clearly in these samples.

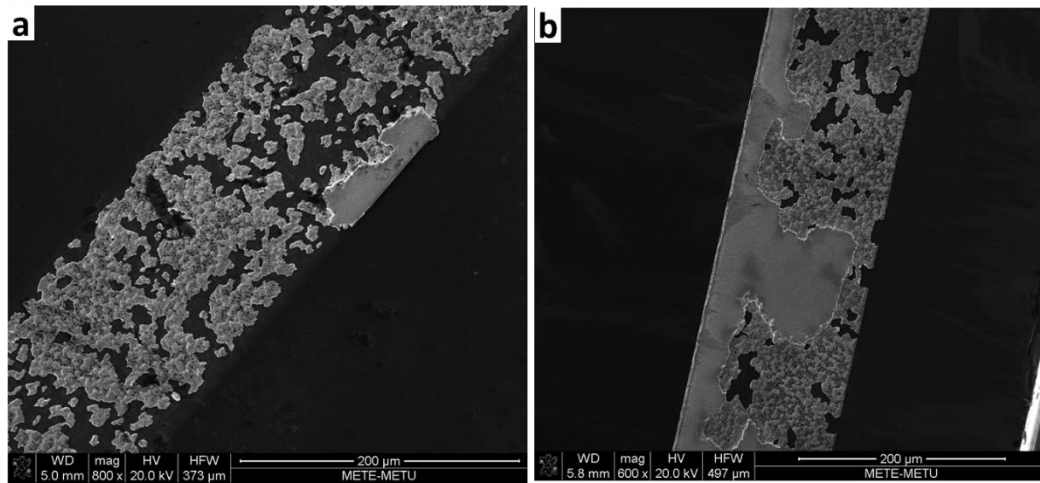


Figure 3.29: SEM images of the shear surface of (a) relatively strong sample (42 MPa shear strength) and (b) relatively weak sample (23 MPa shear strength).

When Mode 3 surface is investigated more closely, the rod-like structures in a continuous matrix can be observed. The EDS analysis, given in Figure 3.30(a), of this structure yields slightly lower than 50 at. % Sn. The EDS result shows that these structures can be AuSn intermetallic, which is not expected to have at the final microstructure. Although the overall composition has reached the target composition (8 wt. % Sn) as shown in Figure 3.23, AuSn could not be dissolved in the microstructure completely. The TEM image taken from a Mode 1 region of a relatively strong sample shows the hexagonal grain of the intermetallic in Figure 3.30(b).

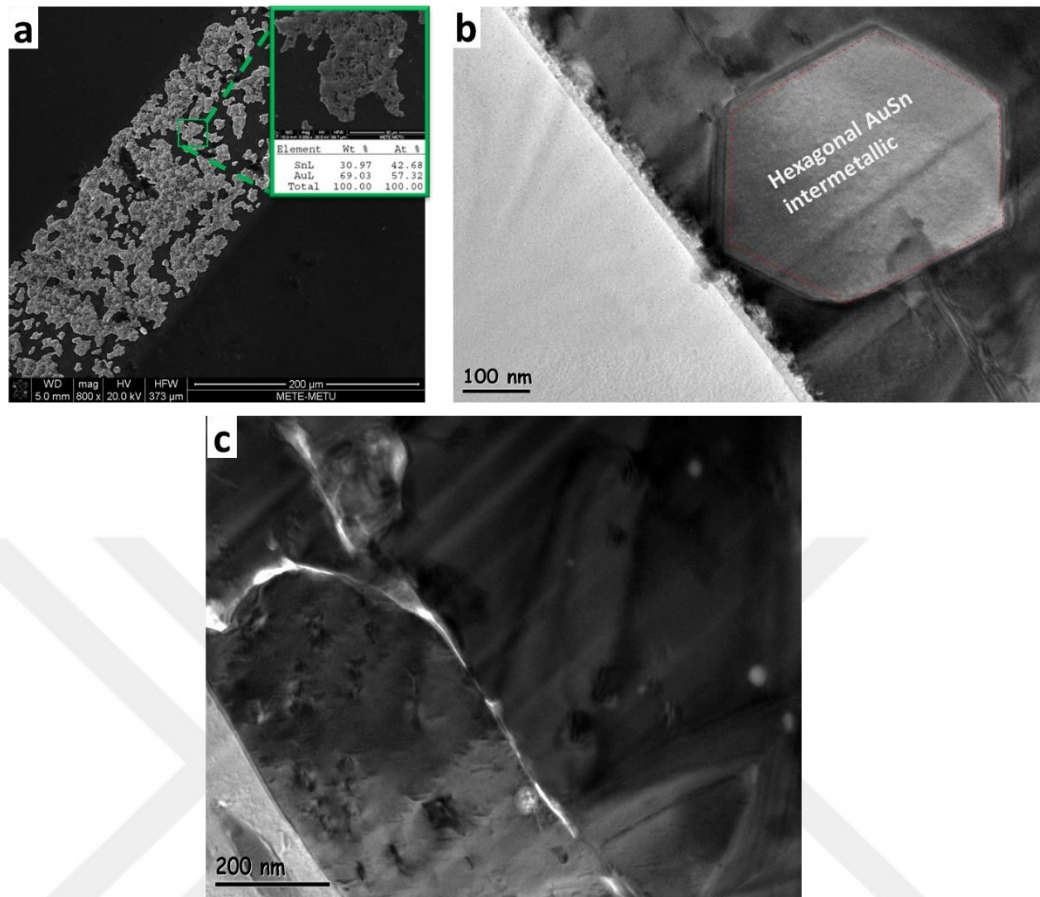


Figure 3.30: (a) The EDS measurement from the Mode 2 region, (b) the cross-sectional TEM image of relatively strong Au-Sn alloy from the Mode 1 region, and (c) the cross-sectional TEM image of relatively weak Au-Sn alloy from the Mode 1 region.

In Figure 3.30(b), the cross-sectional TEM images show a void-free and crack free bond material. In Figure 3.30(c), the cross-sectional TEM image of a relatively weak sample exhibits some crack and delamination in the bond material. Note that it has also observed that the weak samples have higher Failure Mode 1 distribution. Therefore, the low shear strength of these samples can be attributed to the cumulative effects of delaminations, cracks, and poor adhesion to the cap. On the other hand, strong samples typically have Mode 2, which means that the weakest point of these samples is the bond itself. Although all samples satisfy MIL-STD 883 mechanically, the delamination and cracks may cause poor hermeticity.

Hermeticity of Formed Bonds

If the hermeticity of the seals is very poor, there can be a gross leak. Gross leak can be identified with liquid penetration into the sealed cavities of the samples were held in DIW during the SAM investigation, and any package with poor sealing will have liquid penetration during the SAM investigation. The die shown in Figure 3.24 has a gross DIW leak into the cavity. The dies which are close to the edge of the wafer have poor bond formation due to the fabrication defects and non-uniformity caused by the deposition and bonding systems. Therefore, the gross leak of the edge dies has been attributed to these effects during the fabrication.

Although the He-leak test has some limitations on testing hermeticity of ultra-low volumes, it is still applicable for the volumes higher than $2.36 \times 10^{-3} \text{ cm}^3$ [61]. The hermeticity of packages sealed with AuSn TLP bonding using eutectic stack was tested using the He-leak test. The test procedure was applied according to MIL-STD 883 Standard, as mentioned in Section 2. The volume needed for hermeticity testing was formed with cavity etching using DRIE. A cavity with an approximately 150 μm depth formed on the wafers. The 2D and 3D optical profiler measurements performed during fabrication and SEM image of a cavity after the bonding can be seen in Figure 3.31(a) and 3.31(b), respectively. The dark blue region in the optical surface profiler images corresponds to the cavity region. The volume of the cavity formed in the package was $6 \times 10^{-3} \text{ cm}^3$. The test performed after 16 h He-bombardment and approximately 3 minutes dwell time. The samples were annealed at 400 °C for 10 minutes after the bonding in order to simulate the getter activation. The system did not measure any leak higher than its lowest limit, which is $0.1 \times 10^{-9} \text{ atm. cc/s}$. This value is much lower than the rejection limit for the volumes smaller than 0.05 cm^3 required by military standard MIL-STD 883. Therefore, the packages with this bonding satisfy the hermeticity requirement of MIL-STD 883.

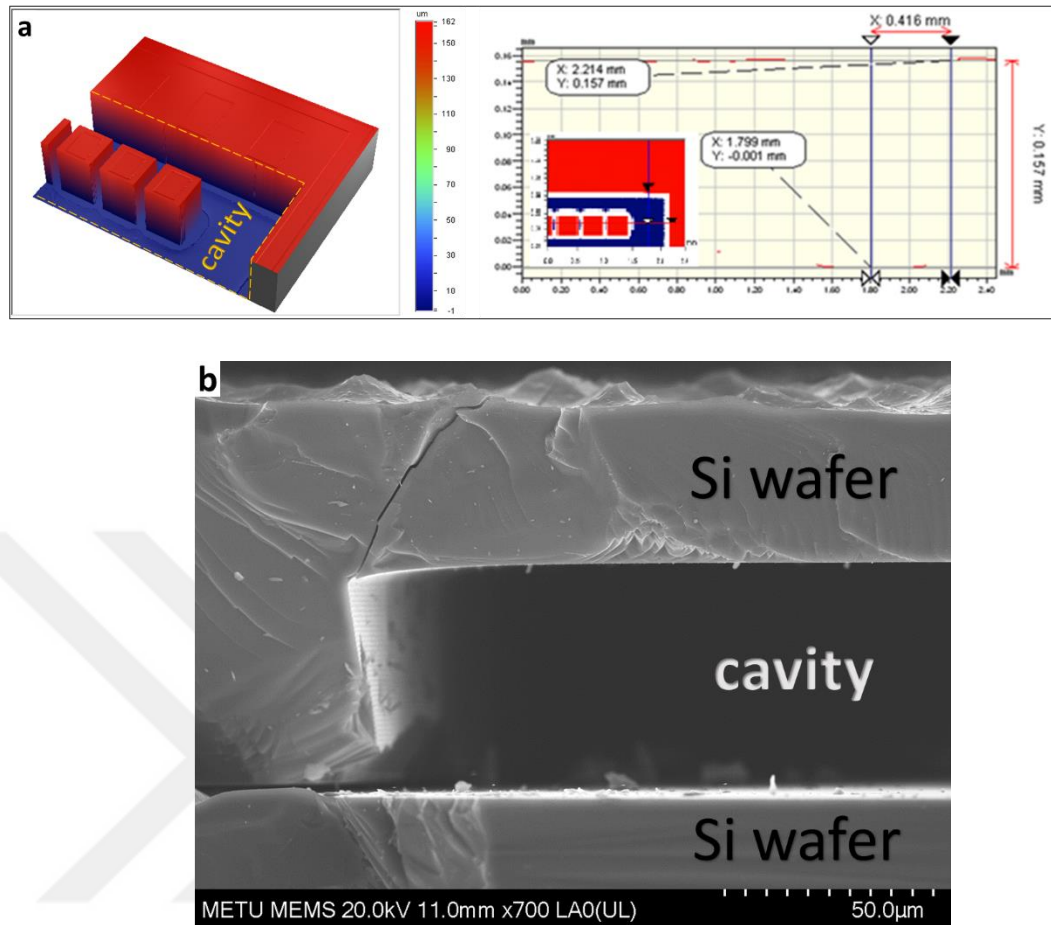


Figure 3.31: (a) Optical surface profile measurement of the cavity during fabrication and (b) SEM image of the cavity after bonding.

For a better understanding of the hermeticity of the seals and packages, the cap deflection method has been applied for the bonding performed using Si wafers on both sides. One of the wafers has been fabricated with a cavity to have vacuum volume in the package, Figure 3.31. After the bonding, the wafer thinning was performed to have a thin diaphragm over the vacuum cavity. Due to the vacuum difference between the cavity and the atmosphere, the thin diaphragm is deflected into the cavity. The deflection method has been performed for two different bonding processes. One with Ti/Ni USM materials and the other is the one with Cr USM layer. The photograph and the optical surface profiler measurements of the wafers

with Ti/Ni and Cr USM layers just after the thinning process is given in Figure 3.32 and Figure 3.33, respectively.

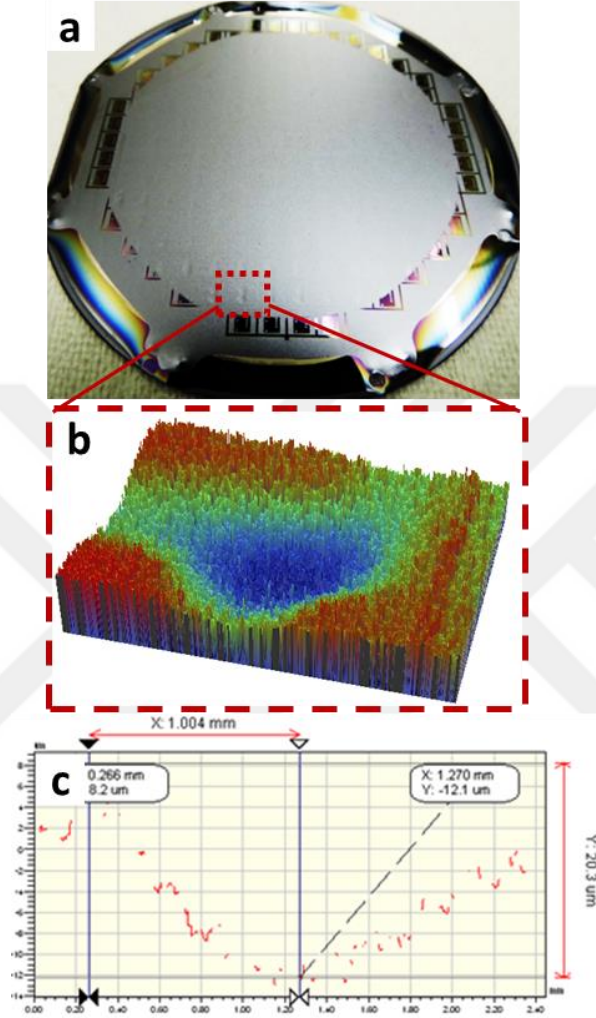


Figure 3.32: (a) The photograph, (b) 3D, and (c) 2D the optical surface profiler measurements of the cap deflection of the wafer with Ti/Ni USM layer.

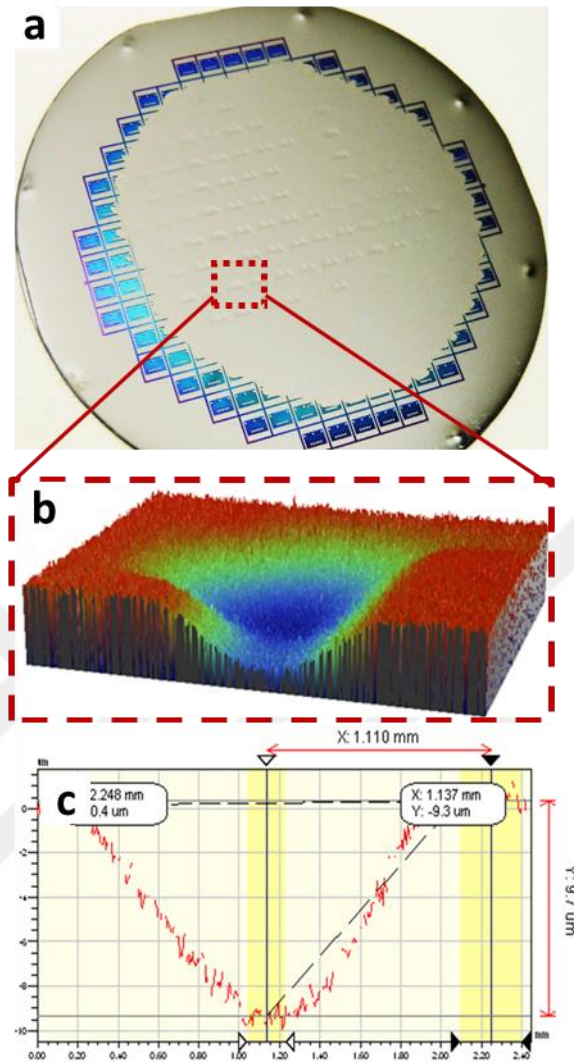


Figure 3.33: (a) The photograph, (b) 3D, and (c) 2D the optical surface profiler measurements of the cap deflection of the wafer with Cr USM layer.

The deflection amount on the dies was measured with the optical profiler. The measurements in Figure 3.32 and Figure 3.33 were performed just after DRIE thinning. The wafer with Ti/Ni USM layer had a 20 μm diaphragm deflection, whereas; the one with Cr USM layer has approximately 10 μm deflection. However, the deflection on the wafer with the Cr USM layer has disappeared after one week. The vacuum inside the cavity has been lost one week after the thinning process, Figure 3.34(a). The measurement of the wafer with the Ti/Ni USM layer after one

week yielded $19.7\ \mu\text{m}$, which is similar to the initial measurement as shown in Figure 3.34(b) .

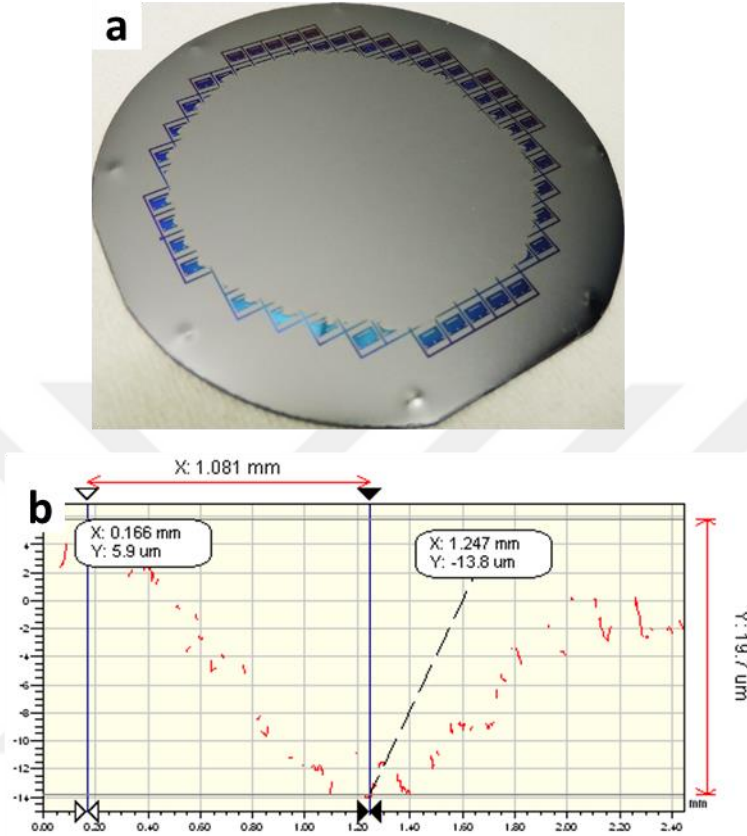


Figure 3.34: (a) The wafer with Cr USM layer after one week and (b) the cap deflection measurement of the wafer with Ti/Ni USM layer after one week.

A wafer bonding method that will be utilized in a MEMS encapsulation process must withstand the getter activation process for vacuum applications. The getter activation process usually needs high temperatures [37]. The most common thin-film getter material is Ti. The activation temperature of Ti getter films is around $400\ ^\circ\text{C}$ [52]. Therefore, the seal must be stable during the activation process at $400\ ^\circ\text{C}$. Annealing at $400\ ^\circ\text{C}$ for 10 minutes was applied to the wafers with Ti/Ni USM layers to simulate the activation process of the getter. The cap deflections on the wafer have been still present after the annealing process. Another optical surface profiler measurement of

the deflection was performed, and the measured deflection was 19.4 μm after the annealing, as shown in Figure 3.35.

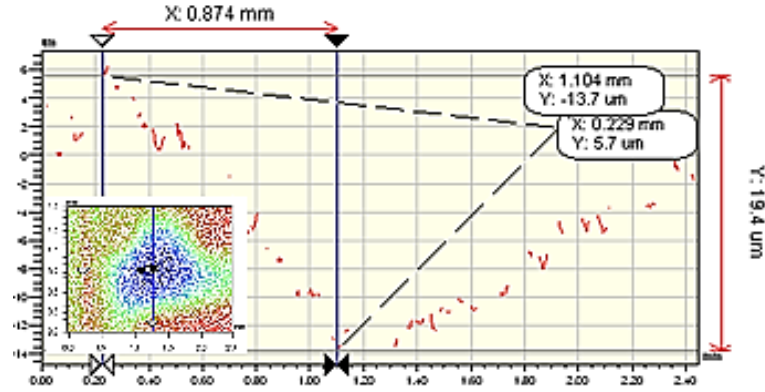


Figure 3.35: The optical surface profiler measurement after annealing at 400 °C for 10 minutes to simulate the getter activation process.

Calculation of the Pressure Inside the Package

The vacuum inside the cavity can be calculated approximately using the mechanical properties of the diaphragm material. Figure 3.36 shows a schematic image of a cap deflection. Using Equation 3.3 and the material parameters of Si diaphragm, the vacuum inside the package can be estimated.

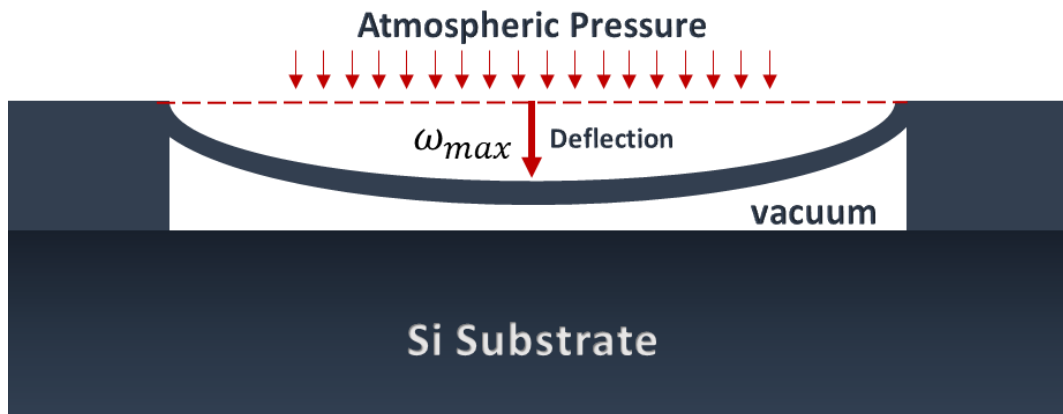


Figure 3.36: The schematic drawing of a cap deflection.

The maximum deflection of a deflected membrane can be calculated using the following equation,

$$\omega_{max} = \frac{5P_{total}l^4w^4}{384D(l^4+w^4)} \quad (3.1)$$

where ω_{max} is the maximum deflection of the diaphragm, l is the length, w is the width, P_{total} is the pressure on the diaphragm, and D is the flexural rigidity given by

$$D = \frac{Eh^3}{12(1-\vartheta^2)} \quad (3.2)$$

where h is the thickness of the diaphragm, E is Young's modulus, and ϑ is Poisson's ratio. Using Equation 3.1 and Equation 3.2, the pressures inside the cavity can be estimated using with Equation 3.3

$$\Delta P_{total} = \frac{32Eh^3(l^4+w^4)}{5(1-\vartheta^2)l^4w^4} \Delta\omega_{max} \quad (3.3)$$

The plot of the pressure inside the cavity versus the deflection amount for the Si diaphragm structure with the dimensions and material properties given in Table 3.5 is provided in Figure 3.37. The marked data point shows the vacuum inside the cavities with the diaphragm thickness given in Table 3.5.

Table 3.5: The mechanical and geometrical properties of the deflected diaphragms on Au-Sn TLP bonded wafer.

Property	Value
Si Poisson's Ratio	0.265
Si Young's Modulus (GPa)	140
h (μm)	40
l (μm)	500
w (μm)	500

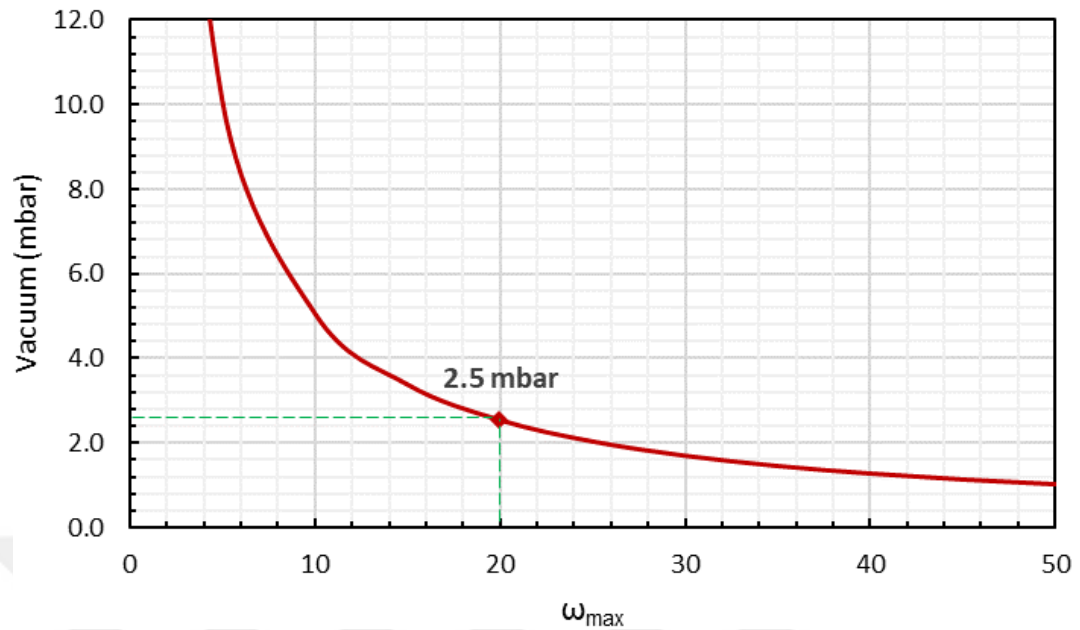


Figure 3.37: The calculated vacuum inside the cavity of the dies on the Au-Sn TLP bonded wafer with Ti/Ni USM layer.

The deflection measurement was repeated after one year and after two years using the optical surface profiler to investigate the long-term stability of the hermeticity of the package. Two measurements on a diced die were performed after one year and two years. It shows that the bond is mechanically strong enough to keep its stability and hermeticity after dicing. The photograph of the diced die with diaphragm deflection and the measurement of the deflection after one year and two years can be seen in Figure 3.38.

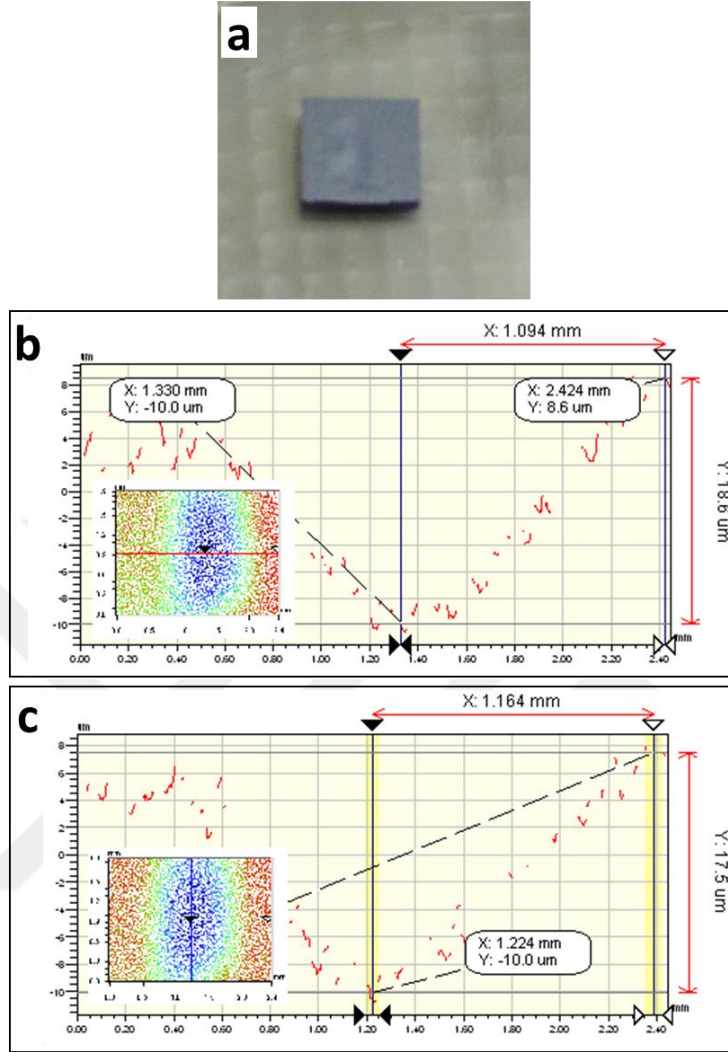


Figure 3.38: (a) The die with cap deflection after the dicing process, the cap deflection measurement after (b) 1 year, and (c) 2 years.

Application of Au-Sn TLP Bonding with Eutectic Stack for μ Bolometer Wafers

The optimized bonding method was applied for real μ bolometer wafers. The process has been integrated into the μ bolometer fabrication process. The Sn deposition system in METU-MEMS center can handle maximum 6 inches sized wafers. Therefore, the bonding process was implemented with 6 inches sized wafers. The bond-ring formation on the μ bolometer wafer has been applied with the method mentioned in Section 2. The PI layer was patterned to have an opening with 250 μ m

width just before the pixel releasing step with O₂ plasma etch of the PI sacrificial layer. 150 μm wide Au bond-ring metal was deposited and patterned with the lift-off method into the PI opening. The images showing the PI opening formed on the CMOS $\mu\text{bolometer}$ wafer and the gold bond-ring patterned into the PI opening are given in Figure 3.39 and 3.40, respectively.

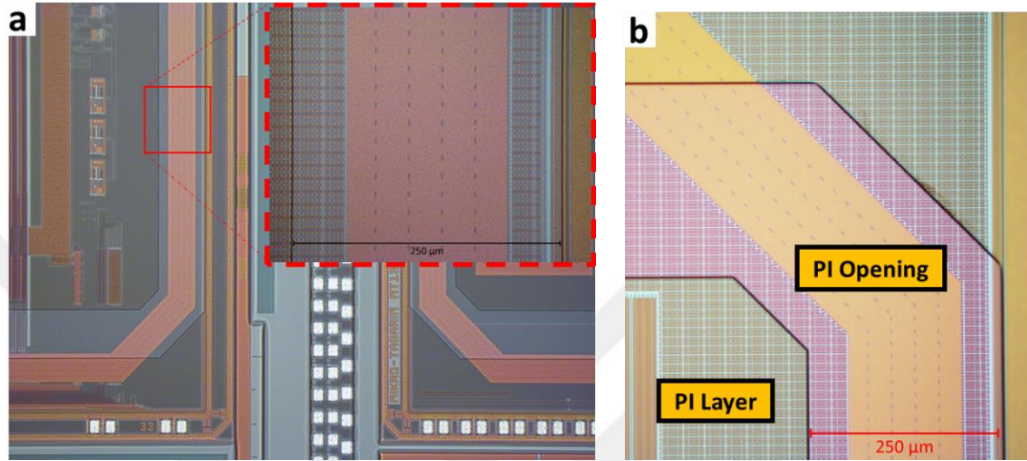


Figure 3.39: The PI opening formed on the CMOS $\mu\text{Bolometer}$ wafer, (a) the PR patterning, and (b) the PI opening after plasma etching.

After the gold bond-ring formation on the CMOS wafer, the wafer is ready for the bonding process. O₂ plasma etching is applied to release the $\mu\text{bolometer}$ pixel structures. Note that the bond-ring metal must withstand this process. Most metal oxides have a negative $\Delta G_{\text{formation}}$, their formation is spontaneous, and they are stable compounds. Consequently, it is crucial to have a bond ring metal whose oxide is unstable as noble metals such as Au and Pt. Au bond-ring makes the integration of the bonding process to $\mu\text{bolometer}$ fabrication easier. It withstands O₂ plasma etching and does not need surface treatment before the bonding process.

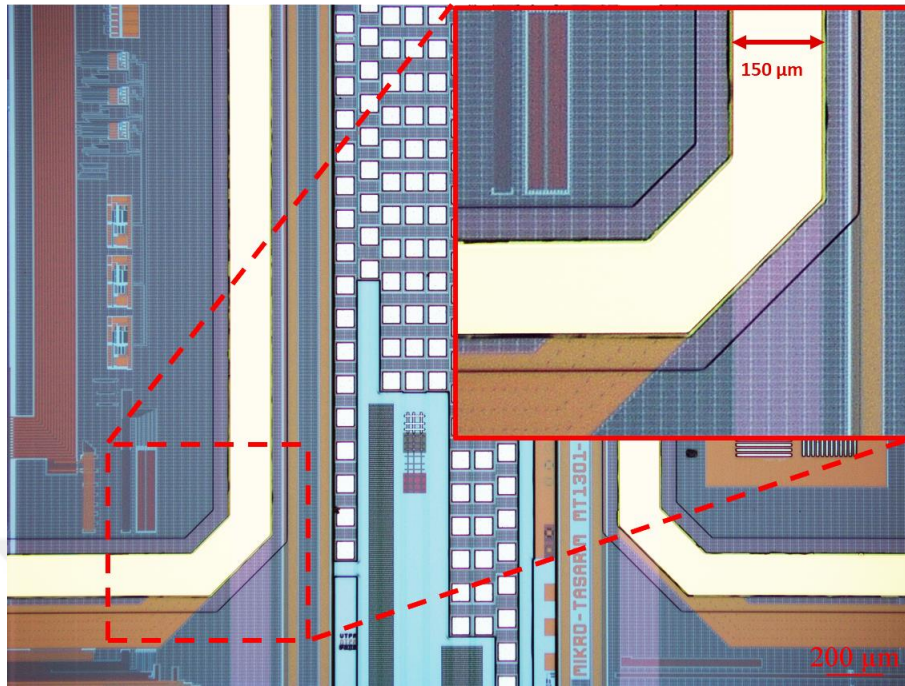


Figure 3.40: The Au bond ring patterned into the PI opening on the CMOS μbolometer wafer.

A cavity and the bond-ring were fabricated on a Si cap wafer. However, conventional Si wafers may have oxygen impurities causing optical absorption around 9 μm. Therefore, the cap wafer has been chosen to have high IR transparency. Si wafers with low oxygen impurity concentration are preferred for IR applications. After the bond-ring metal was deposited on the cap wafer, the cavity formation was performed using DRIE etching. The optical microscope images of the bond-ring and the cavity on the cap wafer are given in Figure 3.41. The photograph of the cap wafer, μBolometer CMOS wafer, and the aligned bonding pair can be seen in Figure 3.42.

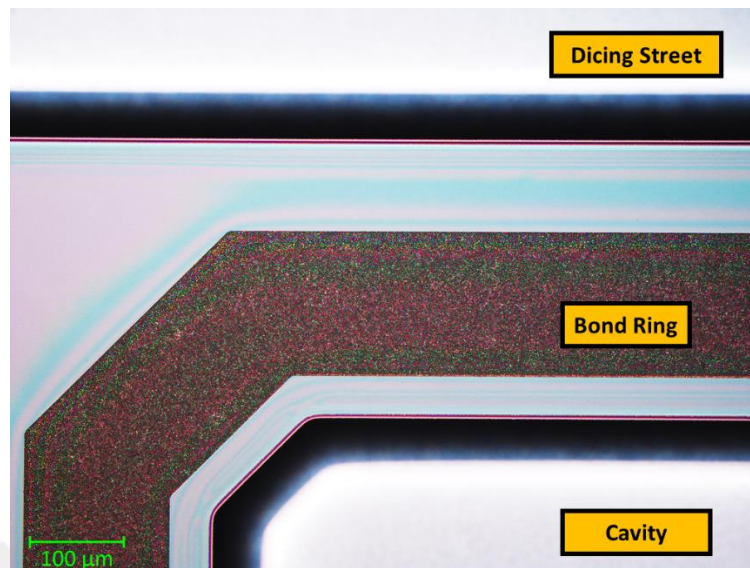


Figure 3.41: The bond-ring and the cavity formed on the cap wafer for wafer-level μ bolometer packaging.

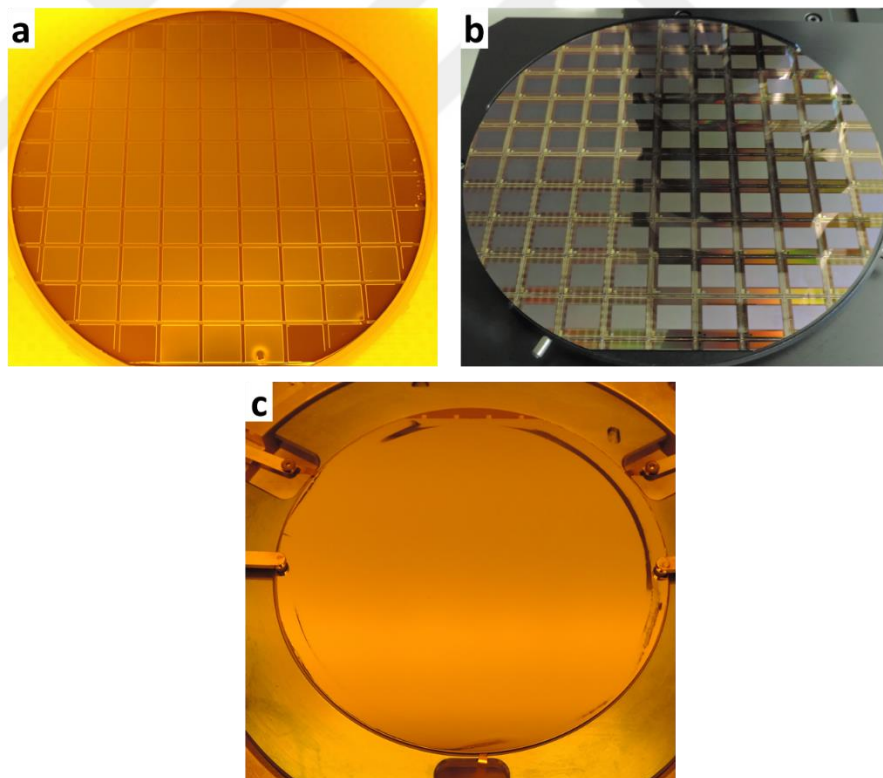


Figure 3.42: (a) Cap wafer, (b) μ Bolometer CMOS wafer before the bonding, and (c) the wafers on the bond chuck after alignment.

The bonding of the wafers has been performed with 3 MPa bonding pressure at 320 °C. However, a good, strong bond could not be obtained with the process. The bond was weak, and the wafers were separated during the dicing process. The wafers have been investigated after the failure. As can be seen in the optical microscope images given in Figure 3.43, the bond metal has been stripped from the substrates as a metal sheet leaving an unexpected transparent layer on the bond region. Around the bond ring line, the squeezed-out eutectic liquid is present, which is the indication of the successful liquid formation. The bond between the two bond ring layers was formed successfully. Nevertheless, the bond metal had an adhesion problem due to the residual transparent layer.

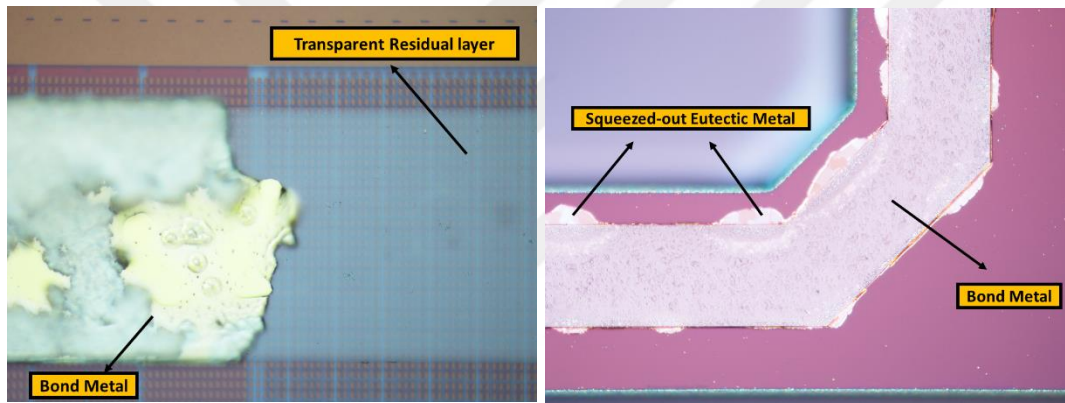


Figure 3.43: Optical microscope image of the failed bonding of CMOS μ bolometer wafer and cap wafer.

The cause of the transparent layer, which is the cause for the low adhesion of the bond metal, was initially attributed to a possible residual PI layer due to insufficient etching during PI opening etch. The wafer has been treated with O₂ plasma cleaning just after the bonding failure to remove presumed PI residue. O₂ plasma cleaning was not able to remove the layer. Figure 3.44 shows the layer after O₂ plasma cleaning after 10 minutes and 20 minutes of cleaning durations. It showed that the transparent layer was not a residual PI layer.

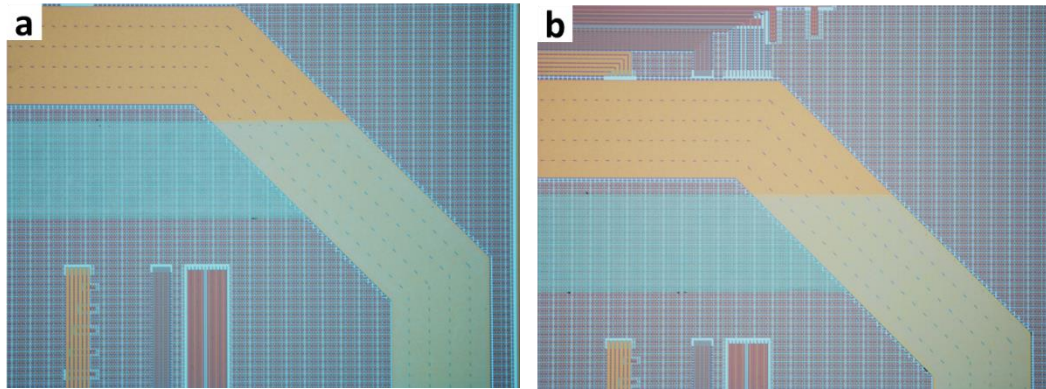


Figure 3.44: The residual layer after O₂ plasma cleaning after (a) 10 minutes and (b) 20 minutes of cleaning durations.

After O₂ plasma cleaning, The wafer has been investigated using SEM. The transparent layer was observed as an insulating layer with dark color in SEM images as shown in Figure 3.45. The EDS analysis of the transparent residual layer has shown that Ti is present in the chemical composition of the layer. It should be noted that the first layer contacting the CMOS wafer is the Ti layer of the USM layers. It can be concluded with the EDS analysis that the top passivation layer of the CMOS substrate has consumed the Ti layer of the USM layer. The consumption of Ti by CMOS passivation was not an expected situation, and it is not observed with the PECVD deposited passivation layers during the development processes. There can be structural and chemical differences between the top passivation layers of CMOS wafers and the PECVD deposited passivation layers used in this work. These differences may cause this unexpected interaction of the USM layer and the substrate.

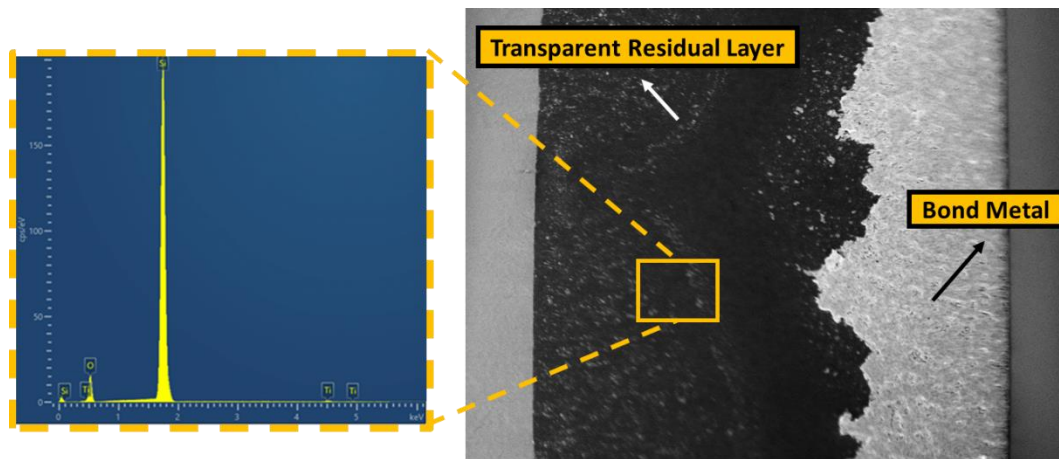


Figure 3.45: SEM image and EDS measurement of the residual transparent layer.

3.3.2 Au-Sn TLP Bonding with Intermediate Barrier Layer

The optimization of the Intermediate Barrier Layer

The initial experiment for the intermediate layer was performed with the eutectic stack on a 10 nm Ti intermediate barrier layer. The experiment was performed with the material stack given in Figure 3.46(a). The material structure was characterized in DSC equipment with annealing with a 45 °C/min heating rate. The DSC result of the sample is given in Figure 3.46(b).

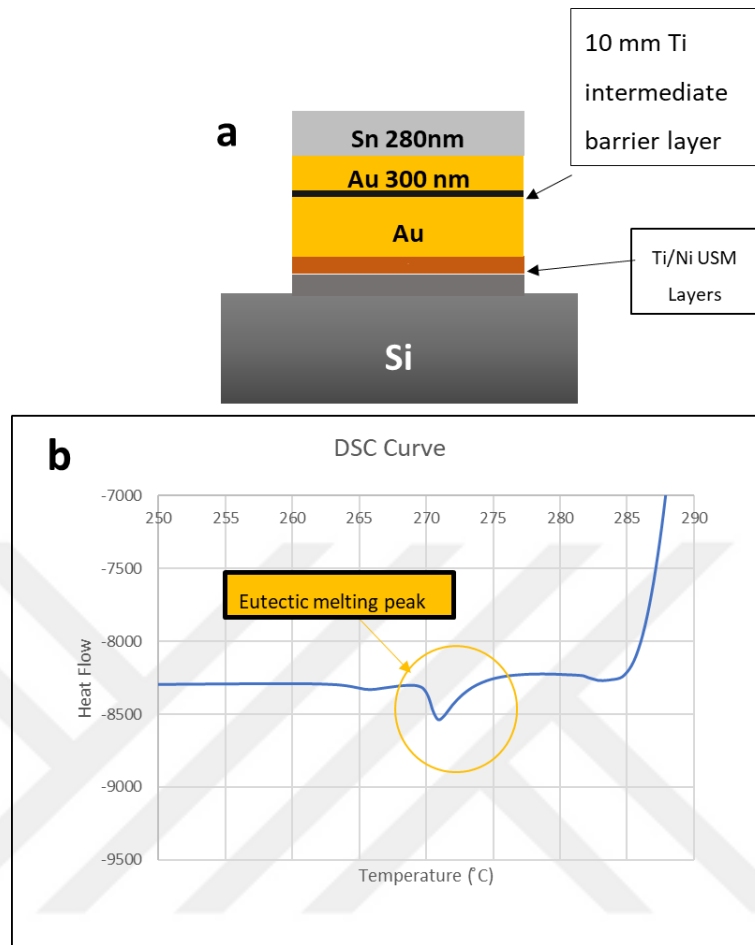


Figure 3.46: (a) The barrier layer between the eutectic stack and gold layer and (b) the DSC curve of the sample.

The configuration in Figure 3.46 uses the eutectic temperature as the liquefaction temperature. The barrier layer has been designed with a pure Sn layer to have a lower bonding temperature. The barrier layer in the configuration, given in Figure 3.46, acts as a barrier to Au atoms and Sn atoms in Au lattice. The intermediate barrier layer design with the Sn layer will act as a barrier for pure Sn metal. The design can be seen in Figure 3.47. Both Ni and Ti intermediate barrier layers were deposited by sputtering. Then, the Sn layer was deposited by the thermal evaporator. The SEM images of the layers on Ti and Ni barrier layers is given in Figure 3.47(b) and Figure 3.47(c), respectively.

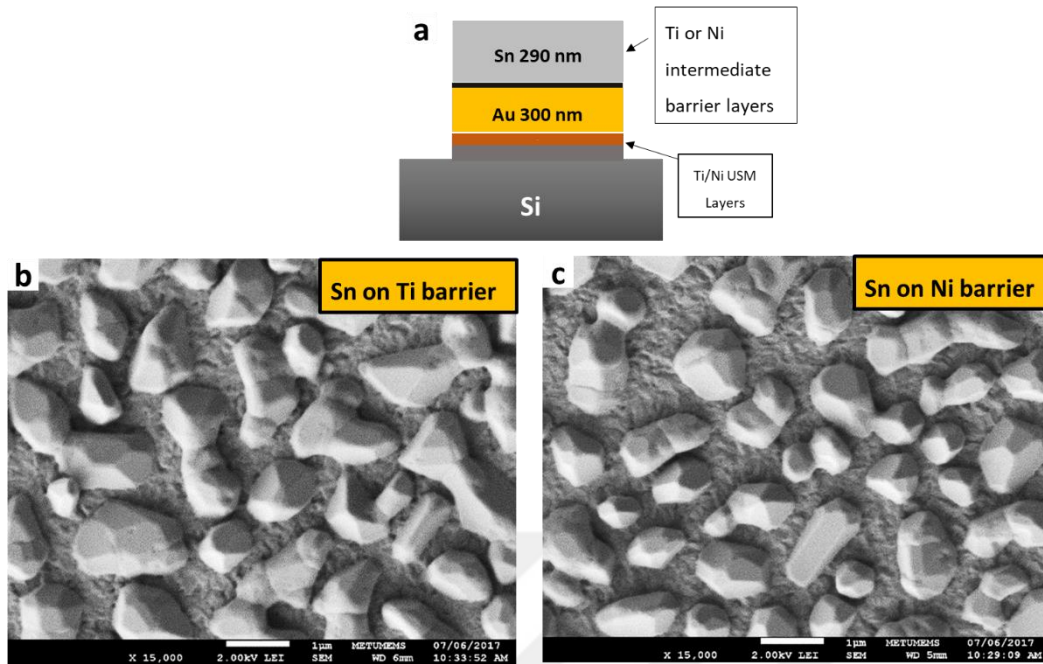


Figure 3.47: (a) The material configuration proposed for TLP bonding with the barrier layer and SEM images of Sn layers on (b) Ti and (c) Ni barrier layers.

Three different barrier layers (20 nm Ni, 20 nm Ti and 10 nm Ti) were tested with the configuration given in Figure 3.47(a). The USM layer, Au layer, and barrier layers were deposited by DC sputtering, and the Sn layer was deposited in the thermal evaporator. The fabricated samples were characterized by DSC. The DSC curves of the three samples are provided in Figure 3.48.

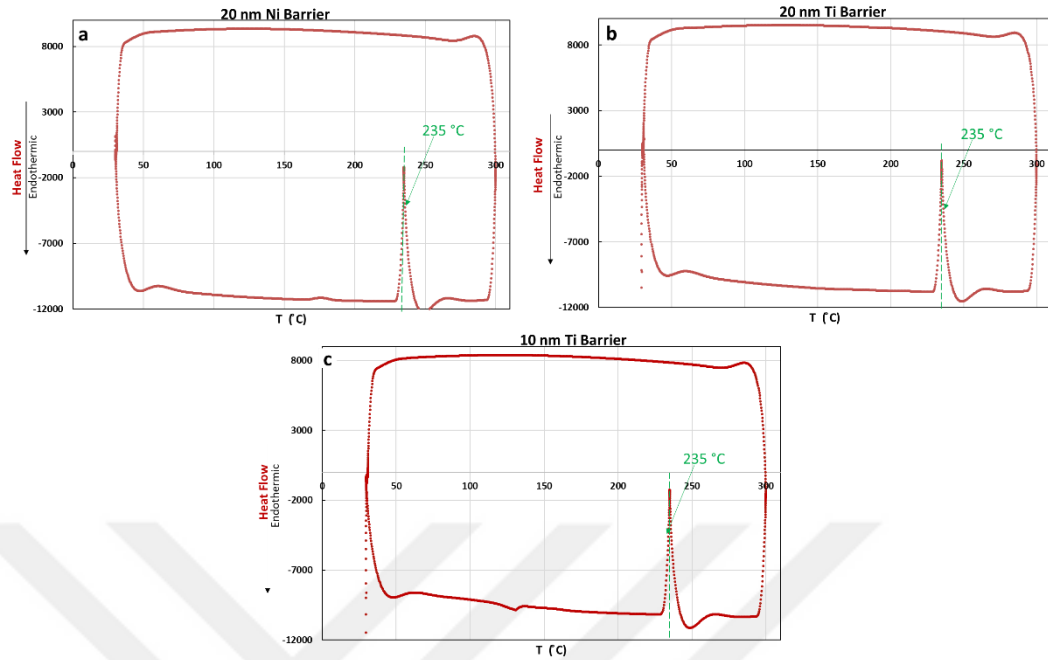


Figure 3.48: DSC curves samples with (a) 20 nm Ti barrier (b) 20nm Ti and (c) 10 nm Ti.

DSC curves of all barrier layers have a peak around the melting point of Sn. The peaks are expected to be endothermic; however, the peaks in the curves are exothermic. Au and Sn system is known for its large negative ΔH_m as the evidence of its intermetallic formation tendency [62]. The exothermic peaks have been probably resulted due to high negative enthalpy of mixing. Each material enables the liquefaction of Sn material. However, due to its lighter barrier properties, Ti is selected as the barrier materials for further experiments. 10 nm barrier thickness has been determined for the bond material to keep the intermetallic formation with Ti minimum. The bonding experiments are designed with the bond ring structure given in Figure 3.49.

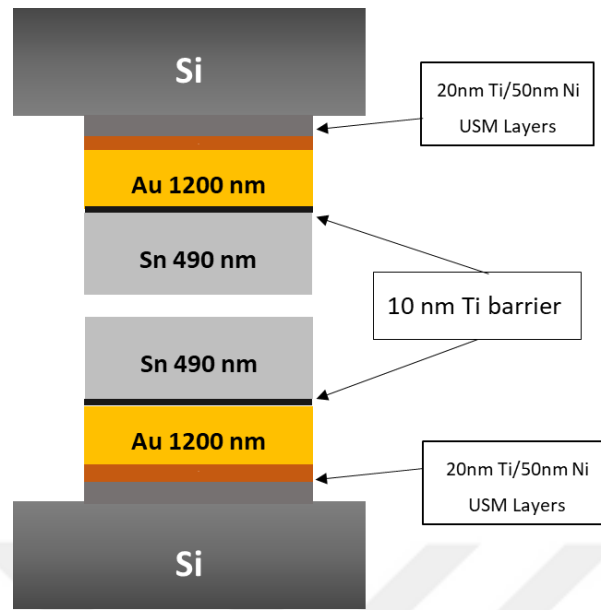


Figure 3.49: Symmetric Au-Sn TLP bonding configuration with intermediate barrier layer design.

The Bonding Experiments with Intermediate Barrier Layer

The bonding configuration is given in Figure 3.49. Note that this bonding configuration is symmetric, and it requires Sn deposition on both cap and substrate wafer. The symmetric configuration limits the process integration potential of the bonding process. The initial bonding experiments with this configuration were performed using non-patterned wafers. The thickness configuration aims a final composition of approximately 8-10 wt. % Sn in the final bond. The structure of the bond is expected to have Au_5Sn (ζ') phase. The wafers surfaces were treated with Ar^+ reverse sputter cleaning before bonding. Two different, 30 sec and 60 sec, cleaning durations were applied for the wafers. The bonding was performed at 300 °C under 3 MPa bonding pressure for 30 minutes. The SAM images of the bonded wafers is presented in Figure 3.50.

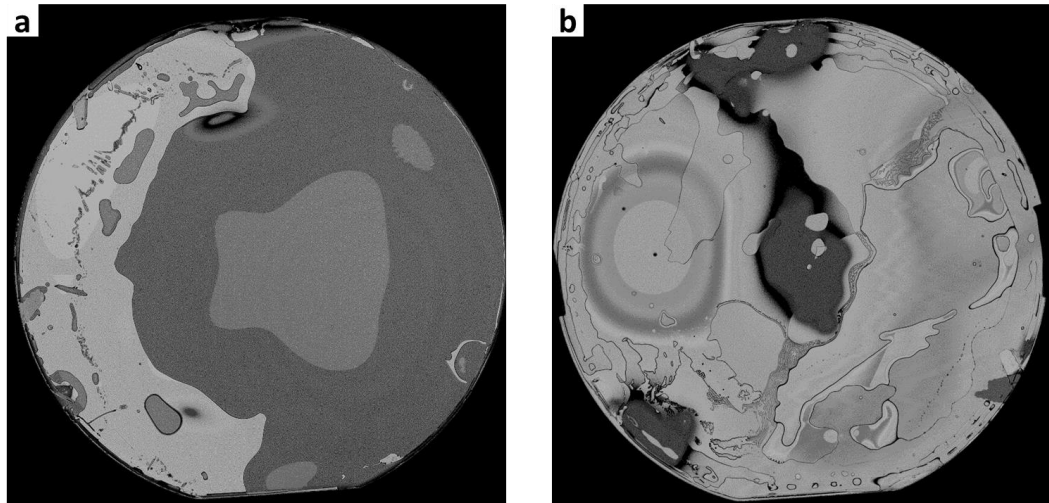


Figure 3.50: SAM images of (a) 30 sec Ar^+ reverse sputter cleaned and (b) 60 sec Ar^+ reverse sputter cleaned wafers bonded with Au-Sn TLP bonding with the intermediate barrier layer.

The interface of the wafers bonded with 60-sec reverse sputter cleaning looks more chaotic than the other with the sign of a better liquid formation. Note that this bonding configuration implements Sn as the liquid phase. So, the advantage of this design is that the bonding temperature can be close to the melting temperature of pure Sn. The bonding temperatures lower than 300 °C has been intended for the next bonding experiments. Another bonding after 60-sec reverse sputter cleaning was performed at 280 °C with 3 MPa bonding pressure. The SAM image of the wafers is given in Figure 3.51.

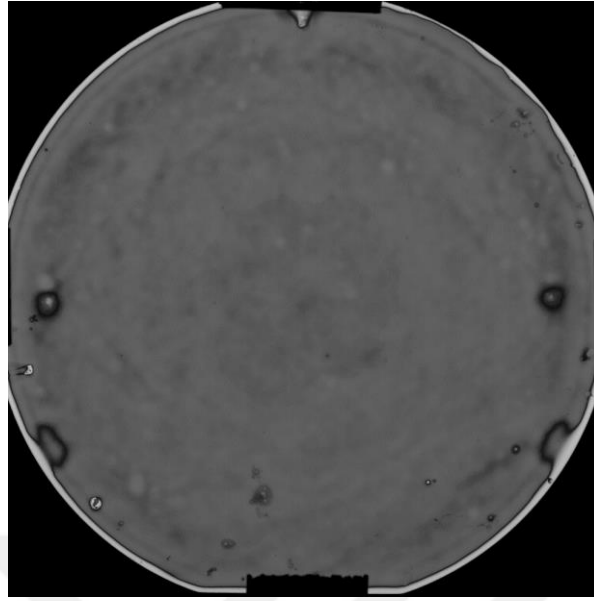


Figure 3.51: The SAM image of the wafers bonded with Au-Sn TLP with intermediate bonding at 280 °C with 3 MPa bonding pressure.

The wafer is diced to test the mechanical strength of the bond. 5mm x 5mm sized samples are used to test with the shear strength tester. The position of the selected dies to be tested, and their test results are given below in Figure 3.52. The shear strength of the selected dies ensures MIL-STD 883 requirement.

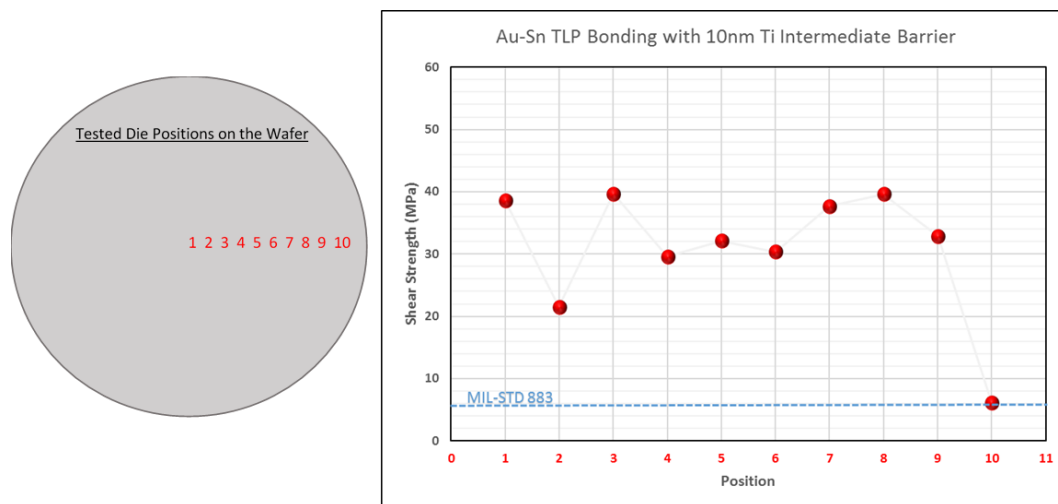


Figure 3.52: The shear test results of the dies from the wafers bonded using Au-Sn TLP bonding with a 10 nm Ti intermediate barrier layer.

Asymmetric Design of Au-Sn TLP Bonding with Intermediate Barrier Layer

The bonding design provided in Figure 3.49 requires Sn deposition on both wafers. As mentioned before, this limits the integrability of the method into device fabrication processes. The more flexible design in terms of integrability of the method into device fabrication processes can be obtained with an asymmetric design, which is shown in Figure 3.53. The asymmetric design implements only Au and intermediate barrier on one wafer. The other wafer has an Sn layer on the intermediate barrier and Au layers.

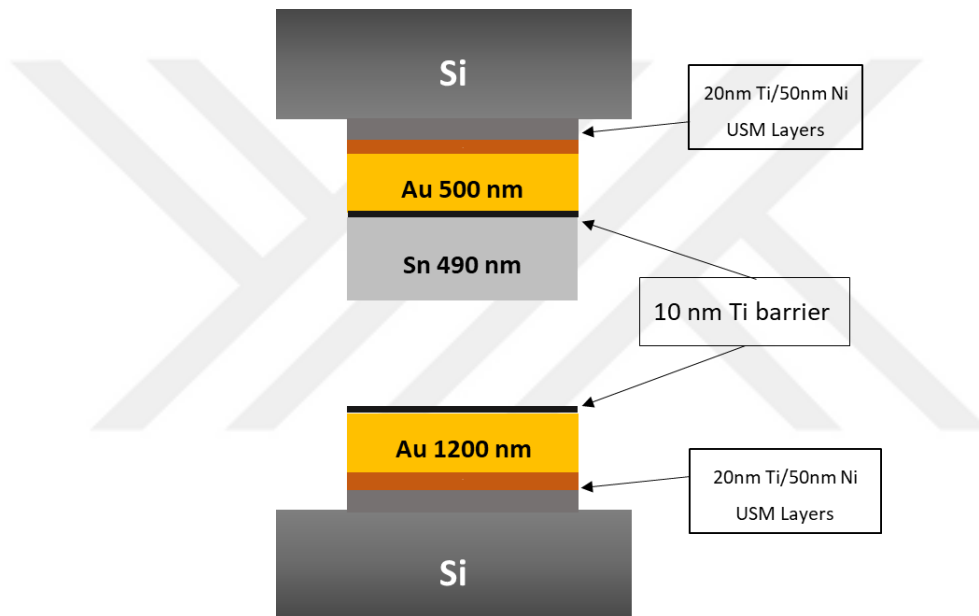


Figure 3.53: The design of asymmetric Au-Sn TLP Bonding with the intermediate barrier layer.

The total composition of this design has been aimed to have 8 wt. % Sn. The Sn containing part of the bond material was deposited and annealed in the bonding chamber at 250 °C for 30 minutes. The SEM image of the annealed material is shown in Figure 3.54. The structure of the material shows that a liquid phase is obtained during annealing. There are some voids in the solidified material. The EDS result of the alloy yielded 22.9 wt. % Sn. The composition is close to the aimed composition for this part of the bond material.

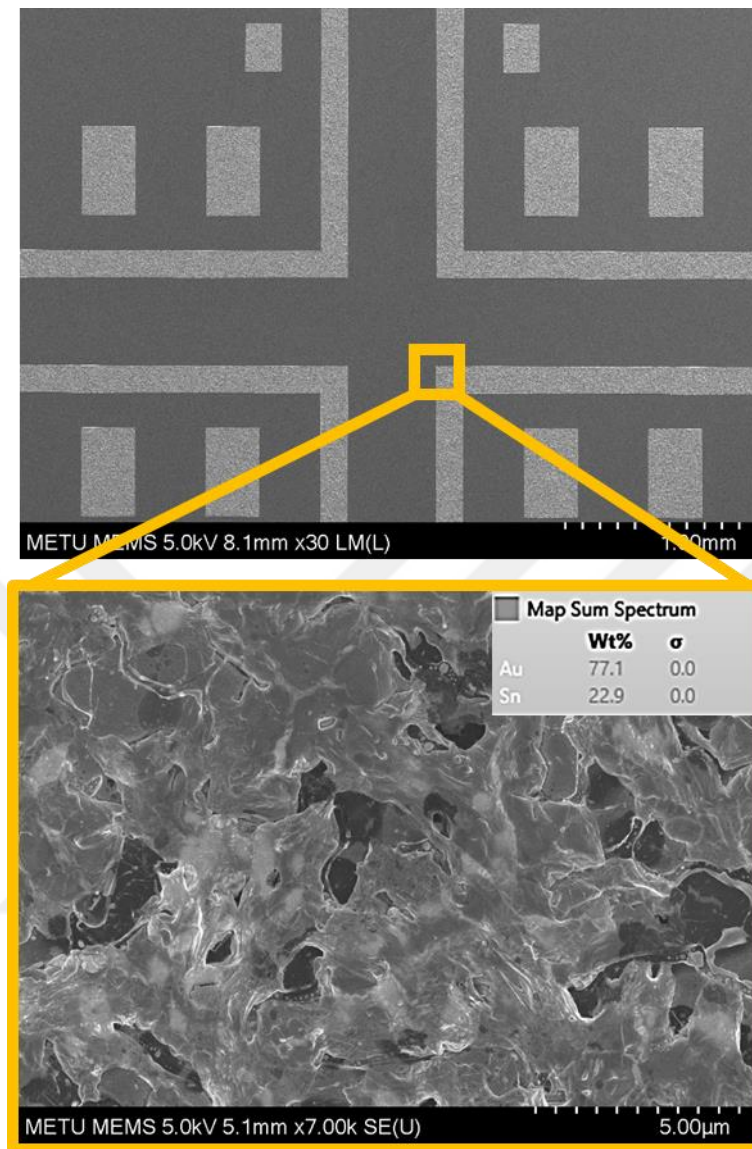


Figure 3.54: The SEM image of the Sn containing part of the asymmetric design of Au-Sn TLP bonding after annealing.

The bonding of the wafers with asymmetric configuration was performed at 280 °C with 3 MPa pressure. Then the wafers were diced for the shear test. However, the bonding performed with the asymmetric design was not strong enough. The wafers have been broken during the dicing. So mechanical characterizations could not be realized. The photograph of the broken wafers is provided in Figure 3.55. The poor

bond that occurred in this process might be caused by the oxidation of the barrier layer on the gold layer.

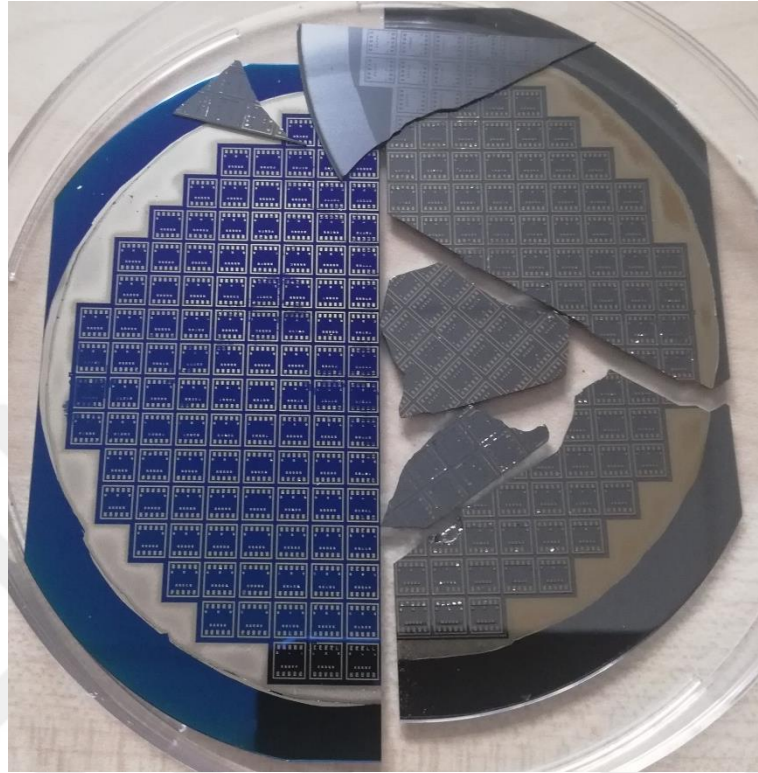


Figure 3.55: The photograph of the failed asymmetric Au-Sn TLP bonding with an intermediate barrier layer.

Although, the barrier layer method promises a low-temperature TLP bonding with relatively low thickness Sn and Au layers. The integration of this method is more flexible with the asymmetric configuration. The asymmetric configuration brings its challenges. The oxidation of the barrier layer does not allow a successful bond formation.

To sum up, Au-Sn material system has been implemented in two different approaches to overcome the critical thickness requirement of the material system and to enable bonding with ultra-thin layers. The TLP bonding approach with eutectic liquid is promising one with hermetic and mechanically robust packages. A comparison of Au-Sn TLP bonding of this work with the other in literature and the

overall summary of the works implementing Au-Sn TLP bonding as a wafer-level packaging method is provided in Table 3.6.

Table 3.6: Summary of Au-Sn TLP bonding works.

Au-Sn TLP Bonding						
Ref.	Total Material Thickness (μm)	Material Deposition Method	Bonding Temperature ($^{\circ}\text{C}$)	Max. Bond Strength (MPa)	Leak Rate (atm.cc/s)	Leak Test Method
This Work	2.24	PVD	320	50	$<10^{-9}$	He Leak
[45]	12	Electroplating	350	24	NA	NA
[47]	10	Electroplating	350	270	NA	NA
[48]	8.3	Electroplating	240	110	NA*	PCT
[49]	16	Electroplating	350	170	NA**	MFG
[50]	6	Electroplating	320	180	NA	NA

* The package is hermetic.

**The package is non-hermetic.

CONCLUSION AND FUTURE WORK

Three different material systems have been investigated in terms of their bond formation and their potential for wafer-level encapsulation of MEMS devices. While the Al-Ge material system has been investigated for the eutectic bonding method, the Au-In, and the Au-Sn material systems have been investigated for the TLP bonding method.

Al-Ge material system is a promising material system for wafer-level encapsulation of CMOS based MEMS devices. In this work, it has been investigated because of its capability to be bonded on widespread passivation surfaces like Si_3N_4 and Al_2O_3 . The bonding can be performed having the eutectic alloy only on the cap wafer, which enables a very high degree of integrability of the method into device processes. The eutectic composition has been optimized, and bonding experiments have been performed. However, this material system needs proper surface preparation and cleaning methods prior to bonding. Native oxide cleaning with wet and dry processes was applied for the material system, but the bonding results were not as good as to obtain hermetically sealed packages. Although very strong bonds have been formed between the wafers, the major strength was delivered by the bonding of squeezed-out material to the substrate surface. An in-situ plasma cleaning method or in-situ formic acid treatment in the bonder system can result in better bonds with hermetic properties along with high strength. Besides, this method still can be applied for the bonding application, which does not require hermetic packages. The future works on this material system can be performed to optimize the oxide treatment processes for the case that the in-situ oxide cleaning methods are not available.

Au-In material system provides a low-temperature solution for TLP bonding applications with indium as liquid phase and IMCs with relatively high re-melting temperatures. In this work, Au-In TLP bonding has been demonstrated in 6 inches sized wafers with 200 nm topography. The bond material was able to compensate 200 nm topography on the wafer and formed strong bonds with 40-50 MPa shear

strength between substrate and cap wafers. The hermeticity of the bonds that were measured as $1 \times 10^{-8} \text{ atm.cc/sec}$ provides the requirement of MIL-STD 883 standard. The demonstration of process integration for MEMS devices, which implement PI sacrificial layers in fabrication steps, has also been performed. The bond ring materials were fabricated on the wafers with a 2 μm thick sacrificial PI layer. The gold layer on the substrate side enabled the PI removal step to simulate the releasing process of suspended MEMS structures. The application of this method to real MEMS devices wafer can be performed in the future works.

The most comprehensive work has been performed for Au-Sn material systems. Although this material system requires relatively thick layers ($>8\text{-}10 \mu\text{m}$) for the TLP bonding method, this work has proposed very thin ($<2 \mu\text{m}$) layers for Au-Sn TLP bonding. Thin layer design enables the use of PVD systems for material deposition. Accordingly, the bond materials can be formed on larger wafers (6 or 8 inches) more uniformly. Also, thinner metal layers make the process integration easier. Au-Sn TLP bonding was proposed with two main approaches.

One approach uses the eutectic material stack to be bonded to the gold layer to form a solid bond with high gold content. The layer thicknesses have been designed to have a microstructure that enables a re-melting temperature higher than 500°C . Therefore, the bonding method can be implemented with MEMS devices that need high-temperature post-processing such as getter activation. This approach has provided strong bonds with 35-40 MPa shear strength. The shear surface analysis showed that AuSn intermetallic phase was present in the structure. The dissolution of this phase may be provided with longer bonding durations. If the device allows higher bonding temperatures, increasing the bonding temperature can also be the solution. The hermeticity of the bonds has been investigated with the He-leak test resulting in smaller leak values than $0.1 \times 10^{-9} \text{ atm.cc/sec}$. The bonding was implemented into CMOS based $\mu\text{bolometer}$ devices wafer using the integration steps developed with Au-In TLP bonding. The integration is performed with 6 inches wafers due to the limitation dictated by the Sn evaporation system, which handles

maximum 6 inches wafers. However, the bonded wafers have been failed during the dicing step. An unexpected residual layer was observed under the bond ring material. It has been investigated that the layer was resulted due to the interaction of the Ti adhesion layer with CMOS surface passivation. The surface passivation of the CMOS wafer acted differently than the ones applied in the development stages. As future work, the adhesion layer combination should be adjusted according to CMOS surface passivation. Nonetheless, the method provided a good bonding that can be integrated into commercially available device processes with some tuning.

The second approach of the Au-Sn TLP bonding proposed in this work employs a thin barrier layer between the Sn layer and the Au layer. The thin barrier layer retards the interdiffusion of layers into each other and provides Sn layers more time to melt. This approach enables the use of a pure Sn layer with thinner thicknesses than the dictated by the critical thickness model. The symmetric approach has been demonstrated with bond strengths of 30-40 MPa. However, this approach is not very flexible in terms of process integration. It can be challenging to use the Sn layer on the device layer processes. Therefore, the asymmetric approach with more integration flexibility has been designed. The asymmetric approach implements the Sn layer only on the one wafer, and the other wafer contains only gold and a thin barrier layer. However, strong bonds could not be achieved using this approach. This weakness of the bonds has been attributed to the possible oxidation problem of the barrier layer. A thin gold layer may be applied to the barrier layer; however, it may be discussed that the formation of Sn rich intermetallic can create problems of intermixing between the underlying gold layer. To increase the bonding temperature above 300 °C may overcome the problem; however, the approach loses its low-temperature bonding advantage in that case.



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BS	METU Metallurgical and Material Engineering	2011
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WORK EXPERIENCE

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2012-2015	METU KANAL	R&D Engineer
2011-2012	Atılım University Metallurgical Eng.	Research Asistant
2010 August	Türk Traktor AŞ.	Intern Eng. Student
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FOREIGN LANGUAGES

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PUBLICATIONS

1 E.C Demir; O. Temel; T. Akin; E. Kalay, “Low Thickness Au-In TLP Hermetic Encapsulation” , TMS Annual Meeting&Exhibition, February 26 – March 2, 2017 • San Diego, California, USA

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