MEMS Compatible Highly Doped Piezoresistive Silicon Nanowires: Fabrication and Electromechanical Characterization

by

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A Dissertation Submitted to the
Graduate School of Sciences and Engineering
in Partial Fulfillment of the Requirements for
the Degree

of Doctor of Philosophy

in

Mechanical Engineering

KOÇ ÜNİVERSİTESİ

August 4th, 2022

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This is to certify that I have examined this copy of a doctoral dissertation by

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and have found that it is complete and satisfactory in all respects,
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To my beloved wife and daughters…

ABSTRACT

Electromechanical properties of silicon nanowires attract technological and scientific interest due to their enormous potential of miniaturization and replacement of conventional transduction schemes. For this purpose, piezoresistivity is mainly employed. Piezoresistive response can differ due to fabrication technique, dopant type, dopant concentration, crystallographic orientation, temperature and humidity. In this dissertation, a specific nanowire array architecture is studied through four-point bending tests. Mechanically coupled vertical silicon nanowire arrays are considered as the building blocks of new generation resonators and their piezoresistivity characteristics play key role in designing such devices. Two different test setups are used. In the first setup indirect bending is induced as an adhesive layer is present between the device under test and a carrier silicon strip. Second setup provides direct bending of silicon nanowire arrays. 3D simulations are carried out to obtain strain of the nanowires. Effective gauge factors are extracted as -29.2±6.47 (standard deviation) for indirect bending, and -105.37±8.12 (standard deviation) for direct bending, providing a clear indication regarding the effect of the adhesive layer used in testing. This work is the first study providing the gauge factor estimation of the vertically stacked silicon nanowires. In addition, this electromechanical study provides substantial experimental evidence as it provides a comparative quantification of direct and indirect bending on nanowire piezoresistivity characterization.

ÖZETÇE

Silisyum nanotellerin elektromekanik özellikleri, geleneksel transdüksiyon yöntemlerinin yerini alabilme ve muazzam minyatürleştirme potansiyeli sebebiyle teknolojik ve bilimsel ilgiyi cezbetmektedir. Bu amaçla, ağırlıklı olarak piezorezistivite kullanılmaktadır. Silisyum nanotellerin piezorezistif tepkisi imalat tekniğine, katkılama türüne, katkılama konsantrasyonuna, kristalografik yönelime, sıcaklığa ve neme göre farklılık gösterebilmektedir. Bu tezde, özgül bir nanotel dizi mimarisi dört nokta bükme testi vasıtasıyla çalışılmıştır. Mekanik kuplajlı, dikey silisyum nanotel dizilerinin yeni nesil çınlaçların temel yapıtaşları olduğu hesaba katılmakta ve piezorezistif özellikleri bu cihazların tasarımında anahtar rol oynamaktadır. İki farklı test düzeneği kullanılmıştır. Birinci düzenekte, testten geçirilen cihaz ve taşıyıcı silisyum şerit arasında yapıştırıcı tabaka bulunması vasıtasıyla dolaylı bükme uygulanmaktadır. İkinci düzenek silisyum nanotel dizilerinin doğrudan bükülebilmesine olanak sağlamaktadır. Nanotellerin gerinimini elde etmek için üç boyutlu benzetimler yapılmıştır. Etken ölçüm faktörü dolaylı bükme için -29.2±6.47 (standart sapma), ve doğrudan bükme için -105.37±8.12 (standart sapma) olarak çıkartılmış, testlerde kullanılan yapıştırıcı tabakanın sonuçlara etkisine ilişkin açık bulgu sağlanmıştır. Bu çalışma, dikey istifli silisyum nanotellerin ölçüm faktörü tahminini sağlayan ilk çalışmadır. Ek olarak, bu elektromekanik çalışma, nanotel piezorezistivite karakterizasyonunda doğrudan ve dolaylı bükmenin karşılaştırmalı nicelikselliğini sağlaması sebebiyle değerli bir deneysel kanıt sunmaktadır.

ACKNOWLEDGEMENTS

Before anything else, I would like to present my extreme gratitude to my advisor Prof. B. Erdem Alaca for accepting me as a part of his great research group. His endless support and guidance during my studies and even in my life helped me to overcome the extreme challenges. His very own perspective of evaluating each problem and life changing advices deserve a full of admiration and appreciation.

I also would like to thank Prof. Yusuf Leblebici for inviting me and providing such an outstanding work environment in LSM-EPFL.

I am indebted to my dissertation committee members Prof. Arda D. Yalçınkaya, Prof. Demircan Canadinç, Prof. Murat Sözer and Asst. Prof. Mohammad Nasr Esfahani for their contributions to successfully accomplish this dissertation.

I am very grateful to the past and current members of Mechanical Characterization Laboratory for their sincere fellowship throughout this journey.

Last but not least, I thank my colleagues in DeltaV Space Technologies, Istanbul and Aselsan, Ankara for their support and company.

This study is supported by TUBITAK BIDEB 2228-B and 2214-A programs.

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ABBREVIATIONS

4-PB	Four-Point Bending
BHF	Buffered Hydrofluoric Acid
BOX	Buried Oxide
CMi	Center of MicroNanoTechnology
CMOS	Complementary Metal Oxide Semiconductor
CNC	Computer Numerical Control
Cr	Chromium
CVD	Chemical Vapor Deposition
DETF	Double-ended Tunable Fork
DIC	Digital Image Correlation
DRIE	Deep Reactive Ion Etching
EBID	Electron Beam-Induced Deposition
FIB	Focused-Ion-Beam
GF	Gauge Factor
GND	Ground
HF	Hydrofluoric Acid
I-t,V	Current-Time, Voltage
I-V	Current-Voltage
IMU	Inertial Measurement Unit
LPCVD	Low Pressure Chemical Vapor Deposition
LTO	Low Temperature Oxide
MCL	Koç University Mechanical Characterization Laboratory
MEMS	Micro ElectroMechanical Systems
NEMS	Nano ElectroMechanical Systems
N/A	Not Available
NMOS	N-type Metal Oxide Semiconductor
NW	Nanowire
PMMA	Poly Methyl Methacrylate
PMOS	P-type Metal Oxide Semiconductor

Pt	Platinum
RIE	Reactive Ion Etching
SCREAM	Single Crystal Reactive Etching And Metallization
SEM	Scanning Electron Microscope
Si	Silicon
SiNW	Silicon Nanowire
SiNWFET	Silicon Nanowire Field-Effect Transistor)
SOI	Silicon-on-Insulator
STD	Standard Deviation
STM-TEM	Scanning Tunnelling Microscope – Transmission Electron Microscope
TEM	Transmission Electron Microscope
TMAH	Tetramethylammonium Hydroxide
VLS	Vapor-Liquid-Solid

Chapter 1

INTRODUCTION

1.1. Piezoresistivity of Materials

Piezoresistivity is the resistance response of a material under a tensile or compressive mechanical load. Gauge factor (GF) and piezoresistivity coefficient (π) are considered as the piezoresistivity measure of materials in general and mathematically expressed as in equations (1.1) and (1.2)

$$GF = \frac{\Delta R/R}{\varepsilon} \tag{1.1}$$

$$\pi = \frac{\Delta R/R}{\sigma} \tag{1.2}$$

where "R" stands for the initial resistance of the unstrained material, ΔR the change is resistance after applied strain, ε applied mechanical engineering strain and σ applied mechanical stress. On the other hand, the resistance of a material can be provided as in equation (1.3),

$$R = \rho \frac{l}{A} \tag{1.3}$$

where ρ is the resistivity of the material, l the specimen length and A the specimen cross-section area as the geometric parameters of the material.

While various materials can exhibit piezoresistive behavior, different research reports reveal gauge factor values as 2-12 for metals, 5-150 for semiconductors and 100-500 for organometallic materials, in general [1], [2].

Benefitting the utility of the gauge factor, the piezoresistive materials can enhance the measurement quality over other methodologies such as capacitive [3]. Therefore, piezoresistivity is considered as a viable candidate for sensing applications such as pressure gauges, flow meters and accelerometers. The metals exhibit low piezoresistance compared to other materials. Metals' piezoresistivity is based on the geometrical deformation under a certain load as other materials can demonstrate increased piezoresistivity due to carrier trapping and depletion. Nevertheless, metals are the easiest to employ into the complex systems. On the other hand, organometallic materials provide tremendously enhance piezoresistivity compared to metals and semiconductors. However, they are not compatible for sensors. Therefore, as the best candidate, semiconductors, especially silicon, becomes the major point of interest in the last few decades enabling integration and stability capabilities with micromechanical sensors. Although semiconductors provide these opportunities, there is still need for more research on the qualified test methods, temperature dependency and durability in chemical environment for future use [4].

1.2. Piezoresistivity in Silicon

Silicon is a widely used fundamental material in the electronics industry, due to its stable performance and well-understood processing technology. Since piezoresistive effect of silicon was first reported in 1954 [5], it has been successfully used in many devices such as pressure sensors [6]–[9], and accelerometers [10]–[12] based on the relationship between the change in resistance and applied stress/engineering strain.

Recalling the gauge factor and piezoresistivity equations (eq. 1.1 and 1.2), the relation $\Delta R/R$ can be expressed as the addition and substruction of the participating relative change terms.

$$\frac{\Delta R}{R} = \frac{\Delta l}{l} - \frac{\Delta w}{w} - \frac{\Delta h}{h} + \frac{\Delta \rho}{\rho} = (1 - 2\upsilon)\varepsilon_{||} + \frac{\Delta \rho}{\rho} \tag{1.4}$$

l is the length, w is the width, h is the height and ρ is the resistivity of the material. $\varepsilon_{||}$ depicts the geometrical terms of relative changes caused by the axial engineering strain. Usually, the resistance change due to piezoresistivity dominates the overall resistance change in a

semiconductor structure as for the metals it is vice versa. Therefore, the resistance change due to geometric parameters can be neglected for semiconductors [13]. At the end, the relative resistance change ($\Delta R/R$) becomes equal to the relative resistivity change ($\Delta\rho/\rho$). ($\Delta\rho/\rho$) is simplified to a vector provided in the equations below as a result of cubic crystal state of silicon.

$$\frac{\Delta\rho_i}{\rho} = \sum_{k=1}^{6} \pi_{ik}\sigma_k \tag{1.5}$$

$$\pi_{ik} = \begin{pmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{21} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{21} & \pi_{21} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{pmatrix} \tag{1.6}$$

Considering equations (1.5) and (1.6), there are only three independent piezoresistivity coefficients in piezoresistivity coefficient matrix for silicon (π_{ik}). Principal axis and stress axis are same for π_{11} (longitudinal piezoresistive effect), Engineering stress/strain is orthogonal to the principal axis for π_{12} (transversal piezoresistive effect), and shear stress is represented as π_{44}. These values are calculated and provided in [14] for p-doped and n-doped silicon under tensile stress. (Table 1).

Table 1: π_{11} π_{12} and π_{44} for n- and p-doped silicon at room temperature [14]

Doping Type	n-Type	p-Type
ρ [Ωcm]	11.7	7.8
π_{11} [10^{-11} Pa^{-1}]	-102.2	+6.6
π_{12} [10^{-11} Pa^{-1}]	+53.4	-1.1
π_{44} [10^{-11} Pa^{-1}]	-13.6	+138.1

Depending on the crystallographic orientation of the silicon, the uniaxial piezoresistive coefficients, $\pi_{[100]}$, $\pi_{[110]}$ and $\pi_{[111]}$, [15] is given in Table 2.

Table 2: Longitudinal piezoresistivity coefficient models for Si along different directions

$\boldsymbol{\pi_{[100]}}$	$\boldsymbol{\pi_{11}}$
$\boldsymbol{\pi_{[110]}}$	$\boldsymbol{\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}}$
$\boldsymbol{\pi_{[111]}}$	$\boldsymbol{\frac{\pi_{11}+2\pi_{12}+2\pi_{44}}{3}}$

As described previously, gauge factor (GF) is another implementation for the piezoresistivity characterization of materials. While preserving the same assumption that geometrical terms are inferior on relative resistance change, GF is expressed as in equation (1.7)

$$GF = \frac{\Delta R}{R\varepsilon} = \frac{\Delta R\, Y}{R\sigma} \tag{1.7}$$

where Y is the modulus of elasticity and σ the applied stress. Gauge factor of silicon can vary from negative 100s to positive 100s, which is strongly affected by the crystal orientation, temperature, doping type and doping concentration.

1.3. Doping and Its Effect on Silicon Piezoresistivity

Doping of a semiconductor is the introduction of impurities into the crystal lattice structure. The main purpose of the operation is to modify the material's conductivity. Boron and Phosphorus are the major atoms preferred in doping and they are named as "dopants". Boron provides three valance electrons while Phosphorus brings five valance electrons. The type of doping is determined depending on the outer electrons. If the dopant is an element providing three valance electrons, it is named as p-type doping. If the dopant has five valance electrons, it is n-type doping.

1.3.1. p-type Silicon

In a silicon atom, there are four electrons which can establish covalent bonds. Upon forming the covalent bonds, the resultant structure inhibits four valance electrons. The resultant number of electrons and holes will always be equal which represents electron-hole balance

at the end. If an atom in the lattice is replaced, this balance will be altered. Considering the replacement atom as Boron, three valance electrons shall be available, which will result with an extra hole. Therefore, extra hole will receive the free electrons.

The final structure gives the extra hole and gets charged positively. Consequently, silicon shall be named as p-type meaning "positive". When subjected to potential difference, the

current is mainly carried by the holes. In this case, holes are the majority carriers and electrons are the minority carrier [16], [17].

1.3.2. n-type Silicon

On the contrary, if the replacement atom in the lattice structure is selected as Phosphorus, five valance electrons will be introduced to the structure. Eventually, there will be extra electron in the lattice. Since it will give the electron, this time this time it will be negatively charged. The resulting structure will be named as n-type meaning "negative". Since electrons are excessive, the current is mainly carried by the electrons. In this case, electrons are the majority carriers and holes are the minority carriers [16], [17].

1.3.3. Doping Effect on Piezoresistivity

Conductivity of silicon is improved through doping. In 1981, Thurber indicated the relationship between resistivity and dopant density [18]. Figure 4 indicates that phosphorus (n-type) and boron (p-type) doped silicon resistivity differs approximately 10% from each other. Determining the resistivity value during piezoresistive device design is utmost importance so that doping density is decided accordingly. In most of the applications, doping is the very first step before jumping to the coating or lithography steps. Doping is also processed in the later steps of fabrication a few times to enhance conductivity of the desired sections of the utility device. For example, a silicon nanowire (SiNW) can be subjected to 10^{18} cm^{-3} while the electrical contact pads can be doped to 10^{20} cm^{-3} to achieve ohmic contact by reducing the contact pad resistance. As the scope of this thesis is based on doped silicon nanowires, it is important to note that one should consider the relationship between resistivity, dopant type and doping level during the analytical design of a MEMS and/or

NEMS device.

Doping concentration (N) and temperature (T) is a principal factor that affects piezoresistivity. Kanda developed and introduced a theoretical model in [14] for the relationship between doping density, temperature and piezoresistive coefficient. These graphics are very beneficial on interpreting piezoresistive coefficients for low doping levels.

P(N,T) in Figure 1 is the multiplication factor which is used to evaluate piezoresistive coefficient at a different temperature by multiplying with room temperature piezoresistivity coefficient at a certain doping concentration. High doping concentration and temperature also decreases the piezoresistive coefficient. Increasing the doping concentration to 10^{20} cm-3 for various temperatures converges to a point. Abdelaziz, [19] also supports this model by studying the same variables, as well.

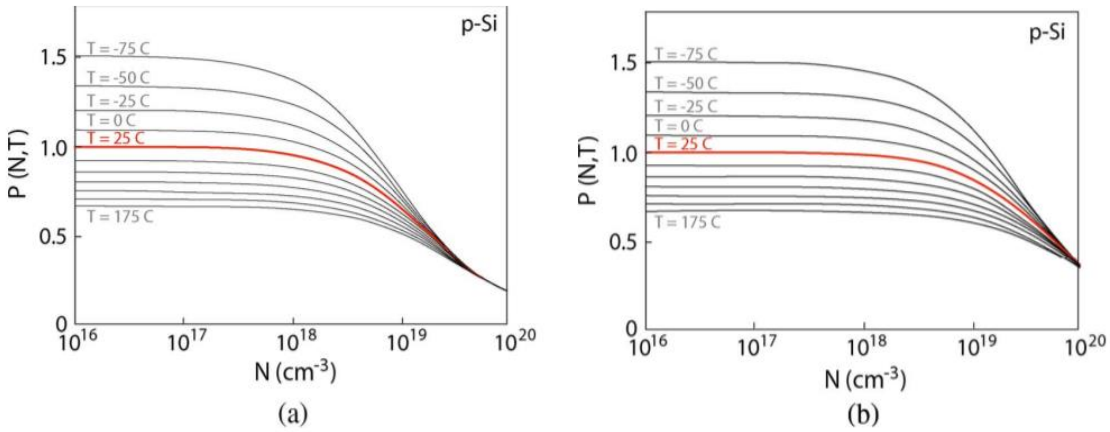


Figure 1: Piezoresistance factor P(N,T) as a function of impurity concentration and temperature for (a) p-type silicon and (b) n-type silicon. Taken from [14].

On the other hand, Mason [20], Tufte [21] and Kerr [22] conducted experiments on the effect of Boron concentration to the piezoresistive coefficient. Harley and Kenny [23] used a regression line to fit the data of these studies and plotted all of them in the same figure with Kanda's findings (Figure 2). It's noticed that Kanda's theoretical calculation for high concentration piezoresistivity coefficient is quite smaller than the experimental results.

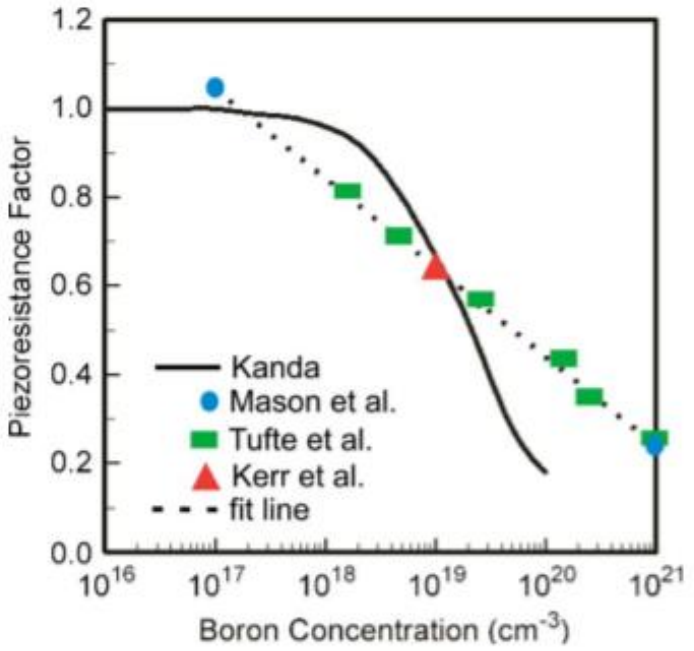


Figure 2: Experimental data and theoretical estimation comparison of piezoresistive coefficients as a function of doping concentration of Boron. Taken from [23].

In addition, it is crucial to identify piezoresistivity with respect to crystallographic orientation. While Smith, Pfann and Thurston provided analyses for n-type and p-type piezoresistors, Kanda widened and implemented these into a scheme that provides graphical representations of piezoresistive coefficients in different directions for both longitudinal and transverse geometries (Figure 3).

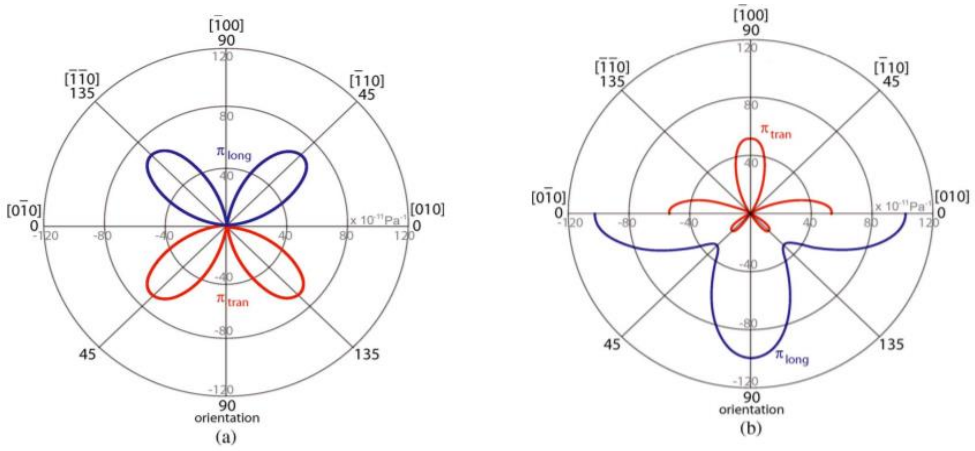


Figure 3: Room temperature piezoresistive coefficients in (a) p-type (b) n-type silicon. Taken from [14]

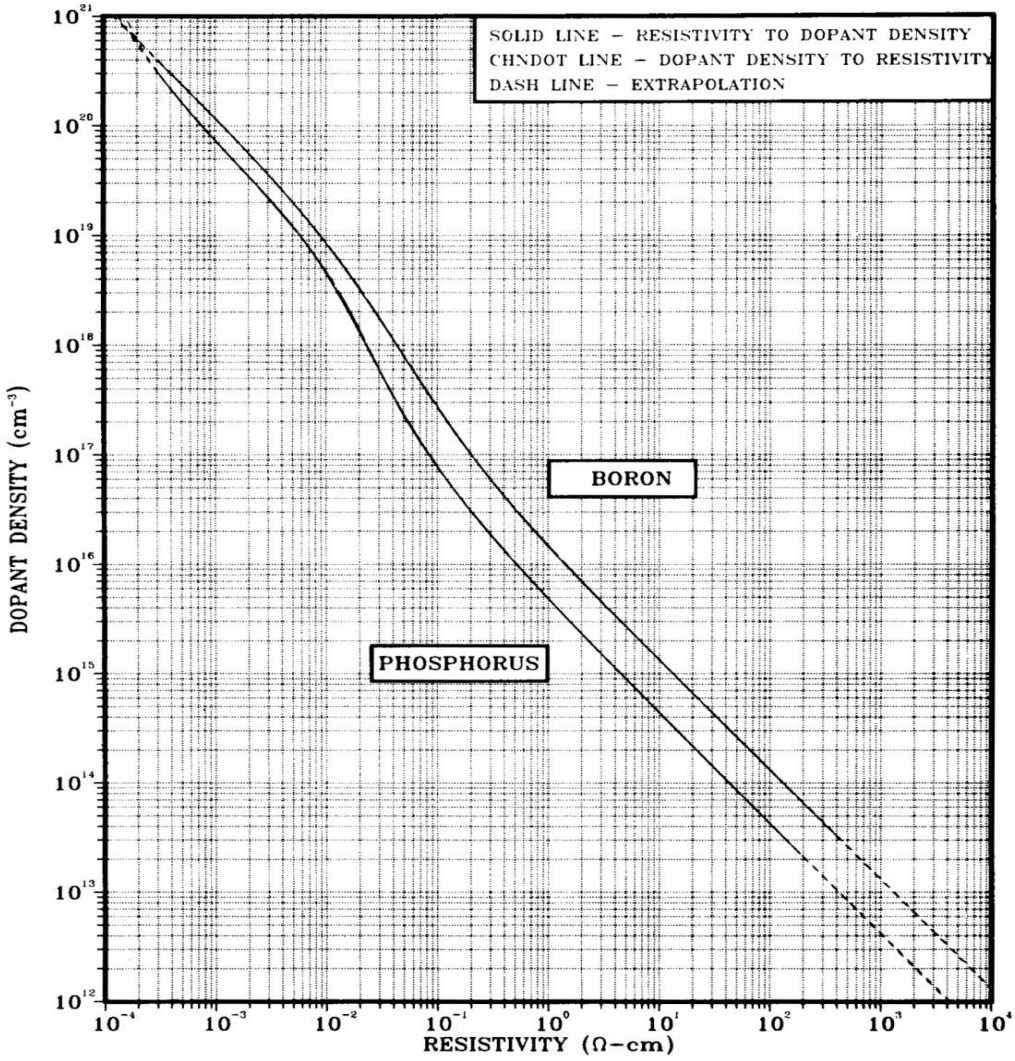


Figure 4: The relationship between resistivity and dopant density for p- and n- doped silicon. Taken from [18]

1.4. Silicon Nanowires

One-dimensional nanostructures such as silicon nanowires (SiNWs) have been receiving significant interest for different applications such as sensors, electronics, MEMS and NEMS. It is accepted that their small dimensions and large surface to volume ratio provides beneficial opportunities [24]. Therefore, an increased effort in understanding of their mechanical, thermal, and electrical properties are necessary. In such manner, it is studied and reported that SiNWs are valuable components for electromechanical applications because of their piezoresistive capabilities. Experiments have been showing that some properties of one-dimensional nanostructures vary from the bulk values [25], [26].

Piezoresistive silicon nanowires are fabricated mainly by two approaches: bottom-up and top-down. Bottom-up approach is based on synthesizing and VLS (vapor-liquid-solid) growing the nanowire along a direction. The process is firstly reported by [27]. Currently, SiNWs are mostly grown via VLS assisted CVD (chemical vapor deposition). [28]. Since SiNWs are considered as valuable technological blocks to replace larger and less sensitive transducers [29] such as capacitive transducers [3] in MEMS, physical integration of MEMS and SiNWs stays as a major challenging issue. To this end, aforementioned synthesized-SiNWs are commonly integrated to the bulky MEMS movable mass via a nano "pick-and-place" procedure which might introduce new challenges such as alignment and rigid /reliable physical integrity between MEMS and SiNW. For top-down approach, such challenges are addressed in terms of development and implementation of monolithic integration and fabrication procedures [3], [24], [30]–[33]. For bottom-up approach, to solve this issue, Winkler et. al [34], conducted VLS process directly on the MEMS anchors and subjected the samples to electromechanical testing. However, counting on commercial concerns, even though this technique brings testing advantages by producing thousands of SiNWs at the same time, individual work for each SiNW requires more effort.

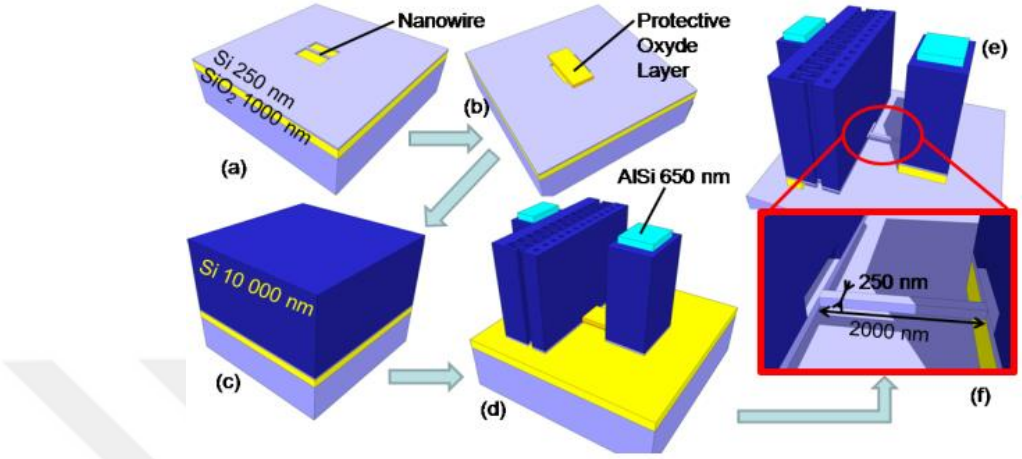


Figure 5: Schematic view of fabrication flow of top-down SiNW fabrication and depositing thick structural silicon. Taken from [3]

Top-down approach, as an alternative to bottom-up method, provides compatibility with conventional CMOS processes. Bringing the advantage of low power consumption and resizable transduction, top-down approach is mainly utilized for thin layer microelectronic substrates (hundreds of nanometers). The thickness of SiNW and the surrounding structure is similar to each other [35]–[37]. Considering the MEMS blocks which are order of magnitude thicker than SiNWs, nanostructure is first fabricated on a thin device layer and then a thick silicon layer is deposited to create MEMS block (Figure 5) [3].

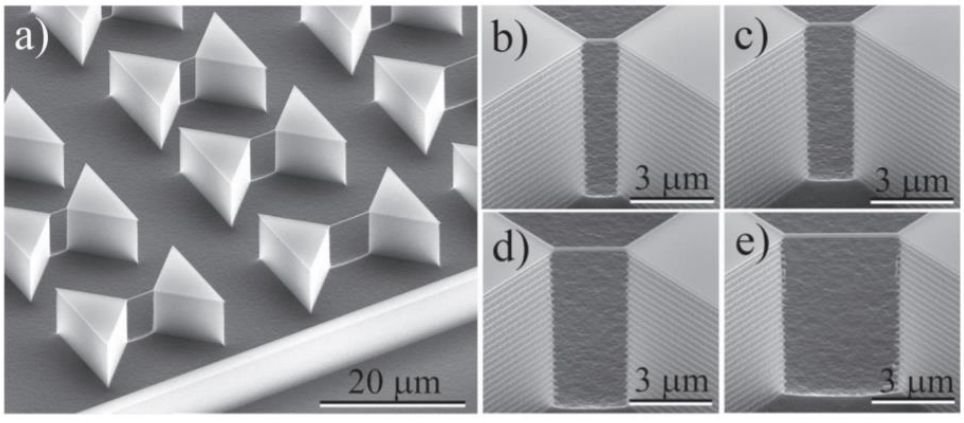


Figure 6: (a) SiNWs on silicon test wafer, 10µm etch depth. (b) width: 35nm, aspect ratio: 50, (c) width: 40nm, aspect ratio: 50, (d) width: 74nm, aspect ratio: 50. Taken from [31]

Top-down fabrication approach is reported to be beneficial for the applications such as accelerometers [12], [38]–[40], magnetometers [41] and gyroscopes [42] which are the main components of an IMU (Inertial Measurement Unit) [43]. IMUs are devices based on inertial sensing and fundamentally used for navigation and stabilization purposes. In the last decade, more complex and convenient studies are conducted to fabricate SiNW based NEMS and MEMS monolithically (Figure 6). Taşdemir, et. al, successfully fabricated the monolithically integrated silicon nanowires with wide anchors. Anchors are 10µm-thick and considered as MEMS blocks out of silicon test wafer for future implementations [30], [31]. This fabrication technique is based on an approach resembling to SCREAM process in which the nanowire is preserved with a surrounding LTO coating, and an e-beam resist through Si deep etch. Following the footsteps of Taşdemir, Esfahani achieved to preserve the SiNWs until a maximum etch depth of 40µm [32] in a silicon wafer. These studies are encouraging and enlightening the pathway of bridging the NEMS and MEMS together. Finally, with the same methodology, Esfahani conducted electromechanical characterization of monolithically integrated n-doped silicon nanowires via using a comb-drive actuation-based MEMS platform [44]. This study will be introduced in later section which introduces available different techniques used to evaluate silicon nanowire piezoresistivity. In addition, the author of this thesis and Mustafa Yılmaz performed in-situ fracture test on a silicon nanowire which utilizes a monolithically integrated 10µm-thick com-drive MEMS based tensile testing platform [33].

1.5. Piezoresistivity of Silicon Nanowires

Mechanical means of engineering stress/strain employment changes the electrical resistance of conductive materials, which yields to the piezoresistive effect. For metals, change in geometrical shape is the main factor this effect, as for silicon the fractional change in resistance is larger quite than metals and is a result of modification in the energy band structure with applied stress [45]. The piezoresistivity is identified by the piezoresistivity coefficient, which stands for the rate of resistance change per unit applied engineering stress and/or strain along a specific direction. Due to the cubic symmetry of silicon, there are only three independent coefficients. Specifically, in p-type silicon these coefficients are known to

be of the order of 10^{-11}-10^{-9} Pa^{-1} [46].

The electrical properties of SiNWs have been detailly studied and reported. Unfortunately, the information is limited and need more convenient testing for various aspects. The great challenge on the study of properties of such materials is the necessity of controlled measurement at very small scale. [47], [48] from CEA LETI (France) and [25] agree on the fact that efficient actuation and sensitive detection of the SiNW displacement/strain remains a challenge. The displacements of these miniaturized devices are on the order of nanometers and the readout signals are stated to be very low which can easily be overwhelmed by parasitic interference. There appear various transduction methods such as magnetomotive [49], capacitive [50], piezoresistive [51], [52] and field-emission [53] transduction in the literature. To compare all with each other; magnetomotive detection is not feasible since it requires large magnetic fields. Field-emission detection brings stability issues over time while requesting expensive equipment. Finally, Piezoresistive detection is superior to capacitive in terms of higher signal to noise ratio [3] and provide benefits at high resonance frequencies [48].

In the literature, gauge factor is usually reported between approximately -150 and +150 depending on the dopant type, concentration, and direction of load. However, there are studies reporting the enhanced piezoresistivity values as named after “giant piezoresistivity” for silicon nanowires. The consensus on the origin of the giant piezoresistivity on the silicon nanowires is not established. [54] suggested that enormous piezoresistivity is caused by carrier trapping and detrapping at the surface, while [55] claims that applied mechanical stress/strain induces carrier depletion within silicon nanowires resulting with giant piezoresistivity. On the other hand, [56] proposes electron trapping might be affecting the giant piezoresistivity of the silicon nanostructures.

So far, giant values of piezoresistive coefficients and conductance enhancement have been extensively studied for both n-type and p-type SiNWs [57]. As more research is available for bulk and top-down nanowires, less work exists on bottom-up grown nanowires due to test

compatibility problems. Integration with larger scale structures is still challenging [58]. The very first experimental studies processed by [59] reveals enormous piezoresistive effect resulting with 3,776% conductance enhancement at single crystal SiNWs in <111> direction. Then, [60] studied on the piezoresistivity as a function of temperature and stress on silicon nanowires which are fabricated with top-down approach. It is reported that up to 633% piezoresistive enhancement is achieved while decreasing the sample diameter in the <110> direction, which is also convenient with the findings of He and Yang. In addition, [61] achieved 2,140% conductance increase compared with the bulk silicon in the same direction, <110>. It was noted that they fabricated 10 nanowires on an SOI substrate. The nanowires consist of various width (25, 50, 75, 100nm) and length (300, 600, 1200 and 2400nm). The nanowires were completely undoped. Test methodology includes employment of uniaxial tensile stress around 200 MPa onto the nanowires.

As another example, there is a study reporting that "anomalous" piezoresistivity is observed at p-type SiNWs under high engineering strain [62]. The measurements are performed on vapor-liquid-solid (VLS) grown Si nanowires which are monolithically integrated in a micro electromechanical loading module. It is noted that positive piezoresistivity is obtained for low engineering strain values (less than 0.8%), whereas ten (10) times resistance reduction of SiNW is achieved for ultrahigh tensile strain values (3.5%). Whereas, [45] influences the n-type SiNWFETs with a back-gate bias to enhance the piezoresistivity. The gauge factor is reported as 1861 after a series of repetitive tensile and released strain cycling.

After all, piezoresistivity of silicon nanostructures is a remarkable area of interest. To conduct the piezoresistivity characterization, fractional resistance change should be measured for applied engineering stress / strain. Due to various components such as doping type, density, temperature, sample crystallographic orientation and amount of engineering stress / strain, empirical results may differ. Therefore, controlled experiments should be planned and conducted accordingly.

Small dimensions of the SiNWs turns the electromechanical characterization into a challenging task. To quantify the piezoresistivity of nanostructures, various experimental

techniques have been implemented. Those experiments often require simultaneous mechanical loading and electrical measurement. [63]. Upcoming section introduces the different techniques utilized for piezoresistivity characterization of SiNWs, detailly.

1.6. Electromechanical Characterization Methods of Piezoresistive SiNWs

Several different methods have been used by different researchers to characterize the piezoresistivity of the silicon nanowires. Depending on the crystallographic orientation of the SiNW, fabrication method, source material specifications for fabrication and application purposes, researchers embrace different test approaches. A cantilever bending type methodology is adopted for bulge testing setups and pressure sensors [7], [25], [63]–[66], while comb-drive MEMS and differential read-out NEMS techniques are adopted to provide CMOS compatibility with MEMS / NEMS world [44], [62], [67]–[69]. On the other hand, four-point bending [24], [45]–[47], [57], [59]–[61], [68], [70], [70]–[75] is the most preferred approach to exert tensile and compressive loads on the specimen. A probe station or wire bonding is required to electrically manipulate the nanowires. As literature survey is conducted, the final method for piezoresistivity characterization is the use of TEM probes for direct tensile and compressive force application [76]–[78]. Detailed silicon nanowire piezoresistivity literature survey is provided in Table 3. Then, each method is described and exemplified.

Table 3: Literature review on the piezoresistivity characterization of SiNWs (T: Tensile, C:Compressive)

Ref	**Output**		**Fabrication Method & Direction**	**Dopant Type and Concentration / Resistivity**	**Test Method**	**Type of Loading**
	GF	**Piezoresistivity Coefficients (Pa^{-1})**				
[59]	up to 5000	-35 to -3.550x10^{-11}	VLS <111>	(p) 0.003-10 Ωcm	4-PB	T, C
[60]	770	N/A	Top-down <110>	(p) 0.4 Ωcm	4-PB	C
[61]	26-2615	1538x10^{-11}	Top-down <100>	(p) Undoped, 20 Ωcm	4-PB	T
[62]	27,3 (calc.)	N/A	VLS <111>	(p)20 Ωcm	MEMS	T

Ref	Output		Fabrication Method & Direction	Dopant Type and Concentration / Resistivity	Test Method	Type of Loading
	GF	**Piezoresistivity Coefficients (Pa^{-1})**				
[45]	1861	N/A	Top-down <110>	(n) $1x10^{18}cm^{-3}$	4-PB	T
[25]	up to 90	$-82x10^{-11}$ $130x10^{-11}$	Top-down <110>	(p) $2x10^{18}cm^{-3}$	Cantilever Bending	T
[64]	up to 5000	N/A	Top-down <110>	(p) 10^{12} ion/cm-^{2}	Cantilever Bending	T
[63]	N/A	up to $188x10^{-11}$	Top-down <110>	(p) 10^{16}-$10^{17}cm^{-3}$	Cantilever Bending	T
[65]	47	$28x10^{-11}$ Pa^{-1}	Top-down <110>	(p) $2x10^{16}cm^{-3}$ (Ga+ implanted)	Cantilever Bending	T
[7]	Only resistance change with respect to tip displacement is provided		Top-down <110>	(p) 10^{14} ion/cm^2	Pressure Sensor	C
[44]	-135 to -145	N/A	Top-down <110>	(n) $5x10^{-4}$ Ωcm	MEMS	T
[67]	-67.1	N/A	VLS <111>	(n) Sample resistance: $5.9x10^{11}\Omega$	MEMS	T
[68]	84 and 53 88 and 68	N/A	Top-down <110>	(p) $1.5x10^{19}cm^{-3}$ $2x10^{20}cm^{-3}$	NEMS 4-PB	T
[57]	-101.5 (calc.) 45 (calc.)	$-601x10^{-12}$ $267x10^{-12}$	Top-down <110>	(p,n) undoped	4-PB	T
[46]	N/A	N/A	Top-down <100> <110>	(p) not provided	4-PB	T
[24]	N/A	$400x10^{-11}$	Top-down <111>	(p) 0.02Ωcm	4-PB	T
[70]	95 88 68	π_{44}=106-118 x (10^{-11}) π_{44}=98-112 x (10^{-11}) π_{44}=76-84 x (10^{-11})	Top-down <110>	(p) $1.5x10^{17}cm^{-3}$ $2x10^{18}cm^{-3}$ $2.2x10^{19}cm^{-3}$	4-PB	T
[72]	65	$38.3x10^{-11}$ (calculated)	Top-down <110>	(p) $1.5x10^{19}cm^{-3}$	4-PB	T

Ref	Output		Fabrication Method & Direction	Dopant Type and Concentration / Resistivity	Test Method	Type of Loading
	GF	**Piezoresistivity Coefficient (Pa^{-1})**				
[73]	-28 32.1	N/A	Thin film <110>	(p,n) not provided	4-PB	T
[77]	-5.9 3.27	$-3.3x10^{-11}$ Pa^{-1} $1.9x10^{-11}$ Pa^{-1}	Top-down <111>	(n) 1-10 Ωcm	STM-TEM	T C
[76]	-11	$-14.4x10^{-11}$ Pa^{-1}	Top-down <110>	(p) 14-22 Ωcm	STM-TEM	T
[78]	-21.6 (calc. -7.8 (calc.)	N/A	Top-down <100>	(p) 14-22 Ωcm	STM-TEM	T C
[34]	N/A	$36.3x10^{-11}$ Pa^{-1} (0.3% strain) $-50.3x10^{-11}$ (1% strain)	VLS <111>	(p) undoped	3-PB	T
[58]	-6±2 -10±3 -30±9	-3±1 x (10^{-11}) -5±2 x (10^{-11}) -16±5 x (10^{-11})	VLS <111>	(n) $2x10^{17}cm^{-3}$ $4x10^{17}cm^{-3}$ $7x10^{20}cm^{-3}$	Squeeze Bending	T
[74]	N/A	$242x10^{-11}$ $115x10^{-11}$ $50x10^{-11}$	Top-down <110>	(p) $1x10^{19}cm^{-3}$	4-PB	T
[69]	3.7 (calc.) 2 (calc.)	$-3.7x10^{-11}$ $-2.1x10^{-11}$	VLS <111>	(n) not provided	MEMS	T
[66]	82 (calc.)	$48x10^{-11}$	Top-down <110>	(p) $5x10^{19}cm^{-3}$	Cantil. Bending	T
[75]	490(calc.)	$2.9x10^{-9}$	Top-down <110>	(p) $10^{15}cm^{-3}$	4-PB	C
[79]	150 (nw) 99 (bulk)	$86.52x10^{-11}$ $57.97x10^{-11}$	Top-down <110>	(p) $3.2x10^{18}cm^{-3}$	4-PB	C
[47]	235 95 65	N/A	Top-down <110>	(p) $5x10^{17}cm^{-3}$ $1x10^{19}cm^{-3}$ $2x10^{20}cm^{-3}$	4-PB	C

1.6.1. Cantilever Bending

Cantilever beam method is commonly used to electromechanically characterize the silicon nanowires. The silicon nanowires are structured in two ways: 1-) fabricated in an embedded fashion in the cantilever beam by means of a series of fabrication steps, 2-) fabricated on the top of the cantilever beam as silicon nanowire is suspended with free surface. The test can be

conducted in a TEM, probe station or an outer environment, depending on the purpose. Ideally, one end of the cantilever beam is fixed while the other one is free to directional moves. Tensile / compressive load is transduced from the load application on the free end of the cantilever. The electrical measurements can be conducted with a probe station needle or a more complex electrical circuitry. The amount of free end displacement of the cantilever beam or applied load should be measured to reach an approximate engineering stress and/or strain value exerted on the SiNW so that piezoresistivity coefficient and gauge factor calculation shall be achievable.

[25] reported their experiments based on a cantilever beam setup (Figure 7) to evaluate the piezoresistivity in single crystalline silicon nanowire, they used top-down approach to fabricate SiNWs along <100> and <110> directions from a 50nm device layer SOI wafer. Each array consists of 15 identical SiNWs connected in parallel and aligned with longitudinal or transverse axes of the cantilever. Doping density is chosen as $1.2\text{x}10^{18}$ cm^{-3}. Piezoresistive coefficient, π_l, is driven by using the equation (1.8). Resistance change ($\frac{\Delta R}{R}$) is obtained through experiments. σ_l, longitudinal stress, established on the surface of the cantilever beam is calculated with the equation (1.9), where F is the applied force, L is the length, b is the width and h is the thickness of the cantilever silicon strip.

$$\frac{\Delta R}{R} \cong \pi_l \sigma_l \tag{1.8}$$

$$\sigma_l = \frac{6FL}{bh^2} \tag{1.9}$$

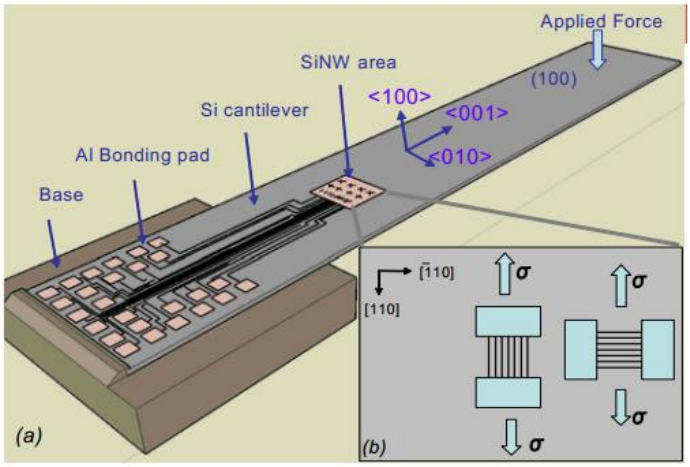


Figure 7: (a) Cantilever beam bending setup, (b) SiNW array pattern. Taken from [25].

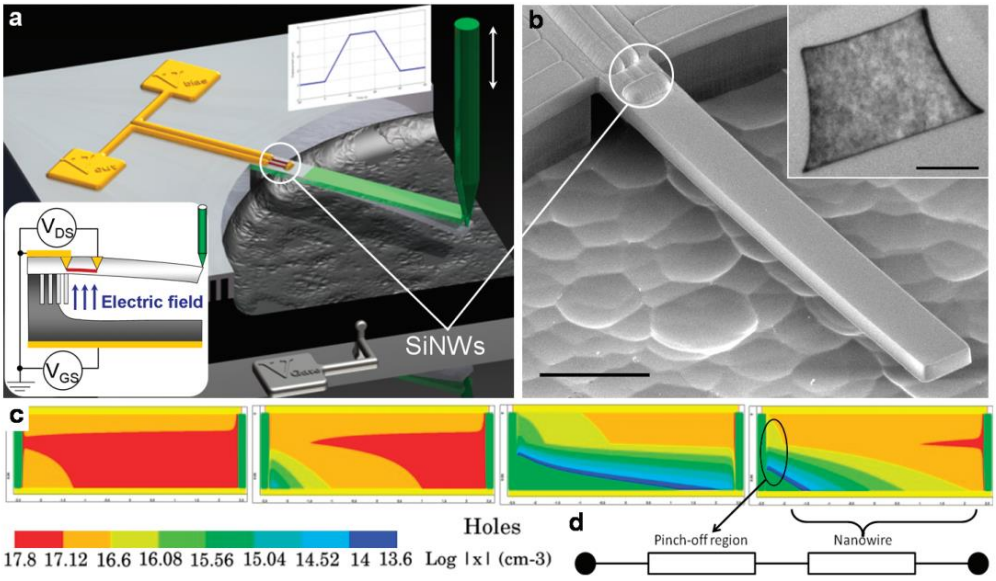


Figure 8: (a) Schematic of the cantilever test setup. Red nanowire is embedded in the cantilever, (b) SEM micrograph of the cantilever mechanism. Taken from [64].

A specific in-situ bending setup is provided in [64] (Figure 8). They aimed to combine electrical biasing with applied load to enhance charge carriers' concentration. By this method up to 5000-gauge factor is achieved. They fabricated the nanowires embedded in SiO_2 cantilevers to eliminate AFM induced surface property modification. Specific stress profiles were induced in the SiNWs by loading the free end of the cantilever with a nanoindentation tip. SiNWs are doped by ion implantation of BF_2^+ at $1x10^{12}$ ion/cm^2. All measurements are

conducted at 24ºC in darkness. They reveal that the nanowire response is dominated at elevated bias by the carrier depletion while smaller bias provided expected standard gauge factor values. Gauge factor as a function of electrical biasing is given in Figure 9.

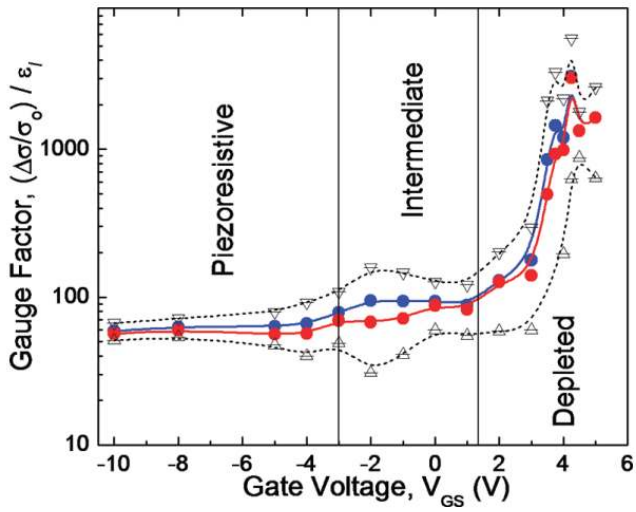


Figure 9: Gauge factor as a function of electrical biasing. Taken from [64]

[63] fabricated the piezoresistive SiNWs in wafers and diced them to cantilever type beams. The samples are tested in a conventional probe station with the help of a manual translation stage. One end is fixed, and the other end is subjected to bending while electrical measurements are taken via a parameter analyzer. Their cantilever beams are 40mm x 15 mm x 0.525 mm in size while the SiNWs are in <110> direction, 100nm wide, 340nm thick with different lengths (8, 28, 48µm). SiNWs are p-type with a concentration of 10^{16}-10^{17}cm^{-3}. The piezoresistivity coefficient is extracted after the experiments and they found that longitudinal piezoresistivity coefficient increases significantly when the NW gets shorter. The maximum π coefficient they extract is 188x10^{-11} Pa^{-1} for the 8 µm-length SiNW. Multiplying the "π" with 169 GPa Young's modulus (Y) in line with the equation $GF = \pi \, x \, Y$, gauge factor can be calculated as 317 which is slightly higher than the literature survey findings.

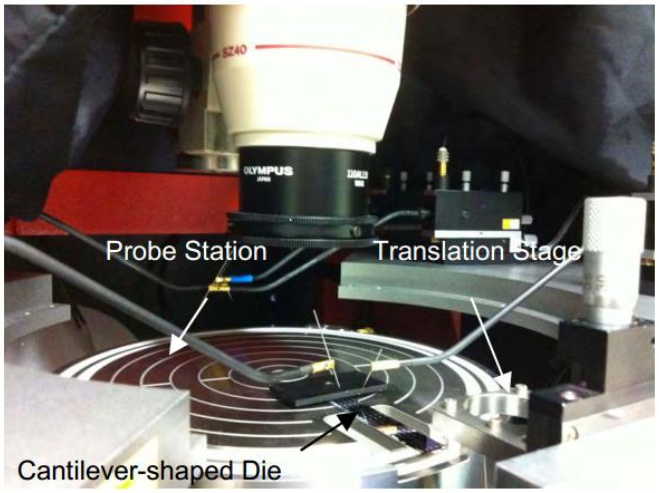


Figure 10: Cantilever type measurement setup in probe station. Taken from [63]

Another study that utilizes cantilever beam bending method (Figure 10) to characterize piezoresistive SiNWs is reported in [65]. SiNWs are fabricated and tested in a 200µm x 3mm x 20mm silicon strip. One end is clamped, and the other end is subjected to the bending load. Since the thickness of SiNWs (200nm) are smaller in orders of magnitude compared to the silicon strip thickness (200µm), they assume the stress is equal to the stress on the top surface of the bended silicon strip. Their sample SiNWs are p-type and fabricated based on top-down approach by using FIB and wet etching processes. Calculated gauge factor upon their experiments is approximately 45.

1.6.2. Pressure Sensors

The SiNWs are crucial elements for new generation pressure sensors. Pressure sensors can be adopted as bulge test setups to electromechanically characterize SiNWs. The test mechanism naturally behaves like a cantilever system so that applied central diaphragm displacement will be transferred as an induced strain to the SiNWs. As the test setup can be utilized for piezoresistivity characterization, it can also be benefitted as a mechanical test setup for fatigue testing of the SiNWs. [7] uses such a setup (Figure 11) to investigate fatigue of the piezoresistive SiNWs for commercialization potential of pressure sensors. They successfully applied large compressive engineering strain up to 1.7% to the top-down fabricated p-type SiNW by utilizing the SiN_x film with high fracture stress. The SiNWs are

embedded in SiNx thin films. The experiments are conducted on a probe station platform. Almost 20% change in resistance is achieved through experiments (Figure 11).

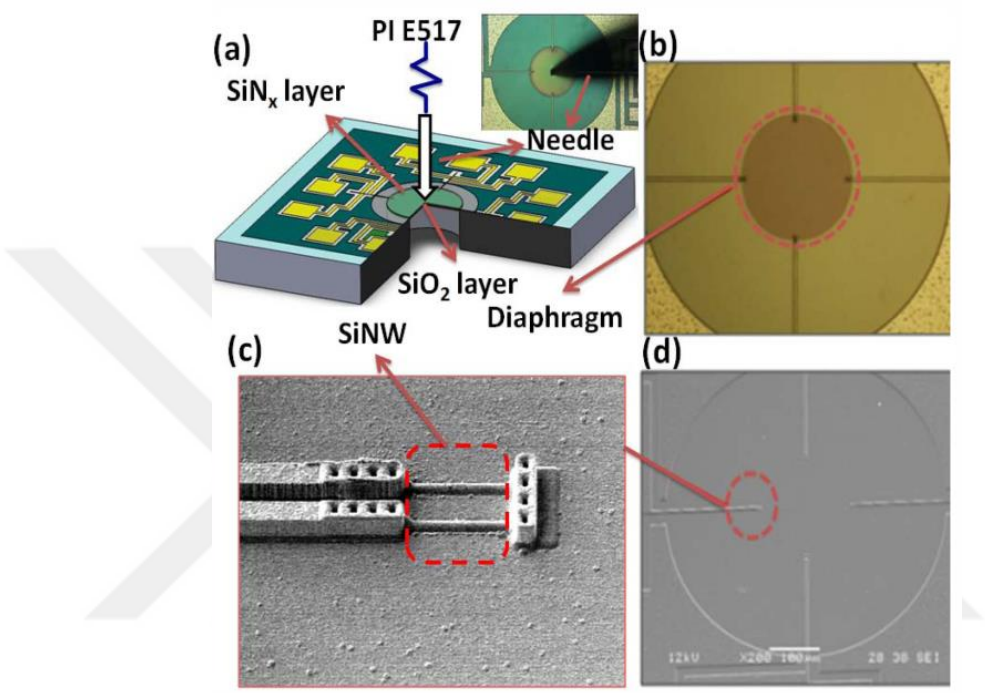


Figure 11: (a) Pressure sensor scheme, (b) under optical microscope, (c) SiNW, (d) SEM micrograph of whole device. Taken from [7].

1.6.3. MEMS & NEMS

For both bottom-up and top-down fabricated silicon nanowires, using a MEMS or NEMS based test setup is applicable. Integration and sample alignment are the crucial factors that will lead a test to catastrophe or success. In that manner, selecting an appropriate facet and synthesizing the SiNWs on the test setup is the mostly preferred option for bottom-up grown nanowires. On the contrary, top-down SiNWs are fabricated monolithically together with the test setup from a suitable wafer, preferably SOI.

[62] utilizes a simple MEMS device to mechanically load the SiNW and measure the electrical response (Figure 12). MEMS section is fabricated via top-down methods. Then the appropriate facet is selected as the basis for the bottom-up nanowire. The SiNW is monolithically grown between a fixed and a moveable end on <111> direction on the test

setup. The mechanical load is exerted via an external probe to the moving end shown in Figure 12, which enables engineering strain up to 3.5%. Two additional probes are placed at two end anchors to apply the potential difference. They measured and monitored the current response simultaneously.

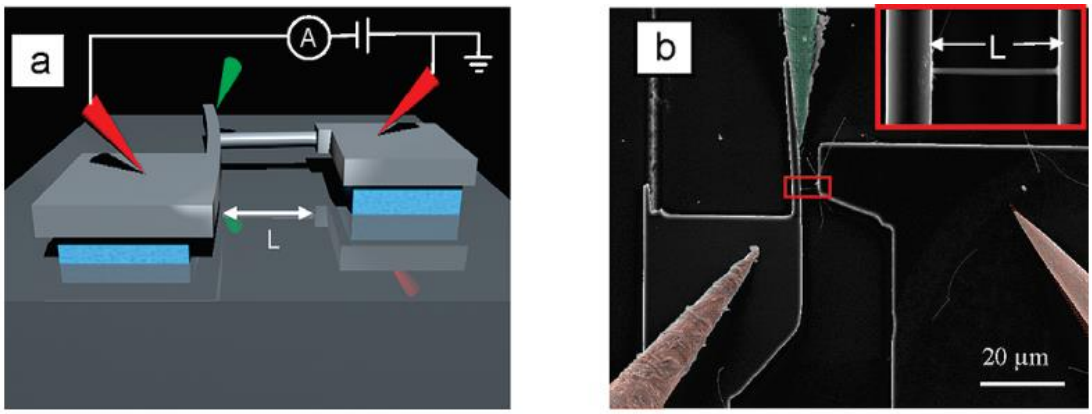


Figure 12: a) Schematic demonstration of the MEMS test setup, b) SEM micrograph of the top-view of test system with electrical measurement probes. Taken from [62].

While [62] preferred a simple design for their test system, [67] and [44] adopted a more complex MEMS mechanism to apply force and measure the response. [67] utilized a complete comb-drive mechanism as actuator and a differential tri-plate measurement scheme to sense the uniaxial force acting on the SiNW. Electrical insulation cuts are implemented to provide electrical isolation between moving MEMS shuttle and SiNW. Both actuation and force sensing is achieved via electrostatic principles. SiNWs are fabricated along <111> direction via VLS method. Then a nano-manipulated pick-and-place procedure is developed to place the nanowire onto MEMS test setup. They conducted in-situ tests under SEM while SEM e-beam is on and off to investigate the effect of SEM imaging. It is observed that due to charge occurred on the nanowire while SEM e-beam is on, I-V characteristics changed.

Zhang utilizes a capacitively exerted MEMS device to apply electrical and mechanical testing on SiNWs [67]. Unlike [44], the SiNWs are not fabricated top-down but synthesized along <111> direction. A nanomanipulation procedure is developed to carry and place the SiNWs

onto (Figure 13) MEMS based test setup. There is already an actuator and force sensor fabricated in the setup so that they do not utilize image processing for characterization. They perform the tests under SEM with e-beam on and off to quantify the effect of SEM imaging irradiation during tests. It is concluded that due to trap charge occurred in the specimen, e-beam changes the I-V characterization of the sample.

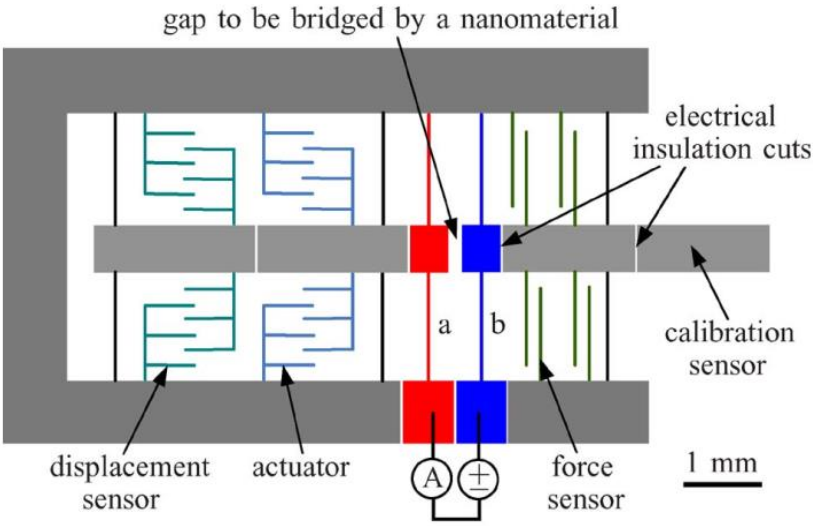


Figure 13: MEMS setup for electromechanical characterization of SiNWs. Taken from [67].

[44] benefits a similar methodology with exceptions. They utilized a fabrication process flow which previously achieved top-down monolithic integration of a SiNW and 10μm-thick MEMS scale building blocks. The process was developed by the same group, as well. Therefore, an additional pick-and-place procedure to locate the SiNW is not necessary. In addition, alignment along uniaxial loading direction between MEMS and SiNW is secured, as whole test setup including the nanowire is defined through a set of e-beam lithography steps (Figure 14). Except from Zhang, Esfahani utilizes additional double folded springs to amplify the SiNW engineering strain.

The tests are conducted under the probe station and nanowire engineering strain is obtained through a set of simulations. The SiNWs are highly n-doped with a resistivity of $5x10^{-4}$ Ω cm. They report -135-to -145-gauge factor as the piezoresistivity characterization of their top-down fabricated nanowires.

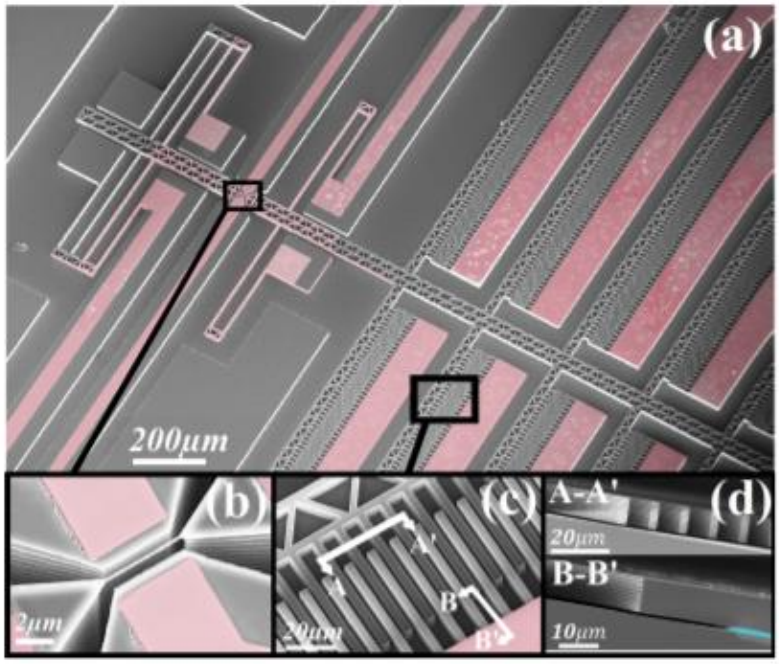


Figure 14: SEM micrograph of MEMS tensile testing setup, (a) MEMS actuator, amplifier springs and SiNW, (b) close view of SiNW, (c) MEMS actuator, (d) comb-finger cross-section. Taken from [44].

There is another innovative method used for piezoresistivity characterization. Fundamentally, this method resembles to the well-known DETF (Double-Ended Tunable Fork) sensing mechanism. The inertial sensing company EMCORE manufactures their commercial tactical grade quartz accelerometers based on this principle. There is a pendulous mass connected to a hinge at one end while the other end is connected a double ended fork structure. On both sides of the fork there are micro beams which can resonate on a particular frequency. As the acceleration acts on the pendulous mass, micro beam on one side is compressed while the other beam on the other side is under tensile effect. Due to the geometrical variation, the resonance frequency of the beams change. Hence, differential reading is performed through capacitive transduction.

The piezoresistivity characterization method reported in [68] is utilizes a similar structure but on the NEMS level. A crossbeam structure is designed as in Figure 15. Unlike EMCORE, they utilize the piezoresistive response of the SiNWs to detect beam deflection. As benefiting the top-down fabrication advantages, and piezoresistivity, this mechanism can be adopted

to the open-loop inertial navigation sensors for future use after full electromechanical characterization is performed. [68] reports that they fabricated the p-type SiNWs along <110> direction monolithically with a dopant concentration of 10^{19} cm^{-3}. The lever arm between the SiNWs is subjected to electrostatic actuation so that tensile / compressive uniaxial force is generated on the SiNWs (Figure 15). SiNW resistance change is monitored, accordingly. They utilize analytical models and simulations to calculate stress induce on the nanowires and then gauge factor is extracted. Since this new measurement technique is proposed by their institution CEA-LETI, they also performed conventional four-point bending test to compare their findings. Gauge factor of the single crystalline SiNWs tested via new method is 84±2 (STD), 85±6 (STD) and 88±4 (STD) while four-point bending results show 88±4 (standard deviation), which are in close proximity.

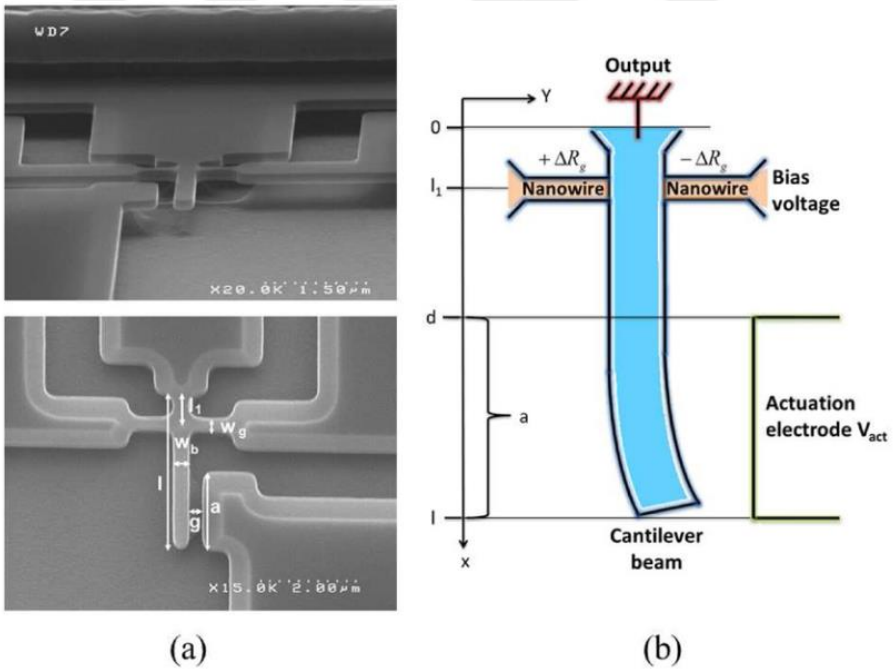


Figure 15: (a) SEM micrographs of crossbeam NEMS structure, (b) Schematic of the proposed crossbeam beam structure. Taken from [68].

1.6.4. Four-Point Bending

Four-point bending is the most common approach to characterize electrical behavior of piezoresistive SiNWs. This technique requires an external device design consisting of four

pins. The sample is placed on two supporting pins. Then the loading pins are set to an equal distance from the center. One side is fixed so that the plate having the other two pins start bending the sample. As the main advantage, compared to the three-point bending, no shear force is generated in the area between inner pins on the sample. As being relatively insensitive to geometrical misalignments, this technique provides a uniform stress along the beam between the pins. Applied stress is described by the sample geometry, the support and load positions, and the magnitude of the applied load [46]. Many researchers use this approach due to its ease of application. Almost all samples can be subjected to this test if a suitable setup is designed. To extract engineering stress/strain different tools are utilized, such as controlled stage actuators, force sensors, laser deflection systems and digital image correlation. Bigger samples can directly be experimented while smaller chips need an additional strip material to be glued on. Using an adhesive material brings extra challenges in qualitative measurement. Therefore, several various methods are embraced to reach more accurate results which can be listed as; 1-) quantifying the adhesive materials with additional mechanical tests [72] such as peel-off tests, 2-) using additional equipment such as laser-deflection setup to measure sample curvature [73] and 3-) using additional strain gauges [72]. In Chapter 3 of this thesis, we described "indirect bending" version with the use of a glue on the test setup and direct bending of the test chips. The effective gauge factor variation is clearly demonstrated for vertically stacked SiNWs.

[57] used four-point bending (Figure 16) approach at room temperature to analyze piezoresistivity coefficient change from wide SOI down to undoped <110> oriented nanowire transistors (NMOS and PMOS). The uniaxial tensile stress calculation formula in the provided in Figure 16 as, well. They report that there is straightforward evidence for the variation of the coefficients as the width shrinks down to nanowire scale for both NMOS and PMOS.

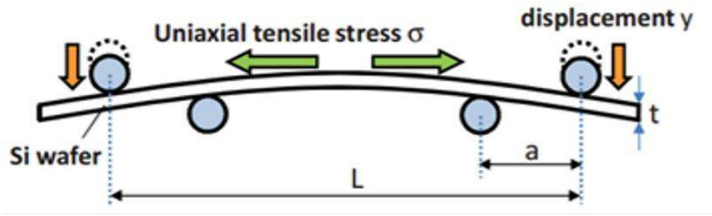


Figure 16: Four-point bending setup schematic used to apply calibrated tensile stress. In the formula, "σ" is the uniaxial tensile stress, "y" is the vertical displacement of moving bar, "t" is the Si wafer thickness, "a" is the distance between a fixed and moving bar and "L" is the distance between two outer moving bars. Taken from [57].

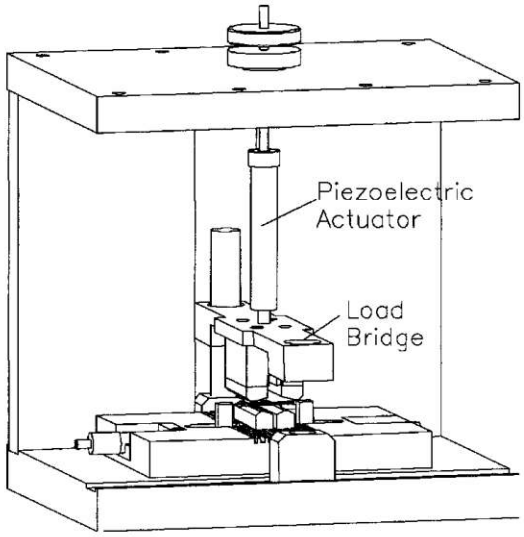


Figure 17: CAD drawing of the experimental setup used in [46]. Taken from [46].

Lund [46] describes a more comprehensive experimental four-point bending setup for their study (Figure 17). The main material for their setup is aluminum as it provides light weight and low thermal expansion coefficient. The pins are manufactured from stainless steel. They used a piezoelectric actuator to accurately control the amount of applied cycling load, as well. The applied stress is calculated via stress formula. Their main objective is to obtain piezoresistivity coefficients semiconductors including p-type silicon for different temperatures. Therefore, the tests are conducted in a closed and temperature-controlled chamber.

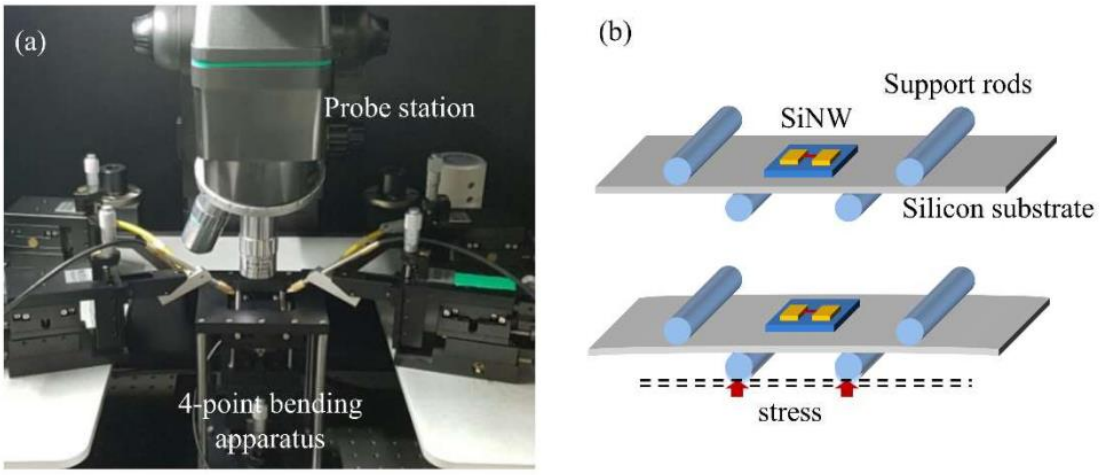


Figure 18: (a) four-point bending setup to electrically characterize SiNWs, (b) representative four-point bending scheme. Taken from [24].

Jang [24] reports using a four-point bending setup to support their model-based studies on the piezoresistivity of SiNWs. experiments are performed in a dark box to remove photo-induced effects in SiNWs. This effect is also observed in our studies and detailed in the Chapter 2 of this thesis. SiNWs are fabricated on a (111)-oriented, p-type, 0.02Ωcm SOI wafer with top-down approach. A manual Z-axis actuation stage and a load sensor is implemented in the test setup to calculate applied stress on the specimen (Figure 18). Their results for 100x100nm to 500x500 cross-sectioned nanowires indicate that piezoresistivity coefficient converges to approximately $400x10^{-11}$ Pa^{-1} for a maximum applied stress of 30 MPa.

On the other hand, Richter [70] reports that they assembled a high precision four-point bending setup designed and calibrated for obtaining piezoresistivity coefficients at various temperatures ranging from 30C to 80C. There is a closed chamber with controlled temperature via thermocouples. A motorized stepper actuator and a dedicated force sensor is included in the test setup to exert well-controlled loads onto the sample (Figure 19). Formula available above is utilized to extract applied stress. Their samples are fabricated in long silicon strips to apply the bending test directly without use of an additional material. SiNWs are <110> oriented, p-type and doped with different concentrations of $1.5x10^{17}$ cm^{-3}, $2x10^{18}$ cm^{-3}, and $2.2x10^{19}$ cm^{-3}. They found relatively low π44 as $106\text{-}118x10^{-11}$ Pa^{-1} for $1.5x10^{17}$

cm^{-3}, 98-112x10^{-11} Pa^{-1} for 2x10^{18} cm^{-3}, and 76-84x10^{-11} Pa^{-1} for 2.2x10^{19} cm^{-3} doped nanowire. This corresponds to approximately 47.3, 45.2 and 34.8 as gauge factors.

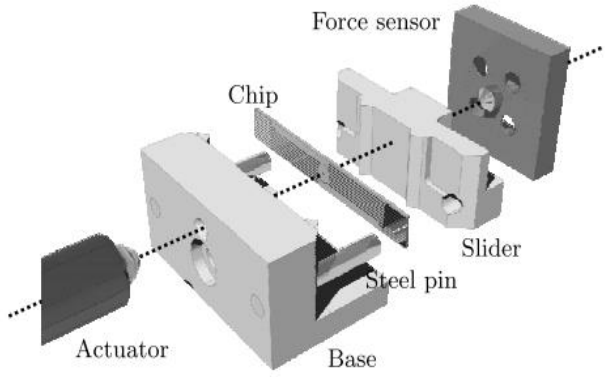


Figure 19: Four-point bending setup exploded view and bending simulation for the sample. Taken from [70].

Giant piezoresistive effect, (1861 as gauge factor) in n-type silicon nanowire field-effect transistors (SiNWFET) is studied and reported in [45] as introduced previously. The mechanical stress is induced along <110> direction via a simple four-point bending test. I-V measurements are conducted for strained and unstrained samples (Figure 20). The magnitude of the tensile engineering strain is determined by a strain gauge mounted on the SOI wafer strip.

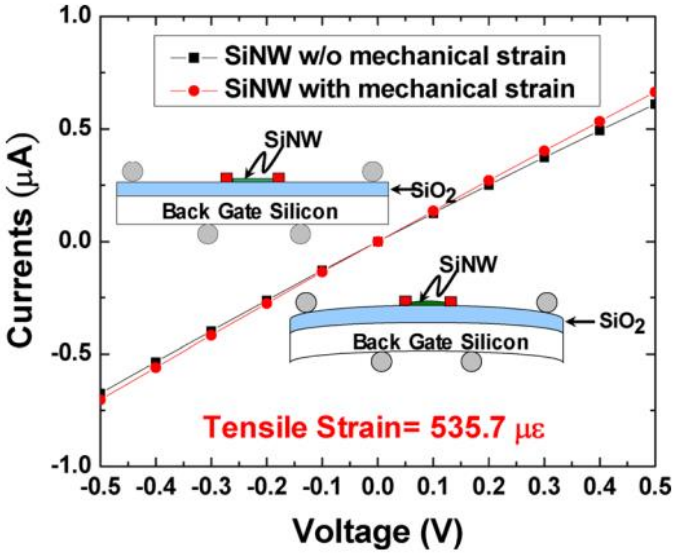


Figure 20: I-V measurements for unstrained and strained n-type SiNWs, 4P bending test. Taken from [45].

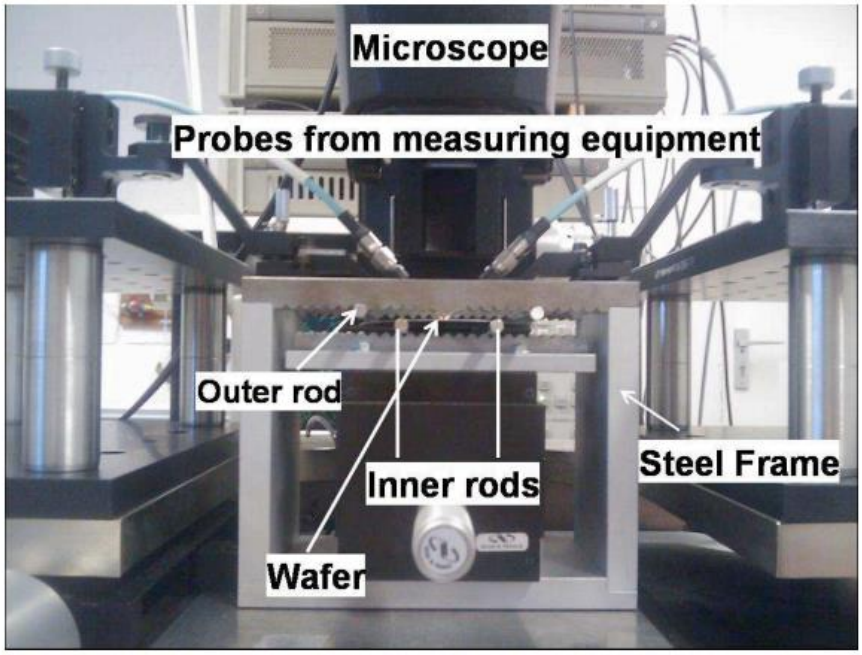


Figure 21: Image of four-point bending fixture. Taken from [61].

Another giant piezoresistivity study is provided by [61]. Silicon nanowires are fabricated in <100> direction with dimension 25-50-75-100nm in width, 300-600-900-1200nm in length. p-type and undoped (20Ωcm) SOI wafer having 50nm device layer thickness is utilized. No additional doping procedure is followed. Depending on the back-gate voltage, reported gauge factor ranges from 26 to 2615. The mechanical excitation is carried via four-point bending fixture with a manual Z-axis stage in a probe station which is used for electrical measurements (Figure 21). They designed the setup such that compressive and tensile loads can be exerted by just adjusting the cylindrical rod positions. The tests are carried out on wafer scale requiring for no dicing.

Bosseboeuf [72] of CEA-LETI introduced relatively expensive and complex setup to realize thermal and electromechanical characterization of top-down fabricated p-type silicon nanowires. The samples are highly doped with boron (1.5×10^{19} cm^{-3}). The nanowires are 80-260 nm in width, 160 nm in thickness and 2.5-5.2 µm in length. These samples are located on (100) silicon dies having dimensions of 20mm x 20mm x 725 µm indicating that no glue is used, and the die is directly subjected to bending. Four-point bending procedure is applied

in a cryogenic probe station to perform thermal and electrical characterization (Figure 22). The setup includes piezoelectric actuator with an embedded strain sensor enabling dynamic

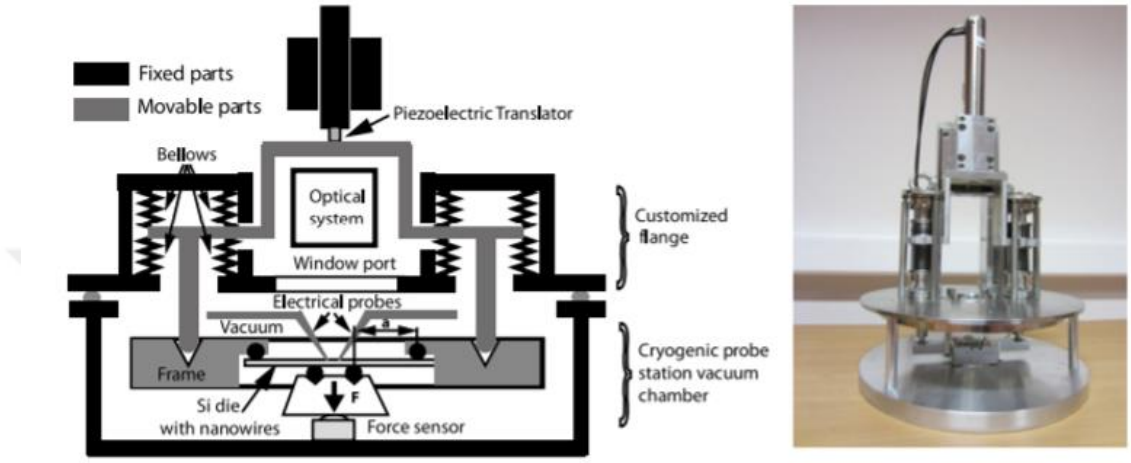


Figure 22: Four-point bending test setup in cryogenic probe station. Taken from [72].

loading opportunity, as the setup is vacuumed to prevent humidity interference on the nanowire resistance. A force sensor is utilized as well to evaluate the applied stress on the sample. The stress value and test results ($\Delta R/R$) are then used to extract piezoresistive coefficient.

The following criteria should be considered for a successful and high-quality measurement as stated in [72]:

(I) Preferably engineering stress/strain should be directly applied to the nanowires. There are works based on application of the load on the samples which are glued to another longer strip. Such case can be named as "indirect bending" and the result quality is highly dependent on the mechanical properties of the glue used as intermediate layer. Even the layer thickness and homogeneity of the adhesive are utmost importance. Therefore, a reference measurement device / method (e.g., an additional strain gauge) can be utilized to support the test metrology.

(II) Designed test setup should be able to provide controlled environment temperature to reach temperature dependent piezoresistance.

(III) Experiments should be conducted in vacuum to prevent humidity or other absorbable particles change the nanowire resistance.

Regarding above criteria, (I) is crucial to follow. As detailed in Chapter 2 and 3 of this dissertation, tested SOI chips are 10mm x 10mm x 726 µm and 12mm x 12mm x 500µm. Comparing with the other studies including long silicon strips utilizing a direct bending methodology, it is challenging to manufacture a four-point bending setup for our samples. Therefore, we initially used an epoxy-based glue as the adhesive layer which brings another challenge for data evaluation. This phenomenon is encountered in [73], as well. Their report is based on a study of the piezoresistivity of doped nanocrystalline silicon thin films. They report gauge factor values as the piezoresistivity characteristics of their samples based on a four-point bending approach (Figure 23). Their samples are glued with an epoxy resin adhesive to a silicon strip, so that bending stress is applied indirectly to the sample.

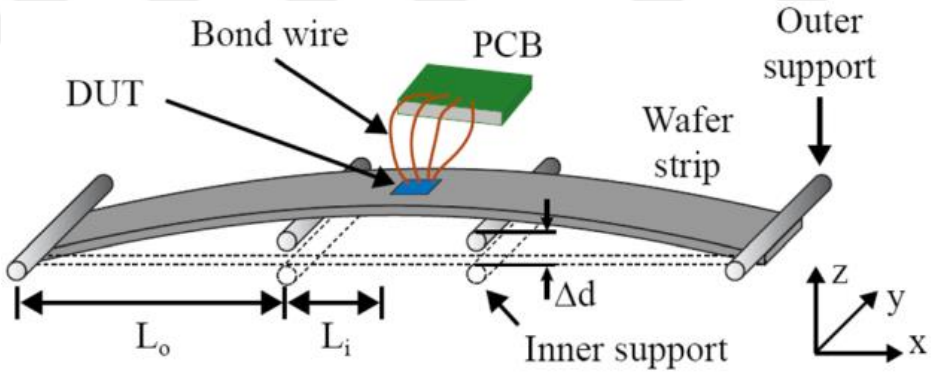


Figure 23: Four-point bending setup taken from [73].

To extract a numerical value for glue effect, C_{glue} constant is defined as a correction factor in strain formulation [73]. The formula is provided as

$$\varepsilon_1 = \frac{3L_0 C_{glue}}{E_{110} w t^2} F \tag{1.10}$$

In the equation (1.10), L_0 is the length of the silicon strip, E_{110}, is the modulus of elasticity on <110> direction. w is the width and t is the thickness of the silicon strip, F is the applied

force on the strip. Eq (1.10) notes that C_{glue} is an important and direct factor affecting the engineering strain induced on the specimen. A laser-deflection equipment is used to evaluate specimen curvature and finite element simulations are carried out accordingly. Consequently, they value C_{glue} as 0.2273 which means obtained engineering strain is almost 4.5 times smaller than the expected engineering strain. Depending on the epoxy type, curing temperature, surface quality and adhesive thickness, this correction factor can vary.

1.6.5. STM-TEM

In TEM (Transmission Electron Microscopy) applying a direct tensile / compressive load is possible, as well. The force is directly exerted through an STM-TEM (Scanning Tunnelling Microscope – Transmission Electron Microscope) holder having a tungsten probe at the tip. Probe is used for both force application and conducting electrical measurements. During the deformation, the I-V curves are recorded simultaneously. The physical contact between sample and probe is achieved via EBID (Electron Beam-Induced Deposition) (Figure 24).

Three reports from the same group are published using this technique [76]–[78]. The tested silicon nanowires in this group are fabricated via a specific FIB procedure, as each report provides results for nanowires having different direction. [77] achieves 3% tensile and 8% compressive engineering strain on n-type and <111> silicon nanowires with this method. The starting wafer has a resistivity of 1-10Ωcm, and additional doping is not realized. Gauge factor of the nanowires are calculated as -5.59 for tensile and 3.27 for compressive test. [76] and [78] electromechanically characterize two SiNW sets which are both p-type but differ in direction: <110>, and <100> respectively. All samples are prepared from a wafer having resistivity of 14-22 Ωcm via FIB. The gauge factors in tensile region are reported as -11 for <110> SiNWs [76] and ~180 for <100> [78], while compressive gauge factor is declared as ~32 for <100> [78].

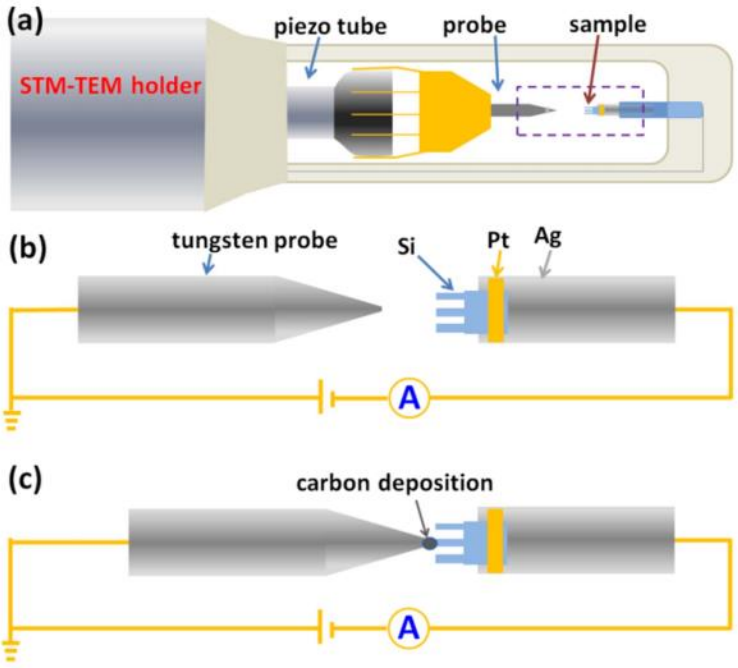


Figure 24: (a) STM-TEM holder and experimental setup, (b) Probe and sample closer view, not to scale, (c) bond and contact between probe and SiNW. Taken from [77].

1.6.6. Three-Point Bending

Three-point bending is the last method which is less used to characterize piezoresistive response of a silicon nanowire compared to four-point bending. Winkler [34] uses this method to characterize VLS grown silicon nanowires on <111> direction (Figure 25). The samples are monolithically synthesized between two silicon anchors to eliminate positioning and welding related problems which is conventionally known as "pick and place" [80]. The test chip is glued on a steel plate, which will eventually cause loss of engineering strain. Three-point bending test is conducted on three types of samples: (i) "as grown" samples which are directly tested after VLS process, (ii) after removal of gold residuals with Aqua Regia and BHF and (iii) thermally coated. Variations in conductance of these materials are reported, accordingly. Due to use of an adhesive layer, to ensure engineering strain exerted on the sample, they utilize confocal μ-Raman spectroscopy.

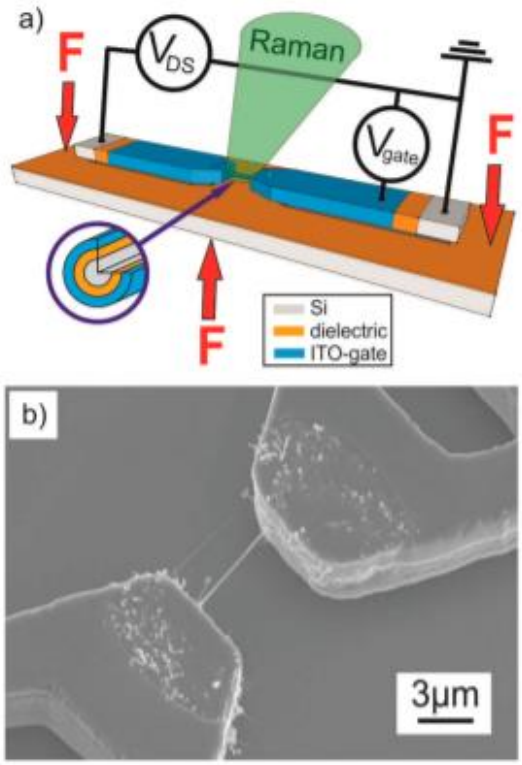


Figure 25: (a) three-point bending setup schematic, (b) monolithically integrated VLS grown SiNW which is subjected to three-point bending. Taken from [34].

After all, the methodologies preferred in characterization of piezoresistive SiNWs depends on application of a tensile or compressive load and design of the test sample/chip. As there are diverse types of methods, four-point bending is the most preferred test method. This approach provides advantages over other methods such as ease of application, no necessity of having costly equipment (e.g., TEM), no necessity on designing a complex MEMS test device, insensitivity to small misalignment errors and being able to provide design options on test variables (e.g., temperature dependency). However, there are drawbacks in four-point bending test, as well. If a researcher utilizes adhesives to interconnect test chip and a long strip, he/she will face inevitable challenges on the measurement quality. Type of the adhesive (due to its mechanical properties) adhesive thickness, homogeneity, and surface quality play key role on the success of the test. The repeatability of the tests is also questionable. Therefore, various additional measurement devices are introduced in test setups such as strain gauges, laser-deflection measurement systems and Raman-spectroscopy.

In this thesis, Chapter 2 describes the electrical measurements conducted on the n-doped ($2x10^{20}$ cm^{-3}), <110>, suspended single silicon nanowires. I-V characteristics are presented for different widths and lengths. Photo-induced effects on the measurements due to the silicon membrane remnants are studied, as well.

In Chapter 3, vertically stacked silicon nanowire arrays which are n-doped ($2x10^{20}$ cm^{-3}) and fabricated along <110> crystallographic orientation, are experimentally tested for their piezoresistivity characterization. Two different approaches are evaluated and compared for four-point bending test: 1-) indirect bending as an epoxy layer is present in the system, and 2-) direct bending. Our samples are prepared on 10mmx10mm SOI chips. We glued the chips to a silicon strip to test them in a four-point bending setup and exert the loading force accordingly. I-V measurements are realized via Agilent B1500A Semiconductor Parameter Analyzer in a dark probe station box to eliminate photo-induced effects on SiNWs. Probe needles are utilized for the electrical connection so that no PCB (Printed Circuit Board) and wirebonding is included on the test setup. Optical camera shots are taken for each measurement to conduct DIC (Digital Image Correlation) analysis on the engineering strain levels. Then, another four-point bending setup is designed and manufactured specialized for 10mmx10mm SOI chips. The device is manufactured with CNC machining. Direct bending tests are performed on the chips to compare the results with glued samples. The results yield that almost four times difference is obtained in gauge factors if no additional technique is used to measure engineering strain on glued samples.

Chapter 2

Fabrication/Electrical Characterization of Doped & Single SiNWs

2.1. Fabrication Process Flow

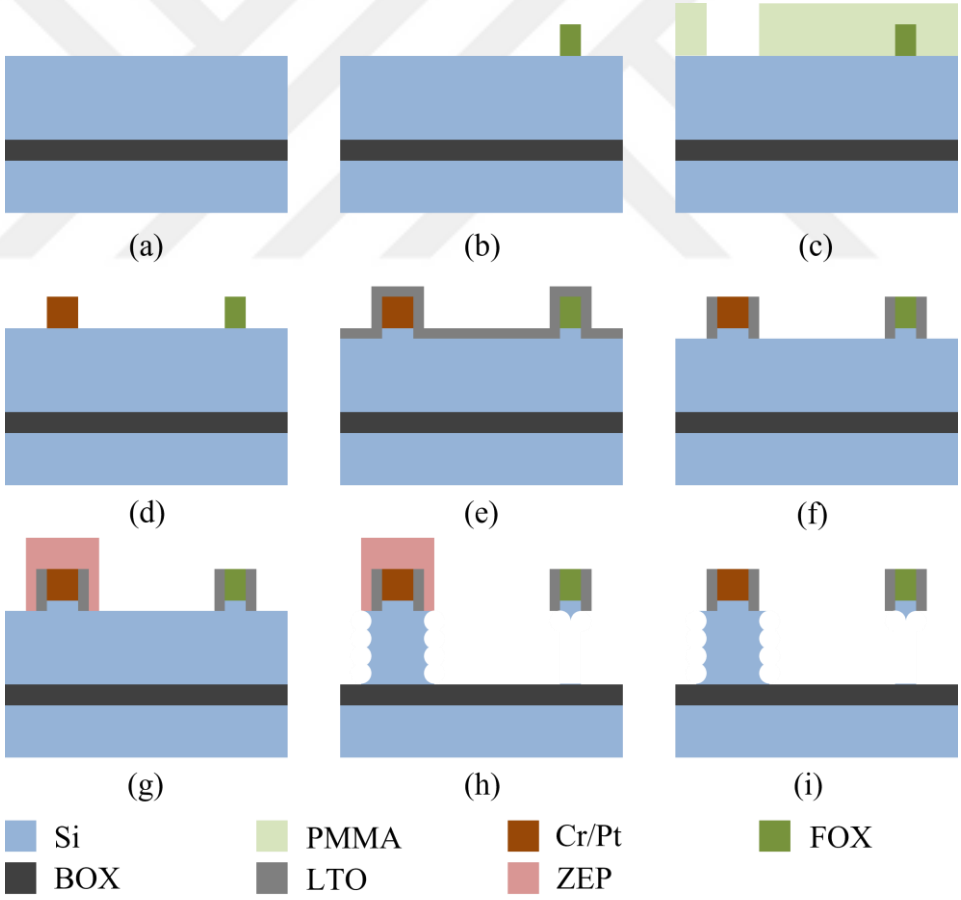


Figure 26: Single piezoresistive silicon nanowire fabrication flow on 10µm device layer SOI: a) n^{++} doping, b) e-beam lithography on FOX16, c) coating and e-beam patterning of double PMMA layers, d) Cr/Pt deposition and lift-off, e) RIE etching of Si and LTO coating, f) directional etching of LTO, g) Dicing, coating and patterning of ZEP520A 100%, h) BOSCH Process on Si, and i) Removal of ZEP520A 100% and other residuals with O_2 plasma.

A <100> SOI wafer having 4-inch diameter, with a Si device layer thickness of 10 µm, a BOX (Buried Oxide) layer thickness of 1 µm and a Si handle layer thickness of 380 µm is used as the starting element. 10 µm as Si device layer thickness is selected due to the previous successful etch depth results for Si nanowire surrounded by bulk Si [31].

The fabrication procedure is presented and summarized in Figure 26. The fabrication starts with an initially cleaned SOI wafer. Then, SOI wafer is subjected to extremely high n-type (Phosphorus) doping. Annealing treatment is applied for doping uniformity as well. Doping level is set to be almost $2x10^{20}$ cm^{-3} which will be the maximum value that CMi facilities can provide. The fabrication proceeds with the exposure of the SiNW with 600-nm-thick FOX16. It is a negative-tone and high-resolution e-beam resist. Proposed dose for 600nm thickness is 5000 µC/cm2 with an accelerating voltage of 100 keV due to characterization studies [Mustafa Thesis]. After exposure, 2 minutes of resist development in %25 TMAH solution is followed. Metal touchpad and signal lines are patterned by the metallization through lift-off of Cr/Pt lines. To achieve that a bilayer lift-off mask including e-beam resist PMMA (poly methyl methacrylate) 495K A8 (400nm thickness) and PMMA 950K A4 (150nm thickness) is patterned. 5-nm Cr and 50nm-Pt metal coating is achieved through e-beam evaporation with a deposition rate of 4 Angstrom/s. Lift-off is completed after resist removal in a 24-hour acetone bath along with the help of sonification. Figure 27 provides representative Cr-Pt signal lines and toucpads, and device distribution in chip-scale.

Using FOX16 as the mask, a shallow-RIE Si etch is performed to a depth of around 130nm for 30 seconds with Cl_2 chemistry in STS Multiplex ICP dry etcher. The recipe is already developed by the CMi stuff and adjusted for the project needs. The process is performed at 20ºC with a 5-mTorr chamber pressure and a flow rate of 50 sccm. Since this process also etches FOX16, at the end of this step, the FOX16 thickness is reduced to around 100nm. Remaining ~100nm FOX16 will be needed as the mask material to perform 10µm deep Si etch process.

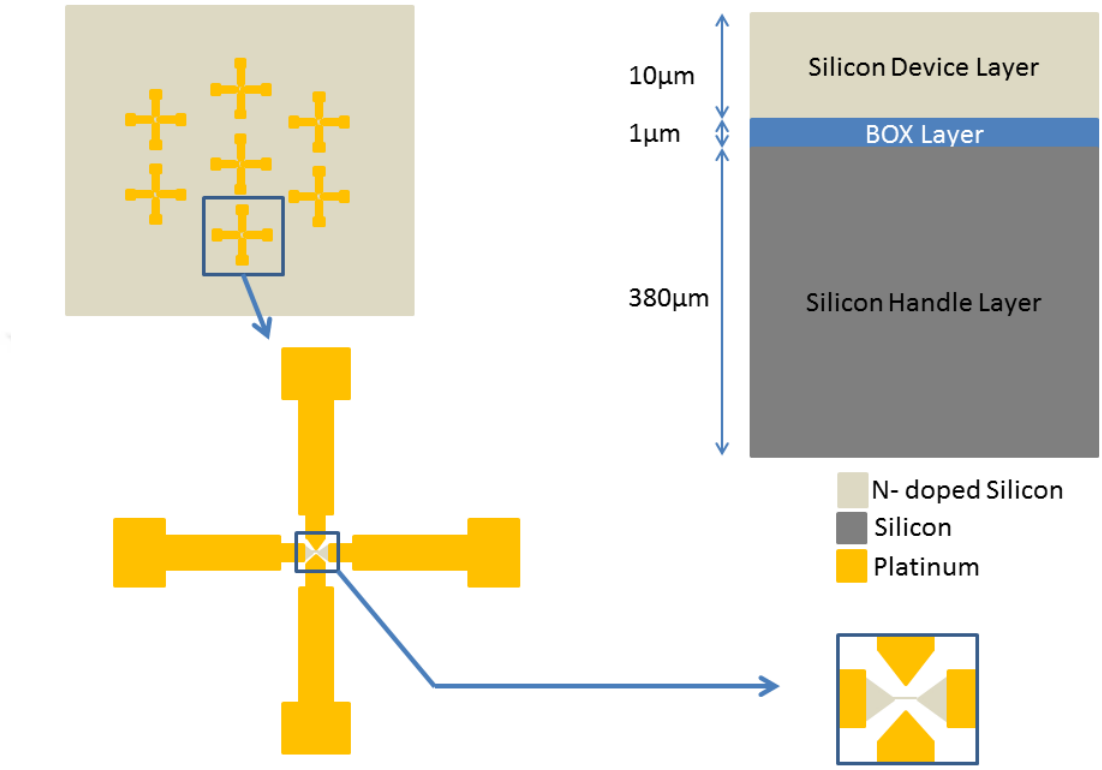


Figure 27: Representative image of an SOI chip including seven devices along with the utilized SOI cross-section.

SiNW fabrication is then completed with a conformal 100nm-LTO (Low Temperature Oxide) coating in a low-pressure chemical vapor deposition (LPCVD) chamber, Centrotherm furnace. LTO is etched away with directional dry etching in SPTS APS dielectric dry etcher at 10ºC. SPTS utilizes He/CHF_3 chemistry to proceed dielectric etch.

Duration of dielectric etch step is at utmost importance so that excessive etch can remove the protective FOX16 from the top surface of the SiNW. Upon removal of undesired LTO, Si surface is ready for patterning of metallic Pt-CR touchpad, signal lines are anchors.

Before the patterning of the remaining parts, we dice the wafer into 12mm x 12mm chips. Dicing is needed for deep reactive ion etching (DRIE) on chip-scale. Mask material patterning for DRIE is completed with a 500-nm-thick positive-tone ZEP520A 100% e-beam resist. E-beam lithography is then followed. After development in n-Amyl-Acetate solution

for 1minute and 45 seconds, DRIE of Si is conducted via Bosch process for 120 seconds in Alcatel AMS 200 SE fluorine dry etcher. Since each DRIE step is carried out for a single SOI chip, a 2-µm-thick AZ9260 positive resist-coated base wafer is used as the chip holder to eliminate the loading effect. AZ9260 offers a cheaper solution providing similar properties in terms of etching selectivity with ZEP520A.

Duration of DRIE step is also at utmost importance as it creates undercuts which may result with failure of the SiNW. A DRIE procedure is formed as the combination of repetitive steps of plasma etching in SF6 (flow rate of 300sccm) for 6.5 seconds and passivation in C_4F_8 (flow rate of 150 sccm) for 2 seconds. Substrate temperature is kept constant at 30°C and 600W source generation power is used. Upon performing such procedure, proper undercuts are achieved to release SiNWs. Protection of the FOX16 mask throughout the whole etch process has to be ensured as well, as FOX16 acts as the etch mask on the top surface of the SiNW, while side walls remain well protected under LTO.

After achieving desired Si dry etch with Bosch process, there are still three materials on the SOI chip: ZEP520A 100% e-beam resist which protects the metallic touchpads and signal lines, FOX16 protecting the SiNW top surface and LTO protecting the side walls of the SiNW. ZEP520A 100% e-beam resist is removed by 5 minutes oxygen plasma in Tepla GiGAbatch Oxygen Plasma Dry Etcher. FOX16, LTO and all remaining native oxide remnants are finally removed in HF Vapor at 40°C, this step can also be referred as “HF cleaning”. Figure 28 demonstrates the expected final view of double-clamped piezoresistive silicon nanowire.

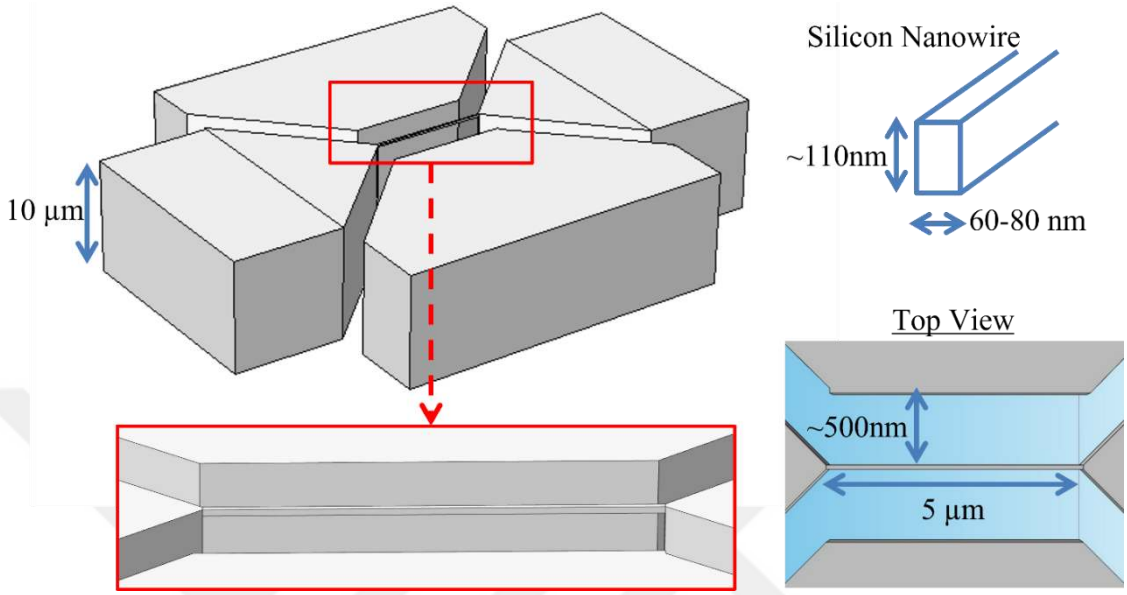


Figure 28: Representative scheme of suspended, single piezoresistive SiNW

From Figure 29 to 31, micrographs of fabricated SiNW are provided. SiNW stands as a solid structure so that well defined SiNW width and thickness is visible in all micrographs. In Figure 29, the state of the SOI chip is demonstrated before HF cleaning step. FOX16 is present above anchors and SiNW. Projected cross-section view of the device layer is provided in the same figure as well. Figures 30-31 show the state of the SiNW device after HF vapor cleaning. Scallops which are formed because of Bosch process are clearly visible. Scallop size is carefully adjusted so that no silicon whiskers shall be remaining after Bosch process. It is calculated that almost 110nm thickness is achieved through fabrication process (Figure 31).

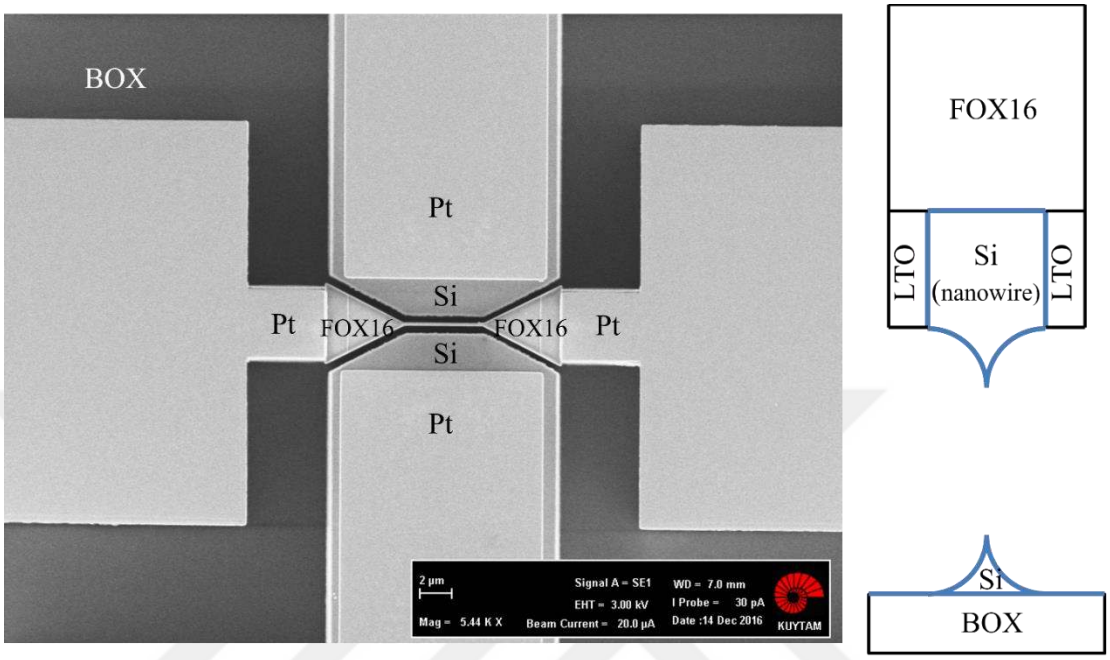


Figure 29: Material labeling before HF and a representative cross-section view of SiNW

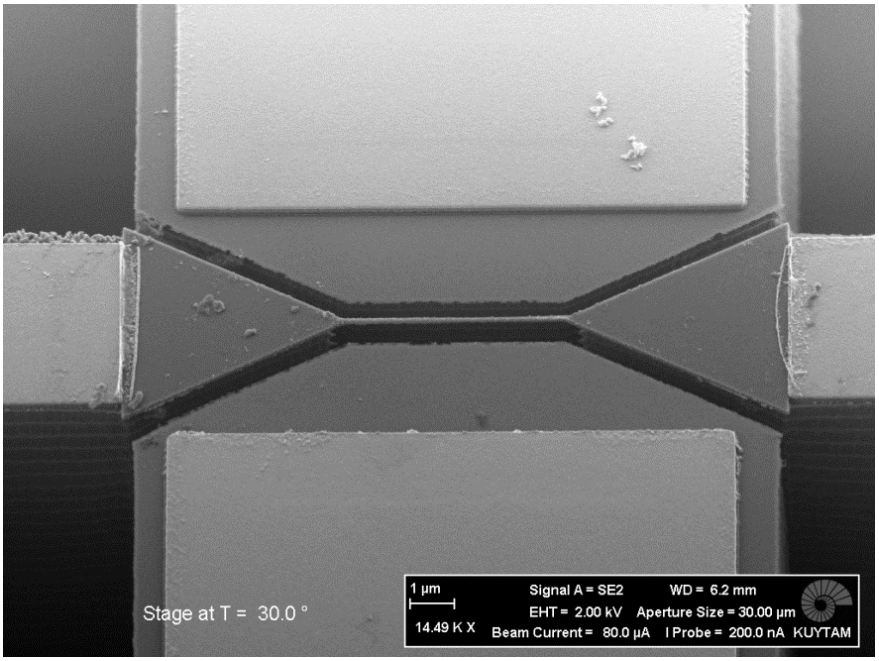
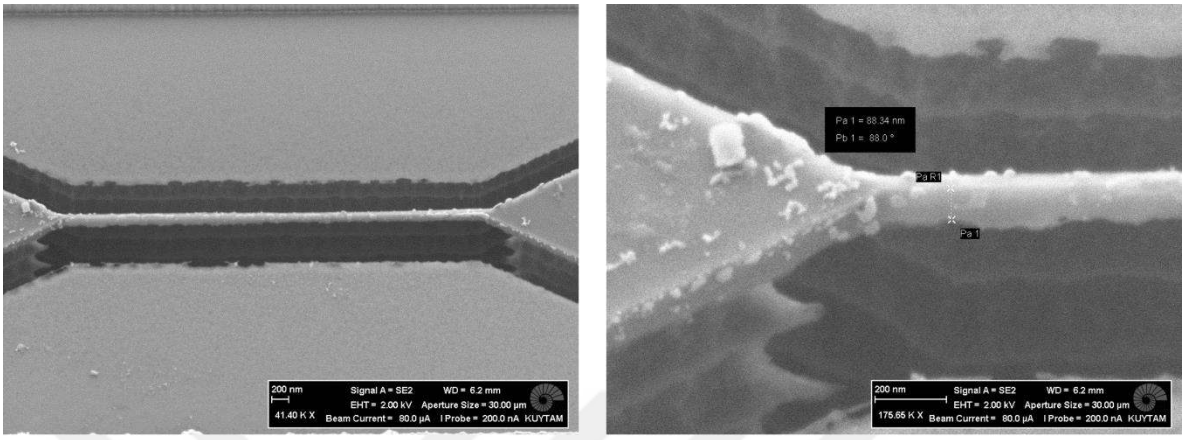


Figure 30: SEM micrograph of SiNW width: 60nm, length: 5µm, including anchor points and side electrode walls, after HF cleaning



(a) (b)

Figure 31: (a): SEM micrograph of SiNW width: 60nm, length: 5µm, close view, after HF cleaning, (b): closer view.

2.2. Electrical Characterization

Electrical characterization of fabricated piezoresistive single nanowires under no-strain condition (no external tensile/compressive loads such as bending or direct tensile/compressive load application) is achieved at Koç University Mechanical Characterization Laboratory (MCL). A probe station and Agilent Semiconductor Parameter Analyzer is utilized for I-V and I-t, V(constant) measurements. The probe station provides four probe manipulators and a BNC-Triax cable system which helps acquiring well shielded signals. Additional external electronics enabling signal processing, filtering, or amplification is not utilized. Measurement figures in this chapter indicate raw data acquired from the unstrained samples.

I-V and I-t, V(constant) measurements are carried out on twenty-one (21) unstrained samples. Samples show good results compared to the theoretical expectancy. SiNW behaves as a resistor so that one end of the nanowire is set to ground while the other end is subjected to voltage sweep. Voltage is swept from 0V to 100mV during the experiments.

High doping on the SiNWs enhances the conductance of the nanowire. Therefore, the current flowing on the SiNW increases significantly which may result with a possible burn-out. To support the idea, we swept the applied potential difference up to 500mV and lost the nanowire

because of the energy generated due to simple $E=I^2xR$ relationship. Hence, limits of applied potential difference is crucial to protect and repeat the experiments.

Our experiments also reveal that some of the chips still have silicon membrane as remnant just above BOX layer. It causes nanoampere scale parasitic current occurrence between different touchpads while we obtain microampere scale current flow on the piezoresistive SiNW, itself. Corresponding measurement figures are demonstrated in the following sections. Recalling that we initially highly dope the SOI wafer with a concentration of $4x10^{20}$ cm^{-3}, even such remnants could provide noticeable current flows. Consequently, we deduct that a diffusion gradient profile must have formed in such a way that doping concentration is lowered along the Si device layer thickness (10µm-depth). Nevertheless, the parasitic readout current is on the order of nanoampere while there is three order of magnitude difference with desired SiNW current. To provide a better insight, doping test along the device layer cross-section (10µm-depth) should be performed. In addition, presence of light effect on measurements is investigated under microscope light by turning on and off. Perfectly separated (no silicon membranes) samples show no indication of light effect while the other samples exhibit a noticeable effect. We demonstrated it with both I-V and I-t, V(constant) measurements. Recalling from the Introduction, [24] suggested that electromechanical characterization of the SiNWs should be performed under a dark environment to prevent photo induced effect on silicon.

Silicon and its products are used as photodetectors, as well [81]–[84]. Therefore, the electro-optical properties of silicon is a spectacular research area for developing photonic devices. Even heterojunctions with silicon is studied for optoelectronic coupling resulting with giant piezoresistance response [85]. One of them, [86] reports a study on neuron stimulation device integrated with silicon nanowire based photodetection circuitry. It is stated that the resistance of their SiNW is 5.6GΩ in dark, while it is 2.9MΩ under 4040 lux light and changes with respect to the light intensity (Figure 32). This corresponds to three orders of magnitude of difference between resistance values which they evaluate it as sufficiently large and useful evaluate it as sufficiently large and useful on a dynamic range for their specific purpose.

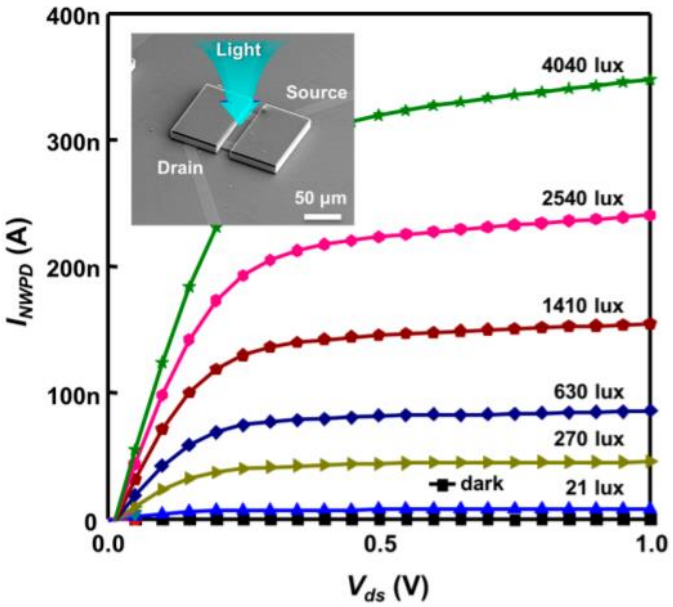


Figure 32: I-V curves of the SiNW under varying light intensity. Taken from [86].

Due to existance of silicon membrane at the bottom of our device layer, there are extra resistance paths might be affecting the electrical measurements. Therefore, membrane caused circuitry around SiNW is studied and explained later in this section, as well.

There are six groups of successfully tested SiNW geometries. Number and size of SiNWs is provided in Table 4. Starting with the first group, Figure 33 shows the theoretical expectation and measured I-V data for four SiNWs having 60-nm width and 5-µm length. These samples are in different SOI chips. It is observed that even though they are located on different chip, the resultant readout values are close to each other. 34.3kΩ, 38.3kΩ, 38.6µA and 40µA is achieved for four different samples which yields to 2.5kΩ, 2.59kΩ, 2.61kΩ and 2.91kΩ resistance, respectively. This supports the achievement of having a repeatable fabrication process. 3.3kΩ is calculated due to the information in Figure 33.

Table 4: Size and number of successfully tested SiNWs

Width (w)	Thickness (t)	Length (L)	# of Tested Devices
60nm	110nm	5 µm 10 µm	4 4
70nm	110nm	5 µm 10 µm	1 1
80nm	110nm	5 µm 10 µm 15 µm	3 5 3

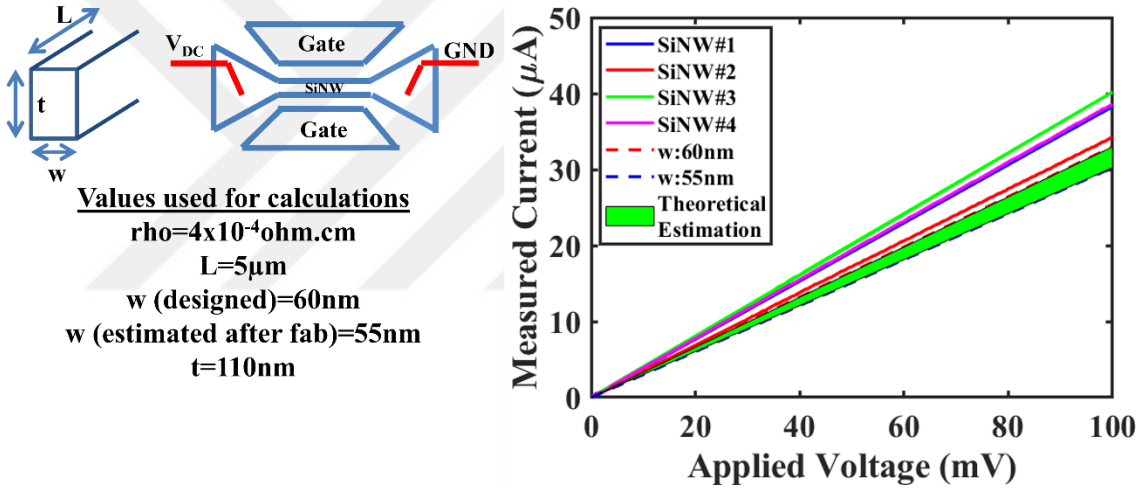


Figure 33: I-V measurement for four SiNWs having width:60nm, length 5µm and theoretical estimation.

The experimental SiNW resistance values are 25% off from the theoretical expectation, as well. Theoretical values are considered by assuming a rectangular cross-section is present. In contrast, our group's previous study revealed that our fabrication flow results with SiNWs having a trapezoidal shape (Figure 34) depending on the RIE step of the fabrication flow. Therefore, to have a better comparison between the theoretical expectation and experiments, TEM cross-section analysis should be performed.

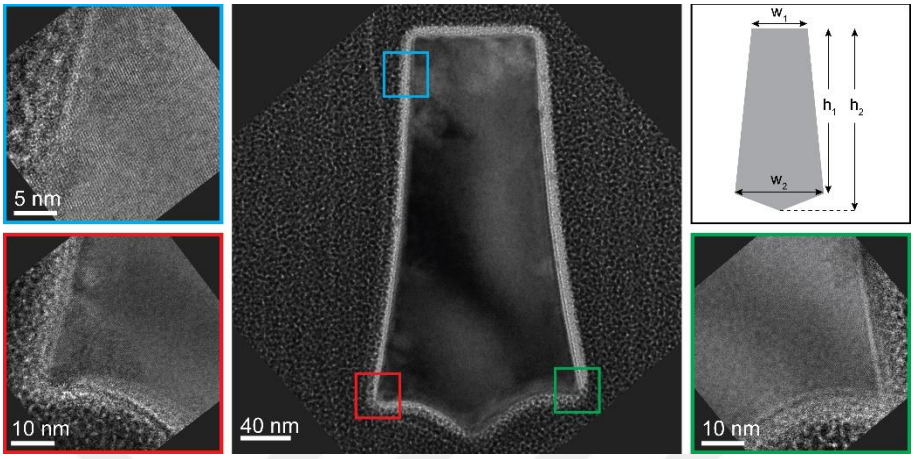


Figure 34: High-resolution TEM image of trapezoidal cross-section of SiNW. Taken from [33].

To come up with a starting point, for cross-section, we assumed 5nm shorter width and 40nm shorter thickness values than design pattern due to lithographic and RIE errors which we experienced previously. Estimated dimension values are given in Table 5.

Equation $R = \frac{\rho L}{A}$ is used to evaluate the expected SiNW resistance. ρ(rho) is the resistivity value for n-type doping extracted from Figure 14 (provided at Introduction) which enables conversion between doping density and resistivity, L is the length and A is the cross-section area of the SiNW.

Table 5: Designed and estimated dimensions of SiNW

	Width (Design)	Width (Estimation)	Thickness (Design)	Thickness (Estimation)	Length (Design)	Length (Estimation)
SiNW#1	60 nm	55 nm	130 nm	90-100 nm	5 µm	5 µm
SiNW#2	60 nm	55 nm	130 nm	90-100 nm	10 µm	10 µm
SiNW#3	70 nm	65 nm	130 nm	90-100 nm	5 µm	5 µm
SiNW#4	70 nm	65 nm	130 nm	90-100 nm	10 µm	10 µm
SiNW#5	80 nm	75 nm	130 nm	90-100 nm	5 µm	5 µm
SiNW#6	80 nm	75 nm	130 nm	90-100 nm	10 µm	10 µm
SiNW#7	80 nm	75 nm	130 nm	90-100 nm	15 µm	15 µm

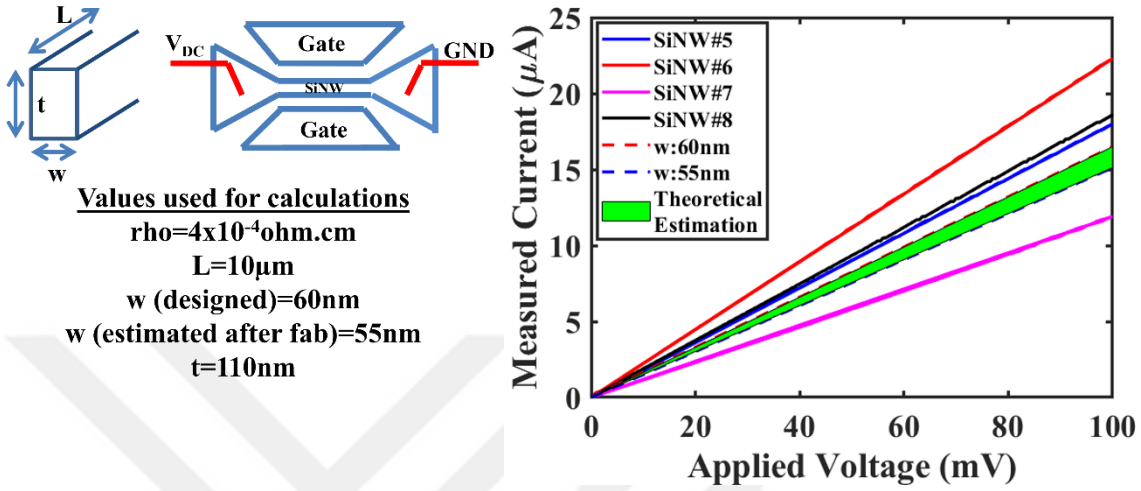


Figure 35: I-V measurement for four SiNWs having width:60nm, length: 10µm and theoretical estimation.

Figure 35 demonstrates the theoretical and experimental results of four SiNWs 60nm in width and 10µm in length. Results reveal that fabrication repeatability performance is poorer than SiNWs having 60nm x 5µm. 11.9µA, 18µA, 18.6µA and 22.3µA is obtained at 100mV potential difference for different SiNWs. 4.48kΩ, 5.37kΩ, 5.56kΩ and 8.40kΩ experimental resistance values are calculated while 6.61kΩ is obtained for the given information in Figure 35. Experimental resistance values of the SiNWs vary up to 90% from each other. This might be due to having a longer nanowire geometry. Controlling the silicon etchant performance in DRIE is more challenging for longer nanowires. Therefore, variations in cross-section might be possible, such that it affects the I-V characteristics of the samples.

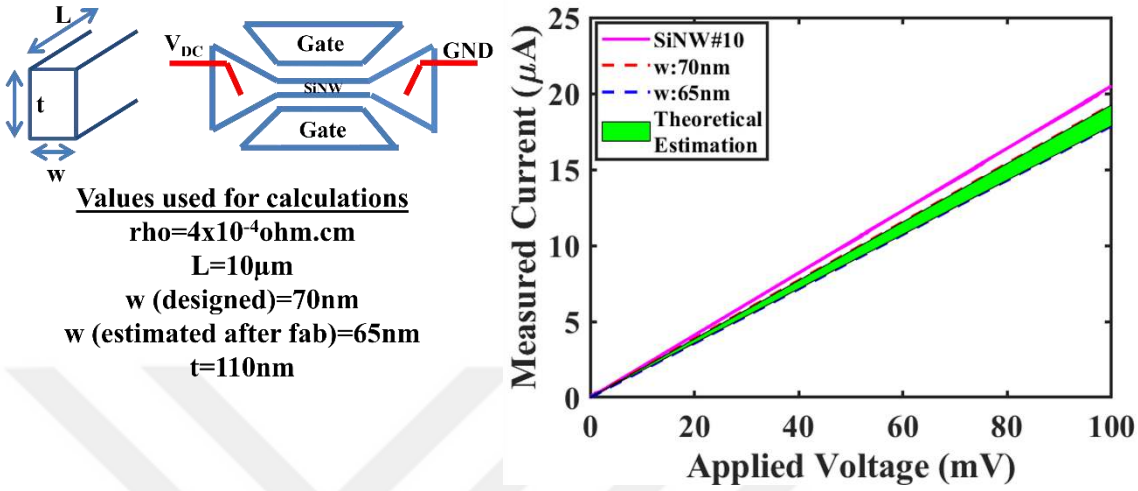


Figure 36: I-V measurement for each SiNW having width:70nm, length: 10µm and theoretical estimation.

We could only get one working SiNW having 70nm in width and 10µm in length which results in a very good accordance with theoretical expectation. 20.7µA is achieved for 100mV. 4.83kΩ is the experimental resistance of the SiNW while 5.59kΩ is obtained as the theoretical resistance with the provided information in Figure 36. Almost 15% resistance difference is calculated between theoretical and measured data.

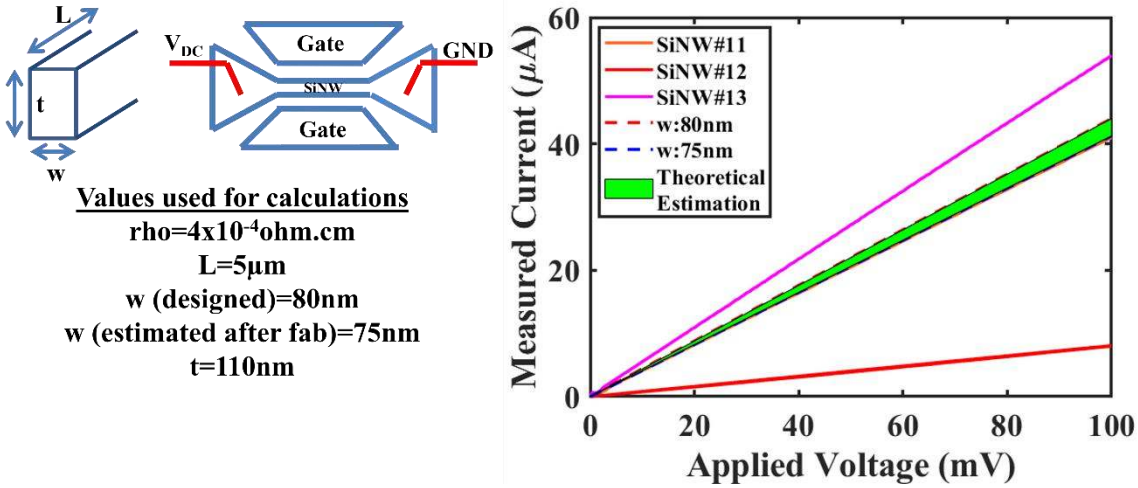


Figure 37: I-V measurement for two SiNWs having width: 80nm, length: 5µm and theoretical estimation.

There are three set samples for 80nm-width nanowires: 5µm, 10µm and 15µm in length. I-V measurements on the first group (two SiNWs:80nm x 5µm) and expected result are presented in Figure 37. One of the measurements almost overlaps with the theoretical I-V line while

the other one is obviously deviating from them. 1.85kΩ, 2.44kΩ and 12.42kΩ are calculated as the result of measurements. Theoretical nanowire resistance for the information in Figure 37 is calculated as 2.42kΩ.

Five SiNWs are subjected to testing for SiNW group having 80nm width and 10µm length. They demonstrate good accordance with respect to each other and expectancy (Figure 38). 26µA, 26.2µA, 26.4µA, 28.5µA and 29.2µA is obtained for the SiNWs while 3.42kΩ, 3.51kΩ, 3.81kΩ, 3.79kΩ and 3.84kΩ are calculated, respectively. We found theoretical resistance as 4.85kΩ for the information in Figure 38.

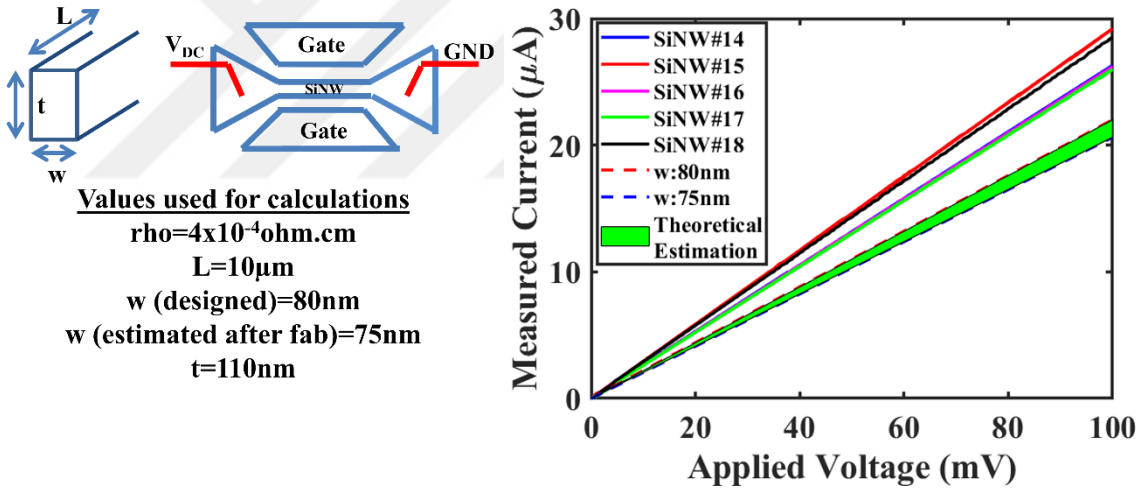
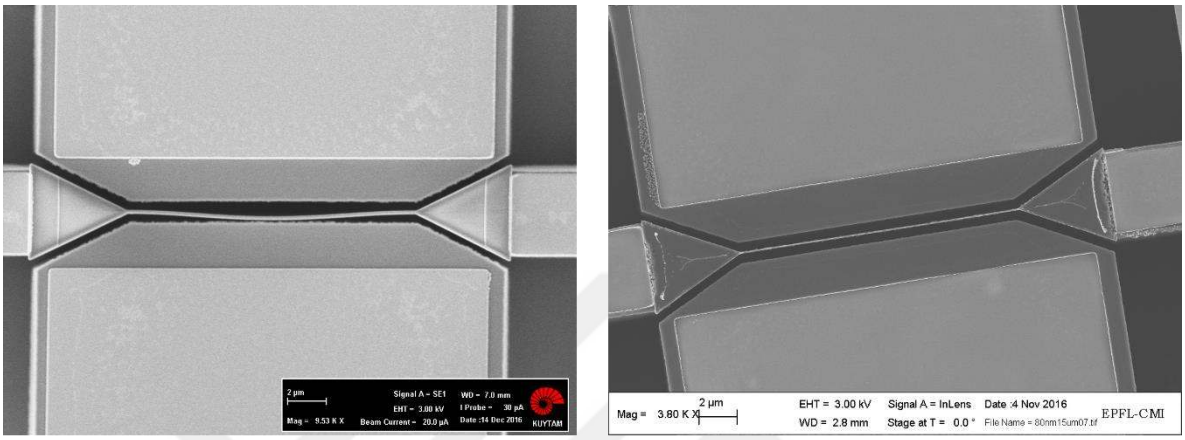


Figure 38: I-V measurement for width:80nm, length 10µm nanowire and theoretical estimation for five SiNWs.

Finally, last group of samples designed as 80nm-width and 15µm-length is tested (Figure 40). 15µm is the maximum length of a silicon nanowire that we tried to fabricate. To note, we noticed that some of the SiNWs having 15µm length are bended after the Bosch process step (Figure 39). This might be due to stress generated on the nanowires during the 10µm Si deep etch. Lesser number of 10µm-length nanowires show bending while none of the 5µm-length nanowires demonstrated such behavior. Due to its higher length/area ratio, stress might be causing the resultant bending. 4.78kΩ, 4.90kΩ and 5.65kΩ resistances are obtained for the measured current outputs under 100mV potential difference, respectively. 7.27kΩ

is expected for the provided information in Figure 40.



(a) (b)

Figure 39: SEM micrographs of a SiNW having 80nm-width, 15µm length, (a) bended after Bosch process, (b) not bended after Bosch Process.

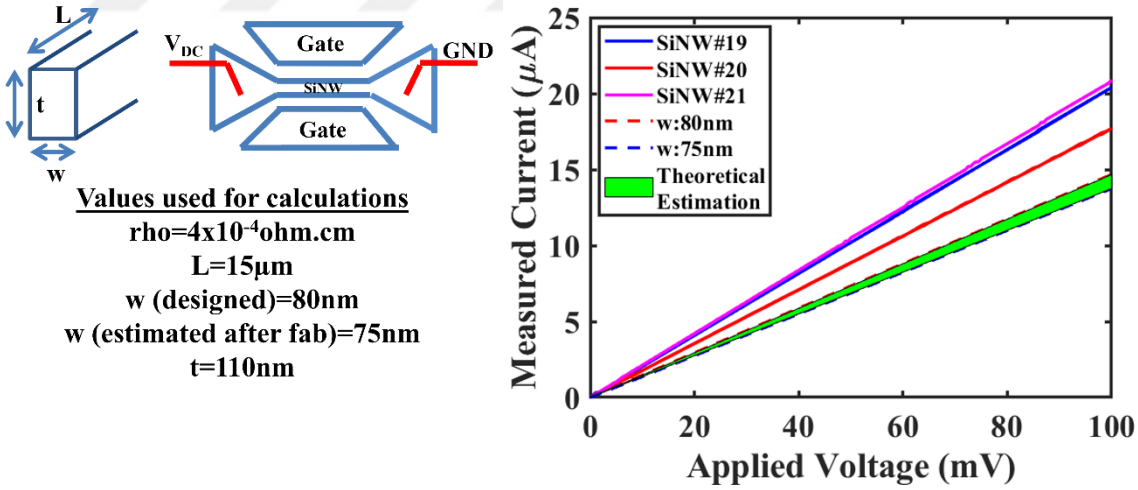


Figure 40: Experimental I-V measurement for width:80nm, length 15µm nanowire and theoretical estimation for two SiNWs.

It was already noted that light is an important factor affecting the electron excitation in the silicon so that a dark-room setup is a mandatory requirement for more reliable experimental results especially when studying nanoampere scale measurements. Since our samples are highly doped, the measured current for 100mV potential difference is expected on the order of microampere which is three orders of magnitude higher than a possible photo induced

effect. Therefore, such effect can be considered as a negligible noise which will be analyzed with the upcoming I-V measurement plots.

2.3. The Effect of Silicon Membranes and Light on Electrical Measurements

To investigate photo induced effect on our working samples in microampere scale I-t, V(constant) measurements are performed. This measurement method simply employs a constant potential difference on the specimen, while the current response is measured for a certain period. Four our case, applied potential difference on the SiNWs is kept constant at 100mV and current change with varying time interval is obtained. During the tests, microscope light is turned on and off for certain period to detect any change on the measured current. Figure 41 shows that there is no significant and visual light effect on the readout current. Before the test, it is ensured that there is no silicon membrane underneath the SiNW and the SiNW is still encapsulated with FOX16 and LTO.

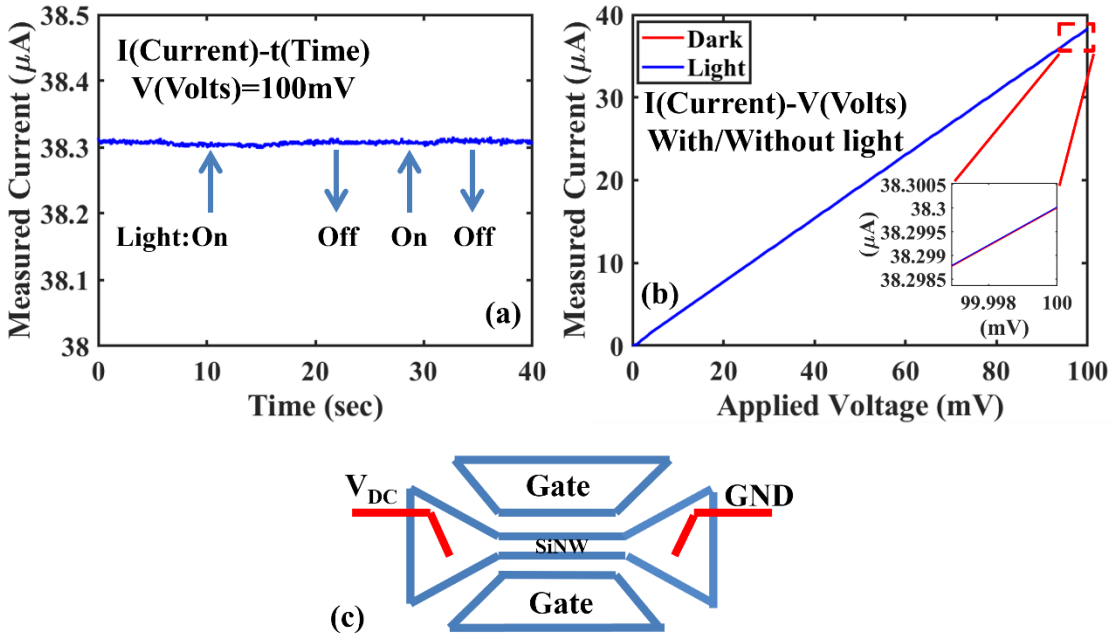


Figure 41: (a) I-t, V(100mV) measurement while turning on and off the light, (b) I-V measurement with and without light, and (c) measurement configuration of SiNW having width 60nm, length 5µm.

However, repeating the same experiment for a different sample (width: 80nm, length: 10µm), it is observed that turning light on and off slightly affects the results on the order of

nanoampere. Figure 42(a) shows I-V measurements in dark and under microscope light between 0-100mV. While Figure 42(b) demonstrates I-t, V(constant) measurements at 100mV potential difference for light presence and absence. This sample has an encapsulated SiNW and silicon membranes that is not etched at the bottom of the silicon device layer. Although it seems dark and light measurements overlap each other in Figure 42(a).

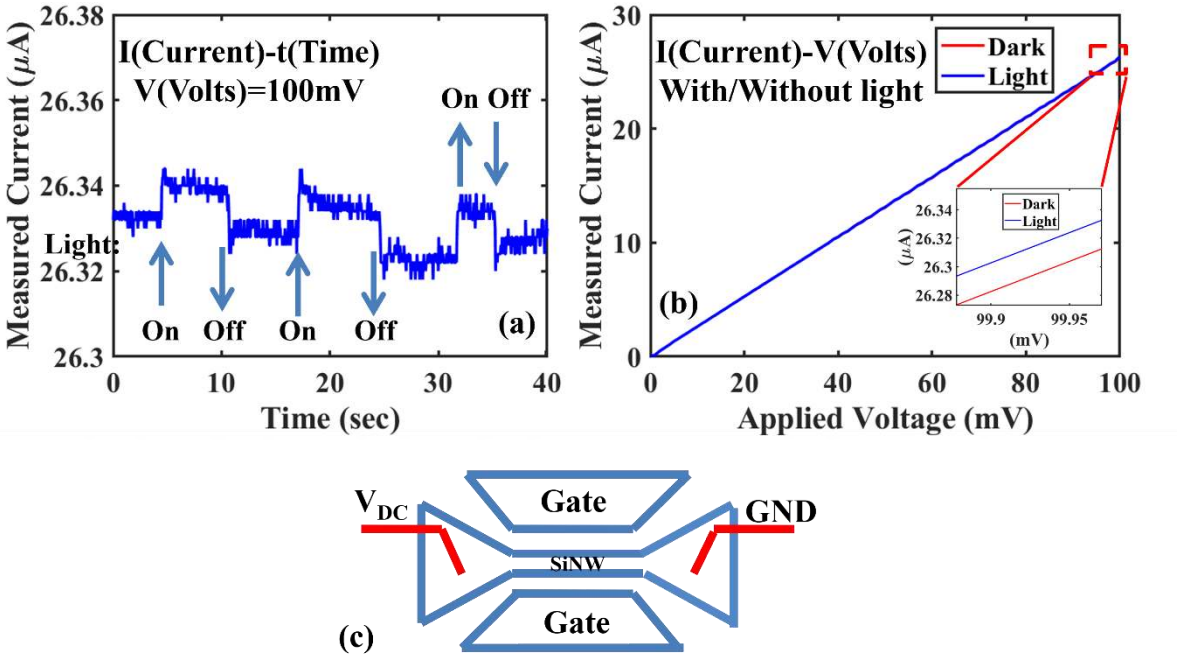


Figure 42: Electrical measurement of a SiNW having silicon membrane: (a) I-t,V (100mV) measurement while turning on and off the microscope light, (b) I-V measurements in dark and under microscope light and (c) measurement configuration.

Figure 42(b) reveals almost 20nA light effect in the measurement. In an ideally timed Si Bosch process scheme, there should be no silicon membrane at the bottom of silicon device layer. Figure 43 provides a representative image showing how the bottom of the device probably appears and how it is supposed to look like after fabrication. Performing I-V measurements from the gates will constitute a proof to presence of silicon membrane. Picoampere measurement should be expected in a perfectly separated silicon environment. Even though, identifying the light effect was not the scope at first, encountering silicon membranes made it crucial to clarify and it became a noteworthy phenomenon. Therefore, these measurements serve to fulfill the idea of lightly/no doped silicon membrane is affected

by the illumination. Nevertheless, not all chips and samples include such silicon membranes. We conducted I-V measurements with gate-gate, gate-anchor and anchor-anchor configurations mentioned before on every sample / chip. It is observed that samples which do not include silicon membranes exist, as well. Hence, there is no physical connection between gates and SiNW anchors except the nanowire itself. Figure 44 shows the in-light I-V response of a sample having no silicon membrane. The measurement is conducted between an anchor and a gate terminal. Same measurement is reconducted in dark and obtained the same plot, repeatedly. This sample has a highly doped SiNW which already generates 17.5µA current for 100mV potential difference and plotted in Figure 35, previously. The readout current is in the order of picoampere and sinusoidal. This is a very good example of accordance between etching through whole device layer silicon in the narrow regions and protecting the SiNW.

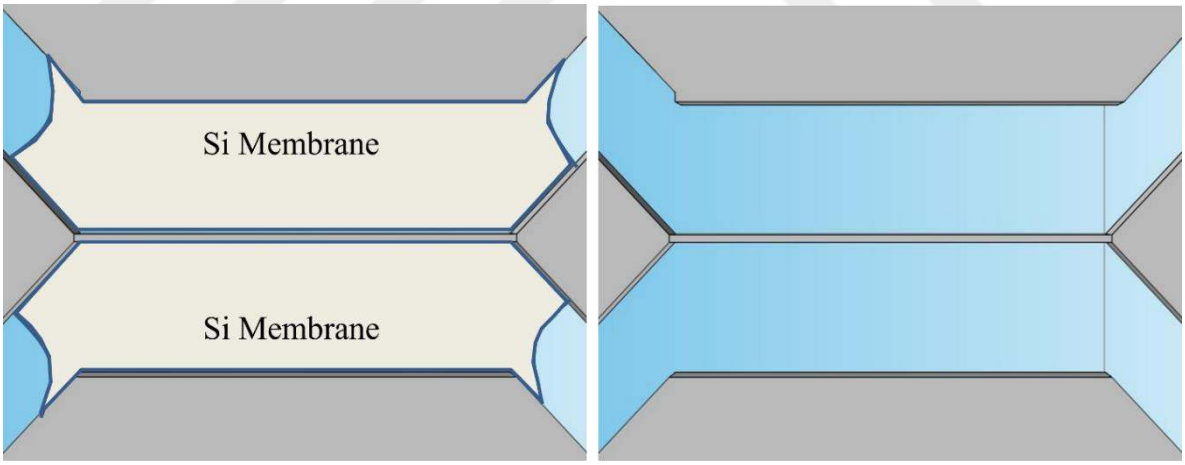


Figure 43: (a) Representative scheme of silicon membrane left just above the BOX layer, (b) how it is supposed to look like after a clean silicon etch.

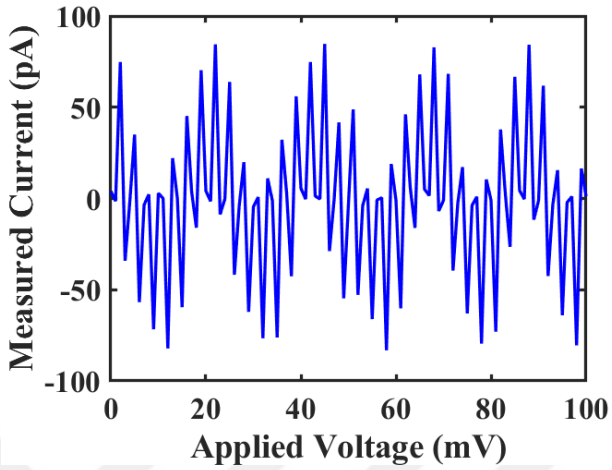


Figure 44: I-V meas. from the gate and anchor SiNW: 60nm-width, 10µm-length as microscope light is on.

If there is a silicon membrane left after fabrication, it should have a lower doping density because of its distance from the top of the device layer (10µm) due to the plot given in Figure 45. This plot provides the diffusion profiles for varying diffusion durations at 950 ºC [87]. Doping procedure in our fabrication process employs 30mins of diffusion time at 950ºC. Therefore, it can be stated that the dopant concentration drastically decreases almost after 250nm depth. There are also open areas on the silicon membrane, which makes it susceptible to direct light presence. Therefore, it can be concluded that aforementioned nanoampere scale changes in the measurement should be based on the light effect on the silicon membrane but not the nanowire itself.

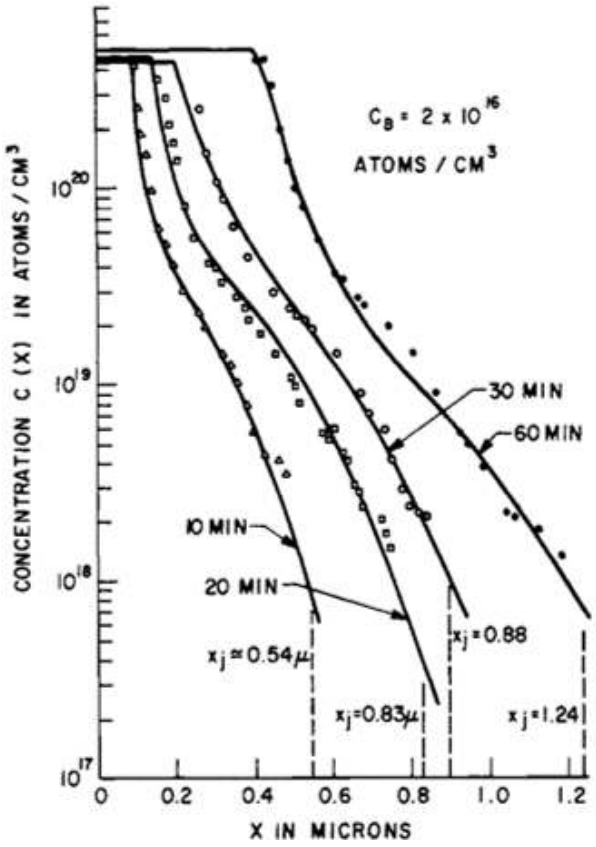


Figure 45: $POCl_3$ source diffusion profiles at 950ºC diffusion for 10, 20 ,30, and 60 minutes. Taken from [87].

To find a proof that solidifies the idea of silicon membrane is present and affected by the microscope light, we performed detailed measurements from each gate terminal and anchor, as well. As a critical point, selected samples should not have SiNW so that we would only measure the silicon membrane performance. Figure 46 shows the SEM micrograph of the selected sample. To note, silicon membrane is already located in 10µm depth and SEM capture window is too narrow to observe through (almost 500nm). Measurement configurations related with the I-V and I-t,V(constant) measurements are demonstrated in Figure 47.

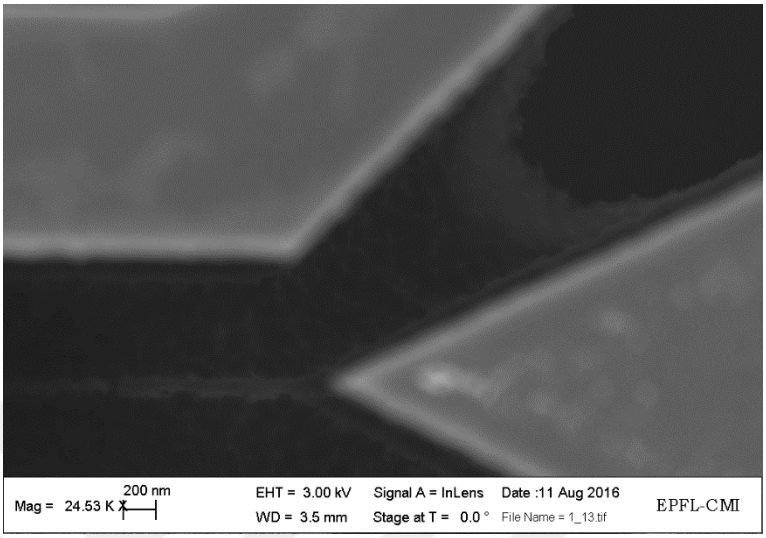


Figure 46: SEM micrograph of silicon membrane remained at the bottom of device layer.

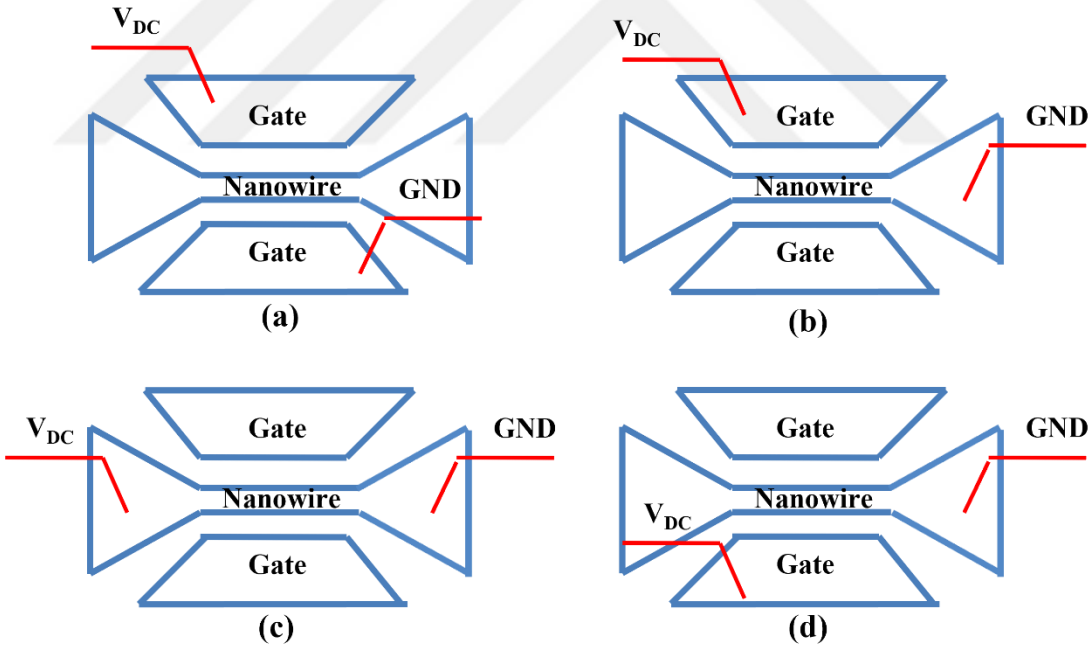


Figure 47: Electrical measurement configurations between a) both gates, b) gate-anchor, c) SiNW anchors, and d) gate-anchor.

We demonstrate the first set of measurement in Figure 48: (a) provides the I-V measurements on silicon membrane in dark and (b) in the illuminated environment. (c) provides the measurement configuration and (d) shows the I-t, V (100mV) measurement while turning on

and off the light. Recalling that no SiNW exist in this device, measured current between anchors slightly increases with the increasing voltage in dark. Almost 700 mega ohms-resistance is calculated for an average of 0.15nA change in current under 100mV. However, introducing microscope light into the test chamber drastically changes the measurements as shown in Figures 48 (b) and (d). In Figure 48 (b), I-V measurement is obtained during sweeping the applied potential difference while the microscope fluorescent light is constantly kept on. 30nA current change is obtained for 100mV which results with 3.33 mega ohms-resistance. Comparing (a) and (b), significant effect of illuminance on the silicone membrane is achievable. On the other hand, to see how quickly system responds to the light presence we also performed I-t,V(100mV) measurement while constant 100mV potential difference is provided in (d). It should be noted that maximum light intensity provided during the test. Consequently, readout current responds quickly as providing a steep slope response when an instant fluorescent light is provided in/out to/from the chamber. The fluorescent light used in these tests is a simple probe station optical microscope light which fulfills the requirements of standard illumination purposes.

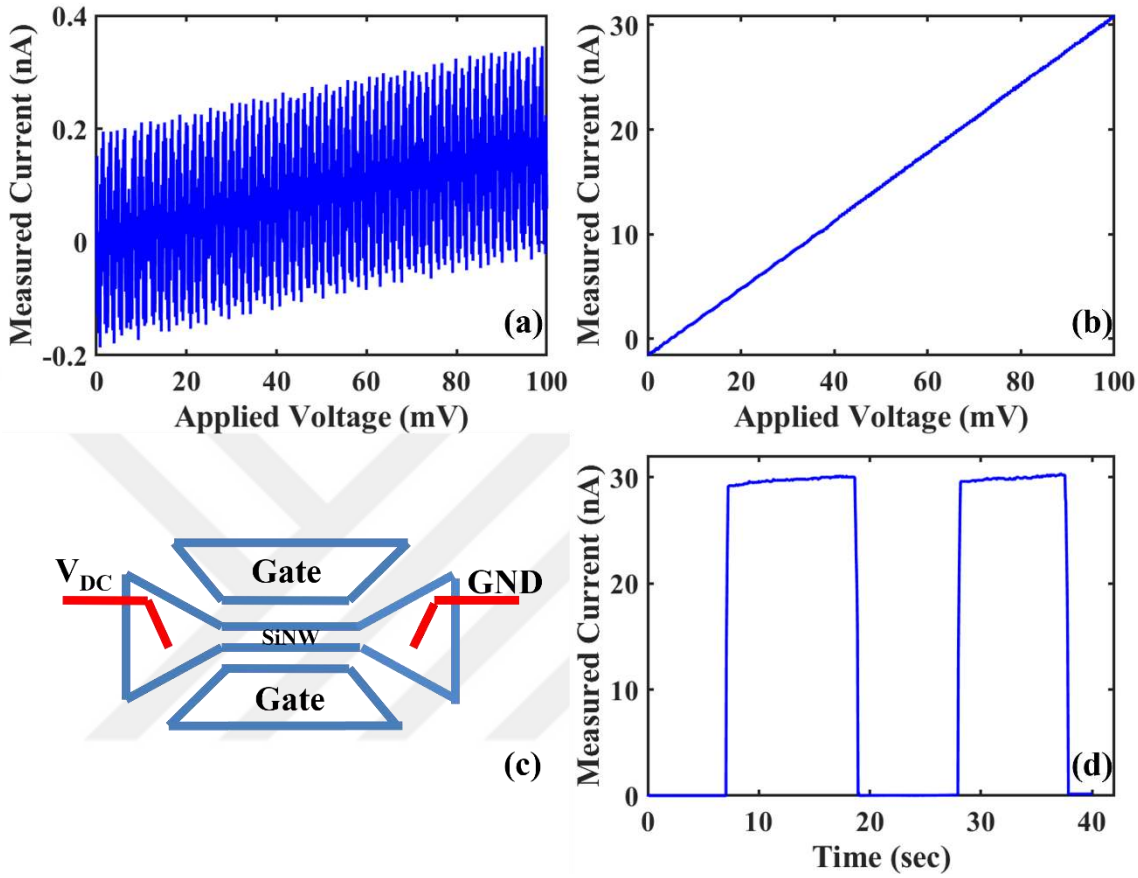


Figure 48: Electrical measurement of a device which does not have silicon nanowire, but silicon membrane: I-V measurements (a) in dark, (b) under microscope light, (c) between the gates and (d) I-t,V (100mV) measurement while turning on and off the microscope light.

Second set of measurements involve gate-anchor configuration. In Figure 49, I-V measurements in dark (a) and light (b) provided. 0.17nA change in current is obtained for 100mV potential difference. Resistance in this measurement scheme is calculated as almost 590 mega ohms. When the microscope light is presented to the setup measured current increased to 28nA, which results with an average resistance of 3.6 mega ohms. Measurement configuration is provided in (c), as well. Finally, I-t,V (100mV) test is conducted to realize the response due to instant change from dark to light and light to dark (d). Effect of microscope light on the measurement is repetitively observed. A curious reader can visit Appendix to analyze rest of the measurements conducted with other configurations. It can be concluded that all measurement configurations substantiate the photo induced effect on the lightly doped silicon membrane.

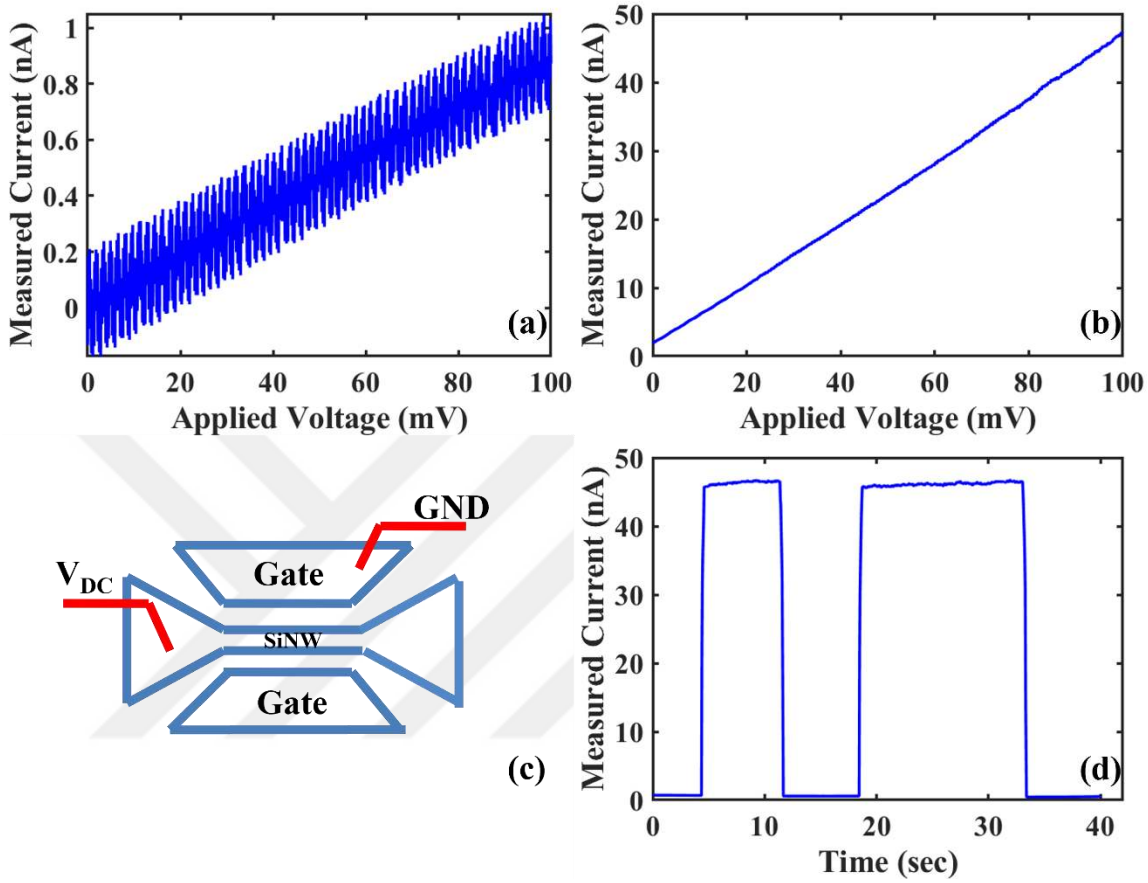


Figure 49: Electrical measurement of a device having no silicon nanowire: I-V measurements (a) in dark, (b) under microscope light, (c) between a SiNW anchor and a gate and (d) I-t,V (100mV) measurement as we turn on and off the microscope light.

2.4. Circuitry Simulations on Parasitic Effect of Silicon Membrane

There should be only two terminals, "A" and "B", and a SiNW resistor in an ideal measurement scheme. However, existence of silicon membrane introduces more complex scenario. Silicon membrane acts as a parasitic structure and adds additional resistances into the measurement system. All resistors including such parasitic resistances on the system is simply demonstrated in Figure 50 (a) and (b). SiNW resistor is represented as "R" while rest of the parasitic resistances are denoted from "R1" to "R6". "A" and "B" stands for the SiNW anchors while "C" and "D" represents surrounding gate pads. Each resistance symbol corresponds to an assumptive resistance located between "A", "B", "C" and "D" terminals. To evaluate the effect of parasitic resistances on the measurements, a simple simulation is

conducted on a web platform: www.circuitlab.com. This website provides a user-friendly interface to reach a quick solution by applying circuitry analysis. Arbitrary values for R, R1, R2, R3, R4, R5 and R6 are assigned considering the I-V measurements from all terminals. Simply, data from measurements is nanoampere and microampere scale from which we understand that some resistance values are comparably high in terms of order of magnitude and others are low. Therefore, arbitrary values are selected as R1=60 Ohms, R2=80 Ohms, R3=65 Ohms, R4=85 Ohms, R5=90 Ohms, R6=100 Ohms and R=0.1 Ohms which indicates that SiNW resistance is almost three order of magnitude lower than the others because of its higher level of doping concentration.

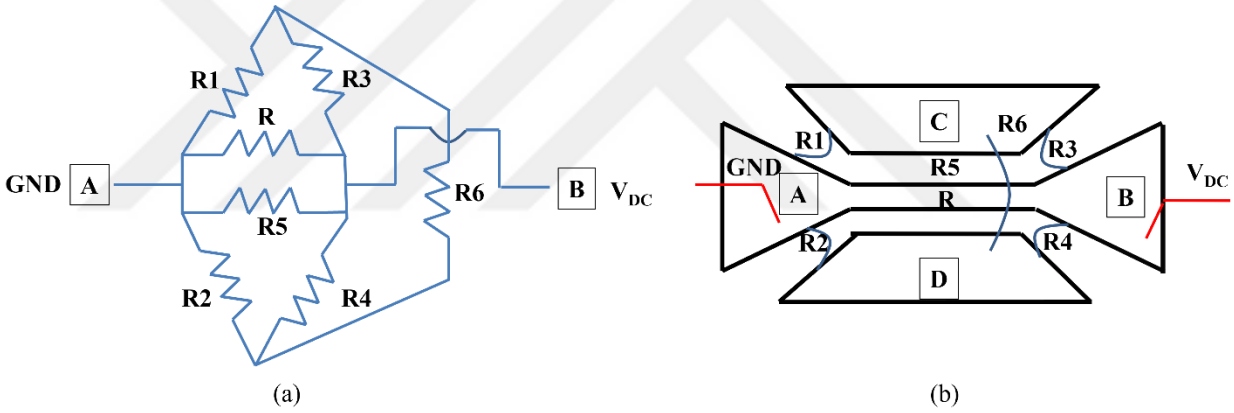


Figure 50: (a) Circuitry scheme of electrical measurement conducted on SOI chips, (b) physical demonstration of (a), top view.

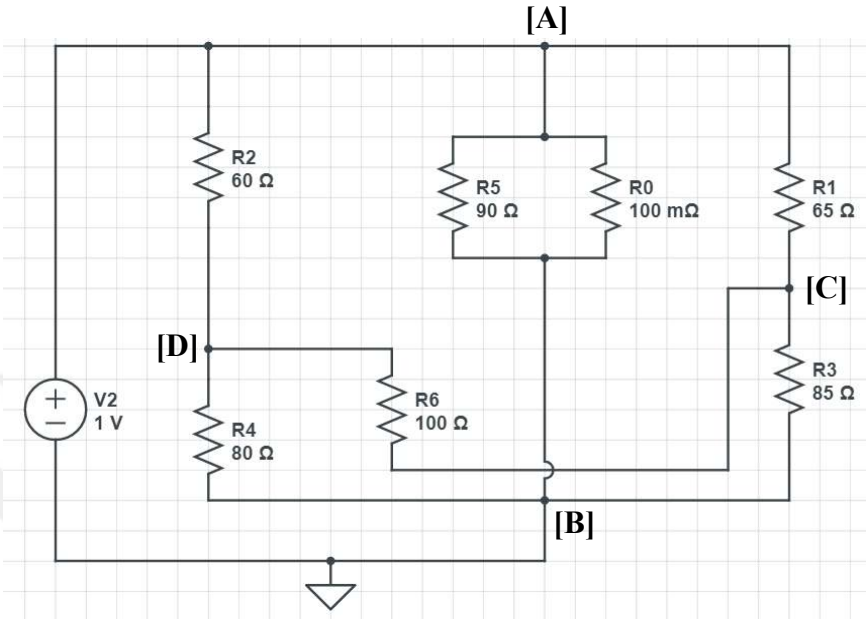


Figure 51: Path A-B circuitry simulation from www.circuitlab.com.

To realize the effect of silicon membranes, we conducted simulations based on different terminals (Figures 51-53). A-B current flow path (Figure 51) is the actual route that we pursue, which basically considers the SiNW as the main resistor. D-C (Figure 52) and A-C (Figure 53) considers at least one terminal from surrounding gates. The current flowing over each randomly selected resistance is extracted from the simulations and tabulated in Table 6. For path A-B, simulated current flowing over R0 is 10 A and 10.02 A on the voltage source. This outcome confirms that R0 dominates the overall circuitry. For path D-C, only 66.79 µA flows over R0 while voltage source has 24.06 mA in total. For path A-C, 14.91 mA current flows over R0 and 34.57 mA over voltage source. Comparing the three different path simulations we understand that R0, which depicts the SiNW resistor, dominates the other resistances only in the simulation A-B, while its contribution in A-C and D-C is inferior. Consequently, we can confirm that our actual I-V measurements from A to B terminal are reliable with a slight margin, even if we have silicon membrane.

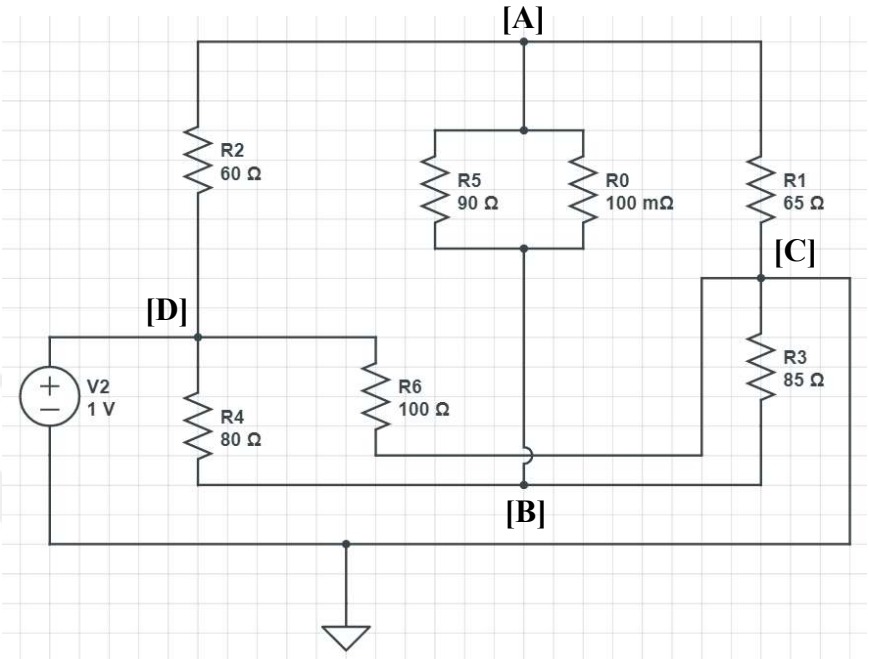


Figure 52: Path D-C circuitry simulation from www.circuitlab.com.

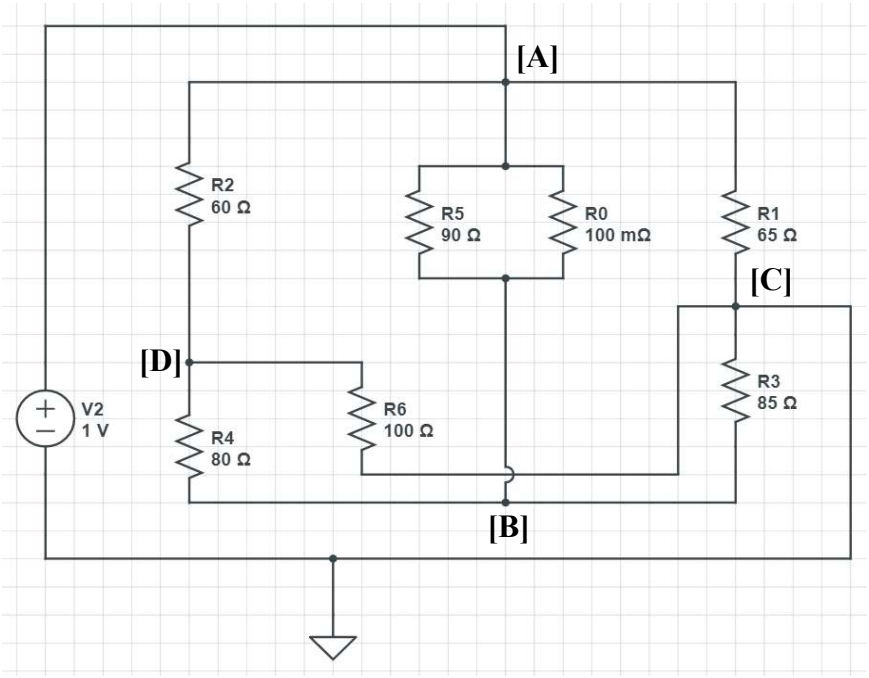


Figure 53: Path A-C circuitry simulation from www.circuitlab.com.

Table 6: Proposed circuitry simulation results between terminals A-B, D-C and A-C

Resistance Name	Assumptive Resistance Value	Readout Current (A-B)	Readout Current (D-C)	Readout Current (A-C)
R0	0.1 Ohms	10 A	66.79 µA	14.91 mA
R1	65 Ohms	6.651 mA	7.918 mA	15.38 mA
R2	60 Ohms	7.159 mA	8.035 mA	4.263 mA
R3	85 Ohms	6.679 mA	6.093 mA	11.75 mA
R4	80 Ohms	7.131 mA	6.026 mA	3.179 mA
R5	90 Ohms	11.11 mA	74.21 nA	15.57 µA
R6	100 Ohms	27.83 µA	10 mA	7.442 mA
Source (V2)	Source(V2)	10.0025 A	24.06 mA	34.57 mA

Even though, identifying the light effect was not the scope at first, encountering silicon membranes made it crucial to clarify and it became a noteworthy phenomenon. Therefore, these measurements serve to fulfill the idea of lightly/no doped silicon membrane is affected by the illumination and how it affects the overall measurements.

2.5. Results and Discussion

Highly doped ($2x10^{20}cm^{-3}$) double clamped piezoresistive silicon nanowires are fabricated in CMi, EPFL, Lausanne, Switzerland. SOI wafer (10-1-380µm) is utilized to obtain 12mm x12mm sample chips. Each sample chip contains twenty-one (21) devices: 60nm-5um, 60nm-10um, 70nm-5um, 70nm-10um, 80nm-5um, 80nm-10um, and 80nm-15um in width and length, respectively. Electrical characterization step, including I-V and I-t,V (constant) measurements of the fabricated devices are performed at Mechanical Characterization Laboratory (MCL), Koç University, Istanbul, Turkey. During the measurements, mechanical bending which employs a geometrical change at the SiNW shape is not implemented. Therefore, current change due to stress state and gauge factor of the SiNWs are not obtained and calculated. Each measurement is repeated five times to ensure repeatability. 100mV is set to be the upper limit for sweeping voltage as a safety measure. This value is used for I-t,V (constant) measurements as well. Electrical characterization is completed for anchor to

anchor, gate to anchor and gate to gate combination scheme to determine any existing additional parasitic resistance in the device. Results reveal that some of the fabricated SiNWs provide microampere order of current readout while others stay in nanoampere scale. μA-measured SiNWs show consistency with each other and theoretical calculations. Theoretical resistance calculation is based on a rectangular SiNW cross-section. The obtained SiNW width, thickness and length is also estimated based on our previous experiments. Successfully fabricated SiNWs showing μA scale readout illustrate linear I-V characteristics which is expected due to reliable resistor behavior. We also noticed presence of silicon membrane remnants at the bottom of 10 μm silicon device layer which indicated one or two more Bosch Process etch cycles is necessary for those samples. Effect of silicon membrane on electrical measurements is studied in terms of a simple circuitry analysis. It is found that parasitic effect of silicon membrane in electrical measurements is noticeable but negligible due to three order of magnitude difference between highly doped SiNW and probably lightly doped silicon membrane. To quantify the doping concentration profile along the device layer, a quantitative test should be conducted for doping density. Since the device layer thickness is 10um, which is quite excessive for ion implantation to provide the requested doping density, we believe, the silicon membranes are not doped and has the resistivity of the SOI wafer-at-start. Therefore, the resistivity of silicon membrane should be orders of magnitude higher than the SiNW.

Chapter 3

Piezoresistivity Characterization of Vertically Stacked SiNW Arrays

3.1. Vertically Stacked Silicon Nanowire Arrays

The piezoresistive nanowire array tested in this project consists of eight vertically stacked silicon nanowires. Silicon nanowires have dimensions of ~70nm in width and thickness, and 2µm, 3µm, 4µm and 5µm in length. The vertical arrays of piezoresistive silicon nanowires are fabricated on an SOI wafer to use the advantage of having an insulator buried oxide layer between two silicon layers: silicon device layer and silicon handle layer. SOI wafer has 1µm silicon device layer, 1µm SiO2 buried oxide layer (BOX) and 725µm silicon handle layer which supports and carries the fabricated structure. Fabrication process is completed in Center of MicroNano Technology (CMI) cleanroom facility in EPFL (École Polytechnique Fédérale de Lausanne) in Lausanne, Switzerland. Fabrication flow and details are presented in [88].

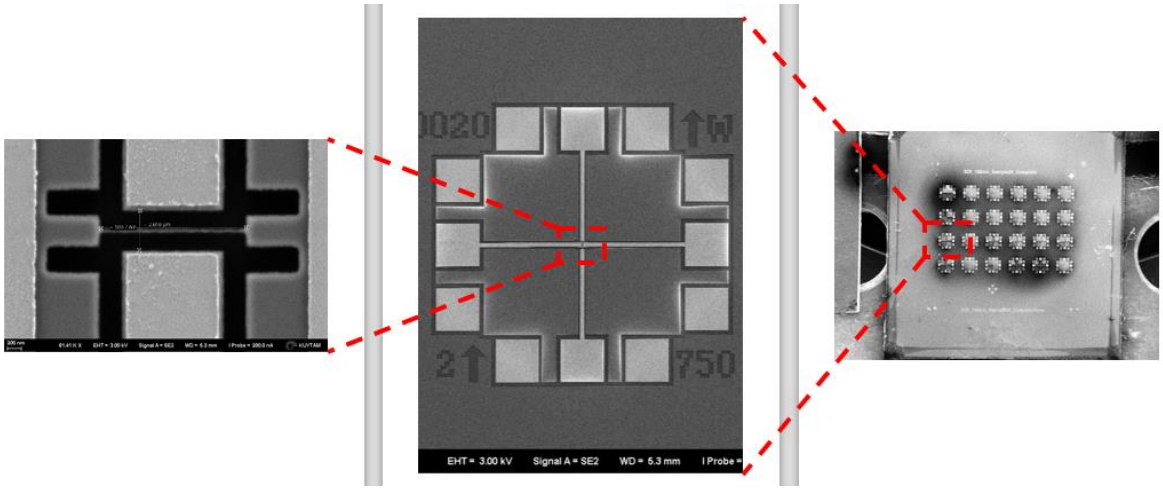


Figure 54: Sample SOI chip and inner sections.

Fabrication starts with an initially cleaned SOI wafer. RCA1 and RCA2 cleaning procedures are applied to remove all organic and inorganics remnants. Then SOI wafer is subjected to very high n-type (Phosphorus) doping. Annealing treatment is applied for doping uniformity as well. Doping level is set to be in the near edge of 10^{20} cm^{-3}. Upon doping, lift-off mask is defined by e-beam lithography to deposit metallic alignment marks. 5nm Cr and 50nm Pt is deposited on the wafer in an e-beam evaporator. Then lift-off process is finalized in an acetone bath. At this point, SOI wafer is diced into smaller chips with a dimension of 10mm x 10mm. E-beam lithography procedure is repeated to define metallic signal lines and touch pads. Lift-off is completed in an acetone bath upon depositing 5nm Cr + 50nm Pt, respectively. Then, SiNW pattern is defined by e-beam lithography and followed with DRIE dry etching process to obtain SiNW array, touchpads and signal lines. E-beam lithography resist is removed via oxygen plasma and SOI chip (Figure 54) is realized to be ready for testing electronically. Process development and characterization studies for e-beam lithography and DRIE etching processes are completed as well. A curious reader is encouraged to visit [88] to investigate the process development of each step of the silicon nanowire array fabrication.

Having BOX as an insulator layer between device and handle silicon layers is essential to preserve electrical control of the nanowire system. If a silicon test wafer is used, upon applying potential difference to both ends of the nanowires, it is expected to measure parasitic current flowing through all gates which we must model and consider for a reliable characterization, eventually. This problem can be studied with a carefully and deeply investigated electrical modeling of whole test chip/wafer. A descriptive test to identify how doping profile changes through whole chip / wafer thickness must be performed. Then electrical model should be considered accordingly. Even with these suggestions, a successful analysis might not be accomplished. Thanks to SOI wafer technology, such complicated modeling is not necessary.

Silicon nanowire arrays are subjected to indirect and direct four-point bending tests for electromechanical characterization. Experimental setup and electromechanical test results

are evaluated and presented in the upcoming sections.

3.2. Indirect Four-Point Bending Setup and Procedure

Different approaches for electromechanical characterization of piezoresistive silicon nanowires are introduced at "Introduction" chapter. Among various techniques, four-point bending mechanism is chosen for tests due to its applicability to our samples. There are two ways of realizing the test: a) indirect approach and b) direct approach. Indirect and direct bending approach is described as schematic in Figure 55 and in 3D in Figure 56.

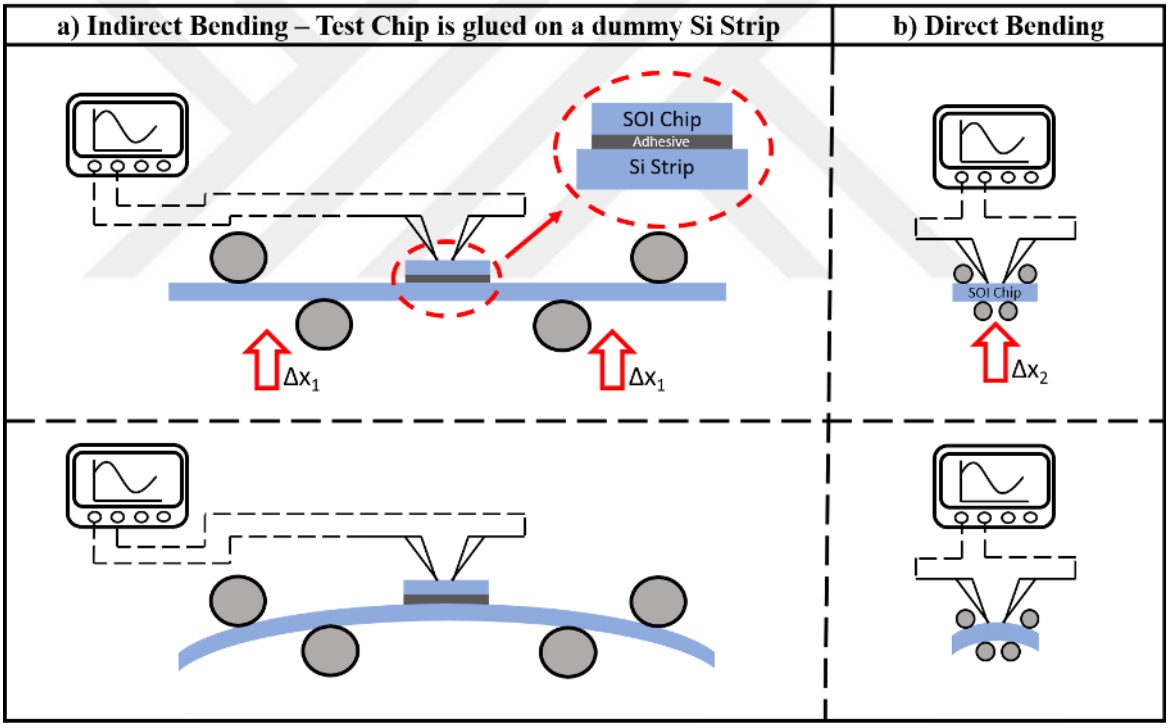


Figure 55: Bending methodologies used for the piezoresistivity characterization of silicon nanowire: a) indirect bending and b) direct bending.

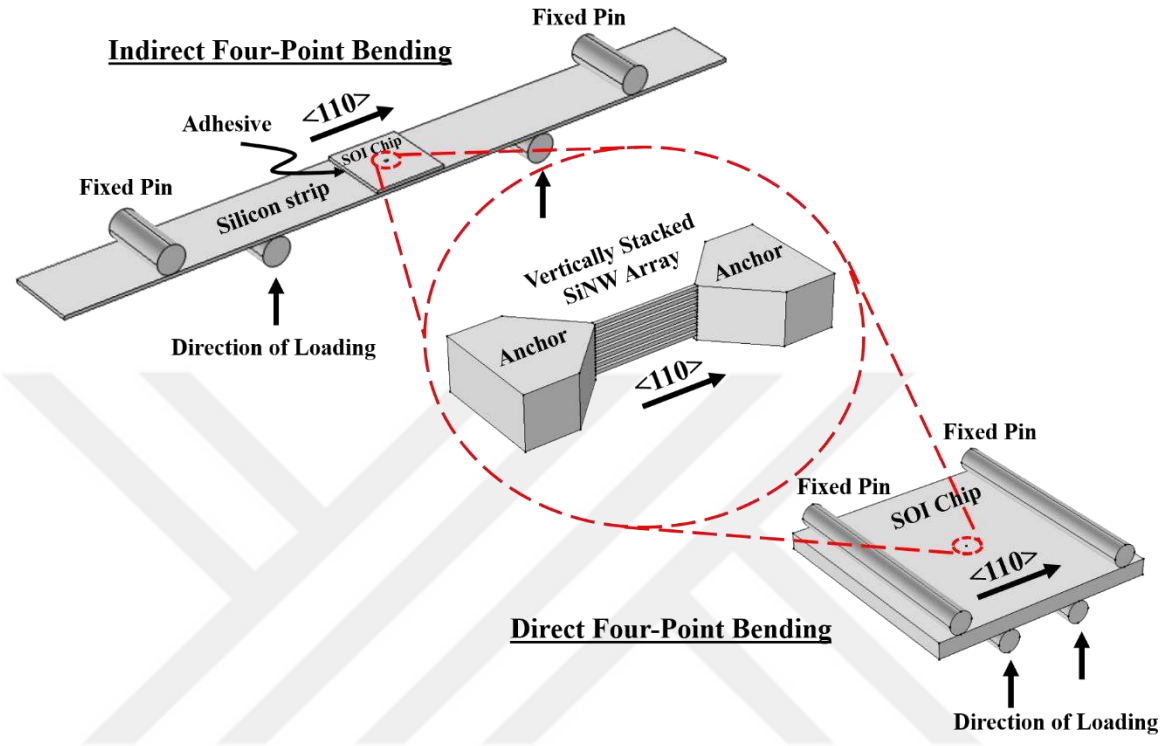


Figure 56: 3D details of utilized bending approaches in this dissertation: Indirect and direct four-point bending.

Indirect approach is based on using an adhesive material which is used to glue the sample chip onto a longer material. Upon adhesion, conventional four-point bending test is applied to achieve compressive and/or tensile load on the SiNWs. Indirect bending introduces extra challenges while evaluating the test results such as adhesive material characterization and engineering strain acquisition. Although adhesive material properties can be extracted from a data sheet, each test has its own characteristics. Nevertheless, test related identification is a necessary step to understand the success of the experiments. To realize that, in the literature, different methods are utilized. In a study, curvature of the bended silicon is measured, and analytical calculations are considered to estimate engineering strain values [73]. Other studies report the use of additional strain gauge and consider the readout strain as the actual engineering strain [45], [89]. In our indirect bending approach, we used 3D simulation-based results for engineering strain estimation. Starting from assuming a perfect binding state, until a very soft adhesive layer stiffness, simulations are performed, respectively. Simulation

results and experimental performance are presented in the later subsections. The effect of using an adhesive layer at four-point bending test is compared and discussed as well.

Conventional four-point bending methodology (Figure 57) involves two outer and two inner loading pins that exert bending moment on the specimen. Placing the specimen in the middle and taking account of the neutral axis of the system, application of tensile or compressive forces on the specific parts is achievable. (Figure 58). The advantage of four-point bending test is that a larger portion of the specimen between two inner loading pins is subjected to a constant bending moment. In addition, there is no shear force generation in the area between two loading pins. Therefore, this test is more suitable for brittle materials that cannot withstand shear stresses very well. Consequently, transferring tensile and/or compressive forces on the silicon nanowires, will provide current change during I-V measurements to evaluate piezoresistive effect.

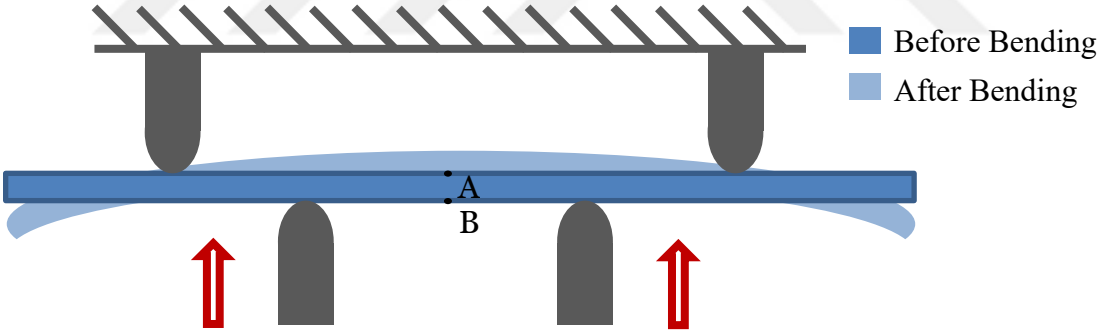


Figure 57: A typical four-point bending schematic.

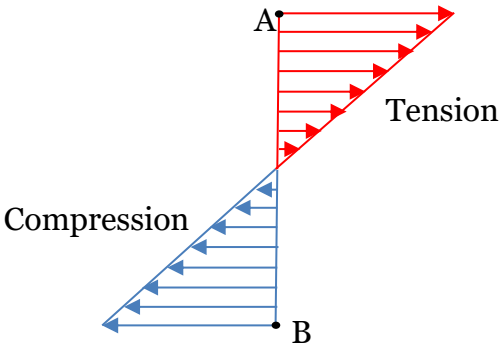


Figure 58: Stress distribution on points And B shown in Figure 57.

Our indirect four-point bending setup (Figure 59) consists of four aluminum loading pins and a silicon strip 80mm in length, 12mm in width and 530µm in thickness. Silicon strip is scribed out of a 4-inch single crystal silicon (SCS) test wafer. Silicon-on-insulator (SOI) chip is glued with JB Weld, which is described later in this section, onto the middle of the silicon strip. Upper two aluminum pins are fixed by a frame and lower two pins are left to move freely upwards and downwards. There is a special xyz stage attached to the lower pins of the bending system. The stage is M-562-XYZ ULTRAlign precision metric linear stage which features stainless steel construction for superior long-term stability. Having multiple M6 hole patterns provide convenient mounting options to the user. The precision-manufactured bearing reference surfaces provide linear 13mm travel range. For operations on z-direction we utilize an extra piezo equipment which can be mounted on the xyz stage. Piezo equipment provides more than 10mm moving range manually. In our tests, we used only 1.25mm predetermined displacement as a safe limit on z-direction. We observed that upon displacing more than 1.75mm, SCS strip is broken multiple times.

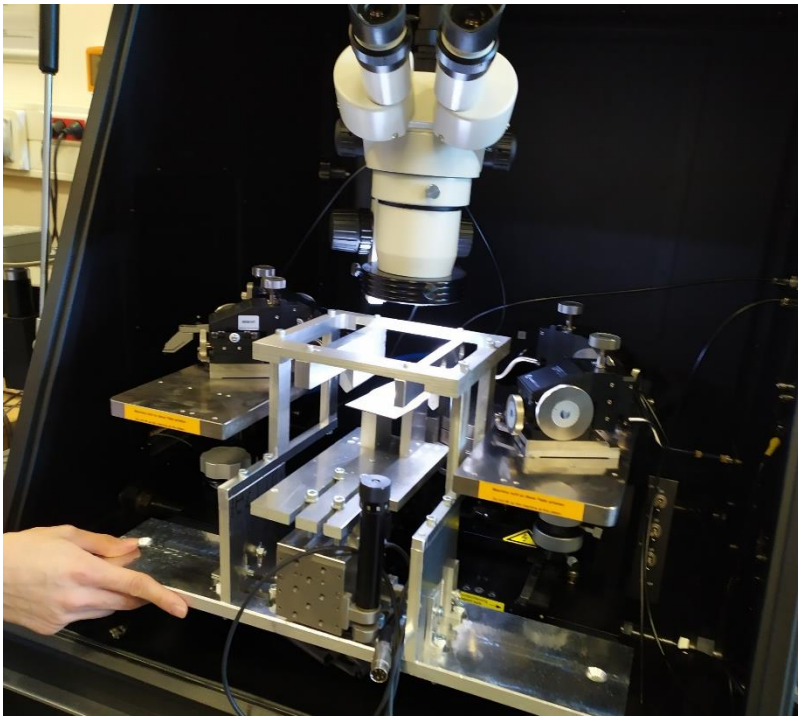


Figure 59: Experimental setup consisting of aluminum pins, XYZ stage, and probe station.

The dimensions of the tested SOI chips are 10mm x 10mm x 727µm. The adhesive material utilized in this test procedure is JB Weld which is a commercially well-known two-part epoxy system. It provides strong, lasting repairs to multiple surfaces and creates a bond stronger than steel. It is a widely utilized adhesive repair material for automotive, marine, craft repair and many more industrial areas. We previously tested commercially available different epoxy-based adhesives for their binding quality to silicon. JB Weld is preferred because of its high strength applications as a reference. Other adhesive products peeled off during tests as well.

JB Weld two-part epoxy system is prepared with a ratio of 1:1. It is mixed until having a uniform "grey" color before applying to the silicon surface. Adhesive mixture is applied onto the silicon strip surface and then, SOI chip is placed on it carefully. The thickness of the adhesive is around 1mm. When such adhesives are applied on metal surfaces in the industry, using a clamping tool is suggested during the curing to have a perfect binding. However, having SOI chip as the main part, it is impossible to use a clamper so that we left the samples as they are until JB Weld cured in room temperature. The curing time is 24-48 hours according to the humidity and temperature of the room. After curing is completed, sample is subjected to the indirect four-point bending test by pursuing the procedure in Appendix D.

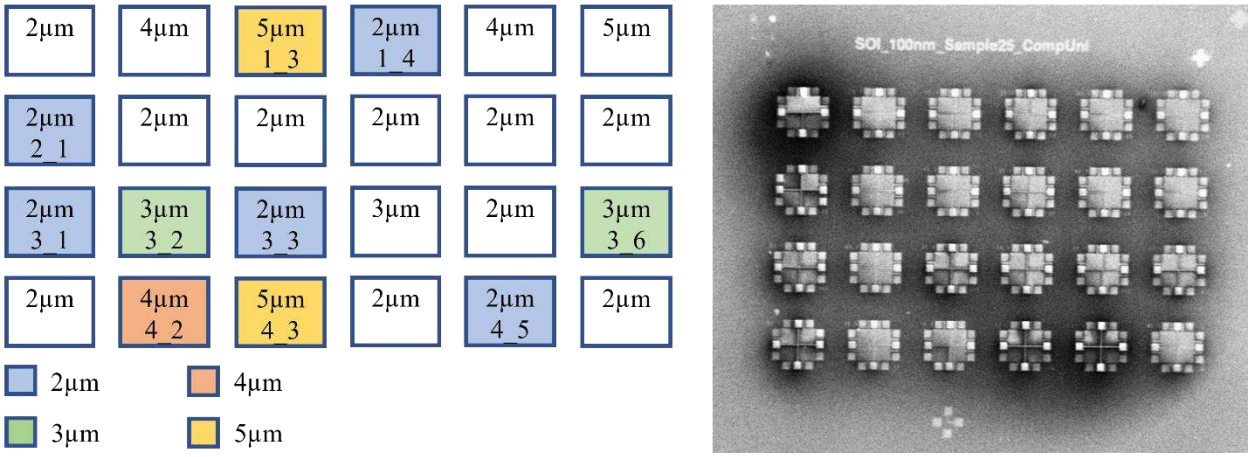
Following the procedure, continuous stress relief on the chip-strip system and re-straining is aimed to protect chip-strip system. Therefore, upon each straining step, a relief step is followed.

In this experimental setup, wire bonding is not used. Wire bonding is the method of making interconnections between an integrated circuit (IC) or other semiconductor device and its packaging during semiconductor device fabrication. Wire bonding is considered as a cost-effective and flexible interconnect technology. Frequently used bond wires are aluminum, copper, silver, and gold wires, while gold and aluminum pads are preferred as the bonding pads. For a better connectivity minimum thickness of a few hundreds of nanometers for metal bonding pads is requested. In this project, platinum (Pt) is used as touch-pad material and

thickness is set to 50nm with a 5nm Chromium (Cr) coating underneath. Cr is used to provide stronger adhesion between Pt and Si. At least 200nm metal thickness is usually requested for wirebonding. Since Pt metal thickness is quite thinner in our chips, wire bonding operation becomes a challenge, so that electrical characterization is conducted without wire bonding. Each time after running a bending step, probe tip needles which are connected to Semiconductor Parameter Analyzer are contacted directly to touch-pads. We also tried and studied silver paste as an in-house alternative for wire bonding. The methodology and results of silver paste application is presented in Appendix A.

3.3. I-V Measurements During Indirect Bending Tests

I-V measurements of double clamped, vertical piezoresistive silicon nanowire array is conducted at Mechanical Characterization Laboratory in Koç University, Istanbul, Turkey. Probe station equipped with micro-manipulators and tungsten needles, and Agilent B1500A Semiconductor Parameter Analyzer is used to get the direct measurement data. Applied potential difference between SiNW touchpads is swept from 0V to 100mV.



(a) (b)

Figure 60: (a) successfully electrical measurements performed samples on chip, different colors are used to group SiNWs with respect to their lengths, (b) SEM micrograph of tested SOI chip.

Tested SiNW arrays can be classified into four groups due to their different lengths: 2µm, 3µm, 4µm and 5µm. Figure 60(a) shows the successfully tested devices (a device is composed of a SiNW array, metallic signal lines and electrode gates) in an SOI chip (Figure 60(b)). Rest of the devices unfortunately do not provide a reliable current reading due to having silicon membrane underneath, a phenomenon detailly explained in Chapter 2, and/or absence of SiNW due to over etching of silicon. One identical measurement result for each SiNW length is introduced in this section.

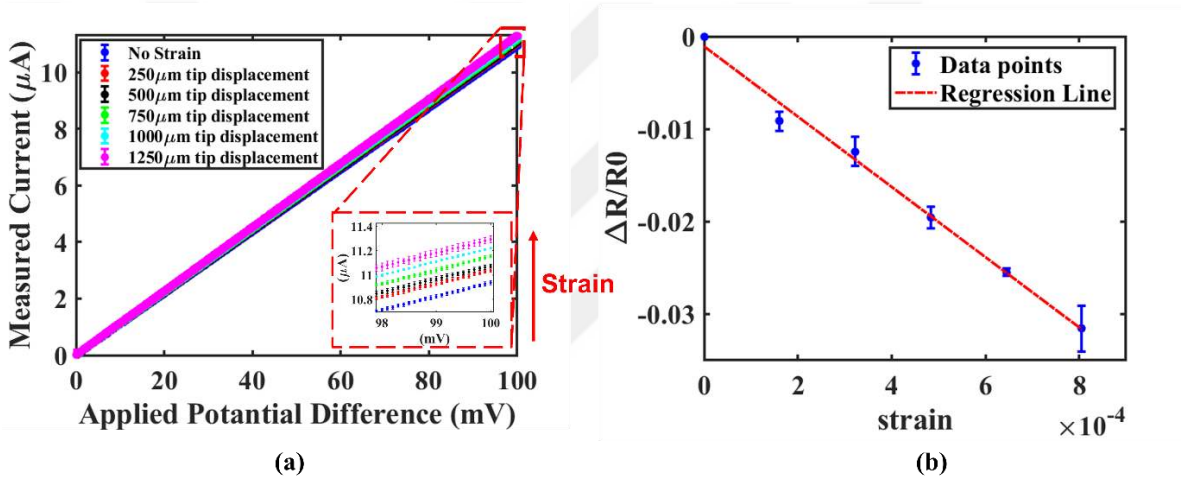


Figure 61: (a) I-V measurement during discrete steps of four-point bending prescribed pin displacement (0-250µm-500µm-750µm-1000µm-1250µm), Sample 1_3, SiNW dimensions: w:70nm, t:70nm, L: 5µm, (b) Average current plot for applied potential difference.

Figure 61(a) demonstrates I-V measurements between 0V and 100mV for the sample 1_3 located in Chip#25. SiNWs have 70nm-width, 70nm-thickness and 5µm-length. Two devices having 5µm-length SiNW array are successfully characterized. Increase in readout current due to bending is observed as anticipated. The measured current change from initial point to 1250µm fixed pin displacement is 3.20%. Each measurement is repeated five times in dark to eliminate light induced effects while the sample is hold as bended. We notice a slight shift during repeated measurements. The resultant engineering strain – rate in resistance change data is shown in Figure 61(b). The effective gauge factor calculated for this device is -37.94.

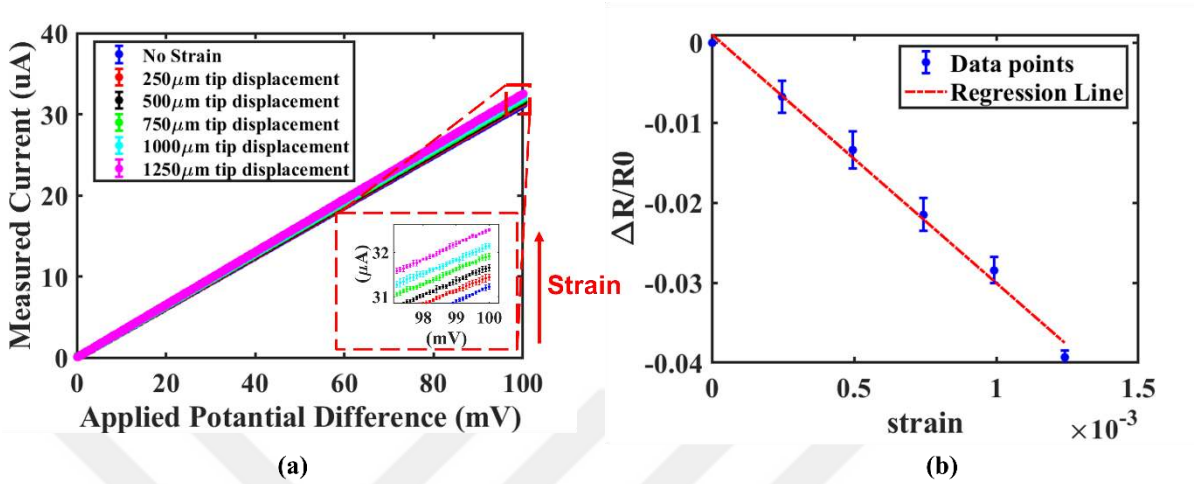


Figure 62: (a) I-V measurement during discrete steps of four-point bending prescribed pin displacement (0-250µm-500µm-750µm-1000µm), Sample 2_1, SiNW dimensions: w:70nm, t:70nm, L: 2µm, (b) Average current plot for applied potential difference.

Same bending procedure is repeated for sample 2_1 having 2µm-length in the same SOI chip. Five devices having 2µm-length SiNWs are successfully bended and I-V characteristics are obtained. In Figure 62(a), repeated I-V measurements for bending steps are in accordance with each other. The measured current change between zero to 1250µm fixed pin displacement is 3.52%. -31.07 is obtained as the effective gauge factor of this device.

Two devices having 3µm-length showed the least performance in terms of current change among all devices. The current change after 1250µm pin displacement is measured as 1.63% for Sample 3_6 and 1.74% for Sample 3_2. Measurement data for Sample 3_2 is given in Figure 63(a) and $\frac{\Delta R}{R_0}$ for applied engineering strain is provided in Figure 63(b). The effective gauge factor calculated for this device is -16.04.

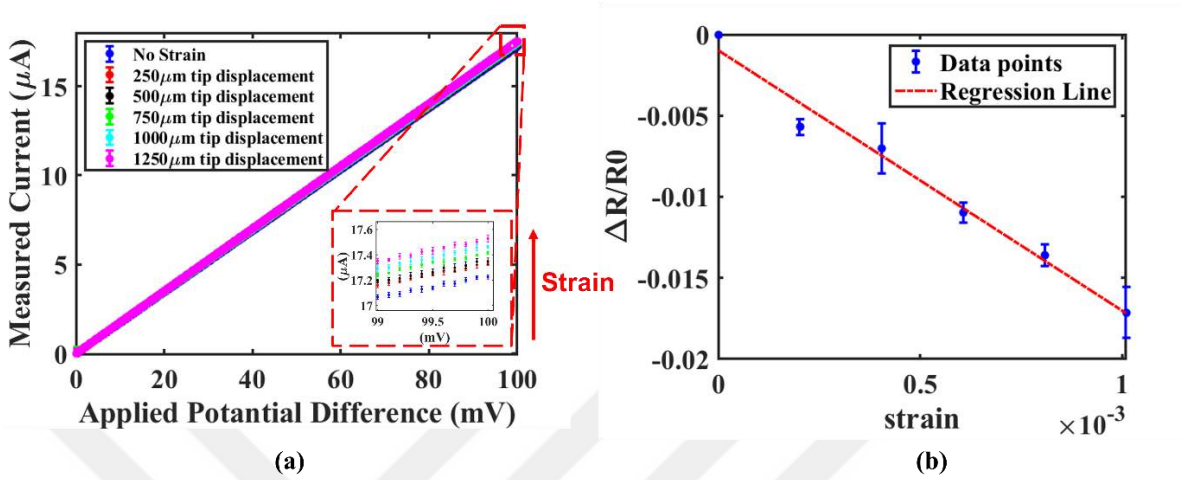


Figure 63: (a) I-V measurement during discrete steps of four-point bending prescribed pin displacement (0-250µm-500µm-750µm-1000µm-1250µm), Sample 3_2, SiNW dimensions: w:70nm, t:70nm, L: 3µm, (b) Average current plot for applied potential difference.

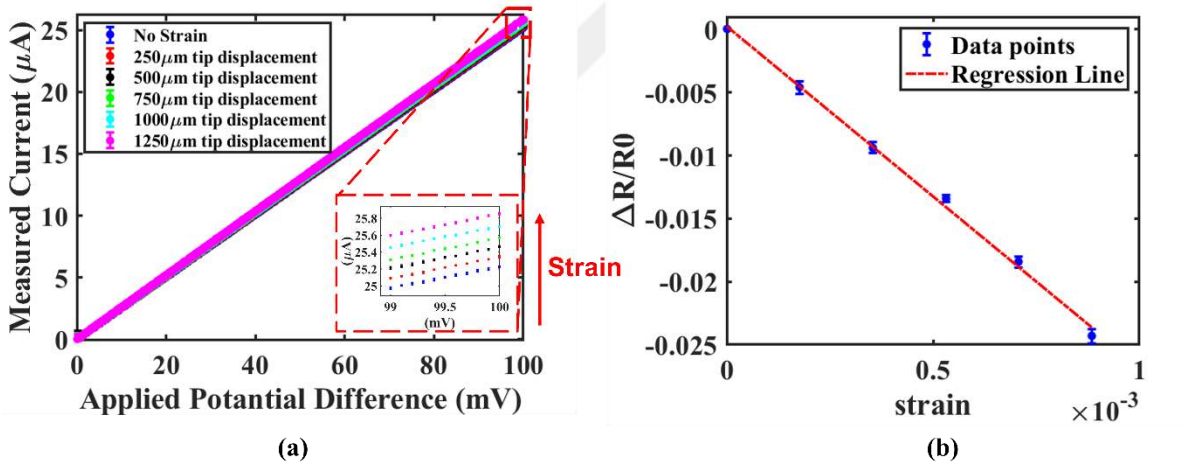


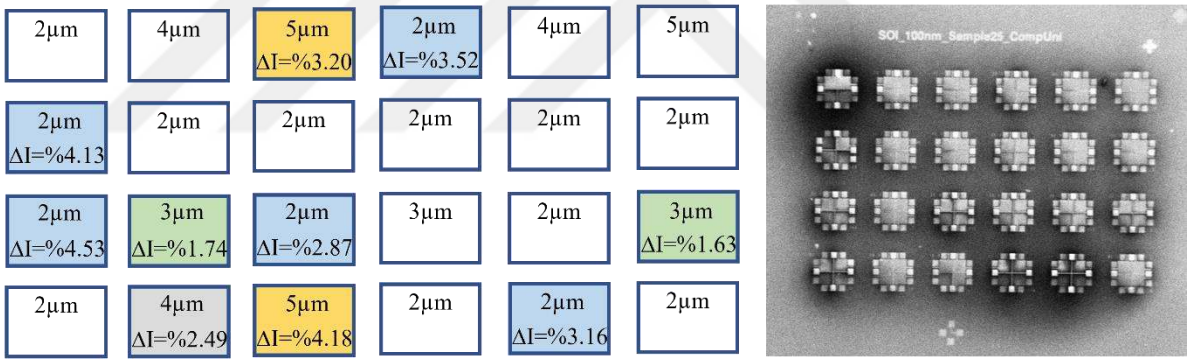
Figure 64: (a) I-V measurement during discrete steps of four-point bending prescribed pin displacement (0-250µm-500µm-750µm-1000µm-1250µm), Sample 4_2, SiNW dimensions: w:70nm, t:70nm, L: 4µm, (b) Average current plot for applied potential difference.

Only one device having 4µm-length SiNW array could be successfully I-V characterized. The maximum current change is measured as 2.49% which is in accordance with the average of other devices (Figure 64(a)). The effective gauge factor calculated due to Figure 64(b) is -26.98. Ten (10) devices in total are successfully tested with indirect four-point bending test approach. All devices demonstrated piezoresistive response due to bending as expected. Current change due to indirect test is summarized in Table 7 for all successfully tested

devices. It is possible to realize the results for device positions in the chip (Figure 65).

Table 7: Measured Current Change for Tested Devices

SiNW Length	Device Name	Current Change	SiNW Length	Device Name	Current Change
2 µm	1_4	3.52%	3 µm	3_2	1.74%
2 µm	2_1	4.13%	3 µm	3_6	1.63%
2 µm	3_1	4.53%	4 µm	4_2	2.49%
2 µm	3_3	2.87%	5 µm	1_3	3.20%
2 µm	4_5	3.16%	5 µm	4_3	4.18%



(a) (b)

Figure 65: (a) Current change at successfully electrical measurements performed samples on chip, different colors are used to group SiNWs with respect to their lengths, (b) SEM micrograph of tested SOI chip.

3.4. Simulations for Indirect Four-Point Bending Test

Simulations for indirect four-point bending tests are completed on COMSOL Multiphysics environment. Mechanical behavior of the setup, Si nanowire array and adhesive material behavior are deeply investigated for different cases. "Structural Mechanics Module" and "Stationary Analysis" metrology is adopted to simulate mechanical response of the system. 3D analysis (Figure 66) is preferred to eliminate plain stress/strain discussion which is a commonly encountered phenomenon in 2D. Presence of SiNW array as an order of magnitude-thin domain violates the assumptions based on both plane stress and plane strain for 2D. Even "change thickness" option is available and widely used, result may vary. We

simulated only one SiNW array each time, rather than drawing twenty-four devices in an SOI chip, which is the main simplification we apply to reduce the mesh element amount.

Considering the four pressure pins on the test setup, contact surfaces are critical elements of the simulation. Line contacts are defined to the model as moving and fixed pins. Additionally, introducing an adhesive layer, which is already present in the actual test sample, is another noteworthy step. JB Weld is applied as the adhesive material and as anticipated it has lower mechanical properties than Silicon. Even the binding quality should be questioned since it changes the effective stiffness. Consequently, the most crucial section of the test setup is adhesive layer which interconnects SOI chip and Si strip. In an ideal condition, we expect to have rigid structure which does not absorb the force exerted on the system. By nature of the four-point bending test, applied force should be transferred completely or as much as possible to the Si nanowire specimen. Having the Si nanowire strained, current change under a certain amount of potential difference is measured, respectively. Eventually, piezoresistive response of the nanowire array is observed and gauge factor is calculated. For our study, SiNW array engineering strain is extracted from the simulations and current values are obtained from the experiments. In such manner, if adhesive layer absorbs the energy (low stiffness case), engineering strain will be low and calculated gauge factor will be high. If it successfully transfers the tensile force to the specimen (high stiffness case), calculated gauge factor will be lower. Gauge factor plots will be introduced and discussed after this section.

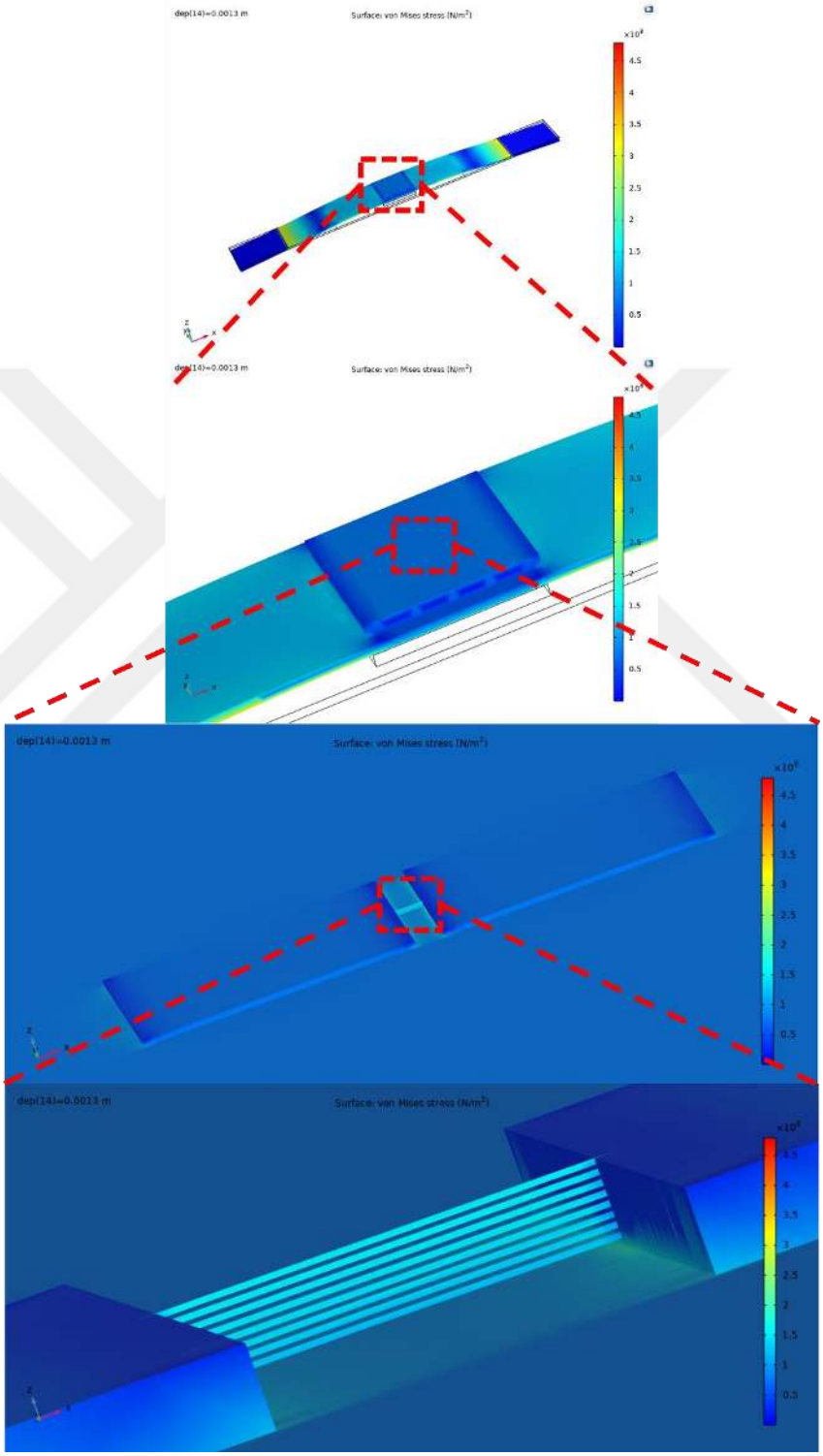


Figure 66: 3D simulations showing silicon strip, SOI chip and SiNW array.

Due to bending, elongation of each SiNW in a vertical array is different. Figure 67 shows each SiNW engineering strain of 2µm-length SiNW array. Perfect binding between SOI chip and silicon strip is assumed. The average SiNW engineering strain for 1250µm pin displacement is 0.125%. On the other hand, changing the effective adhesive layer stiffness to 10^{10} N/(m.m^2), which makes

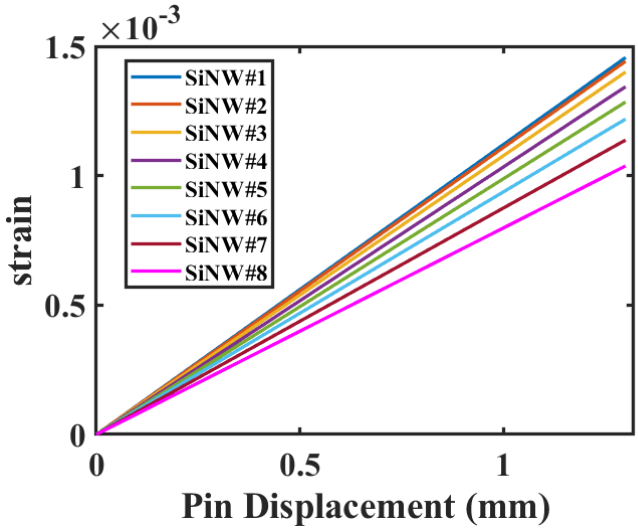


Figure 67: Engineering strain of each SiNW in array, length: 2µm, 3D simulation. Perfectly bonded.

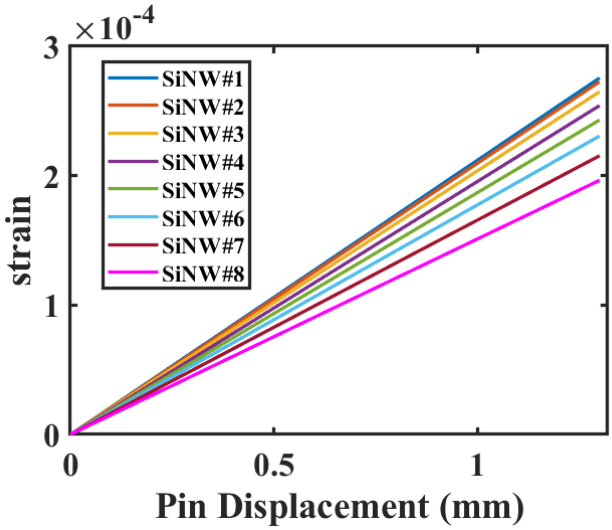


Figure 68: Engineering strain of each SiNW in array, length: 2µm, 3D simulation. 10^{10} N/(m.m^2).

the binding quite softer, decreases the engineering strain almost five times to 0.0235% (Figure 68). An average engineering strain for all SiNWs is obtained from the simulations to calculate effective gauge factor. Average engineering strain values are calculated for

adhesive layer stiffness between 10^{10} N/(m.m^2) and 10^{15} N/(m.m^2). Since the alignment of the test sample is completed manually, we also assume a 1mm shift as disturbance in the positioning. More simulations are performed to analyze the shift effect, respectively. Figure 69 demonstrates the data for 2µm-length SiNW array. Both middle and 1mm shifted positioning of the SOI chip is studied. Simulations for all SiNW lengths from 2µm to 5µm reveal that the effect of chip misalignment for 1mm is negligible.

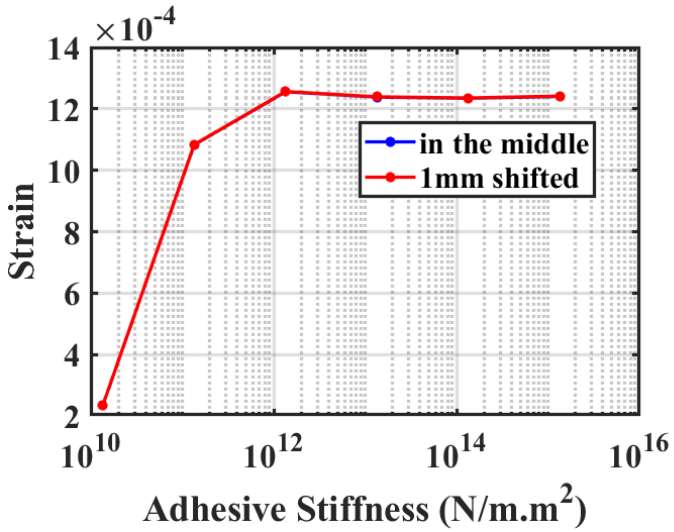


Figure 69: Average engineering strain results for the cases of SOI chip location: blue: in the middle, red: 1mm shifted.

3.5. Digital Image Correlation (DIC)

Digital Image Correlation (DIC) is a non-contact and precise method used for measuring the displacement and/or deformation of a structural material subjected to external loading. The idea is based on the principles of rigid body mechanics. The system consists mainly of a camera and specialized computer software. A camera/cameras is/are used to capture images of the surface of a tested material before and during the deformation period. The obtained digital image data (a number of photos) is analyzed by the software. The mathematical correlation analysis is applied. Finally, a set of displacement/deformation mapping for the entire specimen surface is created.

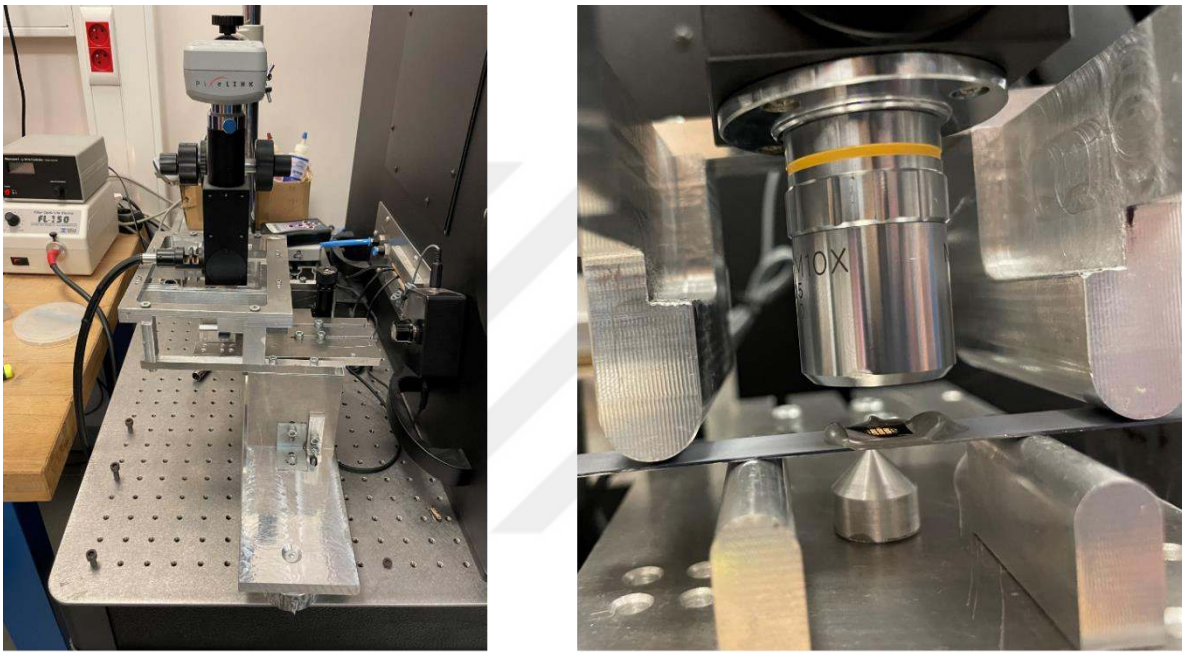
This technique starts with a reference image (before loading) followed by a series of images taken during the deformation. Images can be captured in an outer place with a camera or in

an SEM/TEM environment. Different dot patterns occur during deformation relative to the initial reference image. These pattern differences can be calculated by performing correlation of the pixels of the reference image and any deformed image. Presence of camera in the methodology differs DIC from other experimental techniques [90]. The user can obtain the engineering strain distribution by applying mathematical relations on the displacement field. To achieve this, various patterns like dots, grids, and lines are generated on the sample surface. The resolution of the camera and quality of pattern on the sample are the main factors affecting the quality of the results.

Users can find many commercially available software to analyze. However, as stated in [91] there is an absolute need of a modern and accessible DIC code. Therefore, Ncorr is developed as an opensource and freely available 2D digital image correlation software. Ncorr provides a well-documented flexible code to the users so that it can fit to user needs. The package is implemented in Matlab, which also makes the software preferable to engineer and researcher community [91]. Ncorr, consequently, is a viable measurement tool as compared to the high-end equipment and postprocessing software [90]. We employed a Matlab based script to our experiments to analyze displacement and engineering strain field of our SOI chips during consecutive bending steps.

DIC camera setup is presented in Figure 70. Simply, four-point bending setup is placed under a camera. Bending procedure is repeated for each 250µm fixed pin displacement until 1250µm. At the end of each step, camera is manually focused, and images are captured via PixeLINK Capture software. 10x lens is preferred for the magnification. Before using the camera setup shown in Figure 70, the images taken from the probe station camera in Figure 71 were used to evaluate the engineering strain field. However, the image quality is unfortunately very low and noisy. Although, the visual image is very clear in the probe station microscope, it cannot be transferred to the screen in high quality because of light noise and cabling. All intermediate bending step images for 0µm, 250µm, 500µm, 750µm, 1000µm, and 1250µm are obtained under the microscope. Images are captured via HDMI video capture card which is commercially available in the market and OBS Studio which is freely

available on the internet. DIC analysis is performed for these images to evaluate the engineering strain field. Unfortunately, the analysis did not provide reasonable results due to overwhelming noise. Therefore, we switched to the camera setup presented in Figure 70.



(a) (b)

Figure 70: DIC setup with a camera and four-point bending mechanism: (a) general view of the setup, (b) close view of the lens, bending pins and tested sample.

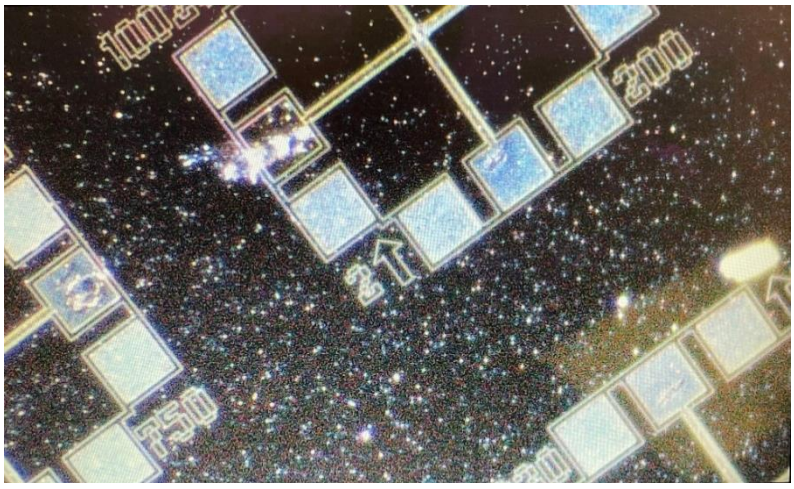


Figure 71: Image taken from probe station camera before bending at maximum magnification.

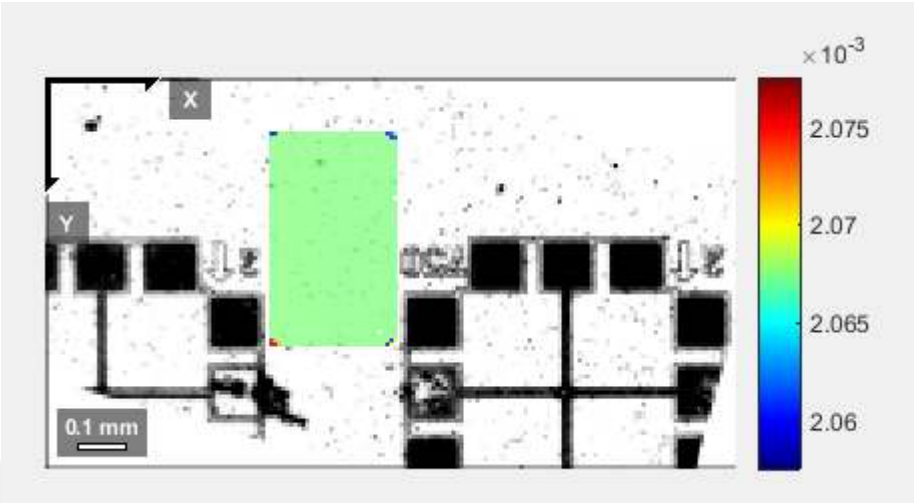


Figure 72: DIC analysis of the image captured from probe station camera. "x": nanowire direction.

Figure 72 shows the DIC analysis performed on the image taken via probe station camera. A large area is selected as the region of interest (ROI) which is green colored. Analysis is performed from 0 to 1250µm fixed pin displacement. Then the median of the resulting contour is taken as the average engineering strain. Figure 73 demonstrates the resulting median engineering strain for each step of four-point bending. DIC calculated 0.2% engineering strain for 1250µm displacement. This value is even higher than the simulation which we assume perfect binding condition occurred. In the Figure 73, "Step" is denoted for four-point bending steps meaning that "step = 0" is no strain, "step = 1" is 250µm pin displacement, "step = 2" is 500µm, "step = 3" is 750µm, "step = 4" is 1000µm and "step = 5" is 1250µm pin displacement. E_{xx} is the engineering strain notation along the SiNW which we seek for to perform gauge factor calculation. E_{yy} is the 90º rotated axis and E_{xy} is the shear component. Because of the four-point bending, silicon strip direction is parallel to the SiNW specimen, ideally, we expect E_{yy} and E_{xy} values to be near zero. However, especially E_{yy} value is on the same order with E_{xx} which we conclude that the noise between the images is high enough to prevent getting better results.

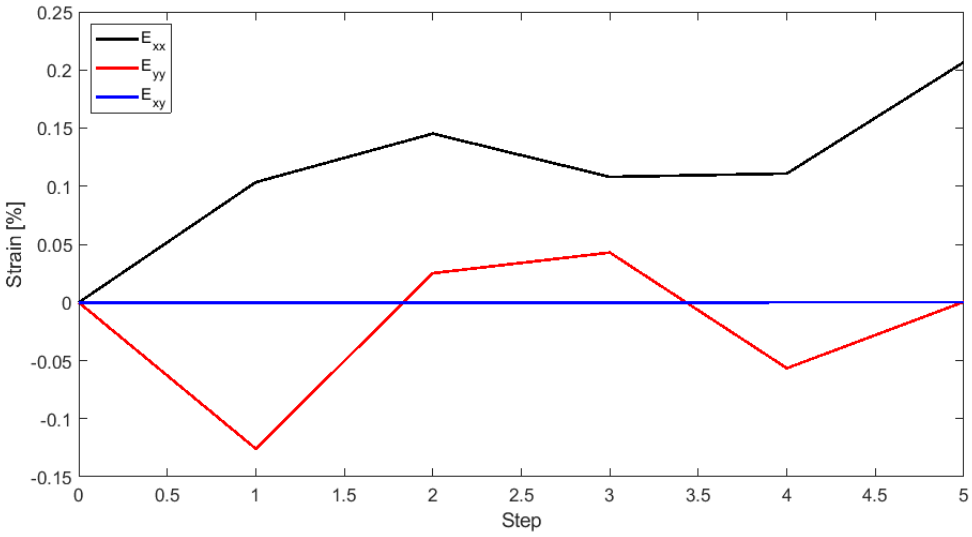


Figure 73: Median engineering strain of the selected ROI for each four-point bending step.

Upon switching to the camera setup in Figure 70, we obtained different images with 10x camera lens. The camera is less noisy but still do not offer black-white image. Black-white images offer better quality on reference point selection. New setup provides images with the color spectrum including greyish colors. We performed the analysis on different ROI selections to evaluate the effect of selection difference.

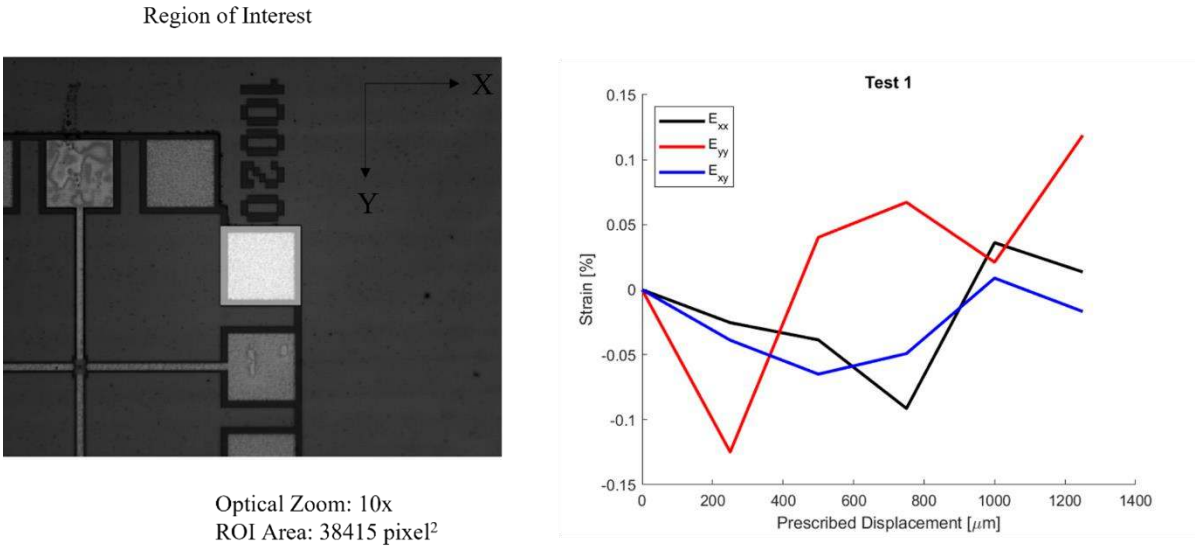


Figure 74: (a) Image taken from PixeLINK camera with 10x lens and selected ROI, (b) engineering strain obtained with DIC analysis for test 1. E_{yy} is the value of interest which is aligned in the SiNW direction.

Figure 74 demonstrates the selected area for DIC analysis during four-point bending experiment and the related analysis result. As it will be shown in other figures, we mostly performed DIC analysis on the Pt coated metal touch-pads. Metal touch-pads provide indented surface profile which enhances the analysis providing more reference points to track, respectively. E_{yy} is the interested engineering strain direction along SiNW array in the figure. 0.1% engineering strain on E_{yy} direction can be evaluated as better than probe station camera images but recalling the simulation results acquired previously, it is still less than the expected. In addition, E_{xx} and E_{xy} values E are considerably high indicating that the camera and DIC performance is still not on the desired level.

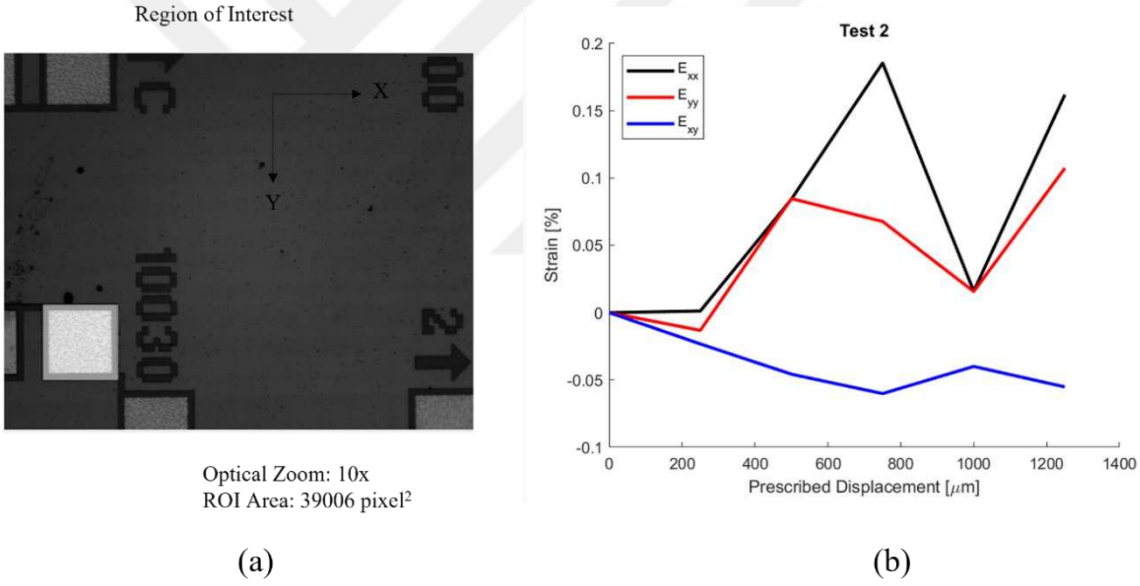


Figure 75: (a) Image taken from PixeLINK camera with 10x lens and selected ROI, (b) engineering strain obtained with DIC analysis for test 2.

Figure 75 demonstrates the selected ROI and DIC analysis results for test 2. Engineering strain on y-direction is still on the order of 0.1% as in test 1. E_{xx} is even higher than E_{yy} while E_{xy} is almost on the same order as in test 1. We also captured images with 5x lens to evaluate our tests. DIC, by definition, is a technique which requires many reference points to track. The aim is to understand if the results deviate from or converge to each other with images captured by different lenses. Keeping in mind that decreasing the lens magnification will also decrease the reference point size. Therefore, the number of pixels able to be tracked should be lowered as well. This might affect the analysis in a negative fashion.

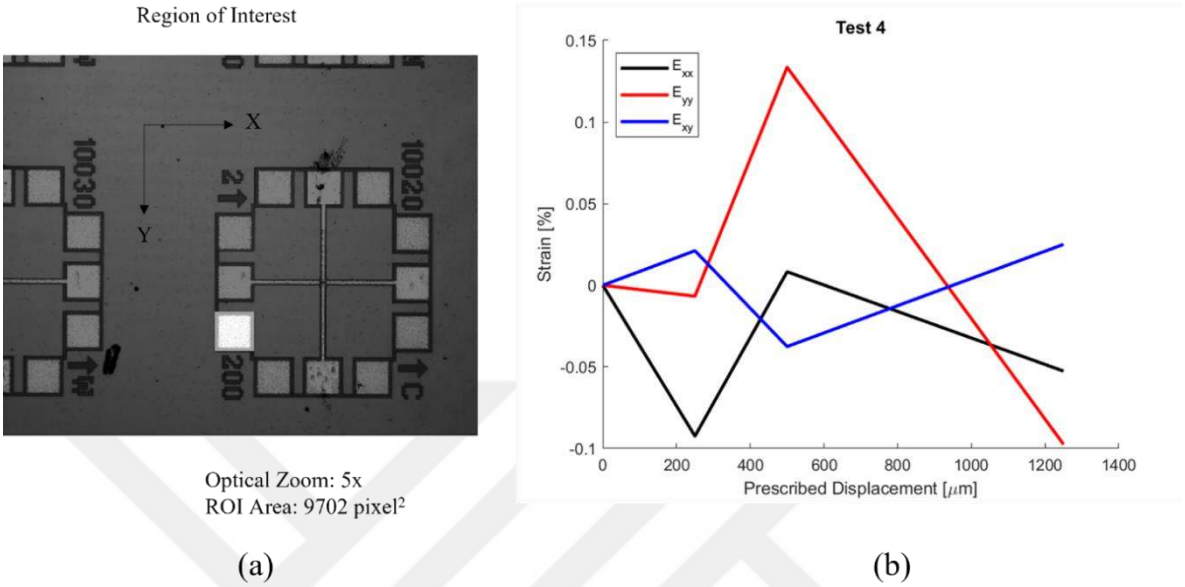


Figure 76: (a) Image taken from PixeLINK camera with 5x lens and selected ROI, (b) engineering strain obtained with DIC analysis for test 4.

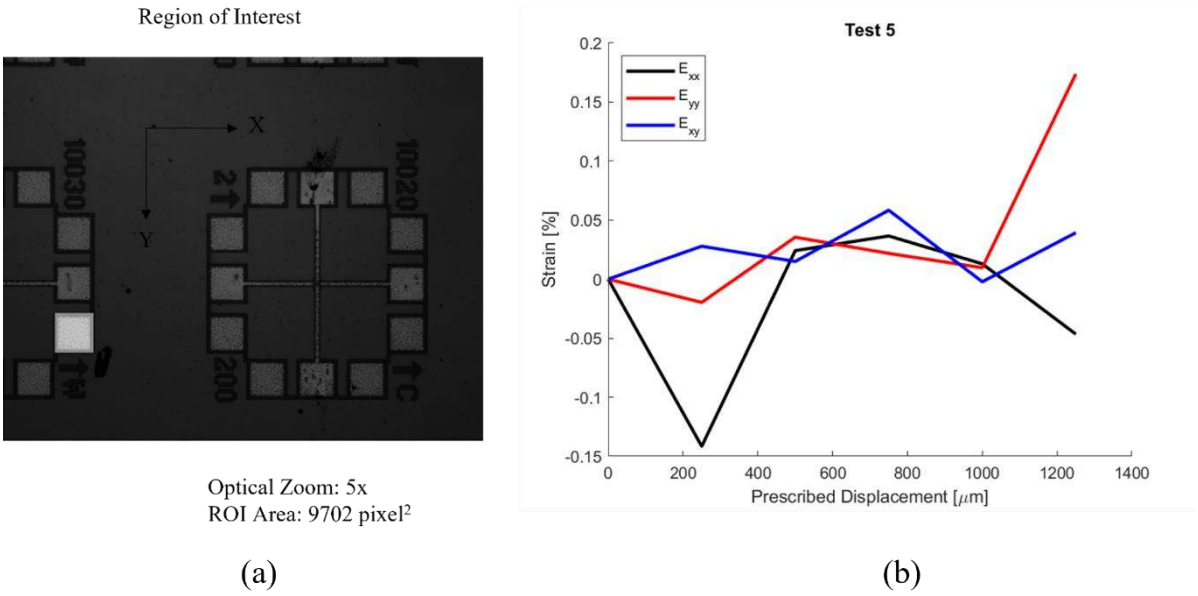
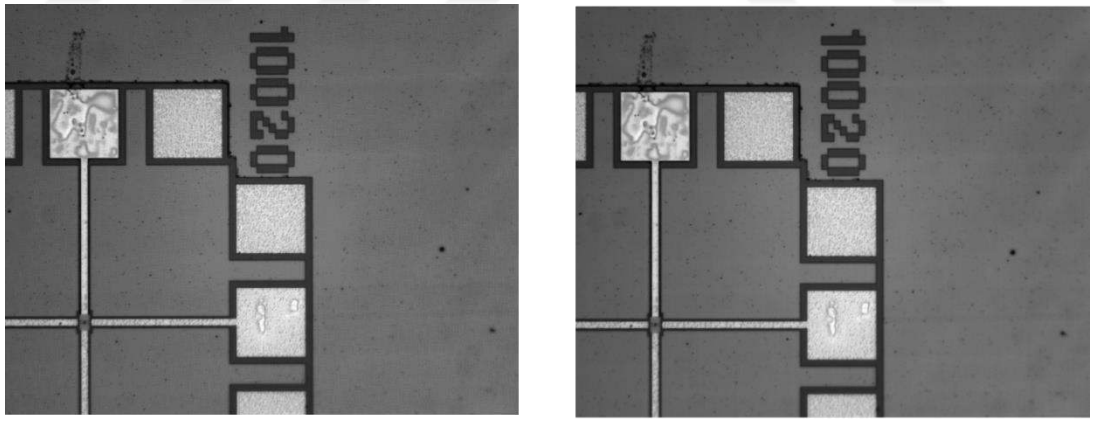


Figure 77: (a) Image taken from PixeLINK camera with 5x lens and selected ROI, (b) engineering strain obtained with DIC analysis for test 5.

Figure 76 and Figure 77 demonstrates images captured with 5x lens and DIC results for tests 4 and 5. Comparing DIC analyses for 5x and 10x lenses, we did not notice a remarkable change in the results. E_{yy}, E_{xx} and E_{xy} values are still in the same range. Increasing number

of pixels for a better analysis should be always preferred so that 10x would be a better option providing four times more pixels in the same ROI.

There is a crucial point which might be dominantly affecting the DIC results. We focus the microscope lens manually, before capturing digital images, so that slight errors can easily be made. By visual inspection, the image can be evaluated as smooth. However, there is always the possibility of losing the reference points for DIC even with slight focus deviation. To characterize the contribution of focus, we captured two images that have slight variation in focus. Three different image pairs are obtained and analyzed for a better insight. Figure 78 shows two images of same spot on the test specimen without any bending. Focus of Figure 78(a) and (b) are slightly deviated from each other. It is not easy to detect the difference between them with a naked eye. We performed DIC analysis between them by choosing the metal touchpad as ROI as in Figure 79, respectively.



(a) (b)

Figure 78: (a) Focused image with 10x lens (b) slightly deviated focus from (a)-Test 1.

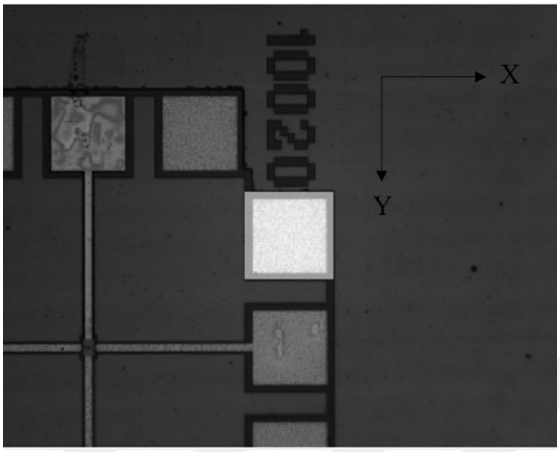


Figure 79: ROI selection for DIC analysis of Figure 78.

DIC analysis reveal that the focus deviation cannot be neglected and should be considered. Acquired engineering strain values for E_{xx}, E_{yy} and E_{xy} for all image pairs are tabulated in Table 8. It can be noted that the values are almost in the range of our four-point bending DIC analysis results. Consequently, DIC analysis is very sensitive to focus deviation. We can also note that focus variation can be evaluated as an operator caused noise on the measurements. Therefore, autofocusing camera / software, which unfortunately increases the cost of setup, can be used to obtain to eliminate such problem. In addition, for nanoscale measurements DIC analyses are mostly performed for the images taken in SEM and TEM. The focus quality in such machines and the focus loss between images are almost negligible compared to our setup. Moreover, our testing method is "out-of-plane" which always requires re-focusing on the specimen. Most of the studies utilizing DIC are "in-plane" and no-refocusing is required so that all captured images stay in the same focus quality.

Table 8: Engineering strain obtained from DIC analysis of Figure 78(a) and (b)

	ε_{xx}	ε_{yy}	ε_{xy}
Test 1	-8.8450e-04	-1.3378e-04	1.6569e-04
Test 2	-7.7691e-04	-5.4951e-04	4.0214e-04
Test 4	6.8036e-04	0.0023	-5.8742e-04

3.5.1. Gauge Factor of Indirectly Tested Devices

Gauge factor is a measure of piezoresistivity. As discussed in "Introduction", *giant* piezoresistivity effect was observed in silicon nanowires under different conditions. Our SOI chips are highly n-doped with a concentration of 10^{20}-10^{21}cm^{-3}. The conductivity is strongly enhanced and ohmic contact is provided rather than a Schottky contact.

Gauge factor is defined as the rate of resistance change with respect to the applied engineering strain. To calculate the gauge factor, resistance change and engineering strain values should be acquired. Since we conducted I-V measurements, resistance change is already obtained. However, engineering strain measurement is challenging. Recalling our group's previous work [44], we expect to be close to gauge factor values because of using similar fabrication methodology. We performed 3D simulations based on presence of adhesive layer and conducted DIC analyses. Detailed work is introduced in Simulations and DIC sections. Since DIC analyses did not provide a reliable solution on the order of 10^{-4} engineering strain as expected, we could not use that data to calculate a gauge factor number. However, DIC results still supports the low engineering strain expectancy. 3D simulation results are used to calculate gauge factor, as a consecutive approach. Based on perfect binding assumption, effective gauge factor is provided for 2µm, 3µm, 4µm, and 5µm-length SiNW arrays.

Figure 80 demonstrates the rate of resistance change for each applied engineering strain for successfully tested five 2µm-length SiNW arrays. Regression line is used to linearize gauge factor. A gauge factor value of -29.2±6.47 is obtained. Same calculation is applied on 3µm, 4µm and 5µm-length SiNW arrays as well. demonstrates gauge factor values for different device sets.

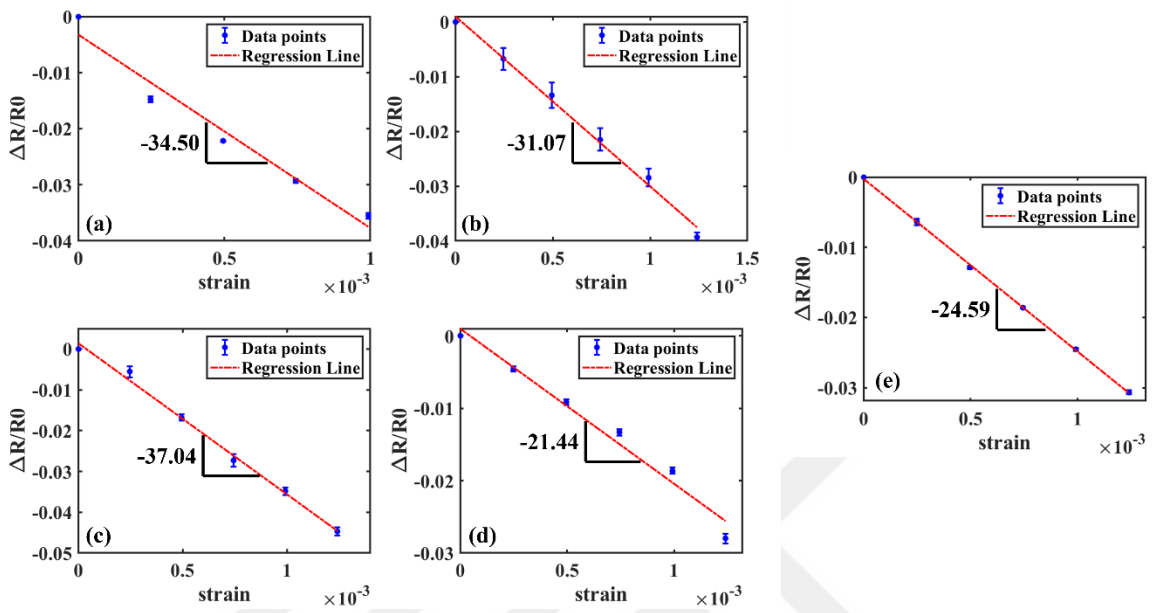


Figure 80: Engineering strain – rate of resistance change and gauge factor all of 2µm-length SiNW array indirectly tested, (a) device name: sample 1_4, (b) device name: sample 2_1, (c) device name: sample 3_1, (d) device name: sample 3_3 and (3) device name: sample 4_5.

Table 9: Gauge Factor of Indirectly Tested Devices

SiNW Array Length	Number of Devices	Gauge Factor
2µm	5	-29.85±6.61
3µm	2	-14.85±0.35
4µm	1	-27.4
5µm	2	-39±4.38

Overall performance of the devices characterized with indirect bending test is lower than expected. Almost 20% current change for 0.13% engineering strain was reported with a calculated gauge factor of 130-140 [44]. The doping type and concentration of the devices are n-type and almost 10^{21} cm^{-3}. Top-down fabrication approach developed by our group is employed to both studies. Therefore, relatively close results are anticipated. The main reason for such variation must be because of introducing an adhesive layer to the test system. Although we can provide different stiffness values for adhesive layer during 3D simulations, selection of correct value remains undetermined. Another setup for direct bending test is designed and manufactured to evaluate adhesive layer related error and inaccuracy.

3.6. Direct Four-Point Bending

The results and application procedure of "indirect" bending of SOI chip is described. The effect of glue as an adhesive layer is investigated. Although there are different methods applied to eliminate the adhesive layer effect such as use of LDV for curvature measurement and gluing strain gages near the test chip, the most suitable way to determine the results is applying "direct" four-point bending test on the DUT. Since our chips are quite small (10mmx10mm), manufacturing an appropriate setup including two inner pins which should be close enough to apply the test is challenging. Thanks to outstanding contributions of CNC milling machines in manufacturing facilities of DeltaV Space Technologies, we managed to manufacture direct four-point bending setup as demonstrated in Figure 81. Whole parts except the XYX stage is manufactured from Aluminum 6061.

M-562-XYZ ULTRAlign stage is used manually to perform bending steps. Probe station and Agilent B1500A Semiconductor Parameter Analyzer is utilized for the I-V measurements. Before bending test, each sample is controlled for current leakage between gates and anchors. Assured samples are subjected to bending test.

In the chip design, there are 24 devices distributed throughout the SOI chip (4 rows and 6 columns). Since the inner pins are just 3.5mm away from each other, only 8 devices in a chip (4 rows and 2 columns located in the middle of the chip) can be subjected to bending test. Rest of the devices are located out of inner pins so that bending application is not suitable for those devices. Wirebonding is not employed in these experiments.

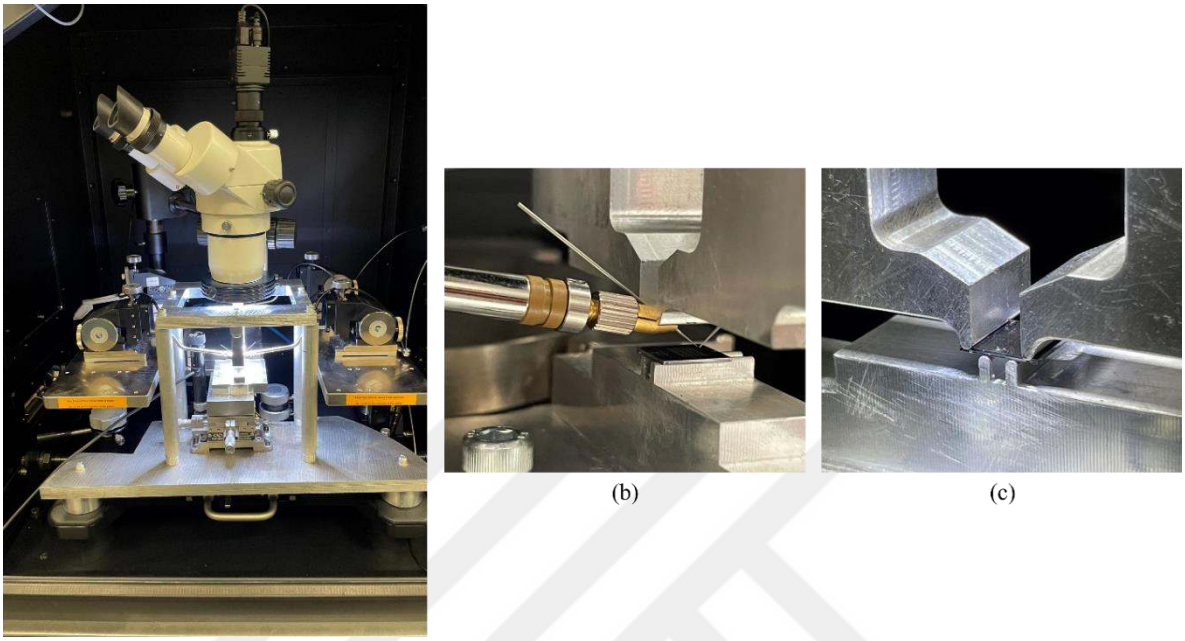


Figure 81: Direct four-point bending test setup (a) overall view, (b) premeasurements on the sample before testing and (c) close view of the pins bending the test chip.

Therefore, the use of probe station with tungsten needles and micromanipulators is mandatory. The procedure provided in Appendix D is applied.

Figure 82: Marks of outer pins where force is applied on the SOI chip. (a) right end, and (b) left end of the chip, captured via optical microscope.

Figure 82 shows the micrographs of outer pin traces for the direct bending setup. Prescribed displacement exerted on the inner pins, creates marks on SOI. They are easily noticed even

with naked eye. Such traces are expected to ensure the pins are contacting along the chip. Otherwise, torsional load will be applied, and results will be deviating. Direct bending has very limited range compared to indirect bending due to small chip dimensions. Test range for direct bending is set to 15µm (20µm for just one experiment), while this value is 1250µm for indirect bending. Even though we set safety limits as range, it is observed that SOI chip can physically fail (Figure 83).

Figure 83: Micrograph of the broken SOI chip at 20µm pin displacement.

3.7. Simulations for Direct Bending Test

Simulations are carried out in 3D by using COMSOL Multiphysics environment. Structural Mechanics module and Stationary solver is utilized. SOI chip width and length is drawn as 10mm x 10mm while thickness is set to 727µm in total including handle layer, BOX layer and device layer. One set of nanowire array including eight nanowires are modeled for meshing and solving simplicity (Figure 84). Nanowire array is placed 0.5mm away from the center as in the actual chip. Therefore, the bending results are obtained from shifted device, not from a centrally located device.

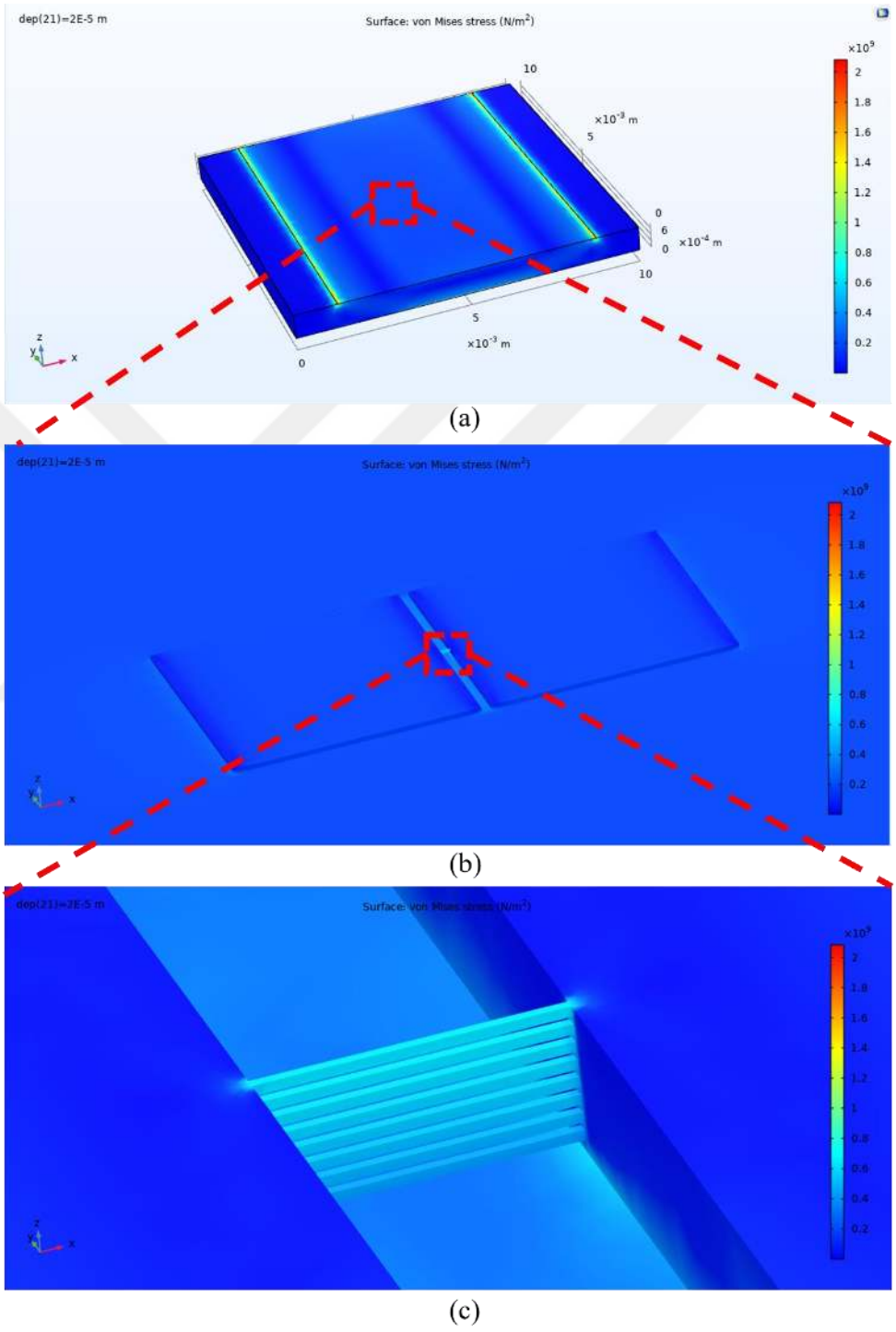


Figure 84: (a) SOI chip, (b) anchors and vertically stacked nanowires, (c) Si nanowire array close view.

Only 2µm-length nanowire arrays are subjected to direct four-point bending test so that 3D simulations are performed, accordingly. Engineering strain value for each SiNW is obtained

from the simulation and the average is taken. Corresponding SiNW engineering strain values are demonstrated in Figure 85 where nanowires are numbered between 1 and 8; nw1 is at the top and nw8 is at the bottom.

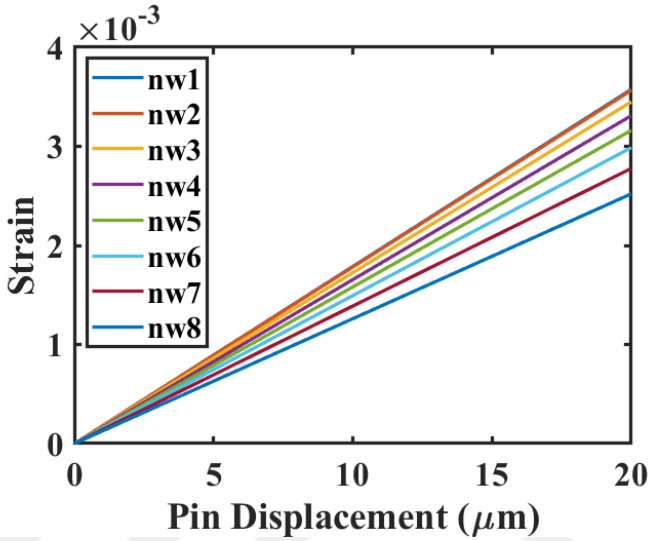


Figure 85: Engineering strain acquired from simulation for each vertically stacked silicon nanowire.

Five different devices are directly bended and I-V characteristics are recorded. Each sample is tested four times individually. Figure 86(a) demonstrates the averaged I-V data for device#1. Minimum achievable tip displacement is 5µm due to the capabilities of XYZ stage we used. Inner pins (movable in z-direction) are subjected to 5µm, 10µm and 15µm displacements, respectively. Red colored data indicates the current measurement for no-strain case and the rest correspond to the bended formation. A clear increase in readout current, almost 40%, is observable. Figure 86(b) demonstrates the rate of change in resistance for each applied engineering strain. Gauge factor of such experiment is calculated as -111.8 which is almost four times of what glued samples provided. Same sample, device #1, experienced the direct four-point bending experiment four times. The corresponding data plots are presented in Appendix. A slight increase in base current is observed each time, almost 0.1-0.3%. Gauge factors of the experiments are calculated as -111.8, -109.9, -110.9 and -110.4. The overall effective gauge factor for device#1 is -110.75±0.8.

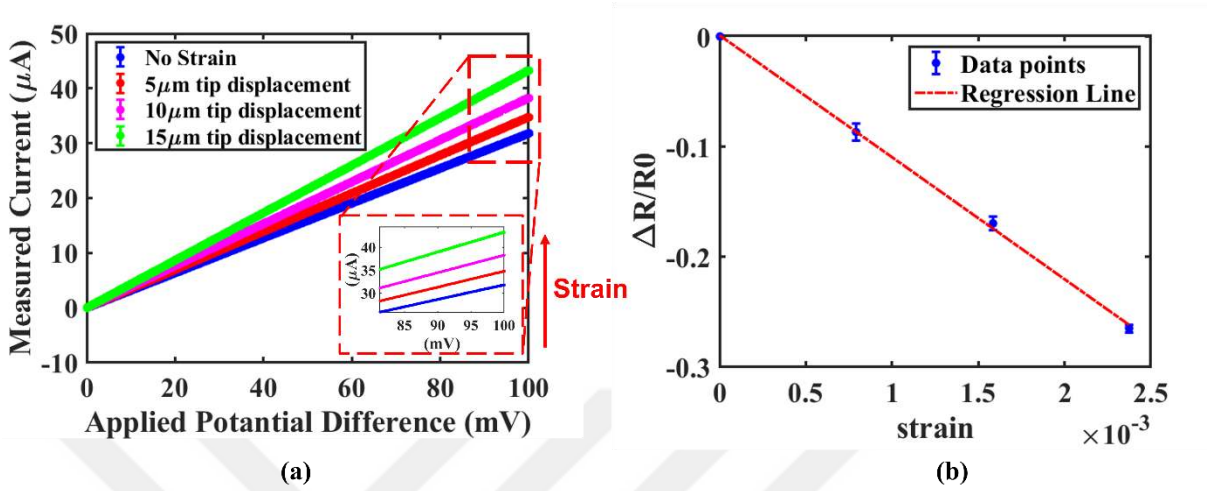


Figure 86: (a) Applied Potential Difference – Current for Each Pin Displacement, (b) Applied engineering strain (from 3D simulation) - $\Delta R/R_0$ (from I-V measurements) for device#1.

Device#2 showed a similar trend increase in readout current due to exerted engineering strain. Slightly lower current change (Figure 87(a)) and gauge factor (Figure 87(b)) is obtained. Upon completing the four experiments on device#2, good repeatability is observed. Calculated gauge factors are -99.1, -100.6, -99.6 and -98.1, respectively. The overall effective gauge factor for device#2 is -99.4±1.04.

Device#3 demonstrated the lowest performance among five devices. The gauge factors after four experiments are (Figure 88(b)): -98.3, -97.8, -96.3 and -93.1. Effective gauge factor is obtained as -96.4±2.34. Device#4 provided the highest the gauge factor values as -116.2, -115.5, -115.3 and -113.4 (Figure 89(b)), respectively. The effective gauge factor is calculated as -115.1±1.19.

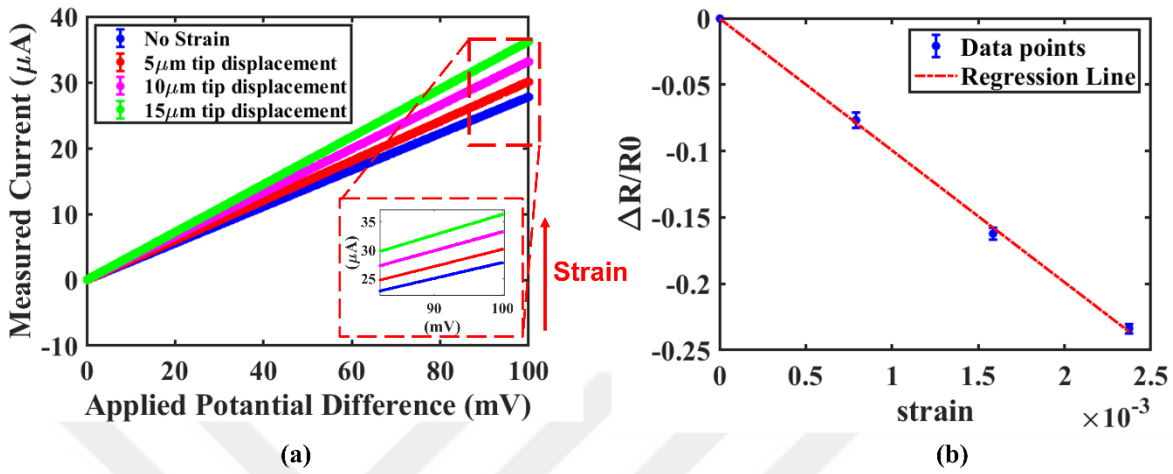


Figure 87: (a) Applied Potential Difference –Current for Each Pin Displacement, (b) Applied engineering strain (from 3D simulation) - $\Delta R/R_0$ (from I-V measurements) for device#2.

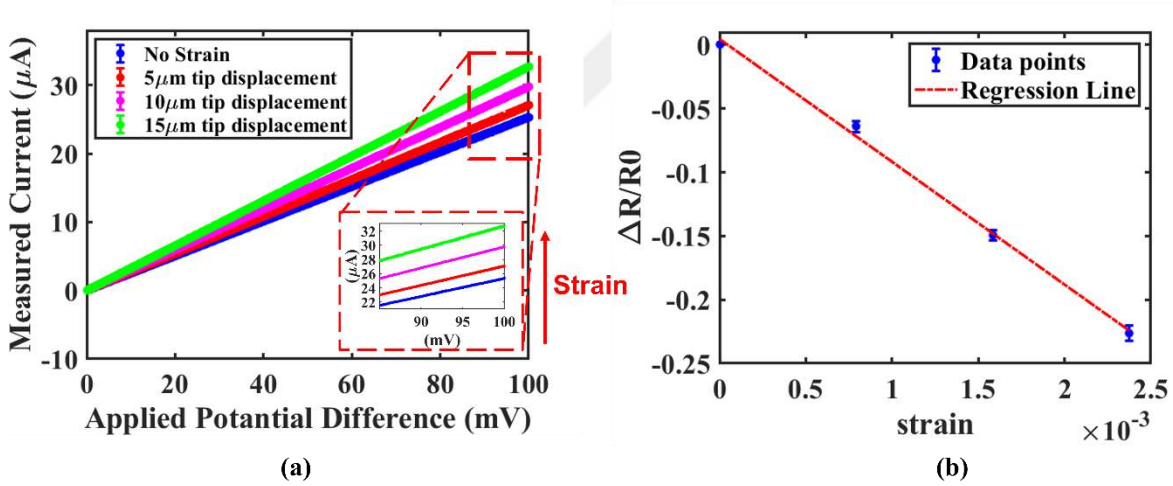


Figure 88: (a) Applied Potential Difference – Average Current Each Pin Displacement, (b) Applied engineering strain (from 3D simulation) - $\Delta R/R_0$ (from I-V measurements) for device#3.

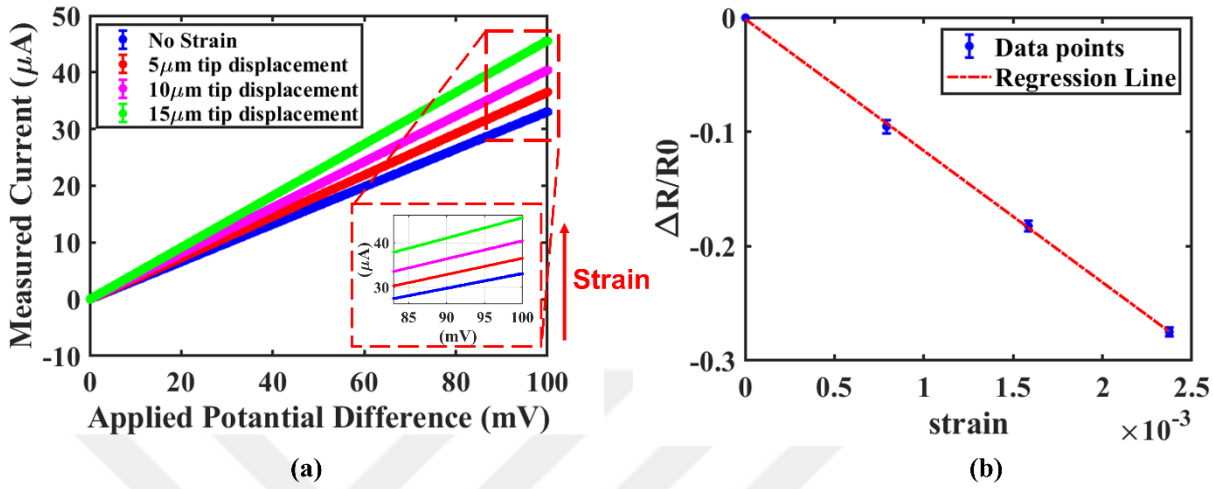


Figure 89: (a) Applied Potential Difference – Current for Each Pin Displacement, (b) Applied engineering strain (from 3D simulation) - $\Delta R/R_0$ (from I-V measurements) for device#4.

As demonstrated in Figure 86 to Figure 89, the decrease in rate of resistance change was almost in linear fashion. Afterwards, we intended to push the limits with device#5 and introduced 20µm prescribed pin displacement which brings 5µm additional out-of-plane displacement. Figure 90(b) shows the rate of resistance change is still in the linear region. Unfortunately, during the last test (4^{th} repeated test), the SOI chip (Figure 83) is broken. Therefore, I-V data is only available until 30mV. The rate of resistance change presented in Figure 90(b) is calculated until this point (30mV). On the other hand, repeatability is confirmed at Figure 90(a). Gauge factor values are calculated as -108.7, -108.3, -108.4 and -106.7, respectively. If the SOI chip had survived, we would introduce 25µm, even 30µm pin displacement as well to investigate the further response of the SiNW array. A curious reader is encouraged to visit Appendix to further see the raw current data figures, averaged current data figures and engineering strain-$\Delta R/R_0$ figures of all individual bending tests. To summarize, gauge factor value of -105.37±8.12 is calculated for all direct bending tests realizing 2µm-length vertical SiNW arrays.

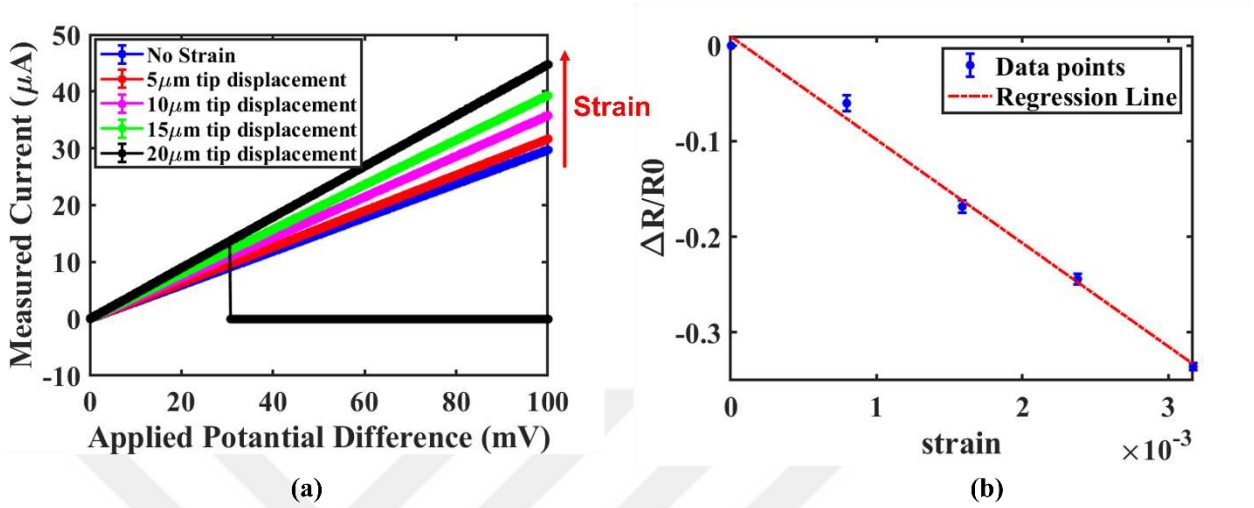


Figure 90: (a) Applied Potential Difference – Current for Each Pin Displacement, (b) Applied engineering strain (from 3D simulation) - $\Delta R/R_0$ (from I-V measurements) for device#5.

3.8. Results and Discussion

The vertically stacked SiNW array devices are electromechanically tested with four-point bending methodology by means of two different approaches: "indirect" and "direct" four-point bending. Indirect method includes a sample chip glued to another longer strip material. The strip material choice depends on the test needs. Experimental procedure (e.g., eligibility for repeatable tests) and the adhesive type defines the strip material choice. Since we have multiple samples in an SOI chip, our procedure requires a repetitive process. Test repeatability is expected to achieve two purposes: testing all samples on the SOI chip and testing them multiple times to have reliable data. Metals such as steel can easily be subjected to plastic deformation which results with necking. Hence, it becomes almost impossible to relieve the load from the glued composite test structure. Selecting strip material as a test SCS, rather than metals, provides the advantage of staying in elastic region. Therefore, we could successfully load and unload SOI chip more than 200 times. JB weld is selected as adhesive material to glue SOI chip and SCS strip to each other. Strength of JB Weld is noted as superior compared to the other commercially available epoxy-based adhesives. Out-of-plane prescribed displacement is exerted on the overall test sample to realize tensile loading on the vertically stacked SiNWs. SiNW arrays having different length are subjected to bending tests and I-V characteristics are recorded via a semiconductor parameter analyzer. Gauge factor as a piezoresistivity measure of the SiNW arrays is calculated based on the rate of relative

resistance change with respect to the stipulated engineering strain obtained via 3D simulations at COMSOL Multiphysics. Results reveal that the effective gauge factor is between -15 and -42 if we assume a perfect binding state between chip and strip. This number is quite lower than expected when compared to our group's previous study [44]. The gauge factor of a highly n-doped single SiNW is reported between -130 and -140. Consequently, presence of adhesive layer is considered as affecting the measurements. It is already reported in the literature [72], [73] that, the effective gauge factor should be lower than the actual value when a glue is used, and it requires additional characterization mechanism on the adhesive, itself. Therefore, to compare, absolute need of a direct bending experiment grows out. Comprehensive results for indirect bending test are provided in Figure 91.

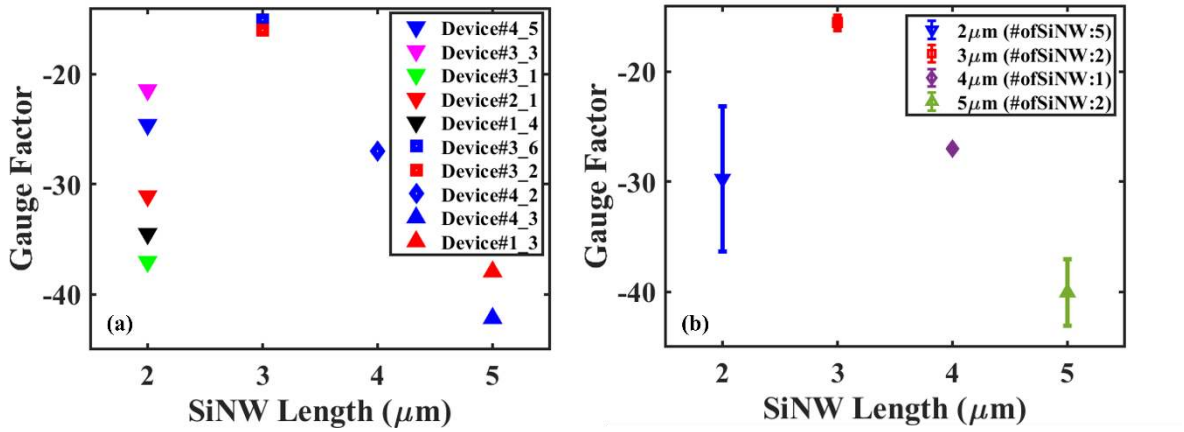


Figure 91: Extracted gauge factor data for indirect bending test. a) for each device, b) for each SiNW length.

To realize a direct four-point bending test, a new design of experimental setup is studied to preserve the compliance with the chip dimensions. Five different vertical SiNW array devices, having 2µm-length, are tested via direct bending. We calculated the gauge factor value as -105.37±8.12. Indirect bending tests on 2µm-length SiNW arrays resulted with -29.2±6.47. Hence, direct bending test results are almost 3.5 times higher than the indirect approach. Figure 92 demonstrates the test result for 2µm-length SiNW arrays for both indirect and direct bending approach. Our comparison between direct and indirect methods aligns with of [73], in which they obtained almost 4.5 times lower engineering strain with the presence of an adhesive layer. Our results confirm that the effect of "gluing" chip onto the test specimen reduces the performance of the bending test, drastically.

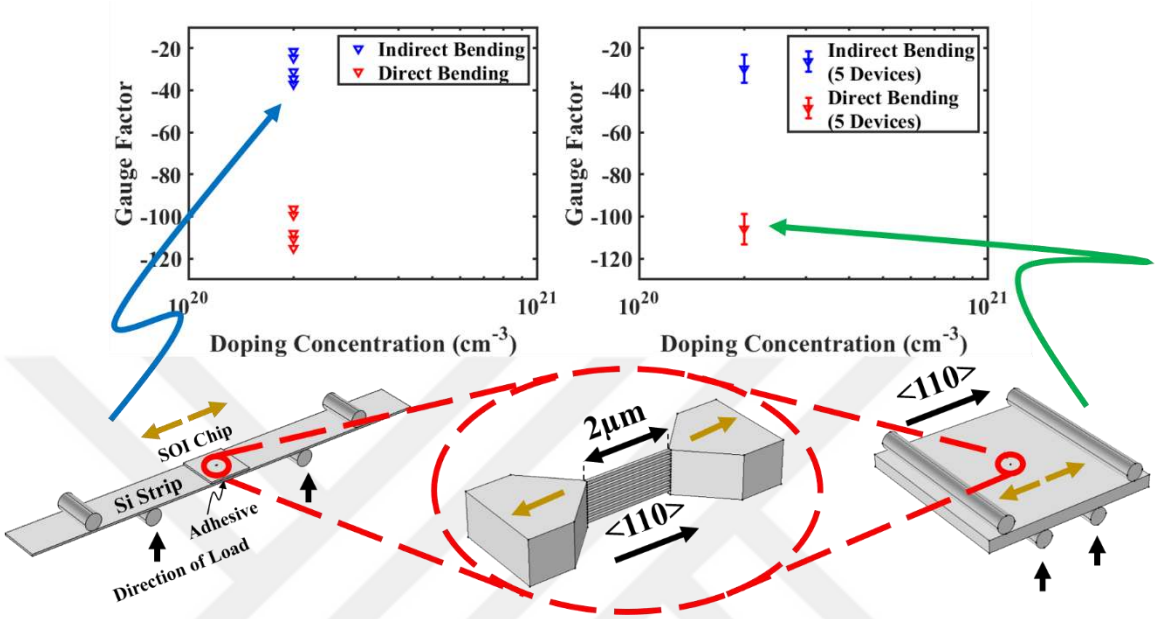


Figure 92: Indirect and direct four-point bending test result for SiNW arrays having 2µm length.

Chapter 4

Conclusions

In this dissertation, a specific SiNW array architecture is studied through four-point bending tests for piezoresistivity characterization. Mechanically coupled vertical silicon nanowire arrays are considered as the building blocks of new generation resonators and their piezoresistivity characteristics play key role in designing such devices. Two different test setups are utilized based on the four-point bending principles. In the first setup indirect bending is conducted as an adhesive layer is present between the device under test and a carrier silicon strip. Second setup provides direct bending of silicon nanowire arrays. Both setups are manufactured via CNC machining. 3D simulations are carried out to obtain engineering strain of the SiNWs. Effective gauge factors are extracted as -29.2±6.47 (standard deviation) for indirect bending, and -105.37±8.12 (standard deviation) for direct bending, providing a clear indication on the effect of the adhesive layer used in indirect testing. The results obtained during the studies are listed in detail.

- Highly doped, n-type, double clamped piezoresistive silicon nanowires are fabricated along <110> direction from SOI wafer having 10µm device layer. I-V measurements construct that linear resistor behavior is obtained up to 100mV potential difference.
- Parasitic effect of silicon membrane at the bottom of device layer, is investigated for the electrical characterization. Four orders of magnitude resistance difference between SiNW and silicon membranes is calculated, resulting that silicon membranes can be neglected during electrical measurements.
- Fluorescence light effect on the silicon membranes is demonstrated. N-doped

SiNWs did not provide a clear indication of photo-induced effect under a typical microscope fluorescent light.

- A cheap, in-house alternative electrical interconnection technique is developed with a commercially available silver paste. I-V measurements indicate that contact problem between copper wire and Pt touchpad prevents a clear readout. More study is necessary for a reliable measurement scheme.
- Two different four-point bending approaches are employed on the vertically stacked SiNW arrays to accomplish piezoresistivity characterization. Gauge factor values are extracted along the tensile response of the nanowires. Indirect bending approach revealed 3.5 times lower effective gauge factor compared to direct bending approach.
- Presence of adhesive layer is found to be depreciating the test quality of the indirect bending approach due to absorbing significant amount of the force exerted. This method can require adhesive material characterization and additional equipment to acquire applied engineering strain. The reliability is questionable due to repeatability issues. The adhesive thickness and bond strength can be deviating at each test attempt. We employed DIC analysis on the sample chip extract local engineering strain. Results reveal that camera resolution should be higher to detect the engineering strain on the order of 10^{-4} and 10^{-5}.
- Gauge factor extracted for direct bending approach is in close proximity with the literature review provided in the Introduction chapter of this dissertation. Figure 93 demonstrates the position of our findings in the related literature. Doping type (n- & p-) is acknowledged in the legend of the figure. Test method utilized for gauge factor extraction is not provided. A curious reader is encouraged to visit Table 3 to investigate the details of literature review.

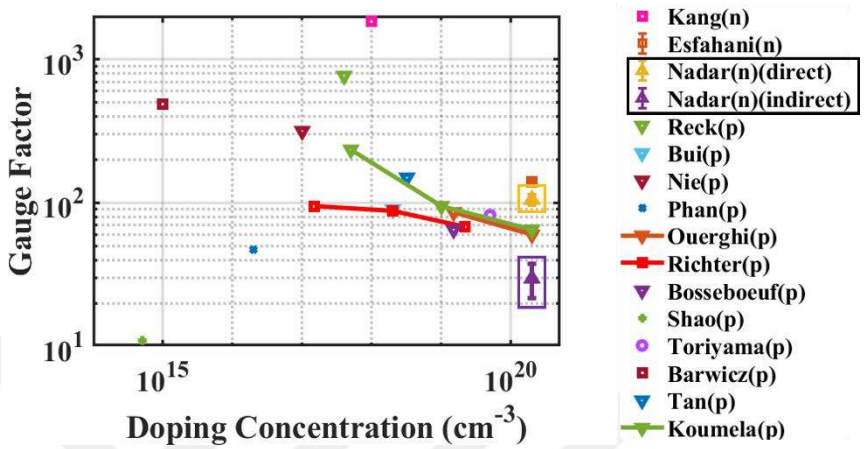


Figure 93: Literature data for top-down fabricated, <110> SiNWs under tensile load.

- TEM cross-section analysis along the device layer thickness for vertically stacked nanowires must be carried out to acquire cross-section of each contributing nanowire. The cross-section of SiNWs can be deviating from top to bottom.
- Even though initial doping concentration is set to be on the order of 10^{20} cm^{-3}, diffusion through 1µm device layer thickness is hardly achievable according to Figure 45. Therefore, dopant profile along the device layer thickness can be studied to understand composite structure of SiNW array.
- Different doping concentrations can be studied to finalize doping level dependency of the piezoresistive response of the SiNWs, in the future.
- The electromechanical experiments are conducted in open-air environment. In that case, a controlled vacuum and temperature profile cannot be realized. Even the humidity variation can change the piezoresistivity characteristics due to electron trapping. Two different future work items can be suggested. 1) Temperature dependency and 2) vacuum - humidity related characteristics relating the effective gauge factor should be studied in a controlled chamber.
- The DUTs are loaded and unloaded 25 times at least. No fatigue behavior and change in piezoresistivity is observed. For fatigue analysis, a motorized test setup should be designed to carry out almost a million times cycling loading

with a specific frequency.

- Experimental results are evaluated with the assumption of there is no intrinsic stress on the SiNWs. There supposed to be intrinsic stress due to the fabrication flow. Vernier gauges can be designed and implemented along the SiNW direction into the wafer layout to measure the intrinsic stress up to a certain limit. The resultant intrinsic stress can be used to evaluate the engineering strain in the 3D simulations.
- To this end, miniaturized transduction capability of SiNWs through piezoresistivity is investigated. Reliable inertial sensing applications require reliability and repeatability. Piezoresistivity is already implemented in the shock accelerometers as the main inertial transduction mechanism. However, high-end accelerometers including tactical plus and navigation grade do not utilize this technology due to its repeatability and sensitivity in both measurements and fabrication. Therefore, optimization between doping concentration, dopant type, crystallographic orientation, structure geometry and fabrication repeatability stays as a crucial intermediate phase between the concept of scientific interest and commercialization.

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APPENDIX A:

An Alternative to Wirebonding: In-house Application of Silver Paste

Wirebonding is a widely used in CMOS technology. It basically is a method of bonding thin metal wires to a pad, as a technology that connects the internal chip to outside. There are different methods developed to achieve a successful wirebonding operations for different metal types. Aluminum and gold are the usual choices as metals for a typical wirebonding setup. For our project, we preferred to deposit our chips with 5nm Cr and 50nm Pt. Even there are suitable wedge tools to wirebond Pt, it is not always available. Moreover, wirebonding operation requires a suitable setup and an experienced operator. As an alternative, tried to develop an in-house method to accelerate the electrical characterization. Basically, our methodology involves using probe station needles. Most of the micro / nano electromechanical systems characterization laboratories has an old or new generation probe station to perform basic electrical characterization steps in-house. Therefore, for us, our methodology should be applicable to most of the research laboratories.

In order to provide a solid interface between the metal wire and signal touchpad, we utilized "Sigma Aldrich 735825 Ag Silver Paste" which is commercially available. This unique chemical is offered in the form of "paste" to the user and has a conductivity of 1-3x10e-5 ohm-cm. Suggested storage temperature is 2-8ºC so that when working on room temperature, the operator should be fast enough to take the Silver paste to a fridge again.

Figure 94 demonstrates a successful application of our methodology on a 250 µm x 250 µm Pt touchpad while Figure 95 shows an unsuccessful trial. Even the Pt metal touchpad is torn off upon silver paste application. The reason of failure is that curing time took more than expected. Therefore, some of the silver paste was still in viscous form. Trying small

loads to test the mechanical integrity resulted with tearing of the metal touchpad.25-µm diameter Cu wire is used as wirebonding wire.

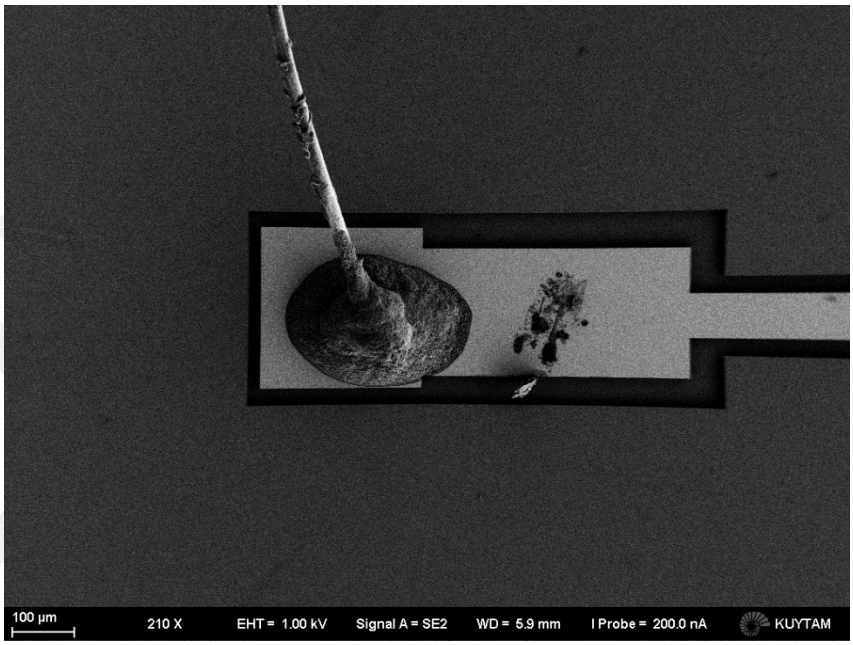

Figure 94: SEM micrograph of a successful physical interface between Cu wire and Pt touchpad.

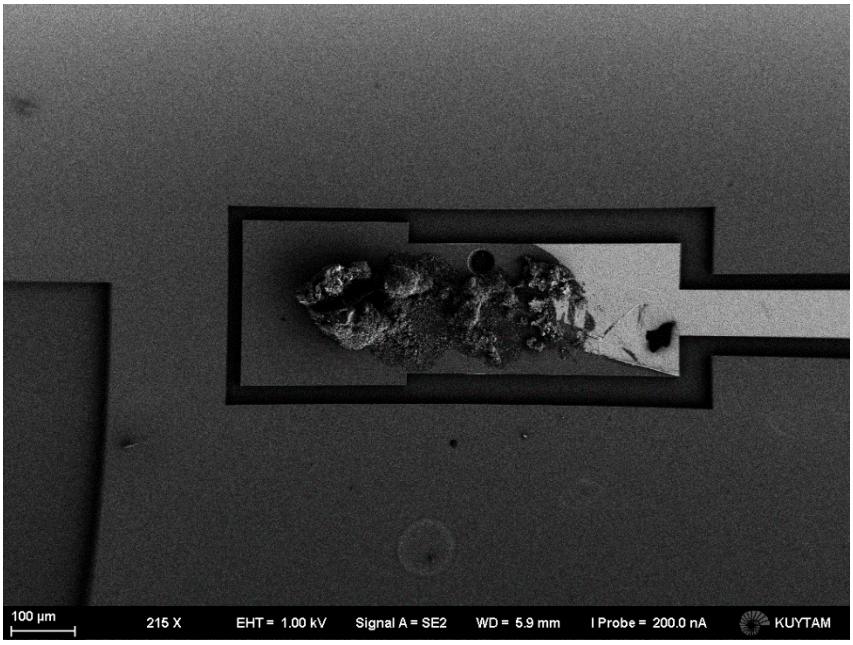

Figure 95: SEM micrograph of an unsuccessful physical interface between Cu wire and Pt touchpad.

Silver Paste Application Procedure

0) Perform I-V measurement on the sample SiNW, glue chip to PCB, weld SMA connectors to PCB. Finalizing this step before silver paste application is mandatory.

1) Mount up a dummy / not useful needle

2) Place the chip / PCB onto the chuck of probe station

3) Three separate manipulators and needles are used, ground them. Let's name them as "M1", "M2" and "M3" for simplicity (Figure 96). Ground SMA connectors welded to PCB as well.

Figure 96: Two separate manipulator-needle system.

4) Apply the silver paste to an outer plate or PCB surface

5) Wrap the Cu wire around the needle of M2, 2-3 times.

6) Use needle of M1 to take "some" silver paste from the outer surface and apply it to the metal touchpad. Here the trick is, operator has to accomplish everything manually so that a lot of practice is necessary. Silver paste application should be as "touch", "wait a few seconds" and "pull back". Therefore, the viscous paste will have enough time to spread on the touchpad.

7) Take M1 back

8) Bring M2 with wrapped Cu wire on the silver paste applied touchpad. Rub the viscous

paste slightly with the tip of Cu wire so that paste will be applied over the wire tip.

9) Leave M2 as it is

10) Use needle of M1 to take “some” silver paste from the outer surface, again and apply it to the place where the tip of Cu wire is touching on the metal touchpad. Silver paste application should be as “touch”, “wait 1-2 seconds” and “pull back”. Therefore, the viscous paste will have enough time to spread on the touchpad Figure 97. If operator waits more, there will be too much silver paste spread around as shown in Figure 98. Eventually, the Cu wire tip will be encapsulated with silver paste.

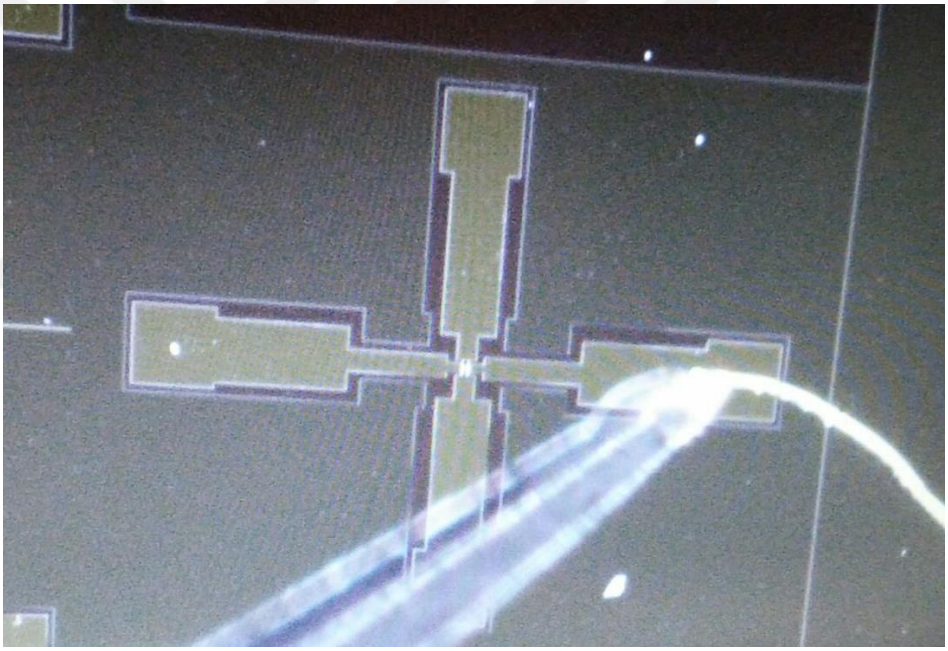

Figure 97: M1 pushing on the Cu wire.

11) Take M1 back, leave still M2 as it is for 24 hours

12) Repeat steps 5-11 for second metal touchpad. Use M3 instead, finally wait for 24 hours for a complete solidification of silver paste.

13) 24 hours later, upon paste solidification, manually take out the wrapped wire form the needle.

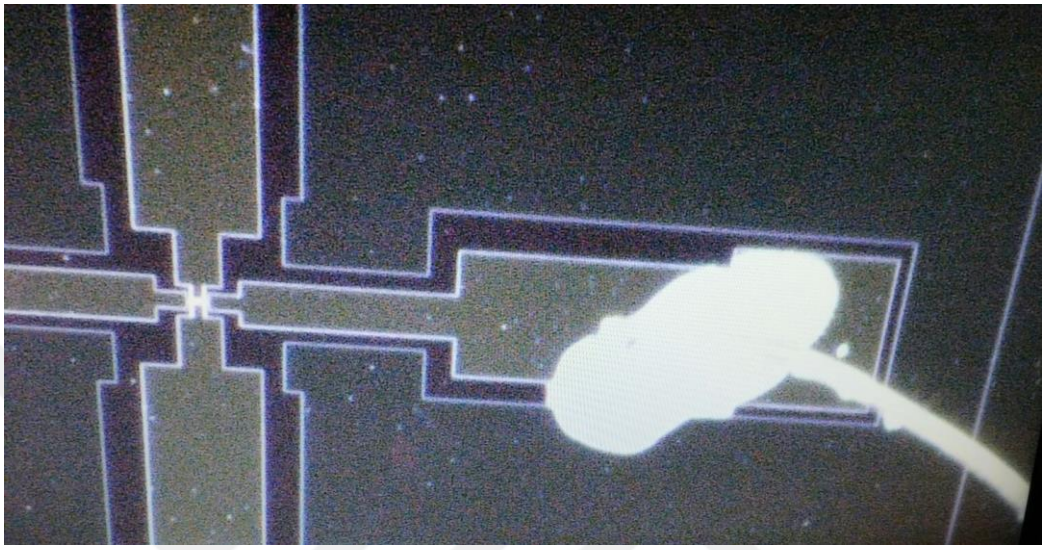

Figure 98: Too much application of silver paste to the touchpad. Picture taken from monitor of optical microscope.

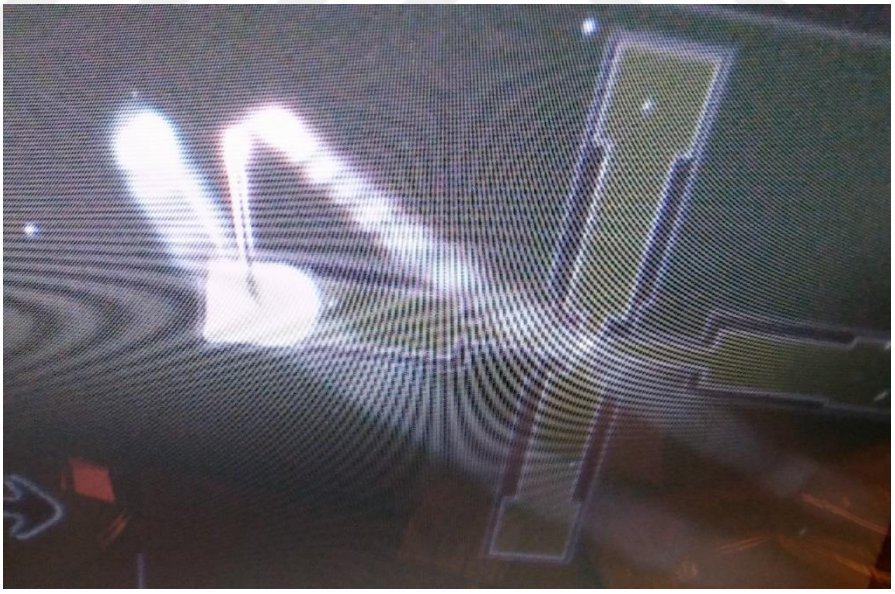

Figure 99: Silver paste and Cu wire left to solidify for 24 hours.

14) Silver paste application on chip is finalized. From now on, procedure steps will explain how to apply the silver paste to chip to finalize the circuitry. Start applying the silver paste to an outer surface, again.

15) Use needle of M1 to take “some” silver paste from the outer surface and apply it to the

PCB touchpad. Silver paste application should be as “touch”, “wait a few seconds” and “pull back”. Therefore, the viscous paste will have enough time to spread on the PCB touchpad.

16) Take M1 back

17) “Bend” the Cu wire by using M2 to make a physical contact between PCB touchpad and Cu wire tip. This step also requires a lot of hands-on-experience. Bending such wires intentionally is very challenging so that operator should firstly try to perform each step on dummy samples.

18) Leave Cu wire and M2 as it is.

19) Use needle of M1 to take “some” silver paste from the outer surface, again and apply it to the place where the tip of Cu wire tip is physically in contact with the PCB touchpad. Silver paste application should be as “touch”, “wait 1-2 seconds” and “pull back”. Therefore, the viscous paste will have enough time to spread on the touchpad and wire tip. Eventually, the Cu wire tip will be encapsulated with silver paste.

20) Take M1 back, leave still M2 and Cu wire as it is

21) Repeat steps 15-21 for second PCB touchpad. Use M3 instead, finally wait for 24 hours for a complete solidification of silver paste.

13) 24 hours later, upon paste solidification, manually take out M2 and M3 needles.

24 hours of waiting for silver paste solidification is a mandatory step. Most of the samples undergone this procedure resulted with burnt SiNWs. Recall that I-V measurement is performed at 0^{th} step to verify that there is a solid and working SiNW. There are a few samples giving reasonable I-V measurements (Figure 100). The reason for such a low yield rate should be the process time of silver paste application. The whole procedure takes almost three days to complete each step. For three days sample is subjected to trap charges. Even though SMA connectors and manipulators are grounded, there are still sharp tips of needles and Cu wires which can trap charges. In addition, recalling the step that the Cu wire is wrapped around needle, a perfect physical contact between wire and needle might not be provided. Nevertheless, the charge trapped may not be grounded steadily, which may result the burn of SiNW. Remember that SiNWs are already highly doped and quite conductive.

I-V Measurements Before & After Silver Paste Application

I-V characteristics of two different pasting trials are extracted to understand the conductive properties of the pasting operation. Measurements are conducted before and after the silver paste application to compare the results (Figure 100). It is observed that while the current response is linear before pasting, it becomes full of spikes after the paste application. The same output is obtained for two different samples. Even though the base current is same for both measurements, spikes would make the applicability on piezoresistivity measurements challenging. The resolution will be quite low. Small current deviation after mechanical load application onto the SiNW will be almost impossible to detect as, well.

The reason for having spike is probably low contact characteristics. Repeating the I-V measurements with a probe needle as providing slight contact properties, similar spikes are observed for different sample. However, increasing the contact properties between needle and touch-pad, the measurement becomes stead. Therefore, deeper experimental studies on resolving the low contact characteristics can provide better output in the future. This will eventually make applying this technique possible for basic in-house testing purposes without the need of an expensive wirebonding setup.

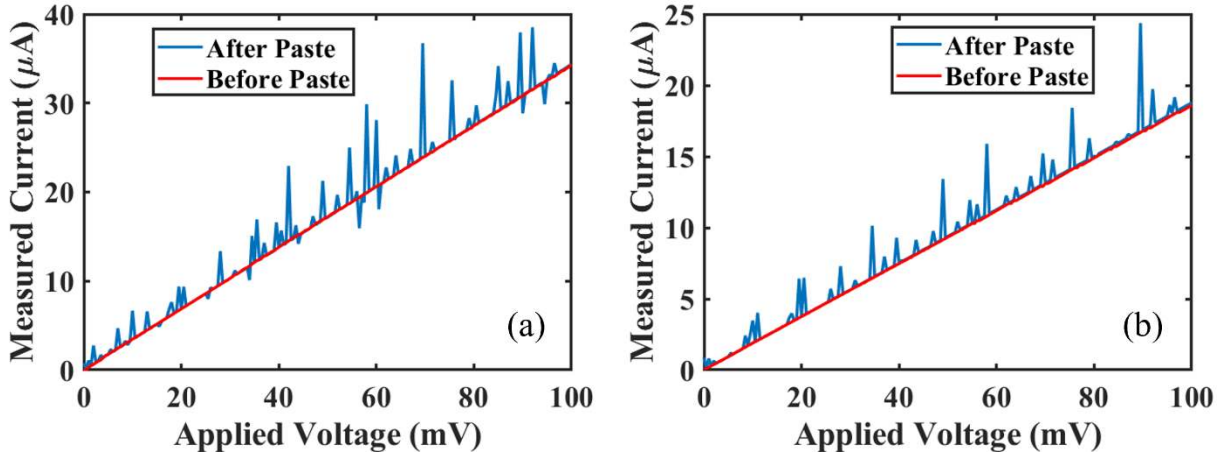

Figure 100: I-V measurements before and after silver paste application for two different samples.

APPENDIX B:

Previously Designed Piezoresistivity Characterization Setups

Several techniques are built and tested to electrically characterize the fabricated doped, single SiNWs. All of the methods are inspired from the literature. Because of having a 10mm by 100mm sized SOI chips, it was a challenging task to find the working methodology for electrical characterization. "Electrical" characterization of SiNWs is performed only for no-strain condition, therefore a probe station or a wirebonding operation is the only sufficient requirement. However, when the task is electromechanical characterization of piezoresistive response studying on a reliable setup is mandatory. Recalling the Chapter 1: Introduction, different methodologies have been introduced and exemplified in detail. Among them, using a MEMS mechanism to excite the specimens is the least relevant choice, due to having chips fabricated already. MEMS would be an option to consider in the design stage so that fabrication would be carried out accordingly. Having the chips fabricated, the methodology that can be interpret is to bend or exert a tensile / compressive load on the chips externally. Meaning that the chip will be physically interfaced with an outer device / material so that bending / load would be applied. In this work, various setups have been developed and studied for this purpose. Consequently, they did not provide reliable and promising results.

PCB as the Cantilever Beam

Cantilever type bending setup is a good option to consider for transferring the load onto the specimen. Most of the time, the piezoresistive nanowires are embedded in cantilever shaped-dies and bending procedure is followed with the help of a stylus, accordingly. Inspiring from this idea, we wanted to permanently attach our SOI chip to FR4-based PCB and use it as a cantilever beam. It was proposed that we would accomplish the electrical connection between

PCB and SOI chip by means of in-house wire bonding technique introduced in Appendix "A new alternative to wire bonding: in-house application of Silver paste". A BNC coax - coax to triax adaptor – triax cable wire connection is suggested. Agilent B1500A Semiconductor Parameter Analyzer is used for electrical excitation and measurements. Figure 101 describes the proposed setup in detail, including the electrical and physical connections as Figure 102 demonstrates the actual setup without SOI chip attachment.

This idea unfortunately did not provide a reliable solution to our problem as FR4 as PCB material has too low stiffness when compared to silicon. Therefore, the amount of the load exerted is directly absorbed by FR4 and the adhesive material used between chip and PCB.

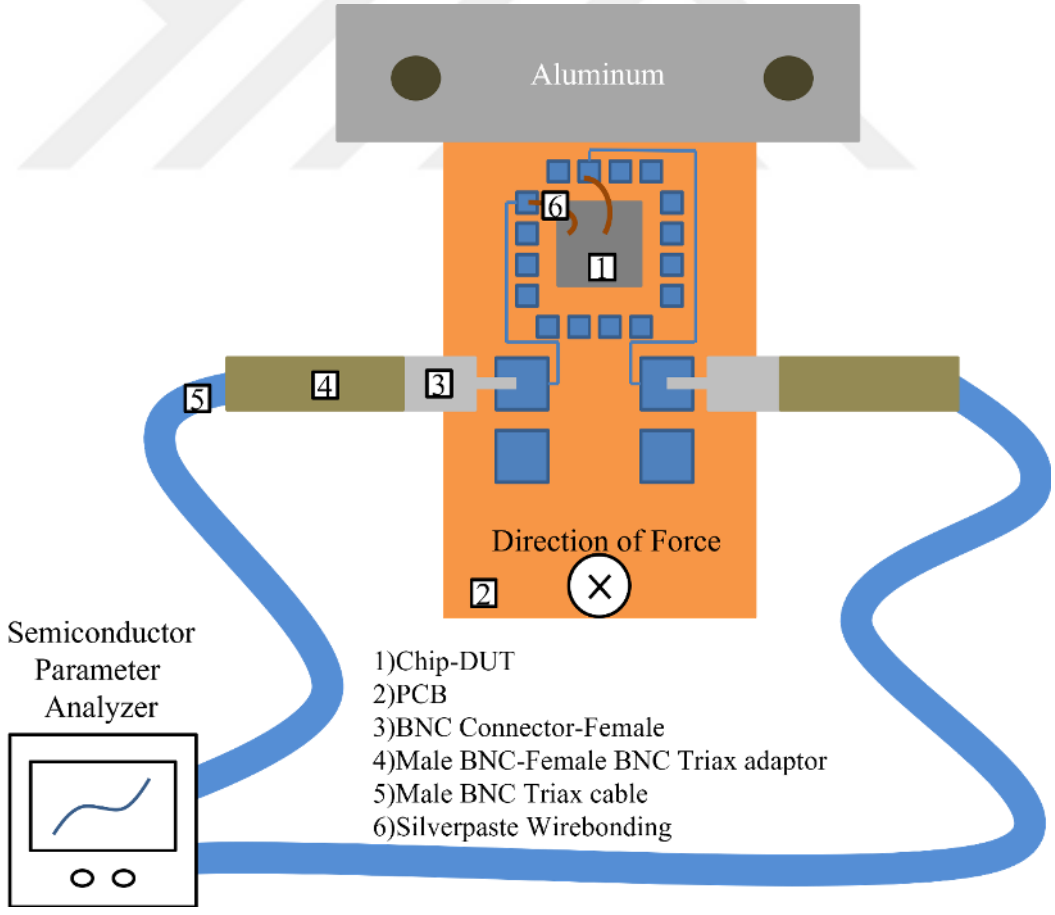

Figure 101: Proposed setup-1 schematic, PCB-Cantilever type bending setup.

We also noticed cracks on FR4 when prescribed displacement is applied on the tip of the PCB. Nevertheless, having a successful, reliable, and repeatable test procedure could not be achieved with this setup.

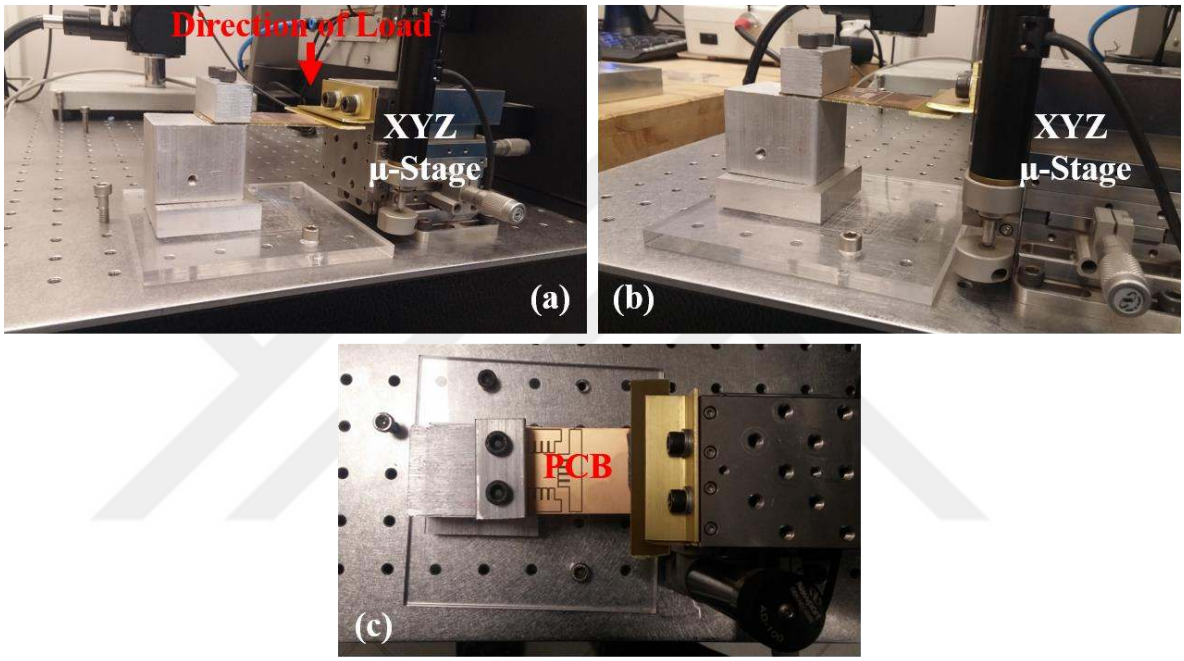

Figure 102: Proposed setup-1. a) and b) side view, c) top view.

Three- Point Bending

Three-point bending approach is not widely utilized in the piezoresistivity characterization of SiNWs. A study [34] reporting a successful implementation inspired us building the setup shown in Figure 103. The idea involves of using a Teflon clamp at both end of the SOI chip. Top of the clamp is left open to achieve physical contact with probe needles to measure electrical response of the nanowires. The bottom side of the clamp has a window opening, as well, to apply the external load in out-of-plane (vertical) direction. The XYZ µ-stage is a manually operated device and used to control the bending displacement in our study. The control is done visually so that the resolution of the device is set to 5µm. Upon the first trial SOI chip is broken as in Figure 103(d). Since this approach is risky on losing more chips, two

different four-point setups are designed as explained in Chapter 3.

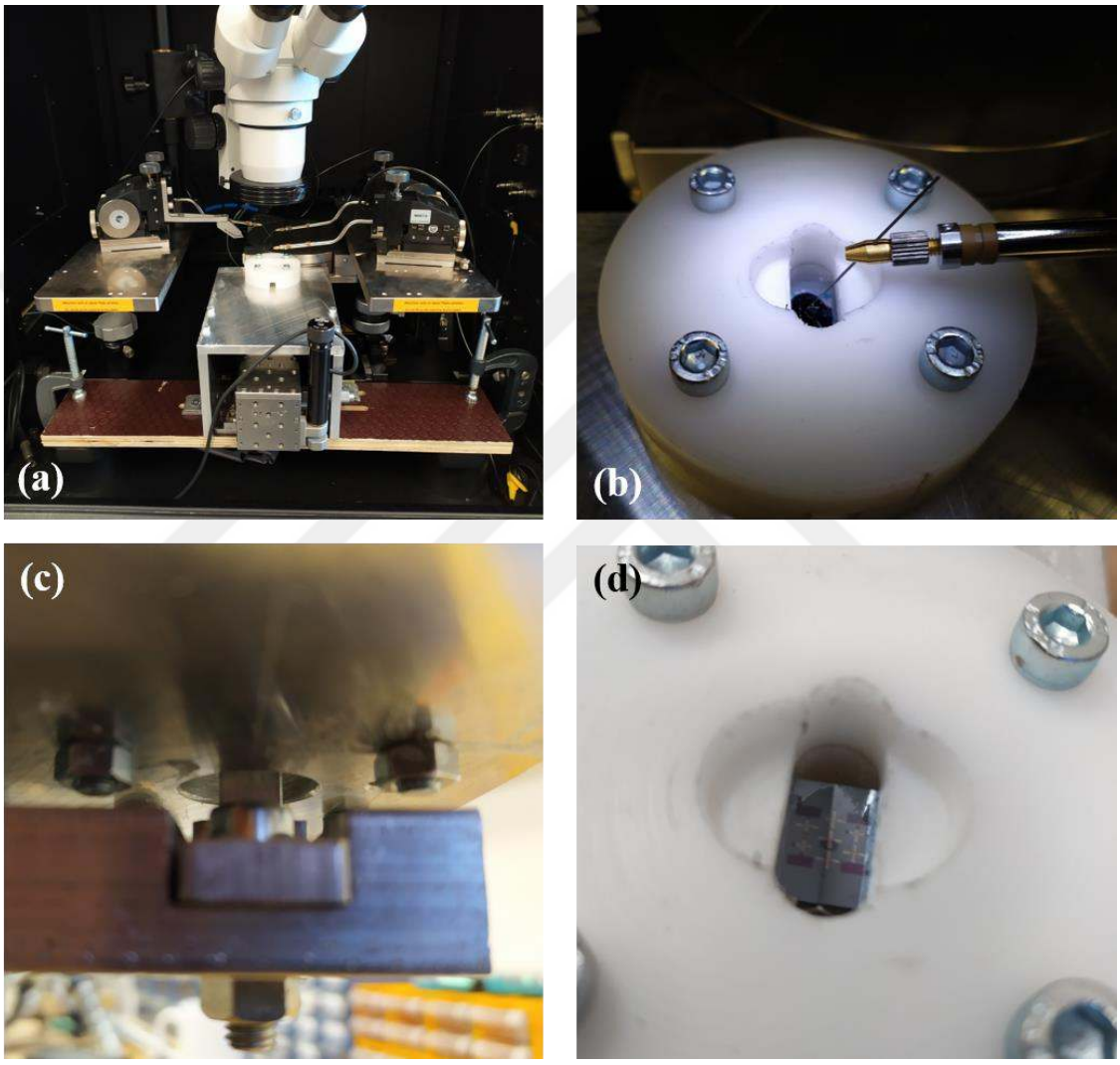

Figure 103: Prosed setup-2. a) in probe station, b) close view of top window of Teflon clamp, c) bottom window of Teflon clamp to exert external force via XYZ µ-stage and d) broken SOI chip after load application.

APPENDIX C:

MEMS Based Test Setup for Mechanical Characterization of SiNWs

Small-scale electromechanical characterization of silicon has gained attention in the last few decades. Scaling down from bulk, size effect on the material properties of silicon (such as piezoresistivity, modulus of elasticity, fracture strength and thermal conductivity) is observed through different studies. Several results are reported for various techniques which are utilized for the characterization of such material properties. Therefore, reliability of techniques should be ensured for small-scale testing.

Bending and tensile tests are the basic approaches which are benefitted along the mechanical characterization of the silicon nanowires. Bending test is conducted with a single or double clamped beam and an Atomic Force Microscopy (AFM) tip. AFM tip bends the sample in a specific orientation and causes deflection. On the other hand, tensile testing mainly relies on MEMS based actuation and sensing mechanism.

In a typical tensile testing, specimen is subjected to a uniaxial force which enables stretching of the specimen. The elongation might be obtained via optical, capacitive reading or piezoresistive methods. Testing platform mainly consists of three major sections: an actuator, a sample, and a sensor. In Figure 104, a representative mass-spring model of test platform is provided.

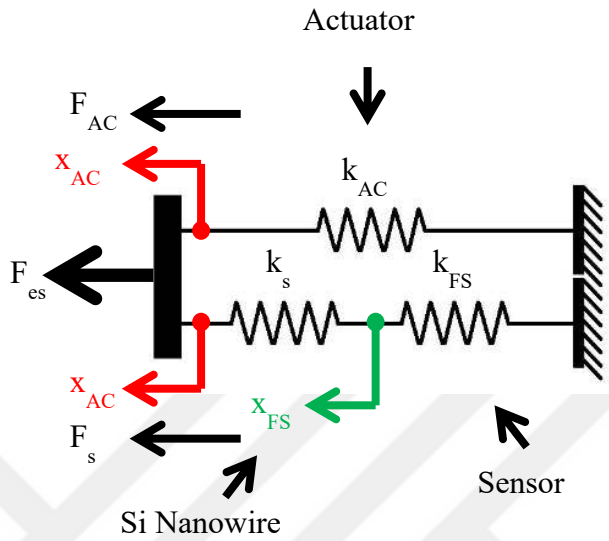

Figure 104: Mass-spring model of a micro tensile testing device. Fes is generated electrostatic force, F_{AC} is force on the actuator springs, x_{AC} is the actuator displacement, F_s is force on the sample, x_{FS} is force sensor displacement, k_{FS} is amplifier sensor spring constant and k_{AC} is actuator spring constant.

In our study, [33], MEMS based micro tensile testing platform is employed. The platform includes a comb-drive capacitive actuator and displacement amplifier springs (Figure 105). Amplifier springs are utilized and designed to enhance the nanowire elongation. A DIC (Digital Image Correlation) procedure can be developed for elongation studies in the future. MEMS design in [33] is achieved by the author of this thesis, while the monolithic fabrication and testing is conducted by my colleague. In [33] a detailed fabrication flow, and micro tensile testing performance is provided. In this section, basic formula, and fundamental considerations on the design of MEMS platform is presented.

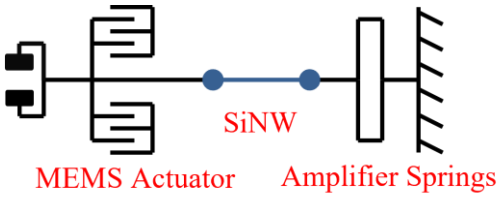

Figure 105: SiNW tensile testing scheme with a MEMS based actuator and mechanical amplifier springs.

MEMS based actuator is the force generator of whole testing device. Its working principle simply depends on electrostatically driven comb drive mechanism. Amplifier springs are

subjected to enhance the readability of the tip displacements of the SiNW. SiNW is monolithically integrated between actuator springs and MEMS based actuator (Figure 105). Since SiNW geometry (width, thickness, and length) is decided prior to fabrication, MEMS based actuator and amplifier spring design calculations are finalized, accordingly.

The formulations and design criteria are deeply introduced in [92]. Therefore, only basic formulae will be provided in this section. A capacitively excited MEMS actuator utilizes the principles of electrostatic energy generated between comb fingers. Due to potential difference, electric field and electrostatic force are generated between comb fingers. Fixed fingers are subjected to a sweeping voltage, as moving fingers and shuttle are set to ground. Electrostatic force can be expressed as in equation (C.1).

$$F_{es} = \frac{\partial W}{\partial x} = \frac{1}{2}\frac{\partial C}{\partial x}V^2 = N_{AC}\varepsilon_0 t\left[\frac{w_{AC}}{(g_x - x)^2} + \frac{1}{g_y}\right]V^2 \tag{C.1}$$

$$\frac{C_y}{C_x} = \frac{(h + x_{ACmax})}{g_y}\frac{(g_x + x_{ACmax})}{w_{AC}} > 40 \tag{C.2}$$

In equation (C.1), "N_{AC}" is the number of comb fingers, "V" is the potential difference between comb fingers and "x" is the amount of moving finger/shuttle displacement while "w_{AC}" is comb-finger width, "g_x" is horizontal gap and "g_y" is the vertical gap between fingers. t stands for the device thickness which is also SOI device layer thickness (10µm). "W" is the total electrostatic energy and "C" is the total capacitance generated between fingers. "ε_0" is the relative permeability of air. As demonstrated in mass-spring model and equations (C.1 & C.2), electrostatic force is the total of force on the actuator springs and the force on the SiNW and amplifier springs. The force acting on the SiNW and the amplifier spring are same. Therefore, the amplifier spring constant should be as low as possible to maximize the displacement readout. Since the test setup aims to axially load the sample until it fractures, the force generated should be higher than the calculated fracture force on the SiNW. Moreover, the overall structure should be a slider mechanism to maximize uniaxial force output. Therefore, C_y/C_x ratio should be almost negligible compared to the axial force

and equation (C.2) is estimated to have a Cy/Cx ratio more than 40. C_y and C_x are generated capacitances in x and y direction in a comb-finger setup, h is the overlap of the fingers and x_{ACmax} is the maximum amount that the actuator can displace along the horizontal x-axis. With these criteria in mind, design geometry is obtained in a series of MATLAB code available in [92]. While determining the final design geometry, criteria such as device simplicity for ease of fabrication, stability for pull-in phenomenon and linearity for longitudinal sliding mechanism are kept in maximum notice. In Table 10, resulting design geometry is given for the sample SiNW having 80nm-width, 200nm-thickness, and 4µm-length.

Table 10: MEMS actuator based tensile testing device design specifications

g_y	W_{AC}	t	N_{AC}	V	k_{FS}	Δ_{SiNW}	Δ_{AS}
3.5µm	5µm	10µm	400	40V	15N/m	282.4nm	5.12µm

The monolithic fabrication of the integrated MEMS-SiNW geometry is accomplished in Center of MicroNano Technology (CMi) cleanroom facilities at EPFL (École Polytechnique Fédérale de Lausanne), Lausanne, Switzerland. Figure 106 demonstrates integrated MEMS-SiNW images captured under optical microscope and SEM. Detailed information on fabrication steps, TEM cross section analysis for can be found in [93] and [33]. Upon fabrication, test setup is excited under SEM. The comb drive mechanism is charged so that a rapid increase in accumulated electron density occurs which yields to electrostatic force generation. Upon achieving required force, SiNW fractures which concludes that the fabrication of MEMS/SiNW monolithic integration is successfully completed, and designed MEMS device can work for future characterization steps.

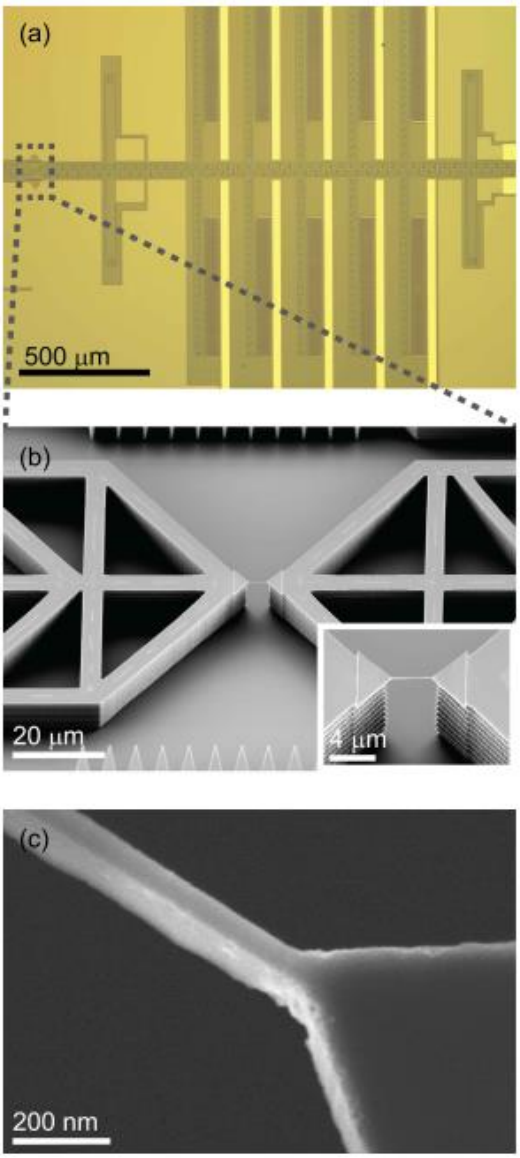

Figure 106: (a) Overview of MEMS under optical microscope, (b) SEM micrograph of double suspended SiNW between MEMS actuator and amplifier spring, (c) SEM micrograph of SiNW-MEMS interface view. Taken from [33].

APPENDIX D:

Indirect and Direct Four Point Bending Procedures

Indirect Bending Procedure

i) place and align the sample on the setup properly,

ii) take zero displacement-no bending I-V measurement with probe tips via Semiconductor Parameter Analyzer, five times

iii) remove probe tips from touch-pads to a safe point

iv) (+250)µm prescribed displacement of the bottom pins to bend silicon strip

v) place probe tips on the touch-pads and take I-V measurement five times

vi) remove probe tips from touch-pads to a safe point

vii) (-250)µm prescribed displacement of the bottom pins to the "no bending position" and wait for 10 seconds

viii) (+500)µm prescribed displacement of the bottom pins to bend silicon strip

ix) place probe tips on the touch-pads and take I-V measurement five times

x) remove probe tips from touch-pads to a safe point

xi) (-500)µm prescribed displacement of the bottom pins to the "no bending position" and wait 10 seconds

xii) (+750) µm prescribed displacement of the bottom pins to bend silicon strip

xiii) place probe tips on the touch-pads and take I-V measurement, five times

-remove probe tips from touch-pads to a safe point

xiv) (-750)µm prescribed displacement of the bottom pins to the "no bending position" and wait 10 seconds

xv) (+1000)µm prescribed displacement of the bottom pins to bend silicon strip

xvi) place probe tips on the touch-pads and take I-V measurement, five times

xvii) remove probe tips from touch-pads to a safe point

xviii) (-1000)µm prescribed displacement of the bottom pins to the "no bending position" and wait 10 seconds

xix) (+1250)µm prescribed displacement of the bottom pins to bend silicon strip

xx) place probe tips on the touch-pads and take I-V measurement, five times

xxi) (-1250)µm prescribed displacement of the bottom pins to the "no bending position" and finalize the experiment.

xxii) Repeat for 5 times.

Direct Bending Procedure

i)place and align the sample on the setup

ii)-zero displacement-no bending I-V measurement with probe tips

iii)-remove probe tips from touch-pads to a safe point

iv)-(+)5µm prescribed displacement of the bottom pins

v)-place probe tips on the touch-pads and take I-V measurement four times

vi)-remove probe tips from touch-pads to a safe point

vii)-(+)5µm prescribed displacement of the bottom pins (10µm in total)

viii)-place probe tips on the touch-pads and take I-V measurement four times

ix)-remove probe tips from touch-pads to a safe point

x)-(+)5µm prescribed displacement of the bottom pins (15µm in total)

xi)-place probe tips on the touch-pads and take I-V measurement four times

xii)-remove probe tips from touch-pads to a safe point

xiii)-(-)15µm prescribed displacement of the bottom pins to the "no bending position" and wait 10 seconds

xiv)-Repeat the previous steps four times