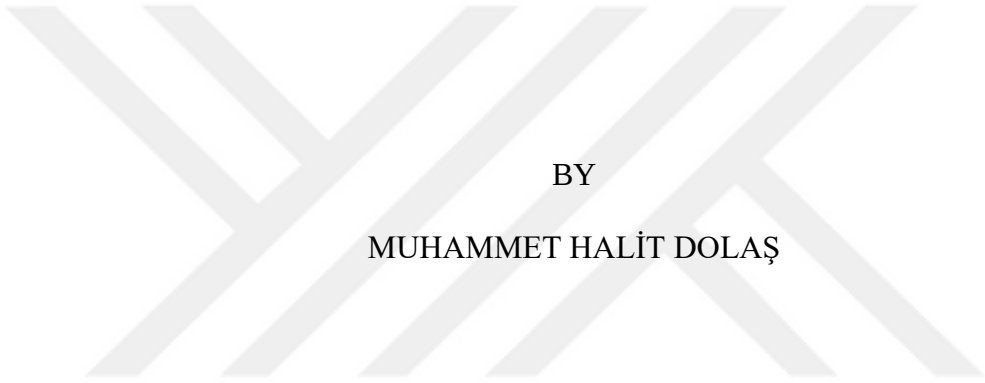


DARK CURRENT OPTIMIZATION DESIGNS FOR MESA AND PLANAR
TYPE PROCESSED SHORT WAVELENGTH INFRARED
PHOTODETECTORS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
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BY
MUHAMMET HALİT DOLAŞ

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
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IN
MICRO AND NANOTECHNOLOGY

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Approval of the thesis:

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TYPE PROCESSED SHORT WAVELENGTH INFRARED
PHOTODETECTORS**

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I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

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ABSTRACT

DARK CURRENT OPTIMIZATION DESIGNS FOR MESA AND PLANAR TYPE PROCESSED SHORT WAVELENGTH INFRARED PHOTODETECTORS

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Doctor of Philosophy, Micro and Nanotechnology
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This thesis aims to report novel designs to achieve lower dark current values for modified pin heterojunction InGaAs/InP SWIR photodiodes for both mesa and planar type production methodologies. Mesa type studies cover novel passivation methodology based on a fully depleted thin p-InP layer. Mesa structured detectors are targeted due to their competitive advantages for applications such as multicolor/hyperspectral imaging. Test detector pixels with different perimeter/area ratios are fabricated with and without etching the thin InP passivation layer between pixels in order to comparatively examine passivating behavior. I-V characteristics of the test detectors are measured at room temperature. Based on the results from differently sized pixel groups, bulk and surface dark current components are separated. Results show that thin InP layer decreases dark current by a factor of 3 while increasing photo current due to higher carrier collection efficiency

Planar type studies with developing novel epilayer structures, junction depth optimization and successful suppression of surface and bulk generation and recombination (GR) dark current components resulted in diffusion current limited high performance planar type SWIR detectors. For 15 μm pixel pitch, we obtained

12 fA pixel dark current at room temperature ($\sim 26^{\circ}\text{C}$) and 1.08 A/W responsivity (at $1.55\text{ }\mu\text{m}$) that is corresponding 86% quantum efficiency (QE). Dark current modeling analysis is performed based on bias dependency of diffusion, GR and tunneling current components. Results show excellent match with experimental data. Utilizing the developed planar type detectors with the state-of-the-art performance, post process optimizations also completed which result high performance megapixel SWIR imaging sensors with record level operability.

Keywords: SWIR, InGaAs, Low Dark Current, Pin Heterojunctions, Photodiodes



ÖZ

MESA VE PLANAR YAPILI KISA DALGABOYU KIZILÖTESİ DEDEKTÖRLERİN KARANLIK AKIM OPTİMİZASYON TASARIMLARI

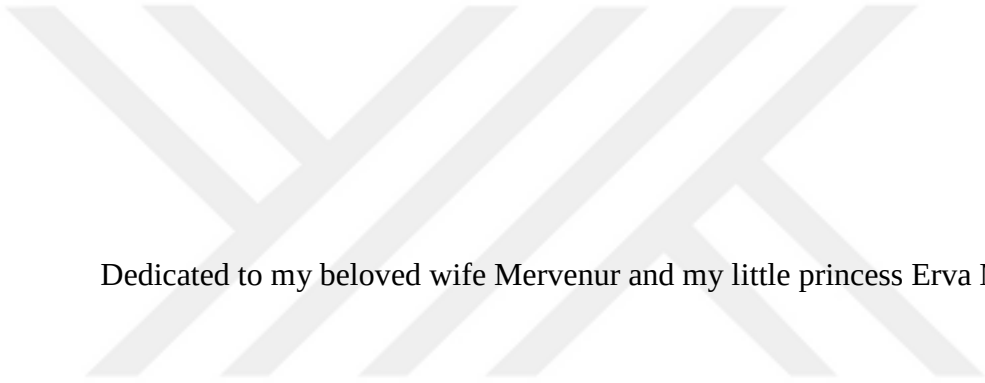
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Bu tez çalışması, mesa ve planar tipte üretilen pin heteroeklem yapısındaki InGaAs/InP bazlı SWIR fotodiyotların karanlık akım seviyelerinin optimize edildiği özgün tasarımları raporlamaktadır. Mesa tip dedektörler için yapılan çalışma kapsamında geliştirilen özgün pasivasyon çalışması, tamamen boşalmış bölge içerisinde kalan p tipi katkılanmış ince InP tabakasının geliştirilmesi temeline dayanmaktadır. Mesa tipindeki dedektörler multi renk, hiperspektral görüntüleme gibi uygulamalar için kullanılmaktadır. Yapılan çalışma kapsamında pasivasyon etkisinin izlenilebilirliği için, tamamı boşalmış bölge içerisinde bulunan InP katmanının aşındırıldığı ve aşındırılmadığı durumların karşılaştırmalı olarak çalışılabileceği, değişik boyut ve sayılarda test dedektörleri üretilmiştir. Test dedektörlerinin I-V karakterizasyonları oda sıcaklığında yapılmıştır. Değişik boyut ve sayılarda üretilen test dedektörleri kullanılarak karanlık akımın hacim ve yüzey bileşenleri ayrılmıştır. Sonuçlar ışığında geliştirilen özgün pasivasyon yaklaşımının yüzey karanlık akım bileşenini baskılayarak genel karanlık akımı 3 kata kadar azalttığı görülmüştür.

Planar yapılı dedektörler için yapılan çalışmada ise geliştirilen özgün epikatman yapısı ile boşalmış bölge derinliği ve katkılama seviyelerinin optimize edilmesi sayesinde karanlık akımın hacim ve yüzey bileşenleri beraber düşürülmüştür. Üretilen 15 µm adımlı pikseller için piksel başına oda sıcaklığında 12 fA karanlık akım ve %86 kuantum verimliliğine karşılık gelen 1.08 A/W tepkisellik elde edilmiştir. Karanlık akım, difüzyon, GR ve tünelleme akım bileşenlerine ayrılmıştır ve modelleme çalışmalarında deneysel çalışmalarla birebir örtüşen sonuçlar elde edilmiştir. Üretilen ve dünya standartlarında en yüksek performansa sahip olan dedektörlerden biri olan bu planar yapılı dedektörler ile temiz oda prosesi sonrasındaki hibritleştirme adımları da optimize edilerek rekor seviyede işlerliğe sahip hibrit sensör geliştirilmiştir.

Anahtar Kelimeler: SWIR, InGaAs, Düşük Karanlık Akım, Pin Heteroeklem, Fotodiyot



Dedicated to my beloved wife Mervener and my little princess Erva Mina

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CHAPTER 1

INTRODUCTION

1.1. Theoretical Background

1.1.1. Photodiode Basics

Bandgap formation between valance and conduction bands in semiconductors, makes them suitable candidates for photon absorbing applications [1], [2]. A photon with greater energy than the bandgap of a semiconductor can give its energy to a valance band electron that jumps to the conduction band [3], [4]. Remaining place for this jumped electron in the valance band creates a hole. Therefore, a conduction band electron and a valance band hole pair (e-h pair) are created in a semiconductor as a result of absorbing a photon [5].

Created e-h pairs tend to recombine after absorption of a photon unless they are separated with high enough electric field [6]. One of the most effective way to separate this optically created e-h pairs, thus creating the external circuit photo-current, is to make use of the built-in electric fields provided in a photodiode [7].

A photodiode is a junction of p type and n type doped semiconductor materials. Majority carriers i.e. electrons in the n type and the holes in the p type semiconductors, diffuse around the junction as they leave ionized immobile impurity atoms that are positively charged donor atoms for the n side and negatively charged acceptor atoms for the p side. These donors and acceptors create a built-in electric field which limits the further diffusion of majority carriers. At the steady state, a region without charge carriers i.e. depletion region is formed around the junction as it is illustrated in Figure 1.1.

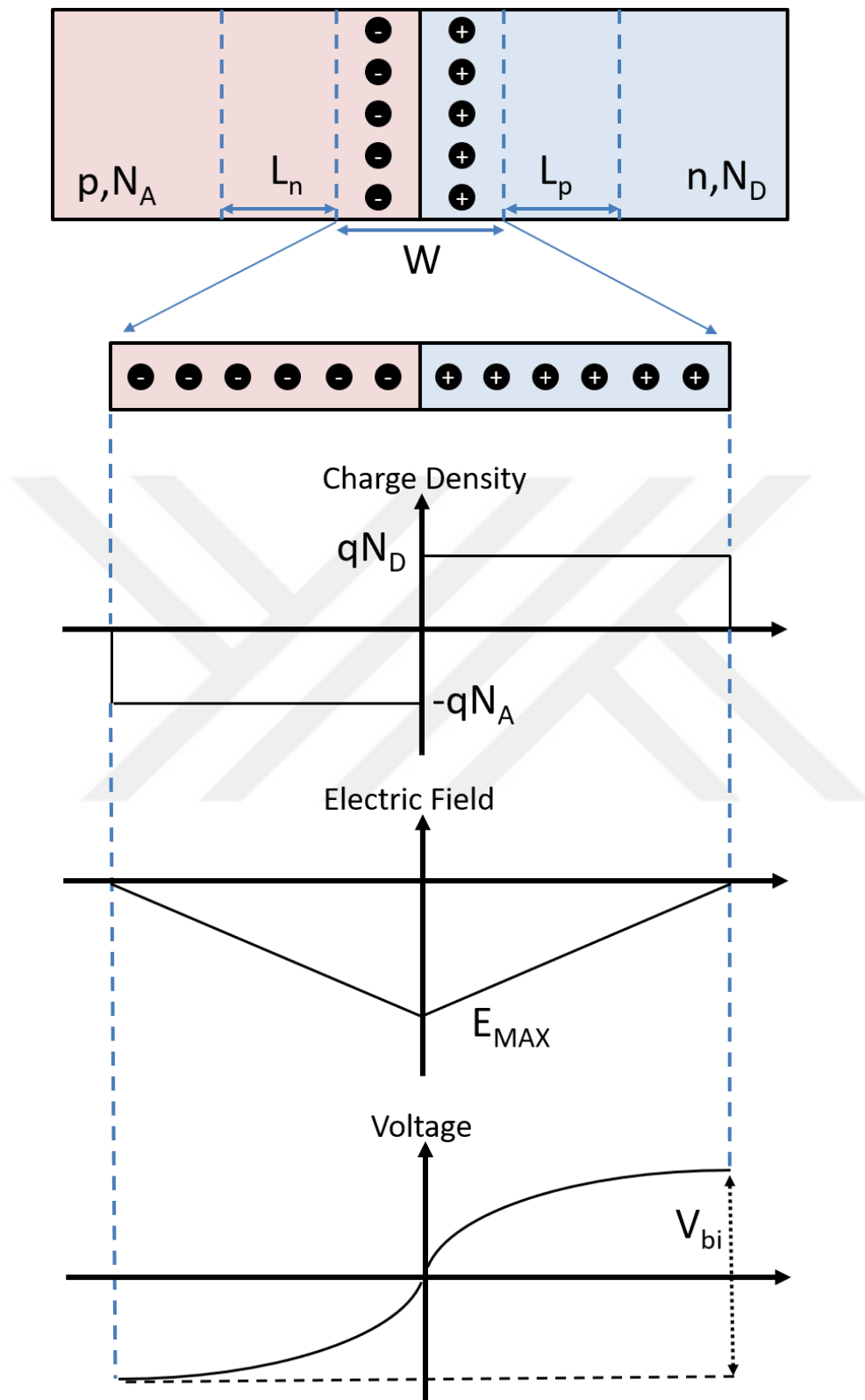


Figure 1.1. Illustration of a pn diode and corresponding depletion region properties

In Figure 1.1, N_A and N_D denote the doping levels of p and n sides respectively, W is the thickness of the depletion region, L_n and L_p are the thicknesses of the region that a minority carrier (electrons in p side and holes in n side) can diffuse to the depletion region. E_{MAX} is the maximum built in electric field and V_{bi} is the built-in voltage. Let x_n and x_p be the thicknesses of depletion region in n and p sides respectively;

$$W = x_n + x_p \quad 1.1$$

Since the number of positive and negative ions in the depletion region is same,

$$N_D x_n = N_A x_p \quad 1.2$$

$$W = x_n \left(1 + \frac{N_D}{N_A} \right) \quad 1.3$$

E_{MAX} and V_{bi} can be estimated as,

$$E_{MAX} = \frac{q N_D x_n}{\epsilon} \quad 1.4$$

$$V_{bi} = - \int_{-x_p}^{x_n} E dx = \frac{1}{2} W E_{MAX} \quad 1.5$$

Where q is the electron charge and ϵ is the dielectric constant. From Eq. 1.3, 1.4 and 1.5, W can be estimated as,

$$W = \sqrt{\frac{2\epsilon(N_A + N_D)V_{bi}}{qN_A N_D}} \quad 1.6$$

In terms of carrier transport, we have two different mechanisms as diffusion and drift. Majority carrier gradients between n and p type material creates diffusion current where the current formed because of built-in electric field causes the drift current. We can define drift and diffusion current mechanisms for n and p type carriers as,

$$I_{ndrift} = qAn\mu_n E \quad 1.7$$

$$I_{ndiff} = qAD_n \frac{dn}{dx} \quad 1.8$$

$$I_{pdrift} = qAp\mu_p E \quad 1.9$$

$$I_{pdiff} = -qAD_p \frac{dp}{dx} \quad 1.10$$

Where A is the cross-sectional area, μ_n and μ_p are mobilities, D_n and D_p are diffusion coefficients of the electron and the hole respectively. Under zero external bias, net current for both carriers is zero at equilibrium. Either one of the equations for both carriers can lead us to find built-in voltage. Let us continue with net hole current,

$$I_p = I_{pdrift} + I_{pdiff} = 0 \quad 1.11$$

$$I_{pdrift} = I_{pdiff} = 0 \quad 1.12$$

From equations 1.9, 1.10 and 1.12, for zero hole current, drift and diffusion hole currents must cancel each other,

$$p\mu_p E = D_p \frac{dp}{dx} \quad 1.13$$

We can write D_p as,

$$D_p = \frac{\mu_p kT}{q} \quad 1.14$$

Where, k is the Boltzmann constant and T is the temperature. From equation 1.13 and 1.14 we find,

$$E = -\frac{kT}{q} \frac{dp}{dx} = -\frac{dV}{dx} \quad 1.15$$

We can define n_n as equilibrium electron density and p_n as equilibrium hole density in n side, p_p as equilibrium hole density and n_p as equilibrium electron density in p side. Equation 1.15 becomes,

$$\int_{V_p}^{V_n} dV = -\frac{kT}{q} \int_{p_p}^{p_n} \frac{dp}{p} \quad 1.16$$

Which yields,

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{p_p}{p_n}\right) \quad 1.17$$

Where we can write equation 1.17 in terms of N_A and N_D as,

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \quad 1.18$$

Where, n_i is the intrinsic carrier concentration.

With equation 1.6 and 1.18 we define equilibrium conditions. There are two other operational modes under external bias as forward bias for which p side is positively biased and reverse bias for which p side is negatively biased. With the depletion region model we used we assume that the voltage drop only occurs at depletion region and other regions are remained as charge neutral regions. With this model, to estimate depletion region thickness in these external bias conditions we can simply add external bias to the built-in voltage;

$$W = \sqrt{\frac{2\varepsilon(N_A + N_D)(V_{bi} + V_R)}{qN_A N_D}} \quad 1.19$$

$$W = \sqrt{\frac{2\varepsilon(N_A + N_D)(V_{bi} - V_F)}{qN_A N_D}} \quad 1.20$$

To estimate the current flow in external bias conditions, first check what happened to drift and diffusion current components. Drift current is generally related to the carrier generation in the depletion region. Although external bias changes the total electric field in the depletion region, the generation rate of the electron-hole pairs won't be affected too much so, the change in drift current for both reverse and forward bias conditions will be insignificantly small. However, for diffusion current,

in reverse bias condition, depletion region width increases which leads to an important decrease in majority carrier diffusion current and in contrast to reverse bias, in forward bias condition, depletion region width is decreased which leads to an important increase in diffusion current. Therefore, overall current flowing through the diode for reverse bias will be dominated with drift current that slightly changes with increasing reverse bias voltage and overall current for forward bias will be dominated with diffusion current which is significantly increases with increasing forward bias voltage.

To reach the current equation under the external bias, first rewrite equation 1.17 as,

$$p_n = p_p e^{\frac{-qV_{bi}}{kT}} \quad 1.21$$

Under the forward bias,

$$p(x_n) = p(-x_p) e^{\frac{-q(V_{bi}-V_F)}{kT}} \quad 1.22$$

Majority carrier concentration changes insignificantly for external bias, so $p(-x_p)$ is equal to p_p . Therefore,

$$p(x_n) = p_p e^{\frac{-q(V_{bi}-V_F)}{kT}} = p_n e^{\frac{qV_F}{kT}} \quad 1.23$$

Similarly,

$$n(-x_p) = n_p e^{\frac{qV_F}{kT}} \quad 1.24$$

Before writing the net current, we need to define excess carrier concentrations (δn , δp) by solving the diffusion equation;

$$\frac{\partial(\delta n)}{\partial t} = D_n \frac{\partial^2(\delta n)}{\partial x^2} - \frac{\delta n}{\tau_n} \quad 1.25$$

$$\frac{\partial(\delta p)}{\partial t} = D_p \frac{\partial^2(\delta p)}{\partial x^2} - \frac{\delta p}{\tau_p} \quad 1.26$$

General solutions for equations 1.25 and 1.26;

$$\delta p(x) = C_1 e^{\frac{x_n}{L_p}} + C_2 e^{-\frac{x_n}{L_p}} \quad 1.27$$

$$\delta n(x) = C_3 e^{\frac{x_p}{L_n}} + C_4 e^{-\frac{x_p}{L_n}} \quad 1.28$$

Where,

$$L_p = \sqrt{D_p \tau_p} \quad 1.29$$

$$L_n = \sqrt{D_n \tau_n} \quad 1.30$$

Boundary conditions at infinity requires C_1 and C_3 are equal to zero and conditions from equation 1.23 and 1.24 gives the solution as,

$$\delta p(x_n) = p_n \left(e^{\frac{qV_F}{kT}} - 1 \right) e^{-\frac{x_n}{L_p}} \quad 1.31$$

$$\delta n(x_p) = n_p \left(e^{\frac{qV_F}{kT}} - 1 \right) e^{-\frac{x_p}{L_n}} \quad 1.32$$

Hole current at $x_n=0$ and electron current at $x_p=0$ can be written as,

$$I_p = -qAD_p \frac{d\delta p}{dx_n} \quad 1.33$$

$$I_n = -qAD_n \frac{d\delta n}{dx_p} \quad 1.34$$

We write the total current as the sum of hole and electron current. From equation 1.31, 1.32, 1.33 and 1.34 we reach,

$$I = qA \left(\frac{L_p}{\tau_p} p_n + \frac{L_n}{\tau_n} n_p \right) \left(e^{\frac{qV_F}{kT}} - 1 \right) \quad 1.35$$

Equation 1.35 under reverse bias will yield reverse saturation current as,

$$I_s = qA \left(\frac{L_p}{\tau_p} p_n + \frac{L_n}{\tau_n} n_p \right) = qA \left(\frac{L_p}{\tau_p} \frac{n_i^2}{N_D} + \frac{L_n}{\tau_n} \frac{n_i^2}{N_A} \right) \quad 1.36$$

Equation 1.36 is the ideal diode reverse bias current [8].

Above equations define a pn diode with same semiconductor materials for n and p type regions i.e. homojunction [9]. Higher quality devices can be possible when different materials are used for n and p type regions i.e. heterojunction [10]. For a heterojunction device, with the absorber semiconductor that the bandgap energy is small enough to absorb photons with intended wavelengths, it is possible to choose the other material which has higher bandgap energy. Thus, increasing the energy barrier that electrons must overcome and therefore decreasing the overall reverse bias saturation current [11].

Built-in voltage and the depletion region width for a heterojunction pn diode can be estimated with a similar approach we used for homojunctions. Equation 1.37 and 1.38 shows the final forms of built-in voltage and depletion region width in heterojunctions [10].

$$qV_{bi} = E_{gInGaAs} + \Delta E_v + kT \ln \left(\frac{N_A N_D}{N_{CInGaAs} N_{VInP}} \right) \quad 1.37$$

$$W = \sqrt{\frac{2}{q} \varepsilon_{InGaAs} \varepsilon_{InP} \frac{(N_A + N_D)^2}{N_A N_D} \frac{V_{bi}}{\varepsilon_{InP} N_A + \varepsilon_{InGaAs} N_D}} \quad 1.38$$

A pn heterojunction diode can be used as a high-quality photodetector under reverse bias conditions with low dark current values [12]. Photon absorber semiconductor material in the depletion region can absorb and separate photo-created electron-hole pairs. To increase the depletion region thickness to absorb more photons, pin diodes which includes an intrinsic “i” layer between p and n type doped layers can be utilized. For a pin diode, absorber semiconductor material is placed in the intrinsic region which becomes fully depleted [13]. Another significant property of pin

photodiodes is increased reverse breakdown voltages [14] and decreased tunneling currents [15].

1.1.2. Figure of Merits

In literature, there are quite number of different figure of merits to be able to compare performances of photodetectors [16]. The motivation is to be able to compare different detectors (sizes, active areas etc.) with different measurement conditions (temperatures, optics, light wavelengths etc.). After all, what really matters, assuming same external conditions, is basically increasing the signal to noise ratio which mostly depended on increasing the responsivity and decreasing the dark current. In this thesis, we focused on both and our comparative results are chosen between detectors with similar external conditions. Thus, for figure of merits, we focused on most basic elements.

1.1.2.1. Dark Current

The current of a photodiode in the absence of light called as a dark current [17]. Dark current is one of the main components of a photodiode noise. Another negative effect caused because of high dark current values is filling the read-out capacity. To increase overall performance of a photodiode, reducing the dark current is a never ending story [18].

Main elements of the dark current can be listed as, diffusion current, generation and recombination (GR) current, tunneling currents and surface leakage current [19]. Decreasing the overall dark current requires separate effort for each component.

Diffusion Current

Diffusion current is the ideal diode current that is also called as reverse bias saturation current. In the previous part of the thesis we showed that this current component can be defined as in the equation 1.36. For a reverse bias photodiode, diffusion current can be modelled as it is independent of the bias voltage. To reduce the diffusion current, easiest way is optimizing the doping densities. In $p^+i(n)$ junctions that the detectors developed for this thesis work also have, diffusion current

is dominated by N_D term while N_A term can be neglected since $N_A \gg N_D$. Thus, increasing the n type doping for intrinsic layer in pin structure can reduce the diffusion current. On the other hand, an optimum doping value should be found otherwise, depletion region thickness becomes smaller and tunneling currents can be problem to some extent.

Generation and Recombination (GR) Current

Current from the generation and recombination of e-h pairs through the device with radiative or non-radiative mechanisms creates the GR current. In pin photodiodes, GR current formed by SRH (Shockley-Read-Hall [20], [6]) mechanism in the depletion region is the dominating factor with the existence of the built-in electric field that separates created e-h pairs [21].

GR current in the depletion region of a pin diode can be defined as [22];

$$I_{GR} = \frac{qn_i W}{\sqrt{\tau_n \tau_p}} \frac{2 \sinh\left(\frac{qV}{2kT}\right)}{\frac{q(V_0 - V)}{kT}} Af(b) \quad 1.39$$

Where,

$$f(b) = \int_0^\infty \frac{dx}{x^2 + bx + 1} \quad 1.40$$

With b defined as;

$$b = e^{\frac{-qV}{2kT}} \cosh\left[\frac{E_t - E_i}{2kT} + \frac{1}{2} \ln\left(\frac{\tau_n}{\tau_p}\right)\right] \quad 1.41$$

Here, E_t is the energy level of the generation and recombination center and E_i is the fermi energy level for an intrinsic semiconductor. Generation and recombination probability is maximum for a trap energy level that is equal to half of the band for an intrinsic semiconductor [23], [24]. So, assuming $E_t = E_i$, $\tau_n = \tau_p = \tau_{GR}$, we can simplify GR current as,

$$I_{GR} = \frac{qn_iWA}{2\tau_{GR}} \quad 1.42$$

From equation 1.42, bias dependency of a GR current mechanism comes from the depletion region width term which is increasing proportional to the square root of the total reverse bias.

GR current also effects forward bias characteristics [25]. While forward bias diffusion current exponentially increases with $\frac{qV}{kT}$ term as shown in the equation 1.35, forward bias GR current exponentially increases with $\frac{qV}{2kT}$. Based on forward bias characteristics, ideality factor “n” is defined as the exponential change in forward bias denoted by $\frac{qV}{nkT}$. The more the ideality factor is close to 1, detector become closer to an ideal detector with high purity crystal material that is consisting very low density of activated GR traps especially in the depletion region [26], [27].

To deal with the GR current, most important factor is having high crystal purity as expected. Another effective way is the decreasing the width of the depletion region. For a p+ i(n) junction, depletion region width can be decreased with increasing N_D as similar to the case in diffusion current.

Tunneling Currents

A carrier always has a non-zero probability to tunnel through the semiconductor band gap. The related e-h pair generation or recombination creates a tunneling current that weakly depends on temperature [28]. There are mainly two types of tunneling currents as band to band tunneling (BBT) and trap assisted tunneling (TAT) [29]. In BBT, carrier tunnels directly through the band gap while in TAT tunneling occurs with the help of a trap as illustrated from Figure 1.2. For BBT, valance and conduction band energies of the p and n sides need to become around same energy level. Therefore, to trigger BBT, reverse bias should be higher than that of TAT. For a p+ i(n) junction with low doping levels in the n side, main tunneling current mechanism is the TAT current [30], [31].

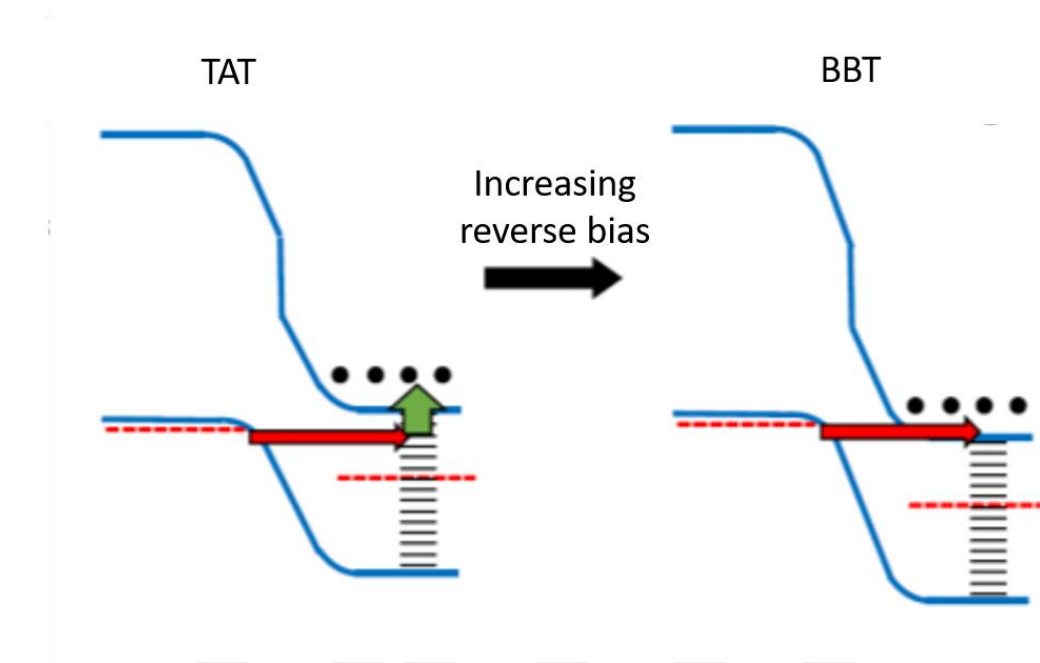


Figure 1.2. Illustration of tunneling current types [32].

TAT current can be defined as [22];

$$I_{TAT} = qN_tAW \left(\frac{1}{\alpha_p p_l + w_v N_v} + \frac{1}{w_c N_c} \right)^{-1} \quad 1.43$$

Where α_p is the hole recombination coefficient for the trap, w_v and w_c are tunneling probabilities from the trap to the valance and conduction bands, N_v and N_c are the effective densities of the valance and conduction bands, N_t is the trap density and p_l can be expressed as;

$$p_l = N_v e^{\frac{-E_t}{kT}} \quad 1.44$$

When $\alpha_p p_l \gg w_c$ and $w_c N_c$ is similar to $w_v N_v$, we can write simplified version of equation 1.43 as;

$$I_{TAT} = qN_tAw_cN_cW \quad 1.45$$

If we assume uniform electric field, $w_c N_c$ can be expressed as,

$$w_c N_c = \frac{\pi^2 q m^* E M^2}{h^3 (E_g - E_t)} e^{-\frac{\left(\frac{m^*}{2}\right)^2 E_g^2 F(a)}{2 q E \hbar}} \quad 1.46$$

Where M is the matrix element and $F(a)$ can be written as;

$$F(a) = \frac{\pi}{2} - a\sqrt{1-a^2} - \sin^{-1} a \quad 1.47$$

with a defined as,

$$a = 2 \frac{E_t}{E_g} - 1 \quad 1.48$$

TAT current is exponentially increasing with increasing reverse bias voltage. As per its high bias dependency, in dark current versus reverse bias spectrum, it suddenly dominates the dark current. To have this triggering point in the higher bias values, doping values of the pn junction should be lowered. pin structure with an intrinsic addition between p and n regions reduces the tunneling currents significantly. On the other hand, p⁺i(n) junction with low level n type doping to decrease diffusion and GR currents can trigger TAT current at lower bias values.

Surface Leakage Currents

Basic mechanisms for surface leakage currents are similar to that of the bulk current mechanisms [33]. Theoretical expressions on the other hand changes since the surface has many impurities and dangling bonds [34]. Also surface quality strongly depends on processing conditions. Therefore, in the case on a strong surface current domination, separation of the current mechanisms from overall dark current is a tough work. What could be done in such a case is first separating bulk and surface related dark current contribution with utilizing detector pixels with different sizes. Alternative ways to do it will be detailed in the following chapters that we discuss the results we obtain from the detectors developed for this thesis work.

An important aspect related to the surface current is the surface cleaning conditions and dielectric passivation [35]. Both will be discussed in corresponding process development chapters of this thesis.

1.1.2.2. Responsivity and Quantum Efficiency

Responsivity is defined as photo response of a detector under illumination and expressed as;

$$R = \frac{I_{photo}}{\Phi} \quad 1.49$$

Where, Φ is the optical power received by detector. The unit for the responsivity is A/W. Another related figure of merit is the quantum efficiency which is denoted by the symbol “ η ”. Quantum efficiency is a measure of detected number of electrons over received number of photons. For an ideal detector quantum efficiency is equal to 1. That means for every photon received, an electron is created and detected. In a real life photodiode quantum efficiency is less than one because of limitations as reflection of light, recombination of created e-h pairs or partial absorption due to not thick enough absorber layers [36]. Quantum efficiency in terms of responsivity can be expressed as [37];

$$R = \eta \frac{\lambda}{1.24} \quad 1.50$$

Where, λ is the wavelength of incident light in micrometers.

Absorption of light in semiconductors as the function of skin depth can be expressed as [38], [39];

$$I(z) = I_0 e^{-\alpha z} \quad 1.51$$

Where I is the transmitted light intensity as a function of depth in semiconductor, I_0 is the incident light intensity at $z=0$ and α is the absorption coefficient of semiconductor. Based on equation 1.51, required absorber thickness can be determined.

1.1.2.3. Noise and Background Limited Performance

Noise can be defined as the unwanted and uncontrolled random fluctuations in the measured signal [40]. Main noise mechanisms in pin photodiodes can be listed as dark current noise, photon (shot) noise, Johnson noise and capacitor noise [41]. Dark current noise and photon noise can be expressed as similar expressions as;

$$i_n = \sqrt{2qI} \quad 1.52$$

Where, i_n is the noise current spectral density, I is the total current (I_{dark} or I_{photo}). Johnson noise can be expressed as;

$$i_n = \sqrt{\frac{4kT}{R}} \quad 1.53$$

Where, R is the resistance. Capacitor noise, in terms of electrons, can be expressed as;

$$q_n = \sqrt{kTC} \quad 1.54$$

Where, C is the depletion capacitance.

Addition to this noise mechanisms, an electronic read-out noise can be defined for the electronic elements needed for photodiode operation. When the shot noise become the dominating noise mechanism, detector reaches the background limited performance. For this kind of an operation, further decrease in other noise mechanisms cannot increase the overall detector performance.

To decrease the detector noise, especially for low light level applications and assuming low read-out noise, dark current and Johnson noise is the remaining noise mechanisms. Dark current of such a detector should be decreased as the dark current noise become lower than the Johnson noise. At that point, decreasing the temperature can be a solution for further performance enhancement.

1.2. Infrared Imaging

The history of infrared imaging technology is started with the discovery of infrared radiation in 1800 by Herschel [42]. He was using a prism to separate sun light into colors and checking the temperature increase in thermometers that he assigned for each color. He found that temperature is increased most for a thermometer placed the invisible part after the red light. After Herschel discovery, infrared detectors are started to improve [43] and for today's technology, with enormous number of applications from medical, industrial and military fields, infrared imaging undeniably become one of the most significant topics [44].

We can divide infrared detectors into two main categories as thermal detectors and photon detectors. Thermal detectors basically change their temperatures after absorbing the light and this change is measured to reach absorbed light data [45]. For photon detectors, e-h pairs are created and separated after absorbing photons and resulted current is measured [46]. For high quality infrared imaging, bolometers from thermal detectors side and photoconductors/photodiodes from the photon detectors side are commonly used devices.

1.2.1. Infrared Sub Bands

Infrared imaging is divided into sub-bands due to the atmospheric considerations. Photons with specific wavelengths cannot propagate long distances due to the absorption of molecules in the atmosphere. Figure 1.3 shows the atmospheric attenuation in infrared spectrum [47].

Sub bands of infrared spectrum can be defined based on the wavelengths of light. Short wavelength infrared (SWIR) band stands between 1-1.7 μm , extended short wavelength infrared (ex-SWIR) band stands between 1-2.5 μm , middle wavelength infrared (MWIR) band stands between 3-5 μm and long wavelength infrared (LWIR) band stands between 8-12 μm .

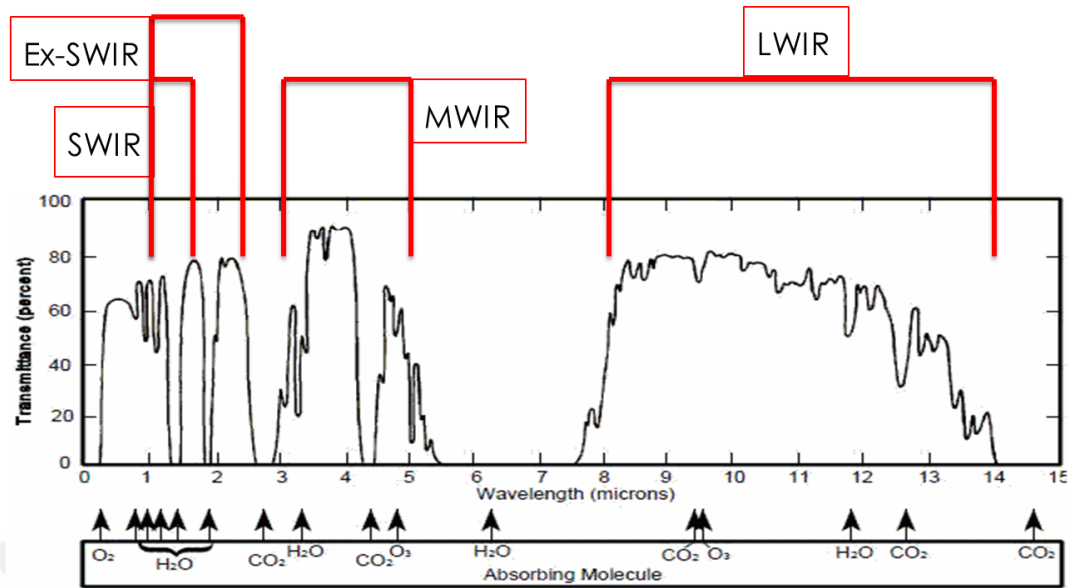


Figure 1.3. Infrared absorption spectrum of atmosphere [47].

1.2.2. Black Body Radiation and Airglow

All materials absorb, transmit and reflect light. In thermodynamic equilibrium point, all absorb radiation energy should be emitted [48] [49]. This emission is called as a black body radiation and it depends on the temperature of the material [50]. An ideal black body absorbs all energy from incident radiation independent of the wavelength of light and emit the absorbed energy as a radiation of light in specific wavelengths based on its temperature as given in Figure 1.4 [51].

Room temperature objects radiates light in infrared region with wavelengths above $2\mu\text{m}$. Based on this radiation, infrared imaging above $2\mu\text{m}$ wavelengths called as thermal imaging [52] [53]. Since all objects around room temperature are self-radiating light sources for MWIR and LWIR band, image contrast for these bands comes from the temperature difference between the objects. On the other hand, for SWIR band, imaging can be done by detecting the reflected lights from objects similar to the visible imaging. Thus, SWIR imaging needs a light source.

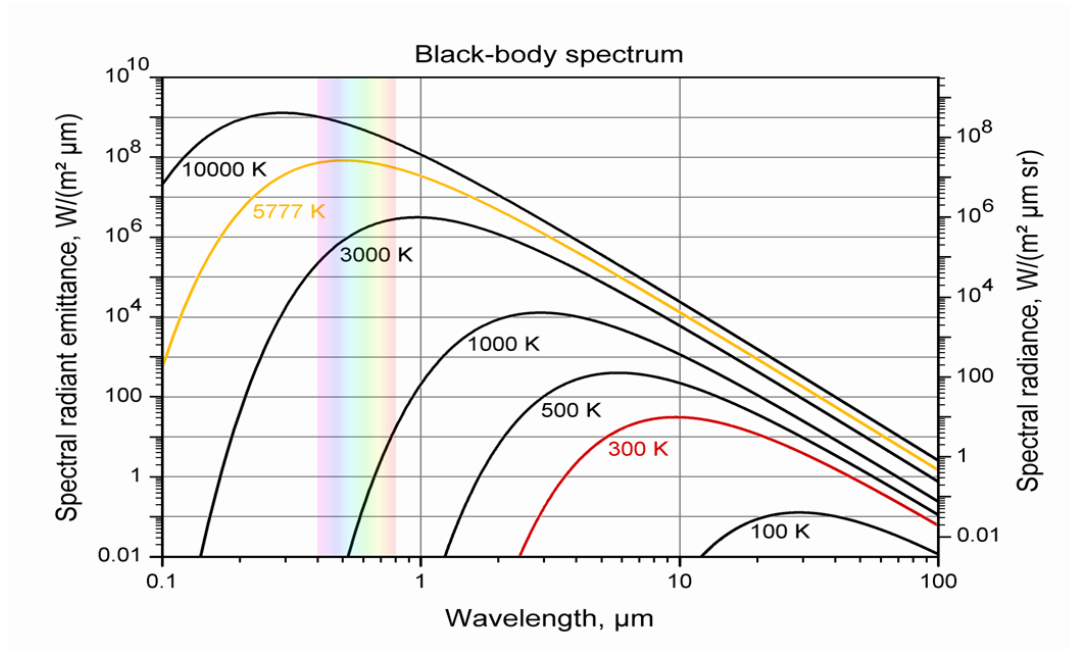


Figure 1.4. Black body radiation spectrum of objects with various temperatures [54].

Sun is a powerful light source for daylight SWIR applications. For nights, active illumination or passive detection with making use of the airglow can be a solution [55]. Airglow is the phenomenon describing the relaxation of hydroxyl groups located in the upper atmosphere which are excited during the day [56] [57].

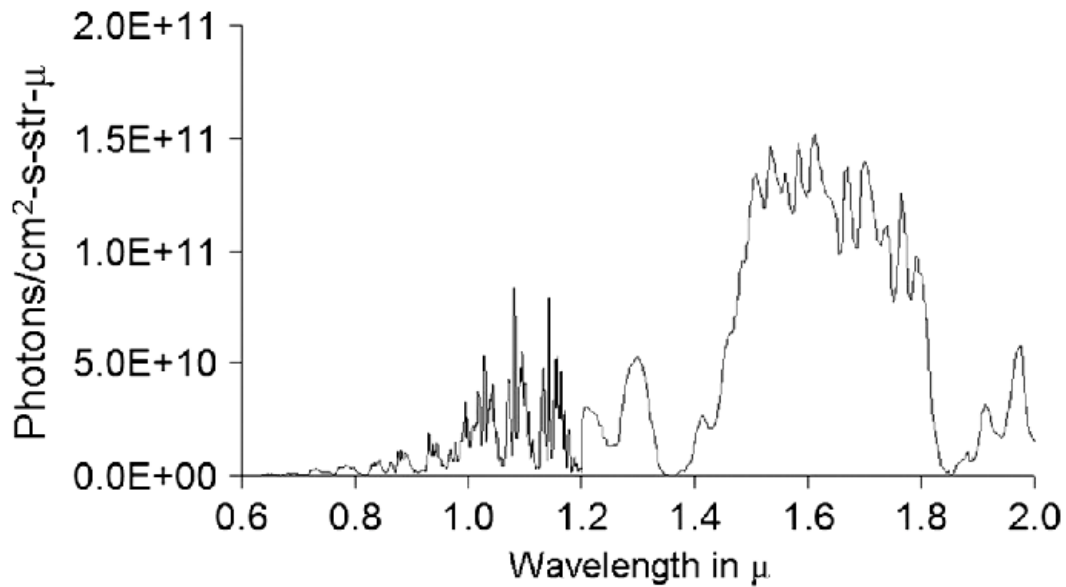


Figure 1.5. Airglow spectrum in SWIR band [55].

Figure 1.5 shows the infrared spectrum of the airglow.

1.2.3. Focal Plane Arrays and Read Out Integrated Circuits

Focal plane array (FPA) is basically an array of large number of photodetectors that is placed at the focal plane of an optical imager [58]. Optics create an image of the area it sees based on its field of view at its focal plane. Photodetectors on the FPAs that are located at this focal plane creates different signal values with incoming different number of photons on them. These different signals are gathered one by one by a read out integrated circuit (ROIC) and brightness of screen pixels for each corresponding FPA pixels are arranged as they formed the image on the screen [59]. The format of the image is labelled based on the pixel numbers and formation on the FPAs as 640x512 or 1280x1024. Of course, ROICs have same number or pixels. If the FPA and ROIC is created in the same semiconductor material, they are called as monolithic detectors which is common for Silicone detectors as large portion of ROICs are made of Silicone [60]. FPAs with different semiconductor materials are generally hybridized to Silicone ROICs by several processing techniques.

1.3. SWIR Imaging

Considering the different working principles of the imaging systems from visible to LWIR bands, a direct comparison is never a good way of characterizing these imaging systems. Yet, bringing up the differences can clarify some advantageous in specific conditions [61].

Detectors in short wave infrared (SWIR) band have relatively low dark current values due to the higher bandgap semiconductor materials compared to the other atmospheric windows in the infrared region. This minimizes the cooling requirement and it even enables room temperature operation [62].

Compact camera systems with small size optics without crossing the limitation of diffraction is another useful aspect of SWIR imaging. Minimum useful detector pixel pitch can be defined as [63];

$$r = 1.22\lambda f_{\#} \quad 1.55$$

Where, $f_{\#}$ is the focal length divided by the diameter of the aperture. Small $f_{\#}$ means larger optics. Since wavelength of light is smaller for SWIR band than MWIR and LWIR bands, higher $f_{\#}$ compact optics are possible for a same pixel pitch detectors [64].

Another operational level advantage of SWIR imaging is the naturally formed image contrast that provides very good results in the applications as face recognition [65], [66]. For thermal imagers, since contrast is created with the temperature differences, specific properties of an object as face of a person would become temperature dependent. In SWIR imaging since the working principle is similar to the visible imaging with detecting the reflected light. Details of an objects becomes clearer and independent of most outer conditions like temperature [67]. Figure 1.6 shows the two images of the author of this thesis from SWIR and MWIR detectors. Naturally formed image contrast and details of the face in SWIR and MWIR images can be compared.



Figure 1.6. Image of the author of this thesis in SWIR (left) and MWIR bands.

Furthermore, considering the deeper penetration depth in SWIR band than in visible band, SWIR images can also provide information that is not distinguishable in visible imaging in situations such as food inspection [68], [69]. Figure 1.7 shows an image

of an apple that seems good in visible camera while SWIR image reveals the decayed parts.

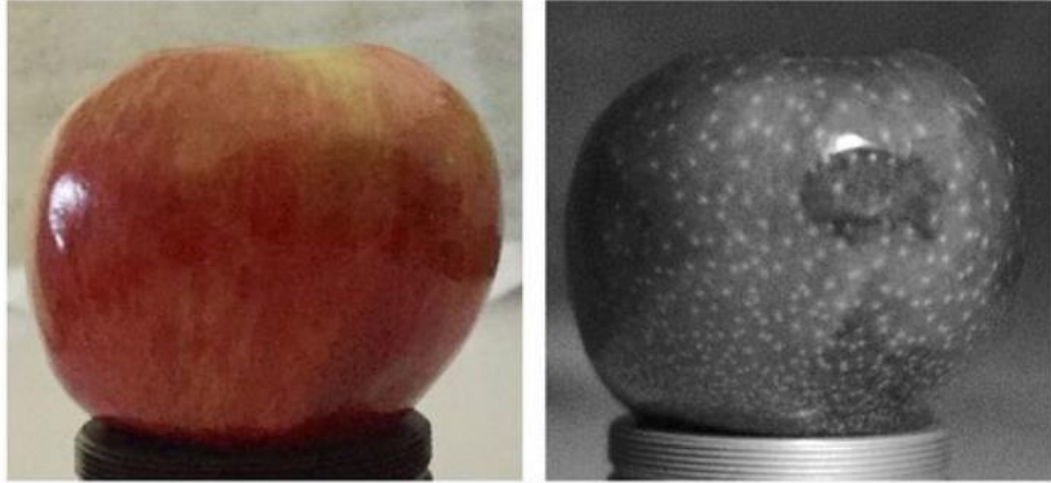


Figure 1.7. Image of an apple with SWIR and visible cameras.

Comparing the visible band, light in SWIR wavelengths can propagate longer distances in hard weather conditions which makes SWIR imaging a good candidate for surveillance applications [70], [71]. Also for newly emerging autonomous car applications SWIR detectors have impressive results [72]. Figure 1.7 shows SWIR and visible images of long-distance building under haze. In SWIR image, building can be clearly seen while it is impossible to see it in visible image.



Figure 1.8. SWIR and visible images under haze [73].

Space applications as telescopes are another important usage area for SWIR detectors [74], [75]. For this kind of applications, very low dark current values are must which would be crucial for very long integration times needed to catch even the smallest light coming from the space.

Among variety of semiconductor materials for SWIR detector production as Ge [76], [77], InSb [78], [79], HgCdTe [80], [81], and InGaAs [82], [83], InGaAs based detectors gives the higher performance between 1-1.7 μm band [84], [85], [86].

1.4. InGaAs/InP Lattice Matched SWIR Photodetectors

InGaAs, that is lattice matched to the InP for 0.53 indium mole fraction [87], is an ideally suited material for SWIR imaging. For simplicity, “InGaAs” will be used to refer “ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ” for the rest of this thesis. Bandgap energy of InGaAs is reported around 0.74 – 0.80 eV which corresponds to a cut-off wavelength around 1.7 μm [88] [89]. Cut-on wavelength is determined by the cut-off wavelength of InP corresponding around 950 nm.

High quality InP/InGaAs crystal growth can be realized by both molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) techniques. Epitaxy market for both type of techniques is available. In terms of epilayer design, pin heterojunctions are the most common detector types with InP p and n layers and InGaAs i(n) absorber layer. There are two main processing types as mesa and planar process.

Highest quality detectors with lower dark current values are produced with planar process for which InGaAs is buried under InP layer [90]. The reason for higher dark current values in mesa process is based on the fact that the surface of device is formed not only on InP but also on InGaAs absorber layer. InGaAs surface is hard to passivate due to surface instabilities [91] and it causes surface related dark currents which dominate the total dark current [92], [93]. However, there are some useful

applications which are only possible with mesa structure such as dual color/band applications [94], [95].

On-device passivation (passivation layer located on the p-n structure) of InGaAs surface in mesa structures can be applied by employing several materials as polyimide [96], Si₃N₄ or SiO₂ [92] and BCB [97], or employing cap layers as InP and InGaAsP [98], [99]. However, dark current usually remains high. To further suppress dark current, in-device passivation (passivation layer located inside p-n structure) methods seem to be a better option. For instance, barrier structures reduce the dark current, however the epilayer structure and the fabrication often get complicated [93]. Another alternative for in-device passivation could be n-type doped or an undoped depleted layer [100], but it is not applicable in InP/InGaAs case since undoped or n-type doped InP above InGaAs absorber acts as a hole barrier which also suppresses photocurrent.

1.5. Thesis Work

This thesis consists of 5 chapters and aims to report novel designs to achieve lower dark current values for modified pin heterojunction InGaAs/InP SWIR photodiodes for both mesa and planar type production methodologies.

In chapter 1, an introduction to the technology is provided. First, a theoretical background information about pn photodiodes is given with extracting the useful equations that helps to understand the discussions for higher performance device development. In following parts, infrared imaging is introduced considering atmospheric attenuation, SWIR, MWIR and LWIR sub bands and corresponding imaging technologies, black body radiation, FPA and ROIC chips. After, SWIR imaging is introduced with more detail as advantages, usage areas, material of choice for imaging. Lately, lattice matched pin structured InP/InGaAs based SWIR detectors with both mesa and planar processing types are introduced.

In Chapter 2, proposed dark current reduction approaches for mesa type detectors are detailed under design, process and characterization sub headings. In design part, both epilayer design and process design parameters are discussed. Details of conditions for a fair comparison is also discussed. In process part, every detail including the photolithography masks, process steps and details of the systems used are given. In characterization part, results of the necessary measurements and confirmation of the achievement of proposed novel approach is discussed. The laboratory work done for this chapter is mainly conducted in the Quantum Devices and Nanophotonics Research Laboratory in Middle East Technical University.

In Chapter 3, low dark current planar type detector development studies are given. The structure of the chapter is similar to the chapter 2 with design, process and characterization parts. In design studies, developed novel epilayer design with details of each layer is given. Process and layout design are also discussed. In process part, as similar for mesa detectors, every detail of planar type detector processing step is given. In characterization part, results of necessary measurement and estimations are given. Planar type detector studies resulted with the development of the state-of-the-art performance planar detectors. The laboratory work done for this chapter is mainly conducted in the Nanotechnology Research Center in Bilkent University.

In Chapter 4, post processing steps for FPA-ROIC hybrid sensors are given. The problems we faced during post processing and developed solutions are discussed. At the end of the chapter, sensors with the record operability values are achieved and corresponding sample images are given. The laboratory work done for this chapter is mainly conducted in the Nanotechnology Research Center in Bilkent University.

In Chapter 5, Conclusion of the studies covered in this chapter and possible future works are discussed.

CHAPTER 2

MESA TYPE DETECTORS

2.1. Design

Design studies will be examined under three sub-headings as epi-layer design, layout design, detector process steps & photomask design and, fan-out process steps & photomask design.

2.1.1. Epi-Layer Design

Standard mesa epi-layer structure consists of an absorbing InGaAs layer that is sandwiched in between p-InP and n-InP contact layers for which all required doping process is performed during the crystal growth. (Figure 2.1).

InP	p type doped	P layer
$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	undoped	Absorber Layer
InP	n type doped	N layer
InP SI Wafer		

Figure 2.1. Standard mesa epi-layer structure

Pixel isolation in mesa process is obtained by etching the p-InP layer around each detector pixel. Main problem associated with the mesa process is very high dark current values that are generally because of unearthing the InGaAs surface during pixel isolation etch. We focused on reducing dark current without harming photo

current and we achieved to show a working methodology with developed novel epi-layer test structure given in Figure 2.2 [101].

In _{0.53} Ga _{0.47} As	0.5 nm	p 1x10 ¹⁷ cm ⁻³	P layer
InP	50 nm	p 1x10 ¹⁷ cm ⁻³	Fully depleted layer
In _{0.53} Ga _{0.47} As	0.7 μm	n 1x10 ¹⁷ cm ⁻³	Absorber Layer
InP	0.3 μm	n 1x10 ¹⁸ cm ⁻³	N layer
InP SI Wafer			

Figure 2.2. Designed mesa epi-layer structure

Mainly, we aimed to keep the absorber InGaAs layer buried under the thin InP layer which is designed as it would be fully depleted even without external biasing which means that this layer is not needed to be etched for pixel isolation. Through the given epi-layer structure, details of the design and the key points that increase the performance of the standard structure will be examined under separate headings for each layer.

2.1.1.1. N-InP Layer

This layer is the layer on which the common n-type electrical contacts are to be coated. To allow the metal contacts to easily show ohmic properties, and to ensure common contact layer feature, this layer is designed to be n type doped during crystal growth around 1x10¹⁸ cm⁻³ levels. The thickness of this layer should be chosen as thick enough so that it can be used as a common contact layer and withstand the chemical etching to be done before metal coating. The 0.3 μm thickness determined in the final design is enough in this sense. On the other hand, higher thickness values are avoided to prevent further defect formations during crystal growth.

2.1.1.2. Absorber Layer

Absorber layer is composed of InGaAs. This layer is the place in which SWIR photons are absorbed and corresponding electron-hole pairs are created. To be able

to obtain maximum amount of absorption this layer needs to be around 2.5 μm thick. On the other hand, in our study, since we aimed to prove applicability of our dark current reduction methodology, we designed 0.7 μm thick absorption layer which is enough to test the proposed epi-layer performance.

2.1.1.3. Fully Depleted Layer

Fully depleted layer is the key point of the epi-layer design for dark current reduction. To better understand how this layer helps we need to reconsider the differences of mesa and planar type processing. In planar type processing InGaAs absorber layer remains buried under InP that has higher energy bandgap which means much lower surface dark current values. To be able to satisfy pixel isolation, only the n type doping is made during crystal growth and the p type doping is realized with local diffusion at top of each pixel. On the other hand, all required doping work is realized during crystal growth for mesa processing. That means for p on n formation, p type doped layers are needed to be totally etched at the region between pixels for isolation. To be able to keep InGaAs absorber buried like planar processing, we aim to create a thin InP layer that is remained totally in the depletion region. Since ideally there are no charge carriers in the depletion region, this layer would not needed to be etched away for pixel isolation. The important point when designing such a layer is not giving any harm to photo current transition. An energy bandgap simulation study is performed for different doping types for this fully depleted region as given in Figure 2.3 [102].

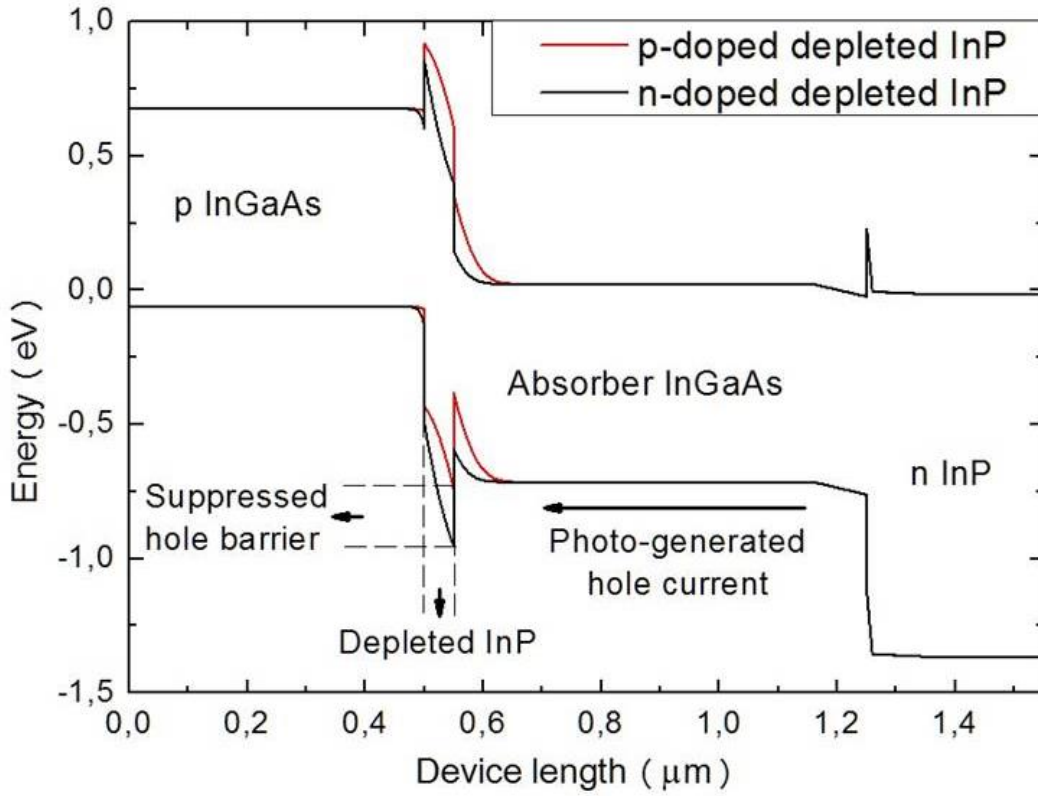


Figure 2.3. Energy band structure of designed epi-layer for different doping types of the fully depleted layer

We found that a hole barrier which may harm photo current is formed in the case of an n type doping but for p type doping we can provide smooth hole transition. Therefore, we chose to continue with the p type doping for the fully depleted InP region. To reduce the depletion GR current, we used $1 \times 10^{17} \text{ cm}^{-3}$ doping level both for p type fully depleted region and n type absorber region. In terms of the thickness of the fully depleted region, we first theoretically estimated built-in voltage (V_{bi}) as 0.98 V and corresponding depletion region width in p side (x_p) as 84 nm by using the heterojunction equations 1.37 and 1.38. Considering the estimated 84 nm depletion width on p side and to ensure to stay on the safe side, we determined thickness as 50 nm for the top InP layer to satisfy fully depletion requirement.

2.1.1.4. P InGaAs layer

This 0.5 μm p-InGaAs layer is the final layer and it is designed to provide easier ohmic contacts. Comparing with p-InP layer, most of the time, without extra annealing steps, metals on p-InGaAs show ohmic properties even in as-deposited form. Having quality ohmic contacts on p-InP however requires sensitive annealing work after deposition [103], [104].

2.1.2. Layout Design

Layout design will be examined under two sub headings as detector layout design and fan-out layout design

2.1.2.1. Detector Layout Design

We design square pixels with changing numbers and sizes to be able to extract surface and bulk components of the dark current. 80 μm sided single standing pixels, 60 μm sided 2x2 pixel arrays, 40 μm sided 3x3 pixel arrays, and 20 μm sided 5x5 pixel arrays are included. Same design is used for production of two different types of detectors. In one of them, fully depleted InP layer is kept intact and only p-InGaAs layer is etched for isolation. While, for the other design, fully depleted InP layer is also etched which become similar process with the standard mesa structure as the surface of the absorber InGaAs layer unearthed at the depletion region. By doing so, we aimed to compare passivation behavior of designed fully depleted layer as its existence was the only changing parameter. These two types of detectors with exactly same layout designs are meant to be placed at the same piece of crystal material and undergo the same process conditions. Designed layout structures for two different types of detectors are illustrated in Figure 2.4.

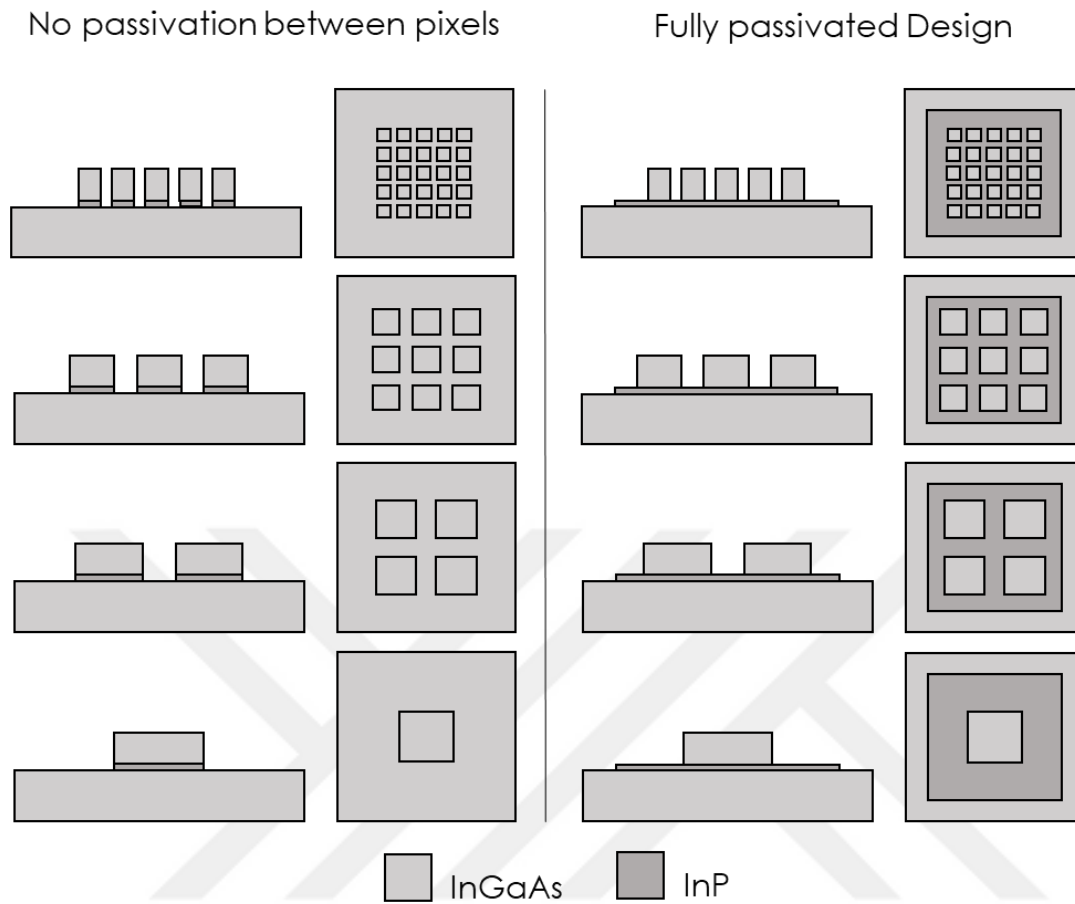


Figure 2.4. Mesa type detectors layout design

A set of 4 detector structures with aforementioned designs and alignment marks are included on a 1 cm x 1 cm mask design as given in Figure 2.5.

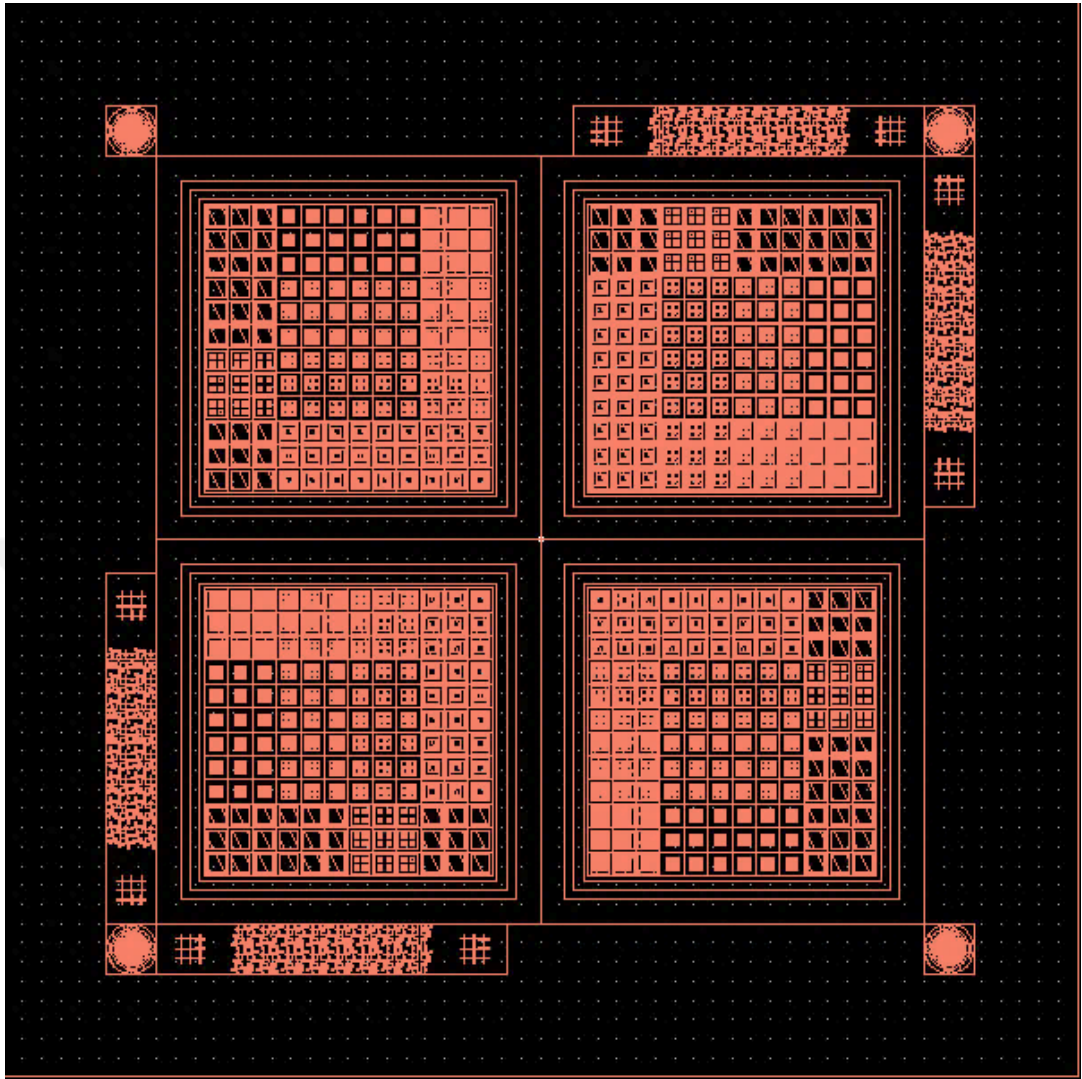


Figure 2.5. Overall mesa mask layout design

2.1.2.2. Fan-out Layout Design

Produced test arrays are flip-chipped to a designed Silicon fan-out device that are used to obtain electrical connections from pixel arrays and increase the connection area as it would be appropriate for wire bonding. 9 fan-out devices are included to the mask design in 3x3 array formations to produce multiple devices in one process cycle. Figure 2.6 shows the general view of the fan-out layout design.

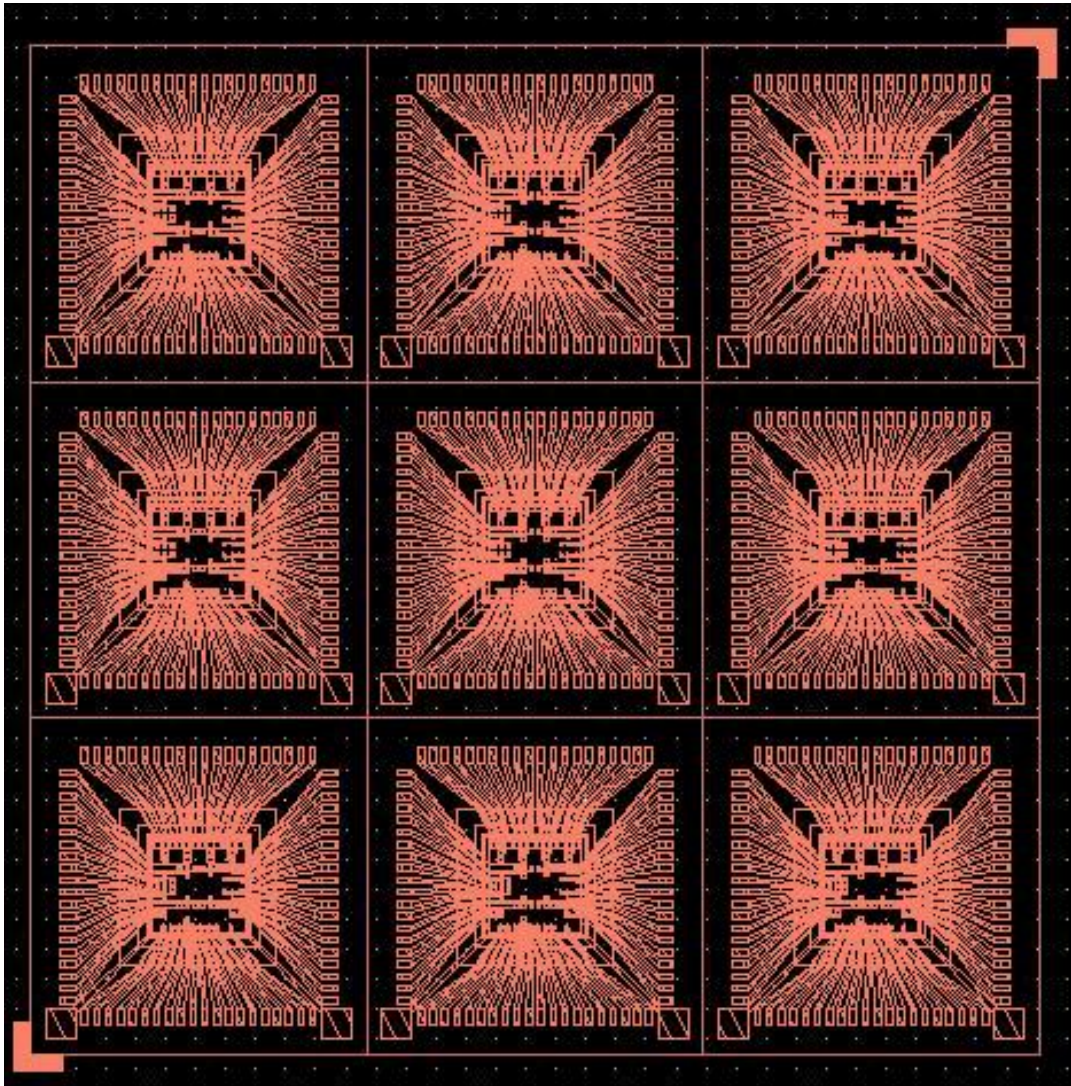


Figure 2.6. General view of fan-out layout design

2.1.3. Detector Process Steps & Photomask Design

After receiving the epi-ready InP substrates from our supplier, all the remaining processes including the crystal growth and cleanroom process are realized in our facilities. Process is divided into 2 parts as detector process and fan-out process. Main steps of the detector process can be listed as;

- Crystal growth
- Cutting and the cleaning of the samples

- Alignment mark and p metal coating
- Isolation etch, and N etch 1
- N etch 2
- N etch 3
- N metal coating
- InP fully depleted layer etch
- Passivation coating
- UBM/Indium coating

2.1.3.1. Crystal growth

Crystal growth is realized with Molecular Beam Epitaxy (MBE) technique by in-house III-V Riber Epineat system (Figure 2.7). This system can work with 4-inch wafers. There are Aluminum, Indium, Gallium, Arsenic and Phosphorus cells together with Silicon (n) and Beryllium (p) dopant cells on the system.

Epi-ready InP substrates are loaded to the system without any treatment and kept at 300 °C for cleaning purposes for about 1 hour in the buffer section which connects loading section to the growth chamber. After cleaning, substrate is transported to the holder in the growth chamber. Before crystal growth, the oxide layer on the substrate is removed from the surface at around 460 °C under phosphorus flux. A Reflective High Energy Electron Diffraction (RHEED) gun is used to check oxide removal. After this de-oxidation step, a thin InP buffer layer is grown to planarize the surface. An automated, computer-controlled recipe that is prepared for aimed design, controls the rest of the growth process.

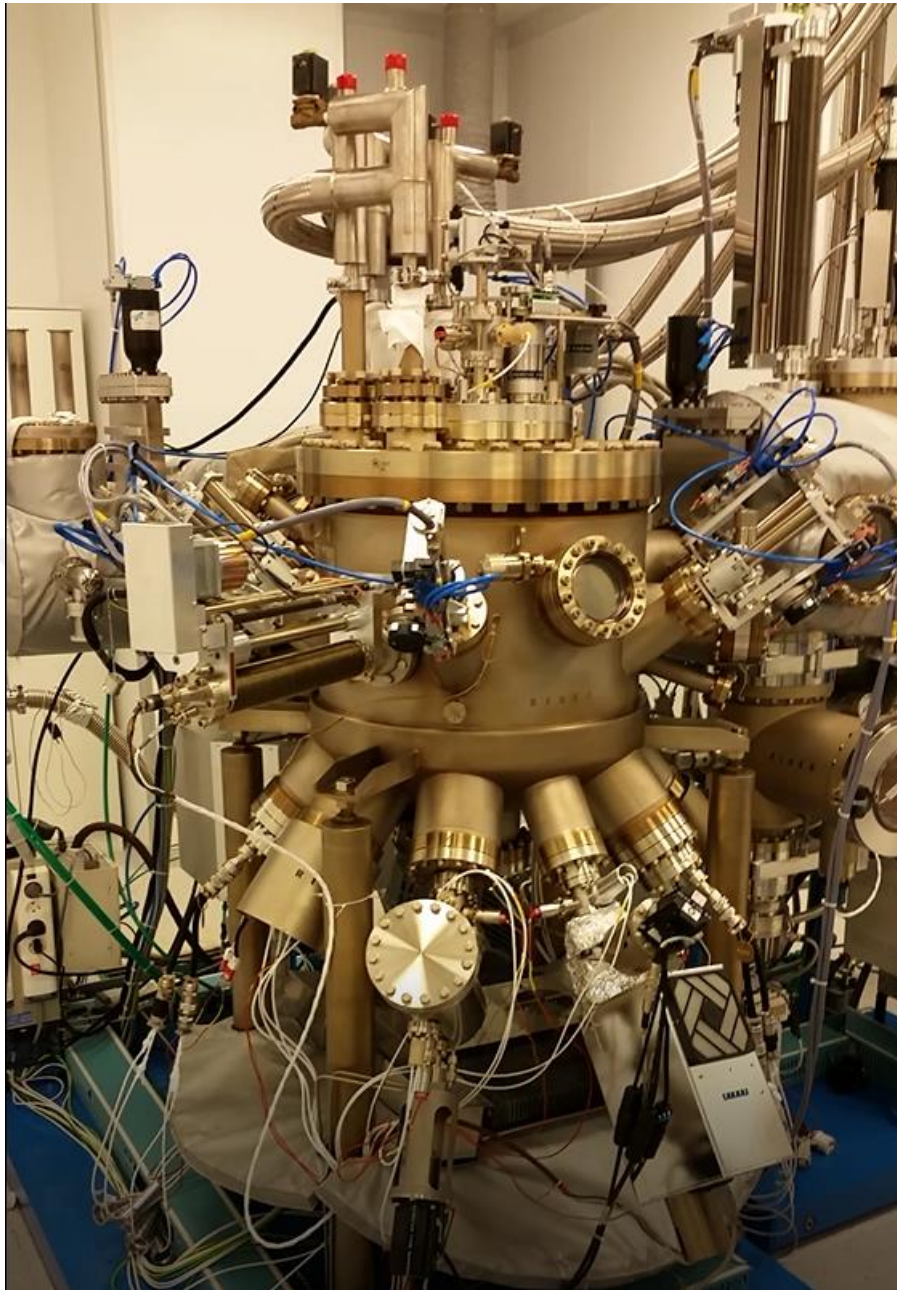


Figure 2.7. III-V Riber Epineat system

2.1.3.2. Cutting and cleaning of the samples

Produced epi-wafers are spin coated with photoresist protection layer without lithography and diced by DISCO Automatic dicing saw. Obtained samples are

chemically cleaned with Acetone, Isopropanol (IPA) and De-ionized water (DIW). Ultrasonic treatment is used during acetone cleaning.

2.1.3.3. Alignment mark and p metal coating

Both alignment marks and p metal pads are created with Ti/Au (25/100 nm) metal coating by Leybold Vacuum thermal PVD system after lithography step with using Shipley S1813 photoresist. Samples are placed in acetone containing glass weighing bottles for an overnight liftoff process. Part of the lithography mask layout design for alignment marks and 2x2, 3x3 pixel containing arrays are given in Figure 2.8 and Figure 2.9 respectively.

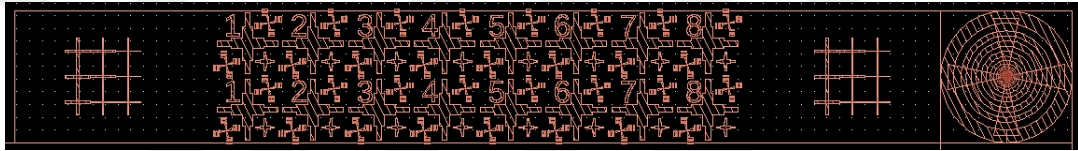


Figure 2.8. Alignment mark lithography mask design

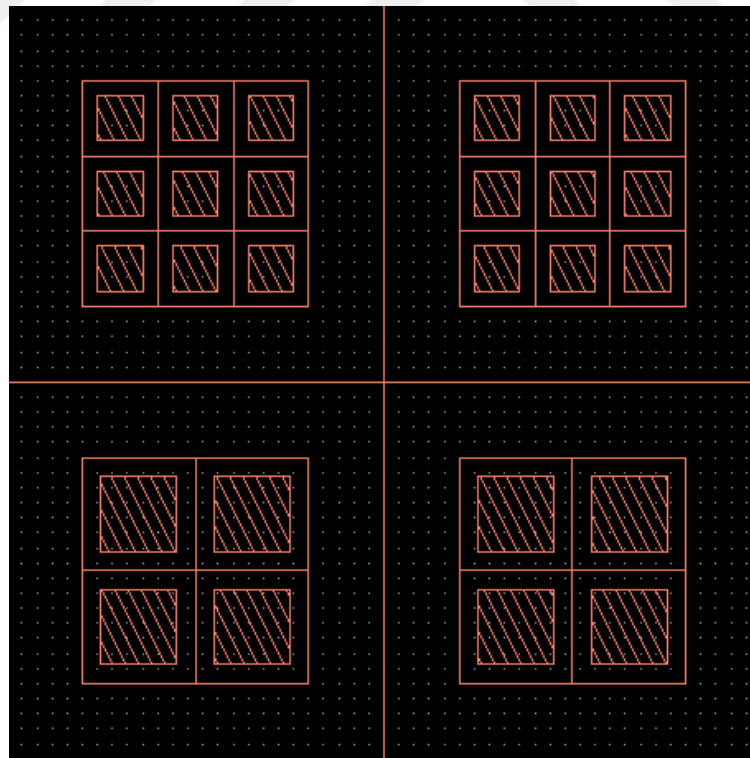


Figure 2.9. P metal lithography mask design

2.1.3.4. Isolation etch, and N etch 1st step

To create mesa structure and electrically isolate each pixel from one another, p-InGaAs layer is etched away everywhere except p metal contacts. Corresponding lithography is realized with Shipley S1813 photoresist as the part of the lithography design given in Figure 2.10. Corresponding etch work is done chemically with $\text{H}_3\text{PO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (1/1/3) acid mixture for 50 seconds.

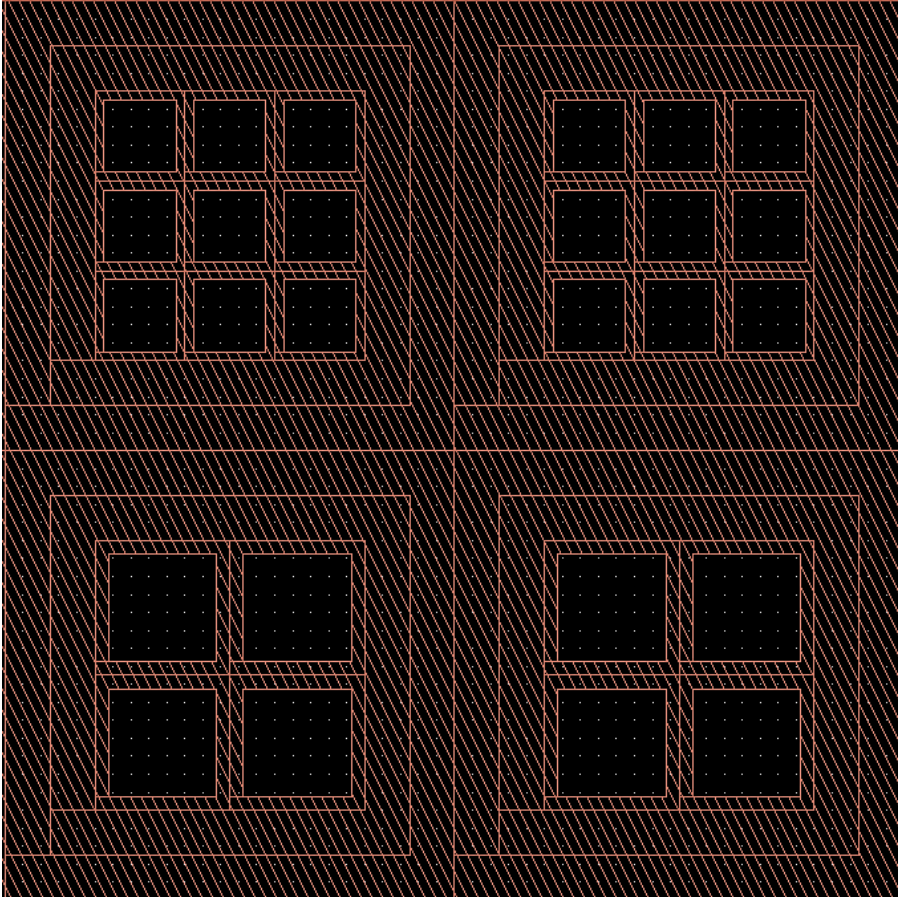


Figure 2.10. Isolation etch lithography mask design

N contacts should be formed on the n-InP layer which is around $1.25\ \mu\text{m}$ deeper than p metal contacts. However, indium bump heights for all ground and FPA pixels must be in the same level to have a successful Flip-chip bonding (FCB) process. Considering this, we kept the ground contact pixel region on the p-InGaAs layer and placed ground contact etching region outside of the ground contact pixel region.

These two regions will be electrically connected with ground contact metal coating. Therefore, we need to ensure metal continuity. To reach the n-InP layer we need to etch 3 layers i.e. p-InGaAs, fully depleted p-InP and absorber InGaAs layers. In the case that we use the same lithography with selective wet etchants, because of under etching, metal cannot be coated continuously. To solve the problem, we designed a ladder-like structure with 3 different lithography steps. First step etching is done together with isolation etch in this step. Part of the lithography design given in Figure 2.11

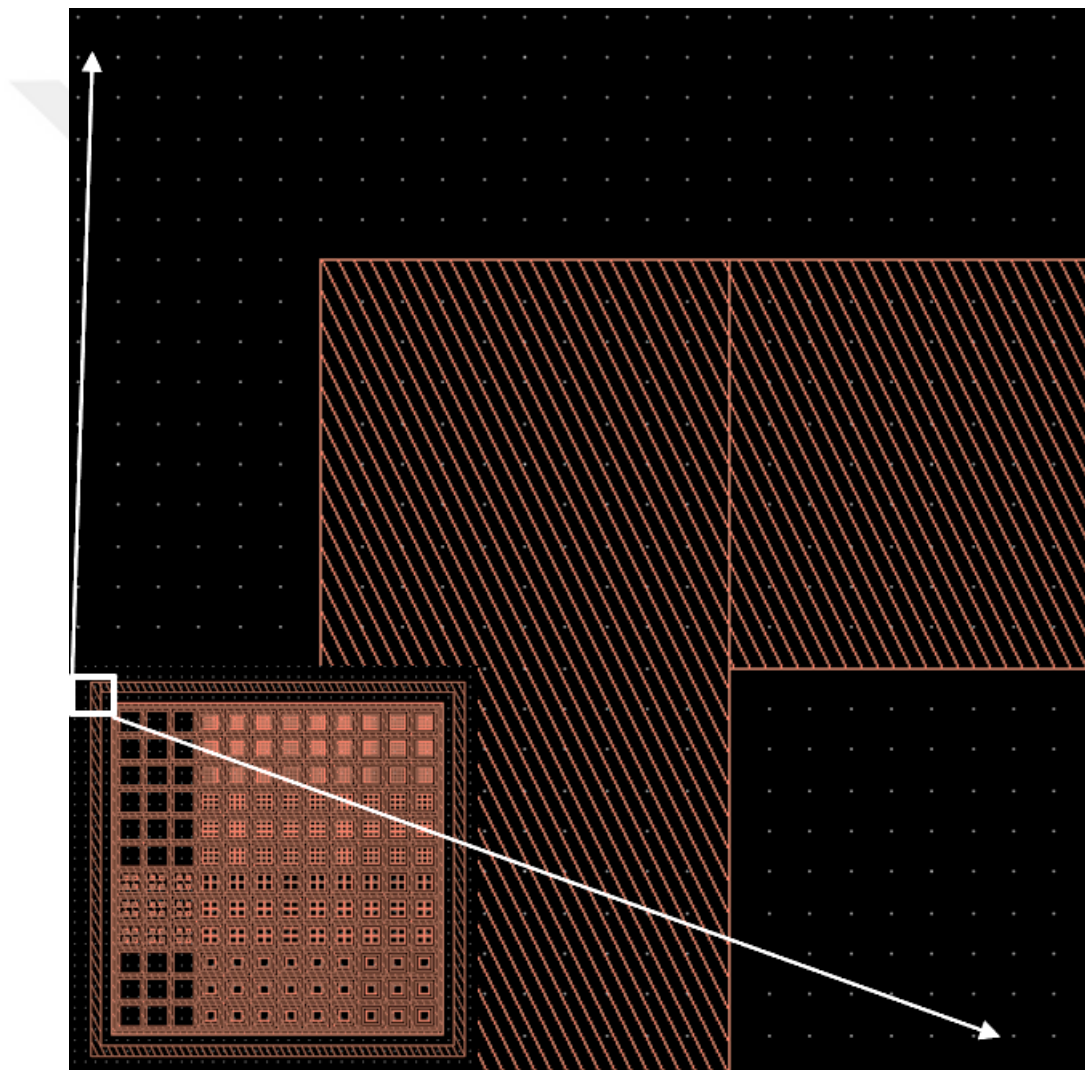


Figure 2.11. N etch 1st step lithography mask design

2.1.3.5. N etch 2nd and 3rd steps

2nd step n etching is designed in a smaller region on the etched layer at 1st step. Similarly, 3rd step etching is designed in a smaller region on the etched layer at 2nd step. Lithography work is done with Shipley s1813 photoresist. Fully depleted p-InP layer is etched with HCl/H₃PO₄ (1/3) acid mixture for 15 seconds and absorber InGaAs layer is etched with H₃PO₄/H₂O₂/H₂O (1/1/3) acid mixture for 70 seconds. Lithography mask layout design is given in Figure 2.12.

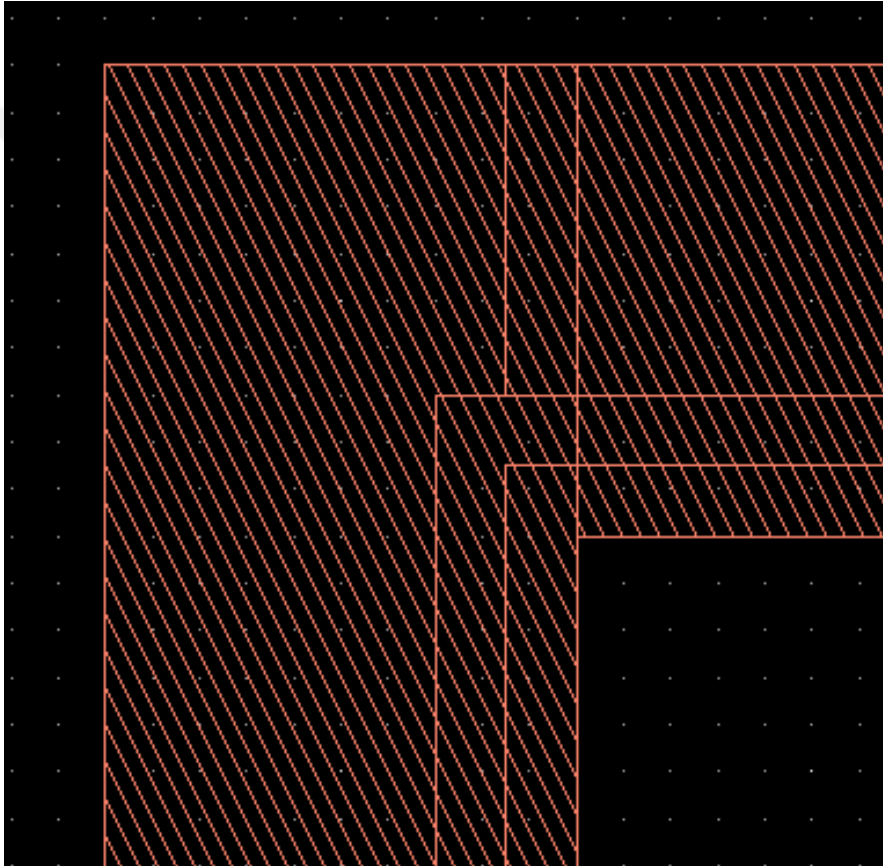


Figure 2.12. N etch 2nd and 3rd steps lithography mask design showed over 1st step

2.1.3.6. N metal coating

Ground contact pixel area and etched n-InP regions are connected by Ti/Au (25/100 nm) metal coating. Corresponding lithography is done with Shipley S1813 photoresist and metals are coated by Leybold Vacuum thermal PVD system. Samples

are placed in acetone containing glass weighing bottles for an overnight liftoff process. Lithography mask layout design is given in Figure 2.13.

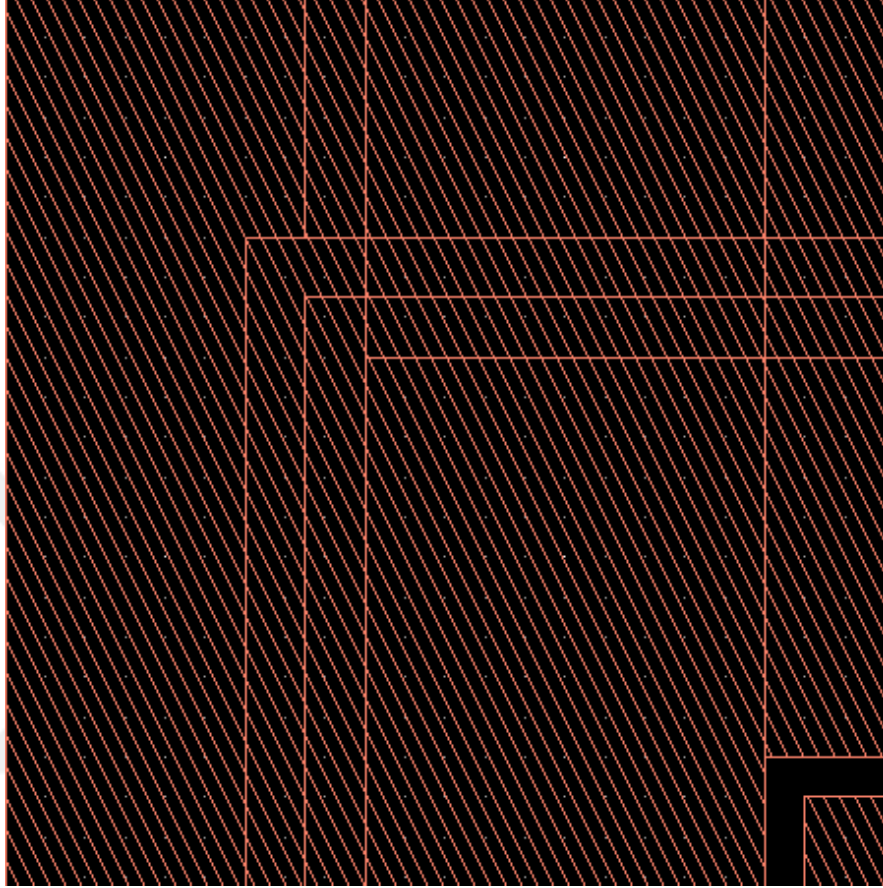


Figure 2.13. N metal coating connecting etched n-InP area and ground pixel regions

2.1.3.7. InP fully depleted layer etch

This step is the step that the two different kinds of detectors that are meant to be compared with each other are created. For the group of pixels that will correspond to the standard mesa type detectors, p-InP fully depleted in-device passivation layer is etched away as the absorber InGaAs under this layer is unearthed. For the other group of pixels, p-InP fully depleted layer is remained untouched as they would show the aimed passivation behavior. Figure 2.14 shows the part of the lithography mask design of this step.

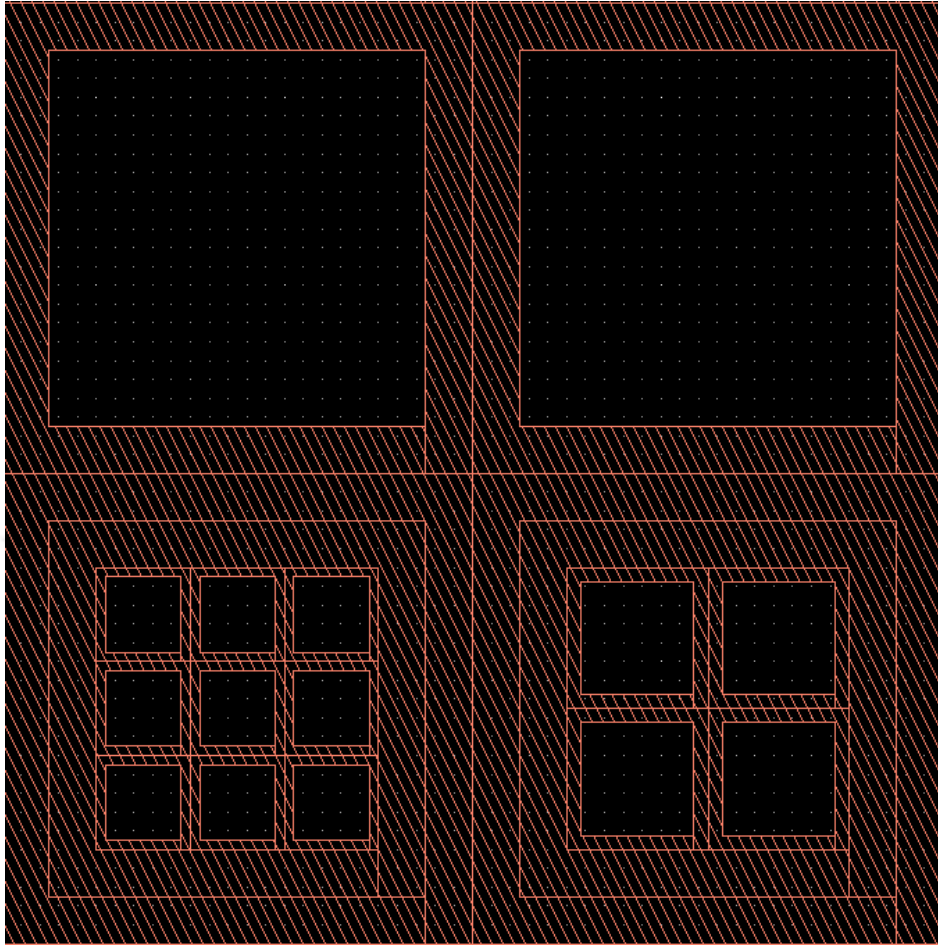


Figure 2.14. Fully depleted p-InP layer etch lithography design. For the group at the top, fully depleted p-InP layer remained untouched while for the group at the bottom, fully depleted p-InP layer etched away.

2.1.3.8. Standard on-device passivation coating

A spin-on dielectric polyimide passivation i.e. PIX 1400 is used as standard on-device passivation. After spin coating of the passivation, 1-minute soft curing at 150 °C is performed. To open this passivation layer on the ground and p metal contacts, Shipley S1813 photoresist lithography is done as the part of the lithography is given in Figure 2.15 and Figure 2.16 for p and ground contacts respectively.

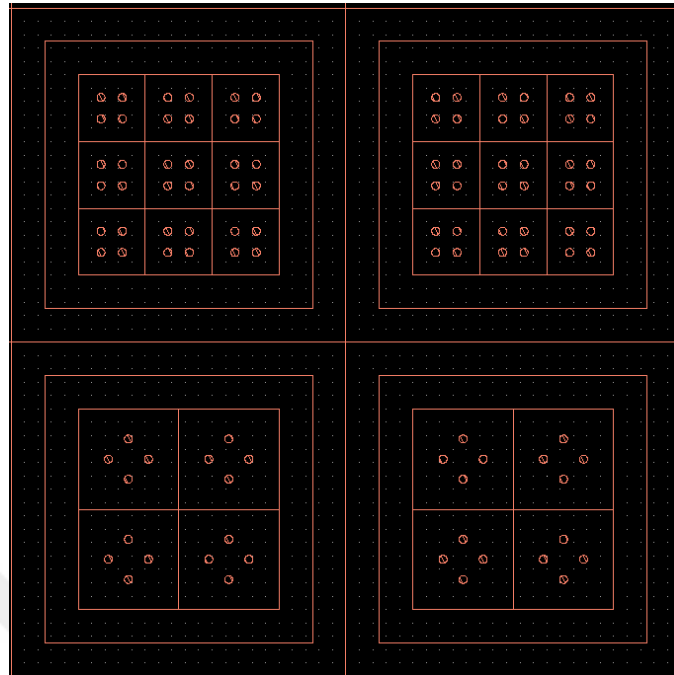


Figure 2.15. Passivation openings for p metal contacts

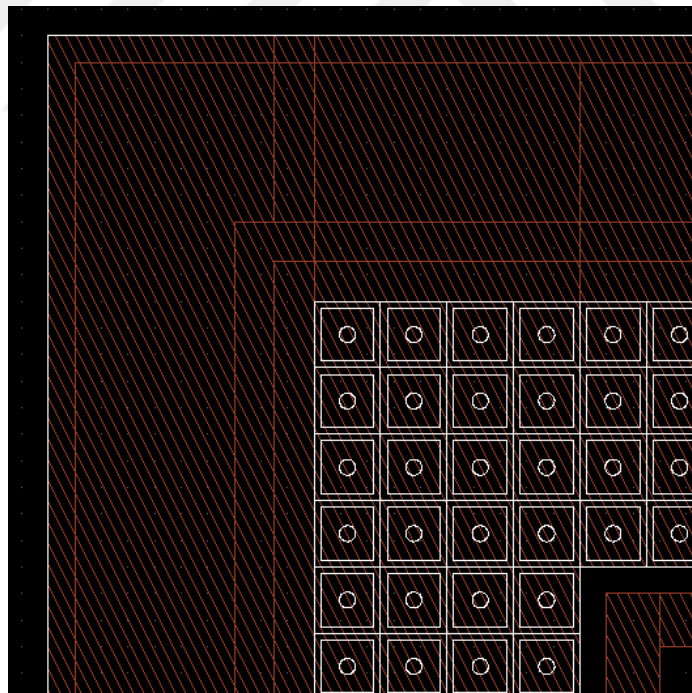


Figure 2.16. Passivation openings for ground metal contacts. Here to understand the placement, mask design is given as white selected while it is on the n metal coating mask.

One of the most efficient part of this process step is that the NaOH based developer solution for Shipley S1813 photoresist is also the remover of the PIX 1400 passivation. Therefore, during the lithography, passivation layer openings are created easily. Since soft cured PIX 1400 is resistant to acetone, photoresist is cleaned with acetone right after the development stage and a temperature ramp from 150 °C to 330 °C on hot plate followed with 5-minute hard baking at 330 °C is applied to the samples.

2.1.3.9. UBM/Indium coating

Similar photolithography design with passivation opening step are used for UBM-Indium coatings as the coating fills all the passivation openings. AZ9260 photoresist is used. Ti/Ni/Au (25/35/100 nm) UBM coating is realized by Leybold Vacuum thermal PVD system and 3µm Indium coating is realized right after UBM coating by Leybold Vacuum e-beam evaporator system. Samples are placed in acetone containing glass weighing bottles for an overnight liftoff process.

2.1.4. Fan-out Process Steps & Photomask Design

Dummy Silicon wafers are used to produce fan-out chips that are basically helps to obtain electrical connections from detectors with flip-chipping. Main steps of the fan-out process can be listed as;

- PECVD SiN coating
- Connection metal coating
- Passivation coating
- UBM/Indium coating

Each process step will be clarified under separate headings and photomask designs will be discussed for the steps that include lithography work.

2.1.4.1. PECVD SiN coating

A dummy silicon wafer is coated with 500nm SiN insulating layer by PECVD to provide electrical isolation. After coating, silicon wafer is diced to square samples that will contain 9 fan-out chips in 3x3 array form.

2.1.4.2. Connection metal coating

A fan-out chip can take electrical connections from 80 different pixel groups with changing sizes and types as including multiple number of connections for each different size and type of detectors to create a reliable data set. Each of these 80 pixels connected to a metal pad that is wide enough for wire-bonding. Also 2 wider metal pads placed at the bottom of the chip provide electrical connection to the ground pixels. All metal pads and paths are created with Shipley S1813 photoresist lithography and Ti/Au (25/100 nm) metal coating by Leybold Vacuum thermal PVD system. Figure 2.17 shows overall connection metal coating mask design of a fan-out chip.

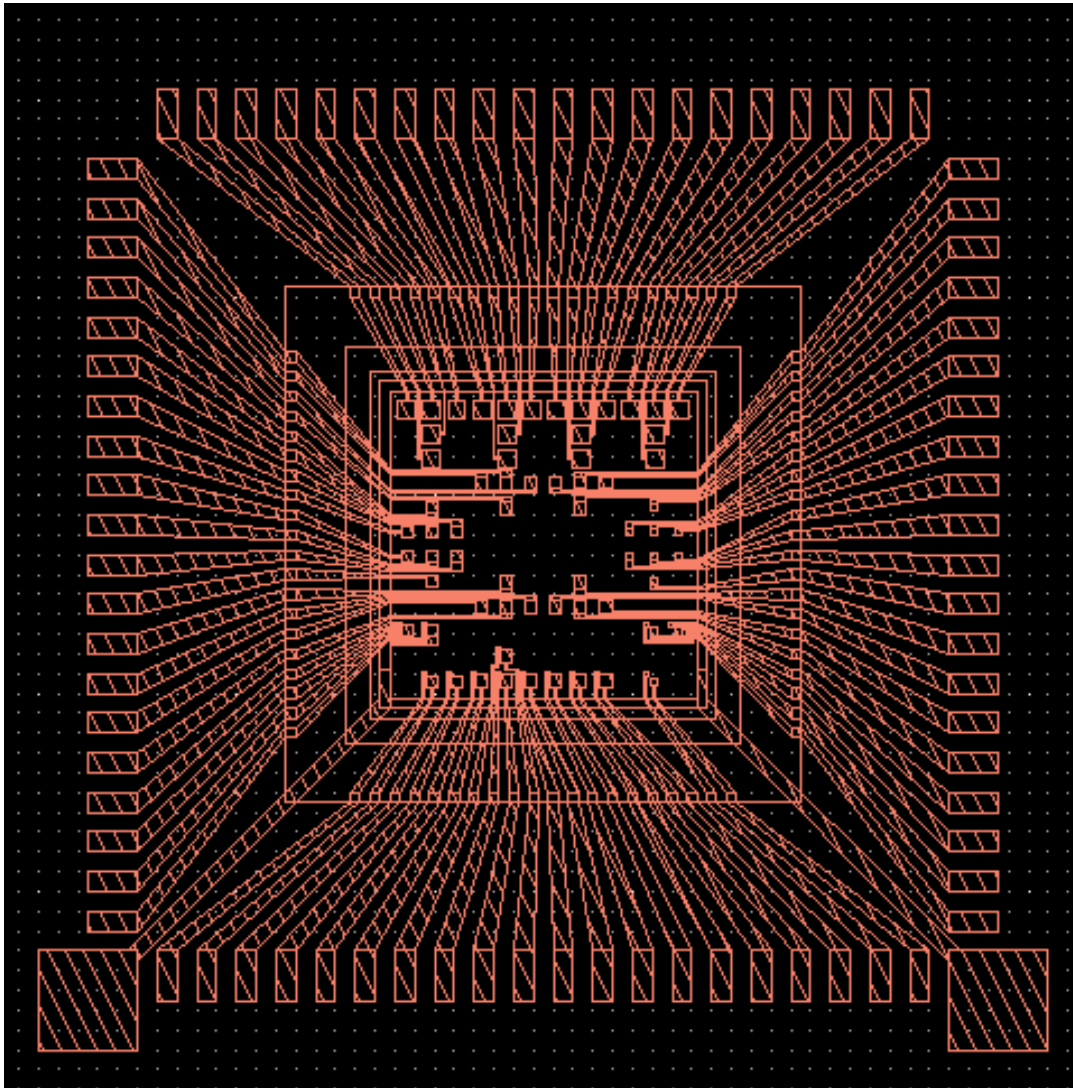


Figure 2.17. Fan-out chip metal connection lithography mask design

2.1.4.3. Passivation and UBM/Indium coatings

Similar to the mesa detector process, PIX 1400 polyimide material is used for passivation with similar process conditions. This passivation is opened at wire-bond pads and at the points on the pixel region that corresponds to the mirror image of the indium coatings on mesa detectors. As doing so, when one of the mesa detector or fan-out chip is flipped, fan-out passivation openings and mesa indium coatings would be facing to each other. After passivation openings are created, with similar

processing conditions, UBM/Indium is coated also on the fan-out chip passivation openings in the pixel region.

2.2. Characterization Results and Discussion

Mesa detectors and fan-out chips are produced with given process steps and diced to pieces. After microscope inspection, detectors and fan-out chips with best conditions are selected and flip-chipped to each other by SUSS Microtech FC150 system with indium bond bonding procedure.

IV characterization is realized both in dark and illuminated conditions. Illumination is provided by a tungsten lamp. In the graphs given below, in-device passivated detectors with fully depleted p-InP layers are tagged as “InP layer not etched” and standard mesa type (InGaAs absorber layers unearthed) detectors are tagged as “InP layer etched”

Figure 2.18, Figure 2.19, Figure 2.20, and Figure 2.21 shows the room temperature dark IV comparison graphs of 20, 40, 60 and 80 μm sided pixels in 5x5, 3x3, 2x2 arrays and single standing conditions respectively. In all of the graphs, in-device passivated (InP layer not etched) detectors has decreased dark current values as expected.

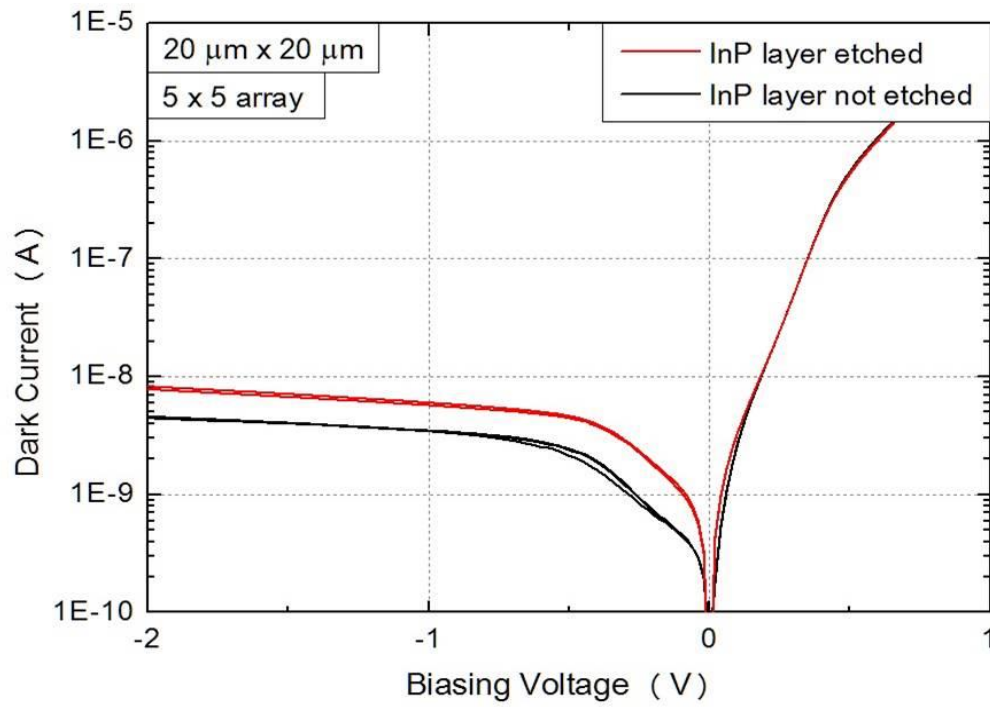


Figure 2.18. Dark IV comparison graph of 20 μm sided square pixels in 5x5 array

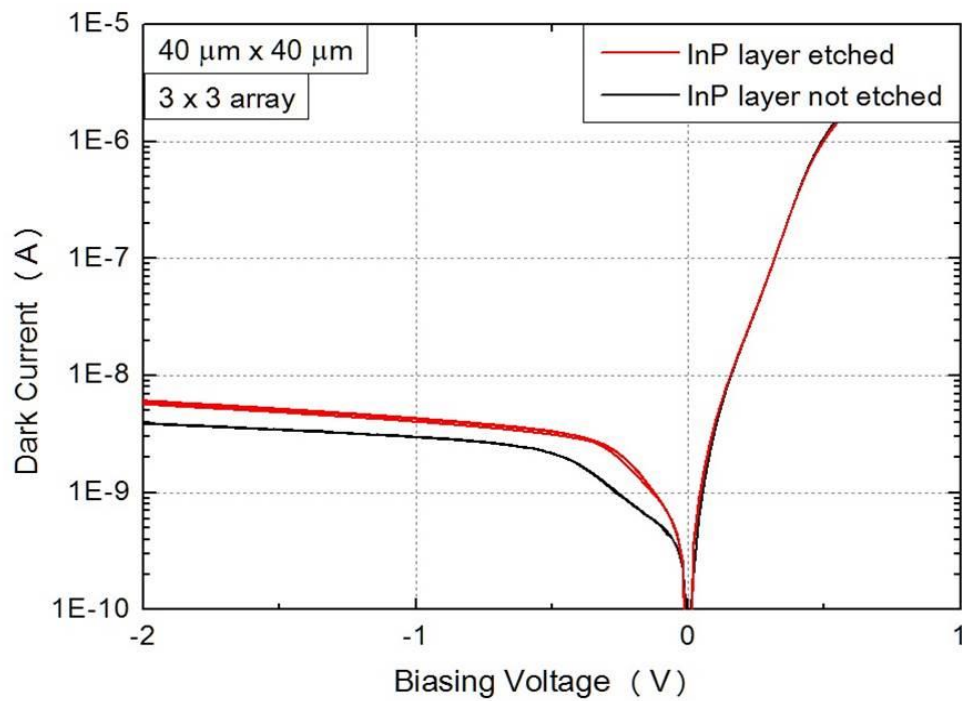


Figure 2.19. Dark IV comparison graph of 40 μm sided square pixels in 3x3 array

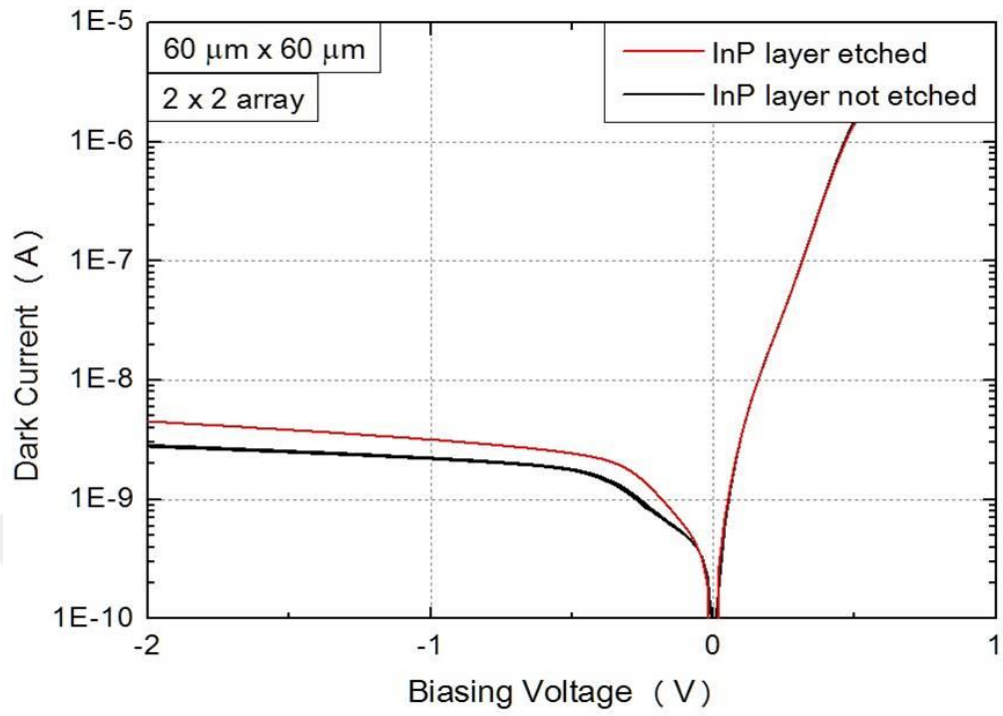


Figure 2.20. Dark IV comparison graph of 60μm sided square pixels in 2x2 array

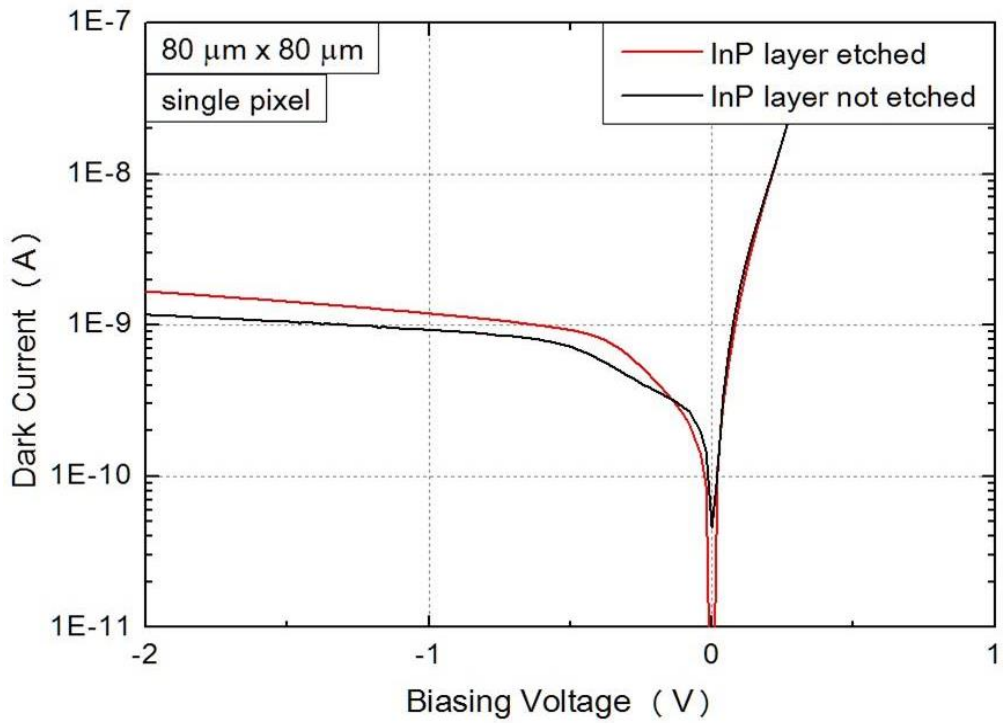


Figure 2.21. Dark IV comparison graph of 80μm sided single standing square pixels

Figure 2.22, Figure 2.23, Figure 2.24, and Figure 2.25 shows the illuminated room temperature IV comparison graphs of 20, 40, 60 and 80 μm sided pixels in 5x5, 3x3, 2x2 arrays and single standing conditions respectively. In all of the graphs, in-device passivated (InP layer not etched) detectors has increased photo current values. This enhancement is coming from the increase in active area and observed similarly in spectral responsivity measurements as well. Some of the optically created carriers in the bulk region between pixels cannot diffuse to the depletion region before they are recombined. When fully depleted p-InP layer is not etched, depletion layer is spread among all inter pixel area and optically created carriers that would normally recombine are able to diffuse to enlarged depletion region and detected as illustrated in Figure 2.26. We note that, InP layer dimensions are all identical for these detectors. Therefore, the fact that photocurrent values changing by the pixel areas, rules out the short connection possibility over p-InP layer and verifies the fully depleted condition.

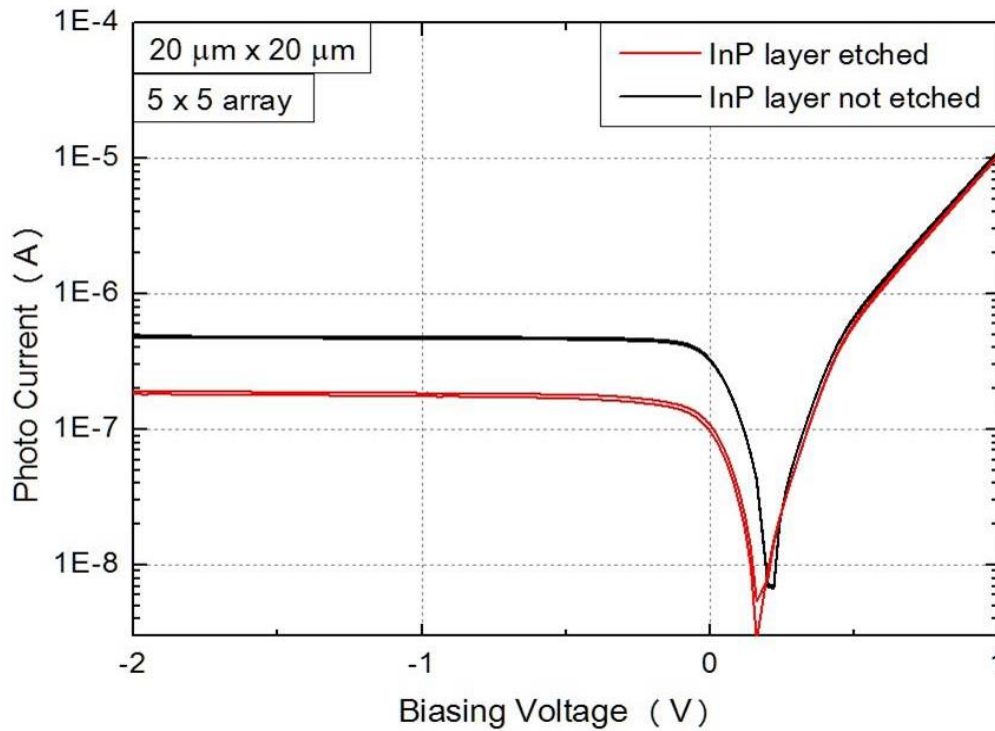


Figure 2.22. Illuminated IV comparison graph of 20 μm sided square pixels in 5x5 array

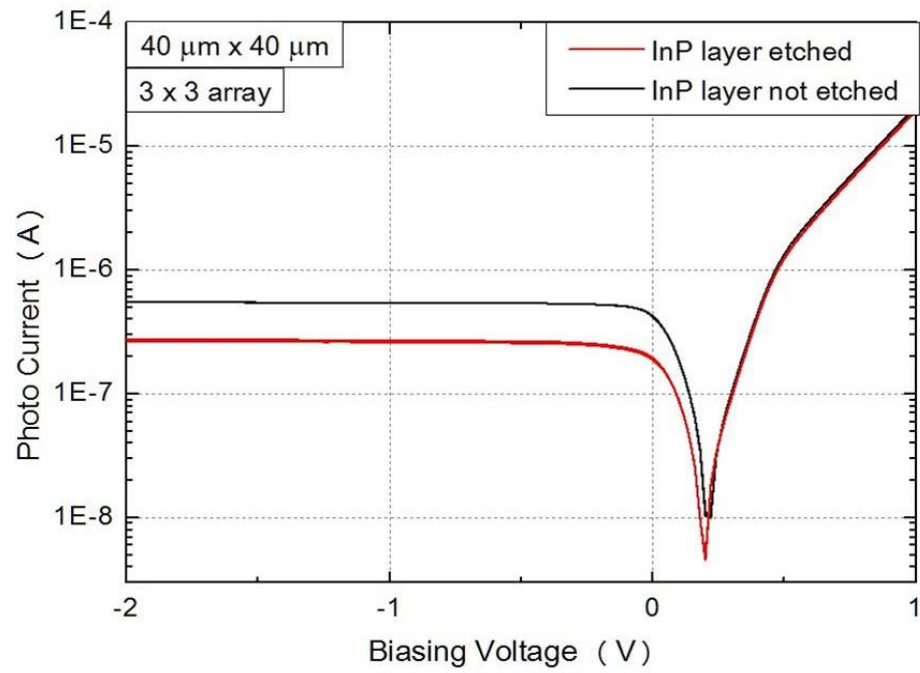


Figure 2.23. Illuminated IV comparison graph of 40µm sided square pixels in 3x3 array

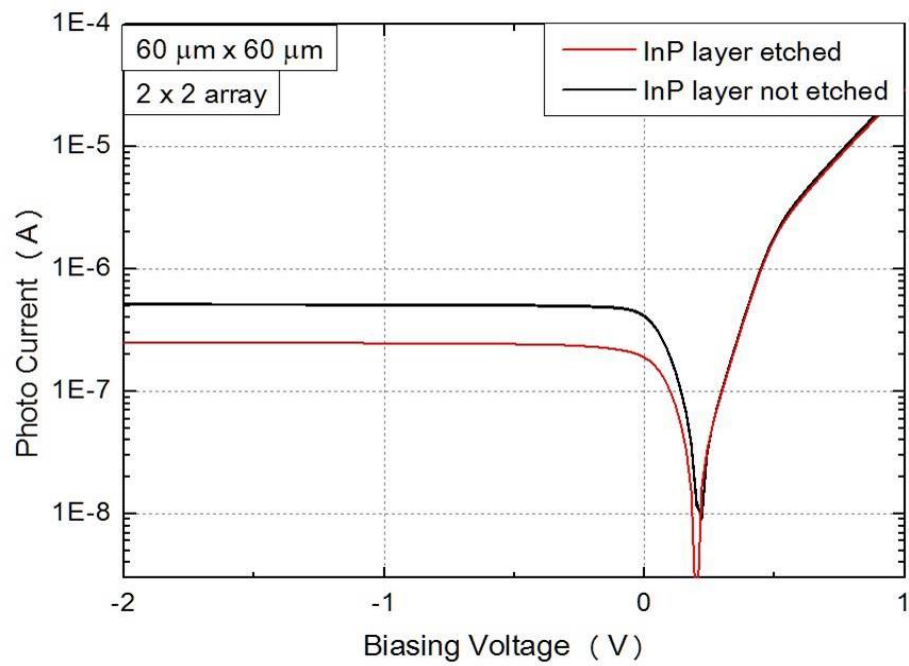


Figure 2.24. Illuminated IV comparison graph of 60µm sided square pixels in 2x2 array

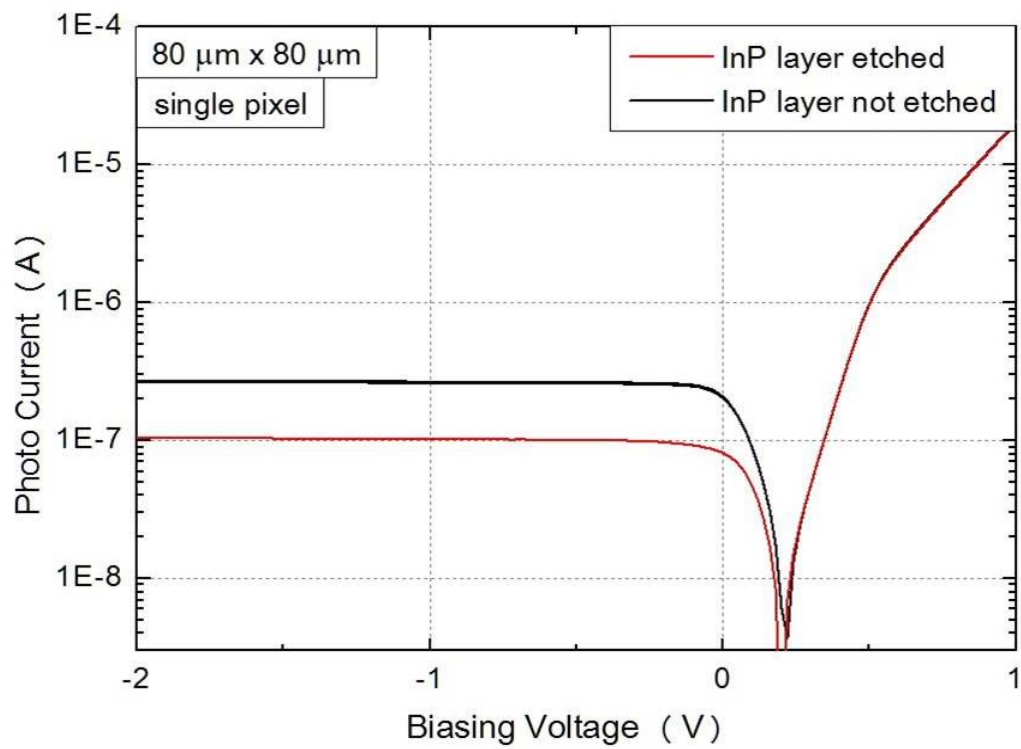


Figure 2.25. Illuminated IV comparison graph of 80 μm sided single standing square pixel

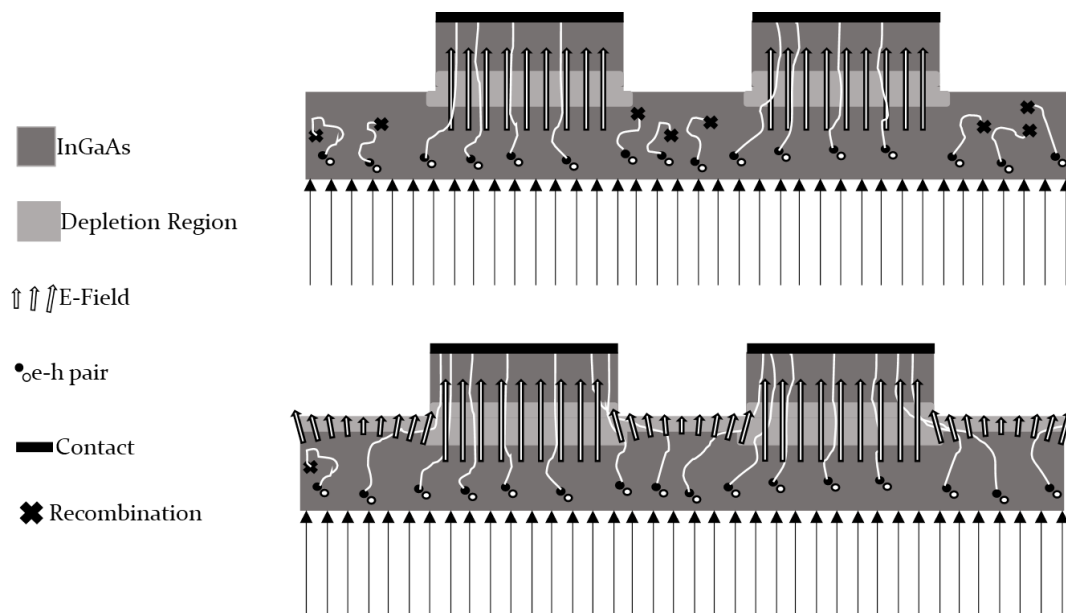


Figure 2.26. Illustrated scheme of photo current increment

Next, we analyzed the bulk and surface related components of the dark current. In comparison between different sized pixels, bulk current changes proportional to the pixel area, whereas surface current depends on the total pixel perimeter as denoted in equation 2.1.

$$I_{dark} = J_b x A + J_s x P \quad 2.1$$

Here, I_{dark} is dark current, J_b, J_s is bulk and surface current densities, A is effective pixel area and P is total pixel perimeter. We can determine total pixel perimeter from the dimensions of the photo-lithography mask, but it is hard to determine effective pixel area due to the uncertain diffusion length. As a solution, we employed photo-current to measure the effective pixel area. Ratio of photo current obtained from two differently sized pixel groups (denoted with sub and superscript 1 and 2 in equations), α , which yields the ratio of effective pixel area calculated as the following:

$$\frac{I_{photo}^2}{I_{photo}^1} = \frac{A_2}{A_1} = \alpha_{21} \quad 2.2$$

Excluding the area term in equation 2.1 for two differently sized pixel groups by using this photo current ratio, we reach:

$$(I_{dark}^2 - \alpha_{21} I_{dark}^1) = J_s (P_2 - \alpha_{21} P_1) \quad 2.3$$

Equation 2.3 gives the relation between dark current and surface current density while it is independent of bulk current density. Based on binary combinations of measurements from different sized detectors at room temperature (~ 295 K) and 1 V reverse bias conditions, we obtained a data set. From the slope of the linear fit of $(I_{dark}^2 - \alpha_{21} I_{dark}^1)$ vs $(P_2 - \alpha_{21} P_1)$ plot we have calculated the surface current density for both with and without etched depleted InP layer detectors as 3.06×10^{-8} and 1.12×10^{-8} ($A \text{ cm}^{-1}$), respectively given as Figure 2.27 and Figure 2.28. These results clearly demonstrate the passivation behavior with 3 times reduces surface current densities.

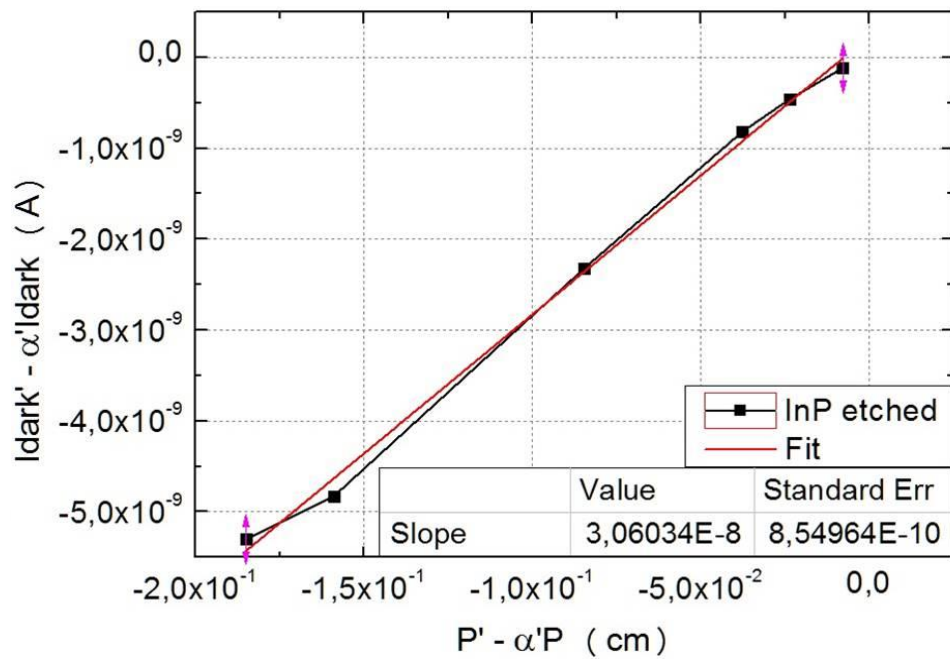


Figure 2.27. Linear fit study for InP etched detectors where slope gives surface current value.

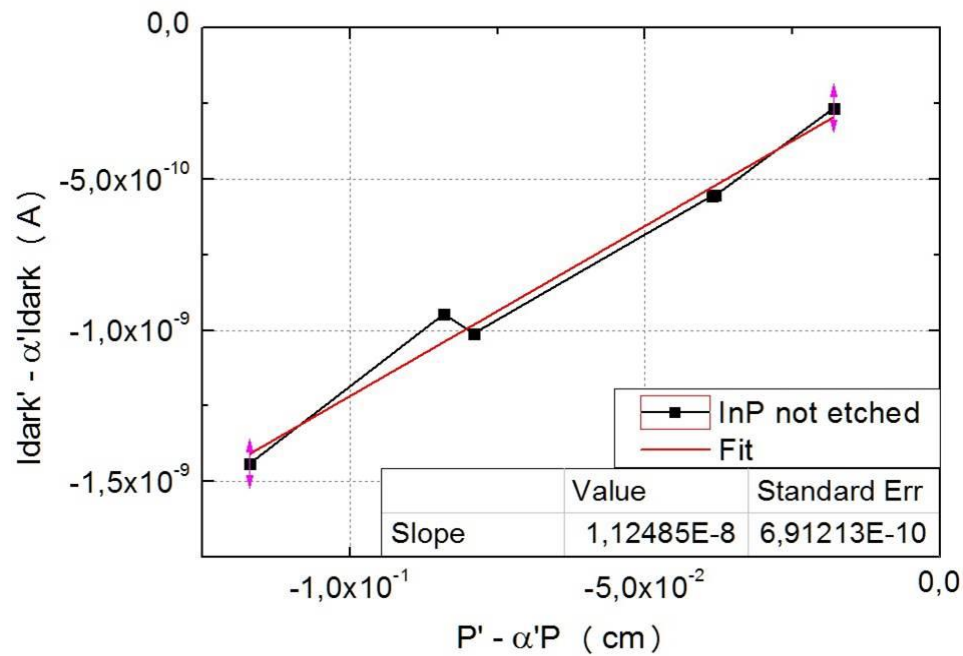


Figure 2.28. Linear fit study for InP not etched detectors where slope gives surface current value.

Furthermore, we have determined the bulk current values using the calculated surface current densities. Summary of the results are shown in Table 2.1. Bulk current contributions for the samples which are passivated by the InP layer agree perfectly with the effective area obtained from the photo-current ratios. The small mismatch in the bulk current ratios for the InP layers etched away samples is due to the fact that surface currents is much more dominant in these samples and small errors get magnified for the bulk current contribution. This is indeed common for mesa type InGaAs detectors and even negative bulk current densities have been reported [105].

Table 2.1. Dark and Photo Currents and Current Components

#	Total Perimeter (μm)	Dark Current (A)	Photo Current (A)	Surface Dark Current (A)	Bulk Dark Current (A)
1	320	9.00×10^{-10}	2.65×10^{-7}	3.60×10^{-10}	5.40×10^{-10}
2	960	2.24×10^{-9}	5.10×10^{-7}	1.08×10^{-9}	1.16×10^{-9}
3	1440	2.99×10^{-9}	5.45×10^{-7}	1.62×10^{-9}	1.37×10^{-9}
4	2000	3.45×10^{-9}	4.78×10^{-7}	2.25×10^{-9}	1.20×10^{-9}

CHAPTER 3

PLANAR TYPE DETECTORS

3.1. Design

Design studies will be examined in a similar manner with mesa type detectors with three sub-headings as epi-layer design, layout design, and FPA process steps & photomask design.

3.1.1. Epi-layer design

Standard planar epi-layer structure consists of an absorbing InGaAs layer that is sandwiched in between p-InP and n-InP contact layers for which n-type layer is doped during crystal growth while p-type layer is kept undoped so that it can be locally doped by diffusion processes after growth (Figure 3.1).

InP	undoped	P layer
$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	undoped	Absorber Layer
InP	n type doped	N layer
InP SI Wafer		

Figure 3.1. Standard planar epi-layer structure

The performance of this standard epi-layer structure is limited in many respects. Within the scope of this thesis, the novel design with double cap layers, which provides the results that are close to the world record performance as reported in the literature as of the date of this thesis, have been developed and presented in the Figure 3.2 [106]. Through this epi-layer structure, details of design and the key points

that increase the performance of the standard structure will be examined under separate headings for each layer.

InP	0.2 μm	undoped	2nd cap layer
$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	0.2 μm	undoped	1st cap layer
InP	1.0 μm	$n\ 5 \times 10^{16} \text{cm}^{-3}$	P layer
$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	2.5 μm	$n\ 5 \times 10^{16} \text{cm}^{-3}$	Absorber Layer
InP	0.3 μm	$n\ 3 \times 10^{18} \text{cm}^{-3}$	N layer
InP SI Wafer			

Figure 3.2. Final planar epi-layer structure

3.1.1.1. N-InP Layer

This layer is designed similar to n-InP layer in mesa design. The usage as a common contact layer and the important points to be satisfied are also the same. Only difference comes from the doping values. This time, n-InP layer is doped at its maximum available level of $3 \times 10^{18} \text{cm}^{-3}$.

3.1.1.2. Absorber Layer

This layer is the active InGaAs layer in which the photons are absorbed, and the corresponding electron-hole pairs are formed. If the active layer is thinner than it should be, it would cause a decrease in the responsivity value as a result of not absorbing sufficient number of photons. While, if the absorber layer is thicker than it should be, the current carriers formed by the absorbed photons would be recombined before reaching the depletion region and thus the contact metal, which also decreases responsivity. In the literature, it is possible to find examples with absorber layer thicknesses between 2.2 μm and 3 μm . In this thesis, the value of the absorber layer thickness was determined as 2.5 μm .

In terms of doping conditions, by the low n type doping of absorber layer, it is possible to reduce the mobility of the thermally produced electron-hole carriers and reduce the dark current. This will also affect the optically generated current carriers and will also cause some reduction in responsivity. However, this decrease in responsivity is expected to be less important than the decrease in the dark current. Thus, the final detector performance can be enhanced in this way. In the experimental studies conducted within the scope of this thesis study, the dark current and responsivity values are examined, and the highest final detector performance is obtained by n-type absorber layer doping at $1\text{-}5 \times 10^{16} \text{cm}^{-3}$ level.

3.1.1.3. P-InP Layer

This layer is grown with low level n-type doping during the crystal growth, and high-level p-type doping by high temperature Zn diffusion is performed locally in pixel regions after the crystal growth process. The region between the pixels remains n-type doped and this reduces the surface leakage current by increasing the depletion region electric field which isolates the pixels from each other. On the other hand, in the case of such, high p-type doping level, the increased n-type doping causes the tunneling currents to be triggered under smaller reverse-bias voltages. As a result of the studies carried out by changing the amount of n-type doping up to $5 \times 10^{16} \text{cm}^{-3}$ level, a high-performance zone is obtained for 0V-1V reverse-bias voltage range in which surface leakage current is suppressed and tunneling currents are not triggered.

In terms of layer thickness, if the p-InP layer is designed thicker than it should be, high temperature Zn diffusion process would cause the pixels to be shorted to each other due to lateral diffusion. On the other hand, the diffusion rate of the Zn diffusion process is exponentially decreasing as the depth is increasing. For a thin InP layer, final diffusion depth would be difficult to control. $1 \mu\text{m}$ thickness that we chose for this layer is safe for each aforementioned issue.

3.1.1.4. 1st cap layer

The 1st cap consists of 0.2 μm InGaAs layer. This layer has two important roles that increase performance significantly. First role is to provide easier ohmic contacts comparing with p-InP layer. Most of the time, without extra annealing steps, metals on p-InGaAs show ohmic properties in as-deposited case. Having quality ohmic contacts on p-InP however requires sensitive annealing work after deposition. The other important role of this layer is decreasing the surface dark current by ensuring clean surface before dielectric passivation. This second role will be discussed with process steps design part in more detail.

3.1.1.5. 2nd cap layer

The 2nd cap layer consists of 0.2 μm InP. This layer is a sacrificial protection layer for the InGaAs 1st cap layer since the surface of the samples may deform in high temperature diffusion process that will be clarified in following process design part in more detail. Besides, cleaning acid mixture used after diffusion process also etches InGaAs while InP is resistant to it.

3.1.2. Layout Design

3.1.2.1. Wafer Dicing Layout Design

We are working piece by piece as each chip includes only one FPA for optimization reasons. We start with 4-inch wafers. To be safe, we leave 5 mm clearance from outer diameter where the epi-layer quality may differ. The remaining region is diced to obtain 5 pieces of FPA chips with 30400 μm x 26560 μm dimensions, and 12 pieces of test chips for early quick & dirty characterizations with 1 cm x 1 cm dimensions. Wafer layout design is given in Figure 3.3.

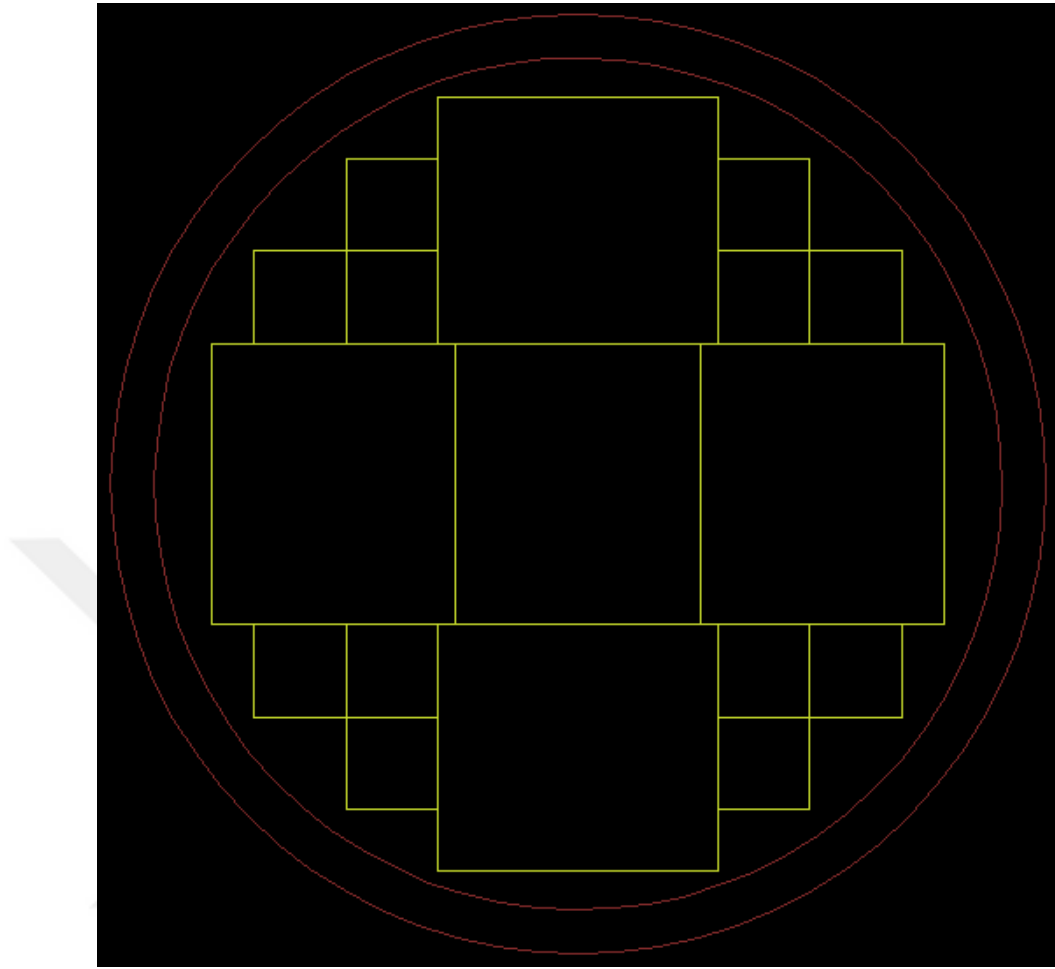


Figure 3.3. Wafer layout design

3.1.2.2. FPA Chip Layout Design

FPA chip includes one 1280 x 1024 format FPA with 15 μm pixel pitch at the middle. FPA includes 9 pixels wide ground line located at all 4 sides with one pixel clearance. Considering the ground line, final format of the FPA becomes 1300 x 1044 pixels. Around the FPA chip we have 150 x 150 format test arrays that have exactly the same design with the FPA. Test arrays include shorted pixel groups with changing number of pixels. FPA pixel characterization is realized using these pixel groups. FPA chip also includes several useful structures as alignment marks, TLM pads, lithography resolution patterns, front illuminated devices and single standing wide area test pixels. Overall chip layout design is given in Figure 3.4.

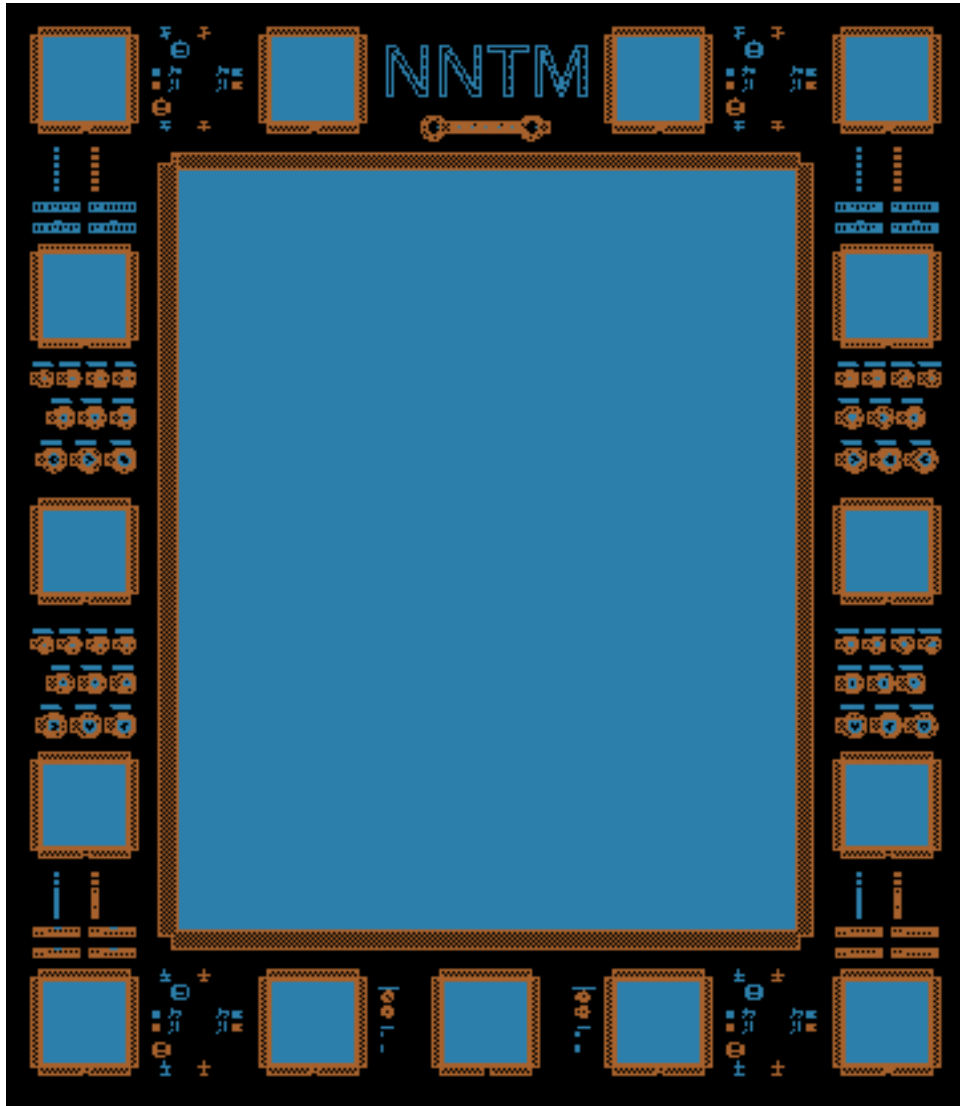


Figure 3.4. Chip layout design

Total of 10 different vernier alignment marks are designed in 2 different styles with $0.5\ \mu\text{m}$ resolution and used to align 11 different lithography steps. Base alignment marks for all steps are located in first lithography mask. Secondary alignment marks that fit the base alignment marks are located in each corresponding lithography masks. Alignment mark layout design is given in Figure 3.5.

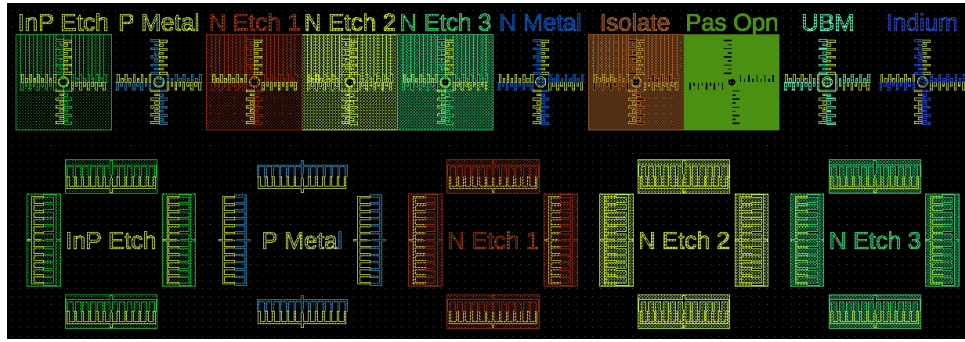


Figure 3.5. Alignment marks layout design

TLM pads are used to measure sheet resistances and ohmic contact properties. They are designed as $100\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$ rectangles for both p type and n type contact metals. Total of 9 pads are located side by side from $5\text{ }\mu\text{m}$ to $50\text{ }\mu\text{m}$ separations with $5\text{ }\mu\text{m}$ increments in each step. TLM pads layout design is given in Figure 3.6.

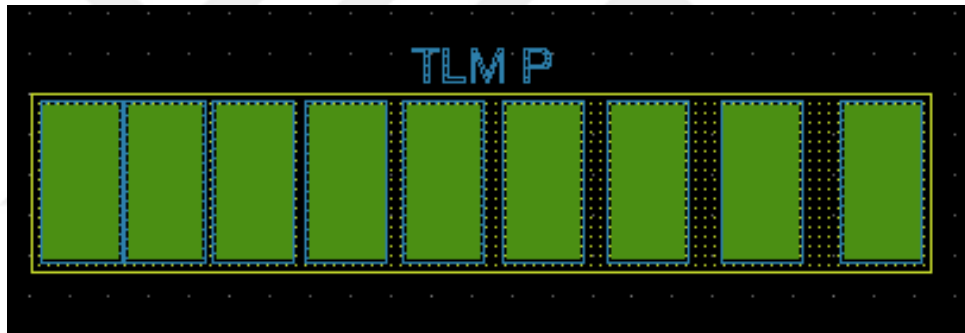


Figure 3.6. TLM pads layout design

Lithography resolution is monitored using resolution designs which include features from $1\text{ }\mu\text{m}$ to $5\text{ }\mu\text{m}$. Resolution patterns layout design is given in

Figure 3.7. Front illuminated devices are used for quick photo-response measurements. 2 different types of front illuminated single standing pixels with $100\text{ }\mu\text{m}$ and $300\text{ }\mu\text{m}$ active areas are located at the top of the chip under the NNTM label. Front illuminated device layout design is given in Figure 3.8.

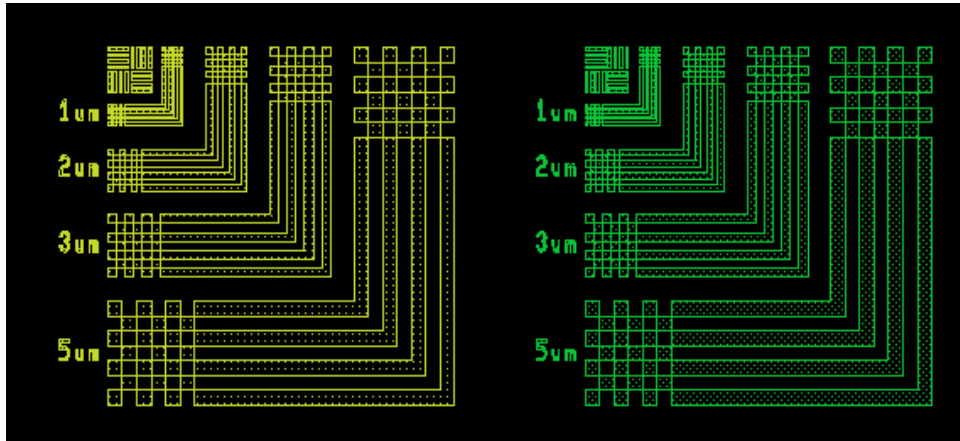


Figure 3.7. Lithography resolution patterns layout design

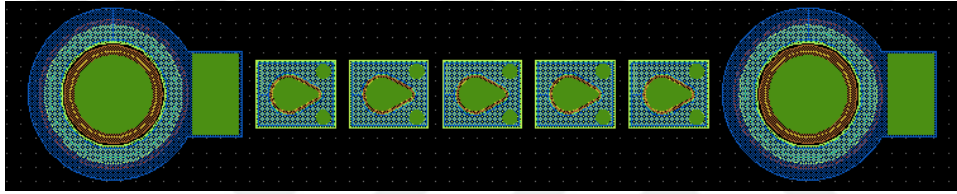


Figure 3.8. Front illuminated device layout design

Circular wide area single standing test pixels are designed with 3 different active area sizes in 100, 200 and 300 μm diameters. Ground line is located as it encircles the active area for each different pixel. Probe station measurements of these different area pixels provide useful information about device quality as it will be discussed in following chapters.

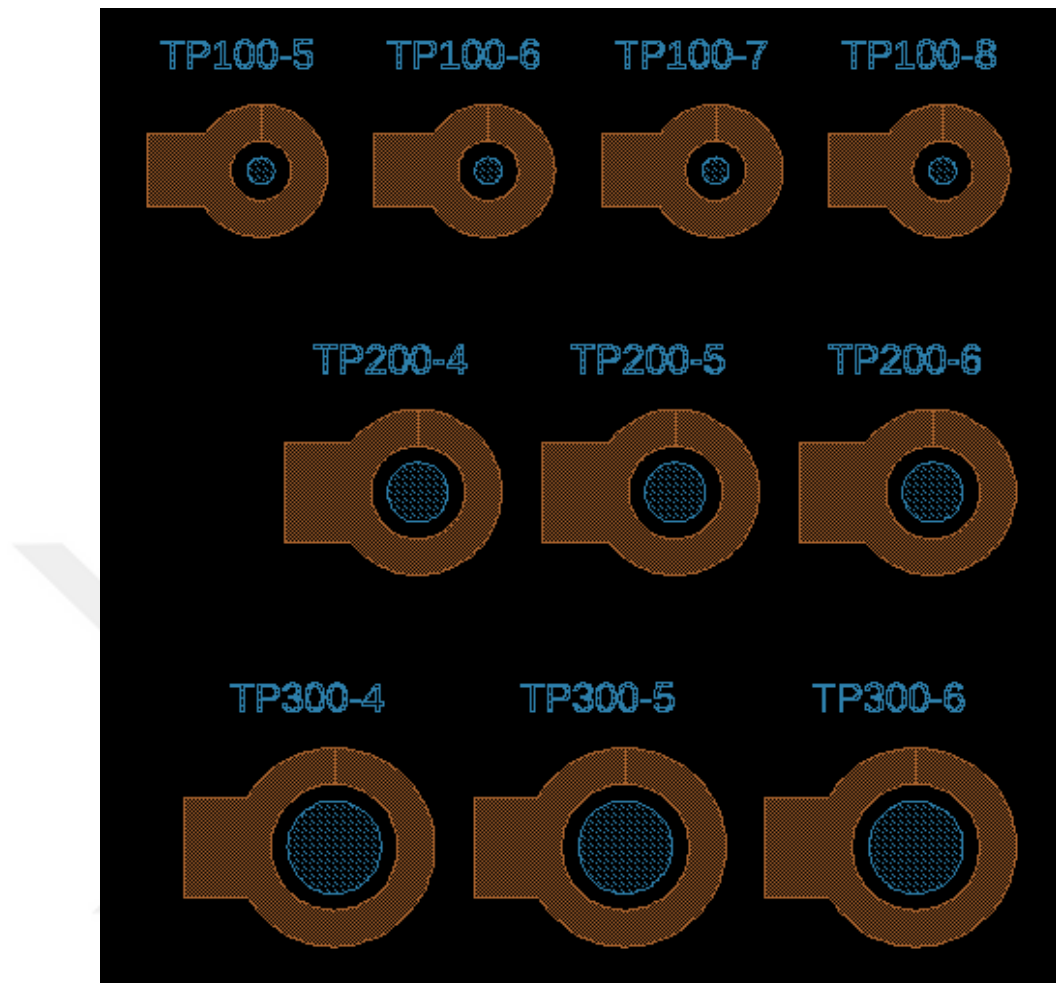


Figure 3.9. Wide area test pixels layout design

3.1.3. FPA Process steps & photomask design

After receiving the InP wafers with designed epi-layer structure from our supplier, all of the remaining cleanroom process is realized in our facilities. Main steps of the process can be listed as;

- Cutting and cleaning of the samples
- PECVD SiN coating
- SiN lithography and etching
- ZnP and SiN cap coatings
- Zn Diffusion

- Diffusion cleaning
- InP 2nd cap lithography and etching
- P metal lithography, coating and liftoff
- N metal triple lithography and etching
- N metal lithography, coating and liftoff
- Metal annealing
- Isolation etching
- Passivation coating and curing
- Passivation opening lithography and etching
- Backside grinding
- AR coating
- Bump lithography, UBM & indium bump coating and liftoff

Each process step will be clarified under separate headings and photomask designs will be discussed for the steps that include lithography work.

3.1.3.1. Cutting and cleaning of the samples

Received epi-wafers are spin coated with photoresist protection layer without lithography and diced by DISCO Automatic dicing saw. Obtained samples are chemically cleaned with Acetone, Isopropanol (IPA) and De-ionized water (DIW). Ultrasonic treatment is used during acetone cleaning. After optical microscope evaluation, if necessary, detailed chemical cleaning with AZ100 remover at 100 °C is applied for 15 minutes.

3.1.3.2. PECVD SiN coating

Cleaned samples are coated with 150 nm thick SiN layer to use it as a hard mask during high temperature diffusion process by SENTECH Plasma Enhanced Chemical Vapor Deposition (PECVD) system. Argon, Silan and Ammonia gasses are used as process gasses. Process temperature was 250 C.

3.1.3.3. SiN lithography and etching

Diffusion openings for FPA pixels are designed circular with 7 μm diameters. Smaller openings would reduce fill factor while larger openings would cause short circuit between pixels considering with lateral diffusion. In this sense, 7 μm is found as an optimum choice. Diffusion openings and base alignment mark patterns are created by AZ5214 lithography on PECVD SiN layer. Using lithography as a mask, SiN is opened by SAMCO ICP RIE system with SF_6 and Argon gasses. Without cleaning the lithography mask, in order to create alignment marks on InP 2nd cap layer, 50 nm dry etch is realized by SENTECH ICP RIE system with BCl_3 and Cl_2 gasses. After chemical cleaning with Acetone, IPA and DIW, O_2 plasma cleaning at 100 W RF power is applied for 2 minutes by Glow Research Asher. Lithography mask layout design and optical microscopy image of a real sample is given in Figure 3.10. Only the fraction of the mask and the sample from the edge is shown for simplicity. Following images will also be shown at the same region. In some steps, mask layout design will include early steps and zoomed one-pixel design will be added for easier understanding.

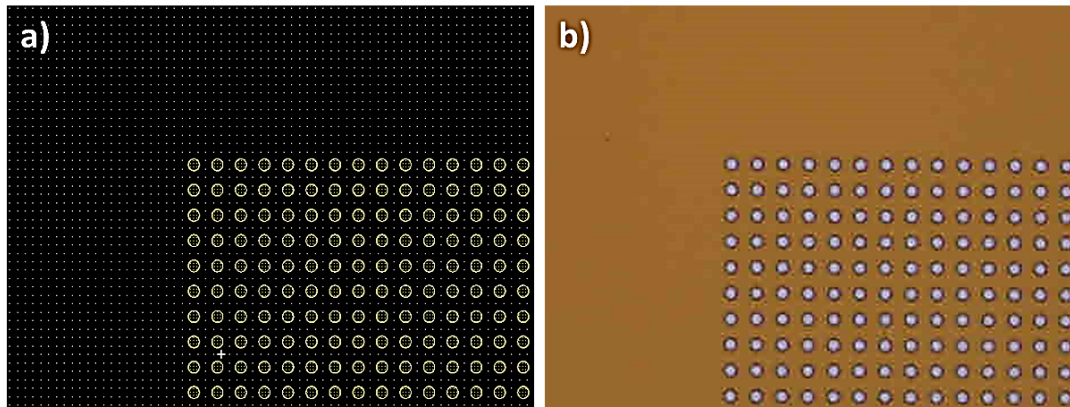


Figure 3.10. a) Diffusion mask layout design, b) optical microscope image of a real sample

3.1.3.4. ZnP and SiN cap coatings

Samples are placed in NANOVAK NVT400 Physical Vapor Deposition (PVD) system that includes both thermal and sputtering sources. ZnP powder is used in thermal source to coat 120 nm ZnP and SiN magnetron target used for sputtering 300 nm SiN respectively. After coating, PECVD SiN mask – ZnP – Sputtered SiN, ready to diffuse stack is formed.

3.1.3.5. Zn Diffusion

Zn diffusion process is optimized by studying 3 different diffusion depth cases given in Figure 3.11. For easier understanding, p-n junction depth after diffusion and the corresponding depletion layer depth in the n side are denoted by d and d' respectively.

In the 1st case, where $d' < 1.4 \mu\text{m}$ ($1.4 \mu\text{m}$ is the depth of the absorber InGaAs and the p-InP layers interface), dark current is found to be decreasing with the increasing junction depth. This shows that the diffusion current is dominating in this case since the increasing junction depth also increases the p type doping level as well as total depletion width. Increasing depletion width also increases the GR current while it decreases the diffusion current. On the other hand, in terms of responsivity, photo current carriers that are located in the absorber InGaAs cannot get through the non-depleted part of the InP near the interface because of the similar hole barrier formation as clarified in the previous chapter with mesa type detectors. Therefore, in the 1st case, we have almost zero photo response. It was impossible to obtain a working detector in this case.

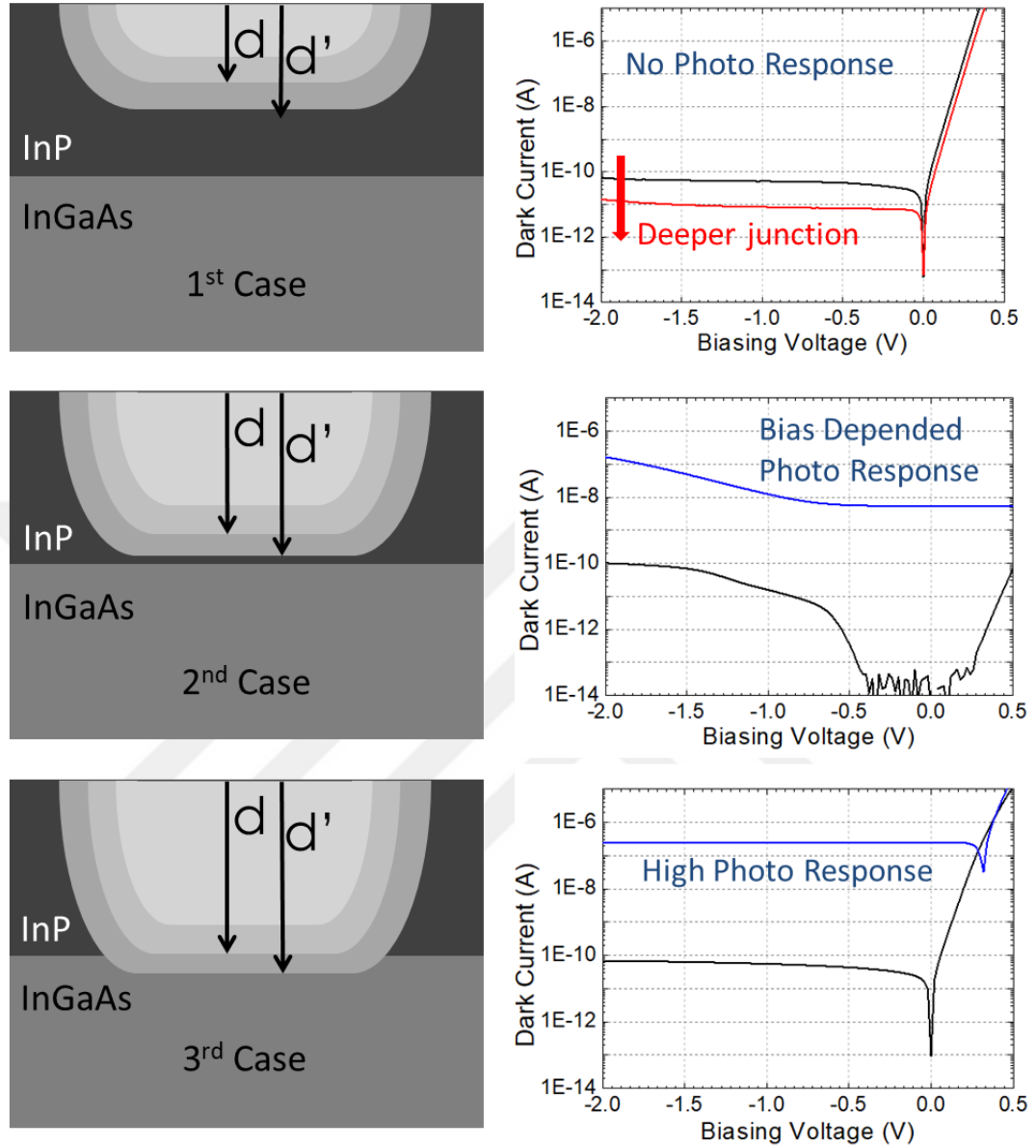


Figure 3.11. Diffusion depth optimization cases

In the 2nd case for which d' is still less than the $1.4 \mu\text{m}$ but with small differences ($<100 \text{ nm}$), both dark and photo current are bias dependent. In the low reverse bias regime, the current characteristics are similar with 1st case with very low dark current values that is under measurement noise limit due to considerably suppressed diffusion current. On the other hand, the photo response is also low. Increasing reverse bias values widen the depletion region as it reaches to the InP-InGaAs

interface and photo carriers created in the absorber InGaAs are started to join to the photo current. However, dark current also starts to increase as GR current created in the depleted interface region, which is formed due to conduction and valance band energy differences among hetero-junction materials (ΔE_c and ΔE_v), joins to the dark current. This 2nd case can be useful for alternative material couples which have small ΔE_c and ΔE_v values that cause smooth transition and suppressed GR current at the interface [107]. Hence, diffusion current would be large due to a decreased hetero-junction energy barrier. Based on these findings, 2nd case is also not suitable for a high-performance detector production.

In the 3rd case, $d' > 1.4\mu\text{m}$, the photo response is bias independent and high enough to give high QE but since InGaAs is depleted even at zero bias, dark current is dominated by considerable InGaAs GR current. To suppress this GR current in p+/n junction, the depletion area can be reduced by n type doping during crystal growth. With careful optimization it is possible to suppress InGaAs GR current almost two orders of magnitude with acceptable increase in diffusion and trap assisted tunneling (TAT) currents and decrease in QE [108]. In terms of performance, repeatability, and ease in processing, we found that an n type doping around $1\text{-}5 \times 10^{16}\text{cm}^{-3}$ levels provides suitable results, which is also given before in the epi-layer design part.

Diffusion process is decided to be realized in the 3rd case. Early optimizations are realized by observing the Secondary Ion Mass Spectrometer (SIMS) measurements of blanked wide area sample with changing diffusion temperatures and durations. Cap layers are etched after diffusion and samples are sent to the AEG Laboratories for measurements. SIMS result of the optimized process is given in Figure 3.12. Process is transferred to the FPA production. In the final form, MTA cylindrical furnace is used for Zn diffusion. Samples are placed in the furnace at room temperature and heated to 475 °C linearly in 60 minutes. After 110 minutes waiting at 475 °C, furnace is cooled down to room temperature and samples are removed afterwards.

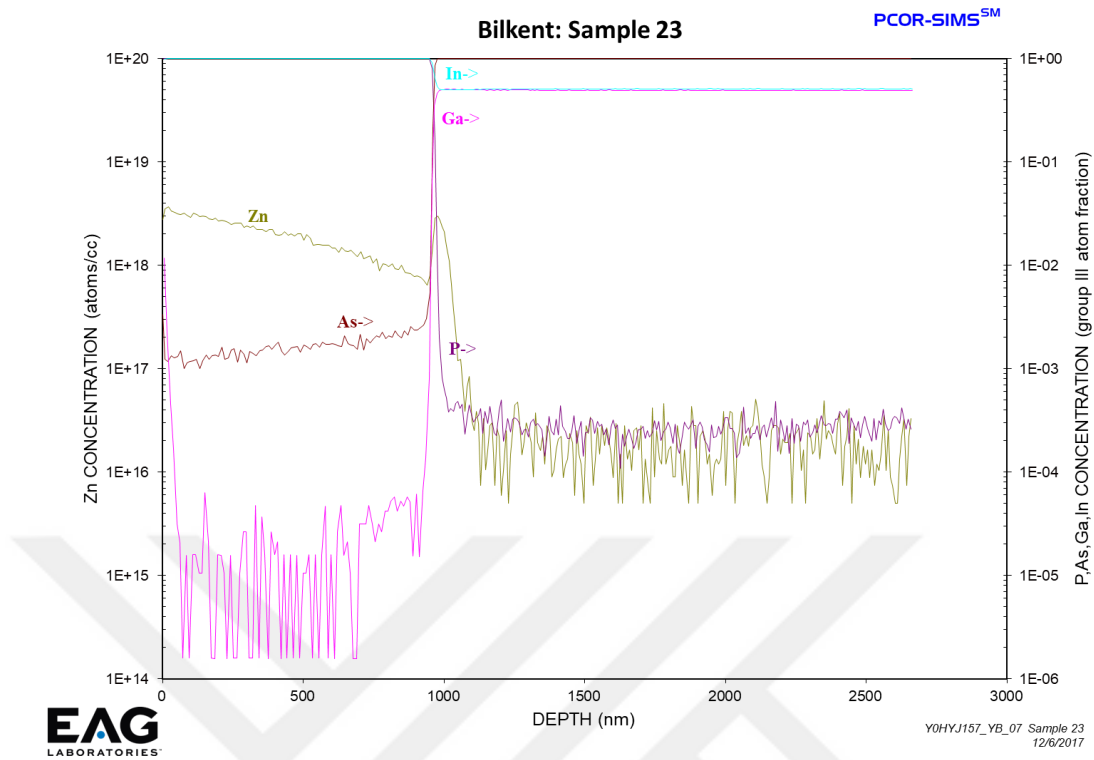


Figure 3.12. Sample SIMS measurement result for the optimized Zn diffusion process

3.1.3.6. Diffusion cleaning

PECVD SiN mask – ZnP – Sputtered SiN coating stack is etched away with HNO₃/HF (1/1) selective acid mixture in 60 seconds. InP 2nd cap layer is remained intact but for longer etching times, crystal impurities on InP starts to grow and creates haziness on the surface.

3.1.3.7. InP 2nd cap lithography and etching

Although the InP 2nd cap is designed as a sacrificial layer, it is not totally etched away on every part of the samples since the alignment marks are created on its surface. Mark areas are protected with AZ5214 lithography process. HCl/H₃PO₄ (1/3) selective acid mixture is used to remove InP 2nd cap layer in 20 seconds, while InGaAs 1st cap layer is kept without significant amount of etching.

3.1.3.8. P metal lithography, coating and liftoff

5 μm openings inside the 7 μm diffusion areas (without considering lateral diffusion) are created with AZ5214 image reversal lithography process. Ti/Au (25/100 nm) metal contacts are coated by Leybold Vacuum thermal PVD system. Samples are placed in acetone containing glass weighing bottles for an overnight liftoff process. Lithography mask layout design and optical microscopy image of a real sample after liftoff process is given in Figure 3.13. Diffusion area in the real sample is invisible to eye therefore only p metal contacts are distinguishable.

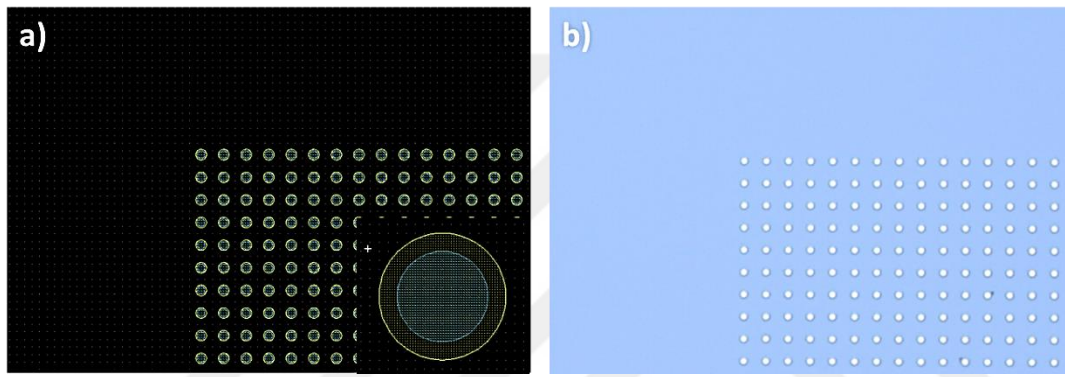


Figure 3.13. a) P metal mask layout design, b) optical microscope image of a real sample

3.1.3.9. N metal triple lithography and etching

After required etching steps, common ground contacts should be formed on the n-InP layer which is around 3.7 μm deeper than p metal contacts. However, indium bump heights for all ground and FPA pixels must be in the same level to have a successful Flip-chip bonding (FCB) process. Considering this, we kept the ground contact pixel region on the InGaAs 1st cap layer and placed ground contact etching region outside of the ground contact pixel region. These two regions will be electrically connected with ground contact metal coating. Therefore, we need to ensure metal continuity. To reach the n-InP layer we need to etch 3 layers i.e. InGaAs 1st cap, p-InP and absorber InGaAs layers. In the case that we use the same lithography with selective wet etchants, because of under etching, continuous connection metal coating will be

very hard, even impossible. To solve the problem, we designed a ladder-like structure with 3 different lithography steps with Shipley S1813 photoresist. In first step, InGaAs 1st cap layer is etched with $\text{H}_3\text{PO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (1/1/3) acid mixture for 30 seconds. In second step, smaller area is opened in the firstly etched region. P-InP layer is etched with $\text{HCl}/\text{H}_3\text{PO}_4$ (1/3) acid mixture for 90 seconds. In the third step, even smaller area than the secondly etched region is opened inside and the absorber InGaAs layer is etched with $\text{H}_3\text{PO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (1/1/3) acid mixture for 150 seconds. Lithography mask layout designs and optical microscopy image of a real sample is given in Figure 3.14.

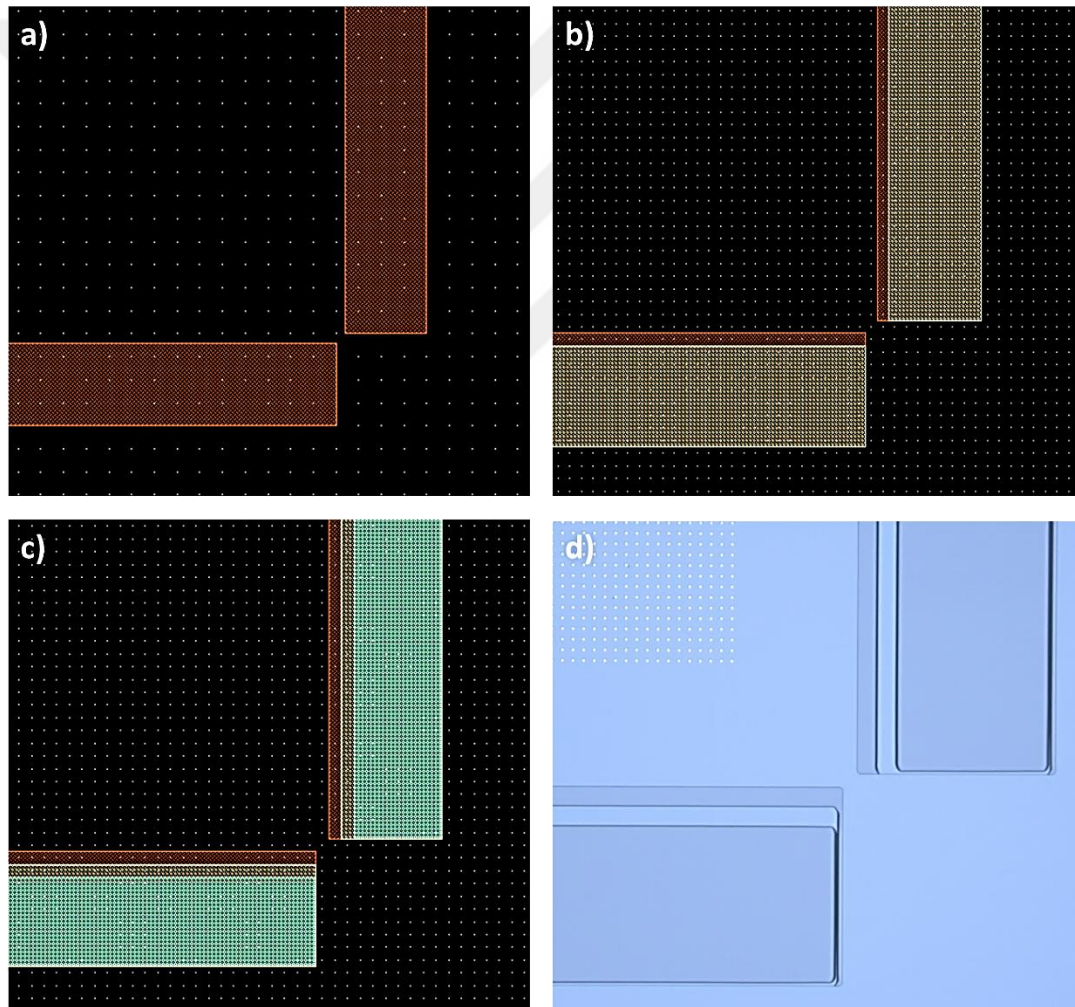


Figure 3.14. Triple n etching masks, a) step 1, b) step 2, c) step 3, d) optical microscope image of a real sample

Scanning Electron Microscopy (SEM) image of triple etched region edge is given in Figure 3.15. Distance between steps of this ladder-like structure is 30 μm . As can be seen from the SEM image, wet etching is created inclined steps, which is also useful for metal continuity.

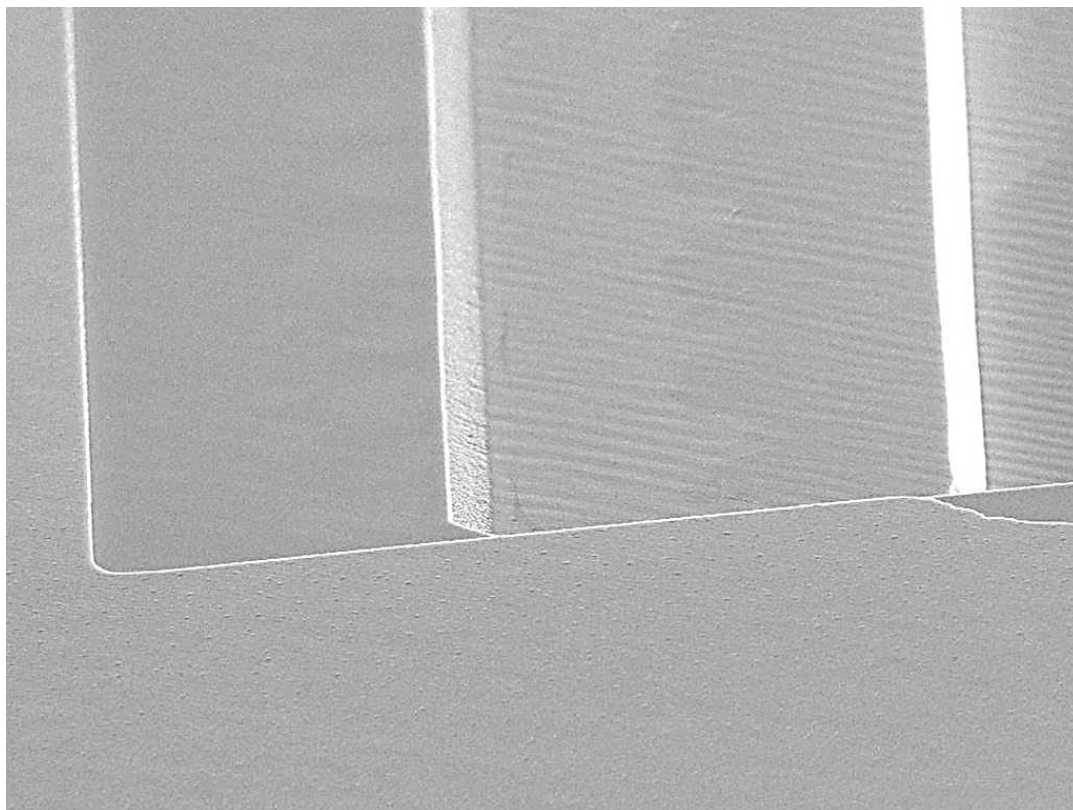


Figure 3.15. Triple n etch SEM image

3.1.3.10. N metal lithography, coating and liftoff

Lithography opening connecting the triple etched region to the ground pixel region is created with AZ5214 image reversal process. Ti/Au (25/100 nm) metal contacts are coated by Leybold Vacuum thermal PVD system. Samples are placed in acetone containing glass weighing bottles for an overnight liftoff process. Lithography mask layout design and optical microscopy image of a real sample after liftoff process is given in Figure 3.16.

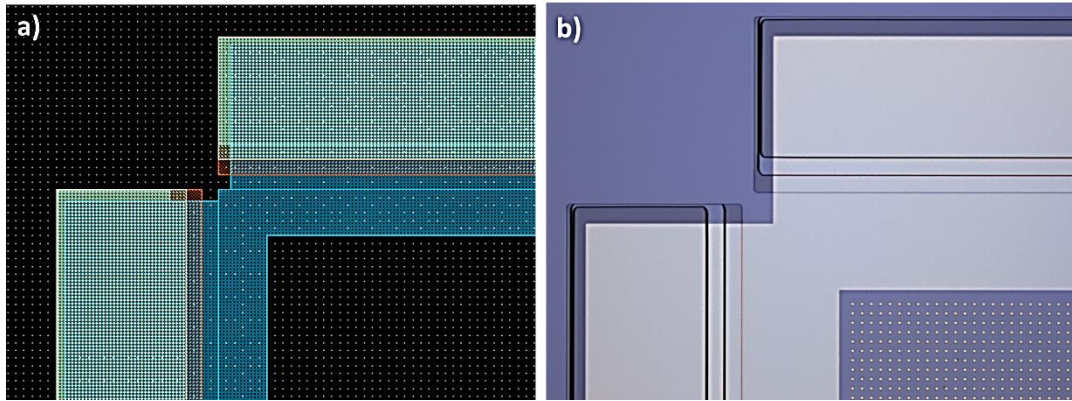


Figure 3.16. a) N metal mask layout design, b) optical microscope image of a real sample

3.1.3.11. Metal annealing

Metal contacts show ohmic behavior even in as-deposit form but to increase contact quality we apply annealing process at 350 °C for 5 seconds by Surface Science Integration Rapid Thermal Annealing (RTA) system. Before the annealing process samples are cleaned with O₂ plasma at 100 W for 60 seconds by Glow Research Asher system.

3.1.3.12. Isolation etching

InGaAs 1st cap layer is designed to obtain easier and high quality ohmic contacts on its surface. However, because of the narrower energy band gap when compared to the InP, it creates critical amount of surface dark current. One way to suppress this dark current mechanism is to etch InGaAs on the inter-pixel area as it will only remain under contact metals. By doing so, depletion region surface which is created around diffusion area is formed on the InP rather than the InGaAs. Depletion region formation on high energy band gap material creates a bottleneck for surface currents as it suppresses them to flow and isolates each pixel from the others. This is realized by isolation etching of InGaAs 1st cap layer with H₃PO₄/H₂O₂/H₂O (1/1/3) acid mixture for 20 seconds. To ensure total isolation, etching is made without any lithography mask. P metal contacts are directly used as masking structures with an acceptable amount of under etching.

3.1.3.13. Passivation coating and curing

Passivation step is one of the most critical steps in detector fabrication. Dielectric material to be coated as a passivation layer is directly effects the surface dark current conditions. We have worked with different type of passivation materials. We have tried SiN and SiO₂ with different coating techniques as PECVD, thermal PVD and sputtering PVD. We have also tried spin-on passivation materials as different types of polyimides and Benzocyclobutane (BCB). Based on our experimental findings, we obtain best device performance with BCB passivation. A sample IV graph of the same test detector before and after the application of BCB is given in Figure 3.17. As can be seen from the graph, IV characteristics are not badly affected even improved after the application of BCB, but this slight improvement most probably related with the cleanliness of the un-protected surface during the measurement. We insert an extra cleaning step after the measurement and BCB is coated to the cleaned surface.

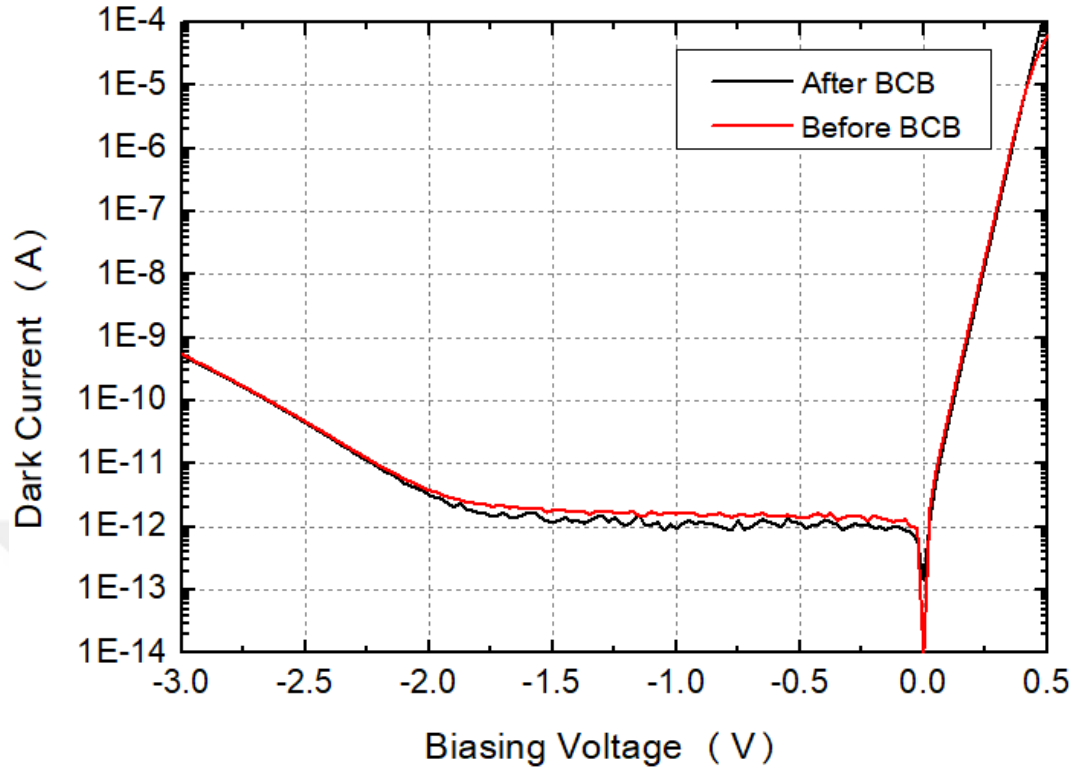


Figure 3.17. BCB passivation effect on the IV characteristics

In FPA process, immediately after the isolation etching process, samples are spin-coated with Dow Chemical's Cyclotene 3022-35 BCB passivation layer. After applying soft bake process on hot plate from 50 °C to 100 °C, samples are placed into an oven and heated from 50 °C to 300 °C in an hour with a slow ramp under nitrogen atmosphere. Hard bake process is realized by waiting for 70 minutes at 300 °C and samples are cooled down to the room temperature.

3.1.3.14. Passivation opening lithography and etching

3 μm openings inside 5 μm p metal contacts and on the n metal coated ground pixel region are created with AZ5214 lithography process. BCB passivation is opened with dry etching by SENTECH ICP RIE system using SF_6/O_2 (1/6) gas mixture. Lithography mask layout design and optical microscopy image of a real sample is given in Figure 3.18.

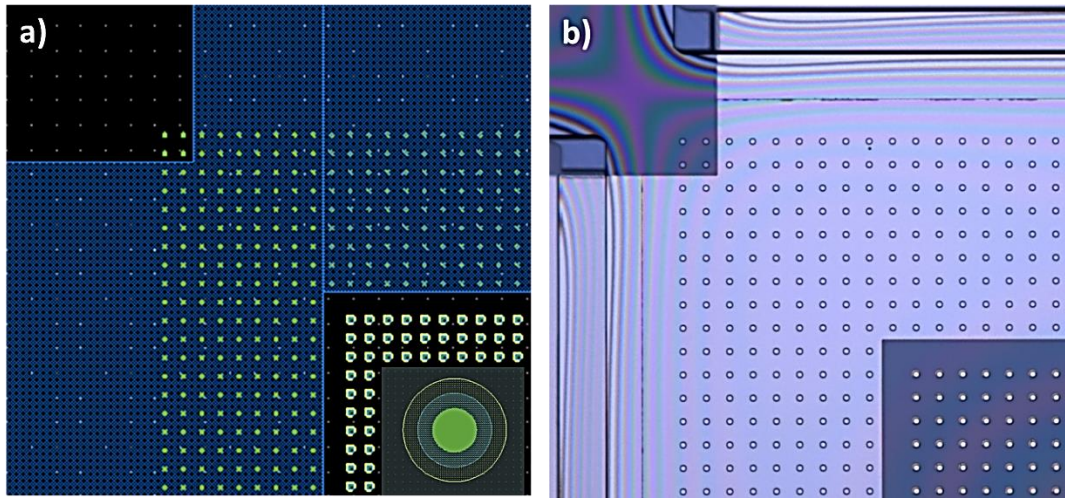


Figure 3.18. a) Passivation opening mask layout design, b) optical microscope image of a real sample

3.1.3.15. Backside grinding

Backside of the samples generally is not clean and smooth when they are first received after MOCVD growth and it is also further damaged during clean room processes. To obtain a clear image, we need to clean the backside of the samples, from where, light enters the detector. Mechanical grinding is useful for both cleaning and smoothing. We use DISCO DAG 810 Grinder system to grind samples for around 30 μm . During the process, surface of the samples are fully covered by AZ5214 photoresist layer for protection purposes.

3.1.3.16. AR coating

Almost %30 of the incoming light radiation reflects back at backside InP and air interface. To increase the QE further, an anti-reflection (AR) layer can be coated at the backside of the samples. Based on available materials in our laboratory, we designed 2 staged AR coating with 140 nm TiO_2 and 240 nm SiO_2 layers. Estimated reflection graph is given in Figure 3.19. As can be seen from the graph, reflection can be reduced under %2 in SWIR region. Surface of the samples are protected with AZ5214 photoresist without lithography and Leybold sputter PVD system is used for coatings.

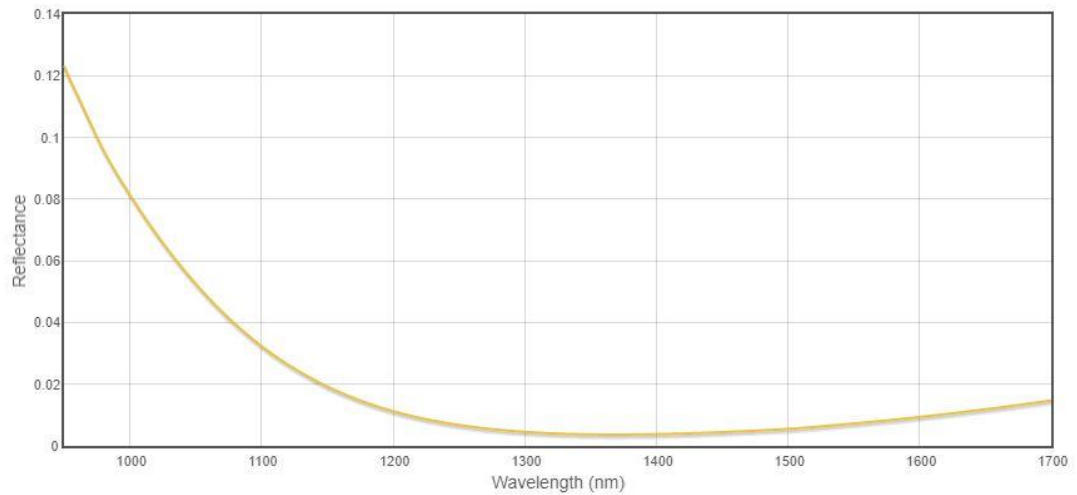


Figure 3.19. a) Estimated reflection graph after AR coating

3.1.3.17. Bump lithography, UBM & indium bump coating and liftoff

8 μm openings are created with AZ2070 negative lithography process. UBM metallization is realized with Ti/Ni/Au (25/35/100 nm) coating by Leybold thermal PVD system. Without removing the lithography, 4-5 μm thick indium is coated by NANOVAK INKAS thermal PVD system. Liftoff process is done by placing samples in NMP containing glass weighing bottles on 80 $^{\circ}\text{C}$ hot plate for an hour. Lithography mask layout design and optical microscopy image of a real sample is given in Figure 3.20. SEM image of the indium bumps after liftoff process is given in Figure 3.21.

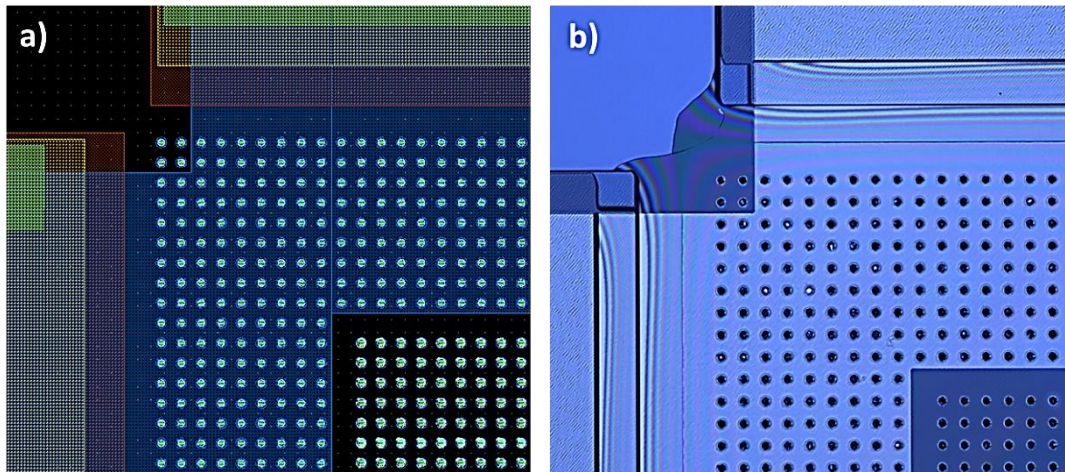


Figure 3.20. a) UBM and Indium coating mask layout design, b) optical microscope image of a real sample

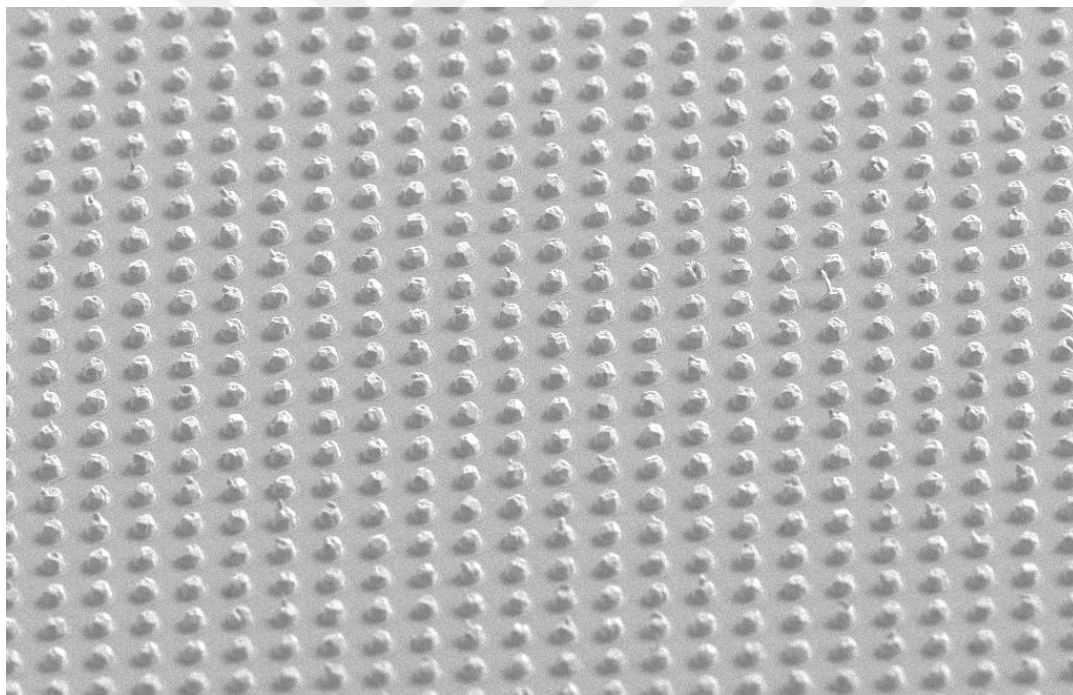


Figure 3.21. a) SEM image of indium bumps after liftoff

3.2. Characterization Results and Discussion

Probe station is used for electrical connections and Agilent B1500 semiconductor analyzer device is employed in I-V characterizations. Measurements are held in an

isolated dark room that is designed as a Faraday cage. In order to reach the single FPA pixel dark current data which remains under the measurement setup noise limitations, we use the characterization pixel arrays consisting of different number of pixels as 96, 56, and 32 that have their p metal contacts as shorted above the dielectric passivation layer. Afterwards, single pixel data is extracted by dividing the measured data with the number of pixels in the corresponding array. Estimated single pixel dark current characteristics from different arrays compared to each other to be able to create a reliable data set and they show very good uniformity as given in Figure 3.22.

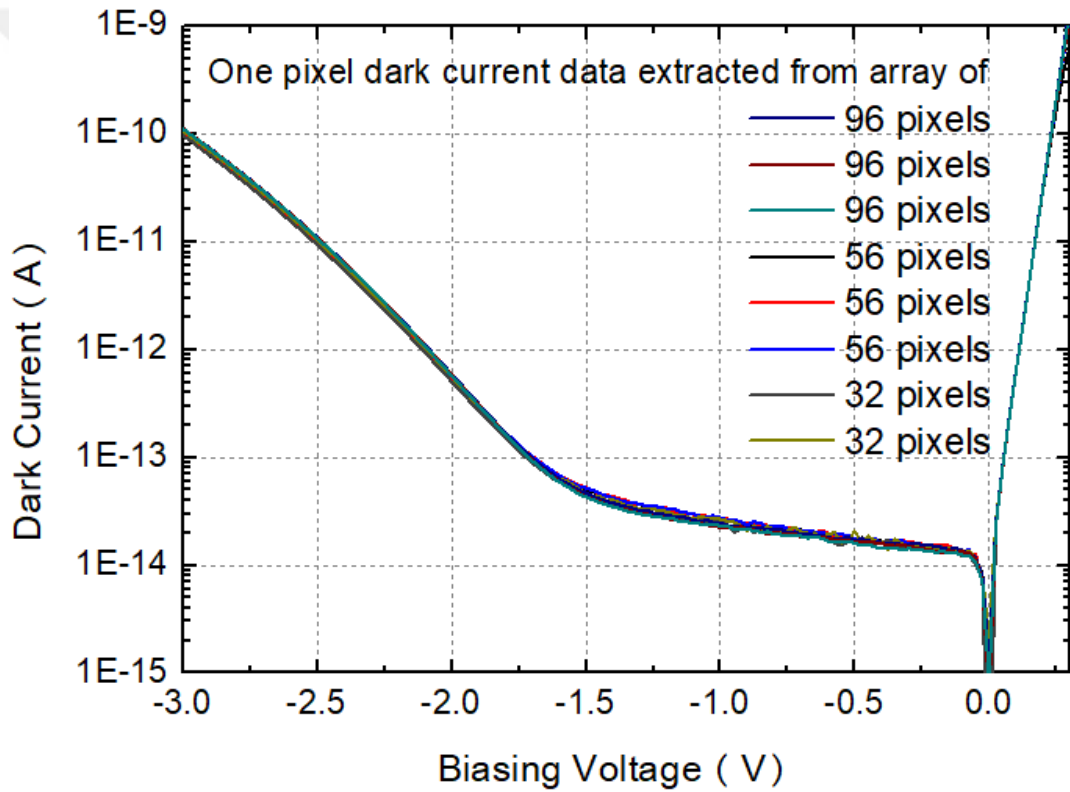


Figure 3.22. One-pixel IV graph extracted from pixel groups with changing number of pixels

Figure 3.22 and all of the following IV figures are drawn with logarithmic Y axis in order to be able to detect small differences. Normally, current values for reverse bias regime are negative as expected but to use logarithmic scale, absolute values are

used. Therefore, the reason of the sharp decrease in current around 0 V bias values normally comes from the change of the sign.

Because of doping values that are designed to reduce the dark current at low bias regime, tunneling currents are triggered at lower reverse bias values. Figure 3.22 also shows that the triggering is occurred around -1.5 V which is harmless for our case since the aimed working bias regime is less than -0.5 V. In all measurements, forward bias currents show expected sudden smooth increase that proves the common contact layer etching and continuous n metal coating are successful and ohmic contacts with low resistances are obtained.

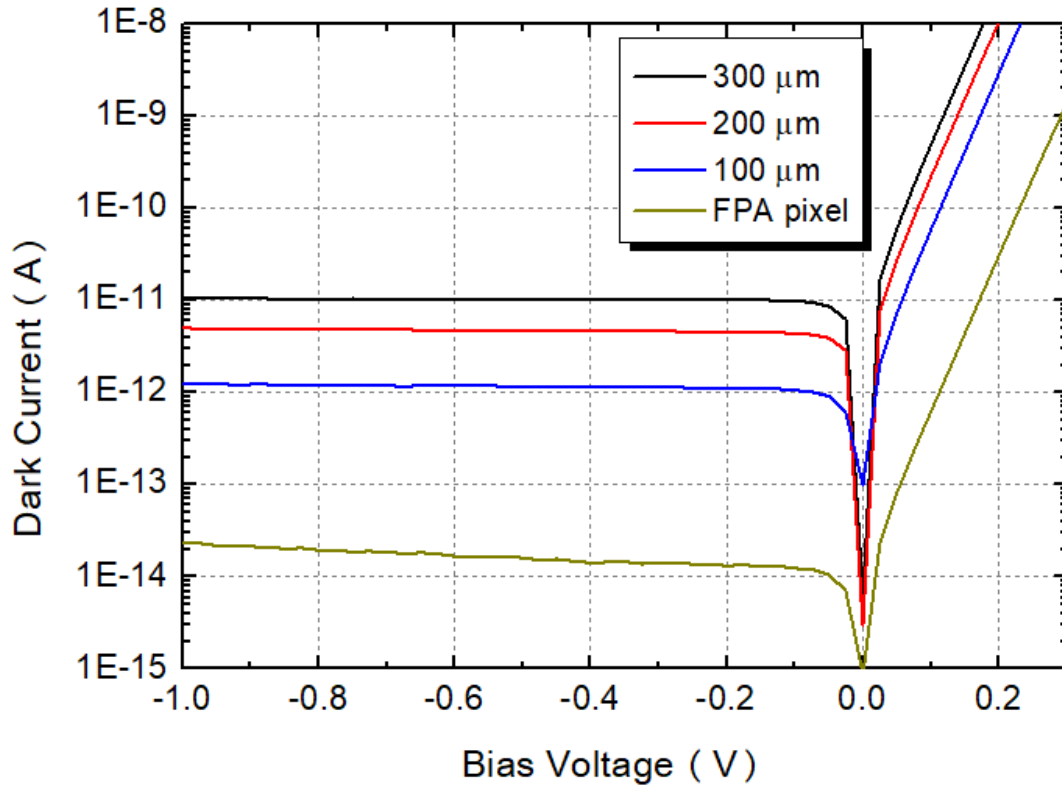


Figure 3.23. Test detectors and estimated FPA pixel dark current graph

Room temperature dark current graphs of the wide area test pixels and the FPA pixel are given together in Figure 3.23. Dark current values at -0.1 V bias voltage are measured as 9.9 pA for 300 μm test pixel, 4.4 pA for 200 μm test pixel, 1.1 pA for

100 μm test pixel and 12 fA for the FPA pixel. All type of pixels shows very good diode characteristics.

Considering the bias dependencies of different dark current mechanisms, we extract components of the dark current by theoretical fitting study for 300 μm test pixel. We achieve perfect fit to the real data by using a model with diffusion and GR current mechanisms. Figure 3.24 shows the separation of total dark current. The diffusion current found as a dominating mechanism. At low bias regime around -0.1 V, total dark current is nearly composed of diffusion current only. When bias is increased to -1 V, GR current starts to be detectable. However, even at -1 V, diffusion current still is the dominating mechanism as it is almost 20 times higher than the GR current.

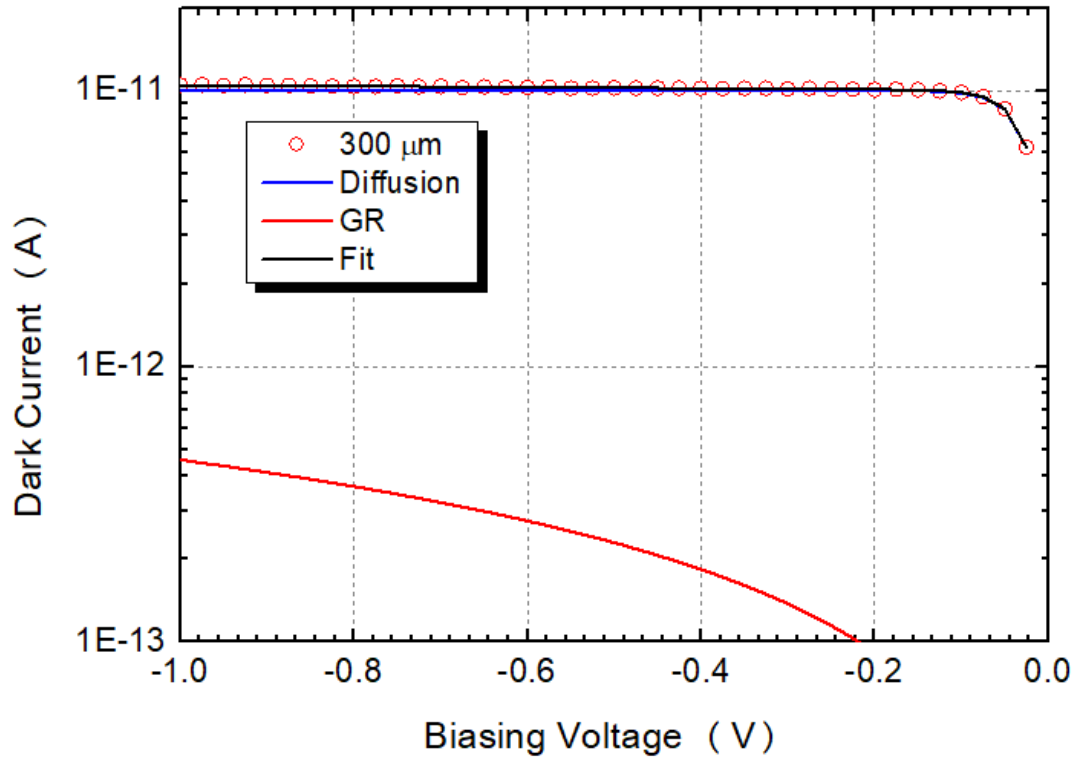


Figure 3.24. Dark current fit study results for 300 μm test pixel

Similar theoretical fitting study is also realized for the smaller area FPA pixels at room temperature. This time to be able to obtain the perfect fit to the experimental data, TAT current mechanism is added to the fitting model. Figure 3.25 shows the

resulted graph. If we compare FPA pixel and wide area test pixel results, we found that the GR current becomes more important and TAT current starts to show itself in FPA pixels. This is mainly caused by the increased area/volume ratio in FPA pixels. However at the low bias regime, diffusion current is still found to be the dominating dark current mechanism.

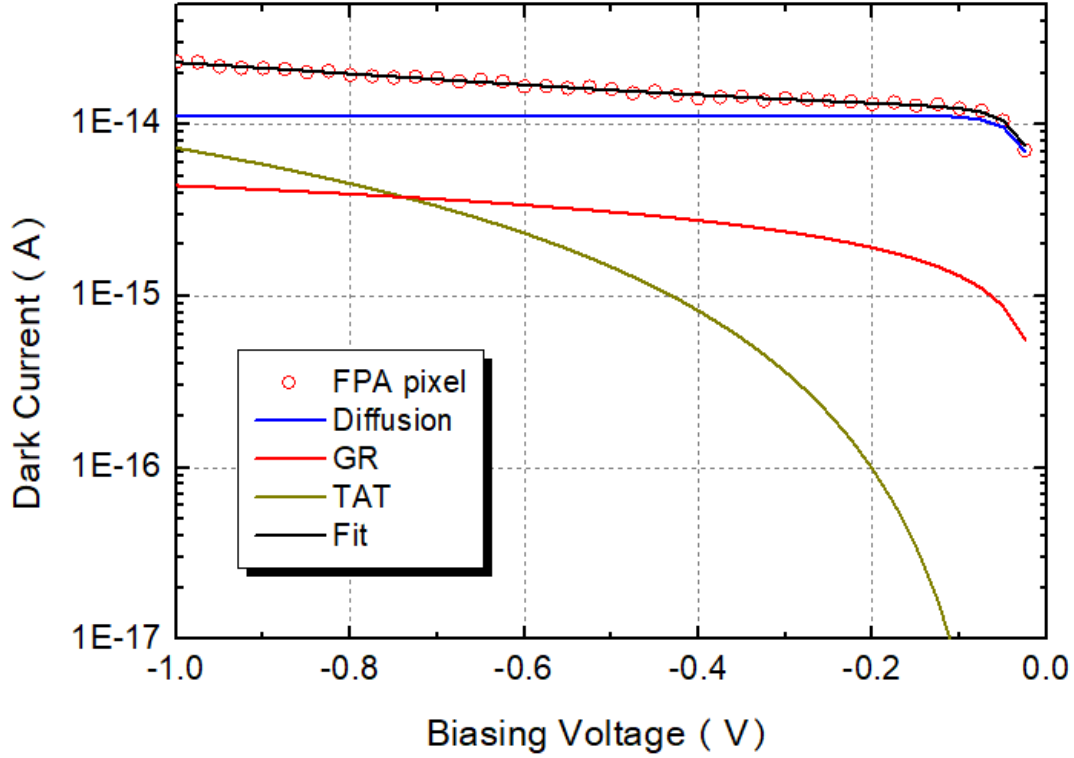


Figure 3.25. Dark current fit study results for FPA pixel

Producing the wide area test pixels and the FPA pixels that have different area/volume ratios also provides us with the ability to separate bulk and surface related dark current components. To do this, we can denote the total dark current of a pixel as;

$$I_{dark} = J_b x S + J_s x P \quad 3.1$$

Where I_{dark} is the total dark current, J_b is the bulk related dark current density in $A/\mu m^2$, S is the active pixel area in μm^2 , J_s is the surface related dark current density in $A/\mu m$ and P is the pixel perimeter in μm .

If we divide both sides with the active pixel area, we get;

$$\frac{I_{dark}}{S} = J_b + J_s \frac{P}{S} \quad 3.2$$

If we plot $\frac{I_{dark}}{S}$ versus $\frac{P}{S}$ graph with dark current data set obtained by each differently sized pixels at -100 mV, slope of a linear fit yields J_s and J_b can be read from the intercept. Figure 3.26 shows the resulted graph. Bulk dark current density is estimated as $1.37 \times 10^{-16} A/\mu m^2$ and surface dark current density estimated as $4.51 \times 10^{-16} A/\mu m$. Both current densities are obtained with a very small amount of error.

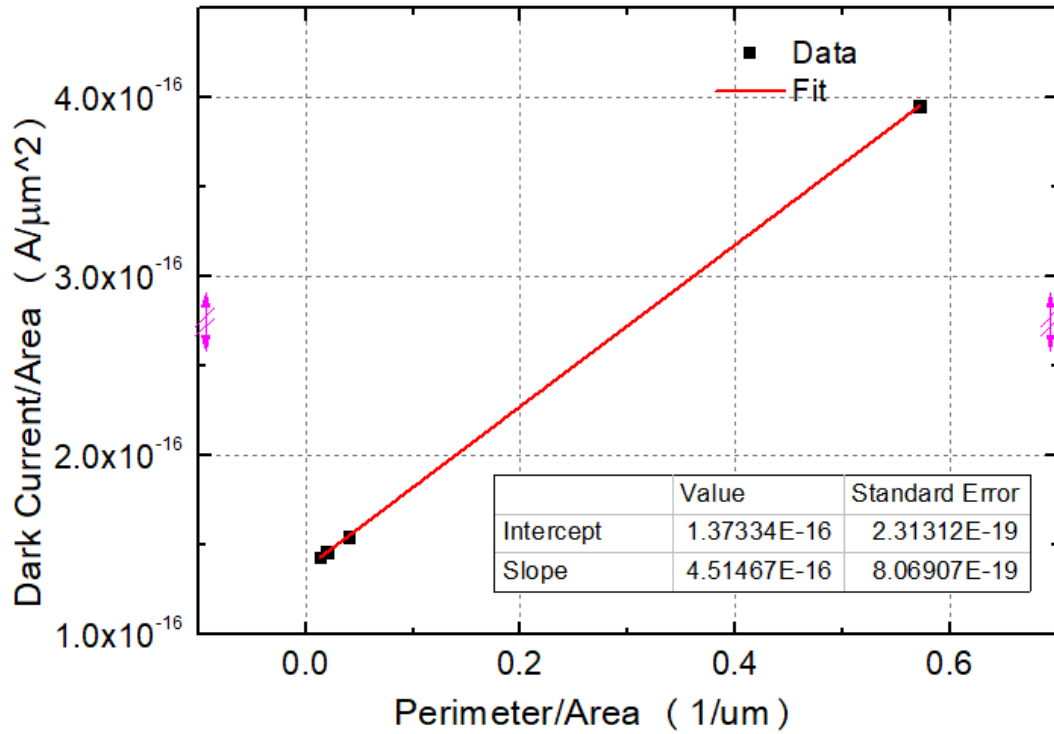


Figure 3.26. Surface and bulk dark current components separation fit

Estimated bulk and surface dark current density values are used to obtain theoretical dark current values with changing active pixel radius. Resulted logarithmic graph is

given in Figure 3.27. As expected, surface current is dominating for small pixels and bulk current is dominating for larger pixels. The crossover point is found around 6-7 μm radius.

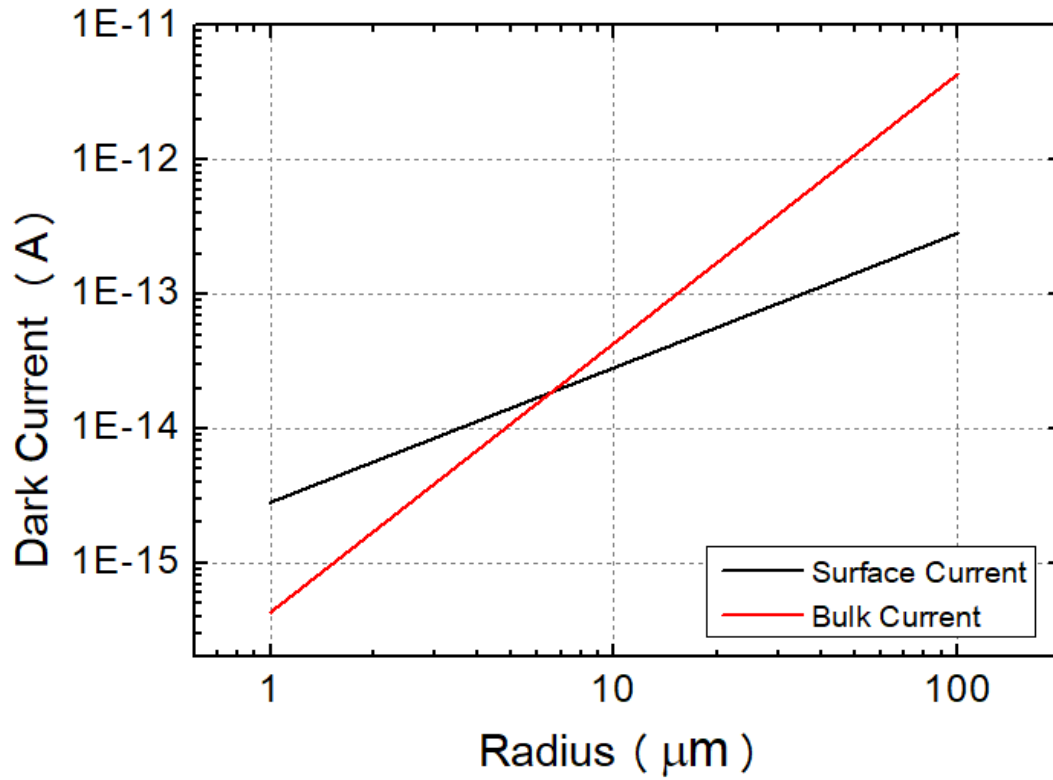


Figure 3.27. Estimated surface and bulk dark current components versus pixel radius

Linear fit study is also applied for all reverse bias values between 0-1 V and surface and bulk dark current components are separated for 300 μm test pixel and FPA pixel. Figure 3.28 and Figure 3.29 show the results respectively. As expected, dark current for the 300 μm test pixel is totally dominated by bulk current while for the FPA pixel surface current is found larger than the bulk current. Besides, just by looking the shape, it is possible to conclude that the bulk current component is mainly composed of the diffusion current, but the surface current component also has important amount of GR and TAT current.

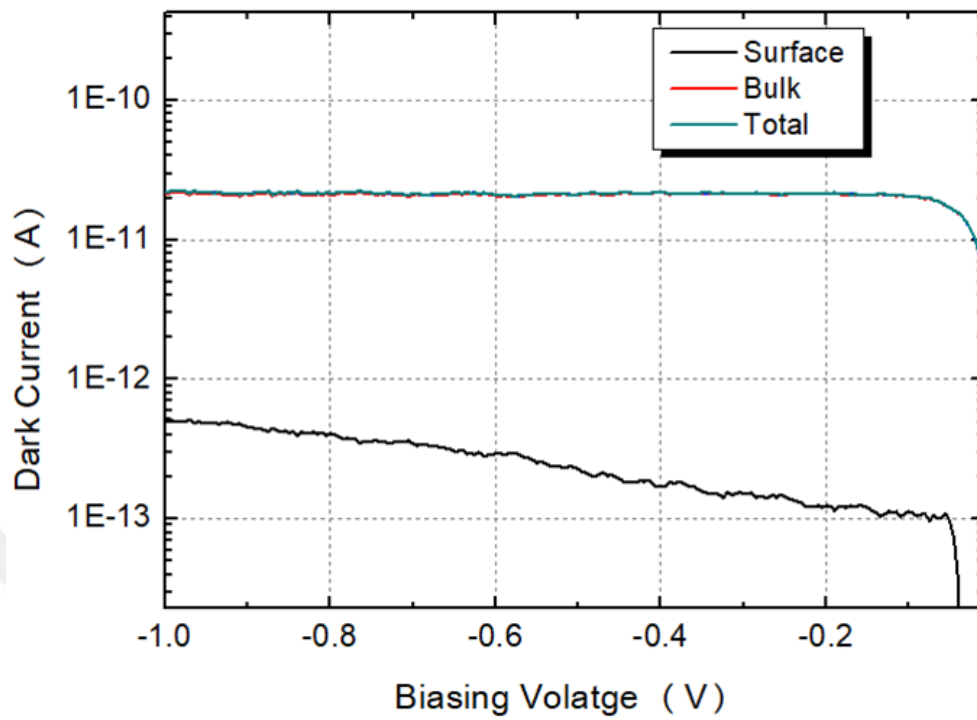


Figure 3.28. Surface and bulk dark current components of the 300 μm test pixel

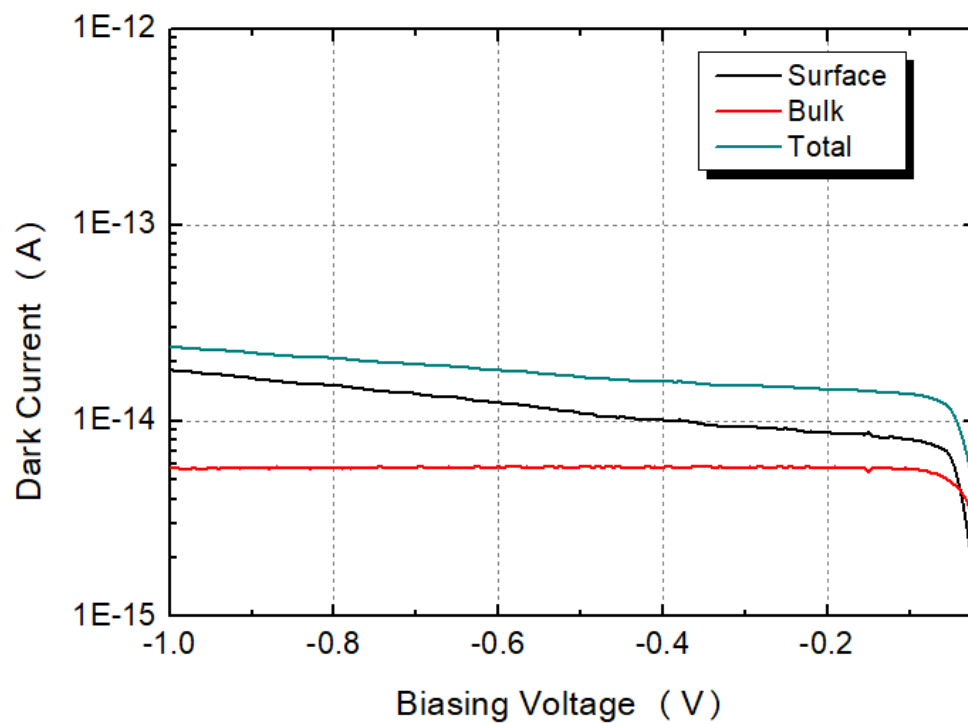


Figure 3.29. Surface and bulk dark current components of the FPA pixel

Fitting study also realized for FPA pixel at forward bias regime by considering the forward bias dependencies of GR and diffusion dark current mechanisms. Results are given in Figure 3.30. The ideality factor is estimated as 1.02 which also proves the dominance of the diffusion mechanism in total dark current. Considering the all aforementioned dark current studies, we can conclude that the dark current is dominated by diffusion current and the surface component is comparable but larger than the bulk component for FPA pixels.

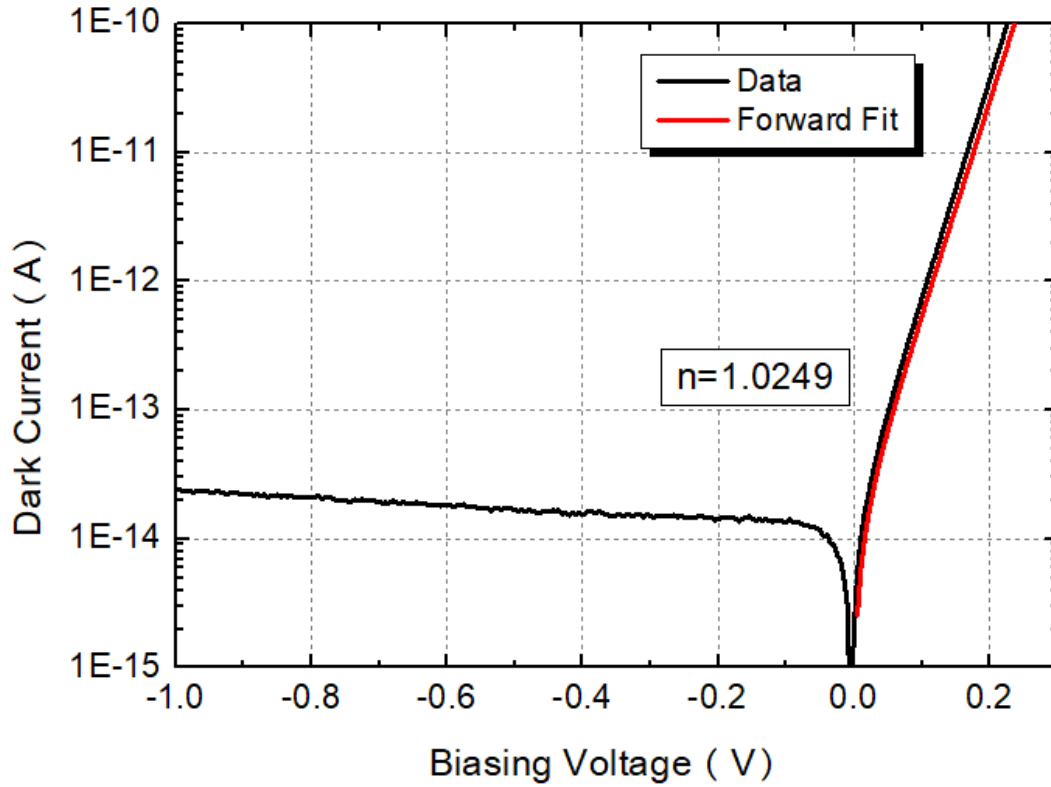


Figure 3.30. Forward bias regime fitting study

Low dark current values are only meaningful with an acceptable responsivity. Responsivity measurements are realized by a 1550 nm laser source coupled to an infrared fiber probe with 10 μm core diameters. Output power is measured in terms of Watts with a calibrated detector. Laser light is directly focused on a large area pixel ($\gg 10 \times 10 \mu\text{m}^2$) in a backside illuminated condition. Background dark current and photo current is measured in terms of Amperes. Difference between photo

current and dark current is estimated. Corresponding responsivity values are directly obtained in terms of A/W without any complicated theoretical work which may reduce the reliability of the results. Figure 3.31 shows the current values under dark and illuminated conditions. Illumination power was measured around 100 μ W. Responsivity is estimated as 1.08 A/W which correspond 86% quantum efficiency at 1.55 μ m. To our knowledge, this is one of the highest quantum efficiency values that are achieved for the detectors with very low dark current values available in the market at the time this thesis is written.

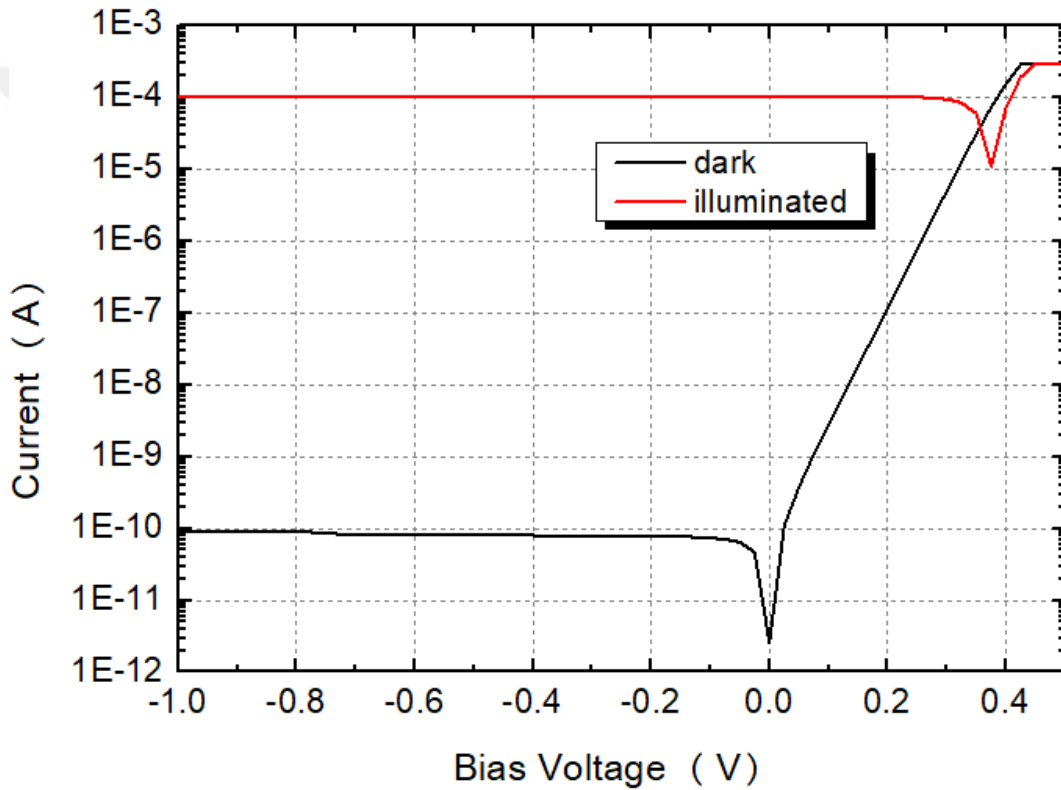


Figure 3.31. Dark and photo current graph used for responsivity measurement

We also check the temperature dependency of dark current for FPA pixels. To do this we use a special chuck that includes thermo electric cooler (TEC). We obtain data from 10 $^{\circ}$ C to 60 $^{\circ}$ C with 2 $^{\circ}$ C increment. Rest of the IV setup was same with room temperature measurements. Measurements for lower temperatures cannot be realized because of humidity condensation on the samples. To avoid it, samples can

be kept under vacuum during measurements, but this was impossible for our experimental setup in which we use probe station to obtain electrical contacts. Another problem was the noise limitations. We have maximum number of 96 pixels in largest group of FPA pixels. Current values fewer than 10 °C were significantly affected by experimental read noise even for the largest group of pixels. The results are given in Figure 3.32. -100 mV FPA pixel dark current at 60 °C is around 600 fA and around 2 fA dark current is measured at 10 °C. Reverse bias IV curve is more flat for higher temperatures as it is dominated by diffusion current. As the temperature is decreasing, diffusion current decreases faster than the GR current. Therefore, GR current becomes more and more significant for lower temperatures and the IV curves become more and more inclined respectively.

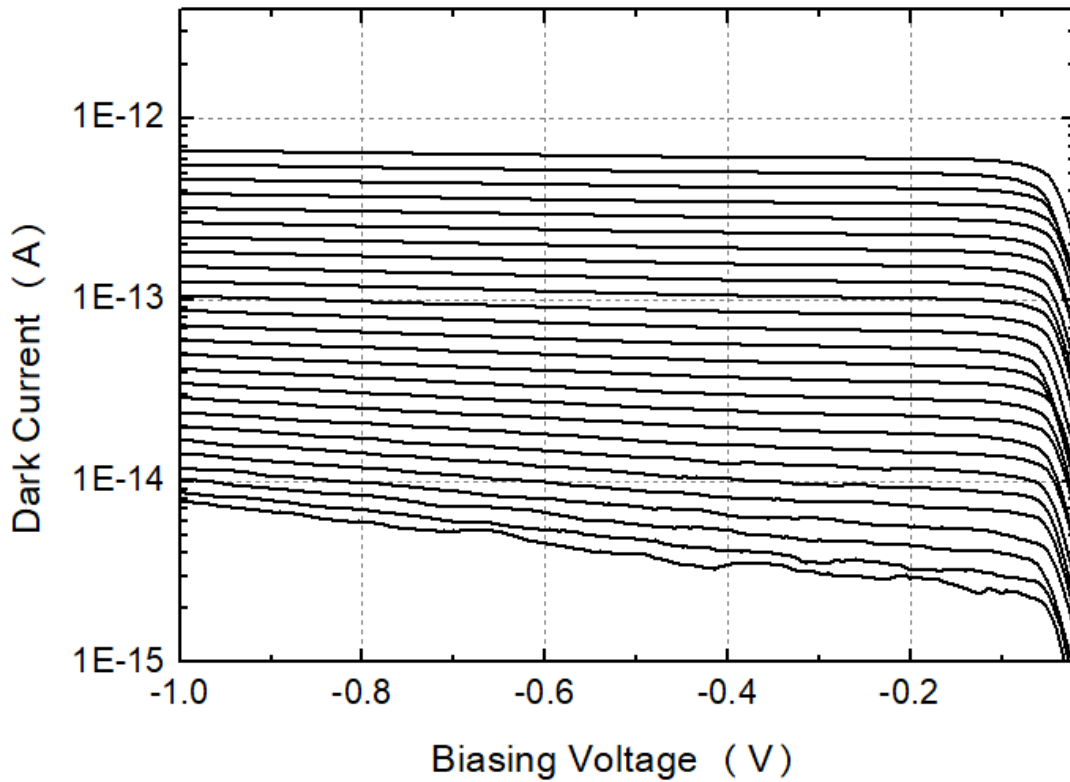


Figure 3.32. FPA pixel dark current values with changing temperatures

Last but not least, we also check the reverse bias dynamic resistances of the FPA pixels. To reduce the Johnson-Nyquist noise, detectors must be biased at the point

where the dynamic resistance has its maximum value. Figure 3.33 shows the dynamic resistance change in the reverse bias regime. We found that the maximum dynamic resistance is obtained around -300 mV bias voltages for our detectors.

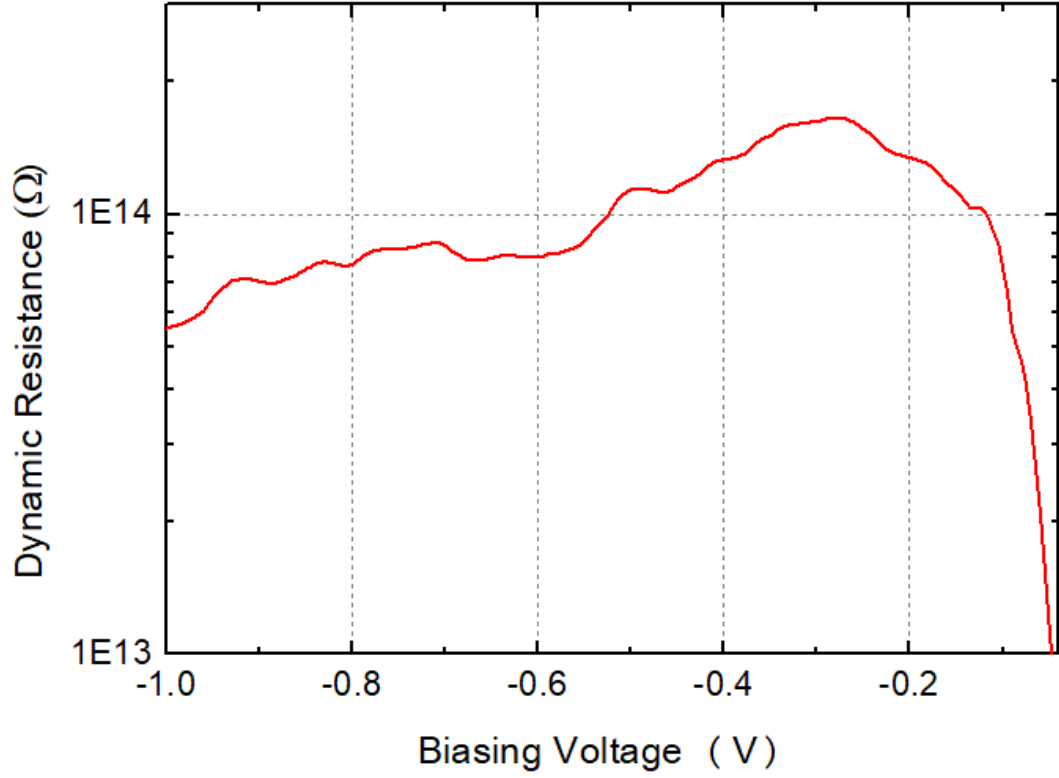


Figure 3.33. FPA pixel reverse bias dynamic resistance graph

Finally, we achieve to design and produce planar type-high performance SWIR detectors with 2 fA dark current and 86% quantum efficiency. The chart given in Figure 3.34 shows the state-of-the-art dark current comparison among the world at the year 2018 [109]. We insert the dark current performance achieved in this thesis work to this chart to show how close we manage to obtain the world's state of the art detector performance.

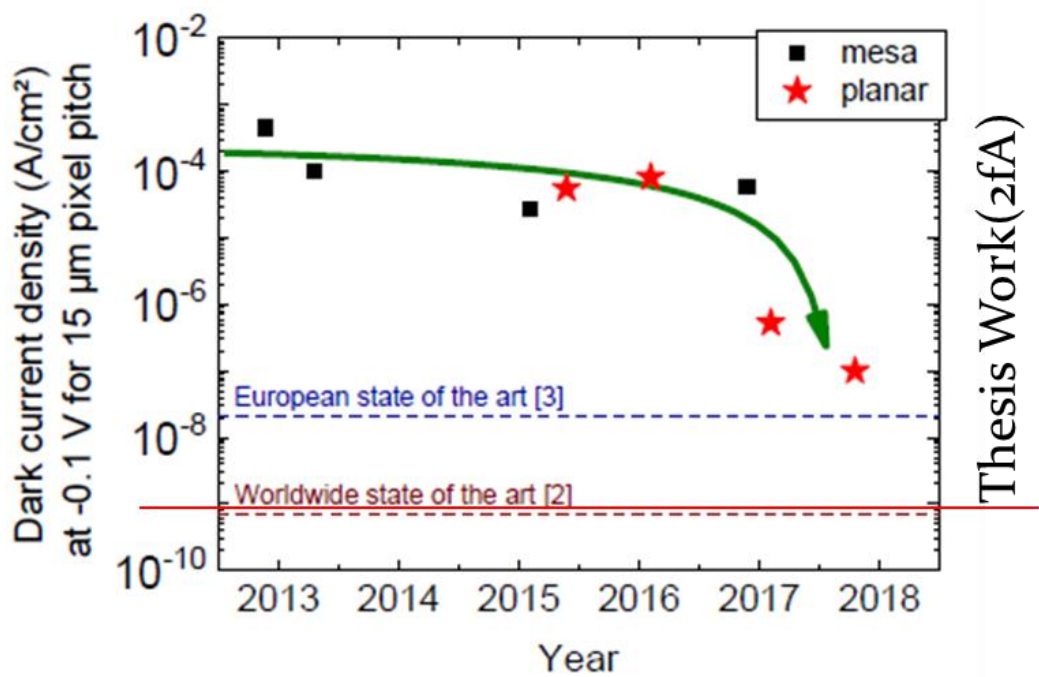


Figure 3.34. FPA pixel dark current comparison chart

CHAPTER 4

POST PROCESS OPTIMIZATIONS AND FINAL PRODUCTS

4.1. Post Process Steps

After finishing clean room processing of the FPA chips, remaining steps to create a working camera, gathered under the post processing title. Main steps of the post process can be listed as;

- FPA dicing and ROIC preparation
- Flip chip bonding
- Under-fill epoxy injection
- Wire-bonding
- Camera design and montage

Each post process step will be clarified under separate headings.

4.1.1. FPA Dicing and ROIC Preparation

FPA chips with indium bumps are spin coated with a thick photoresist protection layer without lithography and diced by DISCO Automatic dicing saw through the lines located 250 μm away from the edge of the n etched region. Obtained FPAs are chemically cleaned with Acetone, IPA and DIW. O_2 plasma cleaning with 50 W RF power is applied for 30 seconds by Glow Research Asher system to remove possible photoresist residuals.

MT12815CA capacitive trans-impedance amplifier (CTIA) ROIC chips designed by Mikro Tasarım Company [110] are used to read signals from the FPAs. ROIC chip specifications are given in Figure 4.1. UBM and indium coating steps are done as similar with the FPA chips. 8 μm openings on each ROIC pixel are created with AZ2070 negative lithography process. UBM metallization is realized with Ti/Ni/Au (25/35/100 nm) coating by Leybold thermal PVD system. Without removing the

lithography, 4-5 μm thick indium is coated by NANOVAK INKAS thermal PVD system. Liftoff process is done by placing samples in NMP containing glass weighing bottles on 80 $^{\circ}\text{C}$ hot plate for an hour. After optical microscopy inspection, final cleaning is made by placing the ROIC chips in AZ100 remover solution at 120 $^{\circ}\text{C}$ for half an hour. Also, O_2 plasma cleaning with 50 W RF power is applied for 30 seconds by Glow Research Asher system to remove possible photoresist residuals.

Product Specifications	Values
Detector Array Format	1280×1024 (SXGA)
Pixel Size	15 μm ×15 μm
Pixel Polarity	Supports both p-on-n and n-on-p detector arrays
Input Circuit Type	Capacitive Trans Impedance Amplifier (CTIA)
Triple Gain	VHG: 10.000 e- HG: 20.000 e- LG: 350.000 e-
Detector Biasing	12-bit programmable in 0.7mV steps
Integration Time	Programmable from 100ns to 1s in 100ns steps
Number of Analog Outputs	Programmable 2, 4, or 8 with reference
Output Swing	< 2.0V with adjustable gain and offset
Readout Modes	Snapshot Operation: ITR and IWR Modes
Windowing	Programmable size and location
Sub-Sampling	2:1 in Rows and Columns for faster scanning
System Clock	Nominal 10 MHz (upto 12.5MHz)
Frame Rate	≤ 60 Hz at full frame, upto 1000 Hz with windowing
Power Dissipation	≤ 350 mW, 3.3V and 1.8V Supplies
Readout Noise	VHG: < 5 e- rms LG: < 110 e- rms
Operating Temperature	Room Temperature (300K) and Cryogenic (77K)
Temperature Sensor	On-chip active sensor with 1mV/K sensitivity
Wafer and Die Sizes	200mm wafers, 21.7 mm × 21.0 mm
Product Delivery	Tested wafers or singulated parts with test data

Figure 4.1. MT12815CA ROIC specifications [111]

4.1.2. Flip Chip Bonding

We use SET (Smart Equipment Technology) FC150 flip chip bonding system with formic acid vapor reflow process ability. Reflow process cleans the indium oxide layer formation on indium bumps to create better bond fusion. When it is done above the melting point of the indium i.e. $\sim 156^{\circ}\text{C}$, reflow process also reshapes the indium bumps into more spherical and uniform structures. Before bonding the FPA and ROIC chips to each other, we apply reflow process at 205°C for 2 minutes. Figure 4.2 shows the SEM images of indium bumps on test samples before and after the reflow process.

FCB system is calibrated before each bonding process. After the calibration, FPA and ROIC chips are loaded to the system as the surfaces with indium bumps facing each other. Samples are heated to the alignment temperatures and kept for minimum of 20 minutes to reach the thermal equilibrium. Two staged, XY and parallelism alignment is realized. In XY alignment stage, positions of each corresponding indium bump on FPA and ROIC chips align to each other with the help of a special microscope system that is able to monitor surfaces of both chips together. In parallelism alignment stage, surfaces of both FPA and ROIC chips are paralleled to each other with auto collimation which is simply, matching the images of the alignment marks that are optically reflected from both chips' surfaces. To ensure good parallelism, auto collimation alignment is performed from the middle of the chips and checked at all 4 edges. Possible particles that may reside the backside of the chips and create a distortion can be detected and cleaned in this way. After finishing the alignment step, chip bonding procedure is applied with optimized bonding cycle. Resulted FPA-ROIC hybrid will be called as detector in the remaining parts of this thesis.

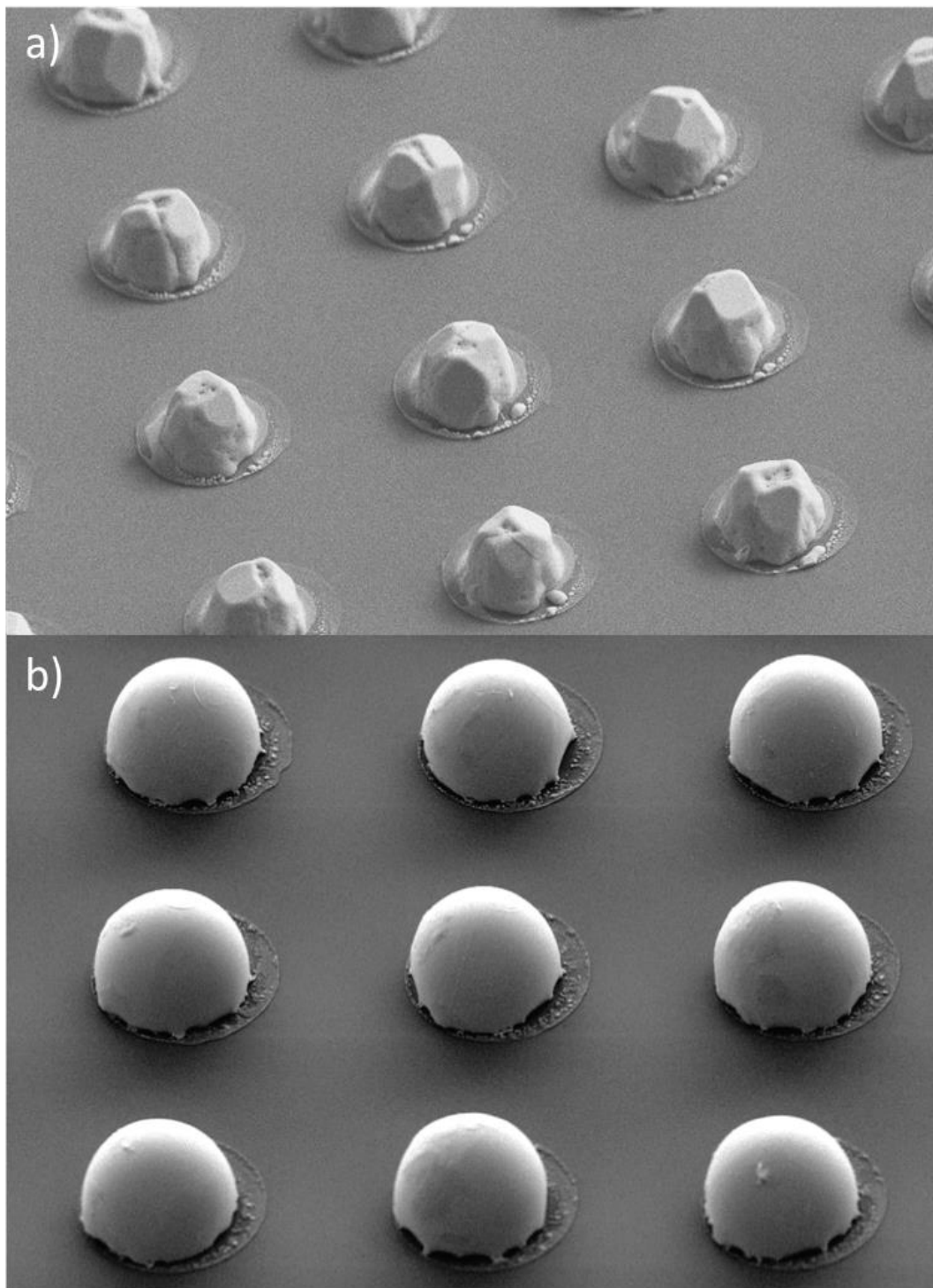


Figure 4.2. Indium bumps on test samples a) before and b) after the reflow process

Bonding cycle has a critical effect on the quality of the image. Therefore, it is optimized carefully with significant amount of time and work. First studies are done by using indium bump coated transparent sapphire FPA and ROIC mimicking samples for both sides to be able to inspect the bonded indium bumps in optical microscope after bonding process. Mainly two different approaches are used as higher bonding forces with lower temperatures and lower bonding forces with higher temperatures. The risk for the first approach is the formation of a high lateral forces that can lead to a sliding of the bumps in the case of even little XY alignment mismatch. On the other hand, second approach requires sensitive control of very low bonding forces and almost perfectly paralleled surfaces as otherwise, melted bonds can easily touch and electrically shorted with neighboring bonds. Studies are continued as two approaches have approximated one another by increasing the temperature while decreasing the bonding force for the first approach, and doing vice versa for the second approach. After the required number of trials, limitations and the possible interval of study is determined.

We continue FCB study with sapphire-silicon FPA and ROIC mimicking samples to optimize the process under the existence of difference in the thermal expansion coefficients. The most appropriate solution for this case was keeping the samples at different temperatures based on the difference between their thermal expansion coefficients in order to be able to create matching expanded sample sizes during the XY alignment stage. We also try to pursue similar approach for bonding step. One of the samples with the smaller thermal extension coefficient is kept at the temperatures higher than the melting point of indium and the other sample with the higher thermal extension coefficient is kept at the temperatures lower than the indium melting point. Another issue was determining the temperatures considering the case when the indium bumps of two samples that are facing each other touches. Temperature of the touched bumps, after heat flow, may stay at the temperatures higher or lower than the melting point of indium. When it is higher, both bumps become melted and fused but, same as aforementioned case, the control of bonding force also becomes hard. When it is lower, at first touching point, melted bump

provides good fusion to the other not-melted bump and after the heat flow they both solidifies. This case provides good control over bonding force and it allows higher bonding forces. We focused our work to this scenario. After optimizing the temperatures and bonding forces, we achieved very good results for sapphire-silicon samples. Figure 4.3 shows the SEM image of a test sample after the optimized FCB process. It is clearly visible that the alignment was very good and indium bonds are fused with very high quality.

We finally switched to the real FPA and ROIC chips. ROIC chip is consists of silicone, yet the FPA chip consists mainly of InP. Considering the thermal expansion coefficient difference between sapphire and InP, required changes are performed and final optimizations are realized directly by inspecting the real camera images of bonded chips. Final FCB bonding recipe is given in Figure 4.4 and in-situ process monitoring graph is given in Figure 4.5

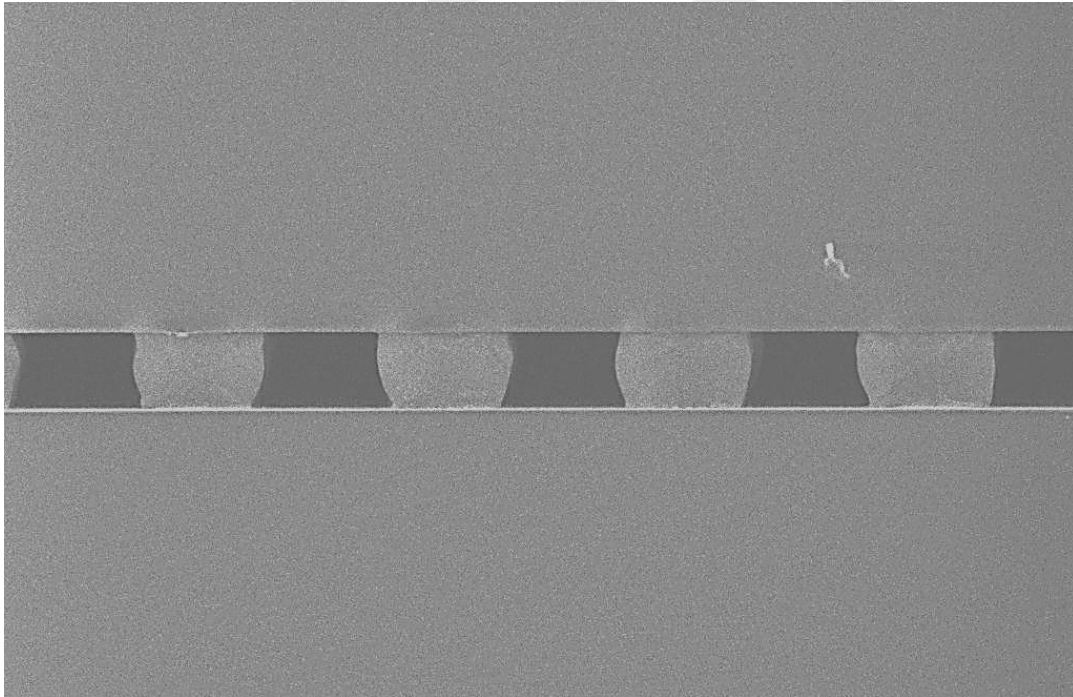


Figure 4.3. Fused indium bumps after FCB process

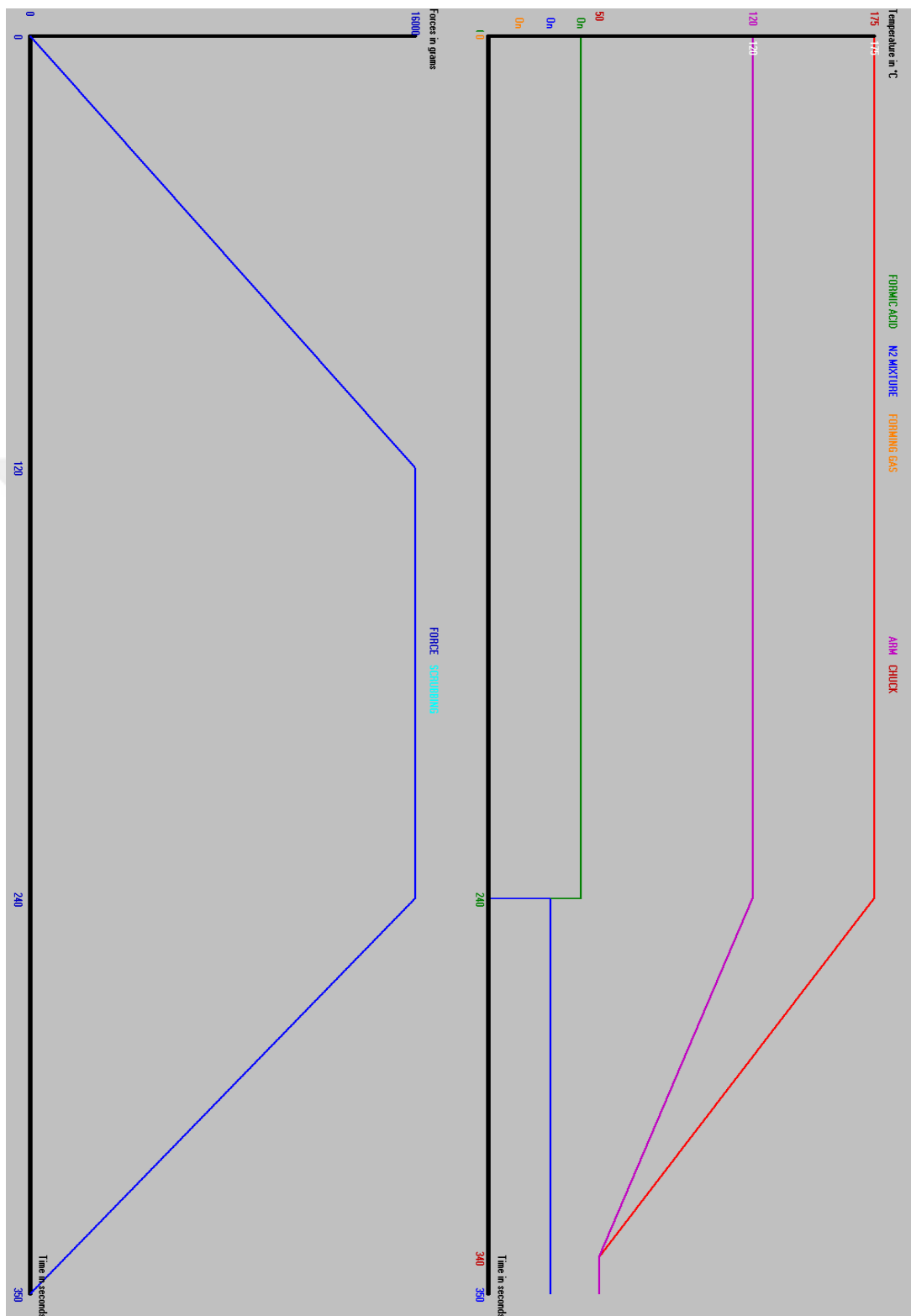


Figure 4.4. Final optimized FCB bonding cycle

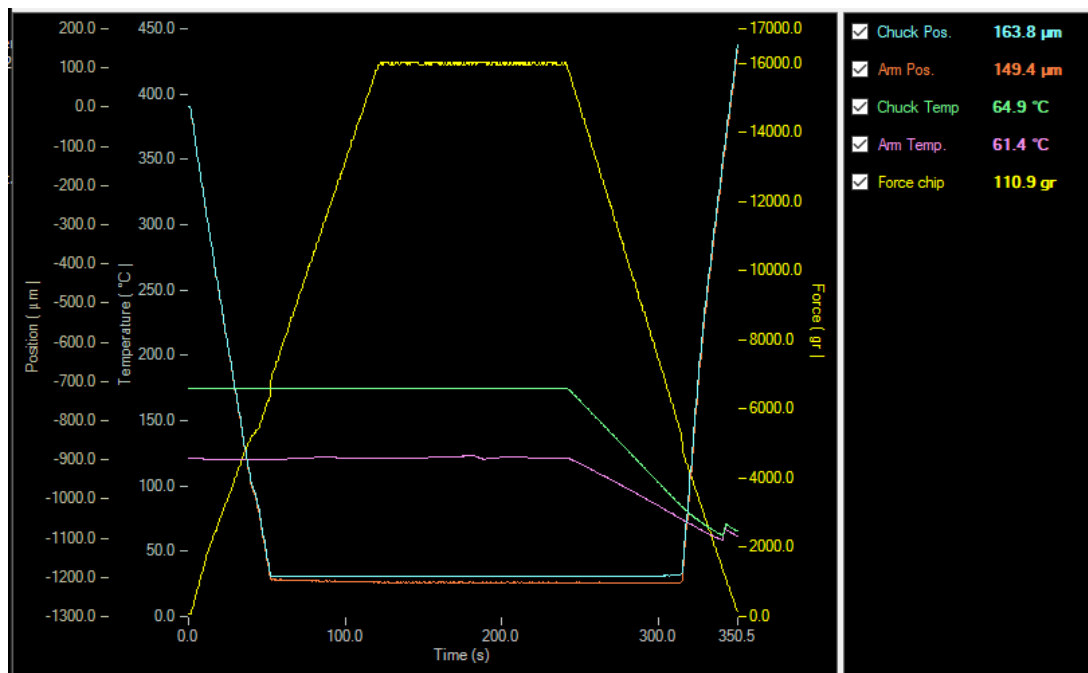


Figure 4.5. FCB process monitoring with real chips

4.1.3. Under-fill Epoxy Injection

After bonding, indium bumps in the detector are open to atmosphere. That may lead to an unwanted possible contamination and oxidation that shortens bumps life. Besides, since the sizes of FPA and ROIC chips perfectly match only near room temperature, indium bumps become the point that feels the maximum stress in the case of a temperature differences or external mechanical bending forces that may arise during camera montage or later also applies stress on the bumps. A dielectric under-fill epoxy can provide a good solution by redistributing the stress and protecting the bump region from external effects by fully filling it.

We chose EPOTEK 301-2 FL under-fill epoxy among couple of alternative materials by directly trying all appropriate materials experimentally. Early under-fill injection study is performed after wire bonding with observing the camera image during the injection in order to be sure that under-fill epoxy fills detector completely without creating trapped air gaps inside. We found that injecting under-fill at the middle of one of the long sides gives the best results. Just 2 drops placed right at the interface

between FPA and ROIC, completely fill inside in around 40 minutes without trapping the air. After being sure about the repeatability of this recipe, we moved under-fill injection step right after the FCB process when the indium bumps are in their cleanest form.

4.1.4. Wire-bonding

MT12815CA ROIC chip have 200+ electrical connection pads. Our electronics engineering group designed a sensor card with a fitting cavity for our detector at the middle. An appropriate aluminum holder is also designed by our mechanical engineering group. Detector is directly attached from the ROIC side onto the aluminum holder by silver epoxy. Sensor card is also attached to the mechanical holder as it is leveled to the ROIC in order to have connection pads on card and ROIC at the same height. Finally, required electrical connections are realized by golden wire bonding among relevant pads of the sensor card and ROIC.

4.1.5. Camera Design and Montage

The studies in this part are mainly completed by fellow group members. Only a short summary of the work without the details is added in order not to deviate from the subject of the thesis.

Our electronics and mechanical engineering groups are designed all required cards, software and mechanical parts for a final complete laboratory prototype. Total of 6 electronics card module is used. Thermo-electro cooler (TEC), which is placed in touch with the aluminum holder of the detector from the other side, and a fan, which is placed in accordance with the air ducts, are added to design to stabilize detector temperature at changing outside weather conditions. Cross sectional view of the final camera design is given in Figure 4.6. Electronic cards and mechanical parts are produced. Gooch and Housego (G&H) Barle and Edmund Optics SWIR lenses are used to acquire camera images. Electro-optic and mechanic tests including thermal tests, vibration tests, liquid tightness tests and etc. are successfully completed. Produced laboratory prototype after camera montage is given in Figure 4.7.

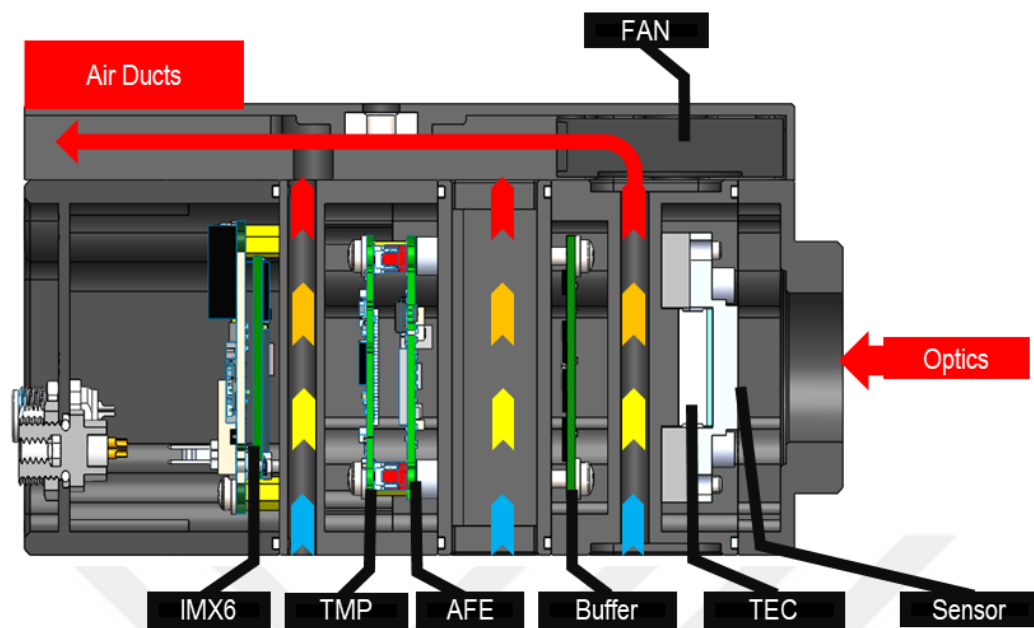


Figure 4.6. Final camera design



Figure 4.7. Final complete camera after montage

4.2. Problems and Solutions

Although every production step is optimized carefully, there always remain indistinguishable effects on the last image quality. Therefore, final optimizations should be realized over real samples by inspecting the camera images. During this thesis work, many detectors are produced with more than 20 different production cycles. In this part of the thesis, common last image problems and solutions will be listed under separate headings.

4.2.1. Bending Related Problems

At the beginning of the FPA production, backsides of the samples were not clean, mainly because of the non-uniform and unwanted material growth at the backside during MOCVD process. To clean it, in early trials we used our old lapping/polishing system. 10-15 μm lapping is performed and followed with polishing. However, we cannot successfully keep the sample surface and backside parallelism. Most probable cause for this issue was the applied protection masking for the surface. Since the process includes chemicals, it is impossible to perform it without surface protection masking. We used spin coated photoresist and wax for masking and adhering. Considering the fact that our samples are diced in rectangular shape, spin coating cannot be performed uniformly, also adhering procedure with wax may cause further non-uniformities. The solution was switching lapping/polishing step with mechanical grinding. By using fine grinding wheels and developing a clean process without further protection mask requirement we achieve to keep the sample surface and backside parallelism. FCB auto collimation function is employed to check parallelism. Figure 4.8 shows the auto collimation marks shape changes before and after lapping/polishing and grinding processes.

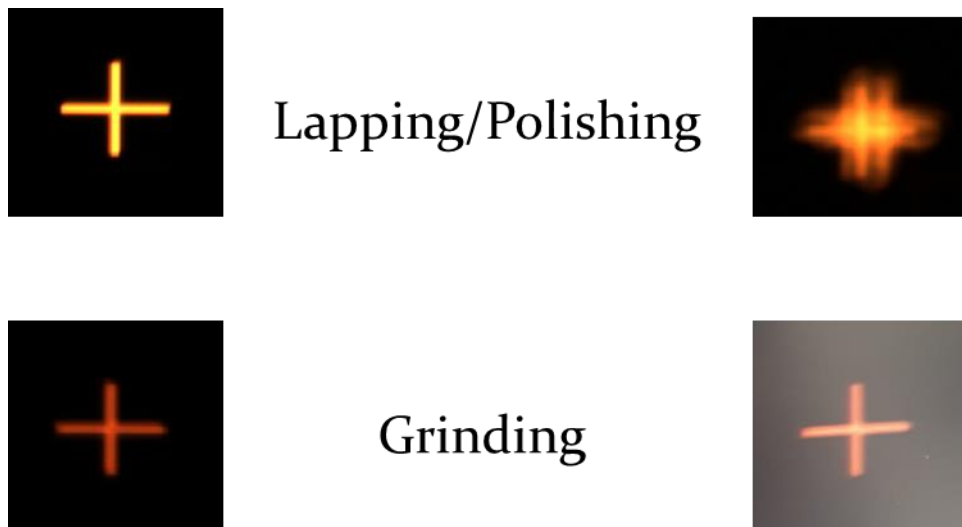


Figure 4.8. FCB Auto collimation marks of samples that are subjected to grinding or lapping/polishing processes.

4.2.2. Passivation Related Problems

One of the challenges related with the spin-on passivation is that the surface of the sample to be passivated needs to be as smooth and clean as possible. Otherwise, passivation can create unwanted openings because of the lack of adhesion, or small hills over contaminations like metal residues during polymerization process under heating.

We mainly faced two different types of unwanted openings. One of them was dot like while the other one was ring like. When the depletion region surface of the pixels becomes unprotected at such regions that the passivation is opened, UBM and indium metal coating residues or other possible contaminations cause very high dark current values that kill the corresponding group of pixels. Figure 4.9 and Figure 4.10 shows sample images from two different detectors that are suffered from unwanted passivation openings. In Figure 4.9, the unwanted opening was ring like and in Figure 4.10, a dot like passivation opening problem occurred.



Figure 4.9. Ring like unwanted passivation opening problem



Figure 4.10. Dot like unwanted passivation opening problem

To solve the unwanted passivation opening problems we worked on polymerization curing recipes. An early solution is obtained by reducing the temperature, but this time passivation become instable under chemicals like NMP. During indium liftoff process, wider unwanted passivation opening is created. Figure 4.11 shows a sample image obtained from a detector with passivation polymerization realized under lower temperatures.



Figure 4.11. Wide unwanted passivation opening problem

Unwanted passivation openings problem is solved by spinning passivation material multiple times between soft and hard bake processes. Passivation process is optimized again for higher temperatures. On the other hand, process becomes more sensitive as hills can be formed easily. At first, these hills seem harmless as they affect only several pixels but after hard bake step, hills become tough enough to disturb very large areas as can be seen in Figure 4.12 and Figure 4.13.

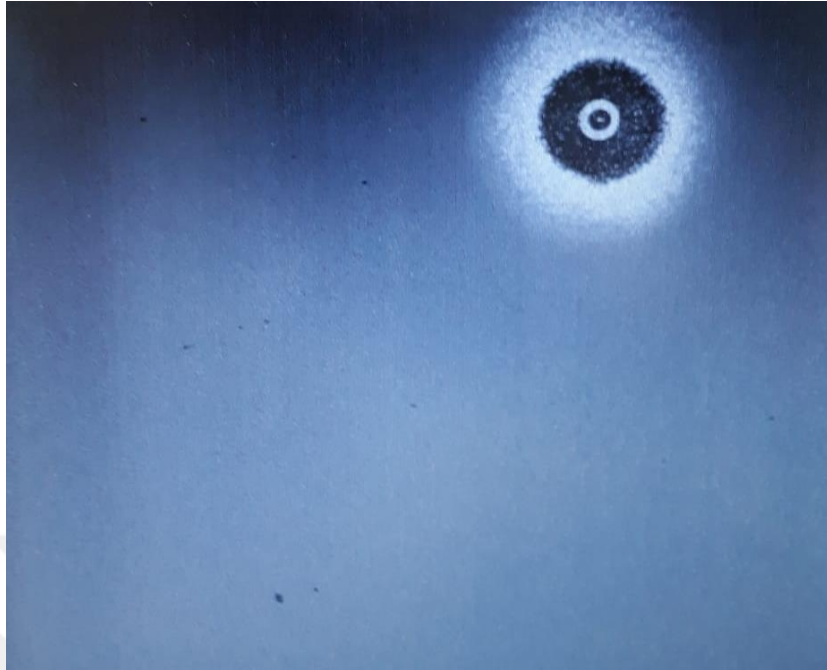


Figure 4.12. Hill formation related passivation problem

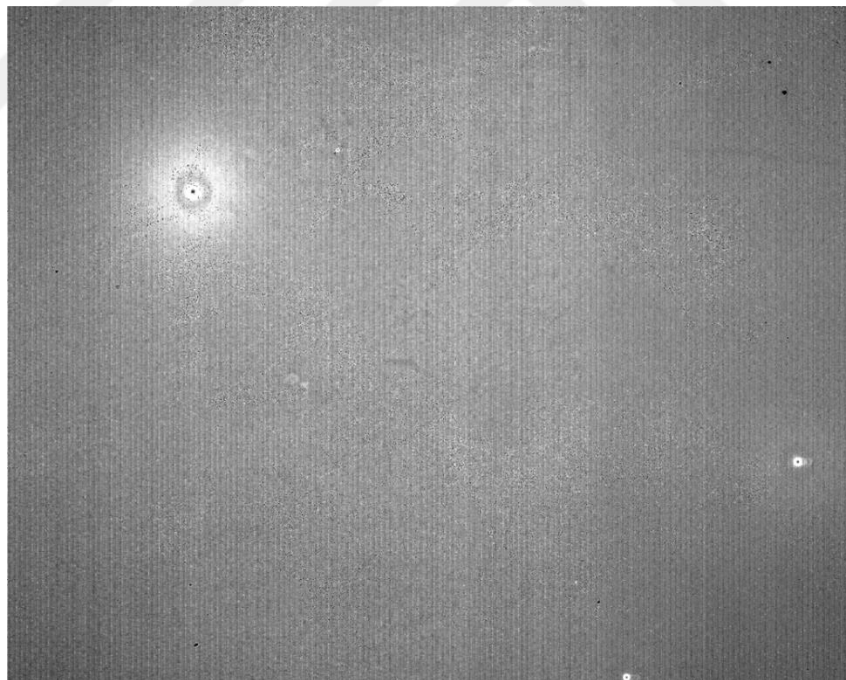


Figure 4.13. Hill formation related passivation problem

To solve this issue, we add extra cleaning steps before passivation. Besides, we inspect samples carefully before passivation and possible contaminations are mechanically removed if needed with needle tip tweezers even it harms couple of pixels around it.

4.2.3. Under-fill Related Problems

One of the challenges we faced during post-processing was choosing the best under-fill material. Worst part of this process was being unable to predict the results without applying the possible under-fill material to a real detector. Figure 4.14 shows a sample image with inappropriate under-fill material. The material used for this detector kills all the pixels it touches and also shrinks a lot during consolidation process. Among the materials that we tried, we found that EPOTEK 301-2 FL is suited for our application.



Figure 4.14. Detector image with inappropriate under-fill material

4.2.4. FCB Related Problems

Considering the sizes of our megapixel chips, FCB becomes a real challenge even SET FC150 system that we used is one of the best systems all over the world. Stress distribution on samples, inevitable bending related to all kinds of coatings, different thermal expansion coefficients between FPA and ROIC chips, non-uniformity of indium bump heights, flatness of multiple times used system calibration tools and chips etc. can have significant effect on FCB quality. Considering together with these possible causes of problems, there are couple of situations for which FCB system limitations play a role.

We can use our system mainly in two modes as controlling the bonding force or controlling the bonding displacement. Force control at very low values (~ 100 gr) is not sensitive enough to have reproducible processes. Our FCB recipes commonly include formic acid and nitrogen purging gasses. To be able to fix the low bonding force in the existence of gas flows can turn into a bonding and de-bonding cycles for which the chips approach each other and move away in a cycle. For such a case, it is logical to use the system with bonding displacement control mode. On the other hand, when we try to control the bonding displacement, we can cure bonding and de-bonding cycles but displacement amount cannot be controlled in a sensitive manner at μm levels in the presence of comparable amount of motor screw backlash. Considering these cases, we try to work with higher bonding forces with lower temperatures without melting the indium bumps on both chips. However, for high bonding forces ($\sim 30\text{kg}$) we faced with a directional gliding problem for some of the samples. Figure 4.15 shows FCB of a sapphire-sapphire test sample with good quality while Figure 4.16 shows FCB of similar samples with directional gliding problem. This problem occurs especially at the corners. Figure 4.17 shows an image taken by a detector with similar FCB problem. This problem can be regarded as a rare problem, yet we developed recipes with under 20 kg bonding forces to stay at the safe side.

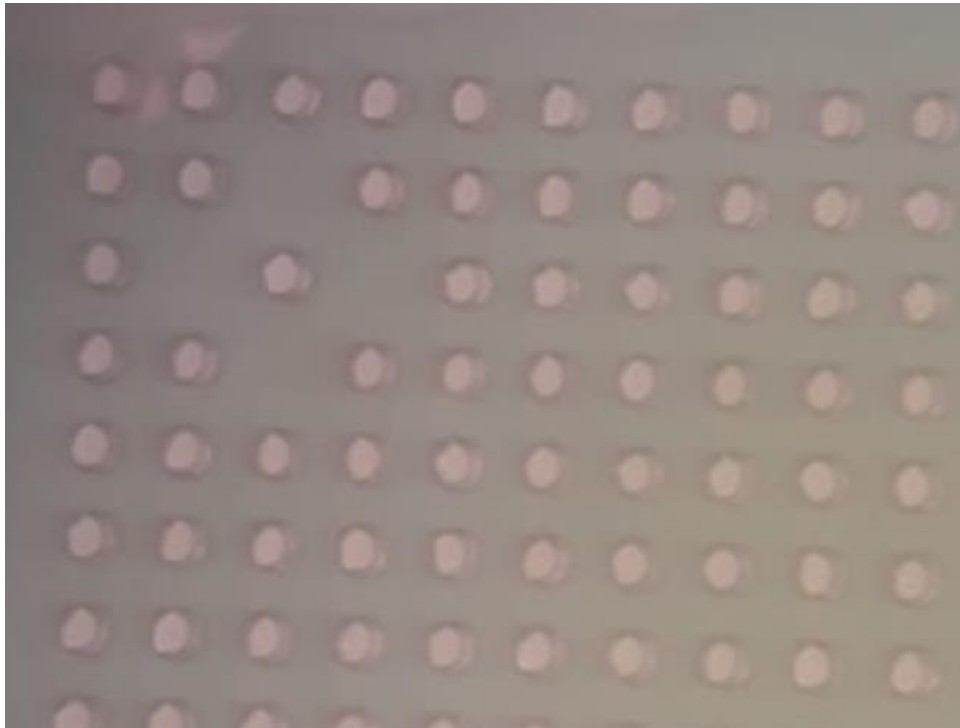


Figure 4.15. Sapphire to sapphire FCB with good quality

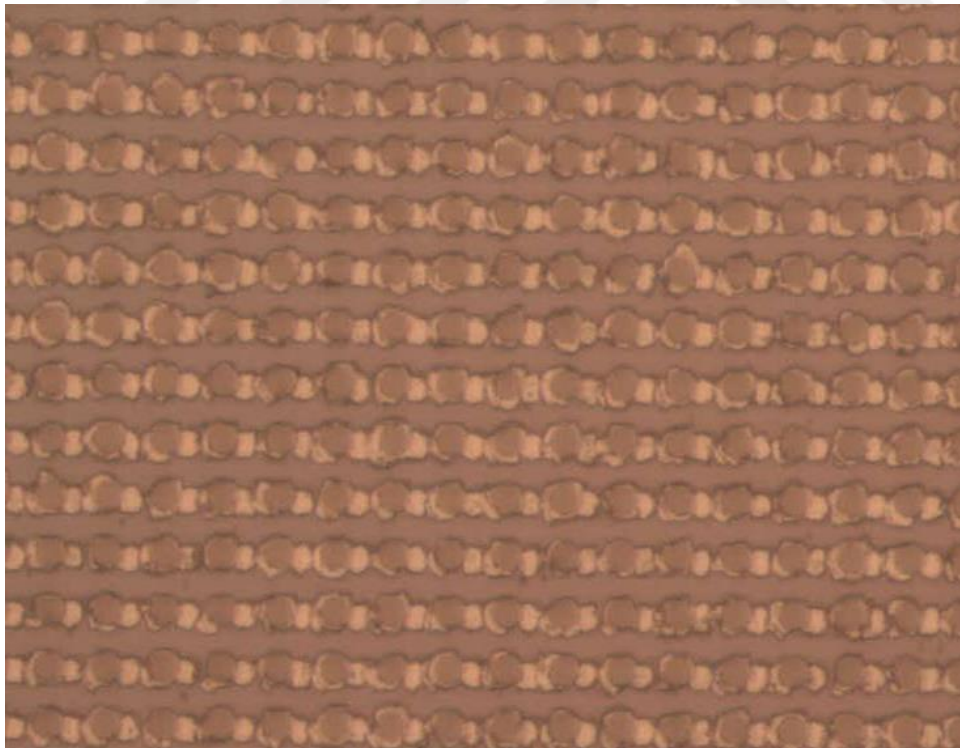


Figure 4.16. Sapphire to sapphire FCB with gliding problem in one direction



Figure 4.17. Image taken by a detector with FCB problems at two corners

4.3. Final Products

We have minimized the risks related to each production step as detailed in this and previous chapters. At the end, we achieve to obtain very high-quality detectors with extremely low minor defects. Less than %0.02 dead pixel ratios are measured. Figure 4.18 shows one of our SWIR images comparisons with visible image taken at the same time. As expected, SWIR image can see through city haze. Other inside and outside sample images taken by different detectors are given in Figure 4.19 and Figure 4.20. Figure 4.21 shows the dead pixel map of a detector with only 184 dead pixels. As a completion to the state-of-the-art detector performance, our final products yield record operability values.



Figure 4.18. Seeing through city haze. Our SWIR image (Top) and visible image



Figure 4.19. Sample images taken by our detectors

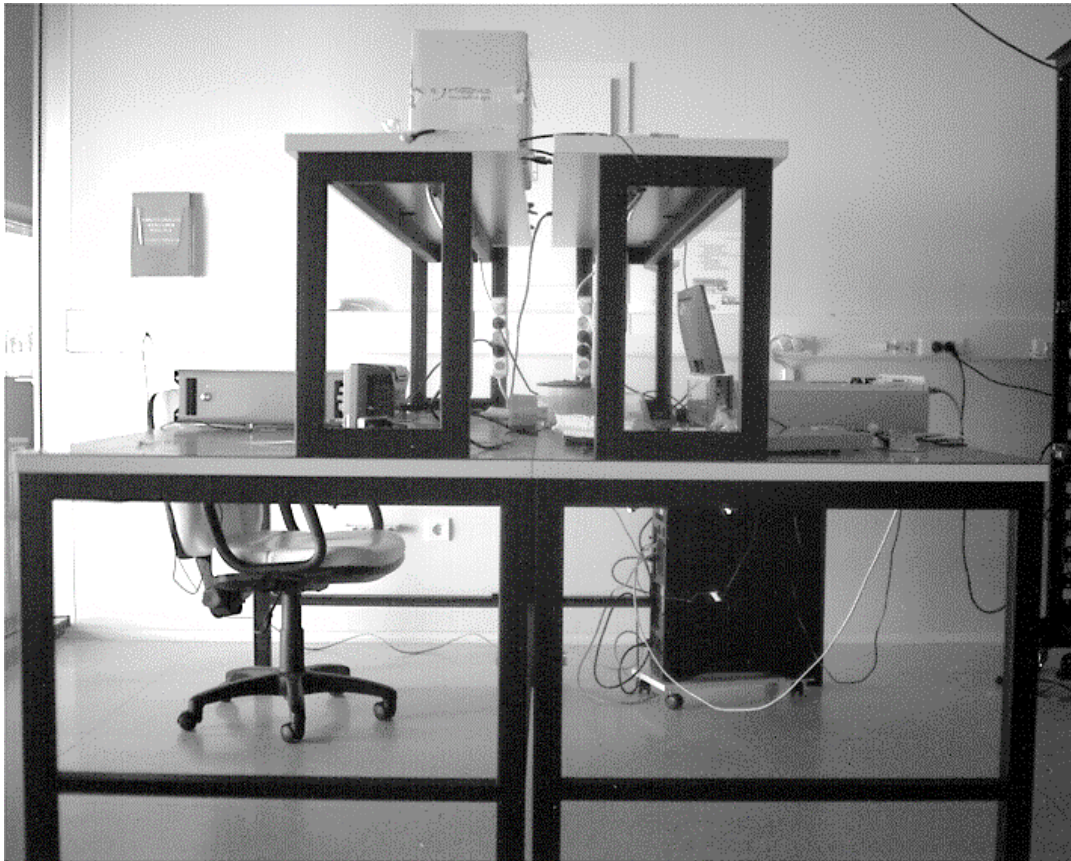


Figure 4.20. Sample images taken by our detectors

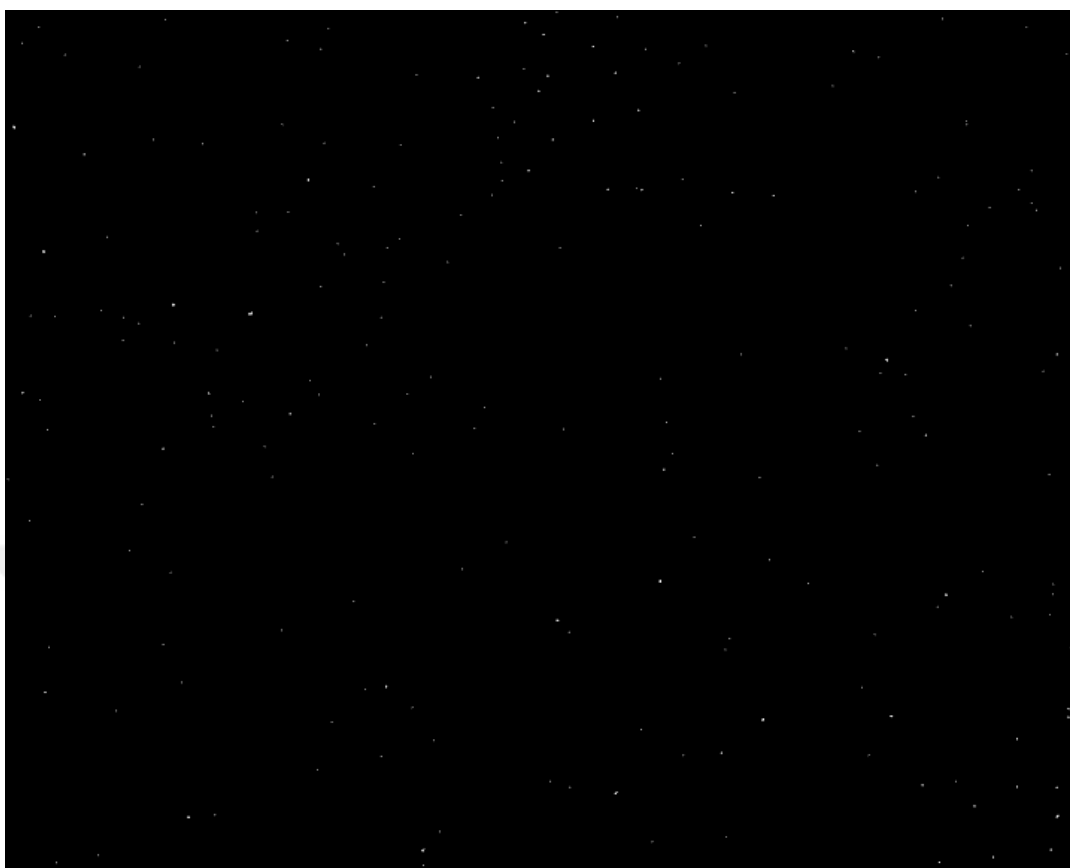


Figure 4.21. Dead pixel map of a detector with record level operability

CHAPTER 5

CONCLUSION AND FUTURE WORKS

InGaAs based SWIR pin heterojunction photodiodes has proven their importance with large number of critical applications from industry to military. High performance InGaAs SWIR detectors are possible with planar type processing while mesa type processing is still crucial for some specific applications as dual band, dual color or hyperspectral imaging applications. In the scope of this thesis work, we created novel approaches that are provides higher performance devices for both planar and mesa type InGaAs SWIR detectors.

Our approach for mesa type detectors consists of design, production and characterization studies of detectors with in-device passivation provided by a p type doped thin and fully depleted InP layer. We processed two types of mesa structured test detectors together on same crystal material with and without etching the depleted p-InP passivation layer. Considering the I-V characterization results, fully depleted p-InP layer decreases the dark current by suppressing surface dark current component while increases photo current by increasing carrier collection efficiency in the area between pixels. With further optimization of doping levels as well as thickness of depleted p-InP layer, we believe that this design could significantly suppress surface dark current component, the dominating component in mesa structured detectors.

In planar type detectors side, as well as designing a novel epilayer structure, we worked on junction placement conditions for planar type InGaAs based photodiodes around an InGaAs absorber and InP cap layer interface. We found that the best device performance is possible when the depletion region end in the n side penetrates into the absorbing InGaAs layer. We optimized the doping and processing conditions for this case to suppress GR dark current component created in depleted InGaAs material

that is a dominating factor in the standard structure. We found that $5 \times 10^{16} \text{cm}^{-3}$ levels n type doping of an absorber InGaAs layer suppresses GR current around 100 times with an acceptable 10% QE tradeoff. After production and characterization phases, we obtained 12fA diffusion limited pixel dark current at 100 mV reverse bias with 86% QE at room temperature, which is, to our knowledge, one of the best room temperature performances measured directly from detector pixels.

Developed state-of-the-art planar 1280x1024 format detectors are employed in post processing studies with FCB, underfill injection, grinding and anti-reflection coating steps. Problem associated with each step is solved and at the end, a record level operability is reached. With the help of our electronics group we assemble the whole camera system and corresponding SWIR images are given.

Our future works for mesa and planar type developed detectors are continuing without a break. For planar type detectors, we are preparing to increase our detector alternatives with different formats. Also packaging studies are developing with the help of our electronics and mechanics team. For mesa type studies, we are developing FPA level characterizations and we are focused on decreasing the possible crosstalk between FPA pixels.

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FOREIGN LANGUAGES

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PUBLICATIONS

1. M. H. Dolas and S. Kocaman, "Fully Depleted InP Nano-Layer for In-Device Passivation of InGaAs SWIR Detectors," *IEEE Electron Device Lett.*, 2017, doi: 10.1109/LED.2017.2763616.
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