

DEVELOPMENT OF A SINGLE-CHIP VISIBLE LIGHT COMMUNICATION RECEIVER

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DEVELOPMENT OF A SINGLE-CHIP VISIBLE LIGHT COMMUNICATION RECEIVER

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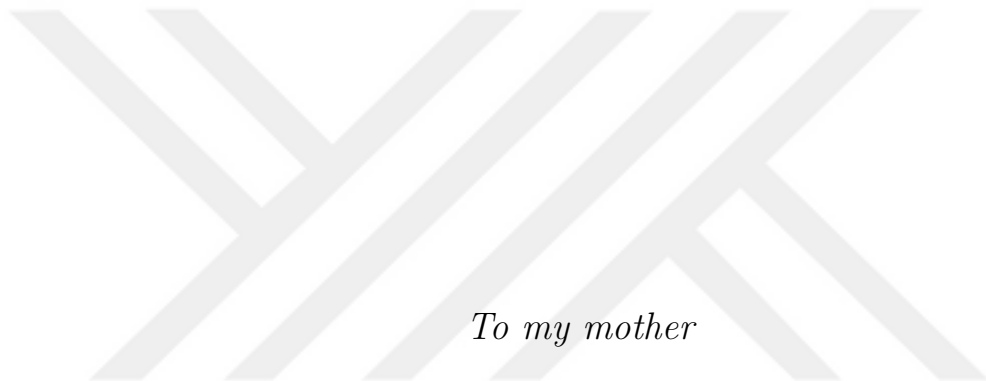
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To my mother

ABSTRACT

The Visible Light Communication (VLC) has drawn the attention in the last decade, which is simply based on the data transmission over the visible light (400nm-700nm). It is considered as an alternative to Radio Frequency (RF)-based technologies and offers unlicensed frequency spectrum to the users. Despite the widely available optical bandwidth, LEDs that are used as a light source in VLC impose a limitation in data rate due to their limited bandwidth, which changes between a few hundred kHz and a few MHz. At this point, the equalization is one the most used method to achieve higher data rates in VLC system. There have been a growing works focusing on the equalization performed for VLC system. However, most of them offer an improvement in data rate at the discrete element level. They are not integrated and consume higher power. The works, which offer a solution at the chip level, are limited. Additionally, a monolithic optoelectronic receiver that can be operated with LEDs with different bandwidths and perform the equalization for the employed LED has been not investigated recently. This work is concentrated on the design and implementation of a monolithic optoelectronic receiver that includes a photodiode with the area of $300\text{ }\mu\text{m}\times 300\text{ }\mu\text{m}$, a Transimpedance Amplifier (TIA), an adjustable equalizer controlled by a switching mechanism, and an output buffer. The designed optoelectronic receiver is implemented in 130 nm Complementary Metal-oxide Semiconductor (CMOS) technology and tested in an experimental setup. It is employed with three different phosphorescent white LEDs and for each of the employed LEDs around 20 times improvement in data rate to their bandwidth is achieved at a distance of 2 meters. The implemented chip has an area of 0.6 mm^2 and consumes around 2.05 mW.

ÖZETÇE

Görünür ışık haberleşmesi son on yılda dikkat çekmekte olup, basit bir şekilde görünür ışık üzerinden (400nm-700nm) veri aktarımına dayanmaktadır. Radyo frekansı temelli teknolojilere alternatif olarak görülmekte olup, kullanıcılara sınırsız bir frekans spektrumu sağlamaktadır. Geniş ölçüde mevcut bir bantgenişliği olmasına karşın, görünür ışık haberleşmesinde ışık kaynağı olarak kullanılan ışık yayan diyotlar, birkaç yüz kHz ile birkaç MHz arasında değişen sınırlı bantgenişliklerinden ötürü veri aktarımına sınırlama getirmektedirler. Bu noktada, denkleştirme görünür ışık haberleşmesinde daha yüksek hızları gerçekleştirmek için olan en çok kullanılan yöntemlerinden biridir. Görünür ışık haberleşmesi için gerçekleştirilen denkleştirmelere odaklanan çalışmalar sayıca artmaktadır. Ancak, bu çalışmaların birçoğu veri hızındaki artırımını ayırık eleman seviyesinde sunmaktadır. Bunlar tümleşik olmamakta ve daha yüksek güç tüketmektedir. Kırmık seviyesinde çözüm sunan çalışmalar sınırlı sayıda olup buna ilaveten farklı bantgenişliklerine sahip ışık yayan diyotlarla birlikte çalışabilen ve denkleştirmeyi kullanan ışık yayan diyot için gerçekleştiren monolitik optoelektronik alıcı şu ana kadar incelenmemiştir. Bu çalışma, $300\ \mu\text{m} \times 300\ \mu\text{m}$ alanına sahip bir fotodiyot, transempedans yükseltici, anahtarlama mekanizması ile kontrol edilen ayarlanabilir denkleştirici, ve çıkış tamponu içeren bir monolitik optoelektronik alıcının tasarım ve gerçekleştirmesine odaklanmaktadır. Tasarlanan optoelektronik alıcı 130 nm CMOS teknolojisinde gerçekleştirilmiş ve deneysel düzende test edilmiştir. Üç adet farklı fosforlu beyaz ışık yayan diyot kullanılmış ve 2 metre mesafede her bir kullanılan ışık yayan diyot için veri aktarımında bantgenişliğine oranla yaklaşık 20 kat iyileştirme başarılmıştır. Gerçekleştirilen kırmık $0.6\ \text{mm}^2$ alana sahip olmakta ve 2.05 mW güç harcamaktadır.

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During the Ph.D. journey, I have met many undesirable and unexpected circumstances. First, the software program, which I have been using for around one year, was crashed and licensed out. Then, the software program had to be changed. After around a month while using the new software, the host computer, which has software licenses for the users, was burned. After it was repaired, it needed to be rehosted, where Covid-19 also started to appear and took around three months to be fixed. I will always remember the period in which only a couple of people were present on the campus due to the pandemic situation while I was working in the laboratory to complete the design regardless of nights and weekends. All of these have taught me to overcome every obstacle. On this journey, there are those whom I would like to thank.

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ACRONYMS

BER	Bit Error Rate
CMOS	Complementary Metal-oxide Semiconductor
CTLE	Continuous-Time Linear Equalizer
ESD	Electrostatic Discharge
HCUR	High Current
HPOT	High Potential
LD	Laser Diode
LED	Light Emitting Diode
LoS	Line of Sight
LCUR	Low Current
LPOT	Low Potential
MIMO	Multiple-Input Multiple-Output
OFDM	Orthogonal Frequency Division Multiplexing
OOK	On-off Keying
PCB	Printed Circuit Board
RGB	Red-Green-Blue
RF	Radio Frequency
SNR	Signal-to-Noise Ratio
TIA	Transimpedance Amplifier
UMC	United Microelectronics Corporation
VLC	Visible Light Communication

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CHAPTER I

INTRODUCTION

During the last decade, there is an exponential growth in mobile devices and wireless services, which resulted in huge demand for RF-based technologies [1–3] and crowding in the RF spectrum [4]. At this point, VLC, also known as LiFi, has become a popular technology and it is seen as a potentially disruptive form of wireless communication [5, 6]. VLC uses a visible light spectrum between 380–780 nm, which provides a huge optical bandwidth [7, 8]. This spectrum is not regulated and hardware readily available [9]. Additionally, the utilized spectrum in VLC is also safe for human eyes since the blinking reflex prevents long exposure [10].

VLC is based on the principle of modulating the light intensity of a light-emitting diode (LED) [11, 12], which is used with the aim of both illumination and communication [13]. In VLC, the information-carrying signal (data) is transmitted through the LED, and it is received by the photodiode.

The use of the VLC systems provides several advantages over conventional RF systems. First, VLC is more secure because light cannot penetrate through the wall [14] and therefore exhibits better performance against eavesdropping [15]. Second, by using light, VLC systems require less power compared to RF systems [9, 16]. Third, the front-end components of both transmitter and receivers are relatively simple and cheap for the VLC system [5].

On the other hand, the main limitation for high data-rate transmission in VLC results from the limited electrical (modulation) bandwidth of the LED [17, 18]. This limitation can be alleviated by using sophisticated transmission techniques such as equalization or multi-carrier communication [19].

1.1 Physics of LED

Solid-state lighting is a rapidly developing area, both in terms of commercial exploitation and academic and industrial research [20]. Recent advances in solid-state lighting provide the development of LEDs. In comparison to traditional light sources such as incandescent bulbs, LED is advantageous in terms of long life expectancy, high tolerance to humidity, low power consumption, and reduced heat dissipation [21–25]. In VLC systems, LEDs are considered as the main light source. The physics of an LED is simply based on the p-n junction, which is formed when p and n-type doped semiconductors are brought together. The p-n junction is shown in Fig. 1.1.

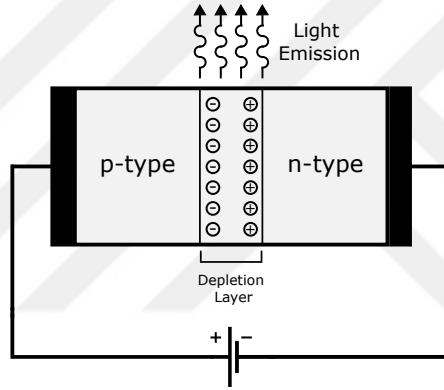


Figure 1.1: p-n junction.

The holes in the p-region diffuse to the n-region, while the electrons in the n-region diffuse to the p-region. The holes and electrons are combined with each other. This results in positively charged acceptor and negatively charged donor atoms. They form the depletion layer, where the internal electric field is directed from positively charged ions to negatively charged ions. This internal electric field sets the barrier for free electrons and holes to flow. When the junction is biased positively, the internal electric field is removed, and therefore the free electrons and holes can combine. With the combination, the light is emitted.

The wavelength of the emitted light is dependent on the band gap energy of the material employed in the p-n junction and the relation is given in Eq. (1.1).

$$E_g = \frac{\hbar c}{\lambda}, \quad (1.1)$$

where E_g , $\hbar$, and λ indicate the band gap energy of the material, Planck's constant, and the wavelength of the emitted light, respectively.

1.2 Literature Review and Motivation

LEDs employed in VLC systems are mostly phosphorescent white LED or Red-Green-Blue (RGB) LED. Their electrical bandwidth varies between a few hundred kHz and a few MHz. There are several techniques to augment the electrical bandwidth comprising blue-filtering, equalization, employing a spectrally efficient modulation scheme, and Multiple-Input Multiple-Output (MIMO)-Orthogonal Frequency Division Multiplexing (OFDM) [26]. In the literature, there have been many works in which different techniques are applied to achieve a higher data rate in the VLC system. Most of the works, reaching a higher data rate for the VLC system, build upon employing equalization and blue-filtering.

Equalization relies on the compensation of frequency response imposed by the LED. This indicates that the limited bandwidth of the LED is extended by the equalization, which can be applied on the transmitter side (pre-equalization), receiver side (post-equalization), and both sides. The equalization can be achieved as analog or digital. In the analog form, discrete elements such as transistors, capacitors, and resistors are used. In the digital form of equalization, digital filters and algorithms are employed.

The blue filter is used in a VLC system to extend the bandwidth of the phosphorescent white LED, which is a phosphor-coated blue LED. Phosphor coating results in creating white light. However, the response of the phosphor (yellow) component is slow due to its relaxation time [27]. To have a faster response, the blue filter is employed since it removes the phosphor component [28]. On the other hand, the received signal is attenuated due to suppressing the phosphor component [29], when the blue filter is used.

Some of the related works [26, 30–55] in the literature, which consider the analog equalization and blue filtering in a VLC system, are presented in Table 1 and it categorizes the works according to the type of the employed LED, the usage of pre- and post equalization, and blue filter.

Table 1: Works for analog equalization

Work	LED Type	Pre-equalization	Post-equalization	Blue filter
[26]	White LED	+	-	-
[30]	White LED	+	-	+
[31]	Red LED	+	-	-
[32]	White LED	+	-	+
[33]	White LED	+	-	+
[34]	Red LED	+	-	-
[35]	White LED	+	-	-
[36]	White LED	+	-	-
[37]	RGB LED	+	-	-
[38]	White LED	+	-	+
[39]	White LED	+	-	+
[40]	RGBY LED	+	-	+
[41]	White LED	+	-	+
[42]	White LED	+	-	+
[43]	White LED	+	-	+
[44]	White LED	+	-	+
[45]	White LED	-	+	+
[46]	White LED	-	+	+
[47]	Red LED	-	+	-
[48]	Blue LED	-	+	-
[49]	White LED	-	+	-
[50]	RGBY LED	-	+	-
[51]	White LED	+	+	-
[52]	White LED	+	+	+
[53]	Red LED	+	+	-
[54]	RGB LED	+	+	-
[55]	White LED	+	+	-

Apart from studies, which focus on analog equalization, an integrated single-chip receiver for a VLC system can be designed and implemented in CMOS technology. At this point, implementing an integrated single-chip receiver would be compact and highly efficient in terms of power consumption. In the literature, there are some studies [56–62], in which the design and implementation of CMOS receiver has been investigated from different perspectives.

In [56], an n-well/p-sub photodiode with the size of $1\text{ mm} \times 1\text{ mm}$ is implemented in a standard CMOS process. The bandwidth of the photodiode is simulated to be around 20 MHz under the reverse bias voltage of 15 V. The photodiode is followed by a commercial TIA (AD8015). To extend the limited bandwidth of the photodiode, two different equalizations with discrete elements are employed. The first and second equalization are based on resistive-capacitive (RC) and resistive-inductive (RL), respectively. As a light source, a red LED at 650 nm with a bandwidth of 70 MHz is used on the transmitter side. Further, an LCR network is applied as pre-equalization for the employed LED. As a result, a Bit Error Rate (BER) of 1.3×10^{-6} at 150 Mbps over 6 m distance is achieved using On-off Keying (OOK) modulation.

In [57,58], a monolithic optoelectronic receiver implemented in $0.35\text{ }\mu\text{m}$ CMOS technology is proposed. The implemented receiver includes an n-well/p-sub photodiode with the size of $100\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$, a TIA with offset cancellation network (OCN), a variable gain amplifier (VGA), an equalization circuit, and an output buffer. The equalization compensates for the frequency response of the photodiode having a cut-off frequency below 40 MHz. Therefore, a red Laser Diode (LD) at 680 nm with high bandwidth of 5 GHz is employed as a light source on the transmitter side. In [57], a BER of 5×10^{-5} at 1.8 Gbps at a distance of 0.46 m is achieved using OOK. In [58], a BER below 10^{-3} at 2.5 Gbps over 12 m is achieved using OOK.

In [59], an avalanche photodiode array with the total size of $200\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$ is implemented in the 180 nm CMOS technology. The photodiode is followed by a TIA, which is discrete. On the receiver side, equalization is not employed. For the transmitter side, μLED array at 450 nm based on the same CMOS technology is fabricated. MIMO technique is used for data transmission. A BER of 2×10^{-3} at around 1 Gbps (aggregated data rate) is achieved at a distance of 1 m.

In [60], a monolithic optoelectronic receiver implemented in $0.18\text{ }\mu\text{m}$ CMOS technology is proposed. The fabricated receiver consists of a p+/n-well-based

avalanche photodiode with the size of $150\ \mu\text{m} \times 150\ \mu\text{m}$, a TIA, an equalizer, a limiting amplifier, a DC-offset canceller, and output buffer. Here, the equalizer compensates for the bandwidth of the photodiode. On the transmitter side, the LD with a bandwidth of 420 MHz is used as a light source. As a result, the sinusoidal waveform of 420 MHz is received from the output of the receiver chip at a distance of 0.5 m.

In [61], μLED based photodiode arrays with diameters of $40\ \mu\text{m}$, $60\ \mu\text{m}$, and $80\ \mu\text{m}$ are fabricated using GaN technology. The photodiode arrays are followed by a commercial TIA (Femto DHPA-100) and the equalization is not employed on the receiver side. For the data transmission, 2×2 MIMO is employed, and therefore two violet LDs with 405 nm are used as a light source. Using the photodiode array with a diameter of $40\ \mu\text{m}$, a BER of below 3.8×10^{-3} at a data rate of 350 Mbps (aggregated data) is achieved at a distance of about 1 m.

In [62], a VLC single-chip receiver is implemented in $0.18\ \mu\text{m}$ CMOS process. The proposed receiver includes a TIA, DC-offset cancellation amplifier, an equalizer, and an output buffer. The used photodiode is commercial and is externally connected to the input of the receiver chip. As a light source, a 4×5 LED array consisting of phosphorescent white LEDs having a bandwidth of 2.2 MHz is used. The designed equalizer compensates for the frequency response of the LED and the zero frequency of the equalizer, corresponding to the electrical bandwidth of the LED, is changed over the transistor's capacitance, which is not linear with an applied control voltage. A BER of 10^{-2} at a data rate of 30 Mbps is achieved at a distance of 2.7 m.

Considering the studies [56–62] that are related to CMOS integrated receiver design, a monolithic optoelectronic receiver achieving the equalization for LEDs with limited bandwidth has been not implemented so far, which shows that there is a lack of study concentrated on this field of application. In the related studies, either the equalization is performed for the photodiode and the LD with a high bandwidth is used as a light source or the designed receiver is not fully-integrated

at the chip level. Embedding a photodiode into the chip, receiving the light emitted by an LED and performing the equalization, is challenging, since on-chip photodiodes have generally much lower active area than the commercial photodiodes and the emitted light by the LED is not as powerful as lasers, making difficult to process the received light further by the following electronic blocks. By this motivation, this work aims to cover this gap in the literature and it deals with the design and characterization of a monolithic optoelectronic receiver, implemented in 130 nm CMOS technology, that can be adapted with LEDs of different bandwidths to achieve a high-speed VLC system.

1.3 Contributions

In the first part of the thesis, we perform the electrical characterization and bandwidth measurement of different commercially available LEDs. We derive the transfer function using LED's equivalent circuit to model the LED's frequency response. Further, we compare the results between the model and the measurement, where the compliance is achieved. In addition, we propose a new LED response model with one zero and two poles for the phosphorescent white LEDs and design an efficient digital equalizer in line with the proposed model. Last, we apply our digital equalizer in an experimental VLC setup, where higher data rates are achieved.

In the second part of the thesis, we propose a monolithic optoelectronic receiver and explain the sub-blocks in detail. First, we analyze the junction capacitance of CMOS photodiode for different structures and design an n-well/p-sub based active and dummy CMOS photodiode with an area of $300\ \mu\text{m} \times 300\ \mu\text{m}$. Second, we design electronic subblocks such as TIA, Continuous-Time Linear Equalizer (CTLE), output buffer, Electrostatic Discharge (ESD) diodes, and CLAMP diodes, where we provide different simulation results. Last, we describe the packaging and design test Printed Circuit Board (PCB) for the proposed receiver.

In the third part of the thesis, we characterize the implemented chip and perform the measurements on an experimental setup. We employ three different

phosphorescent white LEDs with our chip. Moreover, we achieve the data transmission for each of the employed LEDs. Related to the data transmission, we obtain the eye diagrams and measure BER performance. Finally, we characterize the designed CMOS photodiodes.

Some parts of this research have been published as listed below.

Journal Articles

- 1- R. Kisacik**, M.Y. Yagan, M. Uysal, A.E. Pusane, T. Baykas, G. Dundar, A.D. Yalcinkaya, "A 130 nm CMOS Receiver for Visible Light Communication", in IEEE/OSA Journal of Lightwave Technology, 2022, doi:10.1109/JLT.2022.3150250
- 2- R. Kisacik**, M.Y. Yagan, M. Uysal, A.E. Pusane, A.D. Yalcinkaya, "A New LED Response Model and its Application to Pre-Equalization in VLC Systems", in IEEE Photonics Technology Letters 33 (17), 955-958, 2021
- 3- R. Kisacik**, A.D. Yalcinkaya, A.E. Pusane, T. Baykas, M. Uysal, "Characterization of LEDs for visible-light communications", in SPIE Optical Engineering vol. 60, no. 2, 024102, 2021

Conference Papers

- 1-** M.Y. Yagan, **R. Kisacik**, T. Erkinaci, A.E. Pusane, M. Uysal, T. Baykas, G. Dundar, A.D. Yalcinkaya, "Experimental validation of a novel RLL code for visible light communication", 43rd International Conference on Telecommunications and Signal Processing (TSP). IEEE, 2020.
- 2- R. Kisacik**, T. Erkinaci, M.Y. Yagan, A.E. Pusane, M. Uysal, T. Baykas, G. Dundar, A.D. Yalcinkaya, "Opto-electronic receiver system with post-equalization for visible light" communications", 28th Signal Processing and Communications Applications Conference (SIU). IEEE, 2020.
- 3- R. Kisacik**, B.C. Efe, A.E. Pusane, M. Uysal, T. Baykas, G. Dundar, A.D. Yalcinkaya, "Distance and power based experimental verification of channel model in visible light communication", 27th Signal Processing and Communications Applications Conference (SIU). IEEE, 2019.

1.4 Organization

The dissertation is organized as follows: Chapter 2 focuses on the bandwidth measurement of LED and a proposed LED model for phosphorescent white LEDs together with the design of a digital equalizer considering the proposed LED model. Chapter 3 focuses on the design of a monolithic optoelectronic receiver implemented in 130 nm CMOS technology. Chapter 4 presents the measurement results achieved for the implemented receiver.



CHAPTER II

CHARACTERIZATION OF LEDS FOR VISIBLE LIGHT COMMUNICATION

The equivalent circuit of the LED is proposed, and the transfer function is derived based on it. Further, commercially available LEDs are electrically characterized and their bandwidth measurement is achieved. Last, a new LED model for the phosphorescent white LEDs is proposed and a digital equalizer considering the proposed LED model is implemented for a high-speed VLC system.

2.1 Equivalent circuit of an LED

The small-signal equivalent circuit model is presented in Fig. 2.1. V_{in} is the applied voltage to the input. R_i is the source resistance through which a current of I_D flows. The small-signal equivalent circuit (i.e., gray shaded area) includes a series resistance (r_s), a dynamic resistance (r_d), a junction (depletion) capacitance (C_j), and a diffusion capacitance (C_d).

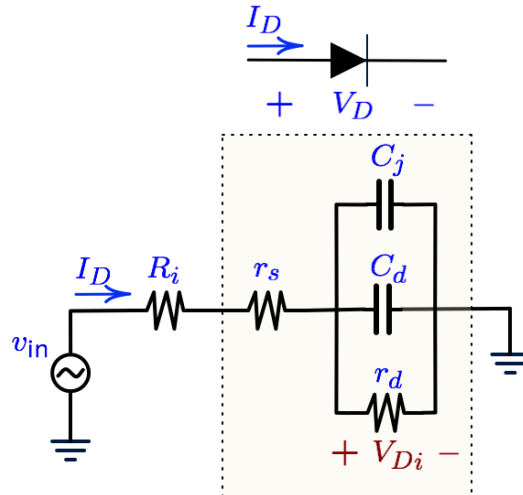


Figure 2.1: Small-signal equivalent circuit of an LED.

The series resistance symbolizes all parasitic Ohmic voltage drops associated with the drive of LEDs. Dynamic resistance models the conduction behavior of

the device around an operating point defined by the direct current bias. Fig. 2.2 delineates the current change of an LED versus applied bias voltage.

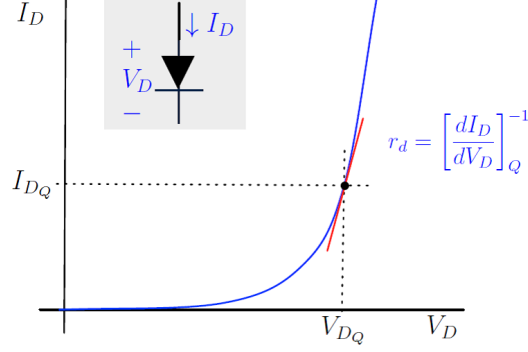


Figure 2.2: Small signal dynamic resistance of an LED around an operating point.

The dynamic resistance refers to the slope of the curve at a bias point and it can be approximated as

$$r_d = \frac{dI_D}{dV_D} = \frac{nV_T}{I_{DQ}}, \quad (2.1)$$

where n , V_T , and I_{DQ} represent ideality factor, thermal voltage, and the current at a bias point, respectively.

When the LED is forward-biased, the junction capacitance and the diffusion capacitance appear. However, the junction capacitance is negligible compared to the diffusion capacitance, which is associated with the minority carrier storage. As the forward-bias voltage is increased, the diffusion capacitance increases due to the carrier injection. The diffusion capacitance is given as

$$C_d = \frac{\tau}{r_d} \quad (2.2)$$

where τ is the carrier lifetime. The transfer function of a LED describes the change in output voltage (V_D) with respect to the input voltage (V_{in}). According to the equivalent circuit model presented in Fig. 2.1, the transfer function of the LED is derived as

$$H_{\text{LED}}(s) = \frac{V_D(s)}{V_{\text{in}}(s)} = K \frac{s + \frac{(r_d+r_s)}{(C_j+C_d)r_d r_s}}{s + \frac{(R_i+r_d+r_s)}{(C_j+C_d)(R_i+r_s)r_d}} \quad (2.3)$$

where K (<1) is dc attenuation, $\frac{(r_d+r_s)}{(C_j+C_d)r_d r_s}$ is the zero, and $\frac{(R_i+r_d+r_s)}{(C_j+C_d)(R_i+r_s)r_d}$ is the pole frequency of the transfer function. The 3-dB bandwidth¹ of the LED corresponds to the frequency where the transfer function drops to 0.707 of its maximum based on Eq. (2.3).

2.2 Characterization and Bandwidth Measurement of LEDs

The electrical characteristic of different commercial LEDs is first investigated. Then, the 3-dB bandwidth of the LEDs is measured.

For electrical characterization, using the Keithley 4200-SCS Semiconductor Characterization System [63] the I-V characteristics of the LEDs are obtained. While electrical characterization, the applied voltage is swept from slight reverse bias to deep forward bias, and the flowing current is monitored by a power source measure unit (SMU) with compliance of 100 mA. To derive the size-independent J-V characteristics, active emitter areas of each sample LEDs are measured. Subsequently, the bias voltages (V_{on}), at which all LEDs are in the safe forward conduction region for the same current density (10^{-3} A/cm^2), are extracted. Moreover, the ideality factor (n) is derived by fitting the measured characteristics to

$$J_D = J_S(e^{\frac{V_D}{nV_T}} - 1), \quad (2.4)$$

where J_D , J_S , and V_D represent the diode current density, the scale current density, and the applied voltage.

The measured J-V characteristics of LED-1, LED-6, LED-8, and LED-9, are presented in Fig. 2.3 as an example by comparing with the analytical model in (2.4). As can be seen in Fig. 2.3, the measurement results are consistent with (2.4) in the active region. As a result of this observation, the ideality factor values of

¹The 3-dB bandwidth is the same as cut-off frequency, electrical bandwidth, and modulation bandwidth. They are used in the literature interchangeably.

different LEDs in the active region can be extracted.

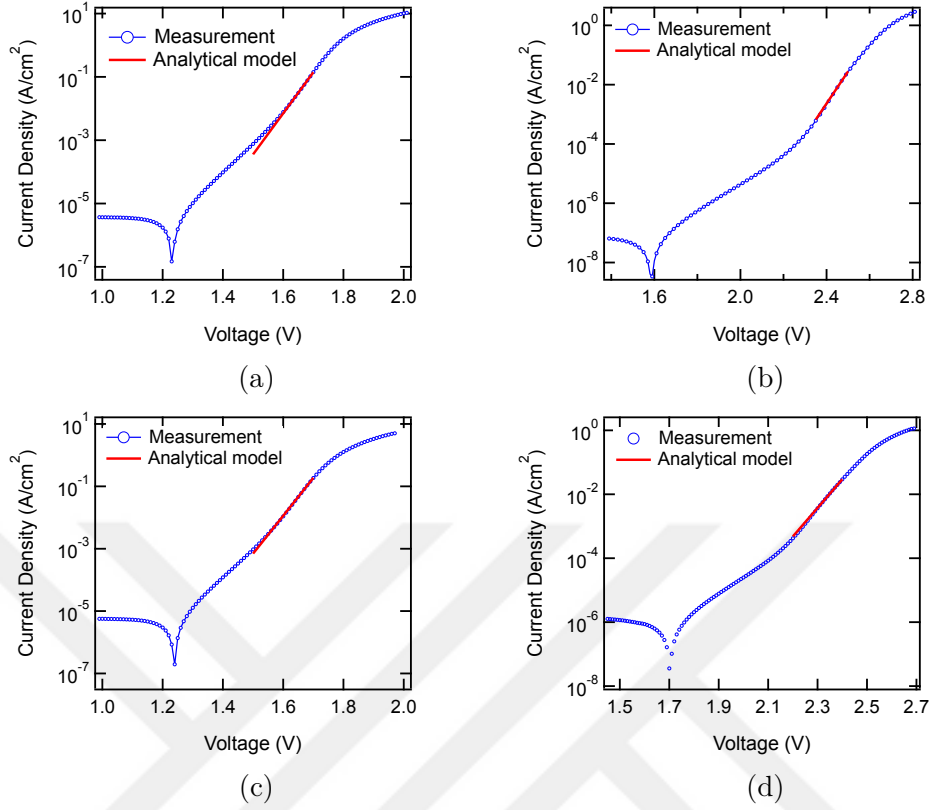


Figure 2.3: Current density versus voltage graph of (a) LED-1 (Red), (b) LED-6, (c) LED-8, and (d) LED-9.

The commercially available LEDs, which are characterized and measured, are categorized in terms of manufacturer, part name, the color of emitted light, V_{on} voltage, ideality factor, electrical bandwidth, and spectral window. All related parameters are presented in Table 2.

Table 2: The on-potentials (V_{on}), the ideality factors (n), the 3-dB bandwidth values and

Led Nr.	Manufacturer	Partname	Color	V_{on} (V)	n	BW (MHz)	Spectral Window FWHM ¹ (nm)
LED-1	BROADCOM	ASMT-MT00-00001	Red	1.51	1.28	3	627-643
			Green	2.01	2	1.2	502-536
			Blue	2.26	1.88	0.75	442-466
LED-2	CREE	XREWHT-L1-0000-00D01	Cool White	2.27	1.72	1.2	442-466
LED-3	CREE	XPEHEW-H1-0000-00AE8	Warm White	2.27	1.9	0.25	443-457
LED-4	CREE	CLMVB-FKA- CFHEHLCBB7A363	Red	1.46	1.55	20	607-631
LED-5	CREE	XMLC7TW-A0-0000 00C2AAAAB1	Neutral White	2.27	1.6	0.35	434-456
LED-6	LUMILEDS	L1T2-30803000000000	Warm White	2.37	1.55	0.125	441-467
LED-7	LUMILEDS	LXML-PWC2	Cool White	2.33	1.45	0.8	435-455
LED-8	LUMILEDS	LXM2-PD01-0050	Red	1.5	1.37	1.2	625-645
LED-9	LUMINUS	SST-90-B-F11-KG300	Blue	2.24	1.87	0.375	448-468
LED-10	OSRAM	LE RTDUW S2W	Cool White	2.31	1.73	1	433-453
LED-11	OSRAM	LE UW S2W-PXQX-4P7R	Cool White	2.32	1.89	1.3	433-453
LED-12	OSRAM	LE CWUW S2W-LZMX-CHCL+NXNY-UW	Cool White	2.38	1.63	1.3	433-453
		LE CWUW S2W-LZMX-CHCL+NXNY-UW	Warm White	2.38	1.63	0.2	442-468
LED-13	OSRAM	GF CS8PM1.24	Red	1.47	1.42	2.3	648-672
LED-14	OSRAM	LB CP7P	Blue	2.17	2	2	453-477

¹ FWHM stands for full width at half maximum and it used related to the emission spectrum of the LEDs.

The measurement technique applied to extract the frequency response of the LED is important, since the frequency response of the LED can be given in different characteristics, which contradict the LED's inherent frequency response. For example, in the studies of [30, 50, 64–68], a bias-tee is employed to drive the LED while extracting the frequency response of the LED. Bias-tee combines the DC signal (illumination) and the AC signal (communication). However, its frequency response appears in the system and therefore it is combined with the LED's frequency response, which results in misleading frequency characteristics. Moreover, using an amplifier to receive a higher AC signal could also affect the measured response. Due to the usage of bias-tee, it is presented in [30, 50, 64–67] that the measured frequency response reaches a peak point first and then starts to decrease with the increasing frequency. On the other hand, in [68], an amplifier is employed additionally and the measured frequency response decreases first and then reaches a peak.

While extracting the frequency response of the LEDs, the external components such as bias-tee and amplifier are not employed not to affect the internal LED's frequency response. The LEDs are directly connected to the signal generator (Tektronix AFG1022 [69]), which generates an AC signal superimposed on a DC level. Moreover, on the receiver side, the output of the photodetector (Thorlabs PDA100A2 [70]) is connected to the signal analyzer (Rohde & Schwarz FSV30 [71]). The employed photodetector exhibits a flat frequency response up to 150 MHz, which indicates that the photodetector does not affect the measured frequency response. The aim of using a signal analyzer is to measure the small signal accurately, since the oscilloscope does not provide a sensitive detection for the small signal as the signal analyzer does.

The measured frequency characteristic of the commercial LEDs (presented in Table 2) is shown in Fig. 2.4. As shown in Fig. 2.4, there is a flat response in the low-frequency range and then the magnitude decreases as the frequency increases, which complies with the LED's inherent frequency response.

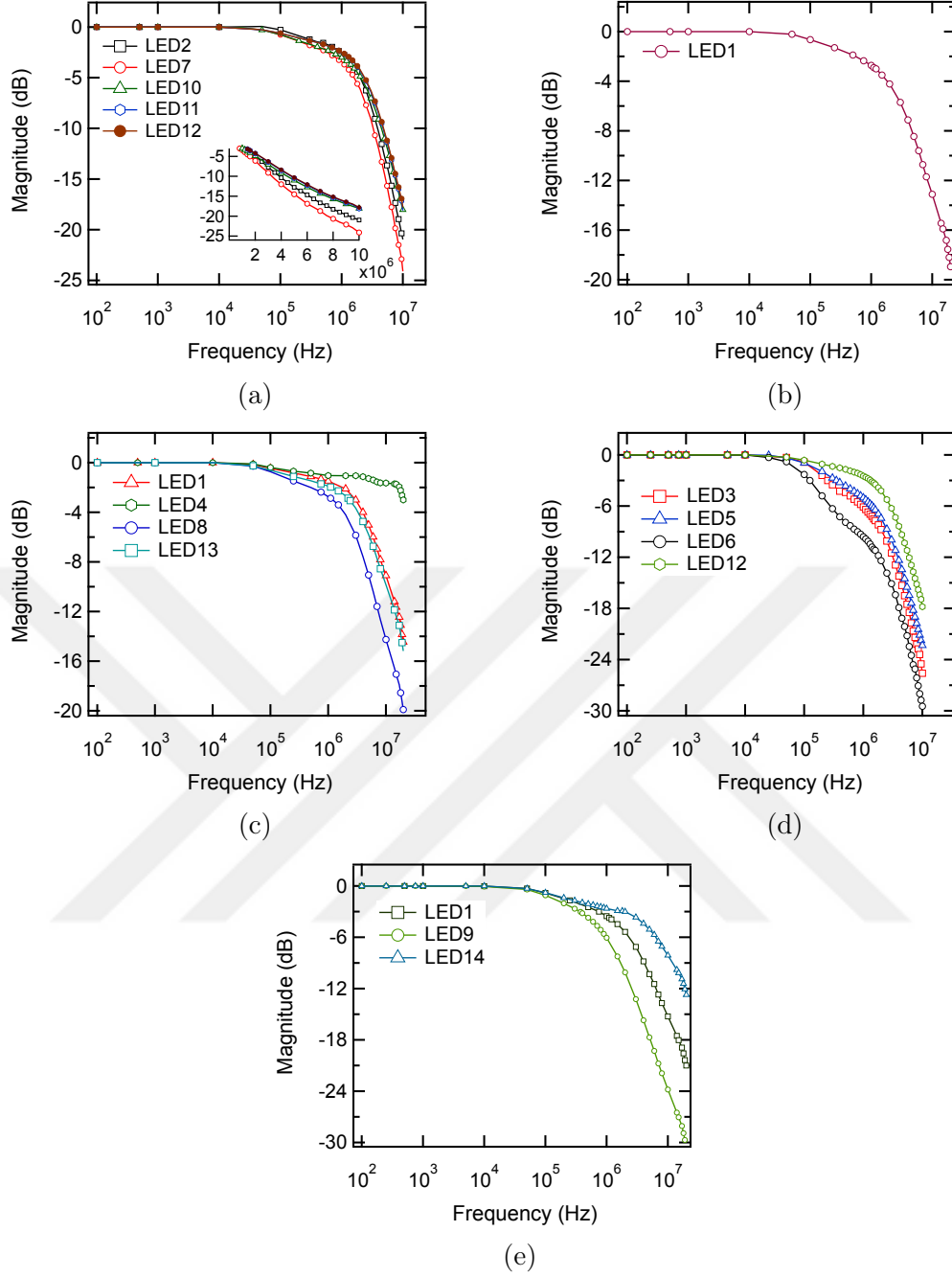


Figure 2.4: Frequency responses of different commercially available LEDs. (a-b) white colored (c) red colored (d) green colored (e) blue colored.

The measured frequency responses are fitted by the derived transfer function in Eq. (2.3) for LED-1 (red), LED-2, LED-11, and LED-13 as examples and they are compared in Fig. 2.5 by giving the fitting parameters. R_i , corresponding to the output resistance of the signal generator, is chosen to be $50 \, \Omega$. The total capacitance, which includes the junction and diffusion capacitance, is denoted as C_T .

As seen in Fig. 2.5, the measured frequency responses and the fitting by the transfer function in (2.3) exhibit a good agreement. The root mean square error between the measurement and fitting is in an acceptable range (0.4-0.8 dB).

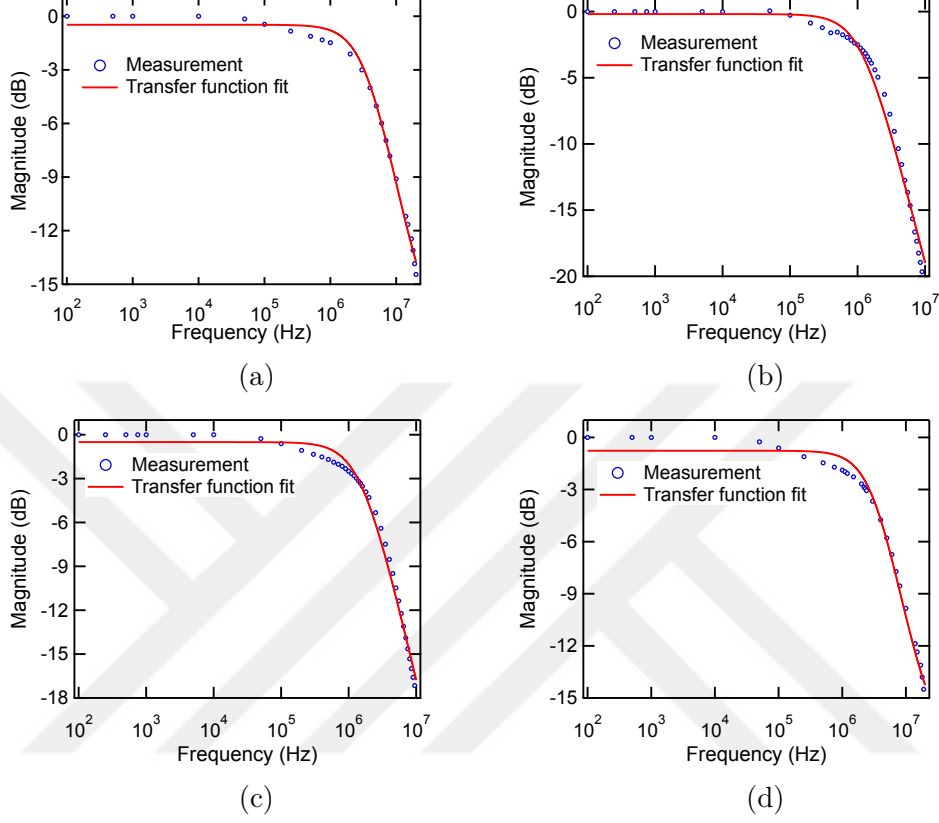


Figure 2.5: Comparison of small signal model of LED with measured modulation characteristic.(a) LED-1 (red) (b) LED-2 (c) LED-11 (d) LED-13; r_s : 0.506, 0.015, 0.138, 0.286 Ohm; r_d : 3.782, 20, 7.946, 1.792 Ohm; C_T : 12.5, 9.6, 15, 28.8 nF; C_j : 0.25, 1.06, 0.048, 0.2 nF K: 0.120, 0.001, 0.018, 0.130

The modulation bandwidth is associated with the chip area and the semiconductor and packaging technology employed for the LED. Looking at Table 2, the highest modulation bandwidth (i.e., 20 MHz) is obtained for LED-4. The modulation bandwidth can be changed by the bias current, which is equivalent to the current injection [72]. Since the carrier lifetime (τ) is shortened by the current injection, the modulation bandwidth is increased. This effect can be observed for the LED with a smaller surface area and higher modulation bandwidth. Thus, the LED-4 is used to observe the modulation bandwidth change over the bias current. The bias current is changed between 10-100 mA and the change in modulation bandwidth over the bias current is illustrated in Fig. 2.6.

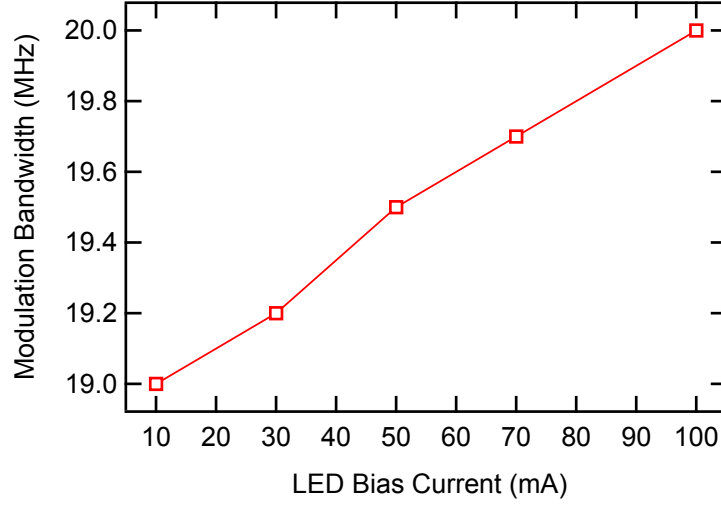


Figure 2.6: Modulation bandwidth change versus bias current.

As can be observed from Fig. 2.6, the modulation bandwidth changes linearly with the bias current (10 kHz/mA) applied to the LED. The change in modulation bandwidth is not considerable. This indicates that more or less the same bandwidth is achieved for the applied bias current. The same data transmission performance can be achieved with lower power consumption. On the other hand, especially for μ LEDs with a modulation bandwidth of a few hundred MHz, the bias current effect can be exploited to have a considerable extension in modulation bandwidth.

2.3 LED response modeling and its Application to Pre-equalization in VLC Systems

There have been some efforts to model the LED's frequency response in closed-form expression in the literature. For instance, in the studies [73–81], the LED's frequency response is modeled by low-pass filter and it is given as

$$H_{\text{LED}}(f) = \frac{1}{1 + j\frac{f}{f_c}}, \quad (2.5)$$

where f_c is the cut-off frequency of the LED. Another used model [82–86] is the Gaussian low-pass filter and it is modeled as

$$H_{\text{LED}}(f) = e^{-\ln(\sqrt{2})\left(\frac{f}{f_c}\right)^2}. \quad (2.6)$$

The models given in Eq. (2.5) and Eq. (2.6) can not match well with the measured frequency response of the LED. Three different phosphorescent white LEDs are considered and their frequency responses are thoroughly measured in a wide-frequency range. Based on these measurements, a new LED frequency response model is proposed with one zero and two poles and it is presented as

$$H_{\text{LED}}(f) = \frac{1 + j\frac{f}{f_{z1}}}{\left(1 + j\frac{f}{f_{p1}}\right)\left(1 + j\frac{f}{f_{p2}}\right)}, \quad (2.7)$$

where f_{z1} is the zero frequency, f_{p1} and f_{p2} are the pole frequencies, respectively.

The measured frequency responses for three different phosphorescent white LEDs (i.e., LED-A [87], LED-B [88], and LED-C [89]) are presented in Fig. 2.7 comparing with Eq. (2.5), Eq. (2.6), and proposed model (2.7), respectively. As can be seen in Fig. 2.7, the Gaussian low-pass filter-based model (2.6) exhibits a great deviation from the measurements, especially after the cut-off frequency. The low-pass filter-based model (2.5) shows a better matching, however, the difference between the model and measurements turns out to be considerable, as the frequency increases. The resulting difference relies on the slope of attenuation,

which is ~ 6 dB/octave in the model (2.5) and ~ 8 dB/octave in measurement. The physical explanation for having a higher slope in the measurement is related to the parasitic network of phosphorescent white LEDs, which brings a higher-order pole and a zero into the system [90]. Therefore, the proposed model (2.7) with one zero and two poles exhibits a well matching with the measurement results in a wide-frequency range.

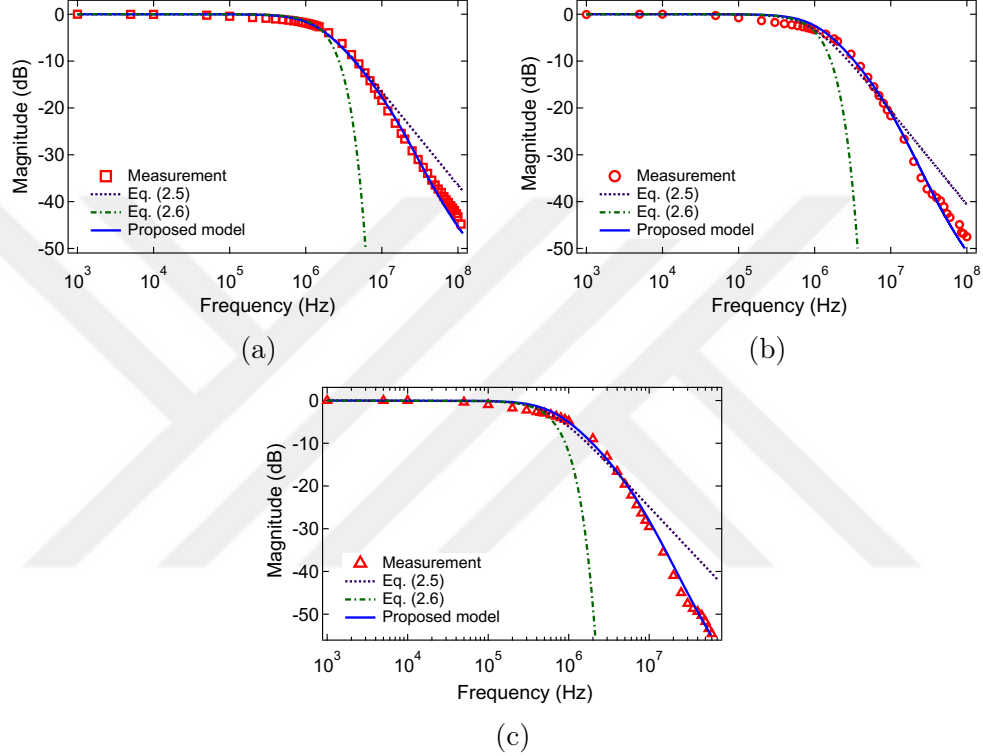


Figure 2.7: Comparison of proposed LED frequency response with measurements a) LED-A, b) LED-B, c) LED-C.

Based on the proposed LED's frequency response model (2.7), a digital pre-equalizer is implemented in Matlab and then applied in a VLC setup. The transfer function of the equalizer is given as

$$H_{\text{PRE}}(f) = \frac{1}{H_{\text{LED}}(f)} = \frac{\left(1 + j\frac{f}{f_{p1}}\right) \left(1 + j\frac{f}{f_{p2}}\right)}{1 + j\frac{f}{f_{z1}}}, \quad (2.8)$$

The equalizer response is the inverse of the proposed LED's frequency model to provide the equalization efficiently. While designing the equalizer, for LED-A, f_{p1} , f_{p2} , and f_{z1} are set to 1.5 MHz, 17 MHz, and 52.6 MHz, respectively. For LED-B,

f_{p1} , f_{p2} , and f_{z1} are set to 1.15 MHz, 11.6 MHz, and 50 MHz, respectively. To achieve the equalization for LED-C, f_{p1} , f_{p2} , and f_{z1} are 680 kHz, 7 MHz, and 70 MHz, respectively. To extract the frequency response of the equalized system, discrete sinusoids at different frequencies are first generated and filtered in line with the equalizer and they are fed to the LED. The frequency response of the equalizer and equalized system are presented for LED-A, LED-B, and LED-C in Fig. 2.8.

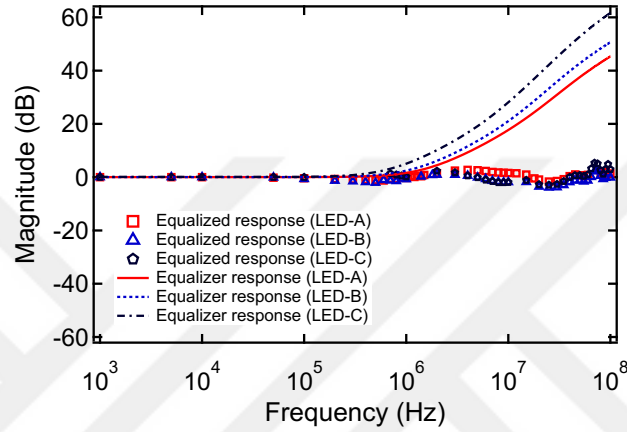


Figure 2.8: Frequency response of the equalizer and equalized system.

In Fig. 2.8, the designed equalizers exhibit gains of around 45 dB, 50 dB, and 62 dB in the frequency range of 100 MHz for LED-A, LED-B, and LED-C, respectively. The resulting gains indicate that the equalizer should reach a higher gain as the LED's pole frequency gets lower. Consequently, the equalized systems exhibit a flat and wide frequency response, where the variation in magnitude is kept within ± 2 dB margin up to 100 MHz.

The VLC setup to achieve the data transmission is presented in Fig. 2.9. LED-A is used as a light source. There are two lenses used in the setup to collimate (Thorlabs LA1608) and focus (Thorlabs LA1131) the light to reach a longer distance between the transmitter and the receiver. The LED and photodiode (Thorlabs PDA10A-EC) are mounted on the optical table and they are aligned using micrometers (Thorlabs PT3A/M). The distance between the LED and the photodiode is 1.5 meters. The signal generator (Tektronix AFG3101) is fed to LED and the arbitrary bit pattern with OOK modulation is generated by ArbExpress

software controlling the signal generator. To monitor the received data, the output of the photodiode is connected to the digital oscilloscope (Rohde & Schwarz RTE1034).

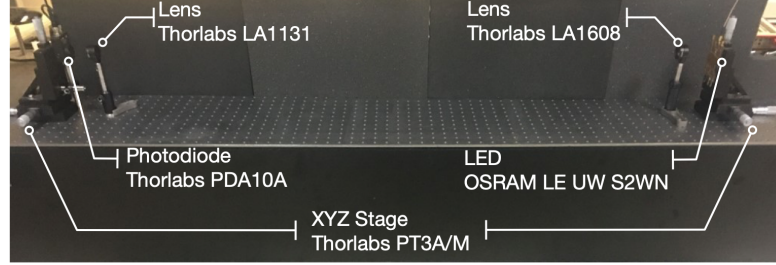


Figure 2.9: Experimental VLC setup.

To observe the effect of the equalizer, eye diagrams of the received data for the case without and with equalization are obtained. The related eye diagrams at different data rates are presented without and with equalization in Figs. 2.10(a-c) and Figs. 2.10(d-f), respectively. Figs. 2.10(a-c) shows that the received data are severely distorted, when the equalization is not applied. Thus, inter symbol interference (ISI) arises from the LED's limited bandwidth and the resulting eye diagram comes out. When the equalization is applied, a clear eye diagram is achieved at a data rate of 100 Mbps, and with increasing the data rate, the eye clearance becomes smaller as seen in Figs. 2.10(e-f).

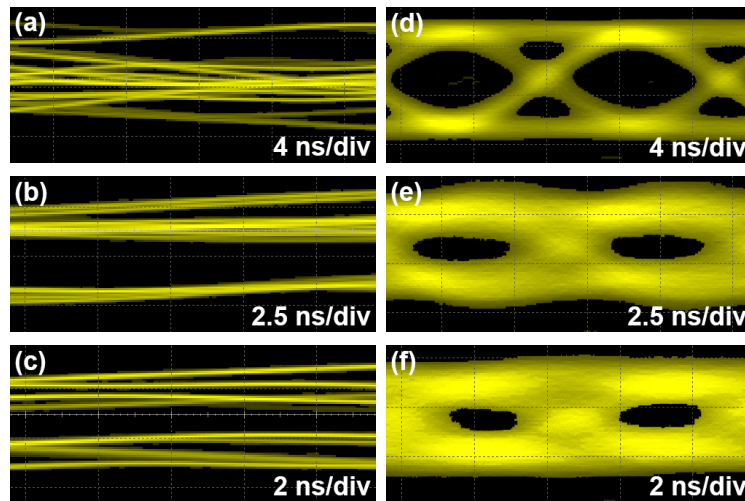


Figure 2.10: Eye diagrams at different data rates w/o and w/equalization (a) 100 Mbps w/o (b) 150 Mbps w/o (c) 200 Mbps w/o (d) 100 Mbps w/ (e) 150 Mbps w/ (f) 200 Mbps w/.

To analyze the BER performance, an arbitrary binary data pattern, consisting of 10^5 bits, is generated. With the employment of the designed equalizer, the received data at different data rates are processed by calculating the bit energy and then a BER is extracted over the data rates. In Fig. 2.11, the BER performance is presented, and compared with equalizers considering the LED model in Eq. (2.5) and the related works [91, 92]. As a result, a BER of 10^{-5} at a data rate of 120 Mbps is achieved at a distance of 1.5 m using the designed equalizer. Furthermore, up to data rates of 180 Mbps, the BER is below the forward error correction limit (3.8×10^{-3}). As seen in Fig. 2.11, the designed equalizer outperforms the compared ones.

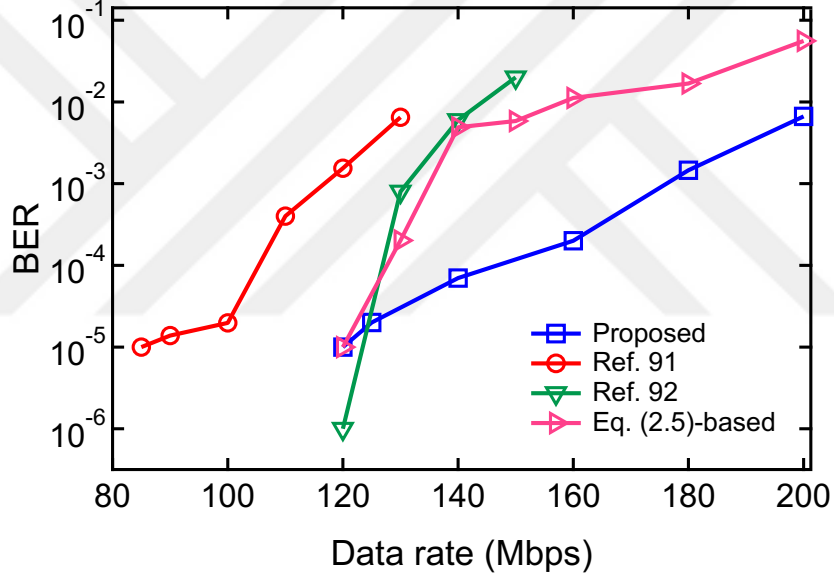


Figure 2.11: BER results versus data rate for performance comparison.

CHAPTER III

CMOS RECEIVER DESIGN FOR VLC

In this chapter, a fully-monolithic¹ optoelectronic receiver implemented in 130 nm CMOS technology is presented and the sub-blocks of the receiver are explained in detail. For sub-blocks, different simulations such as transient, AC, noise, and stability analysis are performed in Cadence Virtuoso. Further, the pre-layout² and post-layout³ simulations are provided.

3.1 Receiver Design Methodology

The receiver to be designed will consider the LEDs as a light source, which is a challenging point in the design, since the light power emitted by the LEDs is much weaker in comparison to lasers. Having the signal with a lower amplitude on the receiver side is associated with the deterioration of the signal-noise ratio. In the worst case, the signal even can not be detected. Moreover, LEDs have a Lambertian radiation pattern, indicating that the light beam propagates with divergence and therefore the alignment needs to be performed to achieve the data transmission for a longer distance. On the other hand, the distance between the employed LED and the designed receiver affects the received power considerably, given the fact that the optical power is attenuated, as the distance increases. Furthermore, the light spot area starts to expand due to higher distance, even the lenses are employed. At this point, the communication channel should be analyzed based on the mentioned effects.

The most used channel scenario in the literature is illustrated in Fig. 3.1. The left side (Source) and the right side (Receiver) in Fig. 3.1 correspond to the LED

¹All sub-blocks are integrated.

²It relies on the schematic design, and the parasitic capacitance is not considered in the simulation, which is before drawing the chip layout.

³It relies on the layout design and the parasitic capacitance is considered in the simulation.

and photodiode, respectively. DC gain ($H(0)$) defines the ratio of the optical power received by the photodiode (P_R) to the transmitted optical power by the LED (P_T) and it takes the Line of Sight (LoS) component into account. It is given as

$$H(0) = \frac{P_R}{P_T} = \frac{m+1}{2\pi d^2} \cos^m(\varphi) A_{PD} \cos(\theta) \text{rect}\left(\frac{\theta}{2\text{FOV}}\right), \quad (3.1)$$

where m and d are Lambertian index and the distance between the LED and the receiver, respectively. φ and θ denote the angle of the irradiance and incidence, respectively. A_{PD} indicates photodiode active area and FOV stands for Field of view.

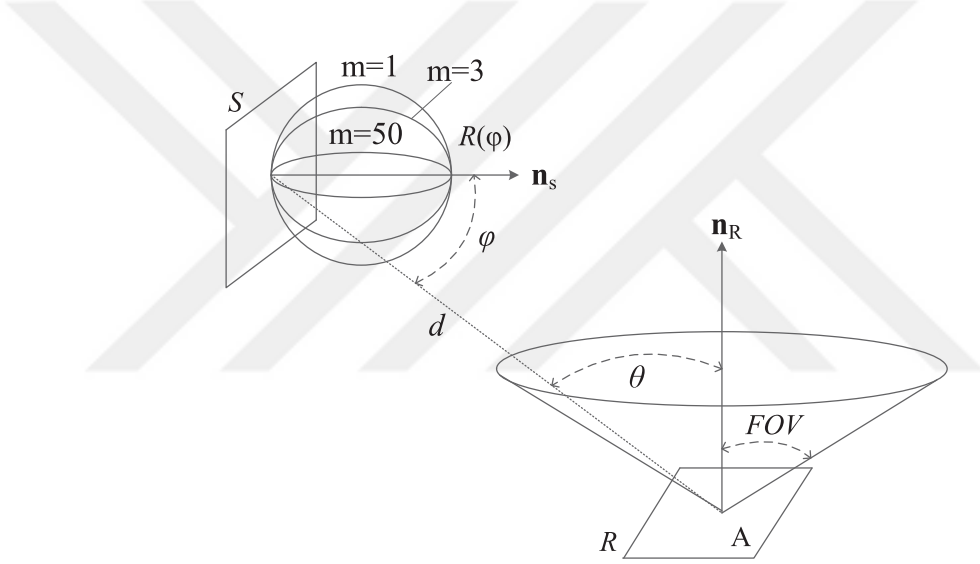


Figure 3.1: A general channel scenario [93].

The considered scenario is point-to-point communication, where (3.1) does not have any angle dependency. Hence, the received signal would be largely dependent on the distance factor. However, (3.1) does not provide any information related to the input current induced by the receiver. The estimation for the input current is required, since it directly affects the active area of the photodiode and TIA design. Therefore, some assumptions should be made based on measurement for the concerning scenario shown in Fig. 3.2. The output voltage (V_{out}) of the receiver can be found as

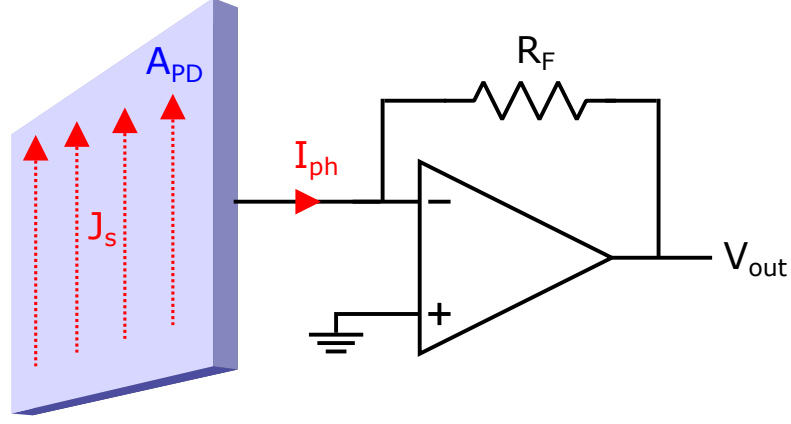


Figure 3.2: The channel scenario for the receiver design.

$$V_{\text{out}} = J_S A_{\text{PD}} G_{\text{TIA}}, \quad (3.2)$$

where J_S and G_{TIA} denote the input current density and the gain of the TIA, respectively. The photocurrent is dependent on the J_S and A_{PD} and it is given as

$$I_{\text{ph}} = J_S A_{\text{PD}} = P_{\text{R}} R_{\text{PD}}, \quad (3.3)$$

where R_{PD} is the responsivity of the photodiode. Based on (3.2) and (3.3), the communication link is modeled as follows: The optical power is converted to the photocurrent by the photodiode's responsivity first and then the photocurrent is transformed to the voltage by the TIA's gain.

The reference measurement to estimate the J_S is performed using a commercial optical receiver, including a photodiode with the active area of 0.8 mm^2 and the TIA with a gain of around $74 \text{ dB}\Omega$. In the measurement, the distance between the LED and the receiver is kept between 1-2 meters and the alignment is achieved using lenses on the transmitter and receiver sides. The amplitude of the AC signal applied to the LED is generally set to $2 V_{\text{pp}}$. Under these conditions, V_{out} is measured as $1 V_{\text{pp}}$. Achieving better alignment using larger lenses may result in higher output voltage, however, this will require additional lenses. For the output voltage of $1 V_{\text{pp}}$, J_S is calculated as $250 \mu\text{A}/\text{mm}^2$, which leads to a photocurrent of $22.5 \mu\text{A}$ for the photodiode area of $300 \mu\text{m} \times 300 \mu\text{m}$. At this point, it should be

noted that the input current is calculated under the assumption that the responsivity of the photodiode employed in the reference measurement is similar to the responsivity of the designed photodiode, whereas CMOS photodiodes have lower responsivity. This difference can be compensated by decreasing the distance or increasing the amplitude of the AC signal applied to the LED while measuring with the chip.

The designed CMOS receiver consists of an active and dummy photodiode, a TIA, a voltage amplifier, a CTLE, and an output buffer. All of these are designed in differential topology. The proposed receiver architecture is shown in Fig. 3.3.

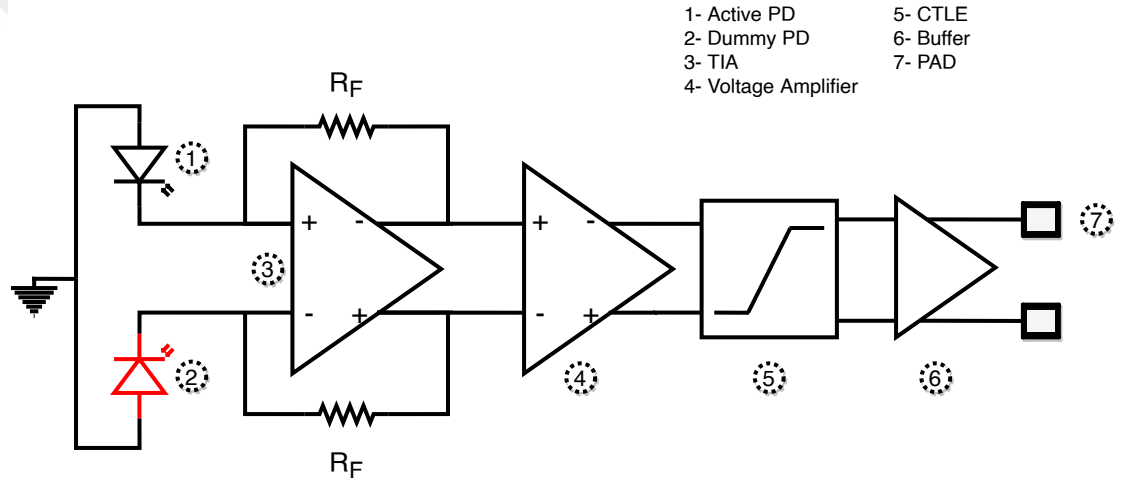


Figure 3.3: Proposed receiver architecture.

In the proposed receiver, the photodiode receives the emitted light by the LED and converts it into an electrical current. Then, the electrical current is transformed to the voltage by the TIA and it is amplified by the voltage amplifier further. The CTLE aims to compensate for the frequency response resulting from the LED by extending the overall bandwidth. Output buffer provides the isolation of the signal from the device equipment to measure. With the employment of the proposed receiver, it is aimed that higher data transmission is achieved using LEDs with different bandwidths.

3.2 Photodiode

The photodiode is a reversely biased p-n junction. In the p-n junction, the depletion region, where the free electrons and holes are not present, is formed. The depletion region acts as a barrier for free electrons and holes in the undepleted region to move. When the photons are absent, only the dark current flows due to the movement of minority carriers, which are free electrons and holes in the p-region and n-region, respectively. When the incident photons with an energy, which is higher than or equal to the band-gap energy of the semiconductor, are present, the photons are absorbed by the junction and therefore the electron-hole pairs are generated. The generated electron and holes are swept away by drift in the depletion region, which indicates that these holes and electrons move towards the p+ and n+ sides, respectively. As a result, the photocurrent is formed and flows in the same direction with dark current.

A reversely-biased photodiode is illustrated in Fig. 3.4. V_a represents the applied voltage in reverse bias. The width of the depletion region (w) changes with applied reverse bias voltage. When the applied voltage is increased in the reverse bias direction, the depletion region becomes wider and a higher photocurrent is obtained. However, having a wider depletion region results in a slow time response, since the capacitance of the depletion region increases.

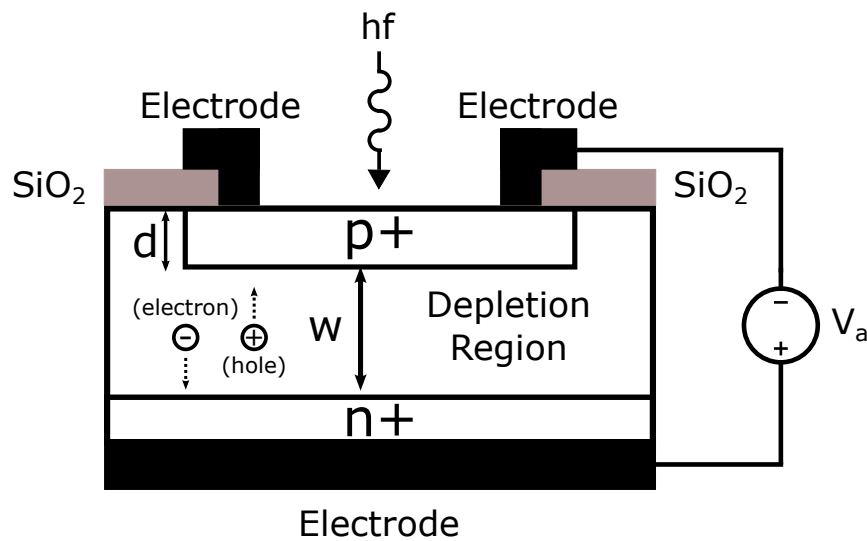


Figure 3.4: Typical construction of a photodiode.

When the light starts to be absorbed, the light intensity decreases exponentially with the penetration depth and absorption coefficient. The relation for change in light intensity is given by Lambert-Beer's Law as

$$\Phi(d) = \Phi_0 e^{-\alpha d}, \quad (3.4)$$

where Φ_0 represents the initial light intensity, α and d are absorption coefficient and penetration depth, respectively. The absorption coefficient (α) determines how far light of a particular wavelength can penetrate into a material before being absorbed.

The absorption coefficient is dependent on the wavelength of the light and the material deployed in the junction. For shorter wavelengths, the absorption coefficient is high. As the wavelength increases, the absorption coefficient becomes lower, since the energy of the light decreases and therefore the light starts to be poorly absorbed. The VLC operates at wavelengths between 400 nm-700 nm. To cover these wavelengths, Si is a suitable material in terms of absorption. The absorption coefficient and light penetration depth are presented in Fig. 3.5 for different materials with respect to wavelength.

As seen in Fig. 3.5, the increase in absorption coefficient for indirect band-gap materials such as GaAs, InGaAsP, and InGaAs is steeper than the direct band-gap materials such as Si and Ge.

The performance of the photodiode is described by quantum efficiency and responsivity. The quantum efficiency indicates the ratio of the generated electron numbers to the absorbed photon numbers and it is given as

$$\eta = \frac{I_{ph}/q}{P_0/(hc/\lambda)}, \quad (3.5)$$

where I_{ph} is the photocurrent, P_0 is the input optical power. q indicates the electron charge. The quantum efficiency is unitless.

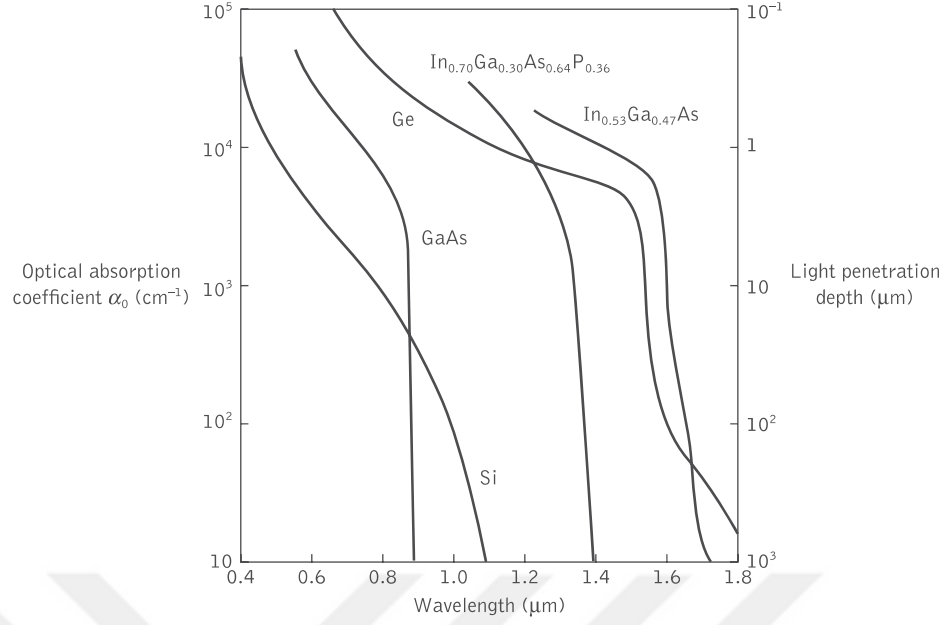


Figure 3.5: Optical absorption curves for some common semiconductor photodiode materials [94].

The responsivity (R) of the photodiode is related to the conversion of the optical power to the electrical current and it is given as

$$R = \frac{I_{ph}}{P_0} = \eta \frac{\lambda q}{hc} = \eta \frac{\lambda}{1.24 \mu m} \text{ (A/W)}, \quad (3.6)$$

The responsivity curve versus wavelength is given in Fig. 3.6 for different materials. When the depletion region has an infinite width, the quantum efficiency (η) is equal to 1 and the responsivity linearly increases over wavelength. However, the depletion width is finite in the reality and therefore the responsivity reaches a peak first and starts to decrease. The typical responsivity of the Silicon photodiode is between 0.2 and 0.4 (A/W) as seen in Fig. 3.6.

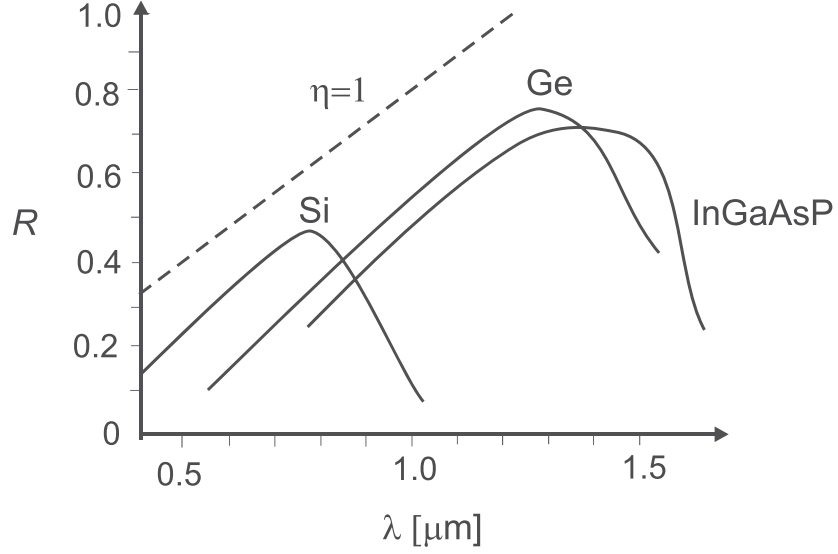


Figure 3.6: Responsivity of a Si, Ge, and InGaAs photodiode versus the wavelength [95].

The speed of the photodiode is related to its equivalent circuit and it is illustrated in Fig. 3.7.

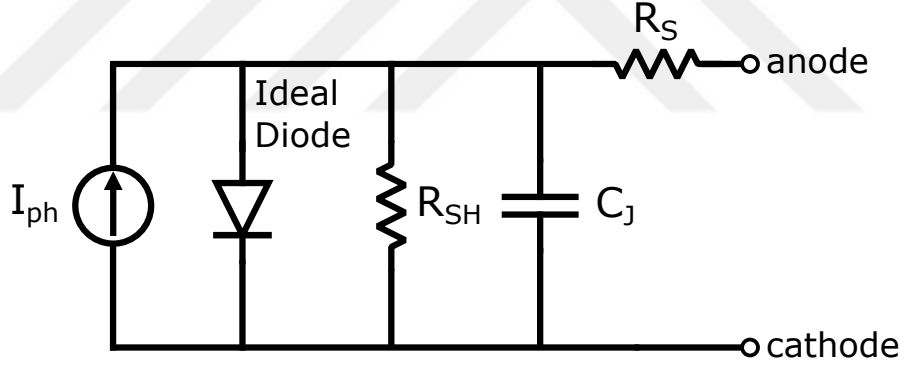


Figure 3.7: Equivalent circuit of the photodiode.

In Fig. 3.7, the current source of I_{ph} represents photocurrent. R_{SH} and R_S are the shunt resistance and the series resistance of the photodiode. C_J indicates the depletion capacitance, which is the main limiting factor for the speed of the photodiode and it is given as [96]

$$C_J = A \sqrt{\frac{\epsilon_{si}\epsilon_0 N_A N_D}{2(N_A + N_D)(\phi_{built-in} - V_a)}}, \quad (3.7)$$

where A , ϵ_{si} , and ϵ_0 indicate the area of the photodiode, the relative permittivity of the silicon, and the permittivity of the free space, respectively. N_A is the

doping concentration of acceptor atoms and N_D is the doping concentration of donor atoms. $\phi_{built-in}$ and V_a represent the built-in potential of the junction and the external applied voltage, respectively.

3.2.1 CMOS Photodiode Structures

To build the photodiode in a standard CMOS process, there are three main structures, which are n+/p-sub, n-well/p-sub, and p+/n-well/p-sub. The cross-section of these structures is illustrated in Fig. 3.8 (a-c), respectively.

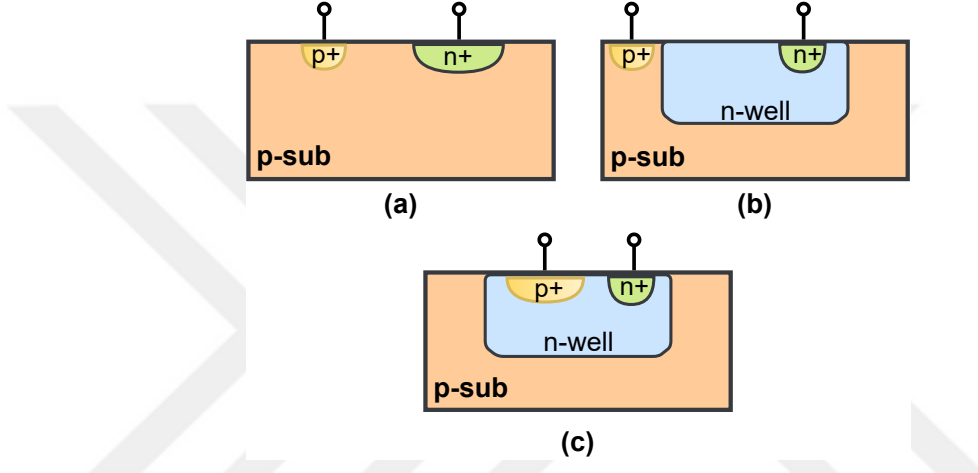


Figure 3.8: CMOS photodiode structures. (a) n+/p-sub, (b) n-well/p-sub, (c) p+/n-well/p-sub.

CMOS photodiode structures shown in Fig. 3.8 (a-c) have different performances. Fig. 3.8 (a) is the n+/p-sub structure, where the photodiode is formed between p-sub and n+. p+ and n+ represent the anode and cathode of the photodiode, respectively. Due to the highly doped n+, the depletion width is low and so the depletion capacitance becomes high [97]. Further, the collection efficiency of free carriers is small since n+ is shallow.

In Fig. 3.8 (b), the n-well/p-sub structure is demonstrated. The photodiode is embodied between p-sub and n-well. Contacts for the anode and cathode are provided by p+ and n+, respectively. The depletion width of the n-well/p-sub is larger than that of n+/p-sub, since the n-well is lightly doped. This leads to a lower depletion capacitance. Due to having a deeper junction (n-well), it has better collection efficiency [98].

The p+/n-well/p-sub structure (Fig. 3.8 (c)) includes two p-n junctions, which are parallel to each other. The first one is between p-sub and n-well, and the second is one is between p+ and n-well. These two p-n junctions contribute to the depletion capacitance. Thus, its depletion capacitance is highest among the CMOS photodiode structures [99]. Additionally, it also exhibits the highest collection efficiency due to having a larger depletion region.

3.2.2 CMOS Photodiode Design

While designing a CMOS photodiode, one of the most important criteria to take into account is the depletion capacitance of the photodiode, which acts as the input capacitance of the receiver. Therefore, it will affect the frequency response of the TIA to be designed. Having a larger active area of the photodiode is advantageous to receive higher optical power, however, it results in higher depletion capacitance and thus lower speed, since the depletion capacitance is proportional to the active area. Eq. (3.7) is mostly presented in the literature to estimate the depletion capacitance of the photodiode. However, the related parameters such as N_A , N_D , and $\phi_{built-in}$ are not disclosed by United Microelectronics Corporation (UMC). The other model estimating the depletion capacitance is presented in some studies [98, 100, 101] and it is given as

$$C_{PD} = \frac{C_{J0}A_D}{(1 - (\frac{V_d}{v_j}))^m} + \frac{C_{J0sw}P_D}{(1 - (\frac{V_d}{v_{jsw}}))^{m_{jsw}}}, \quad (3.8)$$

where C_{J0} and C_{J0sw} indicate the capacitance at zero bias for the bottom and sidewall components, A_D and P_D represent the area and periphery of the photodiode in m^2 and m , respectively. V_d is the DC voltage applied to the photodiode, v_j and v_{jsw} are the built-in potential for the bottom and the sidewall respectively. m and m_{jsw} are the grading coefficients of the bottom and the sidewalls, respectively.

In Cadence Virtuoso software using UMC process design kits, the photodiode component is not available and therefore there are not any related parameters

or characteristics to model the photodiode. On the other hand, the parameters⁴ of different types of p-n junctions are present for diode application in line with Eq. (3.8). Thus, Eq. (3.8) is considered to estimate the photodiode's depletion capacitance.

To make the comparison for the depletion capacitance among CMOS photodiode structures, the active area of the photodiode is assumed to be as $10\ \mu\text{m} \times 10\ \mu\text{m}$ and the resulting depletion capacitance for each CMOS photodiode structure is presented in Fig. 3.9 with respect to applied reverse bias voltage⁵.

As seen in Fig. 3.9, the highest depletion capacitance is resulted for p+/n-well/p-sub. In comparison to p+/n-well/p-sub, for the n+/p-sub, lower depletion capacitance is obtained. Among the CMOS photodiode structures, n-well/p-sub exhibits the lowest depletion capacitance. Furthermore, the reverse bias voltage affects the depletion capacitance as shown in Fig. 3.9. The depletion capacitance for n-well/p-sub has a weaker dependence on the bias voltage. Thus, the selection of n-well/p-sub is advantageous to have the lowest capacitance and faster response time.

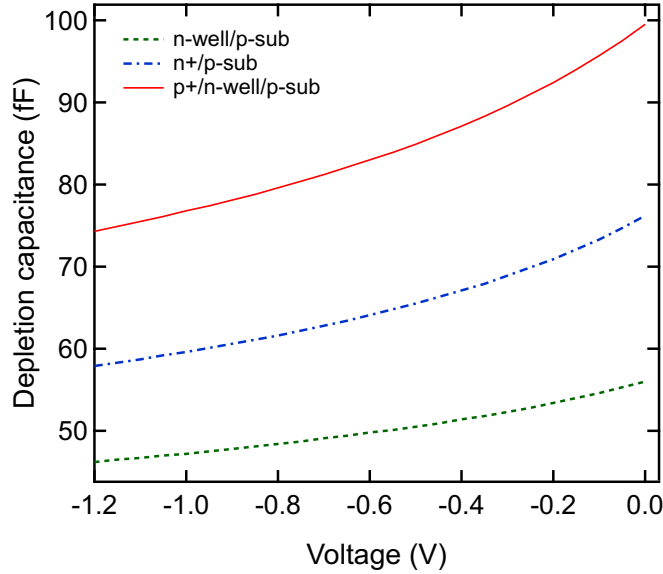


Figure 3.9: Depletion capacitance comparison among different photodiode structures.

⁴confidential information provided by UMC, no disclosure.

⁵maximum allowable reverse bias voltage is 1.2 V in used 130 nm technology.

In the studies [57, 98, 102, 103], for n-well/p-sub structure, the depletion capacitance values, which are not based on the measurement results, are given for different technologies. In Table 3, they are compared with the model using the Eq. (3.8).

Table 3: Works related to the photodiode capacitance

Work	Technology	Type	Dimension (um)	Area (um ²)	Bias (V)	Given Cap (fF)	Eq. (3.8) (fF)
[102]	180 nm	n-well/p-sub	R=30	2827	-1.8	248	175.55
	130 nm				0	404	307.06
					-1.2	498	498.15
					0	631	631.46
[98]	180 nm	n-well/p-sub	5×5	25	-1.4	2.31	1.97
			10×10	100		7.84	7.24
			20×20	400		28.85	27.70
			40×40	1600		110.50	108.25
[57]	350 nm	n-well/p-sub	100×100	10000	-1.2 ¹	650	697.41 ²
[103]	180 nm	n-well/p-sub	80×80	6400	0	428	442.80
	130 nm					1500	2985

¹ for this bias voltage.

² calculated by the parameters of 180 nm.

As seen in Table 3, the depletion capacitance values calculated using Eq. (3.8) are close to the depletion capacitance given in the related studies. This indicates that Eq. (3.8) is reliable and can be used to estimate the depletion capacitance while designing the photodiode. In addition to the photodiode's active area, the number of cells used in the photodiode has also an effect on the depletion capacitance. Therefore, different active areas of photodiodes with different cell numbers are investigated to observe the change in depletion capacitance. Active areas of the photodiode are selected as 100 $\mu\text{m} \times 100 \mu\text{m}$, 200 $\mu\text{m} \times 200 \mu\text{m}$, and 300 $\mu\text{m} \times 300 \mu\text{m}$, respectively. The depletion capacitance change of each photodiode with respect to the cell number at zero bias is tabulated in Table 4.

Table 4 shows that the depletion capacitance becomes higher as the cell number in the photodiode increases. Since the cells come near to each other, the capacitance resulting from the cell periphery will be as considerable as the areal capacitance. When the photodiode consists of one cell, its overall capacitance is

minimum. However, in this configuration, one large n-well is required, which leads to high resistance. To minimize the resistance, several smaller parallel n-well regions, which are separated by substrate contacts, can be employed [103]. Since there is a trade-off between the resistance and overall capacitance associated with the cell number, in the design, the cell number is selected to be 16, 25, and 36 for the photodiode with active areas of $100\text{ }\mu\text{m}\times 100\text{ }\mu\text{m}$, $200\text{ }\mu\text{m}\times 200\text{ }\mu\text{m}$, and $300\text{ }\mu\text{m}\times 300\text{ }\mu\text{m}$, respectively.

For the n-well/p-sub structure, having a lower depletion capacitance is analyzed and discussed. Moreover, n-well/p-sub structure outperforms other CMOS photodiode structures in terms of the sensitivity and Signal-to-Noise Ratio (SNR) [97, 98]. From these reasons, the n-well/p-sub structure is the most suitable one for designing CMOS photodiode. UMC does not provide a schematic for the photodiode and therefore the physical model should be laid out in Cadence Virtuoso software by designer. This implies that Layout versus Schematic (LVS) can not be used for the photodiode.

To operate the receiver as differential, active and dummy photodiodes are laid out. Active photodiode receives the light and dummy photodiode does not receive the light, since its surface is covered. First, the layout of the active photodiode is presented in detail and then the dummy photodiode design is explained.

Table 4: Cell Number, Cell Size, Depletion Capacitance values for different sizes of photodiodes at zero bias

Cell Number	Photodiode Active Area									
	100 $\mu\text{m} \times 100 \mu\text{m}$			200 $\mu\text{m} \times 200 \mu\text{m}$			300 $\mu\text{m} \times 300 \mu\text{m}$			Overall
	Cell size	Cap. per Cell (pF)	Overall Cap. (pF)	Cell size	Cap. per Cell (pF)	Overall Cap. (pF)	Cell size	Cap. per Cell (pF)	Overall Cap. (pF)	
1	100	1.96	1.96	200	7.04	7.04	300	15.25	15.25	15.25
4	50	0.59	2.36	100	1.96	7.85	150	4.11	16.46	16.46
9	33.33	0.30	2.77	66.66	0.96	8.66	100	1.96	17.67	17.67
16	25	0.19	3.17	50	0.59	9.47	75	1.18	18.88	18.88
25	20	0.14	3.58	40	0.41	10.28	60	0.80	20.10	20.10
36	16.66	0.11	3.98	33.33	0.30	11.08	50	0.59	21.31	21.31
49	14.28	0.08	4.38	28.57	0.24	11.89	42.85	0.45	22.52	22.52
64	12.5	0.07	4.79	25	0.19	12.70	37.5	0.37	23.73	23.73
81	11.11	0.06	5.19	22.22	0.16	13.51	33.33	0.30	24.94	24.94
100	10	0.05	5.60	20	0.14	14.32	30	0.26	26.16	26.16

3.2.3 Active Photodiode

The layout of the photodiode with the area of $300\text{ }\mu\text{m}\times 300\text{ }\mu\text{m}$ is shown in Fig. 3.10. Metal-1 and Metal-2 refer to the anode and cathode, respectively. The contact for the p-sub region is provided via Metal-1 and for n-well region the contact is provided via Metal-2. The light leakage takes place on the red-colored area (in Fig. 3.10). The fill factor⁶ is around 67.5 %.



Figure 3.10: Layout of the active photodiode.

3.2.4 Dummy Photodiode

The dummy photodiode has the same junction area with the active photodiode. The only difference between the active and dummy photodiode relies on that the dummy photodiode's surface is covered by metal layers not to receive light, since the light can not leak through the metal layer. According to the process design rule, it is not allowed to bring a large metal block onto the photodiode. To overcome this design rule, small slots are added to the top metal layer (ME-8), providing

⁶It is the ratio of photosensitive area to the overall junction area and this term is mainly used in photodiodes and image sensors.

for relieving the metal stress. However, the light can leak through the small metal slots. To block the light leakage, another metal layer (ME-7) is placed under ME-8 and thereby the light is sandwiched between these metal layers, which prevents the active area from reaching the light. ME-7 has also slots due to the design rule but the slots in ME-7 are shifted in reference to the slots of ME-8. Further, ME-7 and ME-8 are shorted to each other to diminish the additional capacitance as compared to the active photodiode.

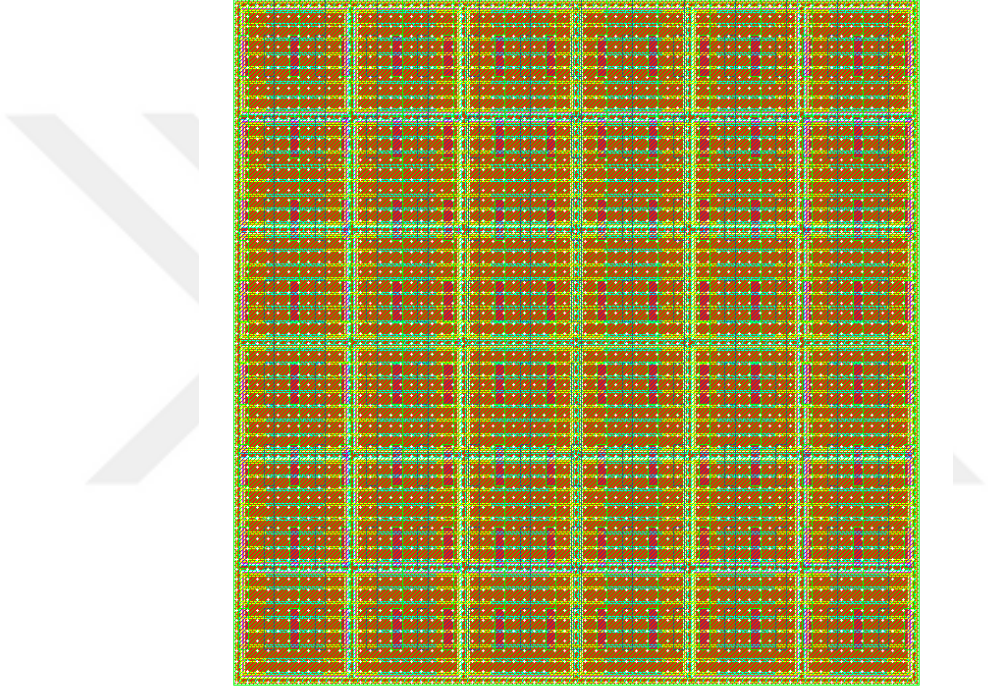


Figure 3.11: Layout of the dummy photodiode.

3.3 Transimpedance Amplifier

After the photodiode converts the incoming optical power into the electrical current by its responsivity, the electrical current should be transformed into the voltage with a gain, since the electrical current from the photodiode is generally a weak signal in terms of amplitude. Moreover, the responsivity parameter for the designed CMOS photodiode is not present and it should be estimated to be much lower than the commercial photodiodes with a responsivity of 0.2-0.3 A/W typically. Additionally, the active area of the designed CMOS photodiode is 7-8 times smaller than a typical commercial photodiode, resulting in obtaining a lower current together with the smaller active area. Therefore, the electrical current should be so converted to the voltage that a minimum amount of noise is added and thereby the signal can be further processed by following sub-blocks. Since the TIA is the first electronic circuit after the photodiode, the noise is largely affected by the TIA.

The TIA does the conversion of the electrical current into the output voltage. This can be simply achieved by adding a load resistor (R_L) parallel to the photodiode⁷ and thus the photocurrent (I_{ph}) is converted to the voltage over the load resistance as shown in Fig. 3.12.

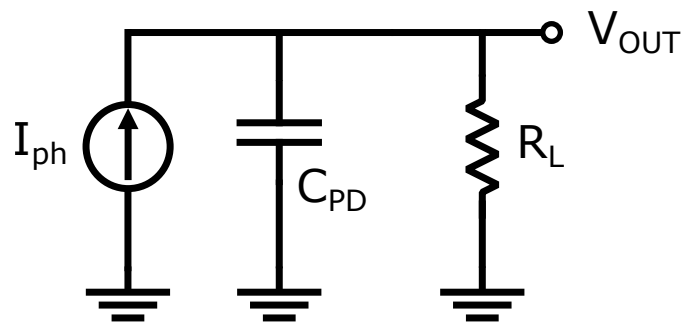


Figure 3.12: Open loop TIA configuration.

The transimpedance gain (Z_T) refers to the ratio of the output voltage to the input photocurrent and it is given as

⁷Photodiode is modeled by a current source and capacitance, since the shunt and series resistance of the photodiode are very large and negligible, respectively.

$$Z_T = \frac{V_{OUT}}{I_{ph}} = R_L, \quad (3.9)$$

As seen in Eq. (3.10), the transimpedance gain is proportional to the load resistance. The photodiode's capacitance (C_{PD}) and load resistance forms bandwidth of the TIA and the 3-dB frequency is given as

$$f_{3\text{-dB}} = \frac{1}{2\pi C_{PD} R_L}, \quad (3.10)$$

Eq. (3.10) indicates that the 3-dB frequency decreases as the R_L increases, resulting in a trade-off between the transimpedance gain and bandwidth. To achieve higher bandwidth, the input impedance, which is R_L , should be lowered. Using shunt-shunt feedback, the input resistance can be lowered, and hence the bandwidth is increased. The shunt-shunt feedback topology is illustrated in Fig. 3.13.

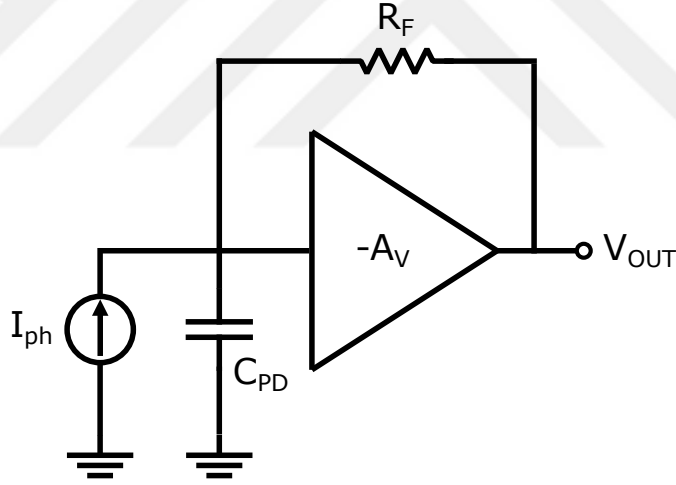


Figure 3.13: Shunt-feedback TIA with resistive feedback.

As seen in Fig. 3.13, the output is given to the input over the feedback resistance (R_F), making use of the negative feedback. The transimpedance gain is equal to R_F . Further, this type of topology achieves lowering input resistance by a factor of the amplifier's open-loop gain (A_V) and the input resistance is equal to $R_F/(1 + A_V)$. Using shunt-shunt feedback, the 3-dB bandwidth is given as

$$f_{3\text{-dB}} = \frac{1 + A_V}{2\pi C_{PD} R_F}, \quad (3.11)$$

The bandwidth of the TIA is extended by the amplifier's open-loop gain as shown in Eq. (3.11). For the TIA, there are two types of topologies, which are open-loop and closed-loop.

As an example of open-loop topology, the common-gate TIA is illustrated in Fig. 3.14. It is based on common-gate amplifier with M_1 transistor and drain resistance (R_D). M_2 transistor is used for biasing. The photocurrent is transformed to the output voltage over R_D . The structure utilizes having a small input impedance of the common-gate amplifier, which is equal to $1/g_{m1}$. Therefore, it exhibits higher bandwidth. However, the input-referred noise is largely dependent on R_D and M_2 , since their noise sources are directly referred to the input. To reduce the noise, the value of R_D and the size of M_2 can be changed but this will affect the bias current and voltage headroom.

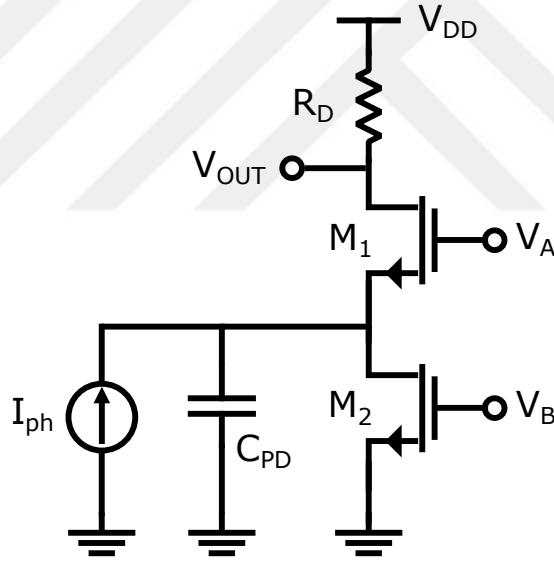


Figure 3.14: Common-gate TIA topology.

The CMOS inverter TIA is presented in Fig. 3.15 as an example for the closed-loop topology. M_1 and M_2 are NMOS and PMOS transistor pair of the inverter, respectively. The feedback is provided by R_F . This topology makes use of larger effective transconductance ($\frac{1}{g_{m1}+g_{m2}}$) due to the transistor pair, which leads to having lower input resistance and thus higher bandwidth. This topology provides high gain, however, it suffers from increasing the parasitic capacitance due to larger PMOS transistor.

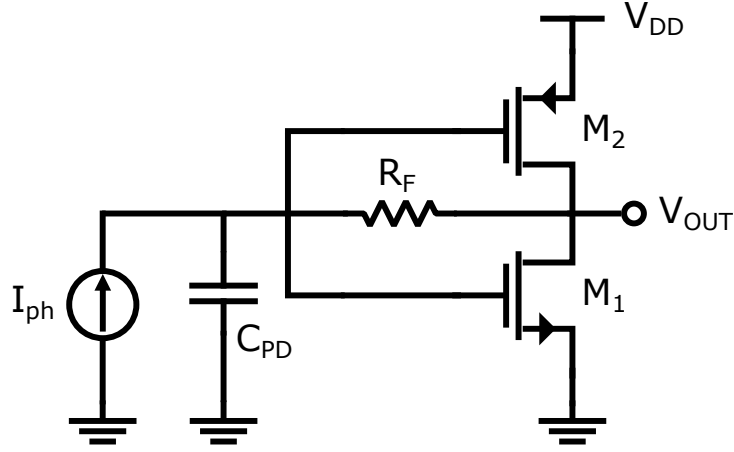


Figure 3.15: Inverter-based TIA.

3.3.1 Design of the transimpedance amplifier

The closed-loop topology relaxes the bandwidth limitation in open-loop topology. Hence, the closed-loop topology is employed while TIA design. On the other hand, it is important to state that differential structure exhibits better noise immunity than the single-ended structure. Since the active and dummy photodiode are laid out, the designed TIA is differential. The active and dummy photodiode introduce the dark current due to the reverse bias. Using differential TIA, the noise resulting from the dark current and supply voltage are minimized [104]. The schematic of the proposed TIA (blue-dashed) is illustrated in Fig. 3.16 together with the succeeding gain stage. The designed TIA consists of two stages.

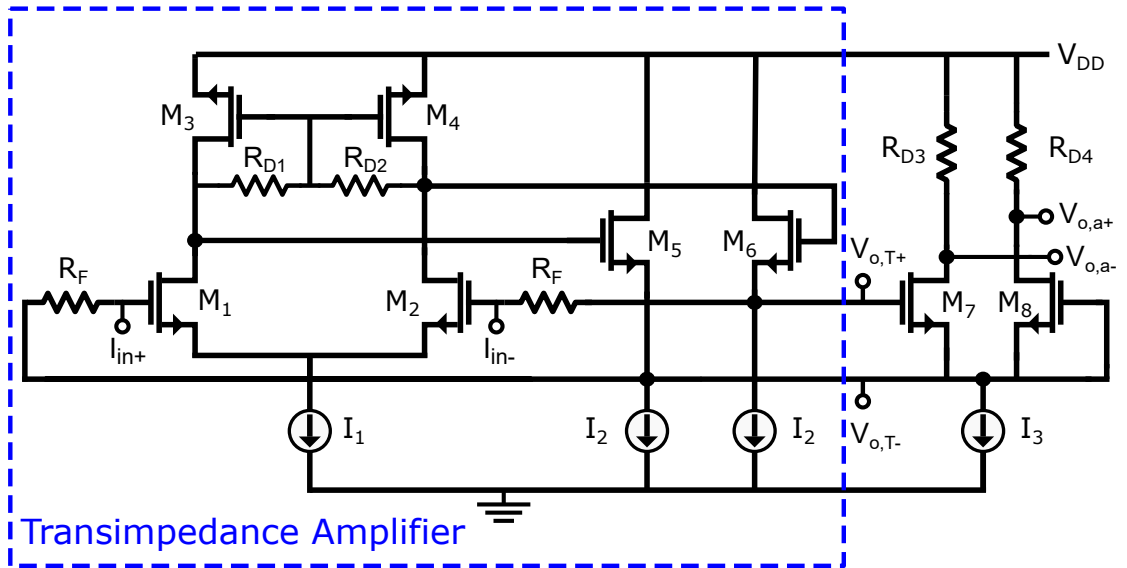


Figure 3.16: The schematic of the designed TIA and succeeding gain stage.

The first stage is a gain stage and it is based on the common-source amplifier, where M_1 - M_2 transistor pair is used for amplification and M_3 - M_4 transistor pair are used as an active load. R_{D1} - R_{D2} resistors act as boosting the first stage's gain. The second stage is a buffer, where M_5 - M_6 transistor pair provides the isolation. I_{in+} and I_{in-} represent the inputs for the current, and the cathode of the active and dummy photodiode are connected to these input nodes, respectively. The anode of the photodiodes is tied to the ground and thereby the reverse bias operation is provided. The resistive feedback is achieved between the first and second stage over R_F . The photocurrent generated by the active photodiode is converted to the voltage at the second stage's output through R_F . As mentioned earlier, the responsivity of the photodiode is unknown and therefore it could be possible to encounter a weak photocurrent after the photodiode implementation. By considering this, it is beneficial to increase the transimpedance gain further by adding a succeeding gain stage. The transimpedance gain can also be increased by keeping R_F higher, resulting in decreasing the bandwidth. This way is not preferred, since the capacitance of the photodiode is only estimated, which indicates that the photodiode could bring higher capacitance than estimated after the fabrication. The succeeding gain stage is a common-source amplifier, where M_7 - M_8 transistor pair and load resistances of R_{D3} - R_{D4} are employed. I_1 , I_2 , and I_3 denote the bias currents. Fig. 3.17 shows the layout of the designed TIA with a succeeding gain stage.

The performance of the TIA is determined by different parameters, such as transimpedance gain, bandwidth and input-referred noise current, which are investigated by performing various simulation analyses. The simulation results for the proposed TIA (Fig. 3.16) are presented in the following subsections.

3.3.2 AC Simulation

The AC simulation is performed to observe the frequency response and determine the 3-dB bandwidth of the TIA. Additionally, the transimpedance gain is extracted based on the frequency response. According to Table 4, the depletion

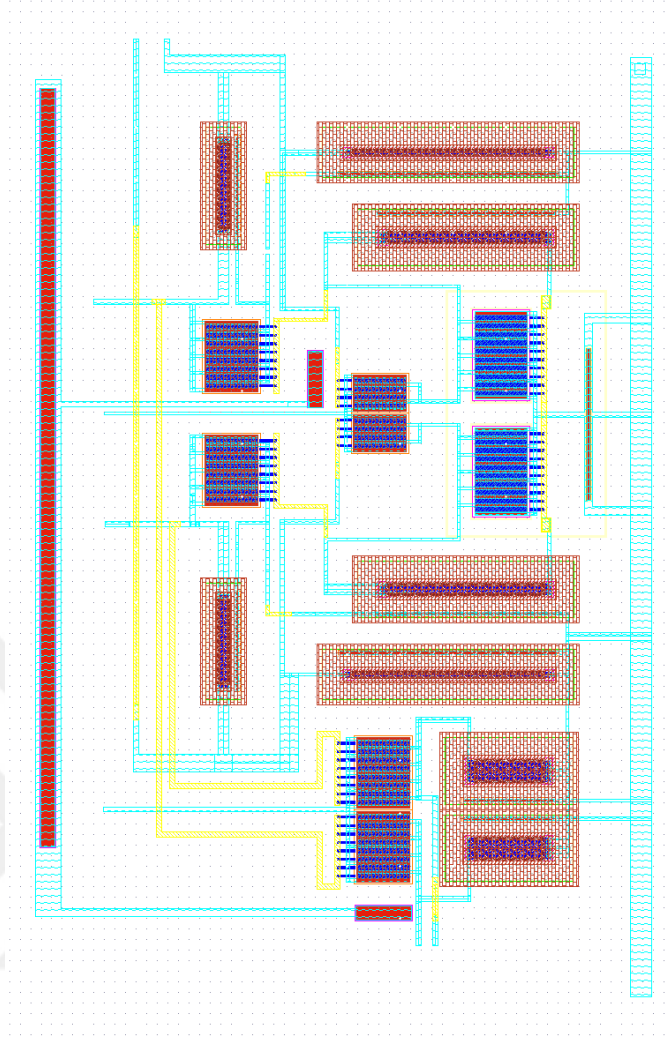


Figure 3.17: Layout of the designed TIA with a succeeding gain stage.

capacitance is estimated as 21.31 pF at zero bias for the photodiode with the area of $300\text{ }\mu\text{m} \times 300\text{ }\mu\text{m}$. The input nodes of I_{in+} and I_{in-} , to which the cathodes of the photodiodes are connected, are biased around 0.6 V, resulting in a depletion capacitance of 18.38 pF. Considering the parasitic and PCB-related capacitance, the input capacitance is selected to be 20 pF while performing the simulation. Further, the shunt resistance of the photodiode is assumed to be 2 MOhm, which is normally in the order of a few MOhm [105]. The frequency response of the proposed TIA is shown in Fig. 3.18 for pre-and post-layout simulations. The pre-and post-layout simulation results comply with each other as seen in Fig. 3.18. The transimpedance gain⁸ is 75.81 dB Ω and the 3-dB bandwidth is around 103 MHz.

⁸The simulated transimpedance gain considers the succeeding gain stage as well.

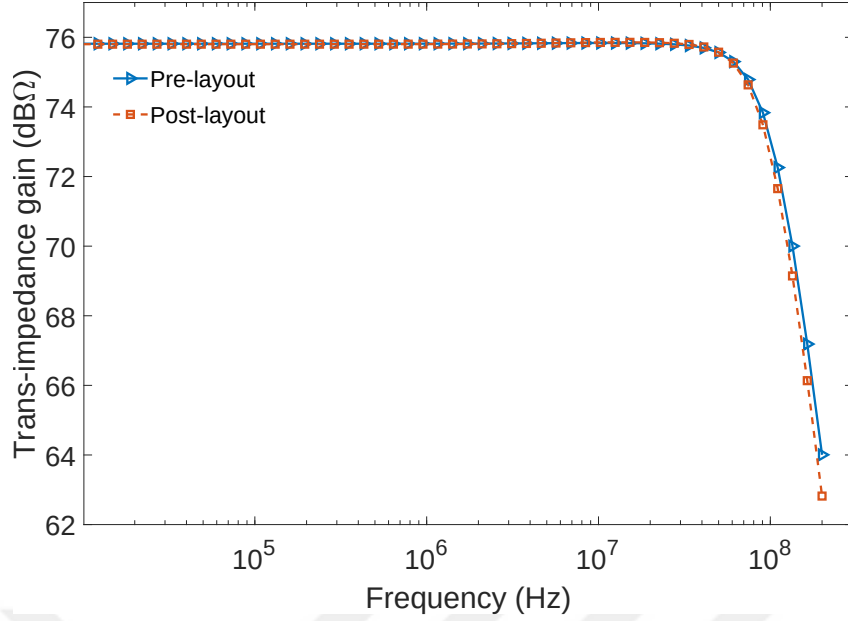


Figure 3.18: AC simulation results of the designed TIA.

3.3.3 Transient Simulation

The proposed receiver is not fully differential and it is operated as pseudo-differential, since the light signal is received by the active photodiode. To observe the operation, the differential outputs of $V_{o,a+}$ and $V_{o,a-}$ are monitored in the time domain performing the transient simulation. A sinusoidal current source with a frequency of 1 MHz, replacing the photocurrent of the active photodiode, is applied from one side and the simulation is performed for 5 μ s, involving 5 periods. The monitored differential outputs are presented in Fig. 3.19.

Fig. 3.19 shows that $V_{o,a+}$ and $V_{o,-}$ are 180° out of phase. DC bias of differential signals is at 0.8 V and the difference between peak-to-peak voltages is around 5 mV, which indicates that the proposed TIA with a succeeding gain stage achieves the differential operation. Additionally, the sinusoidal signals at the differential outputs are not distorted, preserving their waveforms.

3.3.4 Noise Simulation

The noise simulation is performed to observe the input current noise density of the receiver, which is required to estimate the SNR at the input of the receiver. In the noise analysis, photodiode, TIA, and gain stage are considered, since the effect

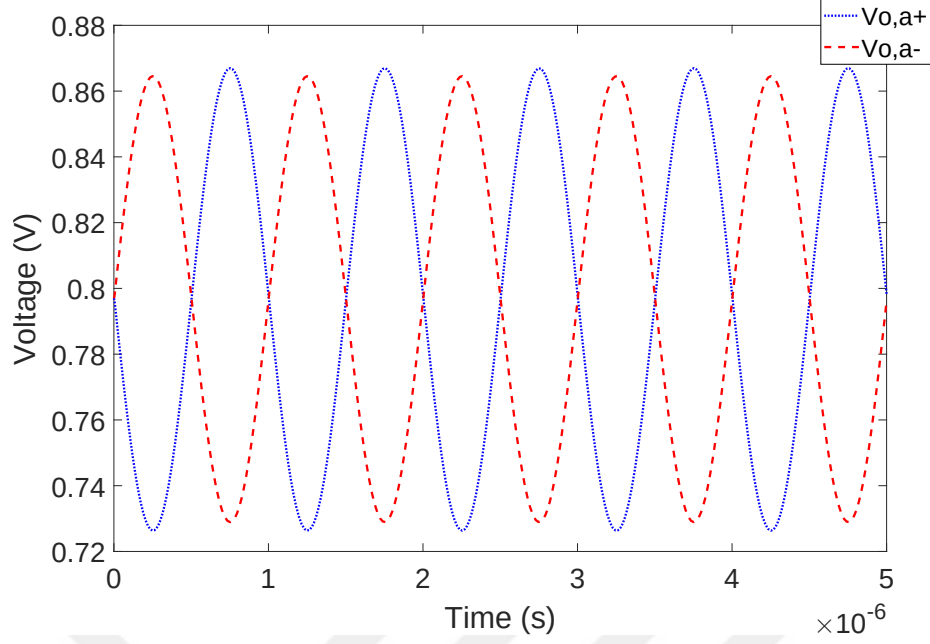


Figure 3.19: Transient simulation results of the designed TIA.

of following stages on the noise is negligible. The equivalent circuit for the noise analysis is presented in Fig. 3.20.

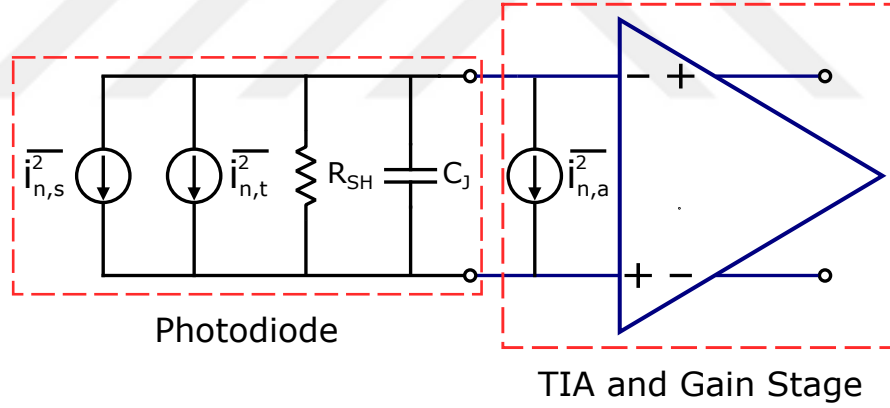


Figure 3.20: Noise equivalent circuit of the photodiode, TIA and succeeding gain stage.

where $\overline{i_{n,s}^2}$ and $\overline{i_{n,t}^2}$ represent the shot noise and thermal (Johnson) noise generated by the photodiode, respectively. $\overline{i_a^2}$ is the noise imposed by the TIA and succeeding gain stage.

The shot noise results from the dark current (I_s) and photocurrent (I_{ph}) generated by the input optical power. The shot noise current density is given as

$$i_{n,s} = \sqrt{2q(I_s + I_{ph})}, \quad (3.12)$$

The thermal noise is associated with the shunt resistance (R_{SH}) of the photodiode and it is given as

$$i_{n,s} = \sqrt{\frac{4kT}{R_{SH}}}, \quad (3.13)$$

In the noise simulation, the input-referred noise of the receiver ($i_{n,r}$) and $i_{n,a}$ are obtained. Shot noise current density and thermal noise current density are calculated using Eq. (3.12) and Eq. (3.13), respectively, since a photodiode model with noise characteristics is not present in the software. The related noise current densities are presented in Fig. 3.21.

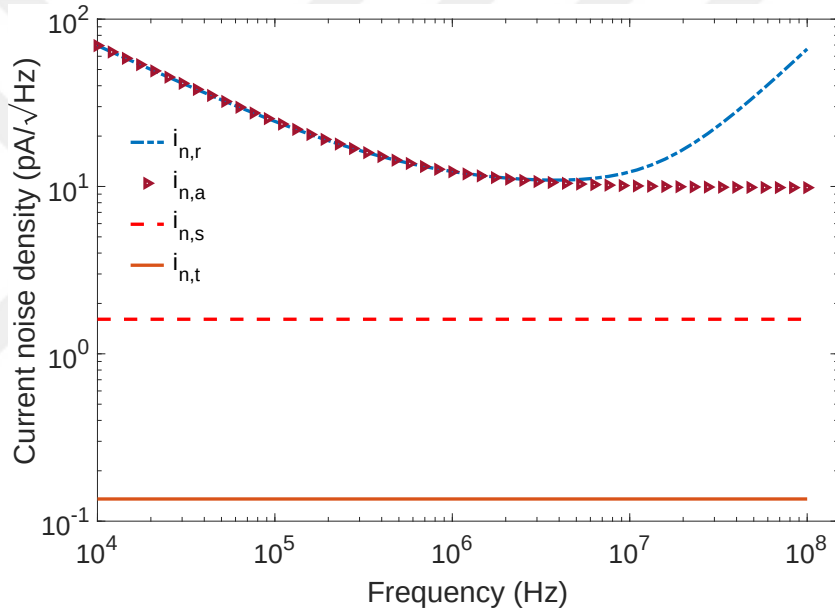


Figure 3.21: The simulated input-referred noise current density of the receiver.

As shown in Fig. 3.21, thermal and shot noise current density are much lower than the noise current density imposed by TIA and succeeding gain stage. $i_{n,t}$ and $i_{n,s}$ are $0.135 \text{ pA}/\sqrt{\text{Hz}}$ and $1.6 \text{ pA}/\sqrt{\text{Hz}}$, respectively. This indicates that the receiver noise is dominated by the first electronic block. While $i_{n,t}$ and $i_{n,s}$ are not frequency-dependent, $i_{n,a}$ and $i_{n,r}$ change over the frequency, where $1/f$ noise (flicker) arises in the low-frequency range. In the flat region, the current noise density is around $12 \text{ pA}/\sqrt{\text{Hz}}$. The difference between $i_{n,a}$ and $i_{n,r}$ with increasing frequency relies on the photodiode's junction capacitance, which is considered for

$i_{n,r}$. Since the impedance of the junction capacitance is varying with the frequency, the input impedance decreases and therefore the input-referred noise current density rises.

The noise current is obtained by integration of the input-referred noise current density over a bandwidth of interest (up to 100 MHz) and it is formulated as

$$I_{\text{noise}} = \sqrt{\int \overline{i_{n,r}^2} df}, \quad (3.14)$$

Using Eq. (3.14), the noise current is calculated as around $0.39 \mu\text{A}$ and this determines the minimum detectable current at the input receiver. SNR corresponds to the ratio of the photocurrent to the noise current, which is given as

$$SNR(dB) = 20 \log \left(\frac{I_{\text{ph}}}{\sqrt{\int \overline{i_n^2} df}} \right), \quad (3.15)$$

The photocurrent is assumed to be $22.5 \mu\text{A}$ based on the reference channel measurement discussed in 3.1. On the other hand, considering the case, where the photodiode has much lower responsivity than it is estimated, a photocurrent is analyzed under the assumption that the differential swing at the input of the equalizer is 50 mV at least, resulting in a photocurrent of $8 \mu\text{A}$. Using Eq. (3.15), SNR is obtained as 35 dB and 26 dB for the photocurrent of $22.5 \mu\text{A}$ and $8 \mu\text{A}$, respectively.

3.3.5 Stability Simulation

The resistive feedback is used between the first and second stages of the designed TIA. Therefore, the stability (STB) analysis is conducted to observe that the system is stable. In STB analysis, the circuit is linearized around the DC operating point, and the related parameters such as loop gain and phase margin are extracted. The probe, which is capable of breaking the differential mode loop, is employed through the feedback line and the stability simulation is performed up to 100 MHz. The loop gain and phase are presented in Fig. 3.22.

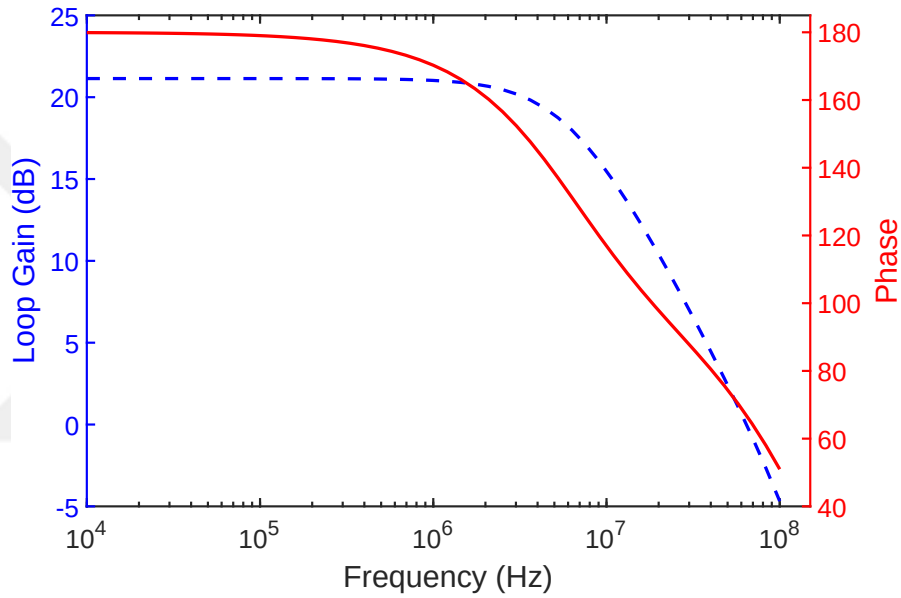


Figure 3.22: Stability simulation results of the designed TIA.

When the loop gain is 0 dB at 64.41 MHz, the phase is around 67°. Therefore, the system seems to be stable. The loop gain is mostly dependent on the drain resistors of R_{D1} and R_{D2} (Fig. 3.16). Increasing these resistors is associated with higher open-loop gain and therewith higher bandwidth. However, this lowers the phase margin and could result in an unstable system. On the other hand, the estimated photodiode's capacitance has a considerable effect on the phase margin. Considering a variation for the estimated capacitance, the phase margin is kept far from the oscillation.

3.4 Continuous Time Linear Equalization

The equalizer aims to provide compensation for the channel's frequency response. It makes use of a high-pass filter characteristic, where the low-frequency components are attenuated and the high-frequency components are amplified. CTLE can be achieved using passive or active structure, which are illustrated in Fig. 3.23.

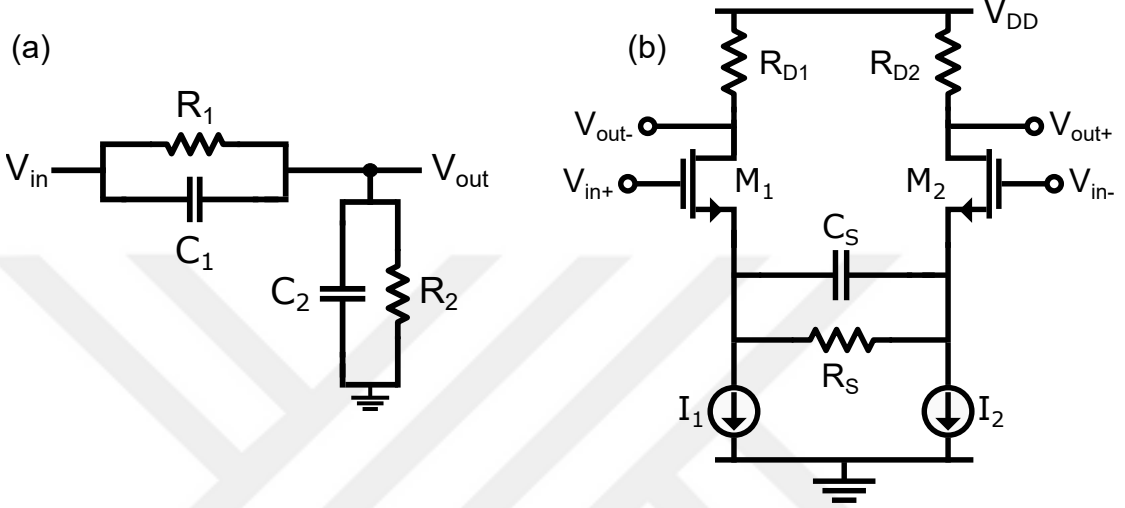


Figure 3.23: The schematic of the CTLE structures, (a) passive, (b) active.

The passive CTLE includes two R-C pairs as shown in Fig. 3.23 (a). R-C pairs form the zero and pole frequency in the circuit. Since R-C components are used, there is not any power injection to operate them. However, tuning of zero- and pole-frequency is difficult using passive CTLE. The active CTLE, presented in Fig. 3.23 (b), is a common source differential amplifier with source degeneration. It relies on shunting the source resistance (R_s), which results in higher source impedance at low frequencies and lower source impedance at higher frequencies. Thereby, the gain is boosted depending on the frequency and the compensation is achieved. Active CTLE generates a zero and a pole frequency and they are changed by source resistance and source capacitance (C_s). Active CTLE can be combined with inductors for shunt-peaking, leading to further bandwidth extension. Nevertheless, the inductor takes a larger area in the layout, limiting the overall chip area.

In VLC, white LEDs are used mostly and they offer limited bandwidth up to a few MHz. The zero-frequency generated by the CTLE should be in accordance with the 3-dB bandwidth of the related LED to enable the frequency compensation. Moreover, to be able to employ white LEDs with different 3-dB bandwidths, the zero and pole frequencies should be adjusted. Therefore, an adjustable CTLE is designed in the optoelectronic receiver. The zero- and pole-frequency are determined by source resistance and source capacitance, and thus they can be physically formed using transistors. However, adjusting the source resistance leads to change in gain simultaneously. On the other hand, the source capacitance change using a transistor exhibits a nonlinear profile [106]. Hence, while CTLE design, the source resistance is selected to be constant and the source capacitance change is achieved using a switching mechanism. The designed adjustable equalizer uses active CTLE topology and it is presented in Fig. 3.24.

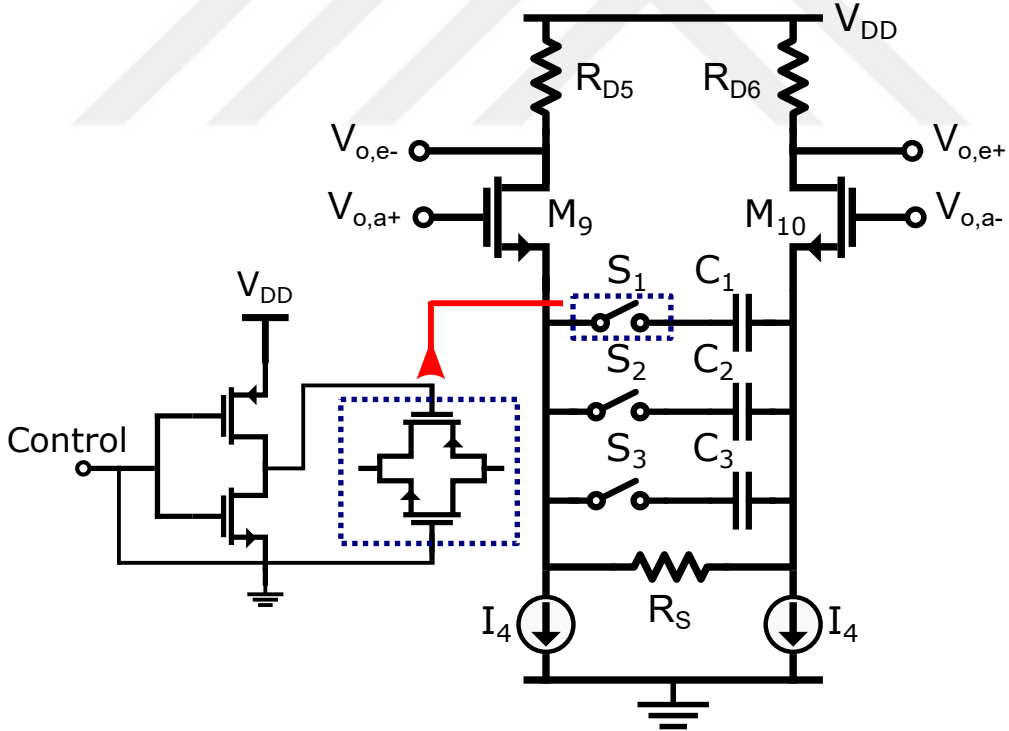


Figure 3.24: The schematic of the designed adjustable CTLE.

The inputs ($V_{o,a+}$ and $V_{o,a-}$) of M_9 and M_{10} are connected to the output of the preceding stage (Fig. 3.16). R_{D5} and R_{D6} are the drain resistances. I_4 provides current for biasing. C_1 , C_2 , and C_3 capacitors are controlled by a switching mechanism, consisting of an inverter and a transmission gate. The switching mechanism is operated as follows: "0" or "1" is applied from the control input and then applied and inverted signal control NMOS and PMOS transistors to activate or deactivate the transmission gate, respectively. According to the chosen capacitance/s, 7 different zero-frequencies can be generated. These zero-frequencies are adjusted considering the 3-dB bandwidth measurement performed beforehand. The frequency response of the designed CTLE is given as

$$H_{CTLE}(s) = \frac{V_{o,e+} - V_{o,e-}}{V_{o,a+} - V_{o,a-}} = \frac{g_{m9}}{C_{d10}} \frac{(s + \omega_z)}{(s + \omega_{p1})(s + \omega_{p2})}, \quad (3.16)$$

where $\omega_z = \frac{1}{R_S C_S}$ and $\omega_{p1} = \frac{1+g_{m9}R_S/2}{R_S C_S}$ indicate the zero- and pole-frequency of the equalizer, respectively. C_S refers to the the equivalent capacitance at the chosen switch state. $\omega_{p2} = \frac{1}{R_{d6} C_{d10}}$ is the second pole frequency, where C_{d10} models the capacitance lumped to the drain of M_{10} .

The CTLE's frequency response is characterized by some parameters such as DC gain and peaking gain. The DC gain is the gain exhibited by the equalizer for low frequencies and it is given as

$$\text{DC gain} = \frac{g_{m9} R_{D5}}{1 + g_{m9} R_S / 2}, \quad (3.17)$$

The peaking gain determines bandwidth extension and implies the ratio of the pole-frequency to the zero-frequency, which is given as

$$\text{Peaking gain} = \frac{\omega_{p1}}{\omega_z} = 1 + g_{m9} R_S / 2, \quad (3.18)$$

The layout of the designed CTLE is shown in Fig. 3.25.

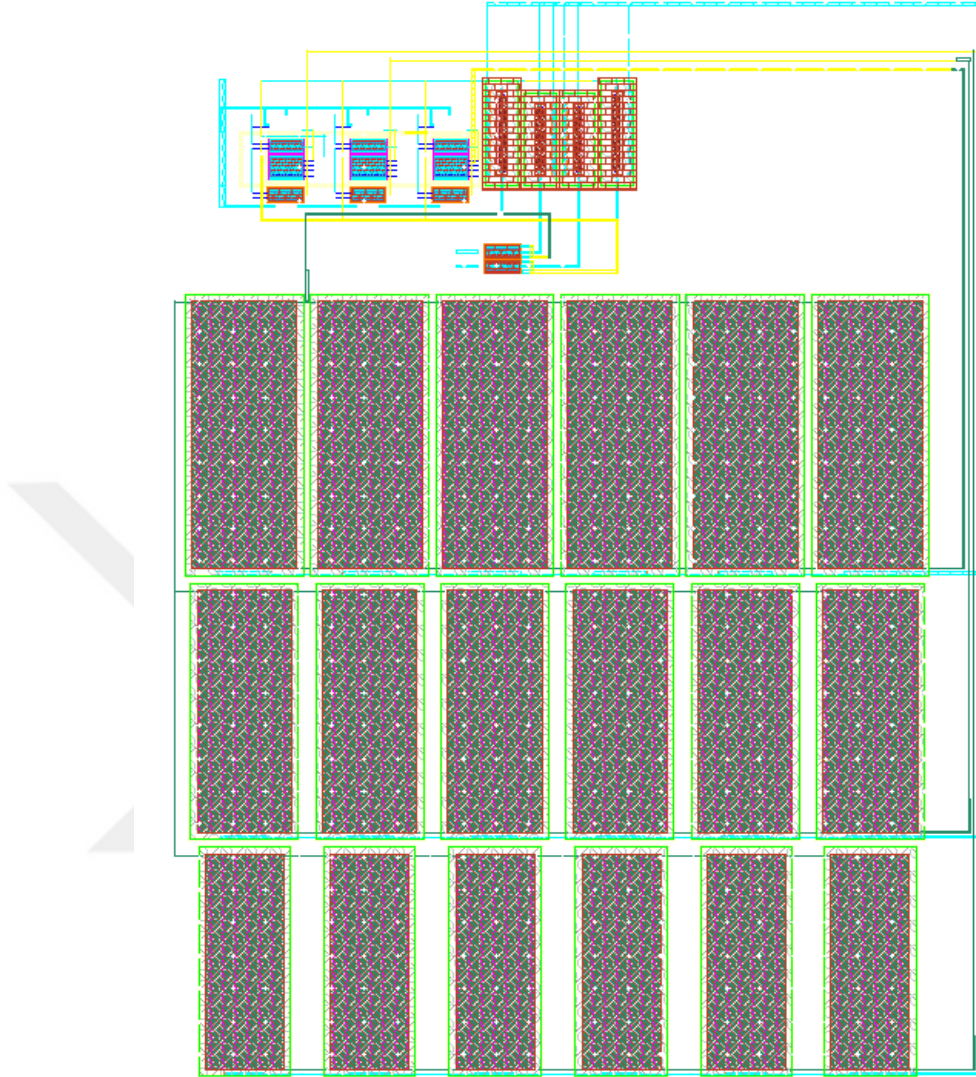


Figure 3.25: Layout of the designed CTLE.

The frequency response of the CTLE is obtained by performing an AC simulation. To observe the effect of the switching mechanism, different switch states are considered. CTLE's frequency response is presented in Fig. 3.26 for pre- and post-layout simulations.

Fig. 3.26 shows that the zero-frequency generated by CTLE is changed according to the switch states, which is suitable for employing LEDs with different bandwidths. "0" and "1" in the states indicate that the concerning switch is deactivated or activated, respectively.

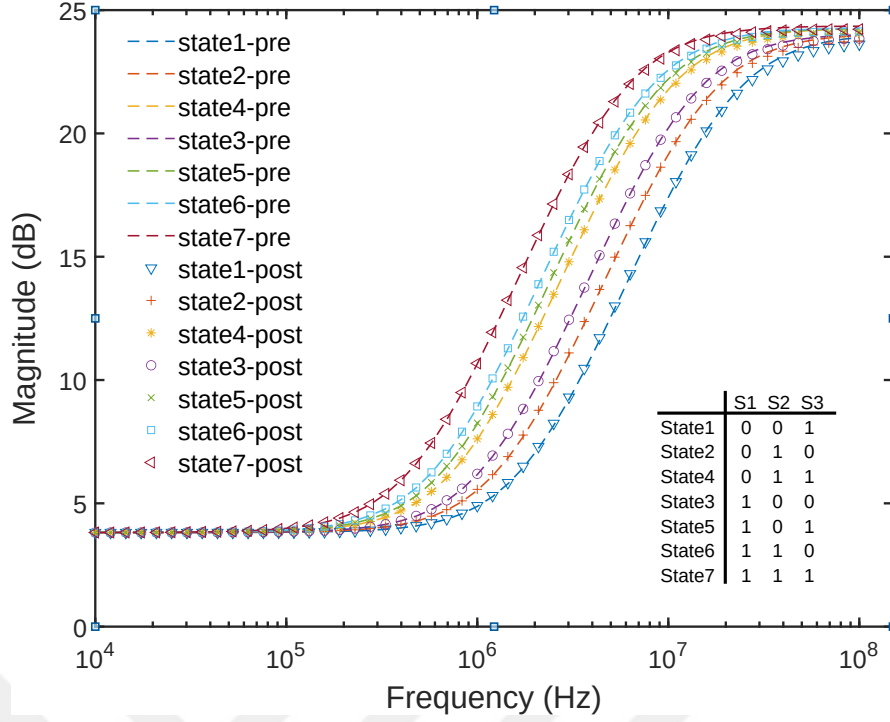


Figure 3.26: Frequency response of the designed CTLE at different switch states.

3.5 Buffer

Buffer is preceded by the CTLE and the function of the buffer is to provide the isolation for CTLE from the electronic equipment such as signal analyzer and digital oscilloscope used in the laboratory while testing the implemented chip, since signal analyzer and digital oscilloscope have an input impedance of 50 Ohm and shunt capacitance. Without using a buffer, CTLE's characteristic is affected by the electronic equipment. Therefore, the buffer should be capable of driving the internal circuit of the electronic equipment. The buffer's output impedance can be designed as 50 Ohm for impedance matching. Additionally, the buffer with a lower output impedance provides the advantage of transferring the output signal onto the equipment. To be able to monitor higher voltage, a buffer with a lower output impedance is designed. The designed buffer is illustrated in Fig. 3.27.

The designed buffer uses the common-drain topology, exhibiting lower output impedance. The outputs of CTLE are connected to the inputs ($V_{o,e-}$ and $V_{o,e+}$) of M_9 and M_{10} transistors. R_{B1} and R_{B2} are to set the bias condition. V_{out-} and V_{out+} refer to the outputs, through which the measurement is achieved.

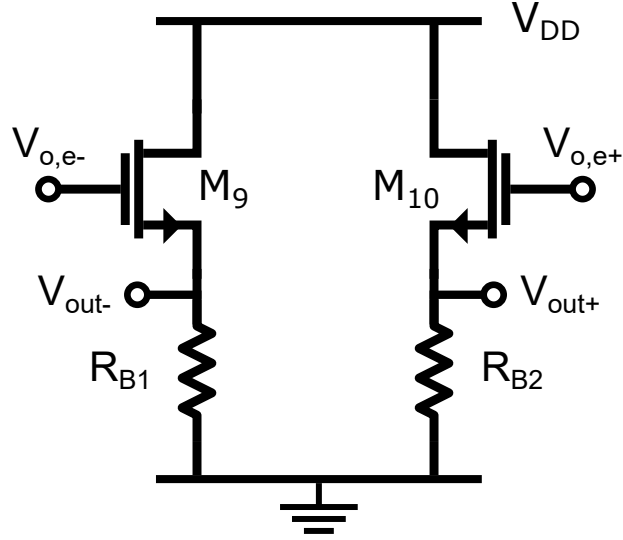


Figure 3.27: Schematic of the designed differential output buffer.

The layout of the designed buffer is shown in Fig. 3.28.

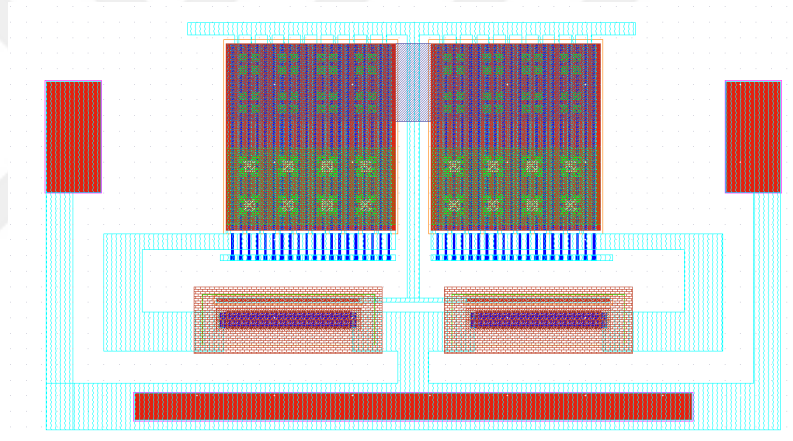


Figure 3.28: Layout of the designed output buffer.

The transient simulation is performed to observe that the designed buffer can drive the electronic equipment input, which is modeled with an impedance of 50 Ohm and a shunt resistance of 18 pF, considering also PCB-related capacitance, for the simulation. A frequency of 10 MHz sinusoidal signal is applied and the buffer's differential outputs are shown in Fig. 3.29.

The DC level of the differential outputs is decreased due to M_9 and M_{10} transistors and the buffer provided the isolation between CTLE's output and the electronic equipment.

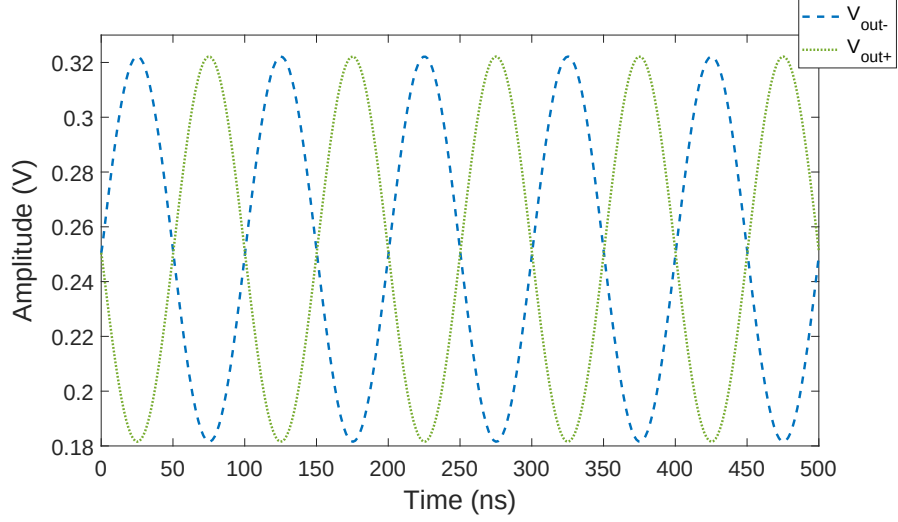


Figure 3.29: Transient simulation results of the designed output buffer.

3.6 Bias Circuit

The bias circuit is achieved using the current mirror shown in Fig. 3.30, providing the bias currents for the subblocks of TIA and CTLE. M_{B1} , M_{B2} , M_{B3} , and M_{B4} generates I_1 , I_2 , and I_3 for TIA. The bias for CTLE is provided by M_{B5} and M_{B6} , generating the current of I_4 . M_{REF} represents the reference transistor for the current mirror. For the resistance of R_{REF} , a potentiometer is employed and it is connected to the chip externally.

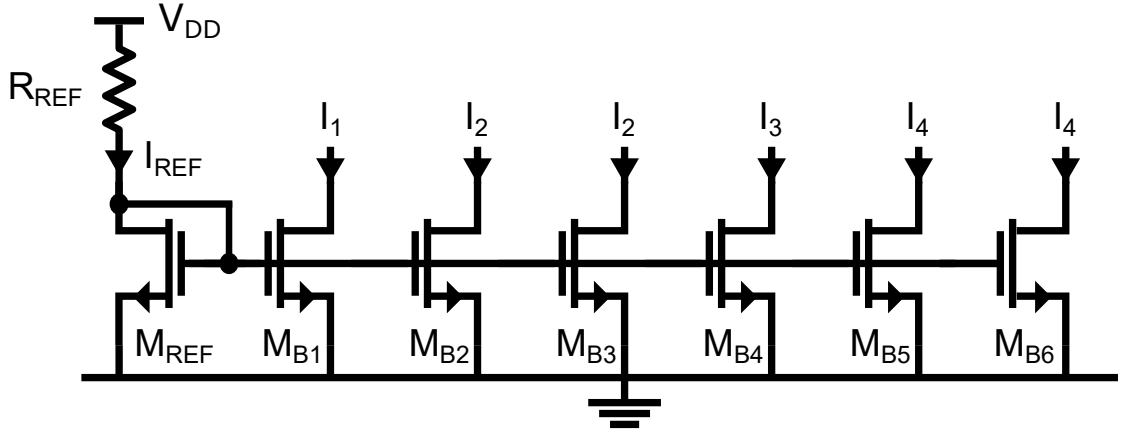


Figure 3.30: Schematic of the designed bias circuit.

The layout of the bias circuit is presented in Fig. 3.31.

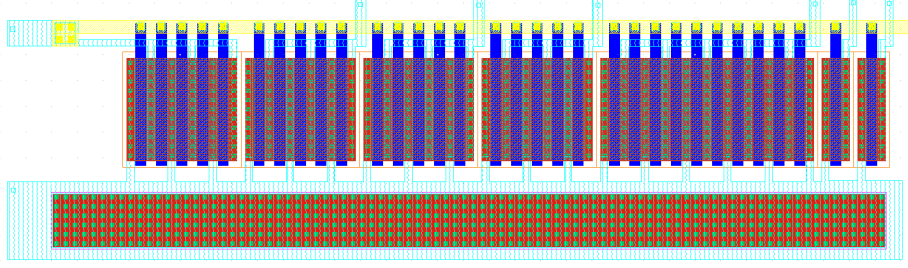


Figure 3.31: Layout of the designed bias circuit.

3.7 ESD and CLAMP

IC chips are sensitive devices to the ESD damages, where the instantaneous high voltage (i.e., spark) arises due to the human body discharging. This high voltage exceeds the transistor's gate-oxide break-down voltage and results in burning out the chip. ESD diodes are generally employed to protect the chip against higher voltage. Therefore, the designed chip is saved by ESD diodes on all input/output pads.

On the other hand, while the transistor's gate oxide is protected by ESD diodes from breaking down, high current flow through ESD diodes can also lead to damage within the chip. To overcome this problem, the clamp diodes are used between ground and supply voltage and thereby higher current follows over them. Additionally, clamp diodes provide clamp supply voltage. The schematic of ESD and CLAMP diodes are presented in Fig. 3.32.

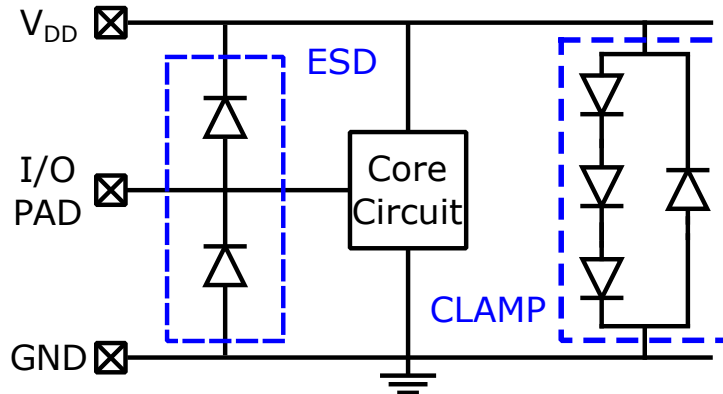


Figure 3.32: ESD and CLAMP diodes structure.

The layout of the ESD and CLAMP diodes are shown in Fig. 3.33 and Fig. 3.34, respectively.

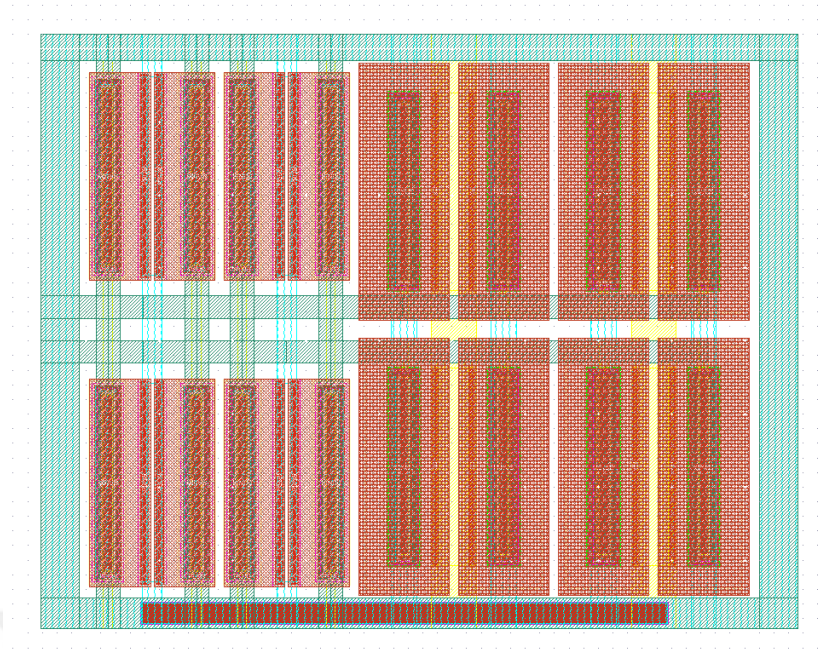


Figure 3.33: Layout of the ESD diodes.

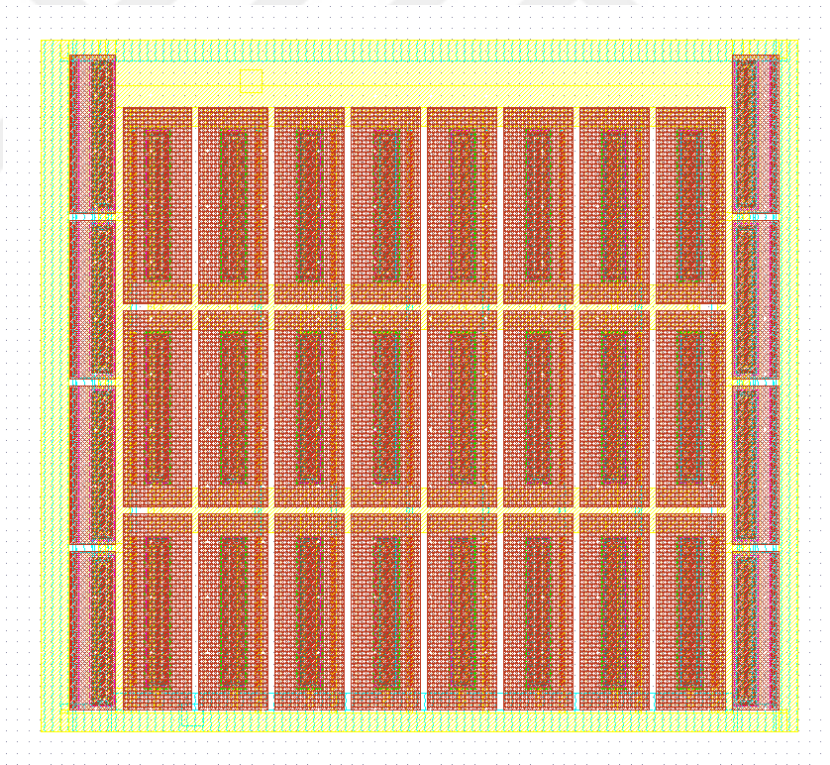


Figure 3.34: Layout of the CLAMP diodes.

The tape-out⁹ of the chip is given in Fig. 3.35. The chip has 48 bonding pads¹⁰ totally, four of which are not used. The size of the chip is 1.5 mm×1.5 mm.

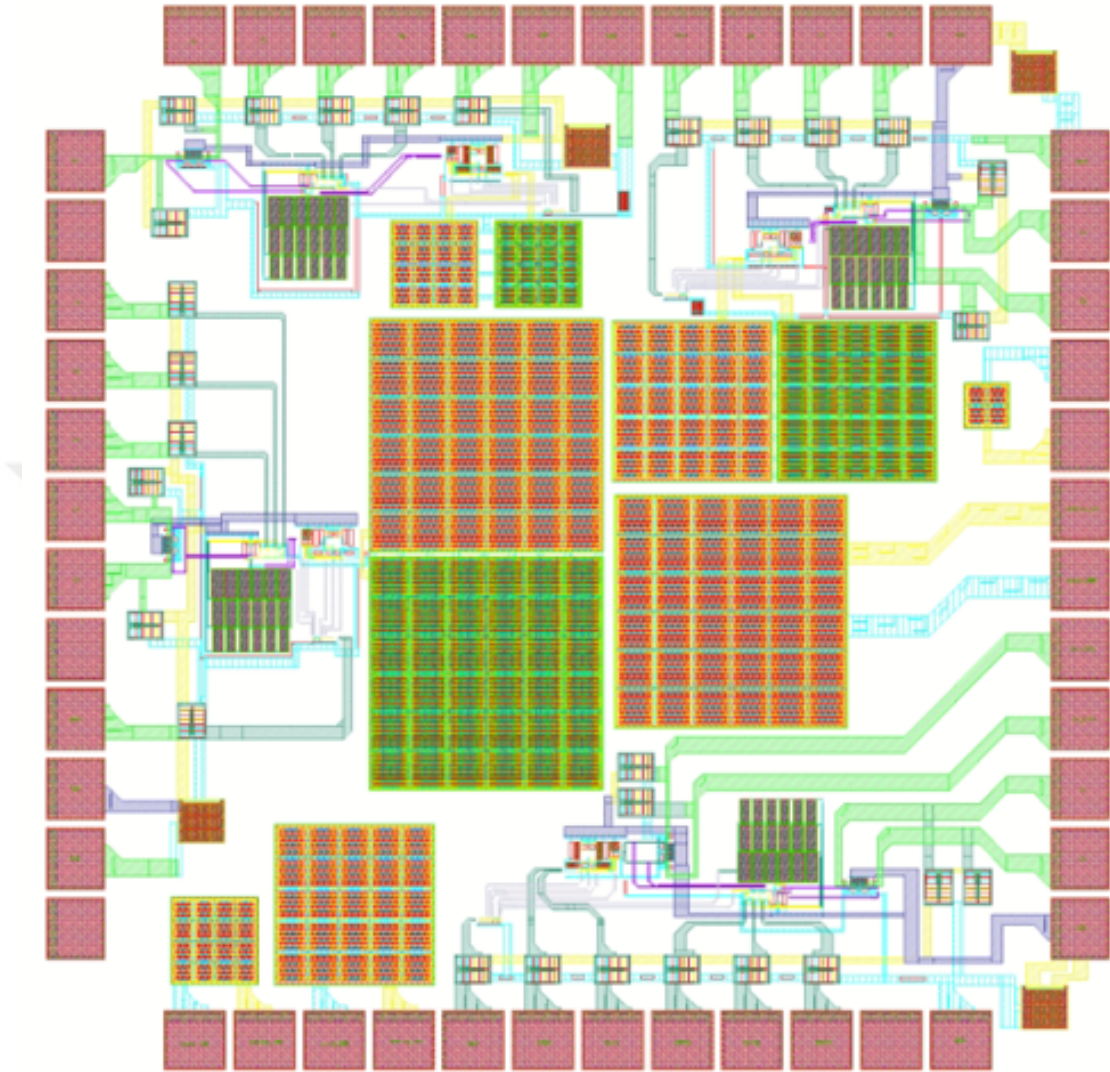


Figure 3.35: Tape-out in 130 nm CMOS technology.

⁹It implies the end-version of the chip that is submitted to the chip foundry to fabricate.

¹⁰They refer to the pads on the chip to which the wire will be bonded.

3.8 Packaging and PCB design

As a chip packaging type, Quad Flat pack No Leads (QFN) is selected and this packaging also supports an open air-cavity, since the designed chip includes a photodiode, receiving the light. The size of the package is $7\text{mm} \times 7\text{mm}$ and it has 48 bonding pins¹¹. The connection between bonding pins and bonding pads is achieved by wire-bonding¹². The wire-bonding scheme for the packaging and the implemented chip are shown in Fig. 3.36 and Fig. 3.37, respectively.

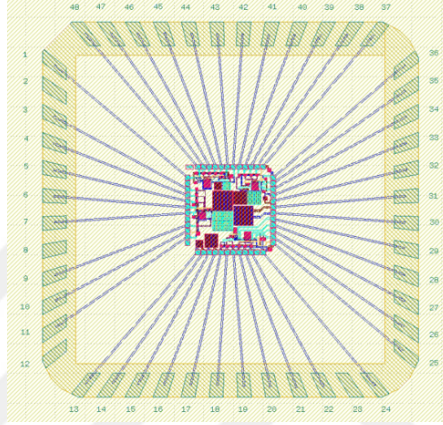


Figure 3.36: Bonding scheme for the packaging.

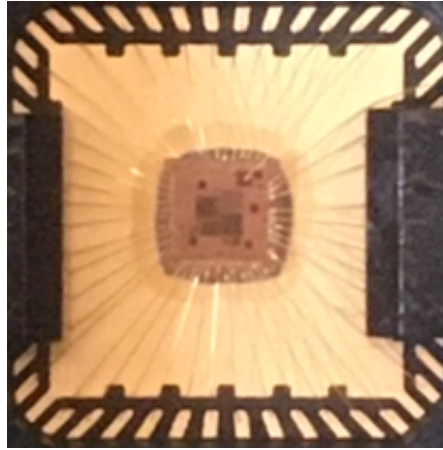


Figure 3.37: Implemented chip.

For characterization, a test PCB, on which the chip will be mounted, is required. Therefore, two test PCBs are designed and implemented. In the first test PCB, a socket, which is suitable for the QFN package, is soldered onto PCB and

¹¹They cover areas of the package on which the wire will be bonded.

¹²Wire bonding is electrical interconnect technology, using gold wire with a diameter of around $25.4\ \mu\text{m}$ typically.

the chip is inserted into the socket. The test PCB is equipped with some electronic components and they are potentiometers, capacitors, resistors, and switches. Potentiometer acts as bias resistors to form the bias current. Capacitors are used to suppress the noise. Switches provide tuning for CTLE and they are protected by resistors. The test PCB has a 2-layer. The schematic of the first test PCB is shown in Fig. 3.38.

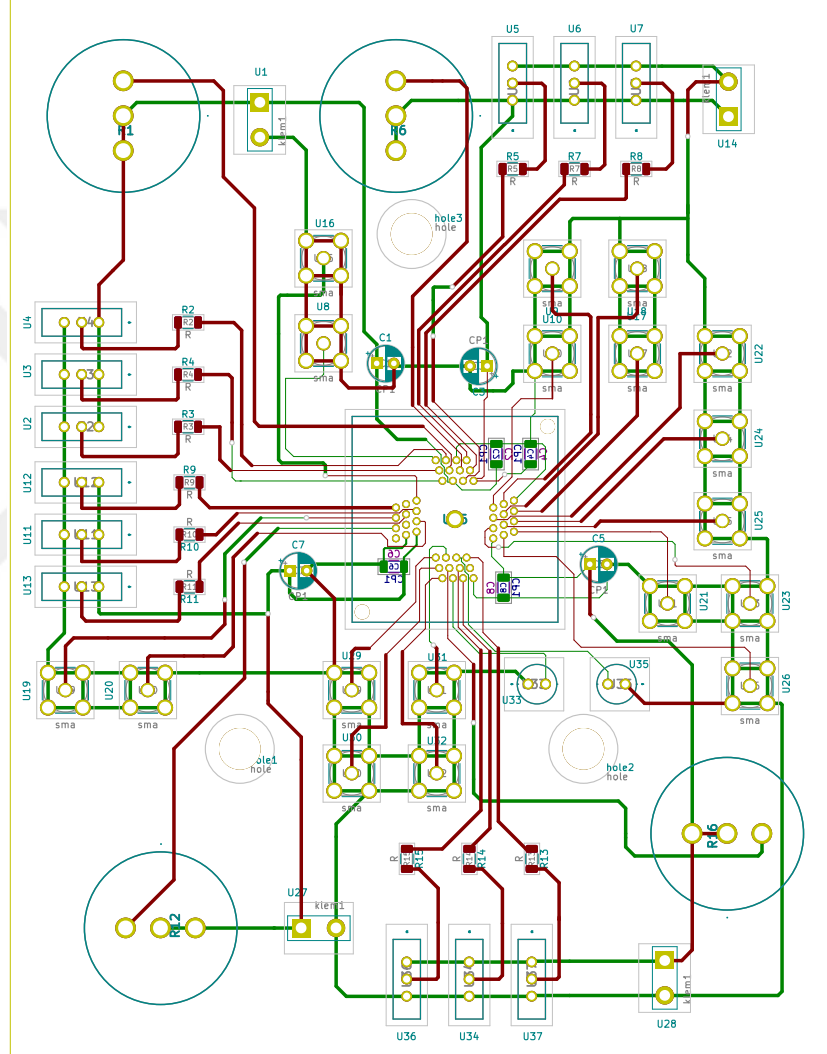


Figure 3.38: Layout of the test PCB with socket.

The socket is placed in the middle of the PCB. The implemented test PCB with a designed chip is given in Fig. 3.39.

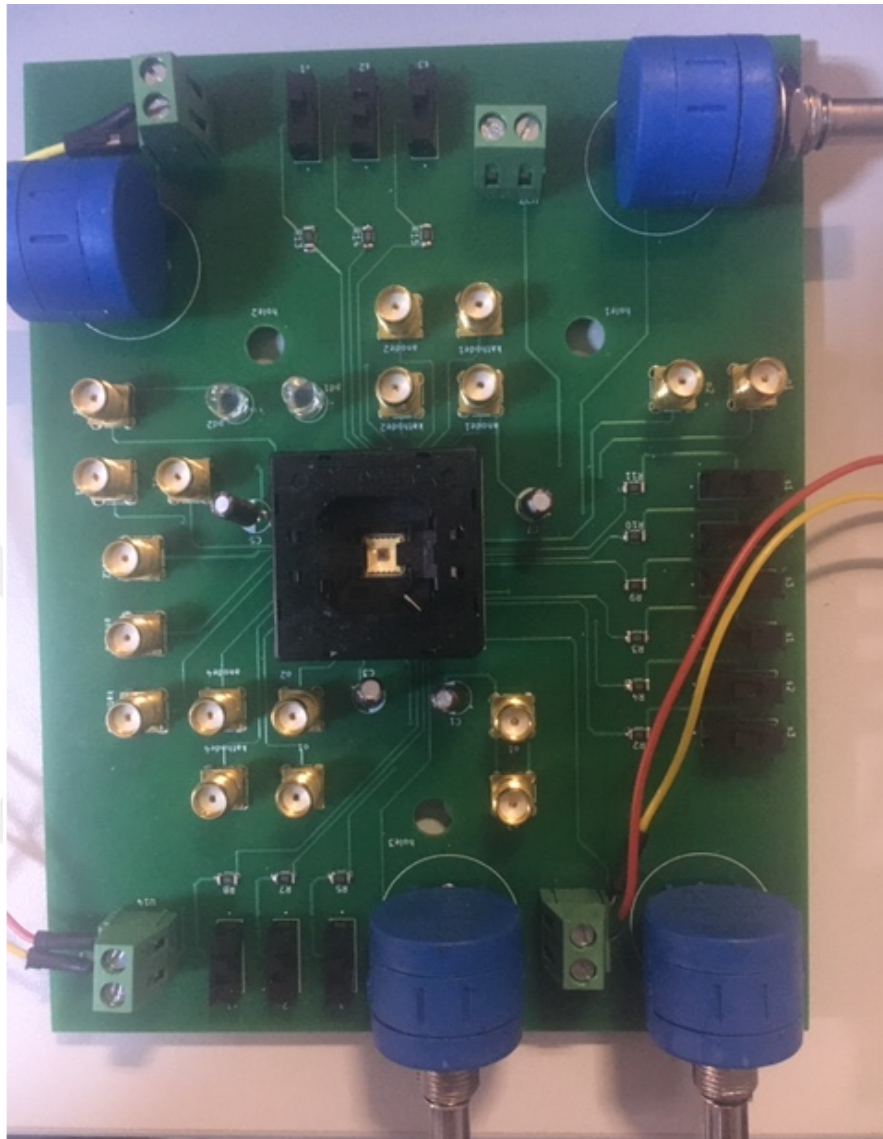


Figure 3.39: Implemented PCB with socket.

The second test PCB is the tailored version of the first test PCB and it is used for characterizing the electronic receiver block to which external commercial photodiodes are connected. In the second test PCB, the socket is not employed and thus the chip is directly soldered onto the PCB. The schematic of the second test PCB is presented in Fig. 3.40.

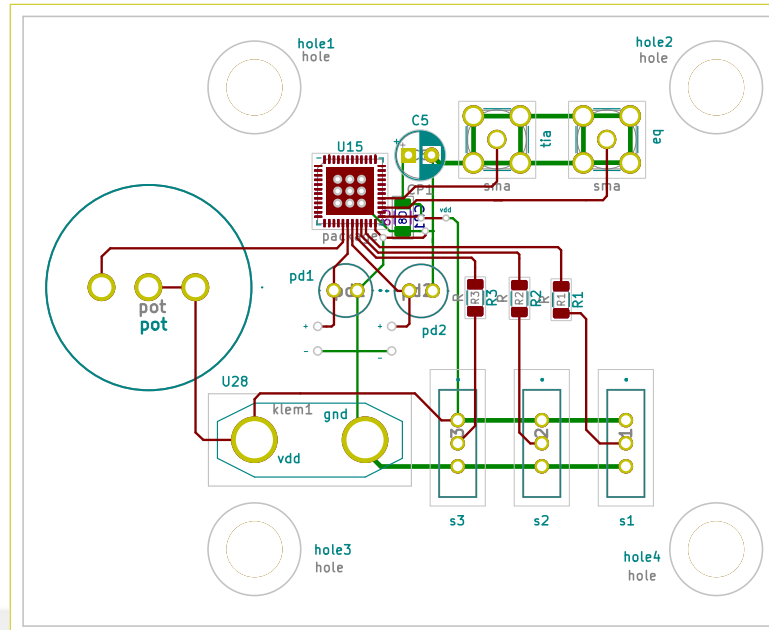


Figure 3.40: Layout of the test PCB without socket.

The second test PCB is shown in Fig. 3.41. The chip package is seen with a lid, blocking the light, since external photodiodes are utilized during the chip characterization.

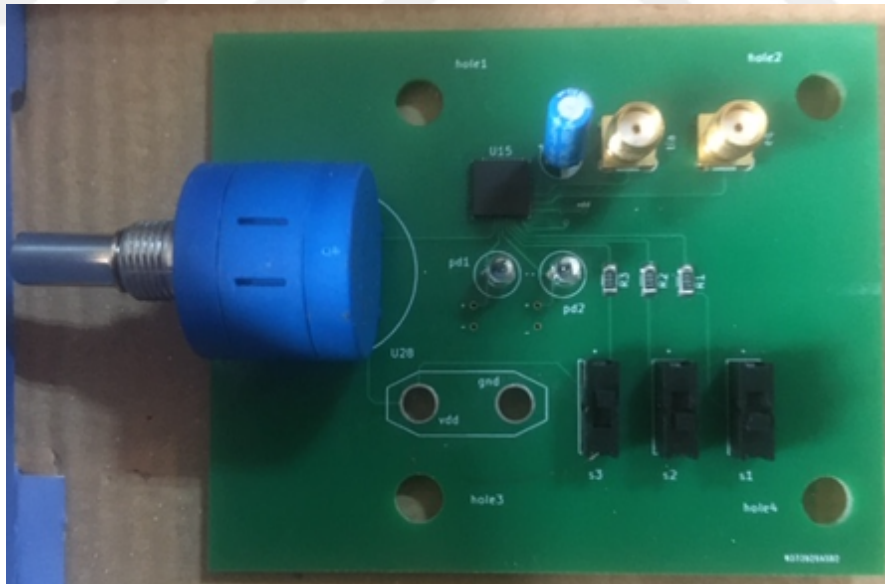


Figure 3.41: Implemented PCB without socket.

The micrograph of the implemented monolithic receiver is shown in Fig. 3.42, where the numbers (1-7) imply the subblocks. The size of the micrograph is $715\text{ }\mu\text{m}\times 850\text{ }\mu\text{m}$.

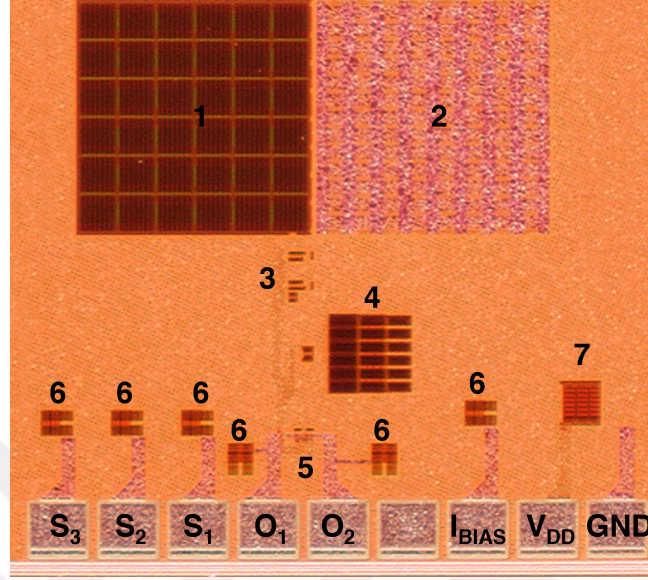


Figure 3.42: Micrograph of a monolithic optoelectronic receiver. (1) Active Photodiode (2) Dummy Photodiode (3) Transimpedance amplifier&Gain Stage (4) Continuous Time Linear Equalizer (5) Output Buffer (6) ESD Diodes (7) CLAMP Diodes.

S_1 , S_2 , and S_3 are used to control switches in CTLE. I_{BIAS} represents the pad to bias the circuit. V_{DD} and GND are supply voltage and ground, respectively. O_1 and O_2 refer to the differential outputs.

CHAPTER IV

MEASUREMENT RESULTS

In this chapter, the experimental setup together with the used equipment is introduced first. Then, the implemented chip is characterized and it is integrated with three different phosphorescent white LEDs for data transmission. For the data transmission, the eye diagrams and BER measurement results are presented. Last, the fabricated CMOS photodiodes with different areas are characterized.

The electronic receiver with an external photodiode is tested initially to check out that the electronic blocks are operating properly, since using the external photodiode is less risky than the on-chip photodiodes in the first step. The experimental setup, where the electronic receiver with an external photodiode is tested, is shown in Fig. 4.1.

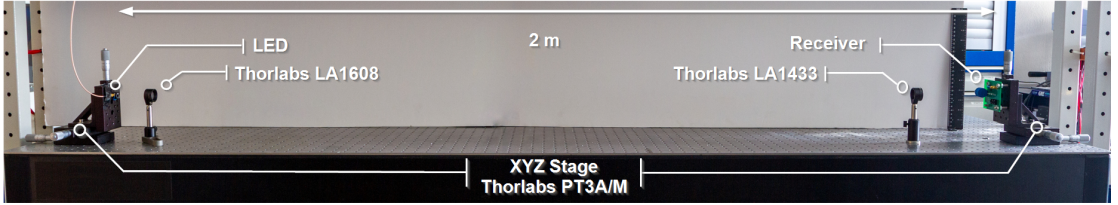


Figure 4.1: Experimental setup for the electronic receiver with an external photodiode.

The fabricated CMOS chip on a test PCB is placed at the receiver side. A longer distance between the LED and receiver (chip) is achieved using the lenses of Thorlabs LA1608 [107] and Thorlabs 1433 [108], providing collimating and focusing the light, respectively. Micrometers (Thorlabs PT3A/M [109]) placed on the transmitter and receiver side are utilized for alignment. The lenses and micrometers are mounted on the optical table. The distance between the transmitter and the receiver is 2 meters.

4.1 Electrical Characterization

To extract the frequency response of the CTLE properly, an LED with higher bandwidth is required, since the measured frequency response is dominated by an LED with lower bandwidth. Therefore, a red LED with a bandwidth of 20 MHz is employed and the change in magnitude is obtained using the signal analyzer [71], while the frequency of the AC signal applied to the red LED is swept. For each switch state, the CTLE's frequency response is extracted, which is shown in Fig. 4.2.

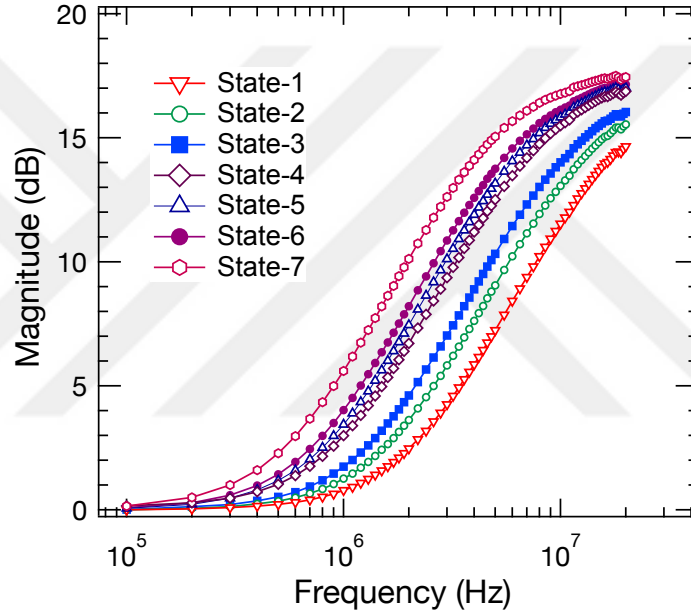


Figure 4.2: The measured frequency response of the proposed equalizer at different switch states.

As seen in Fig. 4.2, the zero frequency generated by CTLE is shifted depending on switch states and the equalizer characteristic is obtained.

4.2 Data Transmission

Data transmission is performed for the electronic receiver with an external photodiode and monolithic optoelectronic receiver, respectively. For both of them, the arbitrary data pattern is generated by Arbexpress [110] software, which controls the signal generator [111]. Thereby, the employed LEDs transmit arbitrary data pattern.

The eye diagram shows the data transmission quality and it is obtained by overlaying bits on top of each other. To monitor the eye diagram, a digital oscilloscope [112] is used. To observe the difference between without and with CTLE, data rates of 5 Mbps and 30 Mbps from the TIA's output are received first. Figs. 4.3 (a-b) show that an eye with higher clearance is obtained at 5 Mbps, whereas the eye diagram is closed at a data rate of 30 Mbps, since the received data is severely distorted, which is associated with the intersymbol interference (ISI). Then, the equalizer is activated and the buffer output is monitored at a data rate of 30 Mbps, which is shown in Fig. 4.3 (c). A clear eye-opening is obtained, since the equalizer compensated the LED's frequency response. Moreover, the blue filter is employed and a clear eye diagram is monitored (Fig.4.3 d) at a higher data rate (45 Mbps), which results from further equalization imposed by a blue filter.

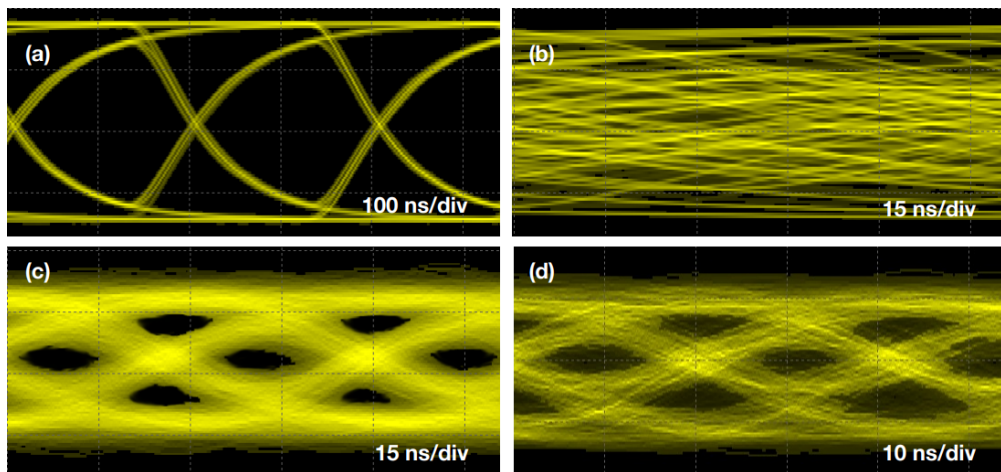


Figure 4.3: Eye diagram results of electronic receiver with an external photodiode for LED-A a) 5 Mbps-TIA output, b) 30 Mbps-TIA output, c) 30 Mbps-buffer output, d) 45 Mbps-buffer output with the blue filter.

To assess the BER performance of the VLC system, an arbitrary binary data pattern, consisting of 10^5 bits, is generated to drive the LEDs, and then the received data are processed by calculating the bit energy to detect the symbols. For LED-A, LED-B, and LED-C, BER at different data rates is measured without and with the blue filter. The BER results are presented in Fig. 4.4, where a BER of 10^{-2} is achieved at a data rate of 32 Mbps, 22 Mbps, and 18 Mbps at a distance of 2 meters for LED-A, LED-B, and LED-C, respectively. For each LED sample, around a 20 times improvement is achieved in data rate compared to the LED's bandwidth. By using a blue filter, a further increase in data rate is obtained and a data rate of 50 Mbps, 49 Mbps, and 24 Mbps resulted in a BER of 10^{-2} for LED-A, LED-B, and LED-C, respectively.

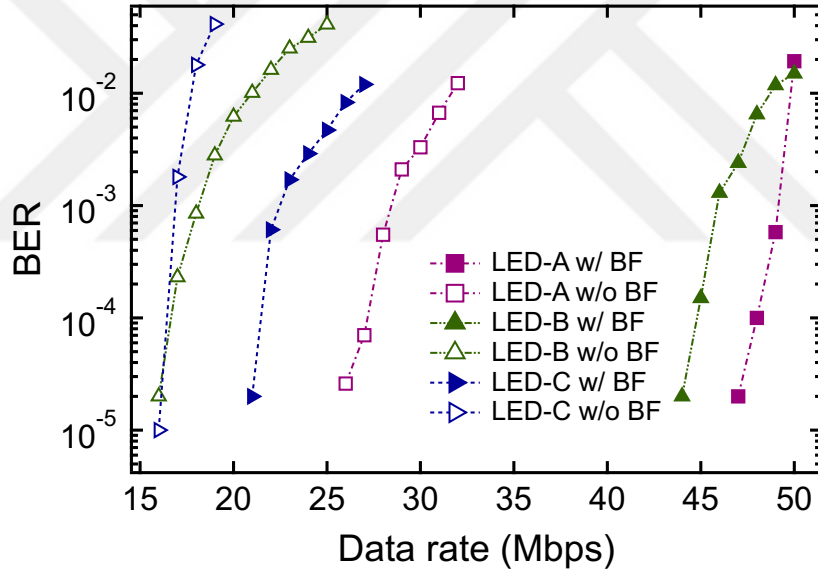


Figure 4.4: Measured BER results using an electronic receiver with an external photodiode for different phosphorescent white LEDs w/o and w/ blue filter.

After the electronic receiver with an external photodiode is tested, it is seen that electronic receiver is operating properly. Following, the monolithic optoelectronic receiver is tested. The experimental setup for the test is shown in Fig. 4.5.

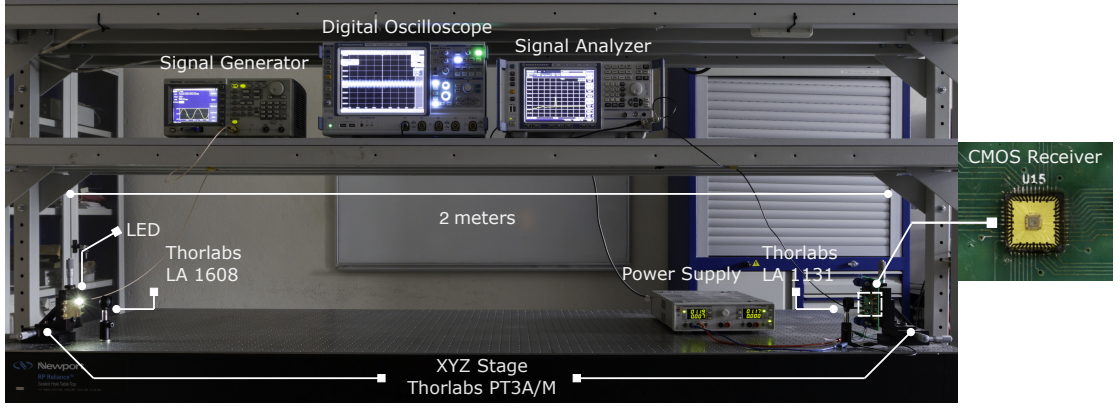


Figure 4.5: Experimental setup for a monolithic optoelectronic receiver.

Since the size of the CMOS photodiode is much smaller than the used external photodiode, the monolithic optoelectronic receiver is more sensitive to the alignment. In this setup, LED-A [87], LED-B [88], and LED-D [113] are utilized as a light source. To observe the effect of the equalization, LED's frequency responses and the equalized channel responses are presented in Fig. 4.6.

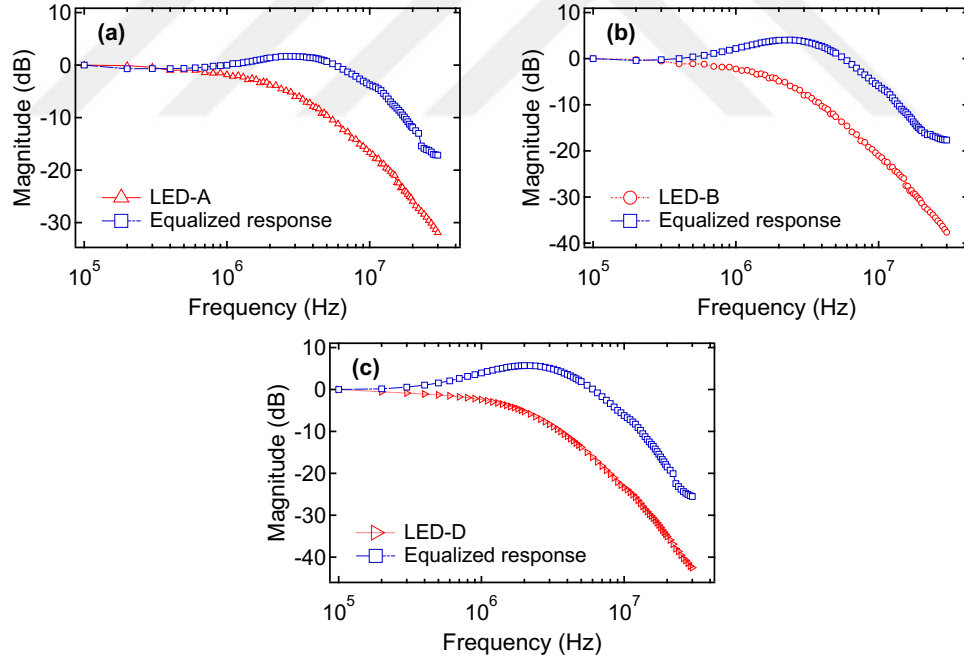


Figure 4.6: LED's and equalized channel frequency responses (a) LED-A, (b) LED-B, (c) LED-D.

As shown in Fig. 4.6, the channel responses are equalized due to the CTLE and for each of the employed LEDs around 18 dB improvement within 20 MHz is achieved for the frequency response.

Data rates of 3 Mbps and 25 Mbps are received from the buffer output, while the equalizer is not activated. Figs. 4.7 (a-b) shows that an eye with higher clearance is obtained at 3 Mbps, whereas the eye diagram is closed at a data rate of 25 Mbps. Then, the equalizer is activated and the output is monitored at a data rate of 25 Mbps and 30 Mbps (Fig. 4.7 (c) and Fig. 4.7 (d)), where clear eye-opening is obtained.

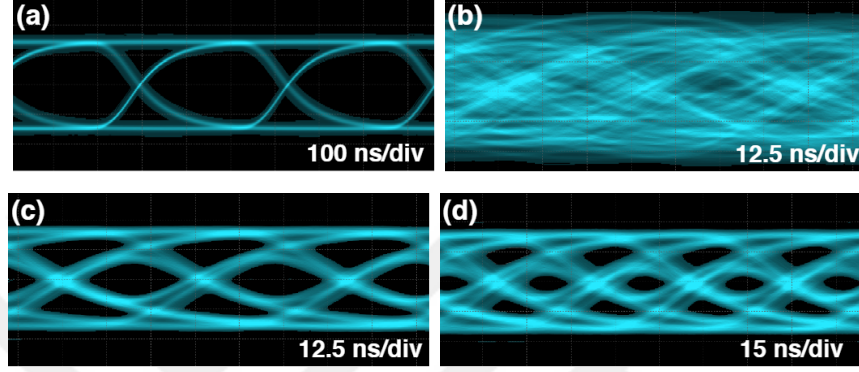


Figure 4.7: Eye diagram results of a monolithic optoelectronic receiver. a) 3 Mbps-w/o eq., b) 25 Mbps-w/o eq., c) 25 Mbps-w/ eq., d) 30 Mbps-w/ eq.

The BER results are presented in Fig. 4.8. A BER of 10^{-2} is achieved at a data rate of 32 Mbps, 23 Mbps, and 20 Mbps at a distance of 2 meters for LED-A, LED-B, and LED-D, respectively. For each of the employed LEDs, around a 20 times improvement is achieved in data rate compared to the LED's bandwidth.

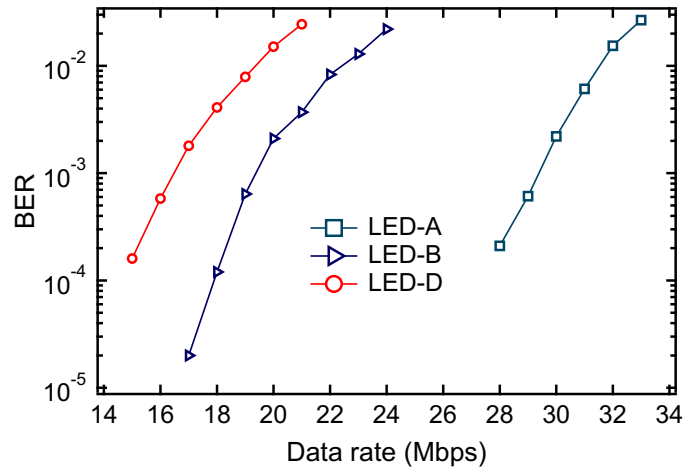


Figure 4.8: Measured BER results using a monolithic optoelectronic receiver for different phosphorescent white LEDs.

4.3 CMOS Photodiode Characterization

The implemented chip also includes separate CMOS photodiodes with the areas of $100\text{ }\mu\text{m}\times 100\text{ }\mu\text{m}$, $200\text{ }\mu\text{m}\times 200\text{ }\mu\text{m}$, and $300\text{ }\mu\text{m}\times 300\text{ }\mu\text{m}$. These CMOS photodiodes are based on the n-well/p-sub structure. First, the capacitance variation over the applied bias voltage is measured. Second, the current variation over the applied bias voltage is measured for different optical powers, which is used to derive the responsivity of the photodiode. In both measurement, Keithley 4200-SCS Semiconductor Characterization System [63] is utilized.

For the capacitance measurement, there are four terminals: High Current (HCUR), Low Current (LCUR), High Potential (HPOT), and Low Potential (LPOT). The device (Keithley 4200-SCS) provides DC and AC voltage simultaneously. DC voltage is swept in time while AC voltage is constant. Under this configuration, the current is measured and it is integrated over time to obtain the change in charge. Then, the capacitance is derived. The setup for the capacitance measurement is presented in Fig. 4.9.

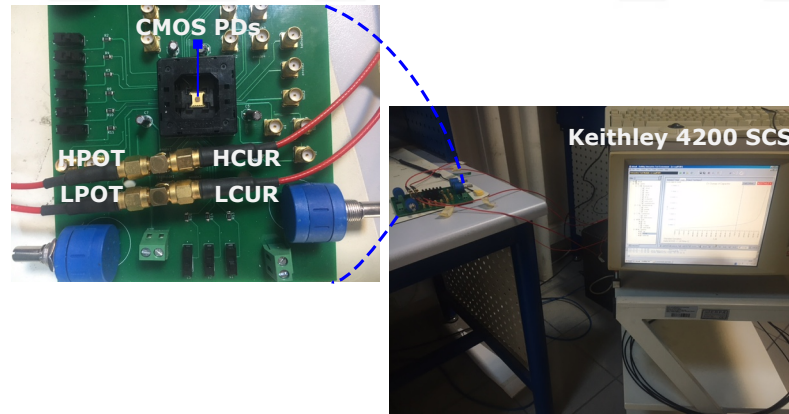


Figure 4.9: Setup for the capacitance measurement of the CMOS photodiode.

HPOT-HCUR and LPOT-LCUR terminals are combined via tee adapter as shown in Fig. 4.9 and they are connected to the anode and cathode side of the photodiode, respectively. The measured capacitances of the photodiodes with the areas of $100\text{ }\mu\text{m}\times 100\text{ }\mu\text{m}$, $200\text{ }\mu\text{m}\times 200\text{ }\mu\text{m}$, and $300\text{ }\mu\text{m}\times 300\text{ }\mu\text{m}$ are presented in Fig. 4.10. In addition, they are compared with the capacitance estimated by the model in Eq. (3.8).

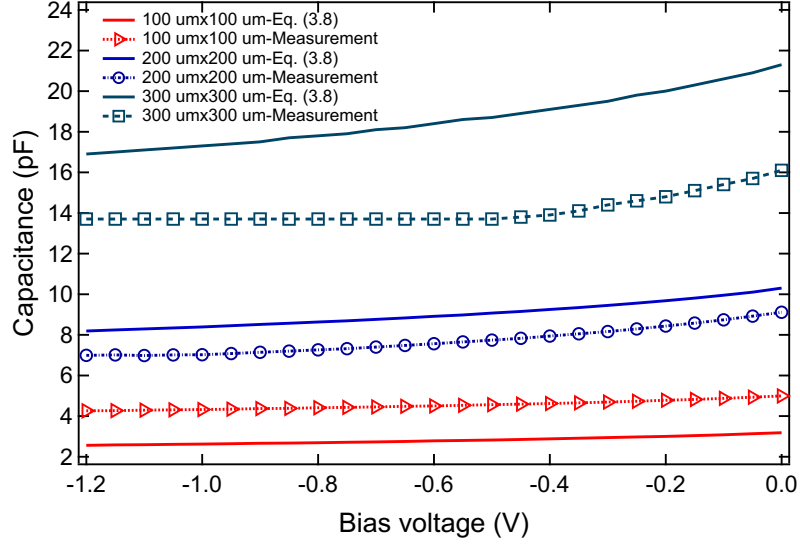


Figure 4.10: Capacitance-voltage characteristics of CMOS photodiode with different areas

The model in Eq. (3.8) is provided by UMC and it is suitable for the diode. During the photodiode design, there is not any model for the photodiode and therefore Eq. (3.8) is applied for the capacitance estimation. The difference between the measurement and model is 1.7 pF, 1.2 pF, and 4.52 pF in average for the photodiodes with the areas of $100 \mu\text{m} \times 100 \mu\text{m}$, $200 \mu\text{m} \times 200 \mu\text{m}$, and $300 \mu\text{m} \times 300 \mu\text{m}$, respectively. This indicates that using the model in Eq. (3.8) provides an approximation accuracy between 60-88 %.

The setup for achieving the current-voltage measurements for the CMOS photodiode is presented in Fig. 4.11. Since the output power can be easily adjusted, a laser diode at 660 nm is utilized as a light source. LA1027 and LA1608 are used to collimate and focus the laser beam, respectively. The photodiode is aligned by the PT3A/M to accurately excite. The anode and cathode terminals of the photodiode are connected to the Keithley 4200 SCS and thereby the current-voltage characteristics at different optical powers are obtained. Furthermore, Thorlabs camera and LB1911 are employed to monitor the laser beam on the chip. The tested CMOS photodiode has an area of $300 \mu\text{m} \times 300 \mu\text{m}$.

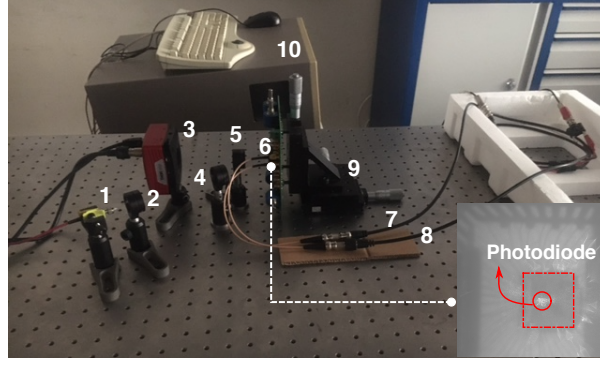


Figure 4.11: Setup for measuring the CMOS PD's responsivity. (1) Cube Laser Diode (2) LA1027 (3) Thorlabs Camera (4) LA1608 (5) LB1911 (6) CMOS PD (7) Anode Terminal (8) Cathode Terminal (9) Thorlabs PT3A/M (10) Keithley 4200 SCS.

Since the laser output power and incident power on the photodiode are different, the optical power meter (Thorlabs PM100A [114]) is used to detect the incident power at 660 nm. The current-voltage characteristic at different powers in linear scale is presented in Fig. 4.12. The power values in Fig. 4.12 refer to the incident powers on the photodiode.

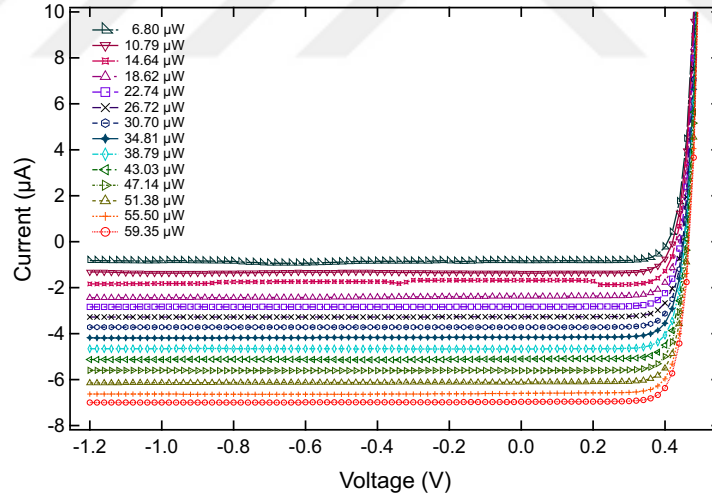


Figure 4.12: Current-voltage characteristics of the CMOS photodiode at different powers (linear scale).

As shown in Fig. 4.12, the measured current is increased, as the incident power on the photodiode increases. This indicates that the more electron-hole pairs are generated with increasing power, resulting in a higher current. In the reverse bias, the current is constant and it increases exponentially due to the charge diffusion in forward bias. The open-circuit voltage (V_{oc}) is around 0.46 Volt.

In Fig. 4.13, the current-voltage characteristics of the CMOS photodiode at different powers are presented in a logarithmic scale with the absolute value of the current.

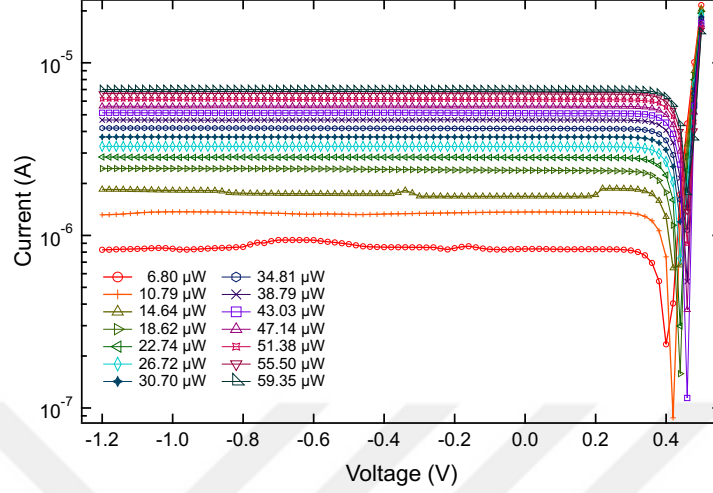


Figure 4.13: Current-voltage characteristics of the CMOS photodiode at different powers (logarithmic scale).

Based on the extracted current-voltage characteristics, the responsivity of the photodiode at 660 nm can be derived. As given in Eq. (3.6), the responsivity is the relation of the current to the optical power. For the current, the short circuit current (I_{sc}) is used due to linearity. On the other hand, the incident power measured on the photodiode is associated with the reflection at the chip surface and the photodiode's fill factor. The reflection takes place between air and silicon (chip) due to the refractive index difference. The refractive index of air and silicon is 1 and 3.48, respectively. In line with Fresnel's formula, around 30 % of the power is reflected from the photodiode's surface. In addition, the metal contacts on the photodiode reflect the light totally. Therefore, the fill factor of 67.5 % is taken into account for the responsivity calculation, which is given as

$$Responsivity = \frac{I_{sc}}{Fill\ Factor (1 - R) P_i}, \quad (4.1)$$

where R and P_i denote the reflectivity from the chip's surface and the incident optical power, respectively. According to the Eq. (4.1), the responsivity is 0.25 A/W at 660 nm.

CHAPTER V

CONCLUSION

In Chapter 2, we investigated the frequency response of LEDs. In the literature, there are some studies, in which the measured frequency response of LED has a misleading characteristic, which is in contradiction with the inherent LED's response. It is observed that this contradiction results from the measurement technique, where external components such as bias-tee and amplifier are employed, and their own frequency responses appear in the measurement. Therefore, without using any external components the frequency responses of several off-the-shelf LEDs are measured. Then, the measured frequency responses are compared with the transfer function derived from the small-signal equivalent circuit model of the LED. The compliance between the measurement results and the transfer function is obtained. On the other hand, there are some models such as first-order or Gaussian low-pass filter for the LED's frequency response, which have been proposed in the literature. For the phosphorescent white LEDs, we proposed a new frequency response model, which has a zero and two poles. It is seen that up to higher frequencies the proposed model exhibits better compliance with the measurement in comparison to the other models. A digital equalizer is designed in line with the proposed LED model and therewith a BER of around 10^{-3} is achieved at a distance of 2 meters for the phosphorescent white LED with a bandwidth of 1.5 MHz, resulting 150 times improvement in data rate in comparison to the LED's original bandwidth.

In Chapter 3, we designed a monolithic optoelectronic receiver using 130 nm CMOS technology for VLC. The designed receiver includes a dummy and active photodiode with the areas of $300\text{ }\mu\text{m}\times 300\text{ }\mu\text{m}$ that are based on n-well/p-sub

structure. Following the photodiode, a TIA, a CTLE, and output buffer are designed. Furthermore, ESD and CLAMP diodes are designed to protect the chip from higher voltage. The designed blocks are laid out and the tape-out is provided for the fabrication.

In Chapter 4, the fabricated receiver is tested in an experimental VLC setup. There are two different receivers and they are an electronic receiver with an external photodiode and a monolithic optoelectronic receiver. For each of them, the measurements are performed. For the electronic receiver with an external photodiode, three different phosphorescent white LEDs are employed separately and the data transmission is achieved at a distance of 2 meters using without and with blue filter. As an example, using a LED with a bandwidth of 1.6 MHz, a BER of 10^{-2} at a data rate of 32 Mbps is achieved. In addition, using a blue filter, the data rate is further increased to 50 Mbps. For each of the employed LEDs, around 20 times improvement in the data rate in comparison to the LED bandwidth is obtained. For the monolithic optoelectronic receiver, three different phosphorescent white LEDs are employed separately without using a blue filter. Using a LED with a bandwidth of 1.6 MHz, a BER of 10^{-2} at a data rate of 32 Mbps is achieved at a distance of 2 meters, and around a 20 times improvement in the data rate in comparison to the LED bandwidth is obtained for each of employed LEDs. This indicates that the monolithic optoelectronic receiver exhibits a similar performance as the electronic receiver with an external photodiode, even though a lower output signal is received due to the photodiode's area and responsivity. The implementation of a monolithic optoelectronic receiver in 130 nm CMOS technology is achieved successfully. This receiver can be integrated with the LEDs of different bandwidths and performs the equalization for them, resulting in reaching higher data rates. Table 5 presents the comparison between receivers achieved in this work and the related works in the literature.

Table 5: Performance comparison

	ISCAS 2016 [57]	JLT 2016 [58]	JLT 2018 [62]	This Work [115]	This Work
Light Source	Red Laser Diode	Red Laser Diode	Phosphorescent White LED Array	Phosphorescent White LED	Phosphorescent White LED
Light Source Bandwidth (MHz)	5×10^3	5×10^3	2.2	1.6	1.6
TX Power Consumption (W)	0.33	0.33	1	0.078	0.078
TX Lens focal length (mm)	26	40	-	75	75
TX Lens diameter (mm)	30	50	-	25.4	25.4
RX Lens focal length (mm)	40	40	100	150	50
RX Lens diameter (mm)	50	50	50	25.4	25.4
Photodiode	Integrated	Integrated	Discrete	Discrete	Integrated
Equalization for	Photodiode	Photodiode	LED	LED	LED
RX power consumption (mW)	215	215	2.2	2.4	2.05
CMOS Process (nm)	350	350	180	130	130
Supply Voltage (V)	3.3	3.3	1.8	1.2	1.2
Circuit area (mm²)	0.8	0.8	0.28	0.21	0.6
Distance (m)	0.46	12	2.7	2	2
Modulation Format	OOK				
Achieved Data Rate (Mb/s)	1.8×10^3	2.5×10^3	30	32	32
BER	5×10^{-5}	1×10^{-3}	1×10^{-2}	1×10^{-2}	1×10^{-2}

In addition to the implementation of an electronic receiver with an external photodiode and a monolithic optoelectronic receiver, CMOS photodiodes with the areas of $100\ \mu\text{m} \times 100\ \mu\text{m}$, $200\ \mu\text{m} \times 200\ \mu\text{m}$, and $300\ \mu\text{m} \times 300\ \mu\text{m}$ are implemented. CMOS photodiodes are characterized by achieving the capacitance-voltage and current-voltage measurements. Since the physical models are not available for the photodiodes, their capacitances are estimated relying on the model given in Eq. (3.8). It is obtained that the related model has an approximation accuracy of 60-88 %. This comparison provides a reference for the designers related to the n-well/p-sub based photodiode implementation in 130 nm technology. Furthermore, the current-voltage characteristics at different optical powers are obtained for a photodiode with an area of $300\ \mu\text{m} \times 300\ \mu\text{m}$ and the responsivity of 0.25 A/W is derived at 660 nm. Being as an integrated photodiode, it has around 7-8 times smaller area and a similar responsivity in comparison to the commercial photodiodes.

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