A DIGITALLY CONTROLLED CLASS-E AMPLIFIER FOR MRI

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR
THE DEGREE OF
MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

By
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August, 2016

A Digitally Controlled Class-E amplifier For MRI
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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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Radio-frequency (RF), or B_1 field is used for slice selection purposes in Magnetic Resonance Imaging (MRI). In an MRI scanner this field is handled by the RF chain which consists on a pulse generator unit, a high power amplifier and a transmit coil. Relatively low efficiency linear power amplifiers are used. These amplifiers are placed in the system room, far from the transmit coil.

In this work we propose to design the amplifier and the coil as a single unit, aiming to decrease cost and complexity while improving performance. Splitting the coil into multiple elements makes possible to drive these elements with individual amplifiers in Transmit Array (TxArray) mode. Also these elements are integrated as the load network of the amplifier, in this case a high efficiency Class-E amplifier.

The Class-E amplifier was modified for the intended application and it was digitally controlled. For the pulse generation two different methods were applied. One was by controlling separately the phase and amplitude of the pulse. The other method generates simultaneously phase and amplitude by controlling the switching pattern of the amplifier. An amplifier of output power 100W with efficiency up to 88% was developed. As a step toward 36 channel complete system, 2 element prototype's operation was tested in a 3T Tim Trio Siemens scanner. In overall, Class-E amplifier is shown to be a promising candidate for on-coil RF excitation in TxArray in terms of size, cost, efficiency and complexity.

Keywords: RF field, Class-E amplifier, Digital control, Parallel Transmission.

ÖZET

MRG CİHAZLARI İÇİN TASARLANMIŞ SAYISAL KONTROLLÜ GÜÇ YÜKSELTECİ

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Elektrik ve Elektronik Mühendisliği, Yüksek Lisans
Tez Danışmanı: Ergin Atalar
Ağustos, 2016

Radyo-frekans (RF) ya da B_1 alanı, Manyetik Rezonans Görüntüleme (MRG) alanında kesit belirleme amacıyla kullanılmaktadır. MRG tarayıcılarında bu alan, RF zincirini oluşturan darbe üretecisi, yüksek güç yükselticisi ve verici sargıları tarafından oluşturulmaktadır. Günümüzdeki MRG cihazlarında düşük verimli doğrusal güç yükselticileri kullanılmaktadır. Genellikle bu yükselticiler verici sargıdan uzakta, sistem odasına yerleştirilir.

Bu tezde, yükselticiyi sargıyla birleştirilerek var olan tasarımını daha düşük maliyetli, daha az karmaşık ve daha iyi performans veren bir tasarım haline getirmek hedeflenmiştir. Sargıyı birden fazla elemana ayırmak, bu elemanların her birinin paralel iletim yöntemiyle farklı yükselticiler tarafından sürülmesine olanak sağlamaktadır. Ayrıca bu elemanlar yüksek verimliliğe sahip E-sınıfı yükselticilerin yük ağları ile bütünleştirilmiştir.

E-sınıfı yükselticiler, hedeflenen uygulama için adapte edildi ve sayısal olarak kontrol edildi. Darbe üretimi için iki farklı yöntem uygulanmıştır. Ilk yöntem faz ve genlik ayrı ayrı kontrol edilmektedir. Diğer yöntemde ise yükselticinin anahtarlama düzenini kontrol ederek faz ve genlik aynı anda kontrol edilir. Çıkış gücü 100W ve %88'e kadar verim ile çalışan yükseltici geliştirilmiştir. 36 kanallı bir sisteme yönelik adım olarak, 2 elemanlı sistem 3T Tim Trio Siemens tarayıcı kullanılarak test edilmiştir. Özet olarak, E-sınıfı yükselticilerin paralel iletim yöntemi ile RF uyarımı konusunda boyut, maliyet, verimlilik ve karmaşıklık açısından gelecek vaat eden bir sistem olduğu gösterilmiştir.

Anahtar sözcükler: RF alanı, E-sınıfı yükseltici, Sayısal kontrol, Paralel İletim .

Acknowledgement

Foremost, I would like to express my deepest gratitude to my advisor Prof. Dr. Ergin Atalar for his guidance, patience and motivation. Also I appreciate Assoc. Prof. Dr. Emine Ülkü Sarıtaş and Prof. Dr. Haluk Külah for being my jury members.

Besides that, I acknowledge my gratitude to Berk Silemek, Taner Demir and Umut Gündoğdu for their direct contribution in this work. This study was part of a project with ASELSAN A.Ş, from which Bülent Şen and Gökhan Cansız with their team have helped a lot with prolific discussion and collaboration.

Additionally I am also thankful to all of the other UMRAM members for providing a warm, friendly and a good research environment. To conclude, as in all times, family has been an important support and source of motivation.

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Chapter 1

Introduction

In Magnetic Resonance Imaging (MRI) scanners radio-frequency (RF) chain is an important system building block used to handle B_1 field required in imaging. The duty of this block is to generate the appropriate pulse, amplify at a required level and apply to the body under examination. Implementation of the RF chain consists on: a pulse generation unit, a high power amplifier and a transmit coil.

In commercial scanners typically these amplifiers are linear amplifiers with relatively low efficiency. The need for a cooling system results in a bulky device placed in the system room, far from the transmit coil inside the scanner. In overall, the system becomes more complex and also due to the distance between coil and amplifier, efficiency decreases further more while the overall cost of the system increases.

As for the transmit coils, birdcage coil [1] has been widely used due to its homogeneity and high transmit efficiency. However, in higher field strengths (>3T) birdcage coils field homogeneity performance degrades. Multichannel transmit systems are proposed in several studies as alternatives for current systems. Katcher [2] summarizes several advantages that are inherent from the degree of freedom introduced when multliple elements are controlled independently as a Transmit Array (TxArray). One of them is the improved B_1 uniformity in

high fields [3–6]. At the same time multiple independent coils present a freedom for local area excitation, shimming and increase in speed [7–9]. In addition to that parallel transmission is shown to be beneficial in reduction of specific absorption rate (SAR) [10–12]. By applying RF power only to local areas or volumes of interest the overall SAR given to the patient may be decreased. Although initially TxArray was thought as a solution to high field inhomogenity problem, it has applications beyond that and it can be useful in lower fields. Our research group (UMRAM) is working on exploiting pTx on 1.5T and 3T fields. Eryaman's work [13] in which RF heating due to an implant was reduced by controlling the electric field is an example of a potential application. More degrees of freedom may be used for a more flexible control of the electric field.

Some studies have been performed on implementing a TxArray system. A complete 8 channel Tx/Rx system was integrated by Graesslin et al. [14] in a 3T Philips scanner. Several novel designs have been proposed using switching on-coil amplifiers [15, 16]. Gudino's design is based on a current-mode Class-D switching amplifiers which drives individually 4 coils for RF excitation at 1.5T. In this case current mode switching amplifiers do not need extra decoupling circuitry and they are load independent. In addition to that, these kind of amplifiers can be designed at high efficiency performance.

Even though parallel transmit array has shown improvement in some aspects, when it comes to implementation, it poses some difficulties. First, is related to the number of elements. As the number of elements increases, the systems becomes more complex. Cabling becomes an issue because control signals and power lines have to be adapted for multiple amplifiers. Another concern that has to be dealt with is the coupling. Dominant one is the coupling between adjacent coils. Coupling between coils may have imaging effects because magnetic field is applied in undesired regions. Additionally it decreases the overall efficiency of the systems and may damage amplifiers.

By considering the previous work on RF chain it can be observed that mainly the studies are focused on developing separately the coil, the amplifier and pulse generation module. In this work it was proposed to integrate the whole system

as a single block and design a TxArray system with on-coil amplifiers. Since separate amplifier for each element was intended to be used, power required from a single amplifier is decreased. After consulting the several amplifier topologies, it was decided that Class-E amplifier, initially presented by Sokal and Sokal [17], is a very suitable amplifier for the intended application. From the novelty point of view, no previous applications of Class-E in a TxArray MRI system are reported. Class-E amplifier is a switching type of amplifier which includes a choke inductor, a switch and RLC load network. On the other side, one element of the coil can be modeled as an RLC network, making it possible to design the coil element as the load network of the amplifier. In this way no matching at 50 Ω was required in both coil and amplifier side. Additionally, since the amplifier was placed close to the coil, long transmission lines carrying high power RF signal were not needed. In this work we presented a 2-channel TxArray system as a step toward a 36-channel TxArray RF chain. Each element was connected to a Class-E amplifier which was digitally controlled. The system was developed for a Tim Trio 3T Siemens scanner, but can be easily adapted for lower field strengths (1.5T). As a summary of the proposed system, by integrating together the coil with high efficiency amplifiers in TxArray, it was aimed to decrease the overall cost while presenting reliable ground for improvement in performance when compared with current conventional systems performance.

Chapter 2

Theory

In this chapter the design of a Class-E amplifier as one element of a parallel transmit array for RF excitation in MRI is explained. At first, the background and design equations for conventional Class-E amplifier are presented. Next, adaptation of Class-E amplifier as an on-coil amplifier was described. This includes the specifications for target performance. Additionally integrating the coil element as the load network after considering the whole chain as a single block is presented. Meanwhile, the whole process of component selection and PCB card design was conditioned by the intended usage as on-coil amplifier, inside the bore of the scanner. In the part 2.1.2 it is shown how the Class-E amplifier was modified by replacing the RF choke inductor with a short coaxial transmission line. The theory and assumptions for which the replacement is valid are explained as well. In part 2.1.3 digitally controlled operation mode is explained. In one mode of operation, supply modulation for envelope control using a half bridge converter is introduced. A more novel method algorithm for digital modulation of Class-E amplifier was put forward. Making use of the nonlinearity of the amplifier, by controlling only the switching pattern of the amplifier, under constant drain supply voltage, both the frequency and amplitude modulation of a desired pulse generation is presented.

2.1 Class E amplifier design

2.1.1 Conventional Class E amplifier

Class-E amplifier,a switching amplifier type, can achieve 100% efficiency in the ideal case. It consists of a load network and a switch as illustrated in Fig. 2.1. In the ideal case, the voltage of the switch and its time derivative are simultaneously zero at the time of switching, resulting in no switch loss, hence all of the supply power is transferred to the load. After Sokal and Sokal's [17] first Class-E amplifier, Raab [18] and Kazimierczuk [19] further worked on deriving the design equations for nearly ideal efficiency.

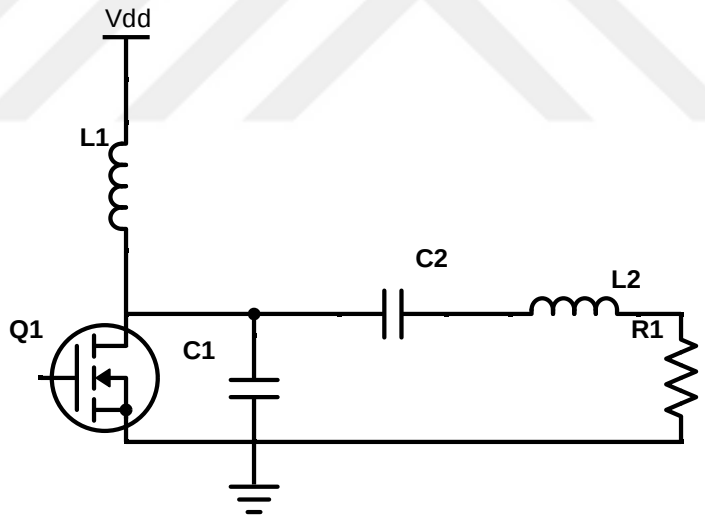


Figure 2.1: Original Class E amplifier

The inductor L1 is used instead of a current source, providing a DC current. The capacitor values C1 and C2 and inductor L1 are calculated by design equations equations Eq. 2.8-2.11. In an ideal case when lossless capacitors and inductors, ideal switch and perfectly tuned values are used, the amplifier will transform the DC power drawn from the supply into RF power delivered at load with 100% efficiency. In this case the components will not dissipate power.

As for the switch, as illustrated in Fig. 2.2 half of the period current flows through the switch, while voltage will be 0. The other half period when there

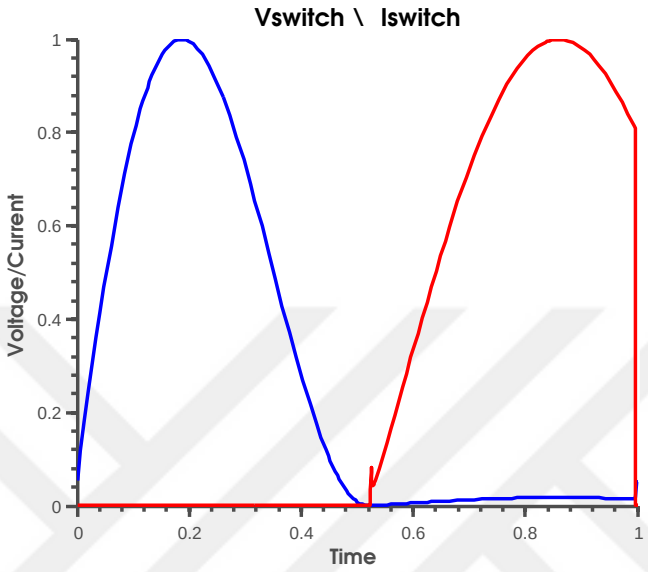


Figure 2.2: Current and voltage on the switch of and ideal Class-E amplifier

is voltage across the switch, current will be zero. The analysis of the Class-E amplifiers has been studied in several works. A very well defined analyses and design equations have been developed by several authors[17–20]. As a summary we can start by solving the following equations:

$$C_1 \frac{d}{dt} V_{C1} = I_{dc}(1 - \alpha \sin(w_s t + \phi)) \tag{2.1}$$

$$V_{C1}(t) = \frac{I_{dc}}{w_s C_1}(w_s t + \alpha(cos(w_s t + \phi) - \cos(\phi))) \tag{2.2}$$

Where, w_s is the desired fundamental frequency, I_{dc} is the DC current flowing in the switch, and constants α and ϕ should be calculated. V_{C1} is the current across capacitor C_1 and the switch at the same time.

The condition for optimum efficiency Class-E amplifier should satisfy the following conditions:

$$V_{C1}(t)|_{\frac{T}{2}} = 0 \tag{2.3}$$

$$\frac{d}{dt}V_{C1}(t)|_{\frac{T}{2}} = 0 \tag{2.4}$$

After solving the equation α and ϕ are found to be:

$$\alpha \approx 1.86 \quad \phi \approx -32.5^o \tag{2.5}$$

After solving the equations, voltage in the switch can be calculated in the full period, separated in two cases: for switch-on and switch-off as shown below:

$$V_{C1}(t) = \begin{cases} \frac{I_{dc}}{w_s C_1}(w_s t + \alpha(cos(w_s t + \phi) - \cos(\phi))) & 0 \leq w_s t \leq \pi \\ 0 & \pi \leq w_s t \leq 2\pi \end{cases} \tag{2.6}$$

In the same way the current in the switch can be calculated:

$$I_{sw}(t) = \begin{cases} 0 & 0 \leq w_s t \leq \pi \\ I_{dc}(1 - a\sin(w_s t + \phi)) & \pi \leq w_s t \leq 2\pi \end{cases} \tag{2.7}$$

By following an analytical approach in the literature, a set of equations that can be used to design a Class-E amplifier can be summarized in the equations below:

$$R_L = \frac{V_{DD}^2}{P_{out}} 0.58(1 - \frac{0.451759}{Q_L} - \frac{0.4}{Q_L^2}) \tag{2.8}$$

$$C_2 = \frac{1}{34.2 f_o R_L}(1 + \frac{0.9}{Q_L} - \frac{1}{Q_L^2}) + \frac{0.6}{(2\pi f_o)^2 L_{ch}} \tag{2.9}$$

$$C_1 = \frac{1}{2\pi f_o R_L}\frac{1}{Q_L - 0.1}(1 + \frac{1}{QL - 1.8}) - \frac{0.2}{2\pi {f_o}^2 L_{ch}} \tag{2.10}$$

$$L = \frac{Q_L R_L}{2\pi f_o} \tag{2.11}$$

Where R_L is the load resistance, Q_L is the quality factor, P_{out} is the desired output power.

In the case of nonideal switch, the loss in the switch was analyzed by Sokal and Raab [21]. Due to the switch on resistance power loss in the switch can approximately be calculated as follows:

$$P_{RdsOn} = 1.37\frac{R_{dsON}}{R_L}P_{out} \tag{2.12}$$

In this case the maximum efficiency can be calculated as follows:

$$\eta = \frac{R_L}{R_L + 1.37R_{dsON}}100\% \tag{2.13}$$

2.1.2 Modified Class E amplifier

In the following part it is explained the Class E amplifier design for RF excitation in MRI. The amplifier designed in this work, replaces the choke inductor with a short coaxial transmission line. In this design the coil that is used for excitation serves as the load network of the amplifier as well. As for the load, R, it comes from coil loading by the body where the RF is to be applied. The amplifier is digitally controlled by an FPGA. The coil is the inductor $L2$ in Fig. 2.1 design. $C21$, $C22$, $C23$ are distributed capacitors equivalent to $C2$ in Fig. 2.1 design.

There are several expected advantages that are aimed to be achieved. First the coil element is used both for tuning as the load network of the amplifier and

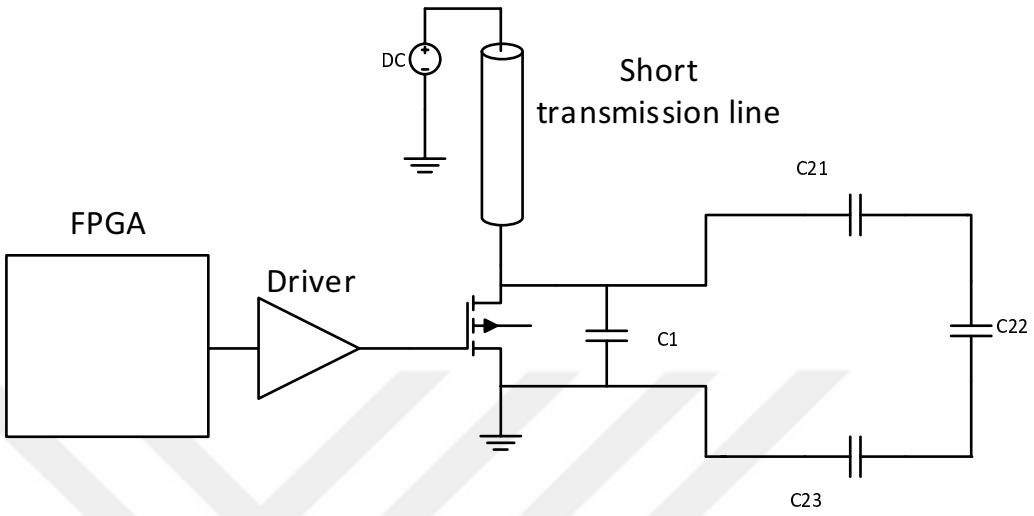


Figure 2.3: Proposed modified Class-E amplifier

for applying the RF field to the body. From hardware point of view, being on coil amplifier, brings no need for extra 50Ω matching circuitry, reducing complexity. From power losses point of view, it is more beneficial since transmission line losses are avoided.

When designing the amplifier the equations as mentioned also by Wilkinson [22] are to be taken into consideration :

$$P_o = \frac{V_{dd}^2}{1.74R} \tag{2.14}$$

Where V_{dd} is supply voltage feeding the drain and R is the load. Maximum switch voltage in this case is:

$$V_{dsmax} = 3.56V_{dd} \tag{2.15}$$

From Eq. 2.14 it can be observed that in order to increase the RF output power either V_{dd} should be increased or R should be decreased. From Eq. 2.15 we observe that there is an upper limit to V_{dd}, related to the peak voltage that

the switching transistor can withstand. On the other hand there is a lower limit to R that is related to a practical issue: the non-zero turn-on resistance of the transistor. As the turn-on resistance becomes comparable to the load resistance, part of the power will be dissipated on the transistor. Consequently the efficiency of the amplifier will decrease. In a standard system an output peak power of $\sim$10 kW is applied to the coil. For the intended 36 element array, each amplifier would need to produce around 300 W in order to achieve the same overall power. Initially a design for a target of around $100W$ output power was to be achieved for the prototype. Considering also Eq. 2.14 and Eq. 2.15 the switch selection was critical. It has to satisfy the several criteria. For example, the switch should have a low R_{dsON} when compared to R_{load} so that losses in the switch are kept minimal. Additionally, input capacitance C_{iss} of the switch should be as small as possible because driving large capacitances at high frequency at low rise and fall times is difficult. Maximum drain to source voltage that the switch can withstand (V_{dsmax}) should be large because at Class-E amplifier drain voltage can rises up to 3.56 V_{dd} level. Maximum working frequency of the switch is at least $5fo$. Last but not the least important is the cost. The switch is the component with highest cost, so price becomes a criterion too.

In several Class-E amplifiers GaN transistors are selected as switches because they have a good ratio of P_{out}/C_{iss}. However we selected BLF871 LDMOS (NXP semiconductors) because it satisfies our selection criteria and has a lower cost and a better heat dissipation performance when compared to equivalent GaN transistors.

2.1.3 Driver

The amplifier is desired to be fully digitally controlled, so a driver that receives digital input and appropriately switches on and off the transistor was to be designed. The digital signal from FPGA (ML509EVB) are sent via Low Voltage Differential Signals (LVDS) outputs for a better noise performance. The driver is designed in three stages as shown in Fig. 2.4.

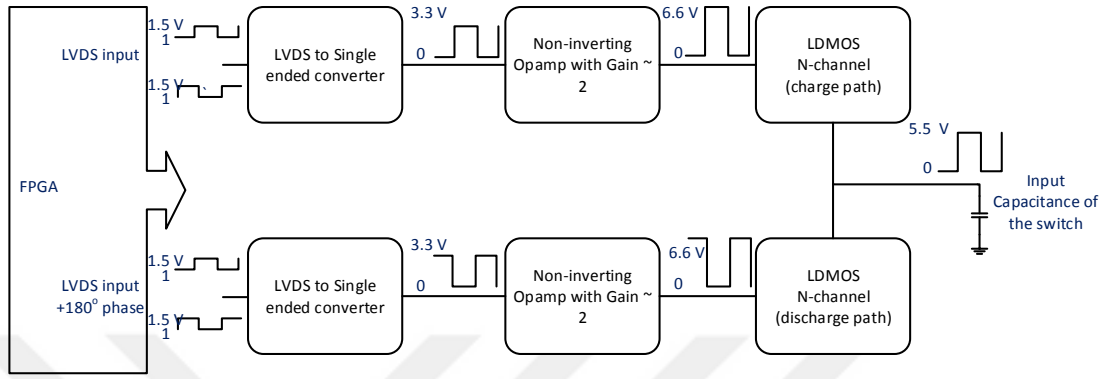


Figure 2.4: Proposed driver diagram

First stage converts the Lvds signal into single ended $0 - 3.3V$ square pulses. The second stage, implemented with non-inverting opamps, amplifies the single ended signals to $0 - 6.6V$. The last stage is needed to supply enough current to charge and discharge the gate capacitance of the switch in minimum time. Two identical signals from FPGA that have 180^o phase with each other control the high and low side of the driver. During the implementation an undesired situation is encountered: since the transistors have a non-zero switch on time during the transition there is a time interval when both transistors are on. In this case two problems are observed.First, switch losses are increased at the driver because even though for a short time, there is a low impedance path from supply to the ground. Second, rise and fall times increase because the current that is supposed to charge and discharge the gate capacitance of the main switch, has another flow path to ground.

Same topology, used in H bridges and DC-DC converters, shows the same problem. For frequency range below 30MHz H Bridge drivers which adjust a dead time are used. Additionally this driver IC provide a floating ground for the pull up switch. There are some studies on DC-DC converters at VHF (30-300Mhz) [23], which includes the desired operation frequency case. In this study a resonant circuits driver is used due to high speed switching times.

For our driver design the deadtime was generated at the FPGA. Pull up and

pull down signals were changed to a duty cycle 40 % and with phase 180^o between the high and low side switches, avoiding switches to be on at the same time. Instead of adding a more complex circuitry, the task was shifted in the control part, as a better solution. The signals generation wasdone as in the following diagram:

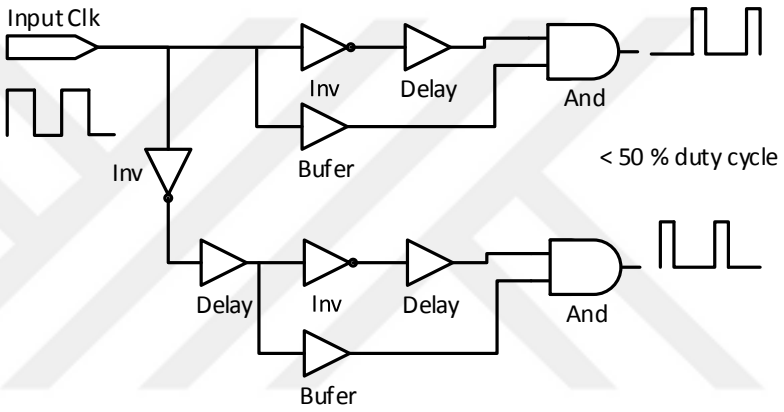


Figure 2.5: Non-overlaping signal generation in FPGA

Tap delay lines are used to arrange the delay such that the signals are less than 50% duty cycles. Similarly, those delay lines are used to perfectly arrange 180^o phase between high and low signals. Initially the rise and fall time of the opamp output signals was measured. After that the duty cycle of the LVDS signals generated in FPGA was arranged. The duty cycle is arranged at such a value that it provides enough time to the last stage transistors to switch on or off in different times. External buttons were used to manually control the delay and arrange the alignment of the signals.

2.2 Using a transmission line in place of the choke inductor in a Class-E amplifier

In the initial presented Class-E amplifier, there is an ideal current source used, often implemented with a choke inductor. In MRI any extra magnetic field inside the bore would lead altering the homogeneity of the magnetic field. Any other source of magnetic field is totally undesired or should be minimized. Consequently, the magnetic field which is produced in the inductor may bring undesired imaging effects. In our case, a coaxial transmission line is used. It has the characteristic of keeping the magnetic and electric fields between its inner and the outer conductor makes it a good candidate for our purpose.

If instead of an ideal current source a large inductor is used as RF choke, the current pulled from the choke will consist on a DC current with small AC ripple additionally. Depending on the value of the inductor the AC ripple magnitude will change. The amplifier may converge on a Class-E amplifier with a finite DC feed inductance case [24]. This AC ripple will have main power in the fundamental frequency, while as n increases n^{th} harmonic will have less power.

If we analyze the current in the choke inductor in time domain we have to consider switch on and off states. In switch on case during half of the period the current in the choke current is:

$$I_{Lch}(t) = I_{Lch}(t_o) + \frac{(t - t_o)V_{dd}}{L_{ch}} \tag{2.16}$$

Where L_{ch} is choke inductance, V_{dd} is the supply voltage.

Since on state will last half period the current increase in the choke will be :

$$\Delta I_{Lch}(t) = \frac{V_{dd}T}{2L_{ch}} \tag{2.17}$$

During the switch off state the current of the inductor will decrease because

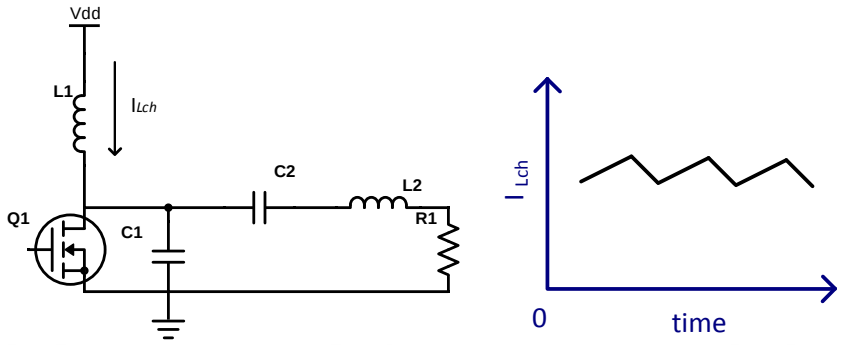


Figure 2.6: RF choke current waveform

the voltage at the lower end of the inductor, at capacitor $C1$, in the steady state will be higher than the V_{dd}:

$$I_{Lch}(t) = I_{Lch}(t_o) + \int_{t_o}^{t} (\frac{V_{dd} - V_{C1}(t)}{L_{ch}} dt) \tag{2.18}$$

In order to substitute the inductor with transmission line it should show an identical behavior for $I_{Lch}(t)$ in both switch on and switch off case. Since transmission line analyzes is easier in frequency domain, we compare it with the impedance of choke inductor in frequency domain.

When switch is on the impedance seen from the V_{dd} is:

Choke inductor used:

$$Z_L = j2\pi fL \tag{2.19}$$

Transmission line used:

$$Z_{TL} = jZ_o \tan(\frac{2\pi fl}{v}) \tag{2.20}$$

Z_o is the characteristic impedance of the transmission line, L is the choke

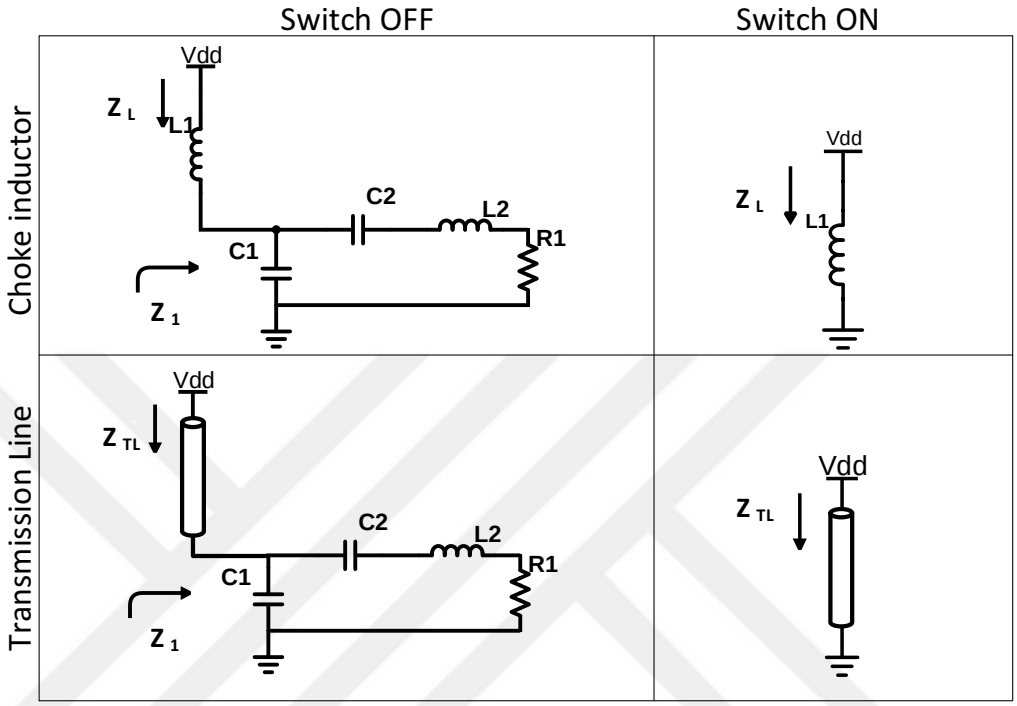


Figure 2.7: Impedance for short transmission line and choke inductor used amplifier for both switch on and off case

inductance, v is the speed in the transmission line, l is the length of the transmission line and f is frequency. Also we assume the inductor and transmission line is lossless. When switch is off the impedance seen from the Vdd is:

Choke inductor used:

$$Z_L = Z_1 + j2\pi fL \tag{2.21}$$

Where Z_1 is the impedance as shown in Fig. 2.7.

Transmission line used:

$$Z_{TL} = Z_o \frac{Z_1 + jZ_o \tan(\frac{2\pi fl}{v})}{Z_o + jZ_1 \tan(\frac{2\pi fl}{v})} \tag{2.22}$$

Both modes of operation should be analyzed separately. When switch is on:

For $\frac{2\pi fl}{v} \leq 0.5$ we can make a linear approximation:

$$Z_{TL} \approx jZ_o \frac{2\pi fl}{v} \tag{2.23}$$

If $L = \frac{Z_o l}{v}$ then $Z_{TL} \approx Z_L$.

When switch is off: For the same condition $\frac{2\pi fl}{v} \leq 0.5$, Eq. 2.22 can be transformed in:

$$Z_{TL} = Z_o \frac{Z_1 + jZ_o \frac{2\pi fl}{v}}{Z_o + jZ_1 \frac{2\pi fl}{v}} \tag{2.24}$$

In desired application: $|Z_1| \leq 10$. Together with $\frac{2\pi fl}{v} \leq 0.5$ and $Z_o \geq 50\Omega$ we can reduce further:

$$Z_{TL} = Z_1 + jZ_o \frac{2\pi fl}{v} \tag{2.25}$$

If $L = \frac{Z_o l}{v}$ then $Z_{TL} \approx Z_L$ for switch off case too.

From the equations above we observe that under conditions $L = \frac{Z_o l}{v}$ the transmission line can replace the choke inductor with a value $L = \frac{Z_o l}{v}$. As for the length of the transmission line we should choose it long enough such that it is equivalent to a large inductor and short enough so that the approximation will be valid for a desired maximum frequency f. Beyond that frequency the approximation is not valid anymore. In an even worse scenario for f such that: $\frac{2\pi fl}{v} = \frac{\pi}{2}$ the transmission line will be short circuited instead of large inductor. Following the same reasoning, no matter what the length of the transmission line is, at a certain n^{th} harmonic of the frequency operation we will encounter the case: $\frac{2\pi fl}{v} \approx \frac{\pi}{2}$. In the operation of Class-E amplifier, a practical and specific solution for our case can be to choose this critical frequency such that it is well above of the fundamental. In that case it will not be a problem because it will be filtered out properly by the load network of the amplifier, making no difference at the output.

2.3 Pulse Generation

The amplifier to be designed was aimed to be fully digitally controlled. In the section 2.1.3 we showed that driver is controlled by an FPGA, adjusting the frequency and phase. Envelope modulation is needed to be added at the pulse. At the end it will have the following form:

$$f(t) = A(t)sin(2\pi f_o t + \theta) \tag{2.26}$$

where $A(t)$ is the desired envelope modulation to be given to the pulse, f_o is the carrier frequency and θ is phase. It can be of *Sinc*, *Gaussian* or other pulse shapes. In order to have a fully digital amplifier both envelope and the phase is controlled from an FPGA.

2.3.1 Digital Modulation

Considering that Class-E amplifier is nonlinear amplifier we thought of making use of this property to modulate both the frequency and amplitude of the desired pulse by controlling the bits FPGA sends to the driver of Class-E amplifier. Lets consider 1 as switch on and 0 as switch off. In normal operation, a Class-E amplifier can be considered as a sequence of 10101... where each bit is long half period of the switching frequency. If we change the bit stream given to the driver, lets say 1001011.. than we can obtain a response different in both amplitude and frequency when compared to the normal operation. We can use this property of nonlinear Class-E amplifier to digitally modulate the envelope of the pulse with a fixed V_{dd}, without needing supply modulation.

The initial idea comes from analyzing the modes of operation of Class-E amplifier itself. First, under the assumption of an ideal switch, the Class-E amplifier can expressed as a mathematical model with two different cases: switch on and switch off.

The state space matrix representation of the circuit as shown in Fig. 2.1 of the system is as shown below.

For switch on:

$$\frac{d}{dt}\begin{bmatrix} I_{L_1} \\ V_{C_2} \\ V_{C_1} \\ I_{Lch} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_1} & -\frac{1}{L_1} & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L_1} \\ V_{C_2} \\ V_{C_1} \\ I_{L_{ch}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{L_{ch}} \end{bmatrix} V_{dd}$$

For switch off:

$$\frac{d}{dt}\begin{bmatrix} I_{L_1} \\ V_{C_2} \\ V_{C_1} \\ I_{Lch} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_1} & -\frac{1}{L_1} & \frac{1}{L_1} & 0 \\ \frac{1}{C_2} & 0 & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 & \frac{1}{C_1} \\ 0 & 0 & -\frac{1}{L_{L_{ch}}} & 0 \end{bmatrix} \begin{bmatrix} I_{L_1} \\ V_{C_2} \\ V_{C_1} \\ I_{L_{ch}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{L_{ch}} \end{bmatrix} V_{dd}$$

Exact solution has to be found for these differential equations. Next the time dependent terms are to be separated from the other ones.

$$\overline{X}(t) = \overline{A}(t)\overline{X}(t=0) + \overline{B}(t)\overline{U} \tag{2.27}$$

$\overline{A}(t)$ and $\overline{B}(t)$ contains the time dependent terms related to initial conditions and input sources correspondingly. $\overline{X}(t=0)$ is a vector with initial state values and $\overline{U}$ includes input vector terms. Once the initial conditions are known, the exact voltages and currents in the system can be calculated at any time t. In order to find the matrix $\overline{A}(t)$, $\overline{B}(t)$ in Eq. 2.27 the following differential equation should be solved.

For switch on:

$$\frac{d^2}{dt^2}I_{L_1}(t) + \frac{R}{L_1}\frac{d}{dt}I_{L_1}(t) + \frac{1}{L_1 C_2}I_{L_1}(t) = 0 \tag{2.28}$$

Solution can be written in the form:

$$I_{L_1}(t) = A\exp(\alpha t)\sin(wt+\theta) \tag{2.29}$$

Where A and θ are calculated from initial conditions in Eq. 2.30, 2.31, $w = \frac{1}{\sqrt{L_1 C_2}}$, $\alpha = \frac{R}{2L}$:

$$I_{L_1}(0) = Asin(\theta) \tag{2.30}$$

$$\frac{d}{dt}I_{L_1}(0) = \frac{-V_{C_2}(0) - I_{L_1}(0)R}{L_1} = A\alpha\sin(\theta) + Aw\cos(\theta) \tag{2.31}$$

Given the initial conditions we can solve the matrices. As for the switch off case the differential equation to be solved is:

$$\frac{d^2}{dt^2}I_{L_1}(t) + \frac{R}{L_1}\frac{d}{dt}I_{L_1}(t) + (\frac{1}{L_1C_2} + \frac{1}{L_1C_1})I_{L_1}(t) = \frac{I_{L_{ch}}(t)}{C_1} \tag{2.32}$$

The current in the RF choke inductor can be expressed as a linear expression $I_{L_{ch}}(t) = at + b$ equation since L_{ch} is relatively large. In this way we can reduce the equation to a 2^{nd} order differential equation. The solution of the differential equation Eq. 2.32 is:

$$I_{L_1}(t) = A\exp(\alpha t)\sin(wt+\theta) + (ct+d) \tag{2.33}$$

Where a,b,c,d are constants, $\alpha = \frac{R}{2L}$, $w = \frac{1}{\sqrt{L_1 C_{eq}}}$ and $C_{eq} = \frac{C_1C_2}{C_1+C_2}$. $I_L(t) = ct + d$ is the particular solution of Eq. 2.32 for input $I_{L_{ch}}(t) = at + b$. In this case the initial conditions are :

$$I_{L_1}(0) = Asin(\theta) + d \tag{2.34}$$

$$\frac{d}{dt}I_{L_1}(0) = \frac{V_{C_1}(0) - V_{C_2}(0) - I_{L_1}(0)R}{L_1} = A\alpha\sin(\theta) + Aw\cos(\theta) + c \qquad (2.35)$$

In this case in addition to A and θ, c and d are also unknowns. If we approximate V_{C_1} to be a constant voltage V_{C_1eff}, which can be acceptable considering the waveform in the Class-E amplifier, we can write:

$$I_{L_{ch}}(t) = I_{L_ch}(t_0) + \frac{V_{dd} - V_{C_1eff}}{L_{ch}}(t - t_o) \qquad (2.36)$$

$$V_{C_1eff} = \frac{1}{\Delta T}\int_{\Delta T} V_{C_1}(t)dt \qquad (2.37)$$

$V_{C_1}(t)$ can be derived from initial conditions, so on the left side the only unknown is V_{C_1eff}. After replacing the exact expression of $V_{C_1}(t)$ we can find V_{C_1eff} and calculate a, b unknowns in the particular solution. In this way an exact solution for the equation can be obtained. Once the initial conditions are known, at any time, at either state, the behavior of the circuit can be calculated. This is beneficial in computational terms because the time related terms are calculated before hand, and the computations is reduced in only matrix multiplications.

As it follows the previous equations the system has two different frequencies.

When switch is on:

$w_1 = \frac{1}{\sqrt{C_1 L_1}}$

When switch is off:

$w_o = \frac{1}{\sqrt{C_{eq} L_1}}$ and $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$

By switching the amplifier between those two frequencies at a certain pattern, we expected to be able to obtain a desired pulse shape with any carrier frequency at the range: $\frac{w_o}{2\pi} < f < \frac{w_1}{2\pi}$

In order to test consistence of this assumption a bitstream, switching pattern, was to be generated and tested. First, Class-E amplifier model was developed in MATLAB with several assumptions. Ideal capacitors, inductors and switch are used. The amplifier can be either in switch on or off state. The short transmission line was modeled with an equivalent inductor after proving they can replace each other under some assumptions.

In order to confirm the consistence of the developed model, MATLAB results were compared with LTSpice simulation of the same circuit. Next, an algorithm to generate the desired pulse was designed. The algorithm operates as diagram shown in Fig. 2.8.

After verifying the model for normal operation, we tried to generate a bitstream which results in the desired pulse. Before that here are some parameters to be defined. The desired pulse has a desired pulse carrier frequency f_d. Meanwhile amplifier is adjusted to operate at f_{stuned} which is close but not exactly the same with f_d. On the other hand f_o and f_1 are the natural frequency when switch is off and on respectively. N is the number of bits to be simulated forward whereas M is the number of bits to be saved out of N simulated. The frequency of switching of amplifier is $f_s = d \times f_{stuned}$ where $d = 1, 2, 4....$

After we determine a desired pulse shape with carrier frequency f_d, the pulse is divided in sections of length N bits and switch at frequency f_s. For the section of interest 2^N possible combinations are simulated. After that, l_1 norm error between the desired section and the generated one is calculated in order to select the bitstream which is closest to the desired shape. After the best bitstream for the current section is selected, M out of N bits are saved together with the last point that will be used as initial condition for the next section of the pulse. Other than for the case when $M = N$, the sections are non overlapping. The design was tested for $d = 1, 2, 4$, for different values of M and N.

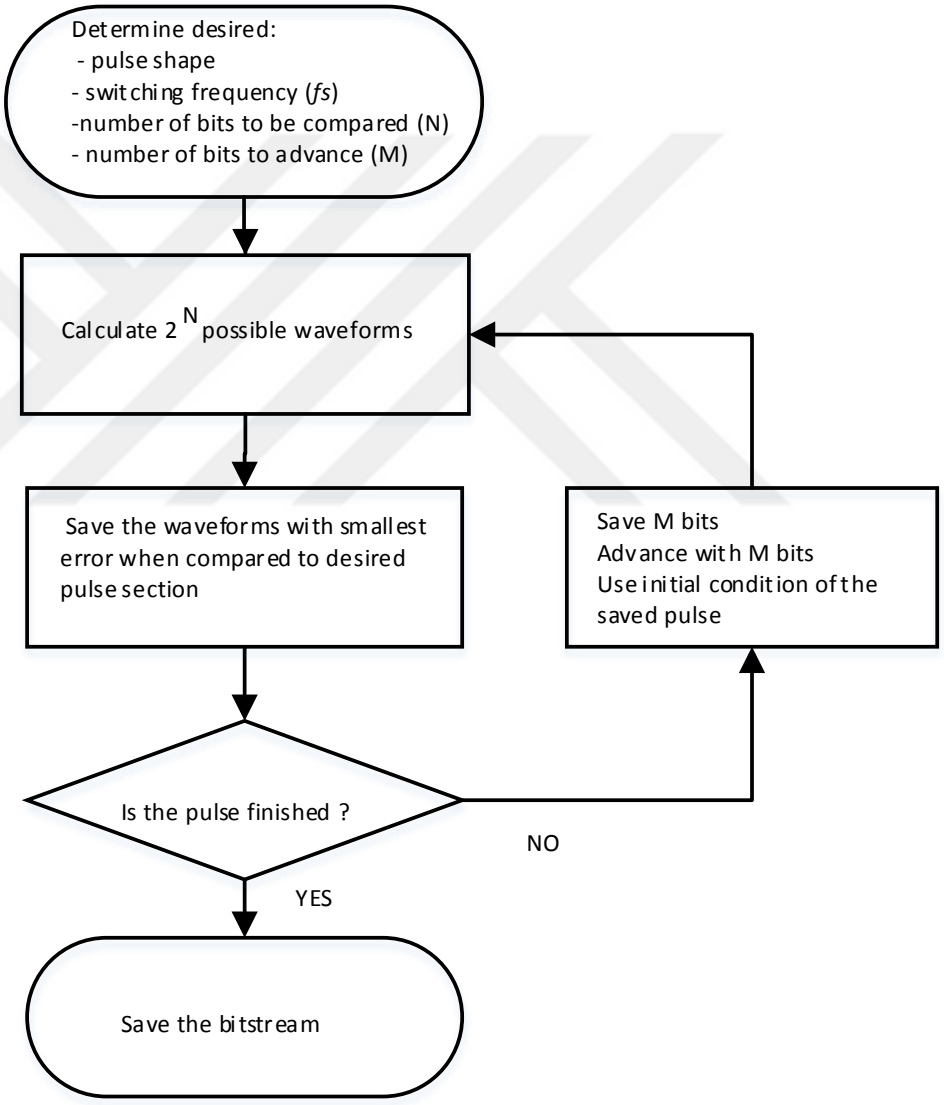


Figure 2.8: Desired pulse generation algorithm

2.3.2 Supply Modulation

In order to apply envelope modulation to the pulse, often for switching amplifiers, supply modulation is a preferred method. The reason for this is that in ideal case there is a linear relationship between load voltage and supply voltage. In practice it is not ideally linear because it is also related to the switch used. Nevertheless a characteristic curve or even a feedback circuitry can be used to correct for that. In [15] a buck converter switching at 1MHz was used. Intended design, a half bridge converter, is very similar to a buck converter. It differs from a buck converter in the part that it has two switches and a filter instead of a single switch with a filter. In one side this means a lower cost. When designing the half bridge converter some important constraints are to be taken into consideration. The switching frequency should be larger when compared to the bandwidth of the target envelope signal. The filter should be able to filter appropriately switching frequency component. Delay due to the filter should be kept minimum. Maximum efficiency is required for this stage too.

In order to satisfy the second constraint filter corner frequency can be decreased. However, inherent delay coming from the filter increases. So, another alternative is to increase the switching frequency. In this case: switching frequency will be larger than the bandwidth of the envelope signal and it will be filtered better with the same filter without increasing filter's delay. So a switching in the order of 1 MHz is appropriate. At the same time implementing it in an even higher frequency is also difficult because of component selection.

Often, desired pulse is generated by comparing a small signal of the desired pulse with a sawtooth oscillator to generate the pulse width modulated signal which controls the switches. The half bridge to be designed was intended to be digitally controlled. In a half bridge:

$$V_o = V_{dd} \times D \tag{2.38}$$

Where D is the duty cycle. The half bridge circuit does not need a comparator

circuit. It contains only the switch driver, two switches and the filter stage as shown in Fig. 2.9. D was calculated in MATLAB by comparing to a desired pulse shape. The switching frequency of the circuit was 1MHz. A step of 5ns is used in FPGA, so for 1MHz the voltage resolution is $0.005 \times Vdd$. The minimum pulse length the hardware can switch is 50ns. So a range of $5 - 95\% \times$ Vdd voltage can be obtained at the envelope in this mode of operation. For the voltages out of the defined range the pulse width is kept 50ns but the switching frequency is decreased such that the desired duty cycle is achieved. So we can determine the duration of each pulse width if we compare it with a digitized desired pulse. The bitstream generated on a PC is sent to the FPGA, which later on controls the Pulse Width Modulation(PWM) signal of the half bridge circuit.

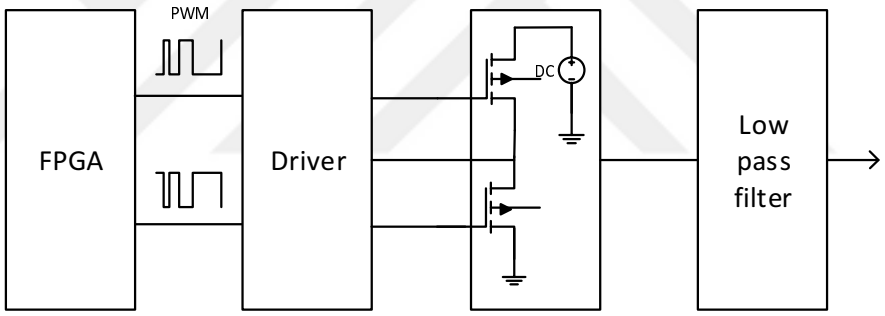


Figure 2.9: Supply modulation diagram

After the consulting similar studies and performing a theoretical study of every component and mode of operation the next step was to manufacture the system component and design proper evaluation experiments methods.

Chapter 3

Methods

In this part the methods used for designing the amplifiers are explained in detail. Two amplifiers and driver versions are introduced, explaining in detailed component selection and implementation. Technical details and information related to Printed Circuit Board (PCB) implementation are shown. Additionally simulation environment and models used during the development are presented. Next the developed experimental setups for measuring amplifier performance parameters are shown.

3.1 Hardware implementation

The whole process for the hardware implementation went through several component selection, simulation and prototyping iterations for different parts of the amplifier. In the initial versions building blocks such as the driver were tested on a two-layer PCB designed and manufactured in-house. In later versions four-layer prototypes were manufactured. Two versions are described in this thesis. Amplifier without supply modulation block (Av1), which is able to drive 100pF input capacitance switch with rise & fall time ≈2ns. Amplifier with a Supply Modulation block (Av2) is able to drive 300pF input capacitance switch with rise

& fall time ≈2ns. Additionally it contains a supply modulation block.

In Fig. 3.1 the design blocks are shown. As can be seen contains the driver block, main switch, transmission line external and the coil attached through an RF connector. In contrast to Av1, Av2 in Fig. 3.2 has the transmission line implemented in the PCB as strip line. Additionally it can be noticed that it contains a supply modulation block with a low pass filter.

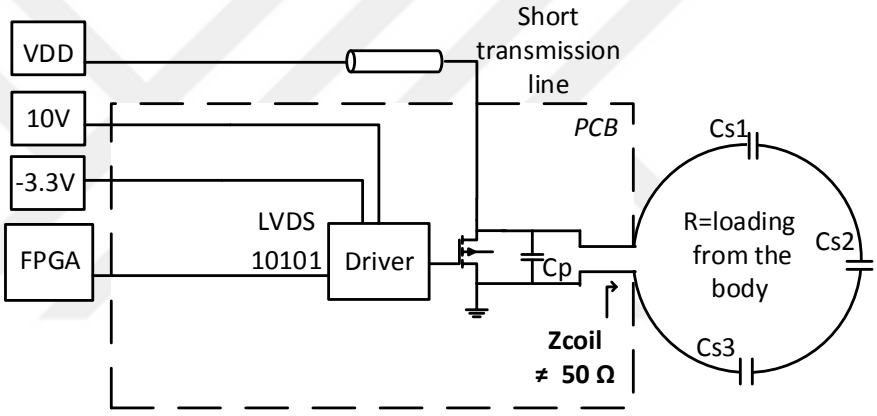


Figure 3.1: Av1 block diagram

Another difference is that Av1 requires an external -3.3V DC supply whereas in Av2 this voltage is generated from the already available 10 VDC.

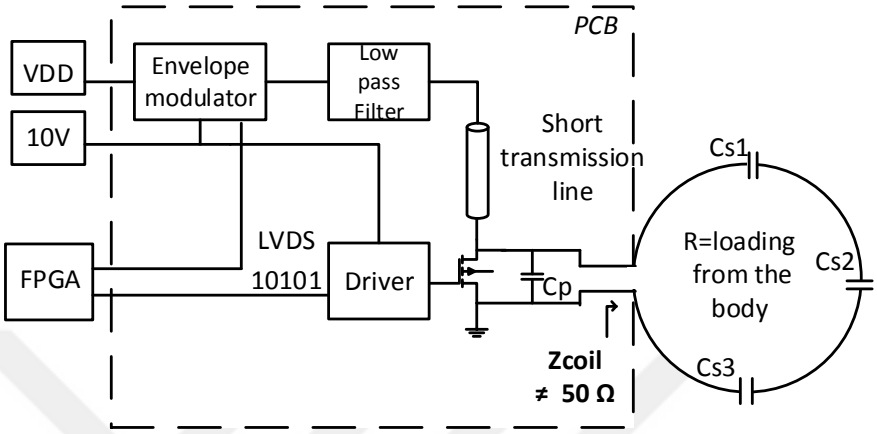


Figure 3.2: Av2 block diagram

3.1.1 Driver implementation

In order to drive the switch, a driver satisfying the requirements mentioned in section 2.1.3 is manufactured. The number of stages is the same for both Av1 and Av2. The difference is in the second stage and third stage. In second stage Av2 uses 2 paralleled opamps whereas in Av1 there is a single opamp. In stage 3 the switch is replaced with a more powerful one. In this way the driving capability of Av1 is 100pF but Av2 can drive 300pF switch at very similar rise and fall times ≈2ns.

In Av1 various components are used. DS90LT012A is an Integrated Circuit Chip (IC) that converts LVDS signals in a single ended 0-3.3V square pulses. It requires 3.3V supply voltage. THS3202 is a high slew rate current feedback opamp used in non-inverting configuration with Gain=2 V/V. It requires supply voltage of 10V and -3.3V. RF10U7P is an LDMOS transistor used to charge and discharge gate capacitance of the switch. LF33ABDT is DC regulator IC with fixed voltage output used to obtain 3.3V out of 10V.

In the driver of Amplifier 2 as shown in Fig. 3.4, in addition to the fore mentioned components, there are additional ones. MAX1861 is a switched capacitor

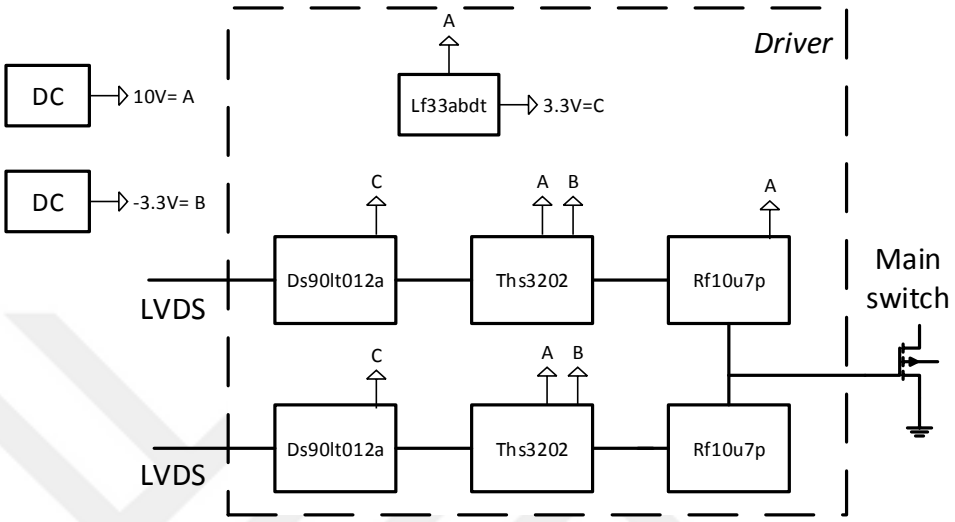


Figure 3.3: Driver of Av1

converter. It transforms the input DC voltage in negative voltage of the same magnitude, -3.3V in this case. It is a very good solution for obtaining a negative voltage without using inductors and complex circuitry while saving space at the same time. MRF1513 is an LDMOS transistor able to supply more current than RF10U7P.

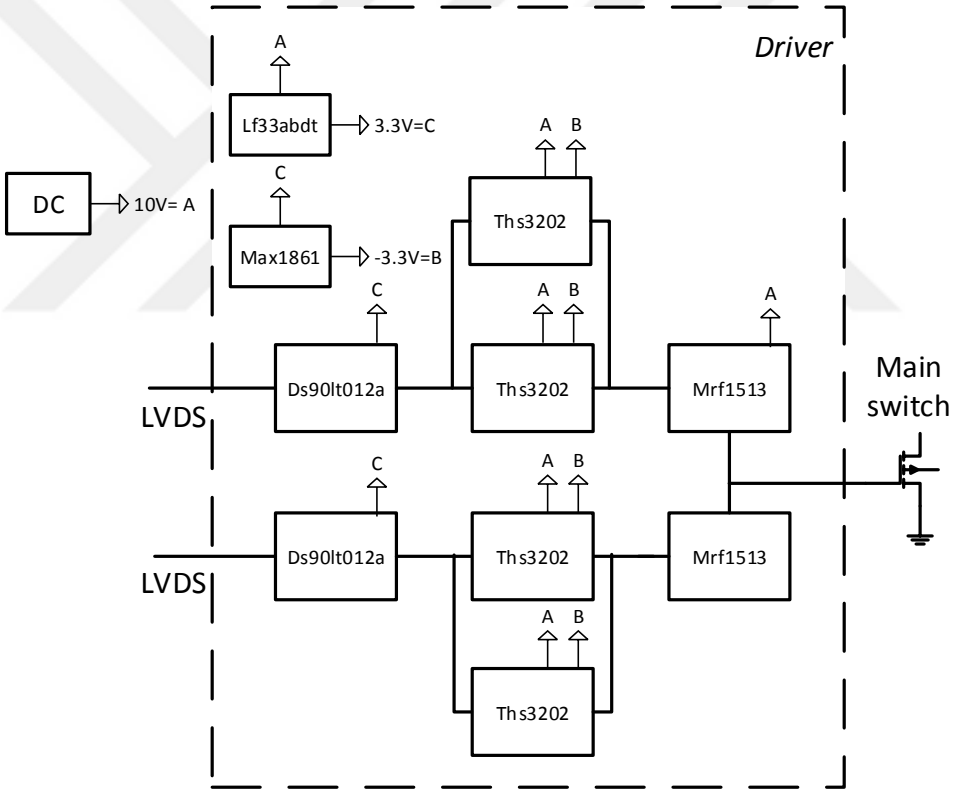


Figure 3.4: Driver of Av2

3.1.2 Supply modulation implementation

In Amplifier 2 supply modulation block was implemented with a half bridge topology and a π low pass filter. The filter is built from 10μF capacitors and a 550 nH air core inductor. The components are shown in Fig. 3.5. MIC4104 is an IC used to drive half bridge switches. The deadtime is arranged by the input signals. IRFH7194PBF is a low on-resistance transistor used for the half bridge switches.

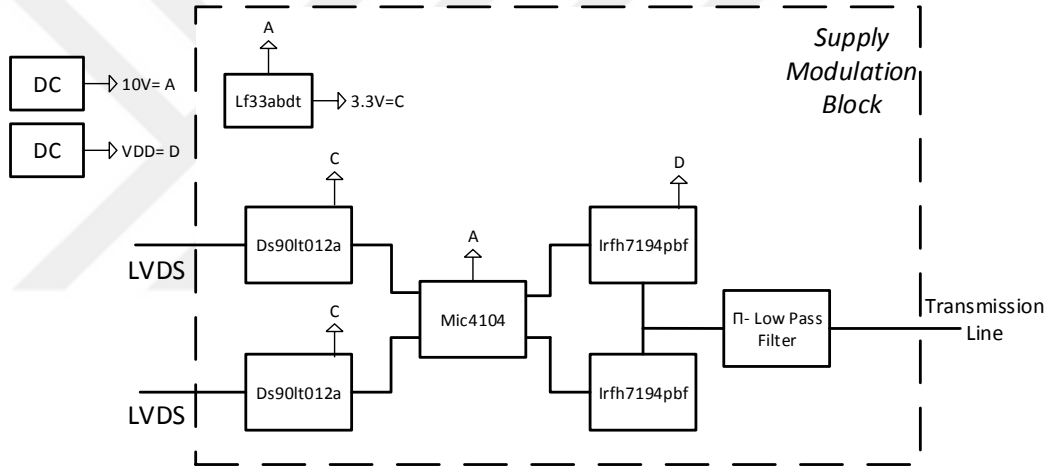
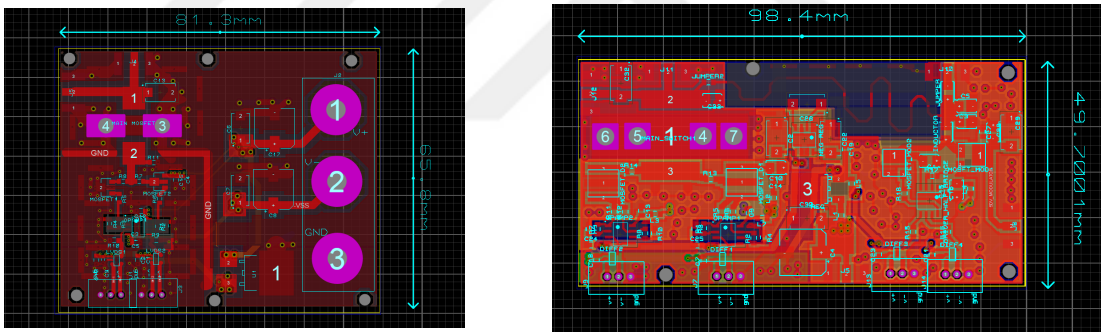


Figure 3.5: Supply modulation block and its components

3.1.3 Layout implementation

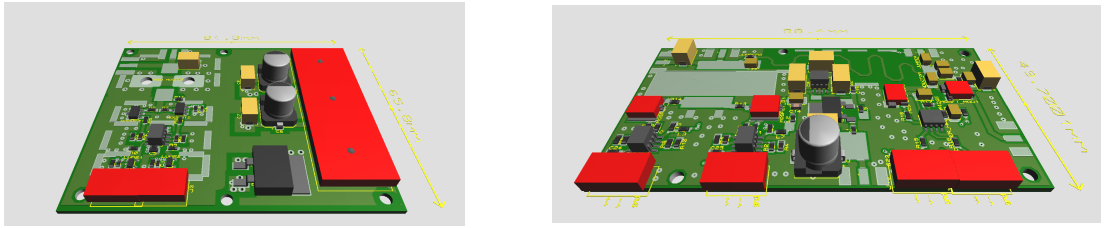
The layout for the PCB implementation was drawn in Proteus 8.0 software. While designing the layout is was very important to design proper grounding, minimize space and include test points at the PCB. Four-layer PCB is designed. First layer is the component layer mainly with signal traces. Second layer and fourth layer is ground layer. Third layer contains DC signal traces.

Thickness of the board was 1.6mm, with component soldering only on the top side. Amplifier 1 had a size of 8.1cm x 6.5cm while the Amplifier 2 has a size of 5cm x 10cm. The layout and 3D illustration of both versions can be seen in Fig. 3.6 and Fig. 3.7.



(a) (b)

Figure 3.6: Layout of Av1 a) and Av2 b)



(a) (b)

Figure 3.7: 3D illustration of the drawn layout for Av1 a) and Av2 b)

3.2 Experimental setup

3.2.1 Power Measurement

In order to measure the output power we developed an custom setup. A small pickup coil, tuned to 50Ω was placed next to the main coil. The pickup coil was connected through a -10dB custom made attenuator to an oscilloscope DSO-S104A (Keysight Technologies).

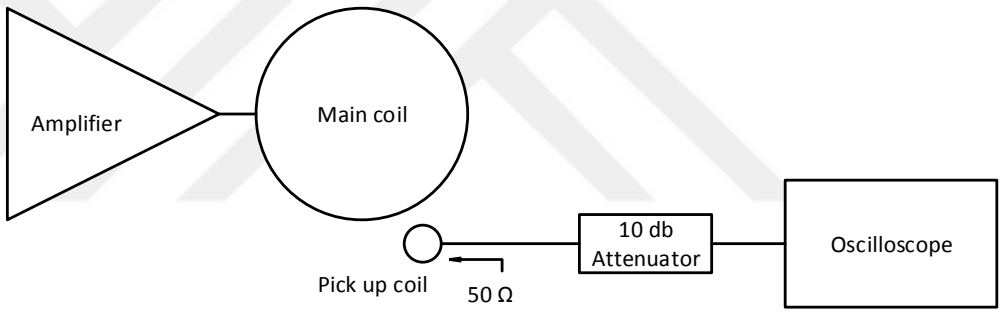


Figure 3.8: Amplifier power measurement setup diagram

By keeping the pickup coil small and in a moderate distance close to the main coil coupling between coils was kept small so that the pickup coil would not load and affect the tuning of the main coil. We know that:

$$B_{coil} = \alpha \times I_{coil} \tag{3.1}$$

Where I_{coil} is the current flowing in the main coil, B_{coil} is the magnetic field produced when I_{coil} flows in the main coil, α is a constant related to other physical parameters.

$$V_{pickup} = \beta \times B_{coil} = \alpha \times \beta \times I_{coil} \tag{3.2}$$

V_{pickup} is the voltage induced at the pickup coil from the magnetic field generated in the main coil, β is a constant related to physical parameters such as coil distance, inductance etc. So, we observe that there is a linear relationship between the voltage induced in the pickup coil and the current flowing in the main coil. In order to determine the value of $\alpha \times \beta$ the following step was applied: In the main coil a 2.2Ω SMD chip resistor was connected in series in the main coil. Next a voltage at different levels was applied at the main coil from a signal generator. By measuring the voltage on the 2.2 Ω resistor, the current flowing in the main coil, I_{coil} was calculated. At the same time V_{pickup} , the voltage induced at the pickup coil was measured. In this way $\alpha \times \beta$ was calculated. Next the chip resistor was removed and then a phantom was attached to the coil. After that the impedance seen at the coil Z_{coil} was measured in a network analyzer. $R_{load} = \Re\{Z_{coil}\}$ is the loading coming from the phantom.

The output power than is calculated as follows:

$$P_{load} = R_{coil} I^2_{coil\_rms} \tag{3.3}$$

As for the input power, a current probe 1146B (Agilent) was used to measure the current flowing to the transmission line.

$$P_{drain} = V_{dc} I_{dc} \tag{3.4}$$

Where V_{dc} is the voltage applied at the drain, I_{dc} is the current measured from the current probe. Drain efficiency was calculated as follows:

$$\eta_{drain} = \frac{P_{load}}{P_{dc}} 100\% \tag{3.5}$$

As for the driver power consumption, it is small compared to the others. It is constant because it is only switching the gate capacitance of the main switch at a certain frequency. Driver power consumption was measured by using the values of current and voltage at DC the power supply.

3.2.2 Digital modulation experimental setup

In order to test the algorithm presented in section 2.3.1 preliminary simulations were performed in Matlab. Eventually several bitstreams were generated. After that they were sent offline as a bit file in the FPGA. Next, the FPGA is used to send the pulse in a burst mode with repetition time 100ms. It also should be mentioned that the bitstream was adapted for the driver as explained in section 2.1.3 by adding the dead time between the pull up and pull down signals. The signal was observed in oscilloscope both in time domain and frequency domain in real time. After that the data were analyzed in more detail offline and the model was optimized further. The overall procedure is explained in Fig. 3.9.

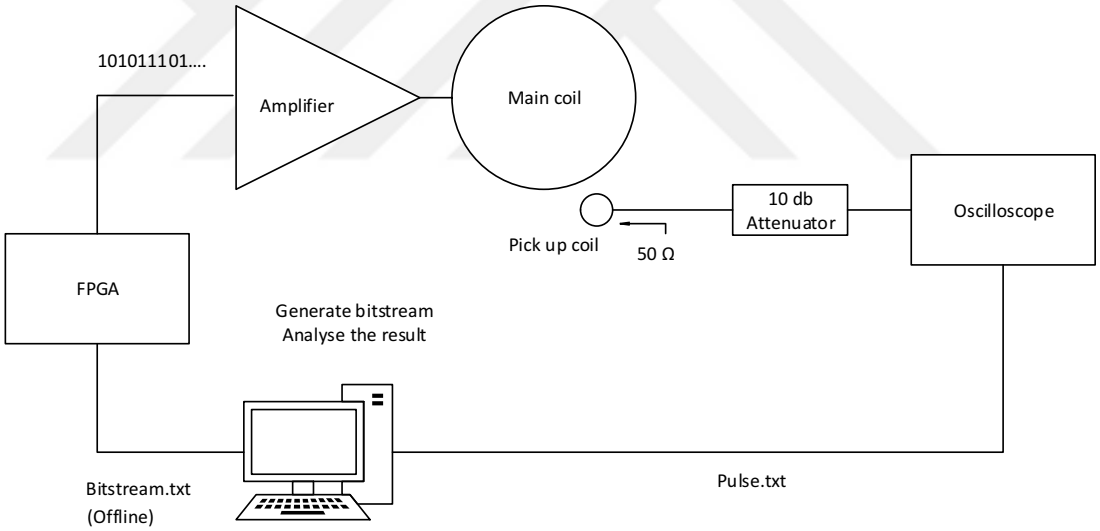


Figure 3.9: Digital modulation experimental setup procedure

After analyzing the performance of the algorithm in experimental results several conclusions on feasibility of this method are explained in further sections.

3.2.3 Coupling Measurement Experimental setup

Since the final goal of this amplifier was to use in an array of amplifiers, the coupling between amplifiers is an important issue because not only it has imaging effects, but also it may reduce amplifier efficiency as well as risk the stability of

the system. Since the system is not a 50 Ω a measurement method was developed. Measuring coupling coils while both amplifiers are working was not a straightforward problem to be solved. Small pickup coils are placed next to each coil in order to sense the current. Two different amplifiers were operated at 123 MHz and 123.2 MHz at similar output power levels. In the pickup coils the coupled signal would have two frequency components from each amplifier respectively. The pickup coils is placed such that the coupled signal from the desired coil is much larger then from the next amplifier. So in the pickup coil next to amplifier at 123 MHz the signal at 123.2 MHz will be due to coupling between Coil 1 and 2, not directly from amplifier 123.2 MHz to the pickup coil. In this way we were able to distinguish the signal of each amplifier and calculate the coupling at different distances between coils. Meanwhile a comparison for the same coils at 50 Ω was done by adding a matching circuit in front of the coils. At the same distance the coupling was measured, but this time with a network analyzer connected. The measurement setup is illustrated at Fig. 3.10.

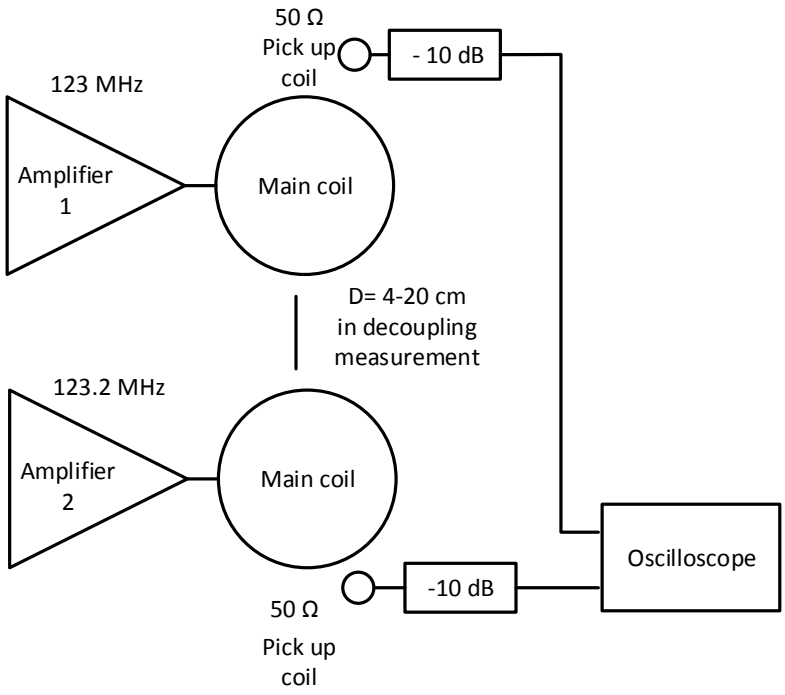


Figure 3.10: Coupling between neighbor amplifiers measurement setup

3.2.4 MRI experiment

After testing the amplifier outside the scanner an MRI scanner experiment was performed. The operation of the amplifiers inside the scanner were to be analyzed. For this purpose a 2-channel transmit experiment was designed as shown in Fig. 3.11. The amplifiers were placed inside the bore and connected to 12 cm diameter circular loop as transmit coil elements. The distance between the loops was 10 cm from each other. The amplifiers signals are controlled from FPGA via LVDS signals sent through a CAT7 ethernet cable.FPGA is programmed externally via USB cable. After programming the FPGA and saving the pulse shape in the Fpga memory, the cable is removed in order to prevent noise flow inside the scanner room. FPGA is connected to systems 10 MHz clock, Unblank signal and 123.2 Mhz. These signals are required to synchronize the pulse generation with the systems sequence. As sequence a 3D Flash sequence with TR=10 ms , TE=4.9 ms, sequence was used. Receive coil was used a 7- Channel Siemens spine receive coil. Both DC power supply and FPGA are placed inside the scanner room at the corners. Two experiments where performed. First in-house prepared loops are connected to developed Class-E amplifier and used to transmit simultaneously. Second, the loops are attached to a matching circuit that matches the coils to 50Ω. After that systems TxArray Analogic amplifiers are used to send the RF pulse to the loops.

The purpose was to have same transmit sensitivity, same phantom, same sequence. In this way a fair comparison between developed amplifier and a conventional one could be done.

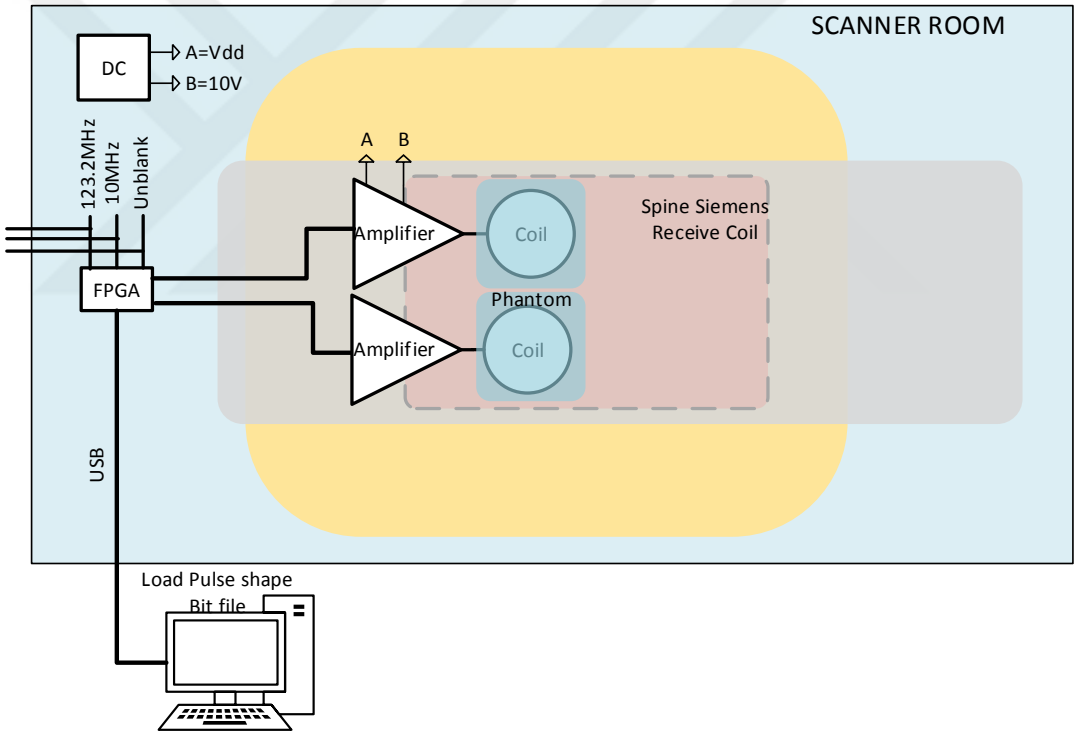


Figure 3.11: MRI experiment setup illustration

Chapter 4

Results

In this part simulation and experimental results are presented and compared. Driver simulation and experimental results show good coherence with each other. Complete amplifier simulations were performed to verify the design. After that, experimental setup calibration performed and power measurement data are obtained. Short transmission line used as an RF choke was simulated in order to verify the assumptions and theory. Digital modulation simulation and experimental results are presented after verifying that the MATLAB model is consistent with simulation model. Results of generated different pulse shapes are shown together with MRI scanners own pulse shapes. Next, simulations and experimental results of digital modulation are presented. Finally an MRI experiment with two channel transmit was performed to evaluate the operation fo the amplifiers inside the bore of the scanner.

4.1 Driver

4.1.1 Driver simulation results

According to the restrictions in driver design, after selecting the components the complete driver simulation was done in the ADS2009. The values of the components presented in the design represent the final values used in last version of the amplifier.

The inputs supposed to be given from the FPGA are given from signal sources. The full schematic is shown in Fig. 4.1. The results for simulation including dead time and no dead time are shown in Fig. 4.3 and Fig. 4.2 respectively. It can be observed that the signals controlling last stage do not switch the MOSFETS on at the same time. In order to verify and compare the difference, one way can be to observe the current flowing from the pull down switch at the last stage. At the last stage each MOSFET is supposed to be on one at a time. Following the same logic the current pulled from the supply should flow once in a period, when the capacitance is being charged. If we observe the case where no dead-time is added, current flows through the pull down switch at the time of transition too. However, when the dead time is added it can be observed that the same issue is not present anymore. It also can be observed that the rise and fall time has improved in the last stage. Also, the power dissipation is reduced in the driver.

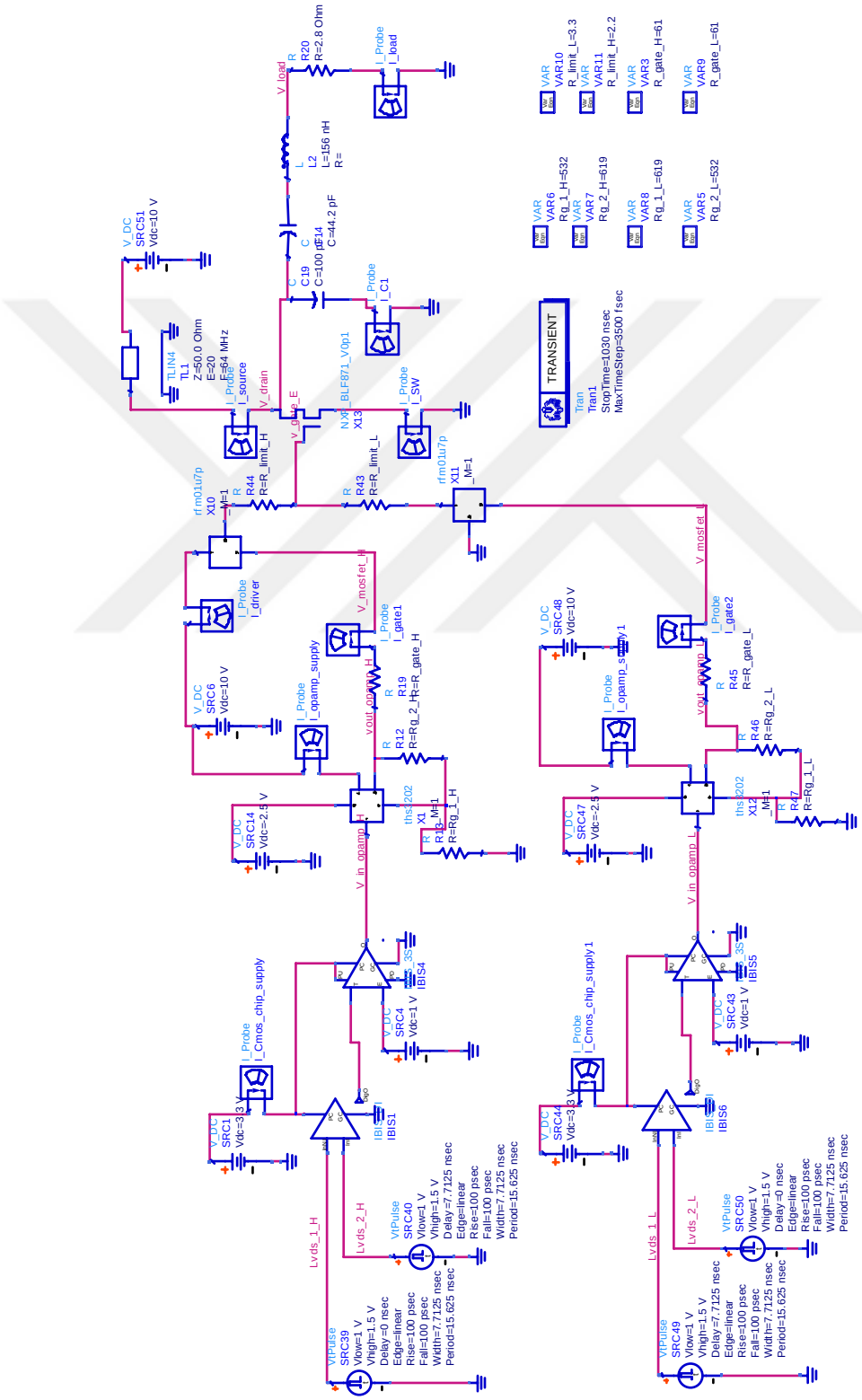


Figure 4.1: Digital modulation experimental setup procedure

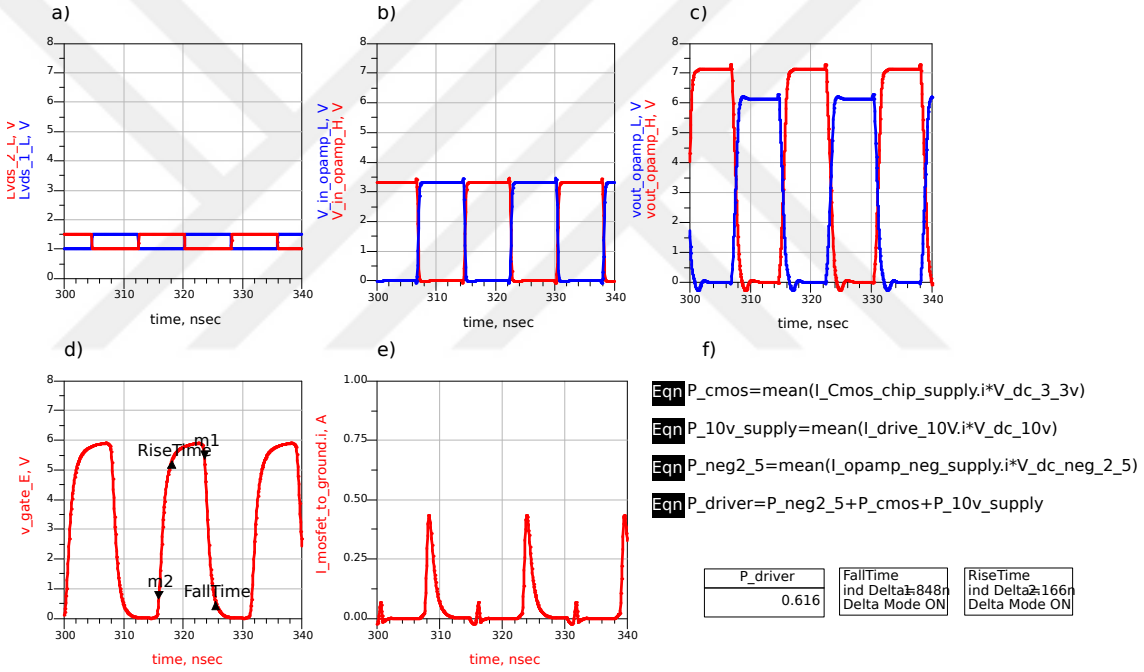


Figure 4.2: Driver with no dead time simulation results. Lvds signal input in Low side (a) Single ended signals (b) Opamp stage output signals (c) Waveform at the gate of Class E amplifier switch (d) Current flowing through the Low side mosfet in the last stage (e) Calculation of driver power consumption (f)

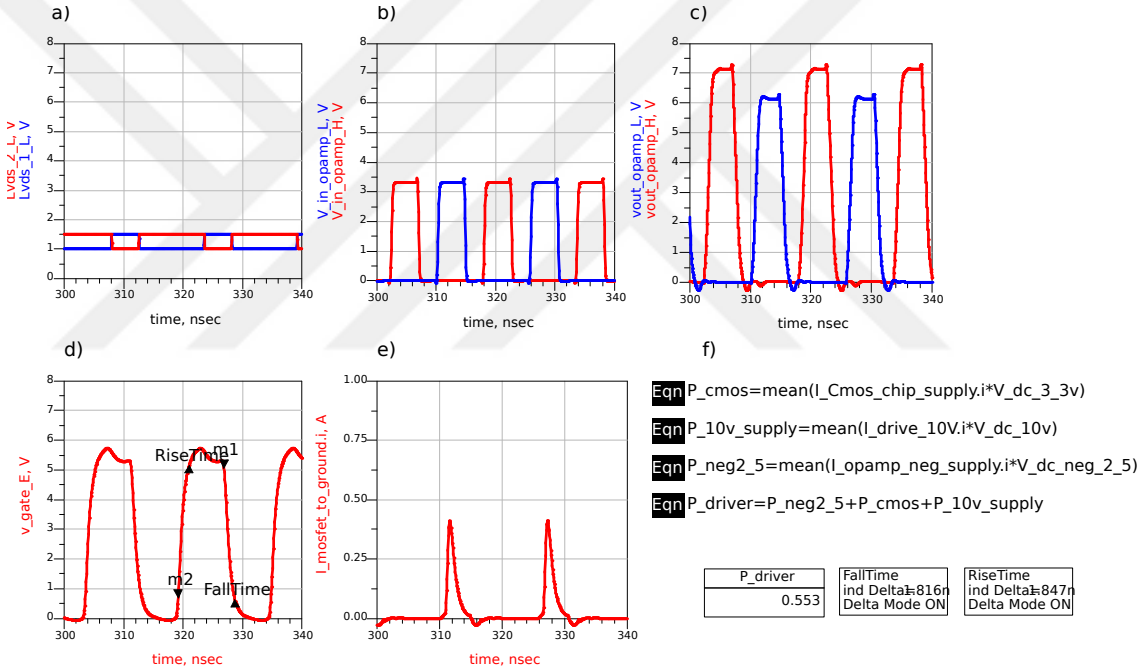


Figure 4.3: Driver with dead time simulation results. Lvds signal input in Low side a) Single ended signals b) Opamp stage output signals c) Waveform at the gate of Class E amplifier switch d) Current flowing through the Low side mosfet in the last stage e) Calculation of driver power consumption f)

4.1.2 Driver experimental result

The driver was tested with dead time and without dead time. The waveform at the gate is as in the following figure. Rise time, fall time and power dissipation was compared for both cases. It can be observed that the improvement expected is following the simulation results.

Figure 4.4: Signals in the driver high and low side at the input of the opamps

In the Fig. 4.3 the signals at the output of the LVDS to CMOS chip converter is shown. The red trace is measured with an active probe, whereas the blue trace is measured with a passive one. Since there was only one available active probe and both of the signals are to be shown simultaneously we used the passive probe. The blue trace is distorted because the probe is loading. However, it can be observed clearly that two signals are not high at the same time.

In the Fig. 4.5 it is shown the signal at the gate of the main switch of the amplifier. In the Tab. 4.1 the rise and fall times, power dissipation of simulation and experimental results are compared.

Figure 4.5: Gate driving signal for 64MHz

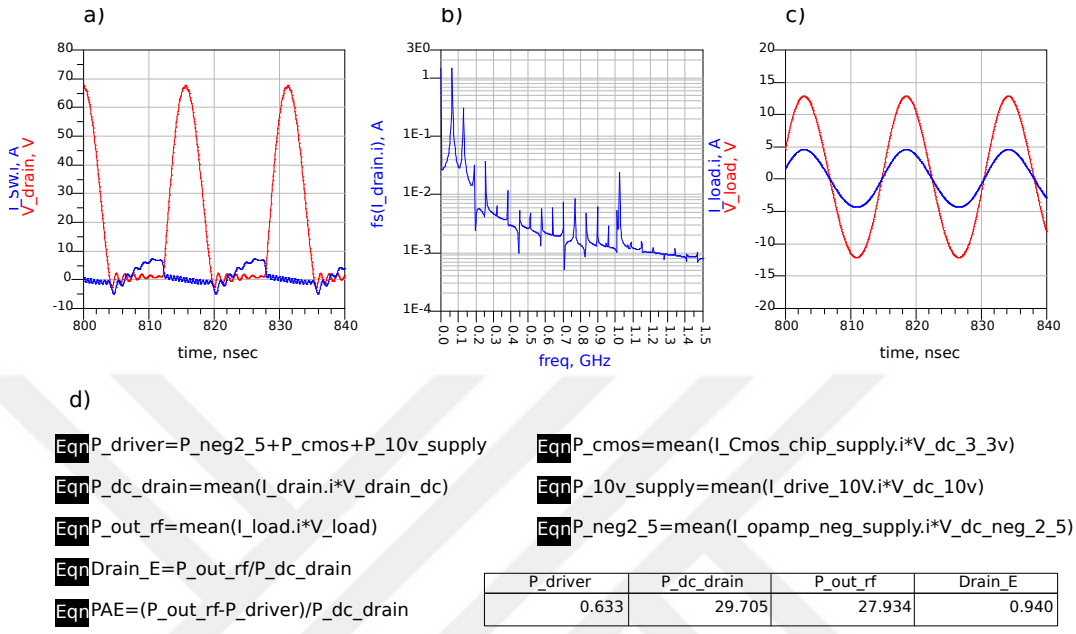
	Simulation		Experimental
	Without dead time	With dead time	With dead time
Rise time (ns)	2.17	1.85	1.75
Fall time (ns)	1.85	1.81	1.68
Power (W)	0.62	0.55	1.08

Table 4.1: Comparison of driver data

4.2 Class E amplifier with transmission line

4.2.1 Simulation results

The amplifier initially simulated in LTSpice with ideal components for faster tuning. After that it was simulated in ADS with the circuit as shown in Fig. 4.1 since the models for components used are available for ADS2009. In the simulated circuit the transmission line is assumed to have no loss. From the simulations 90-94 % drain efficiency has been achieved with the simulated component values and models.



P_driver	P_dc_drain	P_out_rf	Drain_E
0.633	29.705	27.934	0.940

Figure 4.6: Simulation of full circuit and calculation of power results . Current and voltage accross the switch a) Logarithmic view of the current in the transmission line b) Current and voltage at the load c) Signals at the gate of last stage mosfets

4.2.2 Experimental results

After obtaining promising result in simulation, several two-layer and four-layer PCB were designed and built for further test and design.

The coil was designed to be attachable through a connector to the amplifier. In this way different coils could be tested with only changing the tuning of the coil and only one capacitor value in the amplifier board. The same way the short transmission line is connected through a connector, in order to be able to try different length transmission lines.

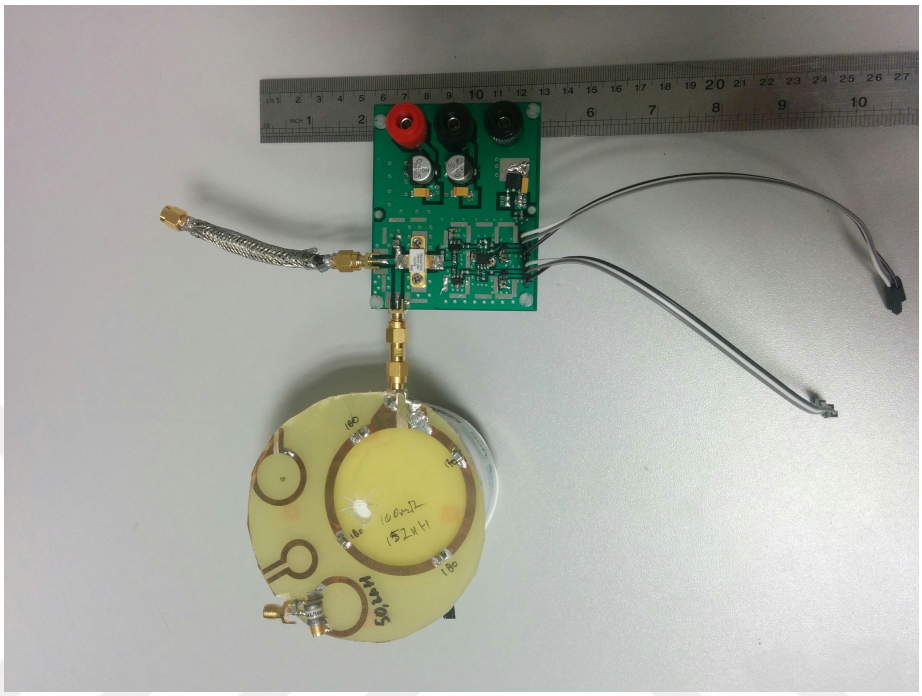


Figure 4.7: Amplifier Av1

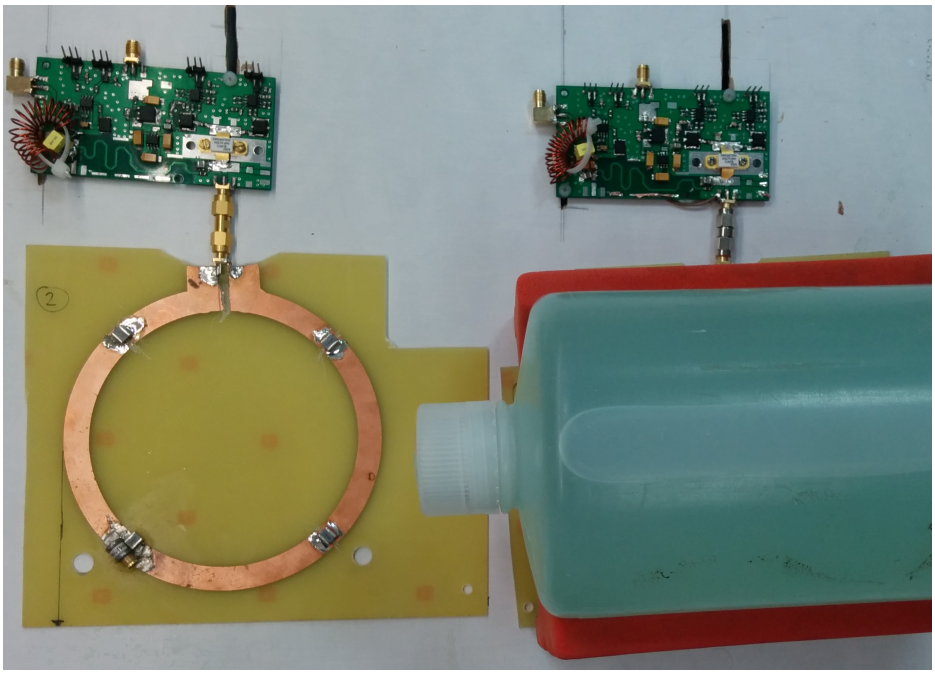


Figure 4.8: Amplifier Av2

Measured			Calculated	
$V_{input}(V)$	$V_R(mV)$	$V_{osc}(mV)$	$I_{coil}(mA)$	$\alpha \times \beta$
1.970	546.000	33.330	243.750	0.137
1.700	423.000	26.300	188.839	0.139
1.400	383.000	23.900	170.982	0.140
1.250	348.000	21.600	155.357	0.139
1.100	304.000	18.900	135.714	0.139
1.000	279.000	17.300	124.554	0.139
0.800	225.000	14.100	100.446	0.140
			Mean $\alpha \times \beta$	0.139

Table 4.2: Calibration measurement data

The amplifier is shown in Fig. 4.7. The phantom which is attached below the coil loads the amplifier with the values shown in the simulation schematic. In order to measure the power and efficiency, the procedure explained in section 3.2.1 was followed. In order to calculate $\alpha \times \beta$ a signal was applied at the coil where a Surface Mount Device (SMD) 2.2Ω chip resistor was connected in series. In this was the current in the coil could be calculated.

Then, the voltage induced in the pickup coil was observed in the oscilloscope. This measurement was taken at different values and the data are presented in Tab. 4.2.

In this way in the following calculations the average of $\alpha \times \beta = 0.139$ was used.

The input power was calculated by measuring the input current with current probe and multiplying with the voltage at the input of the amplifier. The amplifier output power was measured as mentioned in the section 3.2.1. The amplifier was run in a burst mode, 4ms pulses with a repetition time of 200ms. The first reason for this is that the switch cannot deliver more than 20W in continuous operation. It should be mentioned that the desired operation in MRI scanner will be similar, sending burst mode pulses. Power measurement results are presented in Fig. 4.10 and Fig. 4.11.

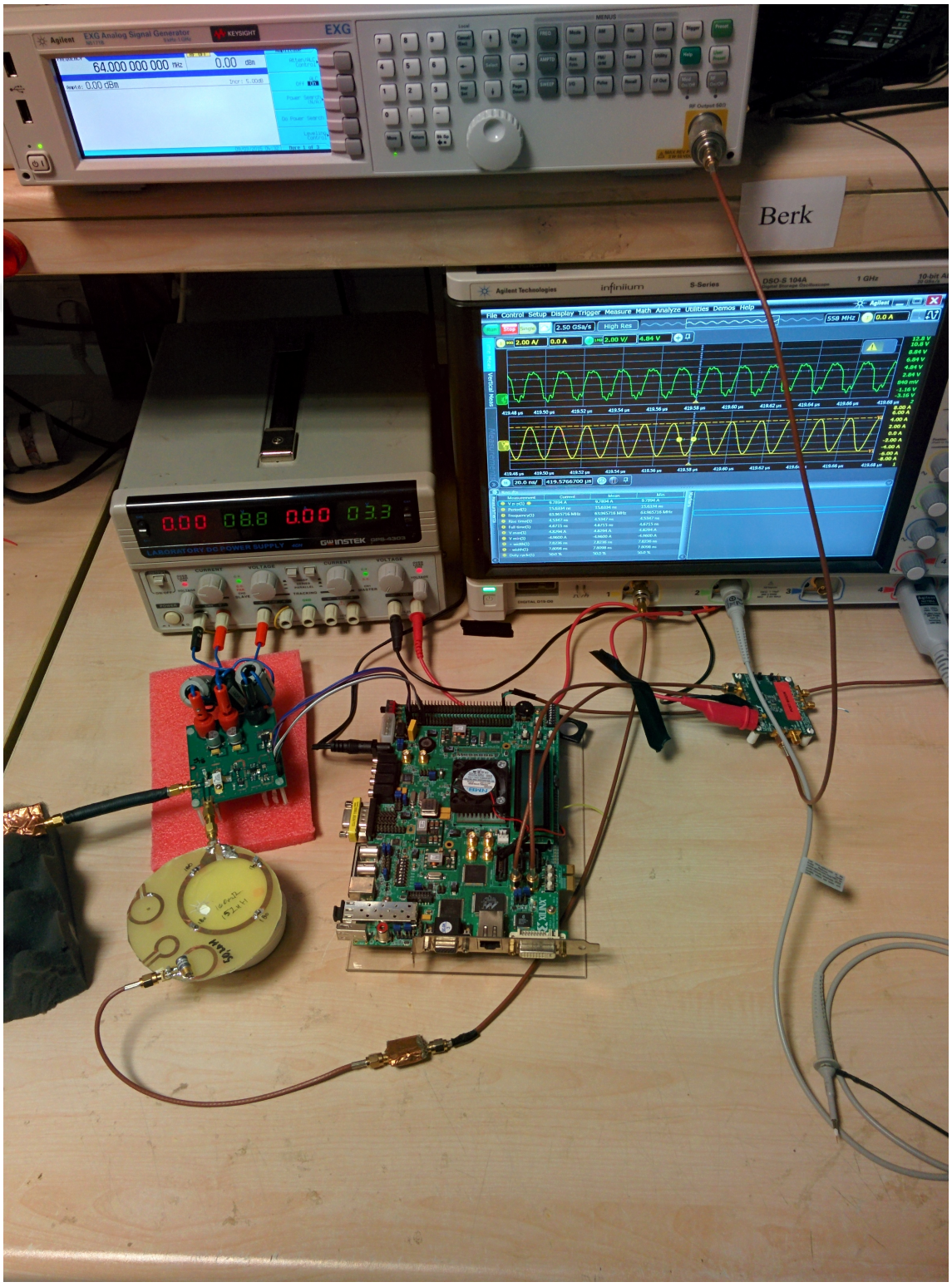


Figure 4.9: Measurement Setup

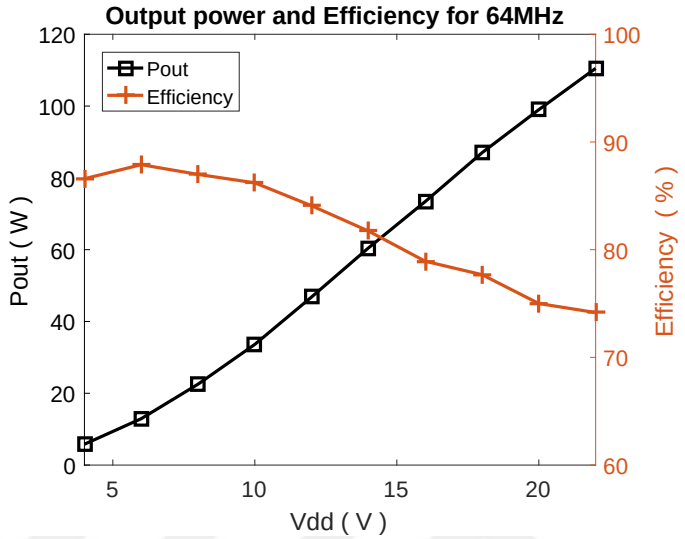


Figure 4.10: Power measurement and efficiency for 64 MHz

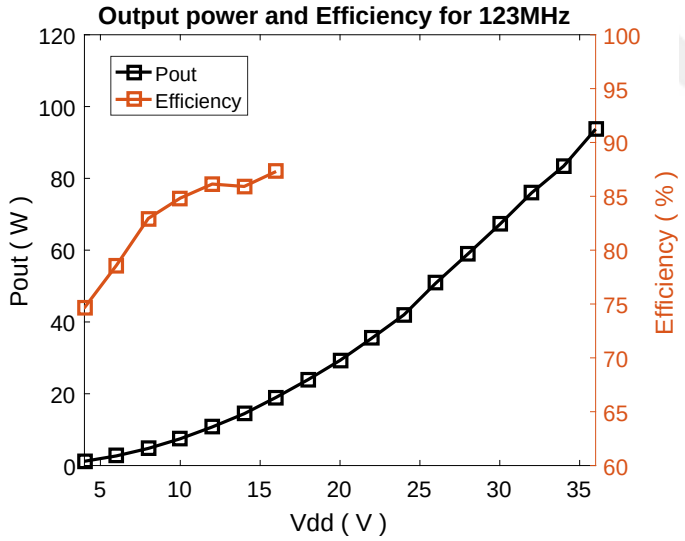


Figure 4.11: Power measurement and efficiency for 123 MHz

Efficiency values for more than 20 W output power are not shown because input power could not be measured due to setup limitations for 123 MHz mode.

4.3 Transmission line results

4.3.1 Simulation results

Initially in order to verify the validity and the range of the assumptions we switch on and switch off case the impedance seen in all harmonics. The simulations are for 64MHz and up to 15 harmonics. The transmission line has characteristic impedance $Z_0 = 100\Omega$ and length 10.3cm. In Fig. 4.12 is shown the case where the first 5 harmonics are within the linear approximation presented in the theory part.

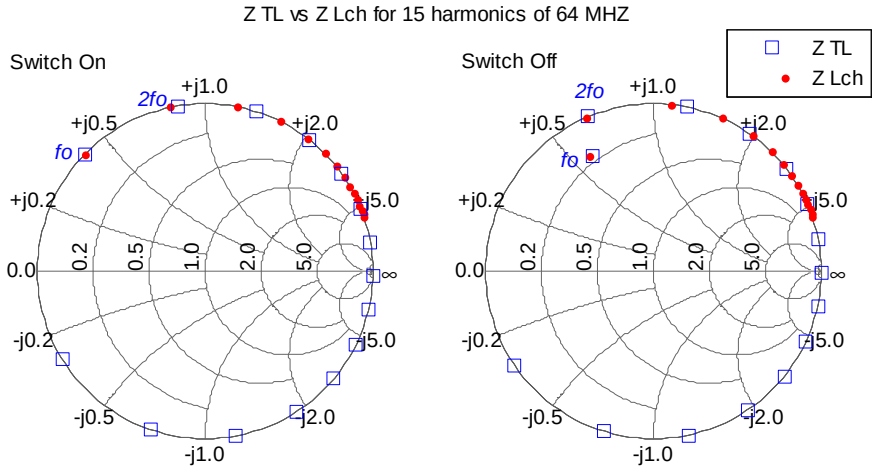


Figure 4.12: Impedance seen from the drain supply for transmission line and choke inductor usage

It can be observed that for higher harmonics the approximation fails. In the desired application this ca be a concern if it fails for frequencies close to f_o. In the Fig. 4.13,4.14 the current entering the drain together with output current are compared for the case when a choke inductor versus short transmission line were used.

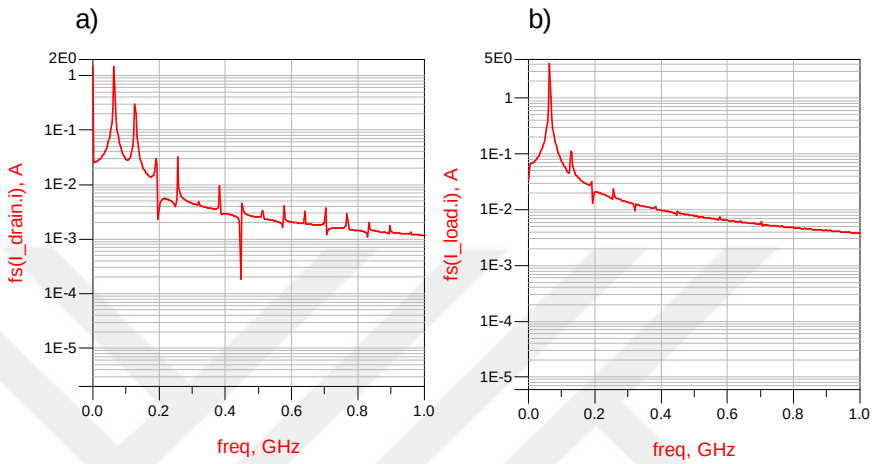


Figure 4.13: Logarithmic view of the spectrum of choke inductor current a) and load current b)

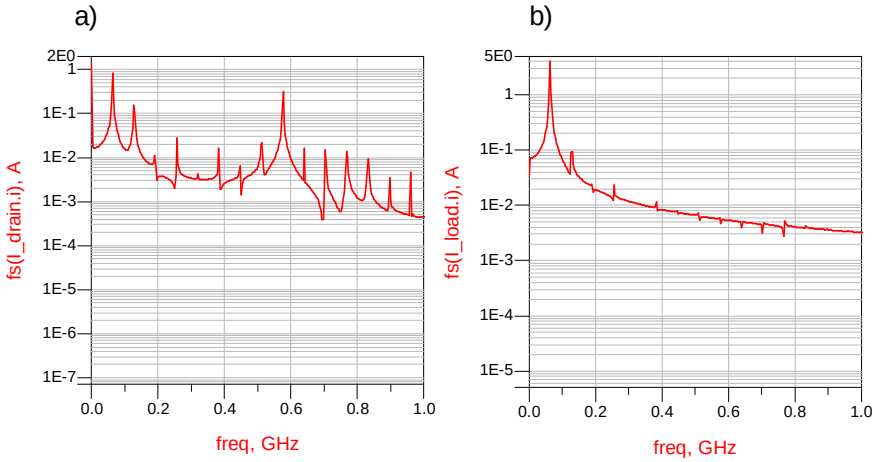


Figure 4.14: Logarithmic view of the spectrum of transmission line current a) and load current b)

4.3.2 Experimental results

In order to verify the assumptions for using a short transmission line instead of an RF choke we plotted in smith chart the impedance seen from the supply in both cases when switch is on and switch is off. In addition to this, also the characteristic of the transmission line the is also measured in a Network Analyzer (NA) E5061B (Agilent).

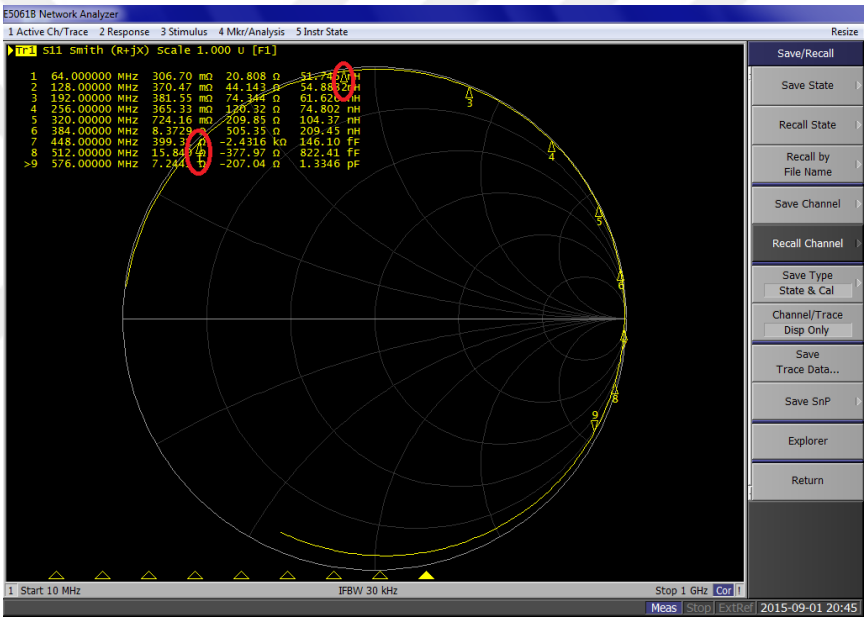


Figure 4.15: Impedance seen from the drain supply for transmission line when the end is short circuited (switch on case)

The experimental measurement for switch off was not done because the drain to source capacitance of the switch is larger than the biased case. In this case any measurement would not be accurate.

4.4 Pulse Generation

4.4.1 Digital modulation

4.4.1.1 Verification of matlab model

In the methods part we described the MATLAB model of the Class-E amplifier. Under the assumptions mentioned there we compared the LTSpice simulation and MATLAB model. In the following results we compare drain voltages, choke current and output voltage for the same input and circuit model. The waveforms shown are enough to compare the models with each other.

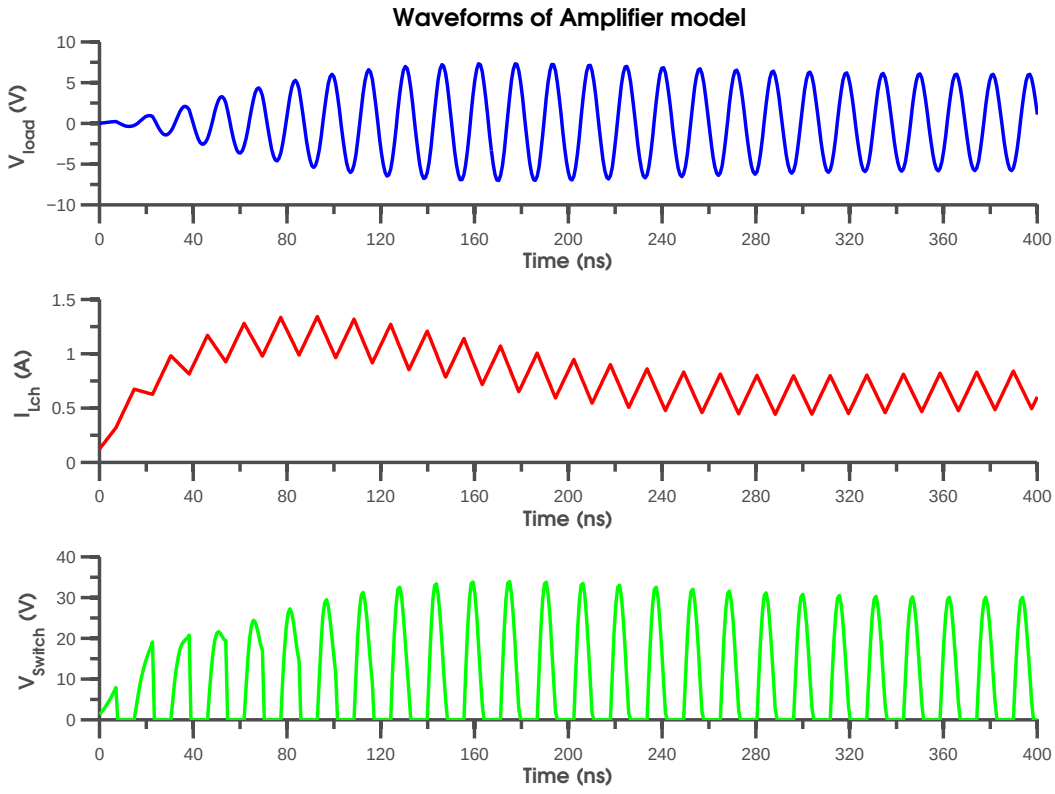


Figure 4.16: Load voltage, Choke current and Switch voltage in Matlab model simulation

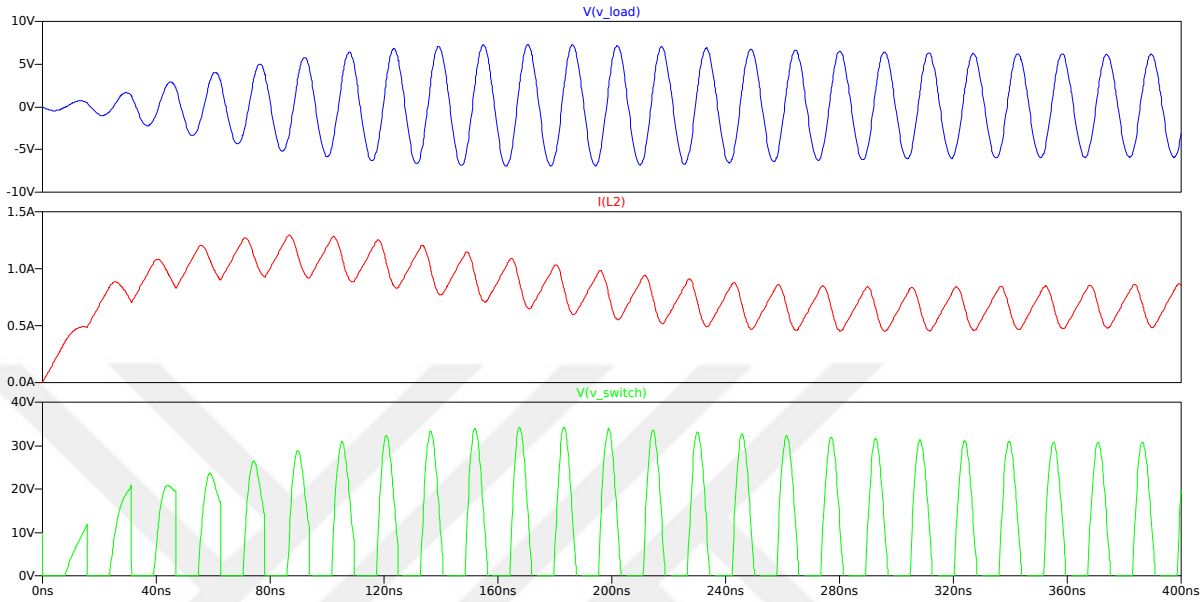


Figure 4.17: Load voltage, Choke current and Switch voltage in LT spice simulation

4.4.1.2 Simulation results

Next step was to try to modulate the desired waveform by varying the switching pattern and predicting N bit decisions forward. The results show that as increasing the number of forward bits a better decision is taken. This comes with a computational cost. At the same time increasing the switching frequency, improves the matching to the desired pulse. The simulations are for 50μs long *Sinc* pulse with 2 lobes, with a carrier frequency 30MHz. This frequency was selected in order to compare the simulations and experimental results, since for d=4 the amplifier operates at 120Mhz, close to the limits of operation. In the figures below desired and generated pulses are shown:

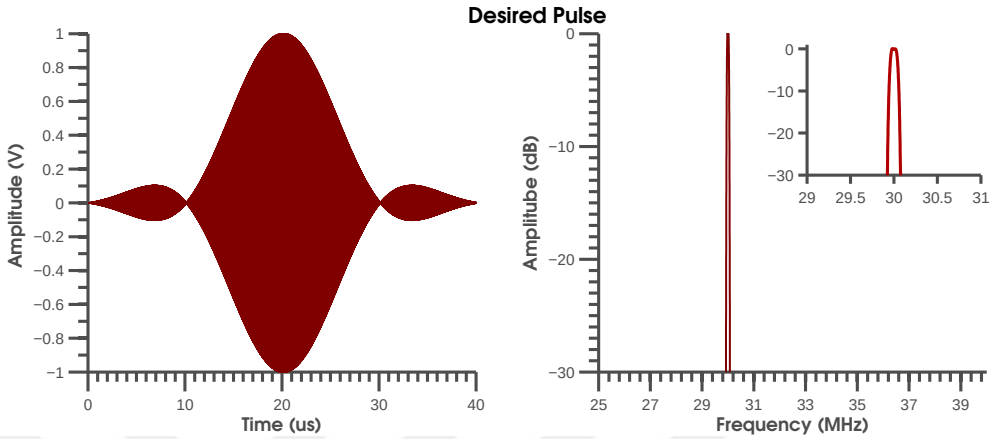


Figure 4.18: Desired pulse and spectrum

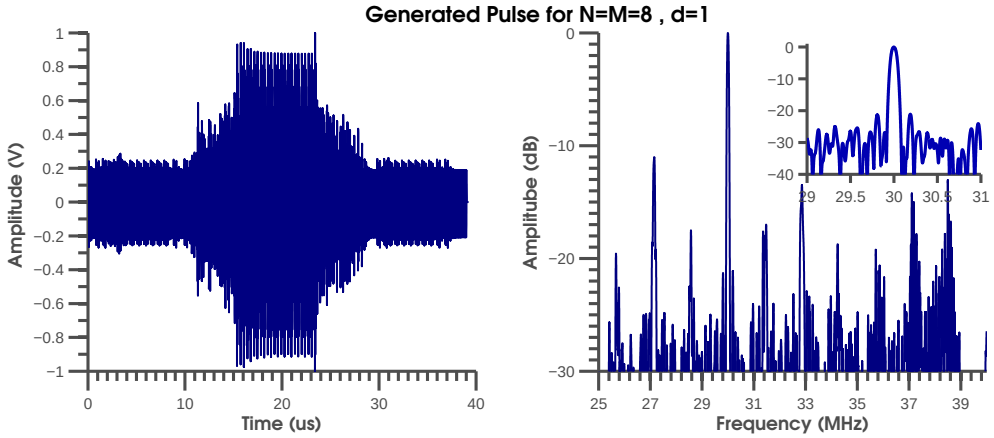


Figure 4.19: Generated pulse and spectrum for N=M=8, d=1

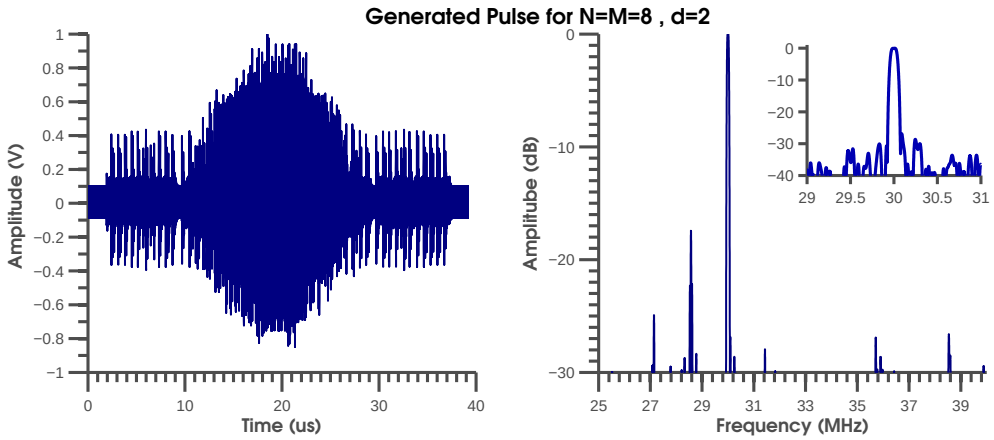


Figure 4.20: Generated pulse and spectrum for N=M=8, d=2

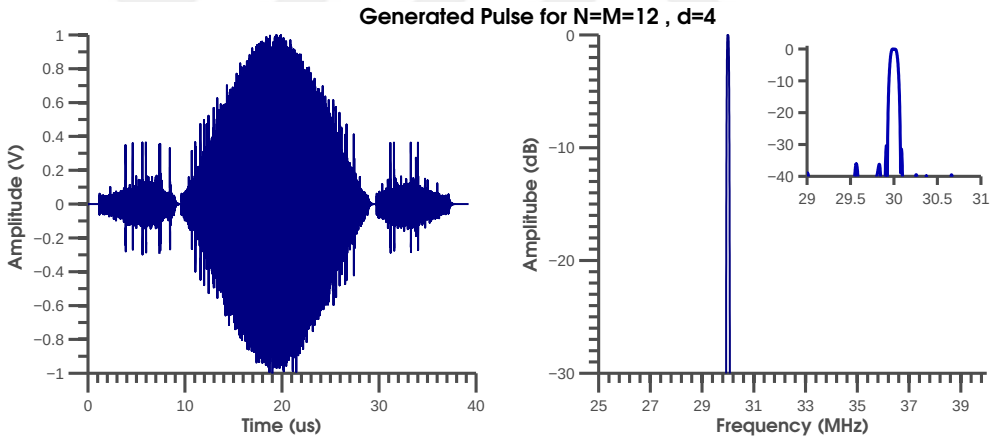


Figure 4.21: Generated pulse and spectrum for N=M=12, d=4

4.4.1.3 Experimental results

The bitstream generated from the simulation in MATLAB was tested in one of the amplifiers. The results presented below are for d=1,2,4 cases with a *Sinc* pulse of 40μs length. The tests showed close results with simulation in MATLAB.

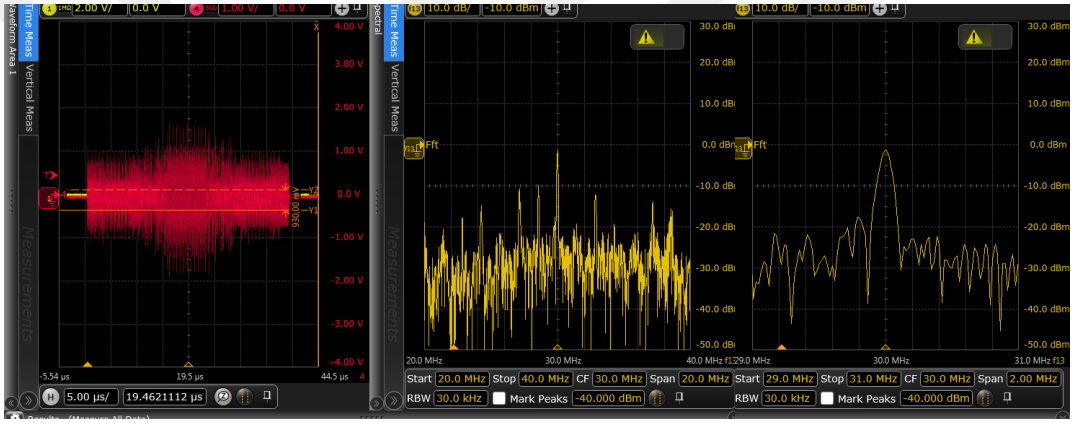


Figure 4.22: Generated pulse and spectrum for N=M=8, d=1

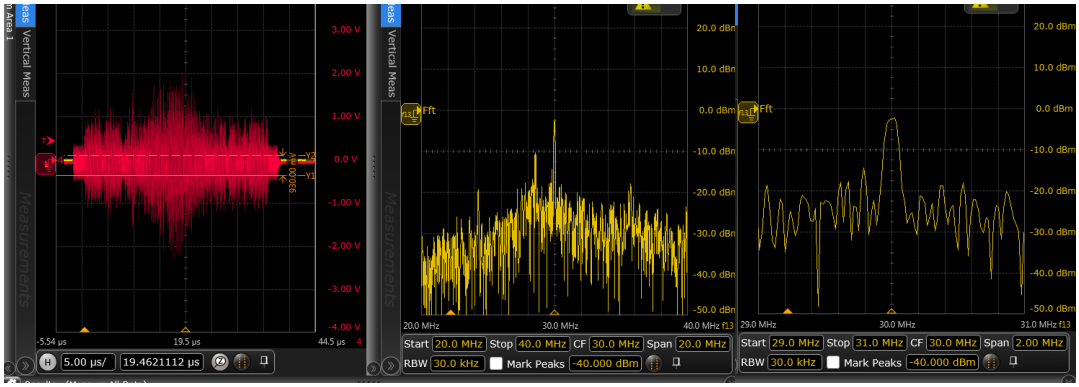


Figure 4.23: Generated pulse and spectrum for N=M=8, d=2

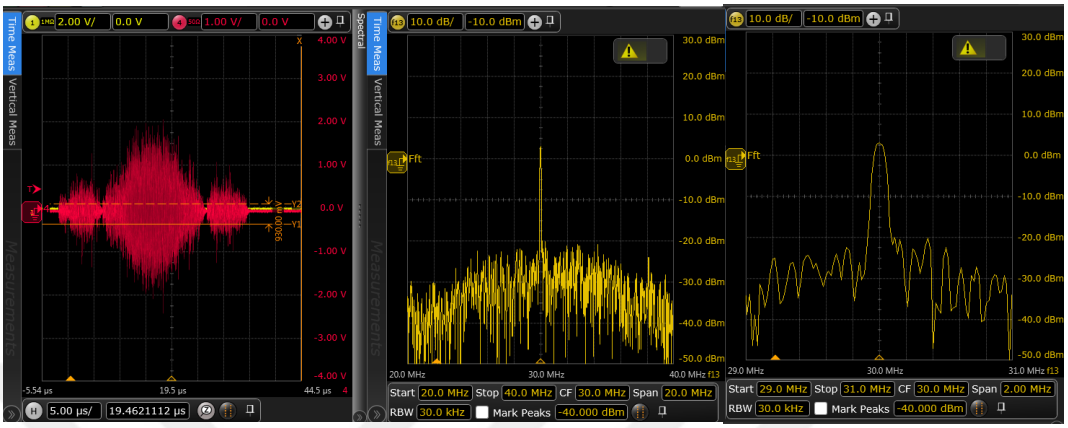


Figure 4.24: Generated pulse and spectrum for N=M=12, d=4

4.4.2 Supply modulation

4.4.2.1 Experimental results

4.4.2.1.1 Pulse generation Different Pulse shapes available in the scanner were compared with the ones generated from designed amplifier. In Fig. 4.25 *Rect*, *Triangle*, *Linear and Gauss* pulses of 1.5 *ms* length were generated both from manufacture prototype and scanners amplifiers.

Next a *Sinc* pulse from the systems amplifier was compared to designed amplifier. This pulse of length 1.5 ms is windowed with a Tukey window with parameter α=1. The *Sinc* obtained from the scanner was of length 2.7τ were τ i half the length of the main lobe. In our case τ=555.5μ . In Fig. 4.26 this *Sinc* pulse and its spectrum is illustrated. Additionally, generated pulse from our amplifier for 3T at 123.28Mhz .

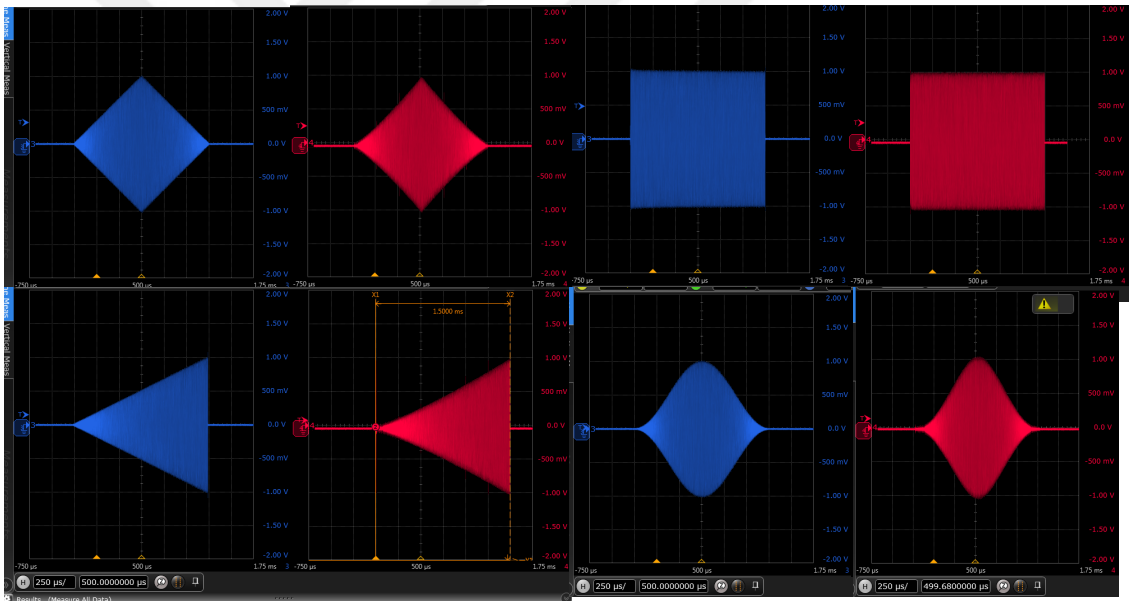


Figure 4.25: Different pulse shapes shown. Blue - Analogic system, Red - Class E amplifier

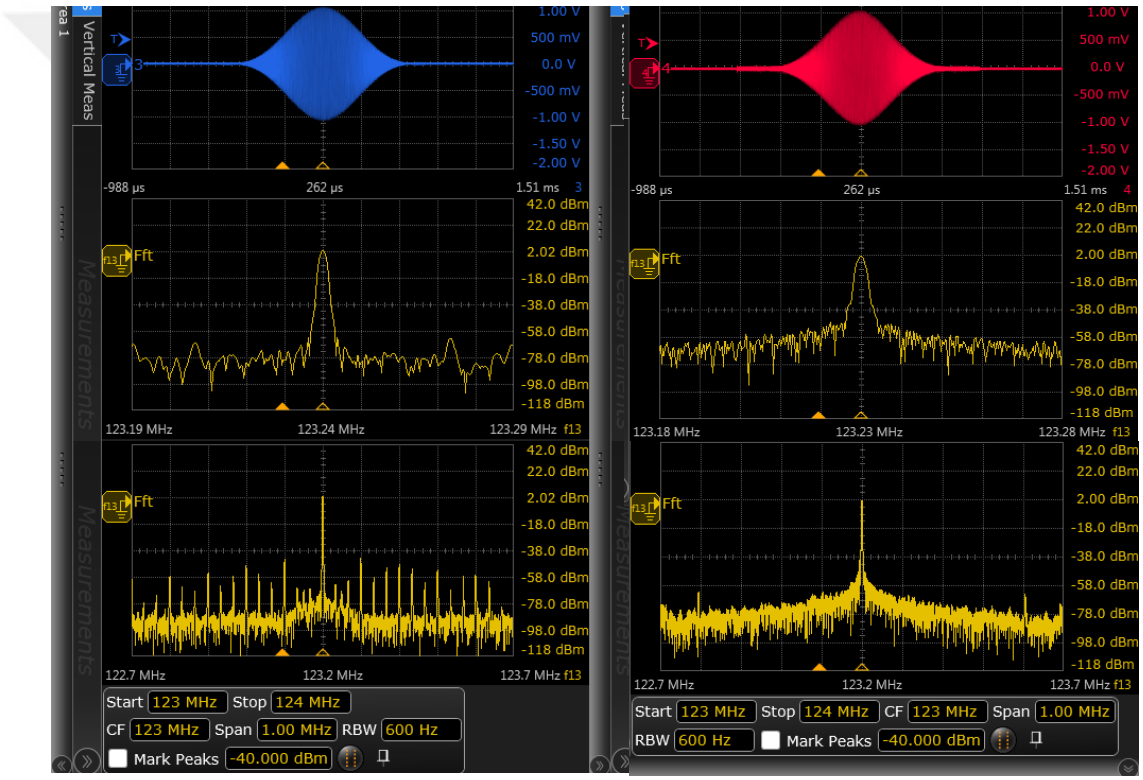


Figure 4.26: Sinc pulse shape shown. Blue - Analogic system, Red - Class E amplifier

4.5 MRI experiment results

4.5.1 System amplifier vs Class E amplifier

The results for 3T Siemens Tim Trio scanner results are shown here. In the 3D sequence it can be observed both within slice excitation, and the slice profile. System amplifier results with the loops matched at 50Ω was compared with developed amplifier in two element transmit with the same loops. The results are for both amplifiers transmitting and the case when only one of them is transmitting, in order to observe coupling.

Figure 4.27: Experimental setup in the scanner room

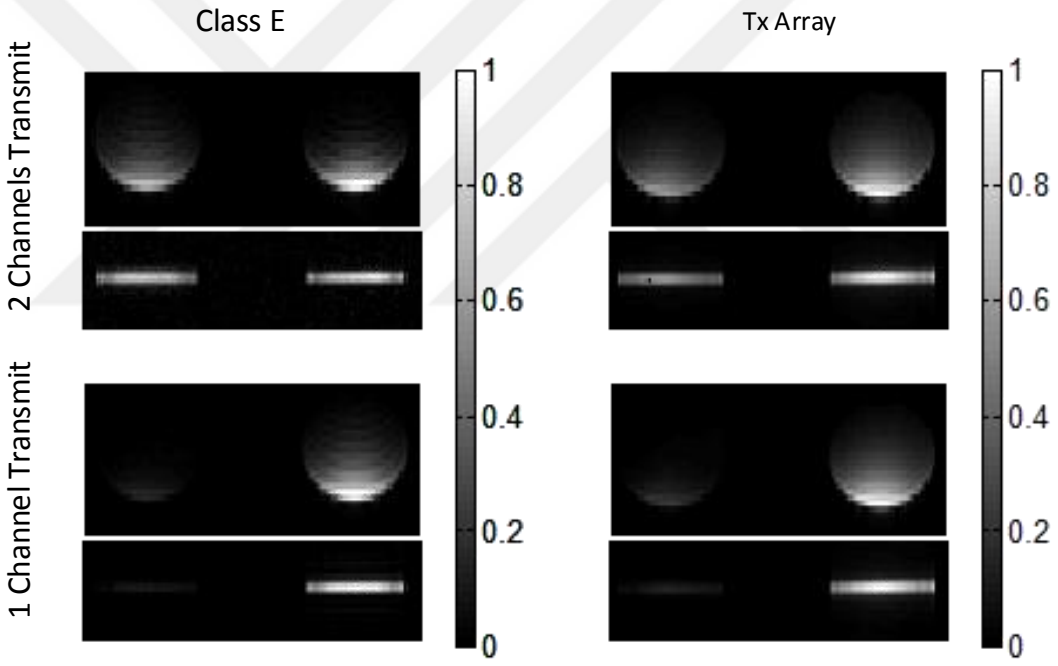


Figure 4.28: Slice selection results between system amplifier and Class-E amplifier operation

Chapter 5

Discussion and Conclusion

In this work a high efficiency Class-E amplifier for RF excitation in MRI is presented. The amplifier is designed for individual elements on a 36 element transmit array system, where the independent driving of each element would mean more degrees of freedom for arbitrary local excitation. Initially this amplifier design was presented with an efficiency of 65% in a conference presentation [25]. In further developed version, the amplifier was able to deliver output power of $100W$ with measured efficiencies up to 88%. In spite of amplifiers high efficiency, there was no need for a heat sink when operated in burst mode. Designing each amplifier for individual element, results in size reduction and splitting the power needed from a single amplifier.

The amplifier was driven with a wideband driver consuming at maximum $1.1W$ switching the amplifier at 123MHz. The driver, controlled by an FPGA, having a rise-time and fall-time below 2ns, can be used to switch also at lower frequency, for lower field designs (1.5T). In order to drive higher input capacitance mosfets for more power the last stage LDMOS switches were changed with more powerful ones, able to switch up 300pF. This means that a switch able to deliver 300W (BLF573) could be driven too. So, the modular design makes possible for the driver to be flexible for higher power or lower frequency implementation with

small changes. The driver part size relatively small, is an important feature because inside the bore of the scanner space is very important. The component cost of the amplifier is approximately 170 US dollar. In the amplifier presented, instead of the RF choke a short transmission line was used. The short transmission line behaved as a choke inductor, showing coherence with simulations. Different length transmission lines were tested. Also a higher characteristics impedance ($Zo \approx 100\Omega$) was tested. In one version of the amplifiers the short transmission line was implemented as strip line in the PCB, saving further space.

In the pule generation a digital control was implemented. The more conventional method supply modulation showed that it is a more preferable choice due to its separate control of the phase and amplitude, high efficiency performance and generated pulse quality. In second method, we introduced a new idea: control both amplitude and carrier frequency of a desired pulse by changing the switching pattern in the nonlinear amplifier, under a constant V_{dd}. A model for the amplifier was developed in MATLAB. After comparing the model with computer simulation, it was used to generate desired pulse. The bitstream was generated by using N-bit forward and switching at f_o, $2f_o$, $4f_o$. In this way we observed that the generated the desired pulse better at the highest switching frequency. The aim was to remove the supply modulation block components in order to reduce cost, complexity of the circuit and deliver an equivalent performance. However, we observe that $4f_o$ switching frequency is required for a better pulse shape. The driver couldn't handle 500MHz switching frequency, so we tested at a lower output frequency, 30MHz. In this case the driver was switched at most 120 MHz frequency. Promising results are obtained but further work has to be done on this side in order to obtain results competing with the amplifier with supply modulation block amplifier.

One issue in the amplifier design was the varying C_{ds} (drain to source capacitance). Since it is changing according to the bias it may bring phase variation in different bias and change the efficiency since it is paralleled with one coil matching capacitor. This is a well known issue [26]. The problem was attempted to be minimized by designing the coil and its elements such that the parallel capacitor is larger than C_{ds} variation, decreasing its overall impact. In MRI experiment

it was shown that the developed two element system was able two select slice similarly to the scanners own system. On the future, it is necessary to move from two element in 36 and test multiple amplifiers at the same time . The coupling between the circuits and the coils is to be tested. On similar works [15, 27], it is shown that since it is a current mode switching amplifier, there is an inherent decoupling between coils and good results are obtained. Additionally, the target output operation with 300W per amplifier is to be tested. Current driver is able to operate such a switch, so no significant changes have to be done. A challenge in the future would be two control all of the 36 elements together properly and be sure they do not interfere on each others operation.

From the manufacturer point of view we believe that this work will lead to a more flexible, efficient and lower cost system. Additionally, we expect it to be a highly controllable powerful tool for ongoing studies including but not limited to reduce of implant heating and SAR given to the patients.

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