77 GHz SiGe BiCMOS FMCW RADAR for Automotive Applications

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77 GHz SiGe BiCMOS FMCW RADAR for Automotive Applications

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Keywords: FMCW, 77 GHz Automotive RADAR, long range RADAR, SiGe BiCMOS, mm-wave Integrated Circuits.

Abstract

SiGe BiCMOS technologies have been improved such that they offer comparable, sometimes even better RF performances with respect to their counterparts, especially III-V technologies. Further, SiGe BiCMOS technologies can integrate CMOS transistors and SiGe HBTs on the same chip. These advancements make possible to implement IC designs with low-cost and high integration. Also, due to the increasing demand for compact system designs with low-cost, and low-power-consumption, millimeter-wave systems became attractive for both industry and academia. These developments have paved the way for millimeter-wave systems. Therefore, in this thesis work, a 77 GHz SiGe BiCMOS FMCW Monostatic RADAR for automotive applications is presented. The system was designed and implemented with IHP's 0.13 μm SiGe BiCMOS SG13G2 technology which offers HBTs with f_t/f_{max} of 300 GHz/500 GHz.

The schematic designs and implementation of each sub-block and the overall system were shown. Then, the simulation results for all the sub-blocks and the system were presented. The total chip area for the system is 5.05 mm^2. The total power consumption of the system is 0.32 mW. The system achieves 8.5 dBm output power with only one TX channel. The simulated NF of the RX-channel is 9.1 dB and RX-gain is 18 dB. The simulation results show that the designed system can detect targets up to 180m distance with a maximum velocity of 170km/h with accuracy. Also, the designed system can separately identify two targets with a range resolution of 15 cm. This work is the first demonstration of a 77 GHz long-range-RADAR designed with an EBD.

Otomotiv Uygulamaları İçin
77 GHz SiGe BiCMOS FMCW RADAR

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Özet

SiGe BiCMOS teknolojileri benzerlerine, özellikle de III-V teknolojilerine kıyasla benzer, bazen daha iyi RF performansları sunacak şekilde geliştirilmiştir. Ayrıca, SiGe BiCMOS teknolojileri, CMOS transistörlerini ve SiGe HBT'leri aynı çip üstüne entegre edebilmektedir. Bu gelişmeler, IC tasarımlarını düşük maliyetli ve yüksek entegrasyonla gerçekleştirmeyi mümkün kılmaktadır. Ayrıca, düşük maliyetli ve düşük güç tüketimli kompakt sistem tasarımlarına olan talebin artması nedeniyle milimetre dalga sistemleri hem endüstri hem de akademi için cazip hale geldi. Bu gelişmeler milimetre dalga sistemlerinin önünü açtı. Bu nedenle, bu tez çalışmasında, otomotiv uygulamaları için 77 GHz SiGe BiCMOS FMCW Monostatik RADAR sunulmuştur. Sistem, IHP'nin f_t/f_{max} 300 GHz/500 GHz'lik HBT'ler sunan 0.13 μm SiGe BiCMOS SG13G2 teknolojisi ile tasarlanmış ve gerçeklenmiştir.

Her bir alt bloğun ve sistemin şematik tasarımları ve uygulaması gösterilmiştir. Daha sonra tüm alt bloklar ve sistem için simülasyon sonuçları sunulmuştur. Sistemin toplam yonga alanı 5.05 mm^2'dir. Sistemin toplam güç tüketimi 0.32 mW'tır. Sistem, yalnızca bir TX kanalıyla 8.5 dBm çıkış gücü sağlar. RX kanalının simüle edilmiş NF'si 9.1 dB'dir ve RX-kazancı 18 dB'dir. Simülasyon sonuçları, tasarlanan sistemin maksimum 170km/s hızda 180m mesafeye kadar hedefleri hassasiyetle tespit edebildiğini göstermektedir. Ayrıca, tasarlanan sistem 15 cm aralık çözünürlüğünde iki hedefi ayrı ayrı tanımlayabilir. Bu çalışma, EBD ile tasarlanan 77 GHz uzun menzilli RADAR'ın ilk gösterimidir.

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List of Abbreviations

ADC	Analog to Digital Converter
ANT	Antenna
BAL	Balance
BEOL	Back-End-of-Line
BJT	Bipolar Junction Transistor
BV_{CEO}	Collector-Emitter Breakdown Voltage
CB	Common-Base
CE	Common-Emitter
CMOS	Complementary Metal-Oxide-Semiconductor
CW	Continuous Wave
EBD	Electrical Balance Duplexer
FFT	Fast Fourier Transform
FMCW	Frequency Modulated Continuous Wave
GaAs	Gallium-Arsenide
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
IF	Intermediate Frequency
IL	Insertion Loss
InP	Indium-Phosphide
LNA	Low Noise Amplifier
LO	Local Oscillator
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
NEP	Noise Equivalent Power
NF	Noise Figure
PA	Power Amplifier
PAE	Power-Added-Efficiency
PD	Power Detector
PLL	Phased Locked Loop
RADAR	Radio Detecting And Ranging
RCS	RADAR Cross Section
RF	Radio Frequency
RX	Receiver
SAW	Surface Acoustic Wave
SiGe	Silicon-Germanium
SNR	Signal to Noise Ratio
TX	Transmitter
VCO	Voltage Controlled Oscillator
VSWR	Voltage Standing Wave Ratio
WWII	World War II

1 Introduction

1.1 Brief History of RADARs

Humankind has been using radio detection and ranging (RADAR) systems for almost two centuries in many applications to detect objects such as military vehicles, planes, ships or satellites and gather information about them. Generally, a RADAR works by sending out a type of an electromagnetic waveform and gathers back the reflection of that waveform which reflected from objects. RADAR systems are used to improve the capability of sensing the environment, specifically in terms of the motion. Although RADAR systems cannot provide detailed or sophisticated visions of the objects of interest as a human eye or cameras, they can operate in hard environmental conditions such as darkness, haze, rain, fog, snow and smoke. Further, RADAR systems have an ability to measure the position, location, distance, and velocity of an object. This is probably the most important attribute of a RADAR system. Therefore, RADAR systems surpass other systems in detecting objects and targets [7].

The basic idea of RADAR originates in the experiments done on electromagnetic waves and radiations which were performed by Heinrich Hertz in late 1880s. Hertz implemented and verified the theoretical work of James Maxwell. Based on the principles that Hertz used, Cristian Hülsmeyer invented the first RADAR system "Telemobiloskop" in 1904 [8]. Until World War II (WWII), there were minor innovations about RADAR systems. The only noticeable development occurred during the 1930s. The United States, Great Britain, Germany, France, The Soviet Union, Italy, the Netherlands, and Japan began experiments on using radio signals for aircraft detection. The first microwave RADAR was invented in MIT Radiation Laboratory at Cambridge during the WWII, which was a significant development [9]. Although the RADAR technology slowed after the WWII., new concepts were published in time and lead the new technologies and ideas in RADAR technology. Phased array [10], pulsed [11], continuous-wave [12] and SAR imaging [13] RADAR systems are the major RADAR types which are used in both civilian and military applications within today's technologies.

1.2 Evolution of Automotive RADARs

One of the most primary applications that RADARs have been using is automobiles. The first commercial automotive RADAR was a distance warning RADAR at 35 GHz built by AEG-Telefunken at 1975 [1], which is shown in Figure 1(a). There were other products from other manufacturers until the middle of the 1980s. All these RADARs were used for comfort and luxury in cars. However, the paradigm had changed from comfort to safety. Because from the beginning 1990s, the number of road deaths was increased. Therefore, for the first time in history, a collision warning system at 24 GHz was developed by EATON-VORAD in 1996 [1], which is shown in Figure 1(b). 24 GHz automobile RADARs were standardized as short-range collision warning systems for a couple of decades.

Recent developments in the automobile industry increased the demands for new and specialized RADARs. There are already many different RADARs in an automobile to help and warn the drivers, as shown in Figure 2. Besides, many companies are currently working on self-driving vehicles [14]. This will change the overall approach to automotive RADARs. RADARs will take a vital role in controlling the vehicle while driving instead of assisting the driver only. However, 24 GHz frequency band will not be available after January 1, 2022, because of the regulations made by the European Telecommunications Standards Institute (ETSI) [15] Also, the increasing demands for higher performance in RADAR applications makes 24 GHz frequency band unattractive for new experiments. Due to the low atmospheric attenuation, 76-81 GHz frequency band was selected as the next-generation automotive RADARs as shown in Figure 3. Also, this frequency band offers more bandwidth than 24 GHz frequency band, thus the measurement resolution increases, which will be detailly analyzed. Further, it will be possible to implement short, middle, or long-range automotive RADARs within the same frequency band. Furthermore, antenna sizes get smaller. Therefore the cost decreases and highly integrated compact designs are enabled [16].

RADARs can be classified into two main categories with respect to their transmitted waveforms: pulsed RADARs and continuous wave RADARs [17]. Pulsed RADARs transmit a burst signal, which is an electromagnetic energy within a very short time interval and receive the echo of the transmitted signal. The time dif-



Figure 1: Telefunken RADAR [1] (a) first collusion RADAR [1] (b) and Bosch LRR [2] (c)

ference between the received and transmitted signal contains the range information about the target, which can be calculated easily. Also, the range resolution can be determined by only adjusting the pulse width. On the other hand, continuous wave RADARs transmit a sinusoidal wave with constant frequency, if it is not modulated, and receive the reflected version of the transmitted signal. Since the signal is continuous, the reflected and transmitted signals have no significant starting points, hence it is not possible to measure the range of an object directly. If the wave is not a modulated signal, there is no possibility to measure the range of an object. If the wave is a modulated signal, it is not possible to determine the range resolution by adjusting the pulse width, because there is no pulse since the wave is continuous.

Although pulsed RADARs seem to be more beneficial then modulated CW RADARs, the latter is preferred for automotive RADARs. Pulsed RADARs require large bandwidth to detect the objects, which increases energy consumption. Since a pulse is transmitted, higher power is required to generate the pulse. These drawbacks make pulse RADARs more expensive than CW RADARs. Also, it is not possible to listen while transmitting the signal with pulsed RADARs. Thus they are not able to operate half of the time. Therefore, CW RADARs are utilized for automotive RADAR systems since the last decade.

CW RADARs are not capable of detecting the range of an object, because an unmodulated signal is transmitted from the RADAR, which has a narrow bandwidth. The bandwidth of the transmitted signal can be broadened by using modulation. Also, to be able to measure range, a kind time marking must be applied to the carrier such that the time difference between transmitted and received signal can be measured. The modulation can be applied to amplitude, phase, or frequency.

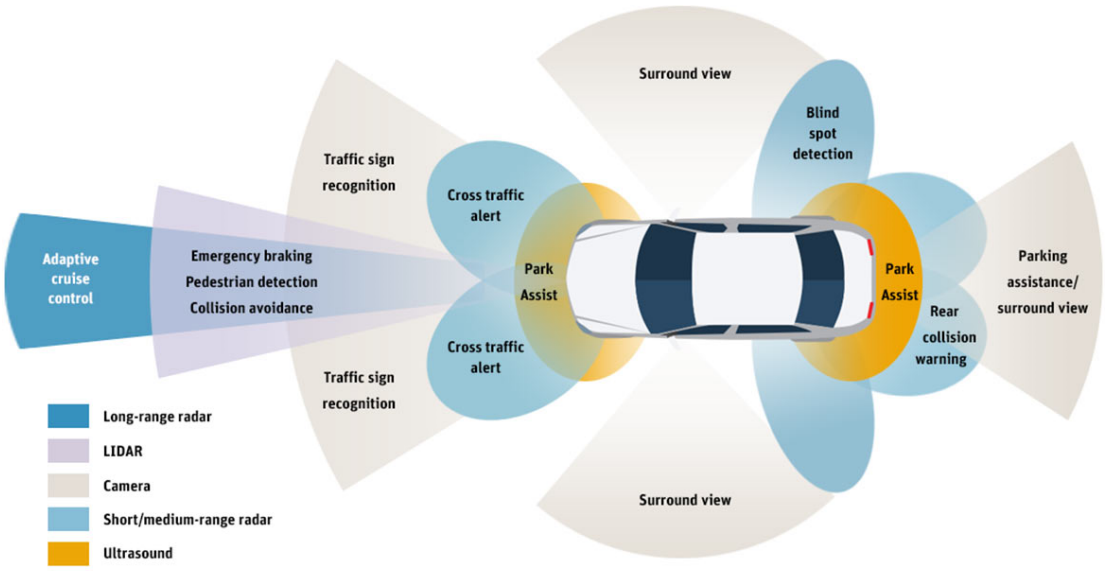


Figure 2: Types of RADAR systems in today's cars [3]

Among these modulation types, frequency modulation is very popular because of its superior advantages. FMCW RADARs can detect and measure targets from small ranges to long ranges. Also, a simultaneous measurement can be done on the range and relative speed of multiple objects. Further, these RADARs have the capability of detecting small distance changes. Signal processing on the measurement data is realized at IF level, which simplifies the complexity of the required hardware and computation to calculate the desired result [18].

Many companies have been developing FMCW RADARs for automobile applications with different technologies due to the considerably recent advancements and necessities mentioned. Texas Instruments developed a single 76-81 GHz chip with RFCMOS process [19] whereas NXP Semiconductors implemented different 77 GHz RADAR chipsets for different measurement ranges with SiGe BiCMOS technology [20]. Further, Infineon Technologies produced a 77 GHz long-range RADAR for automotive with CMOS technology [21].

1.3 SiGe BiCMOS Technology

Currently, IC technologies can be categorized into three different groups. III-V technologies, CMOS technology, and SiGe BiCMOS technology. III-V technologies such as gallium-arsenide (GaAs) and indium-phosphate (InP) surpass their coun-

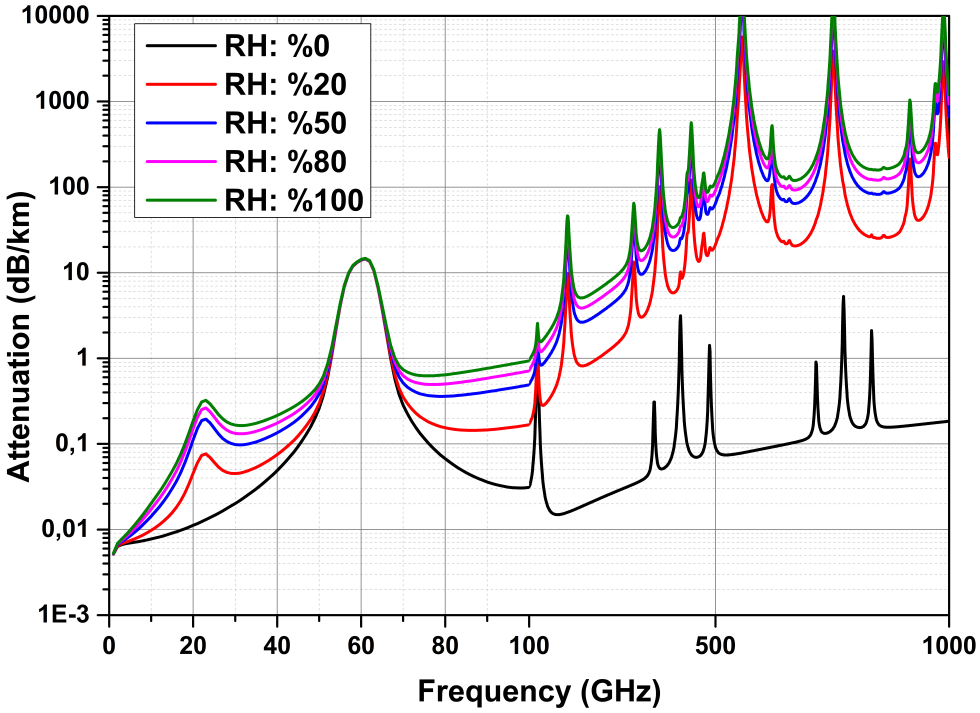


Figure 3: Atmospheric attenuation with different relative humidity (RH) levels. [4]

terparts in terms of RF performance. The transistors belong to these technologies have higher gains, lower noise figures, and higher output powers. Also, the process variations are minimal with III-V technologies when compared with others, which gives a considerable advantage to the designer. However, these advantages require more expensive fabrication cost and a larger die area. Further, the integrity with digital circuits is not possible. These technologies are used in systems that require much higher output powers, which are mostly military applications.

CMOS technologies have improved recently, especially considering their RF performance. CMOS technologies are the cheapest among all three; thus, products for consumer electronics are fabricated with CMOS technologies. Also, these technologies dominate digital integrated circuits. Despite providing these advantages, CMOS technologies have too much process variation. The behavior of passive devices and transistors differ from process to process. This decreases the reliability of the designed circuit because simulation and measurement results can have a mismatch.

SiGe BiCMOS technologies have shown significant advancement through last the two decades. Nowadays, SiGe BiCMOS technologies can have comparable, and even

Table 1: Performance comparison of different semiconductor technologies for radio frequency integrated circuits (Excellent: ++; Very Good: +; Good: 0; Fair: -; Poor: --) [6]

Performance Metric	**SiGe HBT**	**SiGe BJT**	**Si CMOS**	**III-V MESFET**	**III-V HBT**	**III-V HEMT**
Frequency Response	+	0	0	+	++	++
1/f and Phase Noise	++	+	–	– –	0	– –
Broadband Noise	+	0	0	+	+	++
Linearity	+	+	+	++	+	++
Output Conductance	++	+	–	–	++	–
Transconductance	++	++	– –	–	++	–
Power Dissipation	++	+	–	–	+	0
CMOS Integration	++	++	N/A	– –	– –	– –
IC cost	0	0	+	–	–	– –

better RF performances than III-V technologies within smaller die areas. Also, it is possible to integrate digital and RF circuits on the same chip, which allows having cost-effective and more convenient systems with SiGe BiCMOS technology. Also, process variation is less than CMOS technologies, which enables more consistent chips with their simulations. As a result, SiGe BiCMOS technologies perform in between these two other counterparts without sacrificing RF performance. Table 1 compares SiGe BiCMOS technology with other two counterparts.

SiGe BiCMOS technology depends on bandgap engineering when creating the base region of the BJT. Lower bandgap energy enables more electrons or holes to break their bonds and become ready to contribute to the current generation. The base region of the BJT transistor is formed with SiGe compound, which has lower bandgap energy than silicon itself. Hence, higher electron injection is achieved, which results in higher current gain β. Further, the diffusion speed of minority carriers is increased, and thus, the minority carriers in the base region are accelerated. By this way, the base transit time τ_b is reduced. Furthermore, the parasitic effects of the process are reduced by utilizing small-sized and vertically and laterally scaled structure [6]. The high-frequency performance of the integrated circuit technologies is mainly determined by two figures of merit. One of them is maximum oscillation frequency f_{max} and the other one is unity current gain frequency, also known as transition frequency f_t. The maximum oscillation frequency of a transistor is the frequency where the power gain of the transistor is equal to unity. f_{max} can be cal-

culated by using equation 1 where r_b is the base resistance of a BJT. On the other hand, the transition frequency of a transistor is the frequency where the current gain is equal to one.

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_\mu r_b}} \tag{1}$$

The current gain is defined as the short circuit gain of the common source topology. The f_t of a BJT can be calculated as shown in equation 2 where τ_b is the base transmit time, τ_c is the collector transmit time, gm is the transconductance of the transistor, C_π and C_μ are the parasitic capacitances of a BJT and r_e and r_c are the parasitic resistances of a BJT.

$$f_t = \frac{1}{2\pi}\left(\tau_b + \tau_c + \frac{1}{g_m}\left(C_\pi + C_\mu\right) + \left(r_e + r_c\right)C_\mu\right)^{-1} \tag{2}$$

The f_t and f_{max} of a BJT can be improved by utilizing the advantages of the SiGe compound as mentioned. Also, improving these two figures of merit improves the gain and decreases the noise figure that can be achieved. The relationship between the minimum noise figure and f_t is given in equation 3.

$$NF_{min} = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2J_c}{V_t}\left(r_e + r_b\right)\left(\frac{f^2}{f_t^2} + \frac{1}{\beta_{DC}}\right) + \frac{n^2}{\beta_{DC}}} \tag{3}$$

Considering the benefits mentioned above, SiGe BiCMOS technology offers low-cost, high integration with digital circuits system-on-chip solutions for today's and future's millimeter-wave technologies than its counterparts. In this thesis work, IHP Microelectronics 0.13 μm SG13G2 technology process, which offers HBTs with $f_t/f_{max}/BV_{ceo}$ of 300 GHz/500 GHz/1.6 V was chosen as the SiGe BiCMOS technology [22]. The detailed cross-section of the SG13G2 process is given in Figure 4. The back-end-of-line (BEOL) consists of seven metal layers. The first five layers (M1-M5) are thin metallization layers, whereas the two thick layers on the top (TM1-TM2) are used for high quality on-chip inductors and low loss transmission lines. Further, BEOL includes MIM capacitors and three different polysilicon resistors.

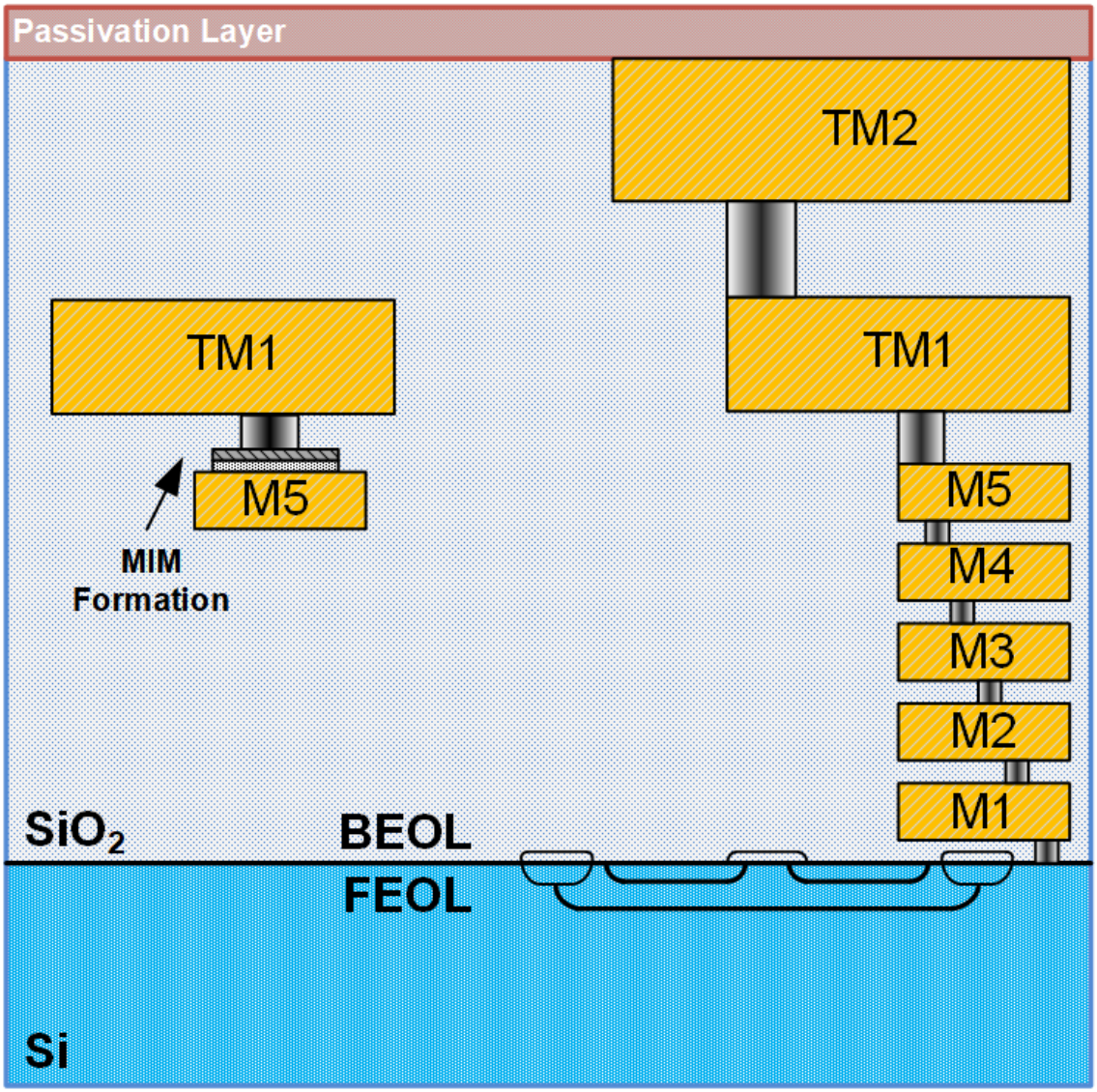


Figure 4: Cross-section view of IHP 0.13μm SiGe BiCMOS SG13G2 technology [5].

1.4 Motivation

Due to the recent advancements in SiGe BiCMOS technologies and new regulations and requirements in the automotive industry as mentioned in the previous sections, there has been a growing interest in designing millimeter-wave automotive RADAR systems by both the industry and the academia. As mentioned before, FMCW type RADAR systems surpass its counterparts. Also, SiGe BiCMOS technologies are the best candidate for designing FMCW RADAR systems. Although III-V technologies provide much higher output powers than SiGe BiCMOS technologies, FMCW RADARs require low transmit powers to operate; thus, SiGe BiCMOS technologies can provide enough performance with lower-cost and more compact

sizes than III-V technologies. Also, FMCW RADAR systems require computation on the measured data to provide information which is done by digital circuits. Therefore, high integration with RF and digital domains is essential, and SiGe BiCMOS technologies fulfill this requirement even though CMOS technologies offer the best integrity within all technology groups. As mentioned before, CMOS technologies have high mismatches and process variations from process to process.

In this thesis study, the main goal was designing a 77 GHz Monostatic FMCW Long Range RADAR system for automobile applications. The monostatic approach has a smaller area than the bistatic version, due to having less number of antennas. The monostatic structure was realized by utilizing an electrical balance duplexer (EBD) for the first time to create the required isolation between the receiver and transmitter chains.

1.5 Organization

This thesis consists of four chapters, and they are organized as follows. Chapter 2 states the fundamentals of FMCW concept. Implementation of the range, velocity, and angle detection is analyzed in detail. The RADAR equations and RCS calculations are presented.

Chapter 3 introduces the designed system, its performance parameters, and sub-blocks. Then, each sub-block is reported with their design techniques and simulation results. Key sub-blocks for the system are compared with the state-of-the-art counterparts. Finally, the overall system is reported with its simulation results and compared with similar studies from the literature and products available in the market.

Chapter 4 concludes the thesis with the summary of the work and provides some additional discussion and suggestions to improve the work presented and solve the existing problems in the literature for future studies.

2 Fundamentals of FMCW RADARs

This chapter includes all the required theoretical and mathematical analysis and information about FMCW RADARs. First, the architectures for FMCW RADARs and the method of how frequency modulation are explained. Then, range, relative velocity, and angle detection are analyzed in detail. Signal processing for computation of the measurement data and commonly used algorithms are explained.

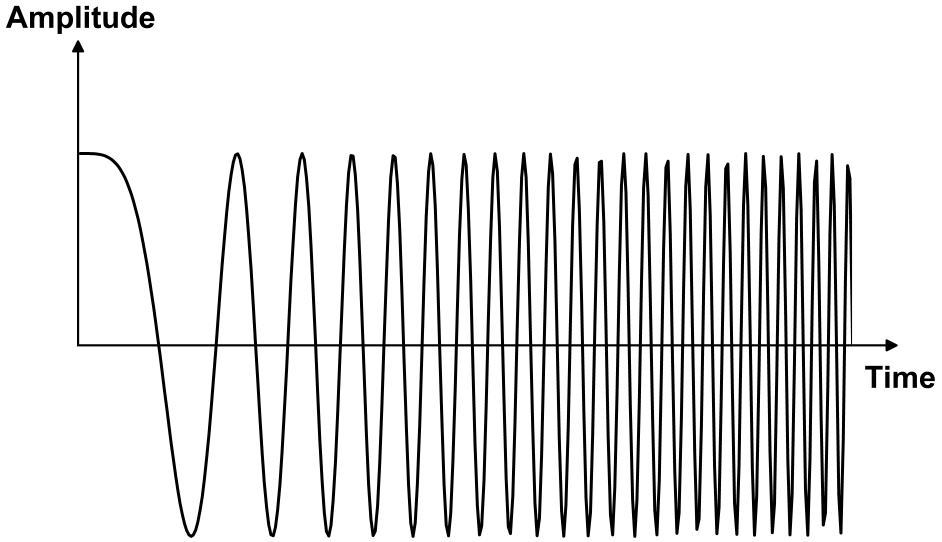
2.1 FMCW Properties

The fundamental operation lies behind in any FMCW RADAR is frequency modulation. Frequency modulation is required to detect the range of objects, as mentioned earlier. Frequency modulation is realized with a "chirp" signal. A chirp signal is a sinusoidal signal whose frequency is changing with respect to time, as shown in Figure 5.

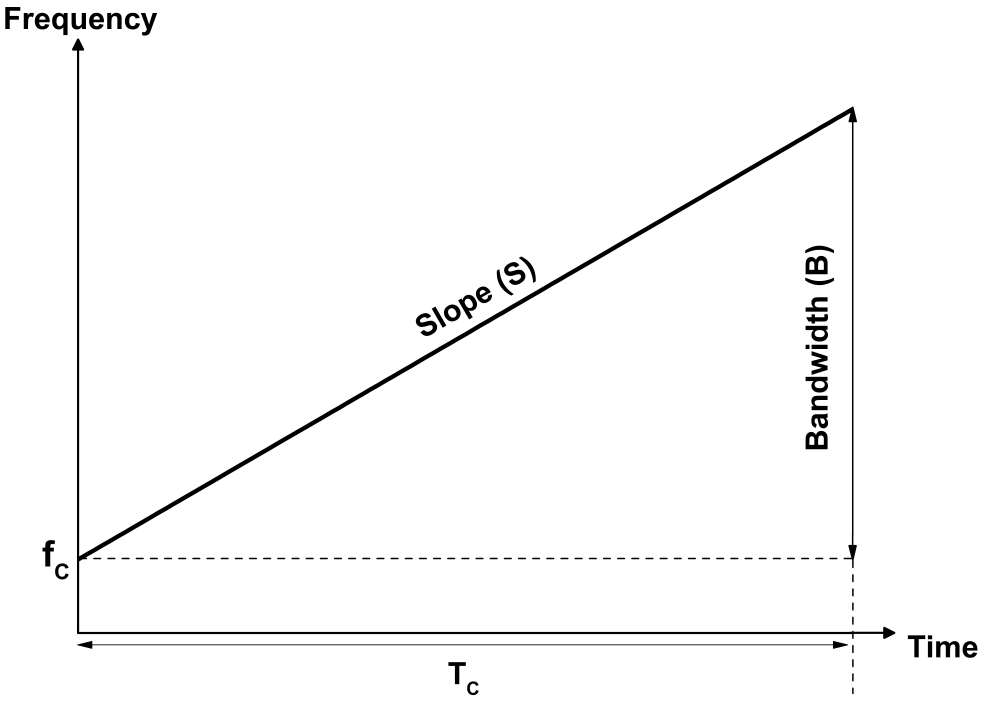
A chirp signal has four critical characteristics that describe itself and makes detection possible for FMCW RADAR systems. The first one is the ramp frequency f_c, which is the starting point of the chirp signal, and also RF bandwidth. The other one is the bandwidth of the chirp B, which is the interval that the chirp is modulated and exactly the same with RF bandwidth of the system. The other characteristic of a chirp signal is chirp duration T_c which indicates the dedicated time for a single chirp cycle. The last one is the slope S of the chirp. This represents the rate of frequency change per unit time for the chirp, which can be calculated as given in equation 4.

$$S = \frac{B}{T_c} \tag{4}$$

Understanding the mechanisms behind a chirp signal is vital because FMCW RADARs operate and detect objects thanks to chirp signals. Also, it will be clearer to understand how a general FMCW RADAR operates. In general, RADAR systems are categorized into two groups: monostatic and bistatic RADARs. The names were designated with respect to the number of antennas. As the names indicate, monostatic RADAR systems have a single antenna, whereas bistatic RADAR systems have two antennas. The block diagrams for FMCW RADARs with both configurations



(a)



(b)

,

Figure 5: (a) A sinusoidal chirp signal, and (b) corresponding behavior on frequency domain.

are given in Figure 6.

The working principle of an FMCW RADAR system can be described as follows. Initially, a chirp signal is generated by a signal source. The chirp signal is amplified and transmitted. Then, the reflection of the transmitted signal is collected by the receiver. The signal is amplified and then mixed with the original chirp signal to generate the IF signal, which contains the information about the environment. Later, the generated IF signal is filtered to remove unwanted frequency components and then digitalized to be processed with different algorithms. The algorithms analyze the digitalized IF signal by performing mathematical calculations and computations. These operations provide the range, relative velocity, and angle estimation of objects.

2.1.1 Range Detection

The most important attribute of an FMCW RADAR is range detection capability due to utilizing chirp signal as a transmission wave, as mentioned before. Range information is the distance between the object and the receiver antenna. This information can be obtained by frequency shift between transmitted and received signal, which creates IF signal. As mentioned earlier, IF signal is the output of a mixer, where transmitted and received signals are down-converted, as shown in equation 5.

$$IF = \sin\left(w_1 - w_2\right)t + \left(\varphi_1 - \varphi_2\right) \tag{5}$$

In equation 5 $(w_1 - w_2)$ is the instantaneous frequency and $(\varphi_1 - \varphi_2)$ is the phase of the IF signal where w_1, w_2 are the frequencies of the transmitted and received signal and φ_1, φ_2 are the phases of these two signals. IF signal can change concerning the number of objects in front of the RADAR system. Transmitted and received signals and the corresponding IF signal is shown in Figure 7 in the presence of a single object. Since there is only one object, the corresponding IF signal has a constant frequency, which can be calculated by using equation 6.

$$f_{IF} = S\tau \tag{6}$$

where S is the slope of the chirp signal and τ is a small fraction of the total chirp

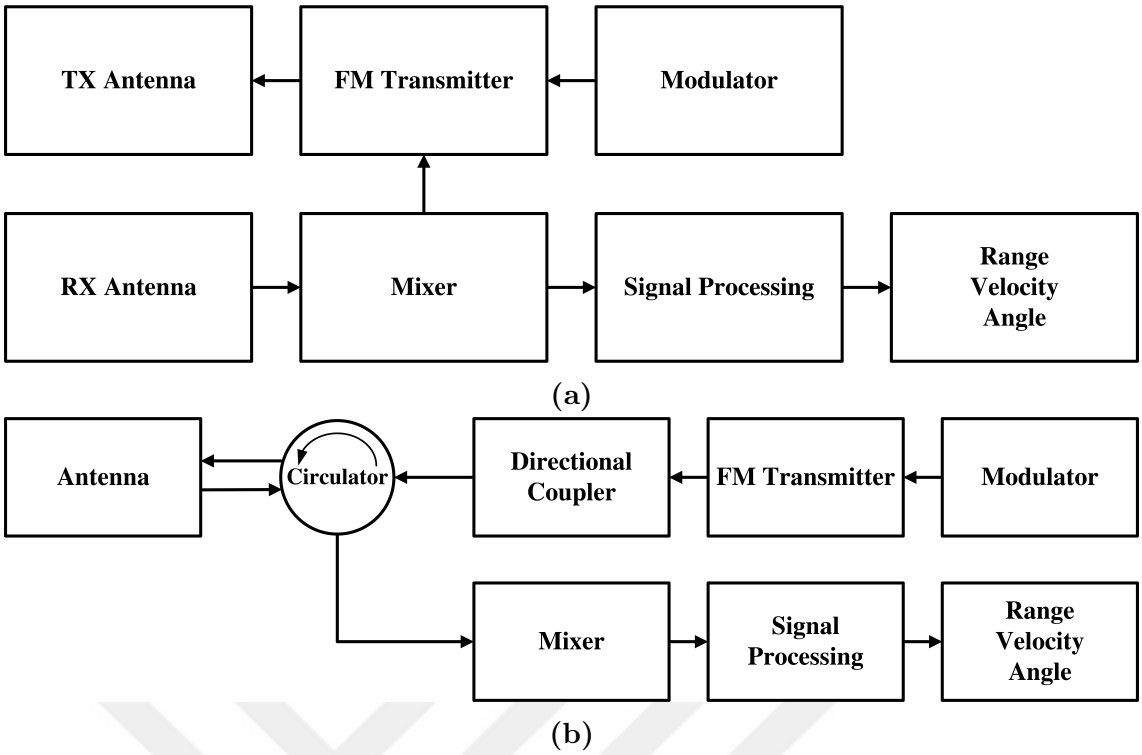


Figure 6: Block diagrams of (a) monostatic and (b) bistatic FMCW RADAR systems.

time, which can be expressed as in equation 7.

$$\tau = \frac{2d}{c} \tag{7}$$

where d is the distance between the target and the antenna and c is the speed of light. Therefore, a single object creates an IF signal with a constant frequency of

$$f_{IF} = S(\frac{2d}{c}) \tag{8}$$

However, the situation changes when multiple objects are present in front of the antenna. Transmitted chirp signal reflects from each of the objects, and multiple reflected signals will be created. Therefore, each of the objects creates an IF signal with a different frequency concerning their distance to the antenna, which leads to multiple IF signals at the output of the mixer. The transmitted and received signals and their corresponding IF signals are represented in Figure 8.

Regardless of either detecting one or more objects at the same time, there are limitations for any FMCW RADAR systems in terms of range detection. One of the two limitations is the maximum detectable range, which can be described as

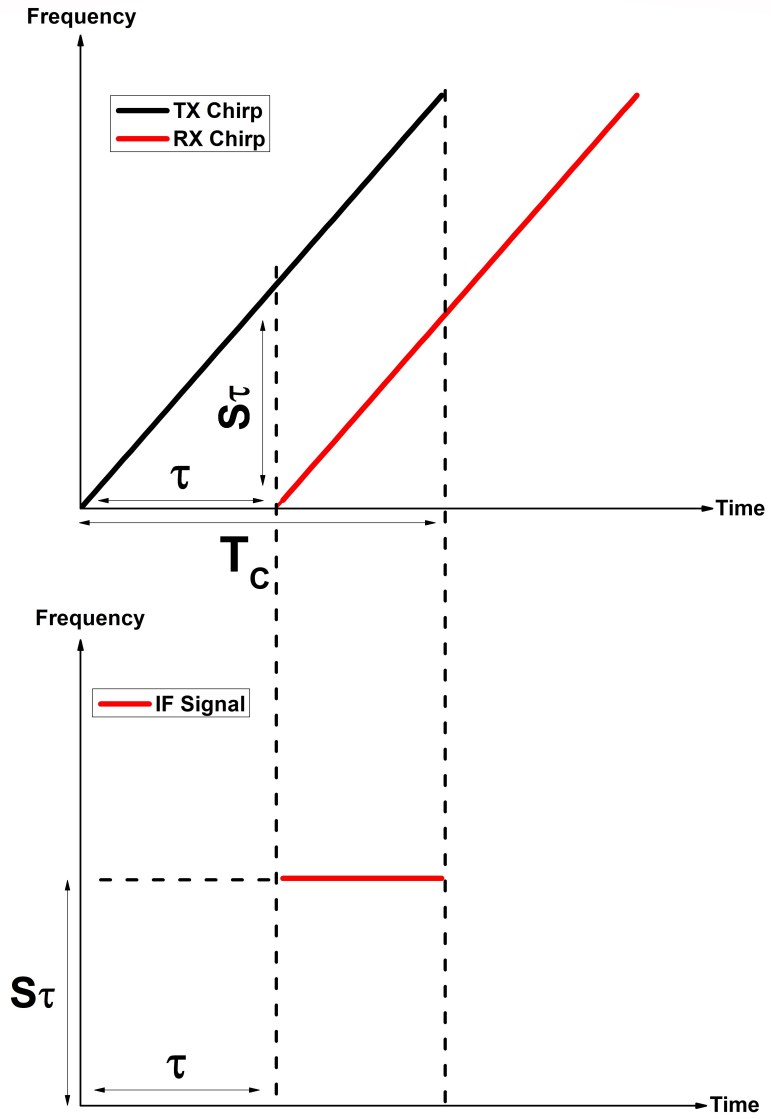


Figure 7: Transmitted and received signals and corresponding IF signal when a single object is in front of the antenna.

how far the RADAR system can locate an object. The other limitation is the range resolution, which is defined as the minimum distance that the RADAR system can separate two different objects. These two limitation factors determine the overall performance of an FMCW RADAR system. Therefore, maximum detectable range and range resolution are the key concepts for range detection.

As referred in equation 8, an object at a distance d with respect to an antenna generates an IF signal with a frequency of $S * 2d/c$. Also, it is important to mention that two signals can be separately resolved in frequency when their frequency difference is larger than the inverse of the period of the chirp, i.e., $\Delta f > 1/T$. If these two information is combined;

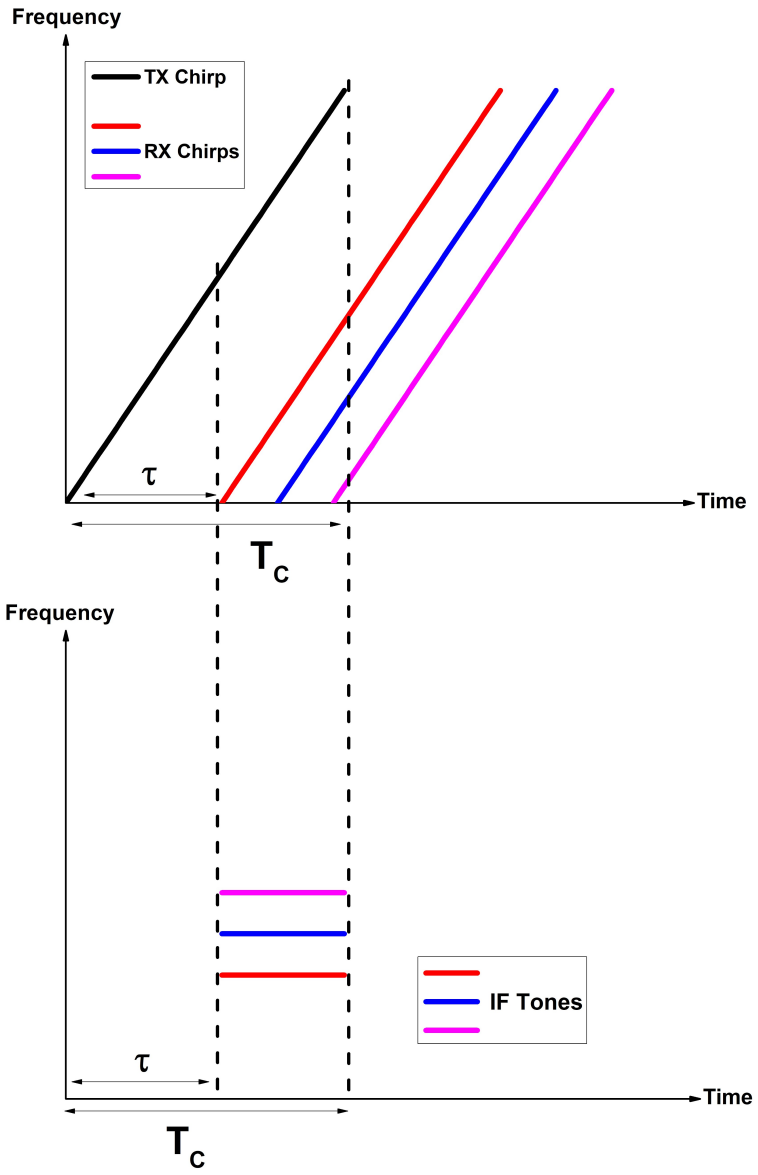


Figure 8: Transmitted and received signals and corresponding IF signal when multiple objects are in front of the antenna.

$$\frac{S2\Delta d}{c} > \frac{1}{T} \tag{9}$$

since the bandwidth B equals to $S * T$, equation 9 can be re-written as in equation (7).

$$\Delta d > \frac{c}{2B} \tag{10}$$

So, it is clear that range resolution depends only on the RF bandwidth swept by the chirp. Therefore, moving the frequency band from 24 GHz to 77 GHz improves

the range resolution directly.

The maximum detectable range depends on the IF signal because IF signal, and the range information is proportional to each other. Theoretically, the frequency of the IF signal can increase as long as the range of an object increases as given in equation 8. On the other hand, IF signal needs to be digitalized by utilizing ADCs for digital processing to obtain information as referred in Figure 6. Therefore, the maximum frequency of the IF signal is limited by the sampling rate F_s of the ADC. Thus, the maximum detectable range can be found as in equation 11.

$$d_{max} > \frac{F_s c}{2S} \tag{11}$$

Maximum detectable range and range resolution capabilities are the performance metrics for range detection for an FMCW RADAR system. Maximum detectable range is limited by the sampling rate of an ADC which digitalizes the IF signal, whereas range resolution only depends on the RF bandwidth. Therefore, these two parameters should be detailly considered for system performance.

Another aspect of range detection is due to the phase of the IF signal. The phase of the IF signal is the phase differences between received and transmitted signal as referred in equation 5. The phase difference $\Delta\varphi$ can be expressed as given in equation 12.

$$\begin{aligned} \Delta\varphi &= 2\pi f \Delta\tau \\ \Delta\varphi &= \frac{4\pi\Delta d}{\lambda} \end{aligned} \tag{12}$$

Latter equation is important since it indicates that when the distance of the object changes, the phase of the corresponding IF signal changes, as well as its frequency, does. When an object changes its position in front of the antenna by $\lambda/4$ ($\sim$1 mm) for a 77 GHz FMCW RADAR system the change in the frequency of the IF signal can be calculated by using equation 8 as 333 Hz. For a general FMCW RADAR system, this much of frequency change corresponds to 0.016 cycles, which is almost impossible to detect in the frequency spectrum. At the same time, the change in the phase of the IF signal can be calculated by using equation 12 as 180°. When these two changes compared, it is obvious that the phase of the IF signal is more sensitive to smaller distance changes than the frequency of the IF signal.

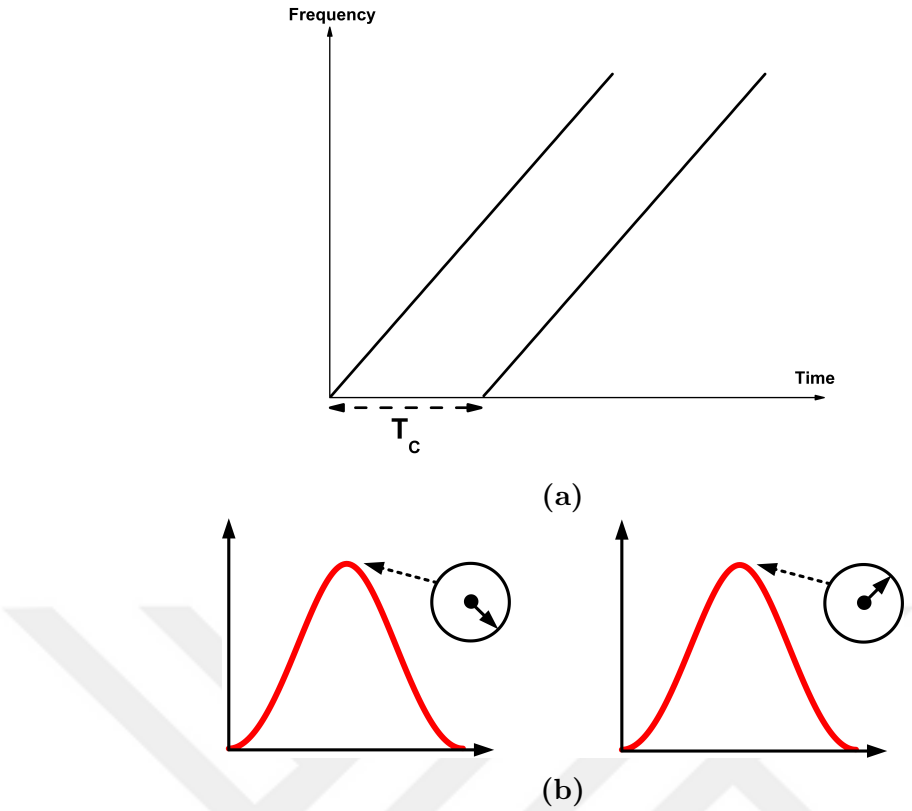


Figure 9: Two transmitted chirp signals and their corresponding peaks in frequency domain. The circles indicate the phase response of each peak.

Therefore, the change in the phase of the IF signal is used for detecting very smaller distance changes, such as vital sign detection systems [23].

2.1.2 Velocity Detection

Velocity detection is another ability for an FMCW RADAR system. The detected velocity is not the actual velocity; it is the relative velocity concerning the velocity of the antenna. To be able to measure the relative velocity an object, at least two chirp signals are needed, which are separated by T_c as shown in Figure 9. IF signals which are corresponding to these two signals will have the same frequencies since the object is at the same range, but they will have different phases. The phase difference w corresponds to mobility for that object, which is $v*T_c$. Therefore, the phase difference can be expressed as

$$w > \frac{4\pi T_c}{\lambda} \tag{13}$$

From equation 13, velocity can be calculated as given in equation 14.

$$v > \frac{\lambda w}{4\pi T_c} \tag{14}$$

When the case is measuring relative velocities of multiple objects which are located at the same distance to the antenna, the measurement method that sends two chirp signals is not enough. Since the objects are positioned at the same distance from the antenna IF signals will be generated with the same frequencies. Thus, after the range FFT operation, there will be only one peak at the spectrum as if there was only one object moving. That single peak contains all the signals reflected from equidistant objects. As a result, simple phase processing methods will not be enough for velocity measurements. Therefore, an extra FFT is needed to detect multiple objects within the same distance in front of the antenna. This FFT is called "Doppler FFT," which should be applied to the peaks of the result of the first FFT, which have the range information. By this method, different peaks can be detected which are located at on the same frequency. To be able to apply this method properly, N equi-spaced chirps must be transmitted from the antenna as the input signal. This pack of chirps is called a frame. The flow of detecting velocities for multiple objects is shown in Figure 10.

Each peak at the Doppler FFT corresponds to a phase difference between the successive chirps for each one of the objects in front of the antenna. Velocities of different objects can be expressed as given in equation 15, which are modified versions of equation 14.

$$\begin{aligned} v_1 &> \frac{\lambda w_1}{4\pi T_c} \\ v_2 &> \frac{\lambda w_2}{4\pi T_c} \end{aligned} \tag{15}$$

There are two limitations for any FMCW RADAR systems in terms of velocity detection, which are maximum measurable velocity and velocity resolution, as in range detection. Maximum measurable velocity can be defined as up to what extent of speed that the antenna can detect an object. Velocity resolution can be defined as the minimum velocity difference between two different objects that the antenna can separate them. The maximum measurable velocity can be calculated by using

equation 14. However, equation 14 becomes ambiguous since there are two different answers for radial movement in phase. Therefore, in order to have an unambiguous measurement of velocity, the absolute value of phase difference w should be less than π. Hence the maximum measurable velocity can be calculated as in equation 16.

$$v_{max} > \frac{\lambda}{4T_c} \tag{16}$$

The velocity resolution can be calculated by using equation 14 as in calculating the maximum measurable velocity. The only limitation arises due to utilizing FFT on the frame. An FFT on a frame which has a length of N can separate two different frequencies if their difference (phase difference - w) is greater than $2\pi/N$. So, if Δw is replaced with $2\pi/N$ in equation 14, the velocity resolution can be expressed as given in equation 17.

$$v_{res} > \frac{\lambda}{2NT_c} \tag{17}$$

2.1.3 Angle of Arrival Estimation

The angle of arrival estimation is another aspect of any FMCW RADAR system. It is necessary when there are multiple objects in front of the antenna traveling with the same relative velocity and positioning at the same distance. Because, when the case is detecting multiple objects with the same speed and same distance, applying range-FFT and Doppler-FFT techniques generate a single peak at both spectrums. Therefore, another FFT operation is required to distinguish different objects. By utilizing a third FFT, angle of arrival can be estimated. However, in order to find the angle of arrival, at least two receiving antennas are required. Hence, the angle of arrival estimation analysis is performed as if there were two receiving antennas. The case for detecting a single object can be visualized as given in Figure 11. Recall that as discussed in range measurement with exploiting phase difference, the differential distance from an object to antennas results in a phase difference in the Doppler-FFT peaks as given in equation 18.

$$w > \frac{2\pi d \sin\theta}{\lambda} \tag{18}$$

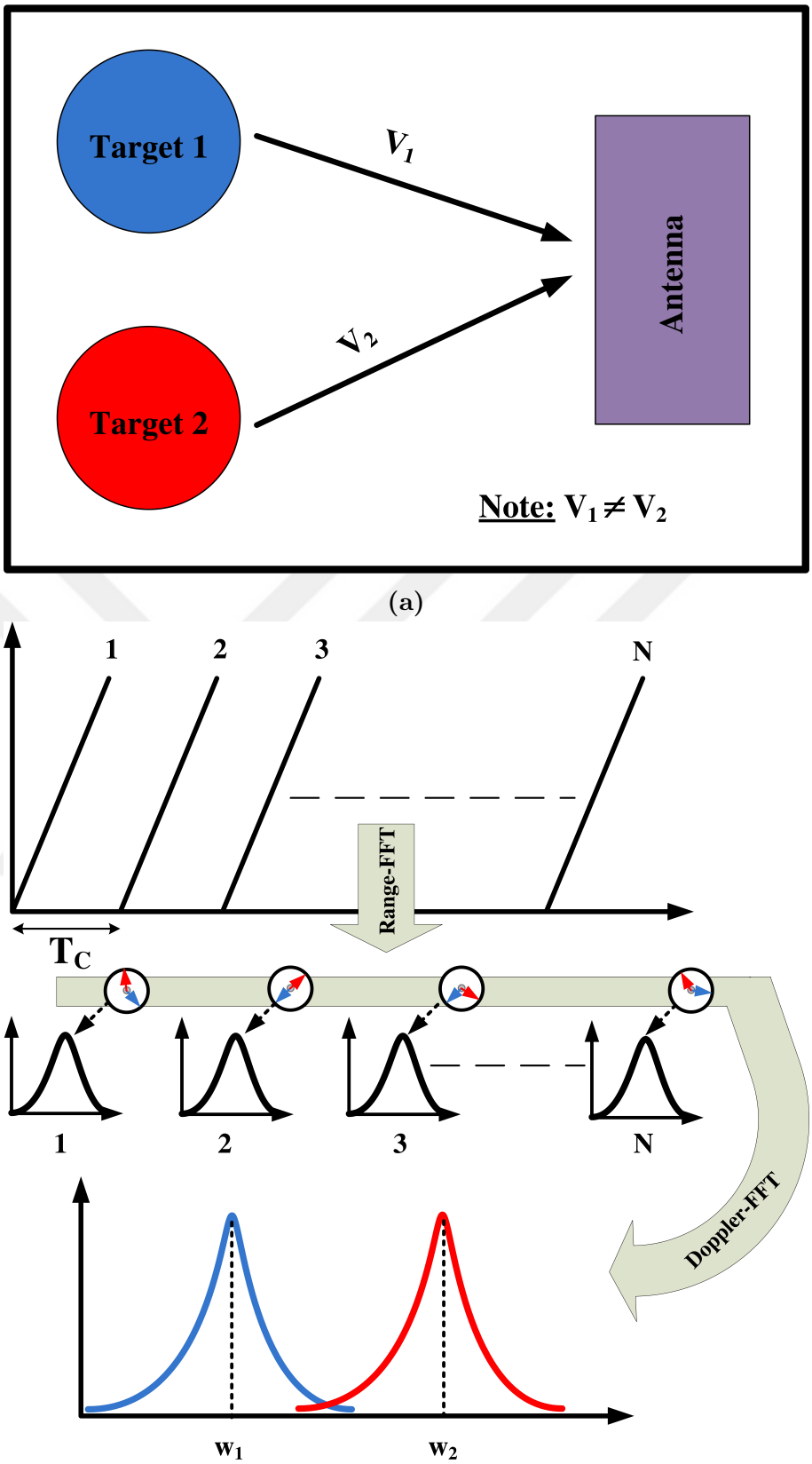


Figure 10: The flow for detecting velocities of two objects. Note that Doppler-FFT is applied to the peaks of the Range-FFT.

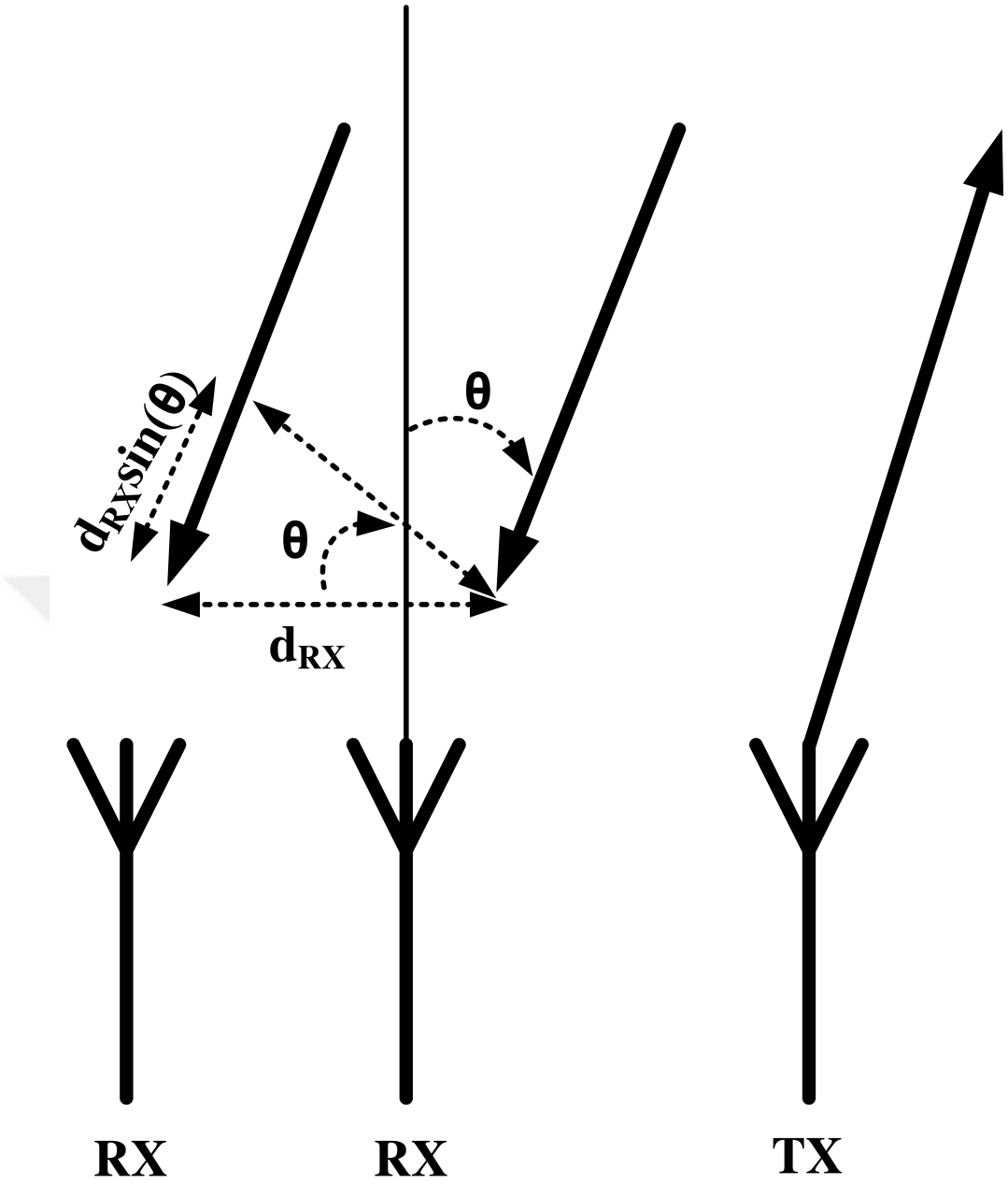


Figure 11: Single object angle of arrival estimation. Angle of arrival is represented as a relationship between reflected signal of he first RX antenna and the extra distance that the reflected signal needs to travel to the second RX antenna.

From equation (15), angle of arrival can be calculated as in equation (16).

$$\theta = sin^{-1}(\frac{\lambda\Delta\varphi}{2\pi d_{RX}}) \tag{19}$$

It should be noted that phase difference w and angle of arrival θ have a non-linear relationship, unlike as in velocity measurement. So, as θ changes from 0° to 90°, the sensitivity of w becomes more insensitive to changes in θ. When the

case becomes measuring multiple targets, the critical situation is when at least two objects are moving with the same relative velocity with equidistance. Because as mentioned at the beginning, after range-FFT and Doppler-FFT processes, there will be only one peak at the spectrum. However, that one peak is the combination of the phase information of every target. By applying a new FFT process, which is called angle-FFT, every peak that corresponds to each of the targets can be discretely obtained. The overall flow of estimating the angle of arrival is given in Figure 8. When equation 19 converted into detecting two objects, angle of arrivals for different objects can be calculated as given in equation 20.

$$\begin{aligned} \theta_1 &= sin^{-1}(\frac{\lambda\Delta\varphi_1}{2\pi d_{RX}}) \\ \theta_2 &= sin^{-1}(\frac{\lambda\Delta\varphi_2}{2\pi d_{RX}}) \end{aligned} \tag{20}$$

There are two limitations for any FMCW RADAR systems in terms of angle of arrival detection as in range and velocity measurements. One of them is the angular field of view, which can be expressed as the observable world that is detected at a particular time. The other one is the angular resolution, which can be described as the value of the minimum angle that RADAR can separate two objects as two separate peaks in angle-FFT. Angular field of view calculation is like maximum measurable velocity. Angular field of view can be calculated by using equation 19 becomes ambiguous since objects positioned on right or left cannot be separated. Therefore, in order to have an unambiguous angular field of view, the absolute value of phase difference w should be less than π. So, the angular field of view can be calculated by using equation 21.

$$\theta_{max} = sin^{-1}(\frac{\lambda}{2d_{RX}}) \tag{21}$$

In the latter equation, d is the distance between receiving antennas. Further, the maximum angular field of view can be achieved by placing the antennas $\lambda/2$ apart from each other. Thus, $\lambda/2$ results in $\pm$ 90° angular field of view.

Angular resolution can be calculated by using a modified version of equation 18 for two different objects with θ and $\theta + \Delta\theta$ such that

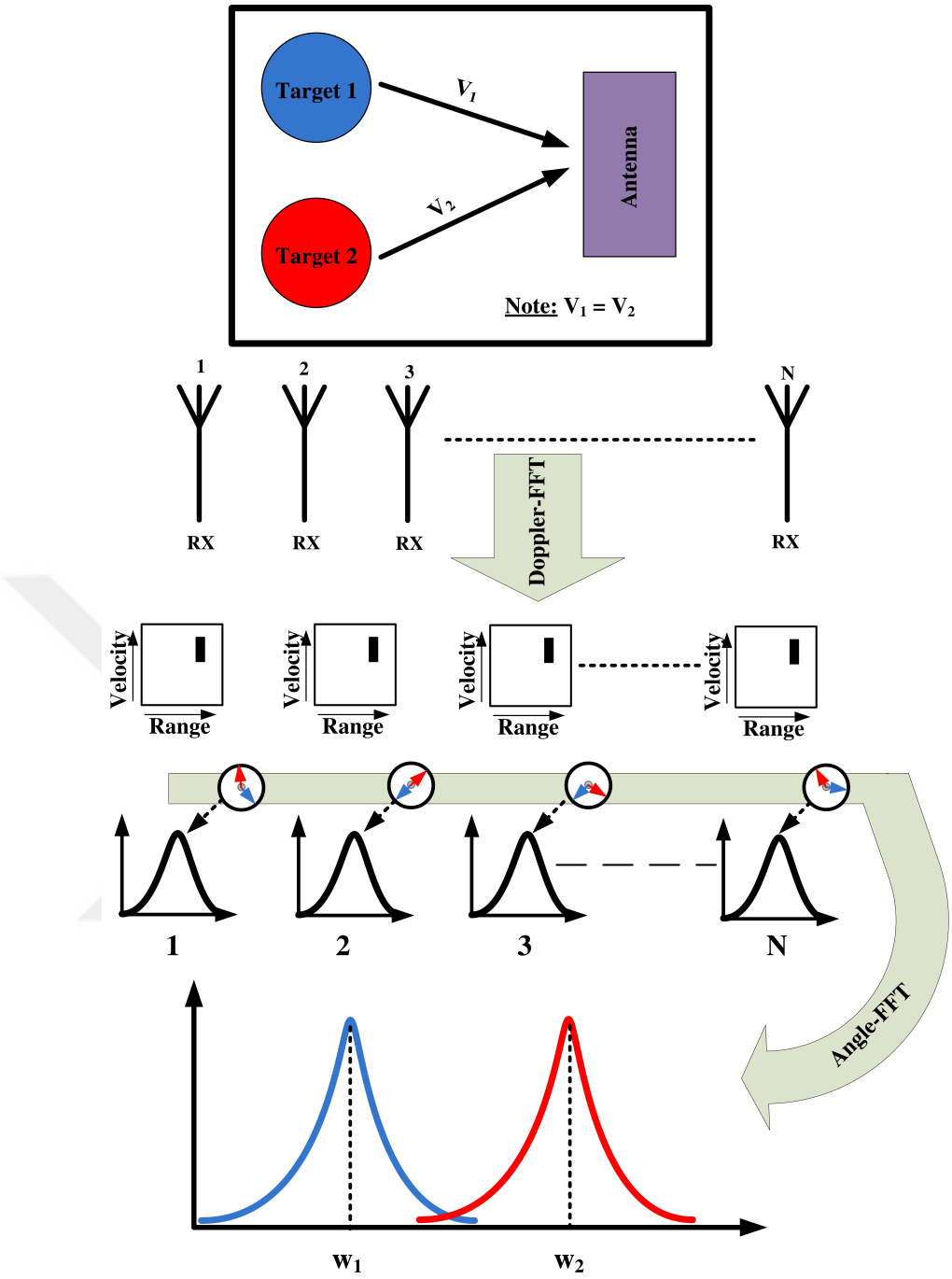


Figure 12: Multiple object angle of arrival estimation. Two objects have the same relative velocity and they are at the same distance with respect to the antenna. It should be noted that Doppler-FFT is 2D and Angle-FFT is 3D FFT.

$$\Delta w = (\frac{2\pi d}{\lambda})sin(\theta - \Delta\theta) \tag{22}$$

Since the derivative of $sin(\theta)$ equals to $cos(\theta)$ equation 22 can be rewritten as

$$\Delta w = (\frac{2\pi d}{\lambda})cos(\theta)\Delta\theta \tag{23}$$

It should be noted that the phase difference Δw is greater than $2\pi/N$, where N is the number of receiving antennas. Therefore, equation 23 becomes

$$(\frac{2\pi}{N}) < (\frac{2\pi d}{\lambda})cos(\theta)\Delta\theta \tag{24}$$

Hence, angle resolution can be expressed as

$$\theta_{res} = \frac{\lambda}{Ndcos(\theta)} \tag{25}$$

2.2 Properties of General RADAR Systems

2.2.1 RADAR Equations

Although the properties and benefits of FMCW modulation, and how to obtain information about targeted objects were discussed in detail in the previous section, it is also important to mention the basics of a RADAR. Because, without analyzing RADAR basics, quality of the received signal and thus measurement about detection will not be entirely accurate. Besides the well-known radar equations, signal-to-noise ratio (SNR) and radar cross-section (RCS) are the most two critical parameters to evaluate the performance of the RADAR system. Also, the relationship between SNR and RCS will be proven.

The RADAR equations are almost the same for both monostatic and bistatic RADAR systems. The only difference is due to the different number of antennas. Equations for bistatic RADAR systems include G_T and G_R, which are gains of the transmitting and receiving antennas respectively. Since there is only one antenna in monostatic RADAR systems, the gain of the antenna G is used for both G_T and G_R. As mentioned before, for a basic RADAR system, the well-known radar equation which defines the power density $p(R)$ targeting an object from a distance R can be expressed as in equation 26.

$$p(R) = \frac{P_T G}{4\pi R^2} \tag{26}$$

The received power P_R at the antenna can be calculated as given in equation 27.

$$P_R = \frac{P_T G^2 \lambda^2}{(4\pi)^3 R^4 L} \sigma \tag{27}$$

where σ is radar cross-section, which will be mentioned later, and $L < 1$ is the combined losses due to design and environment. Therefore, the signal-to-noise ratio (SNR) can be calculated as

$$SNR = \frac{P_R}{P_N} \tag{28}$$

where P_N is the noise power in the baseband, which arises from thermal noise, receiver noise figure, the bandwidth of the operation, and $1/f$ noise. If noise power is modeled as a Nyquist thermal noise which is given as

$$P_N = k_B T \Delta f \tag{29}$$

where k_B is the Boltzmann constant, T is the antenna temperature of the environment, and Δf is the bandwidth. Therefore, SNR can be re-written as

$$SNR = \frac{\sigma P_T G^2 \lambda^2}{(4\pi)^3 R^4 k_B T \Delta f} \tag{30}$$

The threshold value of SNR to detect targets is generally 10 dB. This SNR value provides a low false alarm rate with a reasonable probability of detection [24].

2.2.2 RADAR Cross Section (RCS)

Radar cross-section (RCS) is fundamentally a ratio of scattered power density to incident power density [25]. RCS depends on geometry and type of material of an object. Also, operating frequency and polarization of the antenna of the radar system change the RCS value. The unit is defined as $dBsm$ (dB to relative to one square meter). RCS can change as the interaction between the transmitted wave and object. Therefore, this information can create new opportunities to categorize and estimate new objects concerning their RCS behavior. Therefore, calculating RCS is critical to express the radar performance and characteristics of targets. RCS can be expressed as given in equation 31.

$$\sigma = \frac{SNR(4\pi)^3 R^4 k_B T \Delta f}{P_T G^2 \lambda^2} \tag{31}$$

3 77 GHz FMCW RADAR for Automotive Applications

This section includes general information about the designed system. The block diagram of the designed system and the workflow are provided. Also, theoretical calculations and expected performance parameters are presented. After the system-level investigation is done, the design of each sub-block is detailly explained, and simulation results are provided. Further, every sub-block is compared with similar work from literature. Finally, the simulation results for the designed system and comparison with similar work from literature are presented.

3.1 The Detailed Analysis on the Designed System

3.1.1 Design Considerations and Workflow of the System

In general, RADAR systems can be classified into two categories as monostatic and bistatic, as mentioned in the previous section. Monostatic RADAR systems have only one antenna for both receive and transmit duties whereas bistatic RADAR systems have at least two antennas which are operating for only receive or transmit duties. There are several advantages or disadvantages of using either monostatic or bistatic systems. In this thesis work, a monostatic RADAR system approach was selected due to its cost-efficient structure and reduced complexity. Further, since FMCW operation does not require high transmit powers, the monostatic approach is suitable. The complete block diagram of the system is given in Figure 1.

In general, as mentioned in earlier sections, monostatic architecture is achieved by using duplexers. Utilizing a duplexer provides using the same antenna to receive and transmit operation. Although this seems very beneficial, there are vital design criteria for duplexers to be able to be used in RADAR systems. One of the criteria is the RF performance of the duplexer since it is placed right after the antenna. Since the insertion loss of a duplexer cannot be compensated, duplexer affects the overall performance of the system. The insertion loss is directly added to the noise figure of the receiver. Further, the path between antenna and duplexer should be considered due to additional loss. Besides, duplexer should handle high powers because the transmitted signal would also pass through it. The other criterion

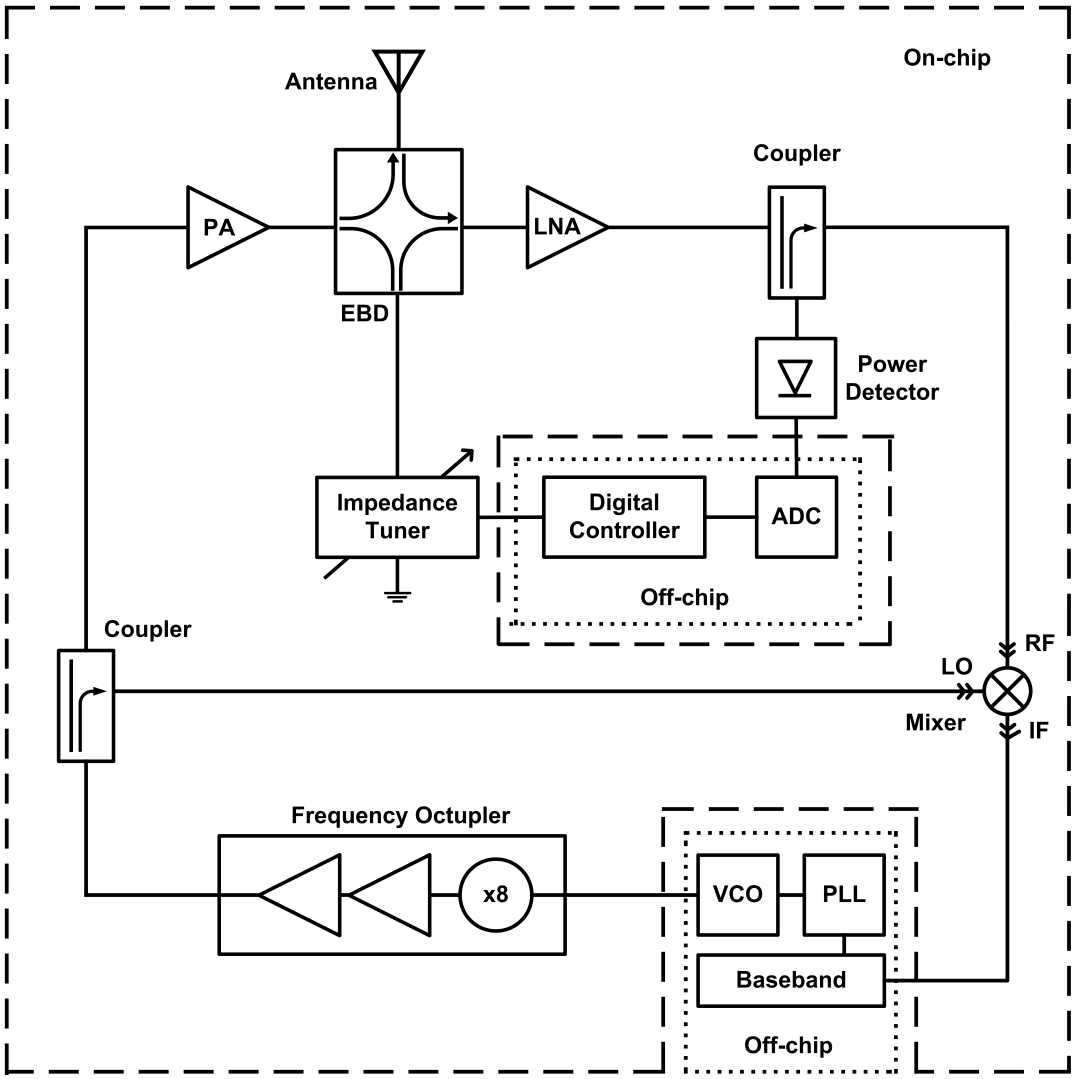


Figure 13: The block diagram of the designed system

is that duplexer must provide enough isolation between receiver and transmitter chains. If the isolation between receiver and transmitter is not enough, the signal will leak from receiver to transmitter, and the measurement results would not be correct. Even further, the receiver chain could saturate due to high-power leakage signal. Hence, the circuit that isolates receiver and transmitter is critical. There are several different circuits used as duplexers such as circulators, surface acoustic wave (SAW) filters, and electrical balance duplexers (EBD).

Circulators have three ports, and they are non-reciprocal devices. The working principle of a circulator is as follows. The signal is applied from one port can only flow to adjacent one, either in the clockwise or counterclockwise direction. However, because of the nature of duplexer reflected signal from a port can leak to other port (transmitter to receiver) can degrade the performance of the system. Although

circulators have low insertion loss and high isolation, they are generally ferrite based [26]. Hence, circulators are only efficient with silicon-based designs until a few GHz designs.

SAW filters have three ports as well as circulators. They are used mostly in frequency division duplexing systems such that the signal is transitioned from the electrical domain to the acoustic domain [27]. Ports of SAW filters are designed for different frequencies. Thus, signals with different frequencies are rotated to the desired ports with high isolation. However, these filters are inefficient to utilize as duplexers in high-frequency systems. Because, as the number of frequency bands changes for either communication or RADAR systems, the complexity of SAW filters increase, and integrity of these filters get decrease. EBD is another type of duplexer, which has a comparable RF performance with circulators and SAW filters. Further, EBD provides higher integration capability to BiCMOS technologies than its counterparts [28]. The advantages of utilizing EBD and design procedure will be discussed later.

The input chirp signal is generated with a voltage-controlled oscillator (VCO) and phase-locked loop (PLL). VCO generates the signal, and its frequency can be changed by tuning control voltage. PLL stabilizes the generated signal to maintain a clear chirp. These two components are on board; thus, they should be connected with wire bonds to the designed chip. Rule of thumb states that a 1 mm wire bond corresponds to 1 nH inductance. Hence, it is not possible to generate a signal at 77 GHz outside of the chip. Due to its internal inductance, up to 10–15 GHz signals can be transmitted over a wire bond without degradation. A frequency octupler (multiplier by eight) is designed to overcome this problem. The input of this frequency octupler is the generated chirp signal from VCO-PLL loop, and the output is the RF signal at 77 GHz, which will be transmitted. Then, the signal flows through a directional coupler, which is required to generate a LO signal for the mixer, as shown in Figure 13. Nevertheless, the chirp signal passes from the through the port of the directional coupler and arrives at the input of the power amplifier (PA). PA generates enough power for the signal to be transmitted. Then, the signal moves into EBD and transmitter from an antenna.

The antenna captures the reflected signal from an object of the transmitted sig-

nal. That signal is transitioned to low noise amplifier (LNA) to have increased amplitude. After that, the signal is moved into the through-port of another directional coupler. Coupled port of this directional coupler is connected to a control system, which will be explained later. The signal flew into the through-port of the directional coupler is transmitted to the RF-port of the mixer. Mixer down-converts the received signal into an intermediate frequency (IF) to be able to analyze and get the measurement data. In the end, IF signal is transitioned into the baseband part via wire bonds. In baseband, there are several blocks for digitalizing and processing IF signal. In general, IF signal is digitalized with an ADC and applied 2D-FFT to get the range and velocity measurement data.

In order to provide high isolation between receiver and transmitter, EBD requires a perfect matching between antenna and balance ports. Therefore, additional circuits are necessary to compensate for impedance mismatches between the antenna and balance port. These sub-blocks are power detector (PD), ADC, digital control circuit, and a tuner circuit, as shown in Figure 1. As mentioned before, the received signal is coupled to the PD by utilizing a directional coupler after the received signal flew through the LNA. PD is capable of detecting the amplitude of the signal changes and produces a DC voltage at the output. Then, the ADC digitalizes this signal and sends it to the digital control circuit. The digital control circuit generates an output such that tuner changes the impedance of the balance-port and compensates the impedance mismatch.

As the antenna of the system, there are several options. Patch antenna array or a horn antenna can be used with enough gain. If patch antenna array is selected, it can be integrated with the rest of the circuit. However, if a horn antenna is selected instead, it is not possible to connect the antenna to RF pads with wire bonds due to the reasons mentioned before. Therefore, packaging should be considered detailly and chosen carefully to have almost no degradation in RF performance.

3.1.2 Theoretical Calculations

In the previous section, the equations for FMCW RADAR systems were provided. These equations are vital for determining system specifications and performance metrics. Antenna gain, transmitted signal power, RCS of the desired objects,

Table 2: Example RCS values of various objects at microwave frequencies [7]

Object	**Square meters**
Conventional, unmanned winged missile	0.5
Small, single engine aircraft	1
Small fighter, or 4-passenger jet	2
Large fighter	6
Medium Bomber or medium jet airliner	20
Large bomber or large jet airliner	40
Jumbo jet	100
Small open boat	0.02
Small pleasure boat	2
Cabin cruiser	10
Pickup Truck	200
Automobile	100
Bicycle	2
Man	1
Bird	0.01
Insect	0.00005

and receiver NF are the most critical design criteria. These criteria determine SNR, which determines whether the system is capable of sensing and detecting the desired signal rather than interference and noise. If it is recalled, the minimum SNR value for any RADAR system should be 10 dB for accurate measurements.

Firstly, the value of RCS is not a variable, and it is fixed for almost all the objects. Table 2 shows the RCS values of several objects for X-band [7].

As it is given in Table 2, the RCS value of a conventional car is 100 m^2 or 20 dBsm. Higher RCS value ensures higher SNR value for the system. Also, it is essential to mention that the RCS values of the objects increase as the frequency increases. Thus, this value can be used as a benchmark value for system specification calculations to achieve minimum SNR value.

Antenna gain is another crucial design criterion, and it depends on the designer or the antenna that is used. As the antenna gain increases, the SNR value of the system improves. For this thesis work, it was assumed that a horn antenna with 20 dBi gain would be used [29] and calculations were done accordingly. On the other hand, integration of the antenna was assumed to be handled with a packaging technique as mentioned earlier, because it is not in the scope of this work.

Transmitted signal power is mostly depending on the performance of PA. Addi-

Table 3: Theoretical results for a long-range RADAR system for minimum and maximum detectable range

	Minimum Range	**Maximum Range**
Parameters (Units)	**Value**	**Value**
TX Output Power (dBm)	1	14
Antenna Gain (Linear)	100	100
Frequency (GHz)	77	77
Radar Cross Section (m2)	100	100
Receiver NF	30	30
	Theoretical Results	
Range (m)	100	300
Receiver SNR (dB)	16.92	10.83

tionally, due to the architecture, the insertion loss of EBD degrades the power level. However, one of the benefits of utilizing an FMCW approach is low power requirement, thus using an EBD does not create a drawback for the system. Achieving high power for the transmitted signal is very important and common for all RADAR applications. As the power of the transmitted signal increase, the power of the received signal is increased; thus, SNR improves.

The last important design parameter that contributes to SNR is the value of the receiver NF. High receiver NF degrades SNR directly. Because of the chosen architecture, first sub-block of the receiver chain EBD, instead of an LNA, which is the usual way. As mentioned earlier, the insertion loss of EBD adds up to NF directly. Hence, designing a low loss EBD is very important. Further, the gain of the LNA is essential too because it decreases receiver NF and improves SNR.

Table 3 shows the results of theoretical calculations. Two different results were shown with different output powers for the system. Ideally, for SNR $>$ 10 dB, it is possible to detect cars between 100–300 meters distance, depending on the power of the transmitted signal.

3.2 Frequency Octupler

3.2.1 Circuit Design and Implementation

Frequency multiplication or division circuits are one of the vital blocks for RF systems. For this thesis work, a frequency multiplier was necessary, as mentioned earlier. The designed frequency multiplier increases the frequency of the input signal

by a factor of eight. In the market and literature, there are passive and active frequency multipliers available [30]. Passive frequency multipliers have the advantage of consuming no DC power consumption. However, a significant drawback of these circuits to have conversion loss because of their nature. Cascading these circuits in any system creates the need for an extra amplifier chain to compensate for the loss generated by passive frequency multipliers. Thus, the cost and complexity are increased. On the other hand, active frequency multipliers can provide conversion gain instead of loss, which leads no requirement for amplifier chain in the systems even if active frequency multipliers were cascaded. Active frequency multiplier can be designed with two different topologies. One of them is push-push topology, which utilizes the internal nonlinear behavior of the transistors. The other topology is using a Gilbert cell as a mixer, which multiplies the frequency by using a time-varying path. Among these two topologies, push-push topology with a balanced configuration is selected for frequency multiplication by eight. The detailed schematic of the designed frequency octupler is given in Figure 14.

The input part and output part of frequency multipliers are designed for different frequencies. Because a frequency multiplier which receives an input signal at a frequency of f_0 would generate and output signal at $f_0 * k$, where k is the multiplication factor. In this case, the frequency multiplication factor is eight, and the output signal must be at 77 GHz. Therefore, the designed frequency octupler receives signal at between 9.5–10.25 GHz to produce an output signal at 76-81 GHz range. So, the input part of the designed octupler is optimized and matched for 9.5–10.25 GHz, whereas the output part is 76-81 GHz. In order to achieve a balanced signal at the input, the unbalanced signal is converted by a transformer-based passive balun. The transformer is implemented with top two thickest conduction layers of the technology, which are TopMetal-2 (TM2) and TopMetal-1 (TM1). The primary winding is realized with TM2, whereas the secondary winding is realized with TM1 such that the k-factor of the transformer is 0.77 [31]. The turn ratio of the transformer is set to unity (1:1), and the self-inductances of both windings were almost 375 pH. The 3D layout view of the designed transformer-based balun is given in Figure 15.

Push-push topology requires two identical transistors or transistor sets that are fed with the balanced input signal, which are out of phase from each other. The idea

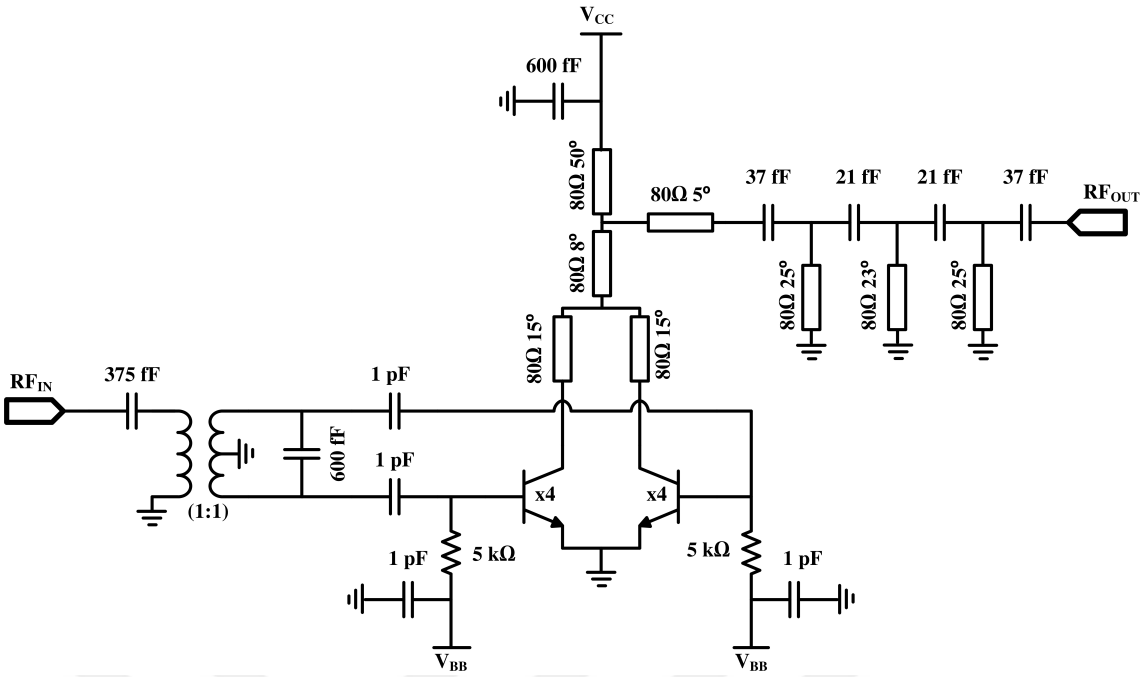


Figure 14: The detailed schematic of the designed frequency octupler (Electrical lenghts are given for 77 GHz).

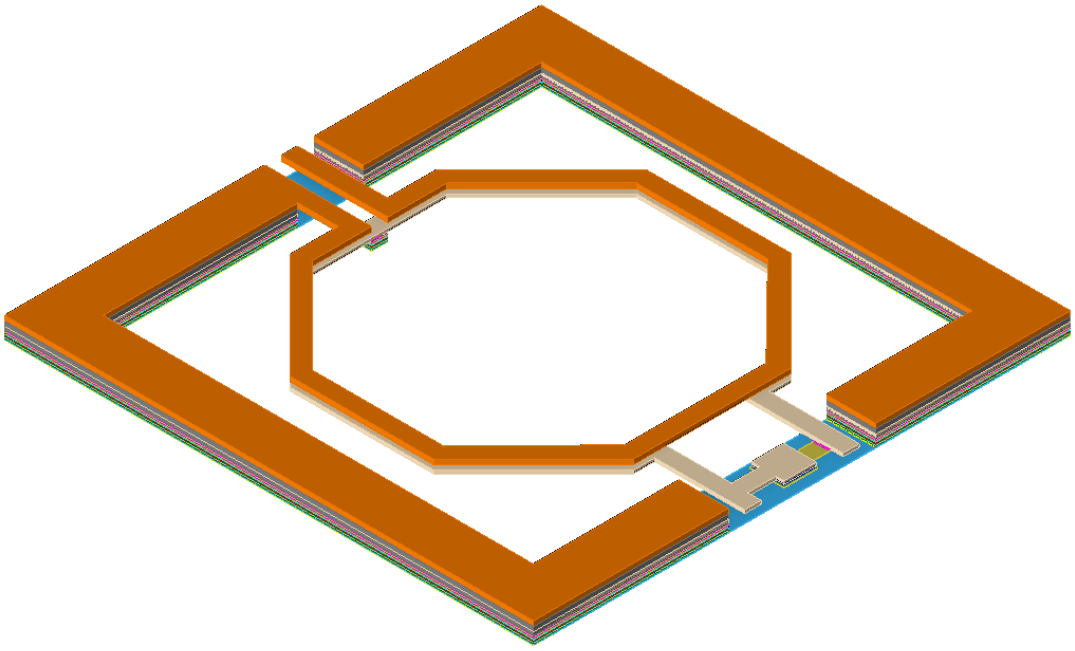


Figure 15: The 3D layout view of the designed X-band transformer-based balun.

behind push-push topology is to generate harmonics of the input signal. Therefore, transistors should be biased as class-B in order to push them to operate in the nonlinear region. Generated harmonics are summed up by connecting the collectors

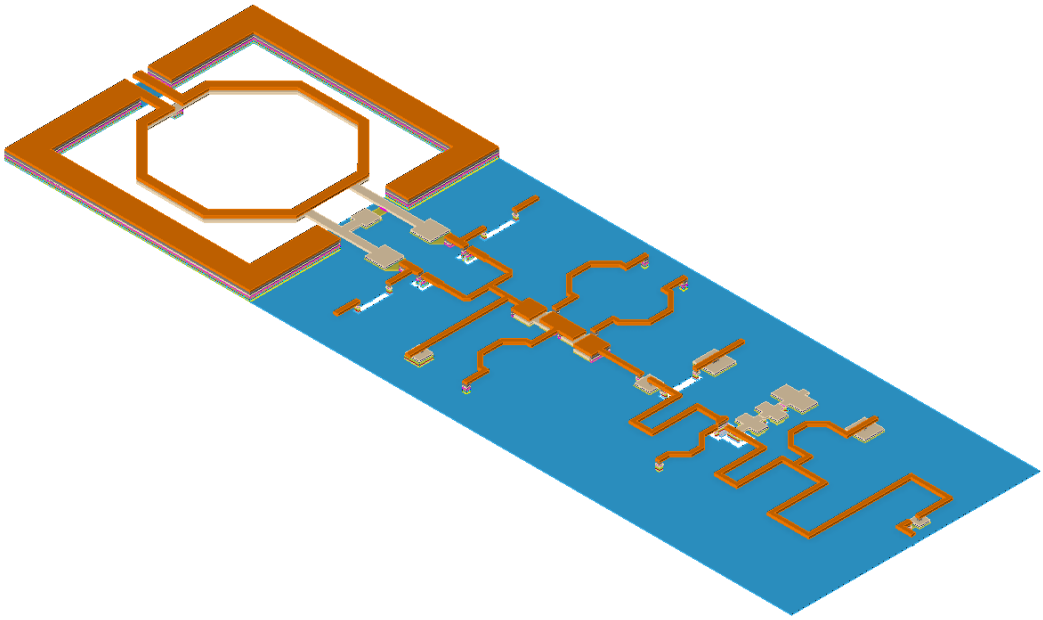


Figure 16: The 3D layout view of the designed frequency octupler.

of these transistors. Since the input signals were identical but out of phase, the generated harmonics also have the same behavior. Thus, when these two harmonic sets were summed, odd harmonics cancel each other whereas even harmonics add up because that connection node behaves as a virtual ground for odd harmonics. Further, to be able to get the eighth harmonic only, there are several different techniques to implement. Three cascaded frequency doublers (multiply by two) can be used. However, this topology increases the occupied area and complexity. A frequency doubler and a frequency quadrupler (multiply by four) can be cascaded to achieve multiplication by eight. However, this approach requires two different designs, which increases cost and complexity. Therefore, for the first time in the literature, multiplication by eight is achieved with one circuit. In order to cancel other even harmonics then the eight, a high pass filter is used. Bandpass filter could be a better solution instead of using a high pass filter, but to be able to implement a narrowband bandpass filter with high bandstop attenuation value inductors are needed with a value of 1 nH or more. These inductance values are not feasible to implement as on-chip components in these frequencies. However, utilizing a high pass filter decreases the power level at the output. Therefore, an additional two buffer amplifiers were cascaded.

Multiplier stage transistors are biased with 0.76 V, which is the class-B bias point for the technology. The number of transistors in each set was chosen as x4 due to matching and conversion gain performance. The input power is set to almost 5 dBm, assuming that the output power level of the VCO that can be bought in the market is generally around 5 dBm. The suppression of the other harmonics until the tenth harmonic is critical because these harmonics can degrade the overall performance of the system. Thus, all harmonics other than eighth harmonics must be eliminated. Although choosing balanced topology helps to achieve this cause, it is not enough alone due to degradation in the amplitude of the signals as the number of harmonics increased. In other words, the eighth harmonic has lower power than previous even harmonics. As mentioned, other even harmonics were even suppressed by utilizing a seventh order high-pass filter. The high-pass filter was designed as Chebyshev topology. The attenuation ripple at the passband is set to 0.1 dB, and amplitude rejection at the stopband is more than 20 dB. All transmission lines were realized with utilizing TM2 layer of the technology. Metal 1 layer was used as a ground plane to implement microstrip configuration. The effects of parasitic capacitances due to RF pads were included in the output impedance matching network. MIM capacitors from the technology were used for bypassing the DC feed lines and DC-blocking purposes on the signal line. Electromagnetic, transient, and harmonic balance simulations were carried out with ADS Momentum software. The 3D layout view of the designed frequency octupler is shown in Figure 16.

3.2.2 Simulation Results

The layout of the designed frequency octupler is given in Figure 17. The total area is 0.532 mm^2, and the multiplier core area without the buffer amplifiers is only 0.266 mm^2. The s-parameter simulation result is shown in Figure 18. Input return loss is 12 dB at 9.625 GHz, which corresponds to 77 GHz at the output. The output power, which is the eighth harmonic, is presented in Figure 19. The simulated output power is -1.47 dBm at 77 GHz. Figure 20 presents frequency spectrum of the output signal. The fundamental suppression is 66.7 dB; the level of suppression is higher than 19.8 dB for all harmonic signals. The simulation results of amplitude

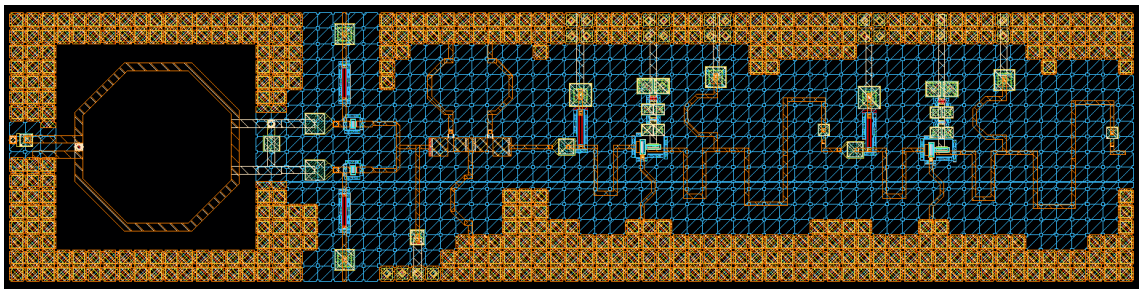


Figure 17: The layout of the designed frequency octupler.

and phase imbalance of the designed X-band transformer-based balun are given in Figure 21. Simulation results show that amplitude difference between the ports of the designed balun is less than 0.2 dB and the phase difference between the ports of the designed balun is very close to 180° for all frequency band. The performance of the buffer amplifiers will be discussed in the next sub-section.

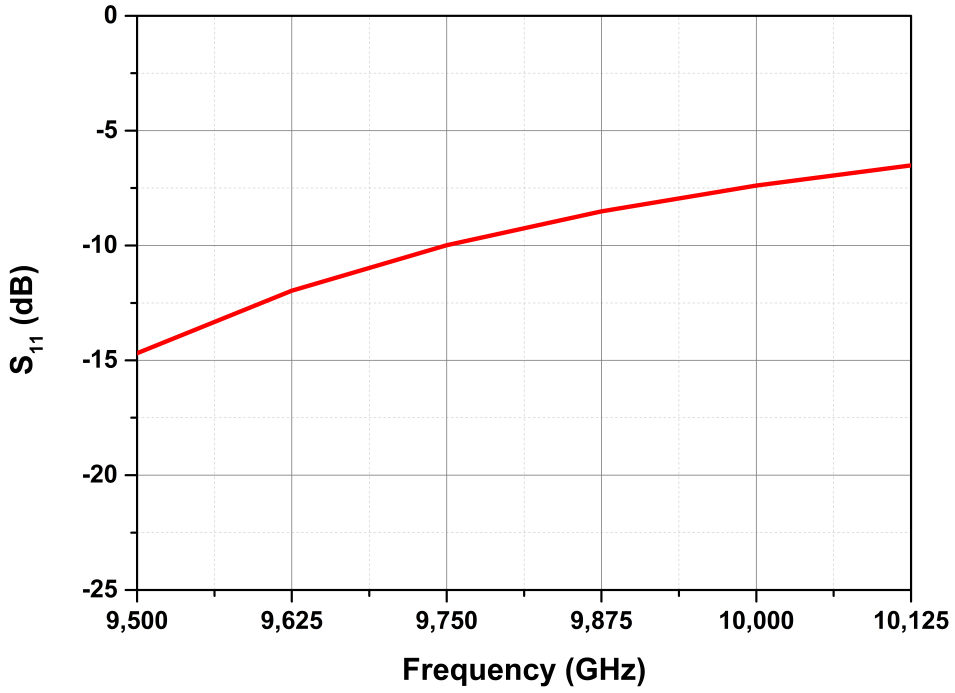


Figure 18: The simulated input return loss of the designed frequency octupler.

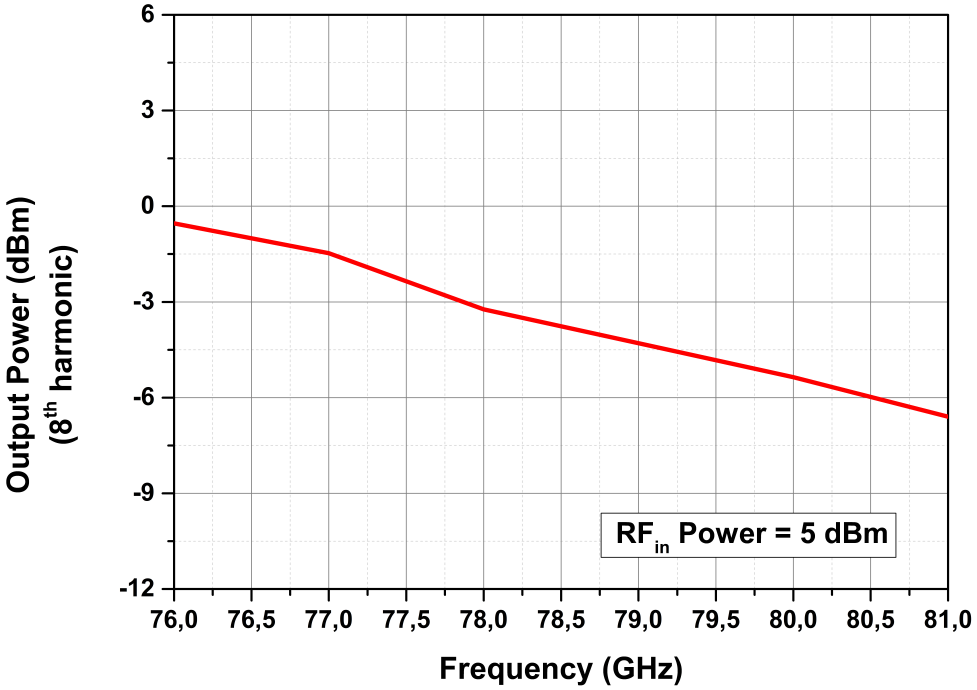


Figure 19: The simulated output power of the designed frequency octupler.

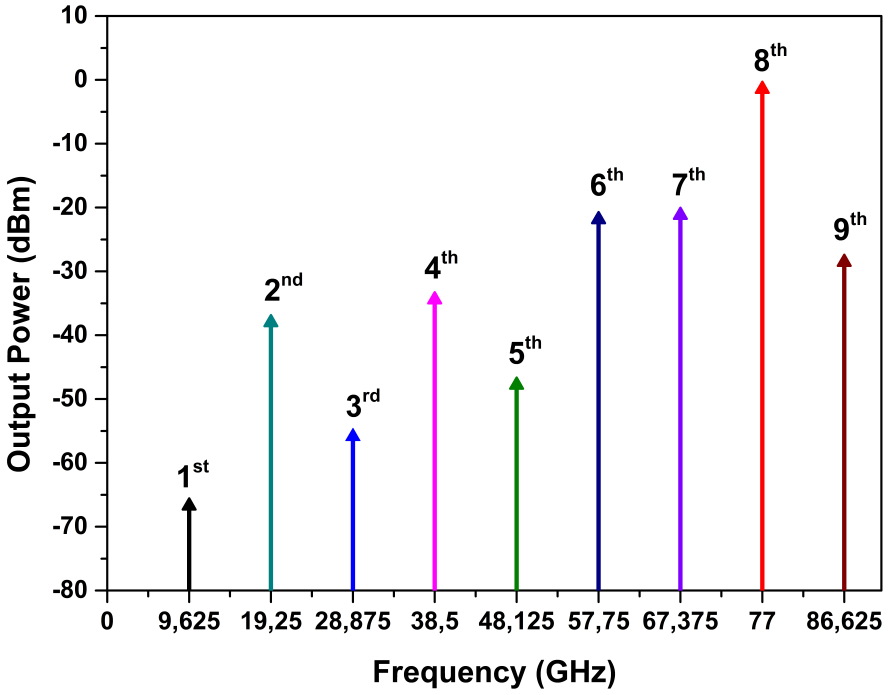


Figure 20: The simulated output spectrum of the designed frequency octupler.

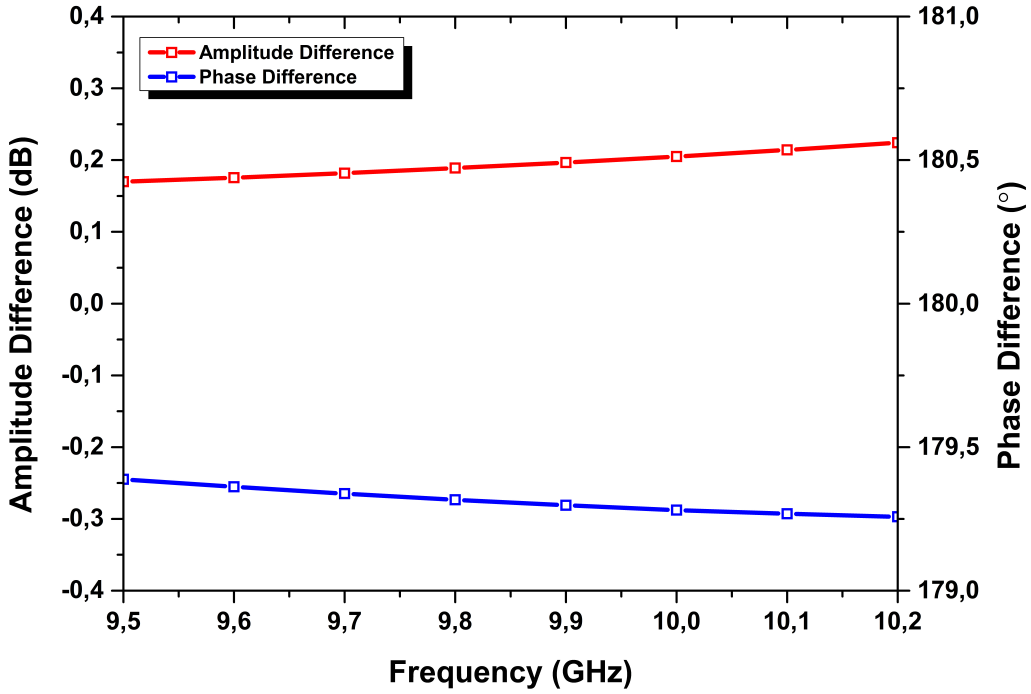


Figure 21: The simulated amplitude and phase imbalance of the designed X-band transformer-based balun.

3.3 Buffer Amplifier

3.3.1 Circuit Design and Implementation

A buffer amplifier is designed to compensate the losses generated by the utilized filters in frequency octupler, as mentioned in the previous section. The impedance matching between the output of the frequency octupler and the input of the buffer amplifier because any mismatch between this intersection would degrade the output power of the frequency octupler. The decreased output power of the frequency octupler downgrades the power level of the transmitted signal and SNR of the system would decrease. This issue leads to a degradation in maximum detectable range, which is undesirable for a long-range RADAR system. Therefore, reverse isolation becomes an important design variable for the buffer amplifier for eliminating the dependence of the output power of the frequency octupler on the input impedance. Besides, the filters utilized in frequency octupler generates a significant amount of loss, which should be compensated, as mentioned in the previous section. Thus, the buffer amplifier should provide enough gain to prevent performance degradation.

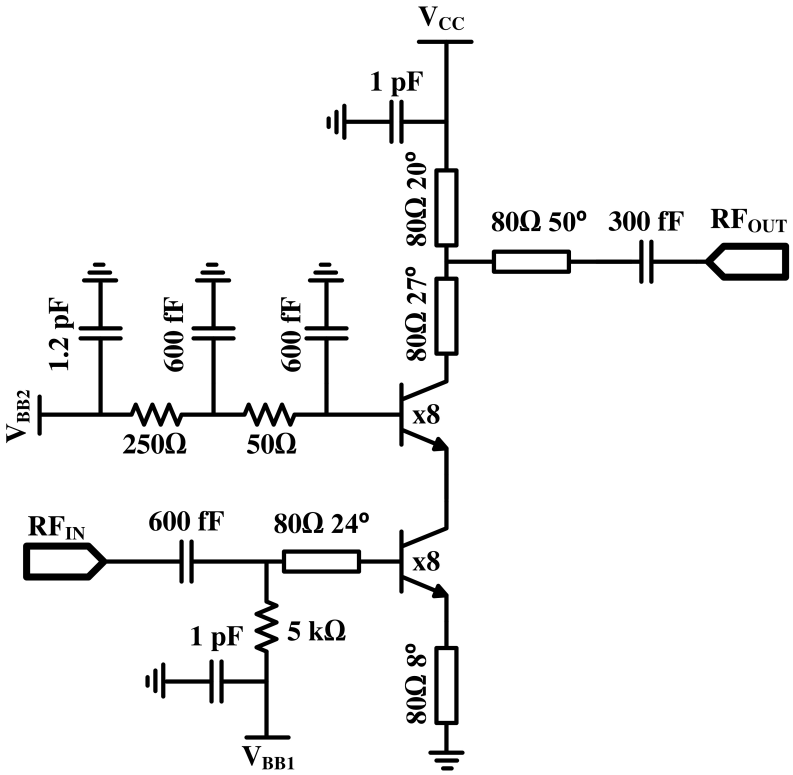


Figure 22: The detailed schematic of the designed buffer amplifier (Electrical lenghts are given for 77 GHz).

Under these circumstances, utilizing cascode topology is the best choice to achieve high gain and significant isolation. Since cascode topology does not suffer from the effect of C_μ capacitance as in the CE topology, the isolation is increased.

The output power of the frequency octupler should be at least 0 dBm for achieving at least 10 dBm power level for the transmitted signal which ensures a detection from 200 meters theoretically, which was shown in Table 3. Therefore, at least 24 dB gain should be provided from the buffer amplifier. Since it is not feasible to achieve such high gain with enough reverse isolation, two identical cascaded amplifiers were used. The detailed schematic of the designed buffer amplifier is given in Figure 22. An inductive emitter degeneration was implemented, which is equivalent to 25 pH inductance value to make the real part of the input impedance to 50 Ω. Also, a series inductance with a value of 60 pH was implemented to achieve an input impedance with almost pure resistance. The number of transistors was selected as x8 by considering the required output power and noise figure. When the gain performance is considered, this designed amplifier achieves the peak gain around 77 GHz and achieves a narrowband performance. Therefore, this behavior can be considered as

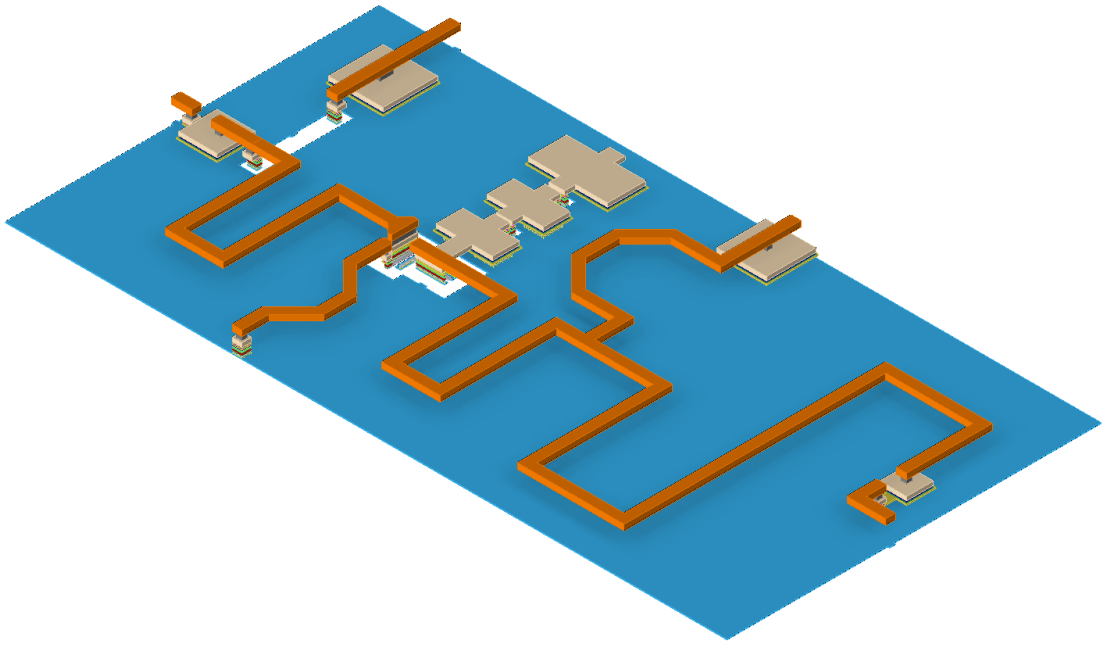


Figure 23: The 3D layout view of the designed two-stage buffer amplifier.

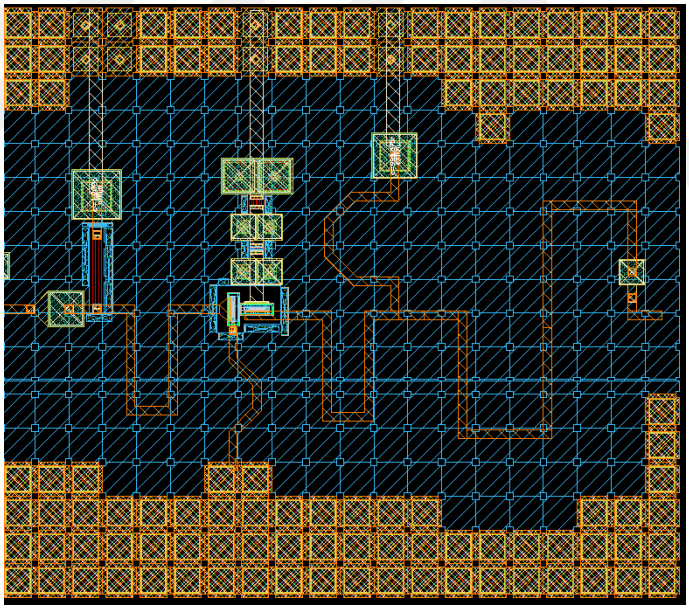


Figure 24: The layout of the designed buffer amplifier.

a bandpass filter, which increases the suppression of the harmonics even further.

TM2 layer of the technology was used to implement all the transmission lines and inductors. Metal1 layer was utilized as the ground plane to implement microstrip configuration. The parasitic effects of RF pads were included in the output impedance matching network in the simulations. MIM capacitors from the technology were used for as bypass and DC-block capacitors. Electromagnetic and harmonic

balance simulations were performed with ADS Momentum software. The 3D layout view of the designed buffer amplifier is shown in Figure 23.

3.3.2 Simulation Results

The layout of the designed buffer amplifier is given in Figure 24. Figure 25 presents the simulated s-parameter results for the single-stage buffer amplifier. The maximum gain is 12.25 dB at 77 GHz. The input and output return losses are better than 10 dB between 76-81 GHz. The reverse isolation is almost 20 dB in the operating frequency. Although it is not unfair to expect higher isolation values with cascode topology, since achieving high gain was the priority, this isolation value is still sufficient to isolate input and the output parts from each other. Input and output power relationship are given in Figure 26. The input-referred 1-dB compression point of the amplifier is -8 dBm which ensures cascading two of these amplifiers would not compress. Also, it can be seen from the figure that this designed amplifier saturates around 6.3 dBm.

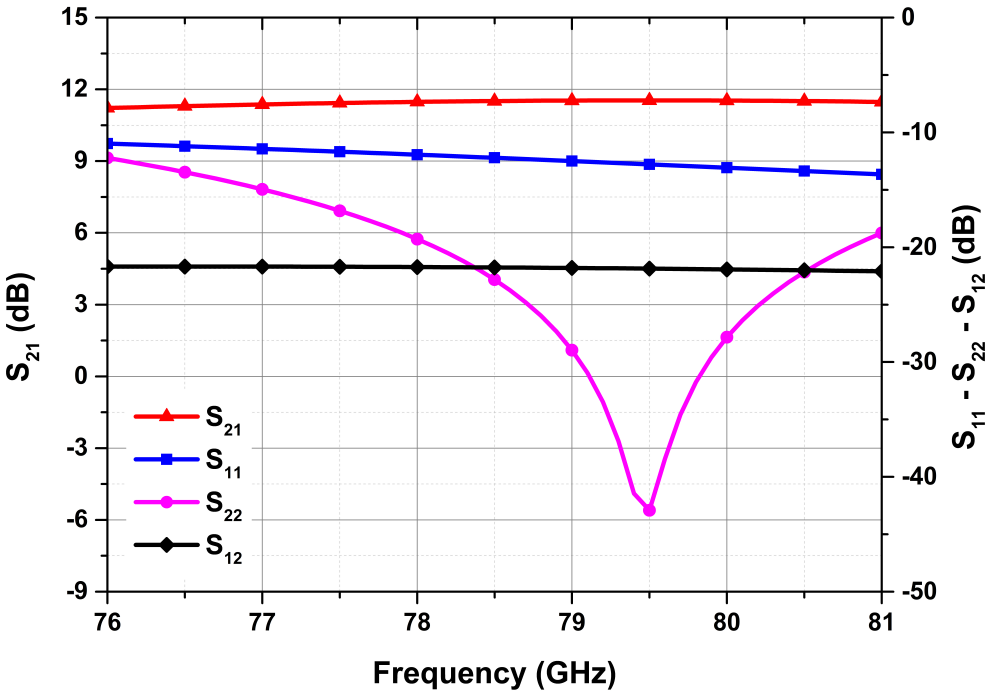


Figure 25: The simulated s-parameter results of the designed buffer amplifier.

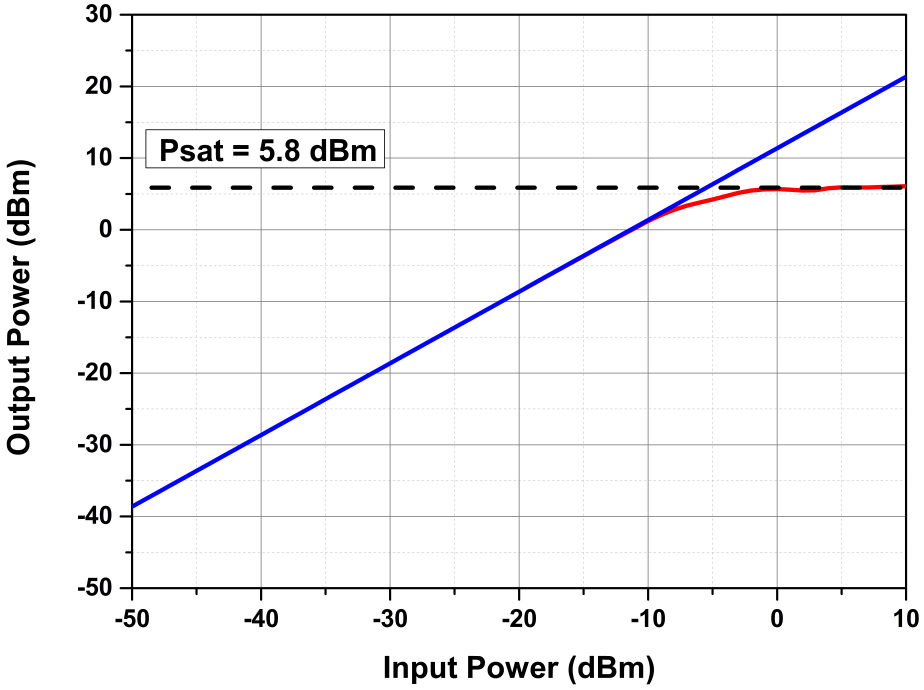


Figure 26: The simulated 1-dB compression point of the designed buffer amplifier.

3.4 Power Detector

3.4.1 Circuit Design and Implementation

Power detector converts an RF signal into a DC voltage at the output. When there is a change in RF signal, DC voltage at the output changes proportionally. In order to make an accurate detection in the output voltage, the relationship between the input RF signal and output DC voltage should be linear. Thus, the power detector designed such that it operates in the square-law region. Also, since the designed power detector should detect the changes in the leakage signal from transmitter to receiver in order to adjust the impedance tuner and compensate the impedance mismatch between the antenna and the impedance tuner, the designed power detector needs to have the ability to sense as low power levels as possible. Because the whole system is a long-range RADAR system, thus received power can be as low as -100 dBm in theoretical calculations.

The detailed schematic of the designed power detector is given in Figure 27. As can be seen from the figure, the power detector was designed with a cascode-

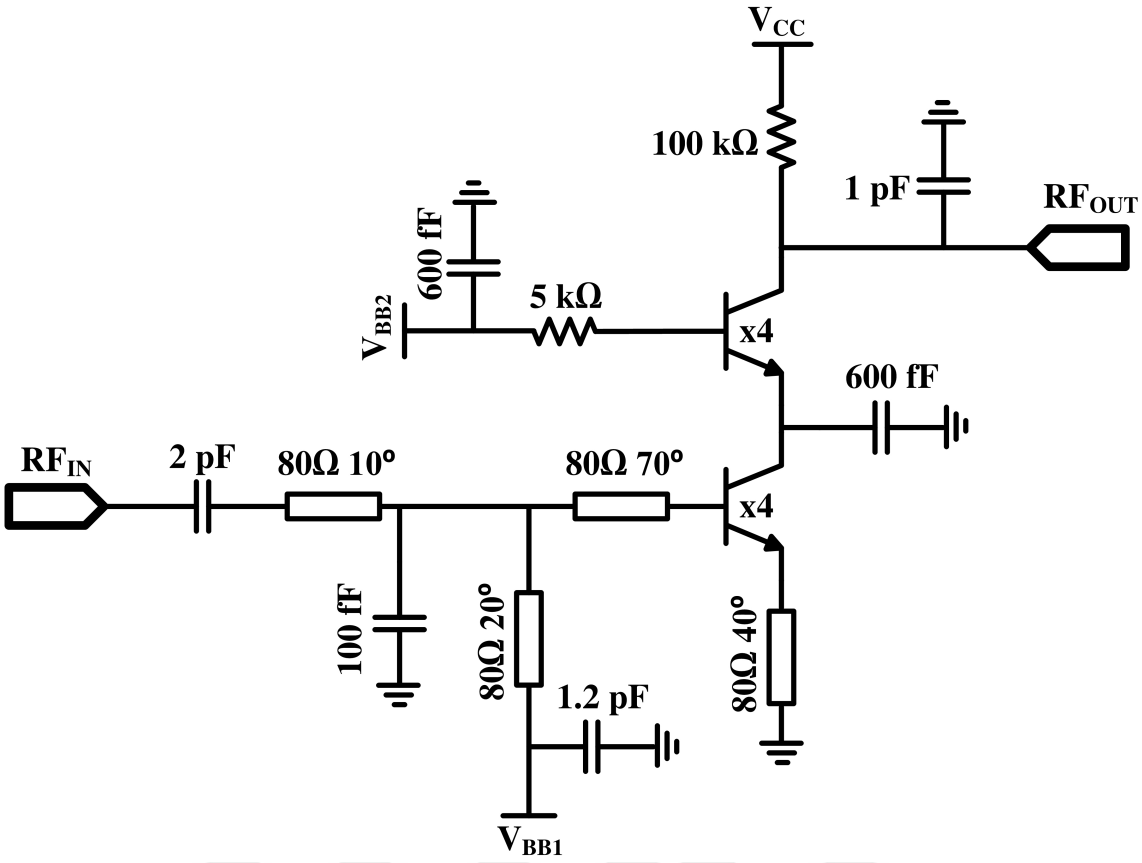


Figure 27: The detailed schematic of the designed power detector (Electrical lenghts are given for 77 GHz).

like configuration. The single-ended design was preferred for reducing complexity. When an input signal is applied, the CE transistor generates a second-order DC response. The shunt capacitor, which has a value of 600 fF placed in between the CE and CB transistors, eliminate the first-order response. Further, this shunt capacitor creates an almost perfect AC grounding at that node, which isolates the input impedance CE transistor from the rest of the circuit. Even though the output noise voltage is increased a little due to CB transistor, since the CB transistor keeps the collector voltage of the CE transistor constant, it becomes easier to keep the CE transistor in the active mode of operation. Thus, the CB transistor operates as a unity gain current buffer amplifier. Further, the maximum voltage drop at the output node is determined by the collector-emitter breakdown voltage BV_{CEO} of the CB transistor instead of CE. Additionally, it has been proven that a SiGe HBT with forced emitter current can achieve almost twice the nominal value of the BV_{CEO} value [32]. Therefore, it is possible to apply higher supply voltage V_{CC} values to the circuit, and it leads designers to use higher valued load resistor. This

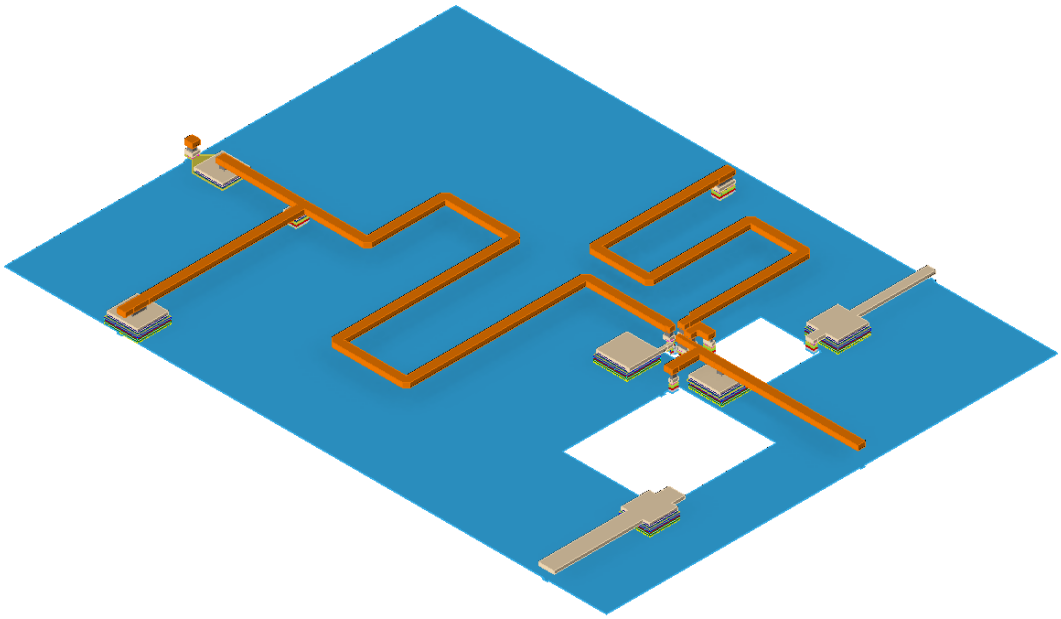


Figure 28: The 3D layout view of the designed power detector.

results in an improvement in NEP performance and larger responsivity values with the power detector.

The relationship between responsivity and NEP is given in equation 32

$$NEP = \frac{v_n}{\beta} \tag{32}$$

where β is the responsivity, itself and v_n is the RMS value of the output noise voltage, which is normalized to 1 Hz bandwidth. It is clear that responsivity and NEP are inversely proportional to each other; therefore, achieving higher responsivity requires minimum achievable NEP value.

Value of the load resistor contributes to the responsivity and NEP of the power detector. The responsivity of the circuit is proportional to the load resistor, whereas NEP does not. Because as the value of the load resistor is increased, the output noise voltage is also increased. If the value of the load resistor is increased, the supply voltage V_{CC} has to be increased in order to keep CB transistor out of saturation region. NEP changes concerning the number of transistors in the design. Also, the number of transistors affect the input impedance matching. Further, the number of transistors affect the nonlinear behavior, which is essential because the second-order response is needed at the output. When the number of transistors is minimum,

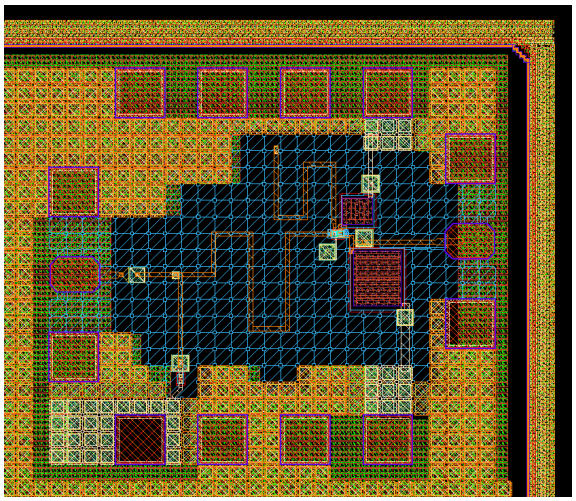


Figure 29: The layout of the designed power detector.

nonlinear behavior is enhanced. Besides, the bias point of the transistors is important for generating harmonics. So, the class-B point which corresponds to 0.76 V for this technology is the best option to generate harmonics. Besides, the quality of input matching affects NEP; therefore, input matching effects responsivity. Since reflected power has no possibility to be detected, the input part of the circuit must be matched over the frequency band. Transmission lines are used as a tee formation with a shunt capacitor to utilize the input matching sufficiently. Lastly, the load resistor was realized as large as possible in terms of area to keep 1/f noise lower at the output. By considering these circumstances, the supply voltage V_{CC} was set to 10 V, the load resistor was chosen as 100kΩ, and the number of transistors was chosen as x4.

All the transmission lines were implemented by using the TM2 layer of the technology. Metal1 layer was utilized as the ground plane to implement microstrip configuration. The parasitic effects of RF pads were included in the input impedance matching network in the simulations. MIM capacitors from the technology were used for as bypassing the feed lines and blocking the DC signals on the RF signal path. Electromagnetic, transient, and harmonic balance simulations were performed with ADS Momentum software. The 3D layout view of the designed power detector is shown in Figure 28.

3.4.2 Simulation Results

The layout of the designed power detector is given in Figure 29. The area of the power detector is only 0.114 mm^2 without the pads. The total quiescent power consumption is 0.89 mW. The s-parameter results of the designed power detector were shown in Figure 30. The input return loss is better than 15 dB between 76-81 GHz. The simulation for responsivity and NEP were calculated by harmonic balance simulations. The DC voltage difference at the output in the logarithmic domain has a linear response with respect to the input power change. This relationship is presented in Figure 31. Between input power levels of -50 dBm and -20 dBm, the output voltage shows a linear response with respect to the change in input power. The slope of this figure equals to the responsivity of the designed power detector. The NEP value of the designed power detector is simulated by using transient simulations. Figure 32 and Figure 33 show the simulation results for responsivity and NEP, respectively. Responsivity was simulated as 94.5 MV/W at 77 GHz whereas NEP was calculated as 2.55 $fW/Hz^{1/2}$ at 77 GHz. The NEP is smaller than 28 $fW/Hz^{1/2}$ between 76–81 GHz.

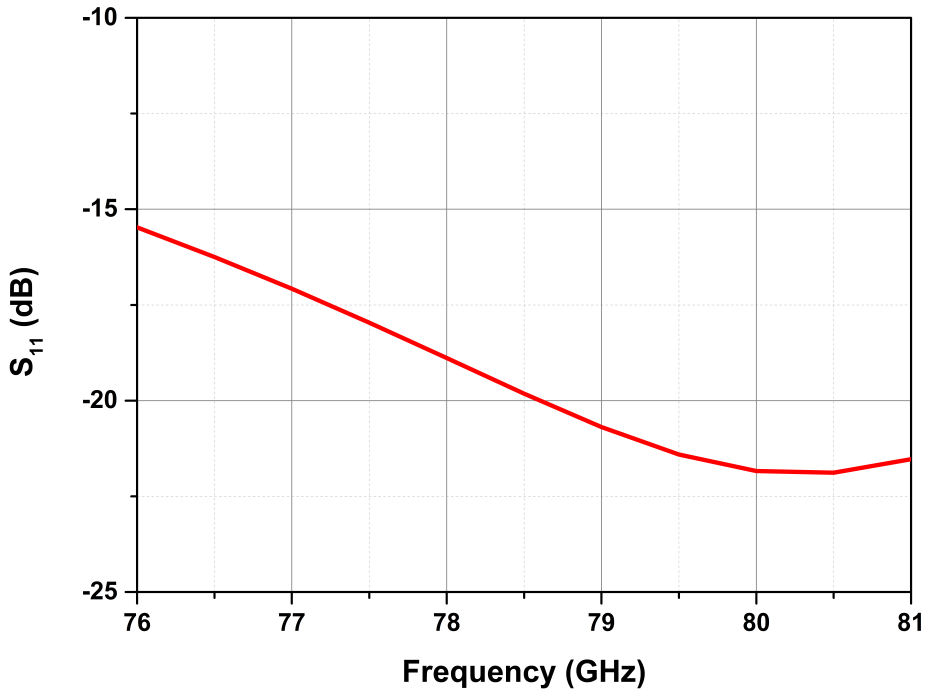


Figure 30: The simulated input return loss of the designed power detector.

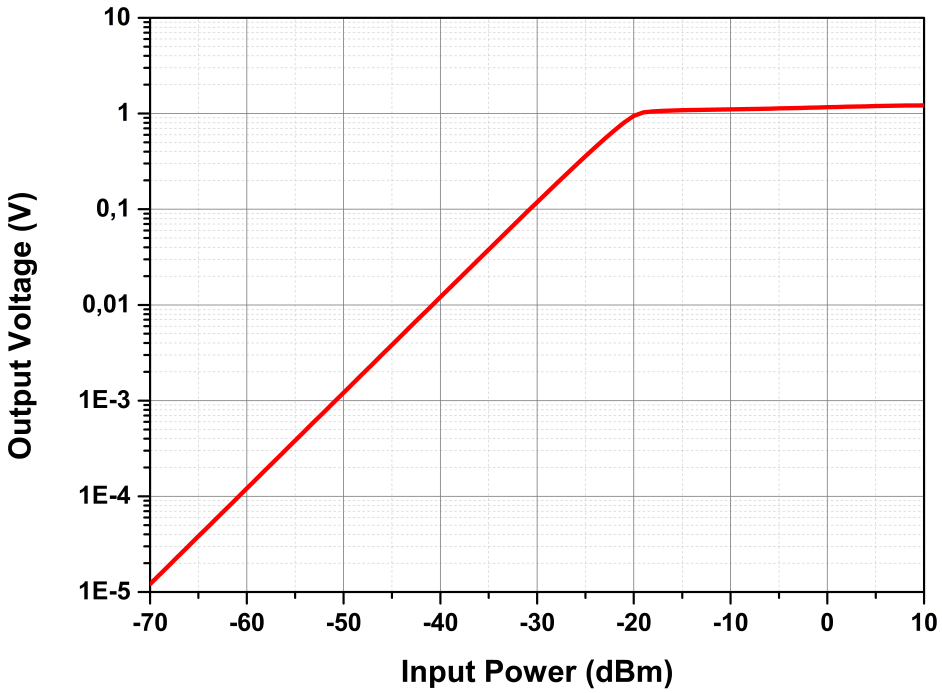


Figure 31: The simulated output DC voltage of the designed power detector.

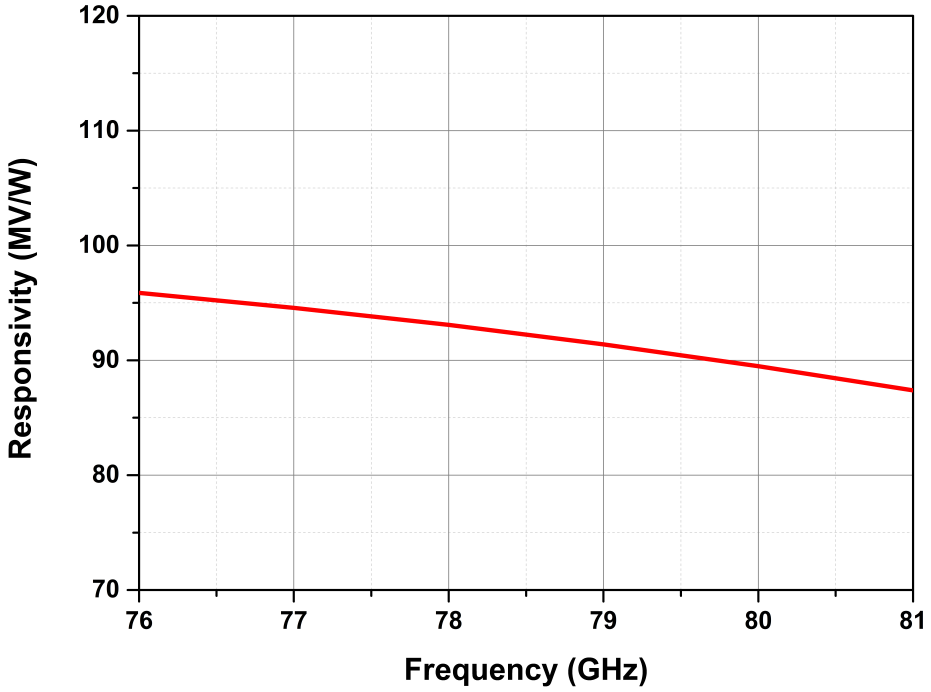


Figure 32: The simulated responsivity of the designed power detector.

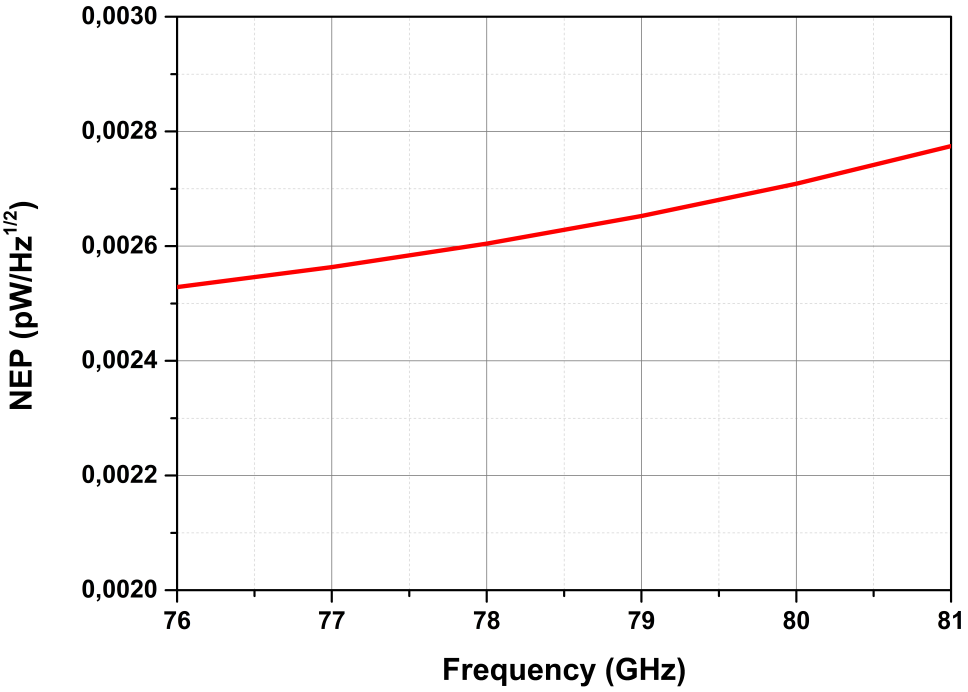


Figure 33: The calculated noise equivalent power of the designed power detector.

3.5 Electrical Balance Duplexer

An electrical balance duplexer (EBD) consists of an impedance tuner, a hybrid transformer, and a digital control circuit. The block diagram of the EBD is given in Figure 34. As given in the figure, EBD has four ports. TX-port is connected to the PA, RX-port is connected to the LNA, ANT-port is connected to the antenna and BAL-port is connected to the impedance tuner. The digital control circuit is connected to the impedance tuner, which can change the impedance and improve the impedance mismatch between ANT-port and BAL-port. Therefore, this section contains the designs of the hybrid transformer, impedance tuner, and digital control circuit.

3.5.1 Hybrid Transformer Design and Implementation

Hybrid transformer can be considered as the core of an EBD that isolates bi-conjugate ports from each other, when certain conditions are satisfied. ANT-port and BAL-port, RX-port and TX-port are the bi-conjugate ports of EBD. These

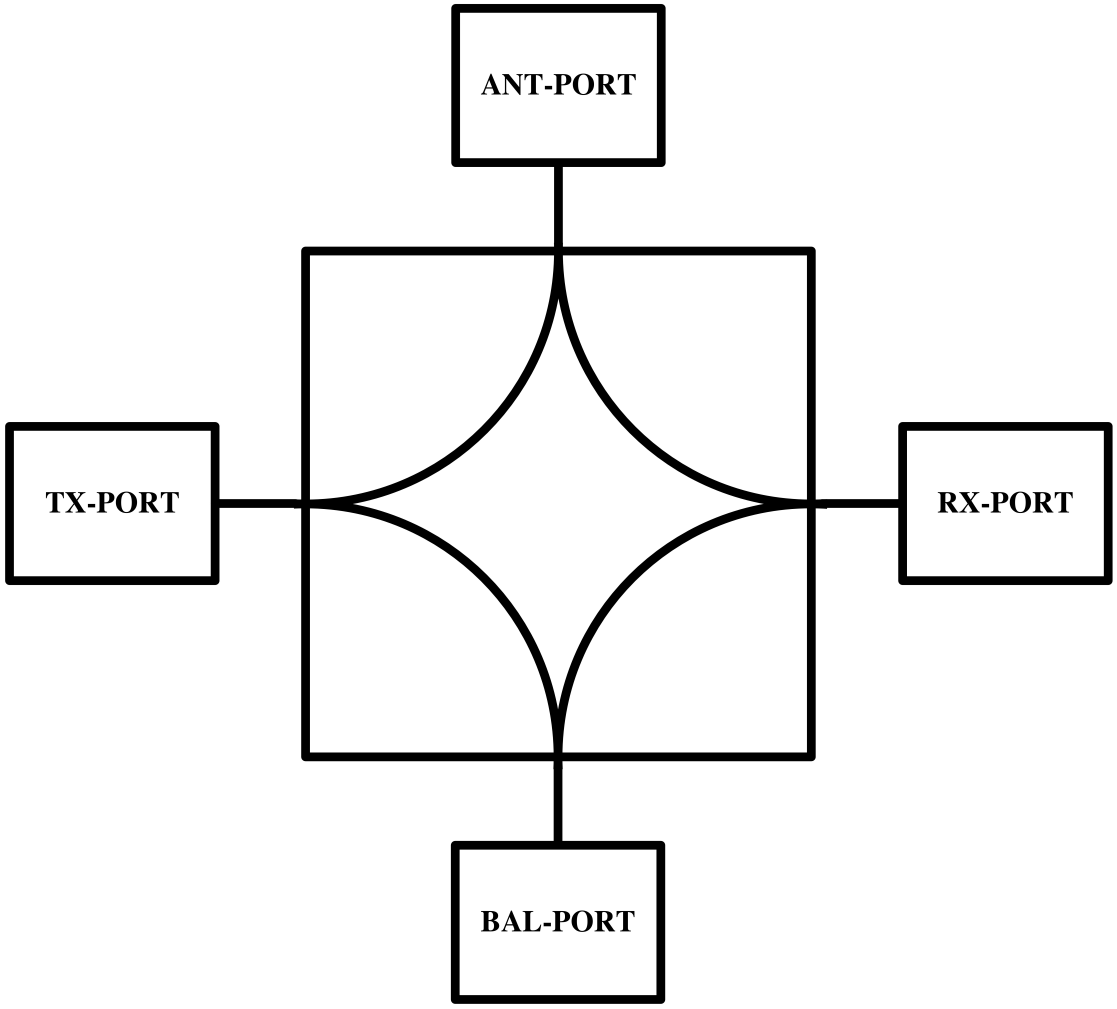


Figure 34: The block diagram of an electrical balance duplexer.

ports are electrically isolated from each other due to this bi-conjugacy property. Perfect bi-conjugate ports and maximum isolation can be achieved when equation 33 is fulfilled [33].

$$Z_{ANT} = Z_{BAL} = \frac{Z_{RX}}{2} = 2Z_{TX} \tag{33}$$

Z_{ANT} is the impedance of ANT-port, Z_{BAL} is the impedance of BAL-port, Z_{RX} is the impedance of RX-port and Z_{TX} is the impedance of TX-port in the equation above. It can be seen from the equation that, when Z_{ANT} and Z_{BAL} are matched to 50Ω, Z_{RX} must be matched to a differential 100Ω and Z_{TX} must be matched to a single-ended 25Ω impedances. Besides, these impedances enhance the RF performances of the corresponding sub-blocks. The differential 100Ω matching

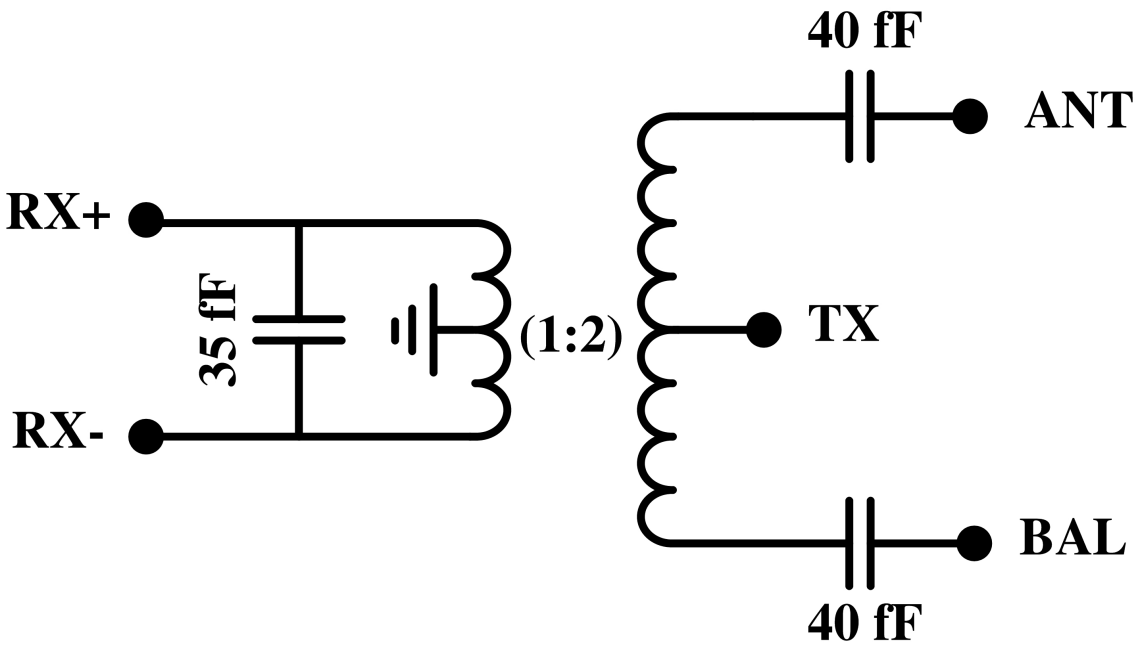


Figure 35: The lumped component model of the designed electrical balance duplexer.

between RX-port and LNA improves gain and noise figure performances of LNA whereas the single-ended 25Ω matching between TX-port and PA helps to achieve high output power for the transmitted signal. The design procedure starts with a lumped-component model in order to determine to estimate the inductance values of the primary and secondary windings. The lumped model of the designed hybrid transformer is given in Figure 35.

One of the most important parameters in hybrid transformer is to determine the turn ratio. In order to achieve simple layout, the turn ratio of this hybrid transformer is selected as (1:2). The geometry of the hybrid transformer is selected as an octagon shape. The primary inductance is found to be 80 pH and coupling coefficient k equals to 0.77. The other important design parameter for hybrid transformers is preferred technology. Since the hybrid transformer consists of inductors, which are basically transmission lines. The thickness of the layers, the distance between adjacent layers, metal resistances, dielectric constant and thickness of the substrate effects the performance directly. The primary coil of the designed hybrid transformer is one-turn octagon whereas the secondary coil is two-turn octagon. Both coils were implemented by utilizing TM2 layer of the technology. The overlapping parts between primary and secondary coils are handled by utilizing TM1 layer of the

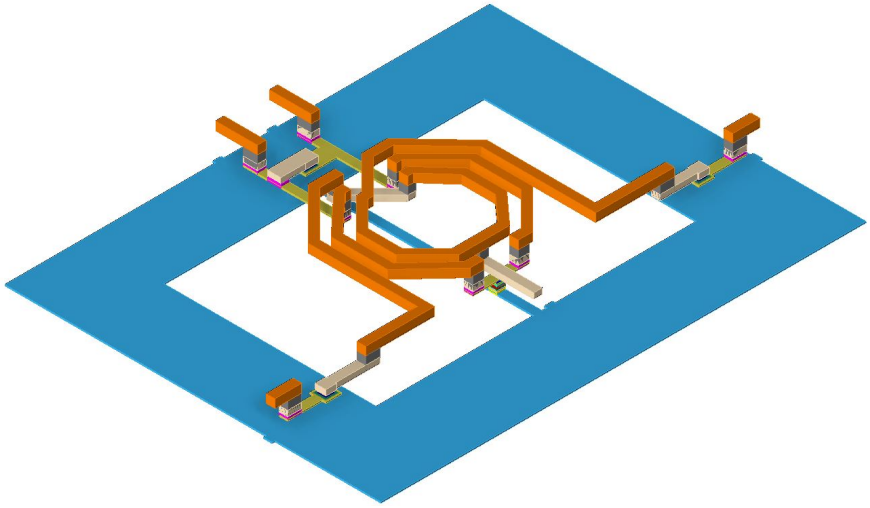


Figure 36: The 3D layout view of the designed electrical balance duplexer.

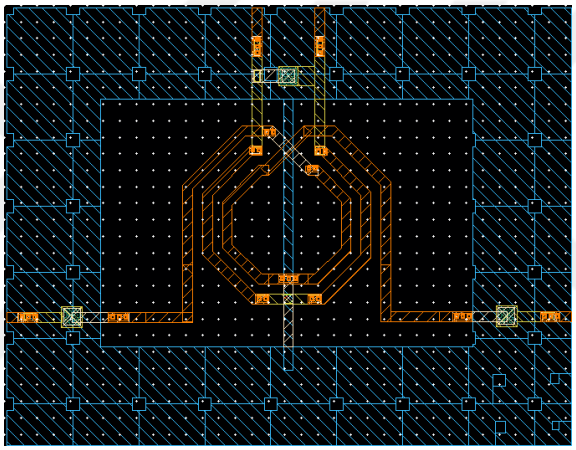


Figure 37: The layout of the designed electrical balance duplexer.

technology. Metal5 layer of the technology is used for the overlapping part between the BAL-port connection and the center-tap of the primary winding since TM1 is already used.

A shunt capacitor is used between the differential inputs of the RX-port which has 37 fF value. Two identical series capacitors were used for ANT-port and BAL-ports which have 45 fF value. Shunt and series capacitors were utilized to achieve better impedance matching and MIM capacitors were used. The thickness of the octagon-shaped windings is 3 μm. The distance between primary and secondary winding and their internal turns are selected as 3 μm as well. The radius of inner circle is 33 μm whereas the radius of the outer circle is 57 μm. The grounded center-tap is realized with Metal1 layer of the technology since Metal1 layer is used as the ground plane for entire design. The width of the grounded center-tap is chosen as 3

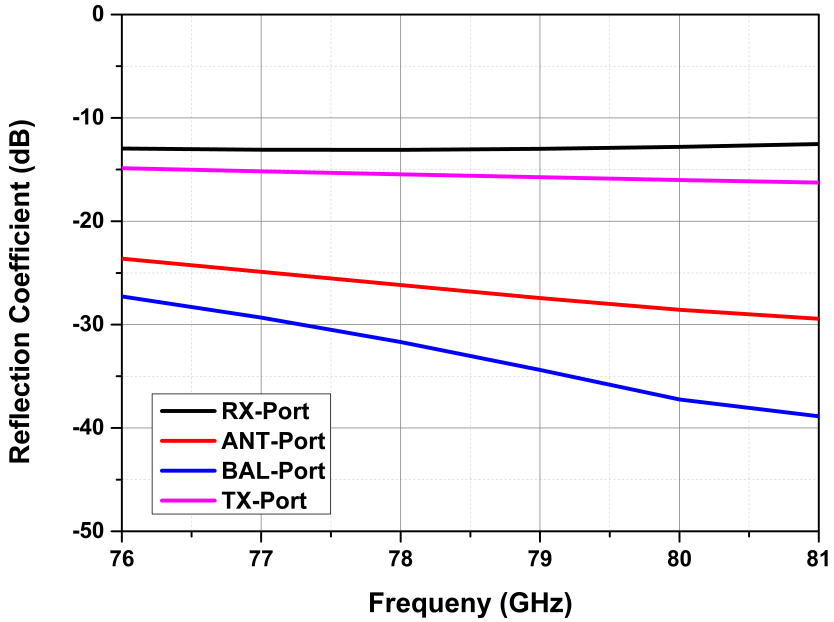


Figure 38: The simulated return losses of the designed hybrid transformer.

μm. This center-tap provides a 180° phase difference between the ports of RX-port. Therefore, a careful design is needed for the grounded center-tap. Otherwise, the differential approach at RX-port would not be achieved. The 3D layout view of the designed hybrid transformer is given in Figure 36.

3.5.2 Simulation Results of the Designed Hybrid Transformer

The layout of the designed hybrid transformer is given in Figure 37. The effective area of the designed hybrid transformer is only 0.022 mm^2. The simulation results of the s-parameters are given in Figure 38. The designed hybrid transformer has return losses for all ports better than 13 dB between 76–81 GHz. Figure 39 shows the isolation between ANT-port and BAL-port, when the both impedances are fixed. The isolation is better than 42 dB between 76–81 GHz when impedances of the antenna and balance ports are fixed. The insertion losses for TX-port and RX-port are shown in Figure 40. The insertion loss of TX-port to ANT-port is 3.85 dB whereas the insertion loss of ANT-port to RX-port is 5.5 dB between 76–81 GHz. The phase difference between the differential ports of RX-port are given in Figure 41. The phase difference is less than 0.4° between 76–81 GHz.

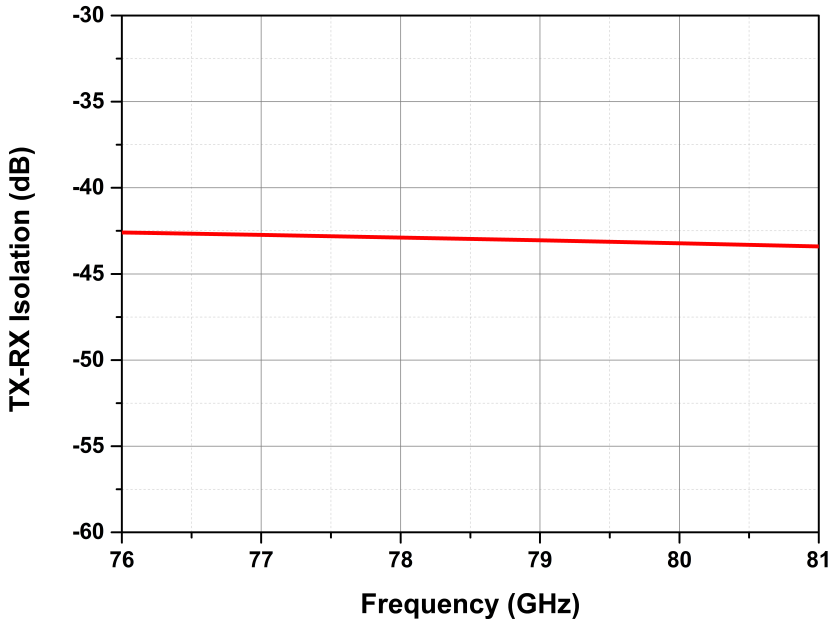


Figure 39: The simulated isolation values between TX-port and RX-port of the designed hybrid transformer.

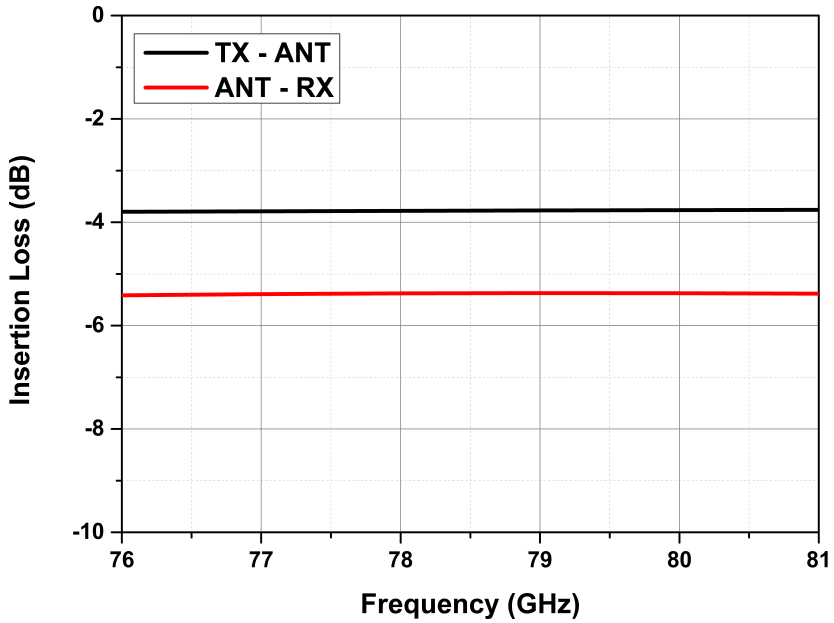


Figure 40: The simulated insertion loss values between TX-port to ANT-port and RX-port to ANT-port of the designed hybrid transformer.

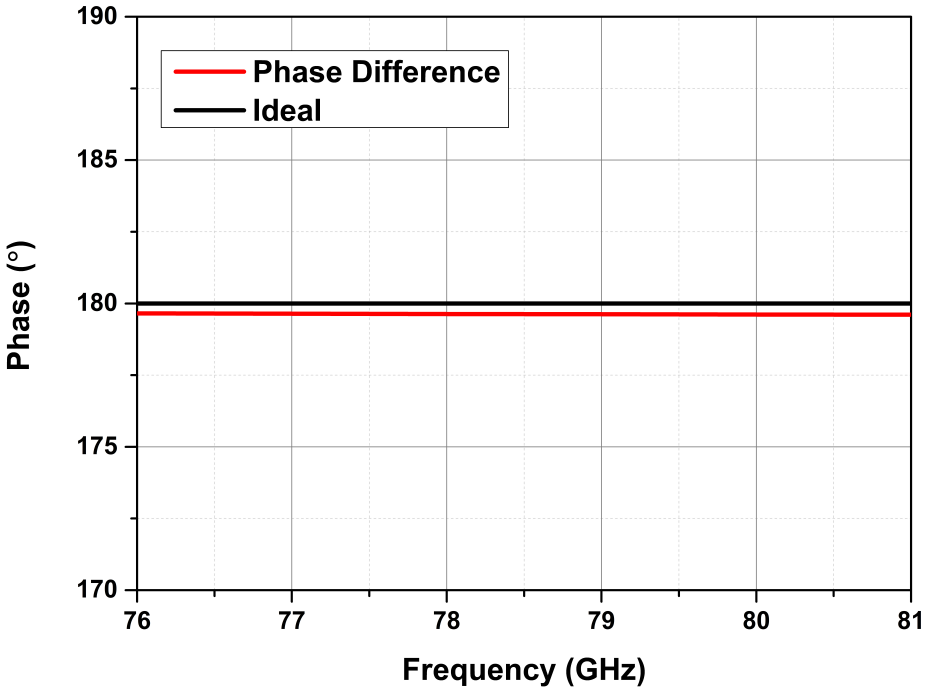


Figure 41: The simulated phase difference between the differential terminals of the RX-port of the designed ehybrid transformer.

3.5.3 Impedance Tuner Design and Implementation

Impedance tuner is necessary to compensate the impedance mismatch between the ANT-port and BAL-port of the EBD. As mentioned before, the impedance mismatch between these ports degrades the isolation between TX-port and RX-port, which deteriorates the overall performance of the system. If the isolation degrades a lot, the leakage signal between TX-port to RX-port is increased. This leakage signal could saturate the RX chain entirely if that signal achieves enough power level. Thus, keeping isolation high enough between TX-port and RX-port is very important for a monostatic RADAR system. This issue puts impedance tuner circuit in a vital place for EBD. Even though antenna is well-matched to 50Ω, impedance of the antenna can change due to the temperature and the environmental effects and process variations. Therefore, an impedance tuner circuit is necessary to compensate the changes in impedance.

In order to determine the tuning range of the impedance tuner circuit, the range of the impedance change in the antenna should be known. Since there is no pre-

determined antenna for in the scope of this thesis work, a general and wider range should be considered. Although the tuning range is important, the resolution of the tuning is also important. Because, isolation is improving as the impedance matching between ANT-port and BAL-port gets better. Therefore, covering as many different probabilities as possible improves the performance. Further, the impedance tuner should have the ability of high-power handling capability. In an extreme case if the ANT-port and BAL-port have a huge impedance mismatch, there can be a leakage from TX-port to BAL-port as well.

An impedance tuner circuit can be realized with different variable components. Resistors, capacitors or inductors can be used as variable components to tune the impedance. These variable components can be controlled either analog-controlled approach or digitally controlled approach. Analog-controlled approach does not require any additional circuits or components for implementing. Generally, analog control is performed with changing the bias voltage of the variable components such that their behavior changes. On the other hand, digital control requires switches or inverters to control the variable components or the variable component banks. The trade-off between analog and digital control is between tuning resolution and complexity. In analog control, tuning resolution is very high, theoretically infinite. The only limitation is the minimum amount of change in the voltage control and corresponding response of the variable components to this change. In digital control, it is easy to control and change the impedance due to existence of switches, which reduces complexity very much rather than analog control.

The variable components can differ as mentioned before. Utilizing variable resistors is one option to implement the variable impedance unit. However, variable resistors create linearity issues and degrades the performance of EBD. Variable inductors can be another option to implement the variable impedance unit. Unfortunately, designing variable inductors is hard and they are bulky elements. Lastly, variable capacitors can be used instead of variable inductors or resistors. Variable capacitors can be achieved with transistors or capacitor banks. Tuning the bias voltages of the transistors can be easily achieved by analog control. However, for automated systems, it is not possible to have analog control with autonomous control systems. Therefore, capacitor banks were used to implement the variable capacitors with

digital control.

The design topology is selected as a similar approach like a loaded-line phase shifter [34]. Loaded-line phase shifter utilizes two different loads that are connected to each other with a quarter-wave transmission line. These loads are controlled with switches. When switches change states, the phase response and the impedance of the phase shifter changes. Thus, this topology is modified and adapted for designing the impedance tuner. Capacitor banks help to cover capacitive parts in the smith chart. In order to cover inductive parts in the smith chart, transmission lines were designed accordingly. Note that even electrically short transmission lines can provide enough inductance at these frequencies. Hence, utilizing transmission lines instead of inductors occupy less area and eases the design.

In this thesis work, it was aimed to cover VSWR = 2 circle which corresponds to almost 10 dB return loss with this designed impedance tuner. The capacitor banks utilized in the design consists of several branches which has a switch and a fixed capacitor. Each branch includes capacitors that have values of multiples of two. Also, each capacitor bank is identical. The minimum value of a capacitor determines the minimum tuning resolution whereas the maximum value of a capacitor determines the maximum tuning range. Also, the length of the transmission lines that connect these capacitor banks contributes the tuning range of the circuit. The minimum and the maximum capacitor values are found to be 10 fF and 40 fF respectively in the ADS simulations. Therefore, the number of branches in each capacitor bank is three. Further, number of capacitor banks is selected as four, to be able to cover the targeted VSWR circle. Since the impedance tuner is a one-port design, the output part of the circuit was terminated with a 50Ω resistor. The detailed schematic of the designed impedance tuner is given in Figure 42.

Switching operation in each capacitor bank was performed with HBT transistors. In order to increase isolation and decrease loss due to the switching circuit HBTs were used as reverse-saturated approach [35]. Number of transistors were selected as x2 in order to optimize insertion loss and isolation performance of the switch. The parasitic effects of the switches were kept as negligible as possible to keep the capacitor banks consistent to their designed values. All the HBT switches are biased with 5kΩ resistor. The bias voltage was selected as 1 V. Further, small-sized HBTs

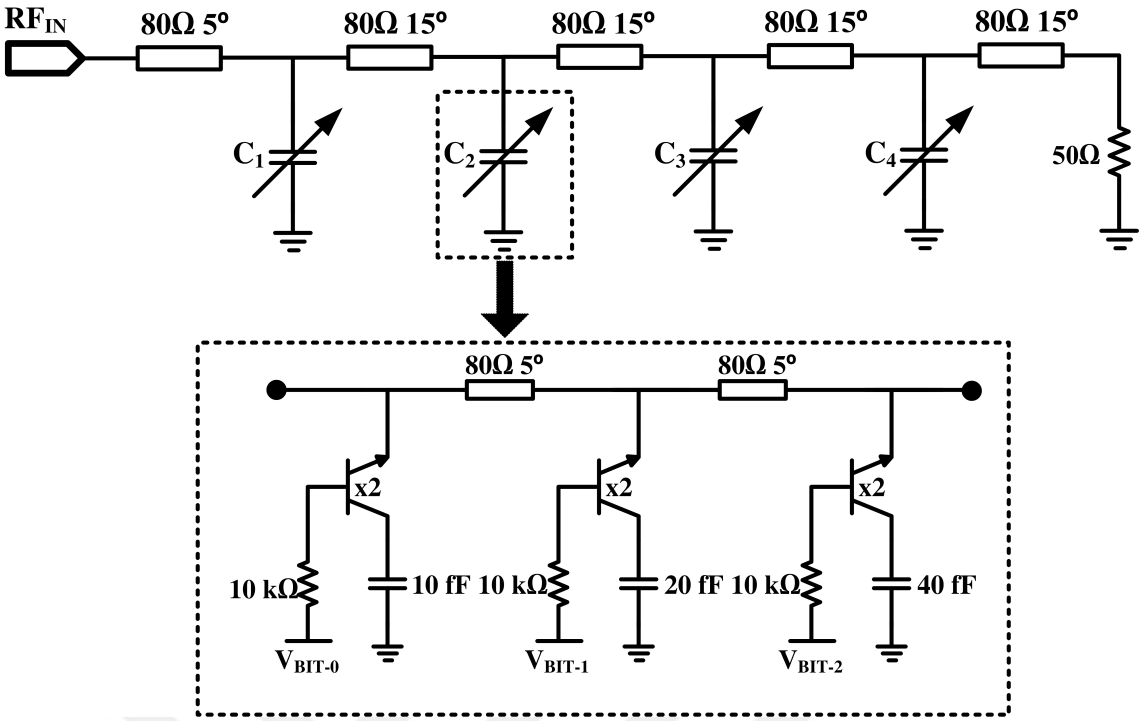


Figure 42: The detailed schematic of the designed impedance tuner.

have better linearity performance, which improves the high-power handling capability. Also, high-power performance of the utilized HBT switches were analyzed. If the power level at TX-port is in between 10–15 dBm, signal power at the BAL-port will be in between 7–12 dB. The lost power arises from ideal 3-dB loss due to the nature of EBD. This power level at the BAL-port corresponds to a voltage values of 0.5–0.9 V. This voltage gap is not affecting the linearity of the designed impedance tuner circuit

All transmission lines were realized with utilizing TM2 layer of the technology. Metal1 layer was used as ground to realize microstrip transmission line configuration. The effects of parasitic capacitances due to RF pads were included to the input and output impedance matching networks. MOM capacitors were used instead of MIM capacitors in the capacitor banks. Because less than 30 fF MIM capacitors correspond to very small dimensions. The unwanted effects of process variations can be dominant with such small dimension. Thus, the value of the capacitors can change, and it would lead distortion in the maximum covering range and tuning resolution. Therefore, MOM capacitors were designed to have consistent capacitor values. The MOM capacitors were implemented by using TM2–M3 layers of the technology. Electromagnetic simulations were carried out with ADS Momentum

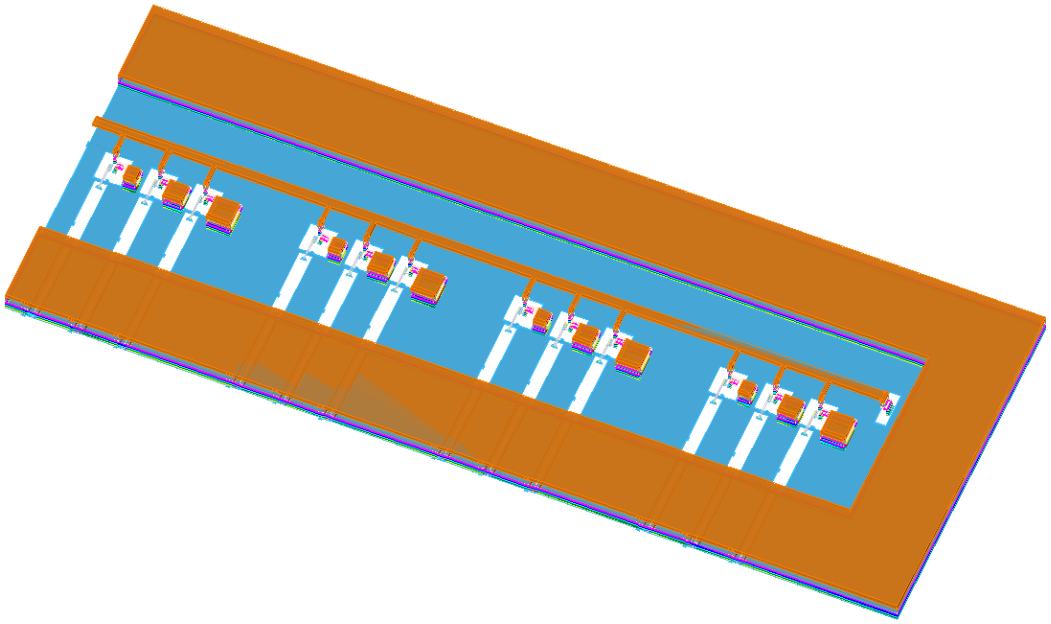


Figure 43: The 3D layout view of the designed impedance tuner.

software. The 3D layout view of the designed frequency octupler is shown in Figure 43.

3.5.4 Simulation Resuls of Impedance Tuner

Figure 44 presents the simulated impedance values for the designed impedance tuner. The blue bold circle represents VSWR = 2 circle and the red dots represent different impedance states. It can be seen from the figure that VSWR = 2 circle is almost fully covered with very fine and separate 2^{12} states. This provides EBD to have a huge covarage capability with high precision.

3.5.5 Digital Control Circuit Design and Implementation

Capacitor banks in the designed impedance tuner are controlled with DC bias voltages applied as logic inputs, either on or off. Since there are twelve capacitor branches in total, it is not feasible to feed DC bias voltages individually to every switch. Because twelve signal pads and at least one more ground pad would be required to implement individual DC bias trees. This would increase the area and the cost of the design. Also, it is not possible to control every bias system in an autonomous way. Therefore, a digital control circuit was designed as a serial to

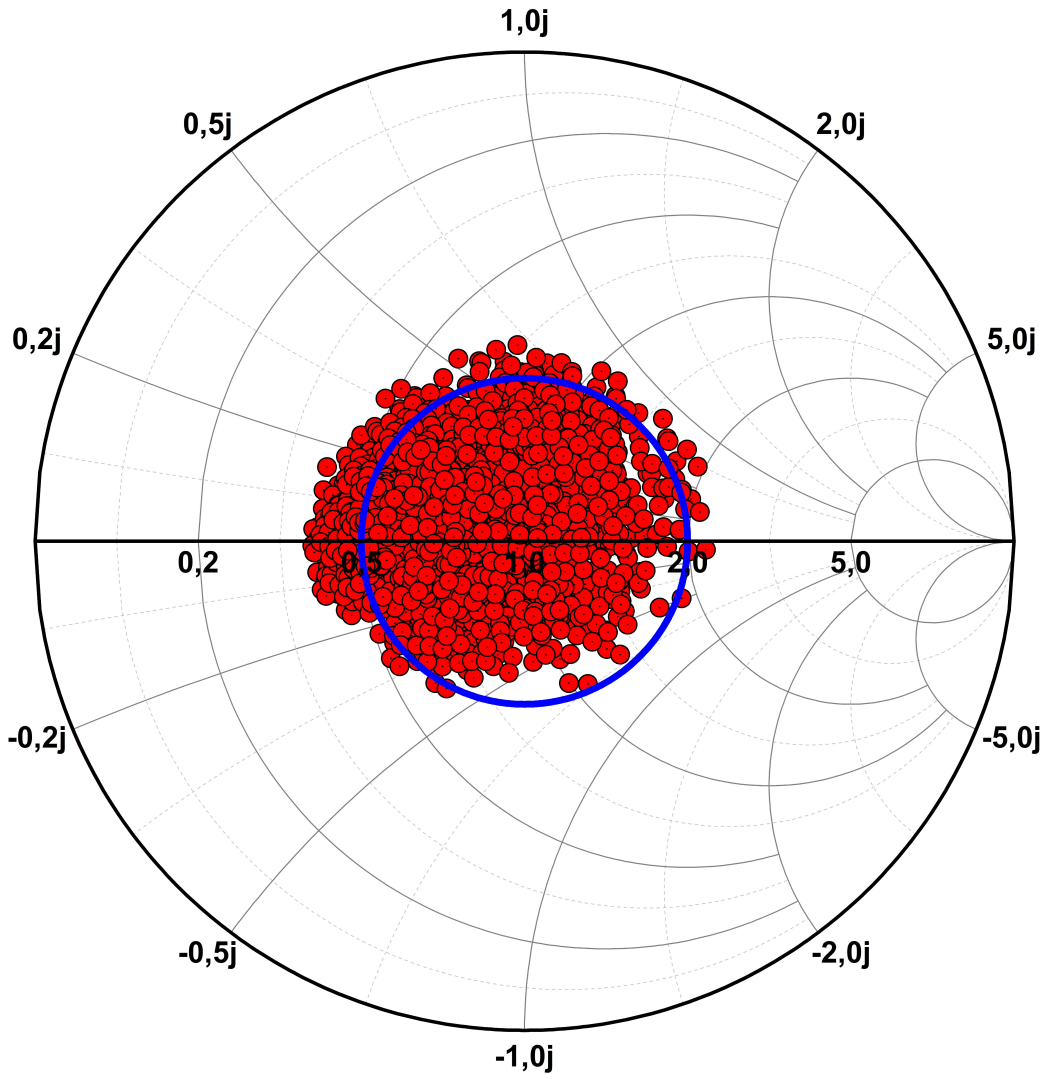


Figure 44: The simulated impedance states of the designed impedance tuner.

parallel interface (SPI). An input is taken for each clock cycle and then all the inputs are pushed into the circuit. The digital control unit was designed with Xilinx ISE Design Suite. The Verilog code was tested and verified that it is functional. After that, the Verilog code of the digital control unit was converted into a netlist file by Synopsis. Cadence Encounter tool was used to generate the layout of the digital control unit with respect to the corresponding netlist file. The layout of the designed digital control unit was given in Figure 45. This circuit was designed by Abdurrahman Burak, who is a member of SÜMER Research Group.

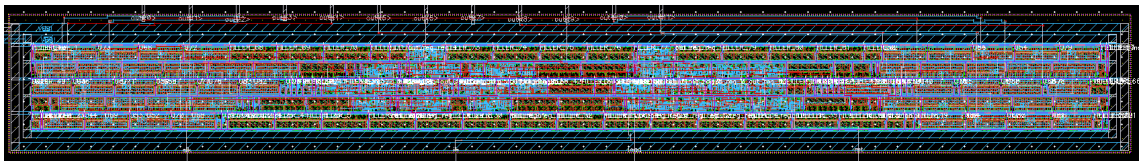


Figure 45: The layout of the digital control unit.

3.5.6 Simulation Results of Electrical Balance Duplexer

Figure 46 & 47 show that the isolation between TX-port to RX-port and the impedance tuning performance of the designed EBD with three different antenna impedances. Figure 46 presents the insertion loss differences between TX and RX ports when antenna impedance is different. The isolation between TX-port and RX-port with three different antenna impedances is given in Figure 47. Both the figures prove that even though the antenna impedance changes drastically, EBD can tune the impedance of the BAL-port and compensates the impedance mismatch. Thus, the isolation between TX-port to RX-port is kept above 30 dB. Table ... shows the performance comparison of the designed EBD with similar works from the literature.

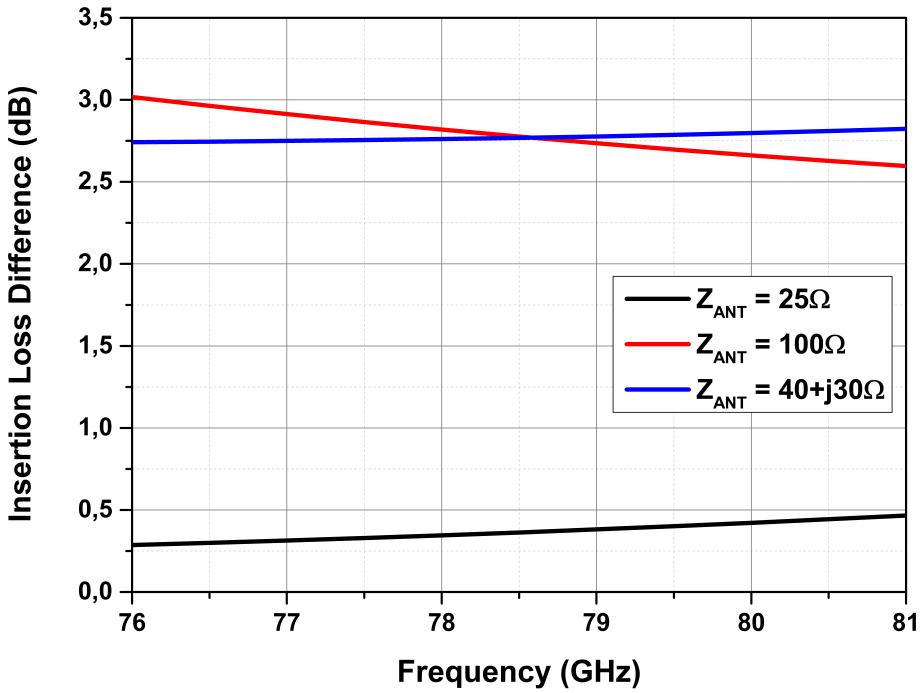


Figure 46: The simulated insertion loss differences of the ports for different antenna impedances.

Table 4: Summary of performance comparison of the designed 77 GHz EBD with previously reported EBDs implemented in silicon technologies.

	Duplexer					**Duplexer with Transceiver**		
Reference	**[36]**	**[37]**	**[38]**	**[39]**	**[40]**	**[41]**	**[42]**	**This Work***
Frequency (GHz)	2	2	2	2.1	30	60	120	**77**
Technology	90 nm CMOS	40 nm CMOS	28 nm CMOS	0.18 μm SOI CMOS	0.25 μm SiGe BiCMOS	45 nm CMOS	40 nm CMOS	**0.13 μm SiGe BiCMOS**
Duplexing Technique	EBD	EBD	EBD	EBD	EBD	Polarization +RF Cancellation	EBD	**EBD**
TX-RX ISO (dB)	>40	>45	>45	>50	>45	>70	>30	**>42.5**
TX-RX ISO Bandwidth (GHz)	0.5	0.2	0.1	0.229	1	1	14	**5**
P_{RX} (mW)	N/A	N/A	N/A	N/A	N/A	111	59.41	**48.69**
P_{TX} (mW)	N/A	N/A	N/A	N/A	N/A	206	13.56	**272.5**

*Simulation Results

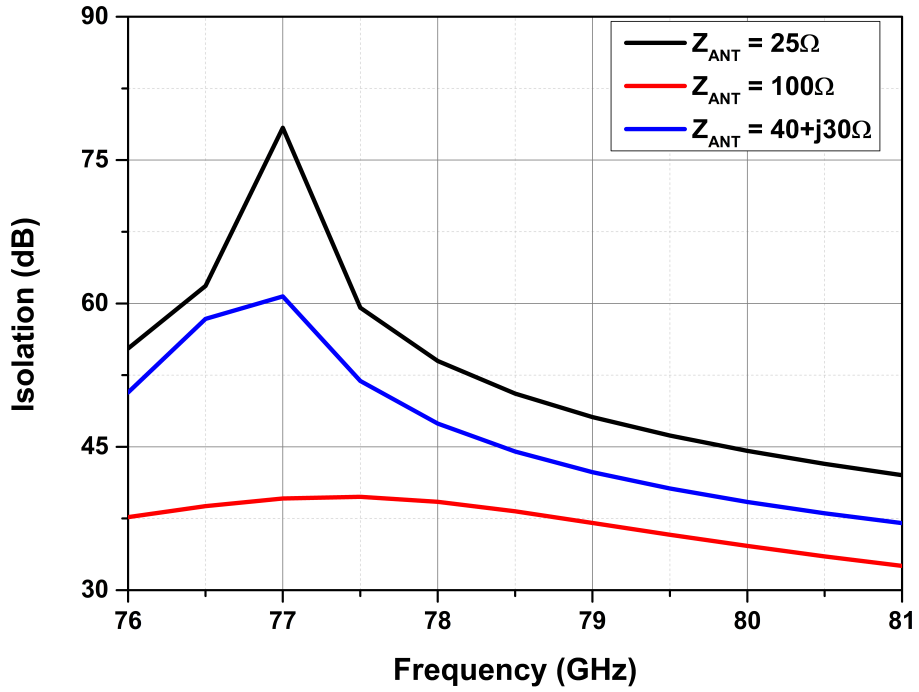


Figure 47: The simulated isolation values between the ports for different antenna impedances.

3.6 Directional Coupler Design

3.6.1 Circuit Design and Implementation

Directional coupler is a passive device with four ports. One of the ports is the input port where the signal is transitioned. One of the other ports is the isolated port, which is generally terminated with 50Ω to achieve perfect isolation. The other two ports are named as the through port and the coupled port. Names indicate the behavior of the ports such that incoming signal flows into the through port and sample of the incoming signal is transitioned to the coupled port. The configuration of a general directional coupler with port names is given in Figure 48. In order to realize the directional coupler, quarter-wave coupled transmission line is used. To achieve a coupling of 10 dB, even and odd characteristic impedances were determined accordingly. All the transmission lines were realized with TM2 layer of the technology. In order to form microstrip lines, Metal1 layer used as ground plane in the design. Electromagnetic simulations were performed in ADS Momentum. The 3D layout view of the designed directional coupler is given in Figure 49.

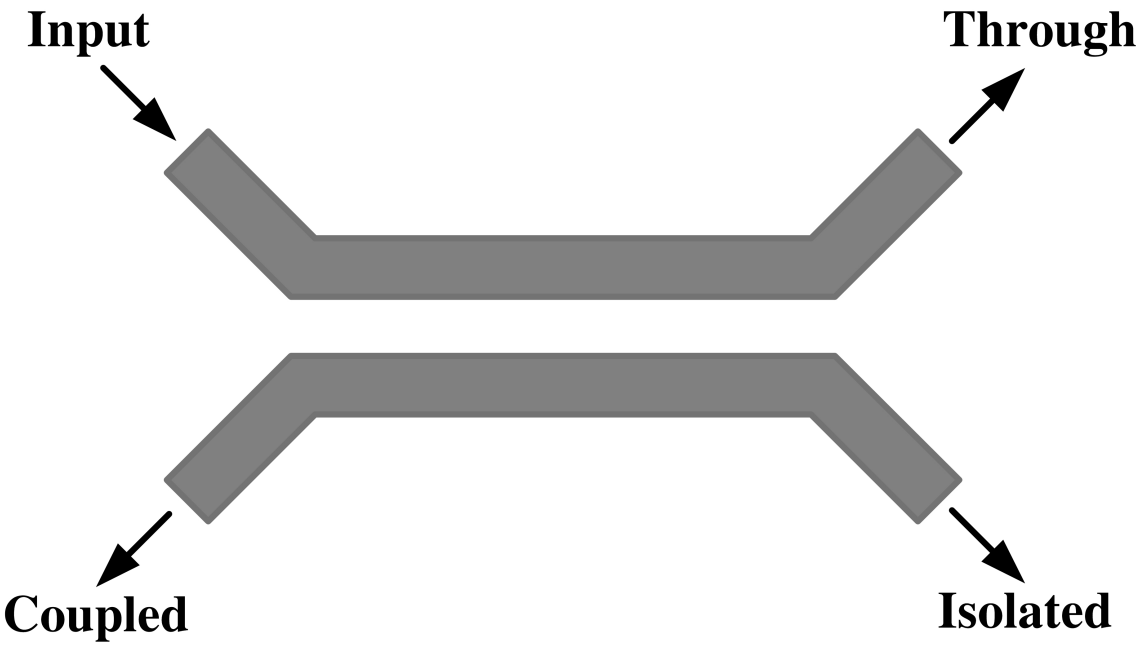


Figure 48: The representation of a single section coupled-line directional coupler.

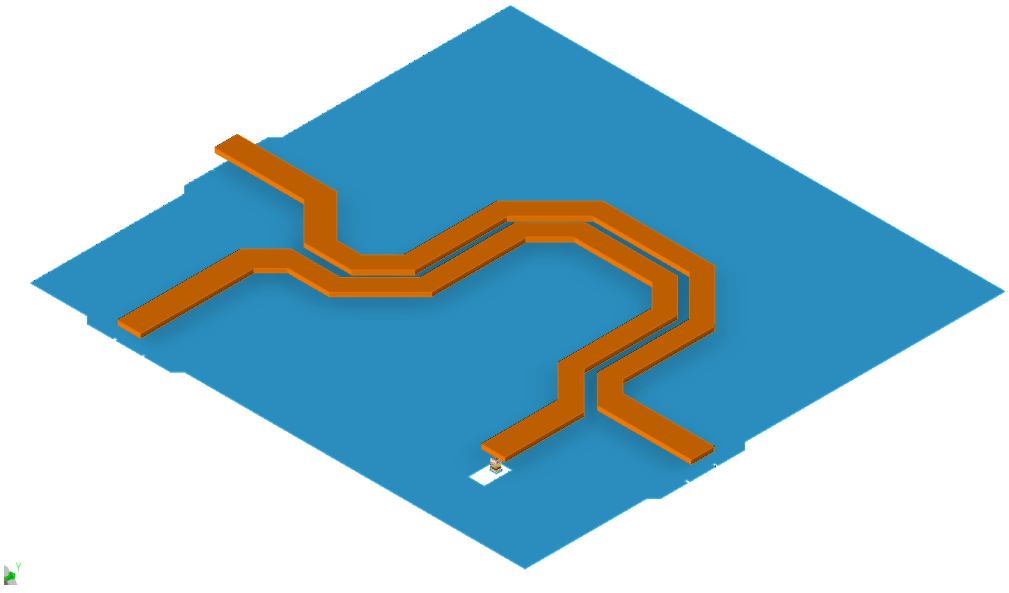


Figure 49: The 3D layout view of the designed directional copuler.

3.6.2 Simulation Results

The layout of the designed directional coupler is given in Figure 50. The simulation results for insertion loss and coupling performances of the designed directional coupler is given in Figure 51. The figure shows that the insertion loss is less than 0.6 dB and average coupling is 12.7 dB between 76-81 GHz. Figure 52 shows the isolation and directivity of the designed differential coupler. The coupler achieves

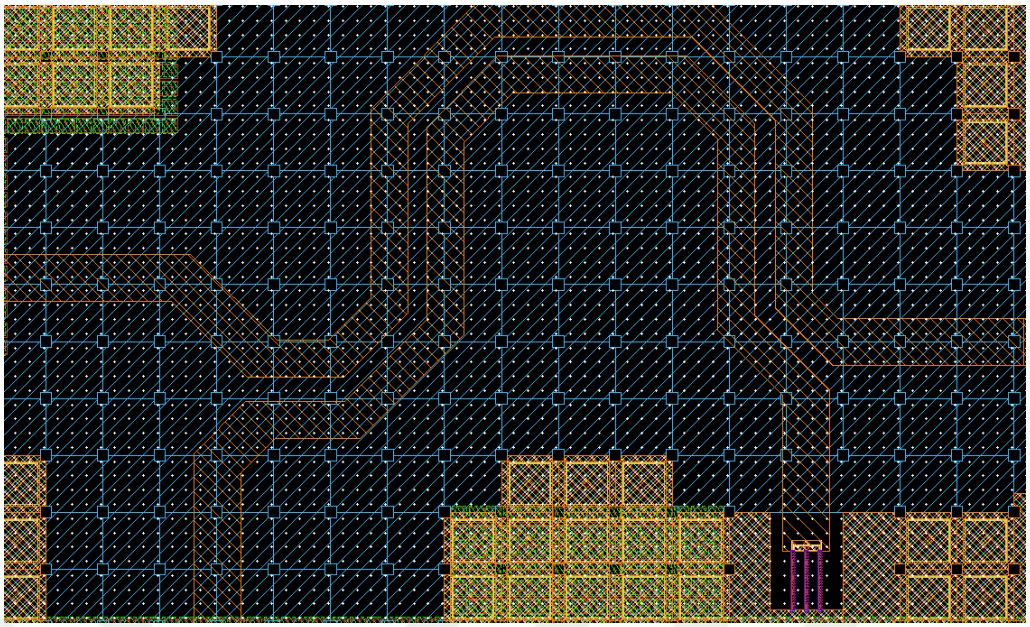


Figure 50: The layout of the designed directional copuler.

more than 36.6 dB isolation and 23.8 dB directivity between 76 – 81 GHz.

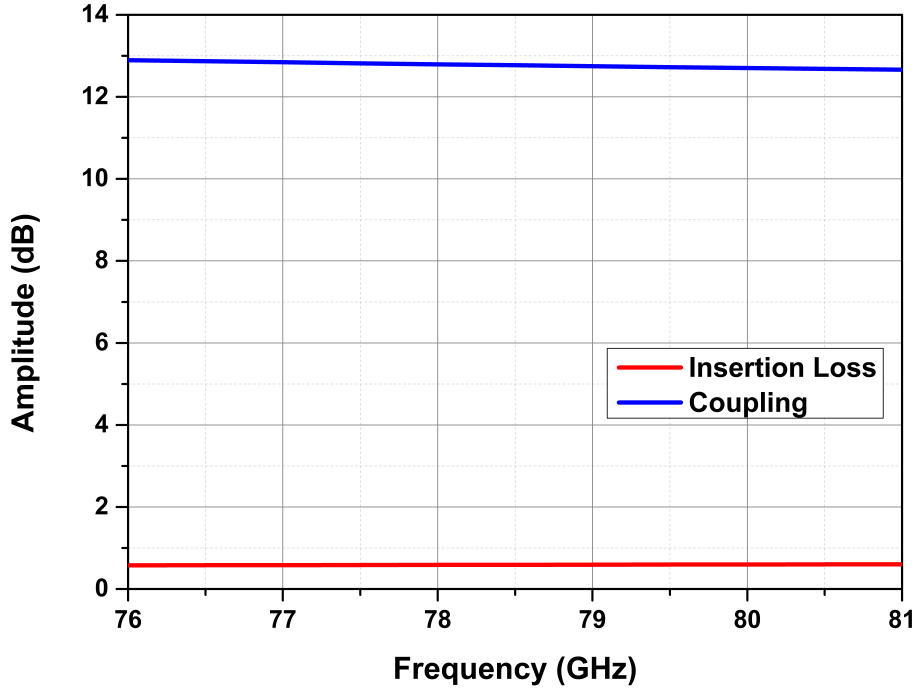


Figure 51: The simulated insertion loss and coupling of the designed directional copuler.

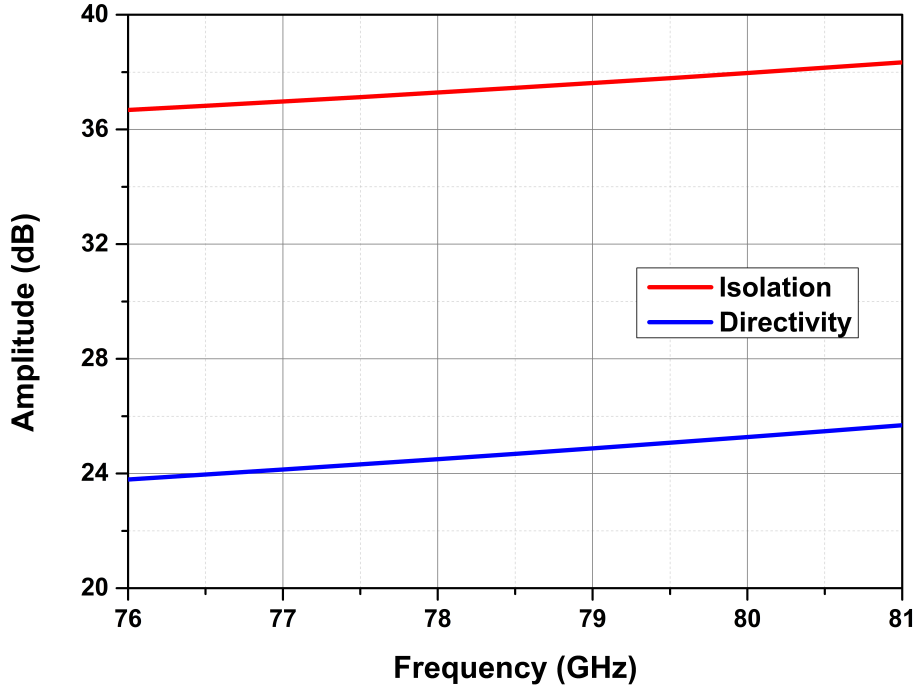


Figure 52: The simulated isolation and directivity of the designed directional copuler.

3.7 Low Noise Amplifier

3.7.1 Circuit Design and Implemantation

LNA is the most critical sub-block of the receiver chain. The designed LNA in this system is connected to RX-port of the hybrid transformer. Therefore, the LNA should be designed as differential configuration. LNA should provide high gain as much as possible because received signal can be as low as -100 dBm, as mentioned in the theoretical calculations in Table 1. The noise figure of the receiver chain is dominated by the loss of the hybrid transformer and unfortunately it is inevitable. Thus, the designed LNA should provide low noise figure. On the other hand, the power handling capability is not a concern since the input signal is very low.

The CE topology provides better noise performance than other configurations whereas the cascode topology offers higher gain performance among all. The trade-off between noise figure and gain should be carefully considered. Since it is obvious that a single stage design is not enough to provide enough gain, the noise figure performance of cascaded CE or cascaded cascode topologies were analyzed. It was

found out that CE topology is not enough to suppress the noise of the next stage. Thus, two stage cascode topology was selected in this design due to its high gain advantage and almost equal noise figure performance with respect to CE topology. However, CE topology was utilized in the last stage to achieve output matching with a proper gain. The detailed schematic of the designed three stage LNA is given in Figure 53.

Several techniques were utilized for the design of the first stage to achieve the required noise figure, gain, power handling and matching performances. Low noise figure performance was targeted for the first stage, thus the collector current for a unit emitter area was determined in favor of noise figure rather than gain. The number of transistors were selected as x6 for CE and CB transistors to realize power and noise matching simultaneously. Inductive emitter degeneration was utilized in conventional method such that the real part of the input impedance was set to 50Ω.

The second stage was optimized to achieve highest gain. Number of transistors were selected as x3 for this stage for both CE and CB transistors. Interstage matching was achieved with transmission lines and series capacitors. Inductive emitter degeneration was primarily used to achieve a peak gain around 77 GHz rather than

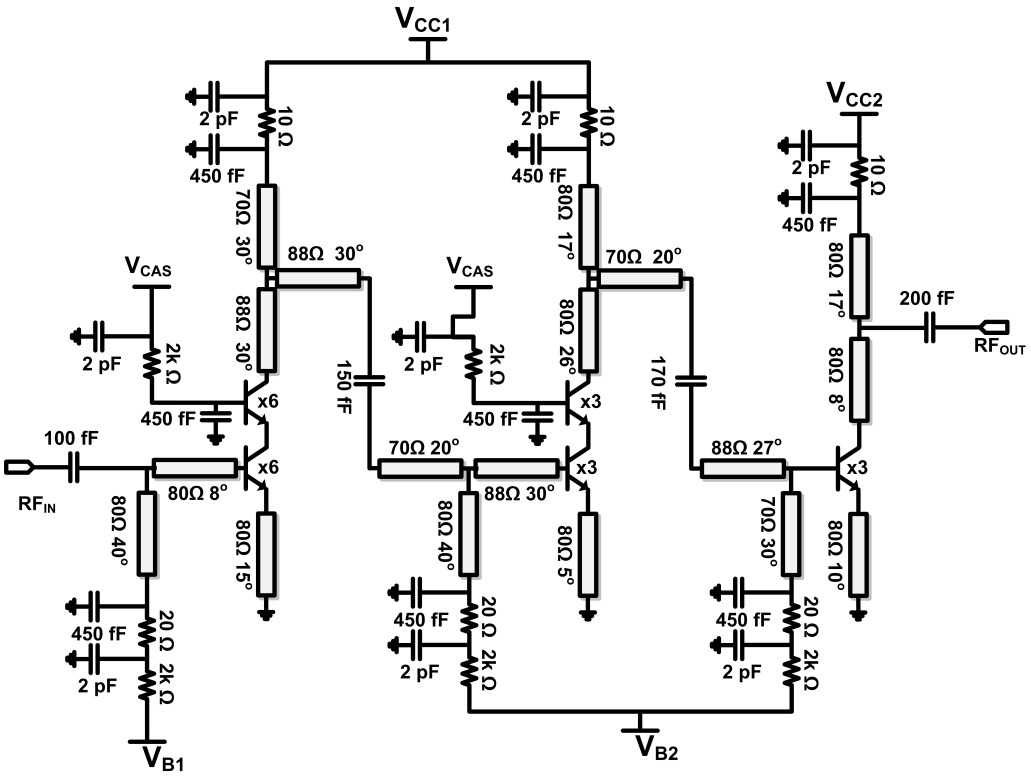


Figure 53: The detailed schematic of the low noise amplifier.

obtaining an impedance with a real part of 50Ω. The third stage was designed as CE topology as mentioned due to easing the output matching and obtaining an acceptable gain. Inductive emitter degradation was again utilized for obtaining a peak gain. Interstage matching was realized with transmission lines and a series capacitor.

Bias circuits are important for amplifier designs because they can change the performance drastically. Since the base terminal of CB transistors in cascode configuration are purely DC terminals, the bias voltage is applied through a high-valued resistor which provides RF-open and shunt capacitors which provide AC-open nodes. However, base and collector terminals of the CE transistors have RF-input and RF-output signals, the bias circuits should be designed by considering effects on RF signal. When input signal power increases, the collector current will increase which leads and increase in base current. If the same bias circuit is used at the base terminal of CE transistor, the increase in base current will cause a higher voltage-drop on the resistor. Hence actual voltage of the base terminal will be smaller. This will degrade the linearity performance. Also, utilizing a high-valued resistor in the bias circuit at the collector terminal can force the transistor to operate in saturation mode due to the same reason. Thus, transmission lines were used instead of resistors to provide RF-open nodes for base and collector terminals of CE transistors. Two different shunt capacitors were utilized to achieve AC grounding for the frequency of interest and lower. However, connecting these two capacitors directly would change the behavior of the individual capacitors, which would cause an unexpected behavior. Thus, small-valued resistors were used between two capacitors in the bias circuits to increase the isolation between them. Also, this technique increases the low frequency stability of the circuit and prevents oscillations. Due to the nature of RX-port of the designed EBD, LNA must be designed in a differential configuration. Therefore, two of the designed LNAs were connected to obtain differential configuration.

All the transmission lines were implemented by using the TM2 layer of the technology. Metal1 layer was used as grounding layer to implement microstrip configuration. The parasitic effects of RF pads were included to the input and output impedance matching network in the simulations. MIM capacitors from the technol-

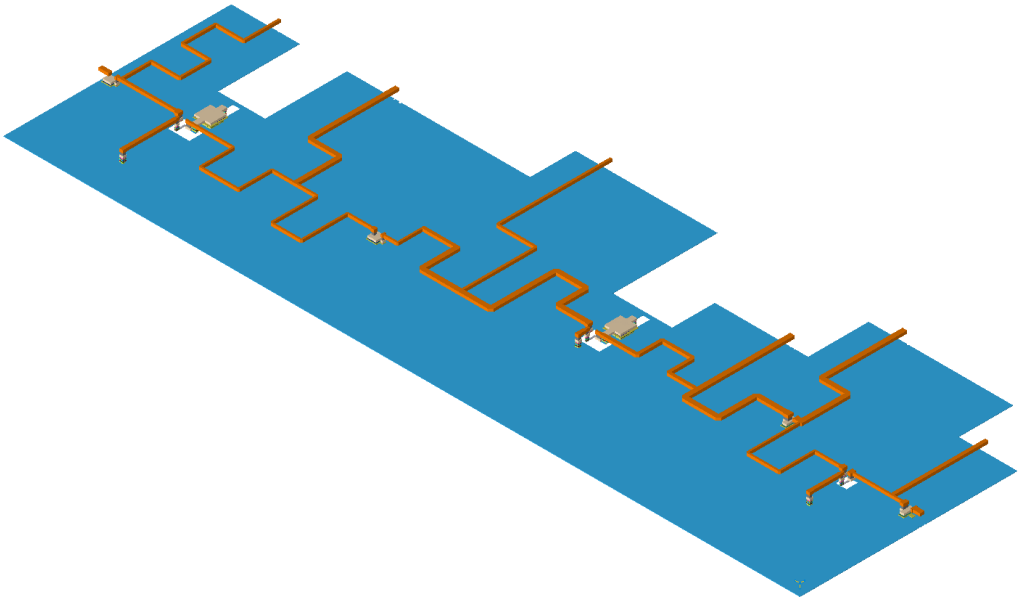


Figure 54: The 3D layout view of designed the low noise amplifier.

ogy were used for as bypassing the feed lines and blocking the DC signals on the RF signal path as mentioned. ADS Momentum software was used for performing electromagnetic simulations. The 3D layout view of the designed LNA is shown in Figure 54. This circuit was designed by Işık Berke Güngör, who is a member of SÜMER Research Group.

3.7.2 Simulation Results

The layout of the designed LNA is given in Figure 55. Figure 56, Figure 57, and Figure 58 shows the simulation results of the designed LNA. Input return loss is better than 11.7 dB and output return loss is better than 11.3 dB between 76–81 GHz. The minimum and maximum gain are 30.5 dB and 29.25 dB respectively. NF is simulated as less than 3.45 dB between 76–81 GHz. The simulated 1-dB compression point of the designed LNA is -31 dBm, which is shown in Figure 59. The comparison of the designed LNA with other reported LNAs realized in silicon technologies is given in Table.... the designed LNA achieves very high gain with the lowest NF performance.

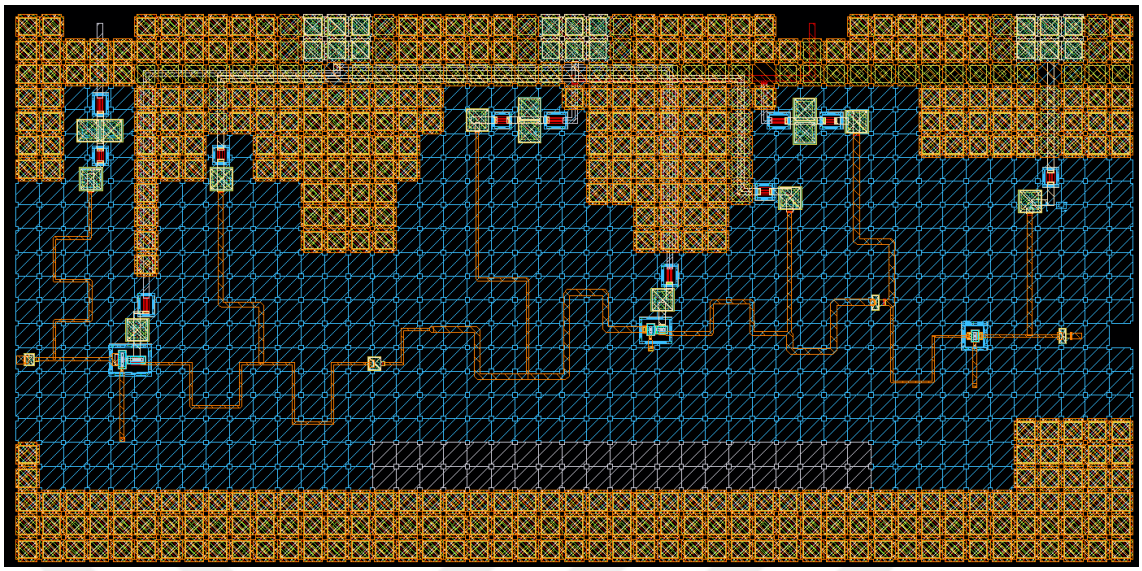


Figure 55: The layout of designed the low noise amplifier.

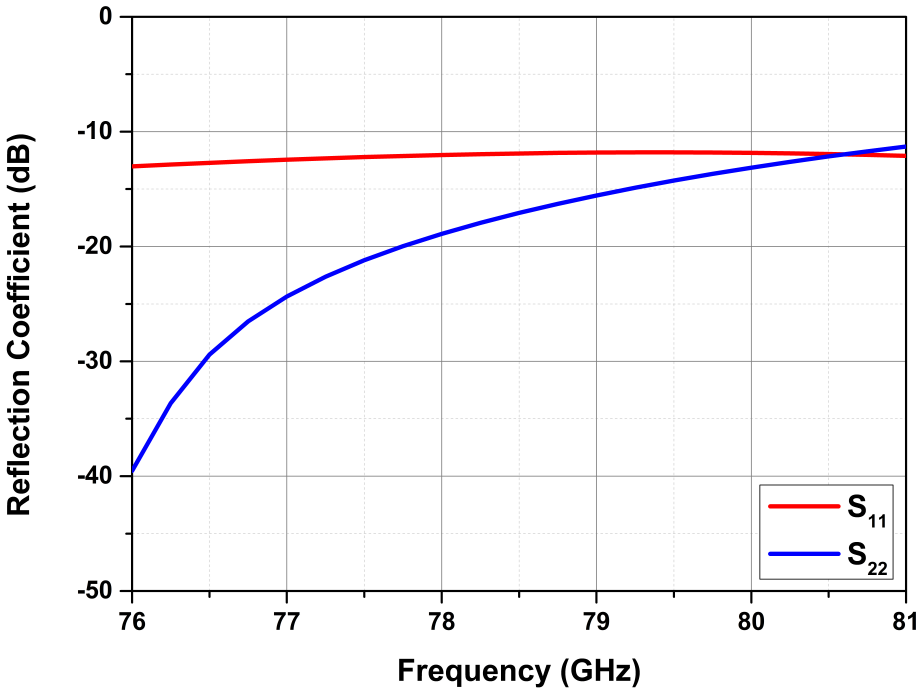


Figure 56: The simulated input and output return losses of the low noise amplifier.

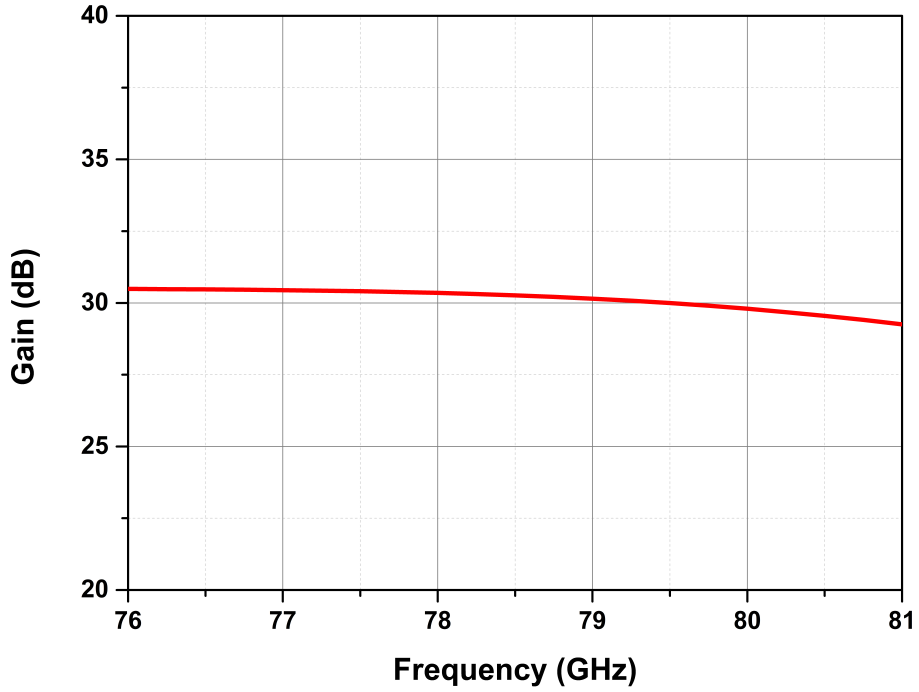


Figure 57: The simulated gain of the low noise amplifier.

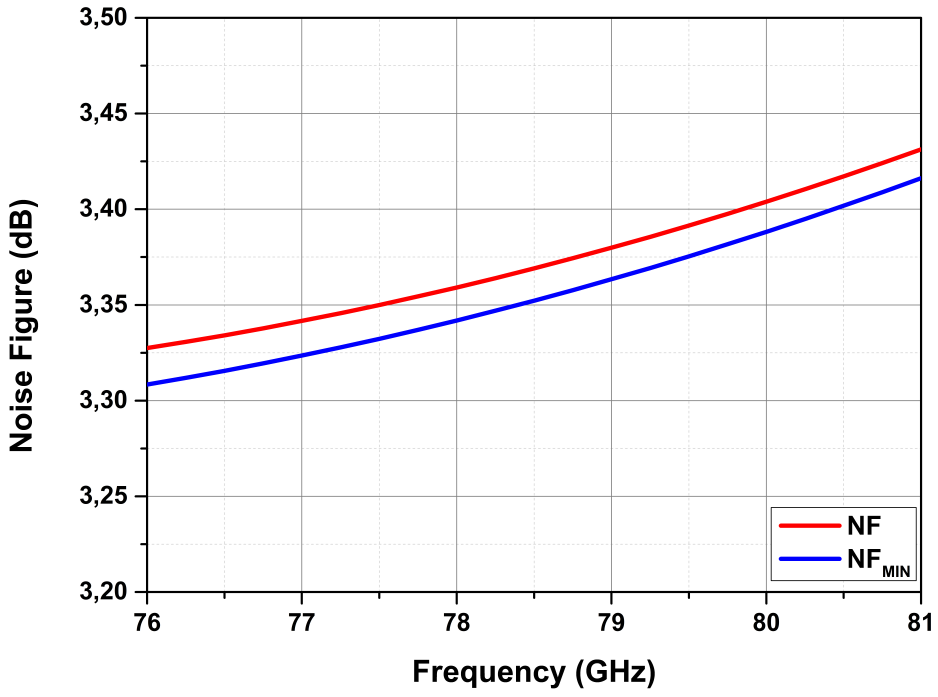


Figure 58: The simulated noise figure of the low noise amplifier.

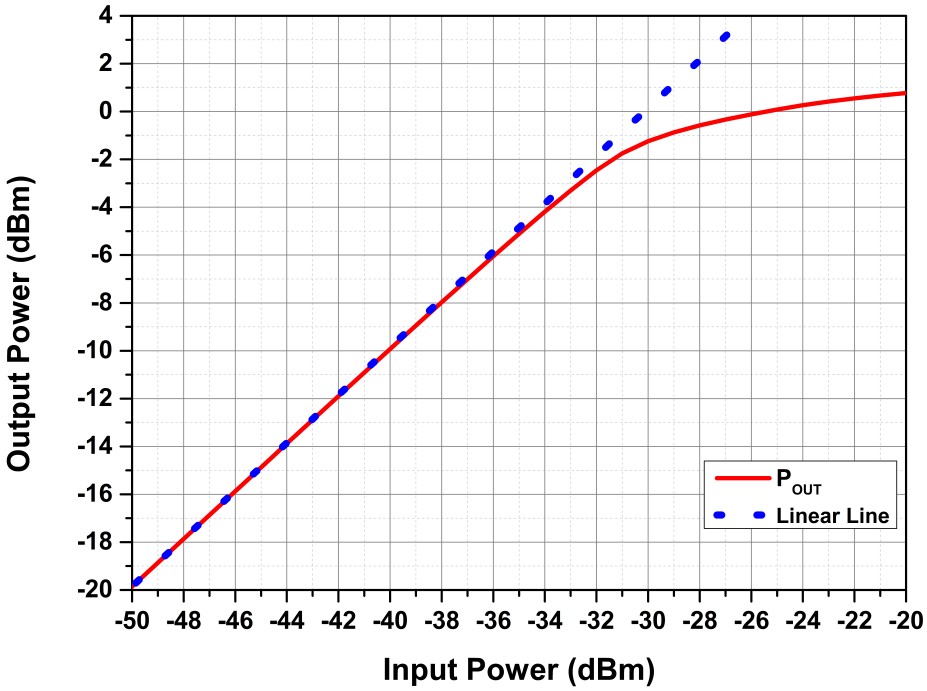


Figure 59: The simulated 1-dB compression point of the low noise amplifier.

Table 5: Summary of performance comparison of the designed 77 GHz LNA with previously reported 77 GHz LNAs implemented in silicon technologies.

Reference	[43]	[44]	[45]	[46]	[47]	**This Work***
Technology	90 nm CMOS	65 nm CMOS	65 nm CMOS	0.18 μm SiGe BiCMOS	0.13 μm SiGe BiCMOS	**0.13 μm SiGe BiCMOS**
Frequency (GHz)	77	77	77	77	77	**77**
Gain (dB)	11.2	18	11	14.5	10.7	**30.44**
S_{11} (dB)	-10	-10	-10	-11	-12	**-11.7**
S_{22} (dB)	N/A	-10	-5	-17	N/A	**-11.3**
NF (dB)	4.8	5.9	7.8	6.9	7.2	**3.34**
IP1dB (dBm)	-7.4	-22	-22	-11.4	-18	**-31**
P_{DC} (mW)	10	20	25.8	37	9	**14**
Area (mm^2)	0.55=	0.23	0.3	0.41	0.3	**1**

*Simulation Results
=Area without pads

3.8 Power Amplifier

3.8.1 Circuit Design and Implementation

PA can be considered the baseline of the transmitter chain. The signal will be amplified here to reach as far as it could possibly manage to detect objects. This designed PA was connected to TX-port of EBD. The PA should achieve high output power levels as possible since the output power and the maximum range that the system can detect are directly related to each other as proven with the theoretical calculations before. Therefore, power handling capability of the designed PA should be enough to ensure that PA is not compressing.

The cascode topology provides sufficiently enough power handling capability, high reverse isolation and higher gain than CE topology. However, due to the nature of EBD, the impedance of TX-port is 25Ω. Hence, the output of the designed PA must be matched to 25Ω. A huge matching network is required to match the output port of the PA to 25Ω with cascode topology. Because, cascode topology has high output resistance when compared with 25Ω. This matching network would increase the loss; thus, the output power would decrease. On the other hand, although a single stage CE topology has lower power handling capability than single stage cascode topology, the performance changes with cascaded stages. It was found out that cascaded CE stages can provide comparable power handling capability with its counterpart, cascaded cascode stages. Further, achieving high gain is not a priority for this PA design. So, three stage CE topology was chosen for this thesis work in PA design to meet the requirements.

Type of biasing is an important design criterion in PA designs. The performance of PAs depend on type of biasing that applied. Although there are different types of biasing in the literature which can provide comparable output powers with higher efficiency, it is not possible to utilize them in this system. Continuous wave systems with any type of modulation applied, or even without modulation applied require high linearity. Therefore, PAs in such systems should be designed with either Class-A or Class-AB. In order to meet the high output power specifications, Class-A type of biasing was chosen in this thesis work.

First stage was designed as a driver stage for generating enough current gain. It can not be possible to drive the next stages directly without a driver stage.

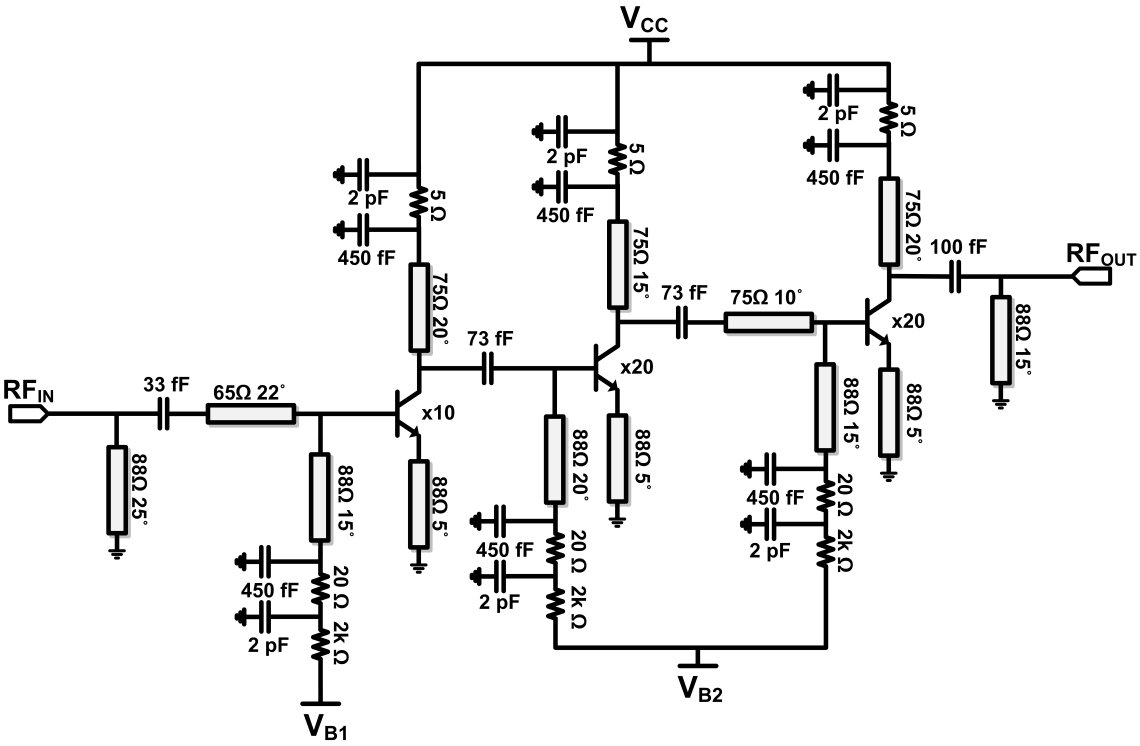


Figure 60: The detailed schematic of the designed PA.

Additionally, since driver stage provides enough current gain, it also generates some power gain. Number of transistors were selected as x10 when matching was taken into account. Second stage was the main amplifier core, and the goal was to achieve maximum power gain possible. Although number of transistors were selected lower at the beginning of the design, it was found out that x20 was the optimum value for the number of transistors to achieve the required P_{sat} value. The third stage was designed with a similar approach as second stage. Since the output impedance of the PA is fixed to 25Ω due to the EBD, the load-pull analysis was not utilized. Since the number of transistors is high, shunt stubs were implemented to achieve a proper impedance matching. The 33 fF capacitor at the first stage was designed as a MOM capacitor rather than MIM capacitor. The detailed schematic of the designed PA is given in Figure 60.

Bias circuits are important for PA designs as well as in LNA designs. Components that are used in bias circuits can affect the stability of the design directly. Resistors were implemented in between of two bypass capacitors for the similar purpose in the LNA design. However, more bypass capacitors were utilized in PA design because PA is more sensitive to stability issues.

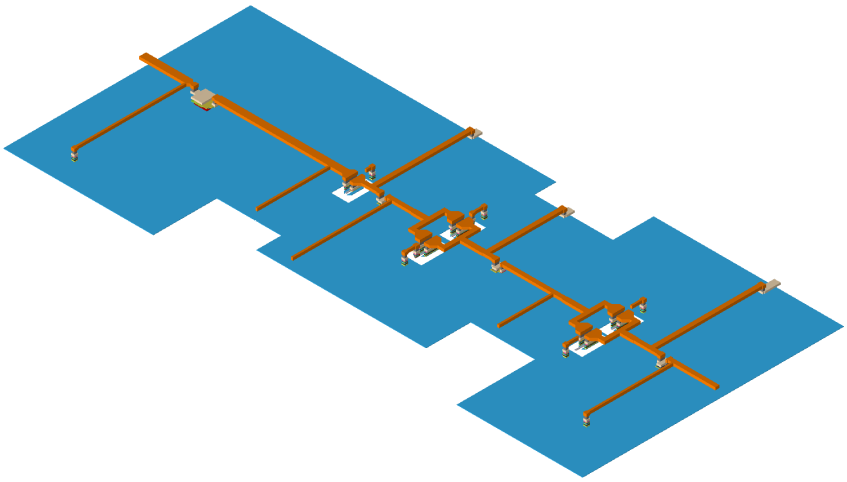


Figure 61: The 3D layout view of the designed PA.

All transmission lines were realized with utilizing TM2 layer of the technology. Metal1 layer was used as ground to realize microstrip transmission line configuration. The effects of parasitic capacitances due to RF pads were included to the input and output impedance matching networks. The MOM capacitor was implemented by using TM2–M3 layers of the technology. Since each of the stages conduct high current, the layout of the components must be arranged by considering maximum current density that each component could handle. Emitter degenerations have more vias than it should be, in order to prevent any breakdown. Many parallel on-chip resistors were used for the same reason. Although higher output power could be achieved with higher current values, it was not preferred due to the physical problems that can occur. Electromagnetic simulations were carried out with ADS Momentum software. The 3D layout view of the designed PA is shown in Figure 61. This circuit was designed by Işık Berke Güngör, who is a member of SÜMER Research Group.

3.8.2 Simulation Results

The layout of the designed PA is presented in Figure 62. The simulated input and output return losses of the designed PA is given in Figure 63. The figure shows that the PA has an input return loss better than 16.9 dB and an output return loss better than 11 dB between 76–81 GHz. The simulated gain of the designed PA is shown in Figure 64. The maximum and minimum gains are simulated as 17.7 dB and 16 dB respectively. Figure 65 presents the simulated 1dB compression

point of the designed PA. The compression occurs at an input power of -6.5 dBm with a corresponding output power of 10.9 dBm. The power added efficiency of the designed PA is given in Figure 66, and it was simulated as 8.8% for -2 dBm input power. Table 6 shows the comparison of the designed PA and similar PAs from literature. The designed PA achieves high gain with a high linearity performance with a low power consumption.

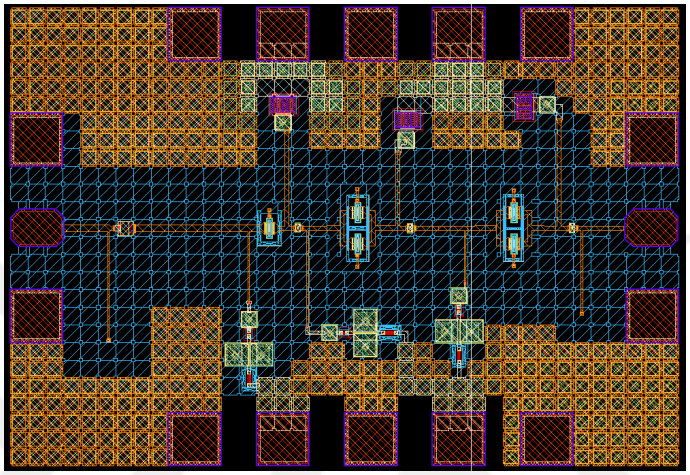


Figure 62: The layout of the designed PA.

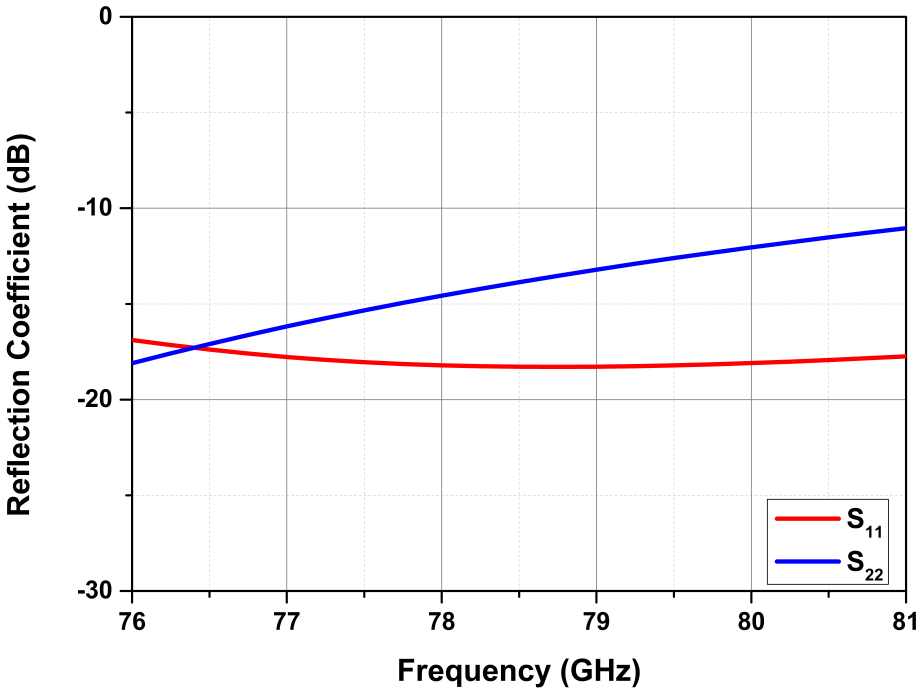


Figure 63: The simulated input and output return losses of the designed PA.

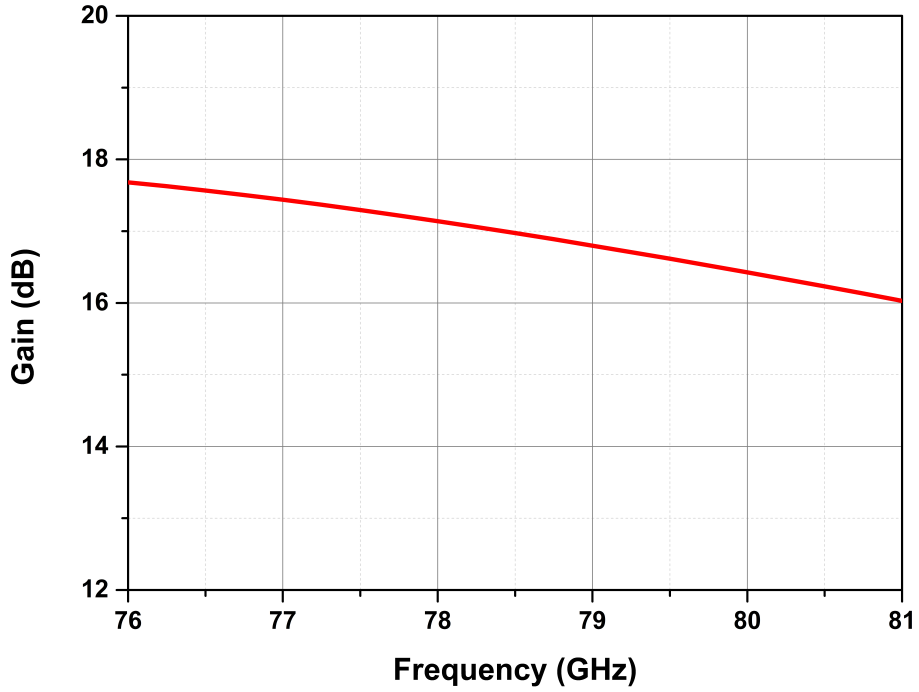


Figure 64: The simulated gain of the designed PA.

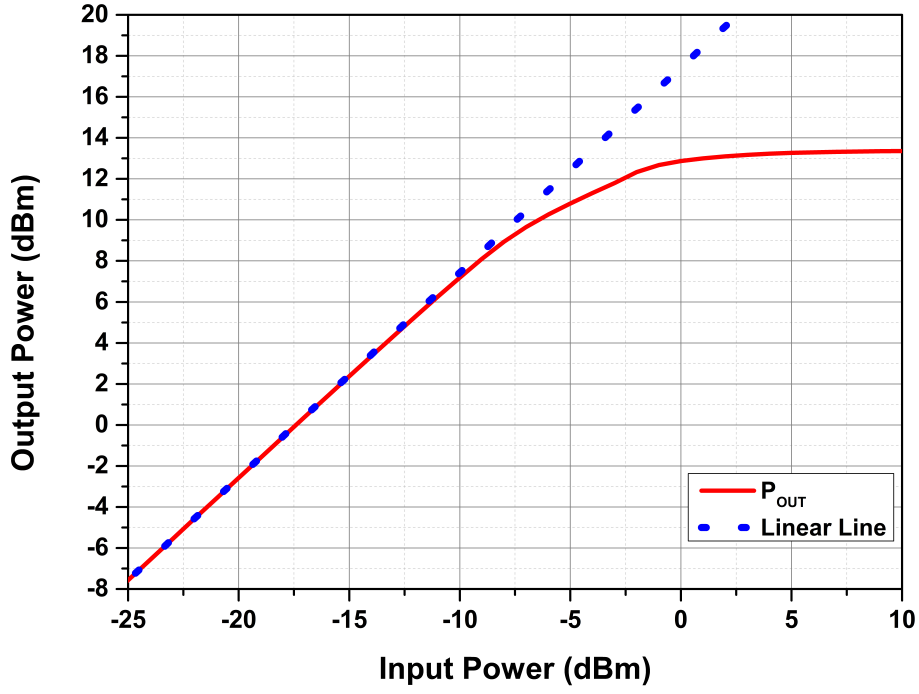


Figure 65: The simulated 1-dB compression point of the designed PA.

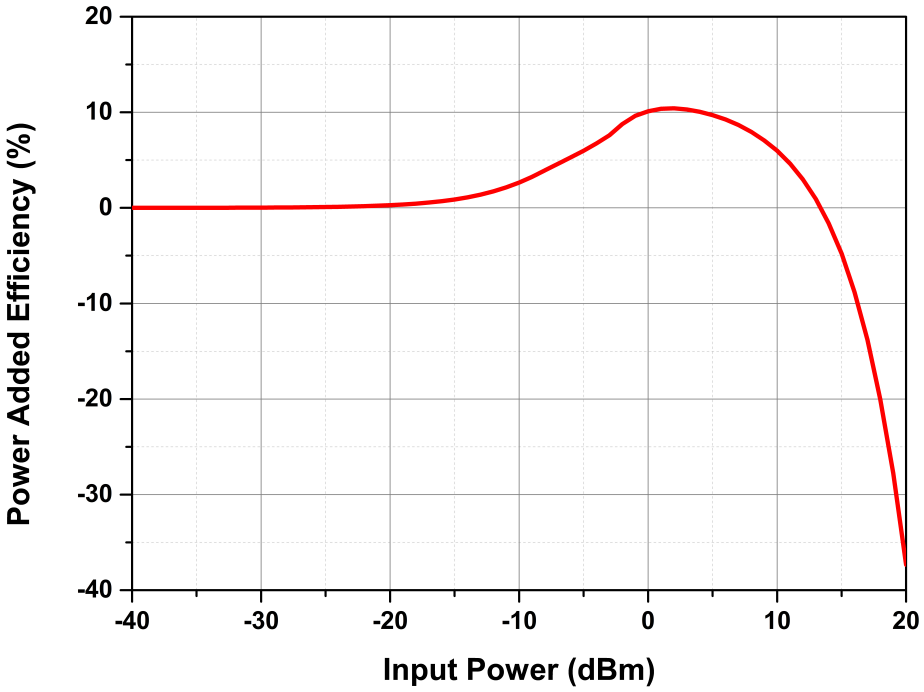


Figure 66: The simulated power added efficiency of the designed PA.

Table 6: Summary of performance comparison of the designed 77 GHz PA with previously reported 77 GHz PAs implemented in silicon technologies.

Reference	[48]	[49]	[50]	[51]	[52]	**This Work***
Technology	90 nm CMOS	90 nm CMOS	0.12 μm SiGe BiCMOS	0.12 μm SiGe BiCMOS	0.13 μm SiGe BiCMOS	**0.13 μm SiGe BiCMOS**
Frequency (GHz)	77	77	77	77	77	**77**
P_{sat} (dBm)	13.2	12	9.5	16	14.5	**13.5**
OP_{1dB} (dBm)	11.2	9.5	14.7	14.5	9	**11**
Gain (dB)	10.4	21	6.1	17	25	**17.4**
P_{DC} (mW)	140.4	90	325	297	250	**189**
Area (mm^2)	0.105=	0.67=	1.575	0.6	0.242	**0.492**

*Simulation Results
=Area without pads

3.9 Mixer Design

3.9.1 Circuit Design and Implementation

Mixer is one of the important sub-blocks in RF domain which enables to up-convert or down-convert the frequency of a signal. These conversions are realized with obtaining the desired harmonic signal by multiplying two different signals. Active mixers can be separated into three different configurations which are single-ended, single-balanced and double-balanced. All three configurations have benefits or drawbacks due to their natures. Single-ended mixer is the simplest configuration to design. Also, this configuration can achieve very low power consumptions. Further, single-ended mixers have the best noise figure performance among all three configurations. However, this topology lacks from isolation between RF and LO ports. This is not feasible for RADAR applications because frequencies of RF and LO signals are very close. On the other hand, single-balanced mixer provides an RF performance in between two other configurations. But it is not feasible for the scope of this thesis work because RF and LO requires two baluns which degrade the overall performance of the mixer. Also, RF signal contains DC component, which should be eliminated with extra effort, since the input is single ended. Further, high LO power is required for this topology to achieve good conversion gain and lower noise figure. But again, LO signal power is not high enough to meet the prerequisite for single-balanced mixer topology in the designed system. Double-balanced mixer configuration is the best candidate for the system. Although the mixing is quite similar to single-ended mixer, mixing can be achieved without any extra components since RF signal has no DC component. Since output of the LNA is differential in the system, there is no requirement for the extra balun to connect the output of the LNA to the RF port of the mixer. Also, double-balanced configuration can suppress the leakage signal between the ports of the mixer, especially the leakage signal between LO and RF ports. This attribute is critical because high leakage signal in any RADAR system can degrade the overall performance. The detailed schematic of the designed mixer is given in Figure 67. Double-balanced mixer topology was selected due to the advantages of the topology. The mixer in this system designed as a down-conversion mixer because of the system requirements.

RF input transitioned as a voltage signal to the CE stage of the down-conversion

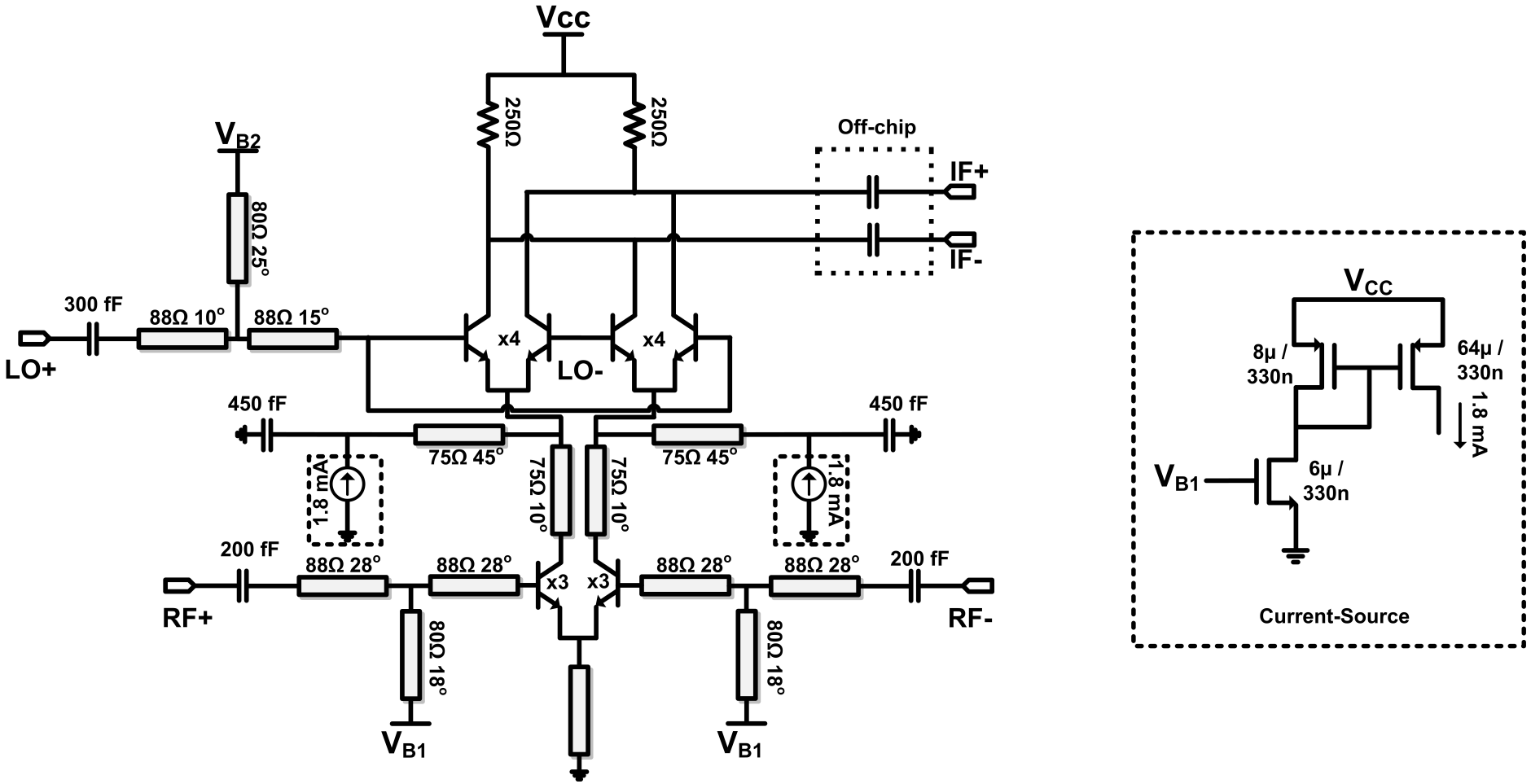


Figure 67: The detailed schematic of the designed double-balanced mixer.

mixer. Differential CE stage converts this RF voltage signal into a current signal. Then, this signal is multiplied with the LO signal by the differential switching stage. Thus, the conversion gain of the mixer depends on the parasitic effects and the transconductance of the transistors in the CE stage. So, the bias point for these transistors were selected where their ft is maximum. The number of transistors for CE stage was found with considering the impedance matching to the output of the designed LNA. In order to increase conversion gain, emitter degeneration was not utilized. The tail source was implemented as a transmission line. Although linearity is important for RADAR systems, conversion gain was preferred due to increase the signal at the IF.

The transistors in the LO switching stage were biased with 0.75 V, which corresponds to Class-B bias voltage for the technology. Since these transistors perform switching operation, biasing these at Class-B point would increase the switching performance. Also, current bleeding technique was applied in order to increase the conversion gain, linearity and noise figure performances. The current of the transconductance stage does not flow through the load resistor thanks to this technique. Hence, the load resistor can be increased to improve conversion gain [53]. Conventional PMOS current mirror circuit was utilized to implement the current sources. Since the bias voltage is set to 3.3 V, high-voltage PMOS transistors of the technology were used in implementing the current sources to eliminate the voltage breakdown issue. Number of transistors in the LO switching stage was found out to be x4 when considering the incoming LO signal power level and LO-port impedance matching. Series peaking transmission line was utilized to eliminate the mismatches between LO and RF stage instead of setting the real part of the LO impedance.

IF port of the designed double-balanced down-conversion mixer is operating less than 200 MHz. Therefore, resistors were implemented instead of inductors for supplying voltage to the mixer. If inductors were utilized to provide high impedance, the value of each inductor would be in tens of nH range at this IF frequency. It is not feasible to achieve an on-chip inductor at these values. However, if it could be achieved, that inductors would occupy larger area than the design. Also, using high-valued resistors degrades the 1-dB compression point of the designed mixer significantly. Thus, 250Ω resistors were placed as a load to create RF-open nodes and

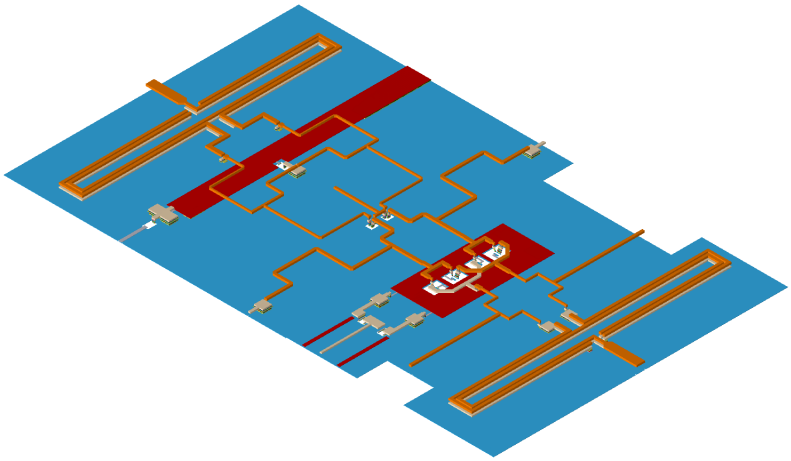


Figure 68: The 3D layout view of the designed double-balanced mixer.

also increasing the conversion gain. Also, bypass capacitors were placed to remove the effects of leakage signals at lower frequencies. A Marchand balun was designed to feed LO signal into the switching stage. Marchand balun can be designed by utilizing two quarter-wave coupled lines. All the transmission lines were realized as microstrip lines between TM2 and Metal1 layer of the technology. Full-chip electromagnetic simulations were performed by ADS Momentum. AC-grounding and DC-blocking were performed by using MIM capacitors. The 3D view of the designed double-balanced down-conversion mixer is given in Figure 68.

3.9.2 Simulation Results

The layout of the designed down-conversion mixer is given in Figure 69. The simulation result of the down-conversion gain of the designed mixer is given in Figure 70. The figure shows that the down-conversion gain is between 4.5–5.75 dB between 76–81 GHz. The simulated isolation values between three ports are presented in Figure 71. The isolation between LO-port to RF-port is simulated as 50 dB whereas LO-port to IF-port isolation is better than 96 dB between 76–81 GHz. RF-port to IF-port isolation is simulated better than other two isolation values, which is greater than 104 dB for the same frequency interval. Figure 72 states the impedance matching values for RF-port and LO-port. The return loss for the RF-port impedance matching is better than 14 dB whereas the return loss for LO-port is simulated less than 10.3 dB between 76–81 GHz. Table 7 shows the comparison of the designed mixer with similar works from the literature.

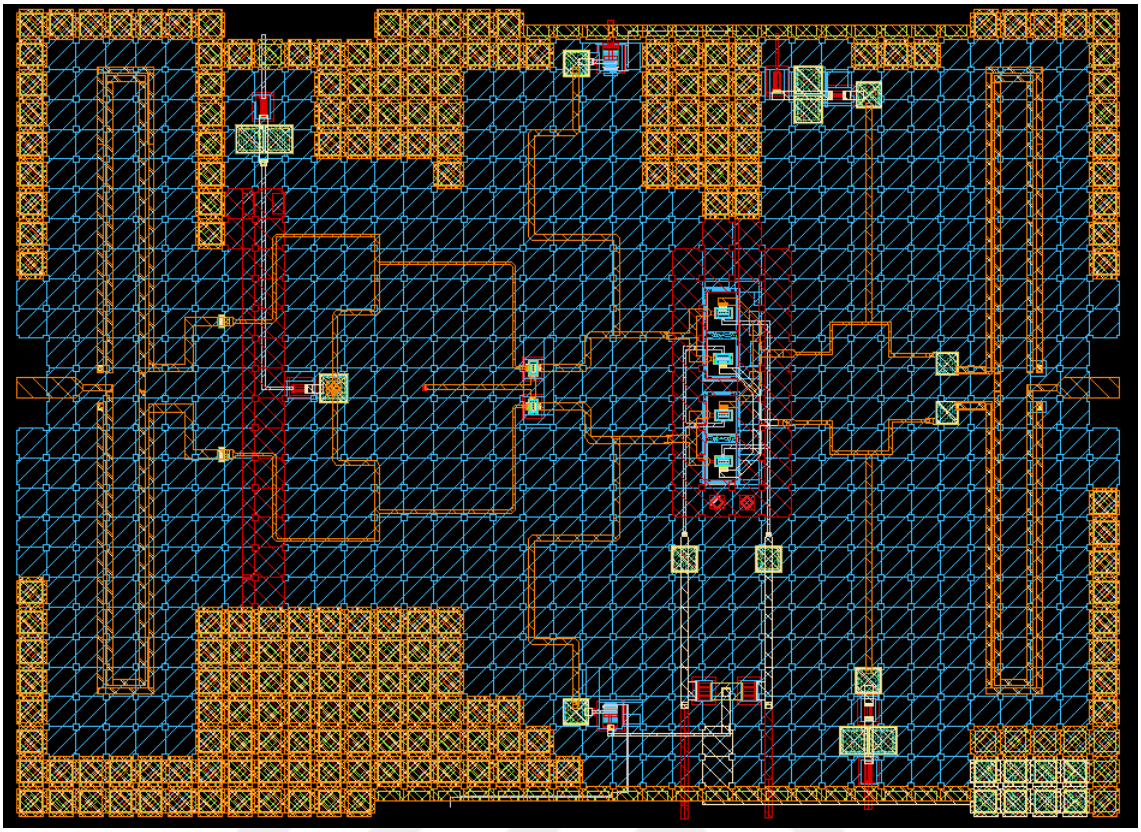


Figure 69: The layout of the designed double-balanced mixer.

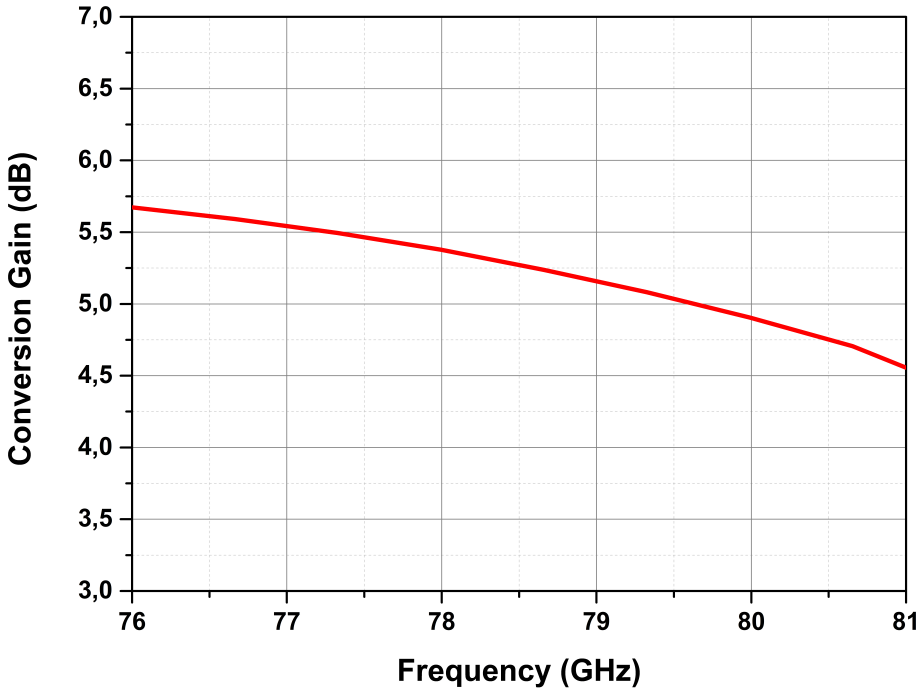


Figure 70: The simulated conversion gain of the designed double-balanced mixer.

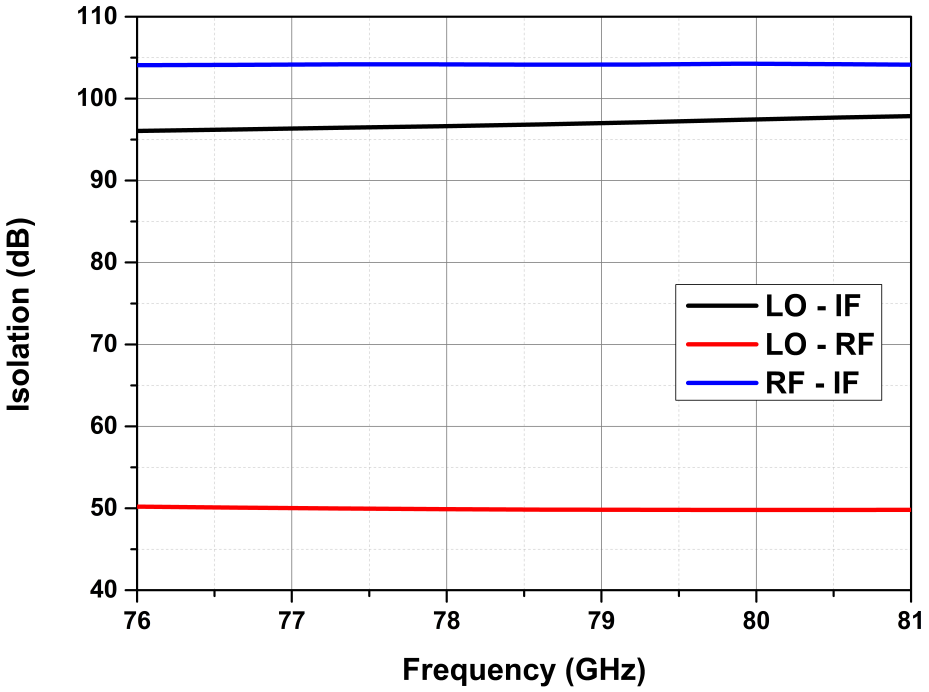


Figure 71: The simulated isolation values between the ports of the designed double-balanced mixer.

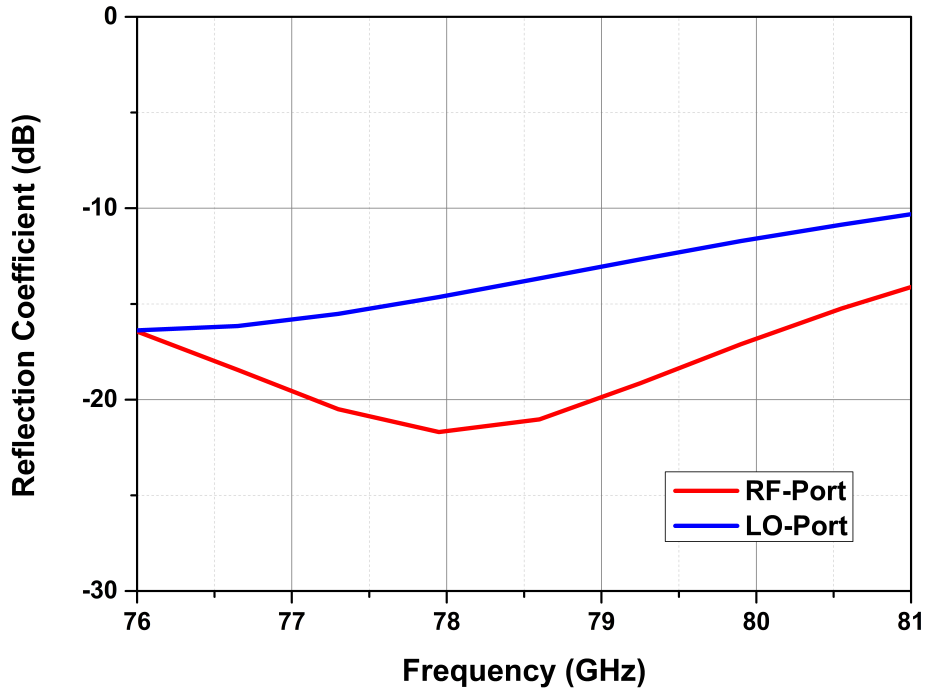


Figure 72: The simulated return loss values of the ports of the designed double-balanced mixer.

Table 7: Summary of performance comparison of the designed 77 GHz mixer with the similar works in silicon technologies.

Reference	**[54]**	**[55]**	**[56]**	**[57]**	**This Work***
Frequency (GHz)	77	77	77	77	**77**
Technology	65 nm CMOS	SiGe	0.13 um SiGe BiCMOS	SiGe	**0.13 um SiGe BiCMOS**
Topology	Single-Balanced	Micrometer with LO Multiplier	Single-Balanced	Double-Balanced	**Double-Balanced**
Conversion Gain (dB)	6.8	20.5	20	20	**5.5**
NF (dB)	21	16.5	12.8	21**	**8.5**
RF-IF ISO (dB)	N/A	N/A	N/A	N/A	**>50**
PDC (mW)	3	0.66	0.18**	72.6	**34.65**
Area (mm2)	0.46	1.16	1.76**	1.16	**0.38=**

*Simulation Results
**Estimated from Figures
=Area without pads

3.10 Results and Discussion about the Designed System

The system was simulated by using MATLAB with a special set of codes called "Automotive Adaptive Cruise Control Using FMCW Technology", which is given in APPENDIX. This code models an automotive adaptive cruise control system with FMCW technique. Also, this code is created for monostatic systems, thus it is applicable to our system. The RADAR model in the MATLAB code was adopted to mimic the designed system. Further, the original code has only one defined target, so another car model was added to the original code for two-target scenario. The same transmitted chirp signal was used for all the cases, which is shown in Figure

Table 8: The range and velocity values for each case in single-target detection.

	Range (m)	**Velocity (km/h)**
Case-1	80	60
Case-2	80	170
Case-3	180	170
Case-4	180	60

73. The layout of the overall system is given in Figure 74.

At first, system simulations were performed for single target detection. Four different cases were analyzed for single target detection with different velocity and distance conditions. Table 8 shows all four cases and their corresponding velocity and range values. Figure 75, Figure 76, Figure 77 and Figure 78 show the IF spectrum and 2D-FFT map results for Case-1 to Case-4 respectively. The results prove that the designed RADAR system can detect objects accurately regardless of their velocities and distances with respect to the antenna.

The modified MATLAB code was used to simulate two-target detection. Two different cases were simulated to test the design RADAR for two-target detection. The first case contains two different objects with different speeds and distances with respect to the antenna. One of the objects were located at 150m away from the antenna with 100 km/h speed towards the antenna. Besides, the other object was located 100m away from the antenna with 60 km/h speed away from the antenna. On the other hand the second case focuses on testing the range resolution capability of the designed RADAR; thus, the objects have different speeds were simulated with a distance of 15 cm between them. Figure 79 shows that the randomly selected two objects were detected successfully in IF spectrum and 2D-FFT map. Figure 80 shows that range resolution of 15 cm were achievable when the objects are located from mid-range with respect to the antenna. Table 9 shows the performance comparison with the similar works in the literature and products available in the market.

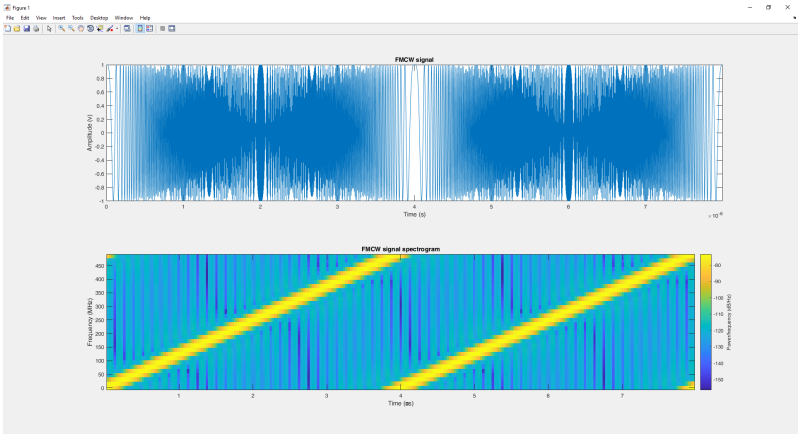


Figure 73: The transmitted chirp frame with time and frequency equivalent forms.

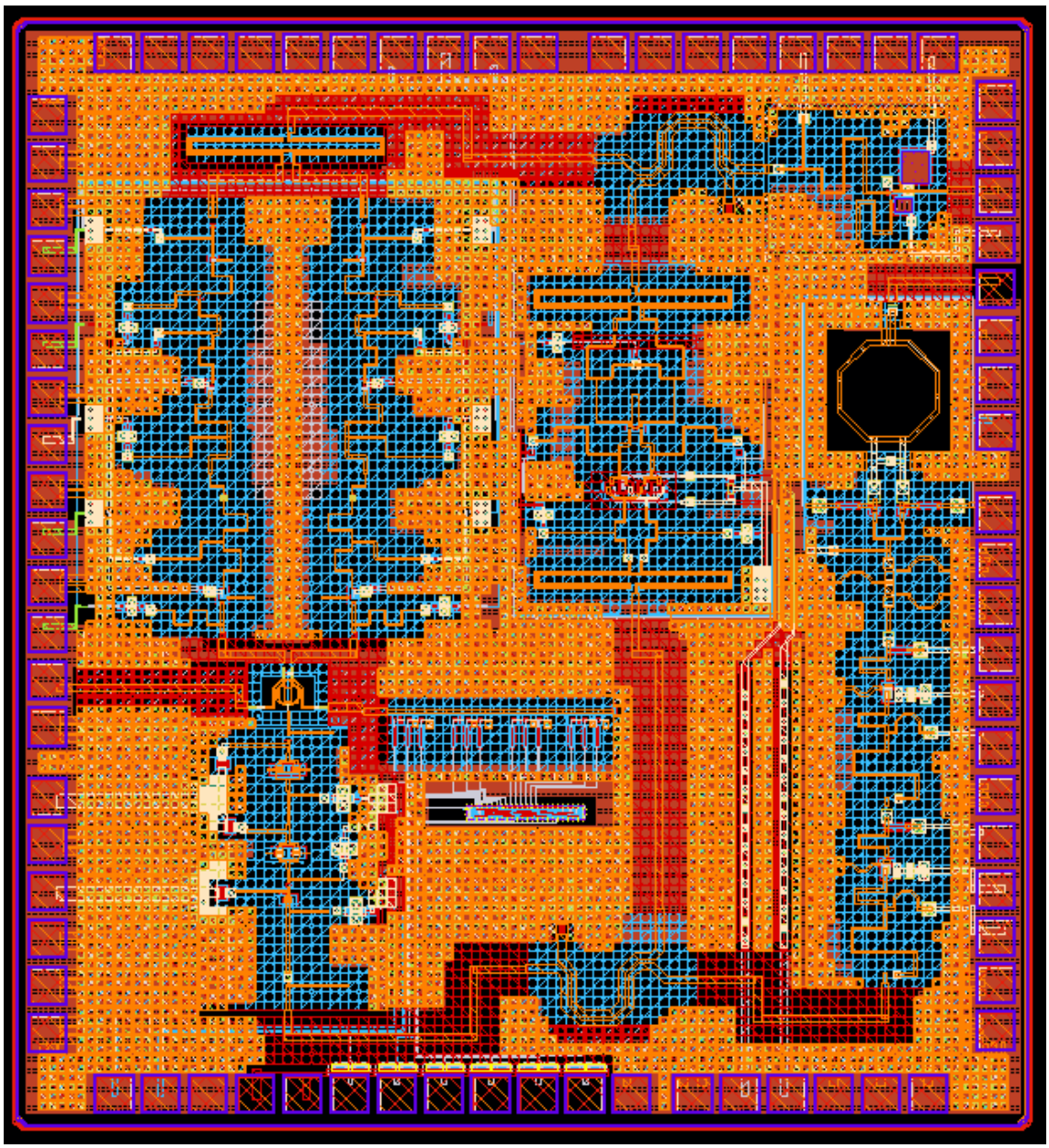
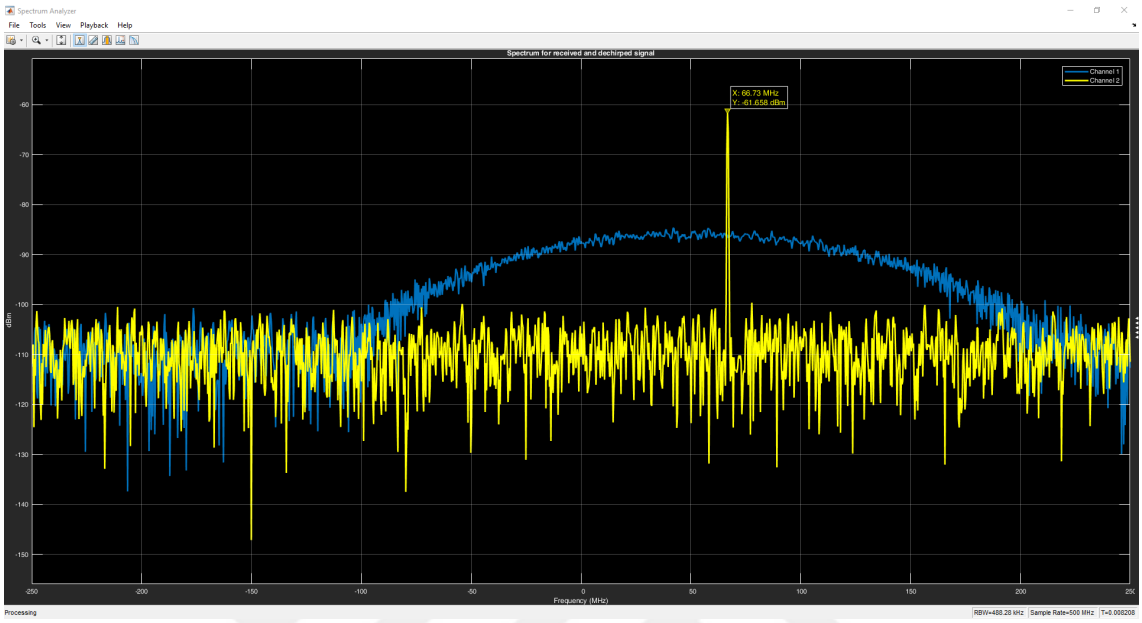
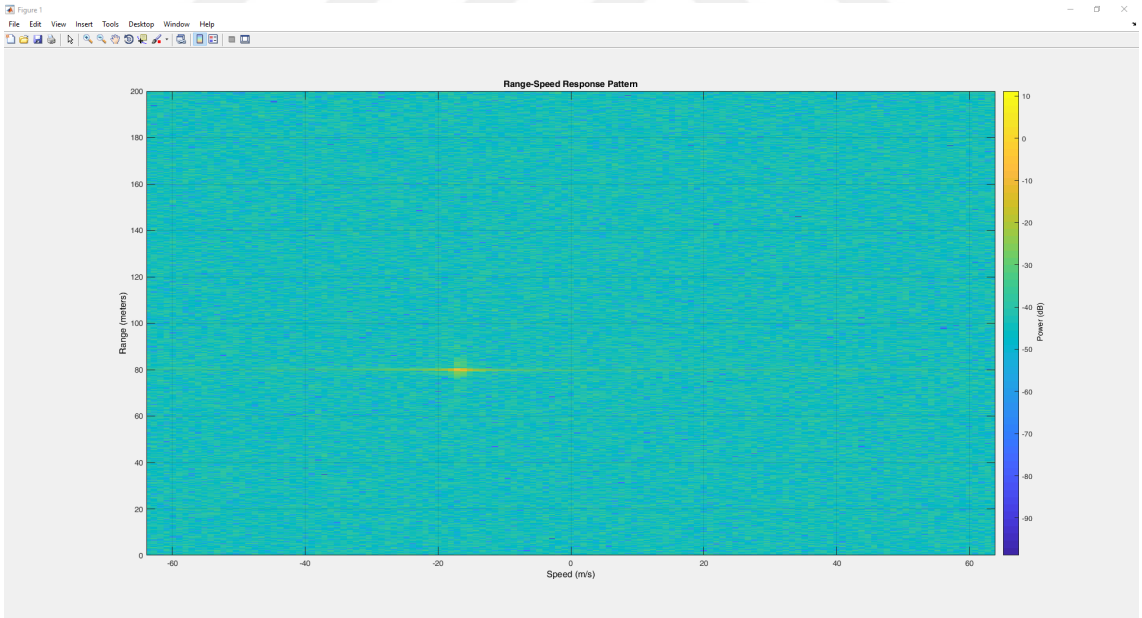


Figure 74: The complete layout of the designed system.

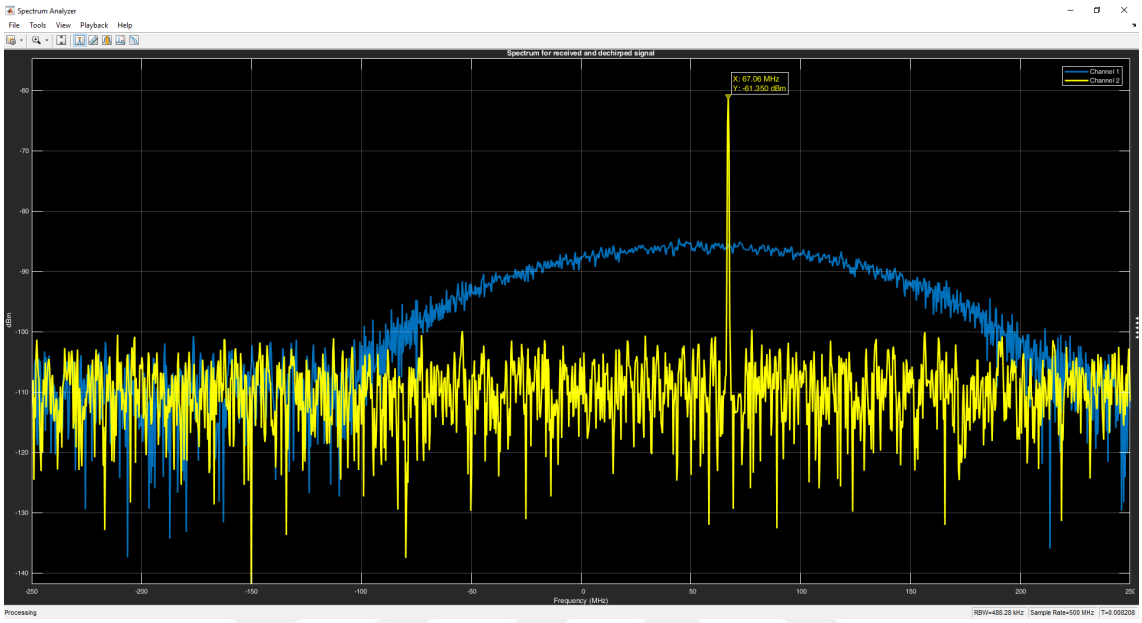


(a)

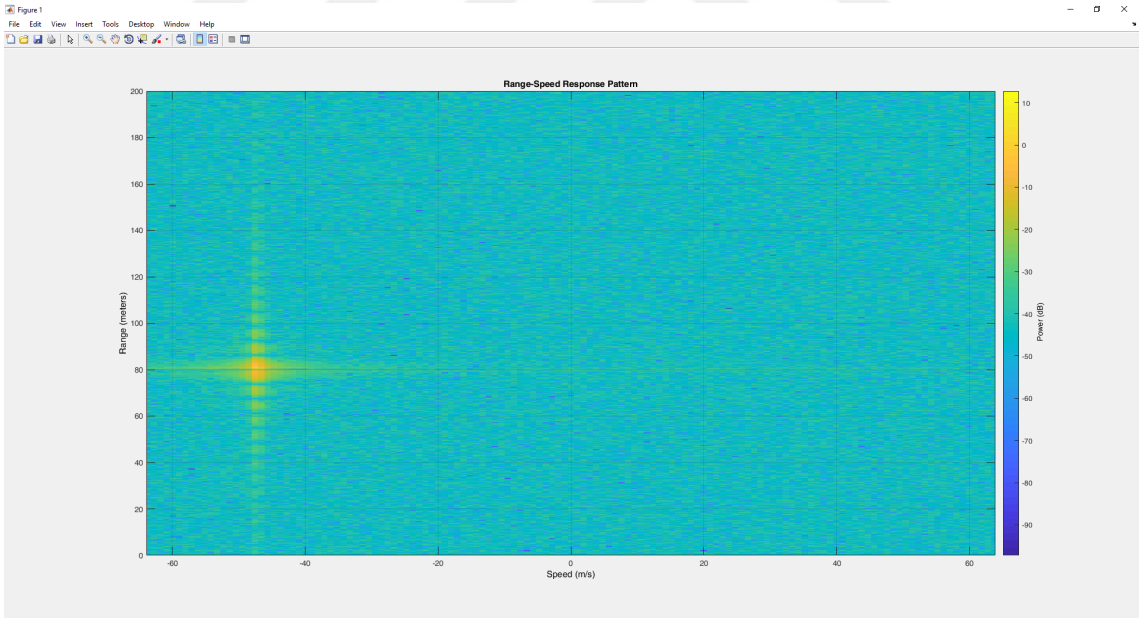


(b)

Figure 75: The simulated (a) IF spectrum and (b) 2D-FFT map for Case-1.

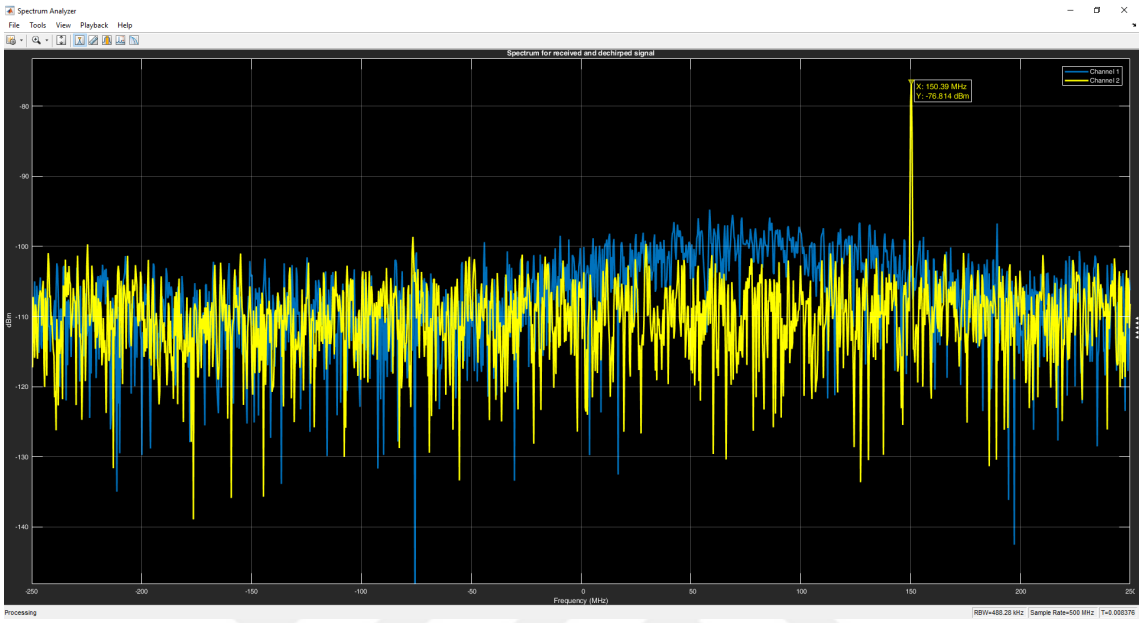


(a)

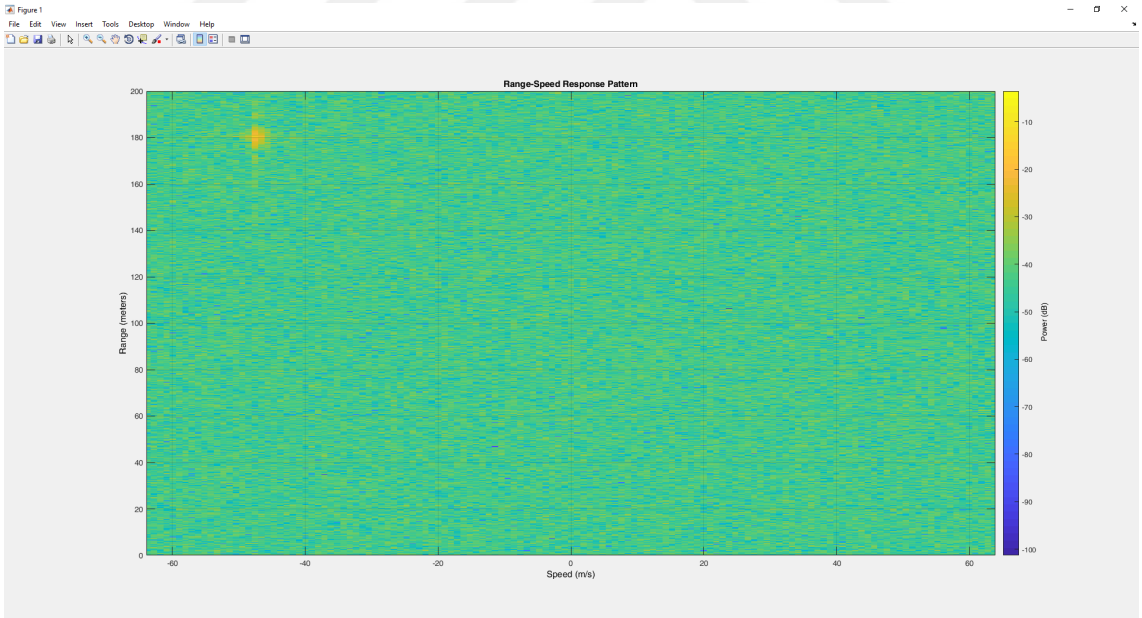


(b)

Figure 76: The simulated (a) IF spectrum and (b) 2D-FFT map for Case-2.

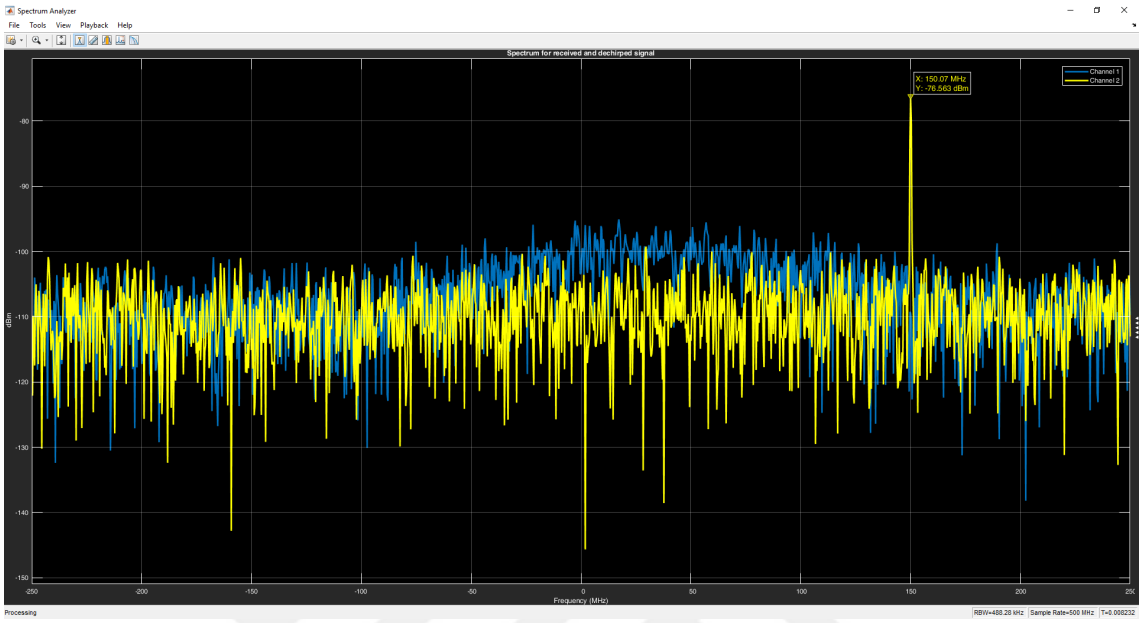


(a)

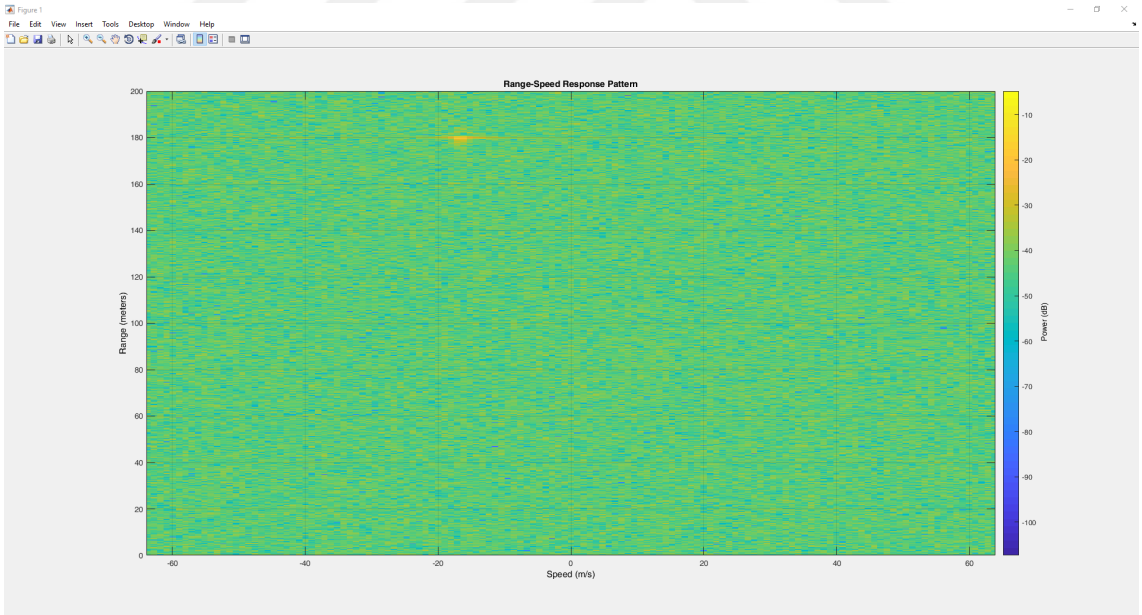


(b)

Figure 77: The simulated (a) IF spectrum and (b) 2D-FFT map for Case-3.

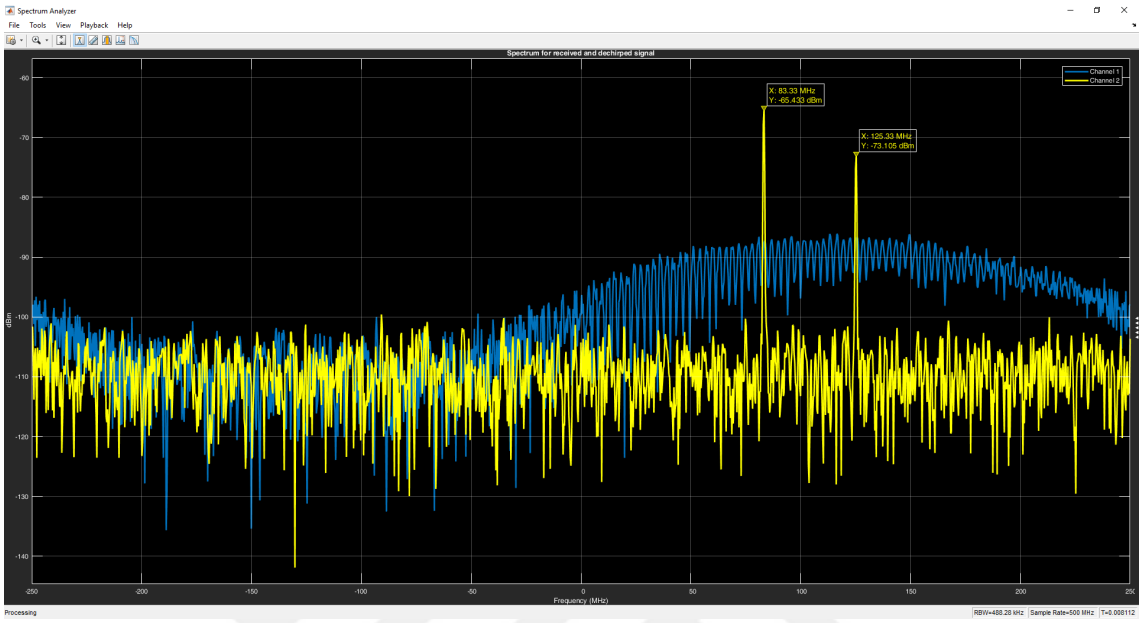


(a)

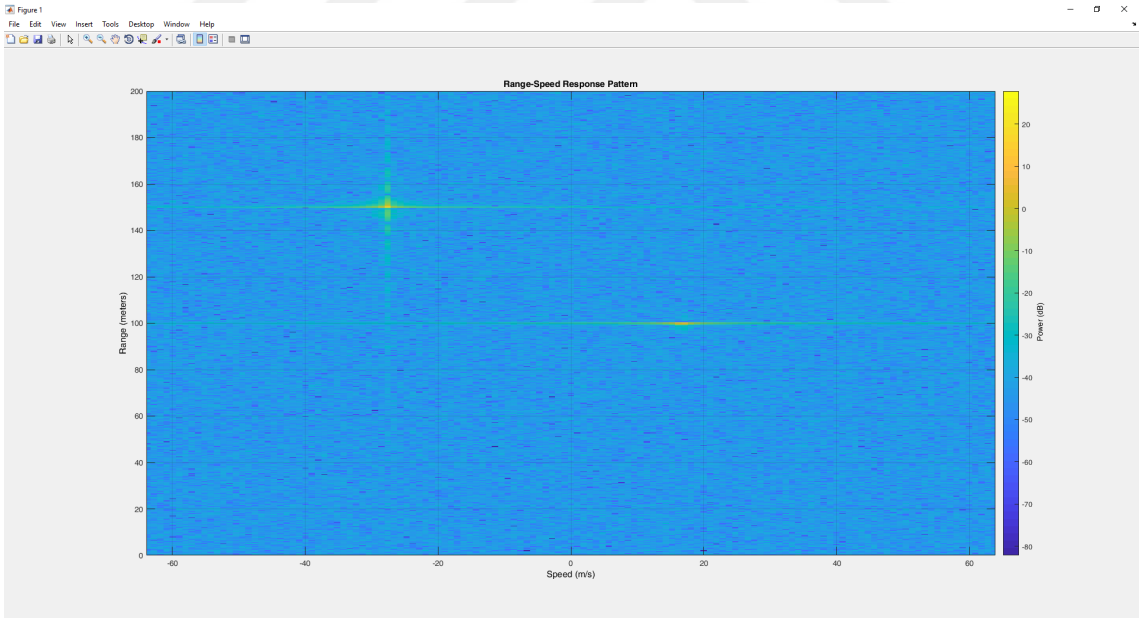


(b)

Figure 78: The simulated (a) IF spectrum and (b) 2D-FFT map for Case-4.

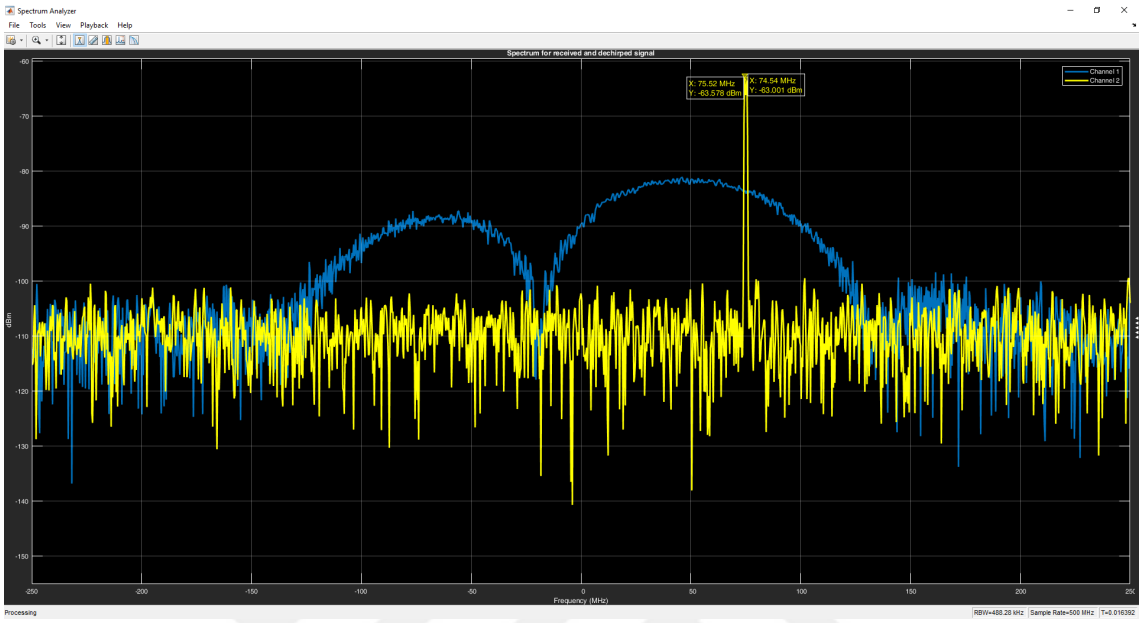


(a)

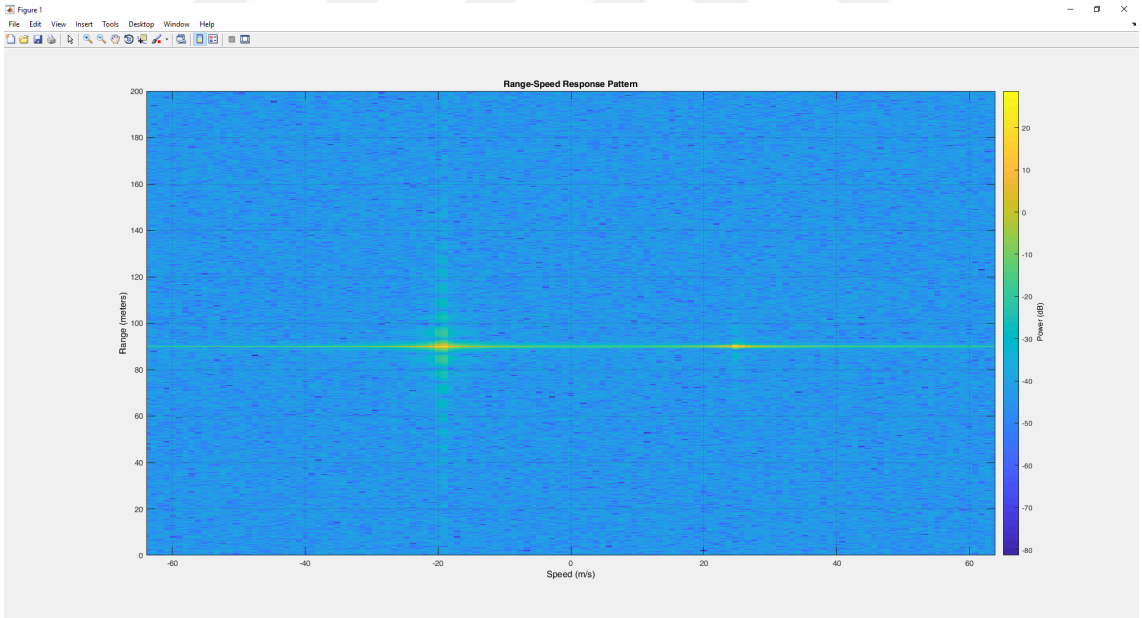


(b)

Figure 79: The simulated (a) IF spectrum and (b) 2D-FFT map for randomly selected two targets.



(a)



(b)

Figure 80: The simulated (a) IF spectrum and (b) 2D-FFT map for two targets with 15 cm between them.

Table 9: Summary of comparison of the designed system with similar works reported in the literature and available products available in the market.

Reference	[19]	[58]	[59]	[60]	[61]	[62]	[63]	[64]	**This Work***
Frequency (GHz)	77	77	77	77	79	77	77	79	**77**
Technology	45 nm RFCMOS	RFCMOS	65 nm CMOS	90 nm CMOS	90 nm CMOS	SiGe Bipolar	SiGe BiCMOS	0.18 SiGe BiCMOS	**0.13 SiGe BiCMOS**
TX Out. Pow. (dBm)	12.5	12	6.4	-2.8	-17	6.2	17	10.5	**8.5**
RX NF (dB)	14	12	14.8	15.6	9	13	12	8	**9.1**
RX Gain (dB)	48	N/A	23	23.1	10	24	16	21	**18**
Pow. Diss. (W)	1.3 (min)	1.2	0.275	0.52	1.37	1.2	1.95	0.61	**0.322**
Technique	FMCW	BPSK	FMCW	FMCW with DDS	PRN with Pulse Comp.	PRN with PRBS	FMCW	Single Pulse	**FMCW**
Modulation BW (GHz)	1	1	0.7	0.614	1	4.25	1	1	**1**
Range Res. (cm)	N/A	N/A	21.4	24.4	15	3.5	N/A	15	**15**
Structure (# of Ant.)	Bistatic (6)	Bistatic (7)	Bistatic (2)	Bistatic (2)	Bistatic (2)	Bistatic (2)	Bistatic (5)	Bistatic (2)	**Monostatic (1)**
Area (mm^2)	108.16=	56.25=	0.97	6.8	4.31	5.9	11.59	7.4	**5.05**

*Simulation Results
=Area with board

4 Conclusion & Future Work

4.1 Summary of Work

SiGe BiCMOS technologies achieved comparable RF performances to their counterparts, especially to III-V technologies. Further, SiGe BiCMOS technologies enable the integration of SiGe HBTs and Si CMOS transistors on the same die. Thus, SiGe BiCMOS technologies offer to implement low-cost, high-performance, and fully-integrated millimeter-wave systems.

Millimeter-wave systems have become popular due to the latest advancements in IC technologies based on silicon. Besides, the low-atmospheric attenuation levels located at 77, 94, 140, 220 GHz and beyond allow millimeter-wave circuits to perform better. Therefore, these attenuation levels have been a right choice for next-generation systems such as automotive RADAR systems, RADAR sensors, communication links, healthcare systems.

In this thesis work, a 77 GHz FMCW Monostatic RADAR system was designed for automotive applications. The system was implemented with IHP Microelectronics 0.13 μm SiGe BiCMOS SG13G2 technology, which offers high-speed HBTs with $f_T/f_{max}/BV_{CEO}$ of 300GHz/500GHz/1.6V. The schematic designs and implementation of the sub-blocks of the system (frequency octupler, buffer amplifier, LNA, PA, Mixer, EBD, directional coupler, and power detector) are presented. Then, the simulation results of the sub-blocks and the entire system were shown. The designed system achieves proper detection up to 180 m range and 170 km/h velocity. Also, the designed system can identify two objects with a range resolution of 15 cm. The system benefits from utilizing a monostatic structure, which reduces the area and cost significantly. Further, the FMCW approach decreases power consumption when compared to the other topologies.

4.2 Future Work

As a short-term future work, the simulation results of the designed system need to be verified with measurement results. Also, this entire system and its sub-blocks were designed for a flip-chip substrate. Therefore, a special board will be designed to connect the system with its required baseband components. Further, instead of

a horn antenna, a patch antenna array can be designed and be integrated to the system with flip-chip packaging.

LNA can be re-designed with a fully differential approach rather than pseudo-differential, to decrease the area. Also, the mixer can be improved in terms of its linearity performance instead of conversion gain.

The possible effects of the phase noise of the chirp signal generated by VCO-PLL chain will be analyzed in MATLAB. The level of the phase noise can change due to the external effects since the chirp is generated off-chip.

As a long-term future work, the control mechanism of the impedance tuning should be finished. The system should be capable of operating a closed-loop system, which can compensate the antenna impedance mismatch preserve the isolation between RX and TX chains automatically.

Also, another long-term future work can be implementing an array structure. Depending on the accuracy, number of array can be determined. Angle of arrival estimation would be included with array structure, which would improve the performance of the RADAR.

APPENDIX

A. Appendix

```
T = 20.0;
Patm = 101.325e3;
rhowv = 12.8;
km = 1000.0;
c = physconst('LightSpeed');
freqs = [1:1000]*1e9;
loss = gaspl(km,freqs,T,Patm,rhowv);
semilogy(freqs/1e9,loss)
grid on
xlabel('Frequency (GHz)')
ylabel('Specific Attenuation (dB/km)')
```

B. Appendix

```
clear all; close all;
fc = 77e9;
c = 3e8;
lambda = c/fc;
rangemax = 200;
tm = 6*range2time(rangemax,c);
rangeres = 0.15;
bw = range2bw(rangeres,c);
sweepslope = bw/tm;
frmax = range2beat(rangemax,sweepslope,c);
vmax = 230*1000/3600;
fdmax = speed2dop(2*vmax,lambda);
fbmax = frmax+fdmax;
fs = 5e08;
```

```
waveform = phased.FMCWWaveform('SweepTime',tm,'SweepBandwidth',bw,...
'SampleRate',fs);
sig = waveform();
subplot(211); plot(0:1/fs:tm-1/fs,real(sig));
xlabel('Time (s)'); ylabel('Amplitude (v)');
title('FMCW signal'); axis tight;
subplot(212); spectrogram(sig,32,16,32,fs,'yaxis');
title('FMCW signal spectrogram');
cardist = 180;
carspeed = 170*1000/3600;
carrcs = db2pow(min(10*log10(cardist)+5,20));
cartarget = phased.RadarTarget('MeanRCS',carrcs,'PropagationSpeed',c,...
'OperatingFrequency',fc);
carmotion = phased.Platform('InitialPosition',[cardist;0;0.5],...
'Velocity',[carspeed;0;0]);
channel = phased.FreeSpace('PropagationSpeed',c,...
'OperatingFrequency',fc,'SampleRate',fs,'TwoWayPropagation',true);
antgain = 20;
txppower = db2pow(8.5)*1e-3;
txgain = 7+antgain;
rxgain = 18+antgain;
rxnf = 9.1;
transmitter = phased.Transmitter('PeakPower',txppower,'Gain',txgain);
receiver = phased.ReceiverPreamp('Gain',rxgain,'NoiseFigure',rxnf,...
'SampleRate',fs);
radarspeed = 0*1000/3600;
radarmotion = phased.Platform('InitialPosition',[0;0;0.5],...
'Velocity',[radarspeed;0;0]);
specanalyzer = dsp.SpectrumAnalyzer('SampleRate',fs,...
'PlotAsTwoSidedSpectrum',true,...
'Title','Spectrum for received and dechirped signal',...
'ShowLegend',true);
```

```
rng(2012);
Nsweep = 1024;
xr = complex(zeros(4000,Nsweep));
for m = 1:Nsweep
[radarpos,radarvel] = radarmotion(waveform.SweepTime);
[tgtpos,tgtvel] = carmotion(waveform.SweepTime);
sig = waveform();
txsig = transmitter(sig);
txsig = channel(txsig,radarpos,tgtpos,radarvel,tgtvel);
txsig = cartarget(txsig);
txsig = receiver(txsig);
dechirpsig = dechirp(txsig,sig);
specanalyzer([txsig dechirpsig]);
xr(:,m) = dechirpsig;
end
rngdopresp = phased.RangeDopplerResponse('PropagationSpeed',c,...
'DopplerOutput','Speed','OperatingFrequency',fc,'SampleRate',fs,...
'RangeMethod','FFT','SweepSlope',sweepslope,...
'RangeFFTLengthSource','Property','RangeFFTLength',2048,...
'DopplerFFTLengthSource','Property','DopplerFFTLength',256);
clf;
plotResponse(rngdopresp,xr);
axis([-vmax vmax 0 rangemax])
clim = caxis;
```

C. Appendix

```
clear all; close all;
fc = 77e9;
c = 3e8;
lambda = c/fc;
rangemax = 200;
```

```
tm = 6*range2time(rangemax,c);
rangeres = 0.15;
bw = range2bw(rangeres,c);
sweepslope = bw/tm;
frmax = range2beat(rangemax,sweepslope,c);
vmax = 230*1000/3600;
fdmax = speed2dop(2*vmax,lambda);
fbmax = frmax+fdmax;
fs = 5e08;
waveform = phased.FMCWWaveform('SweepTime',tm,'SweepBandwidth',bw,...
'SampleRate',fs);
sig = waveform();
subplot(211); plot(0:1/fs:tm-1/fs,real(sig));
xlabel('Time (s)'); ylabel('Amplitude (v)');
title('FMCW signal'); axis tight;
subplot(212); spectrogram(sig,32,16,32,fs,'yaxis');
title('FMCW signal spectrogram');
cardist = 150;
cardist2 = 110;
carspeed = 100*1000/3600;
carspeed2 = -60*1000/3600;
carrcs = db2pow(min(10*log10(cardist)+5,20));
carrcs2 = db2pow(min(10*log10(cardist2)+5,20));
cartarget = phased.RadarTarget('MeanRCS',carrcs,'PropagationSpeed',c,...
'OperatingFrequency',fc);
carmotion = phased.Platform('InitialPosition',[cardist;0;0.5],...
'Velocity',[carspeed;0;0]);
cartarget2 = phased.RadarTarget('MeanRCS',carrcs2,'PropagationSpeed',c,...
'OperatingFrequency',fc);
carmotion2 = phased.Platform('InitialPosition',[cardist2;0;0.5],...
'Velocity',[carspeed2;0;0]);
channel = phased.FreeSpace('PropagationSpeed',c,...
```

```
'OperatingFrequency',fc,'SampleRate',fs,'TwoWayPropagation',true);
channel2 = phased.FreeSpace('PropagationSpeed',c,...
'OperatingFrequency',fc,'SampleRate',fs,'TwoWayPropagation',true);
antgain = 20;
txppower = db2pow(8.5)*1e-3;
txgain = 7+antgain;
rxgain =18+antgain;
rxnf = 9.1;
transmitter = phased.Transmitter('PeakPower',txppower,'Gain',txgain);
receiver = phased.ReceiverPreamp('Gain',rxgain,'NoiseFigure',rxnf,...
'SampleRate',fs);
radarspeed = 0*1000/3600;
radarmotion = phased.Platform('InitialPosition',[0;0;0.5],...
'Velocity',[radarspeed;0;0]);
specanalyzer = dsp.SpectrumAnalyzer('SampleRate',fs,...
'PlotAsTwoSidedSpectrum',true,...
'Title','Spectrum for received and dechirped signal',...
'ShowLegend',true);
rng(2012);
Nsweep = 2048;
xr = complex(zeros(4000,Nsweep));
for m = 1:Nsweep
[radarpos,radarvel] = radarmotion(waveform.SweepTime);
[tgtpos,tgtvel] = carmotion(waveform.SweepTime);
[tgtpos2,tgtvel2] = carmotion2(waveform.SweepTime);
sig = waveform();
txsig = transmitter(sig);
txsigout1 = channel(txsig,radarpos,tgtpos,radarvel,tgtvel);
txsigreflect1 = cartarget(txsigout1);
txsigout2 = channel2(txsig,radarpos,tgtpos2,radarvel,tgtvel2);
txsigreflect2 = cartarget2(txsigout2);
txsig = txsigreflect1 + txsigreflect2;
```

```
txsig = receiver(txsig);
dechirpsig = dechirp(txsig,sig);
specanalyzer([txsig dechirpsig]);
xr(:,m) = dechirpsig;
end
rngdopresp = phased.RangeDopplerResponse('PropagationSpeed',c,...
'DopplerOutput','Speed','OperatingFrequency',fc,'SampleRate',fs,...
'RangeMethod','FFT','SweepSlope',sweepslope,...
'RangeFFTLengthSource','Property','RangeFFTLength',2048,...
'DopplerFFTLengthSource','Property','DopplerFFTLength',256);
clf;
plotResponse(rngdopresp,xr);
axis([-vmax vmax 0 rangemax])
clim = caxis;
```

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