DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

PRODUCTION AND APPLICATION OF N- AND P-TYPE SI WAFER USING CVD METHOD

by
Salih Alper AKALIN

September, 2015
İZMİR

PRODUCTION AND APPLICATION OF N- AND P-TYPE SI WAFER USING CVD METHOD

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by

Salih Alper AKALIN

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M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled "**PRODUCTION AND APPLICATION OF N- AND P-TYPE SI WAFER USING CVD METHOD**" completed by **SALİH ALPER AKALIN** under supervision of **PROF.DR. ERDAL ÇELİK** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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PRODUCTION AND APPLICATION OF N- AND P-TYPE SI WAFER USING CVD METHOD

ABSTRACT

Necessity for electricity is one of the most significant issues of present time. Rapid consume of most used underground resources made it necessary for researching the new kind of energy sources. After the increase of daily requirements and quality necessities, innovations in electric production technologies gained importance. Production of electricity from the sun is based on the principal of contacting the two sides of a semiconductor stimulated by sun and the returning of electrons which have been sent to conductivity level to their initiation locations after completing the entire circuit.

Materials science which is a multidisciplinary branch could be defined as investigation and development of proper tools for providing sources for humanity. In this respect, in the scale of current thesis, production of solar cells for renewable energy obtainment using modified semiconductor silicon wafers was aimed and studied.

Single crystal structured crystal wafers with semi-conductive character were modified and the stimulation of material with sun light was achieved. In order to enlighten the structures of the produced solar cells, SEM, XRD, XPS, UV-vis and profilometer calculations were carried out. In addition of structural analysis, electrical properties of the produced cells were determined.

There are many remarkable factors in current study in order to benefit fully from the sunlight. By texturation, refraction of photons interacted with surface was prevented opposite to the angle they interacted. Optimum realization studies of electron-hole separation were achieved with diffusion time determination. With utilization of reflection blocker coating, absorption of rays interacted with the surface of solar cells was provided.

In addition to the scientific results, with the support of İZ-KA to the current study, more attention to renewable energy in Dokuz Eylül University was gained. Thanks to the energy stations in university in scope of current project, charging the batteries of electrical devices was realized.

Keywords: Solar cell, silicon, doping, semiconductors

CVD YÖNTEMİ KULLANILARAK N- VE P-TİPİ Sİ WAFER ÜRETİMİ VE UYGULAMASI

ÖZ

Elektrik ihtiyacı günümüzün en önemli konularından biridir. Çeşitli elektrik üretim yöntemleri olmakla birlikte, en çok kullanılan yer altı kaynaklarının hızla tüketilmesi yeni enerji kaynakları arayışını zorunlu kılmıştır. Dünyada günlük ihtiyaç ve kalite gereksinimlerin artması ile birlikte elektrikle üretme teknolojilerinde de yenilik arayışı önem kazanmıştır. Güneşten elektrik enerjisi üretimi güneş ışınlarıyla uyarılan bir yarıiletkenin iki ucuna kontak yapılması ve iletkenlik seviyesine geçen elektronlar devreyi tamamladıktan sonra eski konumlarına geri dönmesi prensibine dayanmaktadır.

Disiplinler arası bir bilim olan malzeme bilimi; insanlık ihtiyaçlarını karşılayacak cihazların geliştirilmesi için uygun malzemelerin araştırılması ve geliştirilmesi olarak tanımlanabilir. Bu tez kapsamında katkılanmış yarıiletken silisyum waferlar kullanılarak yenilenebilir enerji üretimi için güneş hücresi üretilmesi hedeflenmiştir.

Kendisi de bir yarıiletken olan tek kristal silisyum wafera katkılamalar yapılarak güneş ile uyarılabilmesi sağlanmıştır. Üretilen hücrelerinin yapılarının aydınlatılabilmesi için; SEM, XRD, XPS, UV-Vis, ve Profilometre ölçümleri yapılmıştır. Yapısal analizlere ek olarak üretilen hücrelerin elektriksel özellikleri, belirlenmiştir.

Çalışmada bir çok önemli faktör vardır. Güneş ışığından maksimum yararlanmak için tüm bu faktörler bir hayli önemlidir. Tekstürleme ile malzeme yüzeyine gelen ışınların geldikleri açıyla yansımaları engellenmiştir. Difüzyon süresi çalışmalarıyla electron-boşluk ayrımının optimum gerçekleşme çalışmaları yapılmıştır. Yansıma önleyici kaplama ile hücre üzerine gelen ışınların absorblanması sağlanmıştır.

Bilimsel sonuçlara ek olarak; çalışmanın desteklendiği İZ-KA ile yenilenebilir enerjiye üniversite içerisinde farkındalık kazandırılmıştır. Üniversite içerisinde kurulan güneş enerjili elektrik istasyonları sayesinde yine proje kapsamında üretilen elektrikli araçların akülerini şarj etmesi sağlanmıştır.

Anahtar Kelimeler: Güneş hücresi, silisyum, doplama, yarıiletkenler

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CHAPTER ONE
INTRODUCTION

1.1 General

Semiconductor technologies are essential for almost all devices that use electronic circuits and chips. Since the discovery of semiconductor characteristic of silicon, developments in this field have accelerated significantly and get chipper way because silicon is the second most abundant element in the earth. Pure silicon is intrinsic semiconductor (described in Chapter Two) and has too low conductivity to use electronic circuits. It should be doped with small amount of other particular elements to increase conductivity and to set electronic response by controlling qualifications of carriers that are compulsory for transistors, solar cells, detectors and other semiconductor devices.

Solar cells are a kind of semiconductor detectors that detect sunlight whereby difference of potential was occurred by movements of electrons that induced by photons from sunlight. This phenomenon takes place in the creation of the p-n junction. To form p-n junction, silicon must be doped with elements that transform intrinsic silicon to p-type and n-type silicon, these are generally boron and phosphorus compounds that use commercially, respectively. This topic is explained in detail in Chapter Two.

One of the biggest issues of this century is energy. Rapid depletion of the underground power resources (oil, coal, natural gas, etc.) indicates that there is a need for new energy. Solar energy, which has become the trend of the types of renewable energy, can play a key role to afford the energy requirements. The initial investment cost is relatively high but it does not require much maintenance that costs are low. Another important point is that there is not any CO_2 emission during power generation; this enables the production of electricity without damaging the environment.

From past to present production of single crystal silicon wafer and study on its solar cell applications has been an important research topic. The previous studies in literature about production and application of solar cells have examined in the frame of this thesis.

Literature researches of the texturing process are given below.

Dimitrov & Du have released a publication entitled “Crystalline silicon solar cells with micro/nano texture”. In this study, p-type Cz c-Si wafers with (100) oriented, 180-240 μm thickness and 3-6 Ω.cm resistivity were used. At first, micron-sized random pyramids were generated in KOH-IPA solution at 80 °C for 45 min. Cleaning process was carried out in HCI:H_2O_2:H_2O (HPM) combination at same temperature for 10 min. Second process was realized to make the surface into nanotextured form onto the pyramids. This is a two-step process. At first step, electroless treatment was performed in $Na_2S_2O_8$ and $AgNO_3$ mixture (acidic aqueous solution) at room temperature for 6 min. Secondly; HF/H_2O_2/H_2O combination was used etching at same temperature for 2 min. As a result, hierarchical structure (nanotexture on microtexture) was successfully performed. SEM images and spectrophotometric reflection data supported these results. SEM images showed that nanotextured structures were produced onto the surface of the micron-sized pyramids. When compared with macrotextured structures, nanotextured ones showed lower light reflection character with values below 3% reflection rate (Dimitrov & Du, 2013).

Han et al have released a publication entitled “Formation of various pyramidal structures on monocrystalline silicon surface and their influence on the solar cells”. In this study, p-type monocrystalline Si wafers with (100) oriented, 200 μm thickness and 0.5-3 Ω.cm resistivity were used. At first, wafers were cleaned by using standard Radio Corporation of America (RCA) cleaning method and then rinsed in DI-water before releasing any etching process. A solution including 20 wt% NaOH at 80 °C for 10 min was used to accomplish the saw damage removal (SDR) step and rinsed completely. After this process, wafer thickness was reduced to 170

μm from 200 μm. 1.5 wt% NaOH, 4 vol% IPA and one additive of 0.1 wt% Na_2SiO_3, 0.06 vol% PEG or 0.01 vol% NPE mixture was used to texturing process at same temperature for 25 min. To decrease the silicon/electrolyte interfacial energy to produce unique pyramidal structure and to modify the speed of reaction, these additives were utilized (Vazsonyi, Clercq, & Einhaus, 1999). Approximately 10 μm-sized pyramidal structures were carry out on sample that treated no additive solution. Na_2SiO_3, PEG and NPE added process could obtain about 5 μm, 1 μm and 200 nm-sized pyramids, respectively. Reflectivity results showed that 1 μm-sized pyramids gave better results although very close to 5 and 10 μm-sized ones (Han, Yu, Wang, & Yang, 2013).

Iftiquar et al have reported a publication entitled "Fabrication of crystalline silicon solar cell with emitter diffusion, SiN_x surface passivation and screen printing of electrode". In this study, Cz-Si wafers with (100) oriented and 300 μm thickness were used. NaOH and IPA mixture was utilized to enhance texturing. IPA increases surface diffusion so that it provides rapid etching (Zubel, 2000). Concentration of the solution can change etching type. 8 % NaOH solution at 80 °C carries out isotropic etching to obtain a polished surface of the wafer but 2 % NaOH by addition of 8 % IPA achieves anisotropic etching to possess a square based pyramidal surfaces at same temperature. 2 wt% and 6 wt% were chosen for amount of wt% NaOH and wt% IPA, respectively and effect of different process times was analysed. Enlarging in etching time caused enlarging in pyramid size, and these two characteristics were directly proportional. The results of pyramids size were 3, 5, 7 and 10 μm when etching times were 25, 30, 35, 40, and average reflectivity of them were 17.2, 17.0, 16.1 and 15.1%, respectively (Iftiquar, Lee, Ju, Balaji, Dhungel, & Yi, 2012).

Literature researches of the doping process are given below.

Ali et al have published an arcticle entitled "Spin-on doping (SOD) and diffusion temperature effect on recombinations/ideality factor for solar cell applications". The aim of this study is investigation of the effect of the different temperatures on diffusion process with spin-on doping. In this study, monocrystalline (100) oriented

Si wafers were used. The dimensions of these wafers were 1.5 cm x 1.5 cm x 290 μm. First, standard RCA cleaning to the wafers to take away oxide layer, DI-water rinsing and N_2 blowing steps were carried out, respectively. After wafers are dried in the oven at 100 °C for 10 min, spinning process was performed at room temperature. Nearly 15 drops of dopant (phosphorus source) were dripped on the surfaces, wafers were spun at 2000 rpm for 25 sec at spin coater to generate 0.5 μm thickness of dopant layer. After this process, wafers were dried at 100 °C for 10 min, and then wafers were heated at 900 °C, 930 °C, 950 °C, 980 °C, 1000 °C, 1050 °C and 1100 °C for 60 min each in a quartz tube furnace. As a result, the maximum sheet resistance value was 108 Ω/sq at 900 °C and the minimum value was at 10.10 Ω/sq 1100 °C with decreasing change by comparison 1030 °C, 1050 °C and 1080 °C. In conclusion, it was found that doping process at 950°C was appropriate with lowest ideality factor and it's sheet resistance value (40 Ω/sq) was also close to mostly industrial values (40-50 Ω/sq) (Ali, Khan, & Jafri, 2012).

Mathiot et al have studied about "Phosphorus diffusion from a spin-on doped glass (SOD) source during rapid thermal annealing". The aim of this study is the investigation of the diffusion kinetics of phosphorus after RTA and comparing for rapid thermal process and standard thermal process. In this study, p-type (100) oriented Si wafers with 1-10 Ω.cm resistivity were used. The dimensions of these wafers were 1.5 cm x 1.5 cm x 450 μm and one side is polished. SOD solution that contains phosphorus dopant taken from Filmtronics Co. (USA) was performed by spin-on technique using spin coater that spun the wafer at 9900 rpm/min for 15 sec. Pre-drying was carried out at 200 °C for 15 min on hot plate, followed by wafers were placed in the RTP furnace where rapid thermal processing was performed at 800-950 °C for 2-120 sec in a tungsten halogen lamp system in Ar ambient. For aim of comparing, some samples coated P-SOD were tempered with classical thermal processing at corresponding temperature for 15 min. As a result, commercial sheet resistance value (40-100 Ω/sq) was achieved in RTP furnace after 25 sec, despite 15 min in a standard furnace (Mathiot, Lachiq, Slaoui, Noel, Muller, & Dubois, 1998).

Tang et al have reported a publication entitled “Preparation of n+ emitter on p-type silicon wafer using the spin-on doping method”. The objective of this study is focusing on using spin-on doping (SOD) approach to produce n+ emitter with phosphorus diffusion and for antireflection coating (ARC) to decrease reflection. In this study, polished p-type (100) oriented single crystalline Si wafers with 1-4 Ω.cm resistivity were used. First, SOD solutions were prepared by a mixture of TEOS:H_2O:C_2H_5OH (10:20:3) (Huang & Chou, 2003), and then addition of phosphorus acid (H_3PO_5) to the mixture was performed to introduce the hydrolysis reaction of TEOS at 70 °C, whole solution was mixed for 60 min followed by cooled to room temperature. The next step for preparing solution is adding NH_4OH to this mix with continuing stirring to begin polymerization process at room temperature and after ammonia was added, this solution was capable to use for spinning process for 30 min. Spinning process was performed at 3000 rpm/min for 30 secs with four solution containing different amount of phosphorus. Pre-drying was carried out at 200 °C in air and then wafers were heated at 750-950 °C for 10-120 min for the thermal diffusion. As a result, sheet resistance value of TEOS/H_3PO_4=1.5:1 sample was minimum (1.2 Ω/sq) and TEOS/H_3PO_4=6:1 one was maximum (800 Ω/sq). This result showed that phosphorus concentration was directly related with sheet resistance and the higher phosphorus concentration was the lower sheet resistance value. Sample 3 (TEOS/H_3PO_4=5:1) was nearly the optimum value and for this reason, various experiments were performed constant temperature – variable time and constant time – variable temperature. As conclusion, it was found that optimum value for temperature and time was 900 °C and 60 min, respectively (Tang, Wang, Hu, Qin, Du, & Shi, 2012).

Lee et al have published an article entitled “17.9% efficiency silicon solar cells by using spin-on films processes”. The aim of this study is investigation of spin-on film (SOF) method for phosphorus diffusion and rapid temperature annealing (RTA) to prepare n+ emitter. In this study, p-type (100) oriented single crystalline Si wafers with 1-10 Ω.cm resistivity were used. The dimensions of these wafers were 1 cm x 1cm x 525 μm. After standard RCA cleaning, the samples are firstly coated with the phosphorus diffusion source by using the spin-on technique. The samples are spun at

a speed of 6000 rpm for 20 s, followed by a prebaking at 200±C for 5 min and at 400 °C for 10 min on the hot plate. Then the sample was hold in RTA chamber at 900 °C for 2 min for a diffusion process. In the result of this article, short-circuit of 5.35 mA, open circuit voltage of 0.56 V, and fill factor of 78.64% are obtained. (Lee, Ho, Syu, Lai, & Yu, 2011).

1.2 Organization of The Thesis

The main purpose of this thesis is to form n- and p-type silicon wafers from intrinsic single crystal silicon wafers using phosphorus and boron compounds, respectively. In addition to the use of commercial wafers, wafers are prepared from ingots that we produced. This process is one of the secondary goals of this thesis. Ingot slicing, lapping and polishing operations were carried out to prepare the wafer, respectively.

In the context of literature review and existing opportunities, it has decided to use $POCl_3$ as a phosphorus source to form n-type silicon and BN as a boron source to form p-type silicon. The other objective is to create a p-n junction with doping phosphorus atoms onto the p-type silicon wafer to generate the basis of the solar cell for application of this thesis. Texturing, anti-reflection coating and contacting operations were carried out to produce laboratory type solar cell.

In Chapter Two, semiconductors, their types, application fields, silicon that is one of the important semiconductor, and its production and application as solar cell are explained as a theoretical background. In Chapter Three, experimental procedures of silicon wafer and its application as solar cell are explained. At the same time this chapter concerns with characterization performed on single crystal silicon wafer. All characterization techniques and applications are described briefly. In Chapter Four, the results concerning silicon wafer and its application as solar cell are demonstrated and discussed in details. The general conclusion of this study and future plans are presented in Chapter Five.

CHAPTER TWO
THEORETICAL BACKGROUND

2.1 Semiconductors

Semiconductors are materials that have conductivity between conductors and insulators. Metals having conductivities on the order of 10^7 $(\Omega.m)^{-1}$ are good conducting materials. Insulators having conductivity between 10^{-10} and 10^{-20} $(\Omega.m)^{-1}$ are very low conductivities. The other most important material type, semiconductors, have generally conductivity between 10^{-6} and 10^4 $(\Omega.m)^{-1}$. This situation was given in Figure 2.1.

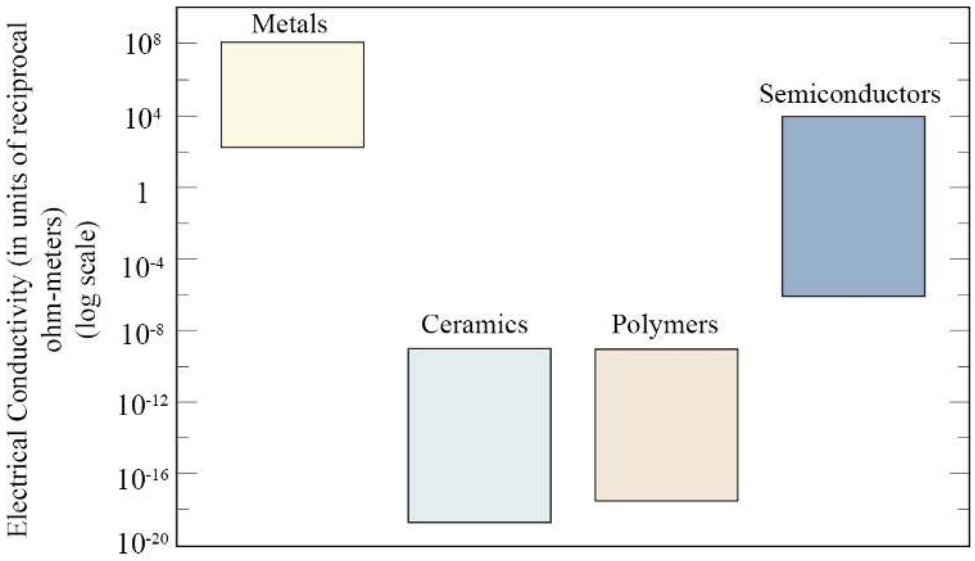


Figure 2.1 Electrical conductivity of some kind of materials (Callister & Rethwisch, 2010)

In order to understand differences of electrical conductivity between these materials in more detail, Figure 2.2 can be analysed. Four distinct sorts of band structures are conceivable at 0 K. E_f is Fermi Energy that means energy corresponding to the highest filled state at this temperature. The electron band structures of some kind of metals are shown in Figures 2.2a and 2.2.b. In insulators, the filled valence band is isolated from the empty conduction band by a generally huge band gap (>2 eV) that is denoted in Figure 2.2c. The electron structure of

semiconductors looks like similar with insulators but the most important difference is the band gap is generally slender (< 2 eV) that is shown in Figure 2.2d.

For semiconductors to become conductor, electrons in the valance band should be reached to the conduction band through the band gap and for that, the electron should be excited to exceed the bang gap energy (E_g) by a different energy source that shown in Figure 2.3. For some materials this band gap is a few electron volts wide so frequently the excitation energy is from a nonelectrical source, for example, light or heat. The electron in the conduction band is called a free electron and the remaining space is called a hole.

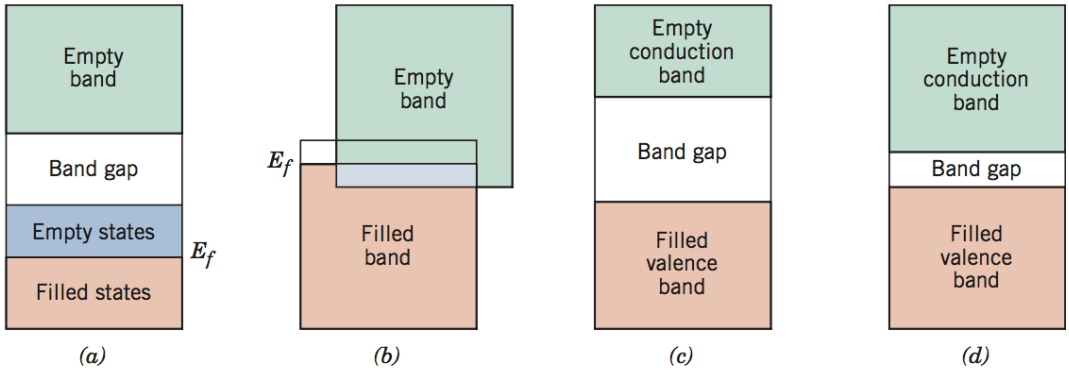


Figure 2.2 The electron band structure of some metals shown in (a) and (b). In insulators, there is a huge band gap shown in (c). There is a smaller band gap in the electron band structure of semiconductors shown in (d) (Callister & Rethwisch, 2010)

In solar cell applications of semiconductors, the excitation energy is the energy of the photons from the sun that is indicated by E_{ph}. If $E_{ph} > E_g$ condition occurs, electrons will be excited as shown in Figure 2.3b. and a potential difference will arise and this means electrical energy is obtained from sun.

Most commonly known semiconductors are silicon (Si) and germanium (Ge). Semiconductivity form also can be seen in the structure of compounds. For instance, gallium arsenide (GaAs), indium antimonite (InSb), cadmium sulphide (CdS) and zinc telluride (ZnTe) are semiconductor compounds. Semiconductors are divided into two as intrinsic semiconductors and extrinsic semiconductors; electrical

properties based on electronic structure of the pure element and impurity atoms, respectively.

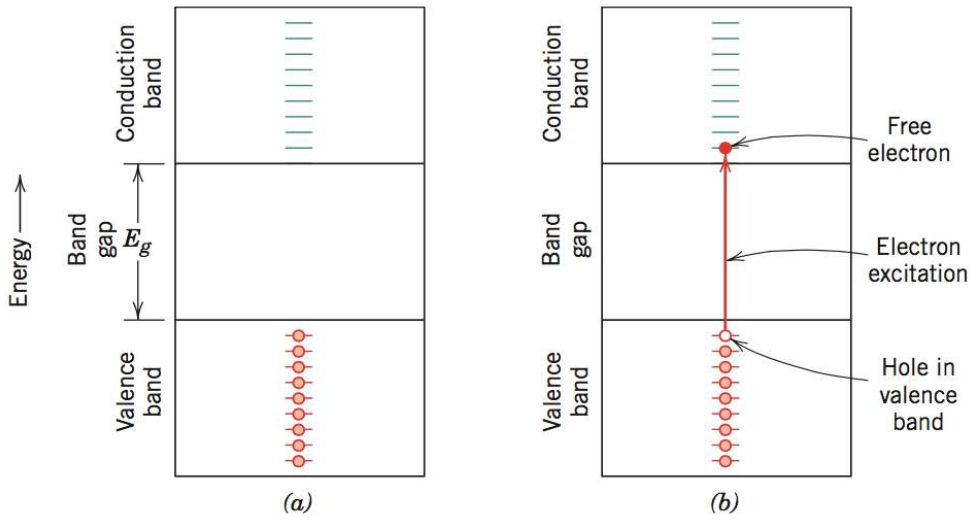


Figure 2.3 Before (a) and after (b) of electron excitation of semiconductors (Callister & Rethwisch, 2010)

2.1.1 Intrinsic Semiconductor

Electrical properties are based on electronic structure of the pure element. The elemental semiconductors are Si and Ge, both are Groups IVA elements and their band gaps are 1.1 eV and 0.7 eV, respectively. There is no need to be pure element to have intrinsic features. Compounds of elements in Groups of IIIA and VA on either sides of the Group IVA possess also intrinsic behaviour, for instance, gallium arsenide (GaAs) and indium antimonite (InSb). In addition to this, compounds of elements in Groups of IIB and VIA show intrinsic features, for example, cadmium sulphide (CdS) and zinc telluride (ZnTe).

If the electric field is applied to the crystal (Figure 2.4a) enough to overcome the energy intervals, an electron is stimulated; a free electron and a hole are consisted that shown in Figure 2.4b. When free electron moves, a hole is left behind. Normally it is not possible hole movement without the electron motion, but the hole can be considered to reverse electron movement.

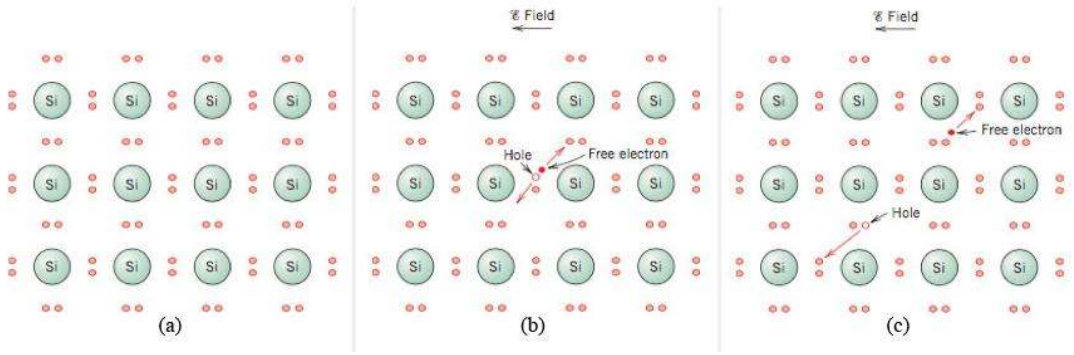


Figure 2.4 Electron bonding model of electrical conduction in intrinsic silicon: (a) before excitation, (b) and (c) after excitation (the subsequent free-electron and hole motions in response to an external electric field) (Callister & Rethwisch, 2010)

Conductivity in an intrinsic semiconductor equals the sum of the two types of charge carriers (free electrons and holes) shown in Equation 2.1.

$$\sigma = \sigma_n + \sigma_p \tag{2.1}$$

where σ_n and σ_p are the conductivity of negative and positive charge carriers, respectively. The equation can be rewritten as follows;

$$\sigma = n|e|\mu_e + p|e|\mu_h \tag{2.2}$$

in which n and p is the number of free electrons and holes per unit volume (cubic meter), respectively. $|e|$ is certain extent of the electrical charge on an electron (1.6 x 10^{-19} C). μ_e and $\mu_h$are mobility of electrons and holes, respectively. Every electron that is excited and activated leaves a hole behind. Therefore, positive and negative charge carriers are equal.

$$n = p = n_i \tag{2.3}$$

where n_i is known as the intrinsic carrier concentration. As a result, conductivity can be written as follows for intrinsic semiconductors.

$$\sigma = n|e|(\mu_e + \mu_h) = p|e|(\mu_e + \mu_h) = n_i|e|(\mu_e + \mu_h) \quad (2.4)$$

2.1.2 Extrinsic Semiconductor

If the additive elements (dopants) are substituted for existing atom into the intrinsic semiconductor materials, the conductivity characteristics are altered. Semiconductors that electrical properties are based on impurities are extrinsic semiconductors. In essence, commercially all semiconductors are extrinsic. For instance, an impurity concentration of one atom in 10^{12} is enough to transform silicon from intrinsic to extrinsic at room temperature.

The aim of making an intrinsic semiconductor to extrinsic is adding donor or acceptor state to them and getting band gap narrower and thus to ensure pass electrons to the conduction band with lower excitation energy. In this way electrical energy is obtained by semiconductor induced by sun energy in solar cell applications in solar cell and other applications. Extrinsic semiconductors are divided into two as n-type semiconductors and p-type semiconductors.

2.1.2.1 N-type Semiconductor

When an impurity atom that has five valence electrons is added to silicon structure with four valence electrons, this impurity will replace the existing silicon; four of five electrons will bond other silicon atoms, one of five will be nonbonding electron and be able to stand around to impurity atom by electrostatic attraction. Binding energy of this electron is rather small (approximately 0.01 eV); causes the onset of electrical conductivity by taking off from impurity atom easily. This situation is shown in Figure 2.5. Silicon, one of the Group IVA elements, could be extrinsic semiconductor with Group VA elements as impurity atoms. Phosphorus is the most widely used commercially for extrinsic silicon semiconductors.

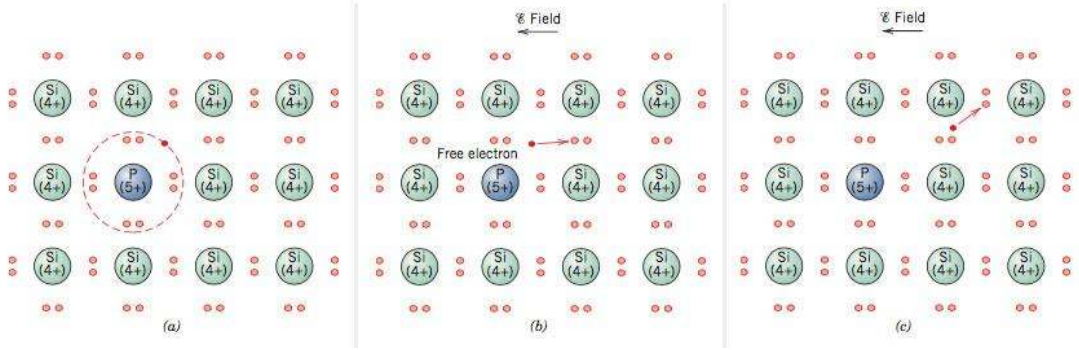


Figure 2.5 Extrinsic n-type semiconduction model (electron bonding). (a) An impurity atom such as phosphorus, having five valence electrons, may substitute for a silicon atom. This results in an extra bonding electron, which is bound to the impurity atom and orbits it. (b) Excitation to form a free electron. (c) The motion of this free electron in response to an electric field (Callister & Rethwisch, 2010).

The excess electron of impurity atom is located almost below the conduction band and this is acceptable as donor state that is shown in Figure 2.6. The excitation energy is stimulated an electron from donor state to conduction band and there is no created hole behind. Even if there is so negligible level of some intrinsic valence-conduction band transition, the quantity of electrons in the conduction band far surpasses the quantity of holes in the valence band ($n >> p$) and it can be said that electrons are responsible for conduction that is shown in Equation 2.5.

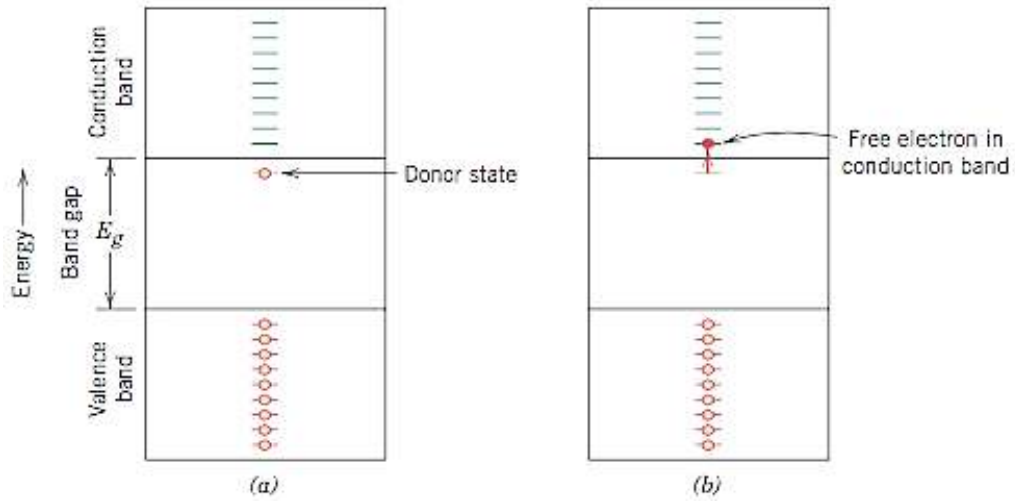


Figure 2.6 (a) Electron energy band scheme for a donor impurity level, (b) excitation from a donor state in which a free electron is generated in the conduction band (Callister & Rethwisch, 2010).

$$\sigma \cong n|e|\mu_e \tag{2.5}$$

This type of material is called an n-type extrinsic semiconductor and in this type; electrons are majority charge carriers while holes are minority charge carriers. The Fermi Energy Level is moved upward in the band gap, towards to the donor state.

2.1.2.2 P-type Semiconductor

The opposite effect can be seen when an impurity atom that has three valence electrons is added to silicon, this impurity will replace the existing silicon atom; all of three electrons will bond other silicon atoms, one hole will carry out. When the structure is stimulated by an energy, this hole acts as the initiator of the electron motion as illustrated in Figure 2.7. Silicon, one of the Group IVA elements, could be extrinsic semiconductor with Group IIIA elements as impurity atoms. Boron is the most widely used commercially for extrinsic silicon semiconductors in solar cell applications and other applications.

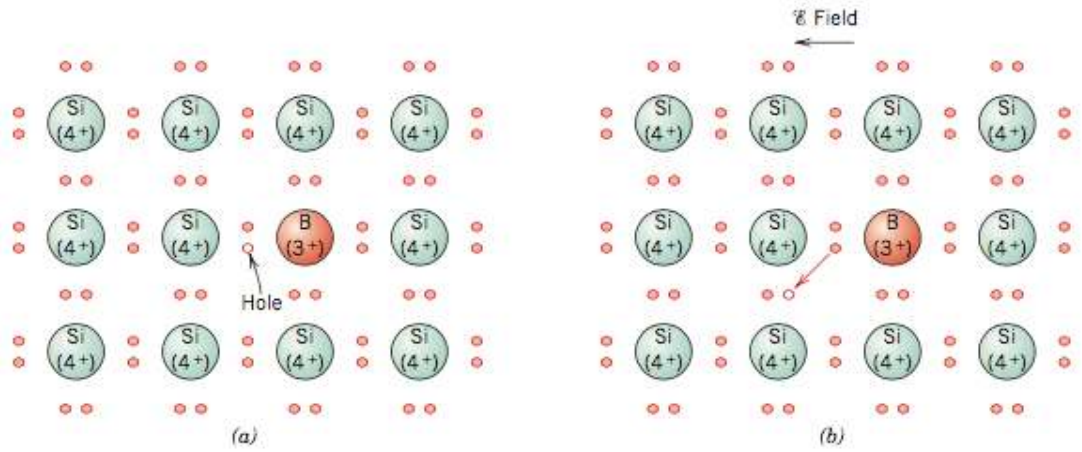


Figure 2.7 Extrinsic p-type semiconduction model (electron bonding). (a) An impurity atom such as boron, having three valence electrons, may substitute for a silicon atom. This results in a deficiency of one valence electron, or a hole associated with the impurity atom. (b) The motion of this hole in response to an electric field.

The hole of impurity atom is located almost above the valence band and this is acceptable as acceptor state that is depicted in Figure 2.8. The excitation energy is

stimulated an electron from valence band to acceptor state; and a new hole is occurred in valance band but there is no created electron in valance band or in conduction band. There is an opposite situation with n-type semiconductor and here, hole concentration is much higher than electrons ($p >> n$), thus it can be said that holes are responsible for conduction as illustrated in Equation 2.6.

$$\sigma \cong p|e|\mu_h \tag{2.6}$$

This type of material is called an p-type extrinsic semiconductor and in this type; holes are majority charge carriers while electrons are minority charge carriers. The Fermi Energy Level is moved downward in the band gap, towards to the acceptor state.

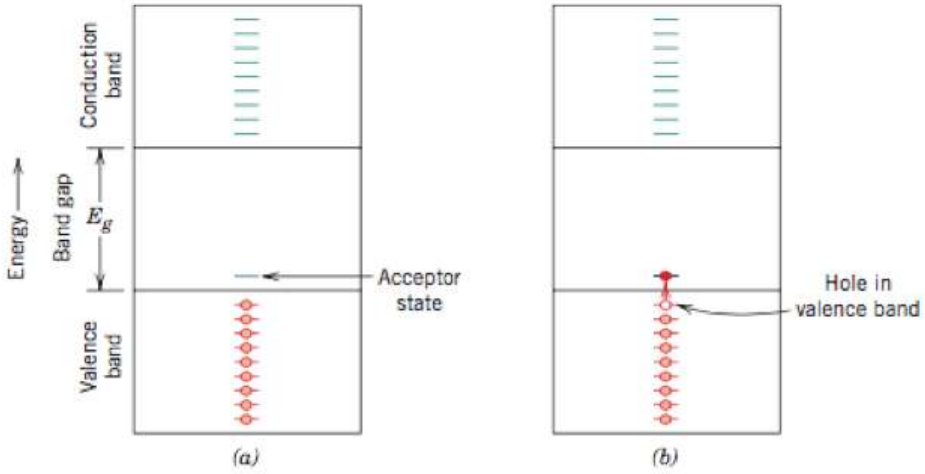


Figure 2.8 (a) Energy band scheme for an acceptor impurity level, (b) excitation of an electron into the acceptor level (Callister & Rethwisch, 2010)

2.2 Application Fields of Semiconductors

Most of electronic devices are developed by utilizing from features of semiconductors. It will be described below that some of them used for what purposes.

2.2.1 Temperature Measurement

Conductivity of semiconductors increases due to temperature and slope of the line in proportion to E_a energy gap. The high E_a value semiconductors become very sensitive to temperature. The temperature difference (10^{-4} °C) can be measured with thermistor developed by utilize from that feature. This feature of semiconductors used in fire alarm installations.

2.2.2 Intensity of Light Measurement

Energy of visible light photons are in the range of 1.7 and 3.5 eV and enough to activate electrons in semiconductors. Light falling on the semiconductors raises the charge carrier to conduction band and provides current flow. Current flow from circuit depends on number of photons, in turn intensity of light. Light intensity measurement devices can be produced due to this feature.

2.2.3 Pressure Measurement

Coordination number of semiconductors materials that bounded covalently is low, under the pressure atoms can be closed quite to each other. In this situation band structure is affected and E_a energy state decreases in turn conductivity increases. It can be utilizing semiconductor crystal calibrated against pressure for pressure measurement.

2.2.4 Materials with p-n Junction Structure

P-n junction is built a piece of semiconductor whose one side is doped to be n-type and the other is doped to be p-type as illustrated in Figure 2.9. If pieces of n- and p-type materials are joined together, a poor rectifier results, because the presence of a surface between the two sections renders the device very inefficient. In addition, single crystals of semiconducting materials must be used in all devices because electronic phenomena that are deleterious to operation occur at grain boundaries.

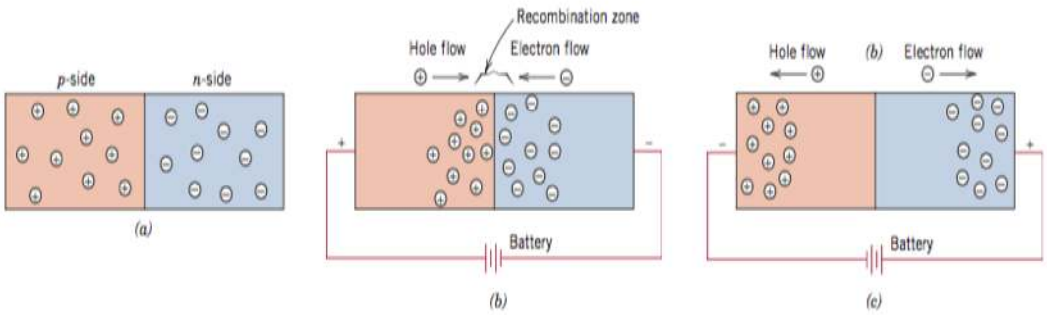


Figure 2.9 For a p–n rectifying junction, representations of electron and hole distributions for (a) no electrical potential, (b) forward bias, and (c) reverse bias (Callister & Rethwisch, 2010)

Since the n-type region has a high electron concentration and the p-type a high hole concentration, electrons diffuse from the n-type side to the p-type side. Similarly, holes flow by diffusion from the p-type side to the n-type side. If the electrons and holes were not charged, this diffusion process would continue until the concentration of electrons and holes on the two sides were the same, as happens if two gasses come into contact with each other. Nonetheless, in a p-n junction, when the electrons and holes move to the other side of the junction, they leave behind exposed charges on dopant atom sites, which are fixed in the crystal lattice and are unable to move. On the n-type side, positive ion cores are exposed. On the p-type side, negative ion cores are exposed. An electric field Ê forms between the positive ion cores in the n-type material and negative ion cores in the p-type material. This region is called the "depletion region" since the electric field quickly sweeps free carriers out, hence the region is depleted of free carriers. A "built in" potential V_{bi} due to Ê is formed at the junction. The animation below shows the formation of the Ê at the junction between n and p-type material.

Before the application of any potential across the p–n specimen, holes will be the dominant carriers on the p-side, and electrons will predominate in the n-region, as illustrated in Figure 2.9a. An external electric potential may be established across a p–n junction with two different polarities. When a battery is used, the positive terminal may be connected to the p-side and the negative terminal to the n-side; this is referred to as a forward bias. The opposite polarity (minus to p and plus to n) is

termed reverse bias. The response of the charge carriers to the application of a forward-biased potential is demonstrated in Figure 2.9b. The holes on the p-side and the electrons on the n-side are attracted to the junction. As electrons and holes encounter one another near the junction, they continuously recombine and annihilate one another, according to (electron + hole → energy). Thus for this bias, large numbers of charge carriers flow across the semiconductor and to the junction, as evidenced by an appreciable current and a low resistivity. For reverse bias (see Figure 2.9c for more details), both holes and electrons, as majority carriers, are rapidly drawn away from the junction; this separation of positive and negative charges (or polarization) leaves the junction region relatively free of mobile charge carriers. Recombination will not occur to any appreciable extent, so that the junction is now highly insulative (Callister & Rethwisch, 2010).

2.2.4.1 Solar Cell

In Figure 2.10, basic solar cell structure is shown. When a photon hits a piece of silicon, one of three things can happen:

1. The photon can pass straight through the silicon - this (generally) happens for lower energy photons.
2. The photon can reflect off the surface.
3. The photon can be absorbed by the silicon if the photon energy is higher than the silicon band gap value. This generates an electron-hole pair and sometimes heat depending on the band structure.

When a photon is absorbed, its energy is given to an electron in the crystal lattice. Usually this electron is in the valence band and is tightly bound in covalent bonds with neighbouring atoms, and therefore unable to move far. The energy given to the electron by the photon "excites" it into the conduction band where it is free to move around within the semiconductor (Figure 2.11). The covalent bond that the electron was previously a part of now has one fewer electron. This is known as a hole. The presence of a missing covalent bond allows the bonded electrons of neighbouring

atoms to move into the "hole," leaving another hole behind, thus propagating holes throughout the lattice. It can be said that photons absorbed in the semiconductor create mobile electron-hole pairs.

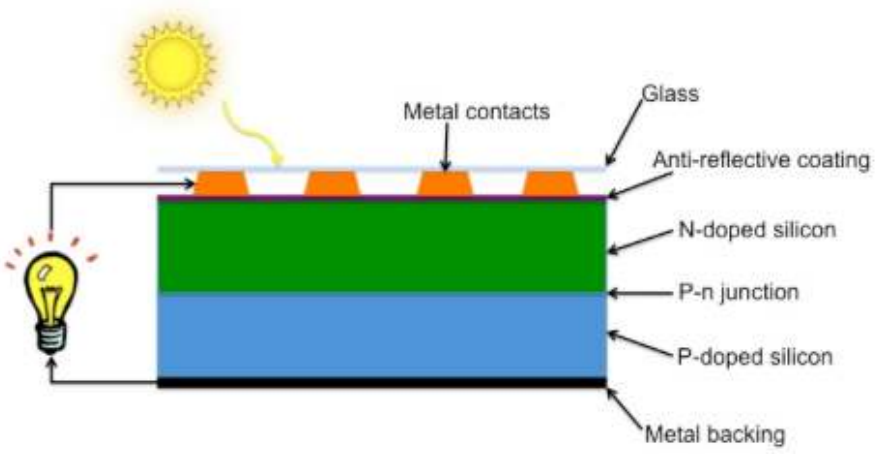


Figure 2.10 Schematic of the basic structure of a silicon solar cell (Reddy, 2009).

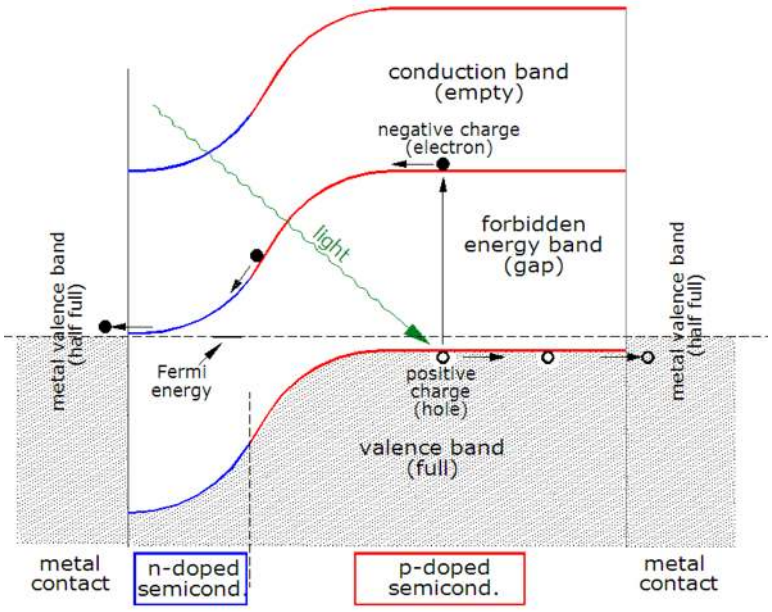


Figure 2.11 Band diagram of a silicon solar cell, under short circuit conditions (Reddy, 2009).

A photon need only have greater energy than that of the band gap in order to excite an electron from the valence band into the conduction band. Much of the solar radiation reaching the earth is composed of photons with energies greater than the

band gap of silicon. These higher energy photons will be absorbed by the solar cell, but the difference in energy between these photons and the silicon band gap is converted into heat (via lattice vibrations — called phonons) rather than into usable electrical energy. The photovoltaic effect can also occur when two photons are absorbed simultaneously in a process called two-photon photovoltaic effect. However, high optical intensities are required for this nonlinear process.

2.3 The Important Semiconductor – Silicon

Silicon is the eighth most common element in the universe by mass, but very rarely occurs as the pure free element in nature. It is most widely distributed in dusts, sands, planetoids, and planets as various forms of silicon dioxide (silica) or silicates. Over 90% of the Earth's crust is composed of silicate minerals, making silicon the second most abundant element in the Earth's crust (about 28% by mass) after oxygen (Lutgens & Tarbuck, 2000).

Single-crystal silicon is perhaps the most important technological material of the last few decades - the "silicon era" (Heywang & Zaininger, 2004), because its availability at an affordable cost has been essential for the development of the electronic devices on which the present day electronic and informatics revolution is based.

The monocrystalline form is used in the semiconductor device fabrication since grain boundaries would bring discontinuities and favour imperfections in the microstructure of silicon, such as impurities and crystallographic defects, which can have significant effects on the local electronic properties of the material. On the scale that devices operate on, these imperfections would have a significant impact on the functionality and reliability of the devices. Without the crystalline perfection, it would be virtually impossible to build Very Large-Scale Integration (VLSI) devices, in which millions (up to billions, circa 2005 (Clarke, 2005)) of transistor-based circuits, all of which must reliably be working, are combined into a single chip to form a microprocessor, for example. Therefore, the electronics industry has invested

heavily in facilities to produce large single crystals of silicon. Pure monocrystalline silicon is used to produce silicon wafers used in the semiconductor industry, in electronics and in some high-cost and high-efficiency photovoltaic applications. In terms of charge conduction, pure silicon is an intrinsic semiconductor which means that unlike metals it conducts electron holes and electrons that may be released from atoms within the crystal by heat, and thus increase silicon's electrical conductivity with higher temperatures. Pure silicon has too low a conductivity (i.e., too high a resistivity) to be used as a circuit element in electronics.

In practice, pure silicon is doped with small concentrations of certain other elements, a process that greatly increases its conductivity and adjusts its electrical response by controlling the number and charge (positive or negative) of activated carriers. Such control is necessary for transistors, solar cells, semiconductor detectors and other semiconductor devices, which are used in the computer industry and other technical applications. For example, in silicon photonics, silicon can be used as a continuous wave Raman laser medium to produce coherent light, though it is ineffective as an everyday light source.

2.4 Production of Single Crystal Silicon

There are 2 important types of single crystal silicon growth techniques. They are Float-Zone process and Czochralski process.

2.4.1 Float-Zone Process

Float-zone silicon is a high-purity alternative to crystals grown by the Czochralski process. The concentrations of light impurities, such as carbon and oxygen, are extremely low. Another light impurity, nitrogen, helps to control micro defects and also brings about an improvement in mechanical strength of the wafers, and is now being intentionally added during the growth stages.

The float zone (FZ) method is based on the zone-melting principle and was invented by Theuerer in 1962. A schematic setup of the process is shown in Figure 2.12. The production takes place under vacuum or in an inert gaseous atmosphere. The process starts with a high-purity polycrystalline rod and a monocrystalline seed crystal that are held face to face in a vertical position and are rotated.

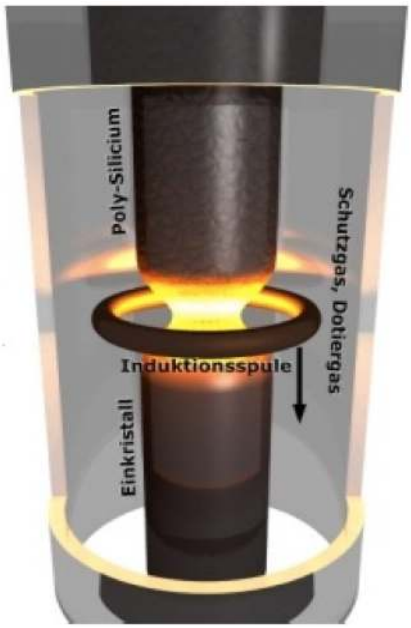


Figure 2.12 Schematic setup for the Float Zone (FZ) process (Leo, 1994)

With a radio frequency field both are partially melted. The seed is brought up from below to make contact with the drop of melt formed at the tip of the poly rod. A necking process is carried out to establish a dislocation free crystal before the neck is allowed to increase in diameter to form a taper and reach the desired diameter for steady-state growth. As the molten zone is moved along the polysilicon rod, the molten silicon solidifies into a single crystal and, simultaneously, the material is purified. Typical oxygen and carbon concentrations in FZ silicon are below $5\text{-}10^{15}$ cm^{-3}. FZ crystals are doped by adding the doping gas phosphine (PH_3) or diborane (B_2H_6) to the inert gas for n- and p-type, respectively. Unlike CZ growth, the silicon molten Zone is not in contact with any substances except ambient gas, which may only contain doping gas. Therefore, FZ silicon can easily achieve much higher purity and higher resistivity.

Additionally, multiple zone refining can be performed on a rod to further reduce the impurity concentrations. Once again the effective segregation coefficient k plays an important role. Boron, for instance, has an equilibrium segregation coefficient of $k_0 = 0.8$. In contrast to this phosphorus cannot only be segregated ($k_0 = 0.35$) but also evaporates from the melt at a fairly high rate. This is the reason why on the one hand it is easier to produce more homogeneous p-type FZ than n-type FZ and on the other hand high resistivity p-type silicon can only be obtained from polysilicon with low boron content. Dopants with a small k_0 like Sn can be introduced by pill doping - holes are drilled into the ingot into which the dopant is incorporated - or by evaporating a dopant layer on the whole ingot before the float zoning process (Leo, 1994).

2.4.2 Czochralski (Cz) Process

Single and polycrystal silicon ingots are grown by the Czochralski process. Charging the polycrystalline silicon chunks into the crucible is the first step of the Czochralski Single Crystal Growth. This polycrystalline must be electronic grade silicon and usually carry with folded double 5 kg bag. Outer layer is separated before this system is useful for blocking any contamination before delivering to charging area. Charge could be in the grower system or firstly crucible could be charged outside of the grower then full crucible is put into the grower.

Important point of this sequence is stacking silicon chunks in the crucible. Within the thermal expansion due to the temperature raise, the charge enlarges although the crucible is unchanged. If chunks do not stack out inside the crucible carefully, chip or crack of the crucible may occur.

Sensitivities of hot-zone and silicon melt to any oxidizing elements explain that growth must be generated under the inert gas atmosphere and reduced pressure. For this reason, the growth chamber must be produced vacuum proof material and before the process, the gas must be unladed and then purged (Anttila, 2010). The schematic setup of Czochralski is shown in Figure 2.13.

2.4.2.1 Melt

The following step is melting. At the beginning, the temperature is raised nearly 1500 °C and kept there to give enough heat to melt all the stack. Limits of temperature is not so wide, because the crucible is almost so soft at this temperature and too much heat could sag the crucible walls.

The crucible, which contains fully molten silicon, is raised to desired position. The stabilization of temperature controlled by a two-colour pyrometer, which senses the surface temperature of the melt nearly seed crystal-dipping area, is generated in the light of the experience of former growth (Anttila, 2010).

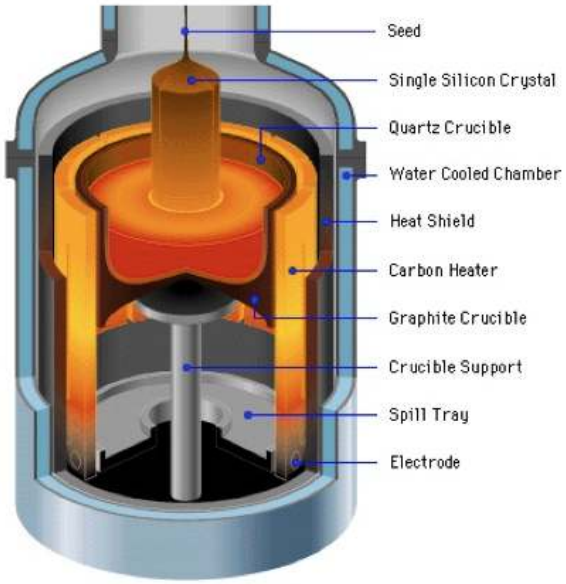


Figure 2.13 Schematic setup for Czochralski process (Anttila, 2010)

2.4.2.2 Neck

In this step, seed crystal, which will specify the crystal orientation of the growing material, dips into the melt. Then the edge of the seed is lifted from the melt and meniscus generates. As seed crystal is lifted towards a higher level, crystallization of new material will take place (Anttila, 2010).

2.4.2.3 Crown

After the necking step have completed with desired length, the crown is begun. Levels of pull speed and temperature are decreased, rotation speeds of crystal and crucible could be altered. Melt level may be accommodated step by step. Making the proper condition is the aim of this step in case of that the crystal obtains diameter at a suitable speed: Too slow speed causes long process time, chance of structure loss, warmer melt and less stability than optimum. On the contrary, the increase in growth rate arises structure loss, too-cool melt that results in unmanageable growth rate (Anttila, 2010).

2.4.2.4 Body

The main part of the whole production is body. Wafers that use in semiconductor industry is acquired from this part. There is an adjustment part called shoulder or transition, which happens immediately before formation of body, is started in the middle of the crown and body. The pull speed is increased notably. The growth in the diameter breaks on top of short distance, the growth turns perpendicular at the required diameter for the body. At that time, the pull speed is decreased to take after the early body. If pull speed goes on upper level, the diameter will become thinner. After the transition part is completed, the next step is body. At this moment, usually temperature reduction is required, but later, this adjustment will decelerate. Pressure, gas flow, rotation rate of the crucible and the crystal are determining parameters for the body length (Anttila, 2010).

2.4.2.5 Tail

At the end of the body, there is a notable portion of the melt that is approximately 10% of the original charge; it can vary from process to process. Tail part comes into existence from that residual melt. At this stage, there are two important purposes: Whilst the crystal pulls away from the melt, slip dislocation will consist of due to the thermal shock. If the growth is separated from the melt immediately at the full

diameter, this slip dislocation will move more than a short distance. First purpose is to prevent proceeding of the dislocation. Secondly, to provide more homogeneous thermal pattern is desirable. If the crystal is separated from the melt at the full diameter, the end part would cool off more quickly than if a long tail is generated. (Anttila, 2010).

2.4.2.6 Shut Off

After the completion of the tail, power may be shut down and the crystal be transferred into the receiving chamber to cool off. Finally, the crystal that called ingot is taken out.

2.5 Wafering

To generate wafers, the ingot must be sliced into the pieces to desired thickness and surface quality. First, shoulder and tail parts of the ingot are cropped; cylindrical (approximately same diameter size) part is left alone. The remaining parts can be taken away to laboratory to measure some characterizations; for example, resistivity measurement and dissolved oxygen and carbon concentration tests with prepared thick slug samples (Tilli, 2010).

Ingot, freeded from excess, may have to cut because of limits permitted by the production but usually the length of grown ingot is adjusted according the slicing systems. There are two types of which systems: ID cutting and wire cutting.

2.5.1 ID Cutting

In this system, there is a thin tensioned diamond blade with a hole at the center whose inner edge exists a thin diamond coating shown in Figure 2.14. The ingot glued to support beam is sliced with this blade moving at a 50 mm/min or higher speed. The biggest disadvantage of this system is only one slicing at a time although wire cutting is able to slice all of ingot. This is a suitable application when small

amount of production is desired and this situation provides good flexibility to entire system (Tilli, 2010).

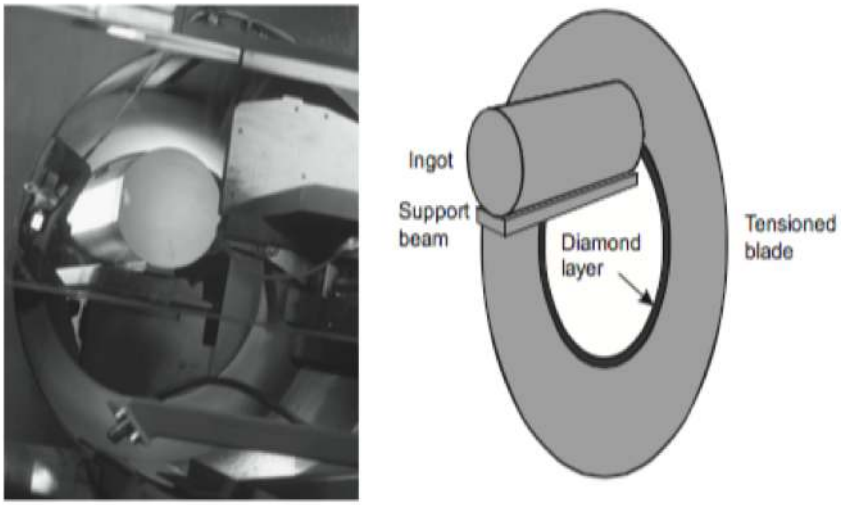


Figure 2.14 ID cutting machine (Tilli, 2010)

2.5.2 Wire Cutting

Wire cutting is a process that permits cutting more than one wafer (up to 1000 wafers depends on system capacity) at the same time. In this system, typically there is a 200-400 kilometres long wire that is wrapped spool and formed a pattern as seen in Figure 2.15.

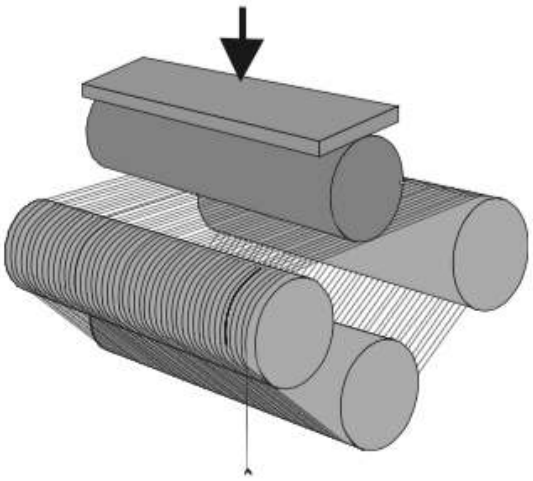


Figure 2.15 Principle of wire cutting (Tilli, 2010)

Wires thickness is about 120-160 μm and abrasive is approximately 12 μm or less. The kerf loss of this system is less than 200 μm in spite of 300 μm at the ID cutting. Cutting is performed by moving the wire. While wire moves horizontally, spool system or ingot moves vertically that varies from machine to machine. Slurry that contains silicon carbide is assisted cutting process; nowadays using only wires that is coated with diamond abrasives is available, too. Heat occurs due to the friction, for this reason the coolant is used. Compared with ID cutting process, surface damage is less but surface waviness is higher (Tilli, 2010).

Even though wire cutting is basically developed for large-scale productions, laboratory scale machine is produced with one or two cutting at a time. One cutting process is completed with moving the wire vertically. After the ups and downs of the wire once, the ingot is moved forward until claimed thickness is achieved and then the next cutting process is started.

2.6 Lapping & Polishing

2.6.1 Lapping

After the slicing process, fluctuations are seen in the wafer thickness, which can be 20 μm or higher from wafer to wafer. Also there is a non-uniform distribution on the wafer surface, which can be different sides. To eliminate problems like these and to achieve an even and uniform wafer surface, this step must be performed.

Traditionally, decreasing dimensional variations and making an even layer are generated with dual-side lapping. Residual material is removed from the wafer surface with abrasive slurry containing alumina powder by rotating the wafers between two flattest, cast-iron plates. After removing 50-100 μm thickness material from the wafer surface, total thickness variation of a wafer will reduce less than 1 μm and average thickness variation of all wafers in the production lot will be a few μm. Surface roughness is usually less than 0.3 μm (R_a) depending on the lapping slurry (Tilli, 2010).

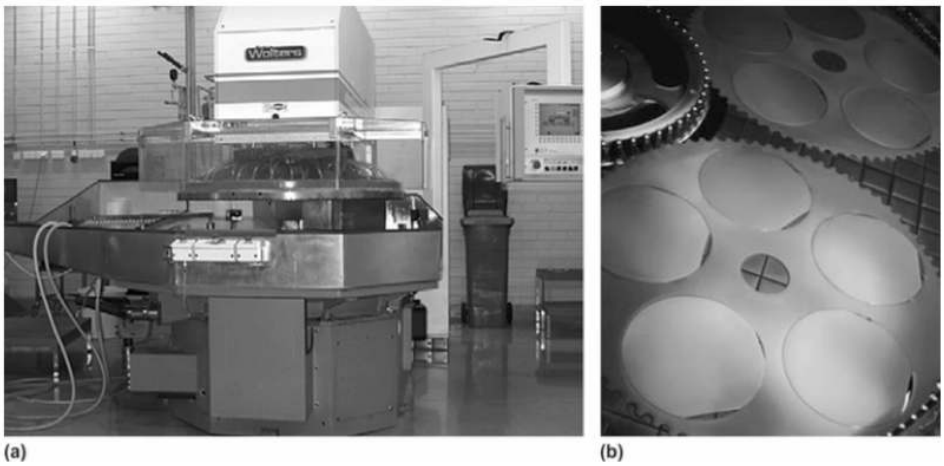


Figure 2.16 Lapping machine, (a) wafers are placed in carrier disk holes on lapping plate, (b) carrier disks are rotated by outer and inner pin rings rotating independently from each other and from upper and from upper and lower lapping plates. Abrasive slurry (alumina, optical emery, or silicon carbide slurry) is fed between lapping plates, and with carefully selected rotation rates and directions of lapping plates and carrier, the best possible flatness and thickness uniformity of wafers can be achieved (Tilli, 2010).

2.6.2 Polishing

Wafers for solar cell applications are polished single side in spite of double side in MEMS applications. Polishing process is generated rotating wafers on the polishing pad made from porous polyurethane using alkaline colloidal silica slurry. Traditionally, ten wafers can be polished at the same time but nowadays the single loading polishing machines is also used. Difficulty is to engage the well wafer flatness succeeded in the former steps.

In the first step of the polishing, material is removed using aggressive slurry while polishing speed is 1 μm/min or more. There is a rugged but flat surface in the result. In the second step, less aggressive slurry is used and as a result, less material is removed and a smooth surface is produced. It was observed when AFM measurement is generated over 1 μm^2 field that surface roughness of the polishing material is about 0.1 nm (RMS) (Tilli, 2010).

2.7 Cleaning

RCA Cleaning Process is one of the most applied cleaning process in Si semiconductor industry and it has been used for more than 40 years in original or modified form (Reinhardt & Kern, 2008). It has been discovered in Radio Corporation of America by W. Kern in 1965, and published in 1970 (Kern & Puotinen, 1970). RCA Standard Clean is divided into two parts, SC-1 and SC-2.

SC-1 consists of HN_4OH, H_2O_2 and H_2O mixture and also known as "APM" which means ammonia/peroxide mixture. Composition range is from 5:1:1 to 7:2:1 parts by volume of H_2O:H_2O_2:NH_4OH. This solution was formulated to clean off organic contaminants from Si, oxide and quartz surfaces.

SC-2 is the second part of cleaning process and consists of HCI, H_2O_2 and H_2O mixture and also known as "HPM" which means hydrochloric/peroxide mixture. Composition range is from 6:1:1 to 8:2:1 parts by volume of H_2O:H_2O_2:HCI. This solution was formulated to dissolve and clean off alkali residues and any residual trace metals (Ag and Au) along with metal hydroxides from Si surfaces.

2.8 Texturing

Inasmuch as solar cells provide electricity from sun, to maximize to benefit from the sunlight is very important. Due to this purpose, surface of the solar cell is etched; thereupon, textured surface is achieved that is depicted in Figure 2.17. Surface texturing provides reduction of reflection losses and enhancing of light absorption, thus causing an increase in efficiency (Dimitrov & Du, 2013).

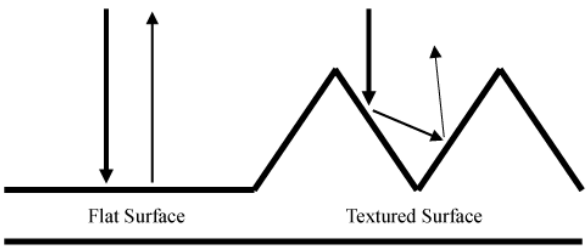


Figure 2.17 Reflection differences of flat and textured surfaces

2.9 Diffusion

After texturing operation, doping process to the wafers are performed to create the p-n junction structure. Diffusion is a frequently used technique for the incorporation of dopant atoms into a semiconductor. The diffusion of impurity atoms into a semiconductor wafer leads to the formation of *p-n* junctions, conduction channels, and source and drain regions (Figure 2.18). The performance of the devices depends critically on the impurity concentration and the impurity profile. In semiconductor technology, the semiconductor wafer is placed in a quartz-tube furnace with dopant species contained in a transport gas that passes over the wafer. There are sufficient dopant atoms in the gas ambient so that the dopants are incorporated in the surface of the semiconductor to concentrations near the solid solubility limit. The furnace is generally heated to high temperatures (app. 900 to 1100°C for Si). At that temperature, the dopant atoms diffuse from the surface into the interior of the semiconductor.

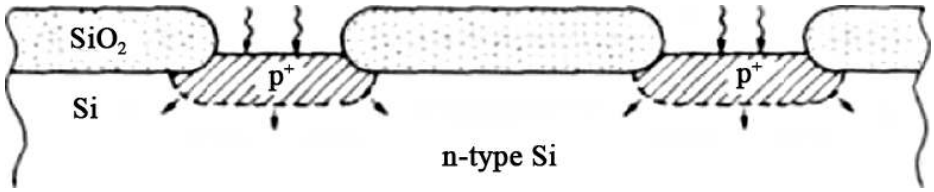


Figure 2.18 Diffusion of boron into the source and drain region (Mayer & Lau, 1998).

The diffusion of impurities into Si wafers is typically done in two steps. In the first step, dopants are introduced into the substrate to a relatively shallow depth of a few thousand angstroms. This process is called predeposition. After the impurities have been introduced into the Si substrate, they are diffused deeper into the substrate to provide a suitable impurity distribution without any additional impurity atoms introduced into the substrate. The second step is called drive-in diffusion. A junction is formed in the substrate after diffusion if the bulk contains the opposite of impurity atoms.

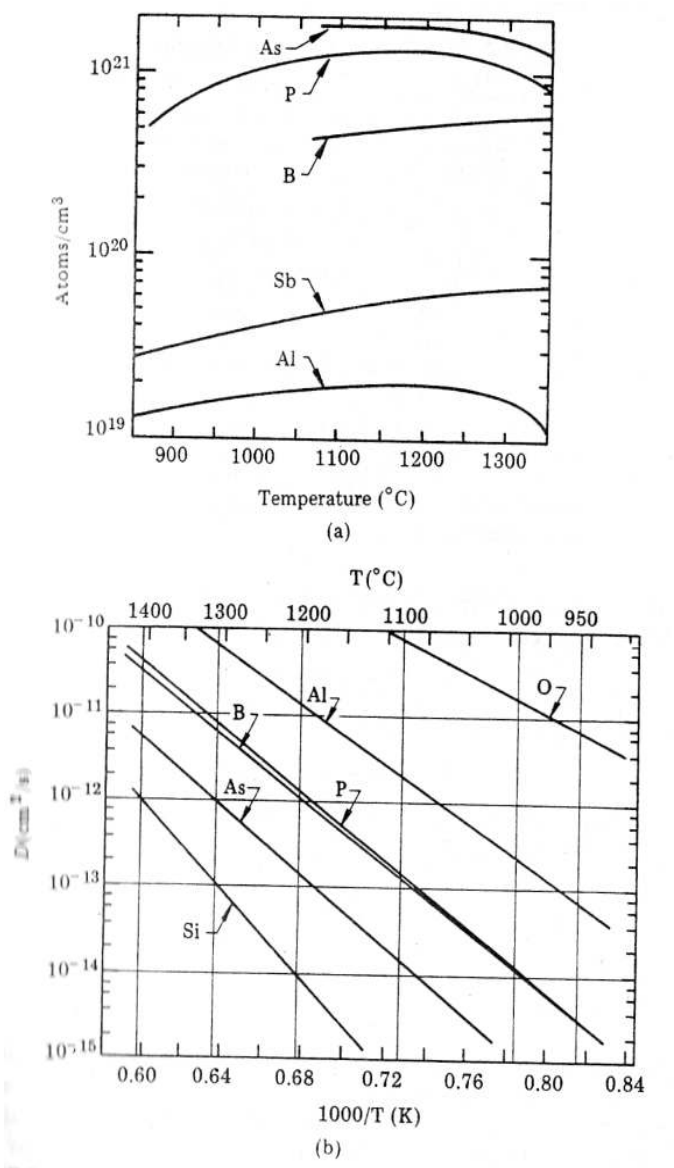


Figure 2.19 Solid solubility of atoms in Si (a). Diffusion coefficient of atoms in Si (b). (Mayer & Lau, 1998).

The predeposition step is typically performed by placing the Si wafers in a furnace with flowing inert gas that carries the desired impurities. The temperature is usually between 800 and 1200°C. The impurities are introduced into the ambient from either a solid or a liquid source. The surface concentration C_s of impurity during predeposition is kept constant are pertinent boundary conditions. Figure 2.19 shows solid solubility of atoms in Si and diffusion coefficient of dopant atoms in Si. The predeposition step gives a constant impurity concentration at the surface. This surface concentration, which often equals the solid solubility of the impurity, may be

too high for device applications. The impurities introduced by the predeposition step can be redistributed deeper in the substrate to lower the concentrations by a drive-in step.

The diffusion of ionized impurities may be enhanced by the presence of an electric field. An electric field sometimes may be generated internally under high-dopant-concentration conditions. Let us consider the diffusion of an n-type dopant into Si with a high surface concentration. At the diffusion temperature, the impurities are fully ionized and we assume that the free electrons obtained from the dopants, *n,* is larger than n_i *(*$n > n_i$ the extrinsic condition). The electrons have much higher mobility than that of the impurity atoms and tend to out run the diffusing atoms, thus creating an electric field between the electrons and the positively charged impurity atoms.

2.9.1 Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a versatile process suitable for the manufacturing of coatings, powders, fibers, and monolithic components. With CVD, it is possible to produce most metals, many non-metallic elements such as carbon and silicon as well as a large number of compounds including carbides, nitrides, oxides, intermetallics and many others. The principle scheme of CVD furnace is shown in Figure 2.20. This technology is now an essential factor in the manufacture of semiconductors and other electronic components, in the coating of tools, bearings, and other wear-resistant parts and in many optical, optoelectronic and corrosion applications.

Chemical vapor deposition may be defined as the deposition of a solid on a heated surface from a chemical reaction in the vapor phase. It belongs to the class of vapor-transfer processes which is atomistic in nature, that is the deposition species are atoms or molecules or a combination of these. Beside CVD, they include various physical-vapor-deposition processes (PVD) such as evaporation, sputtering, molecular- beam epitaxy, and ion plating.

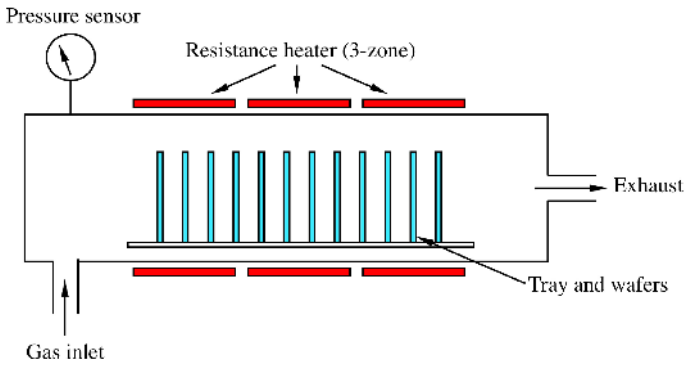


Figure 2.20 Principle scheme of CVD furnace

CVD has several important advantages which make it the preferred process in many cases. These can be summarized as follows:

- It is not restricted to a line-of-sight deposition which is a general characteristic of sputtering, evaporation and other PVD processes. As such, CVD has high throwing power. Deep recesses, holes, and other difficult three-dimensional configurations can usually be coated with relative ease. For instance, integrated circuit via holes with an aspect ratio of 10:1 can be completely filled with CVD tungsten.

- The deposition rate is high and thick coatings can be readily obtained (in some cases centimeters thick) and the process is generally competitive and, in some cases, more economical than the PVD processes.

- CVD equipment does not normally require ultra high vacuum and generally can be adapted to many process variations. Its flexibility is such that it allows many changes in composition during deposition and the co-deposition of elements or compounds is readily achieved.

CVD however is not the universal coating panacea. It has several disadvantages, a major one being that it is most versatile at temperatures of 600°C and above; many substrates are not thermally stable at these temperatures. However, the development

of plasma-CVD and metal-organic CVD partially offsets this problem. Another disadvantage is the requirement of having chemical precursors (the starter materials) with high vapor pressure which are often hazardous and at times extremely toxic. The by-products of the CVD reactions are also toxic and corrosive and must be neutralized, which may be a costly operation.

CVD is a versatile and dynamic technology which is constantly expanding and improving as witnessed by the recent developments in metal-organic CVD, plasma CVD, and many others. As the technology is expanding, so is the scope of its applications. This expansion is the direct result of a large research effort carried out by many workers in universities, government laboratories and industry (especially the semiconductor industry). The outlook is one of constant changes as new designs, new products and new materials are continuously being introduced.

Two major areas of application of CVD have rapidly developed in the last twenty years or so, namely in the semiconductor industry and in the so-called metallurgical-coating industry which includes cutting-tool fabrication. CVD technology is particularly important in the production of semiconductors and related electronic components. It is by far the most important area of CVD and is estimated to comprise three-quarters of all CVD production.

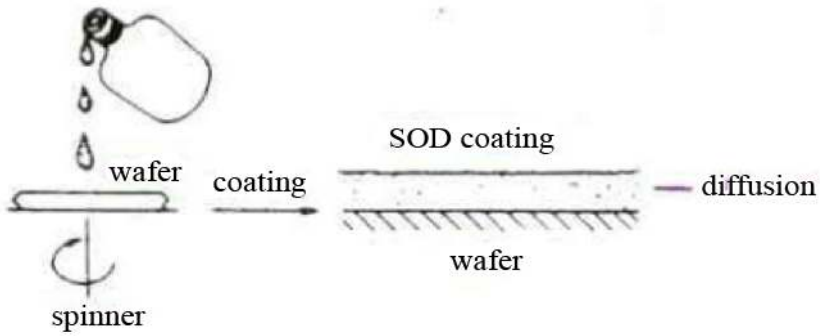


Figure 2.21 Principle of spin-on doping process

In CVD process, doping can be performed to form n- and p-type semiconducting materials. "Spin-on Doping Process" is one of them. In this process, $POCl_3$ bubbling

system is used in the commercial production way of solar cell industry. The alternative way of using liquid with bubbling system or gas for doping in CVD is spin-on doping method. In this method, liquid dopant is coated on the material surface by spin coater, afterwards materials are placed into the CVD machine to dope coated material into the substrate. The principle of spin-on doping process is shown in Figure 2.21.

CHAPTER THREE
EXPERIMENTAL

3.1 Purpose

The main purpose of this thesis is to form n- and p-type silicon wafers from intrinsic single crystal silicon wafers with using phosphorus and boron compounds, respectively. In addition to the use of commercial wafers, wafers are prepared from ingots that we produced. This process is one of the secondary goals of this thesis. Ingot slicing, lapping and polishing operations were carried out to prepare the wafer, respectively. Solar cell production was selected as an application part of this thesis. Since this thesis was prepared with studies scope of "The Manufacture of Integrated Renewable Energy Systems and Application of Transport Vehicles" project supported from IZ-KA (Izmir Development Agency), great attention has been paid to the application part and it was studied for implementation.

3.2 Materials

The main material of this thesis is silicon and its single crystal structure with wafer shape. All chemical components are given in Table 3.1 with their usage area.

Table 3.1 Components that was used in this thesis

Type	Chemical	Formula
Czochralski Process	Polycrsytalline Silicon Chunks	-
	Ar gas	-
Slicing	Boron oil	-
Lapping	Colloidal Alumina Powder + DI-Water	-
Polishing	Colloidal Cerium Powder + DI-Water	-
	Colloidal Silica Powder + DI-Water	-
Texturing	Potassium hydroxide	KOH
	Sodium hydroxide	NaOH
CVD	Phosphoryl chloride	$POCl_3$
	Boron Nitride	BN
PVD	Ag, Al & TiO_2 Target	-

3.3 Production of Semiconductors and Solar Cell

Production flow chart for production of semiconductors and solar cell is given in Figure 3.1. Studies have progressed from the two branches.

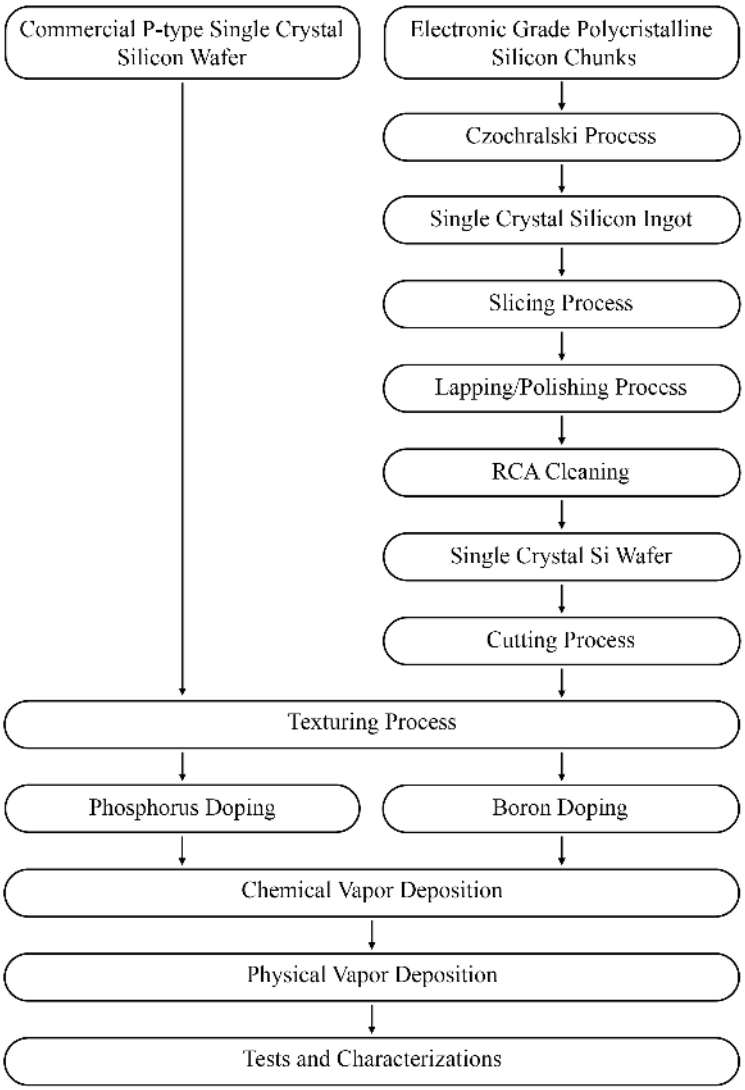


Figure 3.1 Flow chart of production of semiconductors and solar cell

Electronic grade polycrystalline silicon chunks were supplied in 5 kg packets in commercial way. Single crystal Si ingot was produced using PVA Tepla Czochralski Equipment. In terms of the importance of the IZ-KA (Izmir Development Agency) Project, p-type (100) oriented Si wafers were supplied in commercial way and the other branch of studies was engendered. Wafers were generated by slicing ingot in

STX 1202 Precision Slicing Machine, afterwards lapping and polishing process was done using Logitech Lapping/Polishing Machine to be ready to use. Both commercial and produced wafers were cut using Logitech Cutting Machine to use in experimental studies in 1 x 1 cm^2 and 2 x 2 cm^2. The first step of the application part of thesis was texturing process and it was performed. N-layer was generated on the p-type Si wafer by phosphorus doping and the basic structure of the solar cell was taken place by generating p-n junction between p- and n-layer. On the other hand, p-type structure forming studies were generated by doping boron on the pure Si wafer. All doping processes were performed in 1st Nano EasyTube 101 CVD furnace. Ag and Al layers were coated on the front and back surfaces of the wafer, respectively, to use as contact by PVD equipment.

3.3.1 Czochralski Process

Single crystal silicon ingot production was performed by PVA Tepla Czochralski Single Crystal Ingot Growth Machine located in Dokuz Eylul University (DEU) Center for Production and Application of Electronic Materials (EMUM). Working principle of this machine is based on that; desired orientated seed crystal was dipped into the molten polycrystalline silicon liquid that is slightly above the melting temperature in the quartz crucible, and afterwards the seed crystal was hoisted with a determined pull and slew speed to ensure the forming the same orientated structure of the particles around the seed crystal.

5 kg polycrystalline silicon chunks were loaded into the system for a production. The melting temperature was set at 1429 °C and when the system was reached the specified temperature, the seed crystal was hoisted with 1,1 mm/min pull speed and 10/10 rotation/min. Flow rate of the Ar gas was set to 25 L/min during process. Single crystal ingot production was taken approximately 19 hours, ingot with 200 mm length and 90 mm width was produced at the end of process that was shown in Figure 3.2.

Figure 3.2 Czochralski single crystal ingot growth machine and produced ingot

3.3.2 Slicing Process

Ingot slicing process was carried out by using STX 1202 Precision Slicing Machine with a 150 m long steel wire supported with diamond particles. Boron oil was used as coolant and lubricant. Slicing was performed by moving wire in the x and y axes with determined speed. Optimal working values were found by parameter studies. Slicing feed ratio were changed 1 mm/min, 2 mm/min and 3 mm/min while wire feed speed was kept constant. As a result, 2 mm/min slicing feed rate and 5 m/s wire speed were determined as an optimum parameter. Slicing machine and sliced wafers were shown in Figure 3.3.

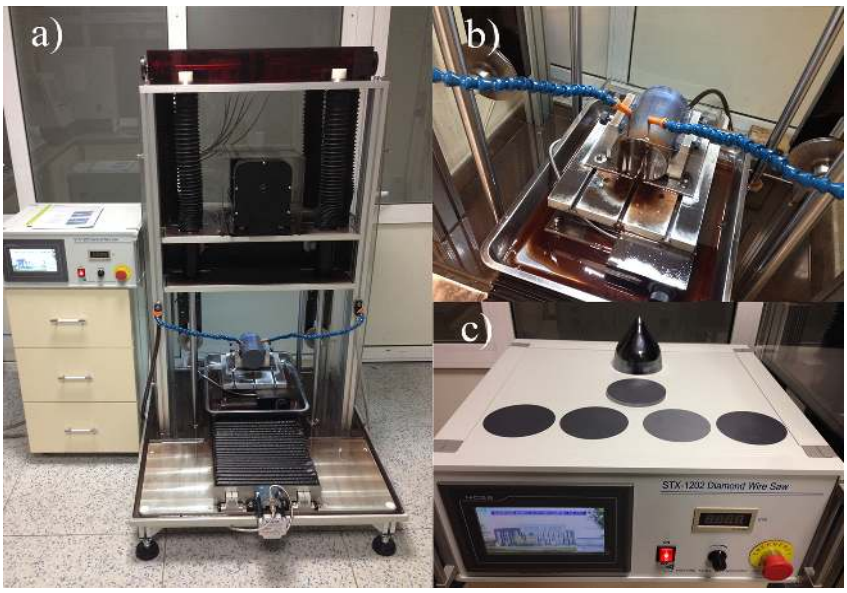


Figure 3.3 STX 1202 precision slicing machine

3.3.3 Lapping and Polishing Processess

Lapping and polishing processess were performed by using Logitech Lapping and Polishing Machine. Wafers must be fixed on the glass substrate to subject to lapping, polishing and cutting process. For this purpose, wafer was bonded by polymer binder on the glass surface, a weight was placed onto the materials for providing a strong adhesion and avoidance of air space between glass and wafer. This machine and its working principle was given in Figure 3.4.

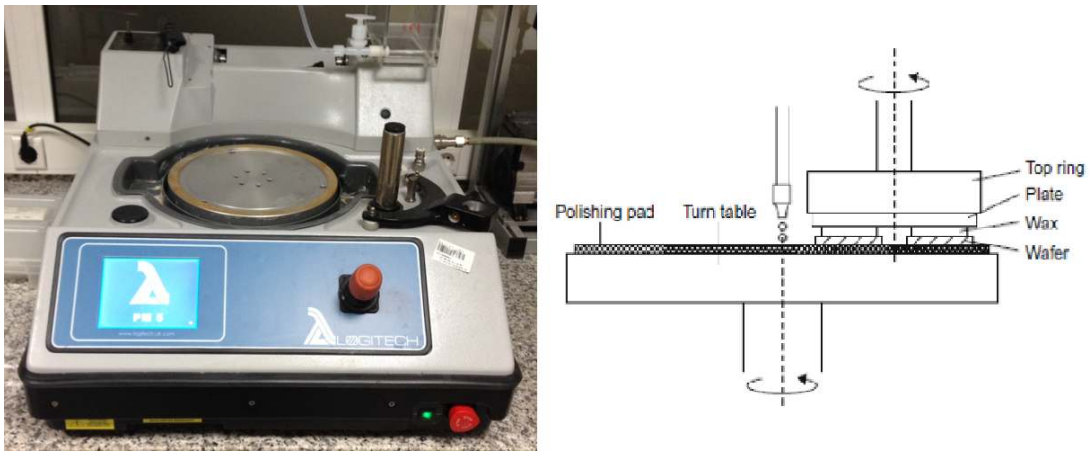


Figure 3.4 Logitech lapping and polishing machine and working principle

Wafer's surface to be polished was placed on the rotating iron drum. Roughness on the surface of the material was removed and obtained the desired smooth surface through incoming lapping and polishing solution. Alumina (Al_2O_3) powder (9 µm) was mixed with DI-water in 1/10 ratio and this mixture was used for rough lapping. This step was taken 1 hour with 45 rpm speed. For precision lapping, ceria (CeO_2) powder (3 µm) was mixed with DI-water in 1/10 ratio. And this step was taken same time with same rpm speed with previous step. The difference from the others of polishing step was using velvet pad instead of iron drum. Polishing process was performed using silica (SiO_2) suspension (40 nm) and taken 30 min with 30 rpm speed.

3.3.4 Cutting Process

Polished Si wafer was cut 2 cm x 2 cm in size for use in experimental studies by using Logitech Cutting Machine that were shown in Figure 3.5. Cutting Disk Rotate Speed and Sample Feed Speed were determined 2300 rpm and 0,25 mm/sec, respectively. Wafer was placed on the cutting table and a rotating disk cut the wafer into required pieces by moving on the wafer surface. Afterwards table was rotated 90° and the process was repeated. As a result, wafer was cut into square pieces.

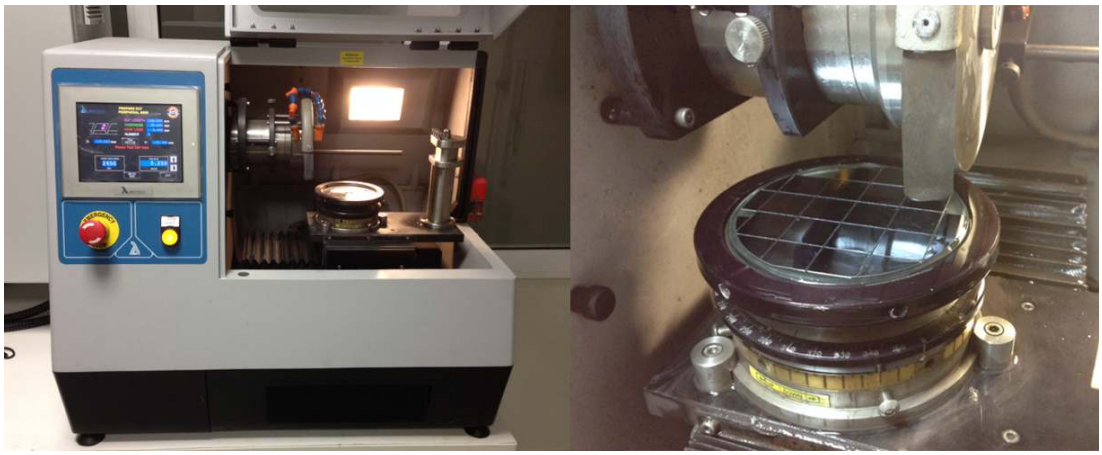


Figure 3.5 Logitech cutting machine and photograph of cutting wafer

3.3.5 Texturing Process

The aim of texturing process is to avoid reflection with the same angle of photons come from the sun and to ensure that reflected photons must move forward towards to the material surface again whereby to create square-based pyramidal structures on the wafer surface.

In the light of this information, literature researches were generated and it was found that NAOH, IPA and DI-water solution could be used to form create square-based pyramidal structures on the wafer surface by searching "Fabrication of Crystalline Silicon Solar Cell with Emitter Diffusion, SiN_x Surface Passivation and Screen Printing of Electrode" article published by S. M. Iftiquar et al. A solution included wt. 2% NaOH, wt. 6% IPA and wt. 92% DI-water was prepared by stirring

in a magnetic stirrer for 5 min. Afterwards the solution was heated to 80 °C and four piece of wafers were placed inside. Samples were taken after 20, 30, 40 and 50 min. to observe the effect of process time on the reflection.

3.3.6 Doping Process

3.3.6.1 Boron Doping

Boron is used to make intrinsic silicon p-type semiconductor. As described before, it was focused on phosphorus doping into the p-type silicon rather than doping of boron into the pure silicon. To product p-type Si semiconductor, the recipe that is taken from CVD firm, was applied using BN boron source. The details of this process was given in Table 3.2

Table 3.2 Procedure of the doping process for boron

Step	Operation	Time
1	Close furnace & purge	05 min
2	Heat to 400 °C	05 min
3	Ramp to 1050 ^{o}C in nitrogen and oxygen	01:05 h
4	Stabilize at 1050 ^{o}C	05 min
5	Inject – Growth in nitrogen	01:00 h
6	Ramp to 800 ^{o}C in oxygen	45 min
7	Purge nitrogen, cool 300 ^{o}C	03 min
8	Purge nitrogen, cool 200 ^{o}C	03 min
9	Ready to unload	-

3.3.6.2 Phosphorus Doping

Due to the high importance of the application part of studies, phosphorous doping process was performed on the p-type silicon wafer to form p-n junction area and also to generate the basic structure of the solar cell. In the light of literature researches, it was decided to use $POCl_3$ in a liquid form as a phosphorus source (Lee, Ho, Syu, Lai, & Yu, 2011). In the commercial solar cell production, $POCl_3$ is also used in CVD furnace with bubbling system. Based on “17.9% Efficiency Silicon Solar Cells

by Using Spin-On Films Processes" article published by Y. Lee et al, $POCl_3$ liquid phosphorus source was coated on the wafers surface using spin coater with 6000 rpm for 20 sec. Diffusion process was begun by placing coated wafers inside of the CVD furnace with preheating step at 200°C for 5 min and 400°C for 10 min. Then diffusion step was performed at 900°C for the range of 2-10 min. EasyTube101 CVD furnace and wafer placement was shown in Figure 3.6. After this process, wafers were cleaned and removed oxide layer by waiting in 10% HF solution for 1 min.

Figure 3.6 CVD furnace and wafer placement

3.3.7 Anti-Reflection Coating (ARC)

The one of the important problem of the solar cell is that incoming photons reflect back. Because this causes the decline of the energy that be transferred from the photons come from sun, efficiency will also decrease. Texturing and anti-reflection coating (ARC) are anti-reflection studies. TiO_2 ARC is divided into two parts in basically, using magnetron sputtering and using sol-gel method. In magnetron sputtering process, electrons were deposited on the base material surface by removing them from the target material surface in vacuum ambient with Ar gas and as a result, ARC layer is formed in 80 nm thickness. For this process, NanoVak NVTH-350 PVD Equipment was used with magnetron sputtering feature shown in Figure 3.7.

Figure 3.7 NanoVak NVTH-350 PVD equipment and some experiments

3.3.8 Metallization

The metallization process is performed to obtain electrically contacts from the produced solar cells. The 99.5% pure silver and aluminium target materials were used in order to get contact from front and back side of wafer, respectively. Nanovak NVTH-350 PVD Equipment and some experiments are shown in Figure 3.7. The important point of this step is coating very narrow metal as possible while getting contact from front side. Thick coating decreases the efficiency of solar cells because it has the effect of shading. Cleaned silicon wafers were placed to sample holder in PVD equipment. Prior to coating process, the chamber of the system was vacuumed under $3x10^{-6}$ Torr. After then, thin film that its thickness is 70 nm was produced on the cleaned silicon wafers using the Ag and Al target at 30 A.

3.4 Characterization of Semiconductors and Solar Cell

3.4.1 X-Ray Diffractometer (XRD)

XRD is an important technique to determine the crystalline phases of materials and based on Bragg's Law that equation shown below.

$$n.\lambda = 2.d.sin\theta \tag{3.1}$$

n is the diffraction order which is an integer, λ is the the wavelength of X-Ray that is known by knowing K_α value of material used for X-Ray source which especially is used Cu K_α. θ is an angle between indecent – diffracted beams and atomic planes. All this values and Bragg's Law is denoted in Figure 3.8.

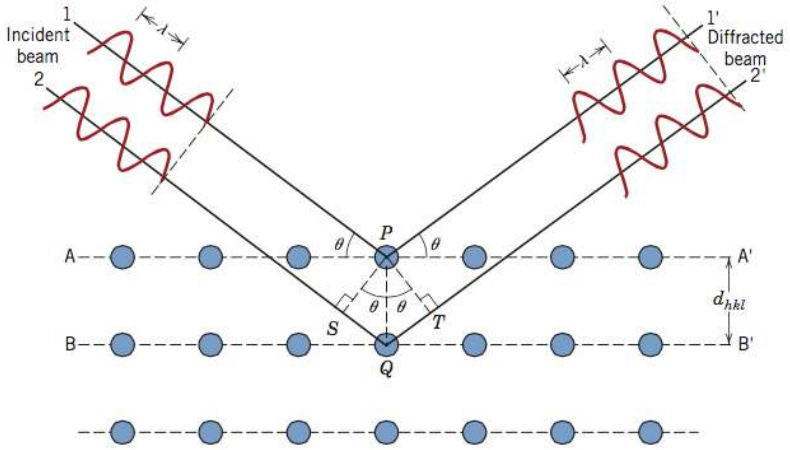


Figure 3.8 Diffraction of x-rays by planes of atoms (A–A` and B–B`)

In this study, X-Ray Diffractometer was used to identify whether produced silicon ingot was single crystal or not. Pure silicon wafer, p-type silicon wafer and n-type silicon wafer were analysed by means of XRD with a grazing angle attachment and an incident angle of 1° (Thermo-Scientific, ARL-K_α). X-Ray radiation of Cu-K_α was set at 45 kV and 44 mA with a scanning speed of 2°/min.

3.4.2 Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) is one of the most common analytical methods to examine surface morphology of the solid-state specimen. In SEM, a tiny high-energy electron beam is scanned across the sample surface. Series of radiations can be produced in terms of the interaction between the electron beam and the sample. Normally, two types of radiation are utilized for image formation: primary backscattered electrons and secondary electrons. Backscattered electrons reveal the compositional and topographical information of the specimen. The secondary electron images produce a depth of field which shows the surface topography. The

signal modulation of the two types of radiation is viewed as images in the cathode ray tube (CRT) and provides the morphology, surface topology and composition of the specimen surface. In this study, the surfaces of pure, p- and n-type silicon wafer and texturing wafer were examined by using JEOL JSM-6060 instrument operating at an accelerating voltage of 20 kV with several magnifications.

3.4.3 X-Ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) is a quantitative spectroscopic technique that measures the elemental composition, empirical formula, chemical state and electronic state of the elements that exist within a material. XPS spectra are obtained by irradiating a material with a beam of X-rays whilst simultaneously measuring the kinetic energy and number of electrons that escape from the top 1 to 10 nm of the material being analysed. XPS requires ultra-high vacuum (UHV) conditions. It can be also used to analyse the surface chemistry of a material in its "as received" state, or after some treatment, for instance: fracturing, cutting or scraping in air or UHV to expose the bulk chemistry, ion beam etching to clean off some of the surface contamination, exposure to heat to study the changes due to heating, exposure to reactive gases or solutions, exposure to ion beam implant, exposure to ultraviolet light. XPS detects all elements with an atomic number (Z) of 3 (lithium) and above. It cannot detect hydrogen and helium, because the diameter of these orbitals is so small, reducing the catch probability to almost zero. It is routinely used to analyse all solid materials. In the present study, produced samples were analysed in elemental manner using XPS (Thermo-Scientific, Al-K_{α}, in DEU-EMUM).

3.4.4 Surface Profilometer

Surface Profilometer is one of the surface characterization devices which gives the surface roughness of materials and that is very important to identify whether processes, slicing, lapping, polishing etc., were completed successfully. A probe (tracing probe) moves across predetermined surface of the specimen and give cross-

section surface profile. There are few roughness parameters like R_a, R_q, R_v, R_p, R_t, R_{sk}, R_{ku}, R_z, and most important ones for slicing, lapping and polishing are R_z and R_t.

These parameters are important for lapping and polishing is the following;

- Mean Roughness Height/Depth (R_z): The mean of roughness heights/depths at each sample length.
- Maximum Roughness (R_{zmax}): The largest of five roughness heights/depths at each sample length.
- Peak-to-Valley Roughness (R_t): The largest peak-to-valley in the entire profile.

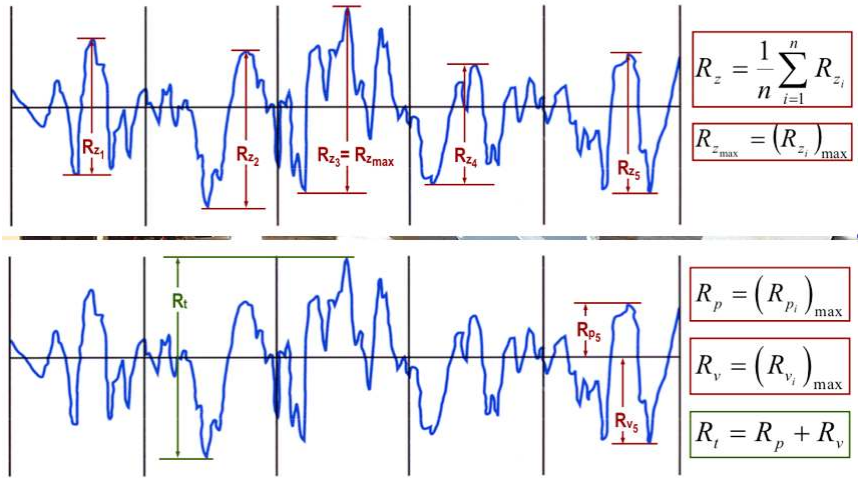


Figure 3.9 Basic of surface profilometer parameters

R_z is more sensitive than R_a to changes on the surface as the maximum profile heights are examined rather than average of peak and valleys. In addition, R_{zmax} is useful for surfaces where a single defect is not permissible. Wafer surface's profiles were investigated with Mitutoyo SJ-301 surface profilometer.

3.4.5 UV-Vis Spectroscopy

UV-Vis Spectroscopy was used to identify reflection characteristic of silicon wafers and for comparison of before & after texturing, before & after anti-reflection

coating and base material. The logic of the system is that a light in predetermined wavelengths is sent to material surface and reflection light from the surface is collected and measured by sensor, percent reflectance value is given as a result. Measurements were performed by Thermo-Scientific UV-Vis equipment with the range of 230 – 810 nm wavelengths to analyse reflection characteristic in visible light region.

3.4.6 I-V Characterization

I-V Characterization has a great importance to identify semiconductor electrical properties of silicon wafer and its application - solar cell. In solar cell applications, it is known that when light source is used during the test, I-V curve shifts downward; while solar cell acts as a large diode without light shown in Figure 3.10. The more photon energy comes to sample surface, the more shifts occurs and the more energy generates.

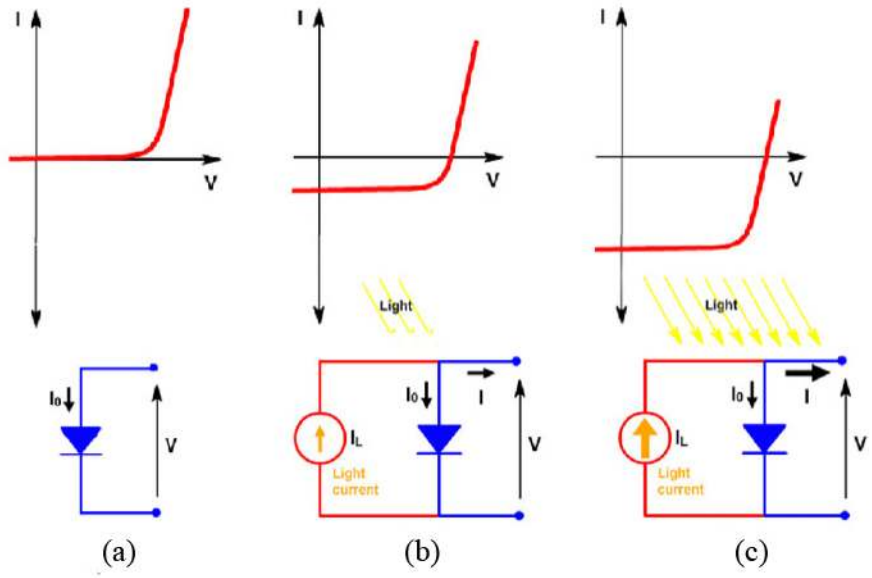


Figure 3.10 (a) Without illumination (b) When light shines on the cell, the IV curve shifts as the cell begins to generate power. (c) The greater the light intensity, the greater the amount of shift.

In order to achieve I-V characterization graphics, an assembly was established consisting of voltage source, electrical measuring table and a computer. On the electrical measuring table one probe touch rear side of sample while the other touch

front side; predetermined voltage range is sending on the sample and current values is obtained depending on incoming voltage. Keithley 2636B was used as a voltage source and setup is shown in Figure 3.11.

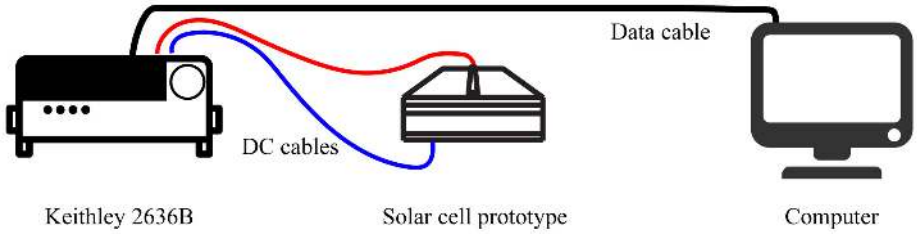


Figure 3.11 I-V measurement setup

CHAPTER FOUR
RESULTS AND DISCUSSION

4.1 Phase Analysis

4.1.1 Pure Silicon

One of the characterization studies of Si wafer prepared from the produced Si ingot was the analysis of phases present in the structure. It was performed by XRD analysis and the result was shown in Figure 4.1.

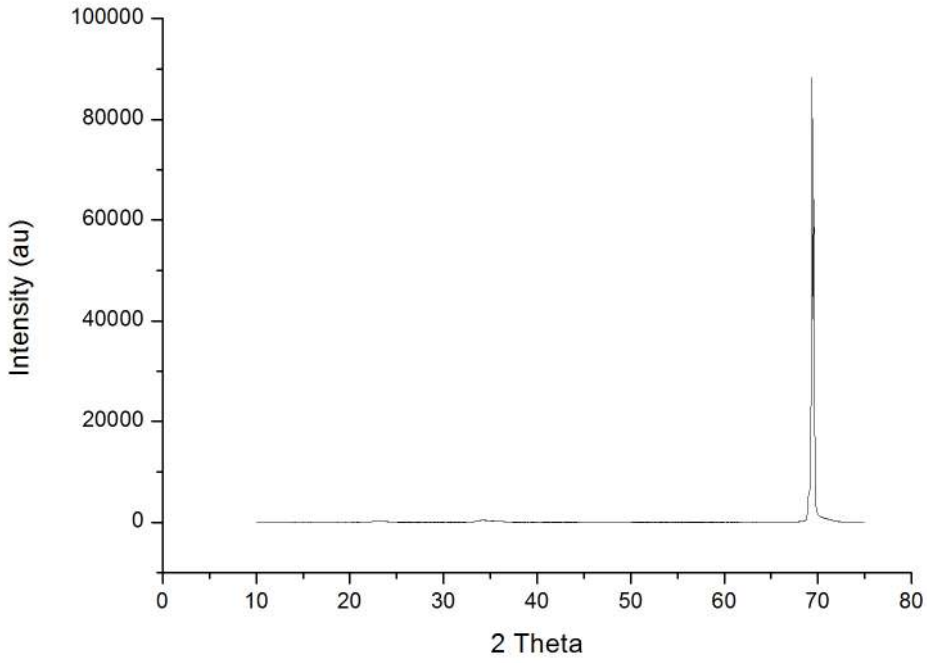


Figure 4.1 XRD pattern of pure Si wafer

In XRD pattern, it was shown that material gave only unique peak and the peak was depicted at 69.56°, corresponding to the crystal plane of (400). The (100) seed crystal was used when ingot was produced, thus this result confirmed that ingot was manufactured as a single crystal. This pattern was supported by the study reported by Rachwal (2010). The obtained result was in accordance with the results of SEM-EDS analysis.

4.1.2 Boron Doping

XRD pattern of the p-type Si wafer was illustrated in Figure 4.2. As was mentioned above, only single peak was determined at 69.46°, corresponding to the crystal plane of (400). Sudesh et al. (2009) approved this data in their experiment. Boron effect could not clearly seen from Figure 4.2, because the content is very low.

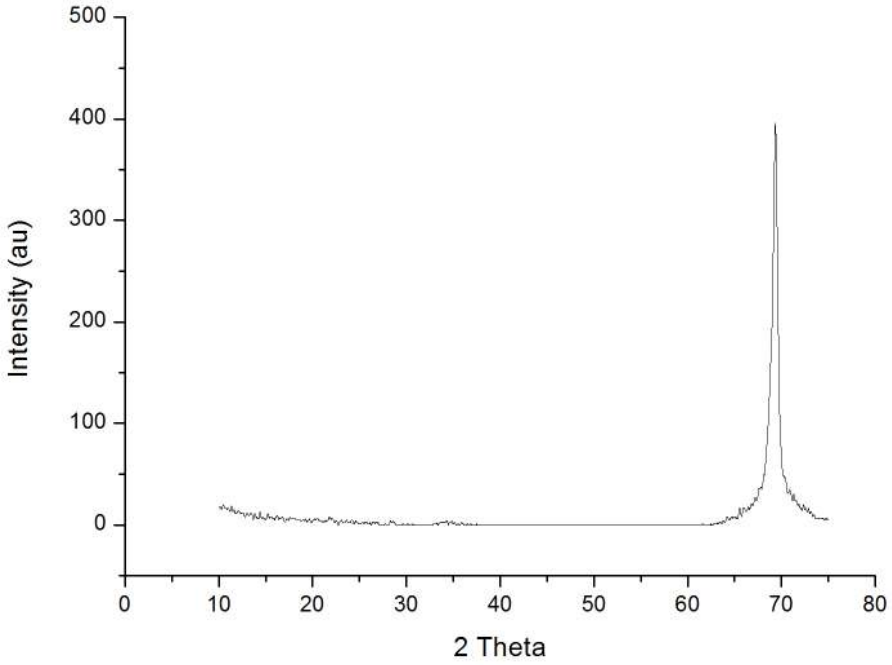


Figure 4.2 XRD pattern of p-type Si wafer

4.1.3 Phosphorus Doping

XRD result of n-type Si wafer was presented in Figure 4.3. Therefore, a single peak was observed specifically at 69.49°, corresponding to the crystal plane of (400). Phosphorous effect could not be obviously seen from Figure 4.3 due to the presence of small content in Si wafer. Result of XRD analysis had similarities with data reported by Aoudia et al. (2006).

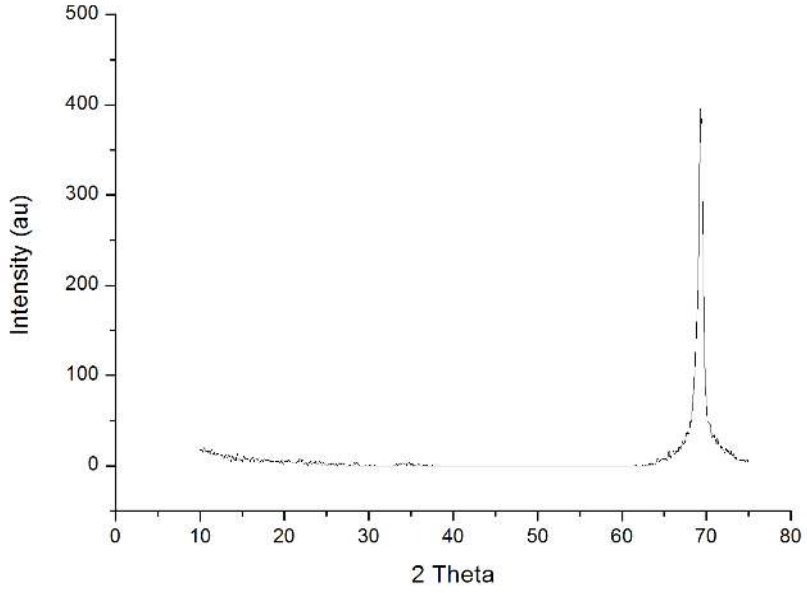


Figure 4.3 XRD pattern of n-type Si wafer

4.2 Microstructure

4.2.1 Pure Silicon

Microstructural characterization studies, Scanning Electron Microscopy (SEM) and Energy Dispersive Spectroscopy (EDS) analysis results of pure Si wafer were shown in Figures 4.4 and 4.5. Note that certain scratches on Si wafer were observed after polishing process.

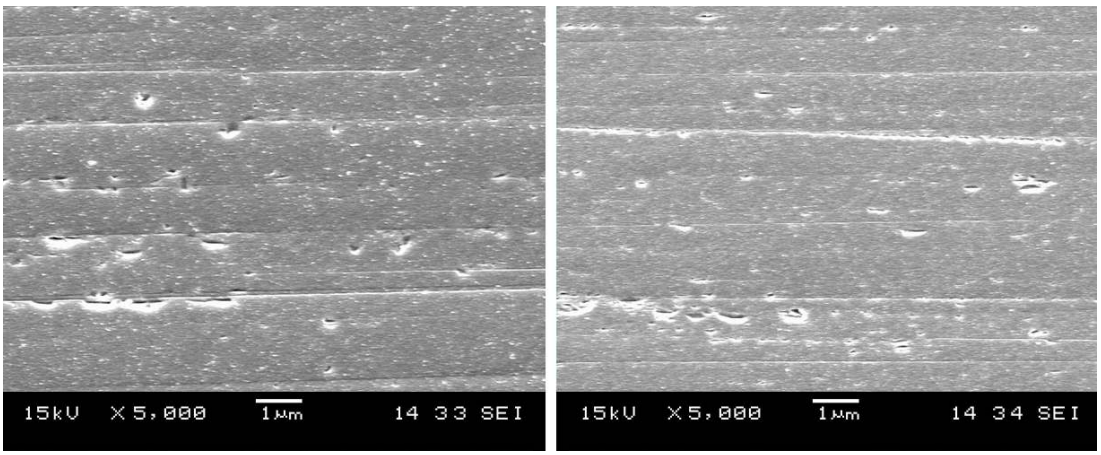


Figure 4.4 SEM images of pure silicon wafer

As a result of EDS analysis, Si and C were found in the structure shown in Figure 4.5. Carbon element shown in the EDS analysis was obtained from the carbon band used to bond silicon wafer sample to the support. Result of analysis showed that produced material contained just a single silicon element. We have a good agreement with a report of Chu (2009).

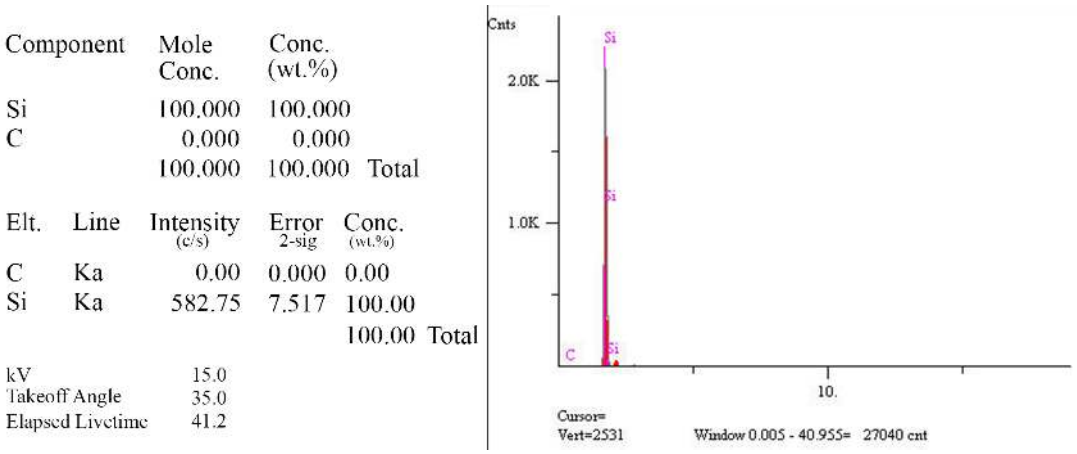


Figure 4.5 EDS result of pure silicon wafer

4.2.2 Boron Doping

Boron doping process was performed to produced pure silicon wafers. To investigate the microstructural features, SEM and EDS analysis were performed and results were displayed in Figures 4.6 and 4.7. Scratches and particles occurred during polishing process on the wafer surface was observed.

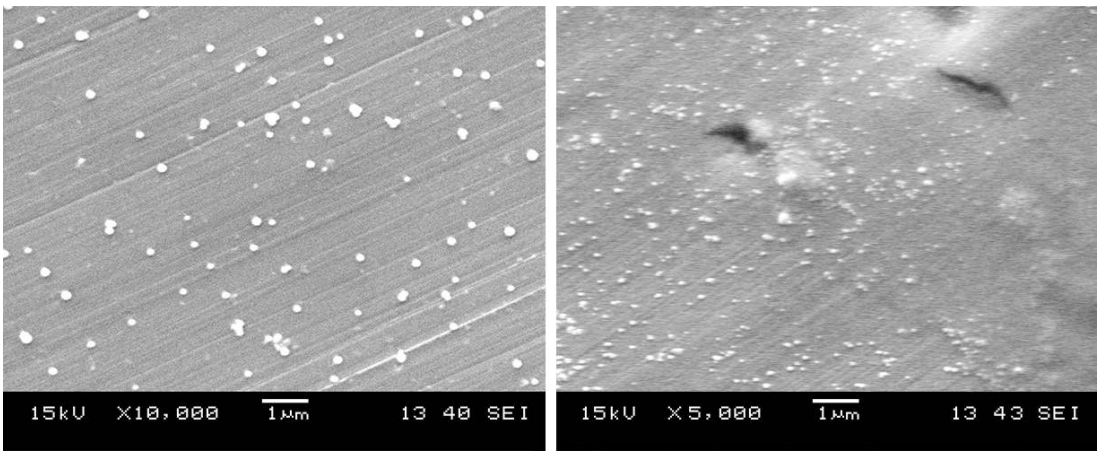
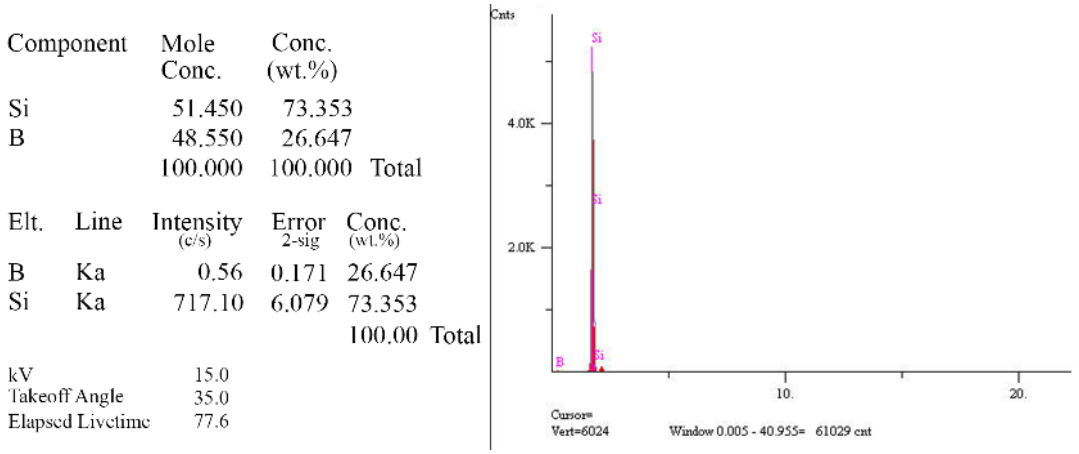


Figure 4.6 SEM images of p-type Si wafer

As a result, the boron element was detected in the structure by EDS analysis and was shown in Figure 4.7. This result was supported by XPS result shown in the next section.



Component	Mole Conc.	Conc. (wt.%)	
Si	51.450	73.353	
B	48.550	26.647	
	100.000	100.000	Total

Elt.	Line	Intensity (c/s)	Error 2-sig	Conc. (wt.%)	
B	Ka	0.56	0.171	26.647	
Si	Ka	717.10	6.079	73.353	
				100.00	Total

kV	15.0
Takeoff Angle	35.0
Elapsed Livetime	77.6

Figure 4.7 EDS result of p-type Si wafer

4.2.3 Phosphorus Doping

Phosphorus doping process was performed on the p-type silicon wafers and SEM results of p-n junction layer was shown in Figure 4.8. Secondary Ion Mass Spectrometry (SIMS) was used for determining the depth of diffusion and usually the SIMS results were given in publications. An alternative method was developed no SIMS equipment was reported in our university and cross-section SEM image of wafer should be taken to observe doping process. For this reason, wafers were moulded in bakelite mount perpendicularly. The images on the SEM analysis results were confirmed by observing the formation of the p-n junction layer shown in Figure 4.8. Contrast difference in BEC mode supported the results of SEM analysis that the doping process was carried out with success.

SEM results were reinforced with EDS analyses presented in Figure 4.9. Not only the determination of phosphorus element in EDS analysis was carried out, but also it was found that the structure contained higher phosphorus content on the surface compared to the inner regions (Figure 4.9a).

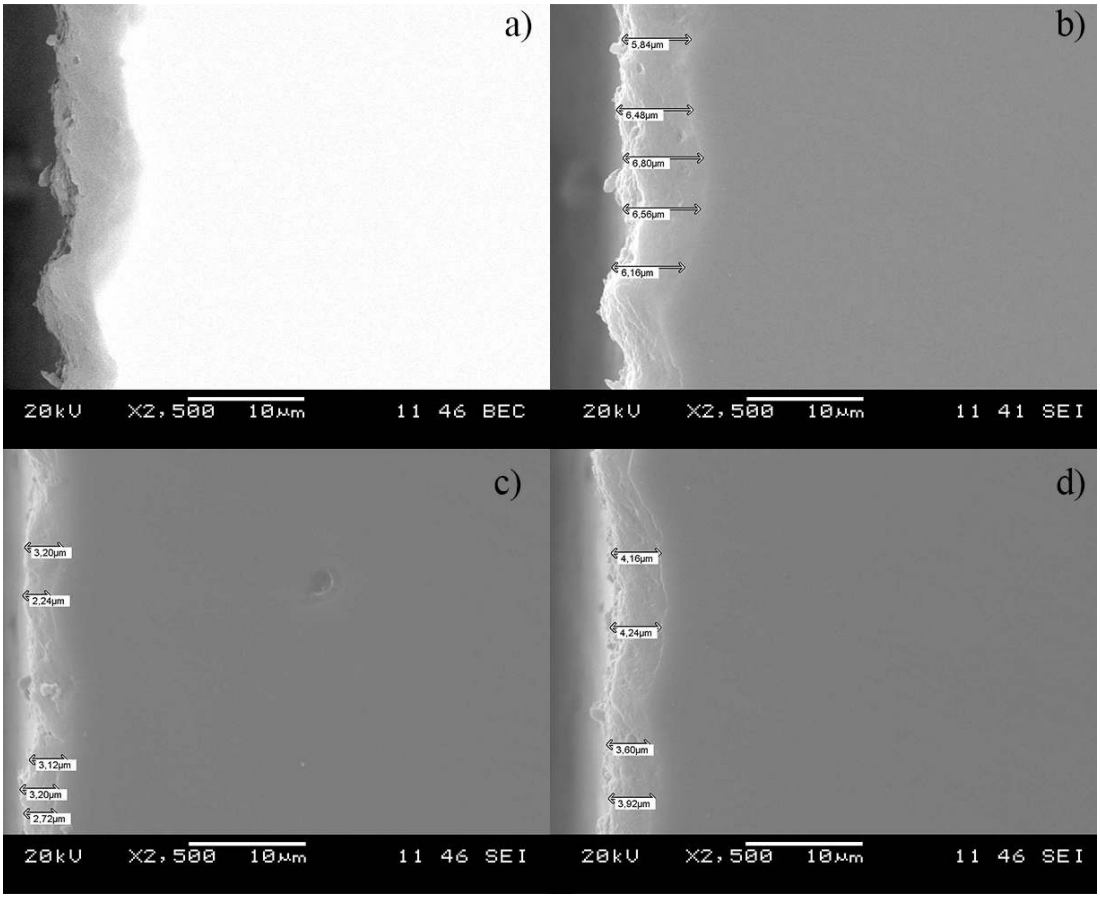
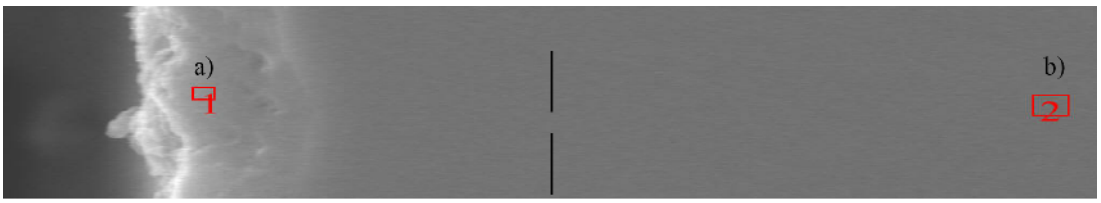


Figure 4.8 SEM images of produced p-n junction layer in the n-type/p-type Si wafer



Component	Mole Conc.	Conc. (wt.%)	
Si	99.116	99.026	
P	0.884	0.974	
	100.000	100.000	Total

Elt.	Line	Intensity (c/s)	Error 2-sig	Conc. (wt.%)	
Si	Ka	196.85	2.599	99.026	
P	Ka	0.59	0.153	0.974	
				100.00	Total

kV	20.0
Takeoff Angle	35.0
Elapsed Livetime	100.0

Component	Mole Conc.	Conc. (wt.%)	
Si	99.791	99.770	
P	0.209	0.230	
	100.000	100.000	Total

Elt.	Line	Intensity (c/s)	Error 2-sig	Conc. (wt.%)	
Si	Ka	740.68	5.443	99.770	
P	Ka	0.60	0.153	0.230	
				100.00	Total

kV	20.0
Takeoff Angle	35.0
Elapsed Livetime	100.0

Figure 4.9 EDS results of produced p-n junction layer in the n-type/p-type Si wafer

4.2.4 Texturing

SEM images were taken to analyse surface topography after texturing process. The aim is to create square based four sided pyramids reported by Iftiquar et al. (2012) and the images on the SEM analysis results were confirmed that similar structure were obtained shown in Figure 4.10. The better images could be taken by tilt mode. UV-Vis results supported the effect of the texturing surface on the reflection. It is clear from Figure 4.10 that nano or micro pyramids are formed on Si surface. Notably nano pyramids produced by texturing process does not reflect sun lights and also reflect less than micro pyramids.

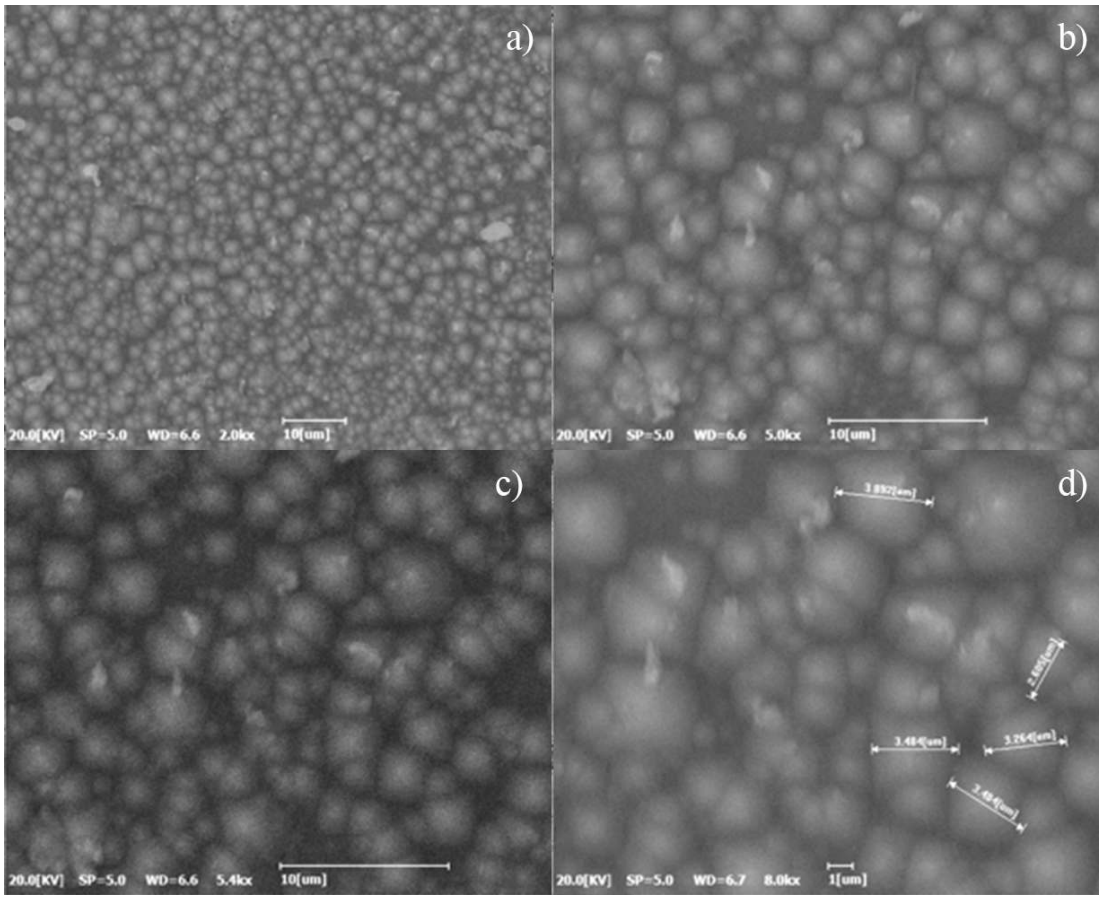


Figure 4.10 SEM images of texturing Si wafers

4.3 X-Ray Photoelectron Spectroscopy (XPS)

4.3.1 Pure Silicon

In the characterization studies carried out with produced Si wafer from Si ingot, phases analysis in structure was determined by XPS technique and the result was shown in Figure 4.11. Obtained elemental analysis values were shown in Table 4.1. Results supported the conclusion of SEM-EDS analysis. It should be keep in mind that, considering the elemental ID and amounts of elements, components other than Si were contaminations that came from lapping and polishing process.

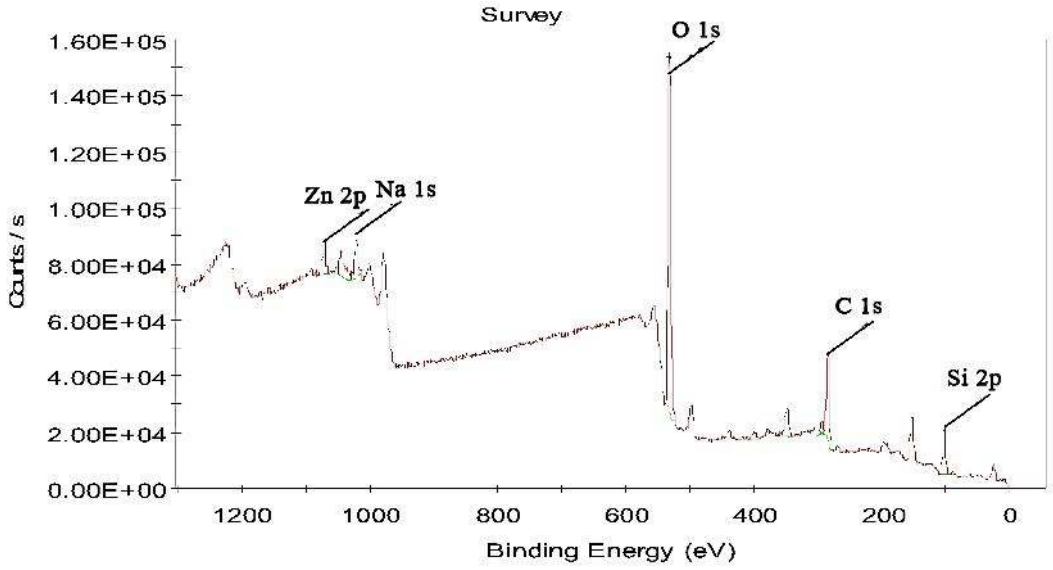


Figure 4.11 XPS results of pure Si wafer

Table 4.1 XPS elemental analysis values of pure Si wafer

Name	*Peak BE*	*At. %*
O 1s	532.17	43.21
C 1s	284.23	29.59
Si 2p	102.84	16.75
Zn 2p	1021.96	2.70
Na 1s	1071.84	2.33
Ca 2p	348.16	2.49
K 2p	294.11	0.87
N 1s	399.13	2.06

4.3.2 Boron Doping

XPS analysis results for p-type Si wafer were displayed in Figure 4.12 and obtained elemental analysis values were illustrated in Table 4.2. The results supported the results of SEM-EDS analysis. Considering elemental ID and amounts of elements, components other than Si and B were contaminations that came from lapping and polishing process.

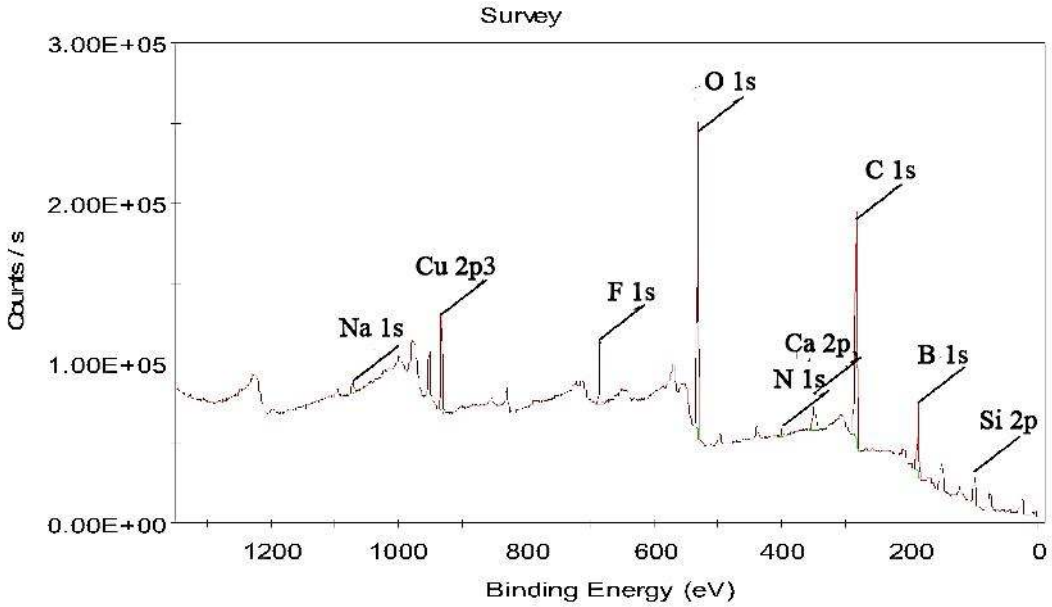


Figure 4.12 XPS analysis result of p-type Si wafer

Table 4.2 Elemental analysis values of p-type Si wafer

Name	*Peak BE*	*At. %*
O 1s	531.88	19.92
C 1s	284.38	40.60
Cu 2p3	932.34	1.49
F 1s	684.86	2.76
Si 2p	99.08	7.57
Ca 2p	347.54	1.79
N 1s	398.78	1.41
Na 1s	1071.40	0.61
B 1s	186.95	23.85

4.3.3 Phosphorus Doping

As a result of performed analysis, Phosphorus element has been identified using THERMO XPS equipment by performing ion etching for 5 min and 15 min. XPS analysis result was represented in Figure 4.13 and elemental analysis values were displayed in Table 4.3.

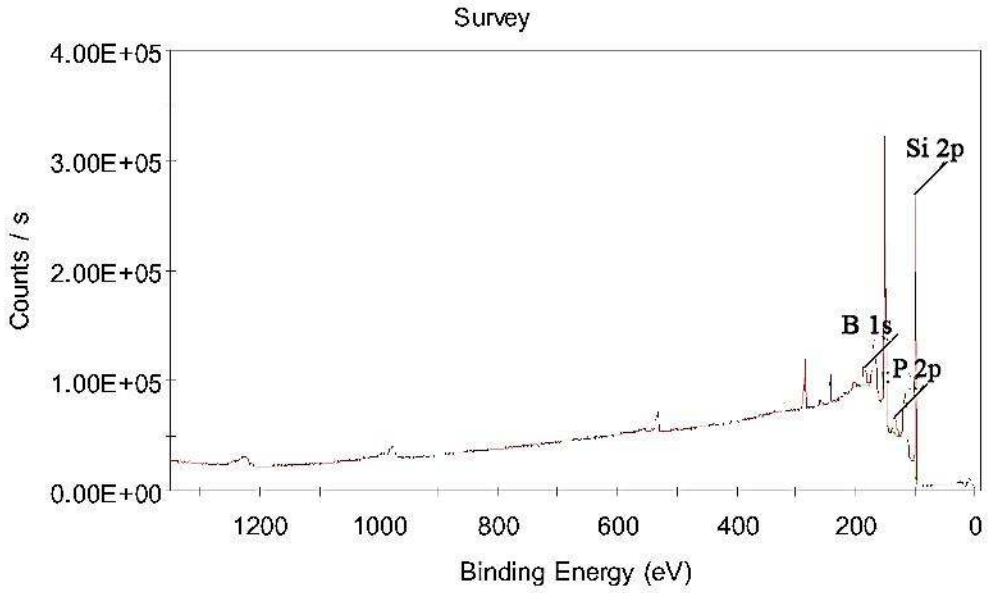


Figure 4.13 XPS analysis result of n-type/p-type Si wafer

Table 4.3 Elemental analysis values of n-type/p-type Si wafer

Name	Peak BE	At. %
Si 2p	99.83	67.45
B 1s	185.37	24.24
P 2p	134.06	8.31

4.4 Surface Profilometer

Surface roughness profile was procured by XP-2 Surface Profilometer to specify surface differences slicing, lapping and polishing. R_t and R_z values of the specimens were measured and also compared.

Three specimens were determined by slicing feed rate, 1 mm/min, 2 mm/min and 3 mm/min and these specimens were titled X1, X2 and X3, respectively. Entire slicing process was generated with 5 m/s wire speed. Lapping process parameters were given as 2 drops/sec abrasive solution feed speed (colloidal alumina solution in 9-micron particle size) and 45 rpm table rotation speed.

Slicing process takes time of 120 min for X1, 60 min for X2 and 40 min for X3. In order to compare them, the first surface roughness measurements were generated. The most frequent fluctuations and the less peak-to-valley heights were observed in X1 sample, there was an opposite situation in X3 sample, while X2 sample contained values between X1 and X3 shown in Figure 4.14.

Table 4.4 Slicing and lapping parameters

Process	Sample	Time (min)	Profilometer Result (μm)			
			R_t		R_z	
Slicing	X1	120	21.07		20.35	
	X2	60	31.80		27.80	
	X3	40	42.76		38.20	
			Flat	Non-Flat	Flat	Non-Flat
Lapping	X1	30	1.61	5.91	1.35	5.22
	X2	30	1.78	12.37	1.57	9.48
	X3	30	1.85	21.72	1.49	18.07
Lapping	X1	30	1.59		1.30	
	X2	30	1.73		1.52	
	X3	60	1.82		1.45	
Total Process Time (min)			X1		180	
			X2		**120**	
			X3		130	

The first lapping processes were performed for 30 min. When visual inspection was performed on the samples, flat and peak-to-valley surfaces was seen and that was shown in Figure 4.15. For this reason, it was decided that the second roughness measurement was generated on both flat and peak-to-valley surfaces.

The aim of the second lapping process was making completed flat surfaces on the samples. For this reason, process time was determined by visual inspection given Table 4.4. After all studies, process of X2 sample proved optimum values when compared to others.

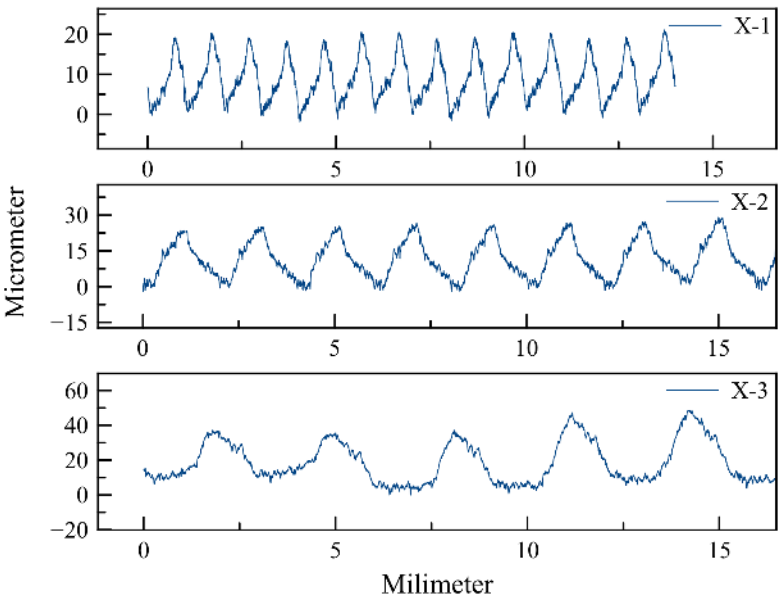


Figure 4.14 Comparison of X1, X2 and X3 samples after slicing process

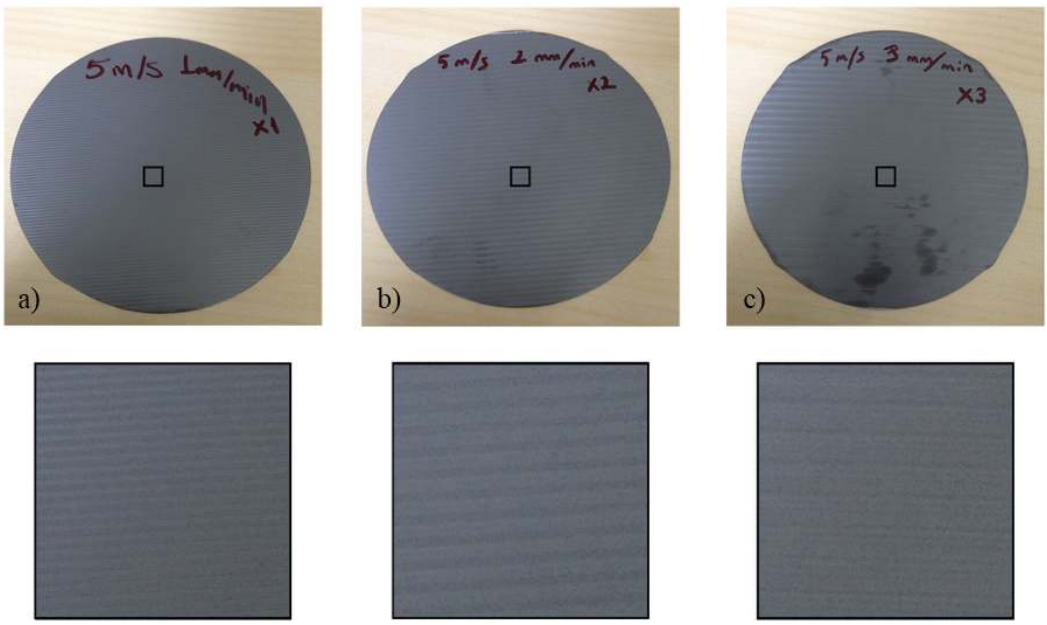


Figure 4.15 Visual inspection after 30 min lapping process.

4.5 UV-Vis Spectroscopy

The reflection of the upcoming photons from the material surface is an undesirable situation. Because of this reason, in solar cell applications, texturing and anti-reflection processes are carried out. In this thesis, texturing process was generated by NaOH solutions in different times and the comparisons were analysed by taking Reflectance (%) – Wavelength (nm) graphics using THERMO UV-Vis equipment.

The reflection was decreased with decreasing process time and better results were generated in 20 min process time (shown in red colour in Figure 4.16). In another study, p-type silicon wafer, solar cell without texturing and coating, texturing in 20 min and TiO_2 coating were compared and these values were shown in Figure 4.17. Base p-type Si wafer and solar cell without coating and texturing samples gave results very close to each other. Texturing with 2 wt.% NaOH solution in 20 min decreased reflection about 35% in range of 300 – 400 nm wavelength from approximately 62%. TiO_2 gave the best result near 550 nm with 2% reflection. The results had similarities with the results of Xi et al. (2004).

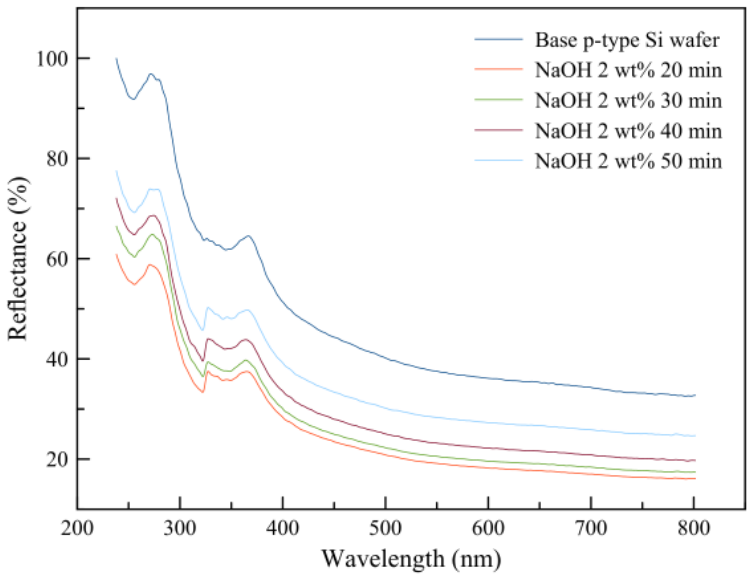


Figure 4.16 Comparison of the different process times of texturing process on the effect of reflection

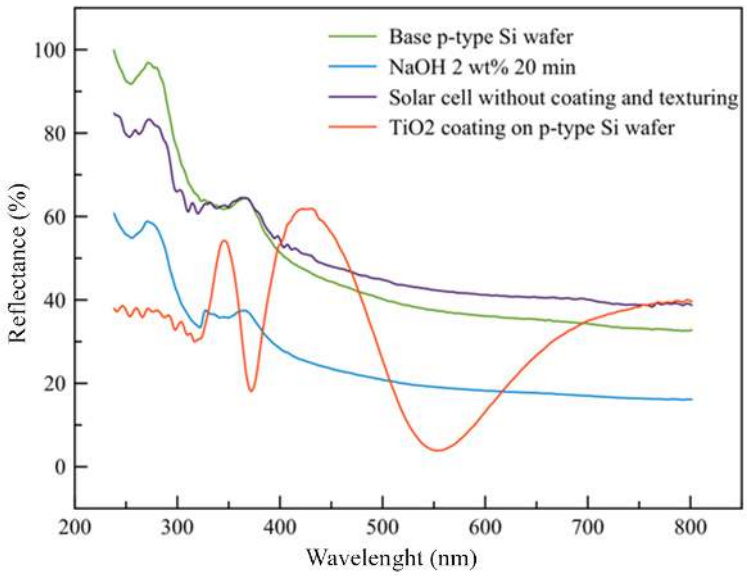


Figure 4.17 Comparison of based p-type Si wafer, texturing with NaOH, solar cell structure without coating and texturing and TiO_2 coating on p-type Si wafer on the effect of reflection

4.6 I-V Characteristic

4.6.1 Pure Silicon

To analyse electrical properties of the produced Si wafer from pure Si ingot, four-point probe technique was performed and result was shown in Figure 4.18. When the graphic of the current-voltage characteristic of the sample was evaluated, it was found that sample showed typical semiconductor characteristic.

4.6.2 Boron Doping

Result of four-point probe analysis for boron doping Si wafer was shown in Figure 4.19. The current sample gave typical semiconductor characteristics with reference of the data given below.

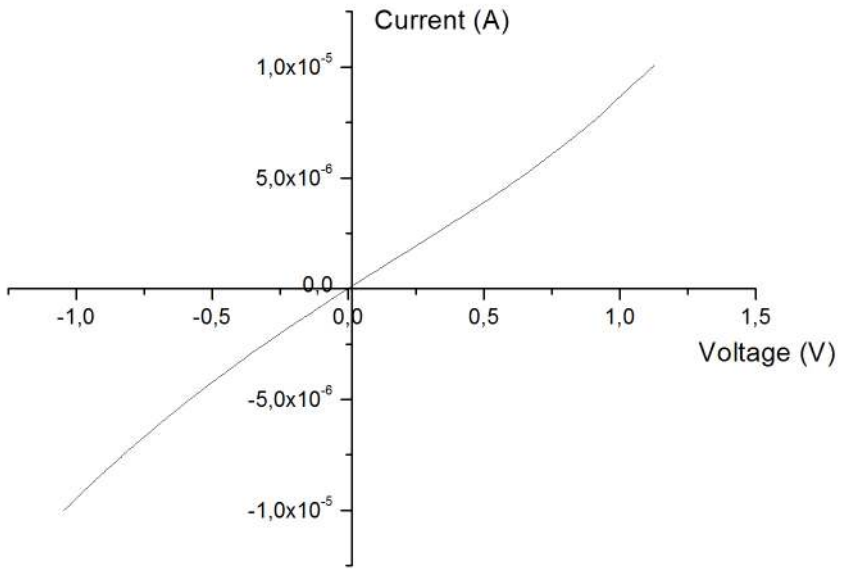


Figure 4.18 I-V characteristic of pure Si wafer

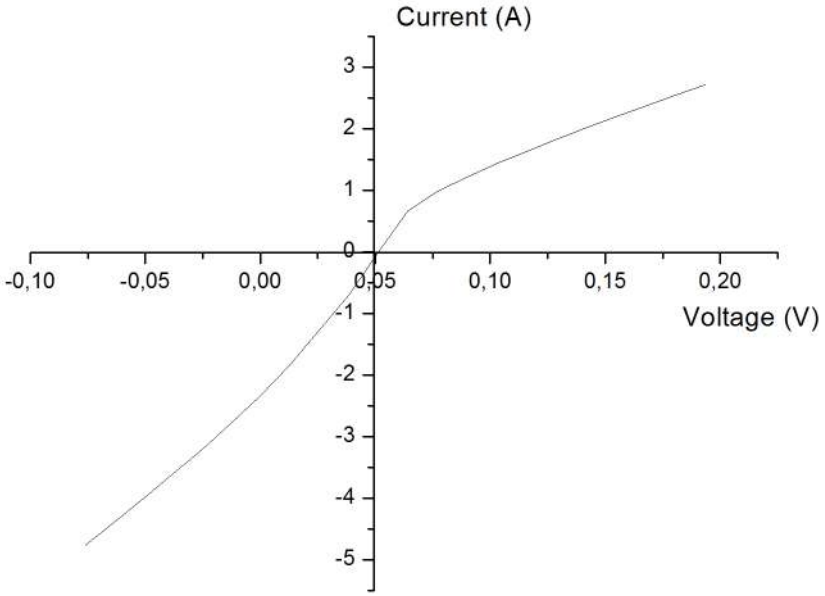


Figure 4.19 I-V characteristic of p-type Si wafer

4.6.3 Phosphorus Doping

The most important features of solar cell application is that when a cell exposes to sunlight, current of the cell increases with increasing sunlight intensity.

In order to identify V_{oc} point, voltage value that breaks diode characteristic was sent to the sample. As seen in Figure 4.20, after 3.62 V value, diode characteristic was broken and current was fixed. This 3.62 V value is V_{oc} value for sample.

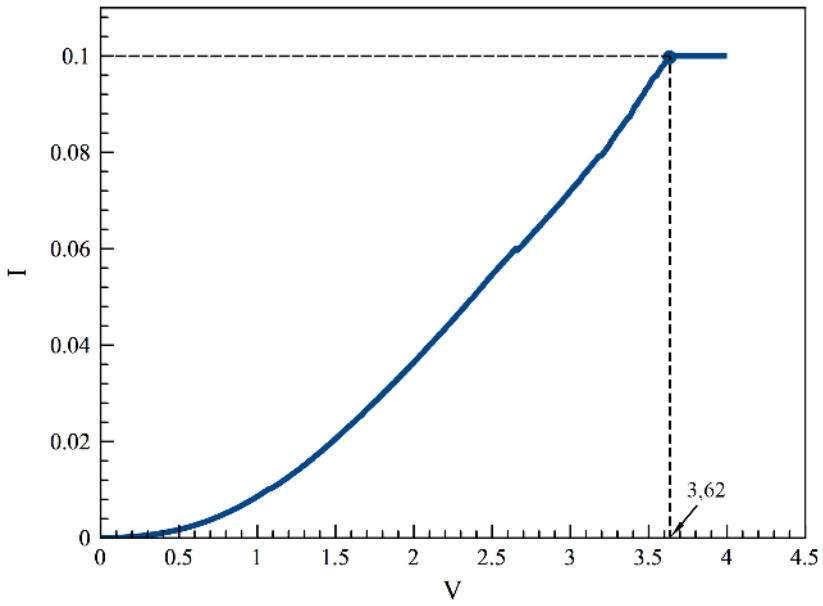


Figure 4.20 V_{oc} determination of phosphorus doped Si wafer

The maximum current value of 0.10 A is the I_{sc} value for this sample and it corresponds to the V_{oc} value. In order to compare the behaviour of the sample under the dark and in room condition, I-V characteristic tests were measured, and as seen on Figure 4.21 in room condition, the solar cell current values have increased. This showed that solar cell application has been successfully concluded in prototype size.

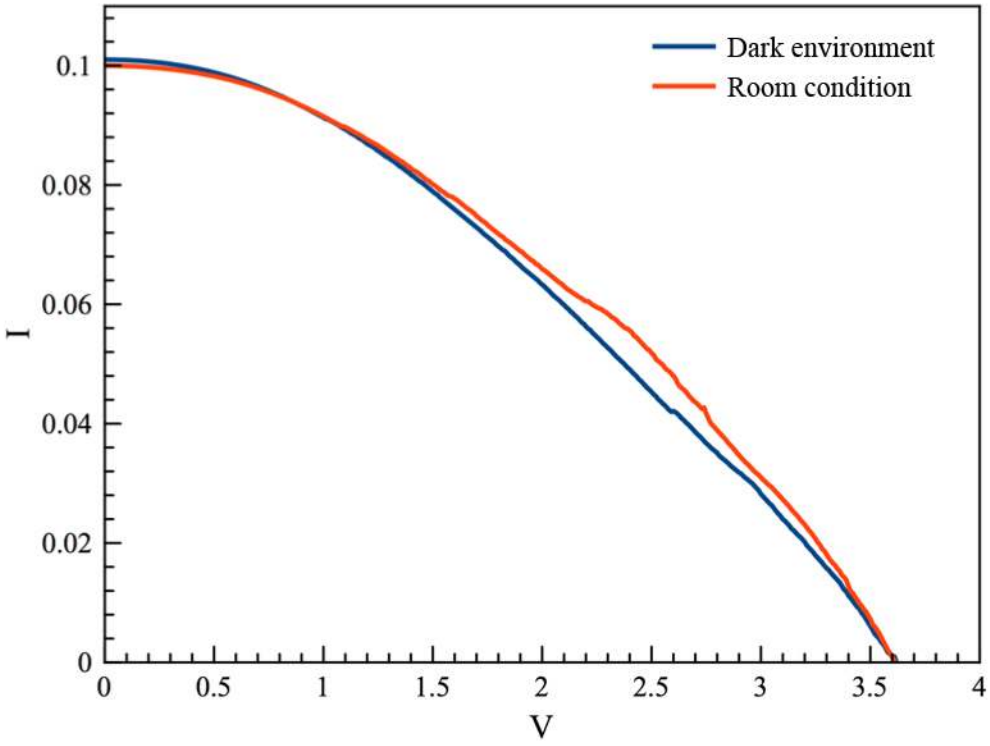


Figure 4.21 Comparison between room condition and dark area measurement of solar cell on changes of I-V characteristic

4.7 Application

As already mentioned several times before, area of interest of current thesis is definitely about solar cells. For this purpose, solar cell structure was gained from the produced Si wafer shown in Figure 4.22.

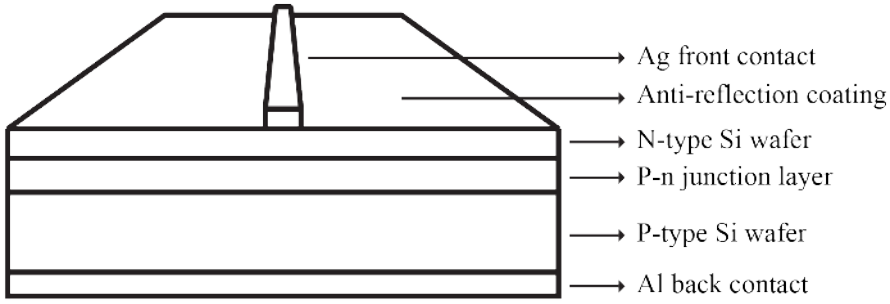


Figure 4.22 Structure of produced solar cell

Ag and Al contact was coated by PVD equipment. Anti reflection coating was performed by magnetron sputtering system. P-n junction was generated by doping n-type layer on the commercial p-type Si wafer by CVD equipment. Testing solar cell was performed under the sun light condition shown in Figure 4.23.

Figure 4.23 Single solar cell test under sunlight with multimeter

One edge of the crocodile clips was isolated to contact only one side of solar cell in 2 x 2 cm size. One probe was touched to front contact while the other was touched to back contact. Under the sunlight, multimeter was turned on and 0.33-0.35 V values could be seen on the screen. The obtained maximum value for one solar cell is 0.39 V whereas this value was 0.56 V in the study of Lee et al. (2011). Measurement was performed in April, the intensity of the sunlight of April was lower than the summer months, so voltage value could be changed by the intensity of the sunlight of the month. The other test was presented in Figure 4.24. Three solar cell were connected in series to simulate solar module system. When multimeter is turned on under the sunlight, 1 V value could be seen on the screen. As a result, this test illustrated that prototype solar cell production was realized successfully.

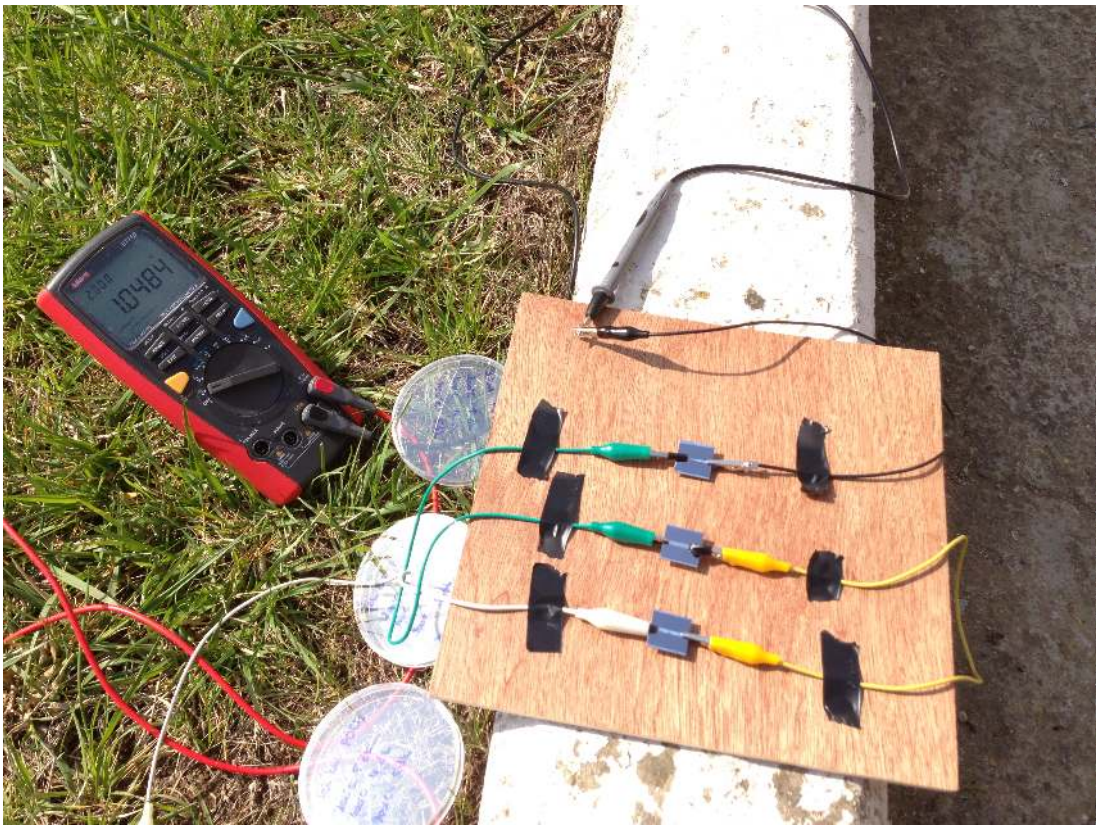


Figure 4.24 Solar module prototype with three solar cells

Solar cell efficiency is the ratio of the electrical output of a solar cell to the incident energy in the form of sunlight.

$$n = Pm / G \; x \; Ac \tag{4.1}$$

where; Pm is maximum power point (W), G is irradiance (input light) in W/m^2 and A_c is the surface area of solar cell in m^2. G is 1000 W/m^2 under the standard test condition, but the measurement was generated in the room condition so around 800 W/m^2 was used to determine the efficiency.

$$n = 0{,}03 / 800 \; x \; (0.02 \; x \; 0.02) \tag{4.2}$$

$$n \cong 0.094 = 9.4\,\% \tag{4.3}$$

The efficiency was found approximately 9.4 %.

CHAPTER FIVE
CONCLUSIONS AND FUTURE PLANS

5.1 General Results

In this study, production n- and p-type Si wafer by using CVD method and one of their application area (solar cell) were investigated. The following conclusions are obtained from the experimental work:

1. The first step of production of Si semiconductor wafer was generated successfully by production of single crystal Si ingot by using (100) Si seed in Czochralski Single Crystal Growth Equipment. That was supported with XRD patterns showed only single Si (400) peak. Produced Si ingot was sliced, then lapped and polished to achieve pure Si wafers. It was examined by surface roughness in profilometer after these operations.

2. N- and p-type Si wafers were successfully produced by using $POCl_3$ for phosphorus source and BN for boron source in CVD equipment, respectively. SEM, EDS and XPS analyses results showed that these elements were present in the structure of Si wafers.

3. The topic of the current thesis is about solar cells. In order to make basic solar cell structure, p-n junction layer must be produced by doping n-type layer on the p-type Si wafer. For this purpose, n-type layer was diffused on the commercial p-type Si wafer by using $POCl_3$.

4. The energy source of solar cell is the photon by sunlight. In order to strengthen the impact of solar cell, texturing and anti-reflection coating processes were generated before and after doping process, respectively. UV-Vis analysis demonstrated that reflection was reduced to %20-25 approximately.

5. The last step of the application was carried out by taking contacts from back and front surfaces of the solar cell. For this purpose, Al and Ag metals were coated on the front and back side by using PVD equipment, respectively. Crocodile clips were touched this coated place and sun test were performed under the sunlight condition in April. The voltage values of single solar cell and three solar cells (series connection) were approximately 0.35 V and 1 V, respectively. In summary, results demonstrated that the solar cell was produced successfully in prototype size. And also the efficiency was found approximately 9.4%; this value can be improved by the developing process steps, especially diffusion process.

5.2 Future Plans

In this study, phosphorus doping process for creating n-type layer was generated by using spin coater to coat liquid $POCl_3$ on the wafer's surface and using CVD equipment to diffuse phosphorus element into the Si wafer. CVD equipment modified with bubbling system could be better controlled in a process allowed for the doping.

Various improvements were needed for contacts. Connect wire did not solder on the Al and Ag metals or Si wafers. The other problem was shadowing, Al and Ag metals needed to be coated in a very thin form to avoid shadowing. In order to solve these two problems, the screen printing process was required.

Most commercial solar photovoltaic cells are made from silicon. To push the efficiency higher, one of the best options is to make tandem solar cells – that is, cells that use multiple light-absorbing materials. For perspective, silicon solar cells have a record efficiency of 25.6%. Using one light-absorbing material, the theoretical limit is 34% efficiency. Using two light-absorbing materials in tandem pushes the theoretical limit to 46% efficiency. In a publication called "A 2-terminal perovskite/silicon multijunction solar cell enabled by a silicon tunnel junction" by

Mailoa et al. (2015), tandem solar cells were made from two light-absorbing materials: silicon and the metal-halide perovskite, a new material with the potential to be manufactured at low cost. Finally, further investigations on tandem solar cells should be increased compared to silicons regarding their present situation in the scientific scale.

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