

DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

**A SINGLE-PHASE VOLTAGE SOURCE INVERTER
WITH ACTIVE POWER DECOUPLING FOR PV
SYSTEM**

by
Oğuz KABAKCI

December, 2021

İZMİR

A SINGLE-PHASE VOLTAGE SOURCE INVERTER WITH ACTIVE POWER DECOUPLING FOR PV SYSTEM

**A Thesis Submitted to the
Graduate School of Natural And Applied Sciences of Dokuz Eylül University
In Partial Fulfillment of the Requirements for the Degree of Master of Science in
Electrical and Electronics Engineering Program**

**by
Oğuz KABAKCI**

December, 2021

İZMİR

M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled "**A SINGLE-PHASE VOLTAGE SOURCE INVERTER WITH ACTIVE POWER DECOUPLING FOR PV SYSTEM**" completed by **OĞUZ KABAKCI** under supervision of **ASST. PROF. DR. ABDÜL BALIKCI** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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Oğuz KABAKCI

A SINGLE-PHASE VOLTAGE SOURCE INVERTER WITH ACTIVE POWER DECOUPLING FOR PV SYSTEM

ABSTRACT

This thesis provides a grid-connected single-phase H-bridge inverter with active power decoupling circuits for second-order harmonic power reduction. Single-phase grid-connected inverters store energy to isolate natural dual-frequency ripple power using the DC port. It can be achieved by using a large electrolytic capacitor known as passive power decoupling. Minimum required passive decoupling capacitance to buffer energy flow among the AC and DC port is signified and the active power decoupling circuits are offered to further the decrements of the DC link capacitor size.

H-bridge inverter and boost converter are analyzed to understand clearly why DC link capacitor is being used. After that active decoupling circuits are analyzed and applied to the system. According to analysis of active power circuits, their efficiencies are compared.

The single phase voltage source inverter with 500 W of power capacity is simulated by MATLAB/Simulink to evaluate the ripple power decoupling methods and associated algorithms in terms of reliability and efficiency.

In this thesis, OSG based control algorithm is applied to grid-connected inverter and MPPT algorithm is applied to the boost converter to get maximum power from PV array. And also three types of APD circuit are applied and the whole system successfully worked. The pros and cons are compared for different APD types. Also the HIL simulation is applied to APD method.

Keywords: Single-phase voltage source inverter, active power decoupling, passive power decoupling, DC link capacitor

PV SİSTEMİ İÇİN AKTİF GÜÇ DEKUPLAJLI TEK FAZLI GERİLİM KAYNAKLI EVİRİCİ

ÖZ

Bu tez, ikinci dereceden harmonik güç azaltma için aktif güç ayırma devrelerine sahip şebekeye bağlı tek fazlı bir H köprü invertörü sunmaktadır. Tek fazlı şebekeye bağlı invertörler, doğru akım penceresi kullanarak doğal çift frekans dalgalanma gücünü izole etmek için enerji depolamalıdır. Pasif güç ayrıştırması olarak bilinen büyük bir elektrolitik kondansatör kullanılarak elde edilebilir. Alternatif akım ve doğru akım penceresi arasındaki güç akışını tamponlamak için gereken minimum pasif ayırma kapasitansı belirtilir ve aktif güç ayırma devreleri, doğru akım bağlantı kapasitör boyutunun daha da azaltılması için sunulur.

H köprü inverter ve yükseltici dönüştürücü, doğru akım bağlantı kapasitörünün neden kullanıldığını açıkça anlamak için analiz edilir. Bundan sonra aktif güç ayırma devreleri analiz edilir ve sisteme uygulanır. Aktif güç ayırma devrelerinin analizine göre verimlilikleri karşılaştırılır.

500 W güç kapasitesine sahip tek fazlı voltaj kaynağı invertörü, dalgalanma güç ayırma yöntemlerini ve ilgili algoritmaları güvenilirlik ve verimlilik açısından değerlendirmek için MATLAB / Simulink tarafından simüle edilir.

Bu tezde, FV diziden maksimum güç elde etmek için şebeke bağlantılı eviriciye OSG tabanlı kontrol algoritması ve yükseltici dönüştürücüye MPPT algoritması uygulandı. Ayrıca üç tip APD devresi uygulandı ve tüm sistem başarıyla çalıştırıldı. Artıları ve eksileri farklı APD türleri için karşılaştırıldı. Ayrıca APD yöntemine HIL simülasyonu uygulandı.

Anahtar kelimeler: Tek fazlı gerilim kaynağı invertör, aktif güç ayrıştırma, pasif güç ayrıştırma, DC bağlantı kapasitör

CONTENTS

	Page
M.Sc THESIS EXAMINATION RESULT FORM.....	ii
ACKNOWLEDGEMENTS	iii
ABSTRACT	iv
ÖZ	v
LIST OF FIGURES	ix
LIST OF TABLES	x
CHAPTER ONE – INTRODUCTION	1
CHAPTER TWO – SINGLE PHASE DC-AC POWER CONVERTER.....	5
2.1 PV Side Boost Converter	5
2.1.1 Circuit Topology	6
2.1.2 Control Algorithm	9
2.1.3 MPPT Algorithm for Photo-Voltaic System	9
2.1.4 Simulation	11
2.2 Passive Power Decoupling	13
2.3 Grid-connected H-Bridge Inverter	15
2.3.1 Circuit Topology	15
2.3.2 Control Algorithm	18
2.3.3 Simulation	20
CHAPTER THREE – ACTIVE POWER DECOUPLING.....	24
3.1 Boost Type DC Active Power Decoupling	25
3.1.1 Circuit Topology	25
3.1.2 Control Algorithm	27
3.1.3 Simulation	28
3.2 Buck-Boost Type DC Active Power Decoupling	32

3.2.1 Circuit Topology	33
3.2.2 Control Algorithm	34
3.2.3 Simulation	34
CHAPTER FOUR – HARDWARE IN THE LOOP	37
4.1 HIL Setup	37
4.2 Software Generation for the Controller.....	39
4.3 HIL Simulation of Boost converter	41
4.4 HIL Simulation of Inverter	44
4.5 HIL Simulation of Boost Type Decoupling Circuit	47
4.6 HIL Simulation of Buck-Boost Type Decoupling Circuit.....	51
CHAPTER FIVE – CONCLUSION	54
CHAPTER SIX – FUTURE WORKS	56
REFERENCES.....	57
APPENDICES.....	60
Appendix 1: MPPT Algorithm.....	60
Appendix 2: Boost Converter Simulink Model	61
Appendix 3: Inverter Simulink Model	64
Appendix 4: APD Simulink Model.....	72
Appendix 5: HIL Setup	76
Appendix 6: HIL Blocks.....	80

LIST OF FIGURES

	Page
Figure 2.1	Grid connected single phase dc-ac power converter 5
Figure 2.2	Boost converter 5
Figure 2.3	Boost converter (mode 1) 6
Figure 2.4	Boost converter (mode 2) 7
Figure 2.5	Voltage and current graph of the inductor..... 8
Figure 2.6	Control algorithm of boost converter..... 9
Figure 2.7	MPPT flow chart 10
Figure 2.8	Boost converter control by MPPT controller..... 11
Figure 2.9	Transient analysis of the boost converter..... 12
Figure 2.10	Steady state analysis of the boost converter 13
Figure 2.11	The general form of single-phase DC-AC power converter 14
Figure 2.12	Grid connected h bridge inverter 15
Figure 2.13	Voltage shape of V_{AB} 16
Figure 2.14	Orthogonal signal generator (OSG) based power calculation 19
Figure 2.15	Produced reference grid current and gate signals 19
Figure 2.16	Transient analysis of the inverter 22
Figure 2.17	Steady state analysis of the inverter..... 23
Figure 3.1	The decoupling circuits..... 25
Figure 3.2	Grid connected h bridge inverter with boost type APD circuit 26
Figure 3.3	Boost type decoupling circuit modes..... 27
Figure 3.4	Gate signal generator of the decoupling circuit 28
Figure 3.5	Transient analysis of inverter with boost type APD circuit 30
Figure 3.6	Steady state analysis of inverter with boost type APD circuit..... 31
Figure 3.7	Grid connected H-bridge inverter with buck-boost type APD circuit 32
Figure 3.8	Buck boost type APD circuit when S_5 is on 33
Figure 3.9	Buck boost type APD circuit when S_5 is off 33
Figure 3.10	Transient analysis of inverter with buck-boost type APD circuit..... 35

Figure 3.11	Steady state analysis of inverter with buck-boost type APD circuit ..	36
Figure 4.1	Serial communication blocks	38
Figure 4.2	Serial communication blocks for code generation.....	39
Figure 4.3	Hardware interrupt implementation.....	40
Figure 4.4	HIL model of boost converter	41
Figure 4.5	Software model of boost converter.....	42
Figure 4.6	Transient analysis of HIL boost converter	42
Figure 4.7	Steady state analysis of HIL boost converter.....	43
Figure 4.8	HIL model of inverter.....	44
Figure 4.9	Software model of the inverter	44
Figure 4.10	Transient analysis of HIL inverter.....	45
Figure 4.11	Steady state analysis of HIL inverter	46
Figure 4.12	HIL model of boost type decoupling connected inverter	47
Figure 4.13	Software model of boost type decoupling connected inverter.....	48
Figure 4.14	Transient analysis of HIL boost APD connected inverter	49
Figure 4.15	Steady state analysis of HIL boost APD connected inverter.....	50
Figure 4.16	Transient analysis of HIL buck-boost APD connected inverter.....	52
Figure 4.17	Steady state analysis of HIL buck-boost APD connected inverter	53

LIST OF TABLES

	Page
Table 2.1 Boost converter design considerations	11
Table 2.2 Inverter design considerations	20
Table 3.1 Decoupling circuit design considerations	28



CHAPTER ONE

INTRODUCTION

The energies which are received from herbal assets inclusive of ocean, biomass, geothermal, hydro, solar and wind are referred to as renewable power sources. In addition, they known as sustainable or alternative electricity. The demand for electricity is increasing in the world, fossil fuel reserves are decreasing, and for these reasons, the demand for renewable energies is increasing all over the world. Also, there are many places that are still without electricity. Even in some remote parts of India there are about seventy-two million families without access to electricity. (Pali & Vadhera, 2017).

Solar energy is converted into DC electrical energy with the help of a solar cell which are also known as a photovoltaic (PV) cell. To refer PV cells as a module, many PV cells shall be connected to each other. In order to increase the current and voltage supply capacity in larger solar power plants, many PV modules shall be connected each other to form a PV array. By using a suitable inverter, the DC output can be transformed into AC. The efficiency calculation of the inverters is another main topic for for PV applications (Akpinar et al., 2017).

The photovoltaic systems can be stand-alone systems or they can be grid-connected systems. Usually solar power plants are designed with a few standby units and hybrid collections along with all other energy systems for continuous power. There are so many hybrid schemes in the literature that combine with solar energy. In (Zhou et al., 2010), an assessment of the stand alone wind energy systems with battery storage is given to analyze the current state of control techniques, simulation and optimization. In (Ahmed et al., 2008) a hybrid system combining solar cells, wind turbines and a fuel cell is given to the residential energy application. A blueprint for optimizing the capacity dimensions of the various components of the hybrid wind-solar energy generation system using a battery bank is given in (Yang et al., 2007).

PV cell is needed to convert solar energy to electric energy. Maximum power point

tracking (MPPT) controller is used, in order to achieve maximum performance for PV module. MPPT is a widely recognized concept applied to PV module. The main aim is to get the maximum feasible power. PV system efficiency is especially relying at the performance of the PV panel, inverter and the MPPT controller (Balikci et al., 2020). The inverter and the PV panel efficiencies can be increased. But this is not always an easy manner, since more superior components are necessary. And additionally, they will require replacing and putting in new hardware components. The fee of installation will be increased by these new elements. On the other hand, it is simple to increase the MPPT controller efficiency through putting in a brand new control algorithm. Also used algorithm can be updated (Ahmed et al., 2017).

The PV modules prices, which approximately from 30% to 50% of the full price of the system, was the number one restriction of PV power usage (Rahim et al., 2012). Since the price of the PV modules are decreasing nowadays, while calculating the full price of the PV system, the prices of the inverters have been an increasing number of standing out. Most of the countries and regions, a high-frequency transformers were applied to the grid connected PV systems. The reason was to isolate the PV module from the grid. However, high-frequency transformer reduced efficient of the system, increased the price and make the system size bulky (Islam et al., 2016). For low power PV applications, transformerless grid-connected inverters may be used to reduce the cost(Akpinar et al., 2018).

Grid connected inverters have developed appreciably with high variety within the beyond 2–3 decades. In existing power electronics and energy systems, grid-connected inverters are taken into consideration as one of the quickest growing technology. Efficiency, size, weight, reliability and so on, along without problems of installation have all stepped forward considerably with the improvement of modern and revolutionary inverter configuration. The cost of manufacturing inverters are influenced by these factors (Jana et al., 2017).

Single-phase systems comprise both the DC power component and the inherent double frequency ripple component. These components cause current ripples or

doubles the frequency voltage on the DC side. Due to these ripples, a few different troubles inclusive of decreased lifetime in battery systems may also arise. The broadly used passive power decoupling technique is connecting an aluminium electrolytic capacitor to the DC port for absorbing this ripple power due to the massive value of the capacitor. The main negative aspects of the electrolytic capacitors (E-cap) are short lifetime and a huge size (Pradeep Kumar & Fernandes, 2018). Consequently, it is far impossible to assemble an inverter that has a long lifetime and compact design with electrolytic capacitors (Qin et al., 2016).

Interest in higher power intensity and higher performance has usually accelerated. Designing a compact unit at the same time as preserving the low input ripple current is the most tough goal (Challenge et al., 2015). By using the passive decoupling method, it is almost impossible to achieve this goal. Consequently, Active Power Decoupling (APD) will become one of the main strategies to overcome this design challenge. Because, that design uses lower capacitance film capacitors and inductors instead of electrolytic capacitor (Qin et al., 2016). Supplying same power through APD circuit as the bulky capacitor does, is the primary concept. The APD approach generally has inductors, capacitors and power switches. Consequently, the main subject might be the efficiency reduction induced via this technique. A set of circuit topologies of APD were offered within the published works, and mostly type of the designs were shunt type (Li et al., 2015) (Tang & Blaabjerg, 2015) rather than connecting the additional circuit in series with DC bus (Wang et al., 2014). The decoupling capacitor voltage polarity classifies the APD methods into AC and DC decoupling.

Active power decoupling and passive power decoupling (PPD) methods can also be used together. PPD can be used to increase MMPT efficiency and get low total harmonic distortion and once MPPT adapt itself to change, APD can be activated (Yang et al., 2021). Bidirectional DC to DC type APD method with high frequency capacitor linked to DC bus can be also used together (Rai et al., 2021). APD method is also used in single-phase current source rectifiers to eliminate the ripple power. These rectifiers normally use LC resonators to eliminate ripple power. But this

method requires huge passive components. The APD method can be replaced by LC resonator and eliminate the ripple power (Liu et al., 2020). There are several control strategies for APD methods in literature and they can be categorized due to control ideas. The pros and cons of the control strategies are differentiate according to the control idea (Liu et al., 2021).

In this thesis, first of all the boost converter connected to the PV module, will be constructed and controlled with MPPT algorithm to get maximum feasible power PV module. Once the boost converter is constructed, the DC voltage of the system will be ready. Secondly, the single phase voltage source inverter will be constructed and controlled according to desired power with unity power factor. Thirdly, to decouple the ripple power, the DC link capacitor will be used. Finally, APD circuits will be used instead of DC link capacitor and the topologies will be compared.

CHAPTER TWO

SINGLE PHASE DC-AC POWER CONVERTER

Power converter is an crucial part of many DC to AC conversion equipments. In PV applications, in lasts many years, the source or load is a simple silicon-based device. The interface for energy conversion among the device and the grid is required for such as systems. The grid is connected as single phase in scaled down applications. The conditions of single phase have wonderful drawback that power flow on the grid side is time various, its variation is double frequency and it has approximately a non-zero mean. DC flow must be observed from panels in PV systems. More operating zone and reduced available average output are required for any variant (Krein et al., 2012). In this thesis, PV source boost converter is used as an DC device and the H-Bridge inverter is used as a converter as seen in Figure 2.1.

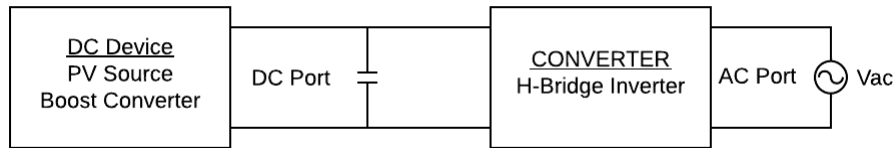


Figure 2.1 Grid connected single phase dc-ac power converter

2.1 PV Side Boost Converter

In this thesis, a PV array is connected to a single phase inverter via using a conventional boost type DC to DC converter.

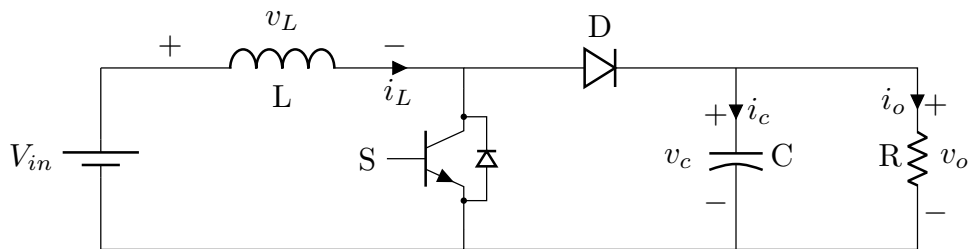


Figure 2.2 Boost converter

Boost converter is basically preferred in PV applications to boost the DC voltage over peak value of the grid voltage. It also provides maximum power point tracking capability. The mean of DC output voltage must be managed so that it equates to the preferred value in these converters, even though the input voltage varies. Output voltage regulation within the DC to DC converter is accomplished by continuously changing the amount of energy getting from the source and sending into the load. (Hasaneen & Mohammed, 2008).

The DC-DC boost converter uses four components: Inductor, output capacitor, semi conductor switch and diode. The inductor is also known as boost element. Depending on the switch mode, the inductor stores energy and then feeds the output. The output capacitor is used to keep output voltage in desired ripple tolerance band. The switch and the diode will determine the current paths.

2.1.1 Circuit Topology

In this thesis, Boost Converter (Figure 2.2) is analyzed under continuous conduction mode (CCM). To drive the converter in the CCM, the inductor current flows constantly and never drops to zero (Masri & Chan, 2010).

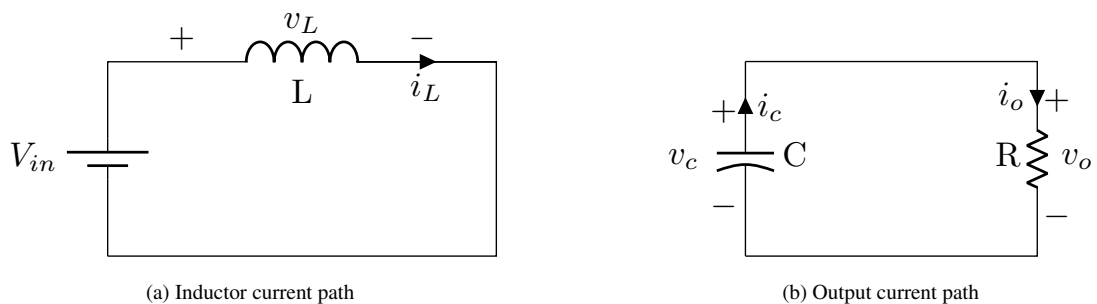


Figure 2.3 Boost converter (mode 1)

Under CCM, it is divided into two operation modes according to switch mode. Once the switch is turned on (Figure 2.3), the input voltage source charges the inductor (Figure 2.3a) and the capacitor feed the output by discharging (Figure 2.3b). During

that time (T_{on}), the input current increases and the output voltage decreases.

$$V_{in} = v_L \quad (2.1)$$

$$V_{in} = L \cdot \frac{di_L}{dt} \quad (2.2)$$

$$di_L = \frac{V_{in}}{L} \cdot dt \quad (2.3)$$

$$\Delta i_{L_{on}} = \frac{V_{in}}{L} \cdot D \cdot T_s \quad (2.4)$$

where D stands for the duty cycle and T_s is the sampling period.

Once the switch is turned off (Figure 2.4), the input voltage and the inductor charge the capacitor and feed the output. During this time (T_{off}), input current decreases and the output voltage increases.

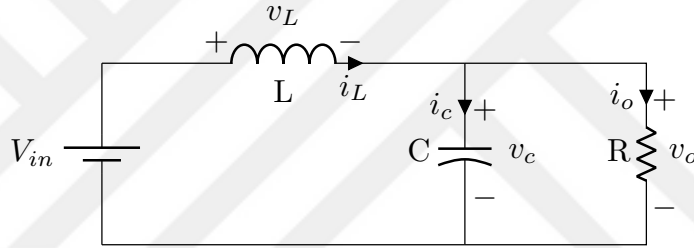


Figure 2.4 Boost converter (mode 2)

$$v_L = v_o - V_{in} \quad (2.5)$$

$$L \cdot \frac{di_L}{dt} = v_o - V_{in} \quad (2.6)$$

$$di_L = \frac{v_o - V_{in}}{L} \cdot dt \quad (2.7)$$

$$\Delta i_{L_{off}} = \frac{v_o - V_{in}}{L} \cdot (1 - D) \cdot T_s \quad (2.8)$$

As shown in Figure 2.5, the current change in Mode 1 and current change in Mode 2 must be equal.

$$\Delta i_{L_{on}} = \Delta i_{L_{off}} \quad (2.9)$$

$$\frac{V_{in}}{L} \cdot D \cdot T_s = \frac{v_o - V_{in}}{L} \cdot (1 - D) \cdot T_s \quad (2.10)$$

$$V_{in} \cdot D = (v_o - V_{in}) \cdot (1 - D) \quad (2.11)$$

$$V_{in} = v_o \cdot (1 - D) \quad (2.12)$$

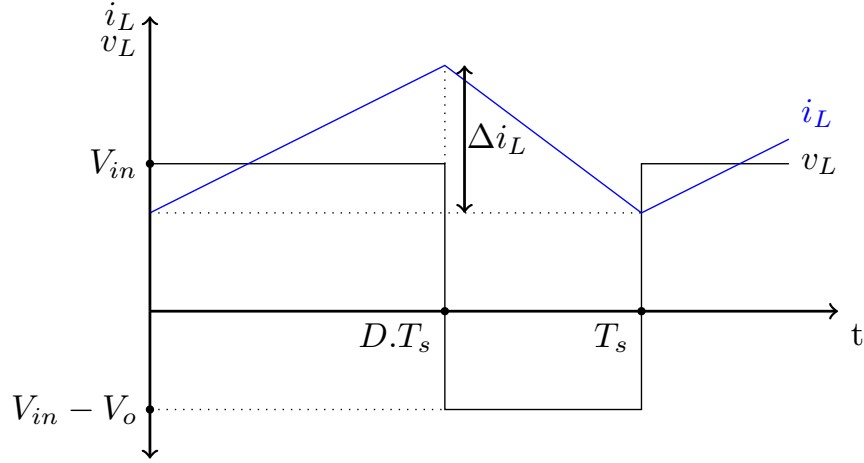


Figure 2.5 Voltage and current graph of the inductor

$$D = 1 - \frac{V_{in}}{v_o} \quad (2.13)$$

In the control algorithm, the duty cycle (2.13) is used to control output voltage. The switch on and off times (T_{on} and T_{off}) determine the current ripple which is determined in design specifications. It shall be assumed that the operation mode of the converter is CCM and the inductance and the capacitance must be calculated according to this design consideration.

The inductance can be found from (2.9) as:

$$L = \frac{V_{in} \cdot (v_o - V_{in})}{\Delta i_L \cdot f_s \cdot v_o} \quad (2.14)$$

where Δi_L stands for the input current ripple and f_s stands for the sampling frequency.

The capacitance can be found from Mode 1:

$$\frac{v_o}{R} = i_{con} \quad (2.15)$$

$$\frac{v_o}{R} = C \cdot \frac{dv_c}{dt} = C \cdot \frac{\Delta v_o}{D \cdot T_s} \quad (2.16)$$

$$C = \frac{v_o \cdot D}{f_s \cdot \Delta v_o} \quad (2.17)$$

2.1.2 Control Algorithm

To control the boost converter, a widely used technique called as PWM is used.(Figure 2.6). According to design specifications, the reference output voltage is given to the control algorithm as V_{ref} . The dissimilarity between the reference and the actual voltage produces the error of the voltage. And by controlling the PI, the current reference can be produced. After that, the dissimilarity between the reference and the actual current produces the error of current. The gate signal is obtained by comparison of the duty cycle, which is equal to the PI controller outcome, and a carrier wave formed as triangular.

$$H_{PI1}(z) = K_{P1} + K_{i1} \cdot T_s \cdot \frac{1}{z-1} \quad (2.18)$$

$$H_{PI2}(z) = K_{P2} + K_{i2} \cdot T_s \cdot \frac{1}{z-1} \quad (2.19)$$

The control algorithm will keep the output voltage of boost converter constant with some amount of ripple which depends on the design specifications.

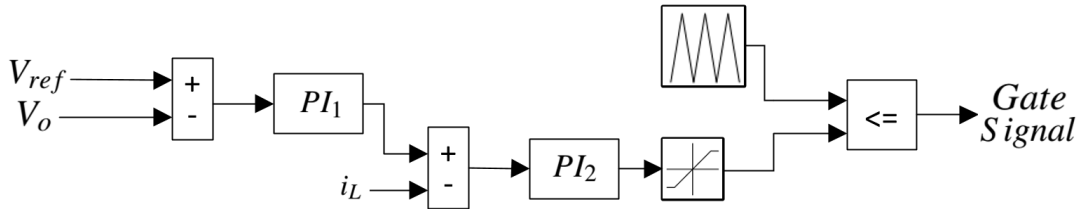


Figure 2.6 Control algorithm of boost converter

2.1.3 MPPT Algorithm for Photo-Voltaic System

As seen from Figure 2.7, the algorithm trying to find maximum power by changing the reference voltage which is used by the control algorithm of the boost converter (Figure 2.8). First of all, the MMPT algorithm senses the PV voltage and the PV current. Secondly, the multiplication of the voltage and the current will determine the power of the PV system. Thirdly, the dissimilarity between the previous and the current voltage will be calculated. Also, the difference between previous power and

the current power will be calculated. After calculating all quantities, the algorithm will check that if the power is changed or not. If power is not changed, algorithm will keep the previous reference voltage. If power is changed then algorithm will check that power is decreased or increased. If the power is increased, it will check the voltage difference. If the voltage is increased, then algorithm will increase the voltage again. If the voltage is decreased, then algorithm will decrease the voltage again. The MATLAB code of this flow chart is also given in APPENDIX 0.1.

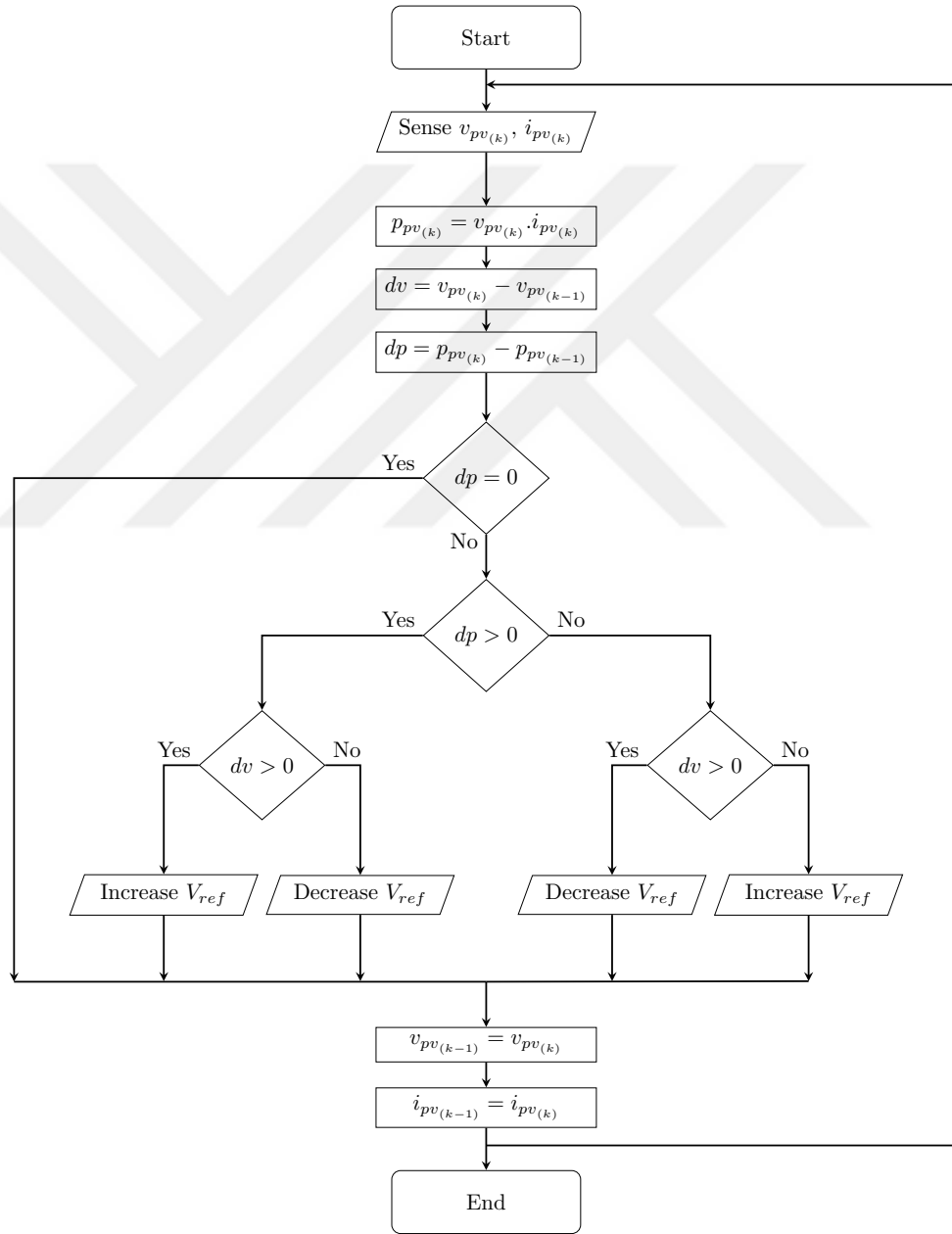


Figure 2.7 MPPT flow chart

Since the reference voltage considered as a DC signal, PI controller can be used with given formula:

$$H_{PI}(z) = K_P + K_i \cdot T_s \cdot \frac{1}{z-1} \quad (2.20)$$

Once the duty is generated by the help of PI controller, gate signals can be generated for the boost converter.

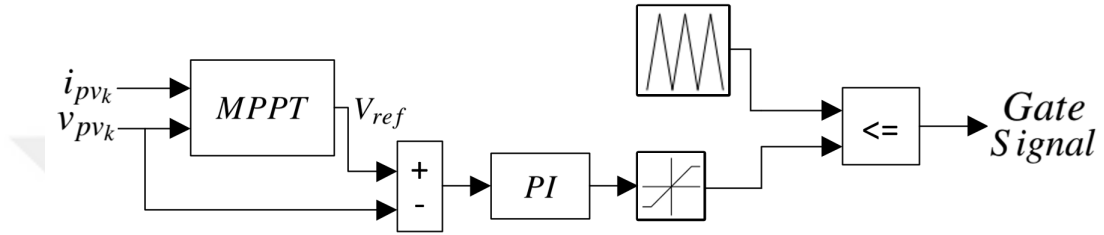


Figure 2.8 Boost converter control by MPPT controller

2.1.4 Simulation

Table 2.1 Boost converter design considerations

Unit	Quantity	Value
PV Array at 25°C and 1000W/m ²	Maximum Power	524W
	Open Circuit Voltage	130.2V
	Voltage at maximum power point	104.4V
	Current at maximum power point	5.02A
Boost Converter	Inductor current ripple	%10
	Switching Frequency	20kHz

The design considerations in Table 2.1 are given according to the user defined PV Array module in SIMULINK (APPENDIX 0.4). And according to these considerations, the inductor current ripple can be calculated.

$$\Delta i_L = 5.02 \cdot \frac{10}{100} = 0.502A \quad (2.21)$$

According to (2.14), the inductance can be calculated:

$$L = \frac{104.4 \cdot (200 - 104.4)}{0.502 \cdot 20000 \cdot 200} = 5mH \quad (2.22)$$

According to the findings, boost converter model is constructed in MATLAB/SIMULINK (APPENDIX 0.2). The transient response and the steady state response are observed as seen from figure 2.9 and figure 2.10.

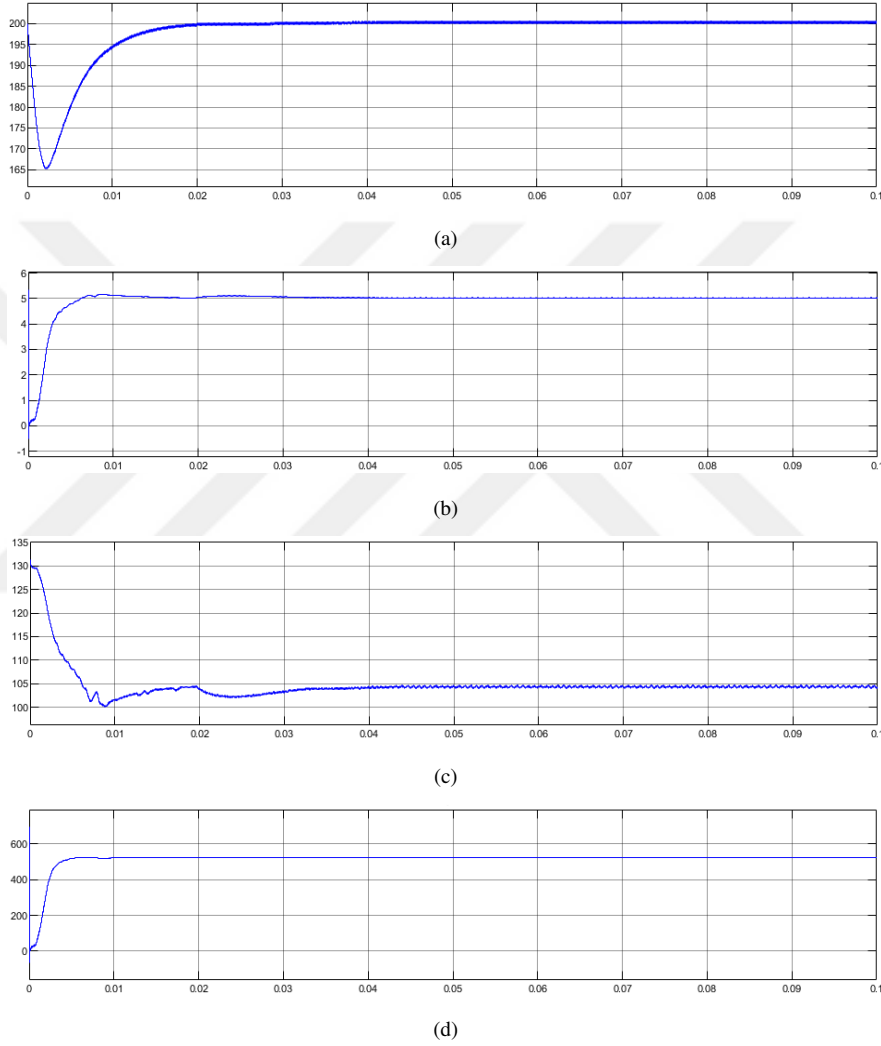


Figure 2.9 Transient analysis (start up) of the boost converter, (a) V_{DC} , (b) i_{pv} , (c) v_{pv} , (d) p_{pv}

As visible from figure 2.9, the PV voltage is to begin with at 130V that is the open circuit voltage of the PV. Then the MPPT algorithm is tracing the maximum power point and it reaches to the maximum power point and keep quantities in that point. Also the output voltage is greater than the input voltage, considering the fact that it is a boost converter.

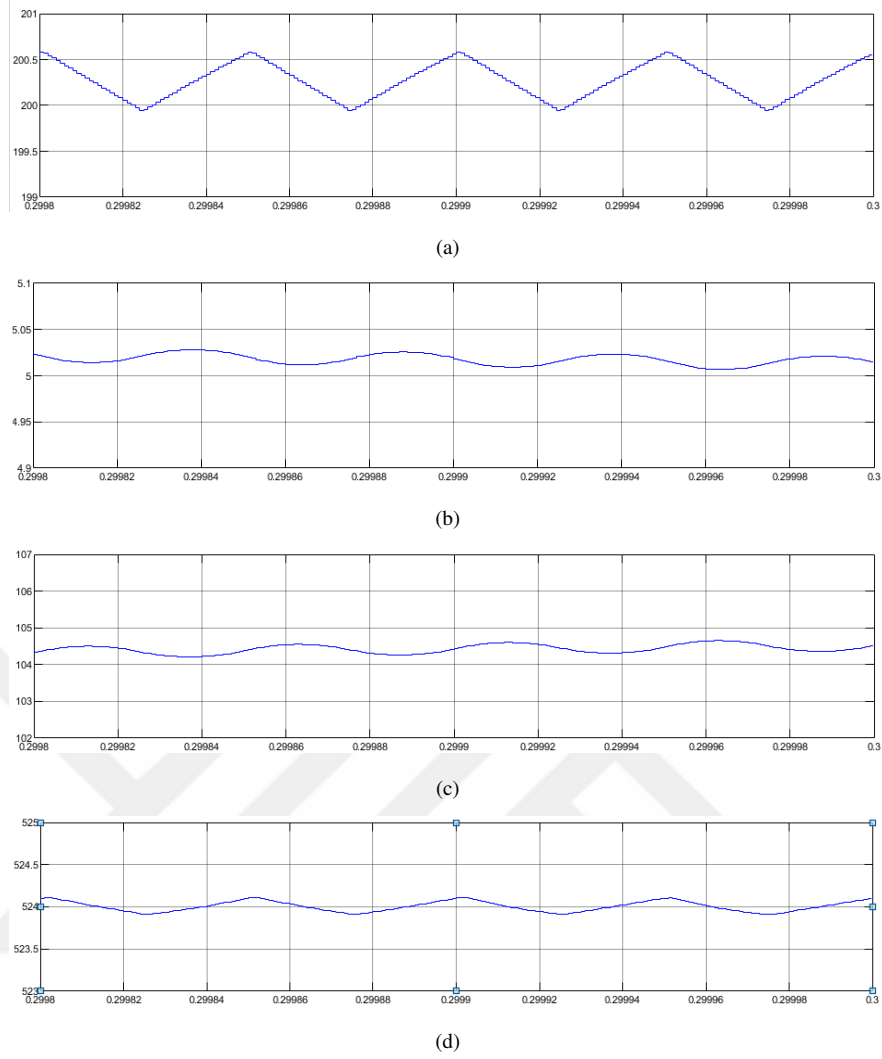


Figure 2.10 Steady state analysis of the boost converter, (a) V_{DC} , (b) i_{pv} , (c) v_{pv} , (d) p_{pv}

As seen from the figure 2.10, at the maximum power point, all quantities match with the PV array. Also the inductor and the switching frequency keeps inductor current ripple below 10% of i_L .

2.2 Passive Power Decoupling

The fundamental form of the single phase inverter is shown in Figure 2.11. The DC port has a stable power flow:

$$P_{DC} = P_o = V_{DC} \cdot I_{DC} \quad (2.23)$$

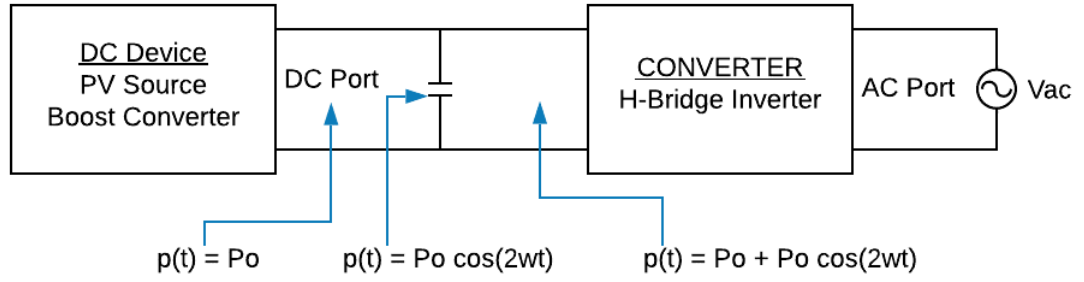


Figure 2.11 The general form of grid connected single phase DC to AC power converter

Time varying power flow occurred on AC port:

$$p_{ac}(t) = v_{ac}(t) \cdot i_{ac}(t) \quad (2.24)$$

Assume the voltage and current are pure sinusoidal on AC port,

$$v_{ac}(t) = V_o \cdot \sin(\omega t) \quad (2.25)$$

$$i_{ac}(t) = I_o \cdot \sin(\omega t + \phi) \quad (2.26)$$

Substituting (2.25) and (2.26) into (2.24):

$$p_{ac}(t) = \frac{V_o \cdot I_o}{2} \cos(\phi) - \frac{V_o \cdot I_o}{2} \cos(2\omega t + \phi) \quad (2.27)$$

Phase shift (ϕ) between grid current and voltage shall be zero at a unity power factor,

$$p_{ac}(t) = P_o + P_o \cdot \cos(2\omega t) \quad (2.28)$$

where P_o is the average value of output power.

As seen from (2.28), Each the DC average power component and an extensive time-various second-order ripple power component are observed in the output instantaneous power. As an instance, at the input side, to be able to hold a twenty percent current ripple, ten percent of the ripple power shall be delivered by the DC source. With this way a constant DC input voltage can be thought. DC-link capacitor will feed the ninety percent of the ripple power (Qin et al., 2016). This technique is known as as passive power decoupling.

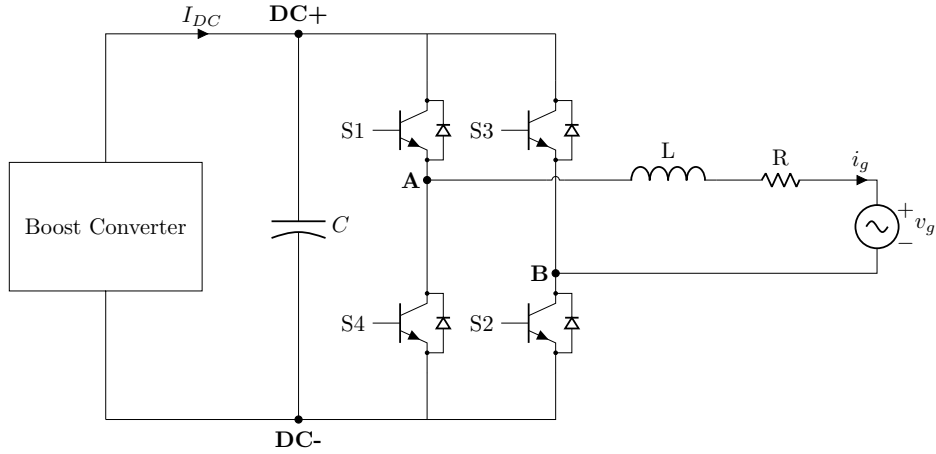


Figure 2.12 Grid connected h bridge inverter

2.3 Grid-connected H-Bridge Inverter

DC voltage to AC voltage conversion is performed through a conventional H-bridge inverter (Figure 2.12). The inverter can be constructed as standalone system for applications which includes solar energy or to work as a backup power supply from batteries that are charged one at a time.

2.3.1 Circuit Topology

When the grid voltage is on its positive polarity, S_1 is continuously on, S_4 is continuously off state, S_2 and S_3 switches toggle alternately. According to the state of S_2 and S_3 switches grid current changes as below:

- S_2 is on, $V_{AB} = V_{DC}$, i_g increases
- S_3 is on, $V_{AB} = 0$, i_g decreases

When the grid voltage is on its negative polarity, S_3 is continuously on and S_2 is continuously off, S_1 and S_4 toggles alternately. According to the state of S_1 and S_4 switches the grid current changes as below:

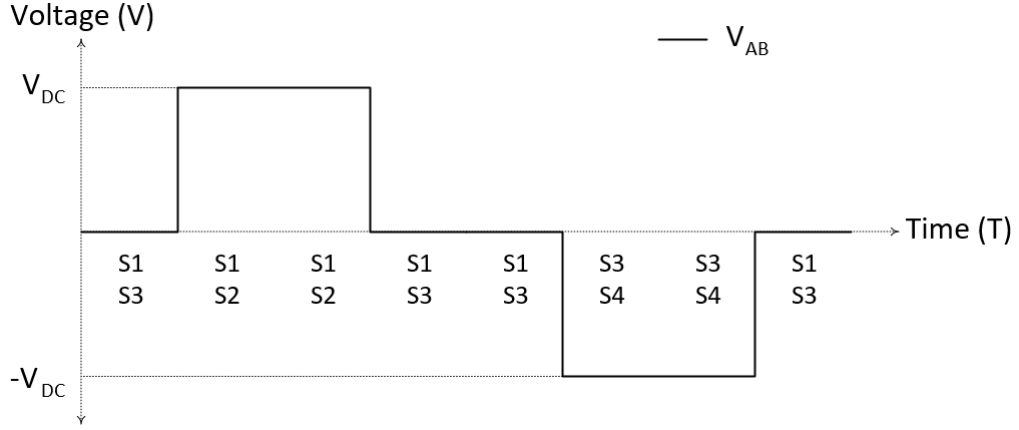


Figure 2.13 Voltage shape of V_{AB}

- S_4 is on, $V_{AB} = -V_{DC}$, i_g increases
- S_1 is on, $V_{AB} = 0$, i_g decreases

According to these switching algorithms the voltage shape of V_{AB} will be square wave. In Figure 2.13, the switch names indicate that the switches are turned ON in that interval and the others are turned OFF.

The inverter uses a large-sized electrolytic capacitor to keep the ripple of input voltage at a minimum value. The output power of the inverter contains 2 components. One of them is DC and the other is a double frequency ripple as shown before (Equation 2.28). This ripple component needs to be filtered by this capacitor. So, the capacitor voltage must be like:

$$v_c(t) = V_r \cdot \sin(2\omega t) \quad (2.29)$$

where V_r is the ripple voltage magnitude and $V_r = \Delta V/2$.

$$i_c(t) = C \cdot \frac{dv_c}{dt} = C \cdot V_r \cdot 2 \cdot \omega \cdot \cos(2\omega t) \quad (2.30)$$

Also, the ripple power needs to be supplied by this capacitor. So, it is known that:

$$p_c(t) = v_c(t) \cdot i_c(t) = P_o \cdot \cos(2\omega t) \quad (2.31)$$

Substituting Equation 2.30 into Equation 2.31:

$$i_c(t) = \frac{P_o}{V_{DC}} \cdot \cos(2\omega t) \quad (2.32)$$

Rearranging Equation 2.32:

$$C = \frac{P_o}{2\pi \cdot f \cdot V_{DC} \cdot \Delta V} \quad (2.33)$$

where P_o is the DC bar power, V_{DC} is the voltage of DC bar, ΔV is peak to peak voltage ripple and f is the grid frequency.

An inductor is used to keep the current smooth. The inductance is important to determine the current ripple. So, it must be chosen according to the current ripple which is determined in design specifications.

$$v_L = L \cdot \frac{di_L}{dt} \quad (2.34)$$

$$V_{DC} - v_g = L \cdot \frac{\Delta i_L}{D \cdot T_s} \quad (2.35)$$

$$\Delta i_L = \frac{D \cdot T_s \cdot (V_{DC} - v_g)}{L} \quad (2.36)$$

Here the duty cycle is a sinusoidal wave and also the grid voltage can be determine as a component of the DC Voltage as shown below:

$$D = D(\omega t) = m_a \cdot \sin(\omega t) \quad (2.37)$$

$$v_g = V_{DC} \cdot D \quad (2.38)$$

Substituting Equation 2.37 and Equation 2.38 into Equation 2.36:

$$\Delta i_L = \frac{D \cdot T_s \cdot m_a \cdot \sin(\omega t) \cdot (1 - m_a \cdot \sin(\omega t))}{L} \quad (2.39)$$

To find maximum Δi_L , the derivative of it must be zero:

$$\frac{d}{dt}[\Delta i_L] = 0 \quad (2.40)$$

Substituting Equation 2.39 into Equation 2.40:

$$\frac{V_{DC} \cdot T_s \cdot m_a}{L} [\omega \cdot \cos(\omega t) \cdot (1 - m_a \cdot \sin(\omega t)) + \sin(\omega t) \cdot (-m_a) \cdot \omega \cdot \cos(\omega t)] = 0 \quad (2.41)$$

$$\sin(\omega t) = \frac{1}{2m_a} \quad (2.42)$$

Substituting Equation 2.42 into Equation 2.39:

$$\Delta i_{L_{max}} = \frac{1}{L} \cdot V_{DC} \cdot T_s \cdot m_a \cdot \frac{1}{2m_a} \cdot (1 - m_a \cdot \frac{1}{2m_a}) \quad (2.43)$$

Rearranging the Equation 2.43:

$$\Delta i_{L_{max}} = \frac{V_{DC} \cdot T_s}{4L} \quad (2.44)$$

From Equation 2.44, inductance can be found as:

$$L = \frac{V_{DC}}{4 \cdot f_s \cdot \Delta i} \quad (2.45)$$

2.3.2 Control Algorithm

To control the gates, the SW must produce the reference current of the grid. The active and reactive power can be calculated as seen in Equation 2.46 and Equation 2.47 (Islam et al., 2016) :

$$P_{cal} = \frac{v_{g\alpha} \cdot i_{g\alpha} + v_{g\beta} \cdot i_{g\beta}}{2} \quad (2.46)$$

$$Q_{cal} = \frac{v_{g\beta} \cdot i_{g\alpha} - v_{g\alpha} \cdot i_{g\beta}}{2} \quad (2.47)$$

where $v_{g\alpha}$, $v_{g\beta}$, $i_{g\alpha}$, $i_{g\beta}$ represent the Clarke transformation of grid voltage and current. α components are the same with system quantities. And the β components are $\frac{\pi}{2}$ lagged form of the system quantities.

Figure 2.14 shows OSG based power calculation. By using OSG system, the reference current for grid is calculated as seen in Equation 2.48.

$$i_g^* = \frac{(P_{ref} - P_{cal}) \cdot G_p(s) \cdot v_{g\alpha} + (Q_{ref} - Q_{cal}) \cdot G_q(s) \cdot v_{g\beta}}{v_{g\alpha}^2 + v_{g\beta}^2} \quad (2.48)$$

Figure 2.15 shows the grid reference current and usage of it to calculate the inverter gate signals.

The grid active and reactive powers are calculated by using single phase instantaneous PQ algorithms. The reactive power reference Q_{ref} need to be selected as zero to accomplish unity power factor. The value of the reference active power P_{ref} depends on the application and design specifications. In this way, the reactive

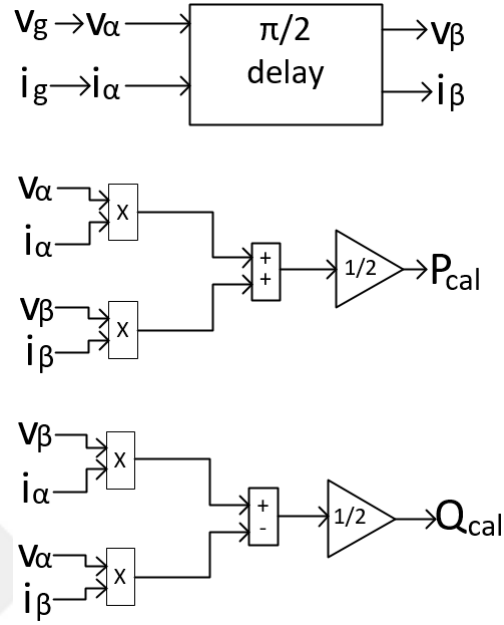


Figure 2.14 Orthogonal signal generator (OSG) based power calculation

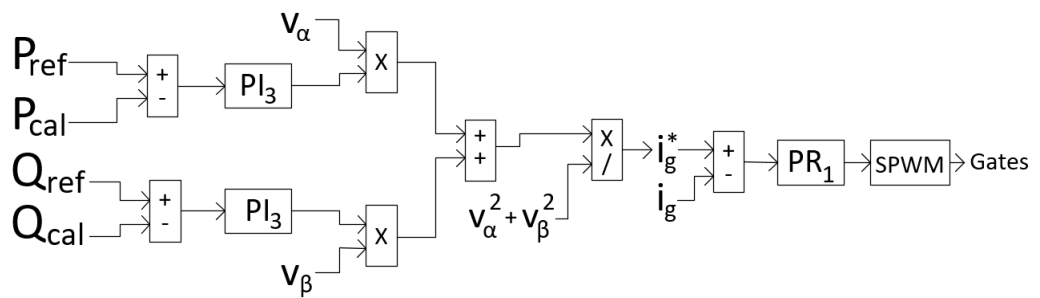


Figure 2.15 Produced reference grid current and gate signals

Table 2.2 Inverter design considerations

Parameters	Boost Converter	Inverter
The input voltage	104V	300V
The output voltage	300V	110V (RMS)
Nominal Power	524W	
Switching frequency	20kHz	
Line frequency	-	50Hz
The Voltage ripple	%1	
The current ripple	%10	

and the active power data will be in reference grid current. So, the system will produce a required grid current to reach reference active and reactive power value.

The formula of PR controller which is used in Figure 2.15 is given in Equation 2.49.

$$PR_1 = 2 \cdot [K_{P_{PR1}} + K_{R_{PR1}} \cdot \frac{s}{s^2 + \omega^2}] \quad (2.49)$$

where $K_{P_{PR1}}$ is the proportional constant and $K_{R_{PR1}}$ is the resonance constant.

2.3.3 Simulation

In this design, PV module and boost converter are used as specified in Table 2.1. Due to the design considerations give in Table 2.2, the voltage ripple can be calculated as seen in Equation 2.50.

$$\Delta V = 300 \cdot \frac{1}{100} = 3V \quad (2.50)$$

And the DC link capacitor can be calculated as given in Equation 2.51

$$C_{inv} = \frac{P_o}{2 \cdot \pi \cdot f \cdot V_{DC} \cdot \Delta V} = \frac{524}{2 \cdot \pi \cdot 50 \cdot 300 \cdot 3} = 1.9mF \quad (2.51)$$

The grid current rms value can be calculated:

$$I_{g_{rms}} = \frac{P}{V_{g_{rms}}} = \frac{524}{110} = 4.7636A \quad (2.52)$$

And the peak value is:

$$I_{g_{peak}} = I_{g_{rms}} \cdot \sqrt{2} = 6.7368A \quad (2.53)$$

So the maximum current peak can be calculated as following:

$$\Delta i_{L_{max}} = I_{g_{peak}} \cdot \%10 = 0.6737A \quad (2.54)$$

Substituting the values into Equation 2.45, inductance can be calculated:

$$L = \frac{300}{4 \cdot 20000 \cdot 0.6737} = 5.6mH \quad (2.55)$$

According to the Table 2.1 and Table 2.2, the system is constructed in MATLAB as given in Appendix 0.5 - Appendix 0.13. The steady state response and the transient response are analyzed in Figure 2.16 and Figure 2.17.

As seen from Figure 2.16, the MPPT algorithm tracing for the maximum power and it reaches to the maximum power point in a short term. At this point, the controller makes the DC bus voltage stay at the desired voltage level. Since the reference reactive power is specified as zero to reach the unity power factor, there is not any phase difference between the grid voltage and the grid current. The output voltage is at 300V as specified. As seen from Figure 2.17, voltage and the current ripple considerations are satisfied due to the design considerations.

If a constant DC input voltage is thought, the DC source shall supply $\frac{10\%}{2} = 5\%$ of the ripple power to be able to preserve 10% current ripple (peak to peak) on the input aspect. The graph of i_c shows these ripples in Figure 2.17.

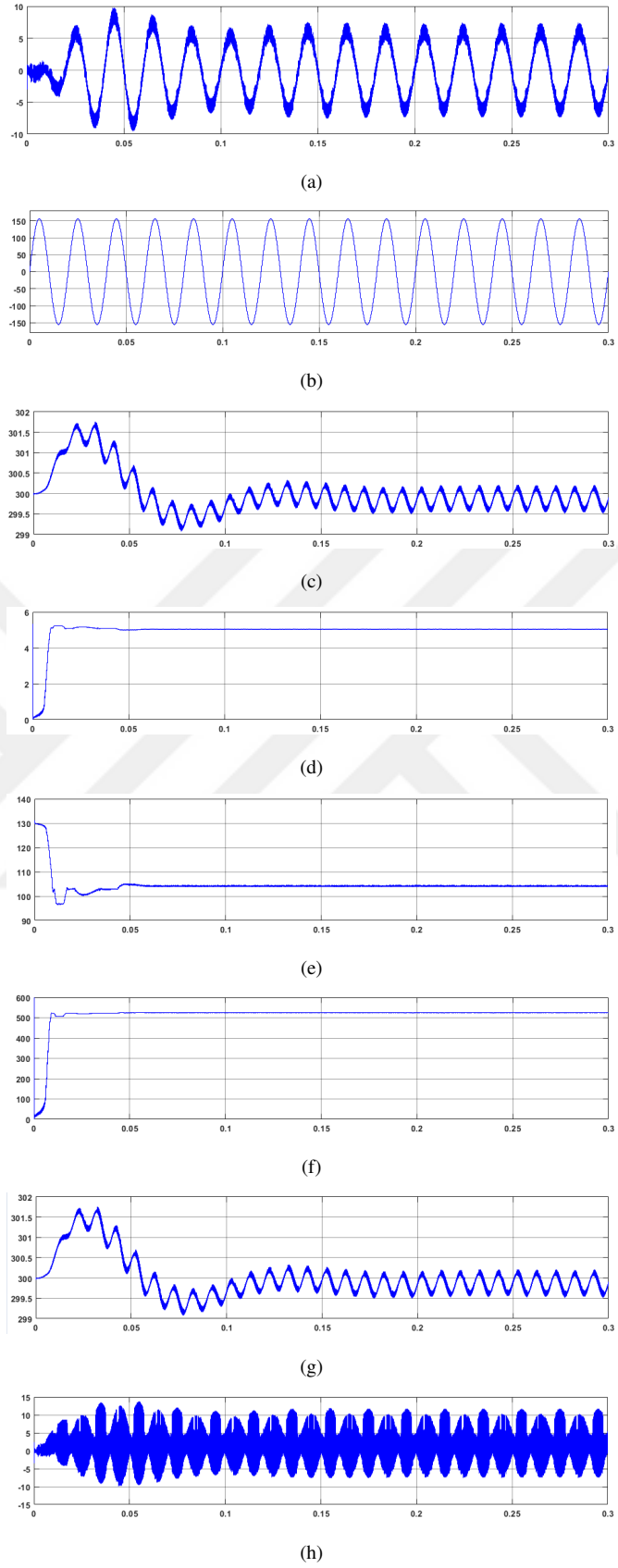
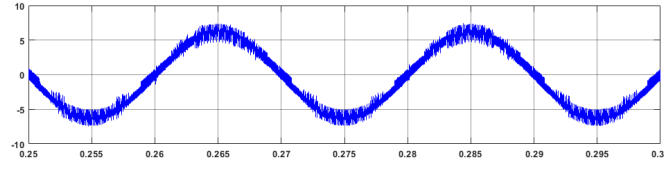
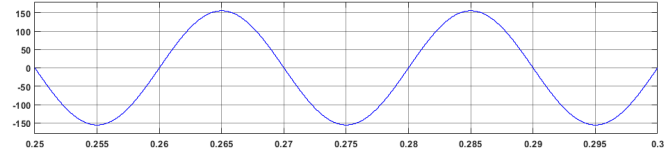


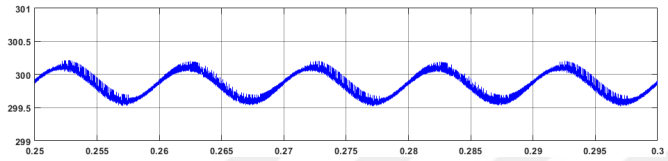
Figure 2.16 Transient analysis (start up) of the grid-connected inverter, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_c , (h) i_c



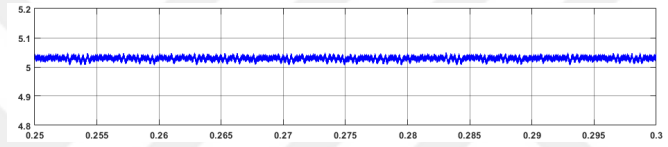
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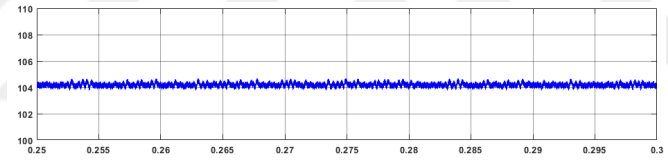
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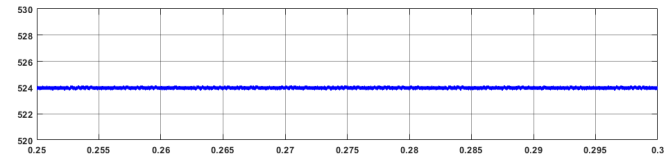
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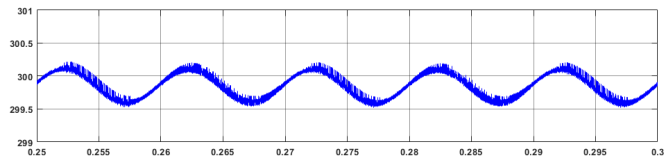
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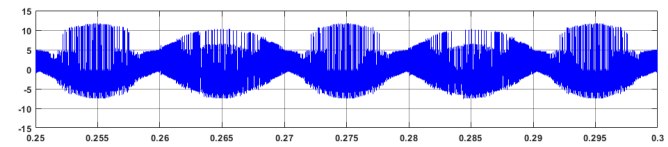
(e)



(f)



(g)



(h)

Figure 2.17 Steady state analysis of the grid-connected inverter, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_c , (h) i_c

CHAPTER THREE

ACTIVE POWER DECOUPLING

The electrolytic capacitor, which is placed on the DC side of the inverter, is used to passively decouple the power. Therefore APD circuit can be used instead of DC-link capacitor. There are several types of APD circuits. Figure 3.1 illustrates the APD topologies and single phase voltage source inverter which are studied in this thesis. APD circuits can be connected to inverter (Figure 2.12) from its DC+ and DC- ports. Figure 3.1a, 3.1b, 3.1c are examples of DC active power decoupling circuits and Figure 3.1d is the example of AC active power decoupling.

The APD methods can be categorised into DC and AC decoupling according to its operation modes. The categorization depends on the voltage of the decoupling capacitor. If it is required to alternate its polarity, categorized as AC decoupling, if not, categorized as DC decoupling. The frequency of the ripple voltage is another fact. For the DC decoupling method, the frequency of ripple voltage is two times the grid frequency. For the AC decoupling method, it is similar to the grid frequency. The capacitor in AC decoupling circuit stores less energy with respect to the DC decoupling (Qin et al., 2016).

The APD method, which can significantly reduce the capacitor requirements, is used to decouple power. In boost type DC APD method (Figure 3.1a), the capacitor voltage is always greater than input voltage (DC). Instead of the DC-link capacitor, the APD circuit supply ripples current to the grid. Boost type APD circuit carry the ripple current (i_f) and its capacitor voltage have double line frequency instead of DC-link capacitor. APD circuit decouples the power by supplying current to the grid or by drawing current from the grid.

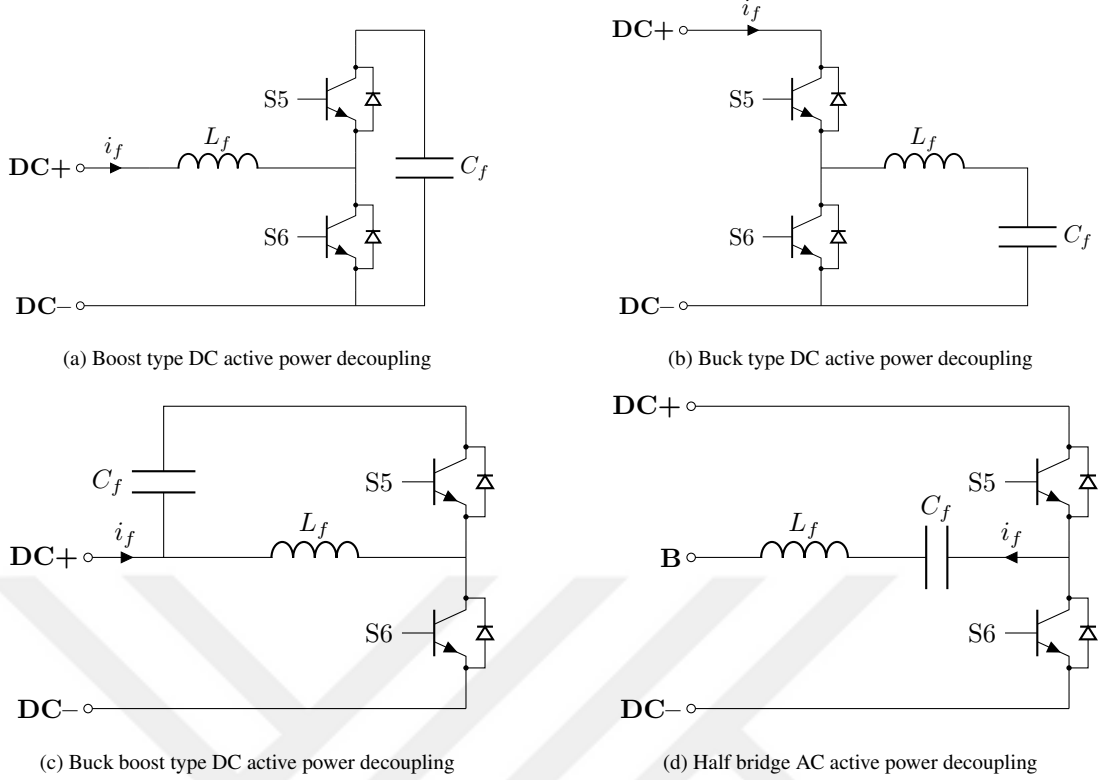


Figure 3.1 The decoupling circuits

3.1 Boost Type DC Active Power Decoupling

E-cap is removed from Figure 2.12 and APD circuit is placed and the overall system is constructed as given in Figure 3.2. The output capacitor of the boost converter which has a very small capacitance is remained connected.

3.1.1 Circuit Topology

The Boost type APD circuit can be analyzed due to its switches (S_5 and S_6). While S_5 is turned on and S_6 is turned off (Figure 3.3a), if the APD circuit draws current from the grid ($i_f > 0$), the inductor voltage will be negative since the capacitor voltage is always greater than input voltage and i_f will decrease. If APD circuit supplies current to the inverter ($i_f < 0$), the inductor voltage will be positive and i_f will increase.

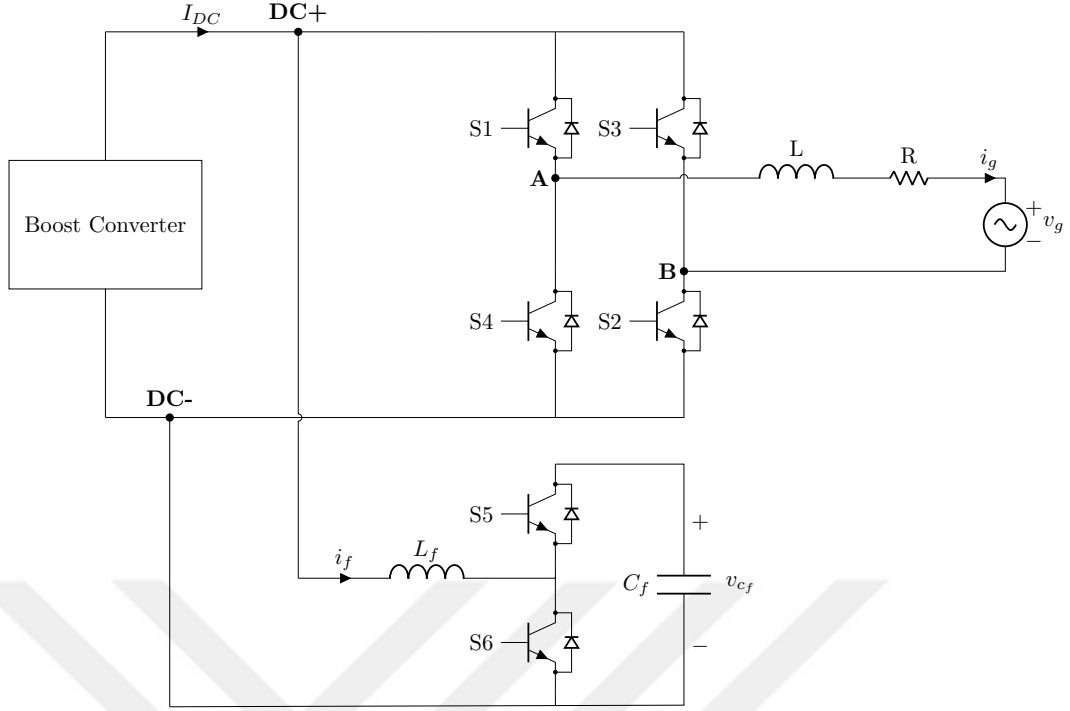


Figure 3.2 Grid connected h bridge inverter with boost type APD circuit

While S_5 is turned off and S_6 is turned on (Figure 3.3b), the inductor voltage should be equal to the input voltage. So, filter current i_f increases while the APD circuit is drawing current from the grid, and i_f decreases while supplying current to the grid.

As seen from APD circuit analysis, according to inverter quantities, i_f the current can be easily controlled by switch S_5 and S_6 . Here the inductor L_f is used to boost input voltage to v_{cf} . The capacitor needs to be selected according to the design specifications. The capacitance value depends on the ripple power, the maximum capacitor voltage and the voltage ripple on the capacitor. The desired decoupling capacitance can be approximated to be (Krein et al., 2012):

$$C_f = \frac{P_r}{2 \cdot \omega_n \cdot \Delta V_{r2} \cdot (V_{c_{max}} - \Delta V_{r2})} \quad (3.1)$$

where ΔV_{r2} stands for voltage ripple of the decoupling capacitor C_f due to design considerations.

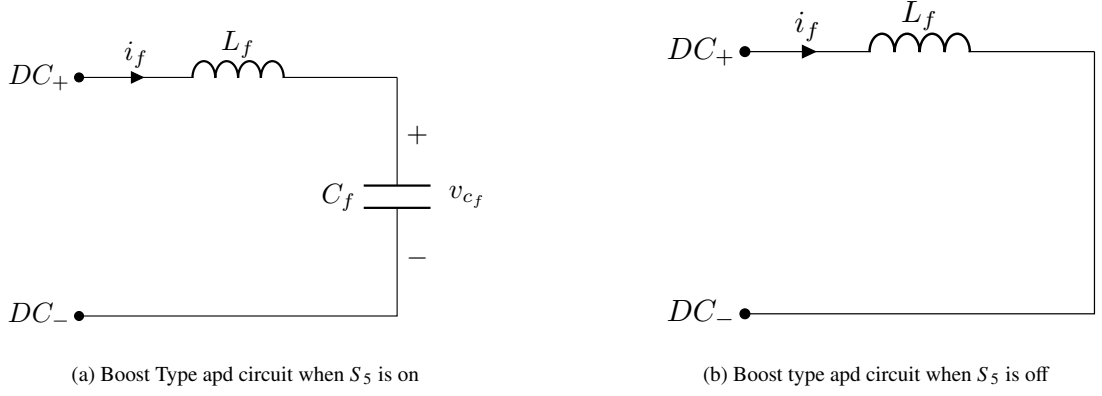


Figure 3.3 Boost type decoupling circuit modes

3.1.2 Control Algorithm

According to Equation 2.27, ripple power can be compensated by explicitly regulating the decoupling current i_f to be sinusoidal whose frequency is two times grid frequency as following (Pradeep Kumar & Fernandes, 2018):

$$i_f^* = \frac{-P_r}{V_{DC}} = \frac{V_o \cdot I_o \cdot \cos(2 \cdot \omega_n \cdot t + \phi)}{V_{DC}} \quad (3.2)$$

Rearrange Equation 3.2:

$$i_f^* = \frac{P_o}{V_{DC}} - \frac{v_g \cdot i_g}{V_{DC}} \quad (3.3)$$

where i_f^* is the reference current for decoupling current. To cancel the DC component $\frac{P_o}{V_{DC}}$ is used. But instead of this expression, the DC component can be eliminated easily by using a band-pass filter $G_{BPF}(s)$. This filter is tuned to pass only the second harmonic component ($2\omega_n$) of the current. So, the current reference can be expressed as:

$$i_f^* = -\frac{v_g \cdot i_g}{V_{DC}} \cdot G_{BPF}(s) = D_o \cdot i_g \cdot G_{BPF}(s) \quad (3.4)$$

$$G_{BPF}(s) = \frac{BW \cdot s}{s^2 + BW \cdot s + (2\omega_n)^2} \quad (3.5)$$

where BW is the bandwidth of the band-pass filter and D_o is the instantaneous duty ratio of the inverter ($\frac{v_g}{V_{DC}}$).

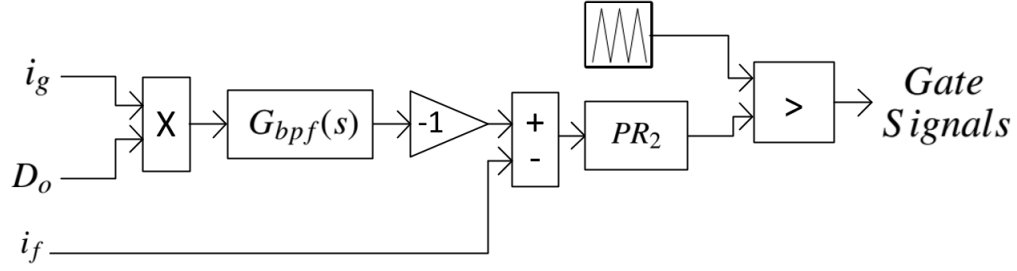


Figure 3.4 Gate signal generator of the decoupling circuit

After generating the instantaneous duty ratio, the reference current for the decoupling circuit can be generated as constructed in Figure 3.4.

Since the reference current is an AC signal, additional PR controller (Equation 3.6) required to generate duty signal and the gate signals.

$$PR_2 = 2 \cdot [K_{PR2} + K_{RPR2} \cdot \frac{s}{s^2 + \omega^2}] \quad (3.6)$$

where K_{PR2} is the proportional constant and K_{RPR2} is the resonance constant.

3.1.3 Simulation

Table 3.1 Decoupling circuit design considerations

Parameters	Value
Maximum voltage of filter capacitor	650 V
Voltage ripple of filter capacitor	%10

In this design, boost converter and PV module are used as specified in Table 2.1 and inverter is used as specified in Table 2.2. According to the Table 3.1 and Equation 3.1, the filter capacitor can be calculated:

$$C_f = \frac{524}{2 \cdot (2 \cdot \pi \cdot 50) \cdot 65 \cdot (650 - 65)} = 22\mu F \quad (3.7)$$

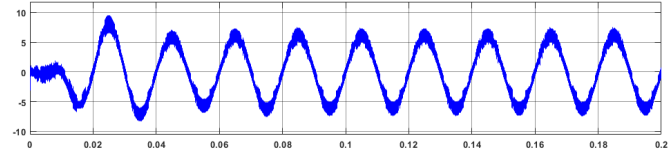
The band-pass filter can be determined as follows:

$$G_{BPF}(s) = \frac{2 \cdot 0.33 \cdot 2 \cdot \omega_n \cdot s}{s^2 + 2 \cdot 0.33 \cdot 2 \cdot \omega_n \cdot s + (2\omega_n)^2} \quad (3.8)$$

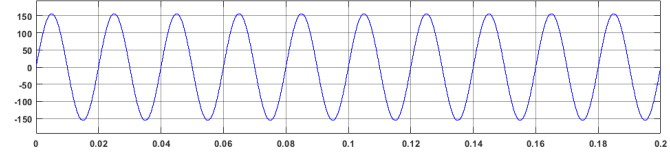
The discrete form of the band pass filter is calculated with the help of a MATLAB script as seen in Appendix 0.14.

According to the design considerations, the system is constructed in MATLAB as given in Appendix 0.15 - Appendix 0.18. The steady state response and the transient response of the system are analyzed in Figure 3.5 and Figure 3.6.

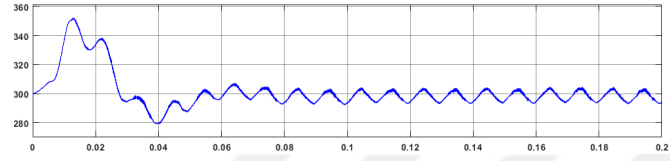
As seen from Figure 3.5, MPPT algorithm works properly to track maximum power and the decoupling circuit works properly to achieve unity power factor and keep input voltage as a DC voltage. The filter capacitor voltage is always greater than the DC link voltage since boost type decoupling circuit is used.



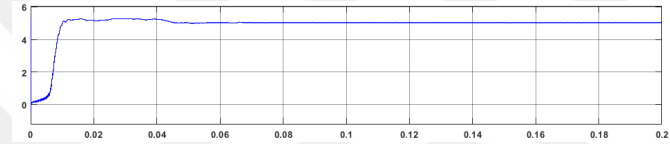
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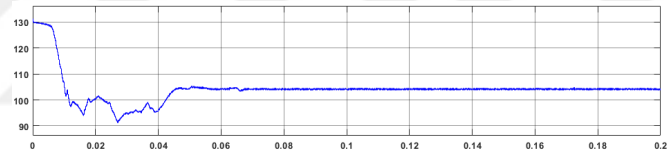
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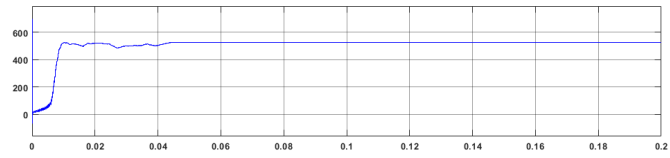
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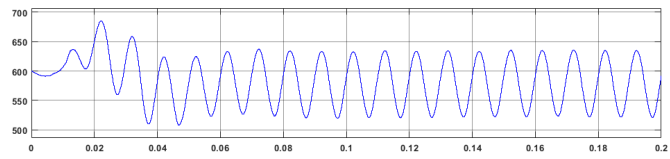
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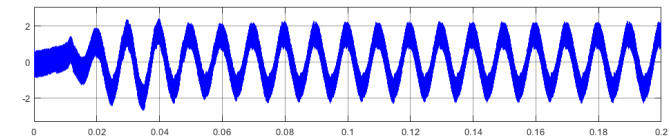
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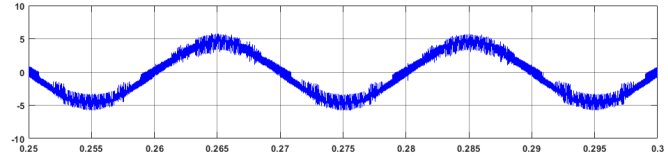


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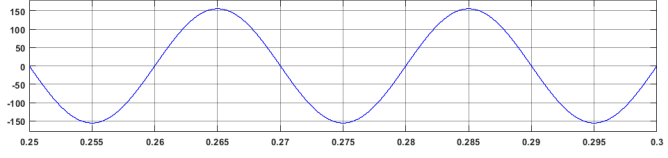


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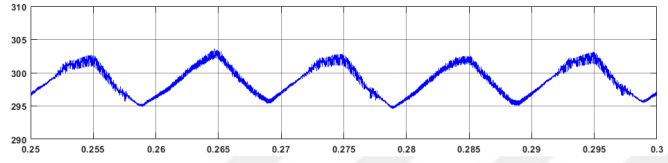
Figure 3.5 Transient analysis (start up) of the overall system with boost type APD circuit, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_{cf} , (h) i_f



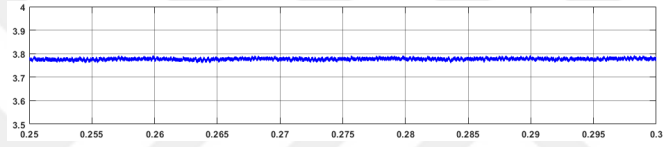
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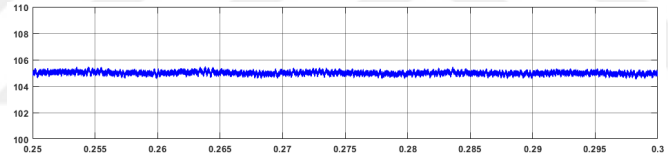
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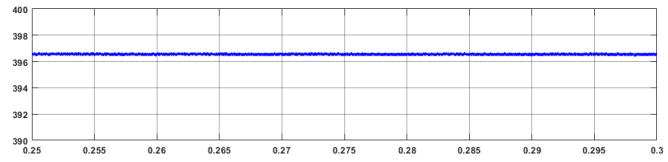
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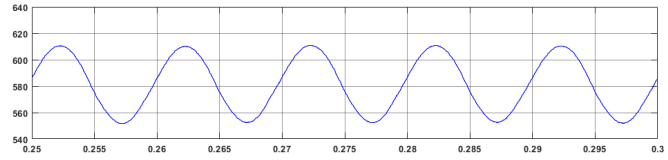
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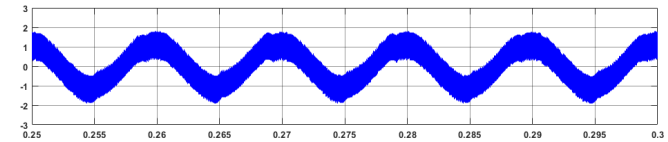
(e)



(f)



(g)



(h)

Figure 3.6 Steady state analysis of the overall system with boost type APD circuit, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_{cf} , (h) i_f

And i_f and v_{cf} are double frequency components as specified in Equation 2.28. As seen from Figure 3.6, the voltage ripple requirements are satisfied due to Table 2.1, Table 2.2 and Table 3.1.

To observe the transient response properly, irradiance of the PV array is changed after 0.1 sec. That will affect to the power and system shall adapt this change quickly.

As seen from Figure 3.6, at 0.1 sec, power lost occurs and the MPPT algorithm tracing the new maximum power point. During that time decoupling circuit adapt itself to this change and avoid the phase difference between the grid voltage and the current.

3.2 Buck-Boost Type DC Active Power Decoupling

Instead of boost type decoupling circuit, buck boost type decoupling circuit is connected to the DC ports of the inverter and the system is constructed as given in Figure 3.7.

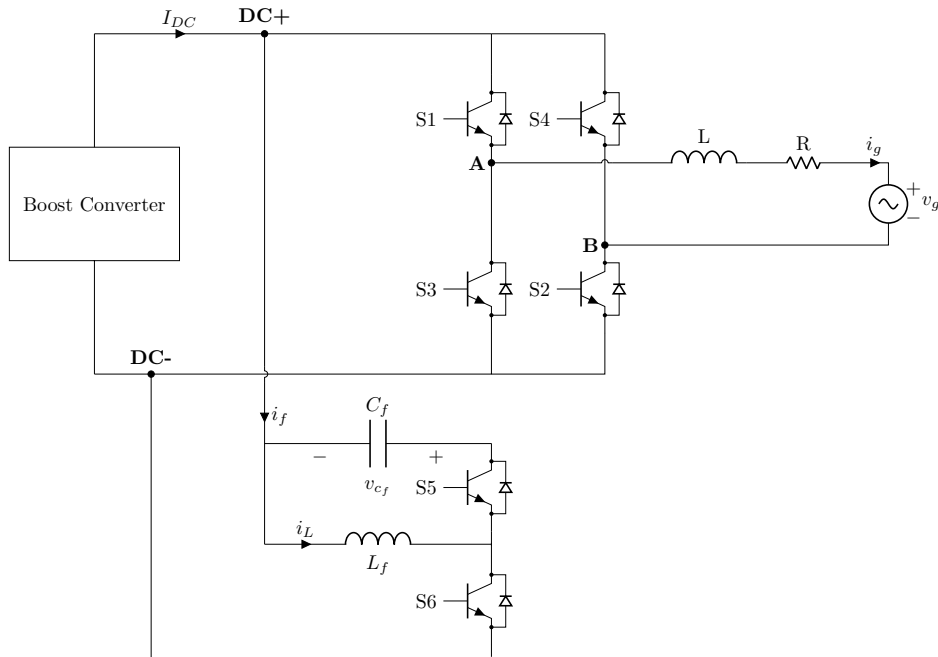


Figure 3.7 Grid connected H-bridge inverter with buck-boost type APD circuit

3.2.1 Circuit Topology

The buck boost type APD circuit can be analyzed due to its switches S_5 and S_6 . While S_5 is turned on and S_6 is turned off (Figure 3.8), $i_f = 0$ which means the decoupling circuit will not draw any current from DC link and will not supply any current to DC link. In this case $i_C = -i_L$.

While S_5 is on, if i_L is positive, the inductor will be discharged and the capacitor will be charged. If i_L is negative, the inductor will be charged and the capacitor will be discharged.

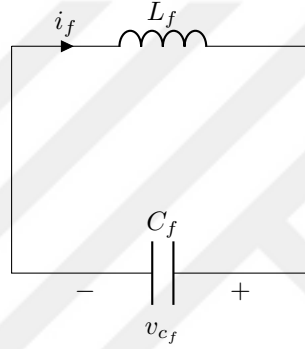


Figure 3.8 Buck boost type APD circuit when S_5 is on

While S_5 is turned off and S_6 is turned on (Figure 3.9), $i_f = i_L$. While S_5 is off, if i_L is positive, the inductor will be charged. If i_L is negative, the inductor will be discharged. In this case $i_C = 0$, so the capacitor will remain its status.

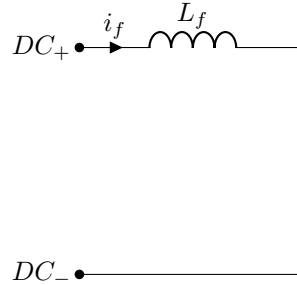


Figure 3.9 Buck boost type APD circuit when S_5 is off

Equation 3.1 can be used to calculate the capacitance.

3.2.2 Control Algorithm

The control algorithm of the boost type decoupling circuit (Section 3.1.2) can be also used for buck boost type decoupling circuit.

3.2.3 Simulation

In this design, all components are the same in boost type decoupling circuit. Only the places of the components are changed and the buck boost type decoupling circuit is created (Appendix 0.19). The steady state response and the transient response of the system are analyzed in Figure 3.10 and Figure 3.11.

As seen from Figure 3.10, MPPT algorithm works properly to track maximum power and the decoupling circuit works properly to achieve unity power factor and keep input voltage as a DC voltage. Since buck boost type decoupling circuit is implemented in this design, the filter capacitor voltage may be greater or less than the DC link voltage.

As seen from Figure 3.11, the voltage ripple requirements are satisfied due to Table 2.1, Table 2.2.

Eventually it can be seen that small ripples as specified in design considerations are observed in DC link voltage and the ripple power are generated by the decoupling circuit. That means decoupling circuit can be successfully used instead of bulky size electrolytic capacitor.

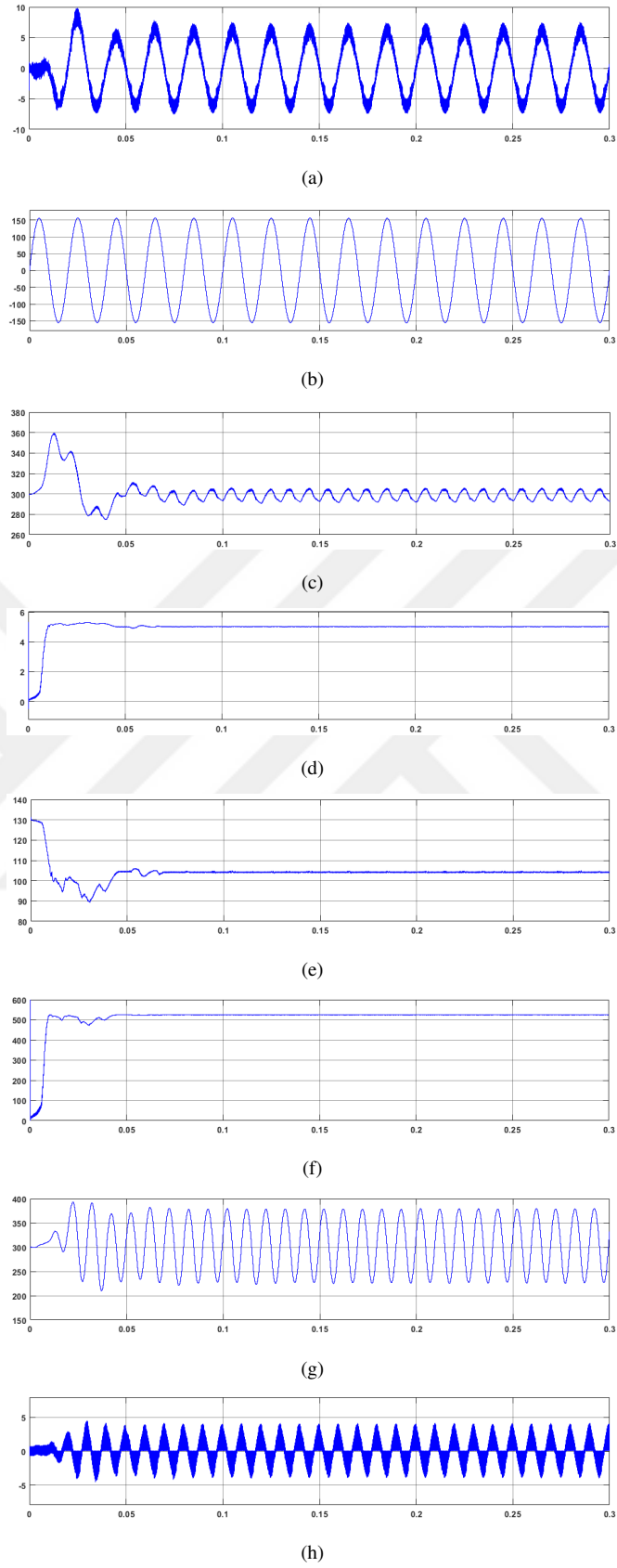


Figure 3.10 Transient analysis (start up) of the overall system with buck-boost type APD circuit, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_{cf} , (h) i_f

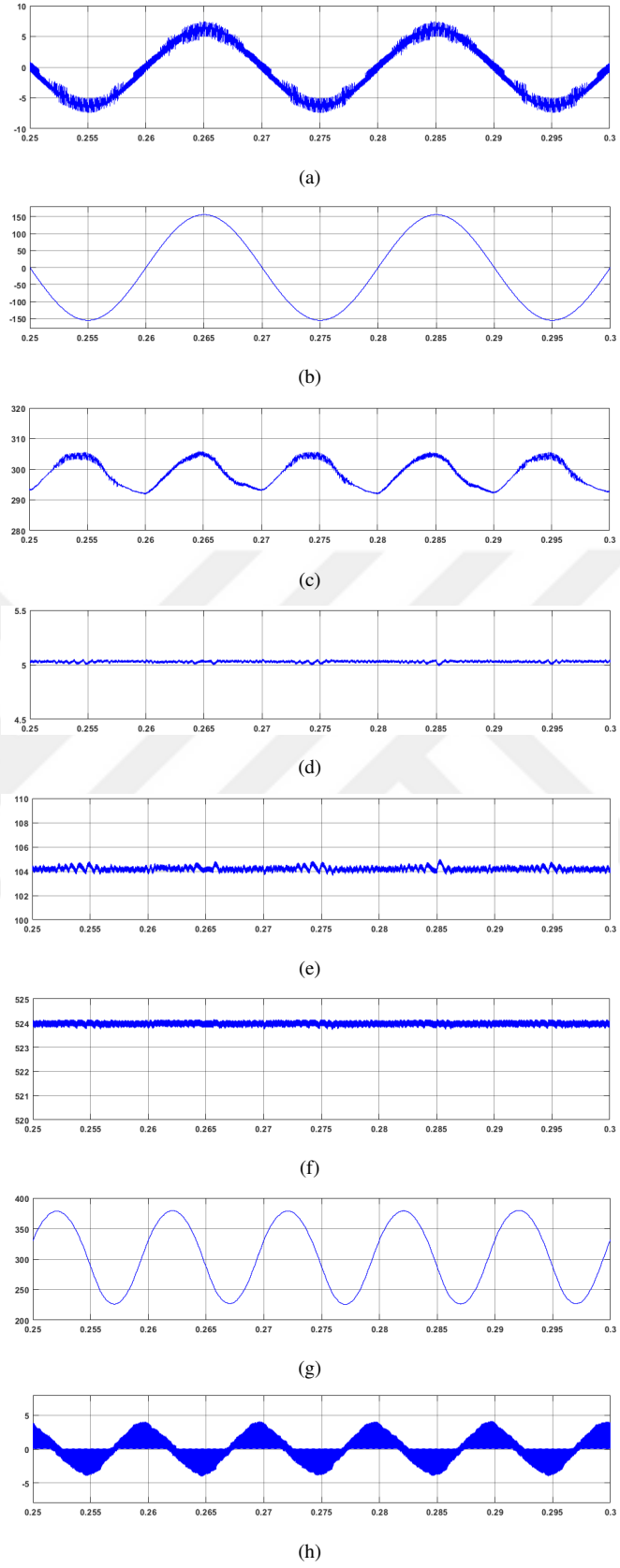


Figure 3.11 Steady state analysis of the overall system with buck-boost type APD circuit, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_{cf} , (h) i_f

CHAPTER FOUR

HARDWARE IN THE LOOP

Hardware in the loop (HIL) simulation is a method running on an supposed target controller for validating the control algorithm, by means of developing a digital real-time environment that represents the physical device to control. The test device that simulates reality is linked to actual signals from a controller. The controller is tricked into thinking it is inside the assembled product. Without physical prototypes, HIL allows to test the behaviour of the control algorithms. Iterations of design and test take place as even though the real-world system is getting used. To correctly workout the controller, heaps of feasible eventualities may be run without the price and time related to actual physical tests.

Within the automotive, aerospace and defence, and industrial automation and machinery industries, HIL simulation is extensively used to test embedded designs. In clinical gadgets, communications, semiconductors, and other industries HIL is likewise being followed.

4.1 HIL Setup

In this thesis, MATLAB/SIMULINK is used for HIL. The model of the hardware is constructed in SIMULINK and the controller signals are processed in this model. The controller is from C2000 family of Texas Instruments. To construct a HIL model in MATLAB, first of all "Embedded Coder Support Package" must be installed to communicate with microprocessor. During this installation, all necessary software packages will be pointed to be installed (APPENDIX 0.20). Once all necessary software packages are installed, MATLAB platform is ready for HIL. The blocks for the TI micro-controllers can be observed in Simulink Library Browser (APPENDIX 0.21).

Since the hardware is constructed in MATLAB, the controller must communicate with the computer. And this communication can be performed via serial

communication. Serial communication blocks can be found in embedded coder library (Figure 4.1). In these blocks, the communication port must be specified. The proper port can be found in device manager in PC. In serial configuration, the baudrate is really important to determine. Because, it determines the data transmission. That defines how many data can be send via that port. The timeout is also important for the simulation time. Because that property determines how much time MATLAB will wait for another data. For instance, if it is determined as 1 sec, and the simulation step is 1 us, and simulation time 1 ms, that means HIL simulation will finished in 1000 sec. So firstly, the time for 1 cycle of the controller software must be observed and this property must be set accordingly.

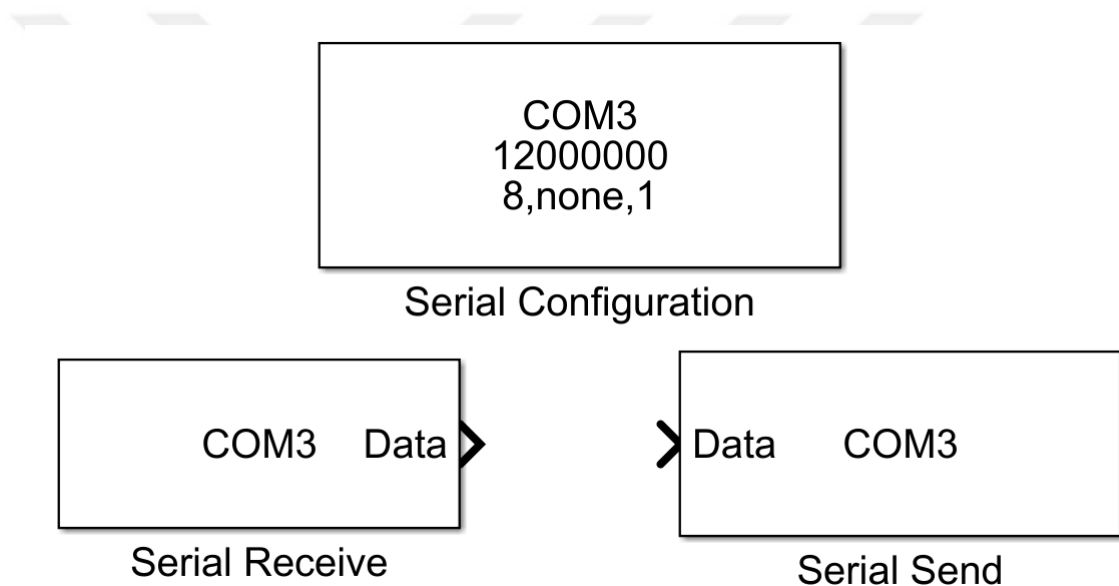


Figure 4.1 Serial communication blocks

"Serial Receive" is used to get data from the specified port. In this block, "Header" and "Terminator" must be determined. The controller must place the data between these header and terminator and then transmit it to the port. With this way, this blocks get the proper data from the received data. Also the "Data size" must be determined here. This block also need to parse the data and to do that it need the data size. If three variable is sent via serial communication port, then "Data size" must be [3 1].

"Serial Send" is used to send data to the specified port. "Header" and "Terminator" must be determined also in this block. Because, also the controller must get proper

data from the received data.

The controller that is used in this thesis (TI Delfino F28379D LaunchPad) doesn't support floating numbers. So, the data must be sent in integer form. Because of this reason, the value must be multiplied with specified value before it is sent. If 6 floating digits are necessary, the value must be multiplied by 10^6 before it is sent via serial send block. And also the data comes from serial receive block must be divided to the same value (10^6 due to the previous example).

4.2 Software Generation for the Controller

There is also software generation option in MATLAB for TI controllers. The control algorithm can be constructed in another simulink window and it can be built. During the necessary SW implementation, MATLAB also requires to install Code Composer Studio. That software is used to flash TI controllers. So, in the simulink window, there is a tab named "C CODE" and the constructed simulink project can be built from this tab. With building the project (APPENDIX 0.22), code will be generated and the flashed directly to the controller if the controller is connected to the PC.

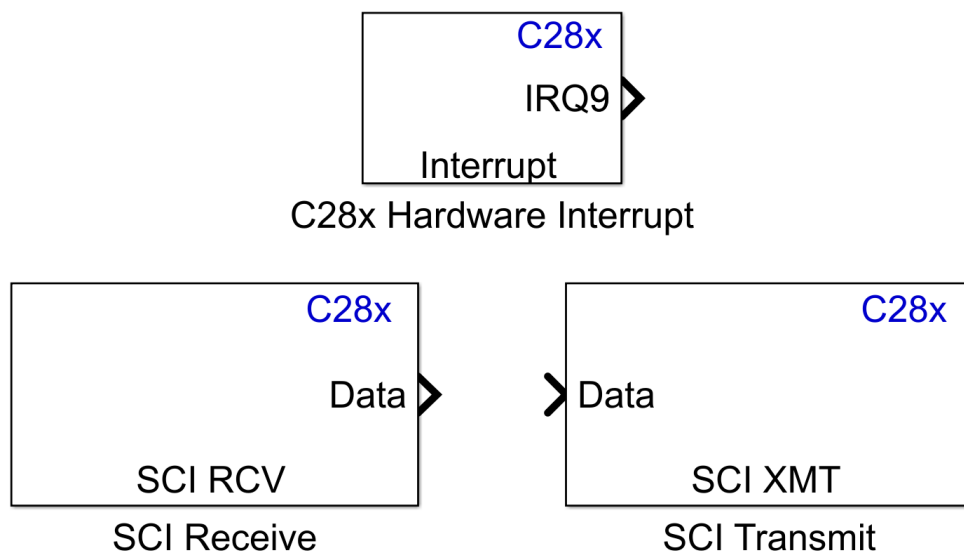


Figure 4.2 Serial communication blocks for code generation

There are serial communication blocks for code generation. The Serial

Communication Interface (SCI) blocks (Figure 4.2) allow controller to communicate via serial communication ports. In SCI Receive block, header and terminator must be same parameter as in Serial Send block which is used in hardware part. And the data length must be specified in this block. If 5 variable are sent via Serial Send block in hardware part, data length must be chosen as 5 in SCI Receive block. Another important point is SCI Module property, the controllers have more than one SCI module. So proper module must be chosen and its properties must be set in the settings. For example, if SCI Module A is used in SCI Receive block, in the hardware implementation settings, the baud rate of SCI A module must be arranged as in Serial Configuration block which is used in hardware part (APPENDIX 0.23). In this settings also GPIO pins can be arranged for real hardware. Because the real signals can be sent via TX and RX channels.

SCI transmit is used to send signals via communication port. Here the important block is C28x Hardware Interrupt block. This block detects if a signal received. Go to help section of this block and find the proper port to detect. Since SCI module A is used in this thesis, the proper peripheral interrupt (PIE) number and CPU number must be determined accordingly (APPENDIX 0.24). By the help of this block software will check if there is an interrupt from hardware model. Once hardware model send signals via communication port, Hardware interrupt block will detect that signals are received and it will allow control algorithm to process that signals as seen from Figure 4.3.

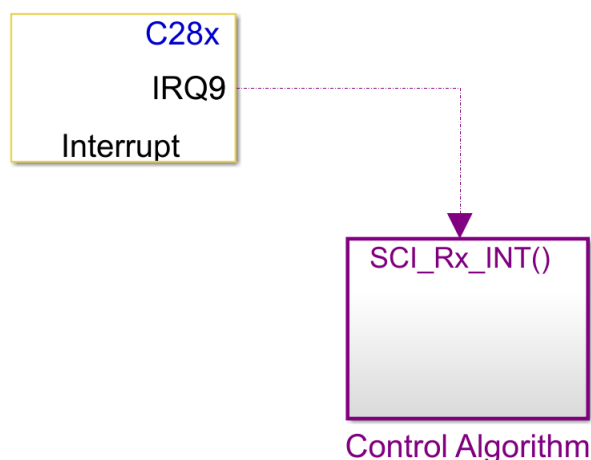


Figure 4.3 Hardware interrupt implementation

4.3 HIL Simulation of Boost converter

HIL model of Boost converter is constructed as in Figure 4.4.

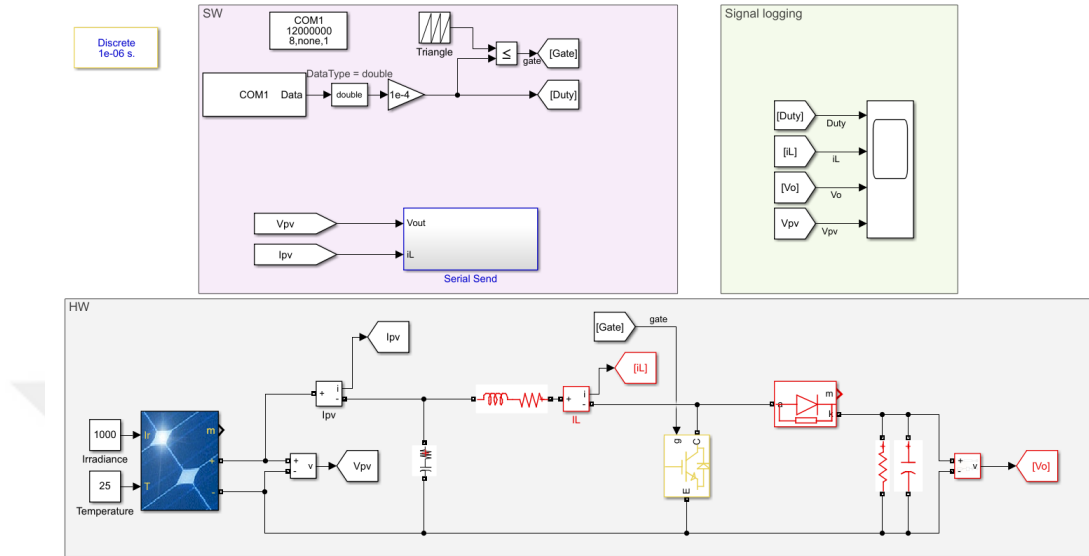


Figure 4.4 HIL model of boost converter

The sensed signals are sent via Serial Send block (APPENDIX 0.25) to the communication port to communicate with controller. In this block rate transition is used to determine sampling frequency. And also there is 10^4 gain to send 4 floating digit.

The signals will be used in the controller and the duty will be sent to the MATLAB. And HIL model will receive that signal from serial receive block. 10^{-4} gain must be used to get proper data since it was sent with 10^4 gain. After that gate signal is generated.

To generate the software and flash it to the controller, software model is constructed as seen in Figure 4.5.

Since it is sent with 10^4 gain, SW shall use these variables with 10^{-4} gain. But before that it must be converted to the double, because they are integer values. If they are not converted, the digits after comma will be lost. The duty generator block (APPENDIX 0.3) is used to generate duty, same block as used in chapter 2.

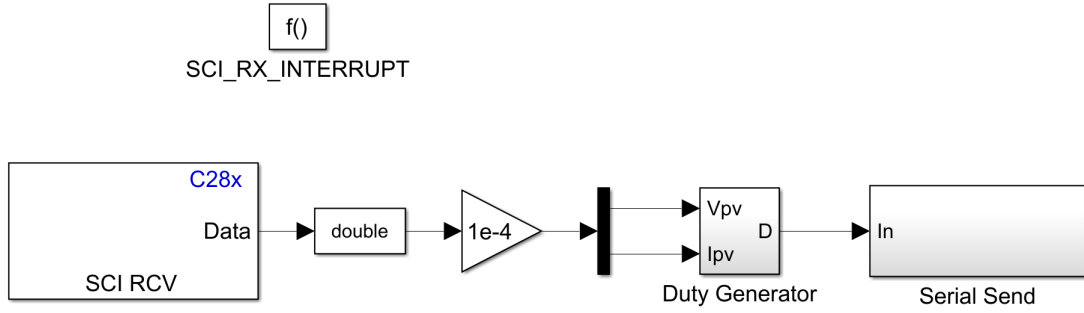


Figure 4.5 Software model of boost converter

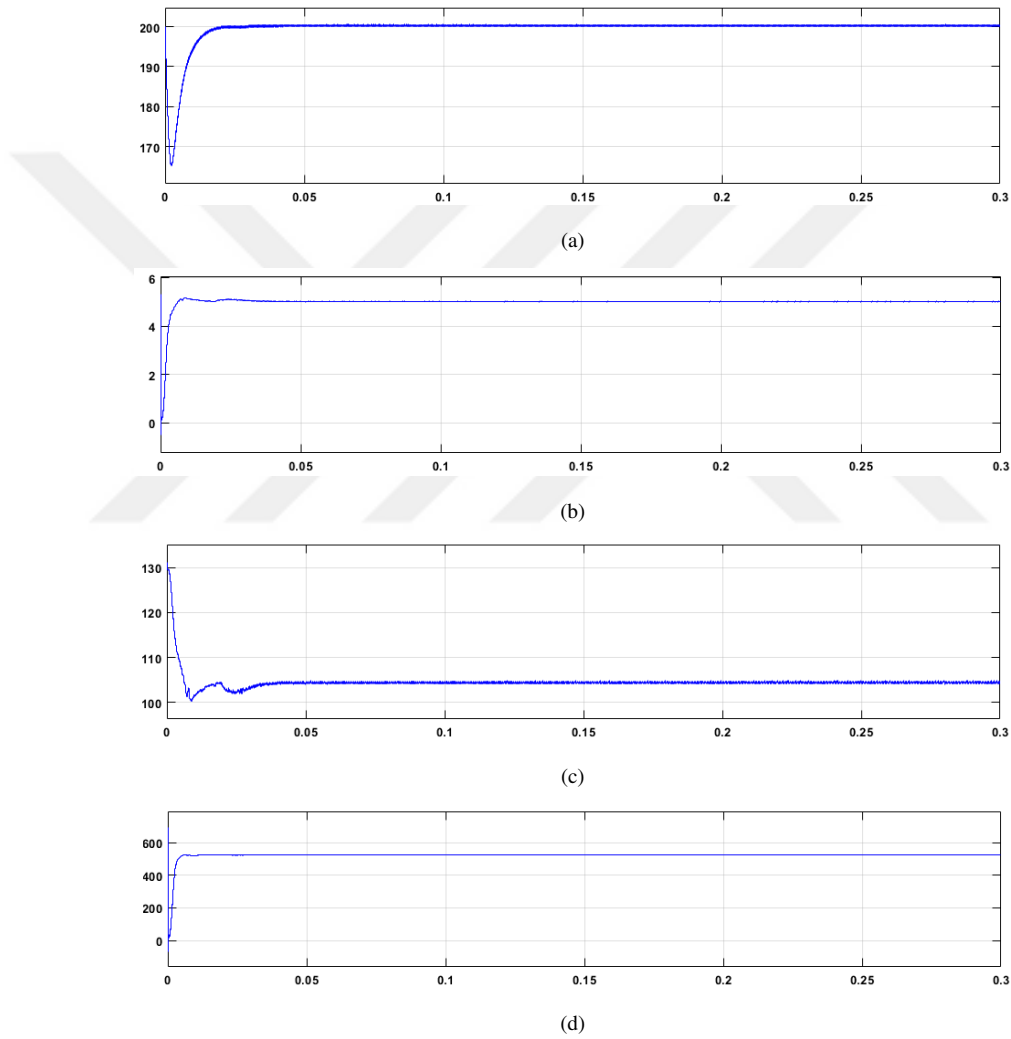


Figure 4.6 Transient analysis (start up) of HIL model of boost converter, (a) V_{DC} , (b) i_{pv} , (c) v_{pv} , (d) p_{pv}

Once duty is calculated, it is sent by Serial Send block (APPENDIX 0.26). Serial Send block first apply 10^4 gain to the data and then add header at the beginning of the data and add terminator at the end of the data. Finally, send the prepared data with SCI

Transmit block.

Once the software is flashed to the controller, the overall HIL system is ready for testing. The transient analysis and steady state responses can be observed in Figure 4.6 and Figure 4.7.

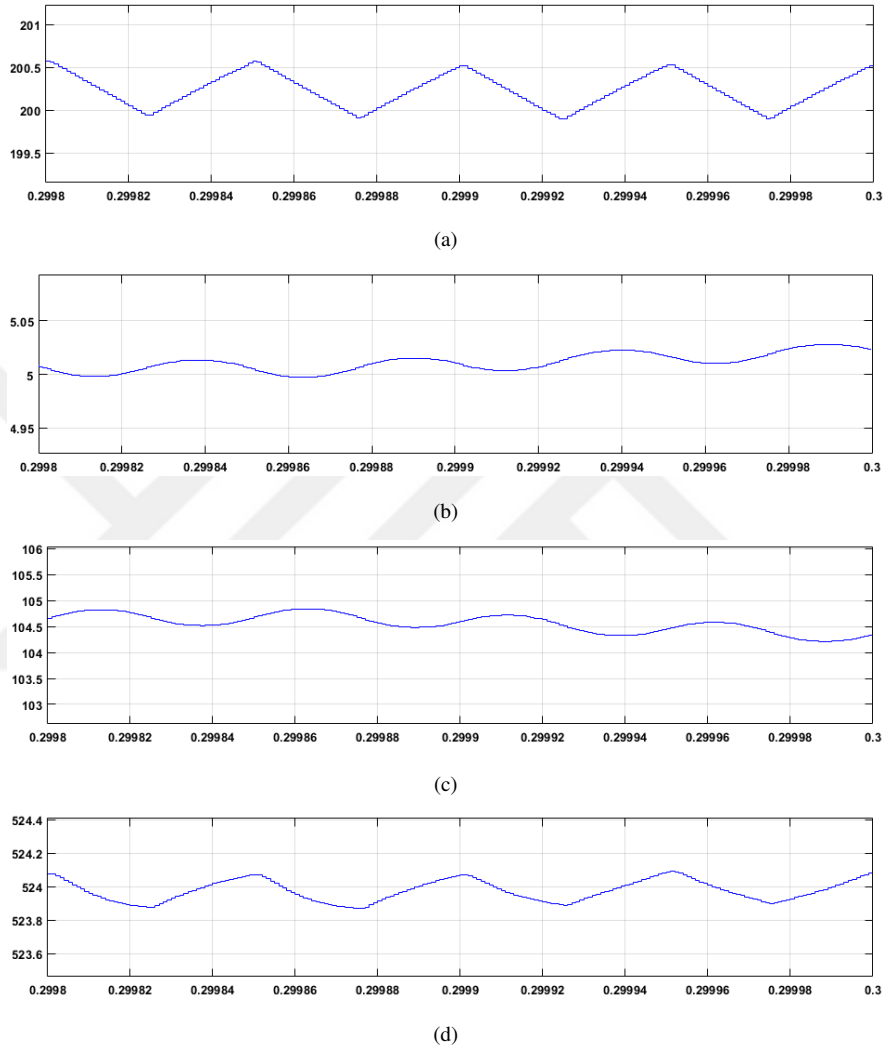


Figure 4.7 Steady state response of HIL model of boost converter, (a) V_{DC} , (b) i_{pv} , (c) v_{pv} , (d) p_{pv}

The transient response and the steady state graphs are almost identical as simulated ones (Figure 2.9, Figure 2.10). It shows that the software can be used in a real circuit.

4.4 HIL Simulation of Inverter

After HIL simulation of the boost converter worked correctly, HIL model of the inverter is placed as output to the boost converter as in Figure 4.8.

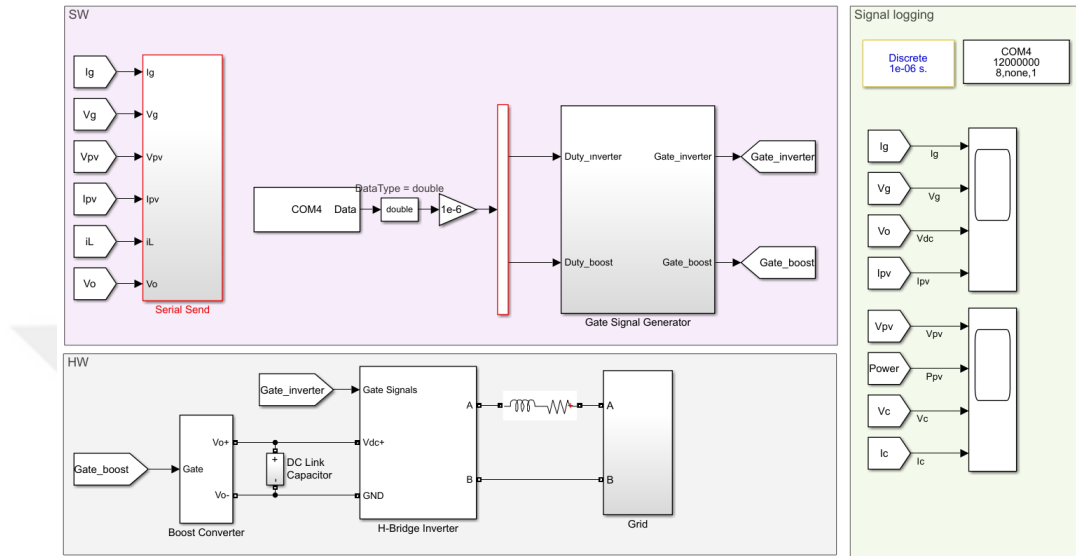


Figure 4.8 HIL model of inverter

The sensed signals are sent via Serial Send block (APPENDIX 0.27) to the communication port. 10^6 gain is used to get into account 6 floating digit. The signals will be used in the controller and the duty signals of the boost converter and the inverter will be sent to the MATLAB. And HIL model will receive those duty signals and generate gate signals.

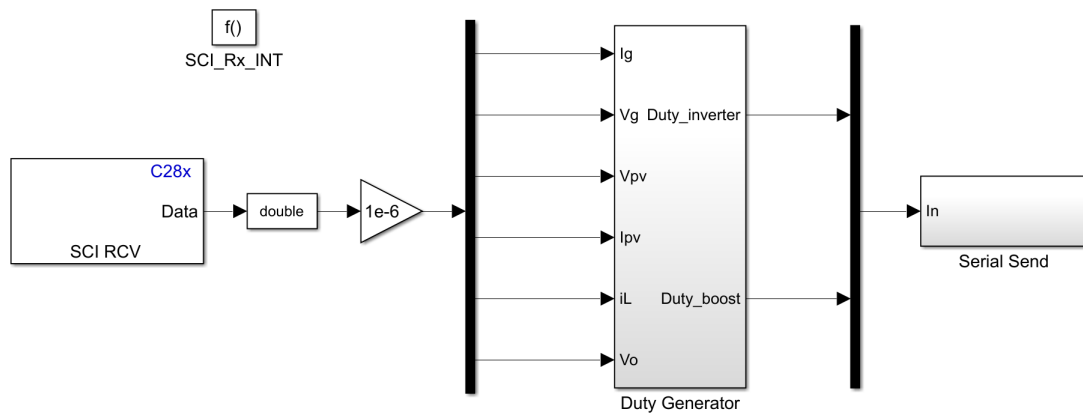


Figure 4.9 Software model of the inverter

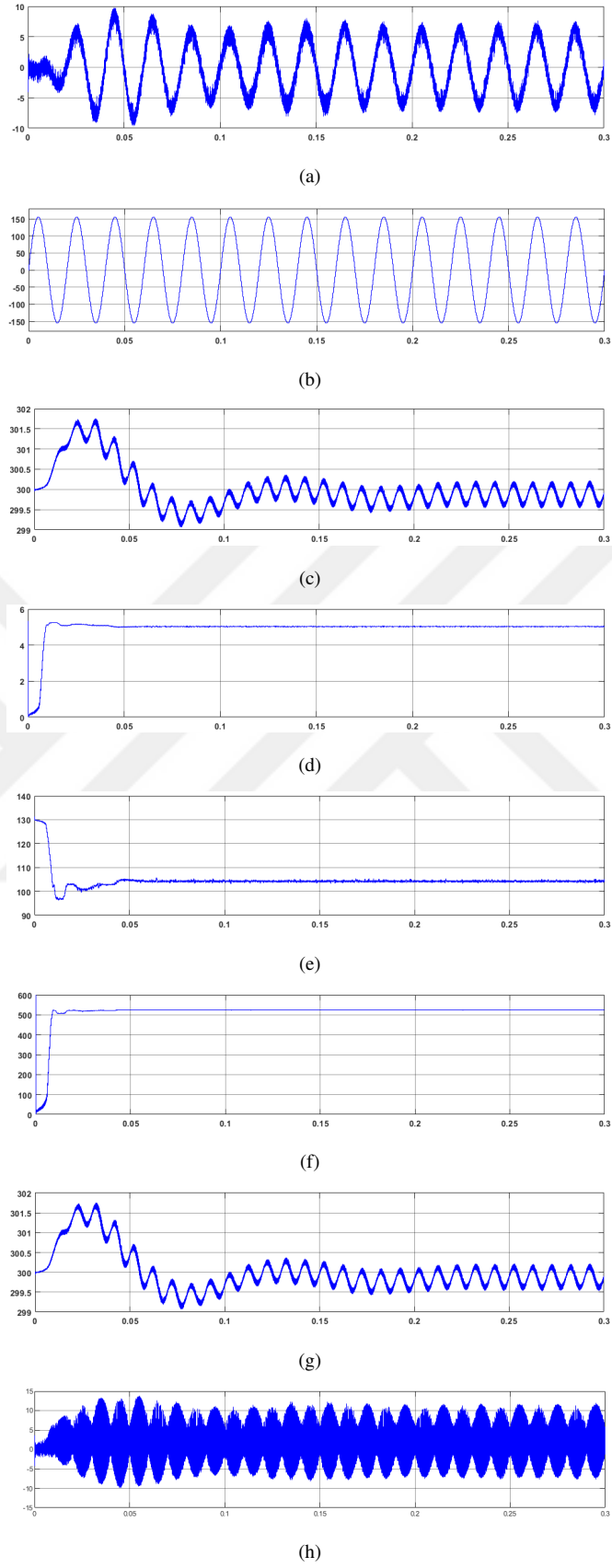


Figure 4.10 Transient analysis (start up) of HIL model of inverter, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_{cf} , (h) i_f

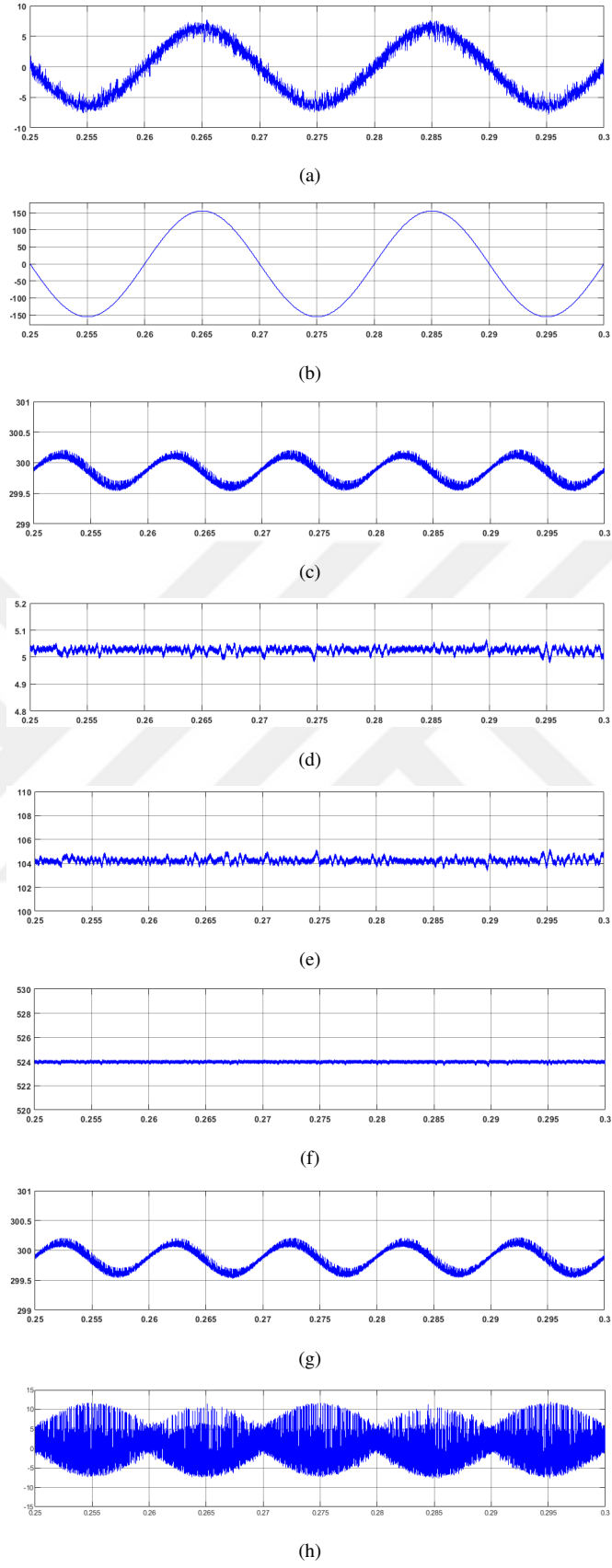


Figure 4.11 Steady state analysis of HIL model of inverter, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_{cf} , (h) i_f

To generate the software, software model is constructed as seen in Figure 4.9.

The duty generator block (APPENDIX 0.5) is used to generate duty, same block as used in chapter 2. Once the software is flashed to the controller, the overall HIL system is ready for testing. The transient analysis and the steady state response is visible in Figure 4.10 and Figure 4.11.

Transient response and steady state graphs are almost identical as simulated ones (Figure 2.16, Figure 2.17). The ripple levels are expected as defined Table 2.2 It shows that the software can be used in a real circuit.

4.5 HIL Simulation of Boost Type Decoupling Circuit

After HIL simulation of the inverter worked correctly, HIL model of the boost type DC decoupling circuit is inserted instead of DC link capacitor as in Figure 4.12.

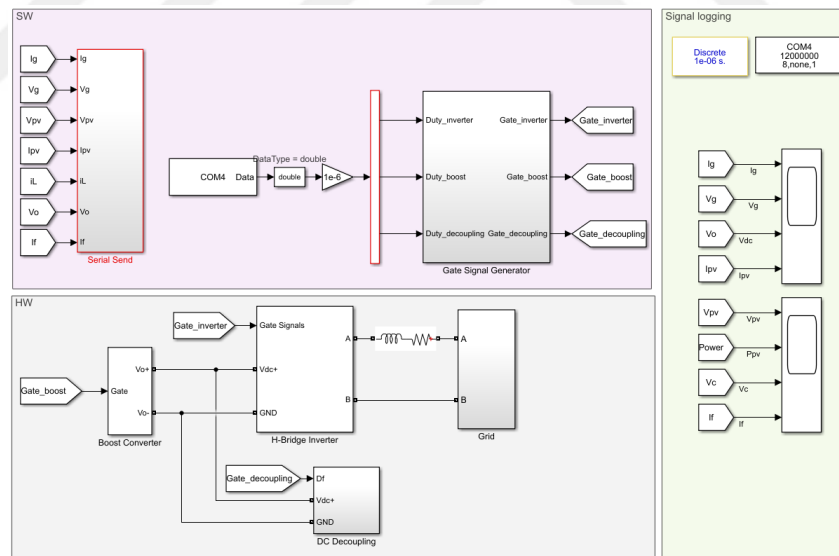


Figure 4.12 HIL model of boost type decoupling connected inverter

The sensed signals are sent via Serial Send block (APPENDIX 0.28) to the communication port with 10^6 gain. To generate the software, software model is constructed as seen in Figure 4.13.

The duty generator block (APPENDIX 0.15) is used to generate duty, same block

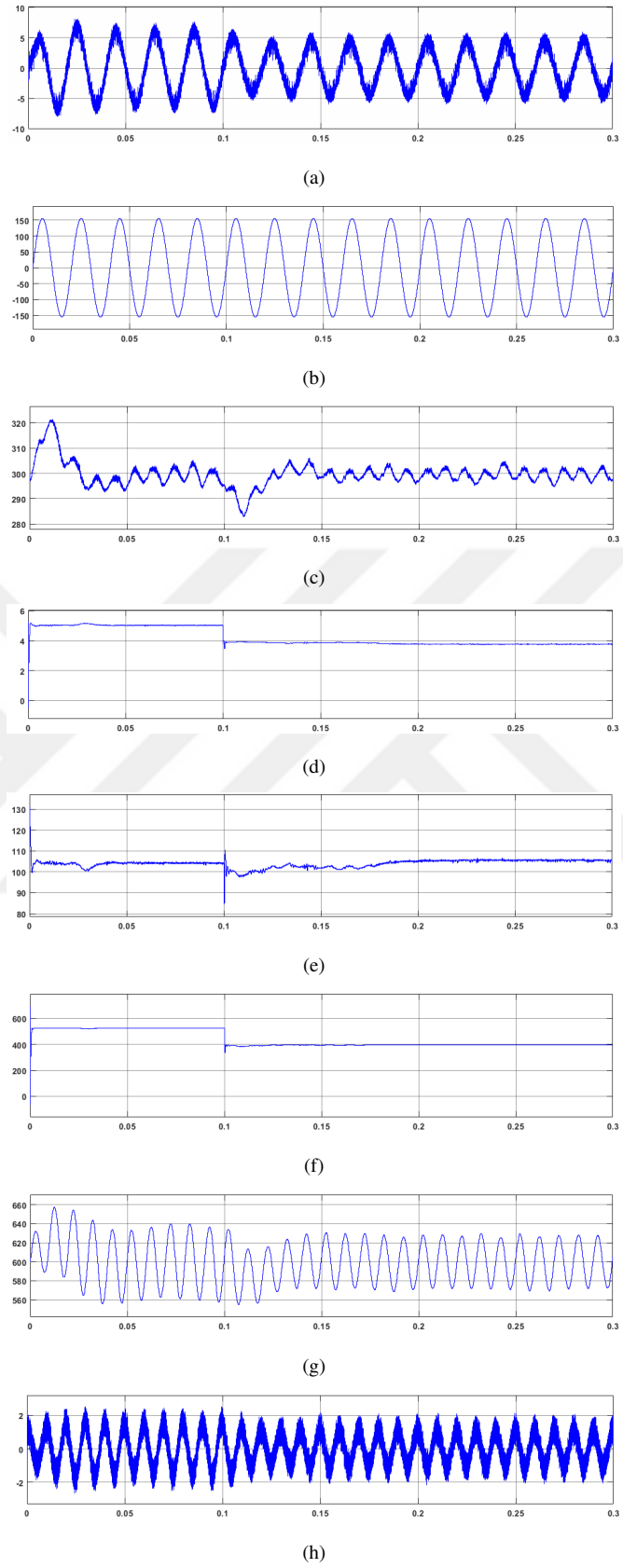


Figure 4.14 Transient analysis of HIL model of boost type APD connected Inverter, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_{cf} , (h) i_f

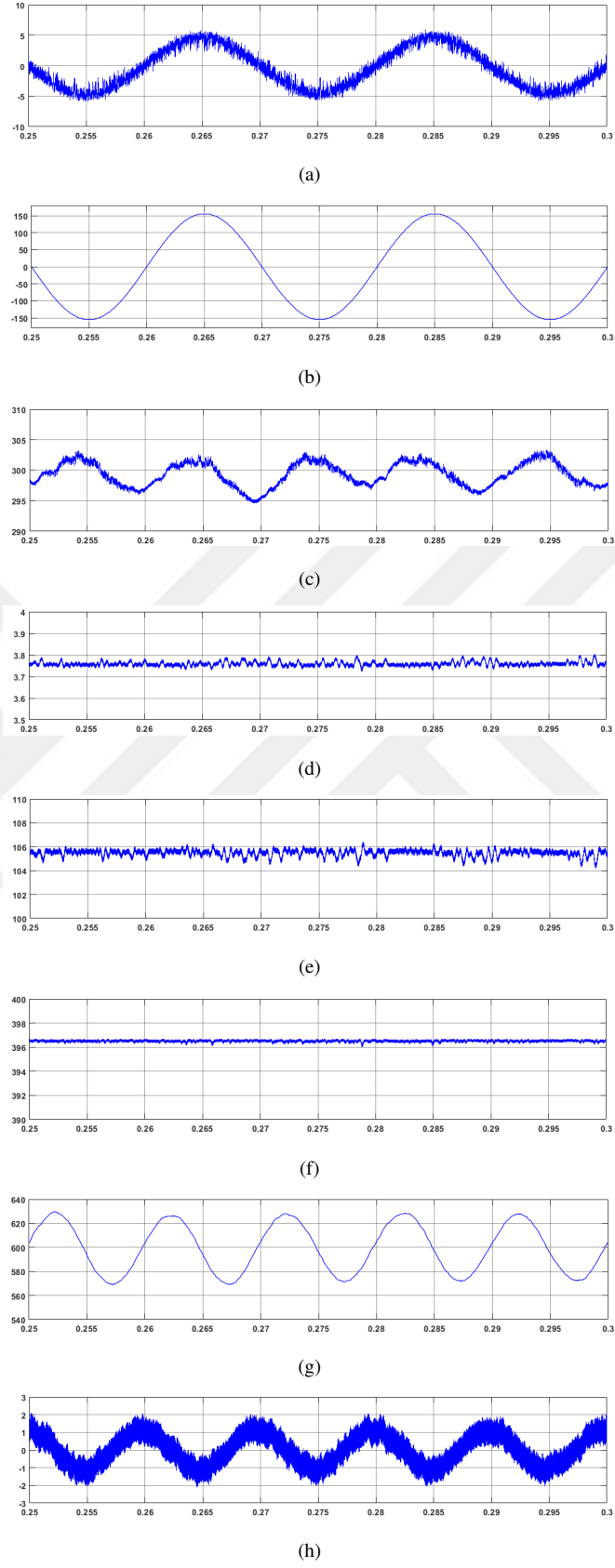


Figure 4.15 Steady state response of HIL model of boost type APD connected inverter, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_{cf} , (h) i_f

4.6 HIL Simulation of Buck-Boost Type Decoupling Circuit

After HIL simulation of the boost type decoupling circuit connected inverter worked correctly, HIL model of the buck-boost type DC decoupling circuit is inserted instead of boost type DC decoupling circuit. Only HIL model is updated to change decoupling circuit. MATLAB model in APPENDIX 0.19 is used. The software model is same as boost type decoupling circuit since the control algorithms are same.

The transient analysis and the steady state response can be observed in Figure 4.16 and Figure 4.17.

The transient response and the steady state response figures are almost identical as simulated ones (Figure 3.10, Figure 3.11).

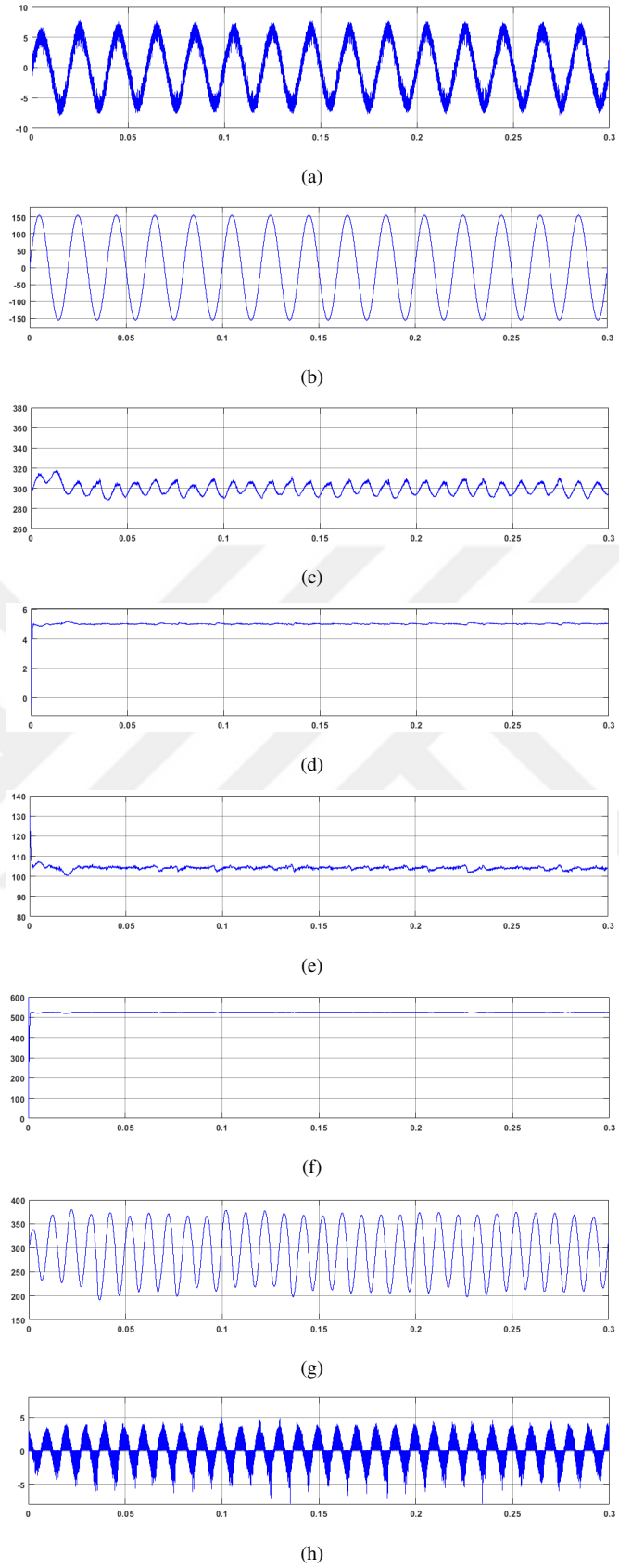


Figure 4.16 Transient analysis of HIL model of buck-boost type APD connected inverter, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_{cf} , (h) i_f

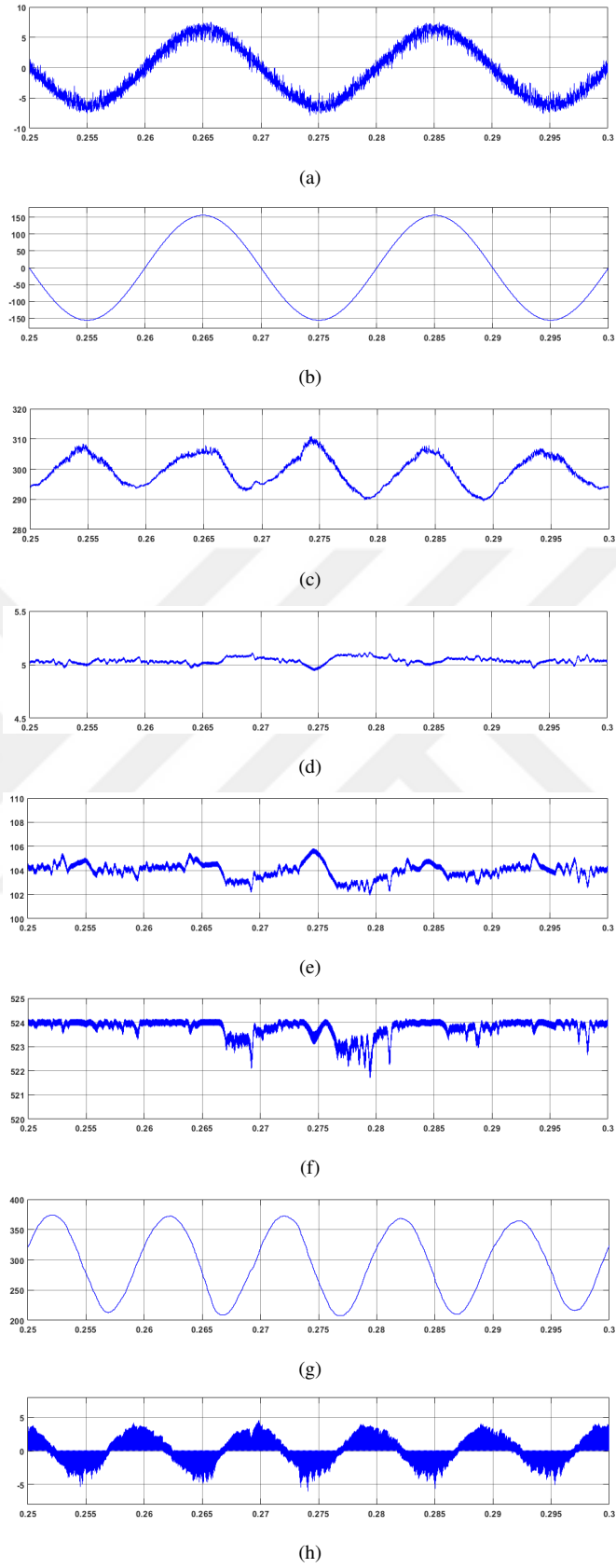


Figure 4.17 Steady state response of HIL model of buck-boost type APD connected inverter, (a) i_g , (b) v_g , (c) V_{DC} , (d) i_{pv} , (e) v_{pv} , (f) p_{pv} , (g) v_{cf} , (h) i_f

CHAPTER FIVE

CONCLUSION

In this thesis, first of all a boost converter is constructed to get feasible maximum PV power. MPPT algorithm is applied for this aim. The most common MPPT algorithm "Perturbation and Observation" is used.. Once the maximum power from PV system is achieved and the output voltage is a DC voltage, it can supply the grid. Then, inverter is constructed to supply grid. H bridge inverter is used for this purpose. It is used to convert DC voltage to AC voltage. By using an inductor the grid current is kept smooth. So the inductor is chosen according to the calculations due to the design considerations. OSG based power calculation is used to determine the grid reference current which uses Clarke transformation of grid voltage and current.

Large-sized electrolytic capacitor is used to keep the input voltage ripple at a minimized value which is the main problem of this design. The main disadvantages of the E-caps are their huge sizes and short life times. These disadvantages makes it difficult to construct an inverter with an compact design and long lifetime. With this reason, active power decoupling circuits can be used. There are several types of decoupling circuits. In this thesis, boost type and buck-boost type DC active power decoupling circuit are used. The electrolytic capacitor is replaced with these circuits. And they allows inverter a compact design and also long life time since they have film capacitors. The main duty of these circuits is decouple the reactive power of the inverter.

There are several differences between boost and buck-boost type DC active decoupling circuits. The voltage of filter capacitor placed in boost type APD circuit is always higher then the input voltage. But for the buck-boost type decoupling it changes according to the grid current. It can be lower or higher then the input voltage. The filter current of the boost type decoupling circuit is a sinusoidal wave with double line frequency because the filter current is also the filter inductor current. But it is different in buck-boost type decoupling circuit, because inductor is not in the input of filter. So, the filter current is not smooth. But the simulation results shows that these

differences does not effects the inverter quantities. So, both of them can be used.

Finally, to test the design HIL setup is constructed. HIL simulation is used to test the controller. The software of the control algorithm runs in the controller. The mathematical model of the hardware runs in the computer. And they communicate each other. The main purpose of the HIL is avoid hardware damages because of the software failure. In this thesis, also HIL simulations are tested for the boost converter, inverter and the decoupling circuits. And the results shows that the algorithm works correctly and it does not brake the hardware.

In conclusion, to design a compact inverter with long life time, active power decoupling circuit should be used instead of bulk size electrolytic capacitor. Inverter design considerations are not affected by this change and maintenance of the inverter is much more easier. And the software algorithm is approved by HIL tests that it is not harm the hardware.

CHAPTER SIX

FUTURE WORKS

In this thesis, only double line frequency ripple power is eliminated by APD circuit. The algorithm can be improved and the system can eliminate the other harmonics of the system. The reference current formula must be updated for this aim. For example 5th harmonic of the grid voltage can be eliminated with APD circuit without another filter circuit.

In this thesis, APD method is applied to single phase inverter but it can be also applied to the multi-level converters. It may also solve another problems of a multi-level converters.

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APPENDICES

Appendix 1: MPPT Algorithm

```
1 function Vref = PandO(Vpv, Ipv)
2 persistent Vrefprev, Pprev, Vprev
3 % Initialization
4 if isempty(Vrefprev)
5     Vrefprev = 0;
6     Vprev = 0;
7     Pprev = 0;
8 end
9
10 % Calculate power
11 Ppv = Vpv * Ipv;
12
13 % Calculate delta values
14 dV = Vpv - Vprev;
15 dP = Ppv - Pprev;
16 dVref = Vpv - Vrefprev;
17
18 % Check voltage diff and determine delta value to change ref voltage
19 if (dVref < 0.1)
20     deltaV = 0.0005;
21 elseif (dVref < 0.20)
22     deltaV = 0.01;
23 else
24     deltaV = 0.1;
25 end
26
27 % Check delta power and delta voltage and change ref voltage accordingly
28 if (dP) == 0
29     Vref = Vrefprev;
30 else
31     if (dP) > 0
32         if (dV) > 0
33             Vref = Vrefprev + deltaV;
34         else
35             Vref = Vrefprev - deltaV;
36         end
37     else
38         if (dV) > 0
39             Vref = Vrefprev - deltaV;
40         else
41             Vref = Vrefprev + deltaV;
42         end
43     end
44 end
45
46 % Limit the reference voltage to zero
47 if Vref < 0
48     Vref = 0;
49 end
50
51 % Save the last values
52 Vprev = Vpv;
53 Pprev = Ppv;
54 Vrefprev = Vref;
55 end
```

Figure 0.1 MATLAB Code of MPPT

Appendix 2: Boost Converter Simulink Model

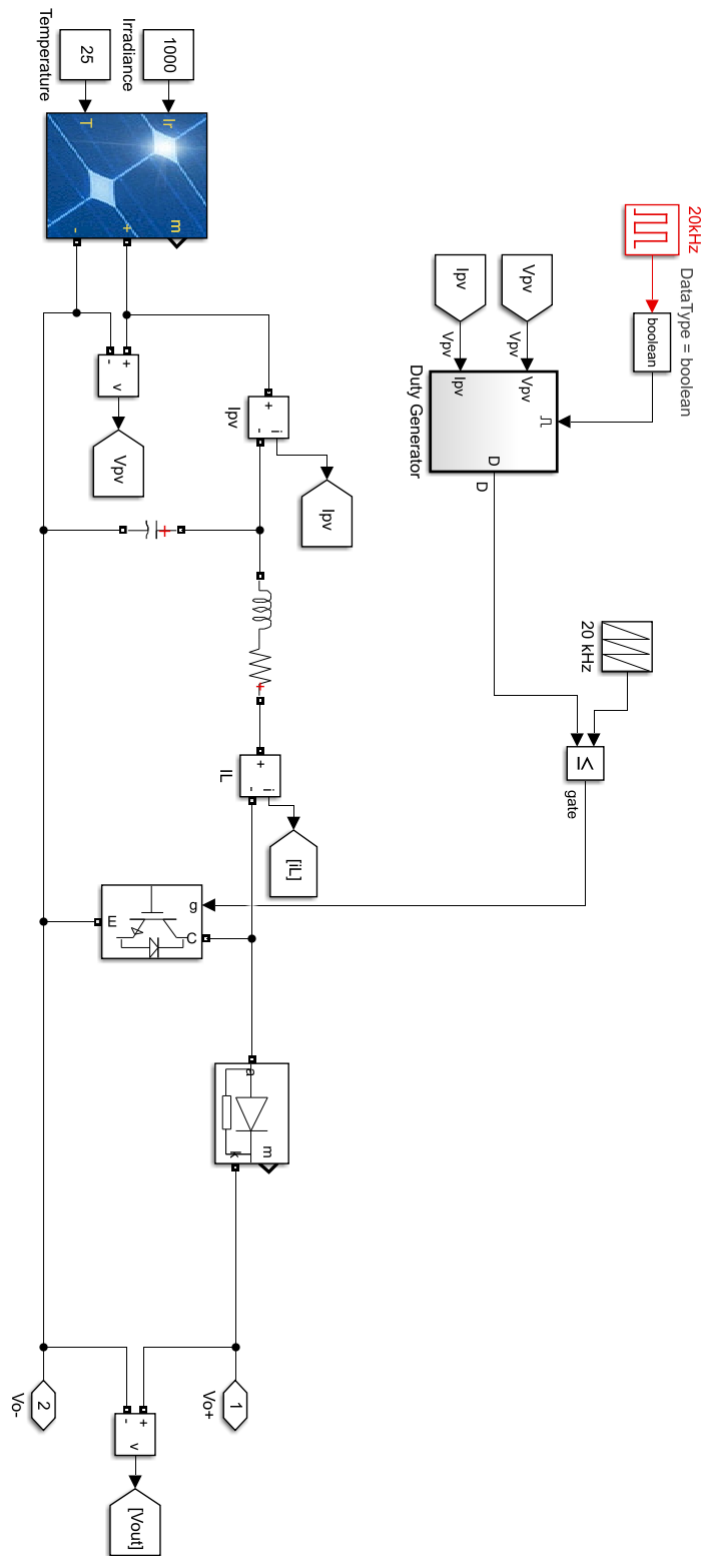


Figure 0.2 SIMULINK Model of Boost Converter

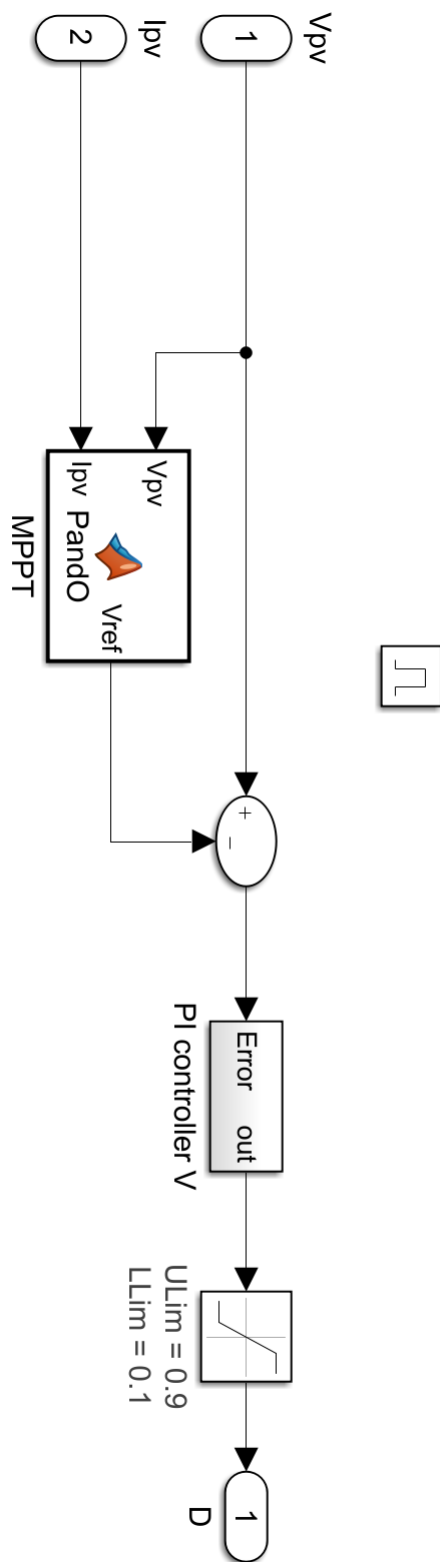


Figure 0.3 SIMULINK Model of Boost Converter Controller

Block Parameters: PV Array

PV array (mask) (link)

Implements a PV array built of strings of PV modules connected in parallel. Each string consists of modules connected in series. Allows modeling of a variety of preset PV modules available from NREL System Advisor Model (Jan. 2014) as well as user-defined PV module.

Input 1 = Sun irradiance, in W/m², and input 2 = Cell temperature, in deg.C.

Parameters

Advanced

Array data

Parallel strings

1

Series-connected modules per string

6

Module data

Module: User-defined

Maximum Power (W)

87.348

Cells per module (Ncell)

30

Open circuit voltage Voc (V)

21.7

Short-circuit current Isc (A)

5.34

Voltage at maximum power point Vmp (V)

17.4

Current at maximum power point Imp (A)

5.02

Temperature coefficient of Voc (%/deg.C)

-0.36099

Temperature coefficient of Isc (%/deg.C)

0.102

Model parameters

array @ 25 deg.C & specified irradiances

Irradiances (W/m²)

[1000 500 100]

Plot

Light-generated current IL (A)

5.3556

Diode saturation current IO (A)

1.9953e-10

Diode ideality factor

1.173

Shunt resistance Rsh (ohms)

377.4061

Series resistance Rs (ohms)

0.33083

Display I-V and P-V characteristics of ...

OK

Cancel

Help

Apply

Figure 0.4 SIMULINK Model of PV array

Appendix 3: Inverter Simulink Model

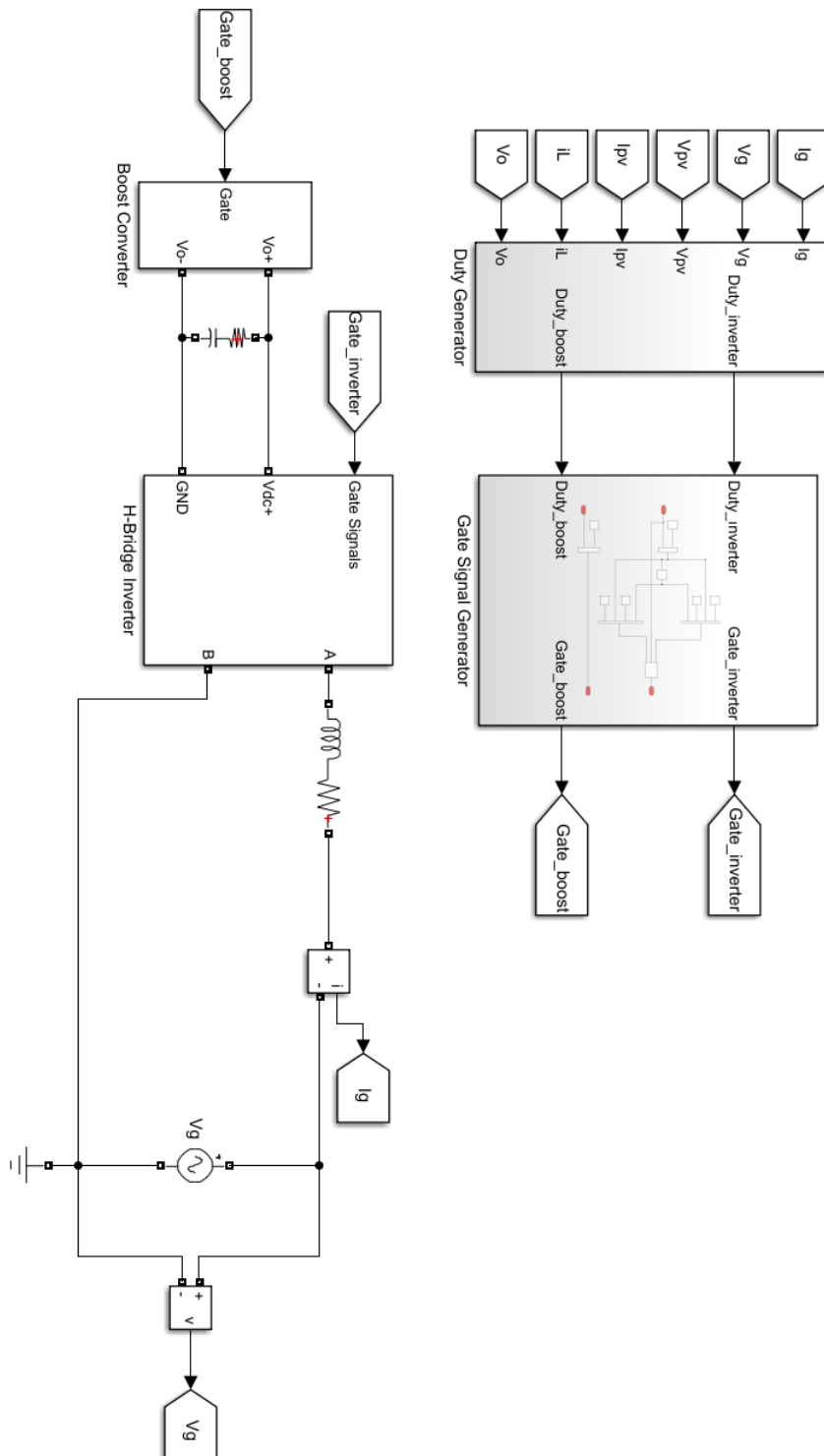


Figure 0.5 SIMULINK Model of Inverter

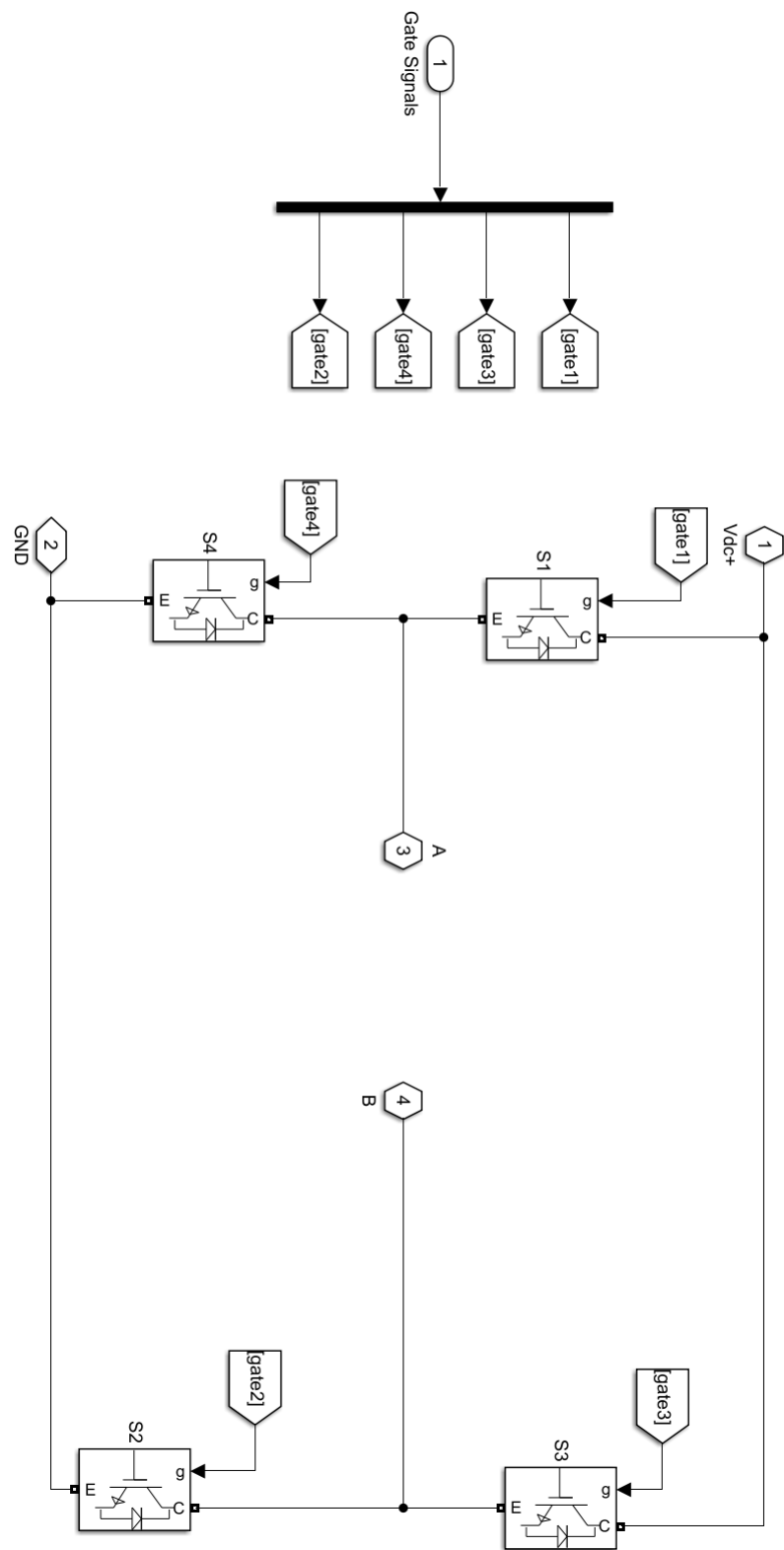


Figure 0.6 H Bridge Inverter in Figure 0.5

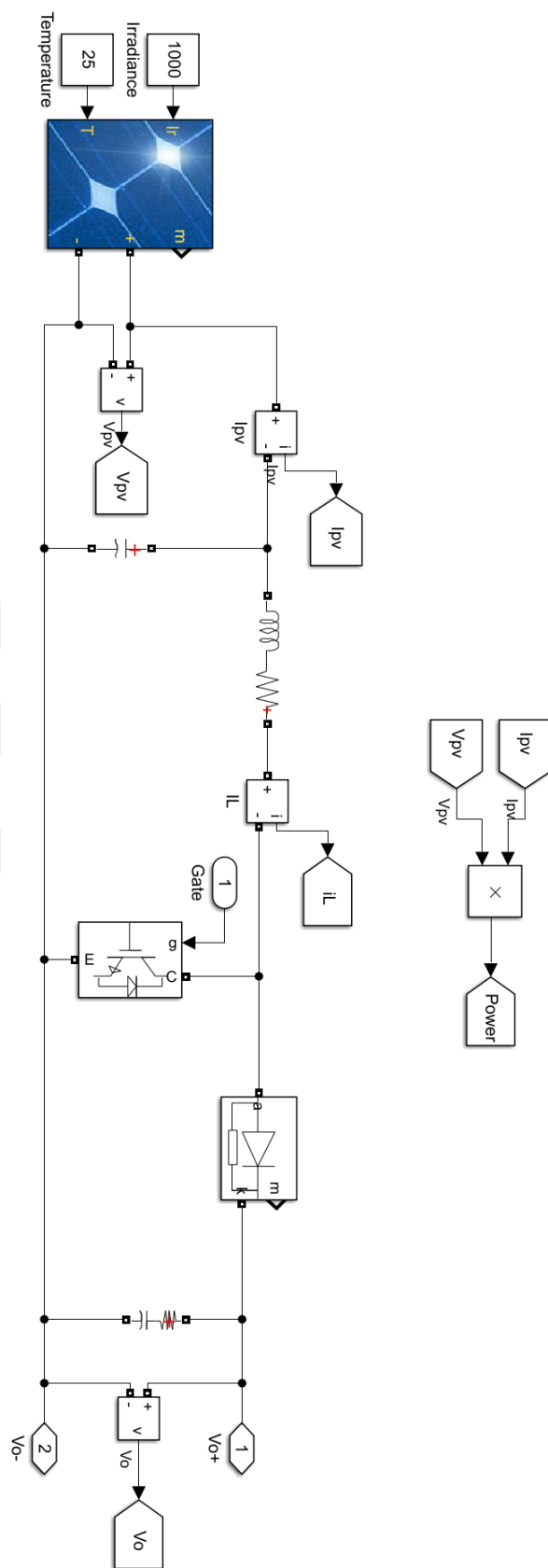


Figure 0.7 Boost Converter in Figure 0.5

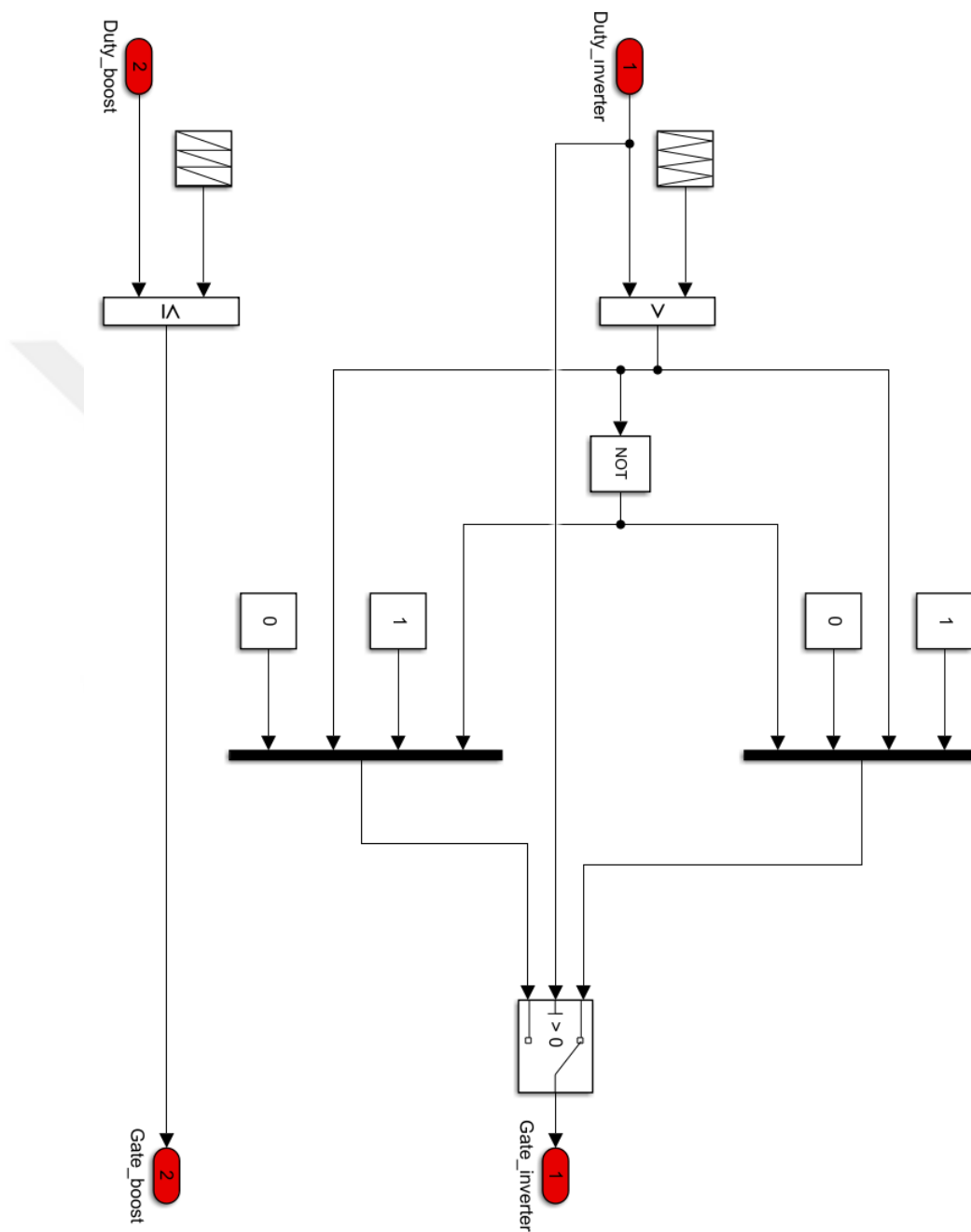


Figure 0.8 Gate Signal Generator in Figure 0.5

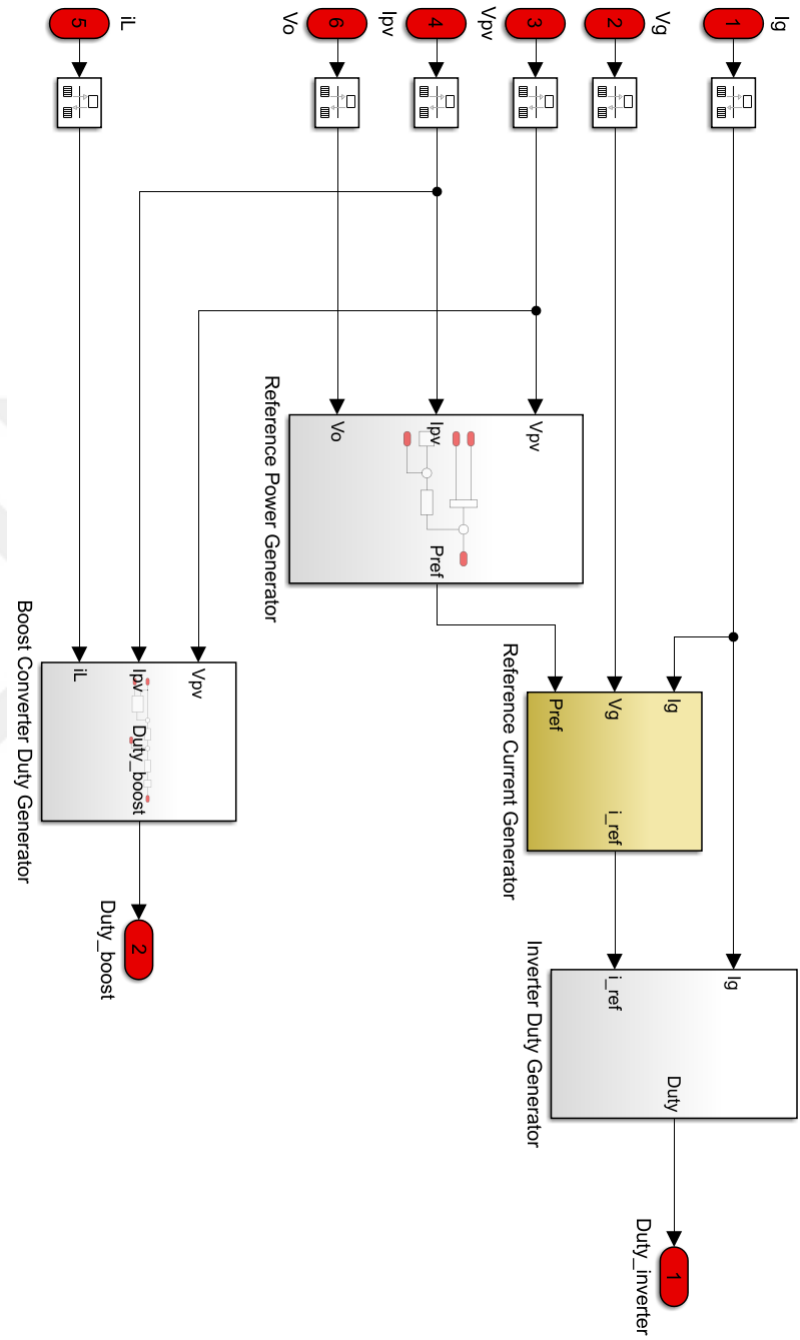


Figure 0.9 Duty Generator in Figure 0.5

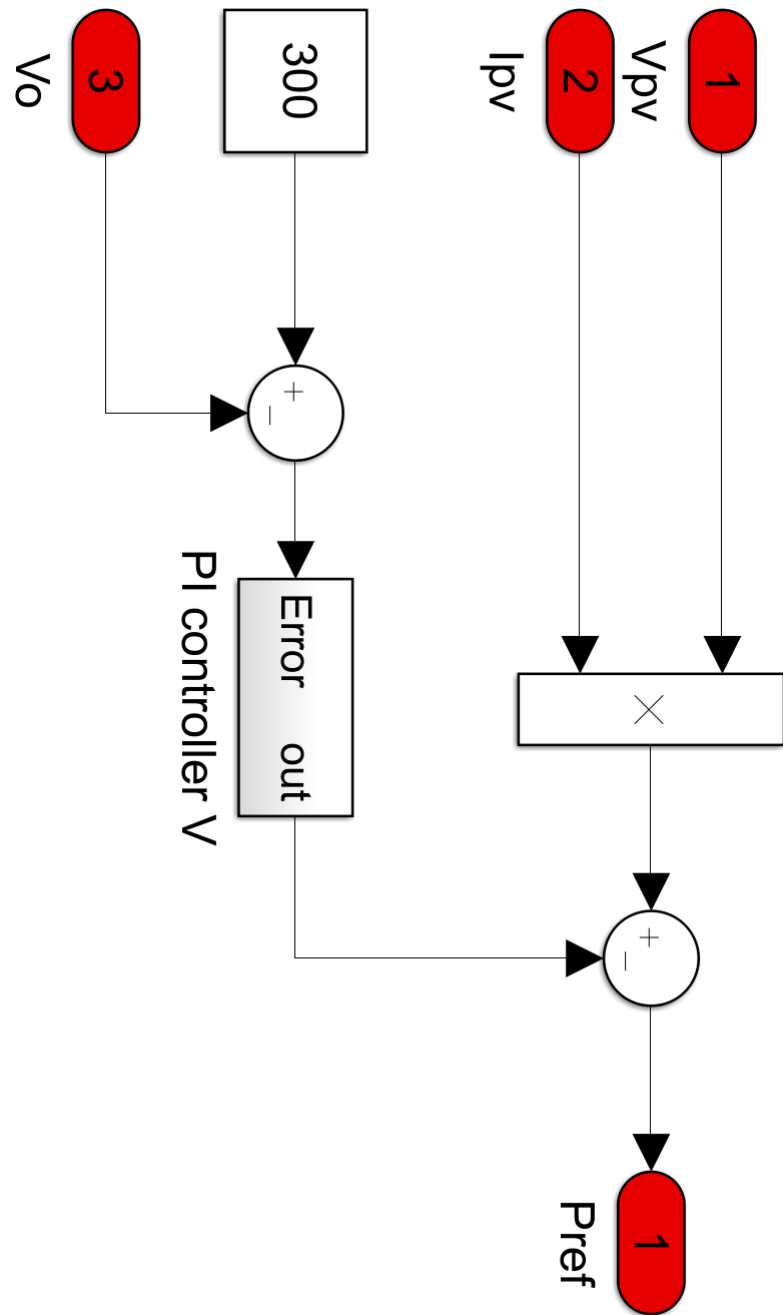


Figure 0.10 Reference Power Generator in Figure 0.9

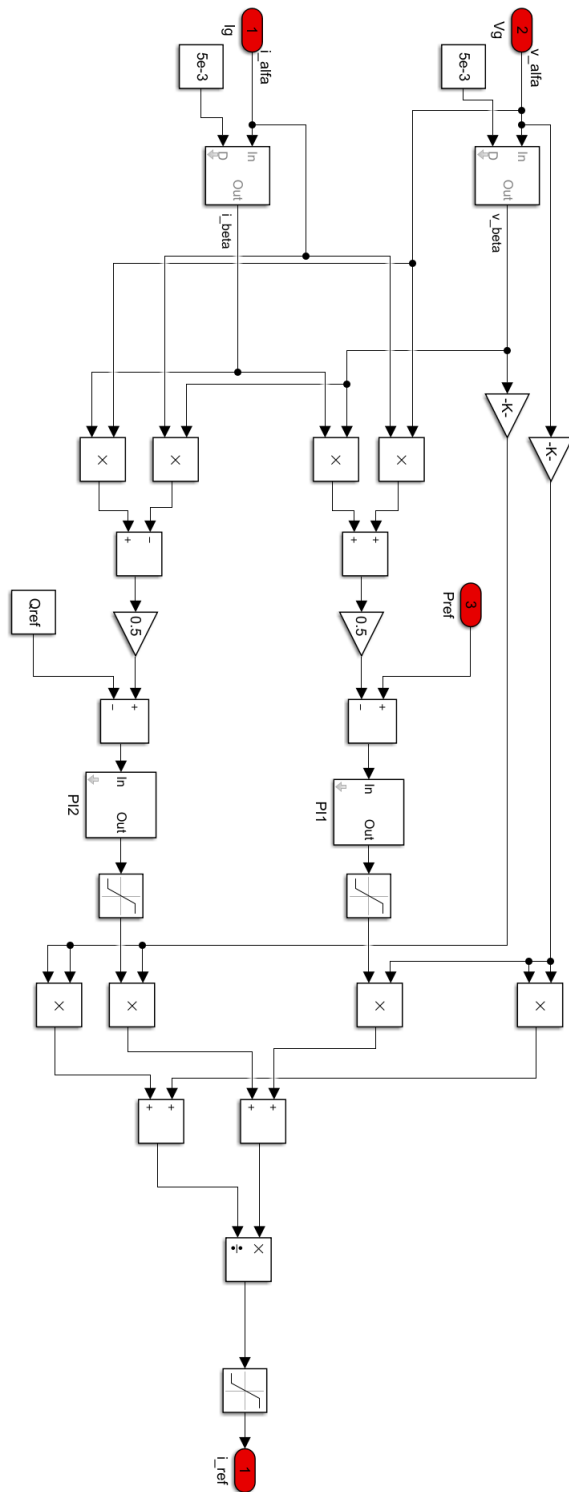


Figure 0.11 Reference Current Generator in Figure 0.9

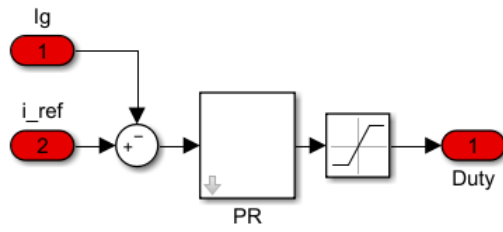


Figure 0.12 Inverter Duty Generator in Figure 0.9

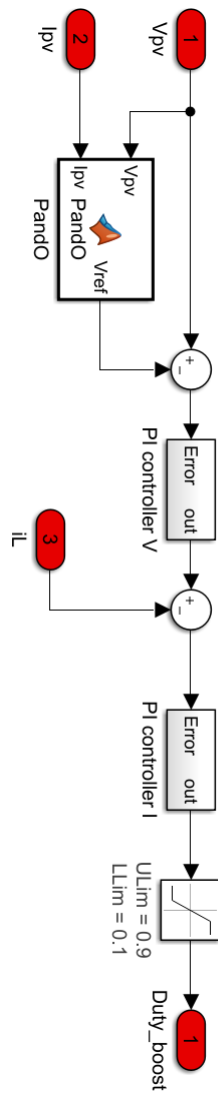


Figure 0.13 Boost Converter Duty Generator in Figure 0.9

Appendix 4: APD Simulink Model

```

1 format long
2
3 %Define parameters
4 BW = 2*0.33*2*pi*50;
5 wn = 2*pi*50;
6 Ts = 1e-6;
7
8 %Define continuous time signal
9 sysc = tf([BW 0],[1 BW (2*wn)^2]);
10
11
12 %Calculate discrete time signal
13 sysd = c2d(sysc, Ts);

```

Figure 0.14 Band-pass filter discrete form calculation

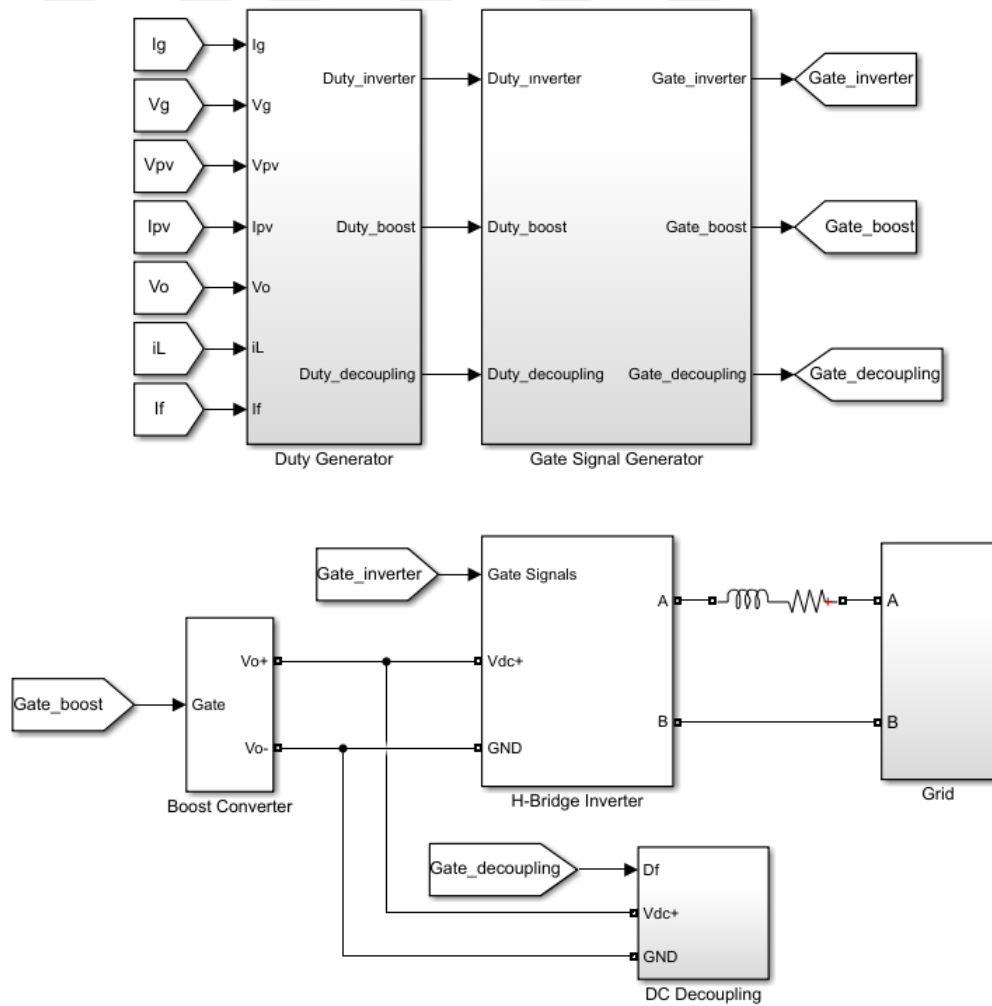


Figure 0.15 SIMULINK Model of the Inverter with DC Decoupling Circuit

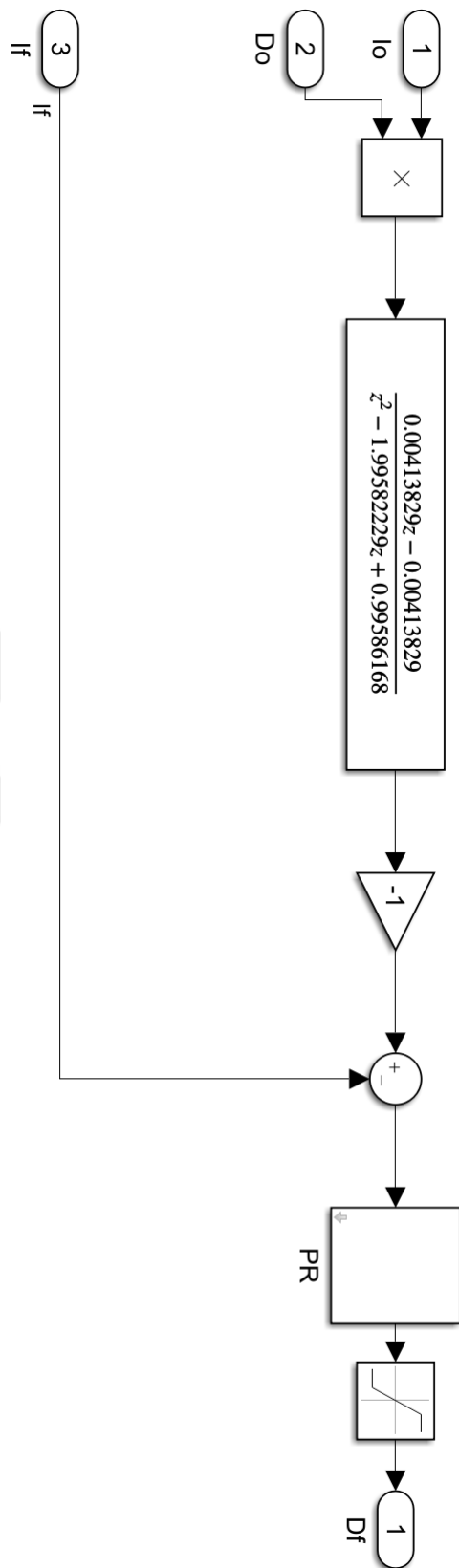


Figure 0.17 DC Decoupling Duty Generator in Figure 0.15

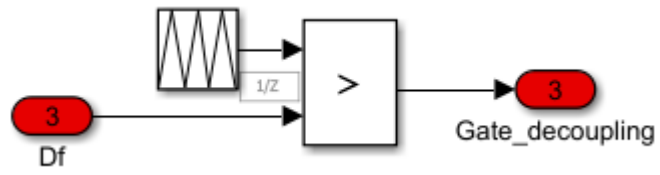


Figure 0.18 DC Decoupling Gate Signal Generator in Figure 0.15

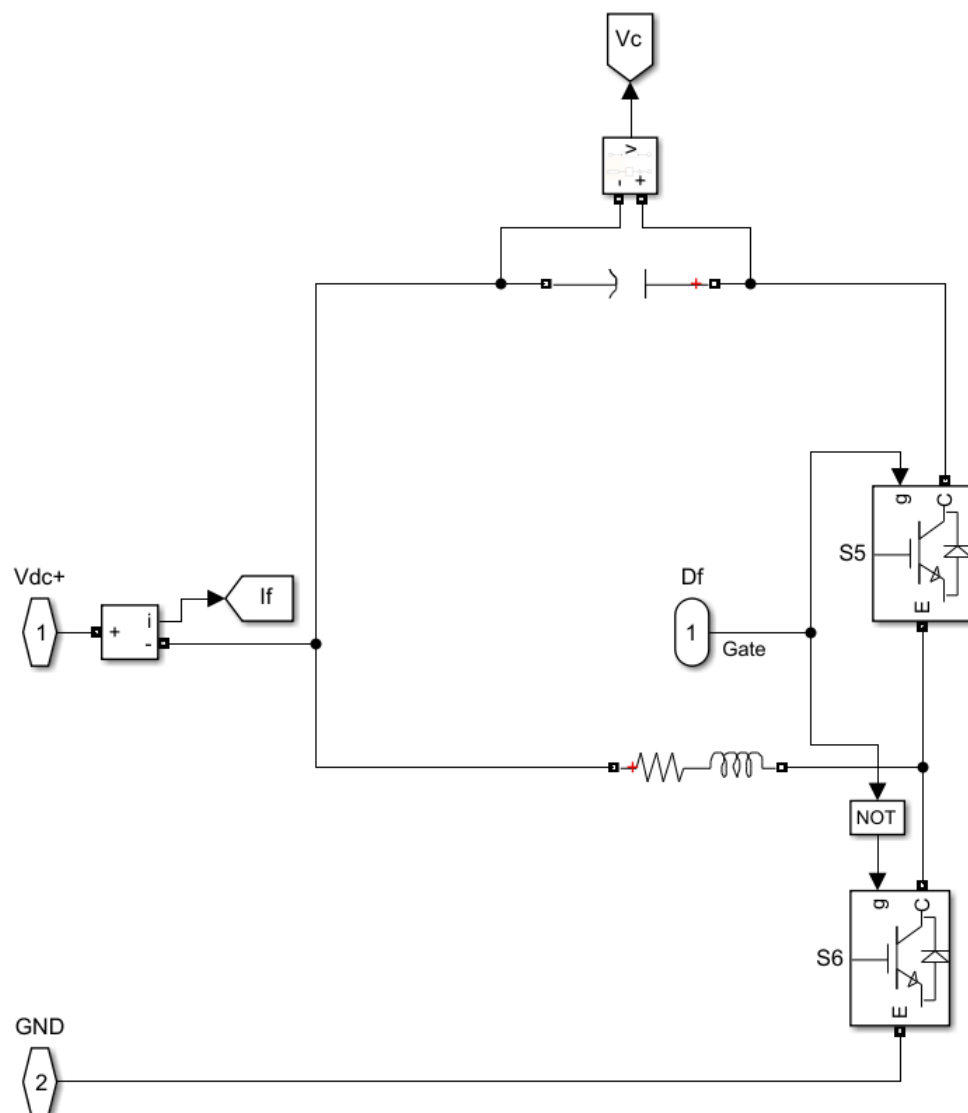


Figure 0.19 Buck Boost Type DC Decoupling Circuit

Appendix 5: HIL Setup

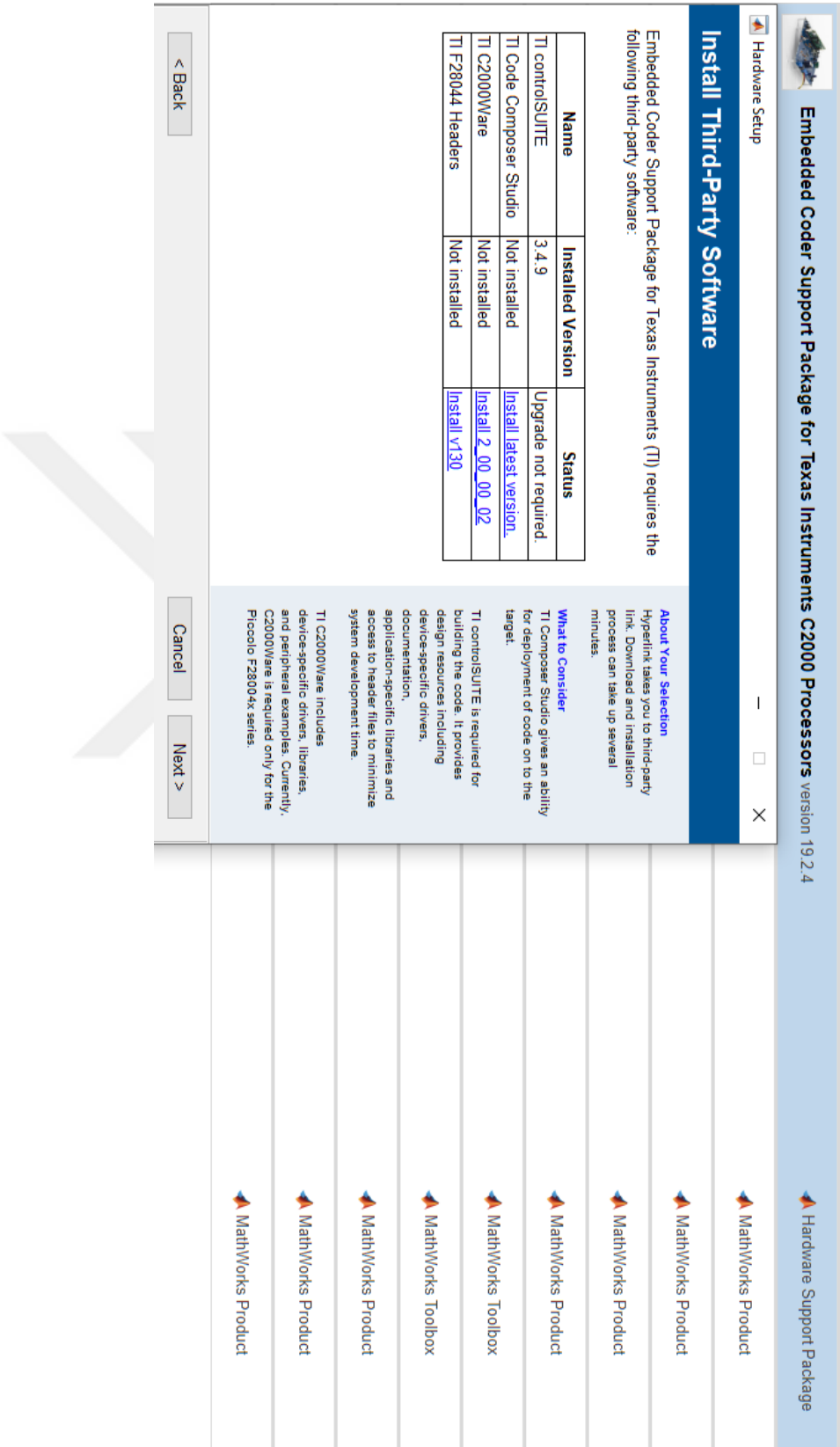


Figure 0.20 Necessary SW Packages for HIL

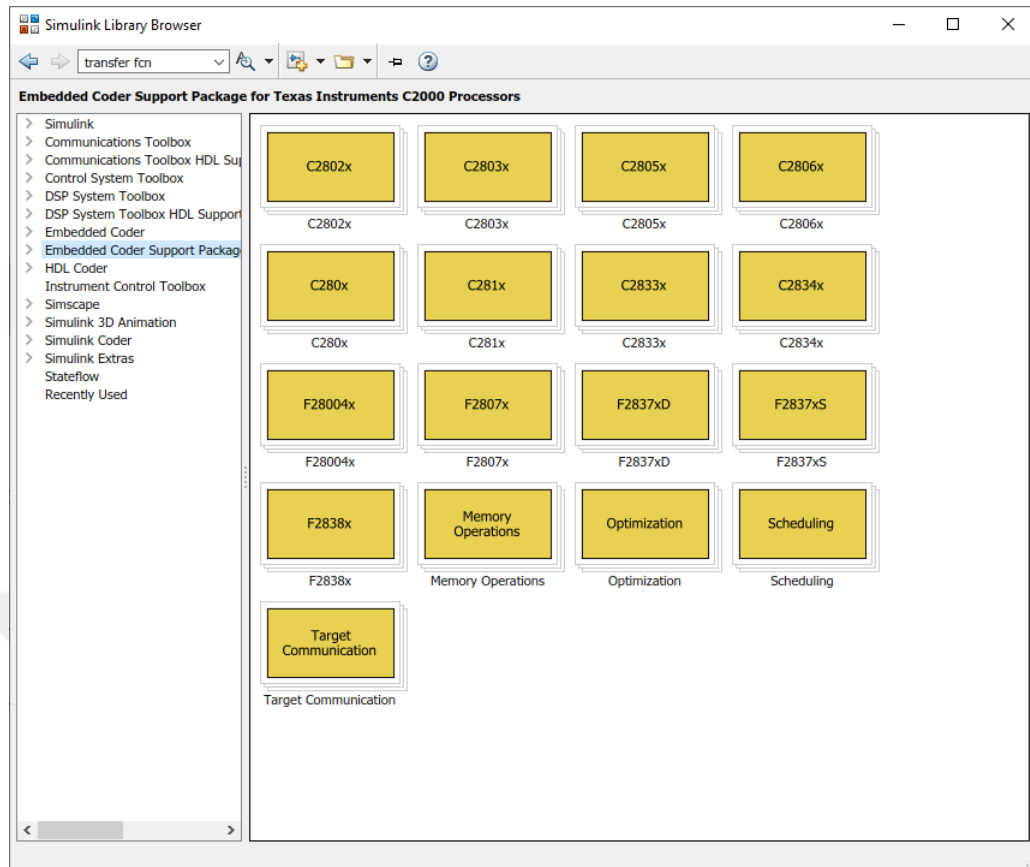


Figure 0.21 Embedded Coder Library

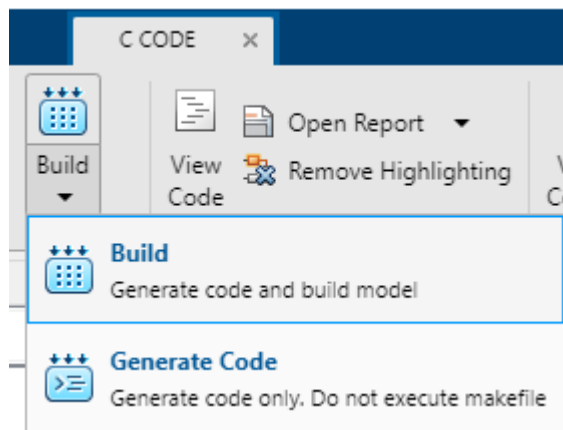
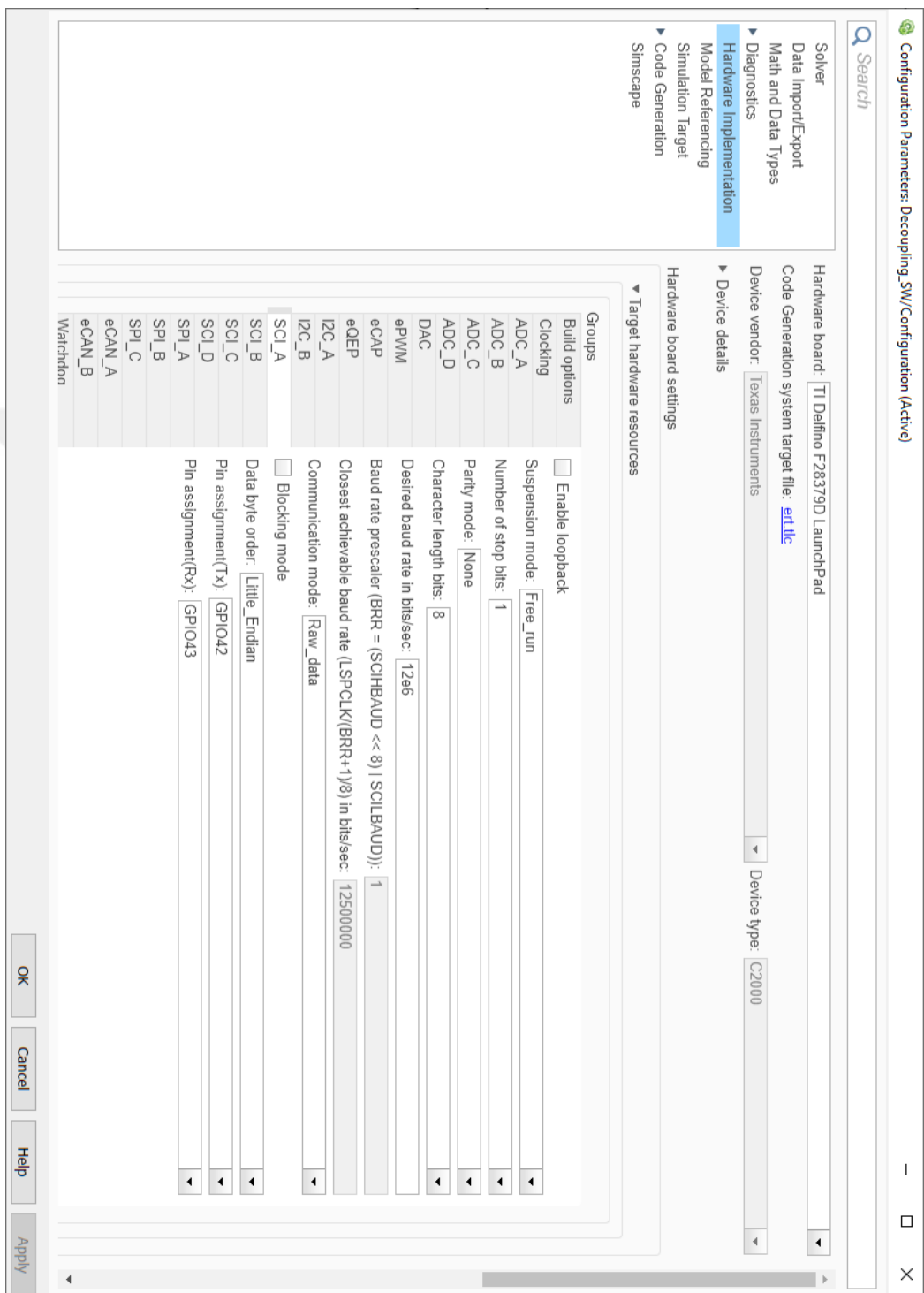


Figure 0.22 Code Generation



PIE and CPU Interrupt Numbers for F280x, F2802x, F2803x, F2805x, F2806x, F2803x, F28M35x, and F28M36x Processors

PIE → CPU ↓	1	2	3	4	5	6	7	8
1	SEQ1INT (ADC) / ADCINT1	SEQ2INT (ADC) / ADCINT2	Reserved	XINT1	XINT2	ADCINT / ADCINT9	TINT0 (TIMER 0)	WAKEINT (LPMWD)
2	EPWM1_TZINT	EPWM2_TZINT	EPWM3_TZINT	EPWM4_TZINT	EPWM5_TZINT	EPWM6_TZINT	EPWM7_TZINT	EPWM8_TZINT
3	EPWM1_INT	EPWM2_INT	EPWM3_INT	EPWM4_INT	EPWM5_INT	EPWM6_INT	EPWM7_INT	EPWM8_INT
4	ECAP1_INT	ECAP2_INT	ECAP3_INT	ECAP4_INT	ECAP5_INT	ECAP6_INT	EPWM10_TZINT / HRCAP1_INT	EPWM9_TZINT / HRCAP2_INT
5	EQEP1_INT	EQEP2_INT	EQEP3_INT	HRCAP3_INT	HRCAP4_INT	Reserved	EPWM10_INT	EPWM9_INT
6	SPIRXINTA (SPI-A)	SPTXINTA (SPI-A)	SPIRXINTB (SPIB_RX) / MRINTB (MCBSP-B)	SPTXINTB (SPIB_TX) / MXINTB (MCBSP-B)	SPIRXINTC (SPIC) / MRINTA (MCBSP-A_RX)	SPTXINTC (SPIC) / MXINTA (MCBSP-A_TX)	SPIRXINTD (SPID) / EPWM12_TZINT	SPTXINTD (SPID) / EPWM11_TZINT
7	DINTCH1 (DMA1)	DINTCH2 (DMA2)	DINTCH3 (DMA3)	DINTCH4 (DMA4)	DINTCH5 (DMA5)	DINTCH6 (DMA6)	EPWM12_INT	EPWM11_INT
8	I2CINT1A	I2CINT2A	Reserved	Reserved	SCIRXINTC (SCH-C)	SCITXINTC (SCH-C)	Reserved	Reserved
9	SCIRXINTA (SCIA_RX)	SCITXINTA (SCIA_TX)	SCIRXINTB (SCIB_RX) / LINA_INT0	SCITXINTB (SCIB_TX) / LINA_INT1	ECANDINTA (CANA_1)	ECANDINTA (CANA_2)	ECANDINTB (CANB_1)	ECANDINTB (CANB_2)
10	EPWM9_TZINT / ADCINT1	EPWM10_TZINT / ADCINT2	EPWM11_TZINT / ADCINT3	EPWM12_TZINT / ADCINT4	EPWM13_TZINT / ADCINT5	EPWM14_TZINT / ADCINT6	EPWM15_TZINT / ADCINT7	EPWM16_TZINT / ADCINT8
11	CLA1_INT1 / EPWM8_INT7 / MTOCPCINT1	CLA1_INT2 / EPWM10_INT / MTOCPCINT2	CLA1_INT3 / EPWM11_INT / MTOCPCINT3	CLA1_INT4 / EPWM12_INT / MTOCPCINT4	CLA1_INT6 / EPWM13_INT	CLA1_INT6 / EPWM14_INT	CLA1_INT7 / EPWM15_INT	CLA1_INT8 / EPWM16_INT
12	XINT3	XINT4 / C28FLSINGERR	XINT5	XINT6 / C28RAMSINGERR	XINT7 / C28RAMACCVIOL	Reserved	LVF	LUF

Figure 0.24 SCI Module A PIE and CPU numbers

Appendix 6: HIL Blocks

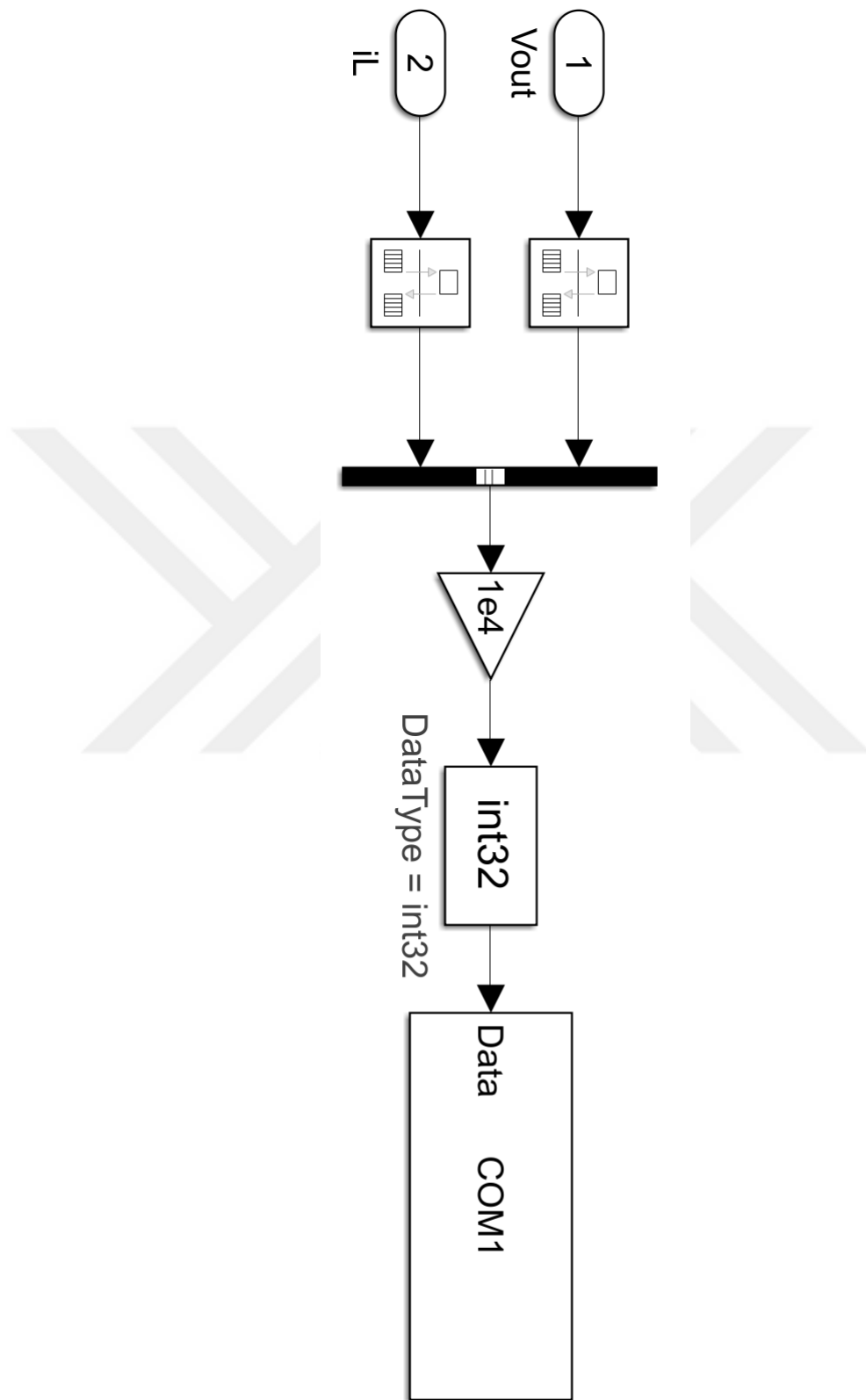


Figure 0.25 Serial Send block in Figure 4.4

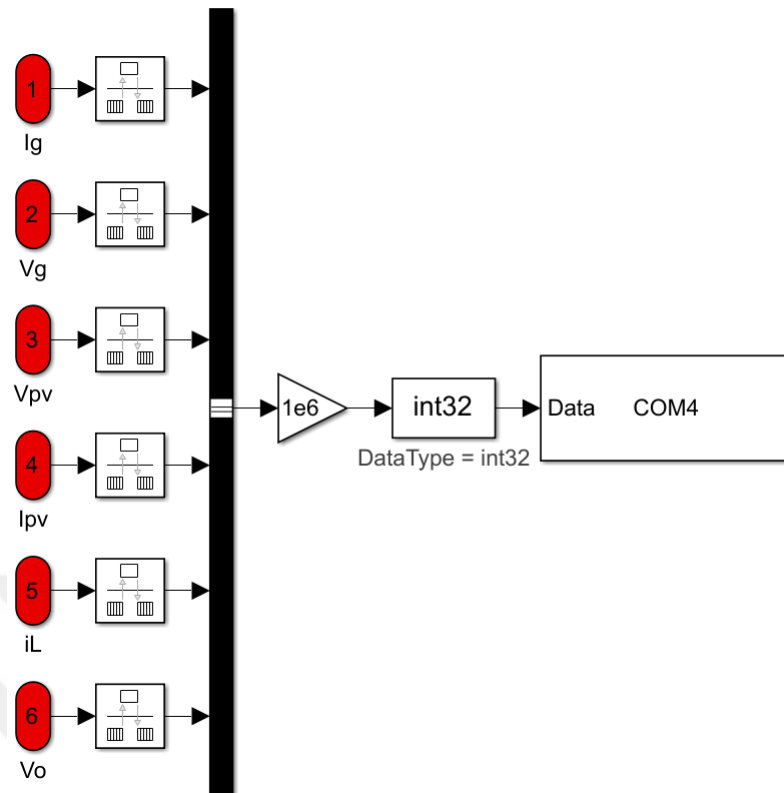


Figure 0.27 Serial Send block in Figure 4.8

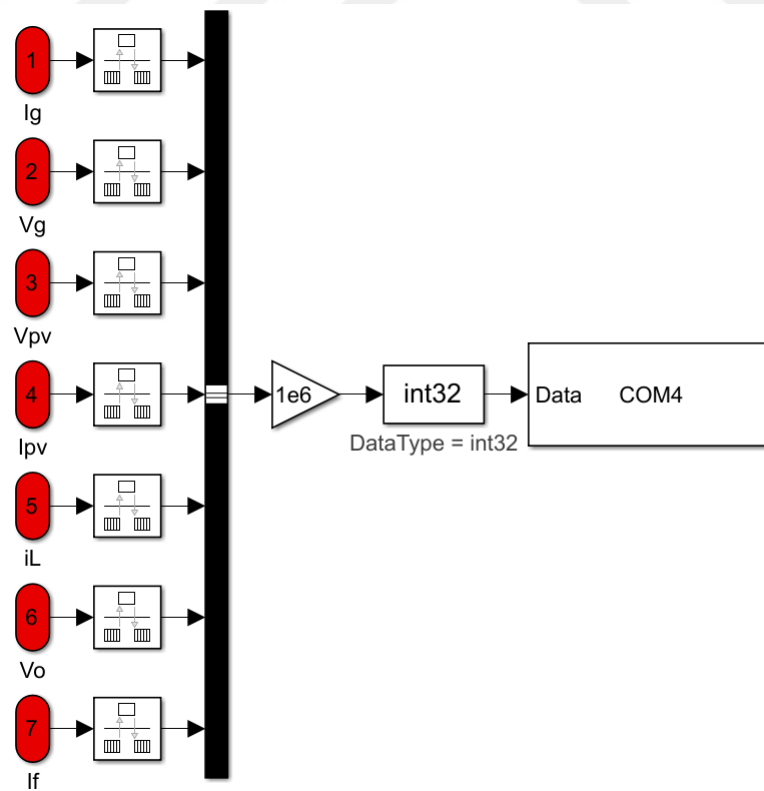


Figure 0.28 Serial Send block in Figure 4.12