T.C.

AKSARAY UNIVERSITY

GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCE

DEPARTMENT OF ELECTRICAL-ELECTRONIC AND COMPUTER ENGINEERING

IMPEDANCE MATCHING AND IT'S QUALITY FACTOR INVESTIGATION FOR RF ENERGY HARVESTING

MASTER OF SCIENCE THESIS

Musaab Mohammed JASIM

SUPERVISOR

Asst. Prof. Dr. FİLİZ SARI

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Aksaray University, Institute Of Science and Technology Approval **Musaab Mohammed JASIM**, M.Sc. with thesis student No. 162335811, successfully presented the M.Sc. thesis titled "**IMPADENCE MATCHING AND ITS QUALITY FACTOR INVESTIGATION FOR RF ENERGY HARVESTING**", prepared after satisfying all the requirements identified in the concerned bylaws, before the jury whose signatures are affixed below.

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Date of Defence: 28/03/2019

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Assoc. Prof. Dr. M.Ali HINIS

DECLARATION

The idea for this present study was taken from the literature regarding the topics. It was announced here that the whole work presented in this project has been composed and originated by myself unless otherwise specified. The study was conducted completely under the supervision of Asst. Prof. Dr. Filiz SARI.

Signature

Musaab Mohammed JASIM

ACKNOWLEDGMENT

First of all, I would like to express my gratitude to my thesis advisor Asst. Prof. Dr. Filiz SARI of the School of Natural and Applied Sciences, Electrical-Electronic and Computer Engineering at Aksaray University. Dr. Filiz SARI was always supportive and helpful without prompting, offering essential information to make my thesis unique and novel. She is an inspiring professor who not only pointed me in the direction of the topic of this thesis, she also shared valuable ideas with me at various stages of the research without sparing useful remarks and suggestions, helping me tremendously in the process. I also would like to thank her for being my inspiration not to give up, and her words of encouragement helped me accomplish what I have done so far. I have never met another professor who loves teaching as much as she does.

Furthermore, thanks to my friends at Aksaray University. Dear friends, you have always believed, helped and encouraged me during my study period.

Finally, I must express my profound gratitude to my parents (Mohammed Al-Azawy and Sahar Al-Azawy) and my brother (Usama Al-Azawy) and my sister (Samar Al-Azawy) for providing me with unfailing support and continuous encouragement throughout the years of my study.

Thank you all, without you, I would not be able to achieve this accomplishment.

Musaab Mohammed Jasim Al-Azawy

AKSARAY, 2019

TABLE OF CONTENTS

YÜKSEK LİSANS TEZİ

RF ENERJİ HASADI İÇİN EMPEDANS EŞLEŞTİRME VE KALİTE FAKTÖRÜNÜN ARAŞTIRMASI

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Danışman: Asst.Prof. Dr. Filiz SARI

ÖZET

Enerji hasadı teknolojisi, elektronik cihazların yaygın kullanımı nedeniyle, özellikle de kablosuz olanların, araştırmacıların çok ilgisini çekmiştir. Kolay ve ücretsiz enerji kaynakları sağlamak için dünyadaki en önemli araştırma konularından biri haline gelmiştir.

Bu tez, -35dBm ile 25 dBm arasındaki giriş gücü için RF enerji hasat parametresinin hasat sistemi verimliliği ve çıkış DC voltajı üzerindeki etkisini sunmaktadır. Bu çalışmada, ikiden altı kademeye kadar olan çok kademeli Dickson Voltaj Çoklayıcı (DVM) tasarlanmıştır ve farklı yük direncine (20, 50, 100, 500 ve 1000 kΩ) ve L, T ve Pi gibi farklı eşleştirme topolojileri için uygulanmıştır. İki Schottky diyot modelli (örn. HSMS-2852 ve HSMS-2822) DVM tasarımında verimlilik ve çıkış DC gerilimi etkisini görmek ayrıca farklı empedans eşleştirme topolojilerinin kalite faktörünü göstermek için kullanılmıştır. Tüm simülasyonlar Advance Design System (ADS) 2017 kullanılarak yapıldı. Tasarımda seçilen hedef frekans, Endüstriyel, Bilimsel ve Medikal Radyo Bandı (ISM bandı) için olan 915 MHz'dir. Simülasyon sonuçları düşük giriş güç seviyelerinde eşleştirilmiş DVM devresinin eşleştirilme yapılmamış DVM devresine göre verimliliğinde gelişme göstermektedir. Ayrıca, simülasyon sonuçları düşük yük kullanımının hasat devresinin verimini arttırdığını göstermektedir. Ayrıca, HSMS-2852 Schottky diyot modeli kullanmak, verimlilik açısından HSMS-2822'den daha iyidir. Düşük giriş gücü için eşleştirme devreli hasat sistemi, tüm tasarım için eşleştirme devresi olmayan hasat sistemine göre, verimlilik seviyesine bağlı olarak bir avantaj sağlar.

Anahtar Kelimeler: Radyo frekansı (RF) enerji hasadı, Dickson-Voltage-Multiplier (DVM), ISM bandı 915 MHz, Empedans eşleştirme topolojisi, Schottky diyot, düşük güç uygulaması.

Mart, 2019; 74 sayfa

M.Sc. THESIS

IMPEDANCE MATCHING AND IT IS QUALITY FACTOR INVESTIGATION FOR RF ENERGY HARVESTING

Musaab Mohammed JASIM

Aksaray University
Graduate School of Natural and Applied Science
Department of Electrical-Electronic and Computer Engineering

Supervisor: Asst. Prof. Dr. Filiz SARI

ABSTRACT

The technology of energy harvesting has received a lot of attention by the researchers in light of the widespread use of electronic devices, especially wireless ones. It has become one of the most important research topics in the world for providing easy and free energy sources.

This thesis presents the effect of RF energy harvesting parameters depend on the harvesting system efficiency and the output DC voltage for input power between -35dBm to 25 dBm. In this study, multi-stage Dickson voltage multiplier (DVM) from two to six stages are designed and implemented for various load resistance (i.e. 20, 50, 100, 500, and 1000) kΩ and with a different matching topology such L-matching, T-matching, and Pi-matching. Two Schottky diode models (e.g. HSMS-2852 and HSMS-2822) are used to design the DVM to see their effect on the efficiency and output DC voltage, also to show the quality factor for different impedance matching topology's. All the simulations were done by using the Advance Design System (ADS) 2017. The target frequency selected in the design is 915 MHZ for Industrial, Scientific and Medical Radio Band (ISM band). The simulation results showed an improvement in term of efficiency for the DVM circuit design with matching compared to the DVM circuit without matching at the low level input power. Also, the simulation results show that low load usage increases the efficiency of the harvesting circuit. Besides, using a HSMS-2852 Schottky diode model is better in term of efficiency than the HSMS-2822. And also, for low input power the harvesting system with matching circuit give an advantage over the harvesting system without matching circuit for all design depend on the efficiency level.

Keywords: Radio frequency (RF) energy harvesting, Dickson-Voltage-Multiplier (DVM), ISM band 915 MHz, Impedance matching topology, Schottky diode, low power application.

March, 2019; 74 pages

LIST OF FIGURES **Page**

LIST OF TABLES

Page

LIST OF ABBREVIATIONS

AC	Alternative Current
ADS	Advanced Design System
AM	Amplitude Modulation
BTS	Base Transceiver Station
DC	Direct Current
DVM	Dickson Voltage Multiplier
ESR	Equivalent Series Resistance
FM	Frequency Modulation
GSM	Global System for Mobile communication
HPD	High Power Design
HPD	High Power Design
ISM	Industrial, Scientific and Medical
LPD	Low Power Design
PCE	Power Conversion Efficiency
Q-factor	Quality Factor
RF	Radio Frequency
TV	Television
UMTS	Universal Mobile Telecommunications System
WiMAX	Worldwide Interoperability for Microwave Access
UHF	Ultra High Frequency

1. INTRODUCTION

In recent years, researchers are frequently attracted to RF power harvesting as an alternative solution to short-life batteries. Harvesting RF signals from the environment are enabled to empower low power devices such as medical implants and network wireless sensors (Lu et al., 2015). The necessity for longer battery life has become risen after the rapidly grown of mobile technology since the 1980s. Besides, the necessity to improve battery life energy it became a major research area, also the advancements of energy harvesting helped manufacturers in their reconnoiter for better power supply (Mitcheson et al., 2008). There are many forms of energy harvesting such as waves harvesting, wind, sun and RF energy. RF energy is harvested from telecommunication systems which is available during the day with low power level.

There are four factors to harvest energy by manufacturer highlighted below (Lee et al., 2013):

1) Device's energy consumption
2) Usage pattern
3) Size
4) Motion and vibration.

Harvesting RF energy considered as one of the most significant types of energy harvesters. Many innovative methods are used to harvest energy such as solar and vibration and wind. Table 1.1 describes the types and value of energy harvested using the previously mentioned methods (Olgun et al., 2012).

The main idea of RF energy harvesting is capturing the transmitted RF energy from the environment to be used in low power circuits or stored to be used later. Receiving and converting RF signals to DC requires an efficient receiver (antenna) and rectifier circuit The efficiency of RF harvesting system relay on both of the efficiency of the antenna and the rectifier circuit. Besides, the system efficiency relies on the antenna impedance and the voltage multiplier impedance. If the voltage multiplier impedance is not matched to the impedance of the receiver (antenna), receiving all the signal at a given frequency would not be possible (Abdin et al., 2013).

Table 1.1. Energy harvesting values and types (Mansour, 2018)**.**

Source	Source power	Harvested Power	Advantages	Disadvantages
Light				
Indoor	0.1 mW/cm^2	10 W/cm^2	1) High power density 2) Mature	1)Not available always 2)Required exposure to light costly
Outdoor	100 mW/cm^2	10 mW/cm^2		
Vibration / Motion				
Human	0.5 m at 1 Hz		1) Implantable 2) High efficiency	1)Not available always 2)Material physical limitation
	1 m/s^2 at 50 Hz	4 W / cm^2		
Machine	1m at 5 Hz			
	10 m/s^2 at 1 kHz	100 W/cm^2		
Thermal				
Human	20 mW/cm^2	30 W/cm^2	1) High power density 2) Implantable	1) Not available always 2) Overflow heat
Machine	100 mW /cm^2	1-10 mW/cm^2		
RF				
GSM	0.3 W/cm^2	0.1 W/cm^2	1) Always available 2) Implantable	1) Low density 2) Efficiency inversely proportional to distance

The meaning of impedance matching is the source impedance is equal to the complex conjugate of the load impedance (rectifier with load impedance). The simple block diagram of energy harvesting system is shown in Figure 1.1, which is consists of the four components as follow (Nguyen et al., 2018):

1) Receiver (antenna)
2) Matching network
3) Voltage multiplier (AC to DC)
4) Load circuits.

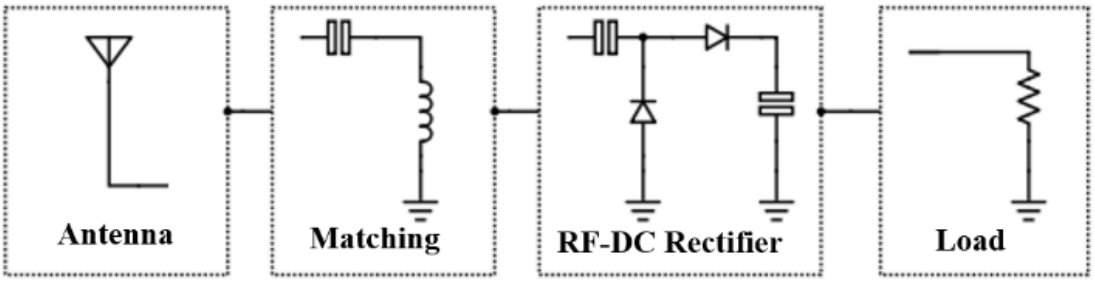


Figure 1.1. Energy harvesting system block diagram (Mansour, 2018).

The received RF signal passes through several units in harvesting system. Firstly, the RF source (Antenna), which collect the RF signal from the free space. Secondly, the matching network, which transfers a maximum RF power from the source (Antenna) to the load (Rectifier) (Felini et al., 2014). Thirdly, the multi-stage voltage multiplier circuit which converts the received AC RF signal to DC and rectified it (Piñuela et al., 2013). Lastly, the load circuit, which is the impedance of the connected device to the circuit (e.g. Battery, wireless network sensor, etc.).

1.1 Background and Context

Recently, rationalization and reduction of energy consumption became researcher's obsession, besides energy saving as well as utilizing it to prevent any wastage of energy. There are several ways to harvest RF energy (Paradiso et al., 2005), such as:

1) Television (TV)
2) AM (Amplitude Modulation)
3) FM (Frequency Modulation)
4) Cellular GSM (Global System for Mobile communication)
5) 2G, 3G, UMTS (The Universal Mobile Telecommunications System)
6) Wi-Fi, Wi-MAX (Worldwide Interoperability for Microwave Access)
7) Other instruments that transmit RF signals.

Radio frequency waves are characterized by having energy that can be harvested and converted into usable DC power at distances more than 100 meters by using antenna and voltage multiplier. By attaching a capacitor to the circuit to produce an efficient DC power ensures the reception of sufficient signals in the circuits with different concentrations of signals (Le et al., 2008). To maintain sufficient supply of energy in

midst of varying RF concentrations, a capacitor can be attached to the circuit system to output the required constant voltage (Han et al., 2013). A brief background on wireless energy harvesting is provided in the following sub-sections.

1.1.1 Global system for mobile communications (GSM 900-1800)

Nowadays Global-System-for-Mobile-Communications (GSM 900/1800) is widely used Around the world to transmit sound and data, as seen in Figure 1.2. (Poranki, et al., 2015).

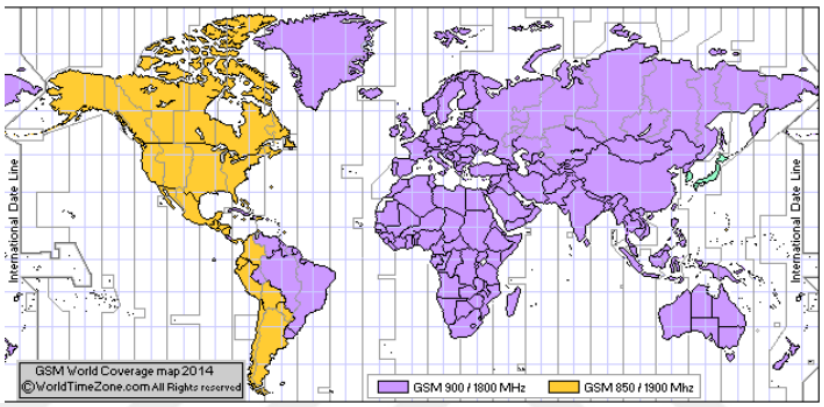


Figure 1.2. GSM 900/1800 world usage.

As illustrated in Figure 1.3. GSM900 used by some countries also it is consisting of two bands uplink and downlink. From 890 - 915 MHz used for uplink which means sending information from Mobile Stations to Base Transceiver Stations (Mobile Station to BTS) and from 935 – 960 MHz used for downlink receiving information from Base Transceiver Stations to Mobile Stations (BTS to Mobile Station). Every uplink/downlink band consists of 124 radio-frequency channels, each channel has 200 kHz bandwidth and the spacing between uplink and downlink is 45 MHz band at either end (Huurdeman, 2003).

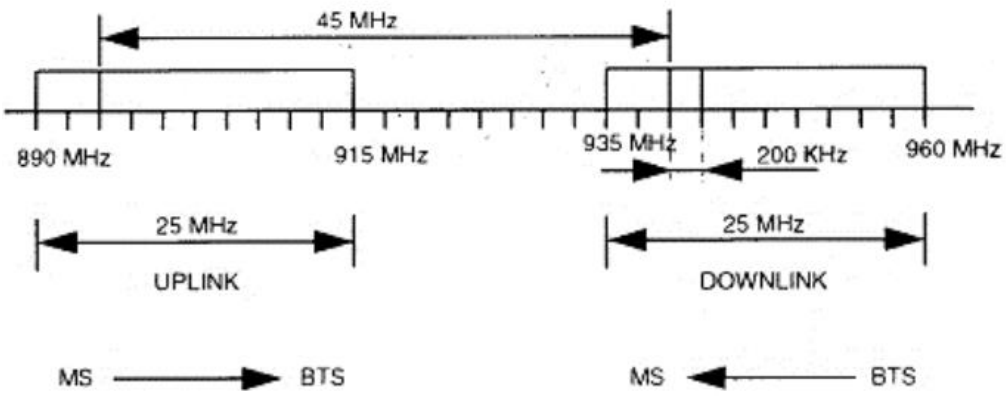


Figure 1.3. Uplink/downlink GSM 900 band.

As illustrated in Figure 1.4. GSM1800 frequency band is used by other countries. Also, GSM1800 consisting of two bands. The uplink band from 1710 - 1785 MHz which means sending information from Mobile Stations to Base Transceiver Station (Mobile Station to BTS). And downlink bands between 1805 - 1880 MHz which means receiving information from Base Transceiver Station to Mobile Station (BTS to Mobile Station). Every uplink/downlink band consists of 374 radio-frequency channels, each channel has 200 kHz bandwidth with 95 MHz spacing between uplink/downlink band at either end.

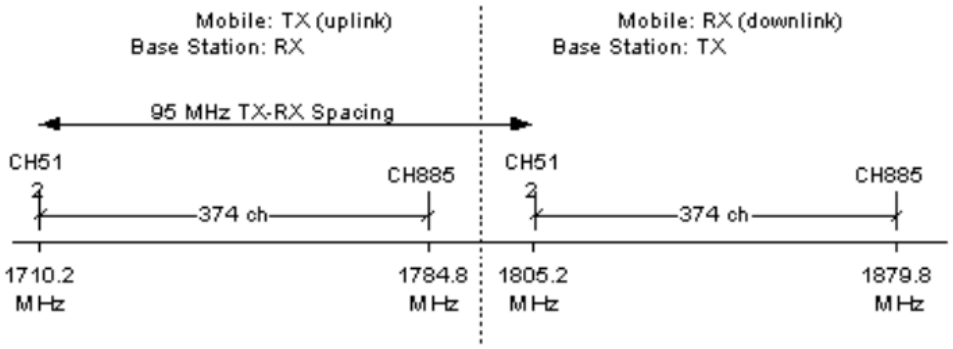


Figure 1.4. Uplink/downlink GSM 1800 band.

1.1.2 Universal mobile telecommunications service (UMTS)

The third generation mobile cellular, also known as Universal Mobile Telecommunications Service (UMTS) of networks based on GSM standards transmit text, voice, video, and digital assets at data rate up to more than 2 Mb per second.

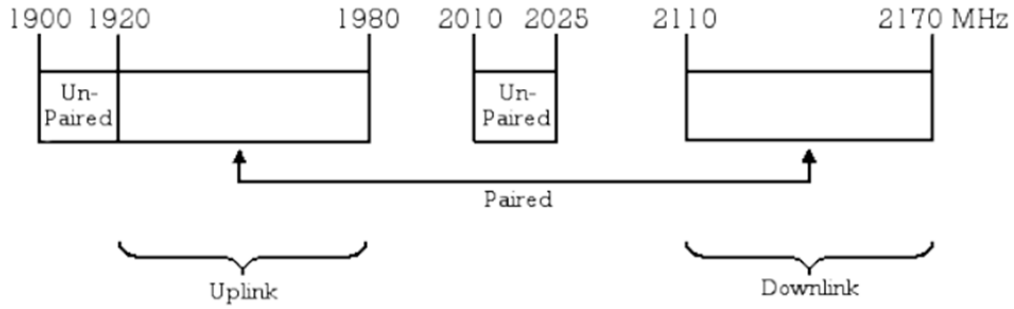


Figure 1.5. UMTS band uplink and downlink

The UMTS consists of two frequency band (i.e. uplink and downlink) the uplink frequency band starts from 1900 MHz to 2025 MHz while the frequency band for the downlink starts from 2110 MHz to 2170 MHz as illustrated in Figure 1.5. Besides, UTMS exists everywhere in the world thus it offers convenient range of services for mobile and smartphone users. UMTS has been adopted by manufacturers as a standard for worldwide mobile users. All UMTS devices (phones and computers) could be connected to the internet anytime/everywhere and all have the same set of capabilities, through a frequency range of accessible wireless and satellite connections (Samukic, 1998).

1.1.3 Wireless fidelity (Wi-Fi)

Wi-Fi (Wireless Fidelity) refers to wireless networking technology, which uses the RF band to provide internet through high-speed networks that allow devices to connect to the network. Wi-Fi band works on 2.4 GHz 892.11b standard from IEEE 802.11 organization WLAN standards. Wi-Fi has been expanded by WiFi Alliance to include all types of wireless (WLAN) based on 802.11 standards comprehensive dual-band, 802.11a, 802.11b, and others (Bloessl et al., 2013). In attempt to reduce noise on the WLAN, 2400 MHz and 2500 MHz are used to transmit low and high Wi-Fi waves, those hundred MHz divided into fourteen chanalls, twenty MHz for each

channel. In cunclusion, every 2.4 GHz overlaps with at least two or four channels as shown in Figure 1.6 (Chintalapudi et al., 2012).

Where Wi-Fi 802.11 standard uses 2400 MHz for uplink and downlink (Boccardi et al., 2016).

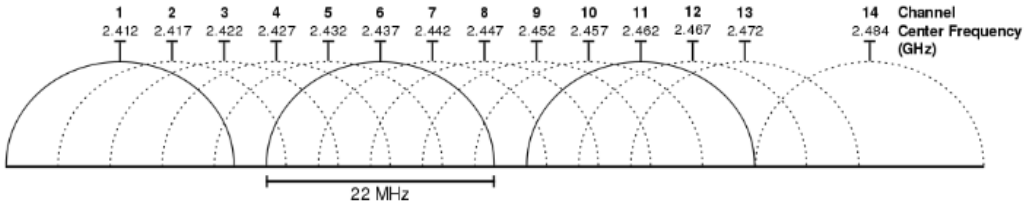


Figure 1.6. Wi-Fi standards channels.

Several tools depend on using Wi-Fi band (e.g. smart devices and homes, observation system, computers, video-game consoles, printers, smartphones, and tablet computers. All of the above can connect to the network by using access points. (Fontes et al., 2015).

1.2 Voltage Multiplier Circuit (Rectifier)

Designing circuit that operates on low voltage with high speed and high efficiency is a significant challenge for manufacturers due to the UHF frequency and low power of the RF signal (Keyrouz et al., 2013). The voltage doubler circuit shown in Figure 1.7 is the third part of the energy harvesting system, which is one of the important part due to its conversion role that epitomized by converting the received AC signal into a usable signal DC. There are several types of voltage multiplier e.g. Cockroft- Walton, Dickson volage doublure, etc. Those types will be further explained in CHAPTER 3.

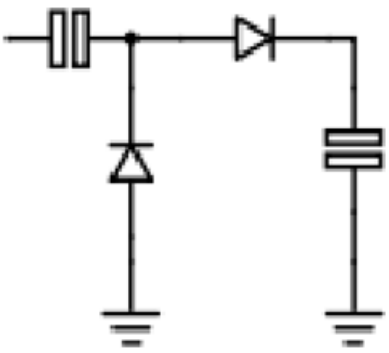


Figure 1.7. Simple rectifier circuit.

1.3 Impedance Matching Circuit

Since the source impedance and the load impedance are not equal, the received signal will reflect from the load towards the source. Therefore, will be lose some power in the received signal. Matching circuit prevents such loss of power due to the equalizing of the impedance of load with source impedance, i.e., the equalization of these impedances prevent reflect signals from load to source. Therefore, the signal will not be reflected and the highest RF power transfer can be done from source to load. (Khonsari et al., 2015).

Impedance matching is the second important part of harvesting system and microwave component design (Multiphysics et al., 2003 ; Kurniawan et al., 2014). As shown in Figure 1.8, there are three topologies to design the matching circuit using lumped element L-matching, T-matching and π-matching, those types will be well explained in CHAPTER3.

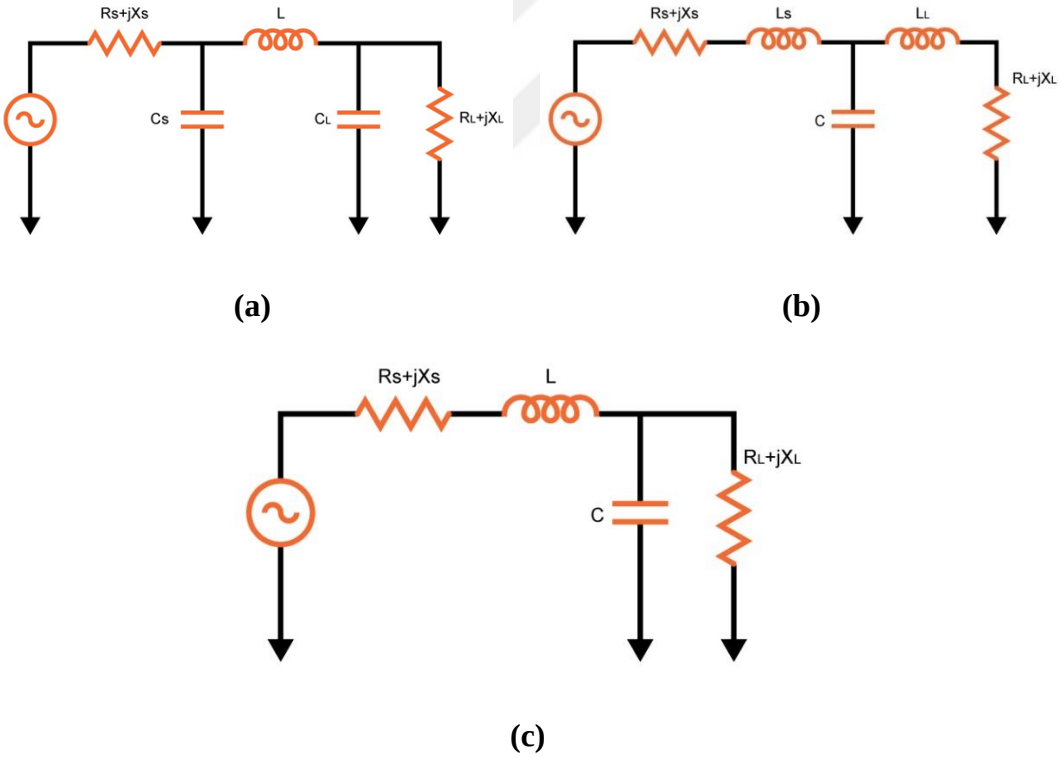


Figure 1.8. Matching topologies networks of (a) π, (b) T and (c) L .

1.4 Scope and Objectives

In this thesis, voltage multiplier characteristics are investigated and simulated for different power meters which are related with input power, number of voltage multiplier stages, diode types, matching topology effect and the quality factor. Efficiency and output voltages are used for comparison of the designed circuits.

1.5 Thesis Outline

This thesis is composed of five chapters:

1) Chapter 1: Introduction to the energy harvesting system component and an introduction for Radio Frequency (RF) band.
2) Chapter 2: Literature Review of RF-harvesting system and a rectifier design.
3) Chapter 3: Methodology of the thesis, detailing the properties of the component used in this thesis.
4) Chapter 4: Simulation result of the designed harvesting circuit and it's quality factor.
5) Chapter 5: Conclusion of this study.

2. LITERATURE REVIEW

Many researchers have improved the methods of RF energy harvesting and its parts such as matching type, voltage doubler, and its structure. Output parameters depending on harvesting circuit designed by them, analyzed and how much efficiency they obtain from their design.

2.1 Related Work

For decades, RF harvesting systems are studied, but only restricted RF sources have been able to supply enough power which may be utilized as a feasible source for low power applications. However, most of the energy management systems aren't efficient at ultra-low power sources such as RF sources because of power feeding in management circuitry. The solution for this issue may be either power consumption reduction that's limited by physical limitations or a different energy supply so as to obtain enough power capable to transmit toward the load

Five-stage voltage doubler with π type matching circuit was investigated in (Anika et al., 2018) as illustrated in Figure 2.1 for RF harvesting system the authors worked on Gsm-900 frequency band. The design and simulation were done by ADS simulator then they select a 180KΩ as a load resistance and measuring the output on it. They sweep the input power from -30dBm to 30dBm and select 915 MHz frequency for the design circuit. The results showed that the output voltage 9.6V at 0 dBm and they get 33.9V as a maximum at 20 dBm is reached at five stages. They also presented a comparison between earlier works on various voltage doubler stages of RF energy harvesting systems. Finally, they achieved that π type matching circuit operates in higher quality than other matching circuits.

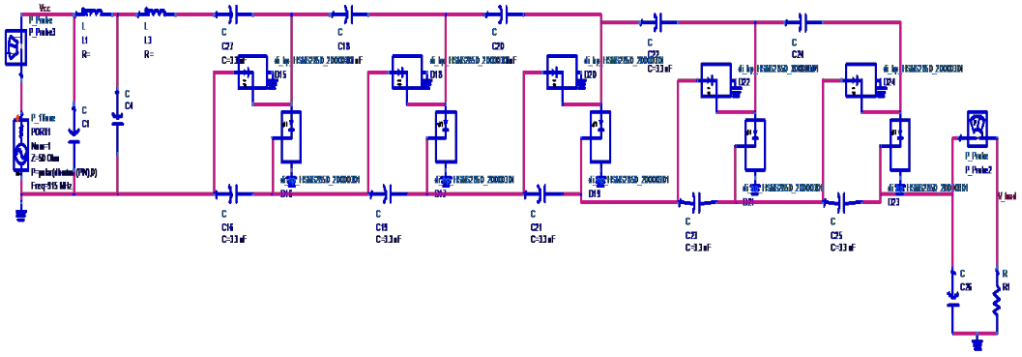


Figure 2.1. Five stage voltage multipliers with diode HSMS-2850 (Agilent ADS)

Devi et al., (2012) was optimized voltage multiplier stages number in their design for RF harvesting system, their design work on a 900 MHz frequency band. The design is built with Villard voltage multiplier. HSMS 2850 Schottky diode was used to design a seven-stage voltage multiplier as shown in Figure 2.2, the RF harvesting circuit modeling and simulation was formed in this research by Multisim program. Their design simulation and measurement was implemented for various power inputs. Their circuit design can harvest 3 mV at -40 dBm input power when the load is equal to 100 KΩ. Their work resultant 22 multiplication factor at 0 dBm input RF power, also achieves 5 V output DC voltage. The achieved voltage could be used to empower low power devices such as sensors wireless network.

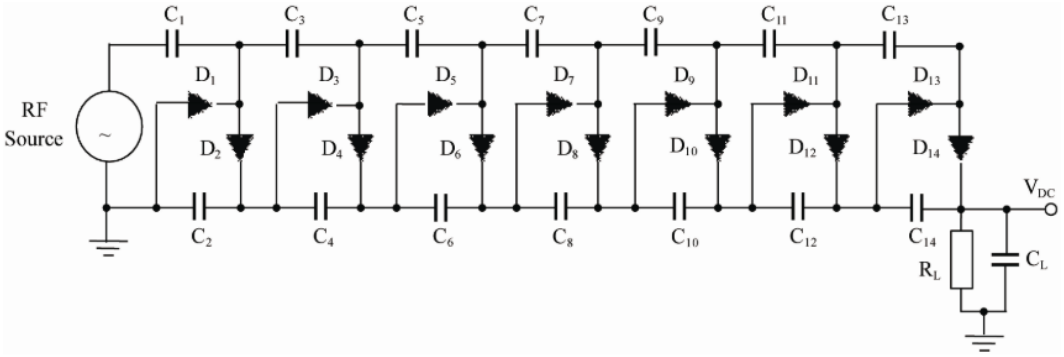


Figure 2.2. Design of a 7-stage voltage multiplier in Multisim.

Transformation of power without reflection between the source (antenna) and the load (Voltage multiplier circuit) both impedances of source and load must be matched. Adam et al., (2015) described and implemented the seven-stage voltage doubler for the harvesting system. Where their circuit works on 1.5 GHz with utilizing a Dickson voltage doubler type. Every stage contains two HSMS 2850 Schottky Diode model

and two 4.7nF capacitors. They have investigated the performance of matching network with Dickson voltage multiplier. As a result, enhancement in terms of efficiency was shown in their designed circuit compares with non-matching network harvesting system.

The continuous power source is a very significant issue in the purpose of the application of WSN. An optimization of the voltage multiplier stages in an energy conversion module for Radio-Frequency (RF) energy-harvesting-system at 950 MHz frequency band is presented by (Akter et al., 2014) as shown in Figure 2.3. Advanced Design System (ADS) simulator was used to design a 10-stage RF voltage multiplier for energy harvesting circuit, which harvests almost 5 Volt at 0 dBm input power and maximum 36.489 Voltage. Two 10 stage voltage doubler was designed and the Schottky diode HSMS-2822 and HSMS-2850 are used to design the rectifier. The result of these two diode models was compared, finally, it was confirmed that the HSMS-2850 works much better than HSMS-2822 diode. The designed system can be used to power low power sensors in sensor networks eventually in place of batteries.

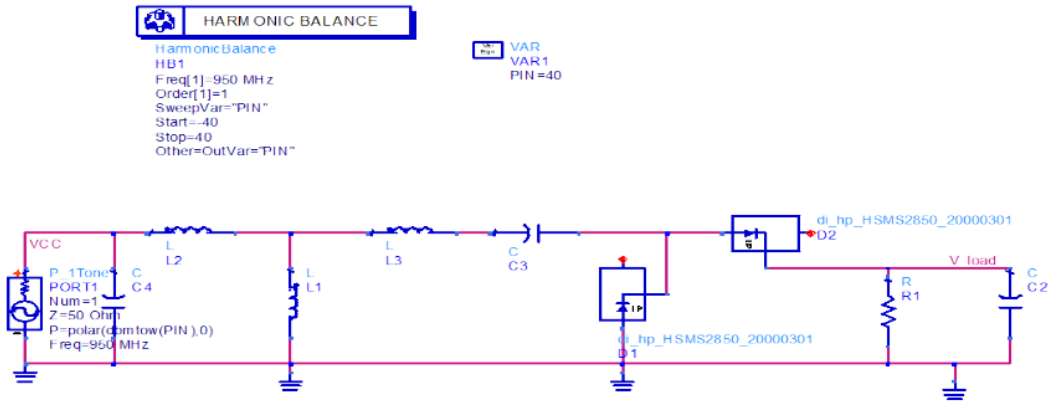


Figure 2.3. Single stage voltage multiplier using diode HSMS- 2850 from ADS at 950 MHz.

Ababneh et al., (2017) presented an improved power management system to progress the efficiency of DC to DC voltage doubler, this was done by employ particle swarm method, where the efficiency of a rectifier was used as the qualification function and inductor are selected as optimized parameters. This design progressed the DC to DC rectifier efficiency and the efficiency of the power management circuit by 9.25% compared with traditional power management circuits through a wide range of input

power, which gives a permission to harvest extra power from RF sources and transfer it to load.

Dickson voltage multiplier for low RF (Radio Frequency) input power was studied by (Marshall et al., 2015) as shown in Figure 2.4. They worked on ISM frequencies band typically utilized in RFID are 915 MHz, 2.45 GHz, 5.8 GHz. For the simulation, the authors used MATLAB software for the design. The paper observed at each of the design parameters and the considerations for choosing optimal values. A step by step process for designing a rectenna was included along with a list of universal procedures. The design used Skyworks diodes SMS7630. After analyzing their work results, they have determined that any more than dual stages will not reliably increase efficiency. But, adding more stages to the rectifier can increase output voltage if the input power and the load resistance are large. Also, through the simulation, they compared which diodes model work better at ISM frequency band for deferent input power levels. In summary, their work could be considered as guidelines that help manufacturers to improve designing Dickson voltage doubler.

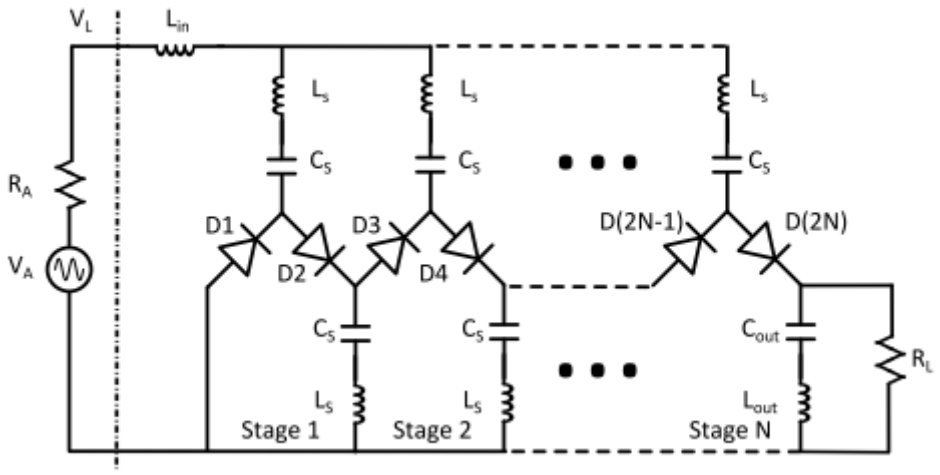


Figure 2.4. AC-DC Dickson voltage doubler for N-stage

Hameed & Moez, (2017) proposed a methodical design procedure to harvest RF signal with impedance matching network, to improve the efficiency of the harvested energy, as shown in Figure 2.5. In this work, the rectifier design depends on low power input such as RF signal, by using a transistor instead of a diode. Their simulation result shows that when the transistor based steady the largest DC harvest power achieve at certain input power. They maximized the harvested energy for various low input power by applying the matching circuit to the harvesting system. In their work, with using an off-chip for the matching network with selecting ISM band started from 902-928 MHz frequency band. In summary of their work, they achieved 32% efficiency at -15 dBm input power and output DC voltage around 3.2 V with connecting a 1MΩ resistive load.

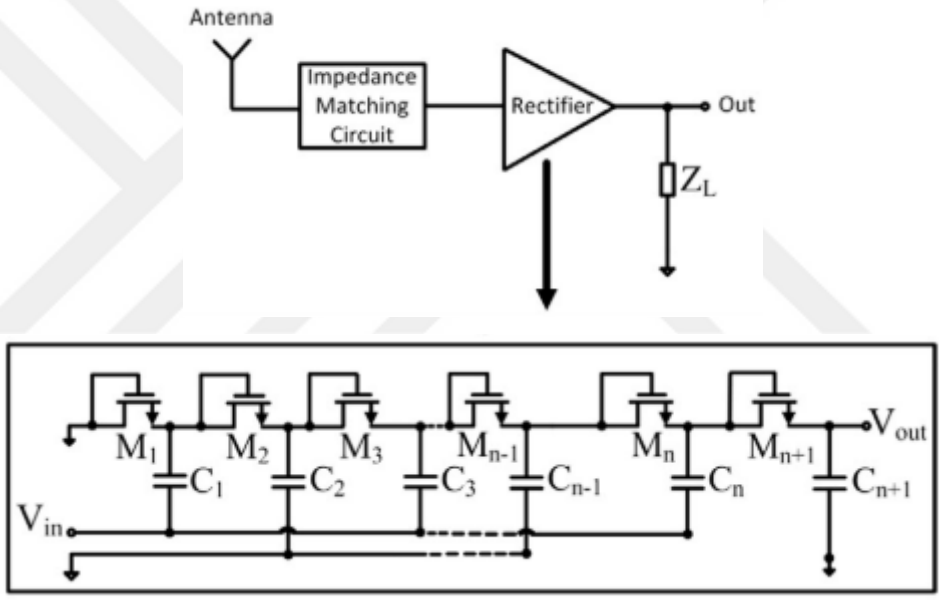


Figure 2.5. RF energy harvester with matching circuit (Hameed & Moez, 2017).

Bouchouicha et al., (2010) presented a study of techniques to harvest RF energy ambient. Bouchouicha and his friends designed two harvesting systems. The first system is for narrow bandwidth frequency starts from (1.8 - 1.9 GHz) along with using a matching network. The second non-matching network system for broadband frequency. They propose to harvest energy from broadcasting stations such as TV, WiFi, and GSM. They use (ADS) software for their design. The author selects a Schottky diode HSMS2850 to design a voltage multiplier as shown in Figure 2.6 below. Their result shows the harvested power not enough to power a small device, the harvested power could be stored in a micro-batteries or super-capacity.

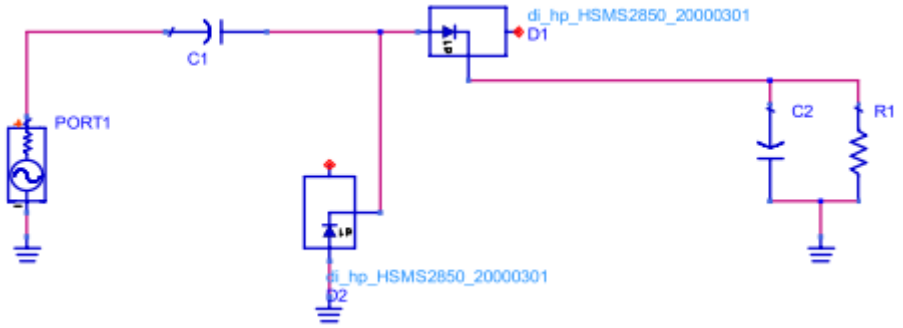


Figure 2.6. Schema of the rectifier (Bouchouicha et al., 2010).

3. DESIGN OF ENERGY HARVESTING CIRCUIT

In this chapter of the thesis we will discuss the whole design starting with the selection of the load resistance, then, the Dickson voltage multiplier and why we use this type in our design, as well as the considerations for diodes. Finally, the impedance matching circuit that we use in the thesis. And how to use the quality factor for designing the resonant network.

3.1 The Load

To start the design process, initially, a load must be chosen. Other researches on this subject, they used a load with high resistance to duplicate the conditions of microcontrollers that could be used in energy harvesting applications (Capstone et al., 2017). The input impedance and the efficiency of the harvesting systems fundamentally affected by the load resistance. So, in our design, we select different value of a load resistance from a small resistance to the large resistance, the values of the resistance that we chose are 20 KΩ, 50 KΩ, 100 KΩ, 500 KΩ, 1 MΩ. In order to compare between a different load resistance on the matching circuit and the efficiency of our circuit. Also, how the circuit we design proses with different load resistance Figure 3.1 shows the R load schematic in Keysight program Advanced Design System ADS 2017.

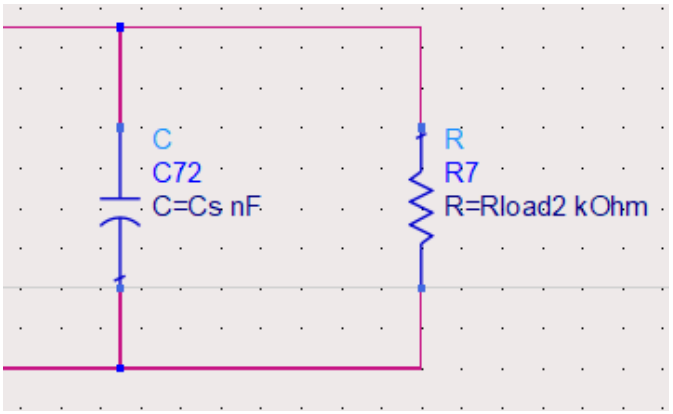


Figure 3.1. Load resistance schematic (Rload2).

3.2 Voltage Rectifier for RF Harvesting System

A cascade of rectifier unit referred to voltage multiplier generates an output voltage greater than the input voltage. A Cockcroft Walton multiplier also referred as Villard multiplier (Nintanavongsa et al., 2016) is given in Figure 3.2, or Greinacher multiplier (Chow et al., 2010) can be used to achieve the voltage multiplication as Figure 3.2. (Cockcroft et al., 1932). The Cockroft-Walton multiplier consists of cascade of rectifier stage including diodes and coupling capacitors to couple the charge from the clock through the diodes.

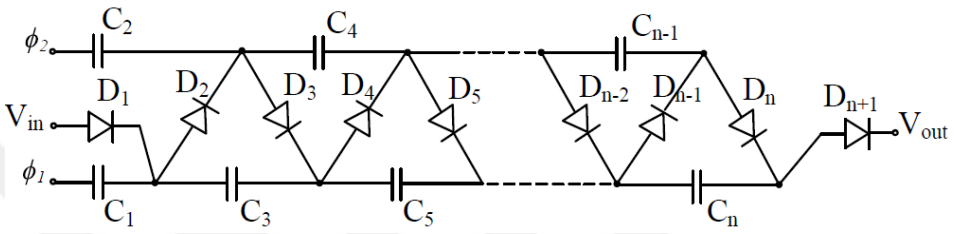


Figure 3.2. Cockroft- Walton voltage doubler.

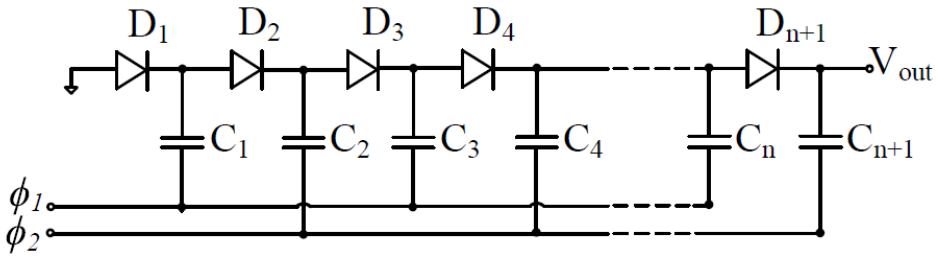


Figure 3.3. Dickson voltage multiplier.

The rectifier operates by transferring the RF signal toward the diode where the coupling capacitor is charged and discharged during each clock-cycle and the voltages will be doubled after each stage of the rectifier. However, increasing rectifier stages number, the coupling capacitor C of the rectifier should be greater than the parasitic capacitance of the diodes to have an efficient voltage multiplication. In order to overcome this limitation, DVM can be used as shown in Figure 3.3. (Dickson, 1976). It operates in a similar manner to the Cockroft-Walton multiplier with the input coupled through the capacitor in parallel instead of a series connection. Efficient multiplication is realized by DVM even with the relatively high value of parasitic

capacitance compared with the Cockroft-Walton multiplier. The circuit implementation of the multistage for RF energy harvesting is generally based on Dickson topology due to the fact of DVM is much proper for low power applications (Le et al., 2008 ; Han et al., 2013 ; Nintanavongsa et al., 2016).

The non-zero resistance of the rectifier circuit must be reduced to increase the power conversion efficiency of the rectifier. By operating the rectifier with minimum-threshold voltage, the value of output voltage and sensitivity of the rectifying devices will increase. Threshold voltage robustly affects the performance parameters of the energy harvesting systems. The input power at the rectifier must produce voltages exceeds the rectifying device threshold voltage to turn on the rectifier unit in the (RF to DC) voltage converter circuit. (Merz et al., 2014 ; Nintanavongsa et al., 2016). In terms of voltage level, a minimum input voltage is required for correct circuit operation and the voltage lies in the dead zone of the rectifier when the input voltage lies below the level (Dickson, 1976 ; Han et al., 2013)

For a multistage rectifier topology in Figure 3.2 with *N+1* diodes, the output voltage V_{out} can be expressed as

$$V_{out} = N \left(\frac{C}{C+C_{par}} V_{in} - V_{TH} - \frac{I_o}{f\,C}\right) - V_{TH} \qquad (3.1)$$

Where C is the coupling capacitance, C_{par} is the parasitic capacitance, Vin is the amplitude of the AC signal, V_{TH} is refered to diode's threshold voltage, f is the operating frequency and I_o is the load current. With increasing in the number of stages, the output voltage increases. An increased output current degrades the output voltage. The threshold voltage V_{TH} of the rectifying device is the critical parameter degrading the output voltage as seen in equation 3.1.

The dead zone of the rectifier is the input voltage levels, $V_{OUT} > 0$, expressed as

$$N \left(\frac{C}{C+C_{par}} V_{in} - V_{TH} - \frac{I_o}{f\,C}\right) - V_{TH} > 0. \qquad (3.2)$$

At the point $V_{OUT} > 0$, the circuit starts operating. The input voltage satisfying the condition is expressed as

$$V_{in} > \left(\frac{C+C_{par}}{C}\ \frac{N+1}{N}\right) V_{TH} + \frac{I_{\circ}}{fC} \qquad (3.3)$$

The major factor determining the dead zone is the threshold voltage (V_{TH}) of the rectifying device. Reducing the threshold voltage is an effective way of reducing the dead zone and improving the performance of the rectifier at low power levels.

3.3 Diodes Selection

The ability to operate the RF energy with low input power and with UHF is the crucial challenge for the energy harvesting system. For a standard 50Ω antenna, the −25 dBm received RF signal which is equal to 34mW power amplitude (URL-1). Becaused of weak peak AC voltage of the RF signal received by antenna wich is smaller than the threshold voltage for the diode (Zhao et al., 2012), than it is better to choose diode with minimum turn-on voltage. Besides, the harvesting system work with RF signals which mean working with very high frequency, therefor the diode should work in high speed switching time. So, care should be taken to choose diode models work in terms of the things mentioned above. In this thesis, Schottky diodes as shown in Figure 3.4 and Figure 3.5 is selected because of its manufacturing technique that is use a metal-semiconductor junction instead of a semiconductor-semiconductor junction. This technique allows the junction to work in a high speed switching time and need lower than 0.15V forward voltage drop to work.

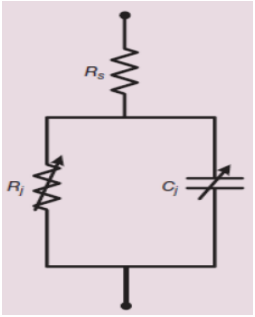


Figure 3.4. Equivalent circuit for Schottky diode.

Figure 3.5. 28XX-HSMS models of Schottky Diode

We select two different models of diodes from Avago Technologies, HSMS-2822 and HSMS-2852 as shown in Figure 3.5. The first one has a 340 mV turn-on voltage while the second model has a 150 mV turn-on voltage these values are taken from diode Datasheet, they measured them at 1 mA and 0.1 mA, separately. Therefore, HSMS-2852 is proper for low input power design (LPD) utilized in the low RF ambient, while HSMS-2822 is better to use for high input power design (HPD) in the crowded RF ambient (Zhou et al., 2012). Another critical parameter in the harvesting circuit is the saturation current because of its affections on the diode efficiency. It is preferred to use diodes with high saturation current, a small equivalent resistance, and low junction capacity. Furthermore, diodes with greater saturation current produce higher forward current. However, larger diodes have a high saturation current, which has substrate capacitance and higher junction. The last two parameters scan lead to an increase in a power wastage, then we will lose the benefit of a high saturation current.

The Current-Voltage {I-V} characteristics were obtained from the diodes circuit shown in Figure 3.5 and It is equivalent circuit shown in Figure 3.4, the output of Figure 3.3, that the Skyworks diode has a lower knee voltage, which made it better suited for low power applications.

Figure 3.6 shows a circuit to test the HSMS-2852 and HSMS-2822 in Advanced Design System ADS, Figure 3.7 and Figure 3.8 illustrated the characteristic of these two Schottky diodes.

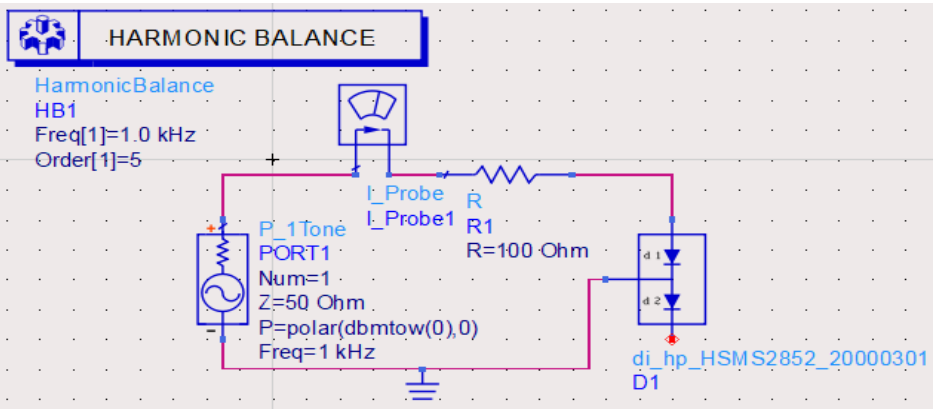


Figure 3.6. Diode testing circuit.

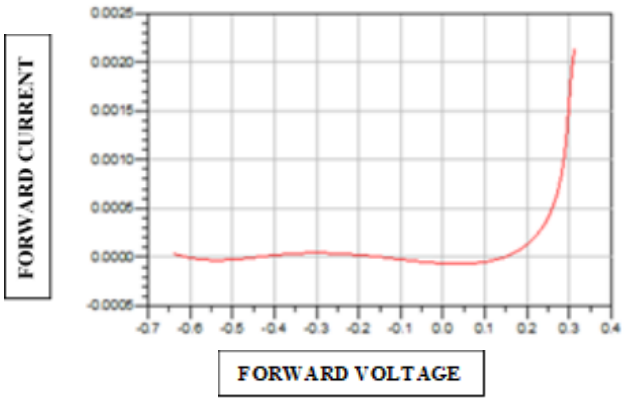


Figure 3.7. Characteristic of Avago HSMS2822.

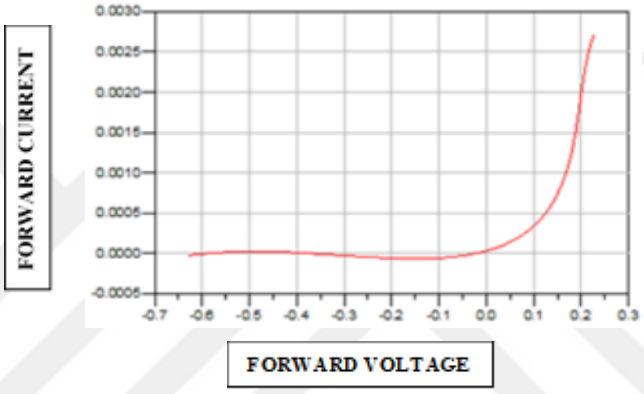


Figure 3.8. Characteristic of Avago HSMS2852.

3.4 Theory of Matching Topology

The moment that the voltages multiplier is designed, the next point is to design a matching circuit so as to transfer maximum RF power from the antenna to the load also to reduce the reflected power toward the antenna. There is various type of matching circuit can be used for this task such as L-matching, T-matching, and π-matching (Breed, 2008). L-matching topology is a popular type matching circuit as shown in Figure 3.9, and it's contains one inductor and one capacitor. However, T-matching and π-matching topology employ three reactive element (e.g. inductor-capacitor-inductor or capacitor-inductor-capacitor) as shown in Figure 3.10 and Figure 3.11. This supplementary element supply T-matching and π-matching circuits elasticity in terms of bandwidth (Saberkari et al., 2016), Figure 3.9 , Figure. 3.10 and Figure 3.11 illustrate the lumped element of the L-matching, Pi-matching, and T-matching circuits respectively. The prevalent rule is that a combined topology should

be used for either of these networks only if the component length is less than one-tenth of the operational wavelength (Brandl et al., 2018). As a model for of the L-matching, T-matching and π-matching applications are shown in (Soltani et al., 2010 ; Şengül et al., 2011). If the design seek for distributed matching circuits, different matching options exist such as employing a single-stub and double-stub tuning circuit (Khansalee et al., 2014). Each of these options minimizes the complexity of industrialization compared to bundled circuits at the expense of the harvesting system size and cost, (John et al., 2012 ; Johnson et al., 2004) give a description detail of the matching circuits.

For our thesis, the L-network, T-network, and π-network are the chosen for the matching circuit because of its design simplicity as well as its capability to be designed with the lumped element. The general concept of any matching circuit is to introduce elements necessary to make the load impedance equal to the complex conjugate of the source impedance. Assume that the source impedance is equal to the characteristic impedance of a transmission line $Z_\circ$ so the complex load impedance is given by Equation 3.4.

$$Z_\circ = R_L + \mathrm{j}\,\mathrm{X}_L \tag{3.4}$$

where R_L and X_L referred to the load resistance and reactance respectively. Rely on the proportional size of R_L compared to $Z_\circ$, There are two unique design configurations with each case. For $R_L < Z_\circ$, the topology shown in Figure. 3.12, must be used to guarantee a solution occur for X and B (John et al., 2012), if the matching is achieved, then

$$\frac{1}{Z_\circ} = jB + \frac{1}{R_L + j(X + X_L)} \tag{3.5}$$

By separating the real and imaginary parts of each side of Equation (3.5) and setting the corresponding components equal to each other, then the values for X and B are given as

$$X = \pm\sqrt{R_L(Z_\circ - R_L)} - X_L \tag{3.6}$$

$$B = \pm\frac{\sqrt{R_L(Z_\circ - R_L)/R_L}}{Z_\circ} \tag{3.7}$$

An important observation from Equation (3.6) and Equation (3.7) is that two solutions exist. One of the result is a shunt capacitor with a series inductance, other result is a shunt inductor with a series capacitor. These two solutions are depending on the application, one arrangement may be more useful than the other. While these two solutions will work for the DVM, the shunt capacitor and series inductor are the matching circuit topology to resonant the DVM (Sogorb et al., 2008).

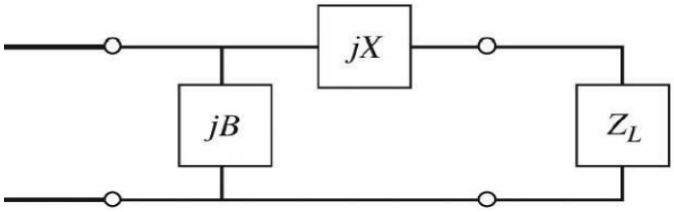


Figure 3.9. L-matching network.

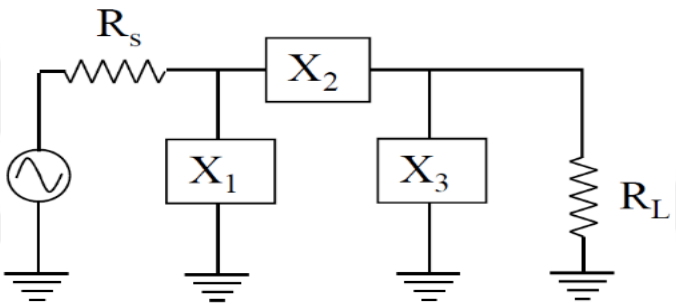


Figure 3.10. π-matching network.

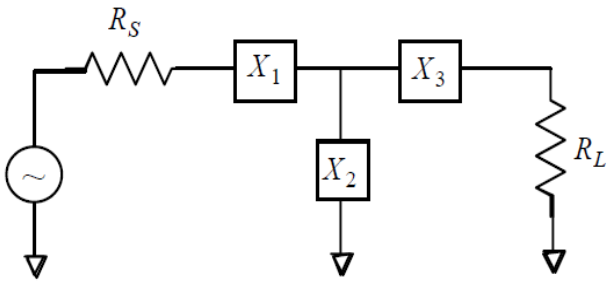


Figure 3.11. T-matching network.

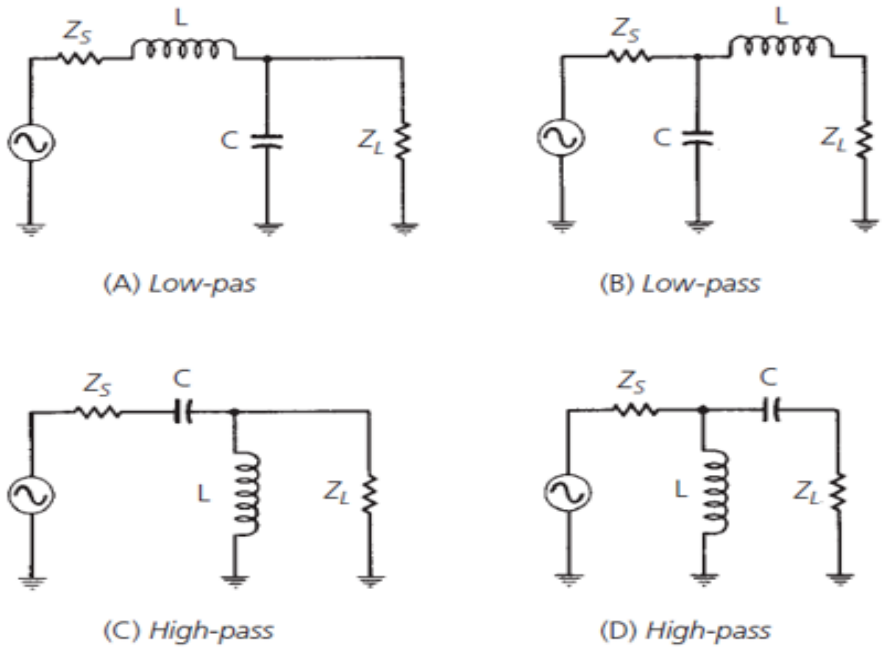


Figure 3.12. L-matching network types.

3.5 Quality Factor (Q-factor)

The quality factor or Q factor is measure of reactance's purity of a coil, capacitor-inductor (how close it is to be a pure reactance and not a resistance) in terms of its losses and resonator bandwidth (Merz et al., 2017). Also, the quality factor is very important parameter of the matching circuit which describes how under-damped a resonator or oscillator is and as well characterizes a resonator's bandwidth relative to the center frequency (Waters et al., 2012). High Q factor indicates lower rate of energy loss relative to the stored energy of the resonator (Wyndrum, 2008). A high quality factor also means that the resonator swings with a higher amplitude at the resonance frequency but has a smaller bandwidth compared to low Q circuits. There is a singularity between different kinds of quality factors in a circuit. The quality factor of a single blind element e. g. an inductor or a leg is called component Q or unloaded Q. The quality factor of a whole circuit is called loaded Q or circuit Q because it describes the passband characteristics of the resonant circuit under loaded or actual in-circuit conditions (Sun et al., 2002).

The quality factor equation as the Q definition (Neo et al., 2006)

$$Q = \pi \frac{\max instantaneous\ energy\ stored}{energy\ dissipative\ per\ cycle} \tag{3.8}$$

The quality factor for a reactive component is given in the two equations below

$$\text{Q of an inductor:} \quad Q = \frac{X_L}{R_L} = \frac{\omega L}{R_L} \tag{3.9}$$

$$\text{Q of a capacitor:} \quad Q = \frac{X_c}{R_c} = \frac{1}{\omega C R_c} \tag{3.10}$$

The Q factor equations used to design the L-matching networks given if Figures 3.12 are:

$$Q_p = Q_s = \sqrt{\frac{R_p}{R_s} - 1} \tag{3.11}$$

$$Q_s = \frac{X_s}{R_s} \tag{3.12}$$

$$Q_p = \frac{R_p}{X_p} \tag{3.13}$$

The X_p and X_s may be either inductive or capacitive reactance but each must be of the opposite type.

T-matching circuit can be understood as two L-matching circuit separated by a virtual resistance (R_V) as shown in Figure 3.13. In this Figure, X_{S1} and X_{P1} are reactance of the first L-matching circuit, and X_{S2} and X_{P2} are reactance of the second L-matching circuit. The two L-matching circuits can be analyzed separately and then combined into a single T-matching circuit by removing the virtual resistance.

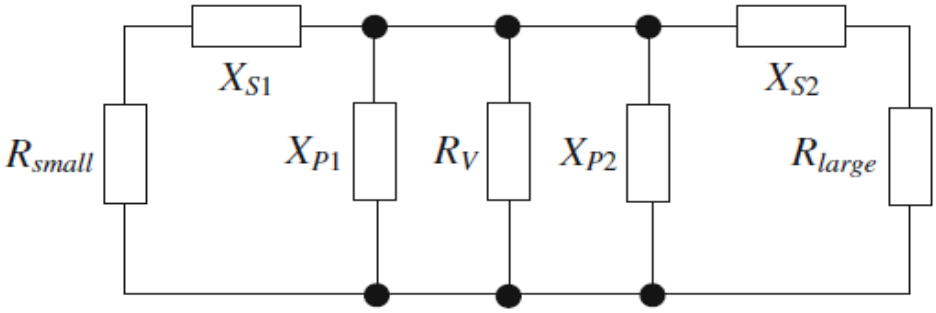


Figure 3.13. T-matching circuit consisted of two L-matching.

The virtual resistance is found using:

$$R_V = R_{small}(Q^2 + 1) \tag{3.14}$$

where (R_{small}) is the minimum value of (R_S or R_L), and $Q = f_0/BW$ is the desired Q-factor of the matching circuit calculated from the operating frequency f_0 and bandwidth BW.

Series reactance X_{s1} is:

$$X_{s1} = QR_s \tag{3.15}$$

Parallel reactance X_{p1} is:

$$X_{p1} = \frac{R_V}{Q} \tag{3.16}$$

For the second L-matching circuit a separated Q- factor should be calculated:

$$Q_2 = \sqrt{\frac{R_V}{R_L} - 1} \tag{3.17}$$

So X_{s2} and X_{p2} are:

$$X_{s2} = Q_2 R_L \tag{3.18}$$

$$X_{p2} = \frac{R_V}{Q_2} \tag{3.19}$$

After all the reactance's have been calculated and the virtual resistance has been removed, X_{P1} and X_{P2} can then be combined in parallel to get the final reactance X_P:

$$X_p = \frac{X_{p1}\, X_{p2}}{X_{p1}+X_{p2}} \tag{3.20}$$

Same procedure can be applied to the π-matching circuit, with the little bit difference, in this case, serial reactance X_{S1} and X_{S2}, instead of parallel reactance X_{P1} and X_{P2}, are separated by a virtual resistor, as illustrated in Figure 3.14.

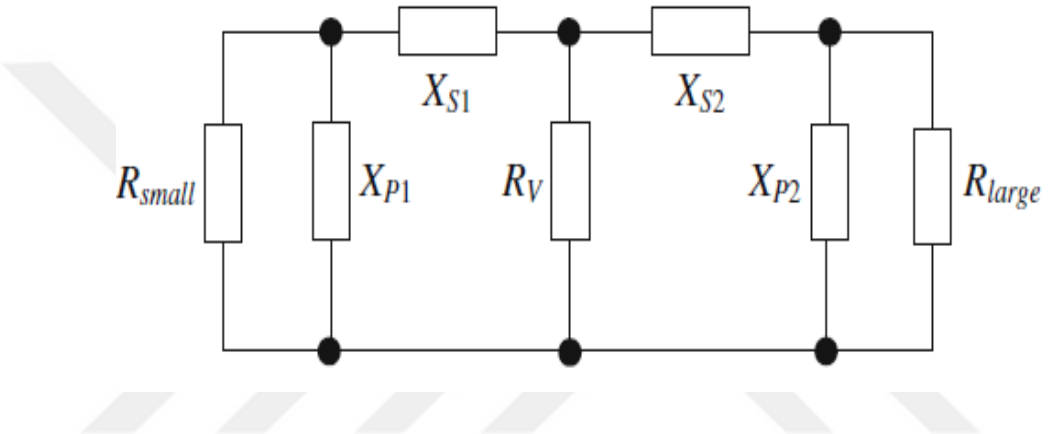


Figure 3.14. Two L-matching circuits separated by the virtual resistance creating a π-matching circuit.

The equation of a virtual resistance is:

$$R_V = \frac{R_{large}}{Q^2+1} \tag{3.21}$$

Where R_{large} is the maximum value of (X_s or X_L).

$$X_{s2} = Q\, R_V \tag{3.22}$$

$$X_{p2} = \frac{R_L}{Q} \tag{3.23}$$

The quality factor of the first L-matching circuit is:

$$Q_1 = \sqrt{\frac{R_s}{R_v} - 1} \tag{3.24}$$

X_{s1} and X_{p1} are can be calculated as:

$$X_{s1} = Q_1 R_V \tag{3.25}$$

$$X_{p1} = \frac{R_p}{Q_1} \tag{3.26}$$

After calculating these values, we can remove the virtual resistance and add (X_{s1} and X_{s2}) together to create a Pi-matching circuit.

3.6 Harvesting System Design and Simulation

Advanced-Design-System (ADS) (Avago technologies 2017) was used to design and simulate a DVM with multi-stage and two modal of a diode by using harmonic balance techniques. In particular, a multi-stage DVM will be considered (i.e. two-stage, three stages, four-stage, five-stage and six-stage) using two model of Schottky diode HSMS-2822, HSMS-2852 from Avago Technologies, and different impedance matching circuit type, like (L – π – T) matching networks. Note that for the designed circuit, the result was collected with a different load resistance 20 – 50 – 100 – 500 – 1000 KΩ, which will be shown later in the next chapter. In all cases, the output voltage increases with increasing input power until the reverse break down voltage of the Schottky diodes is exceeded. The output voltage curves are then relatively constant for the remaining power levels. Besides, the maximum DC output voltage increases with increasing the number of stages. However, increasing the number of stages leads to lower rectified output voltages. This is a reflection of the fact that larger input voltages are required to forward bias the Schottky diodes used in additional stages. Since the matching network provides a gain, it is expected that the use of a matching network would improve the output voltage of the voltage multipliers for low power levels. Figure 3.15 and Figure 3.16 show the design harvesting circuit schematic for a two and five stages DVM with matching circuit.

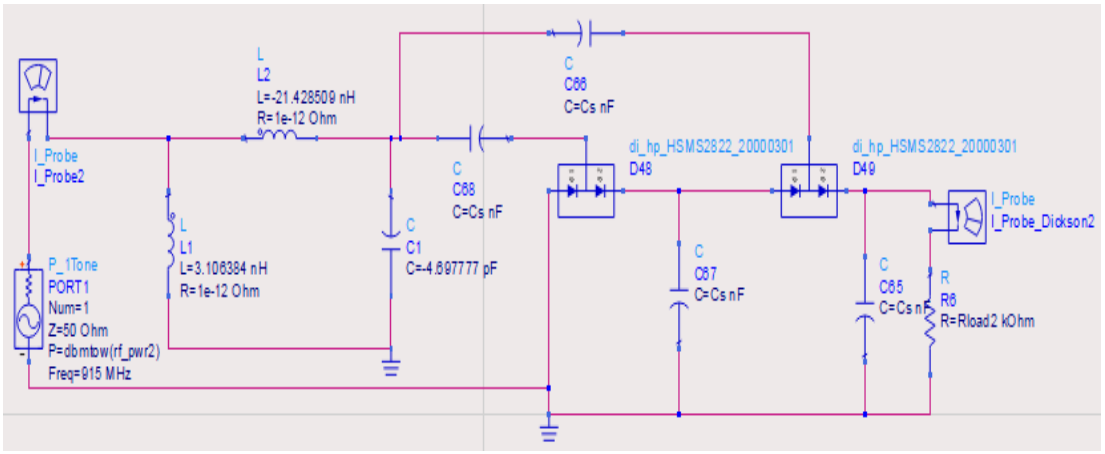


Figure 3.15. Two-stage DVM with the π-matching circuit.

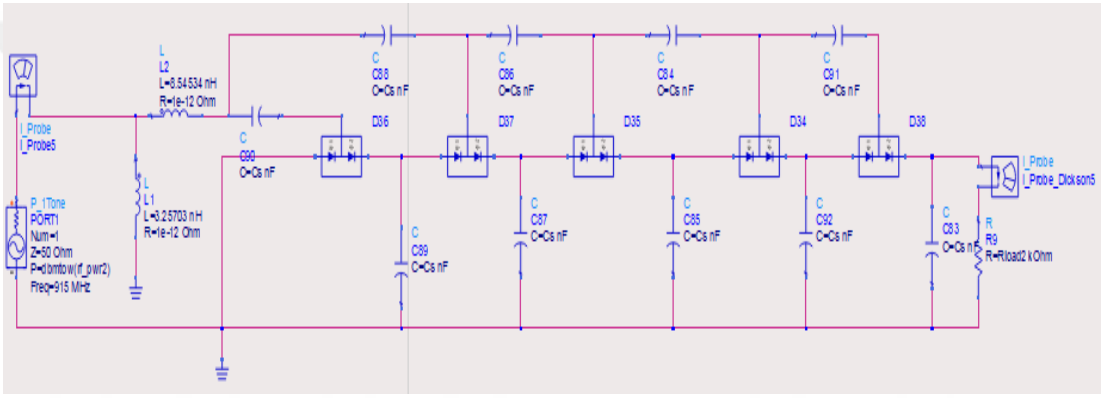


Figure 3.16. Five-stage DVM with L-matching network.

4. SIMULATION RESULTS

ADS simulation software is used for this thesis. Load resistance effect, input power, and matching types are analyzed depending on the voltage multiplier diode modal and the number of stages for the DVM. Efficiency and, output voltages are compared to each other for the harvesting circuit with matching and the harvesting circuit without matching to show the effect of each element in the harvesting system on the efficiency and output voltage.

4.1 Load Effect Comparison

Different load resistances (20 – 50 – 100 – 500 – 1000) KΩ are applied to the harvesting circuit with various stage number (2 – 3 – 4 – 5 – 6) stages of the DVM with two Schottky diode modal (HSMS2822 – HSMS2852) comparison.

The efficiency and output voltage for 20 KΩ load resistance and multi-stages DVM with and without matching circuit for HSMS2852 as can be seen in Figure 4.1 that the two-stage is much better than the higher stage in a low input power and the efficiency of two-stage reaches 45% at input power -10 dBm while the two stages reaches 5% efficiency at -10 dBm when there is no matching circuit.

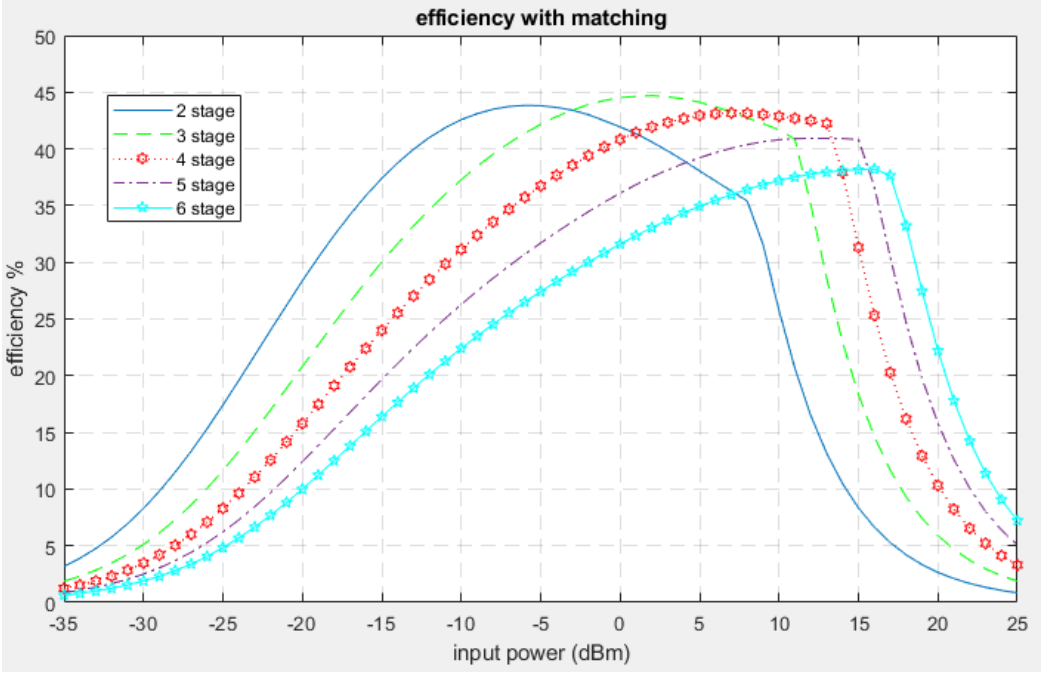


Figure 4.1. Efficiency with matching for 20kΩ load resistance for HSMS2852.

In addition, the circuit with matching is better than the circuit without matching in low input power according to simulation result as shown in Figure 4.1 and Figure 4.2. However, for the higher stages and the circuit without matching gives high efficiency for high input power as shown in Figure 4.2. The six stages achieve 60% efficiency at 15 dBm input power while the six stages achieve approximately 37% at 15 dBm input power when the matching circuit is applied.

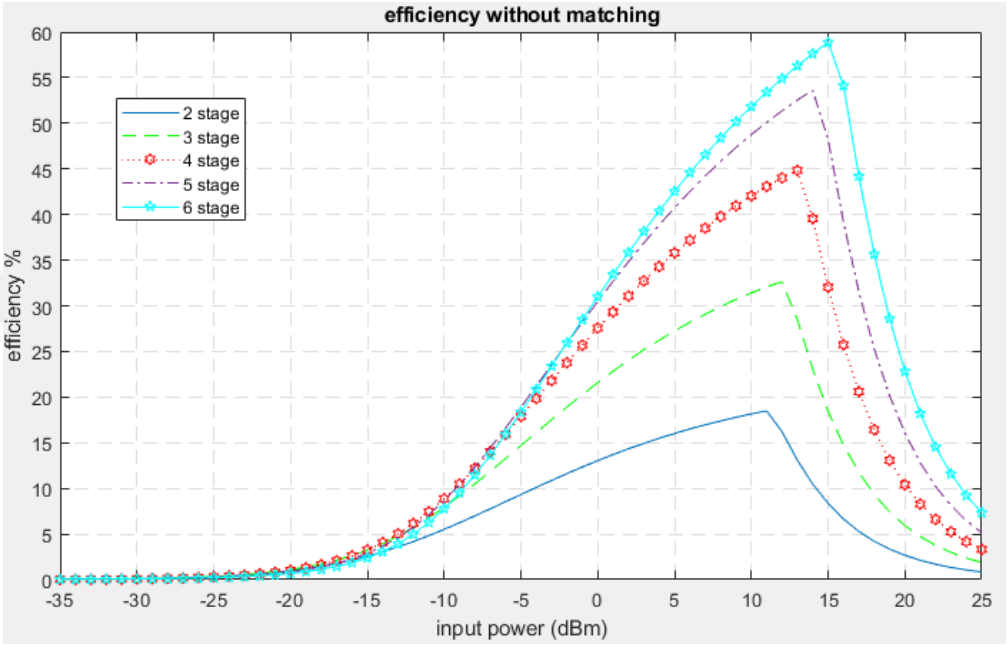


Figure 4.2. Efficiency without matching for 20kΩ load resistance for HSMS2852.

So, the harvesting circuit with a matching network is much better than the harvesting circuit without a matching network in a low input power.

Voltage comparison for 20 KΩ load resistance with different stages number of voltage multiplier with and without matching impedance is analyzed in Figure 4.3 and Figure 4.4. When the number of stages increase the output voltage will increase. In addition, the output voltage does not affect the matching circuit.

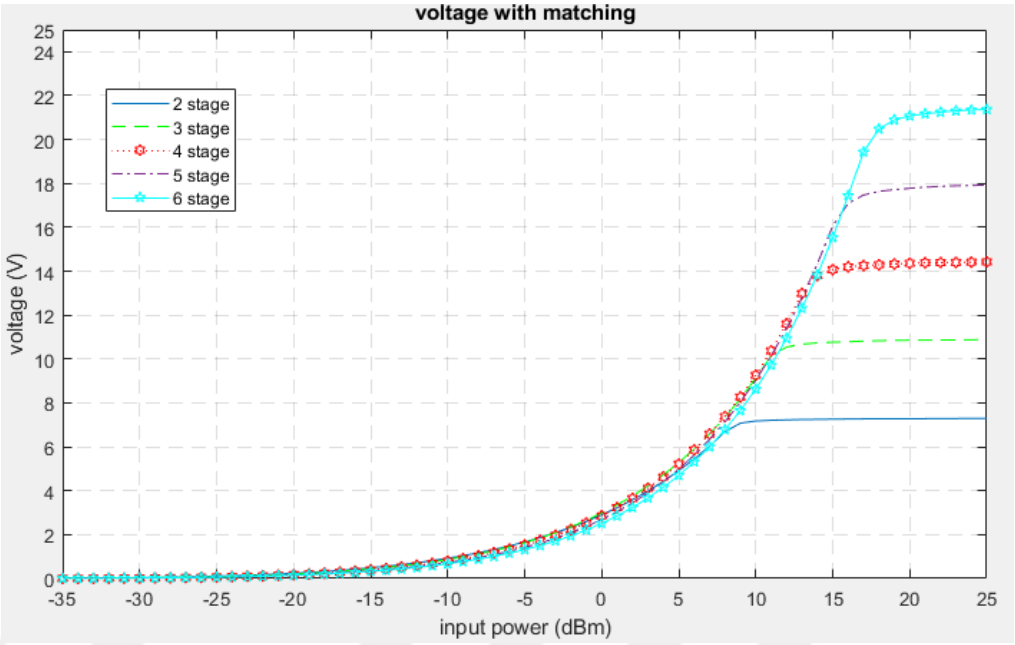


Figure 4.3. Voltage with matching for different stages for HSMS2852.

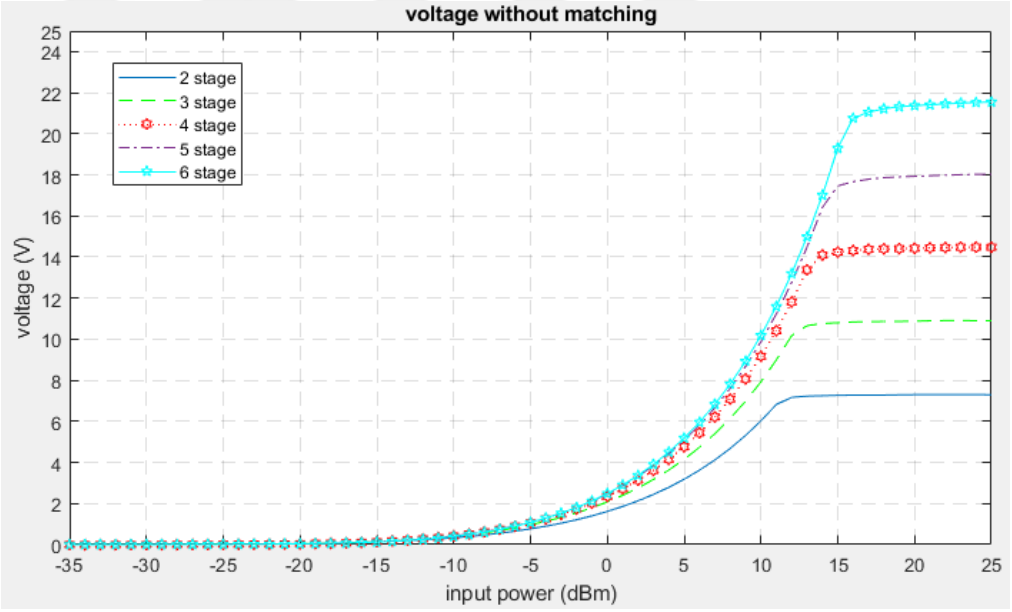


Figure 4.4. Voltage without matching for different stages for HSMS2852.

For HSMS-2822 diode model as given in Figures 4.5 and Figure 4.6 that the HSMS-2822 efficiency is better than the HSMS-2852 in high input power as shown in Figure 4.6 and the maximum efficiency is more than 45% at 25 dBm input power. Furthermore, the two-stage reaches approximately 11% efficiency in -10 dBm input power and it clear that the fewer number of DVM stage give high efficiency than the high DVM stage number as illustrated in Figure 4.5.

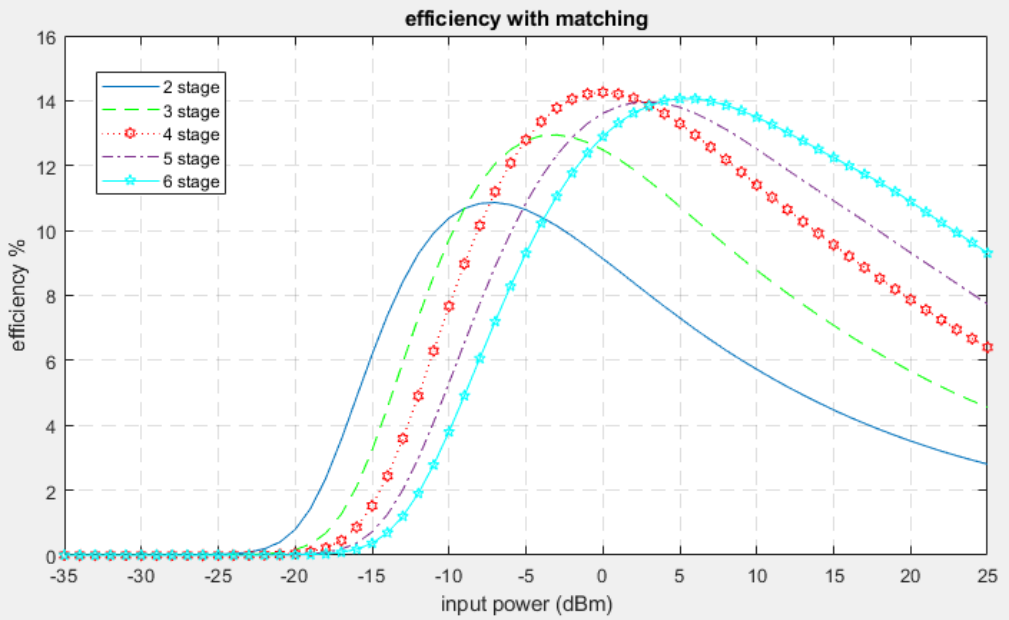


Figure 4.5. Efficiency with matching for HSMS-2822 and 20 kΩ load resistance.

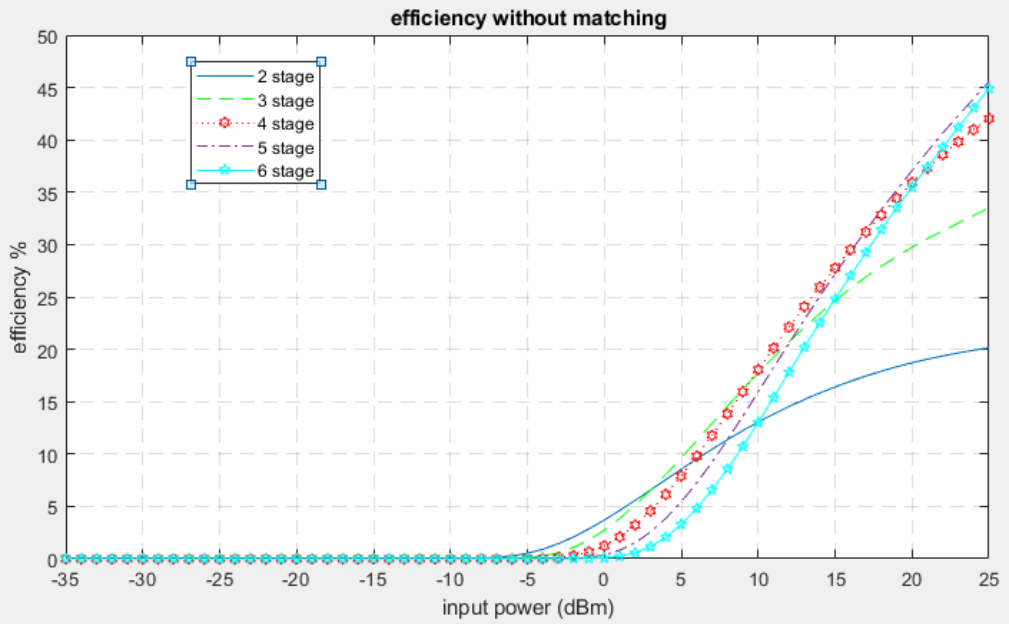


Figure 4.6. Efficiency without matching for HSMS-2822 and 20 kΩ load resistance.

The simulation results for HSMS-2822 give higher voltage than the HSMS-2852 as shown in Figures 4.7 and Figures 4.8. Besides, the circuit with matching and without matching does not affect to the output voltage when HSMS-2852 diode model used to design DVM, however, when HSMS-2822 diode model used to design DVM the output voltage effect to the matching circuit as shown in Figure 4.7 and Figure 4.8.

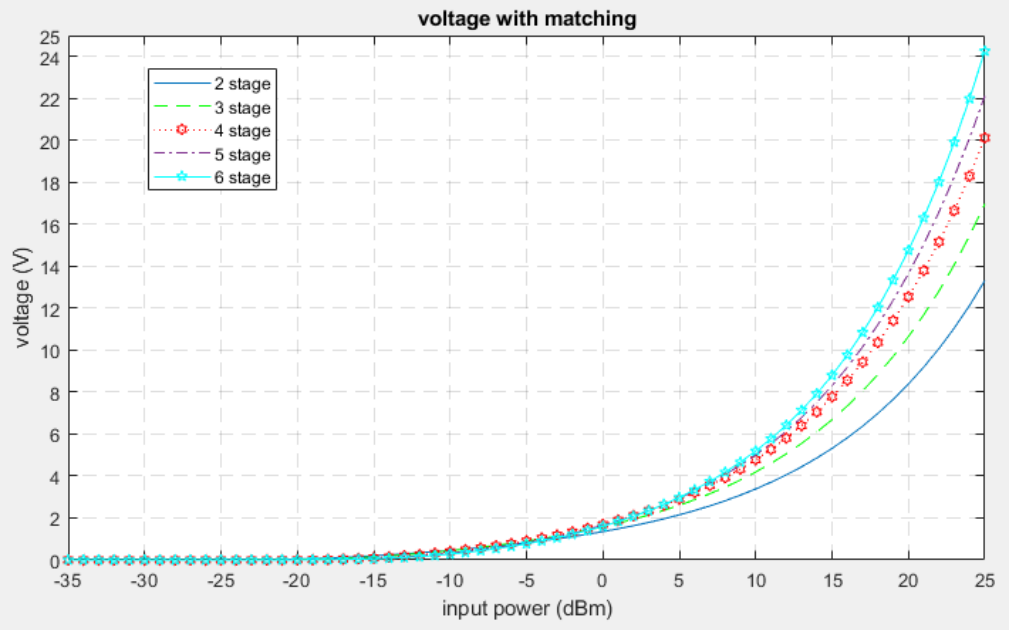


Figure 4.7. The output voltage for multi-stage DVM with matching for HSMS-2822.

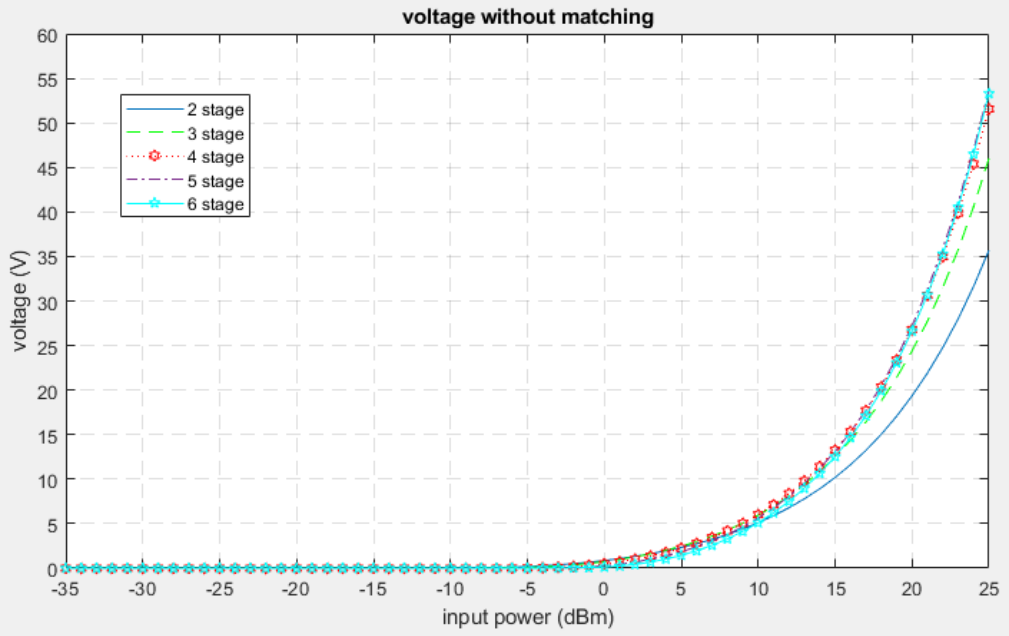


Figure 4.8. The output voltage for multi-stage DVM without matching for HSMS2822.

For the harvesting circuit efficiency and output voltage with 500 KΩ load resistance and multi-stages DVM with and without matching circuit. Firstly, HSMS-2852 diode is investigated the simulation result shows that when the value of load resistance increases the efficiency decrease and the higher stages number is better than the low

stage number. As shown in Figure 4.9 the maximum efficiency is approximately 18% at -15 dBm input power. However, the circuit with matching is better than the circuit without matching as illustrated in Figure 4.9 and Figure 4.10.

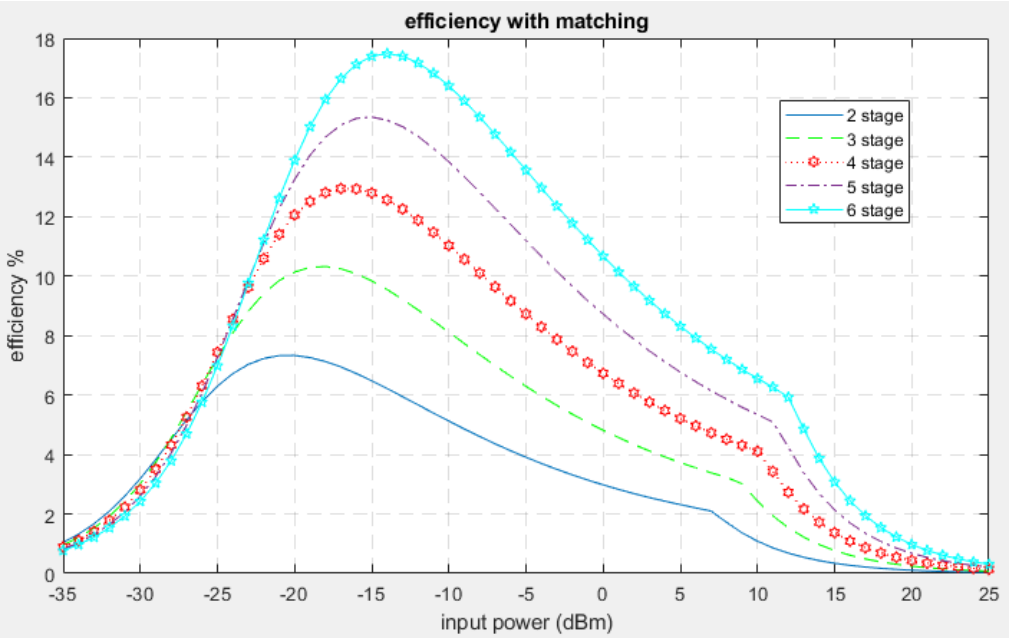


Figure 4.9. Efficiency with matching for 500Khom load resistance for HSMS-2852.

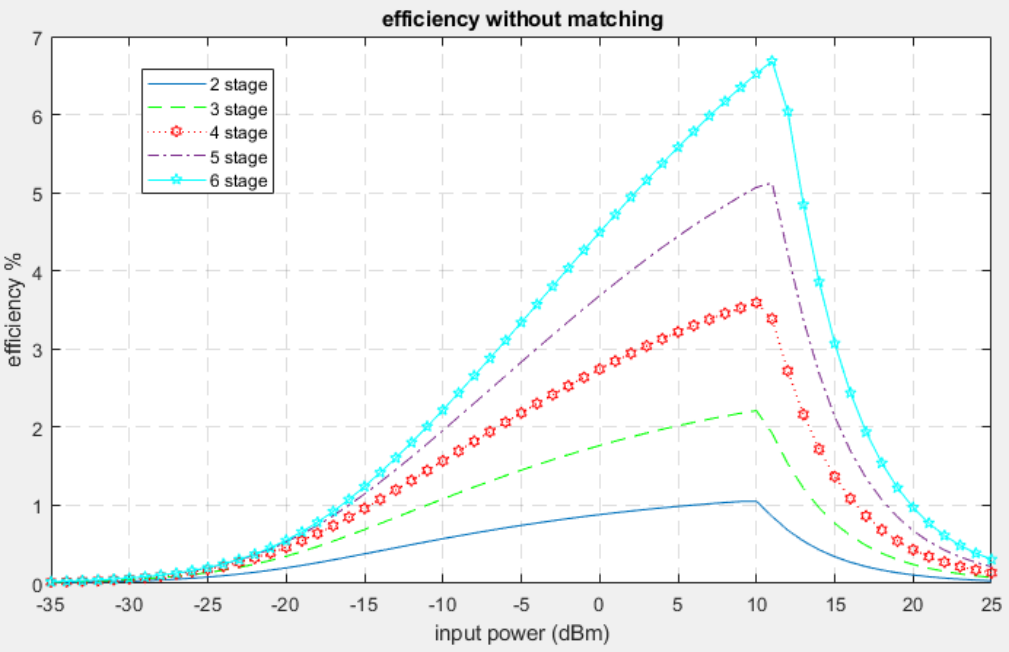


Figure 4.10. Efficiency without matching for 500Khom load resistance for HSMS2852.

The output voltage of the DVM with 500 kΩ load resistance with using HSMS-2852 diode models does not affect to the matching network as illustrated in Figure 4.11 and Figure 4.12.

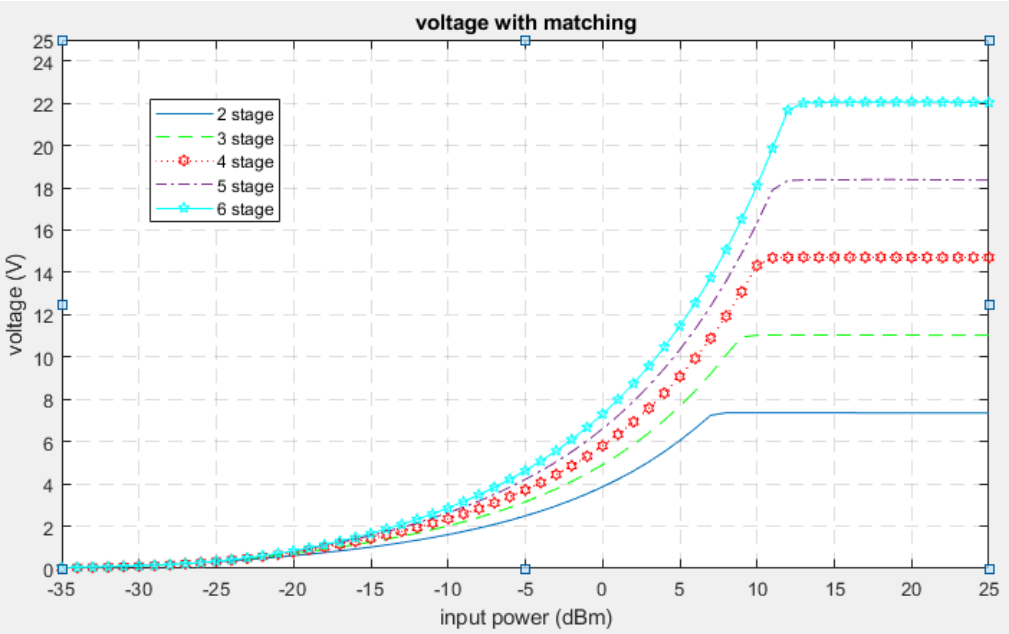


Figure 4.11. Output voltage with matching for HSMS-2852.

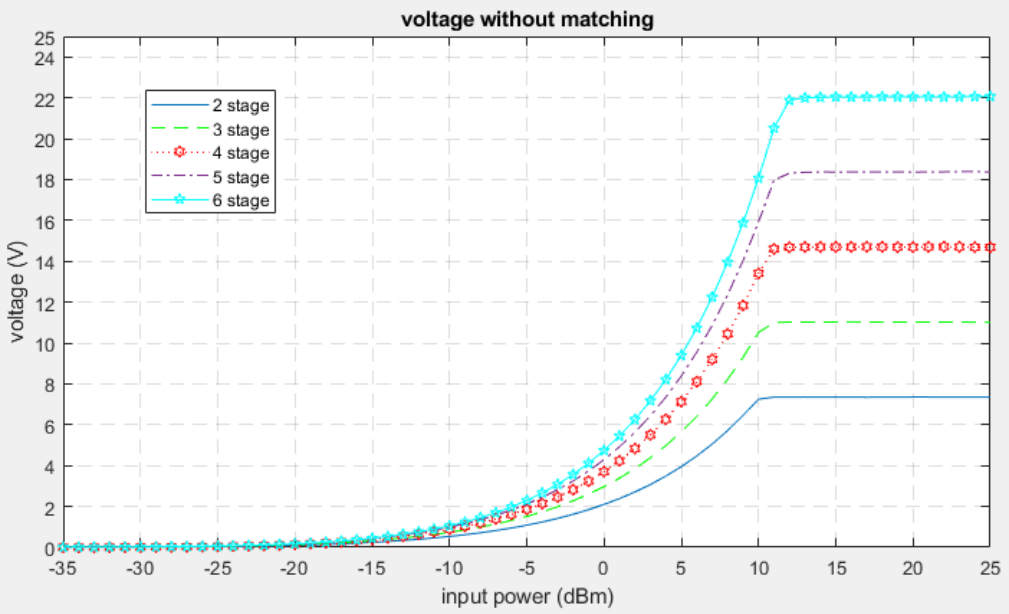


Figure 4.12. Output voltage without matching for HSMS-2852.

Secondly, HSMS-2822 diode models used to design a multi-stage of DVM with 500kΩ load resistance, the simulation results show that when the load resistance increase the efficiency of the circuit decrease as shown in Figure 4.13. In addition, the efficiency for HSMS-2822 in low input power is very low. Besides, the circuit with matching work better in low input power as shown in Figure 4.15.

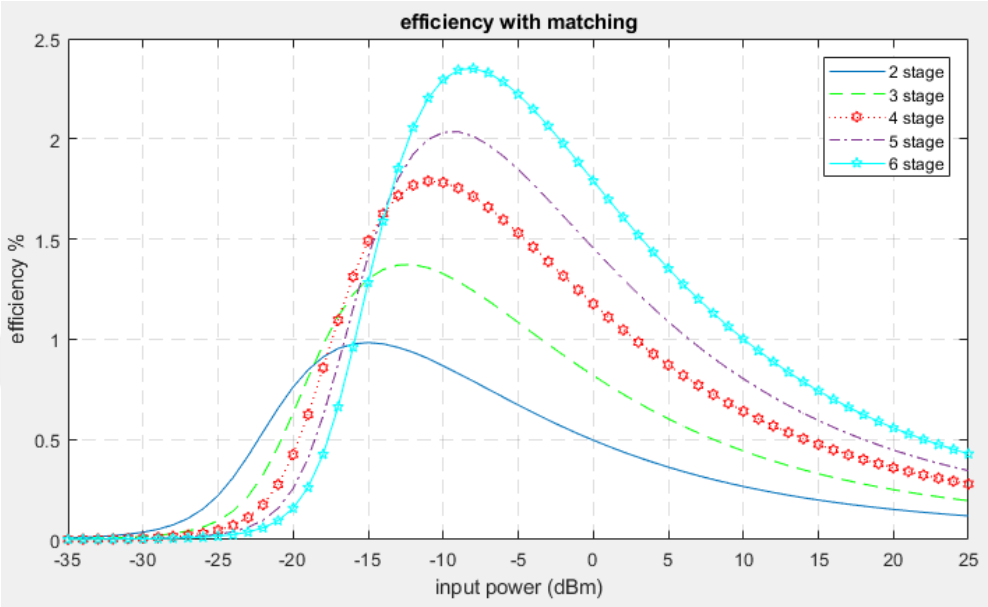


Figure 4.13. Efficiency with matching for multi-stages DVM and 500kΩ load resistance for HSMS-2822.

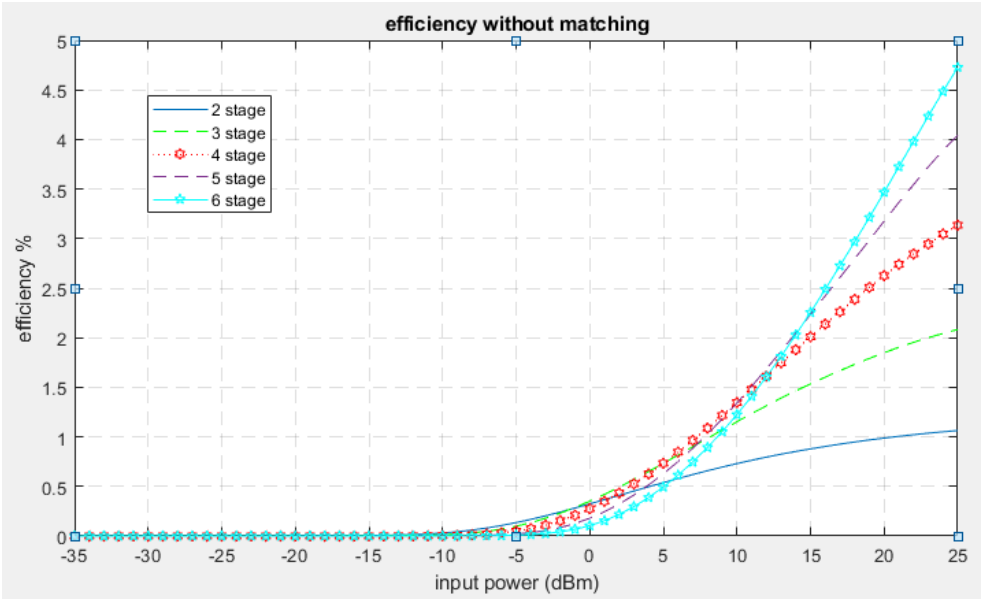


Figure 4.14. Efficiency without matching for multi-stages DVM and 500kΩ load resistance for HSMS-2822.

When the load resistance increases and HSMS-2822 diode model is used to design a DVM without matching network the output voltage increases in high input power as shown in Figure 4.14. However, in low input power, the output voltage is approximately equal even the circuit with matching or without matching as illustrates in Figure 4.15 and Figure 4.16.

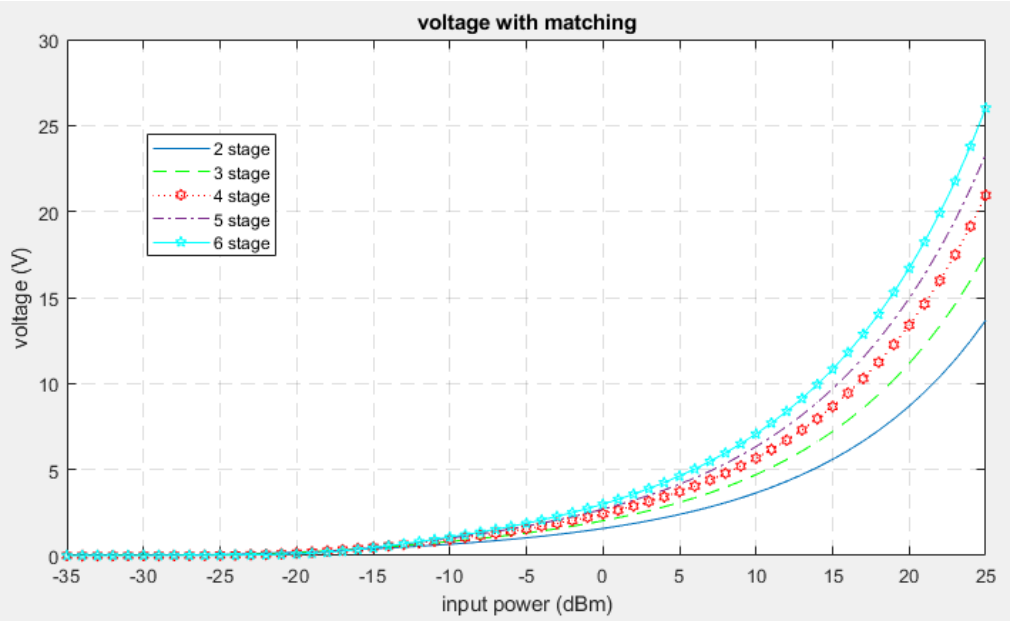


Figure 4.15. The output voltage for multi-stage DVM with matching for HSMS2822.

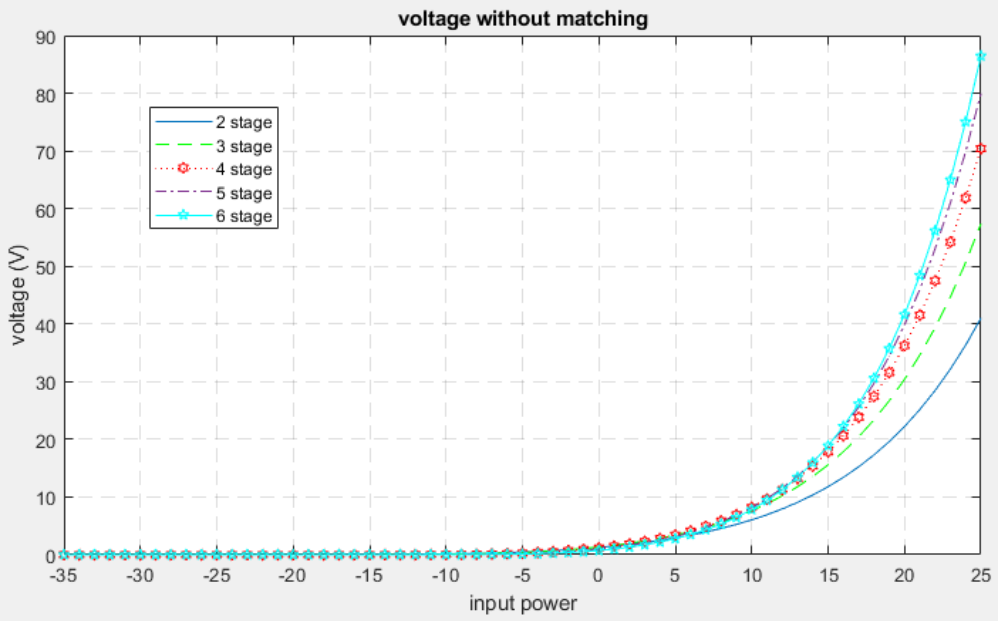


Figure 4.16. The output voltage for multi-stages DVM without matching for HSMS2822.

Lastly, harvesting circuit efficiency for different load resistance with and without matching network for HSMS-2852 diode model and different load resistance the Figure 4.17, Figure 4.18, Figure 4.19 and Figure 4.20 illustrated the efficiency for three stages and six stages DVM with and without matching network for different load resistance (i.e. 20kΩ, 50kΩ, 100kΩ, 500kΩ, and 1MΩ). As shown in Figure 4.17, Figure 4.18, Figure 4.19 and Figure 4.20 how the efficiency affected by the (e.g. matching network, the number of stages and the value of the load resistance).

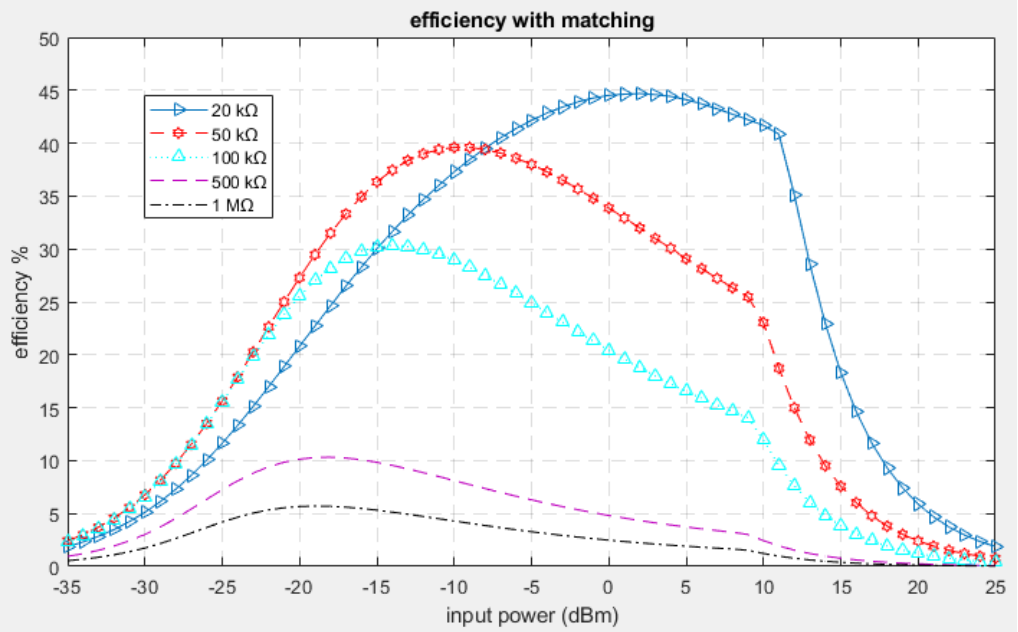


Figure 4.17. Three stage efficiency for different RL with matching for HSMS-2852.

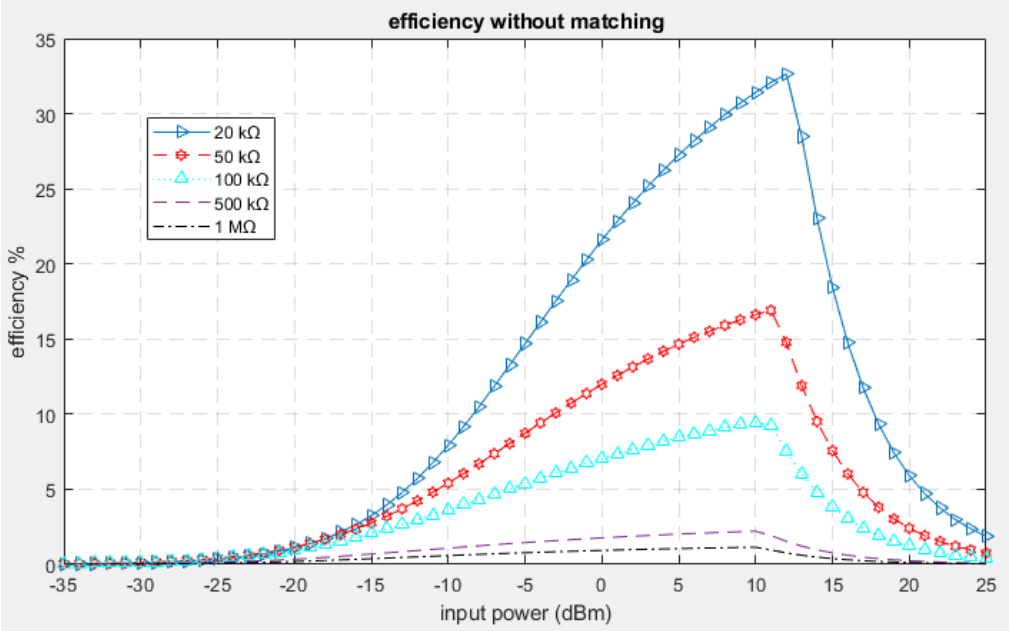


Figure 4.18. Three stage efficiency for different RL without matching for HSMS-2852.

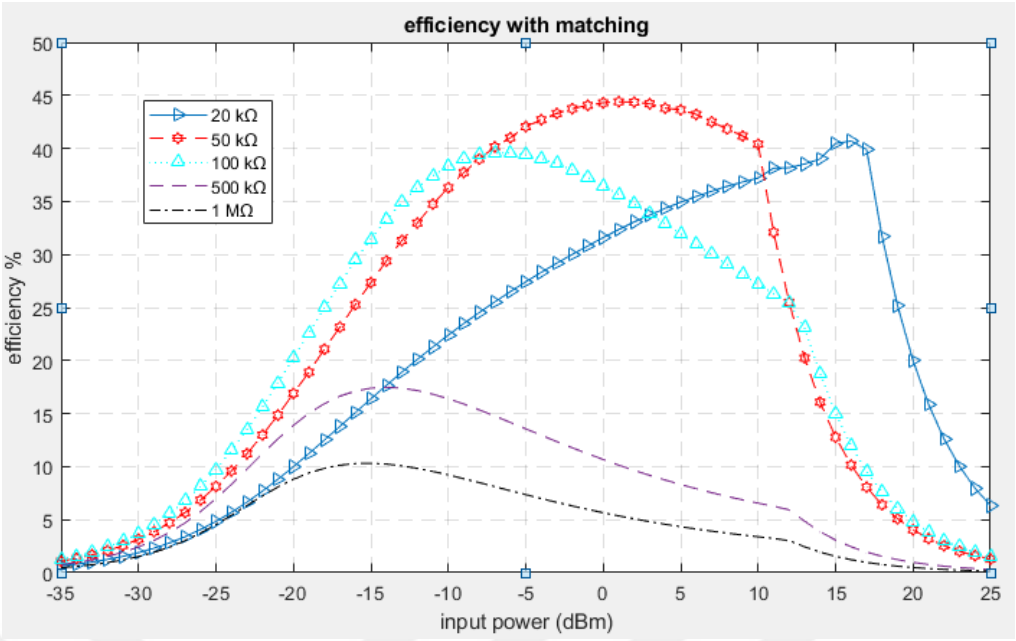


Figure 4.19. Six stage efficiency for different RL with matching for HSMS-2852.

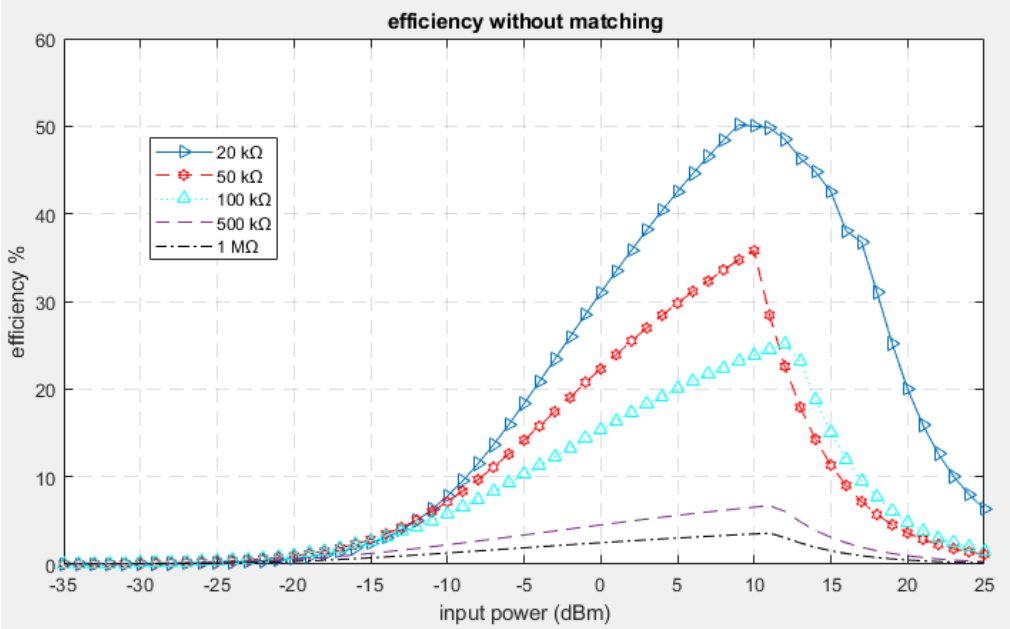


Figure 4.20. Six stage efficiency for different RL without matching for HSMS-2852.

For HSMS-2822 diode model with three and six stages DVM with matching and without matching circuit investigated in this study to show the effect of load resistance for fixed stage number on the efficiency of the harvesting circuit as given in Figure 4.21 and Figure 4.22, three-stage efficiency with and without matching network as can be seen the efficiency decrease when load resistance increase. Figure 4.23 and Figure 4.24 describe the efficiency of six stages DVM with matching and without matching network as shown in Figures below the six-stage efficiency better than the two-stage efficiency for fixed load resistance.

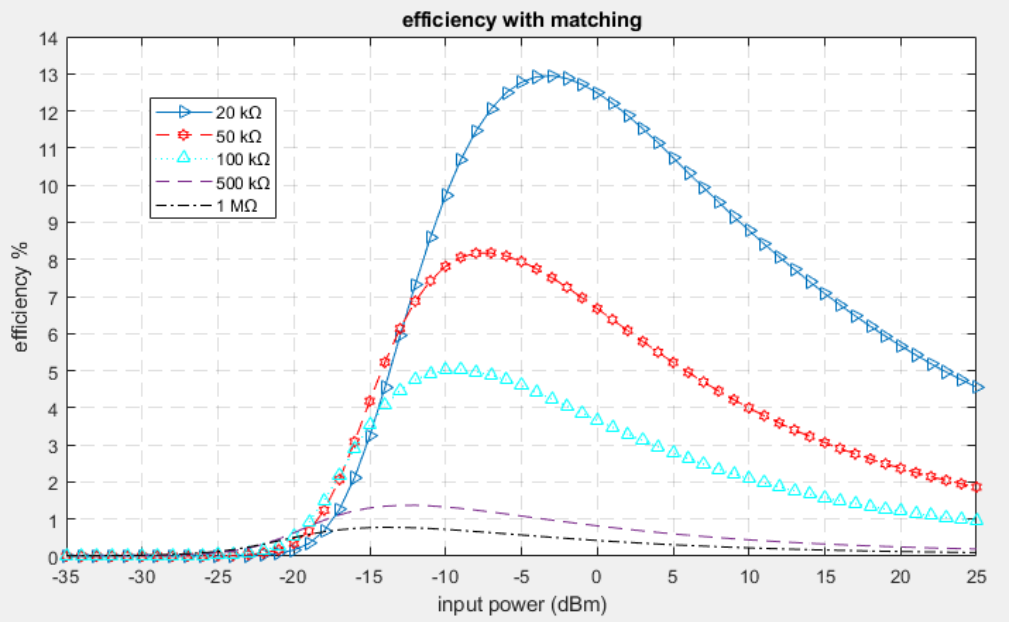


Figure 4.21. Three stages efficiency for different RL with matching for HSMS-2822.

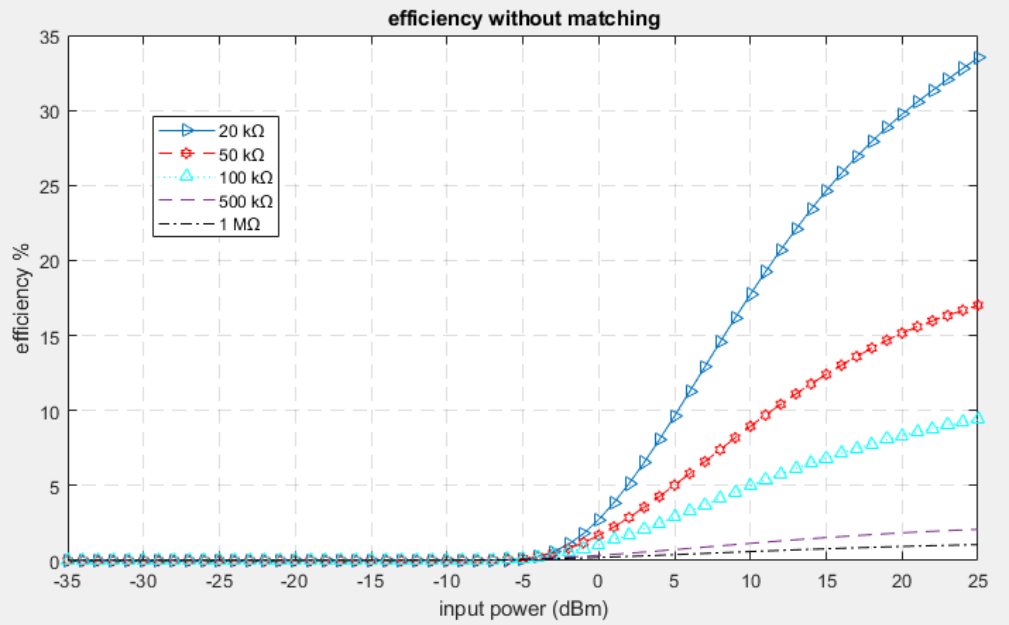


Figure 4.22. Three stage efficiency for different RL without matching for HSMS-2822.

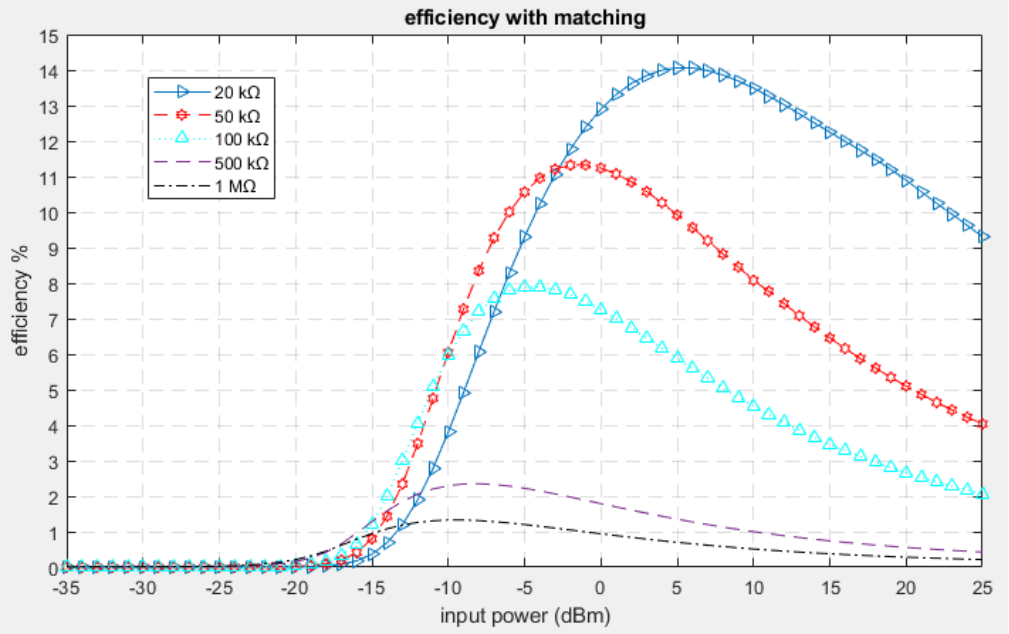


Figure 4.23. Six stage efficiency for different RL with matching for HSMS-2822.

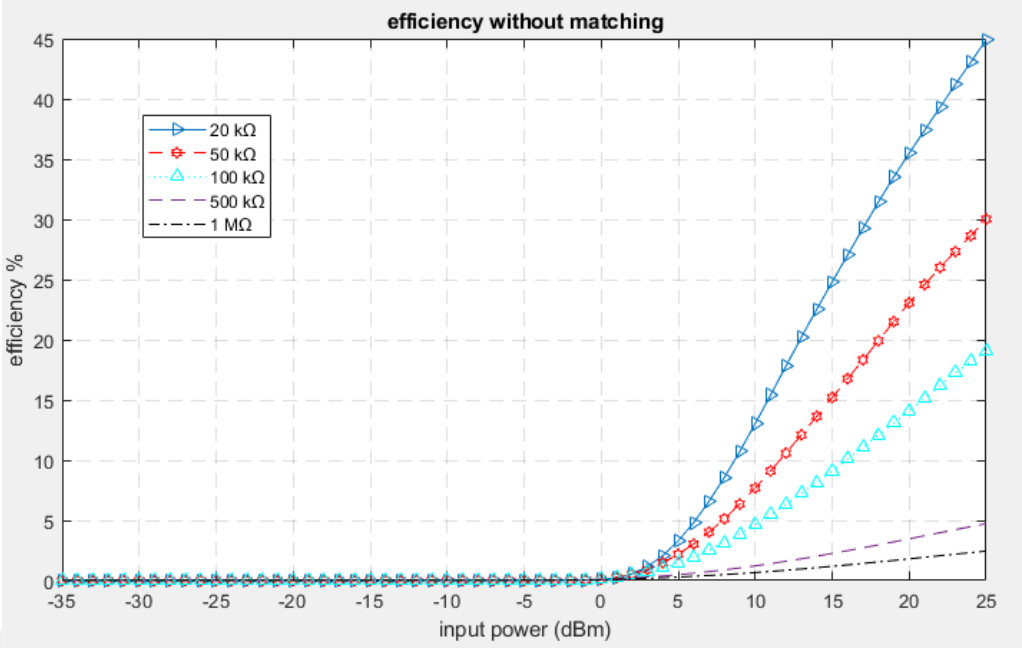


Figure 4.24. Six stage efficiency for different RL without matching for HSMS-2822.

4.2 Stage Number Effect of Dickson Voltage Multiplier.

1) For HSMS-2852 diode model. The DVM stages number investigated in this thesis as can be seen in Figure 4.25 and Figure 4.26 two and six stages DVM with and without matching circuit for 20kΩ load resistance, as given in Figure 4.25 and Figure 4.26, that a two-stage is better than the six-stage in term of efficiency because it achieves approximately 45 % efficiency at -7 dBm input power. In addition, the harvesting circuit with matching is better than the harvesting circuit without matching in low input power, but in high input power the matching circuit doesn't affect to the efficiency (e.g. at 11 dBm input power). For six stage DVM the maximum efficiency approximately 30 % at 0 dBm input power. Besides, the harvesting circuit without matching is better than the harvesting circuit with matching in high input power (e.g. at 0 dBm input power) the harvesting circuit efficiency will increase gradually as can be seen in Figure 4.26 until it reaches maximum efficiency around 60 % at 15 dBm when the harvesting circuit without matching network.

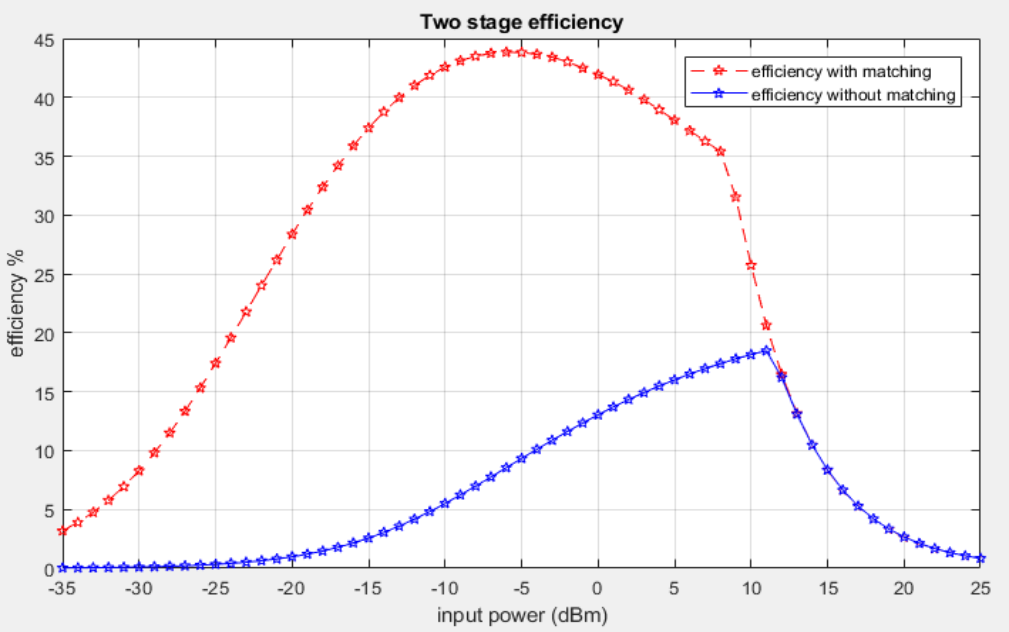


Figure 4.25. Two stages efficiency with and without matching for the 20kΩ load.

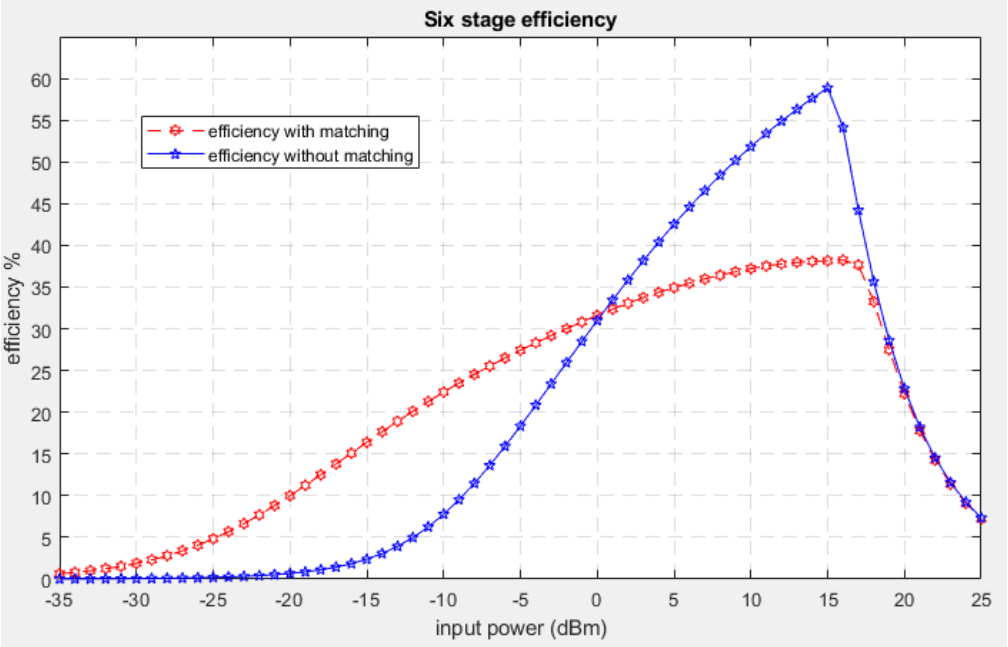


Figure 4.26. Six stages efficiency with and without matching for 20kΩ load

2) For HSMS-2822 diode model. The DVM stage number with using HSMS-2822 diode model is also investigated in this thesis for different stage number (e.g. tow stage, three stages, four stages, five-stage and six stages), we will give a result for two and six stages in order to make the difference clear. For two-stage DVM with 20kΩ load resistance as given in Figure 4.27 the maximum efficiency reaches to 11 % approximately at – 10 dBm input power when the matching circuit applied. However, the harvesting circuit without matching doesn't work at – 10 dBm input power. But, after -10dBm input power point the efficiency of the harvesting circuit with matching network will gradually reduce, while the efficiency of the harvesting circuit without matching network gradually increase until the input power reaches to 4 dBm the harvesting circuit without matching become higher in its efficiency than the harvesting circuit with matching network. For a six stages DVM with matching circuit as given in Figure 4.28 its reaches maximum efficiency around 14% at 0 dBm input power after this point the circuit with matching will decrease gradually and the circuit without matching network will increase gradually until the input power becomes 10 dBm the harvesting circuit without matching will be higher by its efficiency than the harvesting circuit with matching network as illustrated in Figures 4.27 and Figure 4.28.

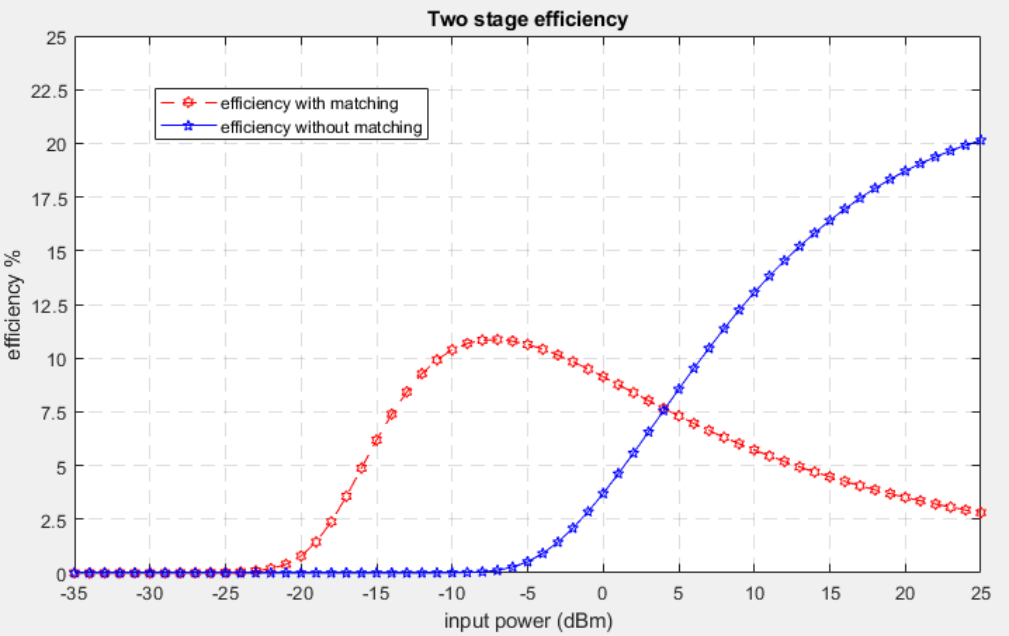


Figure 4.27. Efficiency for two-stage DVM with and without matching for 20kΩ.

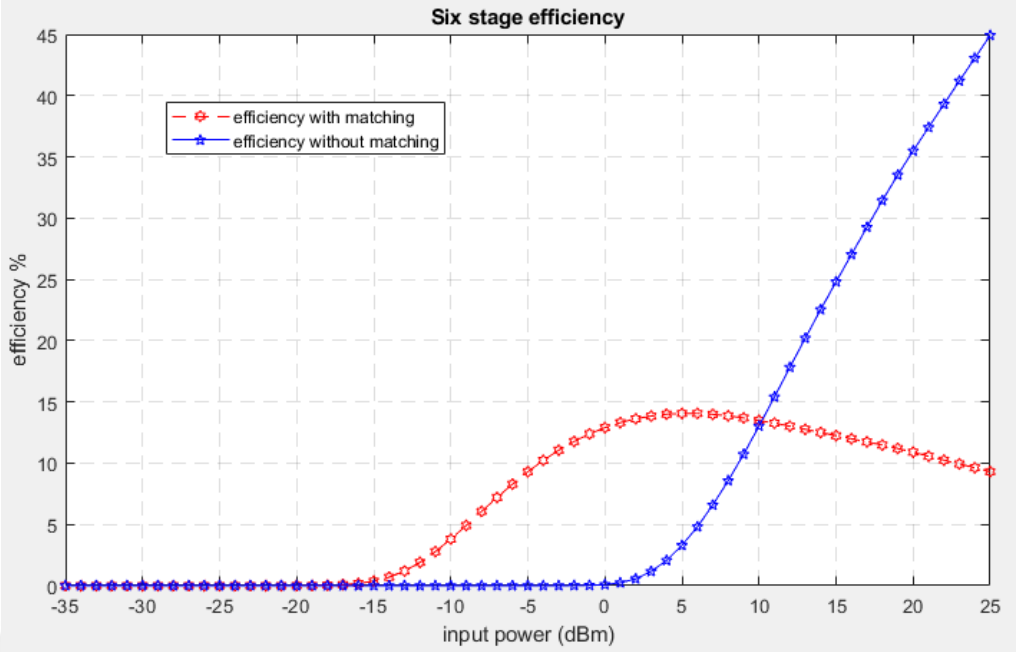
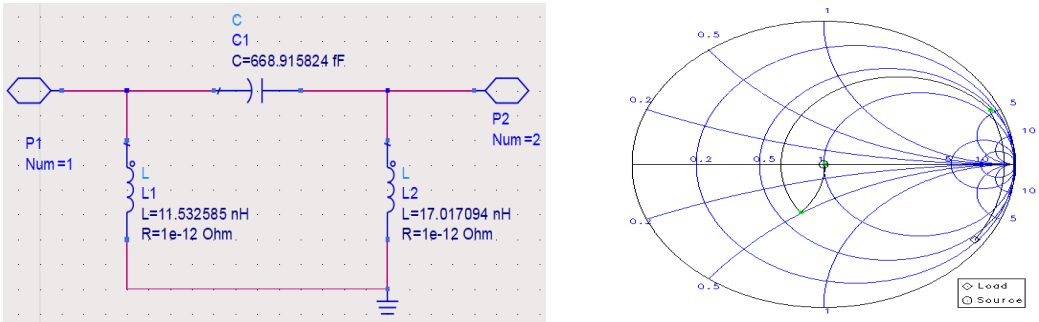


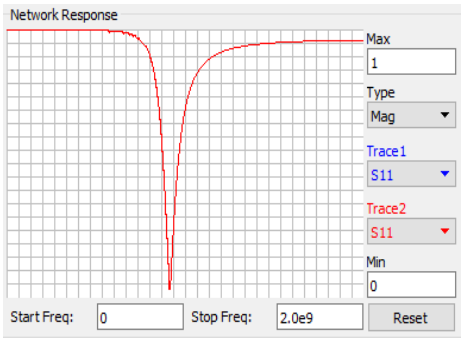
Figure 4.28. Efficiency for six stages DVM with and without matching for 20kΩ.

4.3 Matching Topology Effect

In this study different matching topologies are analyzed (e.g. Pi-matching, T-matching, L-matching) for various stage number of DVM with the 20kΩ load resistance. Firstly, Pi-matching topology applied to the two-stage DVM as shown in Figure 4.29 the Pi-matching schema, Smith chart of the matching circuit and the network response of the Pi-matching topology.



(a) (b)



(c)

Figure 4.29. (a) Pi-matching schema, (b) Smith chart and (c) Matching circuit response.

The simulation result for Pi-matching topology on two-stage DVM with 20kΩ load resistance shows that the maximum efficiency is 40 % at -10 dBm input power as shown in Figure 4.30, besides the matching circuit doesn't affect to the harvesting circuit in high input power.

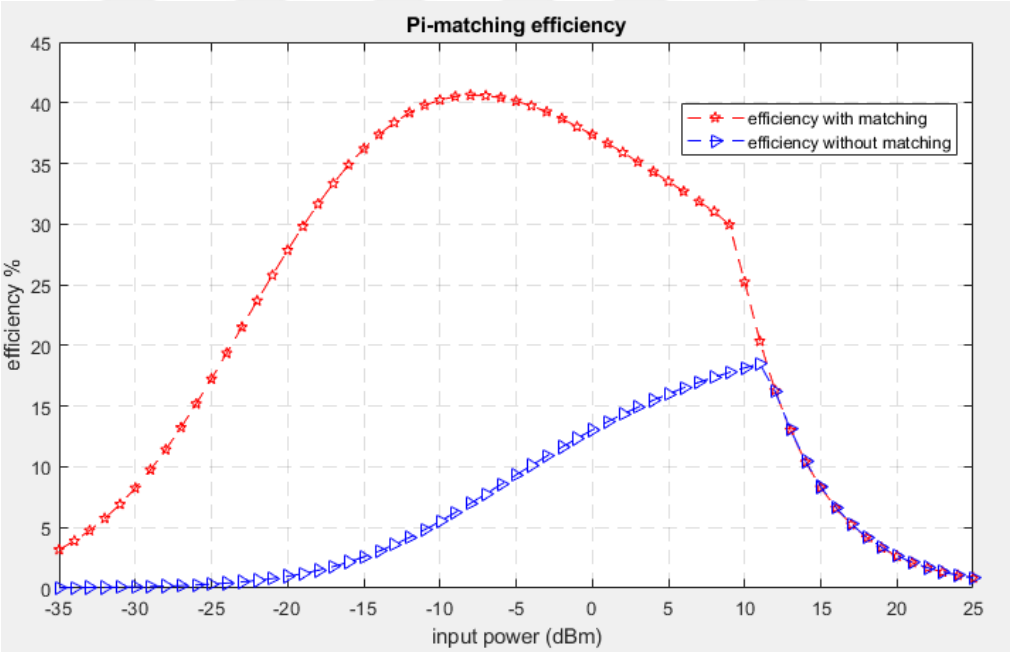
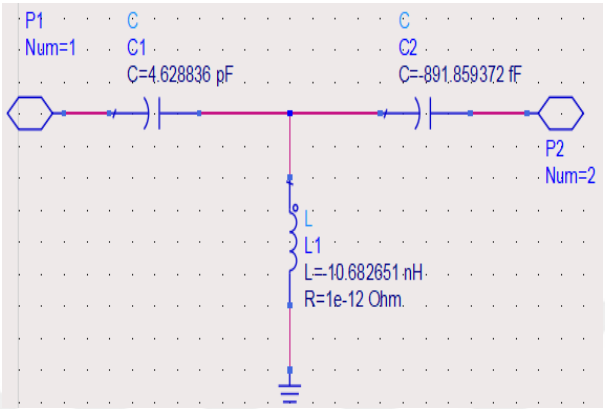
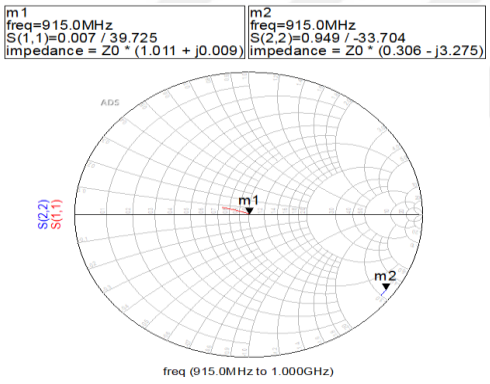


Figure 4.30. Efficiency for two-stage DVM with using Pi-matching topology.

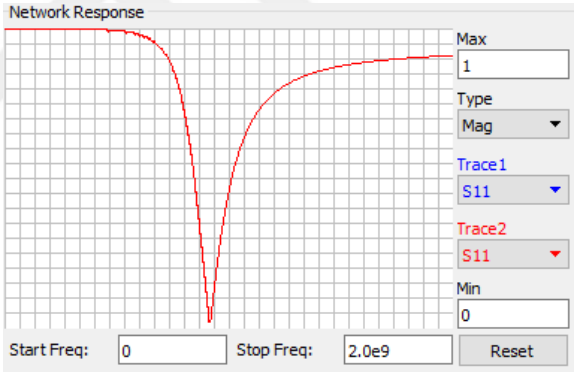
Secondly, T-matching topology applied to the two-stage DVM with 20kΩ load resistance the T-matching network shown in Figure 4.31(a), the Smith chart of the matching network shown in Figure 4.31(b) and the matching network response is shown in Figure 4.31(c).



(a)



(b)



(c)

Figure 4.31. (a) T-matching schema, (b) Smith chart, (c) matching circuit response.

The simulation result for T-matching topology shows that the maximum efficiency of the harvesting circuit approximately 44 % at -10 dBm input power which is better than the efficiency of the harvesting circuit when using a Pi-matching topology. Also, the matching circuit in high input power doesn't affect to the efficiency as given in Figure 4.32.

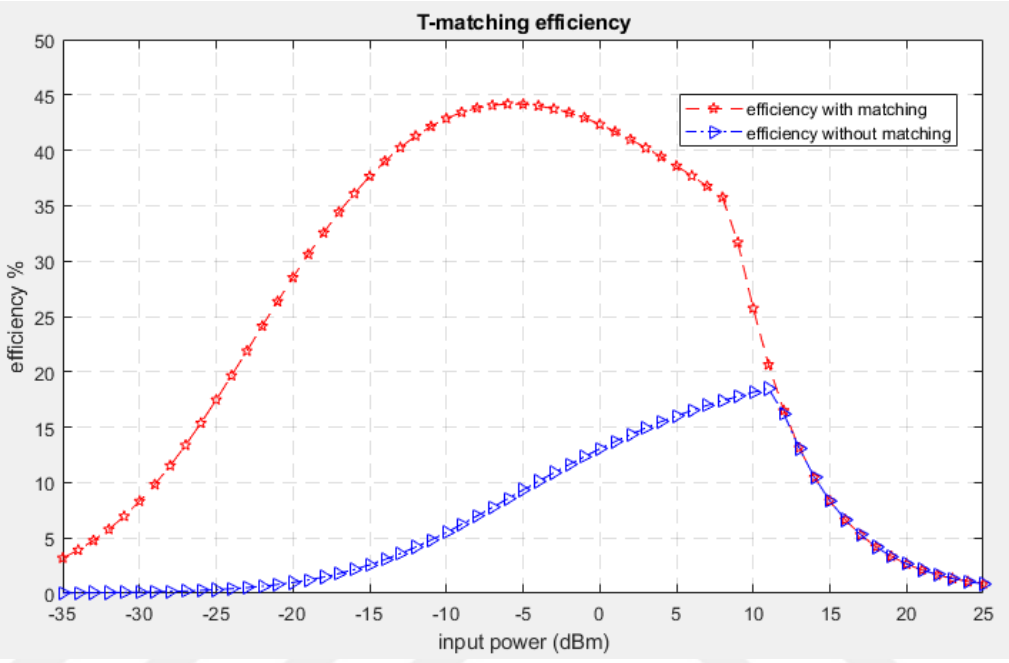
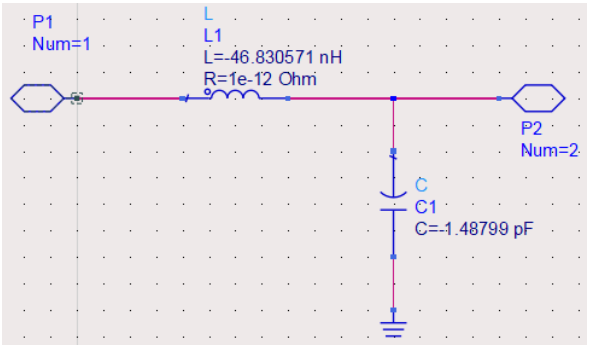
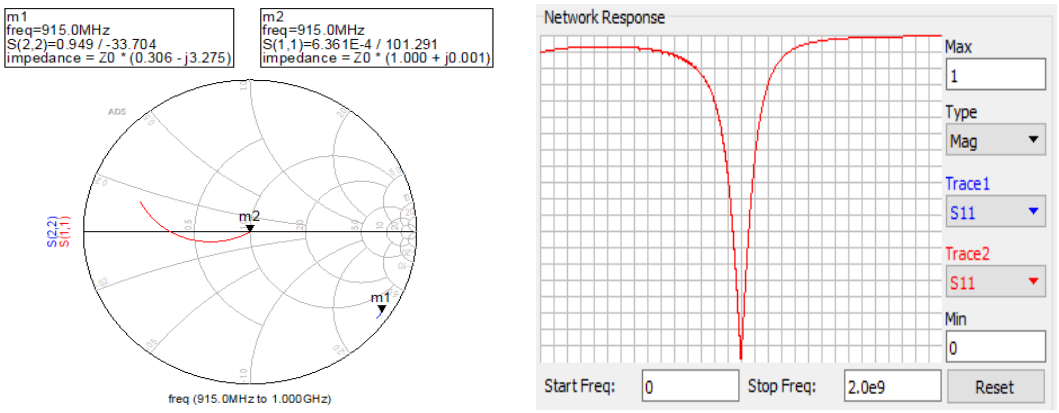


Figure 4.32. Efficiency for two-stage DVM with using T-matching topology.

Thirdly two stage DVM with L-matching topology for 20kΩ load resistance analyzed in this study. The matching circuit is shown in Figure 4.33(a), the Smith chart shown in Figure 4.33(b) and the matching network response shown in Figure 4.33(c).



(a)



(b) (c)

Figure 4.33. (a) L-matching schema, (b) Smith chart, (c) matching Network response

The simulation result for two-stage DVM with L-matching topology for 20kΩ load resistance shows that the maximum efficiency approximately 44 % at -10 dBm input power as illustrated in Figure 4.34, which is same as the efficiency of the T-matching topology. So, the L-matching and T-matching topology are better than the Pi-matching topology. Also, there is no difference in efficiency between the circuit with matching circuit and the circuit without matching in high input power as shown in the Figure 4.34.

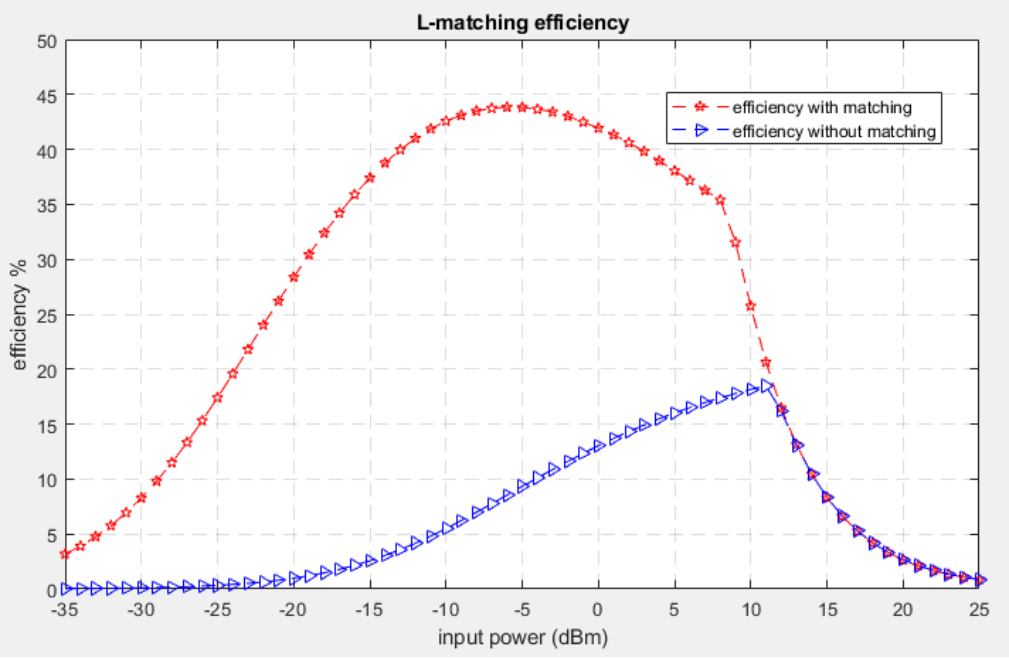
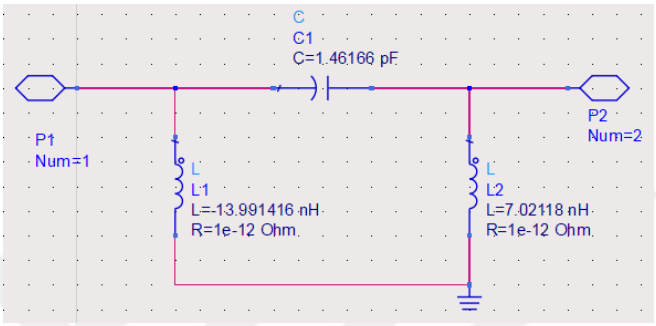
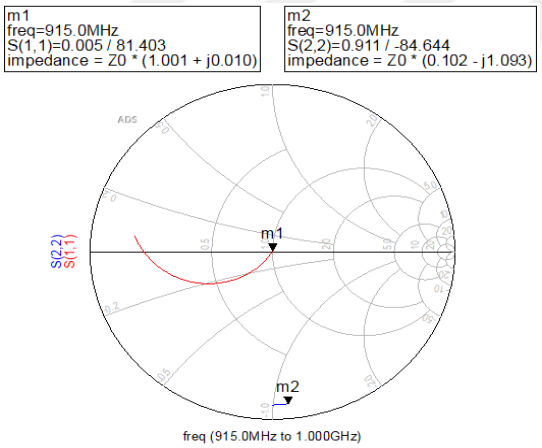


Figure 4.34. Efficiency for two-stage DVM using L-matching topology.

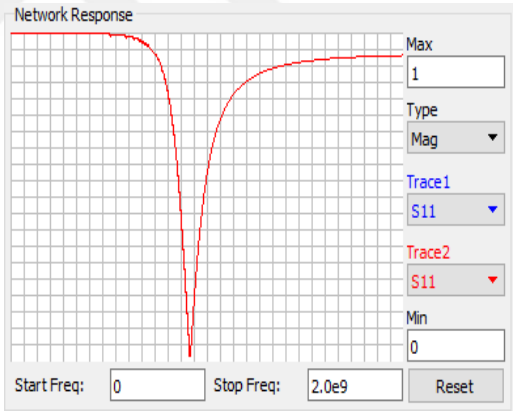
Another approach analyzed in this thesis was the effect of matching topology on a six-stage DVM with the 20kΩ load resistance. Firstly, Pi-matching topology is investigated for a six-stage DVM, the Pi-matching circuit shown in Figure 4.35(a), the matching circuit designed by using the Smith chart utility in ADS, Figure 4.35(b) shows the Smith chart of the Pi-matching circuit, and Figure 4.35(c) illustrate the matching circuit response on a 915 MHz as a central frequency.



(a)



(b)



(c)

Figure 4.35. (a) Pi-matching schema, (b) Smith chart, (c) Matching network response.

The simulation result for a six-stage DVM with Pi-matching topology shows that the maximum efficiency with matching circuit around 32 % at 0 dBm input power, after this point the efficiency of the harvesting circuit without matching increase gradually until the efficiency approximately become 60 % at 15 dBm input power as illustrated in Figure 4.36 however, the harvesting circuit with matching in this point is around 40 %. So, the circuit with matching is better than the circuit without matching in low input power.

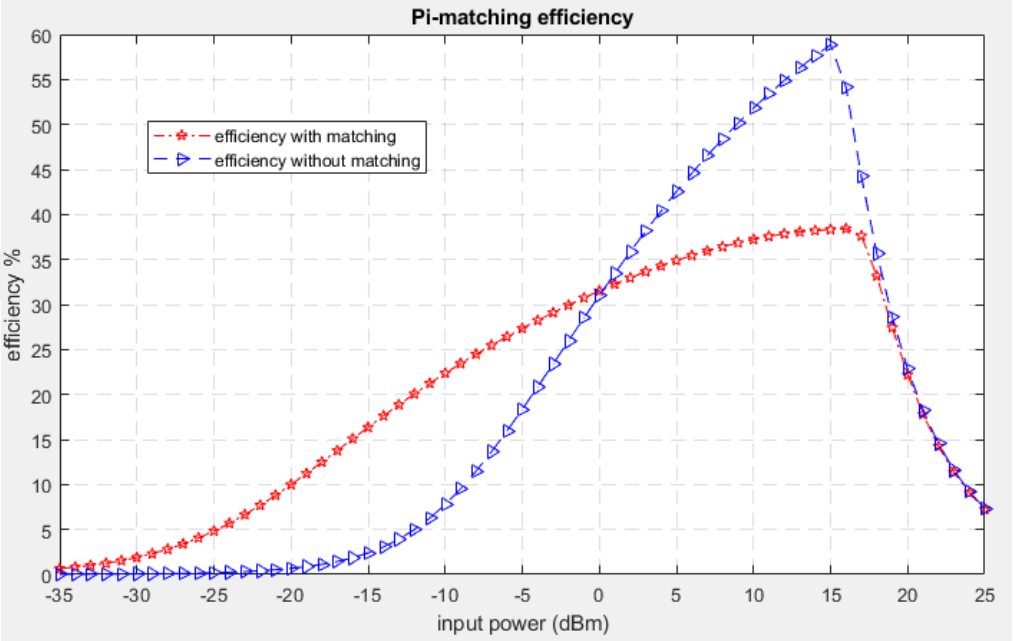
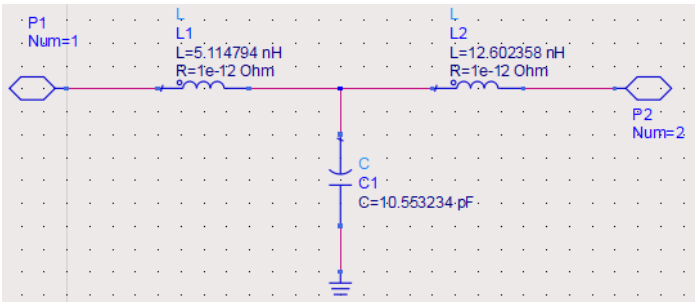
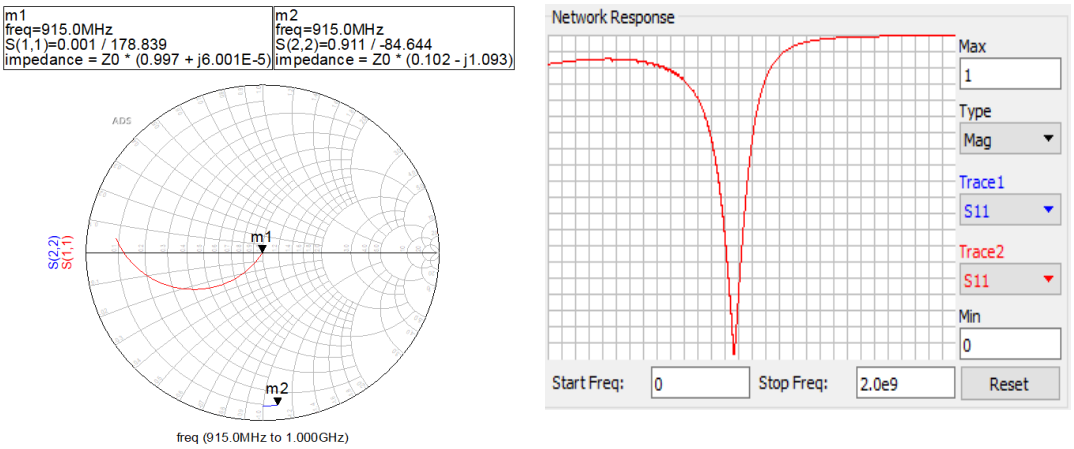


Figure 4.36. Efficiency for six stages DVM with using Pi-matching network.

Secondly, T-matching topology is applied to the six-stage DVM with the 20kΩ load resistance. The T-matching circuit design shown in Figure 4.37(a), the Smith chart of the designed matching circuit shown in Figure 4.37(b) and the matching circuit response shown in Figure 4.37(c).



(a)



(b) (c)

Figure 4.37. (a) T-matching schema, (b) Smith chart, (c) Matching network response.

The simulation result for T-matching topology with a six-stage DVM shows that the maximum efficiency 32 % at 0 dBm input power which is same as the efficiency of the six-stage DVM using Pi-matching topology. After 0 dBm input power the efficiency of the harvesting circuit without matching become higher than the efficiency of the harvesting circuit with matching network and the efficiency without matching gradually increase until it becomes approximately 60 % at 15 dBm input power as illustrated in Figure 4.38, however the efficiency with matching circuit at this value of input power is around 40 %. As a result, there is no different between (Pi and T) matching topology on the efficiency of the harvesting circuit.

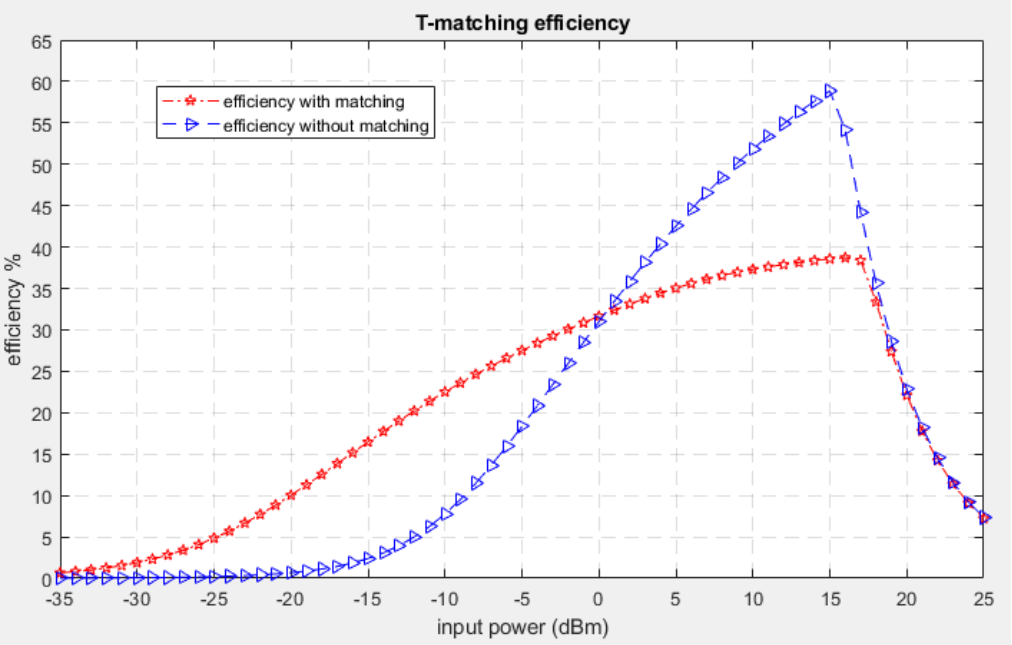
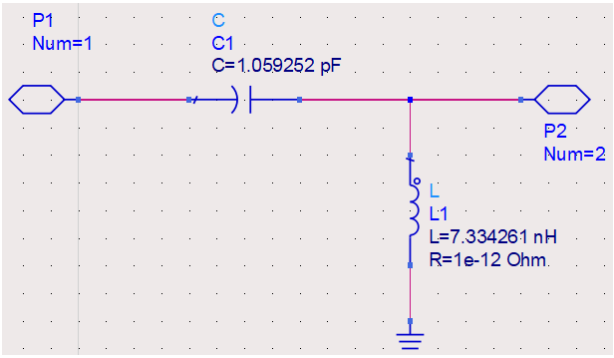
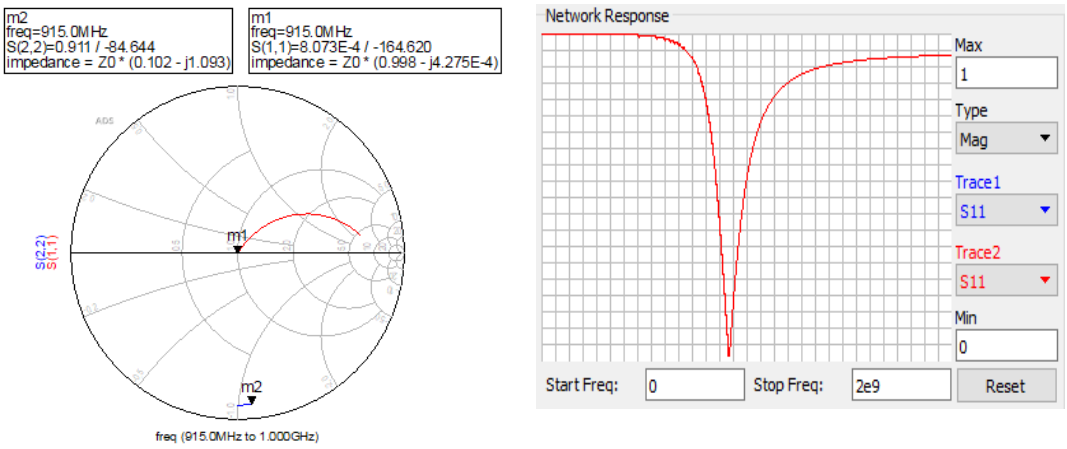


Figure 4.38. Efficiency for six stages DVM using T-matching circuit.

Lastly, L-matching topology applied to the six-stage Dickson Voltage multiplier with the 20kΩ load resistance. The L-matching circuit design shown in Figure 4.39(a), the Smith chart of the L- matching shown in Figure 4.39(b) and the L-matching network response shown in Figure 4.39(c).



(a)



(b) (c)

Figure 4.39. (a) L-matching schema, (b) Smith chart, (c) Matching network response.

The simulation result for L-matching topology for the six-stage Dickson Voltage Multiplier with 20kΩ load resistance shows that the maximum efficiency for low input power is 32 % at 0 dBm input power and also in this point, the efficiency are equal for the circuit with matching and without matching as shown in Figure 4.40. After this point (0 dBm) the efficiency of the circuit without matching will increase gradually until it becomes approximately 60 % at 15 dBm input power at some point the efficiency for the circuit with matching is 38 % dBm as illustrated in the Figure 4.40.

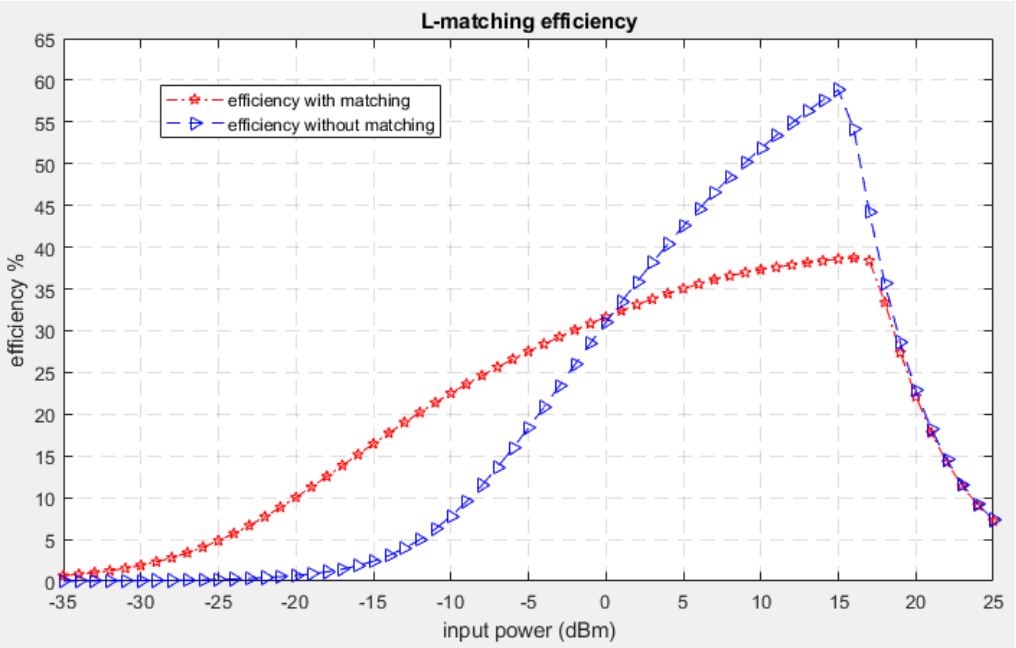


Figure 4.40. Efficiency for six stages DVM using L-matching network.

As a conclusion for the effect of matching topology, (T and L) matching topology is better than the Pi-matching topology when the number of stages is less. But when the number of stages becomes numerous then the circuit efficiency doesn't affected by the matching topology type.

4.4 Quality Factor (Q-factor):

In this thesis, the quality factor of a matching circuit topology investigated for different matching circuit topologies and different stage number of DVM with two different diode model (e.g. HSMS-2852 and HSMS-2822). Firstly, the Q factor result for L-matching network with different stage number (e.g. Two, three, four, five, and six) stages of DVM and different diode model are given in Table 4.1.

Table 4.1. The quality factor for L-matching network.

Number of stages	Q-factor for HSMS-2852	Q-factor for HSMS-2822
Two-stage	5.5	6
Three stage	5.8	5.4
Four stage	4.2	4.4
Five stage	3.8	4.1
Six stage	3.5	4

Secondly, the Q-factor results for Pi-matching network with two and six stage Dickson Voltage Multiplier with two diode model is given in Table 4.2.

Table 4.2. The quality factor for Pi-matching circuit.

Number of stages	Q-factor for HSMS-2852	Q-factor for HSMS-2822
Two-stage	6.3	7
Six stage	4.1	8

Lastly, the Q-factor result for T-matching network with two and six stages Dickson Voltage Multiplier with two diode model is given in Table 4.3.

Table 4.3. The quality factor for T-matching circuit

Number of stages	Q-factor for HSMS-2852	Q-factor for HSMS-2822
Two-stage	2.1	7.4
Six stage	3.5	7.5

There are different Q-factor value for various matching topologies and virous DVM stage number as shown in Table 4.1, Table 4.2 and Table 4.3, the Q-factor value effect to the bandwidth of the matching network response if the Q-factor value is small then the bandwidth of the matching response is broad and if the Q-factor value is high then the bandwidth of the matching network response is thin so, it is useful in some applications and it is not useful in others. For RF harvesting system the broad bandwidth is useful because we want to harvest as much energy in different frequenceies therefore the L-matching topology is better to use. For other applications like radio we want to listen to a specific frequency therefore the bandwidth of the matching network response should be thin inorder to hear the sound clearly and avoid hearing the sound of a second radio frequency near to the frequency that be heard.

5. CONCLUSION

DVM is analyezd and simulated in this thesis. Different design parameters are applied to the simulation. Efficiency and output voltage comparisions are outcomes for these designs. Matching network effect and quality factor of the matching network are also investigated in this thesis for DVM design.

Firstly, fewer voltage multiplier stage is much better in term of efficiency than the higher voltage multiplier stage in low input power. Also, the harvesting circuit with a matching network is better than the harvesting circuit without a matching network in low input power as illustrated in section 4.1. Besides, the higher number of stage and the harvesting circuit without a matching network is better in high input power.

For the output voltage of a harvesting circuit, the result shows that when the number of voltage multiplier stages increase the output voltage will also increase. In addition, the output voltage does not affect the matching circuit as proved in the previous chapter.

With regard to HSMS-2822 diode model is better than the HSMS-2852 in high input power as illustrated in the previous chapter. Furthermore, HSMS-2822 give higher voltage than the HSMS-2852. Besides, the output voltage effected by matching circuit unlike the other diode model which the output voltage is not effected by the matching circuit.

Regards to the result we discover that, when the value of load resistance increases the efficiency of the harvesting circuit decrease and the higher stages number is better than the low stage number when a high load resistance is connected to the circuit.

Matching topology is also analized in this thesis for various stage number, as a conclusion for this comparison. Firstly,when a two stage DVM with 20 kΩ load resistance, the result showed that L-matching and T-matching topology are better than the Pi-matching topology. Also, there is no difference in efficiency between the circuit with matching and the circuit without matching in high input power.

Secondly, when a six stage DVM with 20 kΩ load resistance is applied the result showed that the matching type doesn't effect to the efficiency of the harvesting circuit. Simply, for the effect of matching topology, (T and L) matching topology is better than the Pi-matching topology when the number of stages is less. But when the number of stages becomes numerous then the circuit efficiency doesn't affected by the matching topology type.

REFERENCES

Ababneh, M. M., Perez, S. and Thomas, S., 2017. Optimized power management circuit for RF energy harvesting system, 2017 IEEE 18th Wireless and Microwave Technology Conference, WAMICON 2017.

Abdin, Z., Alim, M. A., Saidur, R., Islam, M. R., Rashmi, W., Mekhilef, S. and Wadi, A. (2013). Solar energy harvesting with the application of nanotechnology. Renewable and Sustainable Energy Reviews.

Adam, I., Fareq, M., Malek, A., Najib, M., Yasin, M. and Rahim, H. A., 2015. Rf energy harvesting with efficient matching technique for low power level application, 10, 18, 8318–8321.

Akter, N., Hossain, B., Kabir, H., Bhuiyan, A. H., Yeasmin, M. and Sultana, S., 2014. Design and performance analysis of 10-stage voltage doublers rf energy harvesting circuit for wireless sensor network. journal of communications engineering and networks, 4, 84–91.

Anika, A., S., Dewanjee, P., 2, S. and Akter, N., 2018. Optimized process Design of RF energy harvesting circuit for low power devices equal contributor, International Journal of Applied Engineering Research (Vol. 13).

Bloessl, B., Segata, M., Sommer, C. and Dressler, F. (2013). An IEEE 802.11a/g/p OFDM receiver for GNU radio.

Boccardi, F., Andrews, J., Elshaer, H., Dohler, M., Parkvall, S., Popovski, P. and Singh, S. (2016). Why to decouple the uplink and downlink in cellular networks and how to do it. IEEE Communications Magazine.

Bouchouicha, D., Dupont, F., Latrach, M. and Ventura, L., 2010. Ambient RF energy harvesting, Renewable Energy and Power Quality Journal, 1, 08, 1309–1313.

Brandl, S. and Dyczij-Edlinger, R., 2018. Parametric model-order reduction for accelerating the gradient-based optimization of microwave structures using finite-elements, IFAC-PapersOnLine, 51, 2, 190–195.

Breed, G. (2008). Improving the bandwidth of simple matching networks. High Frequency Electronics.

Chow, E. Y., Chlebowski, A. L., Chakraborty, S., Chappell, W. J. and Irazoqui, P. P., 2010. Fully wireless implantable cardiovascular pressure monitor integrated with a medical stent, IEEE Transactions on Biomedical Engineering.

Chintalapudi, K. and Radunovic, B. (2012). WiFi-NC: WiFi over narrow channels. Proceedings of the 9th.

Cockcroft, J. D. and Walton, E. T. S., 1932. Experiments with high velocity positive ions, (I) Further Developments in the Method of Obtaining High Velocity Positive Ions, Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences.

Devi, K. K. A., Din, N. M. and Chakrabarty, C. K., 2012. Optimization of the voltage doubler stages in an RF-DC convertor module for energy harvesting, Circuits and Systems, 03, 03, 216–222.

Dickson, J. F., 1976. On-chip high-voltage generation in mnos integrated circuits using an improved voltage multiplier technique, IEEE Journal of Solid-State Circuits.

Felini, C., Merenda, M. and Corte, F. G. D., 2014. Dynamic impedance matching network for RF energy harvesting systems, In 2014 IEEE RFID Technology and Applications Conference, RFID-TA 2014.

Fontes, R. R., Afzal, S., Brito, S. H. B., Santos, M. A. S. and Rothenberg, C. E., 2015. Mininet-WiFi: Emulating software-defined wireless networks, In Proceedings of the 11th International Conference on Network and Service Management, CNSM 2015.

Hameed, Z. and Moez, K., 2017. Design of impedance matching circuits for RF energy harvesting systems, Microelectronics Journal, 62, 4, 49–56.Han, B., Nielsen, R., Papadias, C., and Prasad, R., 2013. Radio frequency energy harvesting for long lifetime wireless sensor networks, Wireless Personal Multimedia Communications (WPMC), 2013 16th International Symposium On, 1–5.

Huurdeman, A. a., 2003. the Worldwide History of, Evolution.

Imran, M. I., Tharek, A. R. and Hasnain, A., 2008. An optimization of beam squinted radial line slot array antenna design at 5.8 GHz, In RF and Microwave Conference, 2008. RFM 2008, IEEE International (pp. 139–142). IEEE.

John Wiley and Sons. 2012. Microwave Engineering (4th ed.), Pozar, David M.

Johnson, J. E. and Branner, G. R., 2004. Harmonic balance analysis of output impedance matching in active RF/microwave frequency multipliers, The 2004 47th Midwest Symposium on Circuits and Systems, 2004. MWSCAS ’04.

Keyrouz, S., Visser, H. and Tijhuis, A., 2013. Multi-band simultaneous radio frequency energy harvesting, Antennas and Propagation.

Khansalee, E., Zhao, Y., Leelarasmee, E. and Nuanyai, K., 2014. A dual-band rectifier for RF energy harvesting systems, In 2014 11th international conference on electrical engineering/electronics, Computer, Telecommunications and Information Technology, ECTI-CON 2014.

Kurniawan, R., Yanti, N. and Ahmad Nazri, M. Z., 2014. Expert systems for self-diagnosing of eye diseases using Naïve Bayes (pp. 113–116), IEEE.

Le, T., Mayaram, K. and Fiez, T., 2008. Efficient far-field radio frequency energy harvesting for passively powered sensor networks, IEEE Journal of Solid-State Circuits, 43, 5, 1287–1302.

Lee, S., Zhang, R. and Huang, K. (2013). Opportunistic wireless energy harvesting in cognitive radio networks. In IEEE Transactions on Wireless Communications.

Lu, X., Wang, P., Niyato, D., Kim, D. I. and Han, Z. (2015). Wireless networks with rf energy harvesting: A contemporary survey. IEEE Communications Surveys and Tutorials.

Mansour, S. Y. (2018). Design of Multi-Band RF Energy Harvesting System Design of Multi-Band RF Energy Harvesting System.

Marshall, B. R., Morys, M. M. and Durgin, G. D., 2015. Parametric analysis and design guidelines of RF-to-DC Dickson charge pumps for RFID energy harvesting, 2015 IEEE International Conference on RFID, RFID 2015, 32–39.

Merz, C. and Kupris, G., 2017. High Q impedance matching for RF energy harvesting applications, 2016 IEEE 3rd International Symposium on Wireless Systems within the IEEE International Conferences on Intelligent Data Acquisition and Advanced Computing Systems, IDAACS-SWS 2016 - Proceedings, 9, 45–50.

Merz, C., Kupris, G. and Niedernhuber, M., 2014. A low power design for radio frequency energy harvesting applications, In 2014 2nd International Symposium on Wireless Systems within the Conferences on Intelligent Data Acquisition and Advanced Computing Systems, IDAACS-SWS 2014.

Mitcheson, P. D., Yeatman, E. M., Rao, G. K., Holmes, A. S. and Green, T. C., 2008. Human and Machine Motion for Wireless Electronic Devices, Proceedings of the IEEE.

Nguyen, T. N., Hoang, T., Minh, Q., Tran, P. T., Voznak, M. and Duy, T. T. (2018). Performance Enhancement for Energy Harvesting Based Two-Way Relay Protocols in Wireless Ad-hoc Networks with Partial and Full Relay Selection Methods. Ad Hoc Networks.

Nintanavongsa, P., Member, S., Muncuk, U. and Lewis, D. R., 2016. Design optimization and implementation for RF energy harvesting circuits, Journal on Emerging and Selected Topics in Circuits and Systems, 2, 2, 24–33.

Neo, W. C. E., Lin, Y., Liu, X. D., De Vreede, L. C. N., Larson, L. E., Spirito. and M., … Nanver, L. K. (2006). Adaptive multi-band multi-mode power amplifier using integrated varactor-based tunable matching networks. In IEEE Journal of Solid-State Circuits.

Olgun, U., Chen, C.-C. and Volakis, J. L. (2012). Design of an efficient ambient WiFi energy harvesting system. IET Microwaves, Antennas & Propagation.

Paradiso, J. A. and Starner, T., 2005. Energy scavenging for mobile and wireless electronics, IEEE Pervasive Computing.

Piñuela, M., Mitcheson, P. D. and Lucyszyn, S., 2013. Ambient RF energy harvesting in urban and semi-urban environments, IEEE Transactions on Microwave Theory and Techniques.

Saberkari, A., Ziabakhsh, S., Martinez, H. and Alarcón, E., 2016. Active inductor-based tunable impedance matching network for RF power amplifier application, Integration, The VLSI Journal, 52, 301–308.

Şengül, M. and Yeşilyurt, G. (2011). Real Frequency Design of Pi and T Matching Networks with Complex Terminations, 1328–1331.

Sogorb, T., Llario, J. V., Pelegrí, J., Lajara, R. and Alberola, J., 2008. Studying the feasibility of energy harvesting from broadcast RF station for WSN, In Conference Record - IEEE Instrumentation and Measurement Technology Conference.

Soltani, N., Yuan, F. and Member, S., 2010. Addis A 1999-01.pdf, 57, 10, 2685–2695.

Sun, Y., and Fidler, J. K., 2002. Design method for impedance matching networks, IEE Proceedings - Circuits, Devices and Systems.

avago technology ., (2017). ADS Tutorial : A Beginners Tutorial System.

Waters, B. H., Sample, A. P. and Smith, J. R., 2012. Adaptive impedance matching for magnetically coupled resonators, Progress In Electromagnetics Research Symposium (PIERS) Proceedings.

Wyndrum, R. W., 2008. Microwave filters, impedance-matching networks, and coupling structures, Proceedings of the IEEE.

Zhao, W., Choi, K., Bauman, S., Dilli, Z., Salter, T. and Peckerar, M., 2012. A radio-frequency energy harvesting scheme for use in low-power ad hoc distributed networks, IEEE Transactions on Circuits and Systems II: Express Briefs.

Zhou, Y., Froppier, B. and Razban, T. (2012). Schottky diode rectifier for power harvesting application. In 2012 IEEE International Conference on RFID-Technologies and Applications, RFID-TA 2012.

URL-1< https://www.rapidtables.com/convert/power/dBm_to_Watt.html>, Date of access: 22.12.2018.

APPENDIX LIST

APPENDIX A: Agilent HSMS-285x Series Surface Mount Zero Bias Schottky Detector Diodes Data Sheet

APPENDIX B: Agilent HSMS-282x Series Surface Mount Zero Bias Schottky Detector Diodes Data Sheet

APPENDIX A

Agilent HSMS-285x Series Surface Mount Zero Bias Schottky Detector Diodes Data Sheet

Agilent HSMS-285x Series Surface Mount Zero Bias Schottky Detector Diodes

Data Sheet

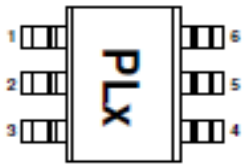
Description

Agilent's HSMS-285x family of zero bias Schottky detector diodes has been designed and optimized for use in small signal (P_{in} <-20 dBm) applications at frequencies below 1.5 GHz. They are ideal for RF/ID and RF Tag applications where primary (DC bias) power is not available.

Important Note: For detector applications with input power levels greater than –20 dBm, use the HSMS-282x series at frequencies below 4.0 GHz, and the HSMS-286x series at frequencies above 4.0 GHz. The HSMS-285x series IS NOT RECOMMENDED for these higher power level applications.

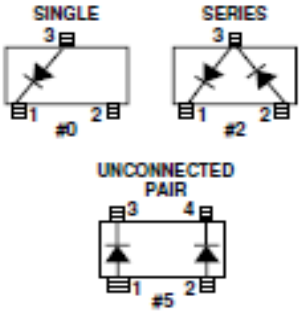
Available in various package configurations, these detector diodes provide low cost solutions to a wide variety of design problems. Agilent's manufacturing techniques assure that when two diodes are mounted into a single package, they are taken from adjacent sites on the wafer, assuring the highest possible degree of match.

Pin Connections and Package Marking

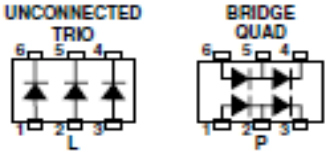


Notes:
1. Package marking provides orientation and identification.
2. See "Electrical Specifications" for appropriate package marking.

SOT-23/SOT-143 Package Lead Code Identification (top view)



SOT-363 Package Lead Code Identification (top view)



SOT-323 Package Lead Code Identification (top view)

Features

- **Surface Mount SOT-23/ SOT-143 Packages**
- **Miniature SOT-323 and SOT-363 Packages**
- **High Detection Sensitivity:** up to 50 mV/µW at 915 MHz
- **Low Flicker Noise:** -162 dBV/Hz at 100 Hz
- **Low FIT (Failure in Time) Rate***
- **Tape and Reel Options Available**
- **Matched Diodes for Consistent Performance**
- **Better Thermal Conductivity for Higher Power Dissipation**
- **Lead-free Option Available**

* For more information see the Surface Mount Schottky Reliability Data Sheet.

Attention:
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)

ESD Human Body Model (Class 0)

Refer to Agilent Application Note A004R: Electrostatic Discharge Damage and Control.

Agilent Technologies

SOT-23/SOT-143 DC Electrical Specifications, T_C = +25°C, Single Diode

Part Number HSMS-	Package Marking Code[1]	Lead Code	Configuration	Maximum Forward Voltage V_F (mV)		Maximum Reverse Leakage, IR (μA)	Typical Capacitance C_T (pF)
2850 2852 2855	P0 P2 P5	0 2 5	Single Series Pair[2,3] Unconnected Pair[2,3]	150	250	175	0.30
Test Conditions				I_F = 0.1 mA	I_F = 1.0 mA	VR=2V	V_R = –0.5 V to –1.0V f = 1 MHz

Notes:
1. Package marking code is in white.
2. ΔV_F for diodes in pairs is 15.0 mV maximum at 1.0 mA.
3. ΔC_T for diodes in pairs is 0.05 pF maximum at –0.5 V.

SOT-323/SOT-363 DC Electrical Specifications, T_C = +25°C, Single Diode

Part Number HSMS-	Package Marking Code[1]	Lead Code	Configuration	Maximum Forward Voltage V_F (mV)		Maximum Reverse Leakage, IR (μA)	Typical Capacitance C_T (pF)
285B 285C 285L 285P	P0 P2 PL PP	B C L P	Single[2] Series Pair[2,3] Unconnected Trio Bridge Quad	150	250	175	0.30
Test Conditions				I_F = 0.1 mA	I_F = 1.0 mA	VR=2V	V_R = 0.5 V to –1.0V f = 1 MHz

Notes:
1. Package marking code is laser marked.
2. ΔV_F for diodes in pairs is 15.0 mV maximum at 1.0 mA.
3. ΔC_T for diodes in pairs is 0.05 pF maximum at –0.5 V.

RF Electrical Specifications, T_C = +25°C, Single Diode

Part Number HSMS-	Typical Tangential Sensitivity TSS (dBm) @ f = 915 MHz	Typical Voltage Sensitivity γ (mV/μW) @ f = 915 MHz	Typical Video Resistance RV (KΩ)
2850 2852 2855 285B 285C 285L 285P	–57	40	8.0
Test Conditions	Video Bandwidth = 2 MHz Zero Bias	Power in = –40 dBm R_L = 100 KΩ, Zero Bias	Zero Bias

Absolute Maximum Ratings, T_C = +25°C, Single Diode

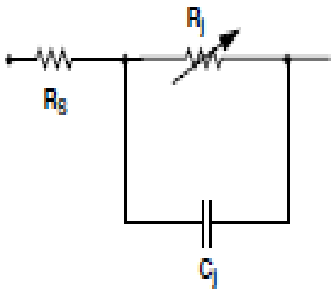
Symbol	Parameter	Unit	Absolute Maximum[1]	
			SOT-23/143	SOT-323/363
P_{IV}	Peak Inverse Voltage	V	2.0	2.0
T_J	Junction Temperature	°C	150	150
T_{STG}	Storage Temperature	°C	-65 to 150	-65 to 150
T_{OP}	Operating Temperature	°C	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	500	150

ESD WARNING:
Handling Precautions Should Be Taken To Avoid Static Discharge.

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Equivalent Linear Circuit Model

HSMS-285x chip



R_S = series resistance (see Table of SPICE parameters)

C_j = junction capacitance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5}\, nT}{I_b + I_s}$$

where

I_b = externally applied bias current in amps

I_s = saturation current (see table of SPICE parameters)

T = temperature, °K

n = ideality factor (see table of SPICE parameters)

Note:
To effectively model the packaged HSMS-285x product, please refer to Application Note AN1124.

SPICE Parameters

Parameter	Units	HSMS-285x
B_V	V	3.8
C_{J0}	pF	0.18
E_G	eV	0.69
I_{BV}	A	3 E-4
I_S	A	3 E-6
N		1.06
R_S	Ω	25
P_B (V_J)	V	0.35
P_T (XTI)		2
M		0.5

APPENDIX B

Agilent HSMS-282x Series Surface Mount Zero Bias Schottky Detector Diodes Data Sheet

HSMS-282x

Surface Mount RF Schottky Barrier Diodes

AVAGO TECHNOLOGIES

Data Sheet

Description/Applications

These Schottky diodes are specifically designed for both analog and digital applications. This series offers a wide range of specifications and package configurations to give the designer wide flexibility. Typical applications of these Schottky diodes are mixing, detecting, switching, sampling, clamping, and wave shaping. The HSMS-282x series of diodes is the best all-around choice for most applications, featuring low series resistance, low forward voltage at all current levels and good RF characteristics.

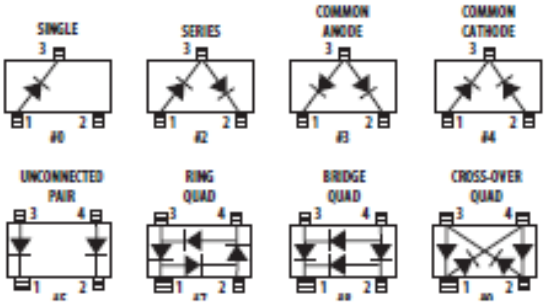
Note that Avago's manufacturing techniques assure that dice found in pairs and quads are taken from adjacent sites on the wafer, assuring the highest degree of match.

Features

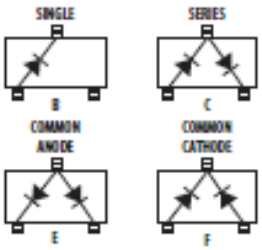
- Low Turn-On Voltage (As Low as 0.34 V at 1 mA)
- Low FIT (Failure in Time) Rate*
- Six-sigma Quality Level
- Single, Dual and Quad Versions
- Unique Configurations In Surface Mount SOT-363 Package
  - increase flexibility
  - save board space
  - reduce cost
- HSMS-282K Grounded Center Leads Provide up to 10 dB Higher Isolation
- Matched Diodes for Consistent Performance
- Better Thermal Conductivity for Higher Power Dissipation
- Lead-free Option Available

* For more information see the Surface Mount Schottky Reliability Data Sheet.

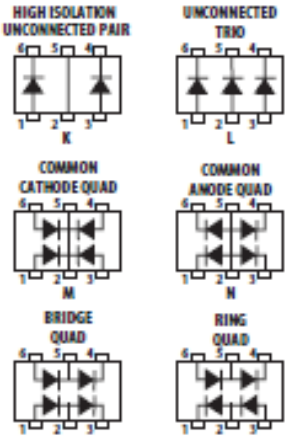
Package Lead Code Identification, SOT-23/SOT-143 (Top View)



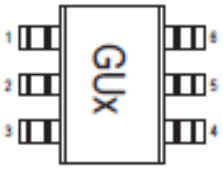
Package Lead Code Identification, SOT-323 (Top View)



Package Lead Code Identification, SOT-363 (Top View)



Pin Connections and Package Marking



Notes:
1. Package marking provides orientation and identification.
2. See "Electrical Specifications" for appropriate package marking.

Absolute Maximum Ratings[1] $T_C = 25°C$

Symbol	Parameter	Unit	SOT-23/SOT-143	SOT-323/SOT-363
I_F	Forward Current (1 µs Pulse)	Amp	1	1
P_{IV}	Peak Inverse Voltage	V	15	15
T_J	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. $T_C = +25°C$, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications $T_C = 25°C$, Single Diode[3]

Part Number HSMS[4]	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	Maximum Forward Voltage V_F (V) @ I_F (mA)	Maximum Reverse Leakage I_R (nA) @ V_R (V)	Maximum Capacitance C_T (pF)	Typical Dynamic Resistance R_D (Ω)[4]
2820	C0	0	Single	15	340	0.5 10	100 1	1.0	12
2822	C2	2	Series						
2823	C3	3	Common Anode						
2824	C4	4	Common Cathode						
2825	C5	5	Unconnected Pair						
2827	C7	7	Ring Quad[5]						
2828	C8	8	Bridge Quad[5]						
2829	C9	9	Cross-over Quad						
282B	C0	B	Single						
282C	C2	C	Series						
282E	C3	E	Common Anode						
282F	C4	F	Common Cathode						
282K	CK	K	High Isolation Unconnected Pair						
282L	CL	L	Unconnected Trio						
282M	HH	M	Common Cathode Quad						
282N	NN	N	Common Anode Quad						
282P	CP	P	Bridge Quad						
282R	OO	R	Ring Quad						
Test Conditions				$I_R = 100$ mA	$I_F = 1$ mA[1]			$V_R = 0V$[5] $f = 1$ MHz	$I_F = 5$ mA

Notes:
1. ΔV_F for diodes in pairs and quads in 15 mV maximum at 1 mA.
2. ΔC_{TO} for diodes in pairs and quads is 0.2 pF maximum.
3. Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 5 mA.
4. See section titled "Quad Capacitance."
5. $R_D = R_S + 5.2Ω$ at 25°C and $I_F = 5$ mA.

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches from the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. Avago defines this measurement as "CM", and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capaci-tances can then be calculated by the formulas given below.

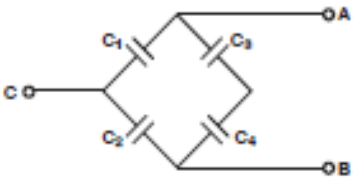
In a quad, the diagonal capacitance is the capacitance between points A and B as shown in the figure below. The diagonal capacitance is calculated using the following formula

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$

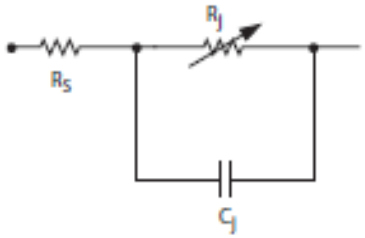
The equivalent adjacent capacitance is the capacitance between points A and C in the figure below. This capacitance is calculated using the following formula

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

This information does not apply to cross-over quad diodes.



Linear Equivalent Circuit Model Diode Chip



R_S = series resistance (see Table of SPICE parameters)

C_J = Junction capacitance (see Table of SPICE parameters)

$$R_J = \frac{8.33 \times 10^{-5}\, nT}{I_b + I_s}$$

where

I_b = externally applied bias current in amps

I_s = saturation current (see table of SPICE parameters)

T = temperature, K

n = ideality factor (see table of SPICE parameters)

Note:
To effectively model the packaged HSMS-282x product, please refer to Application Note AN1124.

ESD WARNING: Handling Precautions Should Be Taken To Avoid Static Discharge.

SPICE Parameters

Parameter	Units	HSMS-282x
B_V	V	15
C_{JO}	pF	0.7
E_G	eV	0.69
I_{BV}	A	1E-4
I_S	A	2.2E-8
N		1.08
R_S	Ω	6.0
P_B	V	0.65
P_T		2
M		0.5

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Analysis of dickson voltage multiplier for RF energy harvesting, Aksaray University, Faculty of Engineering, Electrical and Electronics Engineering Department, Aksaray, TURKEY, ISSRD – International Conference on Communication, Electronics and Electrical Engineering (**ICCEEE**).