HIGH-POWER AND LOW-LOSS SPDT SWITCH DESIGN USING GATE-OPTIMIZED GAN ON SIC HEMTS FOR *S*-BAND 5G T/R MODULES

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Volkan Ertürk

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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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M.S. in Electrical and Electronics Engineering
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Radio frequency (RF) switches are one the fundamental components of modern communication systems. They enable the routing of high-frequency signals into different transmission paths. Therefore, they play a crucial role in transceiver (T/R) modules. Especially, 5G technology creates a demand for compact switches with high power handling, high isolation, and low insertion loss.

GaN on SiC high electron mobility transistor (HEMT) technology stands out with its exceptional electrical and thermal characteristics among other semiconductor technologies. However, switch performance is limited by selected topology and transistor capability. Notably, the T-gate dimensions of the HEMTs directly affect the small-signal and large-signal performance of the switch.

This study focuses on designing a single-pole double-throw (SPDT) monolithic microwave integrated circuit (MMIC) switch using gate-optimized HEMT in AlGaN/GaN on SiC technology. The foot length of the gate is varied from 200 nm to 250 nm, and the head length is varied from 500 nm to 750 nm in the T-gate structure to optimize the RF performance. An asymmetric SPDT switch using transistors with 500 nm head length and 250 nm foot length is designed to demonstrate transistor performance. The switch achieved an insertion loss of better than 0.85 dB throughout the 3.2–3.8 GHz bandwidth. The low-noise path can handle 25 W power level, while the high-power path can withstand up to 50 W of RF power at 1 dB compression level. The isolation performance is about 25 dB, while the return loss of the switch is better than 12 dB. The switch occupies a chip area of 2 x 2.2 mm^2.

Keywords: GaN, HEMT, SPDT, MMIC, high-power, 5G, switch.

ÖZET

S-BANT 5G T/R MODÜLLERİ İÇİN YÜKSEK GÜÇLÜ VE DÜŞÜK KAYIPLI SPDT ANAHTARININ SIC ÜZERİNE GAN KULLANARAK TASARIMI

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Radyo frekansı (RF) anahtarları, modern iletişim sistemlerinin temel elemanlarından biridir. Yüksek frekanslı sinyallerin farklı yollara yönlendirilmesini sağlarlar. Bu nedenle alıcı-verici (T/R) modüllerinde çok önemli bir rol oynarlar. Özellikle 5G teknolojisi, daha yüksek güç kapasitensine, daha düşük araya girme kaybına ve daha yüksek izolasyona sahip kompakt anahtarlar için bir talep yaratır.

SiC tabanlı GaN yüksek elektron hareketlilikli transistör (HEMT) teknolojisi, olağanüstü elektriksel ve termal özellikleri ile öne çıkıyor. Ancak, anahtar performansı topoloji seçimi ve transistör kapasitesi ile sınırlıdır. Özellikle, HEMT'lerin T kapısı boyutları, anahtarın küçük sinyal ve büyük sinyal performansını doğrudan etkiler.

Bu çalışma, SiC teknolojisi üzerinde AlGaN/GaN kullanan kapı geometrisi optimizasyonlu HEMT kullanan tek kutuplu çift atışlı (SPDT) monolitik mikrodalga entegre devre (MMIC) anahtarı tasarlamaya odaklanmaktadır. Kapının ayak uzunluğu 200 nm ile 250 nm arasında, kafa uzunluğu ise 500 nm ile 750 nm arasında RF performansını optimize etmek için T şeklinde kapı yapısında incelenmiştir. 500 nm kafa uzunluğuna ve 250 nm ayak uzunluğuna sahip transistörleri kullanan asimetrik bir SPDT anahtarı, transistör performansını göstermek için tasarlanmıştır. Anahtar, 3.2 – 3.8 GHz bant genişliği boyunca 0.85 dB'den daha iyi bir ekleme kaybı performansı gösterdi. Düşük gürültülü yol 25W güç seviyesine dayanabilirken yüksek güç yolu 1 dB bastırma seviyesinde 50W RF gücüne dayanabilir. İzolasyon performansı yaklaşık 25 dB'dir, anahtarın dönüş kaybı ise 12 dB'den iyidir. Anahtar, 2 x 2,2 mm^2'lık bir yonga alanı kaplar.

Anahtar sözcükler: GaN, HEMT, SPDT, MMIC, yüksek-güç, 5G, anahtar.

To my Family,

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Chapter 1

Introduction

Mobile communication systems are evolving rapidly in the light of technological developments and human needs. In the early 1980s, the 1^{st} generation (1G) mobile wireless communication network was introduced with a limited capability and poor performance. Each generation advanced mobile communication for higher efficiency, lower latency, higher speed, and higher data rates with their standards, features, and challenges. Today, incoming 5^{th} generation (5G) networks with multiple-input multiple-output systems (MIMO) are being deployed for high frequency and large bandwidth operations. These systems generally use the orthogonal frequency division multiplexing (OFDM) techniques due to their high capacity, immunity against multipath fading, and ease of implementation. However, the OFDM modulation scheme requires signal waveforms with a high peak to average power ratio (PAPR) [1].

In a 5G transmit/receive (T/R) system, high-performing radio frequency (RF) switches with low insertion loss and high power handling capacity are required to handle high PAPR signals. Fig. 1.1 shows an illustration of a typical MIMO T/R block. High-power RF switches are critical components for mobile communication systems as well as satellites and radars systems.

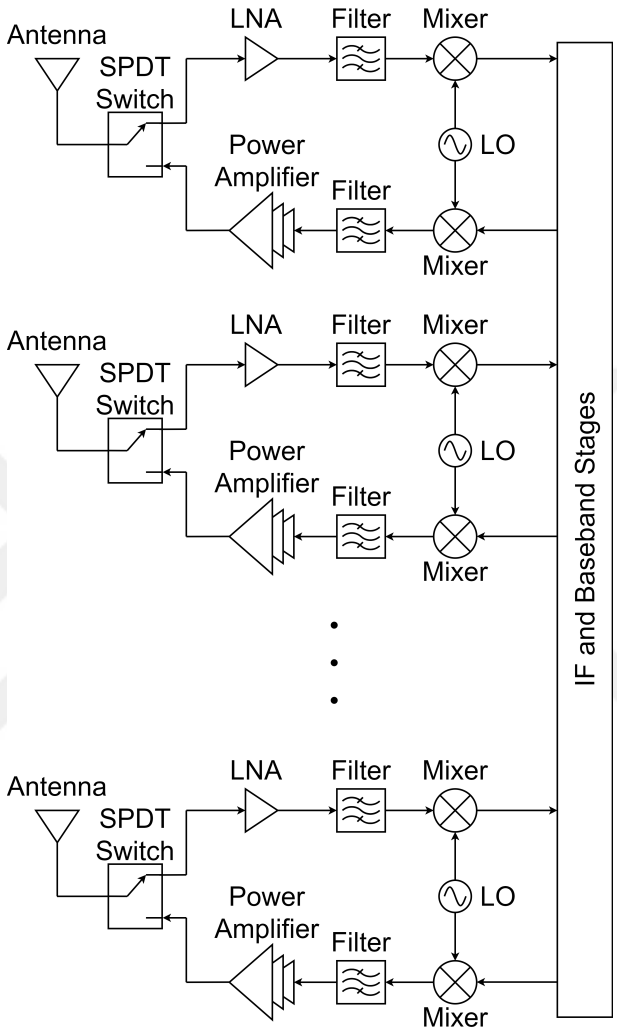


Figure 1.1: Typical MIMO transceiver block diagram.

Currently, several technological solutions are used for high-performance switches. Micro-electromechanical system (MEMS) technology can provide exceptional RF performance in terms of insertion loss, isolation, and power handling capacity [2] while it suffers from slower switching speed and incompatibility with the monolithic microwave integrated circuit (MMIC) process. Likewise, PIN diode switches are capable of handling high power levels with a disadvantage on DC power consumption [3]. High electron mobility transistors (HEMT), on the other hand, have several advantages in terms of low power consumption, high RF performance, ease of integration in MMIC, and low cost over PIN diode

and MEMS technologies. Gallium nitride (GaN) on silicon carbide (SiC) based HEMTs are especially preferred in high-power applications because of their extreme electrical and thermal characteristics.

1.1 GaN HEMT Technology

The global wide bandgap semiconductor market is growing steadily due to the performance limit of Si on existing and emerging technologies. Notably, demand for high-power transistors which able to operate at high frequencies increases. Due to their wide bandgaps, the ability to operate at high voltage levels makes them advantageous. For high-frequency RF applications, saturation velocity and carrier mobility are also important parameters. High power applications require high thermal conductivity to remove heat from hot regions and prevent thermal performance degradation. When those needs come into the picture, there are common semiconductor technologies available in the market, as their physical properties are shown in Table 1.1.

Table 1.1: Physical properties of Si, GaAs, SiC, GaN, and diamond [4, 5].

Materials	**Si**	**GaAs**	**4H-SiC**	**GaN**	**Diamond**
Bandgap, E_g (eV)	1.12	1.42	3.26	3.44	5.5
Relative Dielectric Constant, ϵ	11.7	13.1	10	9	5.7
Electron Mobility, μ_n (cm^2/V.s)	1350	8500	1000	1250	2000
Breakdown Field, E_c (MV/cm)	0.3	0.4	2.0	3.3	13.0
Saturation Velocity, v_{sat} (10^7cm/s)	1	2	2	2.5	2.7
Thermal conductivity, λ (W/m.K)	145	50	490	250	2290
JFOM ($(E_c v_{sat}/2\pi)^2$)	1	7.1	180	760	2540
BFOM ($\epsilon \mu_n {E_c}^3$)	1	15.6	130	650	4410

The comparison table shows that GaN stands out with its high breakdown electric field and saturation velocity. In addition, GaN HEMT devices have exceptionally high-density two-dimensional electron gas (2DEG) due to strong spontaneous and piezoelectric polarization [6]. GaN HEMTs are exceptional candidates for high-power and high-frequency applications. The performance of the semiconductor materials is characterized by the figure of merits (FOMs). One of the widely used FOMs, Johnson's FOM (JFOM), indicates the performance in terms of breakdown electric field and saturation velocity. GaN shows 760 times better performance in terms of JFOM compared to Si. Likewise, Baliga's FOM (BFOM) correlates semiconductor performance with electron mobility, breakdown electric field, and relative dielectric constant, highlighting GaN technology's performance. Although diamond promises the highest performance on the table, its relative cost and immature process make it commercially unavailable for most applications.

The high performance of GaN HEMT compared to other available technologies makes it the top choice for RF and microwave applications. Its high electron density can be engineered through the manipulation of polarization and can reach above 10^{13} cm^{-2} [7]. The electron mobility of 2000 cm^2/V can also be achieved in the 2DEG. Therefore, GaN HEMT technology has low on-resistance transistors and is suitable for high-frequency applications.

With the mentioned physical properties, GaN on SiC HEMT technology is widely preferred in RF switches [8]. High-power RF switches with low insertion loss are studied for higher performances. In the past, several studies on switch topology have been reported with enhanced RF performances [9–11]. However, circuit topology performance is limited by transistor performance. In this study, the performance of switch HEMTs is investigated in different gate topologies. The foot length of the gate is varied from 200 nm to 250 nm, and the head length is varied from 500 nm to 750 nm. By using the gate-optimized transistors, the SPDT switch is designed, fabricated, and characterized with NANOTAM's AlGaN/GaN HEMT on SiC process.

1.2 Organization of Thesis

This thesis investigates the effect of GaN on SiC HEMT gate structure on RF performance. It starts from the fabrication process and includes gate-optimization, SPDT switch MMIC design, and characterization of devices. All transistors are fabricated, and SPDT designs are achieved using HEMT measurements.

Chapter 2 presents the GaN HEMT MMIC fabrication process and its fundamental steps. The whole process is explained, from MOCVD growth to the back-side process.

Chapter 3 presents the fundamentals of RF switches, and their performance figures are discussed.

Chapter 4 introduces the switch performance improvement method and explains the optimization of transistor performance parameters in different gate structures.

Chapter 5 presents the SPDT switch design method and analyses the performance of fabricated switch MMIC using gate-optimized HEMTs.

Chapter 6 summarizes the finding of this study and outlines future work.

Chapter 2

GaN HEMT MMIC Fabrication Process

In this chapter, the fabrication process of 0.25 µm AlGaN/GaN on SiC HEMTs and MMICs will be discussed. Fundamental steps for GaN HEMT and MMIC fabrication like the epitaxial growth, mask design, the front-side, and the backs-side process are explained in detail. Fabrication steps are done at Bilkent University Nanotechnology Research Center (NANOTAM).

2.1 Epitaxial Growth

The first step of AlGaN/GaN HEMT fabrication process is growing an epitaxial wafer on SiC substrate using a metal-organic chemical vapor deposition (MOCVD) system. Initially, a substrate is needed to start the growth process. Although there are several options in the market, the SiC substrate provides several advantages compared to other available alternatives. Si and sapphire show poor thermal conductivity with high lattice mismatch while relatively cheap. Bulk GaN substrate provides better thermal performance without any lattice mismatch; however, it is not available in large wafers and costs more. Diamond show

excellent thermal characteristics at a high price. On the other hand, SiC provides good thermal conductivity and relatively low lattice mismatch as a cheaper option making it suitable for high-power power amplifier and switch MMICs. Table 2.1 shows a comparison table of typical GaN-epitaxy substrate materials. In this thesis, all GaN/AlGaN MMICs are grown on SiC substrates.

Table 2.1: Comparison table of typical GaN-epitaxy substrate materials [12–18].

Substrate	**k (W/(m.K))**	**Lattice Mismatch**	**Available Wafer Size**	**Cost (€/cm^2)**
GaN	130-210	-	2/3-inch	100
Si	150	-16.8%	any	0.1
SiC-4H	380	3.53%	4/6-inch	10
SiC-6H	450	3.49%	4-6-inch	10
Diamond	1800-2200	11.8%	up to 5.7-inch	1000+
Sapphire	25	-16%	up to 8-inch	1

On top of the SiC substrate, layers are formed by mixing trimethylgallium (TMG), trimethylaluminum (TMA), ammonia (NH_3), and decomposing the mixture [19] at temperatures around 1000 C°. Thin layers of GaN materials are deposited using the MOCVD technique, where layers' thickness, composition, and structure can be optimized depending on the application of interest.

The epitaxial structure grown using the MOCVD process is shown in Fig. 2.1. Epitaxial growth starts by depositing a thin AlN nucleation layer on the SiC substrate. After that, high GaN buffer layers, GaN channel layer, AlN spike layer, AlGaN barrier, and GaN cap layer are deposited over the AlN nucleation

layer, respectively. Each layer serves a specific purpose for producing high-quality GaN HEMTs, which are discussed briefly.

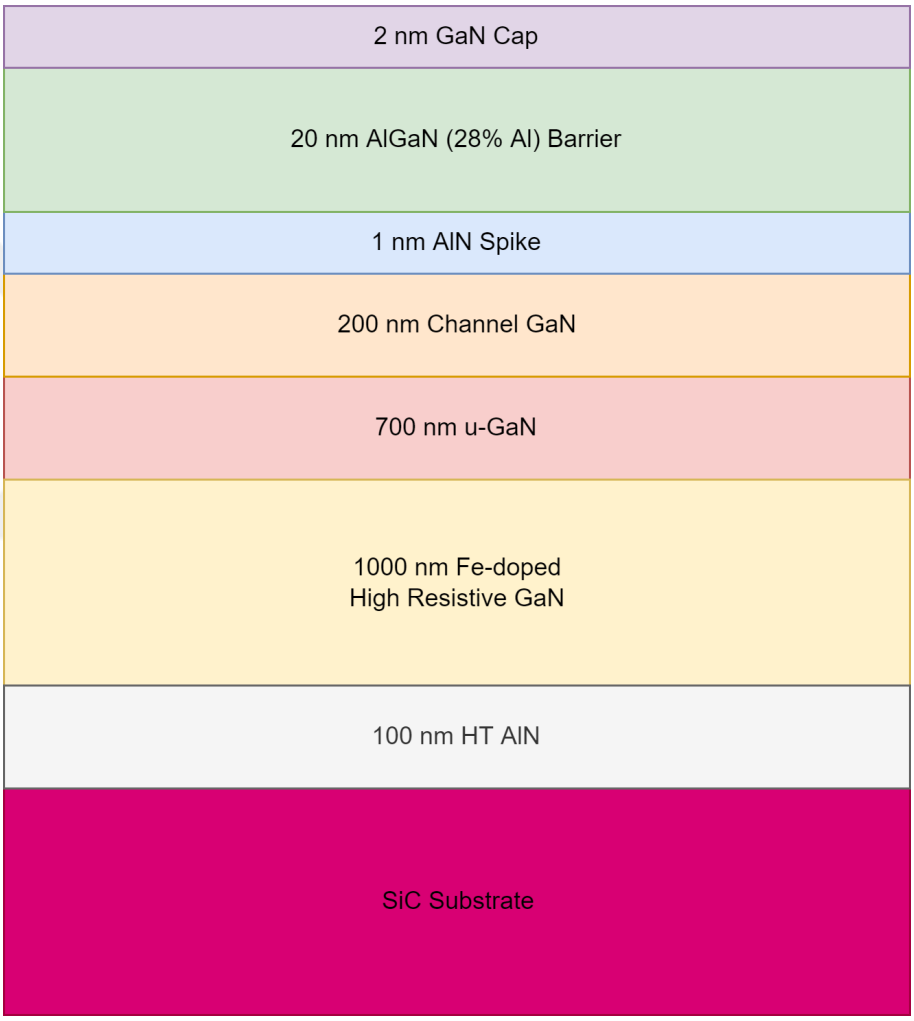


Figure 2.1: Epitaxial layers grown by MOCVD process.

2.1.1 AlN Nucleation Layer

Epitaxial growth of GaN on SiC substrate is not easy to achieve due to thermal expansion coefficient and lattice mismatch between SiC substrate and GaN with

a poor wetting performance of GaN of the SiC surface [20]. Therefore, a high-temperature AlN of 100 nm thickness is deposited on top of 300 µm SiC substrate as the first step of the fabrication. A smaller mismatch between AlN and SiC lattices, lower strain on the GaN buffer, and improved wetting behavior make the AlN nucleation layer commonly preferred for GaN on SiC epitaxy.

2.1.2 GaN Buffer Layer

On top of the AlN nucleation layer, a GaN buffer layer is grown. The purpose of a thick buffer layer is to lower the dislocation defects between top GaN layers and substrate, which are caused by thermal coefficient difference and lattice mismatches. In order to prevent leakages and improve off-state leakage performance, the resistivity of the buffer layer should be high. This resistance level is achieved by doping the buffer with acceptors such as C, Fe, or Mg. However, crystal quality is degraded by dopant atoms which cause a trap-related current collapse in the buffer region. Therefore, growing a high-quality buffer region with good insulating behavior is challenging in AlGaN/GaN HEMT technology [21, 22]. In this study, the buffer layer is doped with Fe atoms due to its shallow trap levels. The layer thickness of the buffer is about 1000 nm.

2.1.3 GaN Transition Layer

A high resistive GaN buffer layer is doped with Fe atoms diffused into adjacent layers. In order to grow a high quality channel layer for the 2DEG region, a transition layer between buffer and channel is grown. An undoped GaN layer is grown at a thickness of about 700 nm. The thickness of this layer should be large enough to prevent the memory effect, which is the segregation of Fe atoms through the GaN layers [23].

2.1.4 GaN Channel Layer

The dopants in the buffer and transition regions suppress buffer leakage and create a semi-insulating layer between the 2DEG region and substrate. However, RF and DC performance are affected by buffer traps around the 2DEG region. An unintentionally doped 200 nm GaN channel layer is deposited over the GaN transition layer to enhance the transistor performance. The GaN channel layer should be high quality with low defect density and high surface smoothness. Since the 2DEG region is built in this region, the quality of the lattice has a high impact on electrical characteristics.

2.1.5 AlN Spike Layer

For high electron density in the 2DEG region, high Al concentration is used in the AlGaN barrier. However, this leads to higher scattering and lower mobility which eventually limits the power performance of the transistor. To overcome this problem, an AlN spike layer is inserted between GaN and AlGaN interface that improves both sheet charge density and mobility [24]. The thickness of the spike layer has an effect on the mobility and electron concentration of the 2DEG region, and in this study 1 nm spike layer is grown between the AlGaN barrier and GaN channel layers.

2.1.6 AlGaN Barrier Layer

AlGaN barrier layer serves as a carrier supply for the 2DEG region. At GaN/AlGaN interface, electrons are accumulated as a sheet of polarization charges due to spontaneous and piezoelectric polarization differences. Al mole fraction of the barrier layer increases 2DEG electron concentration, leading to a larger drain current, higher cut-off frequency, and low channel resistance. However, a larger Al fraction leads to a change in the lattice and results in crystal defects and deep-level traps [25]. Likewise, 2DEG density increases by increasing

the thickness of the barrier layer. Increasing the thickness of the layer also improves the drain current while degrading high-frequency characteristics. Therefore, thickness and Al composition of barrier layers directly affect the device's electrical behavior. In this study, a barrier layer with 28% Al concentration and 20 nm thickness is grown.

2.1.7 GaN Cap Layer

The top layer of the epi structure is the GaN cap layer. 2 nm GaN is deposited over the AlGaN layer to eliminate surface oxidation of Al which creates surface defects and traps. Such a thin layer improves reliability and helps the formation of the Schottky gate.

2.2 Mask Design

After the epitaxial growth, fabricating passive and active devices is the next step of the GaN MMIC fabrication process. Photolithography masks developed to pattern shapes via etching, depositing, or coating. Throughout the process, different masks shape metal layers, form contacts, etch, or form a via are used. These masks define MMIC, HEMT, passive components, process monitoring regions, alignment marks, and Transfer Length Method patterns to control the process. An example photomask used in this thesis is shown in Fig. 2.2.

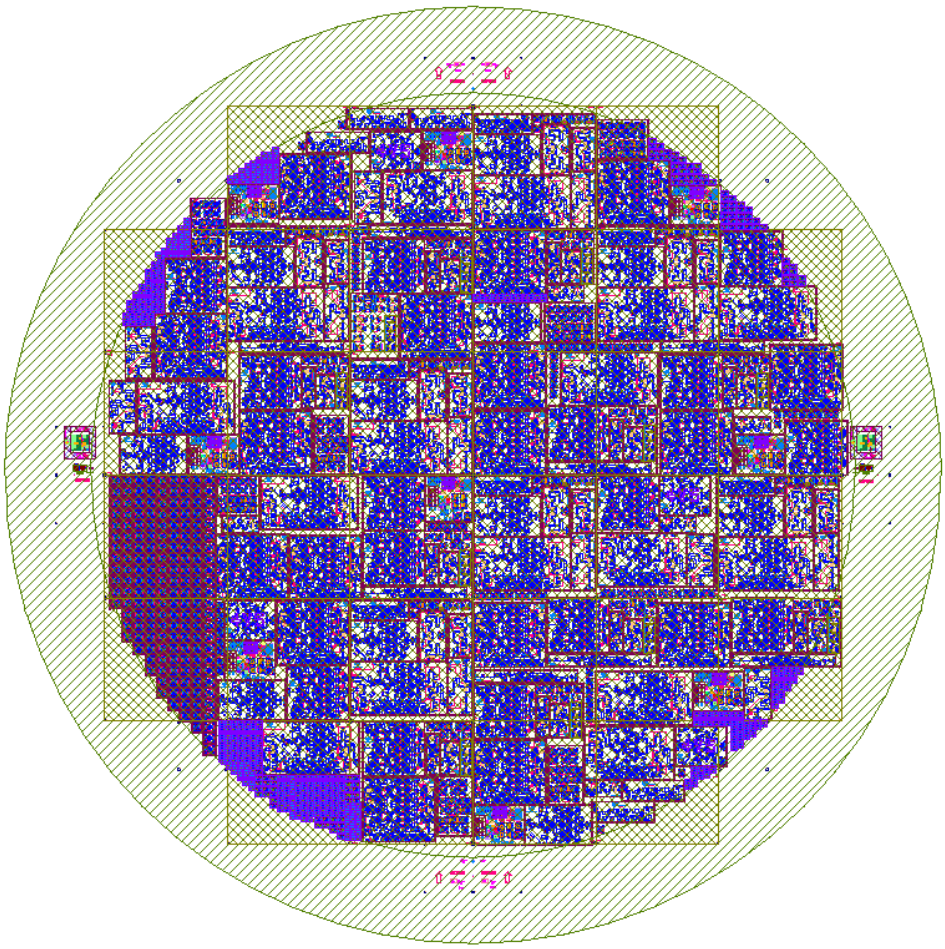


Figure 2.2: An example photomask consisting MMICs, HEMTs, and passive components used in this thesis.

2.3 Front-Side Process

The front-side process contains fundamental steps for passive and active device fabrication. It starts with ohmic contact formation, followed by mesa etching, passivation, gate formation, and metallization. Each process step is discussed in detail in the following sections.

2.3.1 Ohmic Contact Formation

Ohmic contacts in AlGaN/GaN HEMT technology are essential to connect upper conductive layers to the 2DEG region due to their low resistance and non-rectifying behavior. Low ohmic contact resistance is required for high-performing transistors, high power, and low noise applications. AlGaN/GaN HEMTs have ohmic contacts drain and source terminals. Ohmic contact formation starts by depositing Ti/Al/Ni/Au metal stack using the electron beam evaporator. After coating metals over contact vias, rapid thermal processing (RTP) is applied to the wafer in N_2 atmosphere. In Fig. 2.3, the cross-section of a wafer sample with deposited ohmic contacts is shown.

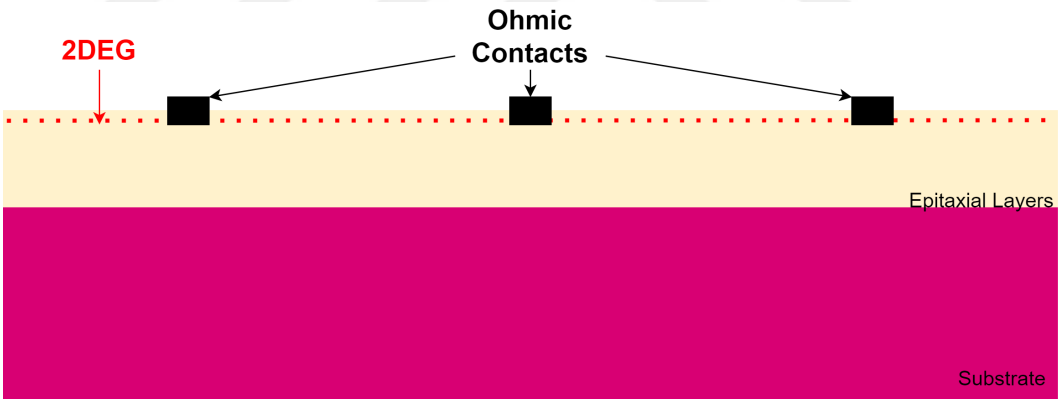


Figure 2.3: Cross-section of the wafer with ohmic contacts.

2.3.2 Mesa Etching

A GaN wafer with a complete epi structure contains 2DEG electrons all over the wafer. In order to isolate active regions throughout the wafer, the mesa etching process is applied. The etching process is achieved using inductively coupled plasma reactive ion etching (ICP-RIE). This process removes whole the 2DEG region and a part of the GaN epi layer creating electrically isolated islands. In Fig. 2.4, the cross-section of a wafer sample after the etching process is shown.

After this step, the four-probe measurement method is applied to Transmission Line Measurement patterns to characterize ohmic contact and sheet resistances.

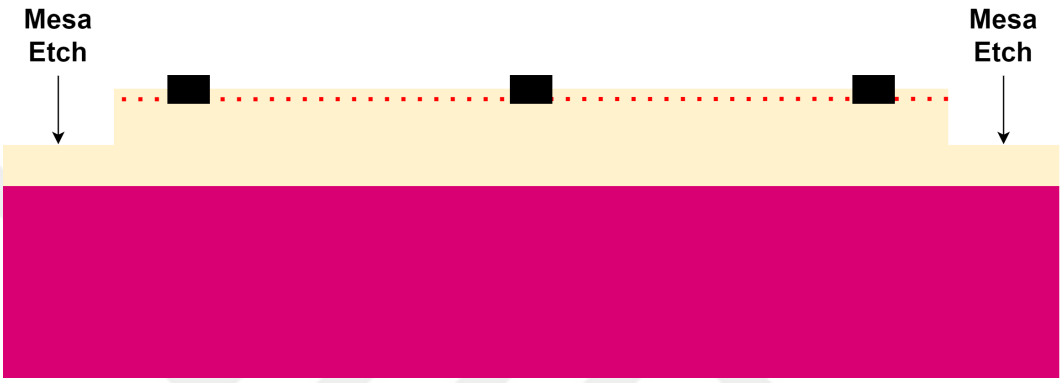


Figure 2.4: Cross-section of the wafer after the mesa etching step.

2.3.3 Passivation

The surface of the wafer contains many surface states which may be caused by defects, crystal disorder, or surface charges. These defects and surface states trap electrons and cause virtual gate formation, eventually degrading device performance. In an effort to eliminate this effect and enhance device performance, the crystal surface is passivated by a dielectric material. The passivation is achieved by coating the surface with Si_3N_4. The material is deposited using a plasma-enhanced chemical vapor deposition (PECVD) method. The gate and metal contact openings are etched by using ICP-RIE. In Fig. 2.5, the cross-section of the wafer after the passivation and etching step is shown.

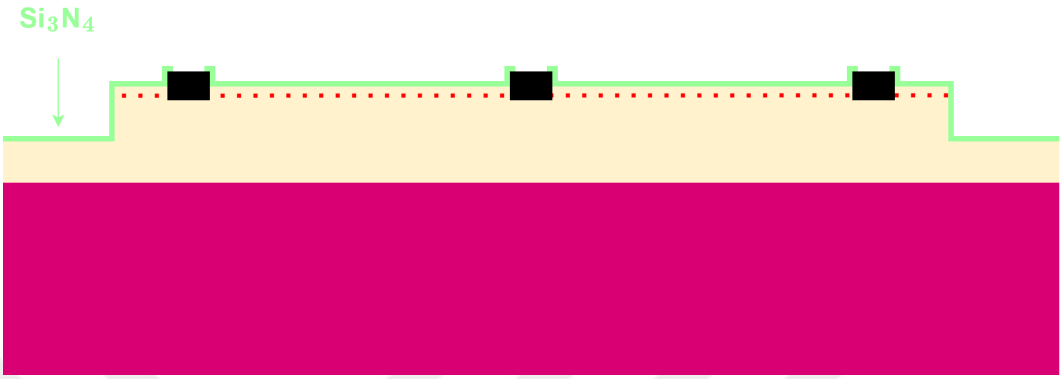


Figure 2.5: Cross-section of the wafer after passivation step.

2.3.4 Gate Formation

Gates in AlGaN/GaN technology control current flow from drain to source in HEMT switches. The head and foot dimensions directly influence device performance. In the following chapters effect of gate dimensions and their optimization will be discussed separately. After the passivation and gate foot lithography steps, Ni/Au metal stack is coated over gate openings using an e-beam evaporator. Thicknesses of gate foot and head of T-gate structure are 100 nm and 600 nm, respectively. In Fig 2.6, the cross-section of the wafer after gate formation is shown.

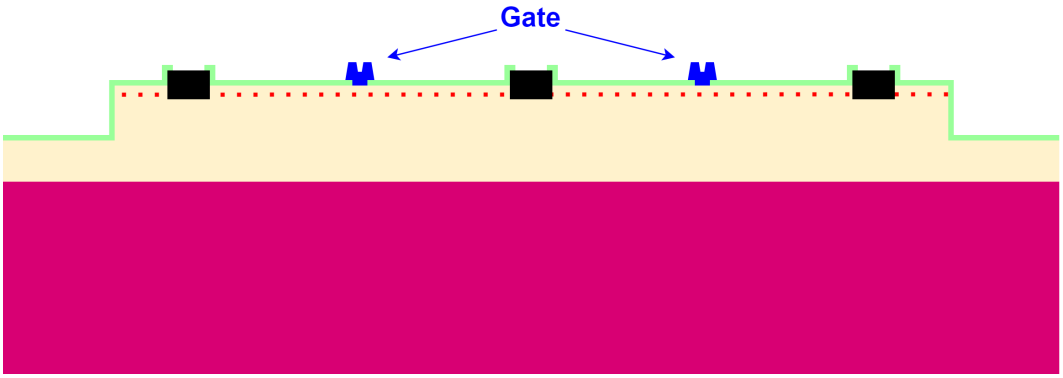


Figure 2.6: Cross-section of the wafer after the gate formation.

2.3.5 Metallization

Metal layers connect transistors to passive components, one of the fundamental fabrication steps of the MMIC process. As the first step metallization process, a second Si_3N_4 passivation layer is deposited over the wafer after the gate formation. Depending on the application, a field plate formation can be applied at this stage. However, switch transistors in this thesis do not have source-connected field plates to improve off-state capacitance. The reason is that the drain-source voltage of an ON-state transistor is equal to 0 V, which eliminates the need for reshaping the electric field profile. Fig. 2.7 shows wafer cross-section with metal contact openings and second passivation layer. After the passivation step, Ti/Au metal stack is deposited using an e-beam evaporator. The cross-section of the wafer with the first metal layer is shown in Fig. 2.8.

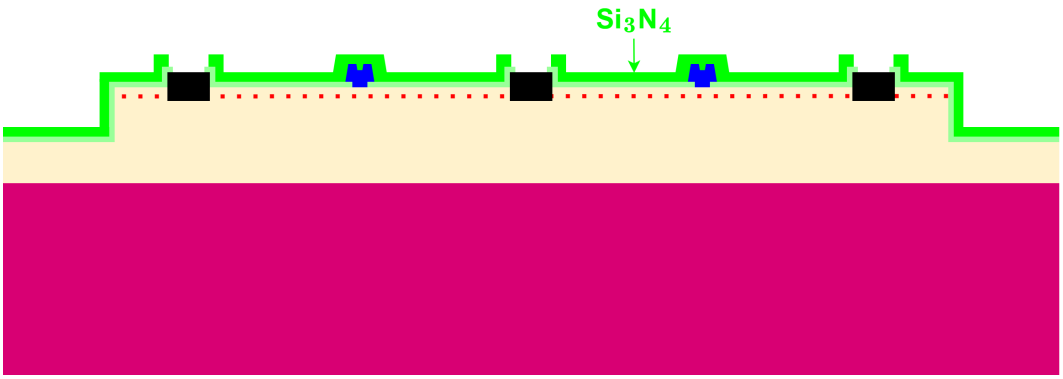


Figure 2.7: Cross-section of the wafer after second passivation layer.

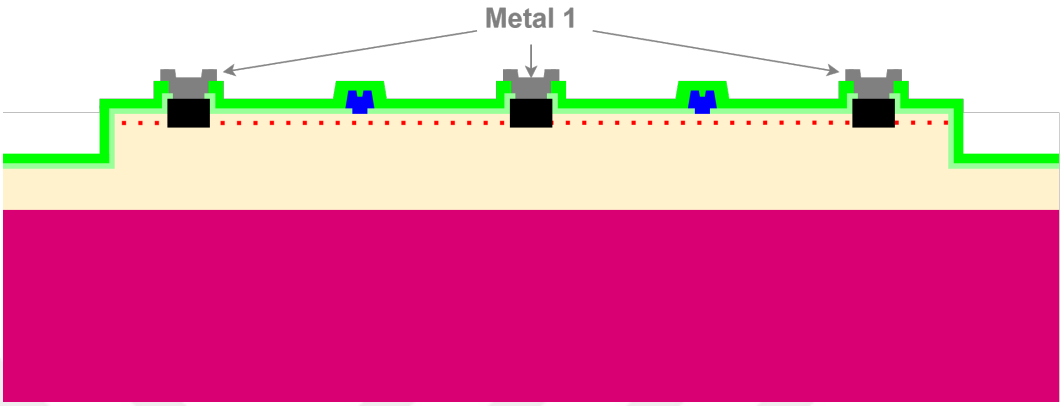


Figure 2.8: Cross-section of the wafer with metal 1 layer.

A second metal layer is deposited over the first layer to improve current capacity with thicker metal and provide connection paths. Like in the previous step, a passivation layer is deposited and etched at contact zones as in Fig. 2.9.

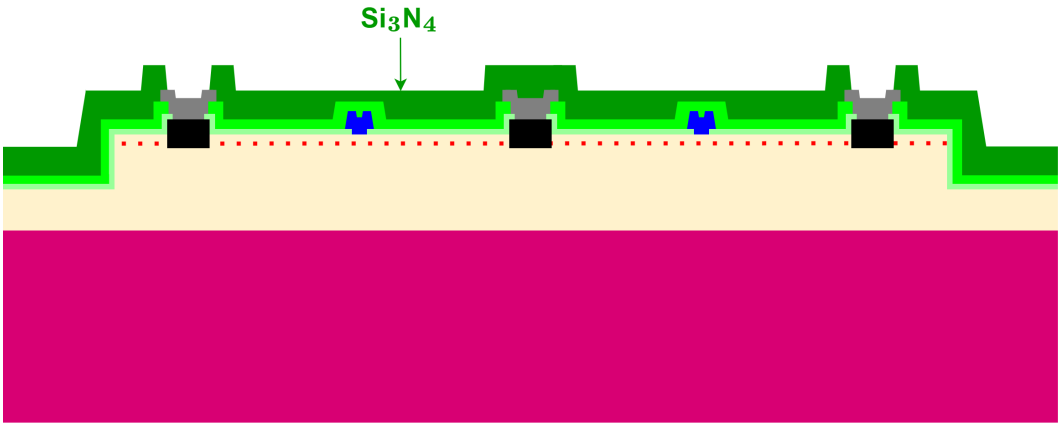


Figure 2.9: Cross-section of the wafer after third passivation layer.

Before depositing the Metal 2 layer, air bridges are built above the third passivation layer. Air bridges create space between two conducting layers so that interconnections can be achieved without a short circuit. After this step, 4 µm Au is deposited with electroplating. Fig. 2.10 shows the wafer cross-section after completing the metallization step.

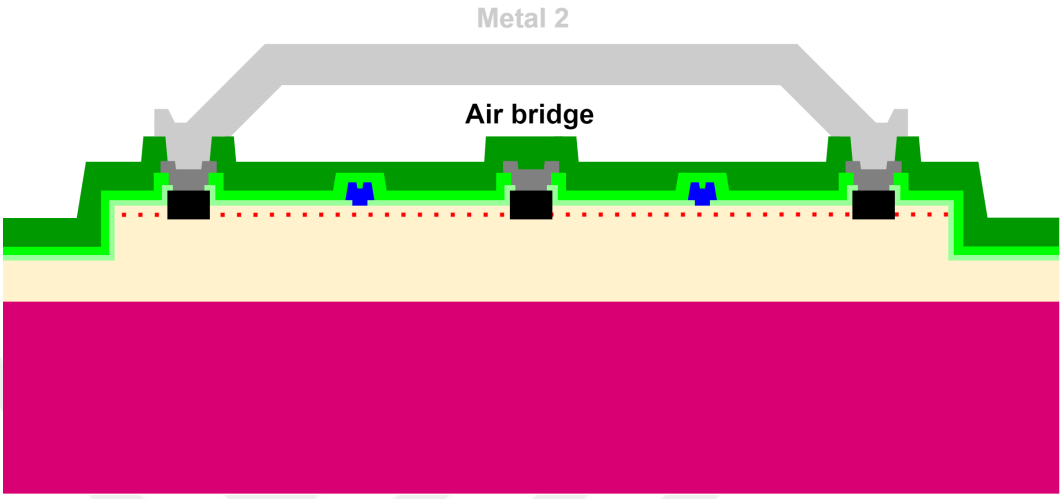


Figure 2.10: Cross-section of the wafer after metallization.

The last (optional) step of the front-side process is coating the surface with a thin dielectric to protect the wafer from external factors. After the coating, the wafer is etched at probing pads. At the end of the front-side process, the wafer cross-section looks as in Fig. 2.11.

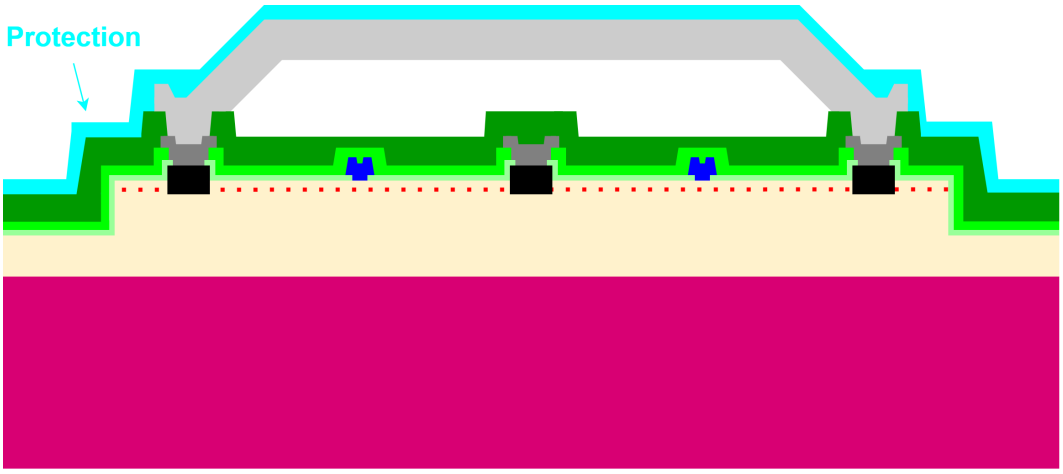


Figure 2.11: Cross-section of the wafer after front-side process.

2.3.6 Passive Components

In the MMIC process, passive components are formed on chip as well as transistors. Thin-film resistor, mesa resistor, MIM capacitor, and spiral inductor fabrication processes are explained. In Fig. 2.12, the cross-section of the wafer with passive components is shown.

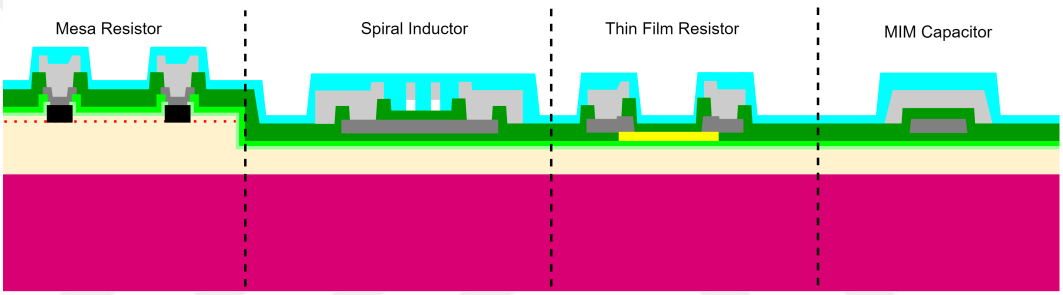


Figure 2.12: Cross-section of the wafer with passive components.

2.3.6.1 Mesa Resistor

Depending on the application, high resistance values may be needed. The gate is connected to control voltage for switch HEMTs via a resistor value in kilo-ohms. In the GaN MMIC process, high resistance values are achieved by mesa resistors. The epi layer has a high sheet resistance of about $350\,\Omega/\square$. Mesa resistors are fabricated by connecting two ends of an isolated active area with an ohmic contact. Therefore, high resistance can be achieved by adjusting isolated area length and width.

2.3.6.2 Spiral Inductor

Spiral inductors are fabricated using air bridges and metal layers. The transmission lines' spiral shape is fabricated in the second metal layer, and the connection from inside the spiral to the outside of the spiral is achieved by using an air

bridge. Metal 1 layer connects the spiral inductor. Fig. 2.13 shows the SEM image spiral inductor where the Metal 2 layer jumps over Metal 1.

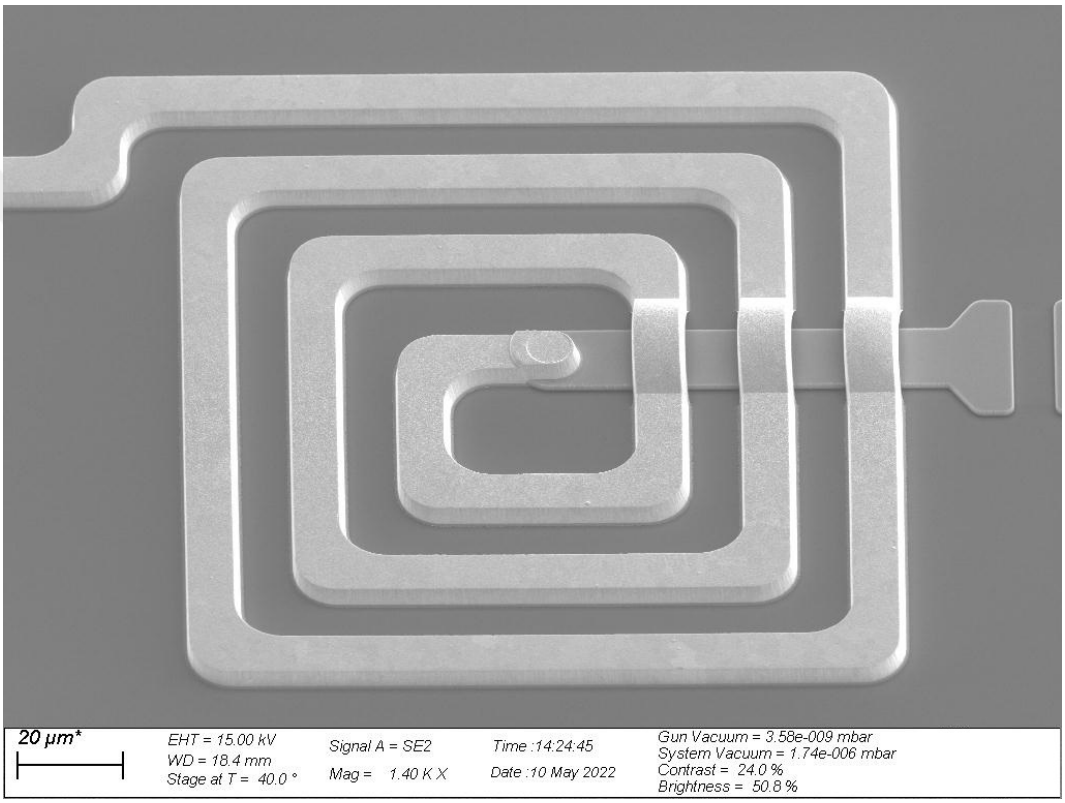


Figure 2.13: SEM image of an on-chip spiral inductor.

2.3.6.3 Thin Film Resistor

The thin-film resistor is achieved by depositing TaN using the sputtering system over the second passivation layer. The rest of the process is completed following the previous steps by connecting resistor ends to metallization layers. Thin-film resistors are found in mesa etched layers, and typically they are set to have $30\,\Omega/\square$. Thin film resistors are usually used at small resistance values.

2.3.6.4 MIM Capacitor

MIM capacitors are realized by placing metal layers on top of each other, insulated by the third passivation layer. The thickness and dielectric constant of Si_3N_4 determine the capacitance density between two conducting layers, which is set to 270 pF/mm^2. The required capacitance value can be realized by adjusting the overlapping area between metal layers.

2.4 Back-Side Process

The last step of AlGaN/GaN MMIC fabrication is the back-side process. In order to connect the ground plane to passive and active devices, connection vias are etched. First, the process starts with etching the substrate down to 100 µm thickness. The back-via holes are etched by using ICP-RIE. The back-side and inner walls of the vias are coated with 4 µm Au metal using the electroplating method. Inner wall metal coating electrically connects the back-side ground to the front side. In Fig. 2.14, the wafer cross-section after backs-side process is shown.

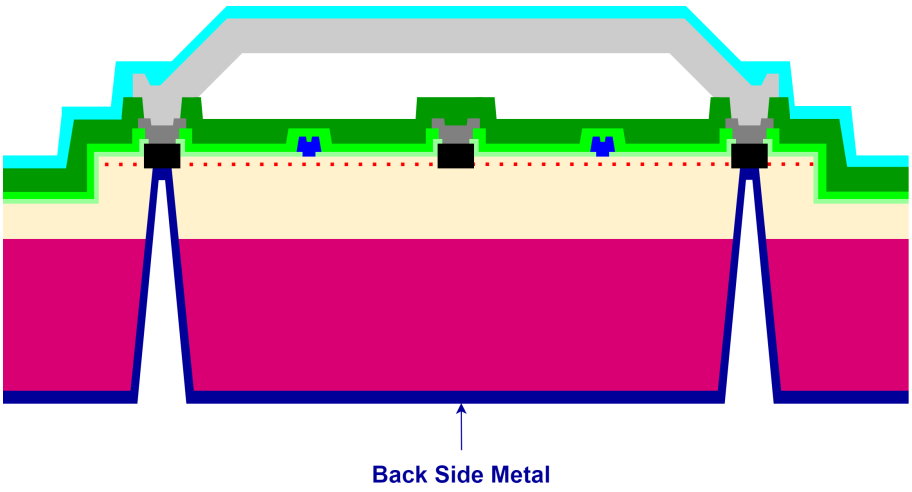


Figure 2.14: Cross-section of the wafer after the back-side process.

Chapter 3

RF Switch Fundamentals

In this chapter, the fundamentals of RF switches and their performance figures are discussed. RF switches are fundamental tools in MMIC designs to control the flow of signals. By the nature of MMIC technology, they have specific characteristics and limits. RF switches are characterized by maximum power handling, insertion loss, isolation, return loss, linearity, bandwidth, switching speed, and noise. Depending on the application, each performance parameter is optimized, which is limited by the technology.

3.1 RF Switch Topologies

RF switches are classified according to the number of inputs (poles, control signals) and outputs (throws, ON positions) they possess. They provide paths for signals to flow from a number of inputs to a number of outputs. Although there are various topologies used in the industry, the four most common switch topologies are single-pole single-throw(SPST), single-pole double-throw(SPDT), double-pole single-throw(DPST), and double-pole double-throw(DPDT). Switch diagrams are showed in Fig. 3.1.

SPST is the simplest switch topology that directs the signal from open-circuit

to output node. SPDT is most commonly used topology since T/R modules require this topology to direct signal from antenna to LNA or PA. DPST topology control two signal paths with their single output node. Likewise, DPDT links two signal paths to their double outputs. This topology has two inputs with four outputs and controls two independent paths.

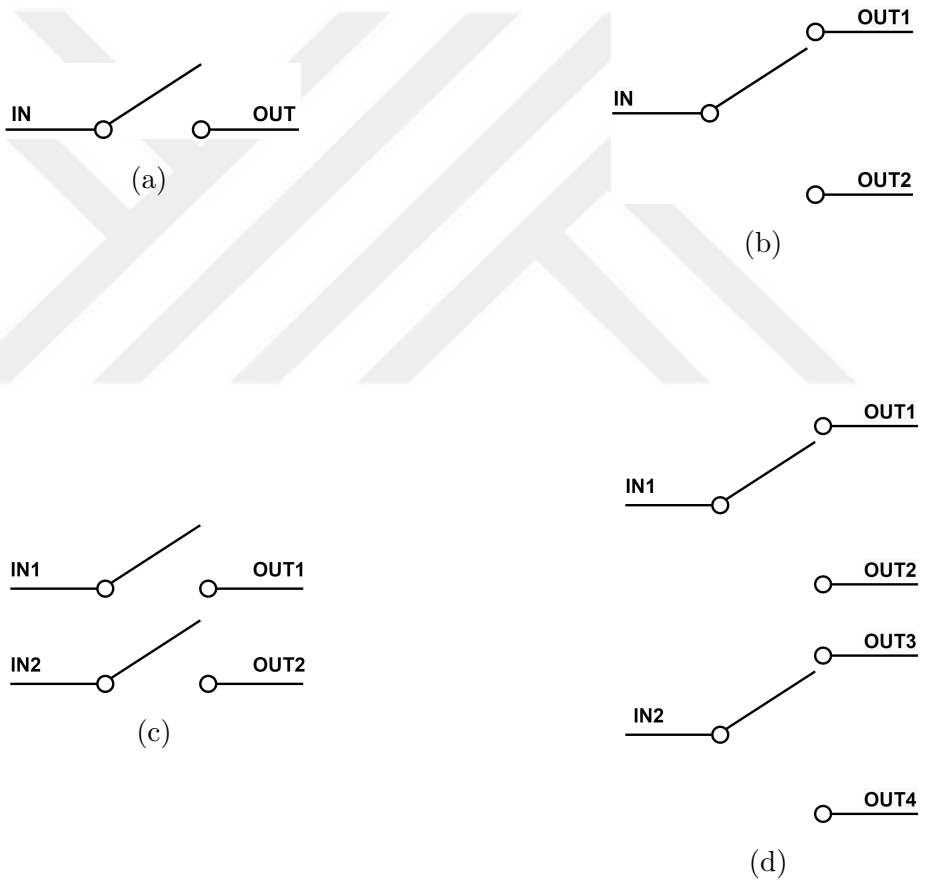


Figure 3.1: (a) SPST, (b) SPDT, (c) DPST, and (d) DPDT switch diagrams.

Outside the fundamental switch topologies, the number of examples may be increased according to applications. In this thesis, the SPDT switch for T/R modules is designed, fabricated, and characterized.

3.2 RF Switch Fundamentals

In this section, basic RF concepts used in RF switch design will be explained. These concepts will be used in the following sections.

3.2.1 Scattering Parameters

In RF design engineering, the scattering matrix is widely used to characterize circuit components. Since it is not practical to characterize a circuit by measuring voltages and currents at microwave frequencies, the magnitude and phase of traveling waves in a particular direction define the electrical characteristics. Therefore, the scattering matrix is used to represent incident, reflected, and transmitted waves which can be directly inferred from the measurements. It can describe any N-port network. In Fig. 3.2, a two-port network with the incident, reflected, and transmitted wave flows are shown. In the figure, a_n defines the waves going towards the nth port, and b_n defines the waves traveling away from the nth port.

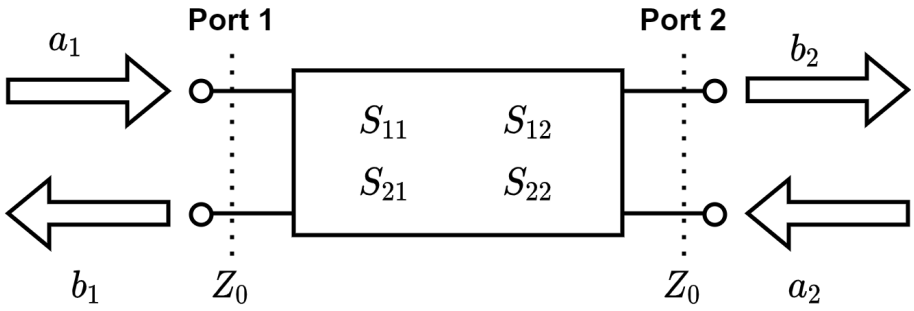


Figure 3.2: Generalized two port network showing power flow.

The 2-port system can be expressed as:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{3.1}$$

where we can expand the matrix into equations as

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{3.2}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{3.3}$$

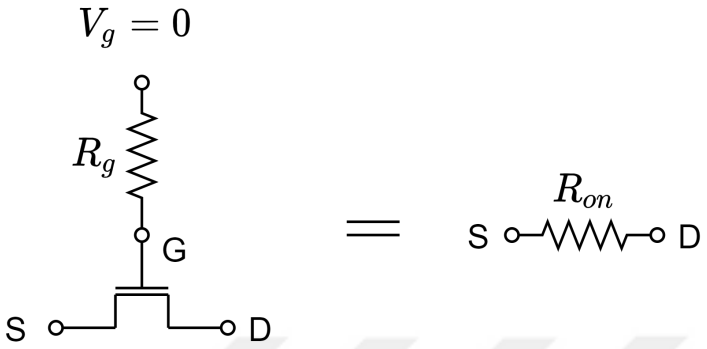
The given equations define the relationship between reflected and incident power waves. In the following sections, scattering matrix definitions will be used to define circuit behavior, such as input and output return losses, insertion loss, isolation, and reflection coefficient.

3.2.2 HEMT Switching Modes

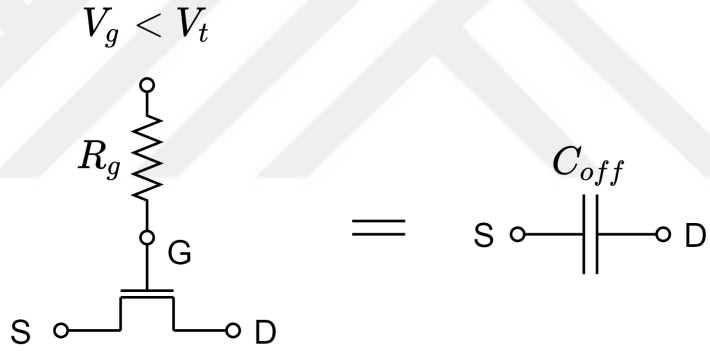
In order to control the flow of electrical signals, transistors are used in two different modes. For normally ON GaN HEMTs, the gate voltage is set to 0 V to switch its ON state. From drain terminal to source terminal, the transistor can be modeled as resistance (R_{on}). Likewise, a negative voltage smaller than its threshold is applied to the gate of HEMT to switch it OFF. Transistor behaves as a capacitor (C_{off}) in this mode of operation. Those values are also functions of applied gate voltage. The larger the negative gate voltage applied results in higher off capacitance. In Fig. 3.3, equivalent representations of ON and OFF mode switch HEMTs are shown. The ON resistance and OFF capacitance can also be defined with S-parameters of the transistor by equations 3.4 and 3.5. R_{on} and C_{off} values can be obtained by direct S-parameter measurement using the given relations [26].

$$R_{\text{on}} = 2Z_0(10^{-S_{21\text{dB}}/20} - 1) \tag{3.4}$$

$$C_{\text{off}} = -\frac{1}{2Z_0 w\sqrt{10^{-S_{21\text{dB}}/10} - 1}} \tag{3.5}$$



(a)



(b)

Figure 3.3: (a) ON-state and (b) OFF-state switch HEMT equivalent circuit.

The small-signal performance of a switch is characterized by its FOM, which depends on its C_{off} and R_{on}. The FOM unit is Hz indicating the switch's operational frequency limit. Eq. 3.6 shows the FOM definition [27].

$$Figure of Merit = \frac{1}{2\pi C_{off} R_{on}} \tag{3.6}$$

3.2.3 1 dB Compression Point

In practice, all active devices behave as a linear system under certain conditions. Active devices such as transistors become non-linear at high input power levels due to saturation, intermodulation distortion, or harmonic generation. At higher power levels, the gain of an amplifier or insertion loss of a switch starts to degrade. The point where the output power of the active devices trails off 1 dB from its linear response is called the 1 dB compression point (P_{1dB}). Fig. 3.4 shows the typical response of a switch which indicates P_{1dB} clearly.

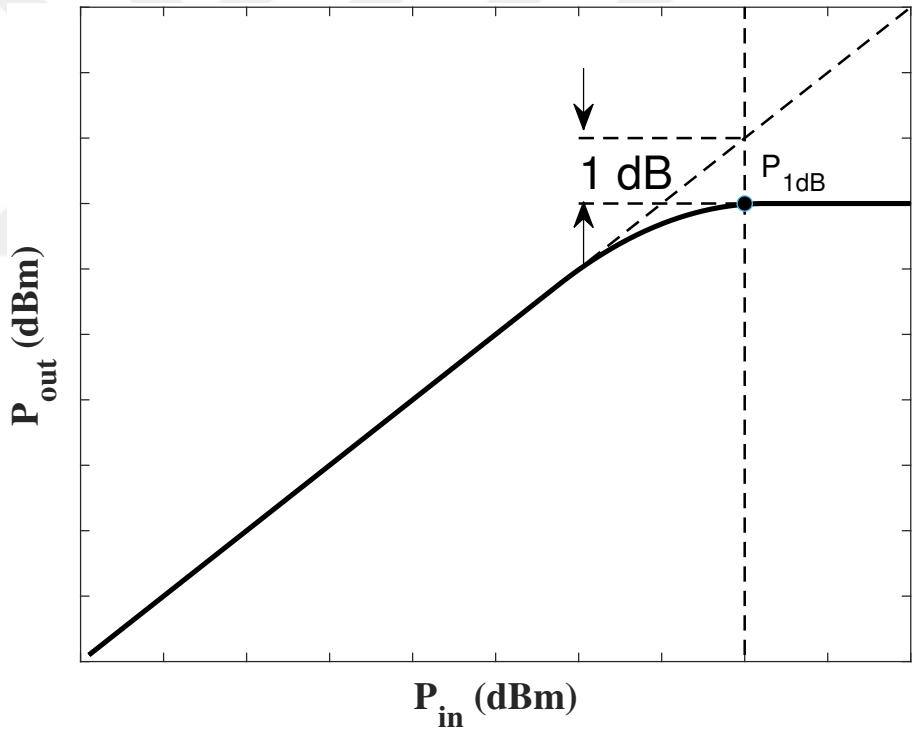


Figure 3.4: 1 dB compression point.

To analyze the compression behavior, first, a simple case where a single-frequency sinusoidal voltage is applied to the non-linear device:

$$v_{\mathrm{i}} = V_0 cos\omega_0 t \tag{3.7}$$

$$v_{\mathrm{o}} = a_0 + a_1 v_{\mathrm{i}} + a_2 v_{\mathrm{i}}^2 + a_3 v_{\mathrm{i}}^3 + ... \tag{3.8}$$

The output becomes:

$$v_{\mathrm{o}} = a_0 + a_1 V_0 cos\omega_0 t + a_2 V_0^2 cos^2\omega_0 t + a_3 V_0^3 cos^3\omega_0 t + ... \tag{3.9}$$

$$\begin{aligned} v_{\mathrm{o}} = (a_0 + \frac{1}{2}a_2 V_0^2) + (a_1 V_0 + \frac{3}{4}a_3 V_0^3) cos\omega_0 t + \\ \frac{1}{2}a_2 V_0^2 cos2\omega_0 t + \frac{1}{4}a_3 V_0^3 cos3\omega_0 t + ... \end{aligned} \tag{3.10}$$

If we consider gain at fundamental frequency component ω_0:

$$G_{\mathrm{v}} = \frac{v_o(\omega = \omega_0)}{v_i(\omega = \omega_0)} = \frac{a_1 V_0 + \frac{3}{4}a_3 V_0^3}{V_0} = a_1 + \frac{3}{4}a_3 V_0^2 \tag{3.11}$$

Typically a_3 has the opposite sign of a_1, which results in compression of voltage gain at higher voltage levels. P_{1dB} refers to the point where this compression terms reaches 1 dB at the output power level.

3.2.4 Third-Order Intercept Point

For a single frequency signal input, analysis of output voltage which involves harmonics of the input signal, is given in the previous section. If a two-tone signal is applied to a system with expressed Eq. 3.8:

$$v_{\mathrm{i}} = V_0(cos\omega_1 t + cos\omega_2 t) \tag{3.12}$$

The output voltage becomes:

$$\begin{aligned} v_{\mathrm{o}} = a_0 + a_1 cos\omega_1 t + a_1 cos\omega_2 + a_2 cos2\omega_1 t + a_2 cos2\omega_2 t + a_3 cos(\omega_2 - \omega_1)t + \\ a_3 cos(\omega_2 + \omega_1)t + + a_4 cos(2\omega_2 - \omega_1)t + a_4 cos(2\omega_2 + \omega_1)t + ... \end{aligned} \tag{3.13}$$

where output voltage contains harmonics in the form on $m\omega_1 + n\omega_2$ with $m, n = 0, \mp 1, \mp 2, \mp 3, ...$ Fig. 3.5 shows harmonics of the output signal in a simple spectrum. All intermodulation products are undesired at the output side. However, intermodulation products that are not closely located to fundamental frequencies are easy to suppress with a bandpass filter. Especially, third-order harmonics $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$ closest to the fundamental frequency degrade system's linearity.

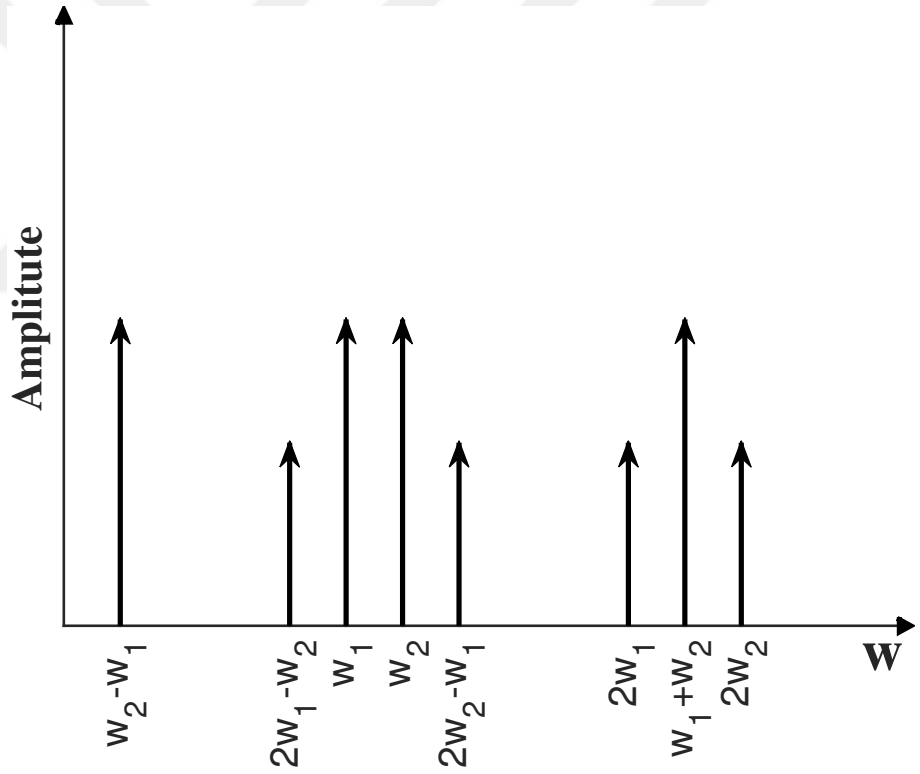


Figure 3.5: Two tone signal intermodulation products.

When input voltage increases by V_0, the third-order harmonics increase by V_0^3. Power-wise, third-order products increase thrice in dB scale while fundamental tones increase by one time. Although this effect is very small at small input power levels, they intersect at a higher power level. The theoretical point where linear responses of fundamental and third-order harmonic meet is called the third-order intercept point ($IP3_3$). The graphical representation of IP_3 is shown in

Fig. 3.6. The input (IIP_3) and output (OIP_3) power levels at this point are used to characterize device linearity.

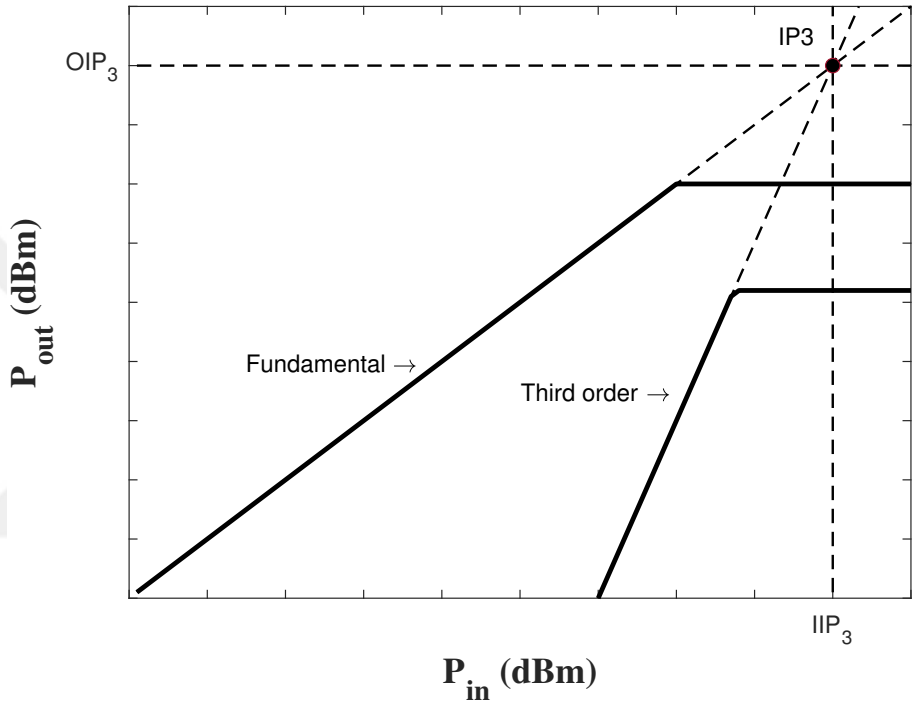


Figure 3.6: Third-order intercept point illustration.

3.3 RF Performance Parameters

There are several figures of merits that characterize a switch's performance. Since there is a compromise between metrics of a switch, it is not straightforward to improve all of them simultaneously. This balance is limited by fabrication technology. Depending on the application, switches may require to show high performance on a specific metric by sacrificing from others. In Fig. 3.7, general performance metrics that characterize an RF switch are shown. In the following sections, they are discussed in detail.

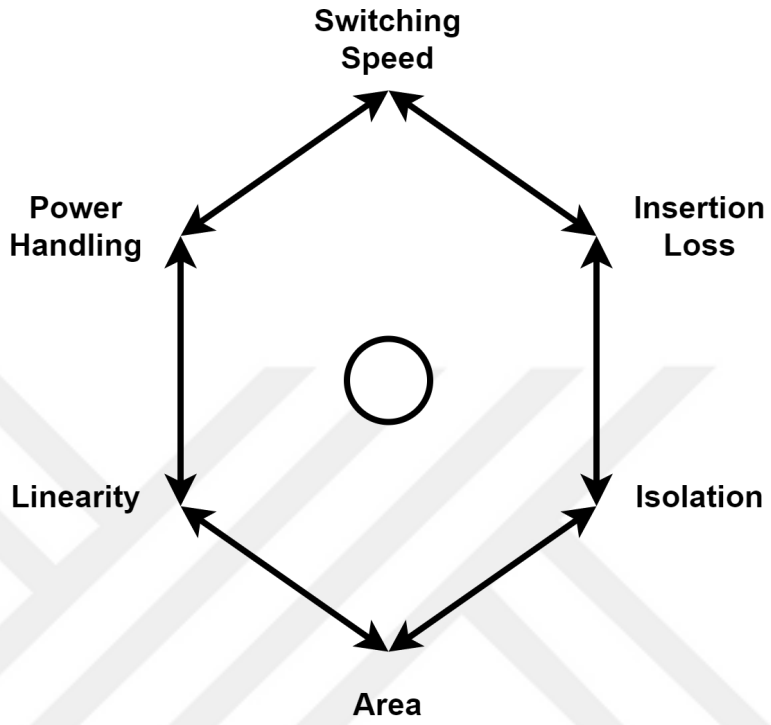


Figure 3.7: RF switch performance metrics.

3.3.1 Insertion Loss

The insertion loss (IL) of a switch characterizes its ON-state transfer performance. When ports are matched, the ratio of input power transferred to output in linear operation equals insertion loss. Since the transmission lines, transistors, or lumped components in the MMIC process are not ideal, they bring loss into the design. A good switch insertion loss should have as small as possible, and ideally, it should be 0. For a good matched circuit, insertion loss can be described in terms of its scattering parameters as:

$$IL = -20log_{10}|S_{21}|\,dB \tag{3.14}$$

3.3.2 Isolation

Isolation is a measure of the power transmitted when the switch is OFF. Ideally, a switch should not leak power in its OFF-mode. However, it is degraded by OFF-state capacitance of the transistor and coupling between transmission lines. The value of OFF-state capacitance becomes more important at higher frequencies. For a good matched circuit, isolation can be described in terms of its scattering parameters as:

$$ISO = -20\log_{10}|S_{21}|\ dB \tag{3.15}$$

3.3.3 Return Loss

Impedance mismatch between input and output ports of circuits may cause loss. This result in a portion of available source power is not delivered to load which is called return loss. The return loss can also be interpreted as a signal reflected back to the subsequent circuit. Input and output return loss for a switch can be described by its scattering parameters as:

$$RL_{in} = -20\log_{10}|S_{11}|\ dB\ or\ RL_{out} = -20\log_{10}|S_{22}|\ dB \tag{3.16}$$

3.3.4 Linearity

The linearity of a switch is characterized by its ability to continue its operation without any distortion. IIP3 and P_{1dB}, which are described in the previous sections, are commonly used metrics to indicate the linearity performance of a switch. Specifically, increasing demand for 5G transceiver modules with better linearity performance.

3.3.5 Power Handling

Power handling of a switch refers to its ability to continue its operation without gain compression. As explained in the previous section, it refers to P_{1dB} point. For ON-state and OFF-state HEMTs, power handling can be described according to maximum current handling and breakdown voltage of the transistor. Equations 3.17 and 3.18 [26] refers to power handling of a transistor at its ON and OFF states. I_{MAX}, V_{BR}, and V_{P} represent maximum channel current, breakdown voltage, and pinch-off voltage, respectively.

$$P_{\mathrm{ON}} = \frac{{I_{\mathrm{MAX}}}^2 Z_0}{2} \tag{3.17}$$

$$P_{\mathrm{OFF}} = \frac{(V_{\mathrm{BR}} - V_{\mathrm{P}})^2}{2Z_0} \tag{3.18}$$

3.3.6 Switching Speed

The switching speed of a switch is a measure of time between its ON and OFF states. At the RF output port, power is measured by a square-law detector when the gate is controlled by an input signal. The ON time of the switch is characterized by the time period between 50% of the input signal and 90% of the square-law detector RF power. Similarly, the OFF time of the switch is characterized by the time period between 50% of the input signal and 10% of the square-law detector RF power. Depending on the shunt-series configuration, the input control signal may refer to high to low or low to high transition. In Fig. 3.8, timing diagram is shown.

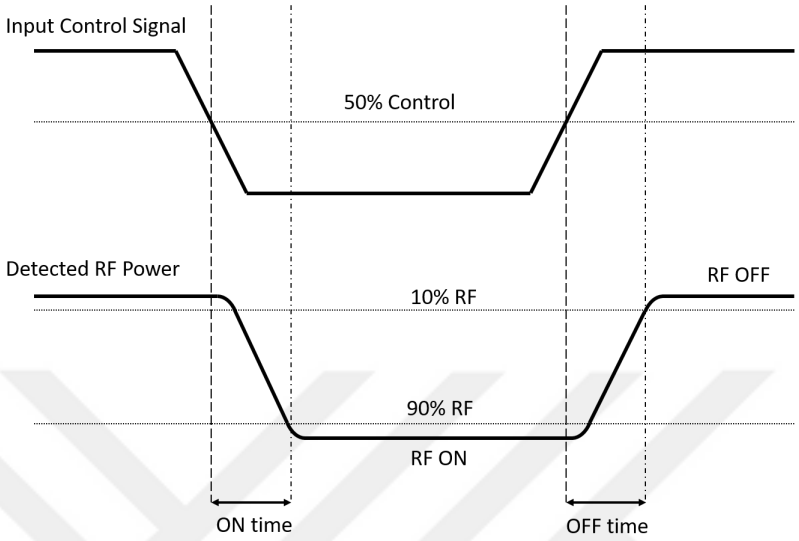


Figure 3.8: Switching time diagram of a RF switch.

Chapter 4

Optimization of Switch Transistor Gates

The performance of switch transistors depends on their R_{on} and C_{off} values with their power handling capacity. Transistors in different gate foot and gate head lengths are fabricated and characterized. In this chapter, optimization of transistor performance parameters in different gate sizes will be discussed in detail.

4.1 Gate Foot and Length Variation

Four different transistors in different gate structures are fabricated and characterized to analyze the performance variation with respect to gate dimensions. The gate head length is varied from 500 nm to 750 nm, while the gate foot length is varied from 200 nm to 250 nm. The switch transistor structure is shown in Fig. 4.1 with the epitaxial layers shown. The gates of transistors are designed to be fingered for larger gate peripheries in a smaller area. In order to compare only the T-gate dimensions, the gate periphery of the transistors is kept at 750 µm with the gate resistance of 2.5 kΩ.

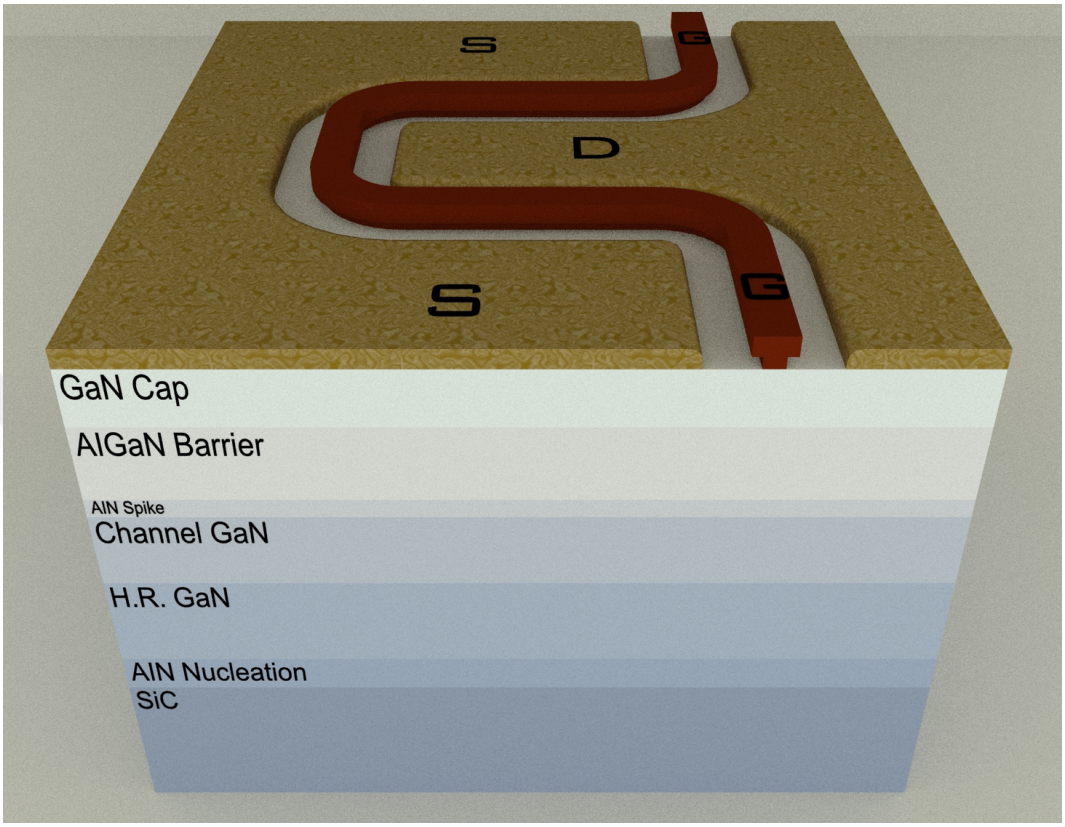
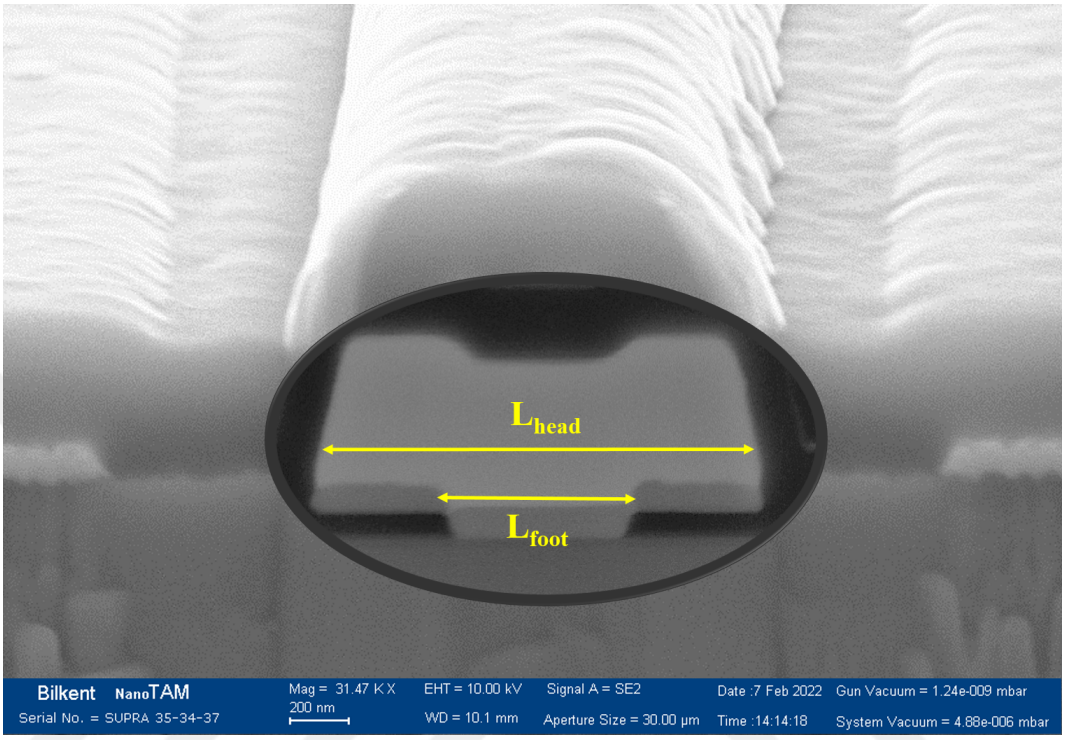
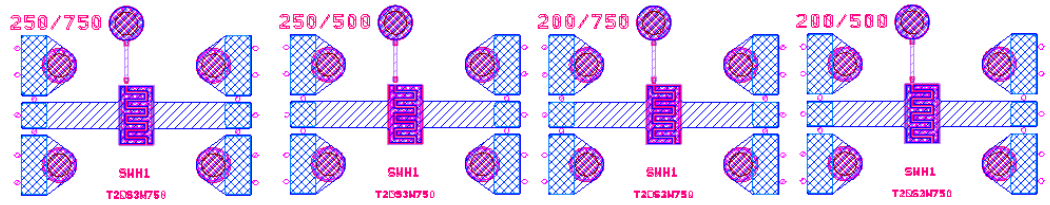


Figure 4.1: Drawing of the HEMT structure.

The scanning electron microscope (SEM) images of the fabricated HEMT and T-gate structure are taken. Fig. 4.2a shows SEM images with gate foot and gate head lengths indicated on the T-gate structure. The transistors with different gate dimensions are placed in a transistor reticle as in Fig. 4.2b. Drain to source distance of transistors are 2.5 µm. The four different types of gate structures have 250-750, 250-500,200-750, and 200-500 gate foot and head lengths in nanometres, respectively.



(a)



(b)

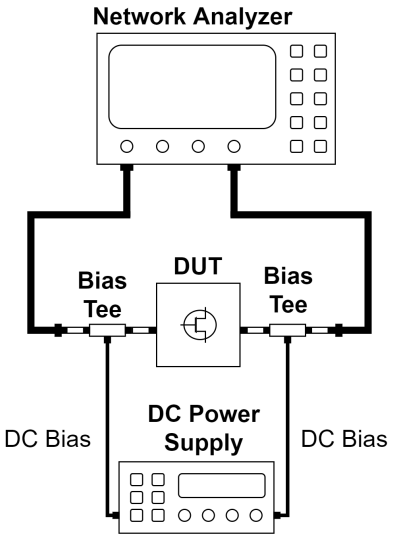
Figure 4.2: (a) SEM image of the fabricated T-gate HEMT and (b) layout of transistor reticle.

4.2 Measurements

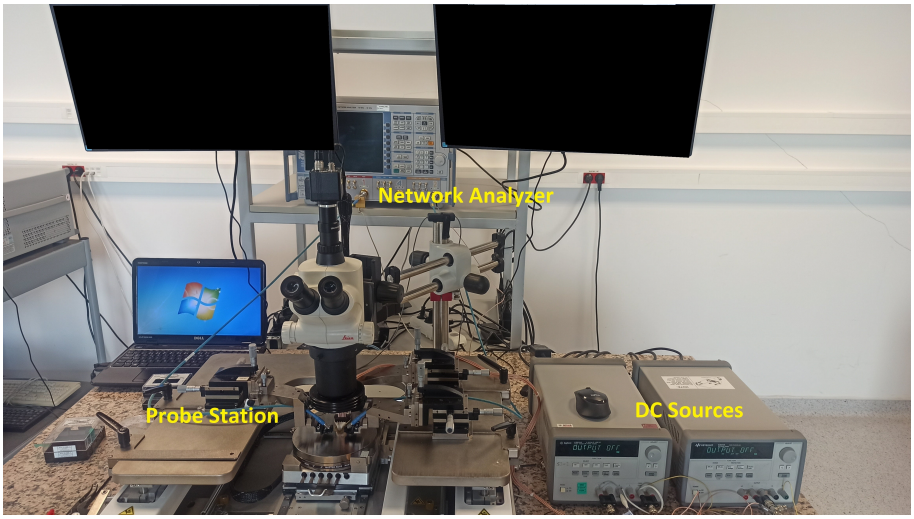
After the fabrication of transistors, they are characterized in terms of their small-signal, large-signal, and linearity performance.

4.2.1 Small-Signal Measurements

Small-signal RF measurement setup is used to characterize the behavior of non-linear HEMTs or MMICs in a linear low-power regime. A network analyzer is used to obtain the S-parameters of the device under test to perform the measurement. The purpose of using a probe station is to measure on-wafer transistors and MMICs. External DC supplies bias the transistors' gate, drain, and source.



(a)



(b)

Figure 4.3: (a) Diagram and (b) photograph of small-signal measurement setup.

In Fig. 4.3, a photograph and diagram of the small-signal measurement setup are shown with DC and RF path connections. Continuous-wave (CW) S-parameters are measured at room temperature. Gates of switch transistors are controlled by 0 V and -28 V for ON-state and OFF-state measurements.

The small-signal measurement results of ON-state transistors with their S_{21} result from 2 GHz to 10 GHz are shown in Fig. 4.4. When the gate foot and gate head of the transistor is reduced in size, the ON-state small performance of the switch improves.

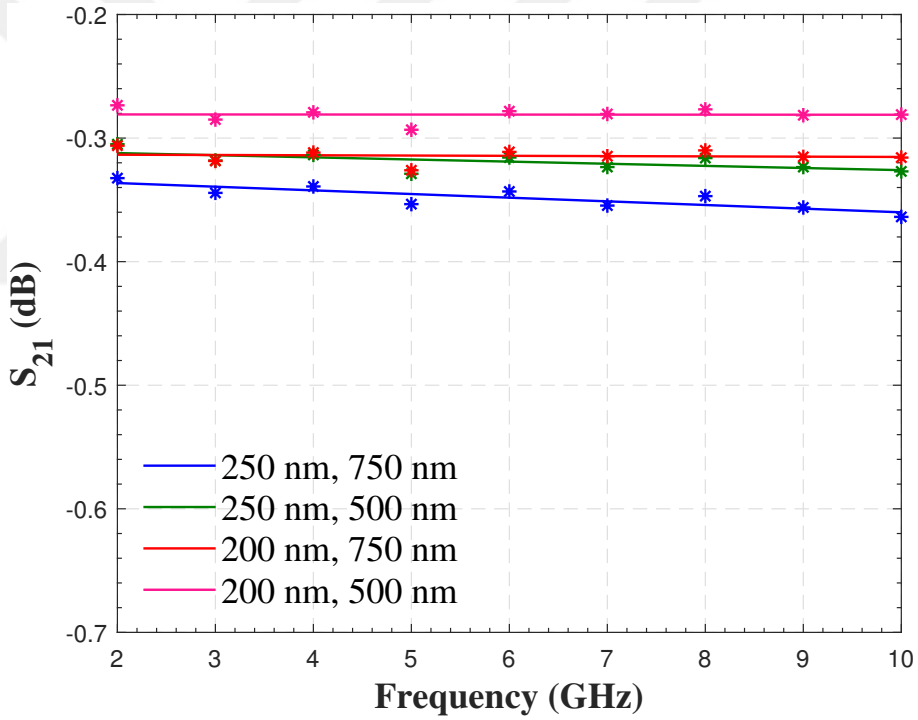


Figure 4.4: S_{21} small signal measurements of ON-state transistors with different gate shapes (legend shows L_{foot} and L_{head} respectively).

Using the Eq. 3.4 and small-signal measurement results of an ON-state transistor, R_{on} values are calculated. In Fig. 4.5, normalized the ON-state resistances for different gate structures are shown. The transistor with 200 nm foot and 500 nm head lengths shows $0.5\,\Omega\,$mm improvement with respect to a transistor with 250 nm foot and 750 nm head lengths. The reduction in the resistance can be explained by enhancing short-channel effects with a smaller gate footprint [28].

Fig. 4.6 shows ON-state and OFF-state resistance and capacitance parasitic components of a T-gate HEMT. R_{sh}, R_c, L_{gs}, and L_{gd} represents sheet resistance, contact resistance, gate-source distance, and gate-drain distance, respectively. Other parameters shows capacitance and resistance between three terminal points under the gate. With a shorter gate footprint, R_{ds} becomes small, which results in better small-signal ON-state performance.

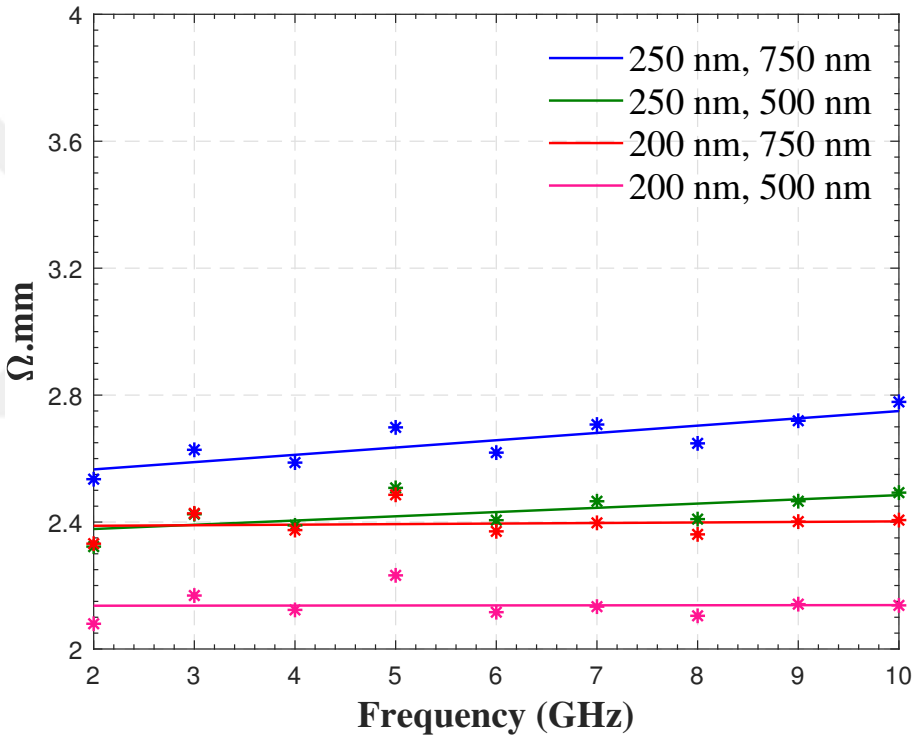


Figure 4.5: ON-state resistance values for different gate topologies (legend shows L_{foot} and L_{head} respectively).

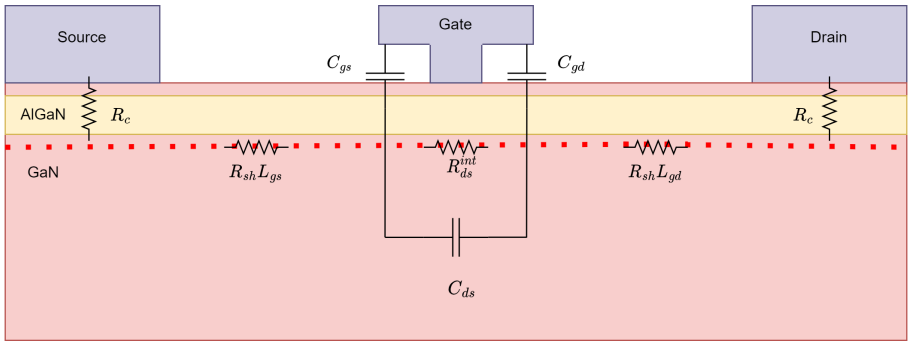


Figure 4.6: Switch HEMT parasitic element diagram.

The OFF-state small-signal performance is characterized by the small-signal measurement setup when -28 V is applied to the gates of transistors. Measured S_{21} results in dB from 2 GHz to 10 GHz are shown in Fig. 4.7. To convert the small-signal measurement to OFF-state capacitance Eq. 3.5 is used. Fig. 4.8 shows normalized OFF-state capacitances for different gate structures.

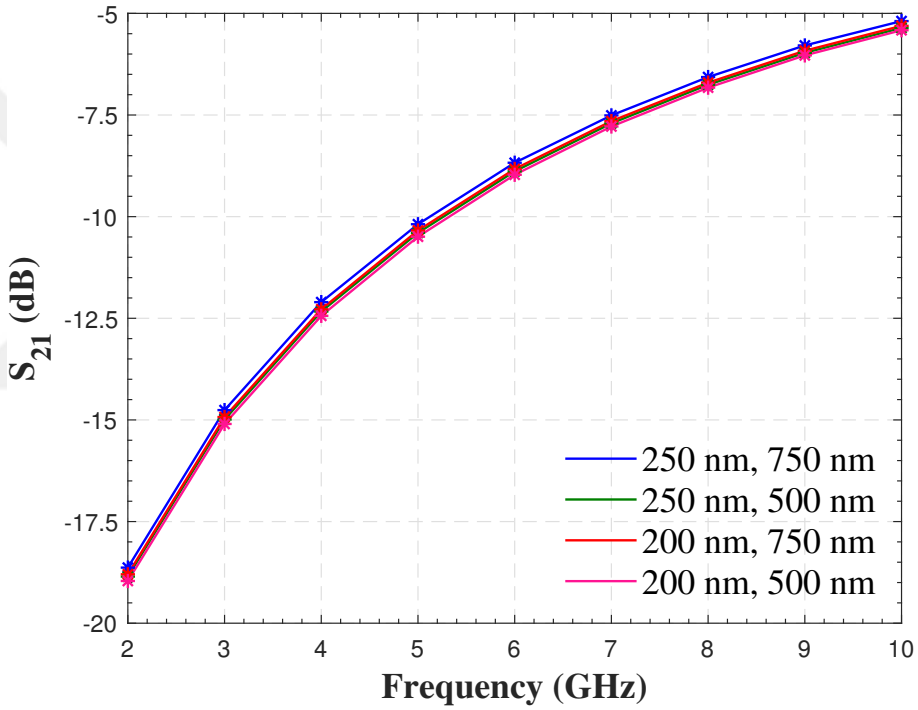


Figure 4.7: S_{21} small signal measurements of OFF-state transistors with different gate shapes (legend shows L_{foot} and L_{head} respectively).

The transistor with 200 nm foot and 500 nm head lengths shows 0.08 pF/mm improvement with respect to the transistor with 250 nm foot and 750 nm head lengths. There are two factors contributing to smaller OFF-state resistance. First, a smaller gate head size results in lower drain-gate and gate-source area and capacitance. The second effect comes from the smaller drain-source capacitance in the OFF-state. For transistors with smaller gate foot length, the charge depleted area beneath the gate shrinks, which leads to a reduction in C_{ds} in Fig. 4.6.

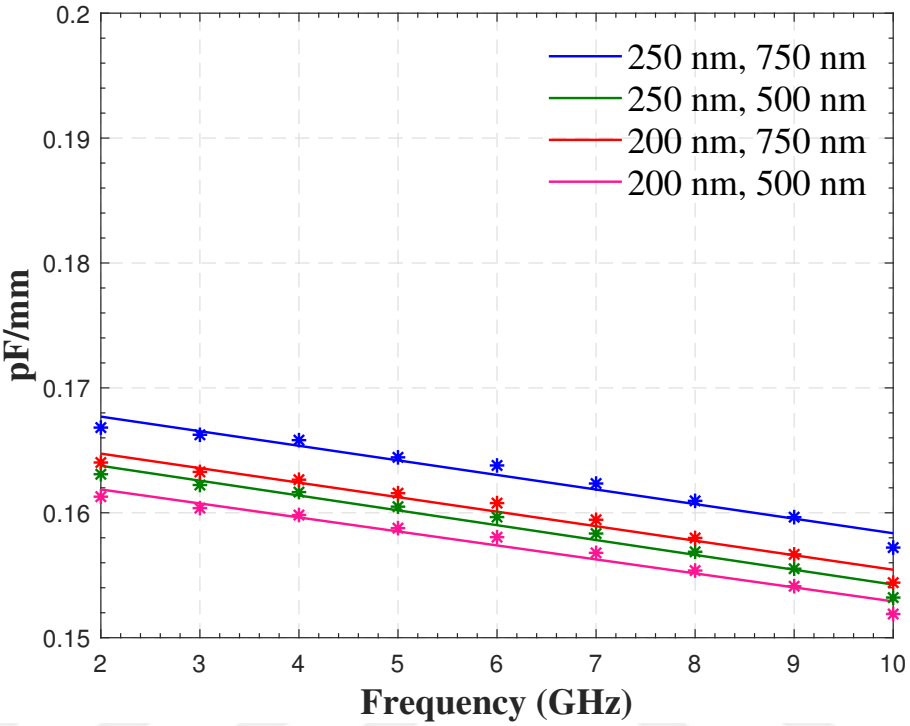
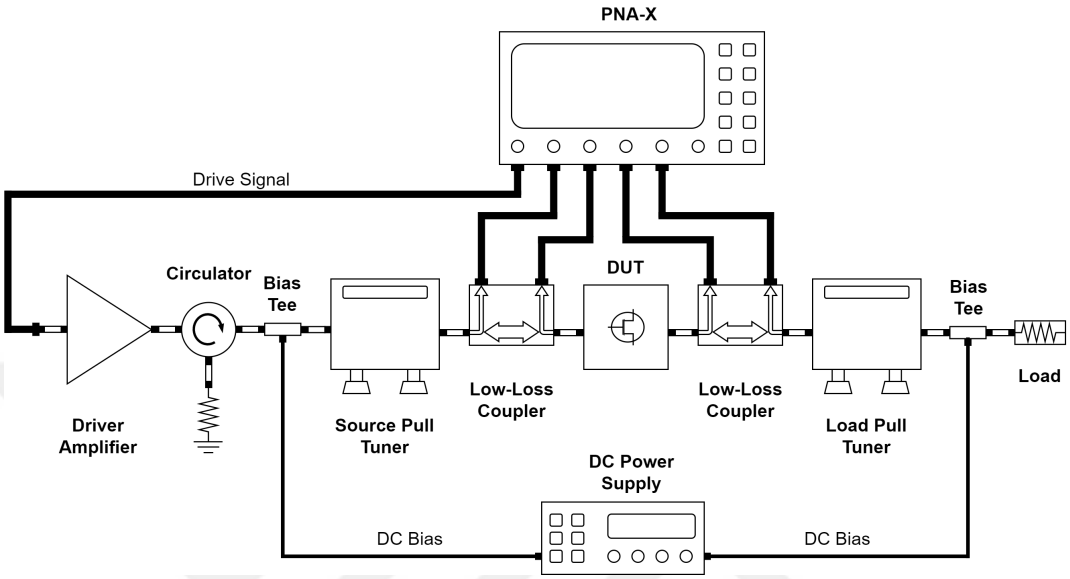


Figure 4.8: OFF-state capacitance values for different gate topologies (legend shows L_{foot} and L_{head} respectively).

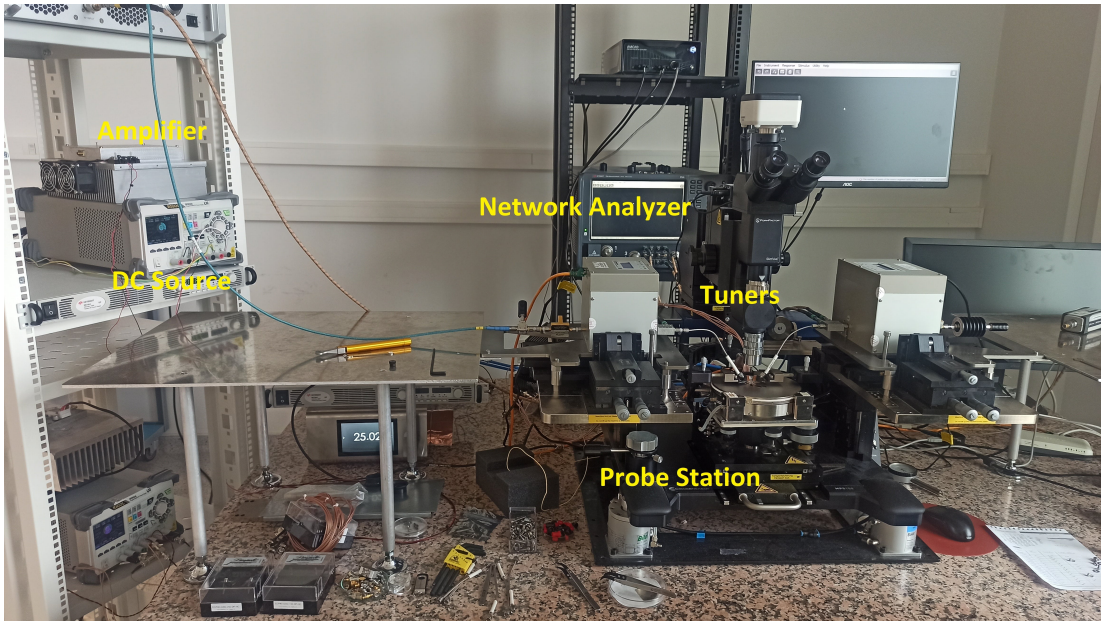
Transistors' small-signal performance is shown to improve with a smaller T-gate dimensions. In the next section, the large-signal performance of the devices will be discussed.

4.2.2 Large-Signal Measurements

The large-signal (load-pull) characterization for switch HEMTs and MMICs is a fundamental method for analyzing their performance at higher power levels. Generally, large-signal measurements are used to characterize transistors for different load and source terminations. These measurement results provide large-signal behavior such as efficiency, gain, or maximum power curves. For switch HEMTs and MMICs, large-signal measurement provides information in maximum power handling capacity without degrading the performance of the device's performance.



(a)



(b)

Figure 4.9: (a) Diagram and (b) photograph of large-signal measurement setup.

In Fig. 4.9, large-signal measurement setup diagram and photograph are shown. Low-loss couplers placed next to DUT is used to sample reflected and transmitted waves. To control the system and measure the sampled waves Keysight PNA vector network analyzer is used as a signal generator and receiver. Source-pull and load-pull tuners are used to calibrate the measurement plane to interested impedance terminations. The DUT is being biased from the DC power supply via bias tees. The circulator placed after the driver amplifier is to protect it from reflected waves. The driver amplifier may be required since the maximum output power of PNA-X is limited. At the end of the measurement setup, a load with high power handling capacity is placed to dissipate generated RF power.

Since the system contains various connection cables, setup components, connectors, and probes, it needs to be calibrated with respect to the measurement plane. AMCAD Engineering's IVCAD measurement software is used to calibrate, analyze and characterize DUT via controlling the presented impedances, delivered and transmitted powers. The calibration needs to be achieved for each frequency of interest and power level.

The switch HEMTs are characterized at $50\,\Omega$ source and load impedance terminations by passive load-pull configuration. The gate control voltages are set to 0 V and -28 V to measure ON-state and OFF-state, respectively, while drain and source voltages are set 0 V. The measurement is repeated for different gate structures. Continuous RF signal and DC voltage are applied during the measurement process. The measurement frequency is set to 10 GHz.

Fig. 4.10 shows ON-state transistor power handling performance. For lower power levels, the transistor is not compressed. Reducing the gate foot and head lengths also leads to early compression of the device [26] compared to devices with larger T-gates and field plates. The reason is that a larger T-gate improves the maximum current handling capacity of switch HEMTs [29].

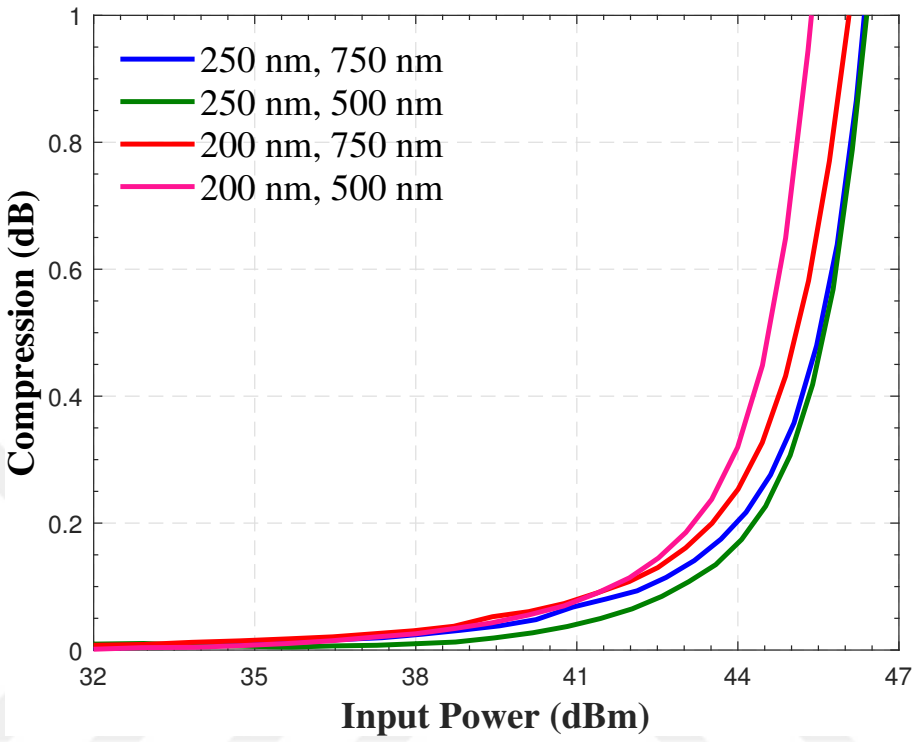


Figure 4.10: Measured ON-state power handling for different gate structures (legend shows L_{foot} and L_{head} respectively).

By analyzing the measurement results, devices with a gate foot length of 200 nm compress 0.1 dB at a 41.5 dBm input power level while devices with a gate foot length of 250 nm compress about 43 dBm for the same setup. This may indicate that small gated transistors perform better in the small-signal region while larger T-gate structures perform better at higher power levels.

In the next measurement, transistors are switched to their OFF-state, and input power is varied up to 43 dBm. The compression of isolation is shown in Fig. 4.11. The compression performance of the switches improves as the T-gate head size is increased to 750 nm. The transistors start to compress earlier for smaller gate heads. Since the purpose of the T-gate is to improve breakdown voltage beneath the gate [29], increasing the gate head length shifts compression to higher power levels.

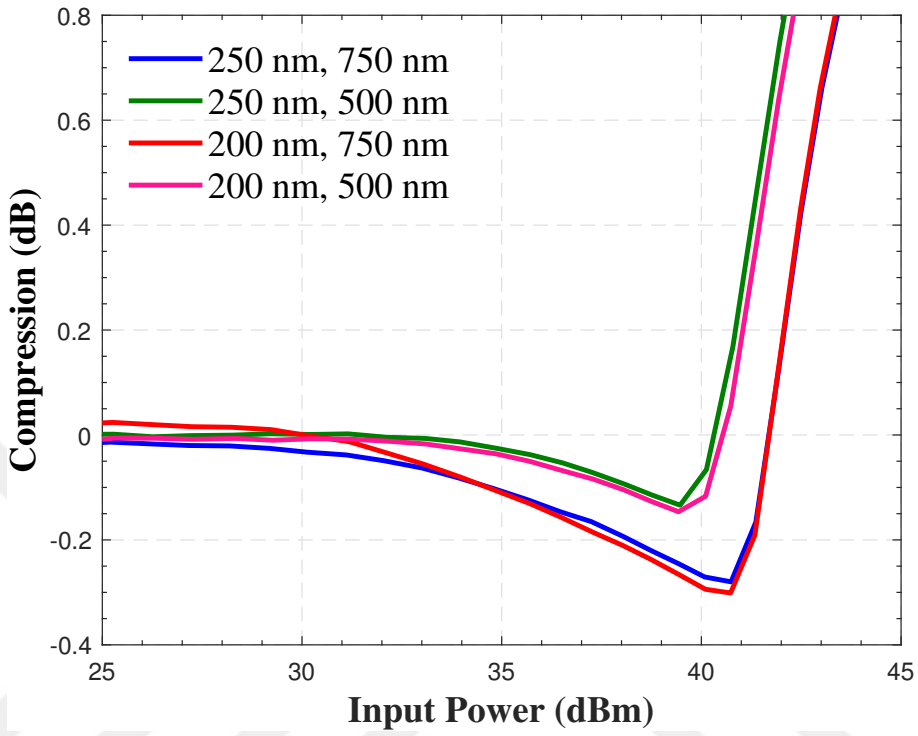
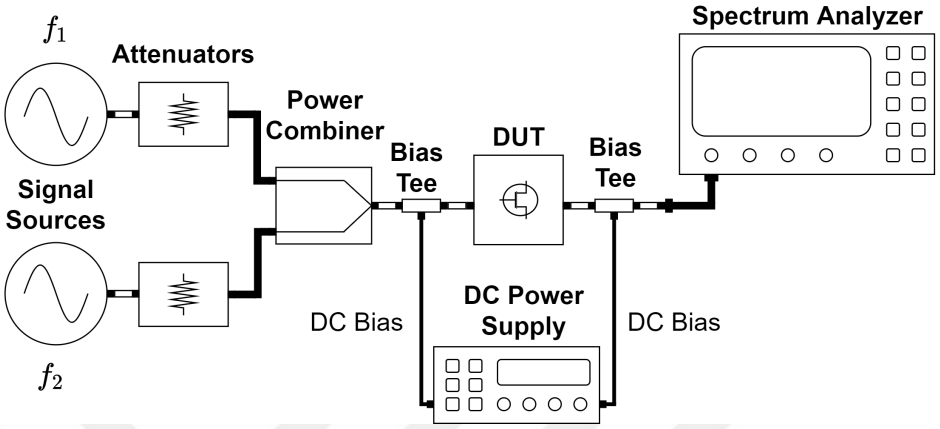


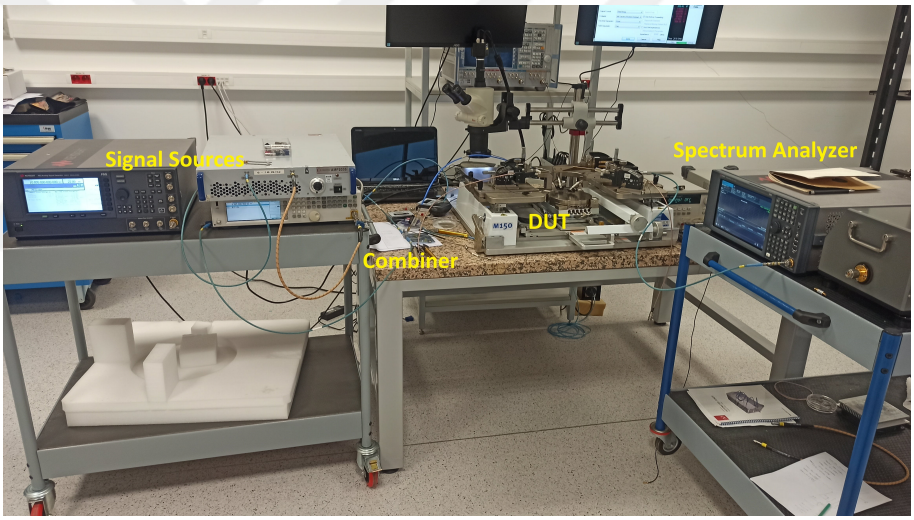
Figure 4.11: Measured OFF-state power handling for different gate structures (legend shows L_{foot} and L_{head} respectively).

4.2.3 IP3 Measurements

The linearity of transistors is characterized by the setup in Fig. 4.12. OIP3 points of each transistor are measured with the given two-tone signal. Signals are generated at frequencies 10 GHz ±5 MHz. In order to isolate signal sources, circulators and attenuators are used at the output ports of signal generators. The transistor gate is biased with 0 V, while the drain and source sides are kept at 0 V as well. The OIP3 is estimated by using the fact that third-order intermodulation components increase 3x while fundamental tone increases by 1x with the given input power.



(a)



(b)

Figure 4.12: (a) Diagram and (b) photograph of IP3 measurement setup.

The measurement results of OIP3 measurements are shown in Fig. 4.13. As it can be seen from the figures, the OIP3 point of the transistors does not affect significantly. OIP3 point of the transistors shows a similar trend with compression behavior. When 750 nm - 250 nm device has 46 dBm of OIP3 point, 500 nm - 200 nm device has 45 dBm of OIP3.

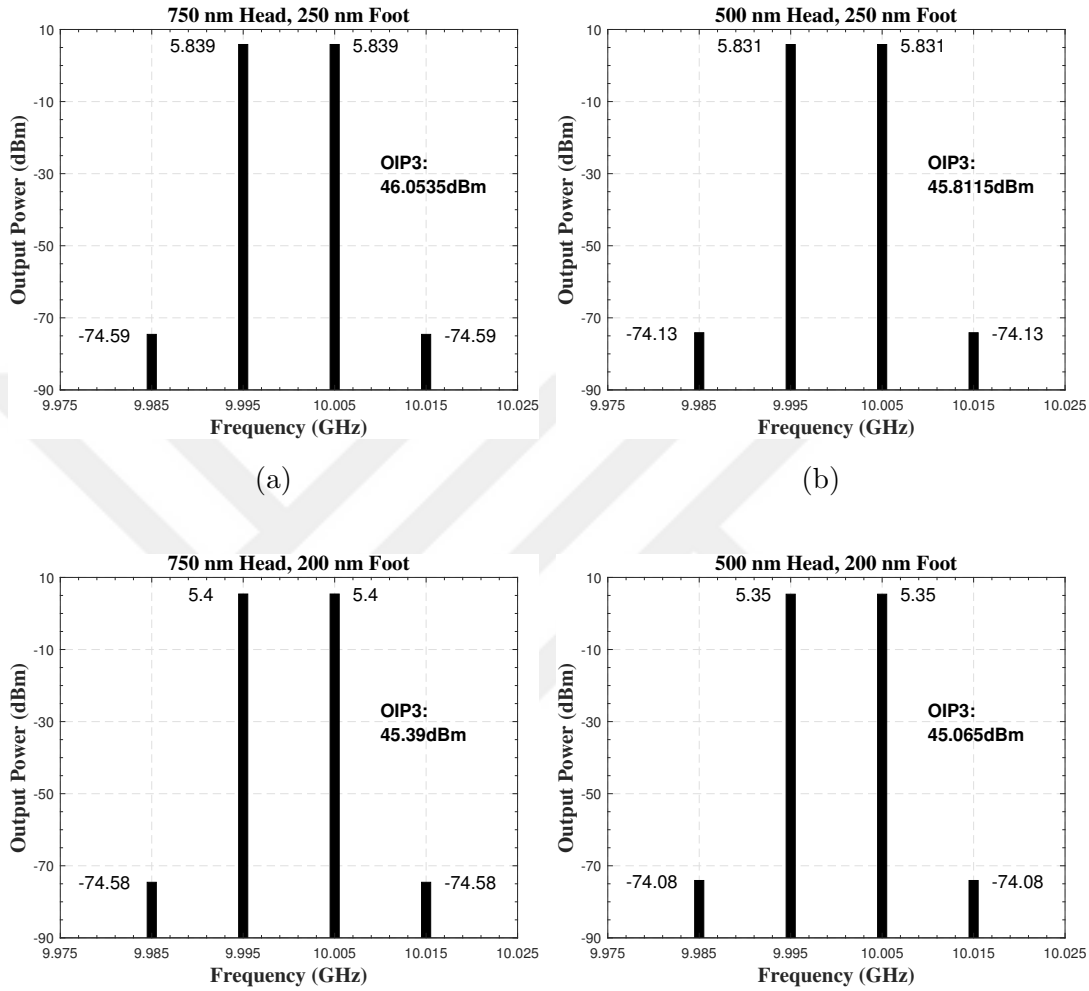


Figure 4.13: OIP3 measurements of (a) 750 nm-250 nm, (b) 500 nm-250 nm, (c) 750 nm-200 nm, and (d) 500 nm-200 nm gate foot and gate head length transistors, respectively.

4.2.4 Transistor Performance Analysis

The transistors in different gate sizes are characterized, and their performance parameters are extracted. Their small-signal, large-signal, and linearity performances were measured. In table 4.1, a summary of measurement results is shown. From measurement results, R_{on} and C_{off} improve as the transistor gate head and

foot shrinks. Therefore, higher performance in the small-signal operation region can be achieved. On the other hand, the power performance of the transistors degrades with smaller gate topologies. Additionally, the linearity of the devices is also affected by the same trend. One of the gate topologies could be preferred over another in different applications.

Table 4.1: Performance summary of HEMT in different gate topologies.

Gate Type	R_{on} (Ω mm)	C_{off} (pF/mm)	FOM (GHz)	P_{1dB} (dBm)	OIP3 (dBm)
250 nm L_{foot} 750 nm L_{head}	2.658	0.163	367	46.39	46.054
250 nm L_{foot} 500 nm L_{head}	2.431	0.161	407	46.37	45.81
200 nm L_{foot} 750 nm L_{head}	2.406	0.1597	414	46.06	45.39
200 nm L_{foot} 500 nm L_{head}	2.116	0.158	476	45.33	45.065

In this thesis, a high-power SPDT switch with a low insertion loss is aimed. Therefore, the transistor with a 500 nm gate head and 250 nm gate foot is chosen for the design. In the next chapter, SPDT design steps, analysis, and characterization of MMIC will be presented.

Chapter 5

SPDT Switch Design and Characterization

In this chapter, SPDT switch design and performance of fabricated switch MMIC using gate-optimized HEMTs will be analyzed. The design procedure is based on the S-parameter and load-pull measurement data of transistors. Simulation of MMICs, designing schematic and layout, small-signal simulations, and EM simulations are completed by using Keysight's Advanced Design System (ADS) software.

5.1 Switch Configurations

Depending on requirements and design choices, an SPDT switch can be implemented in various topologies. HEMTs can be used in two different configurations in those topologies, shunt or series. In Fig. 5.1, switch HEMT configurations are shown.

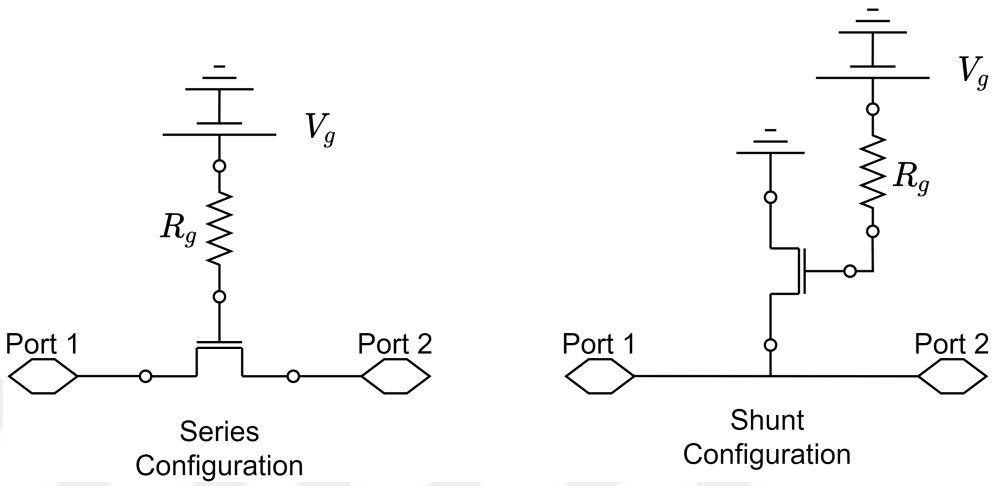


Figure 5.1: Series and shunt switch configurations.

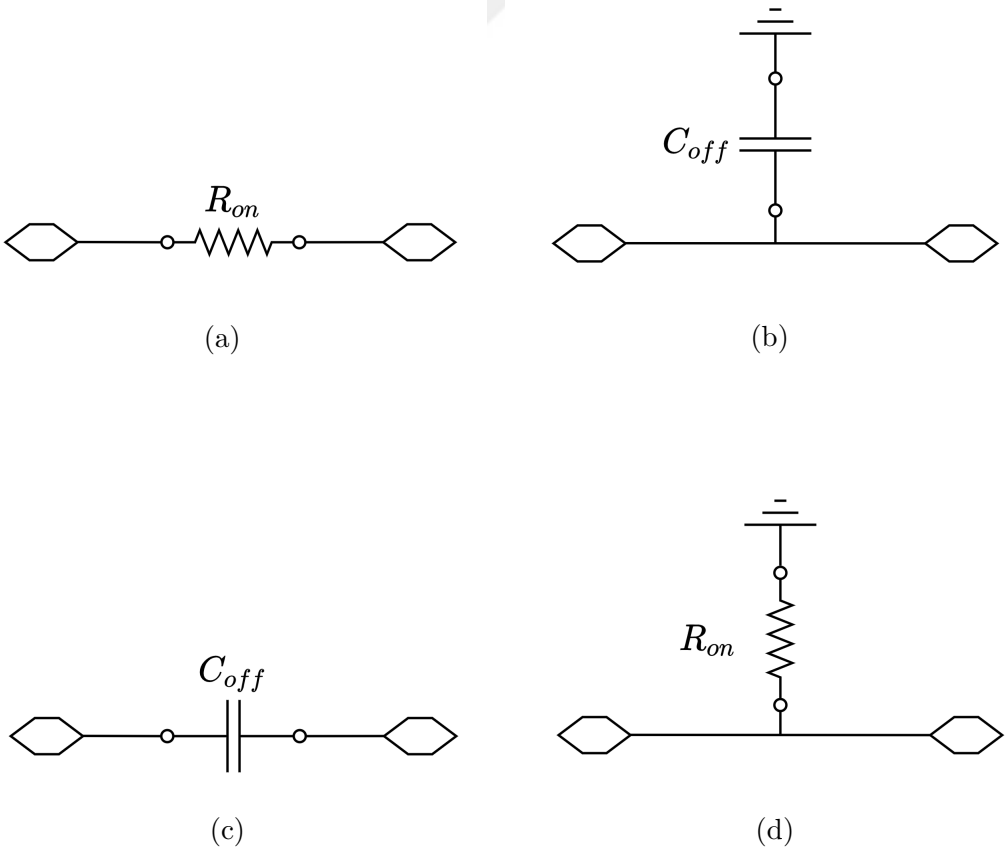


Figure 5.2: (a) Series ON-state, (b) Shunt OFF-state, (c) Series OFF-state, and (d) Shunt ON-state switch configurations.

Transistors can also have either ON or OFF states, as discussed in Chapter 3. Therefore, a switch HEMT can be found in 4 different possible situations. When a gate voltage is above the threshold applied to the gate, the transistor behaves as a low-value resistance. In the series configuration, the signal is transmitted with a small insertion loss while the signal is isolated from Port 1 to Port 2 for the shunt configuration.

When a gate voltage lower than the threshold is applied to the gate, HEMT isolates the signal in the series configuration. Likewise, the signal is transmitted from Port 1 to Port 2 for the shunt configured transistor. In Fig. 5.2, possible switch configurations are shown.

5.2 Effect of Gate Periphery

Devices in different gate peripheries are fabricated to investigate performance variation for different transistor sizes. In Fig. 5.3, switch reticle is shown with 250 µm, 500 µm, 750 µm, 1000 µm, and 1600 µm gate reticle transistors.

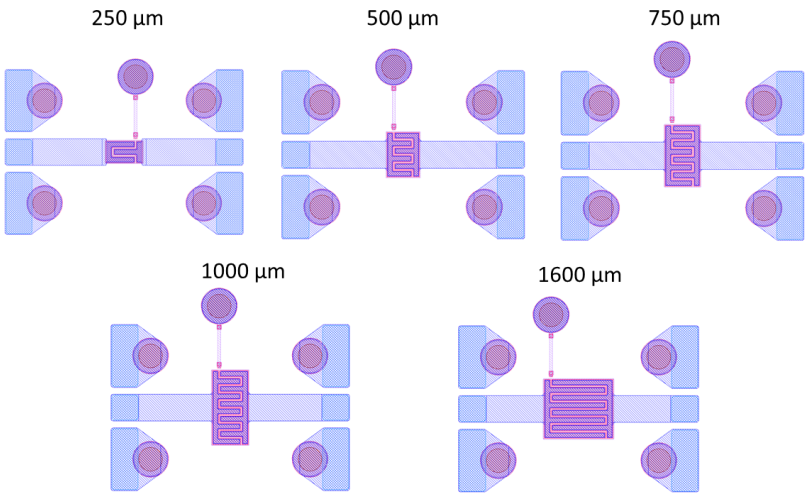


Figure 5.3: Switch HEMT reticle showing transistors in different sizes.

First, transistor gates are biased at 0 V at their ON-states. The small-signal performance of the devices is measured from 2 GHz to 10 GHz. In Fig. 5.4, measured insertion loss of devices is shown. Since the ON-state resistance is inversely proportional to the total gate periphery, larger transistors show better insertion loss.

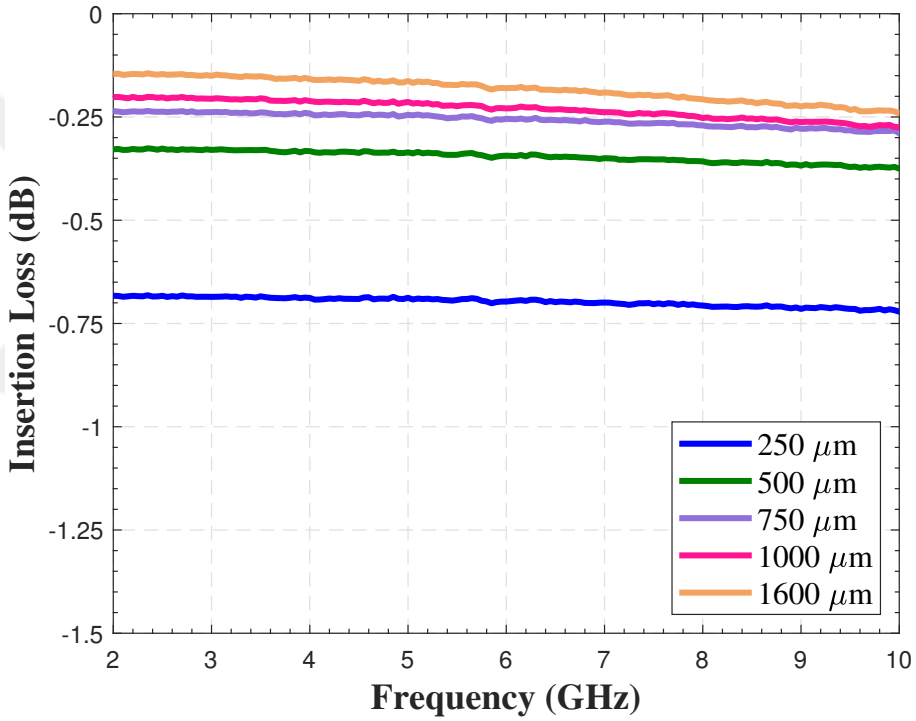


Figure 5.4: Measured ON-state insertion loss of transistors in various gate peripheries.

For their OFF-states, transistors are biased at -28V, and small-signal performance is measured from 2 GHz to 10 GHz. Switches show better isolation performance for small gate peripheries as the OFF-state capacitance is proportional to transistor size. Fig. 5.5 shows the measurement results.

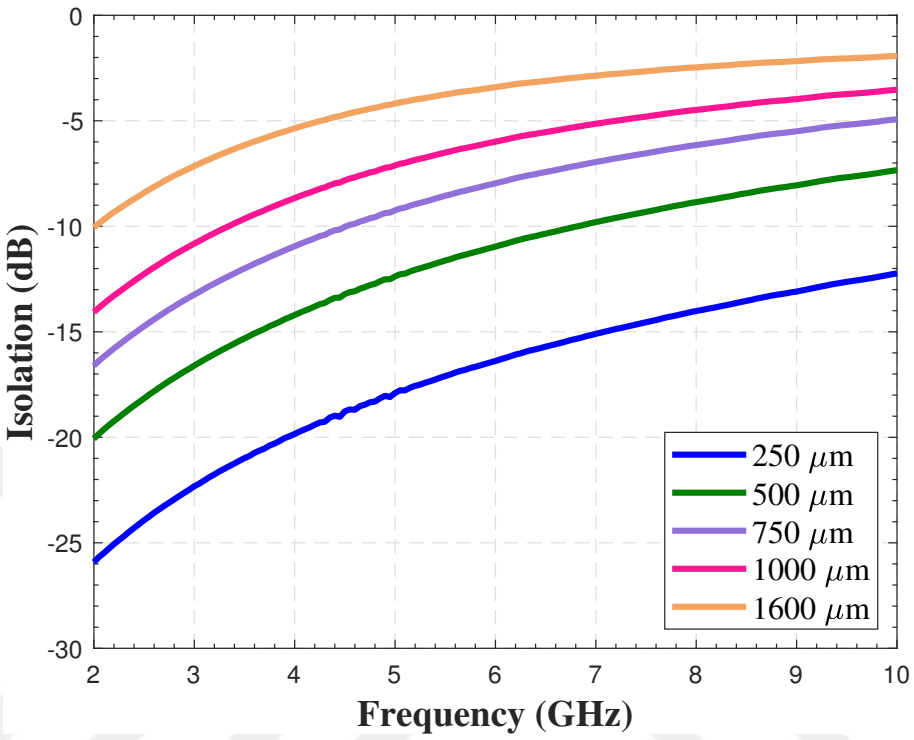


Figure 5.5: Measured OFF-state isolation of transistors in various gate peripheries.

The power handling of switch HEMTs is also characterized by using the large-signal measurement setup. Fig. 5.4 indicates that for larger gate-peripheries, the power handling of transistors increases.

From the characterization results, it can be seen that the transistor periphery determines the switch performance significantly. To design a switch with a higher isolation, smaller HEMTs in the series configuration and larger HEMTs in the shunt configuration should be used. Likewise, the low-loss operation requires larger transistors in the series configuration and smaller transistors in the shunt configuration. While considering the small-signal performance, the device's size should also be taken into consideration for power handling. Increasing the total gate periphery improves the power handling of the design.

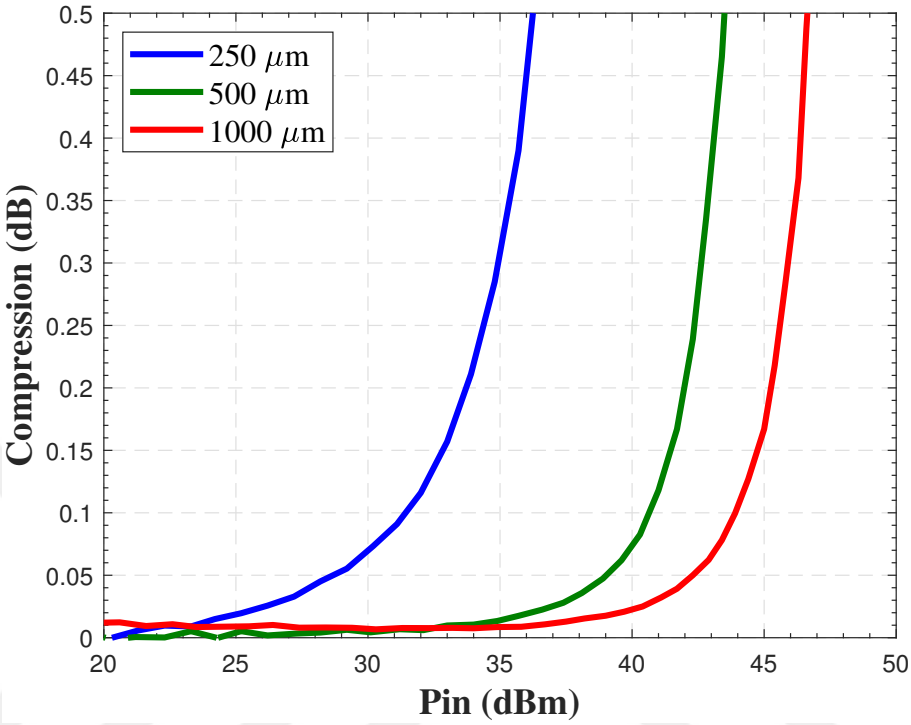
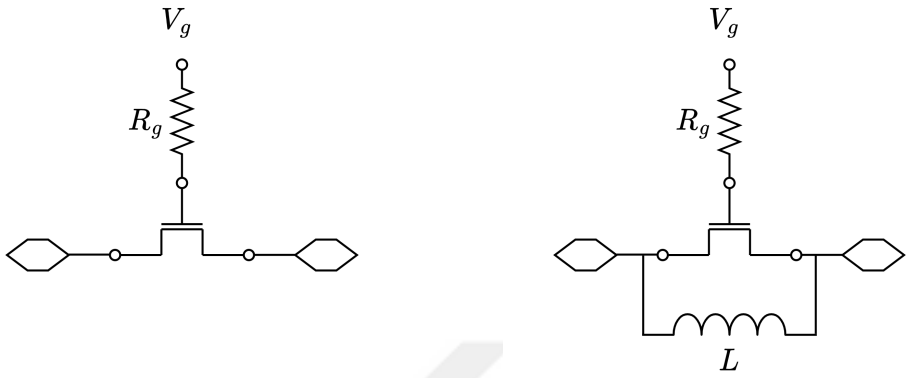


Figure 5.6: Measured power handling of transistors in various gate peripheries.

5.3 SPDT Switch Design

SPDT switch is designed to be asymmetric for low noise and high power modes, separately. Therefore, different switch branches enable designers to optimize the performance separately.

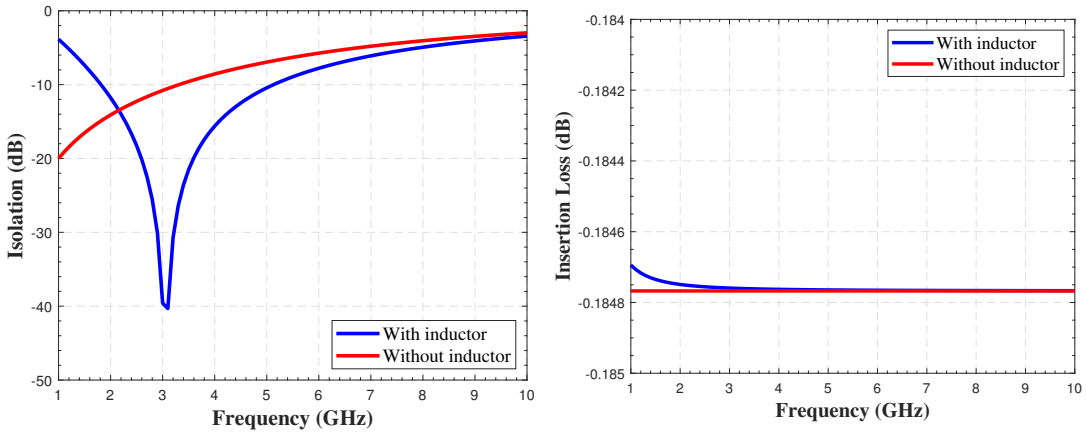
As discussed in the previous chapters, a transistor with larger gate peripheries handles power better. To enhance isolation and power handling of the high power branch, series HEMT is used. However, a series transistor with a large periphery does not isolate the signal good. An inductor placed parallel to the transistor could improve the isolation. To analyze the circuit, an ideal transistor with 0.16 pF/mm C_{off} and 2.15 0.5 Ω mm R_{on} is simulated with 17 nF inductor as in Fig. 5.7.



(a) (b)

Figure 5.7: (a) Single series transistor and (b) transistor with shunt inductor.

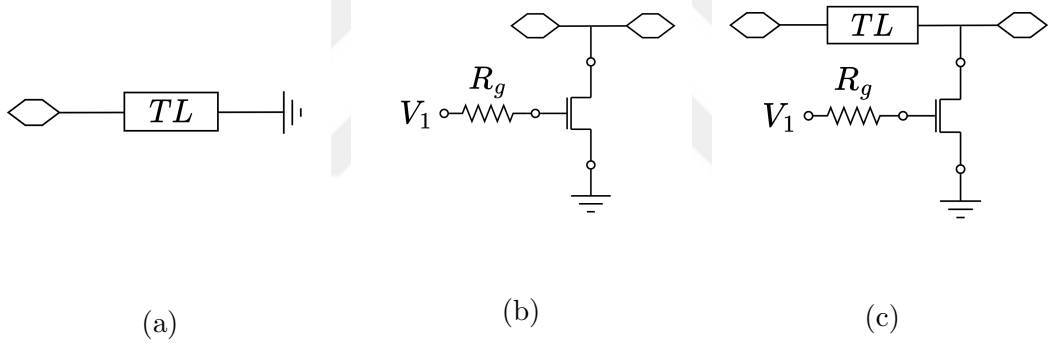
Due to the resonance of the inductor and off-state capacitance of the transistor, isolation is improved for higher frequencies. It does not affect insertion loss due to low on-state resistance. However, resonance frequency should be adjusted carefully to avoid performance loss. The downside of this technique is limiting bandwidth lower frequencies. As show in Fig. 5.8, isolation is improved from 10 dB to 20 dB at 3.5 GHz.



(a) (b)

Figure 5.8: (a) Isolation and (b) insertion loss of single transistor and improved topology.

In GaN MMIC switch design, typically, shunt HEMTs are used with a quarter-wave impedance transformer. A quarter-wave impedance transformer converter an open circuit to a short circuit and a short circuit to an open circuit. The purpose of this configuration is to improve the isolation performance of the switch. Since the switch behaves like a short circuit with a low on-state resistance, isolation of the switch improves by converting the short circuit with an impedance transformer. In Fig. 5.9, three circuit configurations with shunt inductor and impedance transformers are shown.



(a) (b) (c)

Figure 5.9: (a) Short stub quarter-wave impedance transformer,(b) shunt HEMT, and (c) shunt HEMT with quarter-wave impedance transformer.

The impedance seen at the input ports of these three configurations is shown on the smith chart as in Fig. 5.10. A switch HEMT with the gate periphery of 500 µm in shunt configuration behaves like a short circuit. By connecting a 50 Ω $\lambda/4$ transmission line, the closed path impedance is being converted to an open circuit. However, a quarter-wave transmission line limits the bandwidth of the switch, and it occupies a huge area. For broadband applications, different approaches may be required.

For NANOTAM MMIC process, a 50 Ω $\lambda/4$ transmission line has 96 µm width with 8500 µm length at 3.5 GHz. It occupies very valuable chip area which can be minimized with different methodologies.

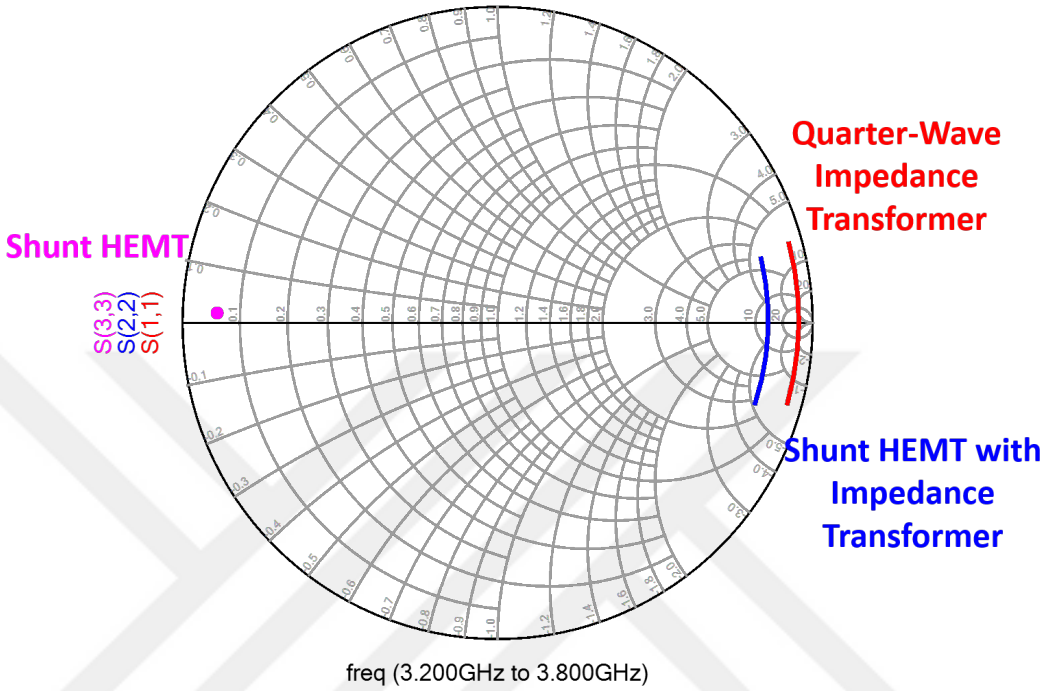


Figure 5.10: S_{11} of shunt HEMT and quarter-wave impedance transformer configurations.

In order to minimize a transmission line length, a shunt capacitor is added to load transmission line as in Fig. 5.12. Instead of using 96 µm width transmission line with a length of 8500 µm, an 80 Ω transmission line with 2600 µm length is placed. Loading capacitance value is 0.9 pF.

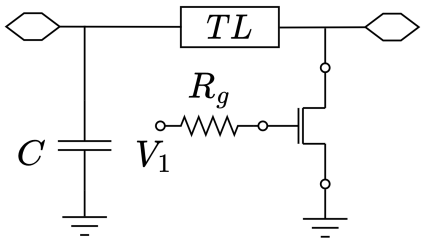


Figure 5.11: Capacitively loaded shunt switch configuration.

In Fig. 5.12, the impedance seen by the closed port is shown on the smith chart. The minimum area occupied by the transmission lines is reduced by a factor of 12.5 compared to a quarter-wave impedance transformer.

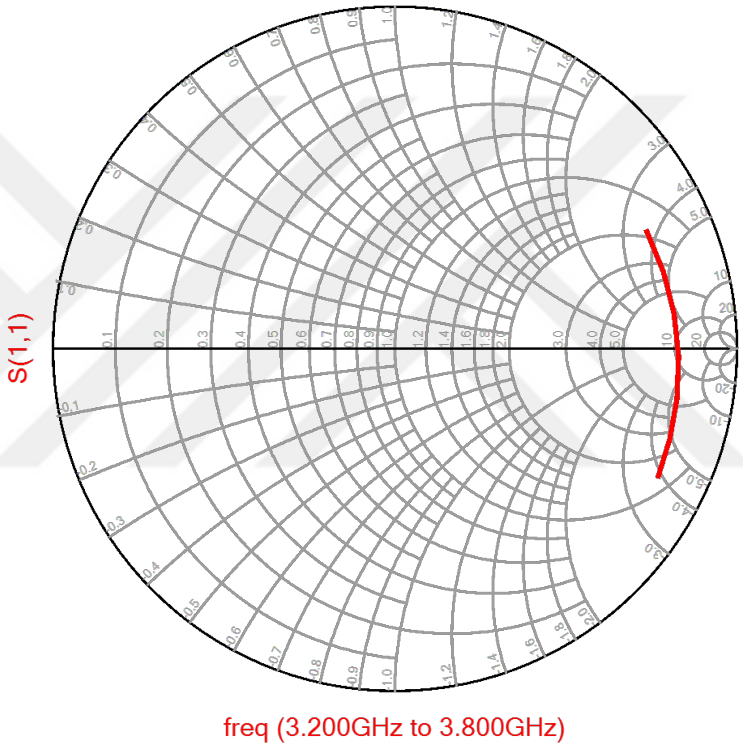


Figure 5.12: S_{11} of capacitively load switch configuration.

Additionally, insertion loss, isolation, power handling, and bandwidth of the switch depend on the number of shunt and series transistors. In order to improve isolation, additional series HEMT may be added with a higher insertion loss. Likewise, a larger periphery HEMT shows better power handling; however, it provides smaller isolation. In the light of those design parameters, an SPDT switch with the topology given in Fig. 5.13. The switch is designed to be asymmetric for low-noise and high-power paths.

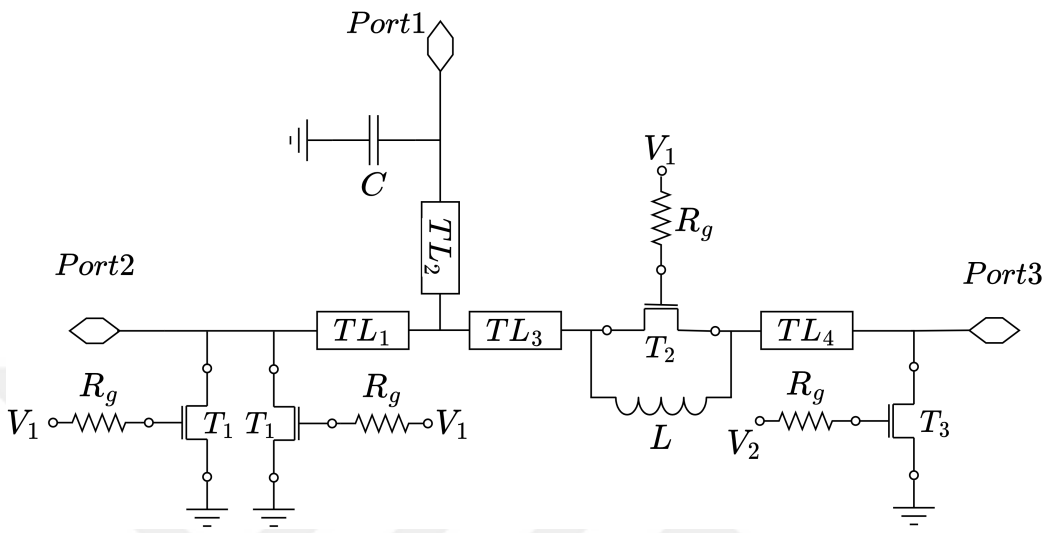


Figure 5.13: Circuit schematic of MMIC SPDT switch.

Transistors with 500 nm gate head and 250 nm gate foot lengths are used for asymmetric SPDT switch. For the high-power path, a series transistor with 1600 µm gate periphery is placed, which can handle power levels above 40W. Since it has comparatively large off-state resistance, an inductor value of 1.2 nH is connected in parallel to the transistor. For further enhancement of the isolation, a shunt HEMT with 750 µm gate periphery is used. For the low-noise branch, two 500 µm transistors are chosen to provide low insertion loss and enough isolation. At the input port, a capacitance value of 1.2 pF is used in shunt configuration to match the circuit. Characteristic impedances of TL_1, TL_2, TL_3, and TL_4 are 80 Ω, 55 Ω, 45 Ω, and 45 Ω, respectively. Electrical length of transmission lines at 3.5 GHz are 27.5°, 2.5°, 17°, and 17.5°, respectively. The gate resistors of the switches are chosen to 3.6 kΩ. The design parameters are tuned to have the optimum performance values inside the minimum chip area. The total chip area, including biasing pads, is 2.2 mm x 2 mm. The gates of transistors are controlled by 0 V and -28 V. The frequency bandwidth of the SPDT switch is from 3.2 GHz to 3.8 GHz, which is a widely used spectrum for 5G communication modules. A fabricated MMIC microscope image is shown in Fig. 5.14. In the following section, simulation and measurement results of the design SPDT switch are presented.

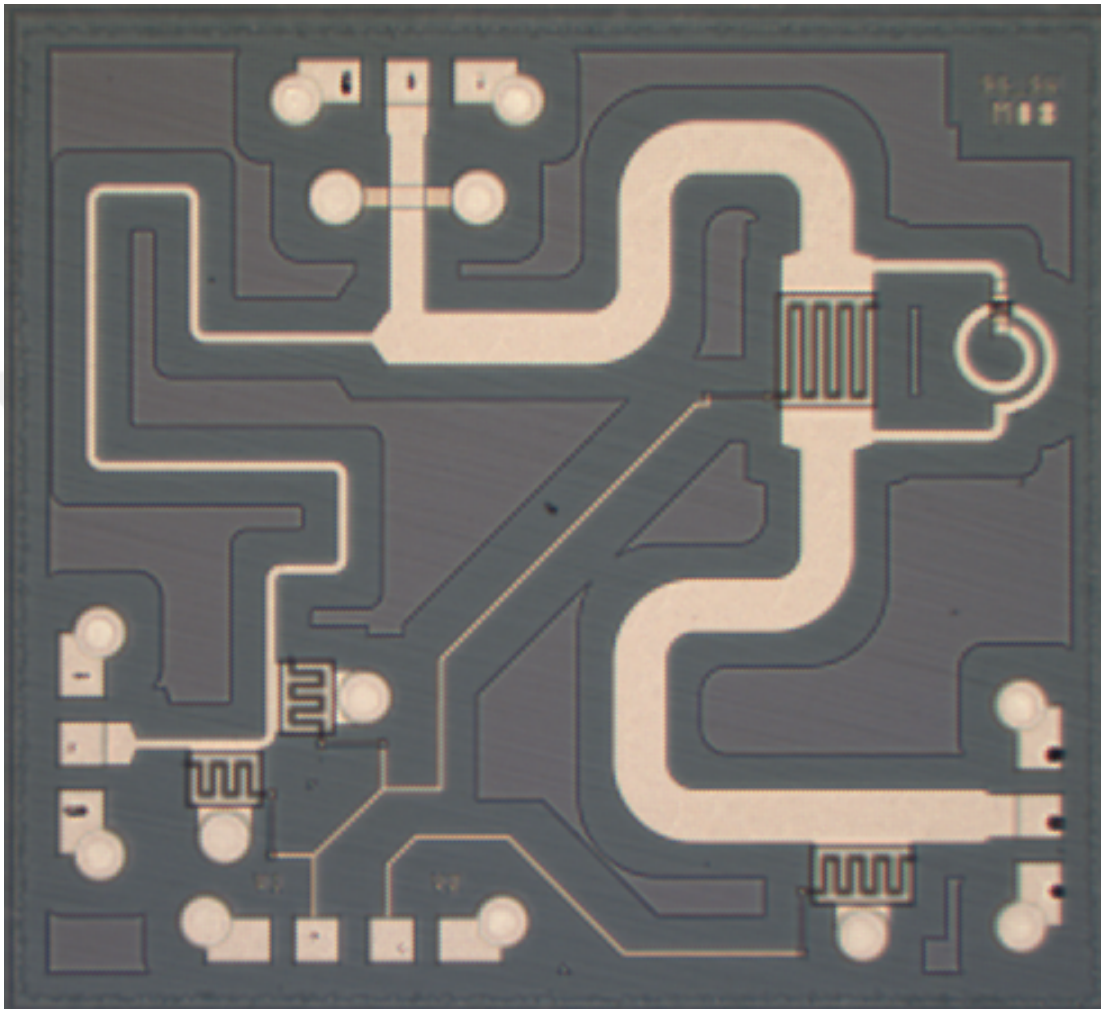


Figure 5.14: Microscope image of MMIC SPDT switch.

5.4 Simulation and Measurement Results

Simulation of the design is achieved by using ADS software using the fabricated transistor data. First, transistors are measured in small-signal and large-signal characterization setups, and measurement pads are de-embedded using the ADS. After characterizing the circuit behavior with switch cores, SPDT MMIC was sent to fabrication. In this section, SPDT switch simulation and measurement results are presented.

5.4.1 Small-Signal Measurement

SPDT switch is characterized by its return loss, insertion loss, and isolation for its high power and low noise paths. Both high-power and low-noise paths show an insertion loss performance below 0.85 dB. Towards the lower frequency end, insertion loss reaches 0.7 dB for the low-noise path. Although there is a small variation between simulation and measurement, which is related to fabrication variation, the measurement result agrees with the simulation. In Fig 5.15, insertion loss for both branches is shown.

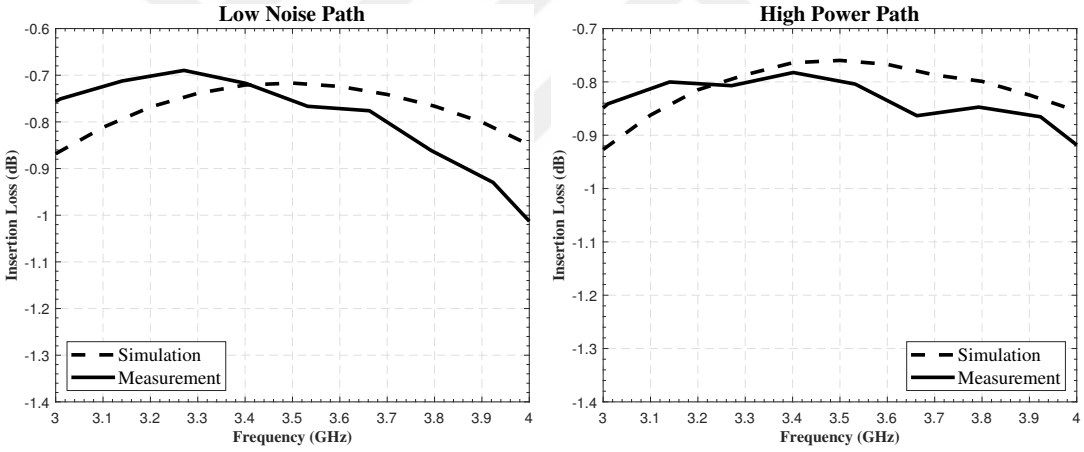
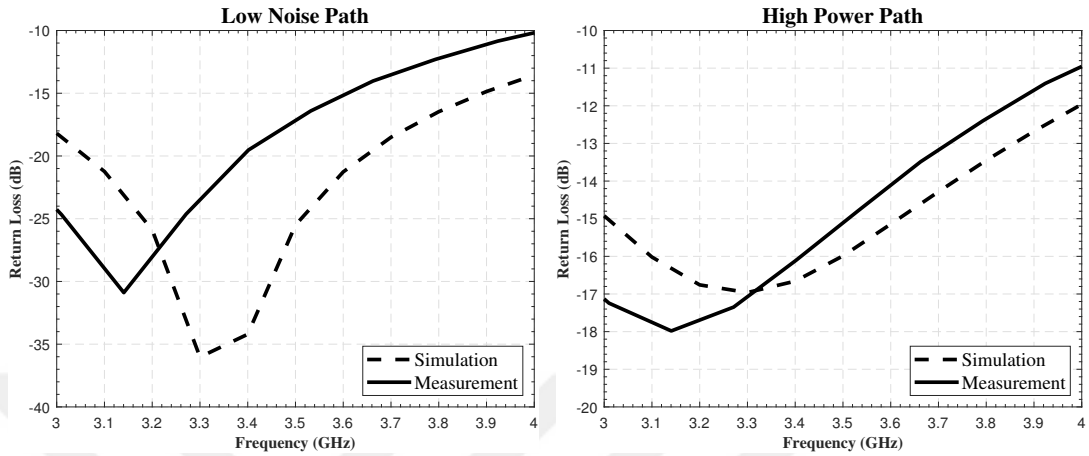


Figure 5.15: Measured and simulated insertion loss of (a) low noise path and (b) high power path.

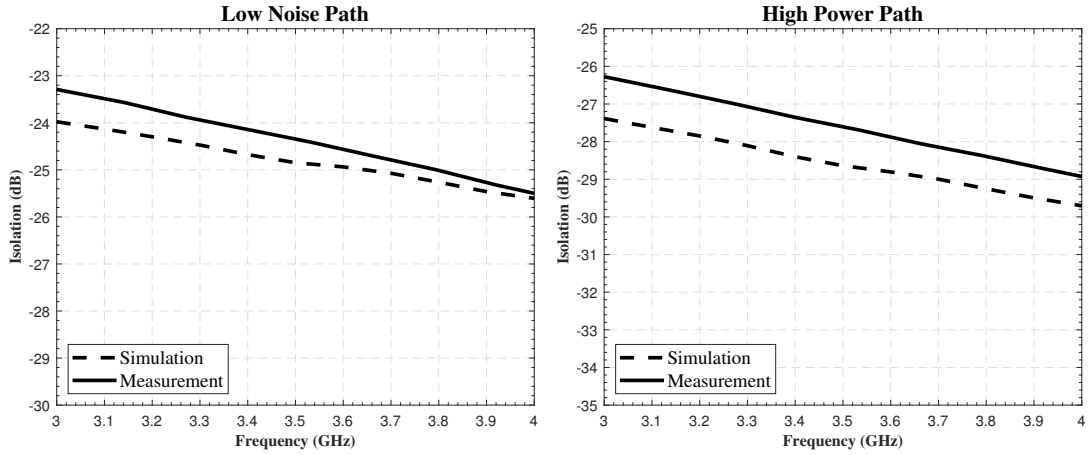
The return loss of the SPDT switch is designed to be lower than 12 dB throughout the bandwidth. For both branches, good return loss is achieved for fabricated MMICs. The return loss of the low-noise path even reaches 25 dB at 3.2 GHz. In Fig 5.15, measured and simulated return losses for both branches are shown.



(a) (b)

Figure 5.16: Measured and simulated return loss of (a) low noise path and (b) high power path.

Measured and simulated isolation of the SPDT switch is shown in Fig. 5.17. Measurement results showed that low-noise and high-power paths are isolated from each other by 23 dB and 27 dB. Especially low-noise path isolation is important to protect the input stage of LNA from high-power generated by PA.



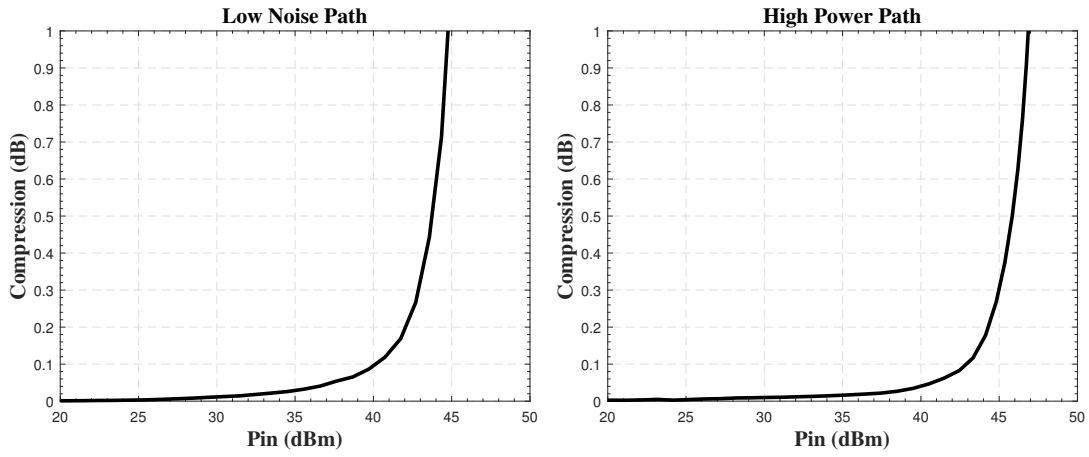
(a) (b)

Figure 5.17: Measured and simulated isolation of (a) low noise path and (b) high power path.

5.4.2 Large-Signal Measurement

Simulation of large-signal analysis couldn't be done due to the lack of a large-signal model. Power handling of the SPDT switch was measured at 3.5 GHz frequency. CW signal is supplied to the input port of the SPDT while the environment is kept at room temperature. In order to protect the device, the compression limit was set to 1 dB compared to the small-signal operation region. Fig.↓ 5.18 shows the large-signal measurement result. The input and output port is set to 50 Ω, and the input power is swept up to 45 dBm for the low-noise path and 47 dBm for the high-power path. The gates of the off-state transistor are biased with -28 V, while the gates of on-state transistors are biased with 0 V.

At 0.1 dB compression level ($P_{0.1dB}$), the low-noise path input power level is 10 W, and the high-power path input power level is 20 W. At 1 dB compression level (P_{1dB}), the low-noise path input power level is 30 W, and the high-power path input power level is 50 W. At this compression point, the switch is able to output more than 40 W of RF power.

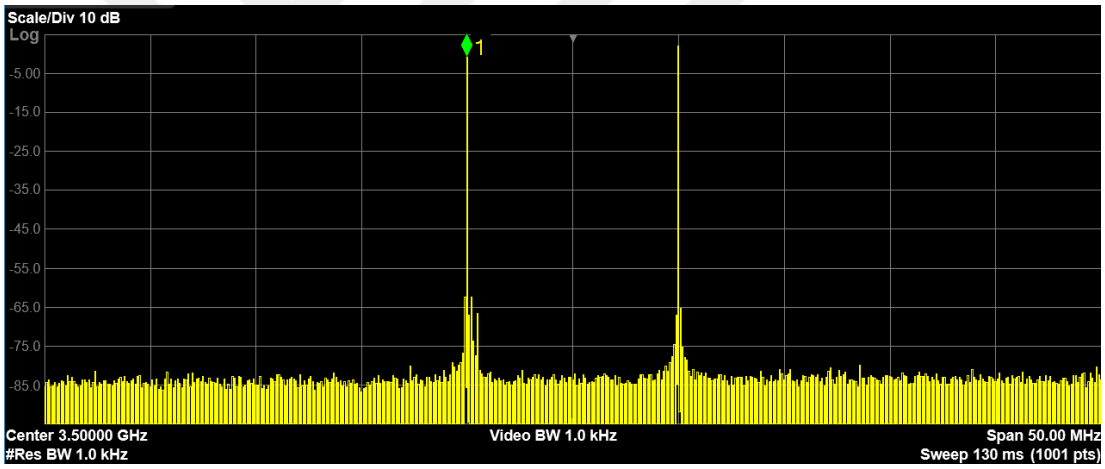


(a) (b)

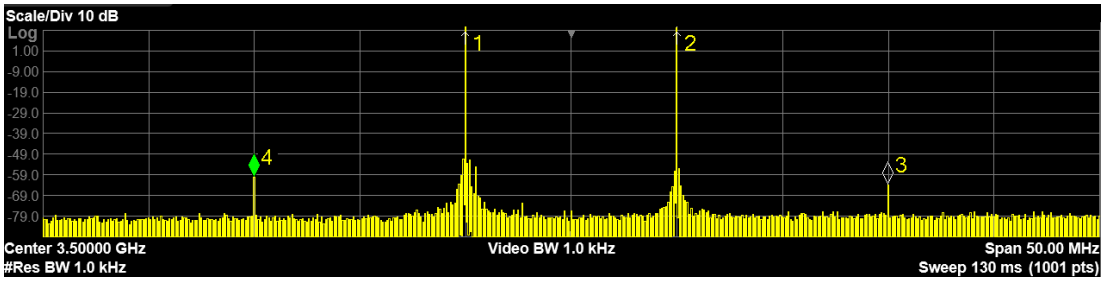
Figure 5.18: Measured power handling of (a) low noise path and (b) high power path.

5.4.3 OIP3 Measurements

OIP3 measurements of the SPDT switch are measured by using the measurement setup defined in Chapter 4. Two-tone signal sources with a center frequency of 3.5 GHz and frequency spacing of 10 MHz. Fig. 5.19 shows the output spectrum of measurement setup with and without the SPDT switch. High-power and low-noise paths are characterized by controlling the gates of transistors with 0 V and -28 V.



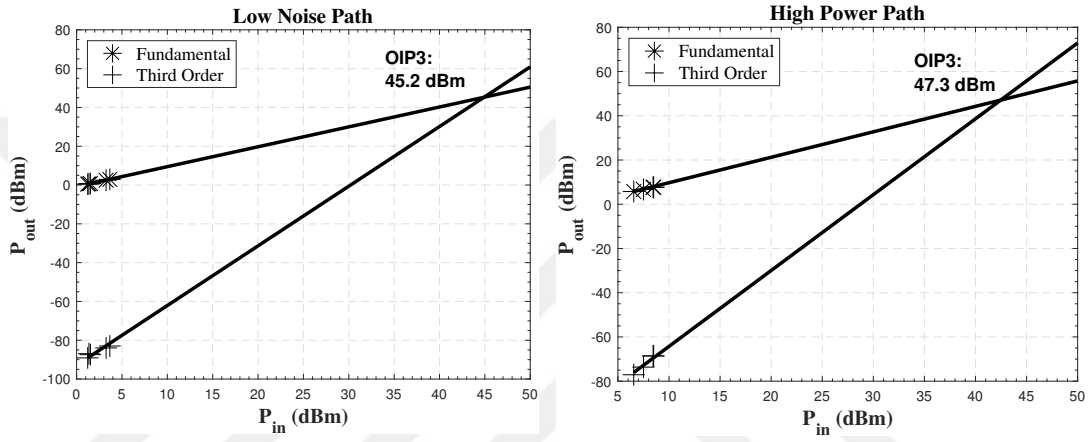
(a)



(b)

Figure 5.19: Output spectrum (a) without the SPDT switch and (b) with the SPDT switch.

Fig. 5.20 shows the extrapolated harmonic and fundamental power levels by using measured data. The low-noise path has an OIP3 of 45.2 dBm, while the high-power path has an OIP3 point of 47.3 dBm.



(a) (b)

Figure 5.20: Measured OIP3 points of (a) low noise path and (b) high power paths.

5.4.4 Switching Speed Measurement

The switching speed measurement setup consists of a signal generator, a pulse generator, detector, and oscilloscope. An input signal is given from Port 1 of the SPDT switch with the generator. DC control voltages of the SPDT switch are stimulated with a pulse from the pulse generator. The output power of the switch is measured with a square-law detector that converts RF power to DC voltage. The pulsed voltage and detector voltage are connected to the oscilloscope to observe switching behavior in the time domain. Fig. 5.21 shows the switching time measurement setup.

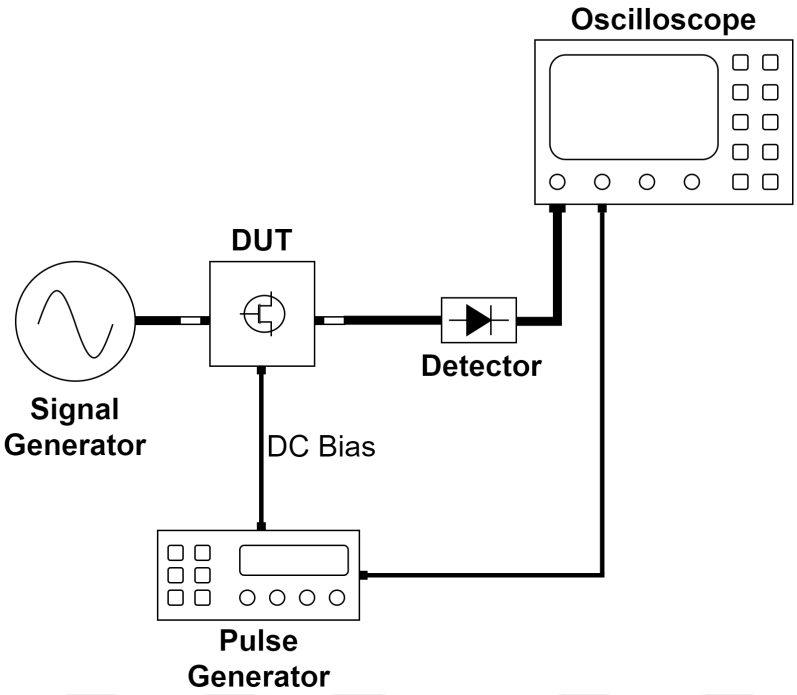
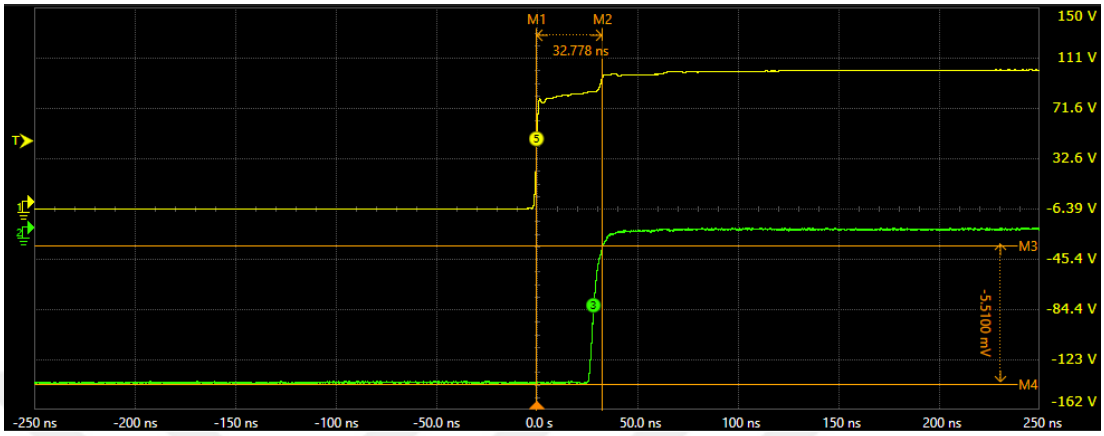
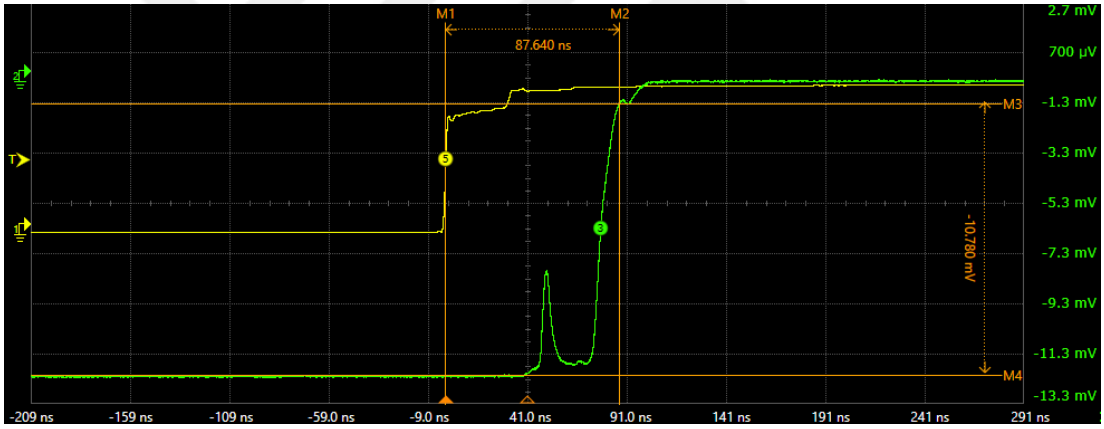


Figure 5.21: Switching time measurement setup.

ON time is characterized from 50% level of the input signal to 90% of the detector voltage, and OFF time is characterized from 50% level of the input signal to 10% of the detector voltage. However, direct measurement can't be applied due to system delays. The turn-on and turn-off delay is characterized by the direct measurement of pulsed signal and detector signal without the SPDT switch. Turn-on and turn-off delays are 32.78 ns and 80.6 ns, respectively. Dominating delay of the system is turning on of high-power path. In Fig. 5.22, the delay of the system is characterized as 54.8 ns. The switching times are measured by applying -28 V to 0 V pulses.



(a)



(b)

Figure 5.22: (a) System delay and (b) SPDT MMIC delay measurement results.

Chapter 6

Conclusion and Future Work

RF switches are one of the fundamental components of modern communication systems which is able to change the direction of signal flow. For 5G T/R modules, high-performing switches with low insertion loss and high power handling capacity are required to handle high PAPR waveforms. Due to its thermal and electrical characteristics, GaN on SiC HEMT is a promising technology for high-power MMIC applications.

For high-performance SPDT switches, different circuit topologies are available for design options. However, in every topology, the performance of switch is limited by transistor performance. In this study, the performance of the switch HEMTs is investigated in different gate topologies. The foot length of the gate is varied from 200 nm to 250 nm, and the head length is varied from 500 nm to 750 nm. Using the gate-optimized transistors, the SPDT switch is designed, fabricated, and characterized with NANOTAM's AlGaN/GaN HEMT on SiC process.

Fabricated switch transistors are characterized by their small-signal, large-signal, and linearity performances. It has been shown that as the foot length and the head length of the gate get smaller, on-state resistance and off-state capacitance reduces. HEMT with 250 nm L_{foot}, 750 L_{foot}, and 750 µm gate

periphery has a FOM of 367 GHz and P_{1dB} of 46.39 dBm, while HEMT with 200 nm L_{foot}, 500 L_{foot} has a FOM of 476 GHz and P_{1dB} of 45.33 dBm. Their linearity performance is also showing the same trend. The OIP3 point of the 250 nm - 750 nm switch is 46 dBm, while 200 nm - 500 nm switch has an OIP3 of 45 dBm.

This thesis proposes switch gate topology as a design parameter in GaN MMIC switch design. Depending on the application, L_{foot} and L_{head} can be engineered for optimum performance. For high power handling and low insertion loss, 250 nm L_{foot} and 500 L_{head} gate topology has been chosen for SPDT MMIC switch design.

An asymmetric SPDT switch is designed with two different branches optimized to be used in T/R modules. The bandwidth of operation is from 3.2 GHz to 3.8 GHz. The low-noise path has an insertion loss of 0.85 dB and 23 dB isolation, while the high-power operation has an insertion loss of 0.85 and 27 dB isolation. The return loss of both paths is better than 12 dB. At P_{1dB} point, the low-noise path can handle 30 W, and the high-power path can handle an input power level of 50 W. At this compression point, the switch is able to output more than 40 W in CW operation. OIP3 of the two branches are 45.2 dBm and 47.3 dBm for low-noise and high-power paths, respectively. The switching time is measured as 54.8 ns.

As future works, SPDT switch performance will be improved with different topologies. Especially the isolation performance of the low-noise path will be improved for more reliable T/R modules. Also, the gate-topology optimization technique will be applied to higher frequencies, especially for *Ka*-Band 5G systems. Optimization of the gate structures will be further supported by technology computer-aided design programs. Furthermore, Doherty PA and LNA at *S*-Band will be designed to complete a 5G front-end module.

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