

S-BAND GAN HIGH POWER AMPLIFIER DESIGN AND IMPLEMENTATION

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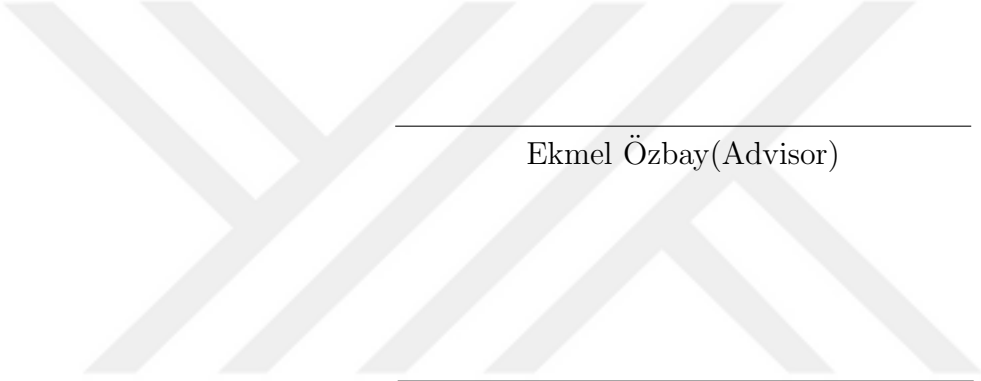
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February 2019

S-Band GaN High Power Amplifier Design and Implementation

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February 2019

We certify that we have read this thesis and that in our opinion it is fully adequate,
in scope and in quality, as a thesis for the degree of Master of Science.



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ABSTRACT

S-BAND GAN HIGH POWER AMPLIFIER DESIGN AND IMPLEMENTATION

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M.S. in Electrical and Electronics Engineering

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High power RF Microwave amplifiers are becoming more important as the telecommunications, defense and aerospace industries' demands develop. GaN on SiC technology offers higher power and better form factors for these applications compared to GaAs. In addition, SiC provides better mechanical properties and thermal performance.

Design, manufacturing and measurements of a S-Band Power Amplifier by using a GaN discrete bare die transistor are presented. GaN on SiC technology, fabrication process, amplifier fundamentals and design steps are explained in detail. PCB laminate properties, manufacturing, wire bonding and importance of heat management are explained. Design, tapeout, characterization of a fabricated HEMT and its packaging are also mentioned. Power amplifier's small-signal gain of 14.5 dB is measured at center frequency. 41.5 dBm RF power at P6dB is measured at 200 μ s pulse width 10% duty cycle at 3 GHz, reaching a power density of 5.4 W/mm. Small-signal gain, IP3 measurements under different biases, AM-AM and AM-PM distortions are also investigated in detail. EM simulations are performed in Keysight ADS design environment. Amplifier design is based on small-signal and loadpull measurements. De-embedding of fixture effects during HEMT characterization and their models are also investigated.

Another hybrid amplifier design by using a packaged commercial GaN on SiC bare die power HEMT is also presented. Small-signal and power measurements are also offered.

Keywords: GaN, Power Amplifier, Microstrip, Hybrid, S-Band, Characterization.

ÖZET

S-BANT GALYUM NİTRÜR YÜKSEK GÜÇLÜ YÜKSELTEÇ TASARIMI VE UYGULAMASI

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Telekomünikasyon, savunma ve uzay sektörlerindeki gelişmeler, Yüksek Güçlü Radyo Frekans Mikrodalga Güç Yükselteçlerinin önemini artırıyor. Silisyum Karbür üstünde Galyum Nitrür teknolojisi, Galyum Arsenit teknolojisi ile karşılaştırıldığında, bu alanda daha yüksek güç ve daha iyi form faktörlerini imkanı kılıyor. Ayrıca, Silisyum Karbür sayesinde aygıtların ısı ve mukavemet yönünden başarısı da yükseliyor.

Ayrık Galyum Nitrür Yüksek Elektron Hareketlilikli Transistor kullanarak, bir S-Bant Güç Yükselteçi yapıldı. Bu yükselteğin tasarım, üretim ve ölçüm sonuçları verildi. Silisyum Karbür üstüne Galyum Nitrür işlemleri, yükselteç temel teorisi, tasarım aşamaları incelendi. Baskı devrenin laminat özellikleri, üretimi, altın tel bağlama ve soğutucu gerekliliği açıklandı. Bir Yüksek Elektron Hareketlilikli Transistorün tasarımı, maskelendirmesi, karakterizasyonu ve paketlenmesinden bahsedildi. Merkez frekansta, 14.5 dB küçük işaret kazancı ölçüldü. 3 GHz'te 200 µs 10% RF atımı ile, 6 dB kazanç sıkışması altında 41.5 dBm çıkış gücü, boyutsal performans olarak ise 5.4 W/mm olarak ölçüldü. Farklı gerilim altında, küçük işaret ölçümleri, üçüncü derece iç çarpım harmonikleri, genlik-genlik ve genlik-faz bozulmaları da ölçüldü. Elektromanyetik simülasyonlar Keysight ADS tasarım ortamında tamamlandı. Galyum Nitrür Yüksek Elektron Hareketlilikli Transistorü ise küçük sinyal ölçümleri ve loadpull ölçümleri ile karakterize edildi.

Bir başka hibrit yükselteç tasarımı da pisayada bulunabilen bir ayrık Galyum Nitrür Yüksek Elektron Hareketlilikli Transistorü kullanarak yapıldı. Küçük işaret ve güç ölçümleri sunuldu.

Anahtar sözcükler: Galyum Nitrür, Güç Yükselteci, Microstrip, Hibrid, S-Bant, Karakterizasyon.

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Chapter 1

Introduction

In this work, we have empirically characterized a 2.5 mm GaN HEMT built by NANOTAM's 0.25 μm GaN on SiC process and successfully built a hybrid amplifier. Results for another hybrid amplifier built with a commercial transistor are also offered.

For the matching circuit, a Rogers 4003C laminate was chosen for its good RF and mechanical specifications. Amplifier topology is a single stage common source amplifier with microstrip transmission lines. S-parameter measurements and loadpull characterization have been conducted for different bias points. Schematic design, layout and full EM simulations are done in Keysight ADS design environment.

Output powers over 13 W have been measured at the centre frequency 3 GHz. A small-signal gain greater than 14.5 dB has been measured. A complete characterization of the amplifier performance is provided with third order intercept point, AM/PM distortion, efficiency and compression characteristics under different bias points.

1.1 RF Microwave Power Amplifiers

RF Microwave Power amplifiers convert DC power into high microwave power according to input waveform. Apropos, a microwave power amplifier aims to deliver maximum power output for a proposed active device [1], usually a transistor for solid state technology. These devices are utilized in many different applications such as environmental radar, radar systems, network and wireless communication systems [2]. Ever continuous growth in these areas increase the demand for amplifiers with higher power output and efficiency. Historically and currently, travelling wave tube amplifiers (TWTAs) have been used in areas where high power output is needed. Developments in solid state technologies such as Silicon and Gallium Arsenide have begun a shift towards solid state power amplifiers [3]. Since the 90s, advances in materials such as Gallium Arsenide (GaAs) and Gallium Nitride (GaN) have led the development of High-electron-mobility transistors (HEMTs). Especially, AlGaN/GaN heterostructures have become a focus due to their wide-bandgap and high saturation velocity since the mid 2000s. Wider-bandgaps, directly correlated with higher breakdown voltages, enable HEMTs to withstand greater voltage swings, producing more power [4]. In addition to their high power capacity, GaN transistors have better form factors which allow the circuits to be smaller. Also, GaN's ability to withstand higher channel temperatures provide better reliability and better operation in high temperatures.

1.2 Why GaN?

Since the advent of GaN HEMTs as a viable technology in early 1990s, GaN technology has developed rapidly. GaN HEMT presents itself as a great prospect for high power microwave applications due to its high electron mobility and wide bandgap. Table 1.1 shows the Baliga's figure of merit for competing materials [5].

High current density combined with high sheet charge and high breakdown

	Mobility $\mu(cm^2/V.s)$	ϵ_r	Bandgap, Eg (eV)	Breakdown field Eb ($10^6 V/cm$)	BFOM ($\mu.\epsilon.Eg^3$)	Tmax $^{\circ}C$
Si	1350	11.9	1.11	0.7	1.0	300
GaAs	6000	12.3	1.43	0.7	4.6	300
4H-SiC	800	9.7	3.2	3.5	60.4	600
GaN	1000	9.5	3.4	3.5	73.9	700

Table 1.1: Material Properties of GaN and competing materials [6]

voltage means GaN HEMTs have the highest power density among other wide bandgap devices. In addition, GaN HEMTs, compared with other technologies, especially GaAs, have higher impedances. High voltage breakdown allows Q-points with high drain voltages resulting in higher impedances. This allows the amplifier to have a higher fractional bandwidth.

Among the other wide bandgap technologies GaN has the advantage of being able to operate at higher temperatures [7]. This advantage is also capitalized more upon the fact that GaN's thermal performance is better compared to GaAs devices. Table 1.2 compares the thermal conductivity between GaAs, GaN, Si and SiC.

	GaAs	GaN	Si	SiC
Thermal Conductivity (W cm/K)	0.46	1.7	1.5	4.9

Table 1.2: Thermal Conductivity

Bulk GaN, Si and SiC have higher thermal conductivity than GaAs. This makes GaN again a more viable option compared to GaAs. Considering the fact that most GaN devices are grown on SiC or Si, these substrates define the limit for GaN devices.

Several high power S-Band amplifiers built with GaN technology have been reported among different research groups [8][9][10][11][12]. One group, by paralleling four $16 \times 140 \mu m$ 4.15 W/mm GaN HEMTs, produced a GaN MMIC (Monolithic Microwave Integrated Circuit). At 3 GHz, under 50 μs pulse operation, they reported peak power output that reached 35 W. The peak power density was

3.9 W/mm [13]. Another group reported output power of 63 W by utilizing four $10 \times 360 \mu\text{m}$ GaN HEMTs. The final device was a 2-stage MMIC. Peak power density of 4.15 W/mm was measured at 3 GHz with 10 μs pulse [14]. Triquint fabricated a 2-stage MMIC with a total output periphery of 14.4 mm. They reported 70 Watts of peak output power at 3.5 GHz, reaching a power density of 4.9 W/mm [15].

1.3 Outline

Chapter 2 gives a general overview of GaN technology and fabrication. GaN properties are explained with regards to competing technologies. A simplified process flow with illustrative cross sections and their significance in terms of final devices were explained.

Chapter 3 gives a brief background on microwave amplifier theory and design.

Chapter 4 explains empirical characterization of an HEMT. Fixture and packaging are also mentioned.

Chapter 5 explains the design procedure of the PA. Design approach, specifications and EM simulations are offered.

Chapter 6 gives a detailed result of the measurements. Also results for the amplifier built with CGH40010f are given.

Chapter 2

GaN Technology and Fabrication Process

2.1 GaN Technology

AlGaIn/GaN HEMT was first demonstrated as a future prospect in 1994 by M. Asif Khan, J. N. Kuznia, and D. T. Olson in a paper published in Applied Physics Letters [16]. The HEMT, high-electron mobility transistor, was based on a structure called heterostructure first described in 1974. These developments led to the development of commercial GaAs and then GaN in mid 2000s. A Japan based company, Eudyna Corporation, was the first to bring a successful AlGaIn/GaN HEMT structures to RF market using GaN on SiC [17].

Since then, many different organizations produced GaN HEMT products but implementation has been slow for sectors other than RF/Microwave due to GaN HEMTs being a depletion mode device (normally-on) and relatively expensive.

For RF applications, GaN has been the material of choice for top performance. GaN has a wide bandgap compared to other materials which means higher breakdown voltage. Higher breakdown voltage for a power amplifier means, higher

voltage swing, generating more power. Furthermore, higher electron saturation velocity provides higher saturation current. Since power is a product of voltage and current swing, these two properties, combined, mean that GaN has higher power for a given chip area.

Design consideration wise, GaN offers great possibilities for the designer and the end user. Since, GaN has a higher power density, chip area can be shrunk. Previously when a certain specification needed multiple GaAs devices, smaller number of GaN devices can accomplish the same task, making the design process significantly easier for a variety of topologies. The gain from device area also brings the cost closer to GaAs, benefiting the end user.

For the broadband designs, specifically distributed amplifiers, GaN offers greater bandwidth as its output impedance is higher compared to GaAs.

2.2 GaN HEMT Device Process

GaN HEMT device fabrication is divided into two major sections:

- Epitaxial growth of GaN layers
- Device Fabrication

2.2.1 Epitaxial growth of GaN layers

2.2.1.1 SiC

GaN devices grown on GaN substrates are not available due to GaN substrates being extremely expensive at acceptable qualities. Compared to other substrates such as Si and Sapphire, SiC has a lower lattice mismatch and low difference of coefficient of thermal expansion with GaN. As a result, 2DEG (two-dimensional

electron gas) properties are significantly better compared to other materials. Relatively similar coefficient of thermal expansion also increases reliability.

2.2.1.2 AlN Growth on SiC

AlN (Aluminum Nitride) layer of 140 nm is grown on 4H-SiC. This layer, also called the nucleation layer, fills the micro cracks occurred on SiC during fabrication and decrease the strain on GaN due to lattice mismatch between GaN and SiC. In addition, quality of the nucleation layer directly affects the quality of the GaN buffer layer. GaN buffer layer's resistance is expected to be relatively high. Strains in this layer could decrease the said resistance. Thus, good quality of the nucleation layer is important.

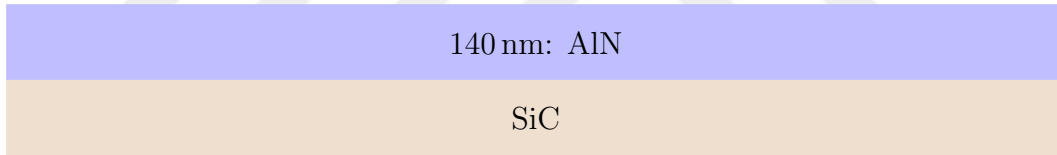


Figure 2.1: Illustration of Layers After AlN Growth

2.2.1.3 Carbon Doped GaN Buffer

GaN layer with high carbon content of 1275 nm height is grown on AlN layer. This layer should have low defect density and high bulk resistance. Indeed, high concentration of defects cause current leaks into the bulk and energy trap levels. These trap levels degrade device performance due to the foremost phenomenon, current collapse. At the extreme, trap levels could potentially disrupt the pinch-off point of the device. Isolation between the devices is also provided by GaN buffer layer, as a result, low quality GaN buffer can cause device parasitics due to coupling.

Finally, GaN buffer is the material formation on which the high quality GaN layer will be grown. Therefore, surface and defect quality affect the final interface between GaN and AlGa_N (Aluminum Gallium Nitride), influencing the

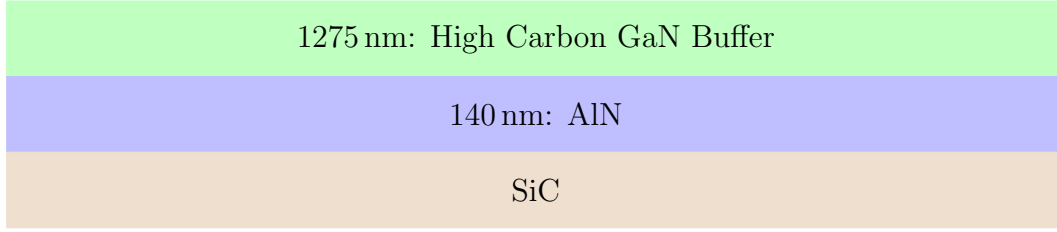


Figure 2.2: Illustration of Layers After GaN Buffer Growth

performance of 2DEG.

2.2.1.4 GaN Transitional Layer

A GaN transitional layer of 380 nm between buffer and channel layer is grown. This layer serves as a transitional layer between the GaN layer which will form 2DEG and GaN buffer layer, so that active GaN layer's quality can increase as much as possible.

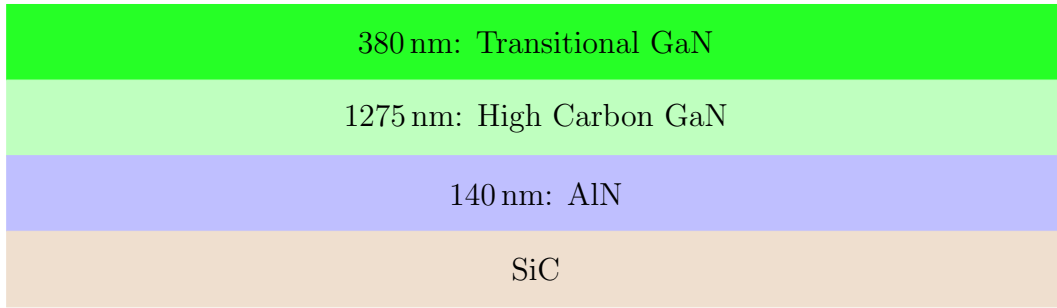


Figure 2.3: Illustration of Layers After Transitional GaN Growth

2.2.1.5 High Quality GaN Layer

200 nm of GaN layer is grown of GaN transitional layer. This GaN layer has high charge mobility, high surface smoothness and low defects. These properties will contribute to the final device performance.

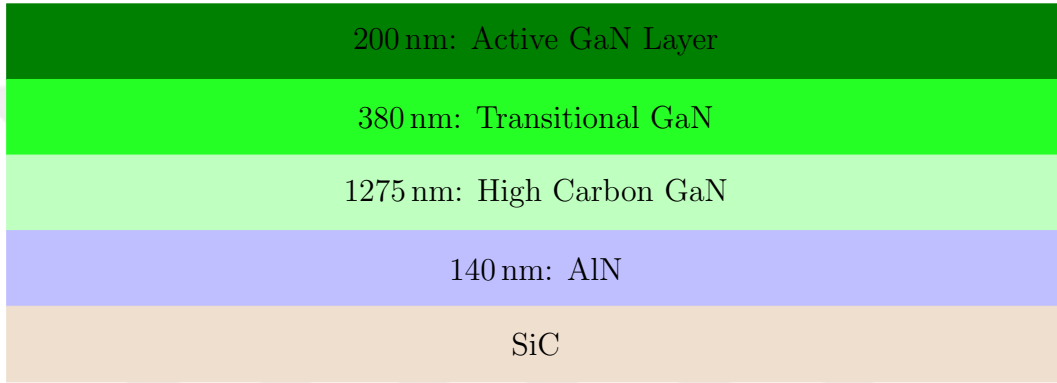


Figure 2.4: Illustration of Layers After Active GaN Growth

2.2.1.6 AlN Spacer

1 nm AlN spacer is grown GaN layer. This layer decreases the Coulomb scattering the charge carriers in 2DEG will confront. As a consequence, electron mobility of the channel will increase substantially.

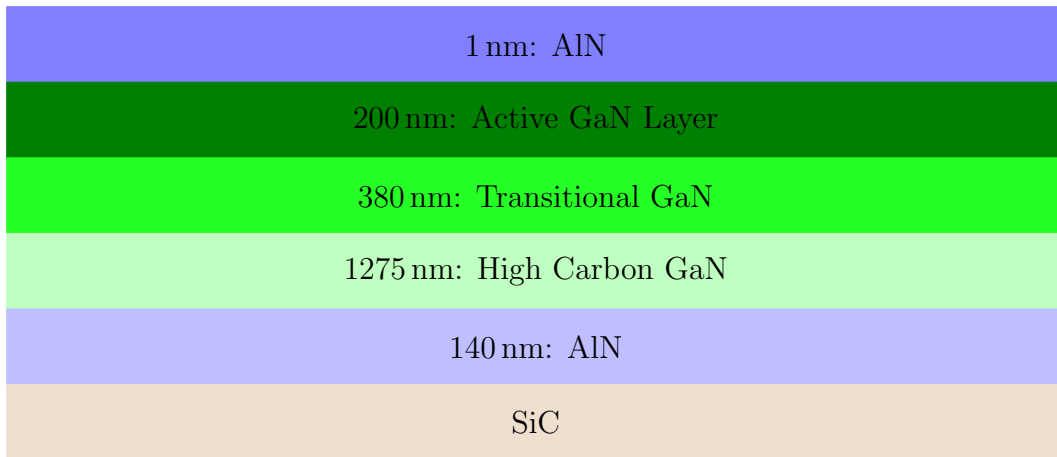


Figure 2.5: Illustration of Layers After AlN Spacer Growth

2.2.1.7 AlGaN Barrier

Immediately after AlN layer, a 20 nm AlGaN barrier is grown on AlN. Finally, the lattice mismatch between GaN and AlGaN layers is what generates the 2DEG.

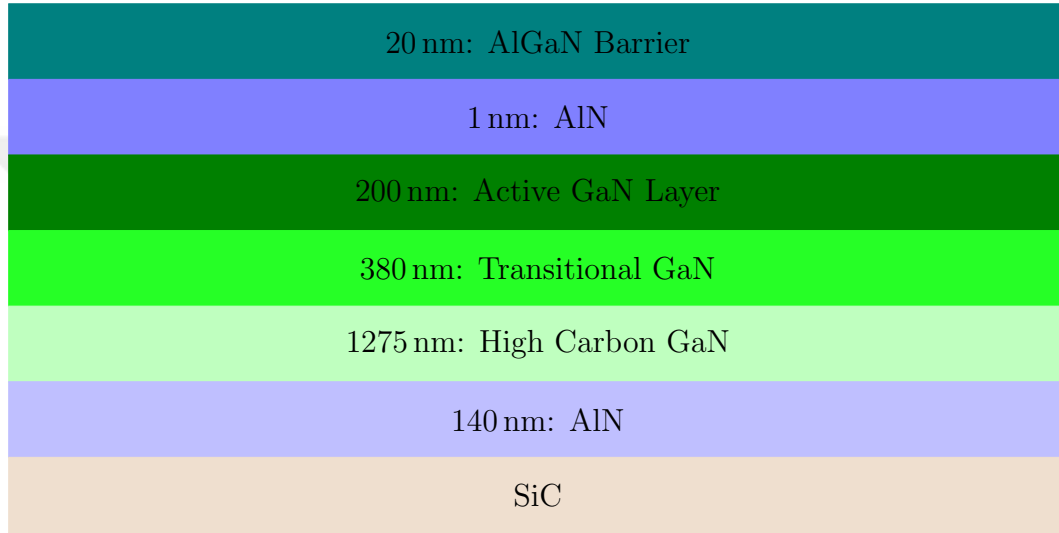


Figure 2.6: Illustration of Layers After AlGaN Barrier Growth

2.2.1.8 GaN Cap

A GaN cap layer is grown to increase Schottky Barrier height and reduce gate leakage current. Also, GaN cap eases the ohmic contact process.

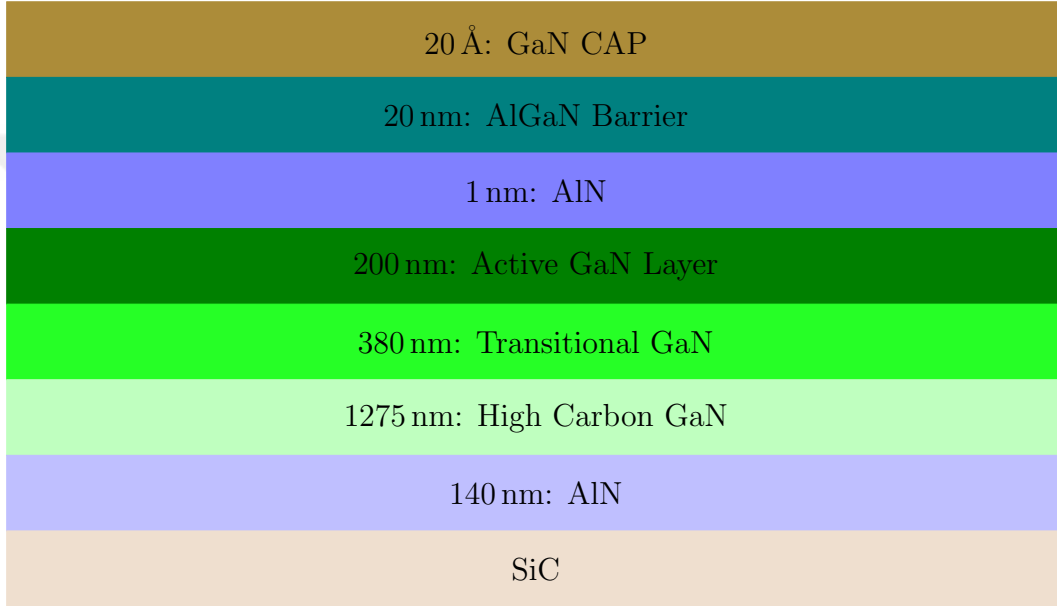


Figure 2.7: Illustration of Layers After GaN CAP

2.3 Device Fabrication

After GaN epitaxial growth, device fabrication takes place. Device fabrication is necessary to form the actual devices such as capacitors, transmission lines and transistors. The gate structures for HEMTs are also completed in this stage.

These processes are done via "masks" of layers prepared during the design process. Figure 2.8 shows the mask of a $10 \times 250\mu\text{m}$.

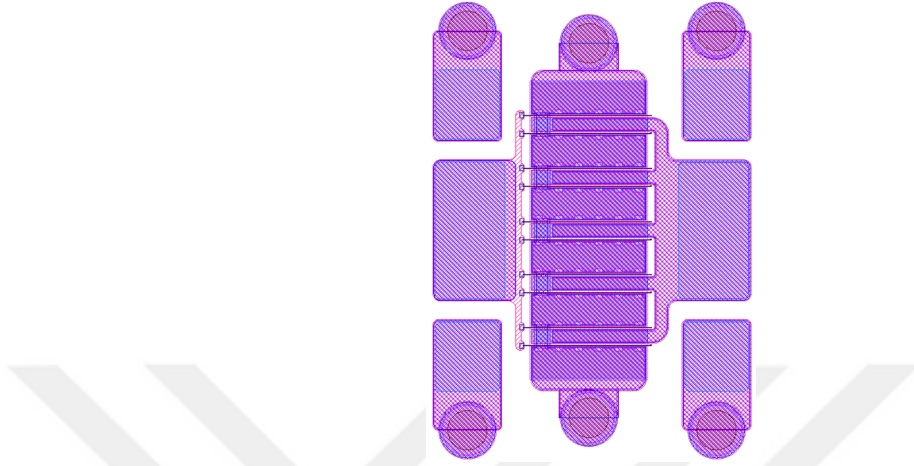


Figure 2.8: Tapeout mask of a GaN HEMT

2.3.1 Ohmic Contacts

In order to get a conducting material to the 2DEG, an alloy is diffused into the wafer. These contacts provide places where the connections for circuitry will be connected. The contact made by this process is also called a ohmic contact due to its voltage and current characteristics.

2.3.2 Mesa Etching Process

AlGaN layer is etched in order to isolate the active devices on the same wafer. During this process, some GaN will also be etched due to similar GaN and AlGaN structure.

2.3.3 Gate Lithography

For HEMT structures, Schottky contacts with high energy barriers have to be built. A metal with a low work function will incur greater gate leakage, impeding transistor behaviour. In addition, gate resistance directly affects input resistance of the HEMT. For this purposes, Ni and Au are used for Schottky gates.



Figure 2.9: Illustration of Layers After Ohmic Contacts



Figure 2.10: Illustration of Layers After Mesa Etch

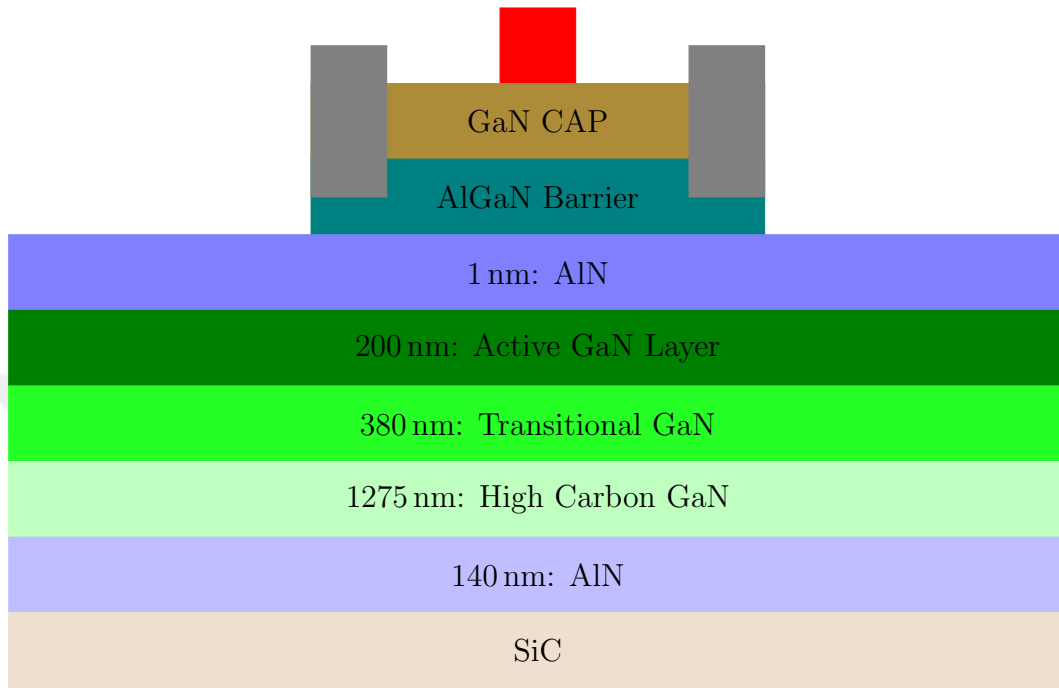


Figure 2.11: Illustration of Layers After Gate Lithography

2.3.4 Metallization

Metal layers necessary for outside contacts are formed during this process. This metal is the interconnect metal that connects other layers. Also, all circuit elements like capacitors and inductors use this metal for main conductor. In addition, waveguides are made from this metal for MMICs.

2.3.5 Backside Via

Back side via is formed to connect the source of HEMTs to backside ground and enable microstrip structures.

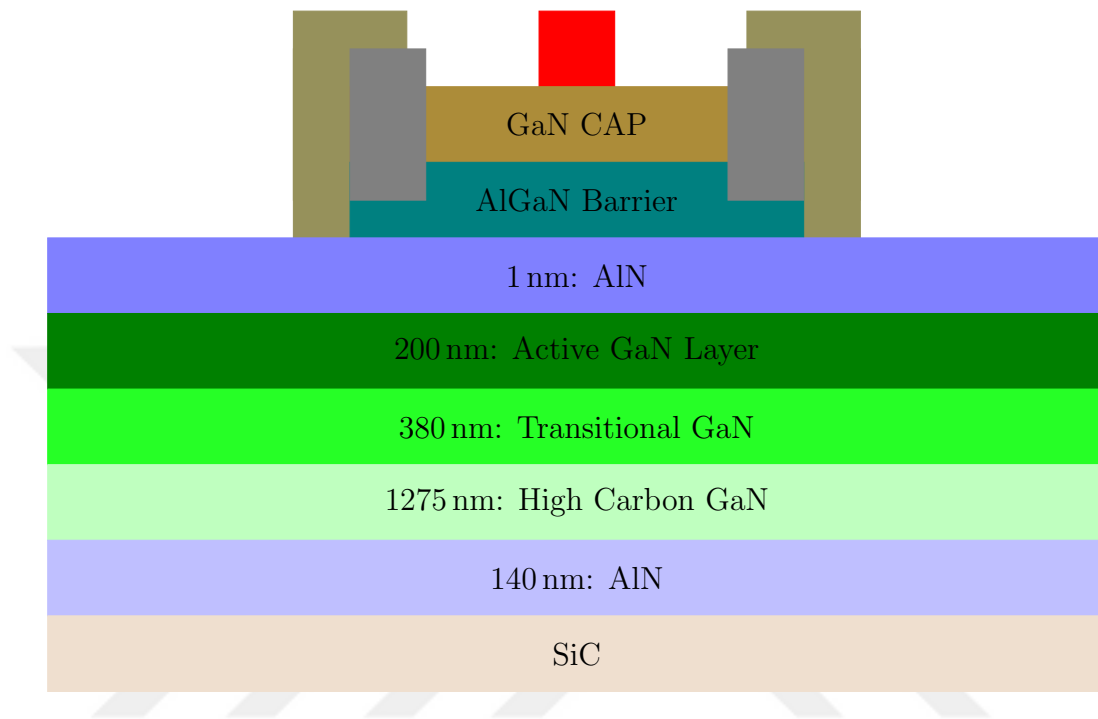


Figure 2.12: Illustration of Layers After Metallization

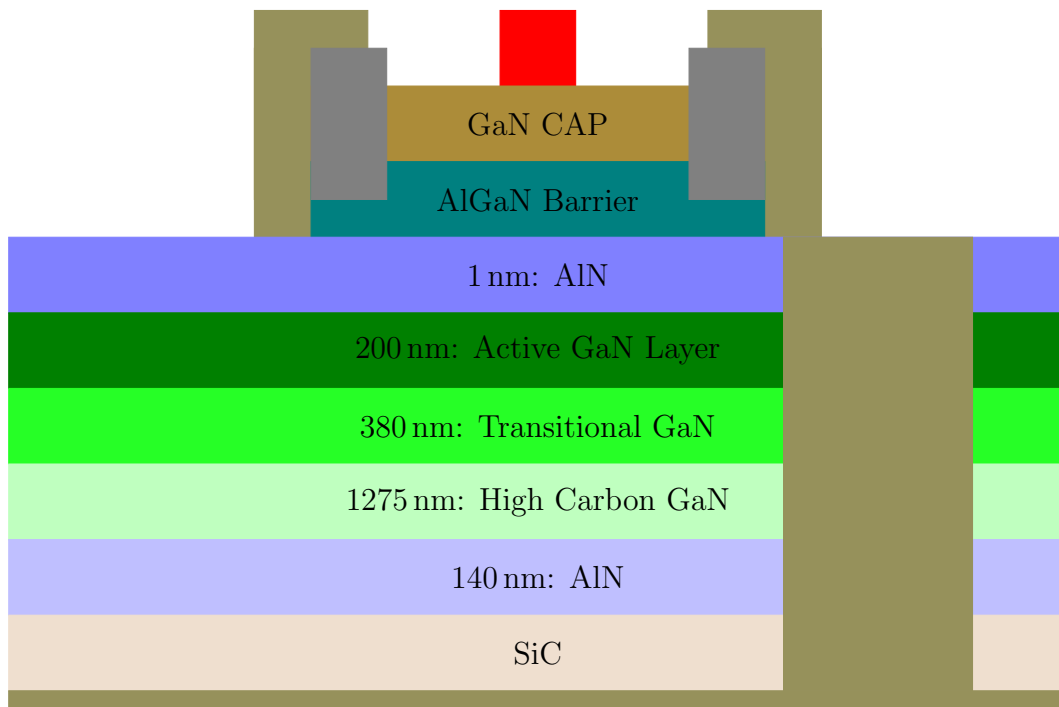


Figure 2.13: Illustration of Layers After Via Process

Chapter 3

Power Amplifier Fundamentals

For many front-end structures, power amplifiers are one of the most important devices. They are used in many applications such as telecommunications, medical imaging and radar applications.

Power amplifiers are devices that convert DC power to RF power. Specifically, this RF power is in large signal operation because power amplifiers deliver high levels of power. Non-linear effects become more prominent at these levels compared to small-signal operation.

Small-signal characteristics, such as scattering parameters, are well defined for devices which are designed for fixed-gain or low-noise amplifiers and do not depend on input power level. Since, the PA's output signal is compressed, or clipped, due to high power output (1 dB compression or 3 dB compression), the device is not in the linear region. The input and output impedances become dependent on input power levels, which increases the design complexity of the overall device.

Thus, this chapter will introduce fundamentals that are required to design a PA.

3.1 Basic Parameters

In order to understand specifications and evaluate performance, important features of PAs will be defined and discussed.

At any given time, instantaneous power is defined as:

$$P(t) = V(t) \times I(t) \quad (3.1)$$

$$P_{in}(t) = V_{in}(t) \times I_{in}(t)$$

$$P_{out}(t) = V_{out}(t) \times I_{out}(t)$$

Power gain is defined by the ratio of the output power over input power:

$$G = P_{out}/P_{in} \quad (3.2)$$

Since, amplifiers with power gains over 1000 are available, logarithmic scale is usually used while referring to power gain,

$$G_{db} = 10 \log(G)$$

In addition, a logarithmic power unit, dBm, is also defined. dBm is the ratio of power over 1 mW in logarithmic scale.

$$Power_{dBm} = 10 \log(Power_{mW}/1 \text{ mW}) \quad (3.3)$$

Thus,

$$P_{out} = P_{in} + G \quad (3.4)$$

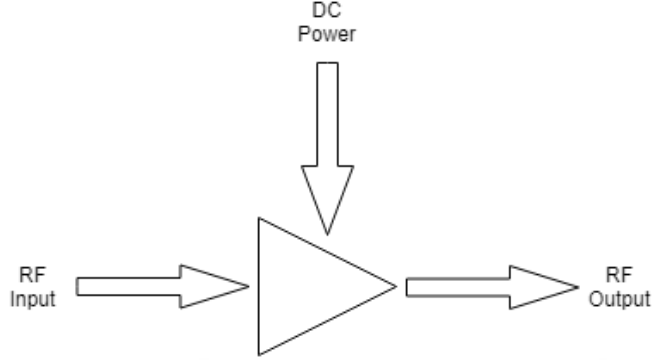


Figure 3.1: Illustration of a basic RF power amplifier

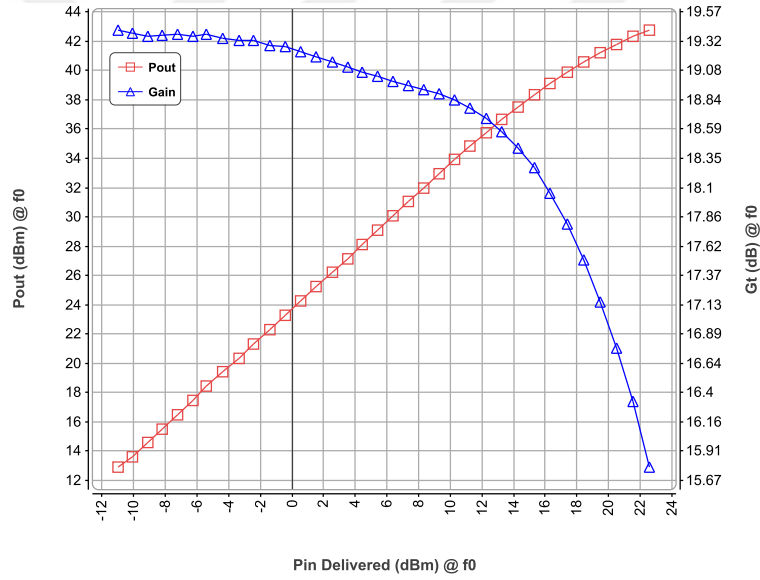


Figure 3.2: Typical large signal input, output power and gain measurement

From the above equation, output power seems to increase with input power continuously, but unfortunately that's not the case. The gain of the amplifier only remains constant if the PA is in the linear region, that is the output waveform is not clipped and amplifier's gain is not compressed. During this mode of operation, device becomes nonlinear. As shown in the figure above, as the input power increases, gain becomes compressed and declines steeply after output power saturates. Figure 3.2 is a typical large signal measurement.

Since power amplifiers' greatest importance is the output power, two figures of merit are used to evaluate their output characteristic. P_{1dB} is defined as the

output power where the small signal gain is decreased by 1 dB. P_{1dB} is used to measure the compression character of an amplifier. Compression behavior is unique to almost every amplifier and it is very important to characterize it. Compression may occur fast or slow relative to the input power, which might affect the overall system design.

Since, PAs are usually the biggest consumer of DC energy in any system, their efficiency affects the efficiency of the total system greatly. Efficiency is a significant factor for thermal management and depending on the application, battery management. For high power outputs, high efficiency means easier thermal design and longer available operation time which also increases battery life. This is especially important for mobile applications. Therefore, efficiency specification is an important factor that affects the whole design.

First definition of efficiency is derived from how well a PA generates RF power from DC power. Hence, this efficiency is also drain efficiency.

$$\eta = \frac{P_{out}}{P_{DC}} \quad (3.5)$$

Though, this definition does not include input power. The input power becomes significant because PA amplifiers are designed have maximum saturated power output, where input and output power become comparable. Equation 3.6 is the “power added efficiency”.

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \quad (3.6)$$

3.2 Amplifier Classes

RF/Microwave Amplifiers are usually designated as different classes depending on the relation between input and output signals. For a given design, choice of operation depends on noise figure, power levels, linearity, gain, efficiency and

weight. In terms of operational comparison, each class offers a trade of between linearity and efficiency.

Different topologies and design considerations are acknowledged to better elaborate different classes.

Amplifier classes are divided into two main categories; transconductance amplifiers and switch-mode amplifiers. Transconductance amplifiers, Class A, AB, B and C are driven by a sine wave. While the switch-mode amplifiers are usually driven by square waves.

3.2.1 Class A

Class A amplifiers have an angle of conduction of 360 degrees, meaning they amplify the input signal for all of its phase. Since, the signal is amplified for its whole period, crossover distortion compared to AB, B and distortion compared to Class C are avoided. This means Class A amplifiers have the best linearity of all classes. In this case, the Q-point(quiescent point) of the transistor is biased at the center of the load line. This is also why Class A amplifiers have their theoretical maximum drain efficiency of 50% [1]. Figure 3.3 shows the biasing of different classes on the I_{DSS} vs V_{ds} graph.

Class A amplifiers are biased for maximum linearity and similar to small-signal amplifiers in that regard. As such, they are conjugately matched on both the input and output. As long as they are not pushed into deep compression, the input and output waveform will be the same while harmonics and distortion are low.

3.2.2 Class B

Class B amplifiers are biased right on their pinch of voltage, so that their $I_{DQ} = 0$ A. Thus, they do not consume power when there is no RF input power. As the

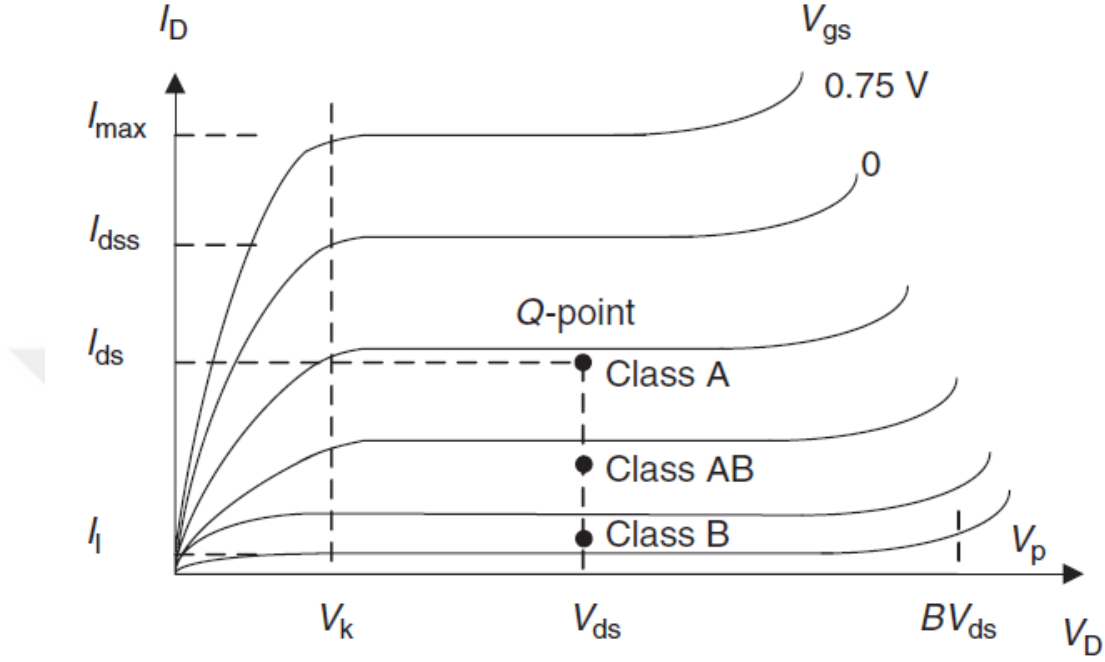


Figure 3.3: Biasing for different classes[18]

device turns on by the input RF power, Class B amplifiers have conduction angle of $\theta = \pi$. At RF frequencies push-pull configurations are available to amplify the whole period of the waveform. At microwave frequencies, two parallel single-ended amplifiers which have 180° phase difference can be used to amplify the whole signal. These two configurations improve linearity and power at the cost of design complexity and area. Their theoretical maximum drain efficiency is 78.5%.

3.2.3 Class AB amplifiers

As the name suggests, Class AB amplifiers' Q-point lie between Class A and Class B. Therefore, Class AB amplifiers have an angle of conduction $0 < \theta < 2\pi$. This means the signal is not amplified for the whole period, and output signal is clipped. They are a compromise between where they are more linear compared to Class B and more efficient compared to Class A.

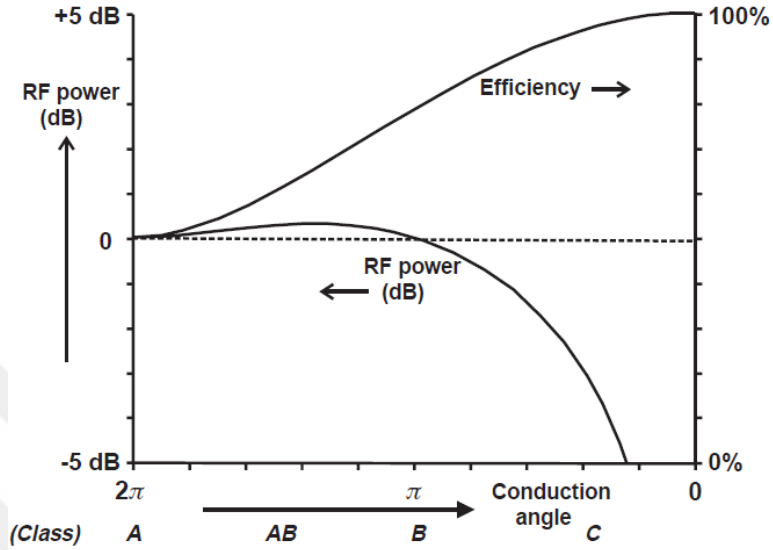


Figure 3.4: RF power and efficiency relative to the conduction angle

3.2.4 Class C

On the spectrum between linearity and efficiency, Class C amplifiers remain as the most efficient for transconductance amplifiers. Class C amplifiers' conduction angle is $\theta < \pi$. Meaning they only conduct in less than the half of the cycle of the waveform which increases their efficiency. This is possible by biasing the transistor below the threshold voltage such that the device only turns on for some portion of the positive cycle of the waveform. Class C amplifiers are usually used for modulation schemes where linearity is not vital.

3.2.5 Class D and Class E

Class D and E use the transistor as a switch to control the output waveform. These topologies can reach high efficiency at the expense of linearity. In the ideal conditions these classes can reach to 100% efficiency but during the transition phase, power is dissipated nonetheless. As the frequency of operation increases, this effect becomes more prominent.

3.2.6 Class F

In order to increase efficiency, a multiple-resonator is present at the output of a Class F amplifier. Ideally, even harmonics are shorted while odd harmonics are shown open.

In practice, a Class F amplifier is designed essentially the same as Class AB/B amplifier with addition of aforementioned output matching circuit. However, practically, only the second harmonic short is viable for wide bandwidth operation.

3.2.7 Stability

3.2.7.1 Even-mode stability

An important issue for the operation of a power amplifier is stability. An unstable amplifier will oscillate at the frequencies where $|\Gamma_{in}| > 1$ and $|\Gamma_{out}| > 1$. Positive feedback provided by this condition will cause large signals at the output independent of the input signal, eliminating the functionality of the amplifier. Stability is examined under two conditions:

- Unconditional stability where the amplifier is stable for all $|\Gamma_S|$ and $|\Gamma_L|$
- Conditional stability where the amplifier is stable for only some $|\Gamma_S|$ and $|\Gamma_L|$

Depending on the input and output mismatch shown to the amplifier, *conditionally stable* amplifiers can be utilized, but this is beyond the scope of this work.

Since the reflection coefficients are frequency dependent, a network may be stable at a frequency but not at another. Therefore, the stability analysis should be done from DC to f_{max} .

Γ_{in} and Γ_{out} can be expressed as:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (3.7)$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (3.8)$$

Based on these definitions, Rollett's unconditional stability conditions state that for the complex impedances that satisfy, $|\Gamma_L|, |\Gamma_S| < 1$, the circuit is unconditionally stable if the following statement is true: $|S_{11}|, |S_{22}|, |\Gamma_{in}|, |\Gamma_{out}| < 1$.

As a result of these conditions, by Rollett's Stability factor k , a device is unconditionally stable if:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1 \quad \text{and,} \quad (3.9)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$

μ' is another factor which measures the relative stability of a two-port device. A two-port device is unconditionally stable if:

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta(\overline{S_{22}})| + |S_{21}S_{12}|} > 1 \quad (3.10)$$

μ parameter also has a graphical meaning on the Smith chart, the distance between the center of the Smith Chart and the instability circle. As the distance increases, stability also increase [19].

3.2.7.2 Parametric Oscillations

Due to the nonlinear behaviour of transistors at large signal operation, a phenomenon called parametric subharmonic instability can occur. Under large RF

voltage swings, non-linear behaviour of capacitances such as C_{gs} and C_{gd} become dominant and can show pumped nonlinear reactance or negative resistance [18]. For power amplifiers, this behaviour can cause oscillations.

Stability can be improved by using parallel RC circuits or narrow-band matching circuits for suppressing the low frequency behaviour of subharmonic oscillations. These precautions improve stability for narrow band amplifiers but difficulties arise when dealing with wide band circuits. To model this effect, accurate large signal models, especially accurate modelling of the non-linearity of C_{gs} and C_{gd} , are needed.

3.2.7.3 Low Frequency Oscillations

These oscillations can occur due to non-linear behaviour of amplifiers at low frequencies. Gain could increase substantially and device can become unstable. Since most microwave models do not feature characterization between 10 Hz-50 MHz, stabilization of these frequencies are usually dealt with outside the package [18].

Chapter 4

Characterization of Active Devices

In order to design a power amplifier, linear and nonlinear properties of the active devices have to be known. These properties determine the device capability and under what conditions those capabilities are possible. Power amplifiers operate in large signal modes, therefore their non-linear behaviour is important as their small signal behaviour. As such, more “sophisticated” approaches are needed. Thus, characterization is a crucial part of the design process. Characterization of an active device is examined under four approaches:

- Models derived through a PDK (Process Development Kit),
- Analogous device models where physical effects are represented by appropriate circuit elements
- Complete physical models characterized with device physics and accurate geometry
- Empirical models derived through various measurements.

In this work, we relied on empirical characterization, which we gathered

through measurements in our own lab. Each measurement models a different aspect of the HEMT. For instance, DC measurement gives the breakdown and a possible range of bias for the transistor, while small signal measurements give the impedances needed for matching under those conditions. Proper characterization is the first step in designing since the device will be limited by these parameters. Therefore, significant care and understanding should be applied when characterizing devices for the sake of both the device specifications and test equipment health.

4.1 DC Measurements

First step in characterizing an active component is DC measurement. DC measurement gives information regarding possible device capabilities, biasing conditions and linearity. Also, DC measurement is usually the first electrical stress test the devices undergo during characterization. Thus, proper care and understanding should be applied during DC tests.

Firstly, conventional DC measurement is conducted on Keysight 1505A. Figure 4.1 is a picture of 1505A.

Figure 4.2 is the IV curve for a $10 \times 250\mu\text{m}$ HEMT from our process.

As the gate voltage is swept from -6 V to 0 V , we measure saturated drain current I_{DSS} as $>2.5\text{ A}$ which is inline with our expected saturated drain current of 1 A/mm . Figure 4.3 shows the transconductance, g_m measurement.

Peak of the g_m curve gives an idea of gain for linear operation if there were no parasitics involved. Also, position of the peak with respect to gate-source voltage shows a possible bias option for maximum gain. Figure 4.4 is the graph of breakdown measurement.

But conventional behaviour of an active device under continuous DC may differ from RF operation significantly. This is due to energy trap levels [20] whose

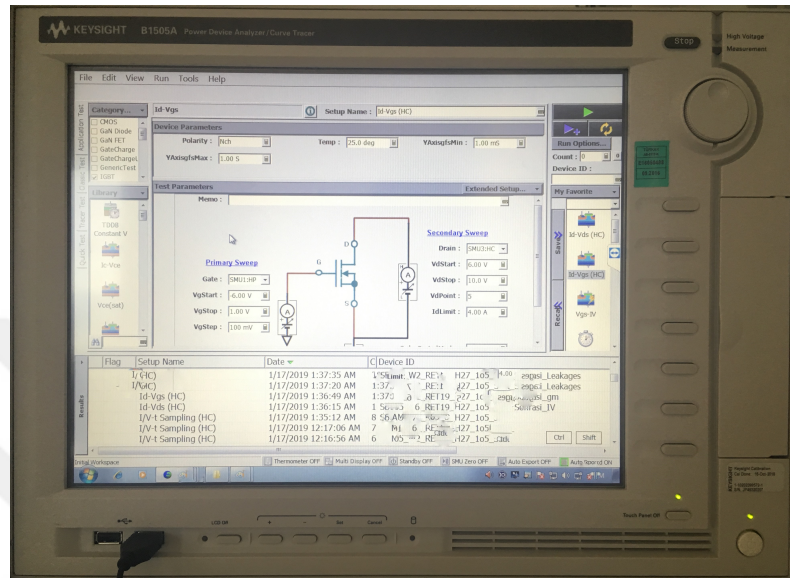


Figure 4.1: DC measurement setup

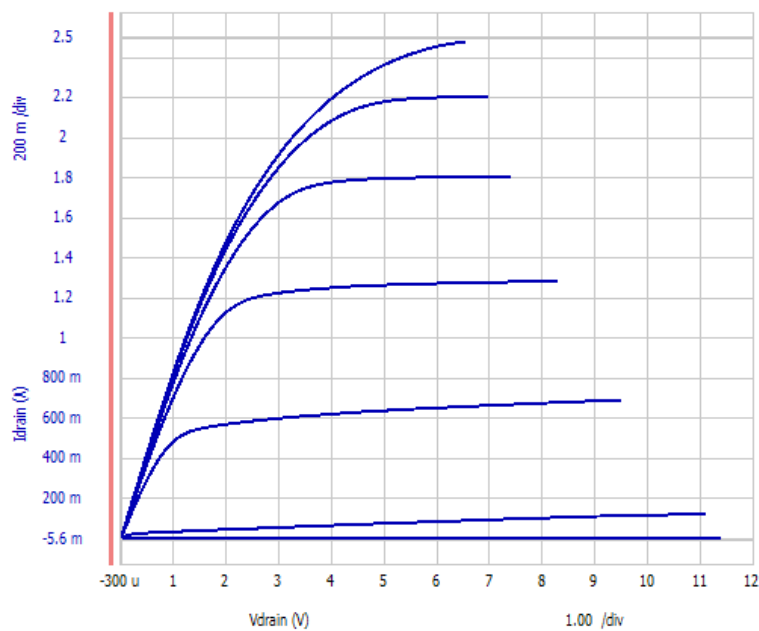


Figure 4.2: IV curve of a $10 \times 250\mu\text{m}$ HEMT

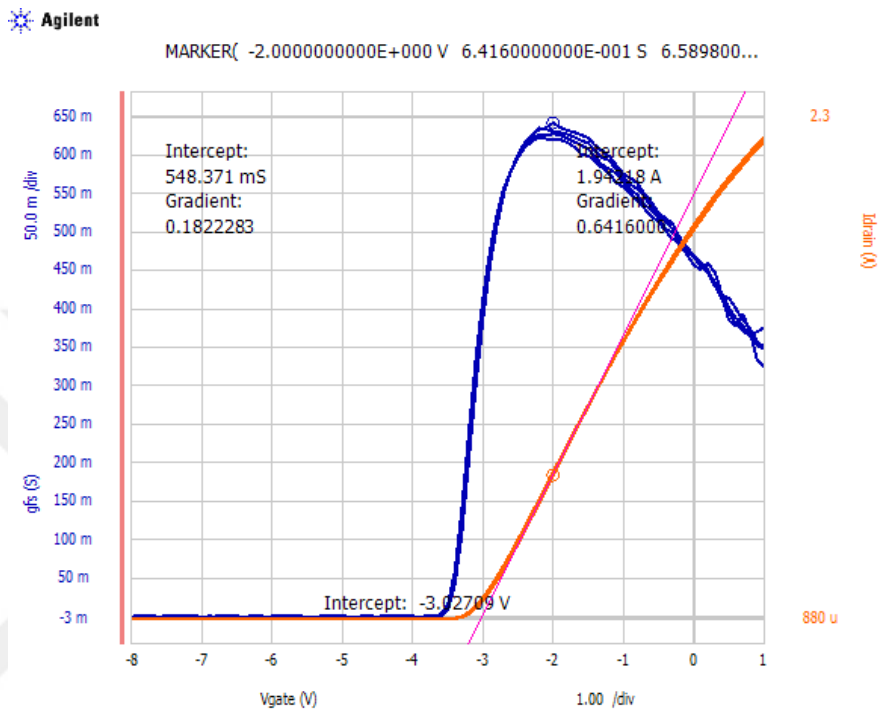


Figure 4.3: Transconductance vs V_{gs}

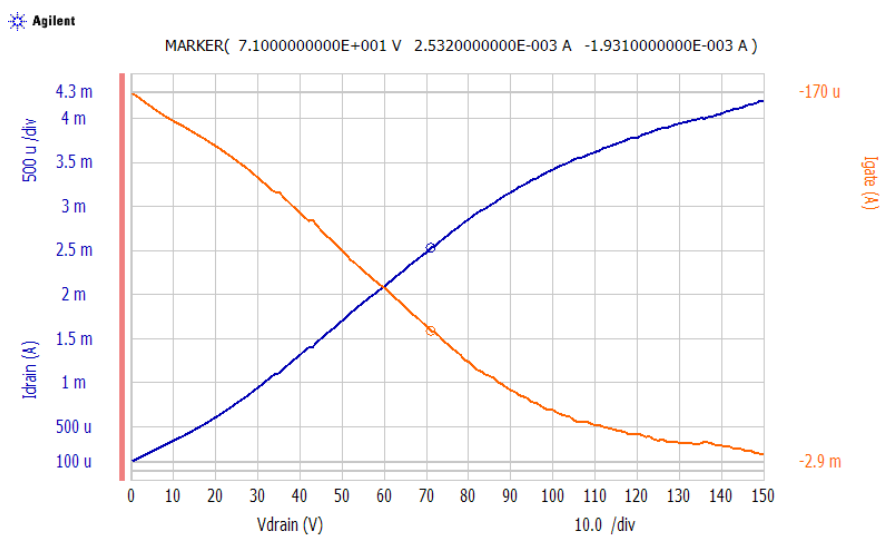


Figure 4.4: Breakdown behaviour under high drain voltage

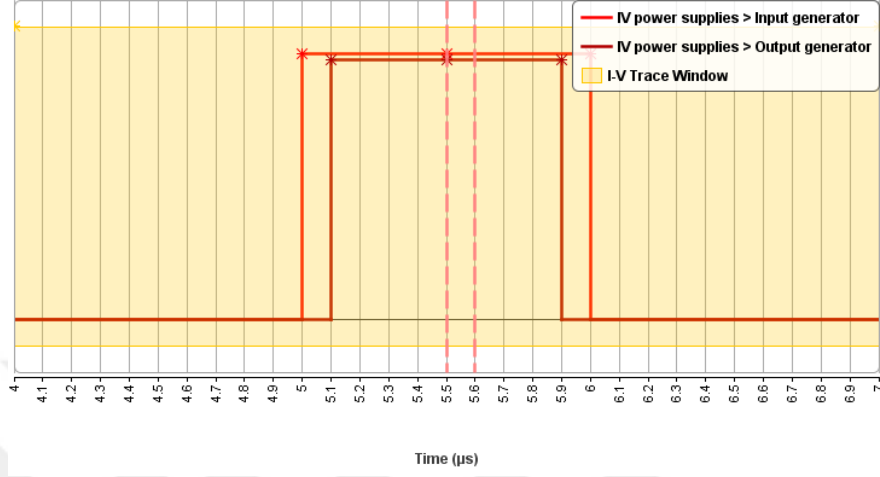


Figure 4.5: Chronograph of the pulsed IV measurement

behavior may be hysteretic on voltage and depend on frequency of operation. An instance of this behaviour is sudden decrease in I_{DSS} after applying high voltage [21]. Due to this phenomenon, device character will significantly change especially in large signal operation. This is important in power amplifiers since the device power output will be affected. In the extreme conditions device may even turn off for good. Therefore, a pulse IV measurement is proposed to observe this behaviour.

To observe this effect quantitatively, we measure the drain current under different conditions. Before each pulse measurement, transistor is initially biased. This bias is called Q_{in} . Table 4.1 shows the Q_{in} pairs for gate and drain biases. Then, the pulsed measurement is conducted as the drain voltage is swept from 0 V to 20 V for two different gate values. Change in I_{dss} is noted. Figure 4.5 is the chronograph of the pulsed signals.

	V_{gs}	V_{ds}
$Q1_{in}$	0 V	0 V
$Q2_{in}$	-6 V	0 V
$Q3_{in}$	-6 V	32 V

Table 4.1: Initial State Pairs for Pulsed IV Measurement

Figure 4.6 shows the pulsed IV for a $8 \times 125\mu\text{m}$ HEMT device.

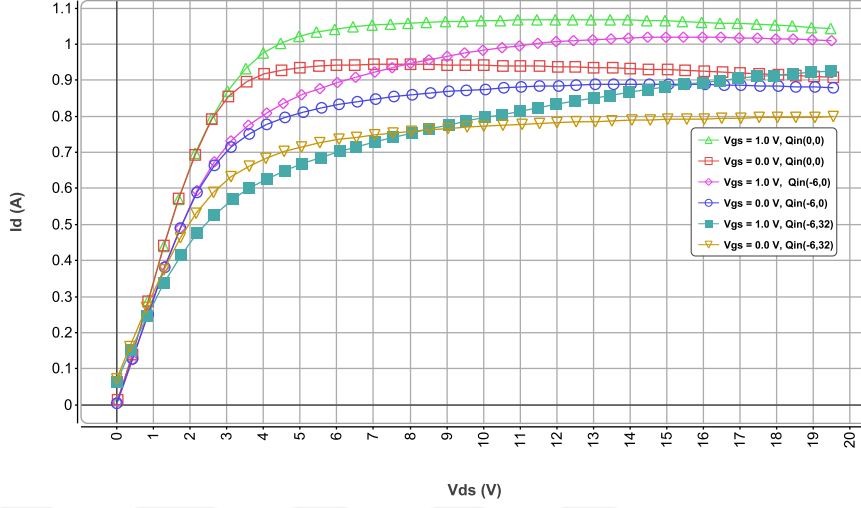


Figure 4.6: Pulsed IV of a $8 \times 125\mu\text{m}$ HEMT

As seen on the Figure 4.6, saturated drain current for $V_{gs} = 0$ drops by 15%, staying significantly below 1 A/mm which is the target saturated drain current density GaN devices. Although, this will affect the peak device performance (especially at high voltage swings) [22], it will not cause a total disruption for the amplifier. However, this behaviour could possibly make a transistor turn off during high voltage swings in the extreme conditions. Therefore, this behaviour should be properly analyzed for GaN and GaAs HEMTs.

4.2 Fixture

Since the device will be packaged, proper fixture design is needed. The transistor die should be properly situated on the fixture package such that thermal conduction and electrical connections occur in a desired way. Any stray inductance will affect the possible bandwidth negatively therefore, grounding should be properly managed, so that stray inductance between the source and the ground is minimal. The electrical connection between the package and the HEMT is of utmost importance. Proper choice of an adhesive with both good electrical and thermal properties is desired.

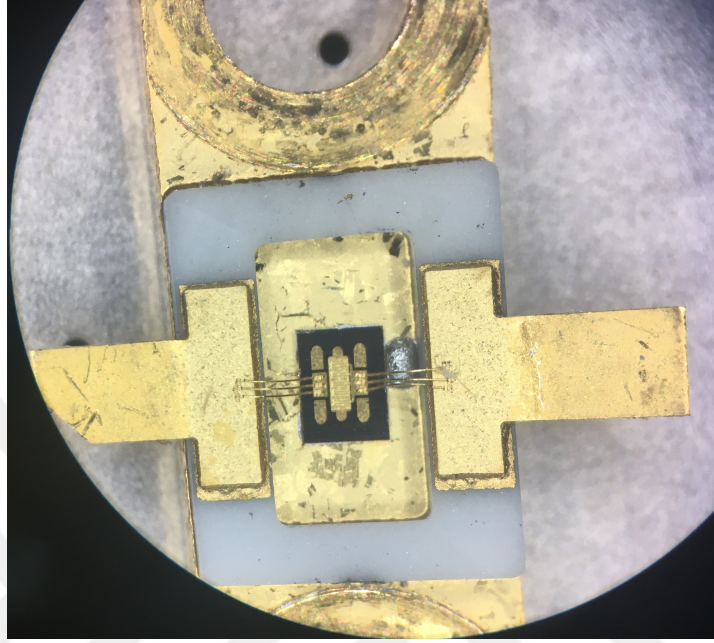


Figure 4.7: HEMT with the package and wire Bonds

For these reasons, the die is glued onto the package with EPO-TEK H20E Silver epoxy. The epoxy while being a mechanical connection between the HEMT and the package, also has to provide good electrical and thermal conduction. The adhesive is then cured for 1 hour at 150 °C. Table 4.2 shows the properties of EPO-TEK H20E Silver epoxy.

H20E Silver Epoxy	
Thermal Conductivity W/mK	2.5
Volume Resistivity @ 23 °C $\Omega \text{ cm}$	0.0004

Table 4.2: H20E Silver Epoxy Thermal and Electrical Properties

Gate and drain connections between the transistor and package are produced by wire bonds. However, wire bonds introduce inductive high impedance discontinuities. Bond modelling and in-situ thin film capacitors close to wire bonds can improve the response over a bandwidth and decrease parasitic effects [23].

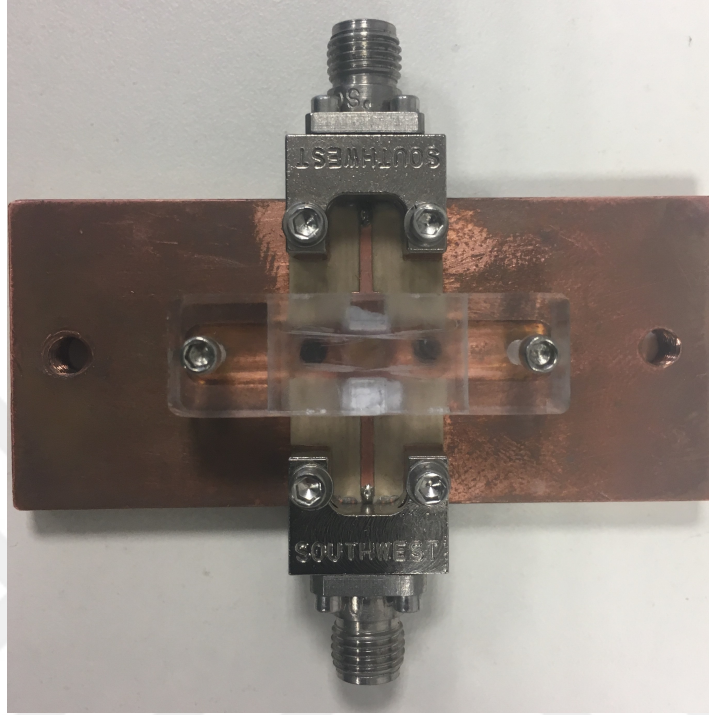


Figure 4.8: Test fixture for the package

In our fixture, we only utilized wire bonds and conducted the RF characterization under that condition. Finally, a copper fixture which provides the support for connectors and the PCB is manufactured. Figure 4.8 shows the final test fixture for the HEMT device.

4.3 Small Signal Analysis

Unlike lower frequencies, parasitic reactances increase in impact as the frequency of operation increases [1]. These reactances need to be resonated out in the matching circuit so that devices' gain become useful. In order to measure these effects, devices have to be characterized at these frequencies. Small signal analysis, for a given bias point, measures these effects under low power which is also called linear region. Figure 4.9 is the setup used for S-parameter measurement.

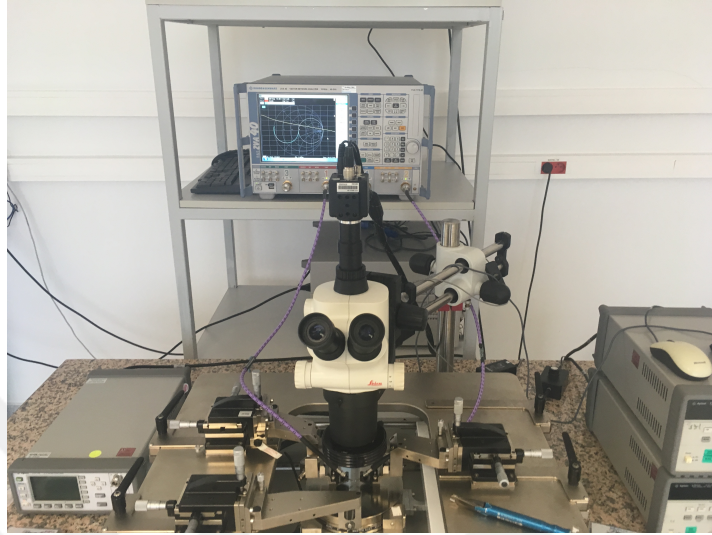


Figure 4.9: Small signal setup used in characterization

These measurements enable us to model the transistor as a linear 2-port s-parameter matrix at the given bias point.

4.4 Large Signal Analysis (Loadpull)

As the output power is a strong function of output match, measurement of multiple data points on different impedances contribute to design process. Fundamentally, loadpull consists of a calibrated output tuner which shows different impedances to the DUT. By this operation, different contours such as power, gain and efficiency can be observed under large signal conditions.

Performance of a loadpull system is mostly assessed based on its ability to cover Smith Chart, in other words, showing impedances close to $|\Gamma| = 1$. As the desired reflection will only hold for a single frequency, different setups for loadpull systems are available. Figure 4.10 shows the loadpull setup that we used to characterize the large signal behaviour.

Loadpull performed only at fundamental frequency will still present non-ideal impedances at harmonic frequencies [1] and may even effect the operation at

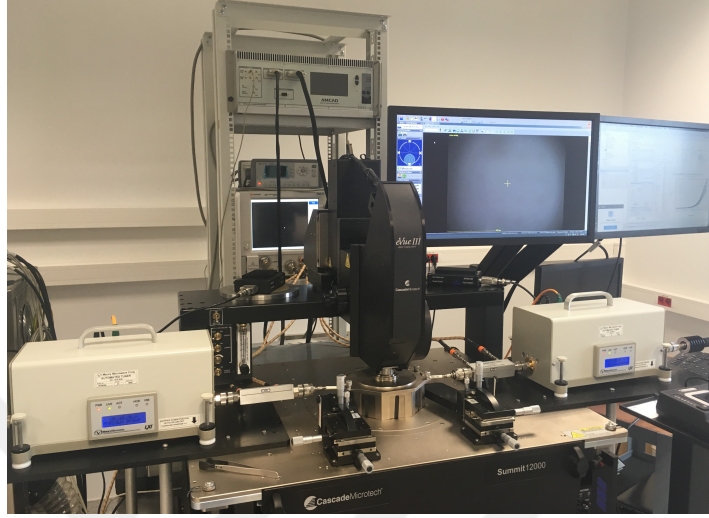


Figure 4.10: Pulsed IV setup

fundamental frequency, driving the output impedance away from the normally-desirable point. Therefore, loadpull setups available with harmonic matching are preferable, especially for Class AB amplifiers. However, harmonic loadpull is beyond the scope of this work.

Rapid developments in the device technology still allow the use of these devices, as the modelling of a novel device is significantly faster compared to building a CAD model. Figure 4.11 shows the P_{out} and gain contours measured at 28 V 100 mA at pulsed wave conditions under 1 dB compression. Notice that gain and power contours converge around different points. Figure 4.12 shows the typical loadpull contours.

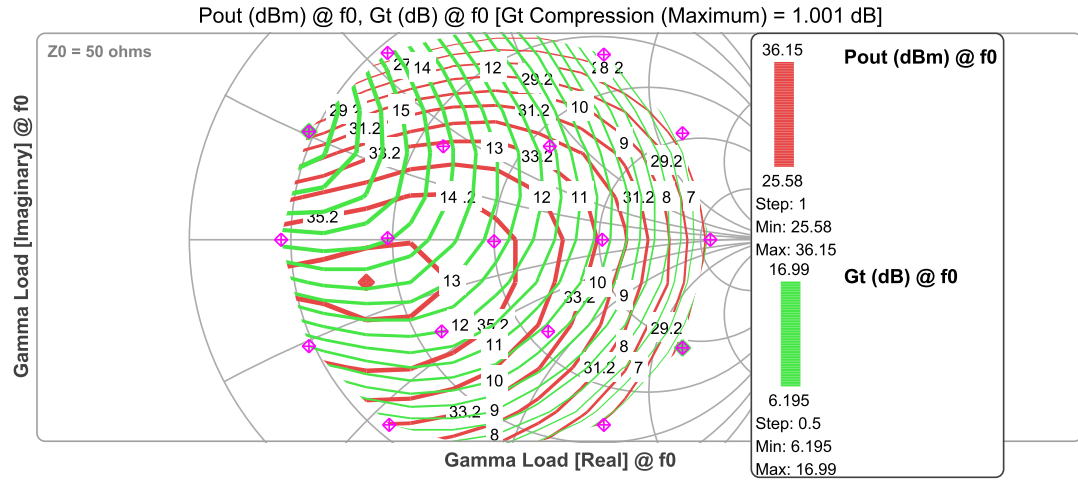


Figure 4.11: Our transistor under 1 dB compression @ 3 GHz

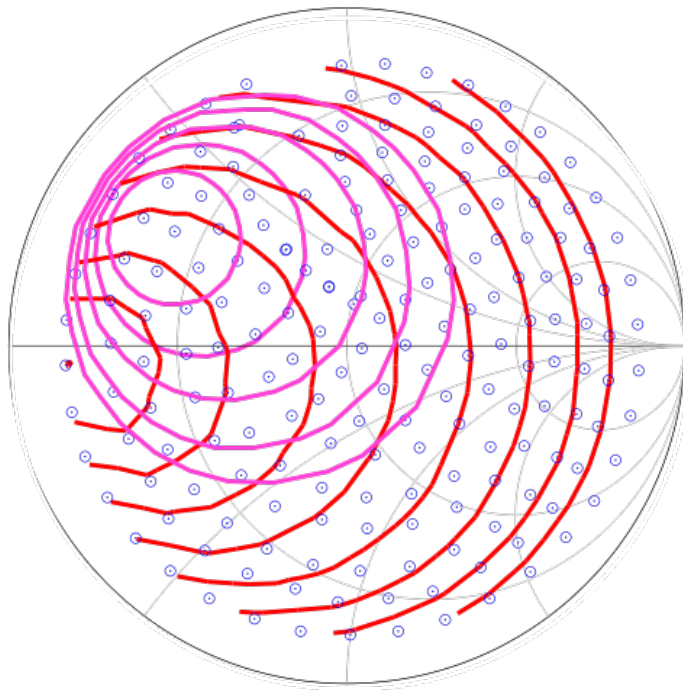


Figure 4.12: A generic loadpull contours, Red: gain, Magenta: power

Chapter 5

Amplifier Design

PA design process is a multi-dimensional problem in its own right. A brief summary would be to get as much as “power” out of the system, but the conditions at which this power is attained is also important. While a design is obviously affected by IV, small-signal and large-signal character of the active design, device specifications and design goals influence the overall topology and approach. For instance, a design that aims to reach high efficiency suffers linearity and may need its harmonics shorted, whilst a design that has a higher drain current bias in favor of better linearity needs a wider DC feed line that could potentially introduce a low impedance line to device’s output. Thus, device character coupled with design objectives affect the final design.

Active device, laminate and component choices will be discussed in detail. Their properties and relation to frequency band will be examined.

CAD tools will be also be discussed. As this is a microwave design, schematic design, optimization and full EM simulation tools are necessary to have a design with minimum tuning after realization. Utilization of device and component models and proper simulation of substrate through modelling the laminate by CAD tools will be explained in praxis.

5.1 Design Process

A methodological approach should be taken when designing a PA to ensure optimum management of time. Determining the required specifications is the first step towards designing a system because following items will all depend on specifications. Ultimately, development will be completed only when results and measurements satisfy the specifications. Figure 5.1 shows the design flow used in this work.

5.2 Design Specifications

As mentioned in the previous chapters, different aspects affect the overall design. In our design, we aimed to produce a s-band high power amplifier with higher efficiency, while still being fairly linear. Table 5.1 offers the general design specifications.

Specification	Minimum	Maximum	Desired	Frequency
Input Return Loss	10 dB	-	15 dB	2.7 GHz - 3.3 GHz
Gain _{ss}	13 dB	15 dB	14.5 dB	2.7 GHz - 3.3 GHz
CW P _{sat}	39 dBm	-	40 dBm	3 GHz
Pulsed P _{sat}	40 dBm	-	41.5 dBm	3 GHz
Pulsed Drain η	55%	-	60%	3 GHz

Table 5.1: Design Specifications of the PA

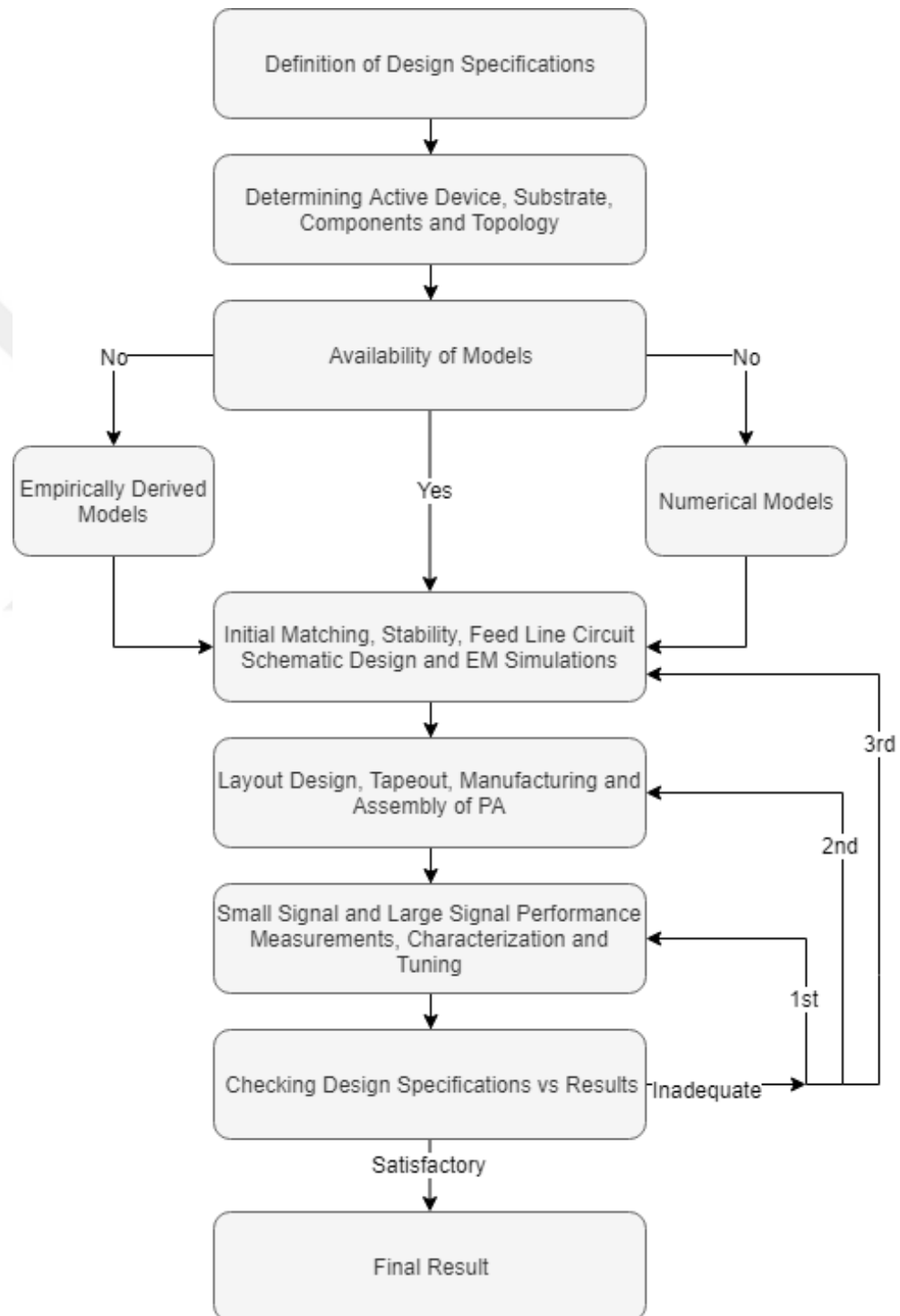


Figure 5.1: Design flowchart of a power amplifier

5.3 Active Device, Substrate, Component and Topology Selection

5.3.1 Active Device

One of the most crucial design choices of a power amplifier is the transistor selection. Since, the focus of our work is an hybrid amplifier, a discrete transistor solution will be chosen.

Transistor selection is a direct result of design of specifications. For a variety of specifications such as, power density, thermal performance, gain and operating frequency, different technologies are available. For instance, for a low power output amplifier, CMOS technology might be viable for reduced costs, while to achieve higher power output at high frequency, GaAs can be preferred. If an increased fractional bandwidth is desired, coupled with higher power density, GaN technology would be viable due to having higher output impedance compared to GaAs due to the nature of the substrate at a higher cost.

In addition, operation environment is also an important issue. Availability of an heat sink and environment temperature do effect the transistor choice. GaN, due to its wide-bandgap, is able to operate at high voltages and high channel temperatures [6]. Nevertheless, an efficient thermal management is also needed for a high power amplifier. For instance, in the case of a 10 Watt RF power HEMT with a $10 \times 250 \mu\text{m}$ total gate width, a drain to source distance of $5 \mu\text{m}$, creates a $80 \text{ kW}/\text{cm}^2$ average heat flux from the gate area on top side. Without proper thermal management, device reliability would cause serious concern.

A system wise consideration reflecting on efficiency should also be taken. For a given RF Microwave system, the greatest likely consumer of power is the amplifier. GaN having a better efficiency rating compared with other technologies make it a candidate for high power amplifiers.

Since NANOTAM has the ability to fabricate devices according to our own

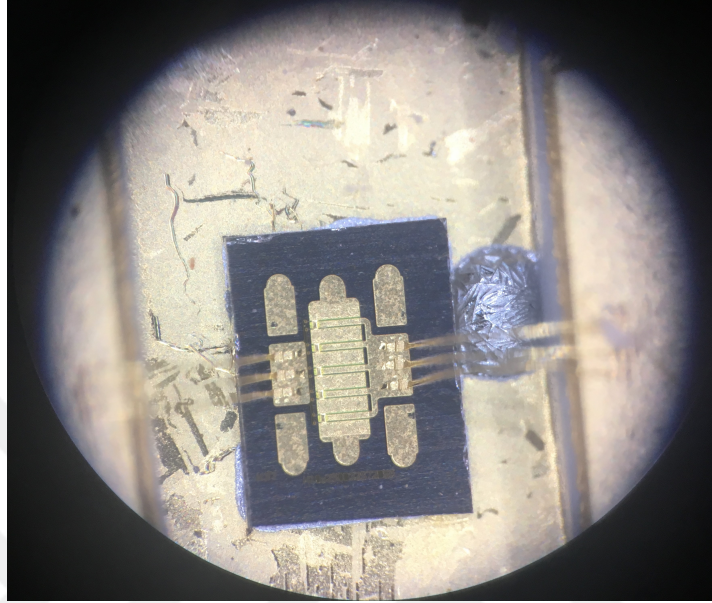


Figure 5.2: GaN HEMT under optical microscope

specific needs, we have investigated other foundries' products available in S-band to determine our specifications but also to create a similar performance. With these reasons in mind, we have chosen CGH40010f from Wolfspeed. CGH40010f is a GaN HEMT designed for telecommunications industry specifically. Its intended operation range stretches from DC to 6 GHz. Wolfspeed claims the transistor is able produce 13 Watts of RF power under saturation conditions while providing a small signal gain of 14 dB at 4 GHz. As a match, we have selected a GaN HEMT with similar performance capabilities from NANOTAM.

Our transistor is a HEMT with $10 \times 250 \mu\text{m}$ total gate width. Drain pad length is $32 \mu\text{m}$, source pad length is $72 \mu\text{m}$. Drain to source distance is $5 \mu\text{m}$. Source field plates are present. Figure 5.2 shows the transistor chosen under optical microscope with wire bonds and conductive adhesive.

5.3.2 Substrate

An important issue to mention is here why an hybrid solution was favored rather than MMIC in this work. Although, MMICs have better scalability in terms of

mass production, better unit cost and greater performance capability, hybrid approach becomes reasonable when prototyping. Depending on the manufacturing techniques, for a single PCB, manufacturing process can be shortened to mere days while for an MMIC, time duration is in weeks at best. Another practical point is that most of the time a wafer would be divided into multiple reticles designed by multiple engineers, therefore the total time it would take to finalize would be considerably longer.

Laminate choice is an essential matter in designing an RF Microwave circuit. Ultimately, after determining and characterizing the active devices, majority of the time is spent on designing the PCB. Different aspects regarding the whole circuit such as frequency of operation, special requirements of handling procedures, manufacturing specifications, physical properties of the material and other points should be taken into account. In return, PCB's performance will affect the overall performance of the circuit.

Principal feature when choosing a laminate is its dielectric constant. For a given waveguide, dielectric constant affects the overall size of the circuit. For microstrip lines, characteristic impedance of the waveguide is a function of both the dielectric constant and the height of the material. A transistor that have a large total gate width and high power output would require a low impedance to be seen at its output. In terms of a practicality, it would be easier to realize a low impedance with higher dielectric constant in that case. If paralleling of smaller devices with higher output impedances were required, a laminate with lower dielectric constant would be viable. Equation 5.1 shows the relationship between characteristic impedance and dielectric constant.

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\epsilon_e}} \ln \left(\frac{8d}{W} + \frac{W}{4d} \right), & \text{for } W/d \leq 1 \\ \frac{120\pi}{\sqrt{\epsilon_e} [W/d + 1.393 + 0.667 \ln(W/d + 1.444)]}, & \text{for } W/d \geq 1 \end{cases} \quad (5.1)$$

Furthermore, dielectric loss is a significant concern for the designer, too. Dielectric loss is simply defined as dielectric material's capacity to convert electromagnetic energy into heat. This property mainly affects the losses in waveguides,

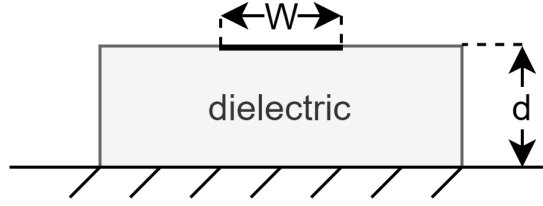


Figure 5.3: Cross section of a microstrip line

and so efficiency. Depending on the design, their loss may increase the stability of the network. Nonetheless, highly lossy material is detrimental to a power amplifier since, despite of the fact that transistor is capable of providing more power, resulting power of the circuit is less than what the transistor produces. Another important issue regarding dielectric material is its homogeneity throughout the whole plate. A non-homogeneous material will incur a design difficulty where different parts of laminate will have different dielectric constant and appropriately different electrical properties. As a result, laminate choice significantly influences the electrical design process.

For the surface finishes, smoothness of the conducting layer is also a factor in circuit performance. Rough surfaces increase loss, and may alter the electrical length, as a result final circuit might be significantly different than EM simulations. These effects become more prominent as the frequency of operation rises such that skin effect formula becomes inaccurate because fields around rough metals behave different compared to smooth metals [24].

As mentioned in the previous section, thermal properties of the laminate is a dominant factor in device performance. Desirably, it should be a good conductor of heat so that it can quickly dump the excess heat into the heat sink, without being a significant bottleneck. Performance of the circuit will increase as the thermal gradient between bottom metal and top circuit decreases. This is especially true for GaN because the device performance is sensitive to temperature [25].

In addition, thermal expansion of both the dielectric material and conductive

layers should be taken into account. The temperature differences during operation introduce different mechanical stresses on the PCB, namely tensile stress on the surface as the thermal expansion of metals is generally less than composite materials. In an extreme condition, PCB might become damaged or RF performance might suffer since electrical length of waveguides is proportional to their physical length.

Chemical properties of the materials are also a matter of concern. For instance, copper suffers corrosion when left open to air. Although, copper oxide forms a protective layer around copper, preventing total oxidization, surface roughness, conductor height and total dielectric constant will vary nonetheless. Effects of these changes will become more prominent at high frequencies. PCB manufacturers use tin or nickel or both as a final surface finish to prevent corrosion altogether. Depending on the design frequencies, effects of these materials might need to be considered during the design process.

Finally, manufacturing process and equipment are to be considered, too. In this work, PCB manufacturing was done by a rapid PCB prototyping mill bench by LPKF. This ruled out laminates which had too brittle or too soft dielectric material in them. As there was no chemical etching involved, peel strength of the copper plating is also important during the removal process of unused copper regions.

With the design considerations mentioned above, we decided on using a Rogers RO4003C. RO4003C is a durable hydrocarbon ceramic laminate with good RF performance. It has a stable dielectric constant over varying temperatures and frequencies [26]. Figure 5.4 shows the value of the relative dielectric constant of the laminate.

Table 5.2 shows the mechanical and electrical properties of RO4003C.

Our laminate had 1/2 oz. 17 μm copper plating on both sides, with a dielectric thickness of 0.02 inches 508 μm . Figure 5.5 is the substrate created.

Property	Typical Value	Direction	Units
Dielectric Constant, ϵ_r , Process	3.38 +- 0.05	Z	
Dielectric Constant, ϵ_r , Design	3.55	Z	
Dissipation Factor, δ	0.0027 0.0021	Z	
Thermal Coefficient of ϵ_r	+40	Z	ppm/C
Volume Resistivity	1.7×10^{10}		M Ω cm
Surface Resistivity	4.2×10^9		M Ω
Electrical Strength	31.2		kV/mm
Tensile Modulus	19650 19450	X Y	MPa
Tensile Strength	139 100	X Y	MPa
Flexural Strength	276		M Ω
Dimensional Stability	<0.3	X, Y	mm/m
Coefficient of Thermal Expansion	11 14 46	X Y Z	ppm/C
Tg	>280		°C TMA
Td	425		°C TGA
Thermal Conductivity	0.71		W/(m K)
Density	1.79		g/cm ⁻³
Copper Peel Strength	1.05		N/mm

Table 5.2: Mechanical and Electrical Properties of RO4003C [26]

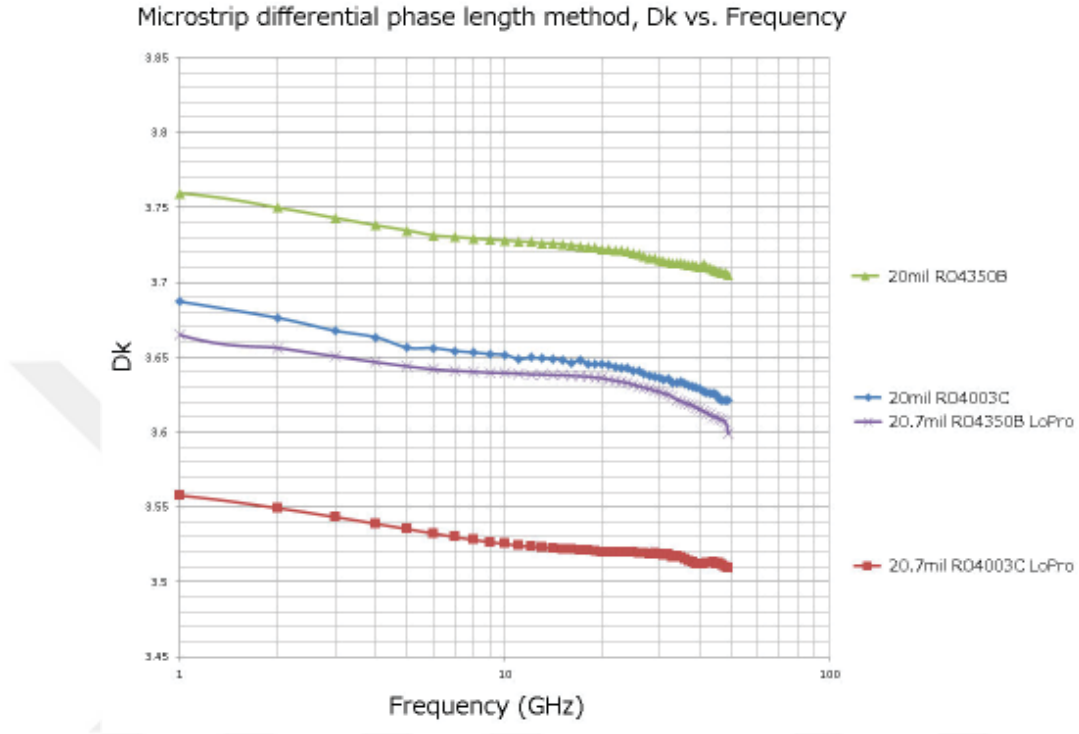


Figure 5.4: Dielectric constant over frequency [26]

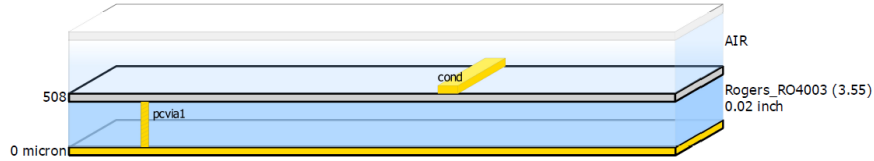


Figure 5.5: Cross section of the substrate built in ADS

5.3.3 Component Selection

In this work, matching circuits were designed on the PCB. Matching elements such as stubs and transmission lines are produced during the PCB manufacturing, however other circuit elements such as capacitors and resistors have to be implemented through discrete components. Depending on the frequency, discrete components offer great flexibility. An important issue here is that, just as non-linear effects become prominent for other aspects of the circuit, behaviour of passive components also change. At microwave frequencies, rather than how

much capacitance the device has valued at DC, designer needs to know the frequency response of the component at the operating frequency. Therefore, passive component models should be available.

For these reasons, we have chosen GJM Series of ceramic capacitors from Murata in 402 packages. GJM series is a high Q series of capacitors suitable for operation at microwave frequencies. Their main intended area of uses are wireless communications, high frequency tuning and matching circuits. Also, they are available from 0.1 pF to 47 pF and in tolerances down to 0.05 pF and rated at 50V. Murata also offers S-parameter data for GJM series, which greatly contributes to the design process.

For the stability network, we have opted to use American Technical Ceramics' ATC 504L series 25 Ohm resistor in 402 packages. 504L is a thin-film with a flat response from DC to 30 GHz.

5.4 Design

PA design starts with a simple schematic design with ideal components generally to decide the topology. The input and output impedance will give an idea of how wide bandwidth is achievable. Initial implementation of the stability circuit is also vital as it is usually the only desirable lossy element and will affect the device impedances.

Since the device characterization of the packaged transistor was done on a fixture, the fixture response has to be removed from the S-parameter measurement. Figure 5.6 shows the device under test and and fixture blocks the Vector Network Analyzer (VNA) measures.

Since, VNA measures everything between the reference planes, connector and fixture effects should be removed. This is done by either modelling or measuring the fixture devices themselves and then de-embedding them. Although physical

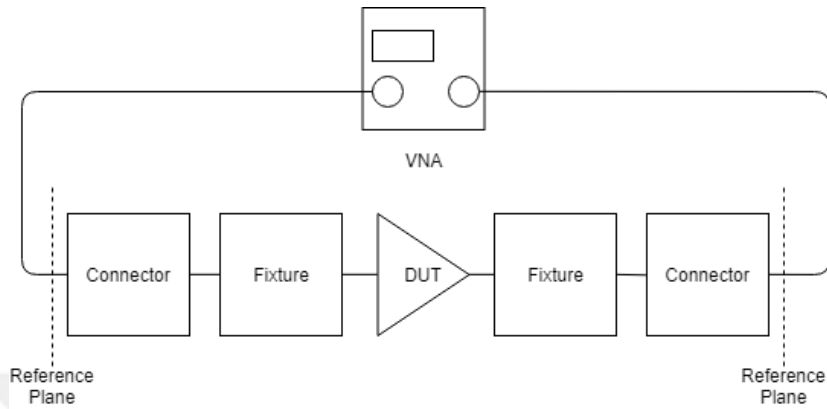


Figure 5.6: Small signal characterization diagram

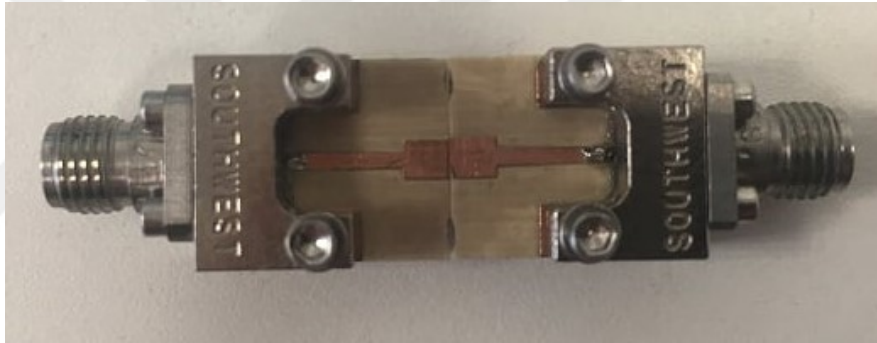


Figure 5.7: De-embedding circuit to characterize

dimensions of the connectors are provided by the manufacturer, pinpointing the reference plane is not straight forward, therefore, characterization of the connectors contribute to design accuracy.

In order to properly measure the phase added by Southwest end launch connectors, a simple microstrip through line is manufactured and measured. Fig 5.7 shows the passive de-embedding circuit.

At 3 GHz, the end launch connector added 64° electrical length. Layout of the fixture PCB was simulated in ADS. Layout is shown in Figure 5.8 The resulting S-parameter was used to de-embed the VNA measurement, finally resulting in only the packaged transistor response.

Figure 5.9 shows the schematic of the de-embedded fixture.

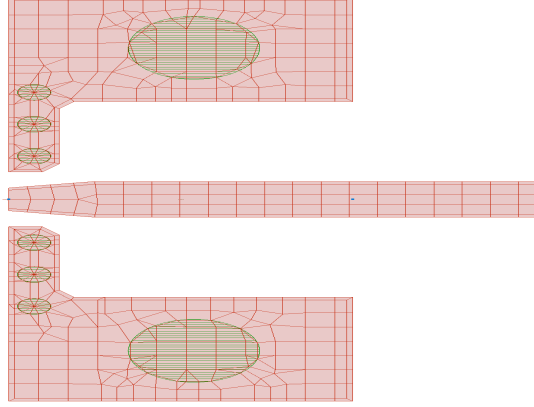


Figure 5.8: Layout of the de-embedding circuit

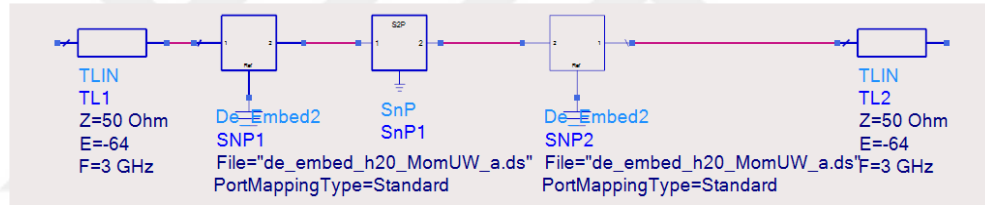


Figure 5.9: Schematic of the de-embedded fixture

5.4.1 Stability Circuit

De-embedded circuit is analyzed first for stability. A rule of thumb approach to designing a high power RF amplifier is to focus on stability block early. This makes sure that transistor never sees impedances which can cause oscillations even if the matching circuit changes. Figure 5.10 and Figure 5.11 show the Rollett stability factor and maximum gain from 100 MHz to 8 GHz and the source stability circles respectively.

Although, the band frequencies are stable, lower and upper frequencies need to be stabilized. For the lower part, a parallel RC circuit will be used. An ATC RF resistor of $25\ \Omega$ and Murata GJM series RF capacitor of 5 pF are used. Figure 5.12 and Figure 5.13 show the RC circuit added stability factor k and the stability circles respectively.

Although, lower GHz frequencies' stability has been improved, below 500 MHz

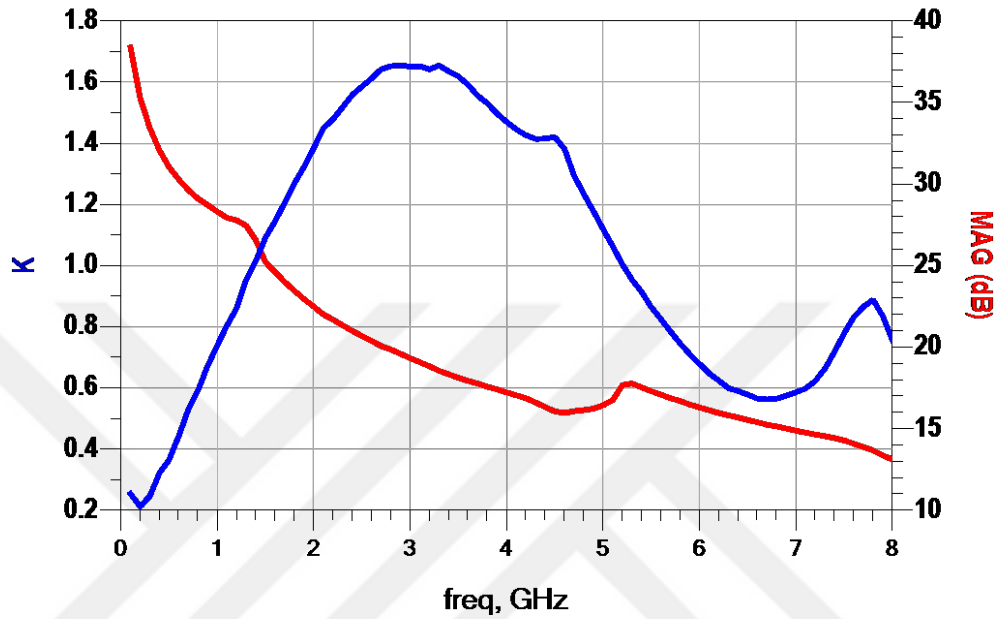


Figure 5.10: Rollett stability factor k and maximum gain from 100 MHz to 8 GHz

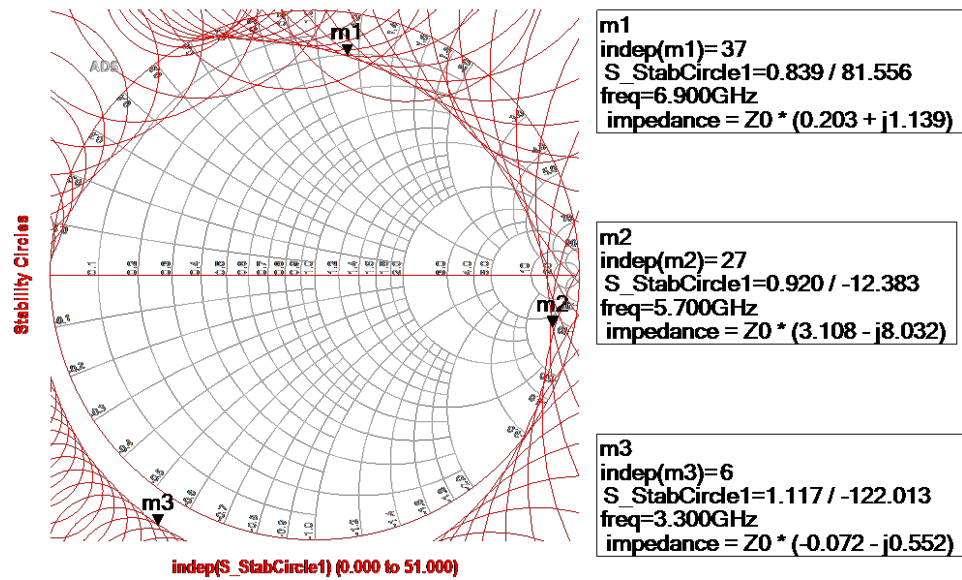


Figure 5.11: Source stability circles from 100 MHz to 8 GHz

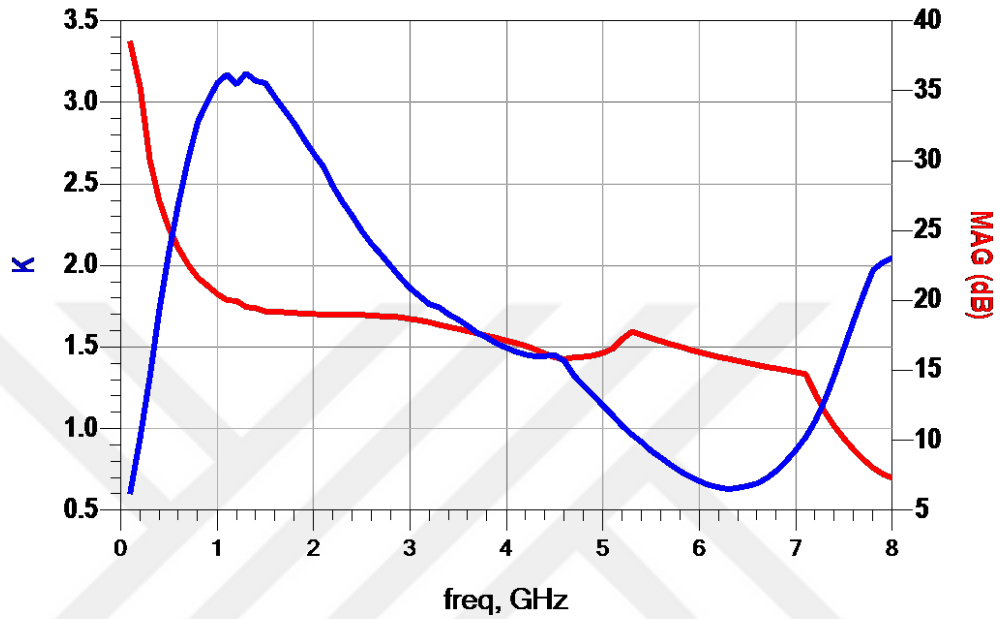


Figure 5.12: Rollett stability factor k and maximum available gain from 100 MHz to 8 GHz

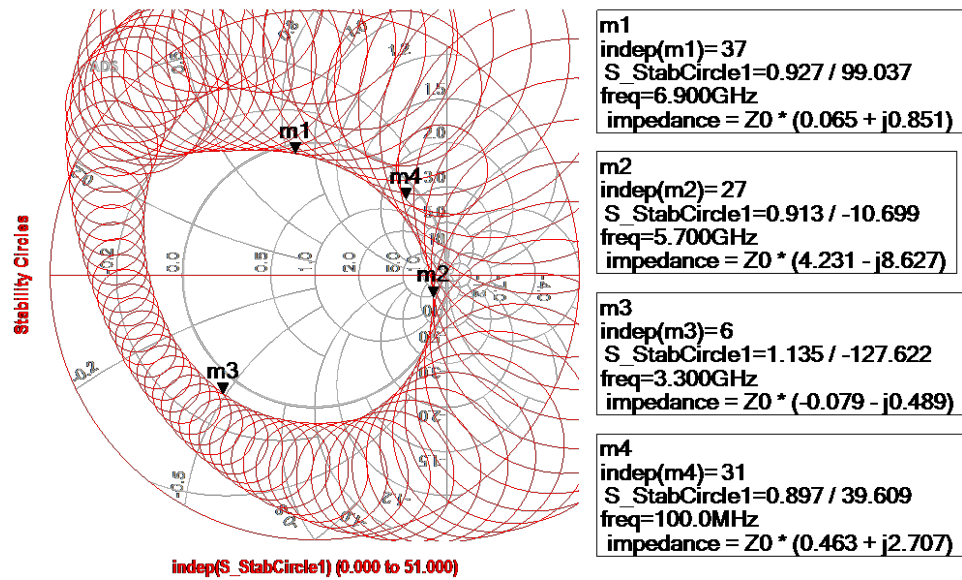


Figure 5.13: Source stability circles from 100 MHz to 8 GHz

Value	Input	Output
470pF	+	+
1uF	+	+
10uF	+	+
33uF		+

Table 5.3: Values of the capacitors in bias lines for stability

may still cause oscillations. By looking at the stability circles, lower frequencies cause oscillations if the input sees an open. Thus, large capacitors will be placed on bias lines to ensure the transistor sees a short circuit at low frequencies. Table 5.3 shows the values of capacitors at gate and drain line added to stabilize the circuit at low frequencies.

Frequencies above 8 GHz are stable for two reasons. Firstly, gain decreases as the frequency of operation increases. Secondly, our capacitor at the stability block is a non-linear element which has a resonance frequency of approximately 4 GHz. This means it will start behave like an inductor at frequencies greater than 4 GHz, thus becoming an open. Therefore, the transistor will only see the resistance. Also, frequencies between 6 to 7 GHz will become stable due to copper losses originating from laminate as the stability circles are almost out of $|\Gamma| = 1$.

5.4.2 Parametric Cells

Although the schematic design offers the needed matching tools, final complete EM simulation of the layout might differ significantly from the schematic design. At microwave frequencies different effects have to be considered which the ideal components neglect. In order to provide a more accurate solution, transmission lines and bends have been simulated in ADS. With components of real behaviour, we then proceed with our design.

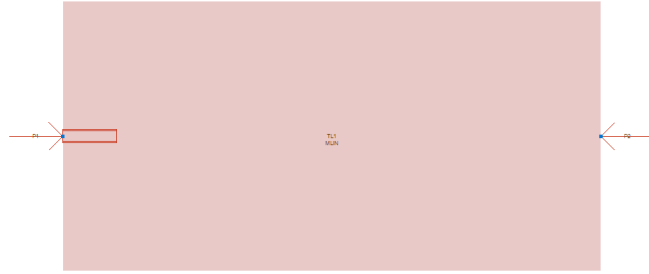


Figure 5.14: Layout of the parametric transmission line

5.4.2.1 Transmission Lines

A transmission line with **W** width and **L** length is defined from ADS Microstrip Library. Figure 5.14 shows the simple layout of transmission line.

From the design parameters screen, **W** and **L** are defined. Figure 5.15 shows the design parameters screen.

S-parameter ports are chosen as TML point ports. TML ports are used when a “long” transmission line will be connected to the port therefore, TML port calibration ignores the open line effects [27]. A point port placed on the edge of a polygon, excites the mesh from that edge. Figure 5.16 shows the port setup.

Frequency range of the simulation is from DC - 10 GHz. Adaptive frequency selection will be used. Finally, Figure 5.17 shows the mesh options for the EM simulation.

With the layout options ready, on the schematic design window, we setup a simulation controller. Width and length sweep range are chosen according to the physical dimensions of the transmission line. Width is swept from 500 μm to 3000 μm which corresponds to characteristic impedance from 75 Ω to 25 Ω . Length is swept from 1000 μm to 27 000 μm which corresponds to electrical length from 5° to 150° at 3 GHz. Figure 5.18 shows the controller circuit.

Resulting parametric data is shown Figure 5.19.

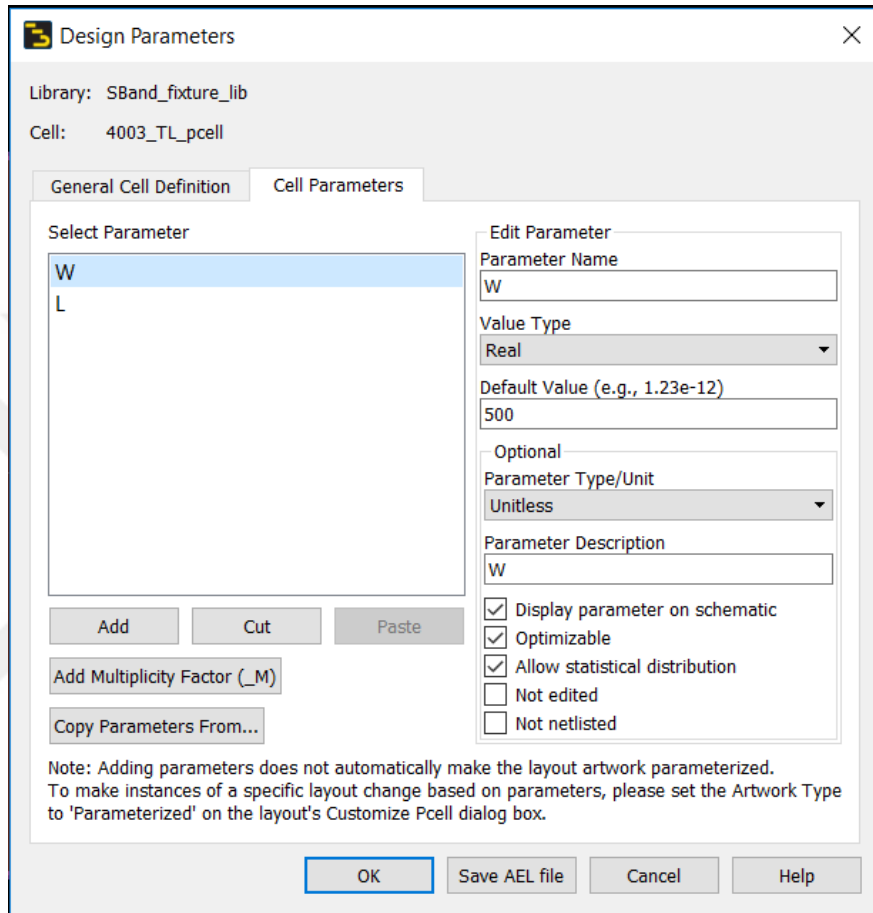


Figure 5.15: Design parameter screen of the parametric cell

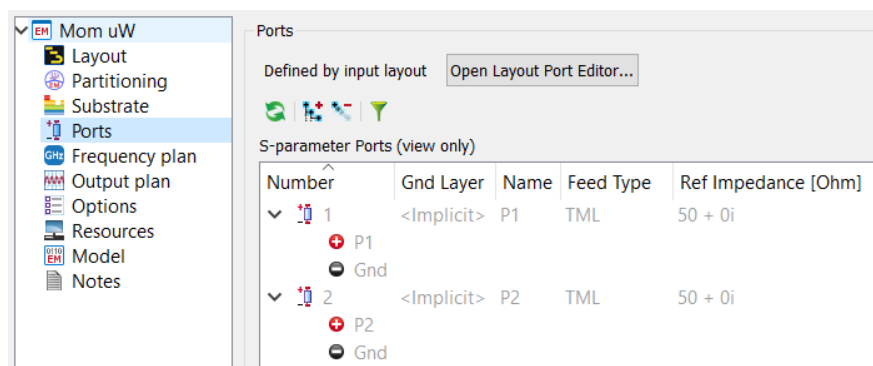


Figure 5.16: Port setup of the transmission line

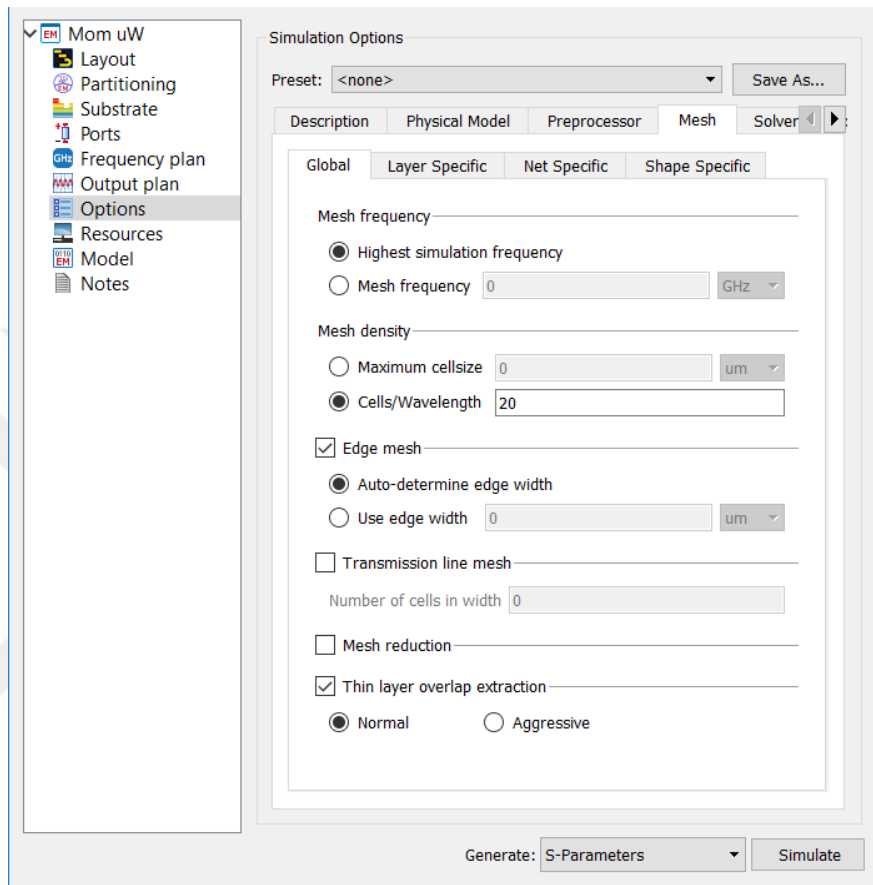


Figure 5.17: Mesh option setup of the transmission line

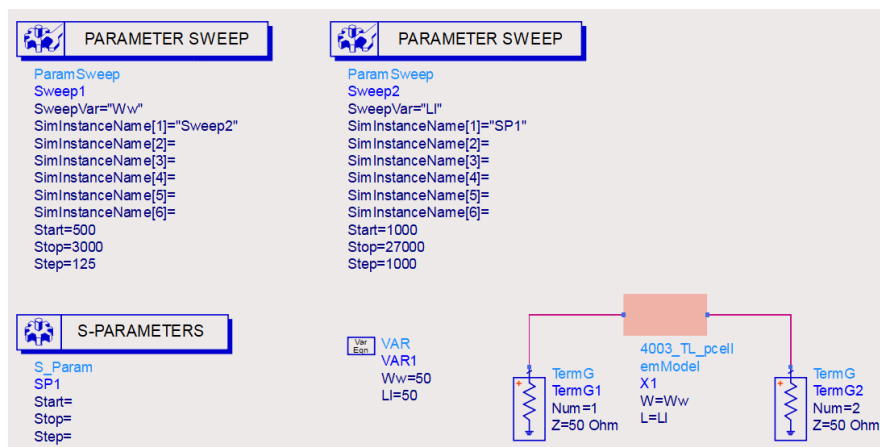


Figure 5.18: Controller schematic of the parametric cell

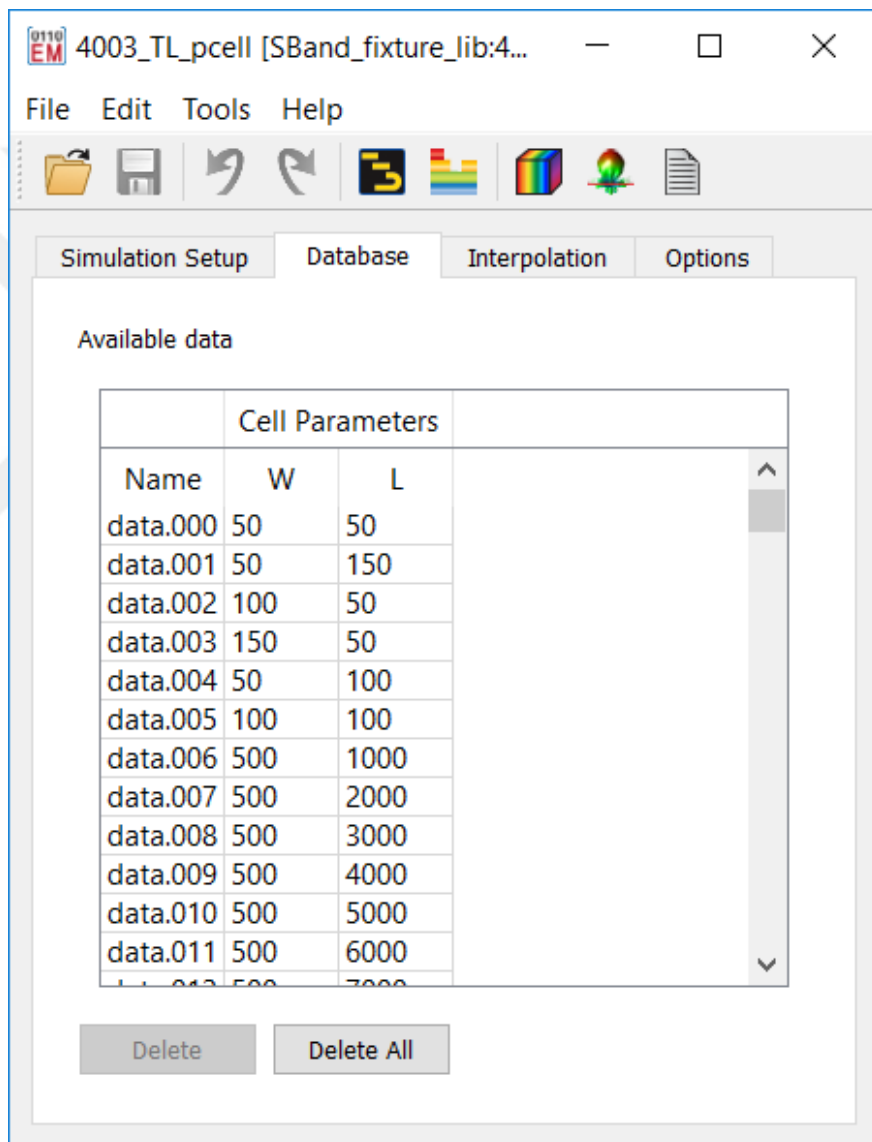


Figure 5.19: EM model data of the parametric transmission lines

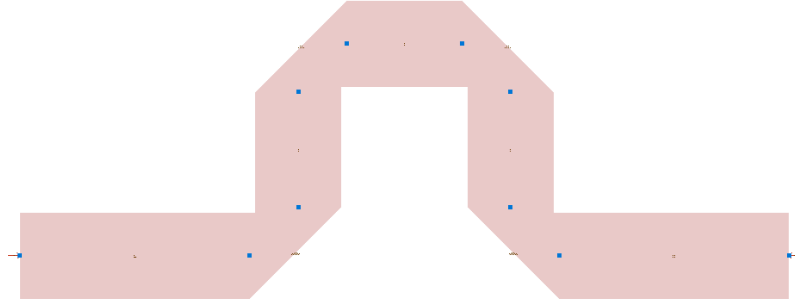


Figure 5.20: Layout of the meandered transmission line

Linear interpolation is done for frequencies where simulation is not available. Thus, a continuous range of values are available for the component.

5.4.2.2 Meandered Transmission Line Parametric Cells

In order to use laminate area more efficiently, long transmission lines are meandered. However, bends introduce parasitic reactance that can affect the circuits performance negatively [2]. Unaccounted bends will affect the phase of the line, and may induce coupling around the corners. In order to compensate for the bends, meandered transmission lines are also parametrized. Figure 5.20 shows the layout of the parametric meandered lined.

With the two parallel lines' distance kept fixed at $1000\text{ }\mu\text{m}$, meandered transmission line is simulated with the same setup as the parametric transmission line.

5.5 Matching

5.5.1 Output Matching

As mentioned previously, PAs deal with high output power. As the output waveform is compressed to produce high output powers, non-linear behaviour become prominent. Specifically, maximum power output impedance and maximum operating gain impedance which are the same in lower input power, diverge at higher input powers. Due to this behaviour, the designer must choose the impedances seen by the device appropriately. For these reasons, rather than matching the device conjugately, device output is matched for max output power.

Figure 5.21 shows constant P_{out} contours at 2 dB compression, 28 V 100 mA at 3 GHz.

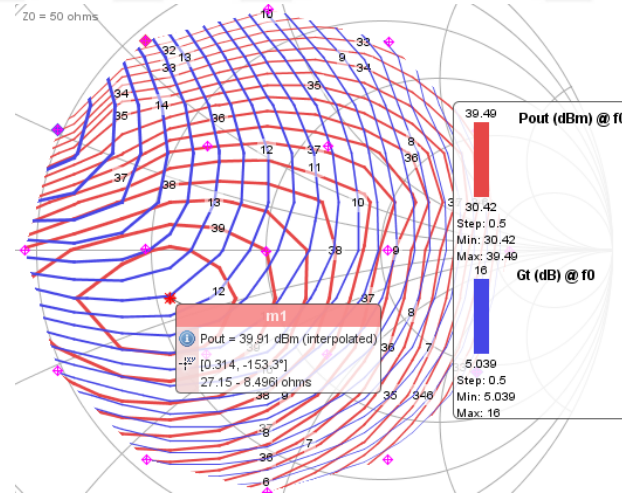


Figure 5.21: Constant P_{out} contours at 2 dB compression, 3 GHz

Figure 5.22 shows constant P_{out} contours at 4 dB compression, 28 V 100 mA.

From the loadpull contours, impedance at maximum P_{out} occurs is 27.15 - 8.5j. To get a compromise between small signal gain and power, we choose the output impedance 25 Ω . But this impedance is seen by the fixture, not the transistor. Therefore, output impedance needs to be transformed to what the transistor sees. Compensating for the fixtures and connectors then de-embedding them, the

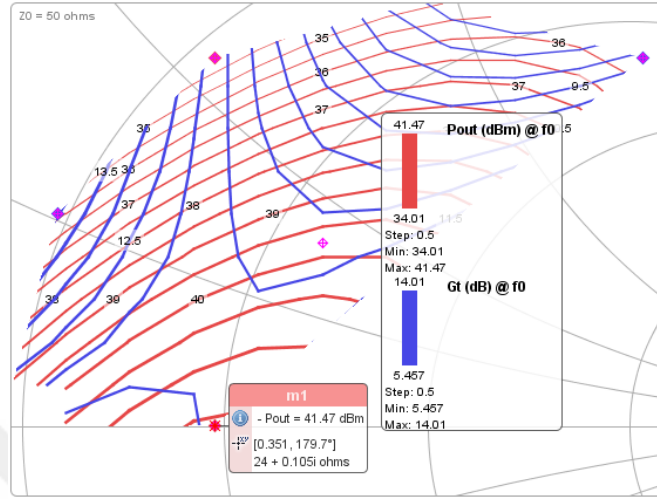


Figure 5.22: Constant P_{out} contours at 4 dB compression, 3 GHz

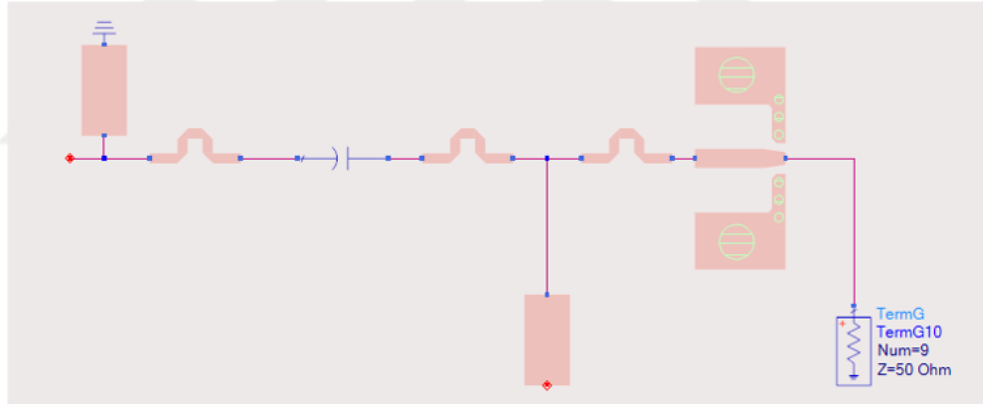


Figure 5.23: Output matching network

output impedance is found to be $28.7 - 11.3j$.

Figure 5.23 shows the proposed output matching circuit.

5.5.2 Input Matching

To decide on a particular topology, we first look at the available gain circles at our center frequency. Another reason to present the max available gain to the transistor is the loadpull measurement. During loadpull, an assumption is made that gate circuit is in linear region and the max power output is somewhat

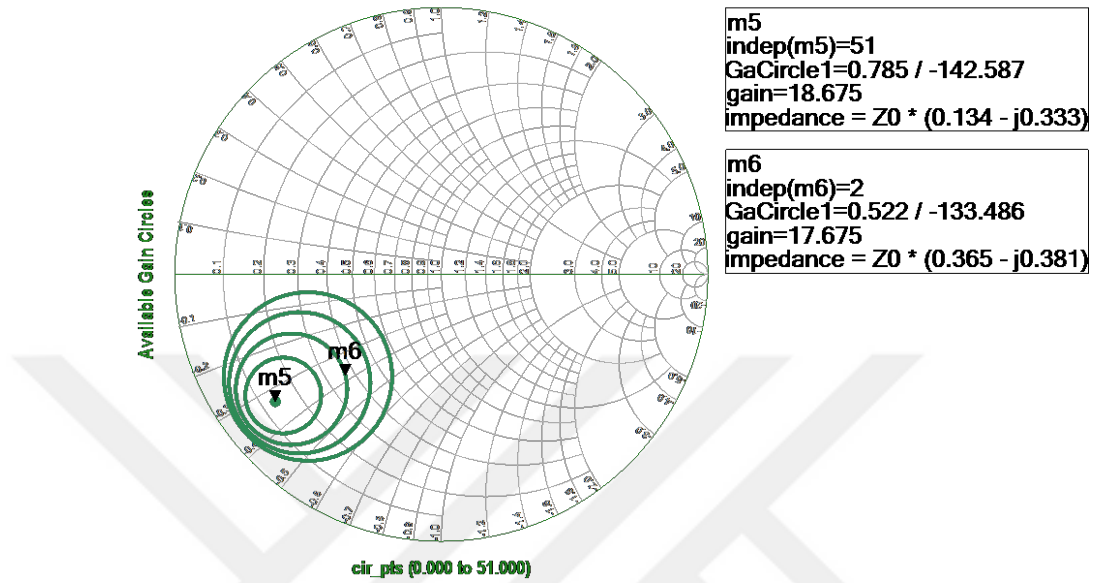


Figure 5.24: Available gain circles at 3 GHz

independent of the input matching. This is not completely true however, but for the majority of the cases, assumption holds. Figure 5.24 shows the available gain circles of the transistor.

From the available gain circle, we deduce that we will use a double open stub circuit for the input matching. However, there are also issues relating to DC biasing which will affect the RF design. Gate bias line has to be added to the circuit. There are two approaches available: use a short quarter wave stub or include the bias network to the matching network. Also, a coupling capacitor has to be implemented to block DC into RF line. Finally, PCB pattern for the end launch connector will be added to the circuit as it is not a perfect $50\ \Omega$.

With these design considerations in mind, Figure 5.25 is the input matching and stability network schematic.

Figure 5.26 is the schematic of the amplifier.

Although, capacitors' s-parameters are available, initial optimization will be done with ideal components, then with the actual device parameters.

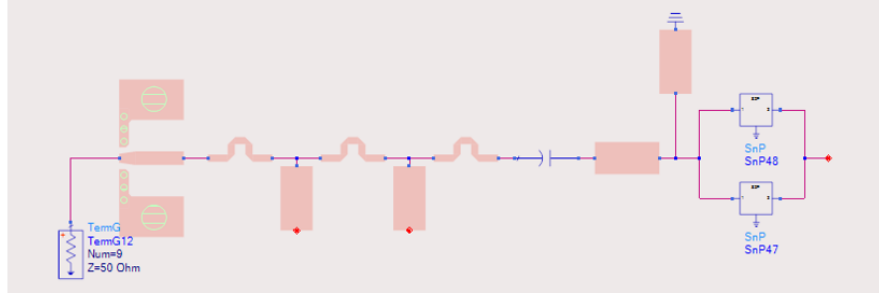


Figure 5.25: Input network

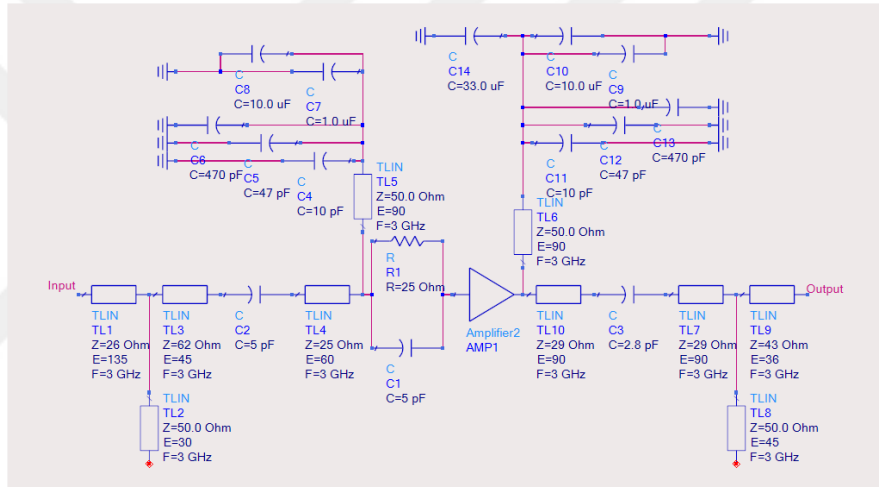


Figure 5.26: Schematic of the amplifier

Full optimization is completed with the goals shown in Table 5.4.

Goal	Min	Max	Frequency
dB(S11)	-	-13	2.7 GHz - 3.5 GHz
dB(S22)	-	-4	2.7 GHz - 3.5 GHz
dB(S21)	14	-	2.7 GHz - 3.5 GHz
$ Z_L - Z_{\text{target}} $	-	0.5	3.1 GHz

Table 5.4: Optimization goals

Figure 5.27 shows the small signal analysis for the final layout.

Figure 5.28 shows the layout of the microwave circuit that's used for EM analysis.

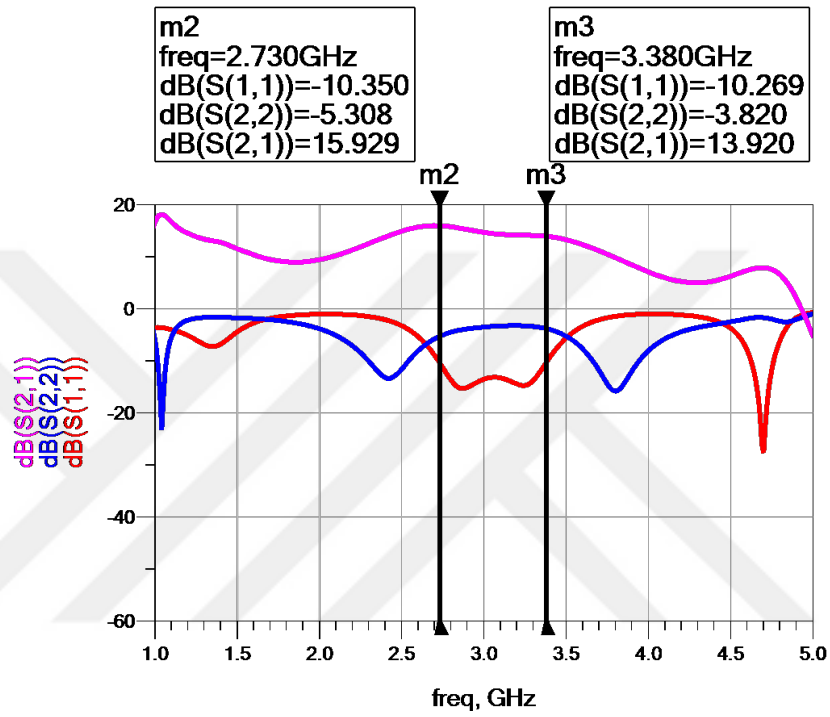


Figure 5.27: Small signal analysis of the full layout

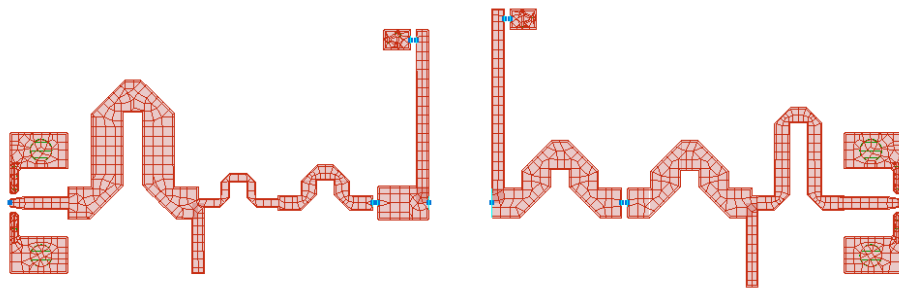


Figure 5.28: Complete layout for simulation

Chapter 6

Realization and Results

In this chapter, final realization of the power amplifier, measurements results and setups are given. Prototyping is finalized and test fixture is presented.

Continuous wave and pulse wave measurements are done under different biases. The amplifier is biased as Class AB and Class B and compressed up to 6 dB from 2.6 GHz to 3.2 GHz. AM/AM distortion, AM/PM distortion and third order intermodulation products are also measured in detail.

Finally, CW power measurement of the second power amplifier, which is built by using CGH40010f, are presented.

6.1 Realization

Before tape-out and manufacturing, layout used to simulate the behaviour of the circuit has to be prepared for the final process. DC components, feed lines, via holes, screw holes are all placed and accounted for in the final phase. Figure 6.1 shows the final layout pre-manufacturing.

Finalized layout is then exported as Gerber files, to start manufacturing on the

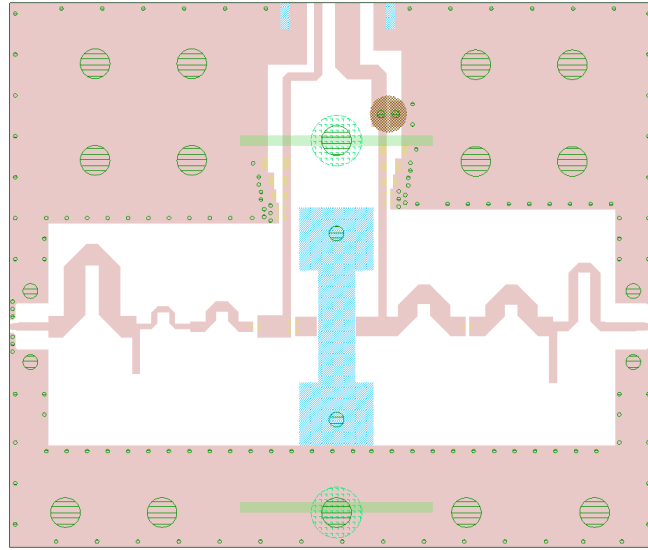
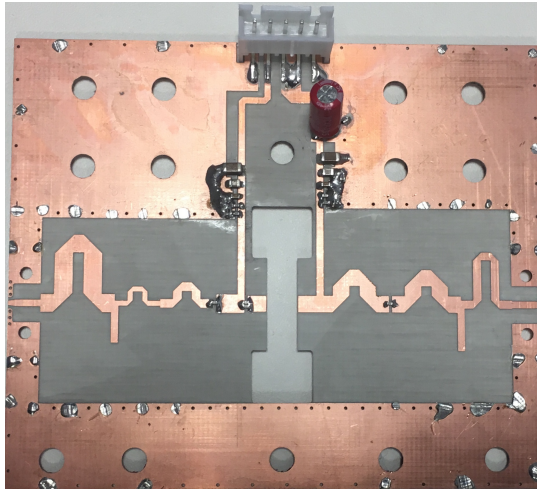
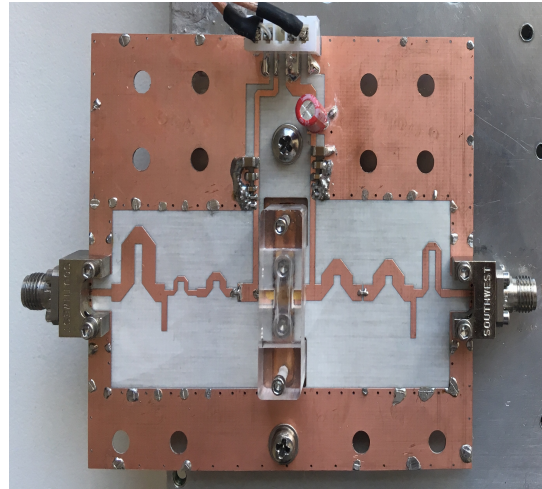


Figure 6.1: Final layout before tape-out

rapid prototyping bench. Figure 6.2a shows the PCB with all surface components attached. Figure 6.2b shows the final fixture.



(a) Completed PCB



(b) Final fixture

6.2 Measurement

6.2.1 Small Signal Analysis

6.2.1.1 Setup

Small signal measurement setup consists of one Rohde & Schwarz VNA and two Agilent DC power supplies. The VNA is calibrated via 2-port connectorized TOSM standards.

6.2.1.2 Measurement

PA is biased at 28 Volts with 3 different currents: 100 mA, 200 mA and 350 mA with 200 μ s pulse. Figure 6.3 shows resultant small signal measurements of the PA.

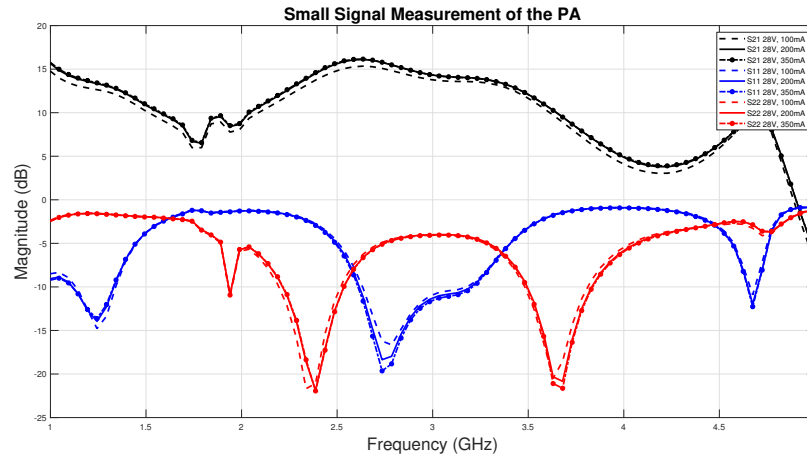


Figure 6.3: Small signal measurement under different biases

Figure 6.4 compares Keysight ADS simulation results with the measurement at 28 V 350 mA.

Looking at Figure 6.4, we can say that the center frequency has shifted down

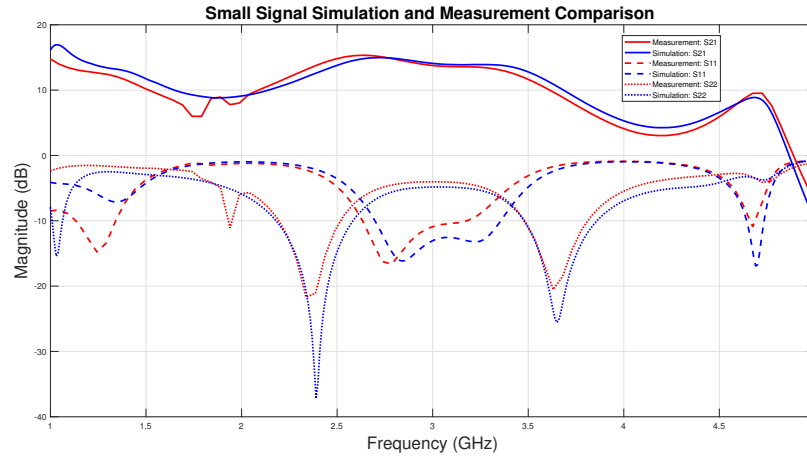


Figure 6.4: ADS results compared with small signal measurement

by 100 MHz. Additionally, the input return loss has suffered. This is due to the unaccounted effects of device packages, solder losses and connector discontinuities.

6.2.2 Power and AM/AM Distortion

Power measurements are done under different bias points. 6 dB compression point is chosen as the maximum input power to compare frequencies.

6.2.2.1 Setup

Figure 6.5 shows the vector based loadpull setup [28]. Unlike a traditional scalar loadpull setup, VNA based loadpull allows the measurement of a_1 , b_1 and a_2 , b_2 signals at every frequency. As the VNA sees the input and output of the device through couplers, we can look for oscillations and mismatches. Moreover, VNA also allows us to precisely determine what impedance the tuners present to the device without de-embedding since the couplers are at the reference plane.

By setting the tuners $50\ \Omega$, we can measure the power while also measuring the a and b parameters.

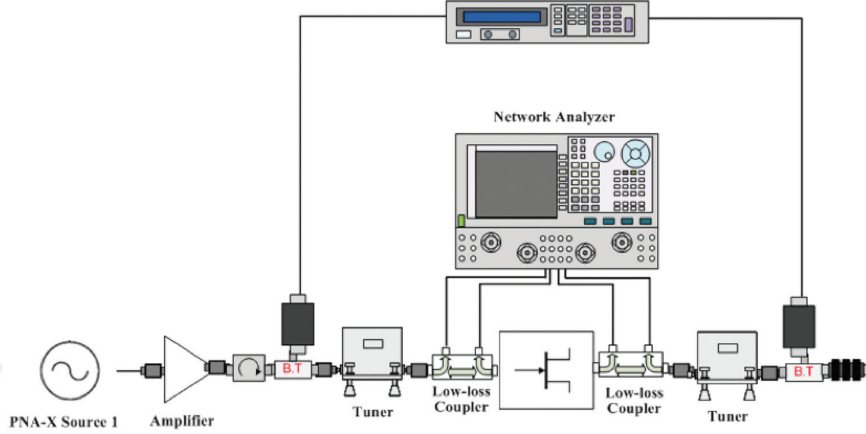


Figure 6.5: Vector receiver based loadpull setup [28]

6.2.2.2 AM/AM and Efficiency Measurement at 3 GHz

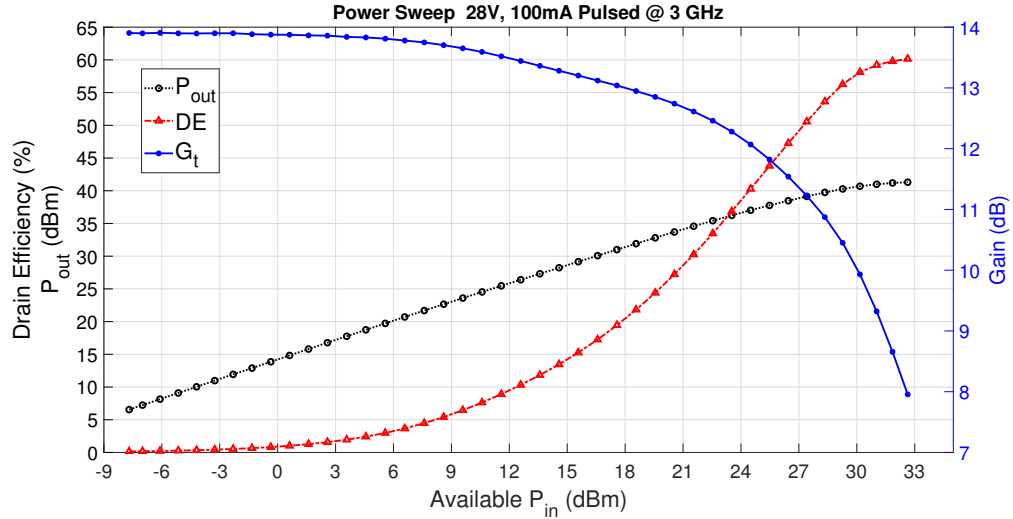


Figure 6.6: Pulsed power sweep @ 28 V, 100 mA

At 28 V 100 mA, Figure 6.6, an output power rating of 41 dBm, that is 12.6 W is observed, under 6 dB compression. Small signal gain of almost 14 dB and a drain efficiency of 60 % are delivered.

At 28 V 0 mA, Figure 6.7a drain efficiency is observed to be 61 %. We have reached an output power rating of 41.21 dBm, that is 13.2 W, under 3.5 dB compression (note that this compression is calculated from the highest gain point). Peak small signal gain of 11.32 dB is observed.

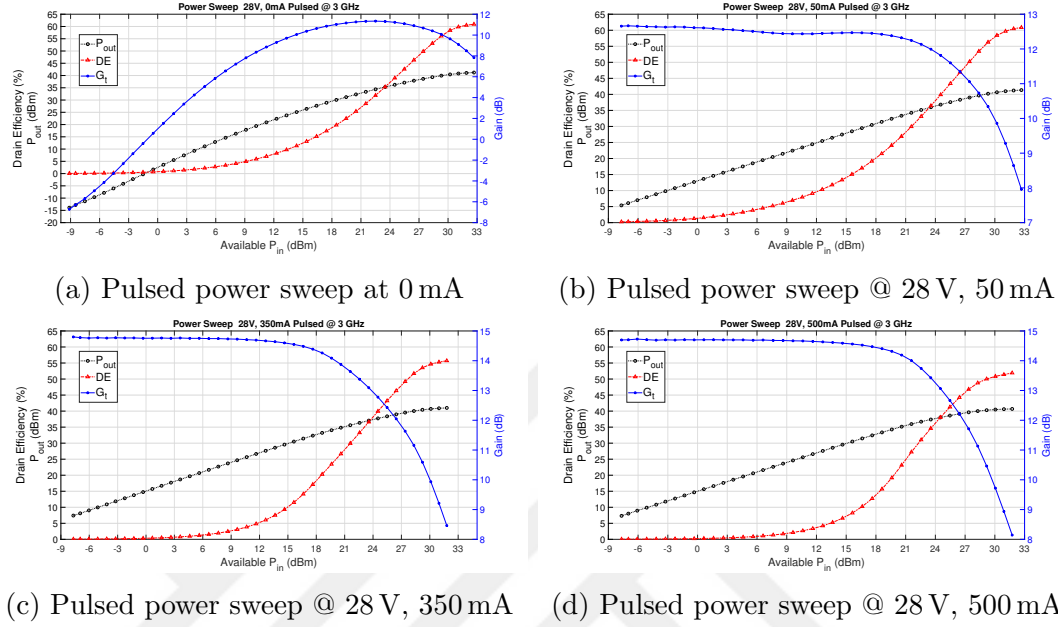


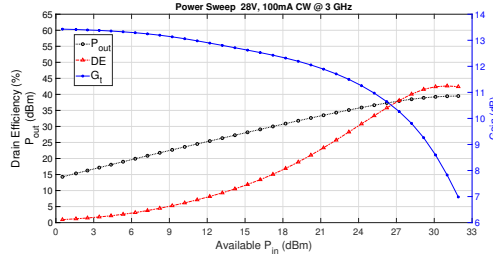
Figure 6.7: Pulsed power sweep under different bias points

At 28 V 50 mA, Figure 6.7b, we have reached an output power rating of 41.34 dBm, that is 13.6 W, under 4.5 dB compression. Small signal gain of 12.6 dB is observed but most importantly a drain efficiency of 61 % is delivered. Power density is recorded as 5.4 W/mm.

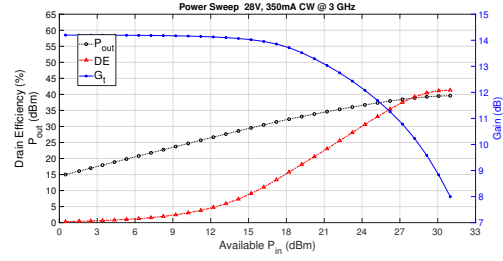
At 28 V 350 mA, Figure 6.7c, we have reached an output power rating of 41 dBm, that is 12.6 W under 6 dB compression. Small signal gain of 14.7 dB is observed but most importantly a drain efficiency of 56 % is delivered.

At 28 V 500 mA, Figure 6.7d, first thing to be noticed is the significant drop in efficiency at 52 %. We have reached an output power rating of 40.68 dBm, that is about 12 W under 6 dB compression. Small signal gain of 14.7 dB is observed.

During continuous operation, thermal dissipation and increase in temperature degrade device performance. This causes a drop in output power. Also, due to non-linearities involved, continuous operation power impedances are not necessarily the same as pulsed impedances. At 28 V 100 mA, Figure 6.8a, P_{out} is measured as 39.49 dBm, 9 W, at 6.43 dB compression. 13.43 dB small signal gain and 42.63 % peak drain efficiency is noted as significantly lower than pulsed



(a) Power sweep, CW 28 V, 100 mA



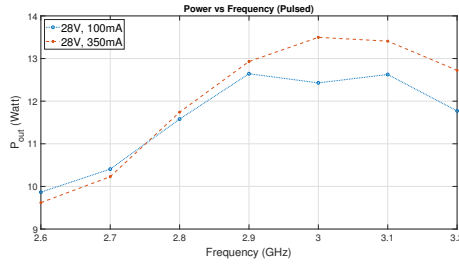
(b) Power sweep, CW 28 V, 350 mA

Figure 6.8: CW power sweep under different bias points

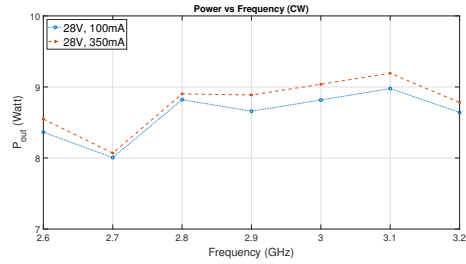
operation.

At 28 V 350 mA, Figure 6.8b, drain efficiency decreased to 41.32 %. We have reached an output power rating of 39.59 dBm, that is 9.1 W, under 6 dB compression. Small signal gain of 14.2 dB is observed.

6.2.2.3 P_{6dB} vs Frequency



(a) Pulsed P_{6dB} vs frequency



(b) CW P_{6dB} vs frequency

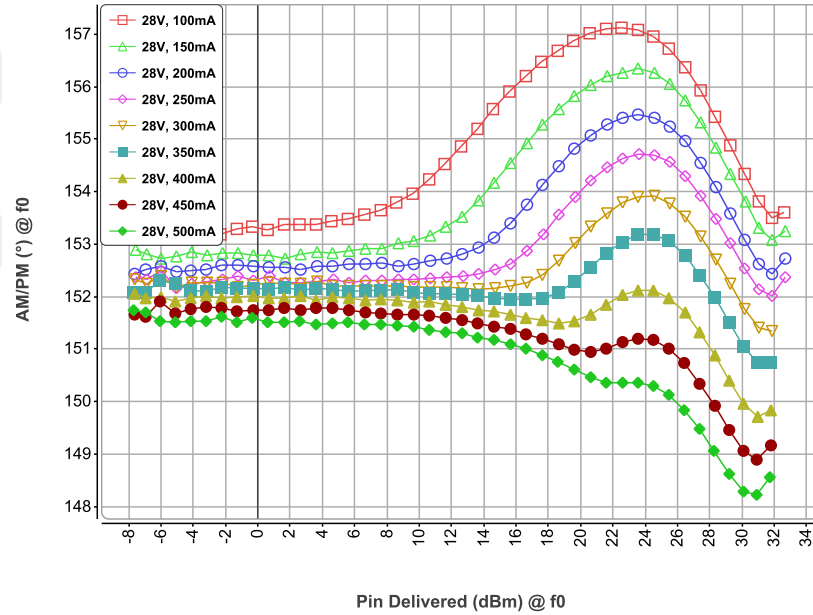
Figure 6.9: P_{6dB} vs Frequency

Pulsed and continuous mode operation power measurements over the frequency band Figure 6.9a, Figure 6.9b show that 28 V 350 mA is slightly higher in output power compared to 28 V 100 mA which is expected as a higher portion of the input signal is amplified in the former bias point. A significant difference between pulsed and continuous wave operation is the output power. Continuous wave operation has significantly low power output because thermal effects and increasing channel temperature degrade device performance.

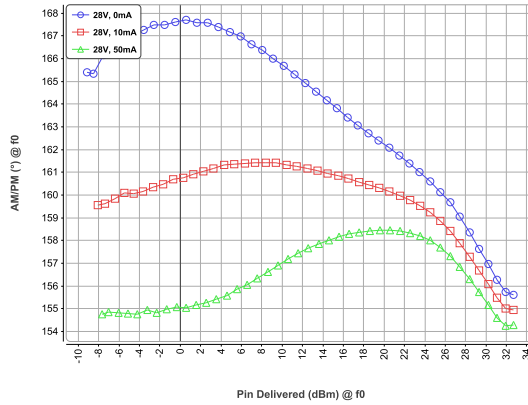
6.2.3 AM/PM Distortion

VNA based loadpull allows us to measure AM/PM while measuring the power since the VNA measures a and b parameters during power sweep. Therefore, we can measure the input and output signal's phase and amplitude simultaneously.

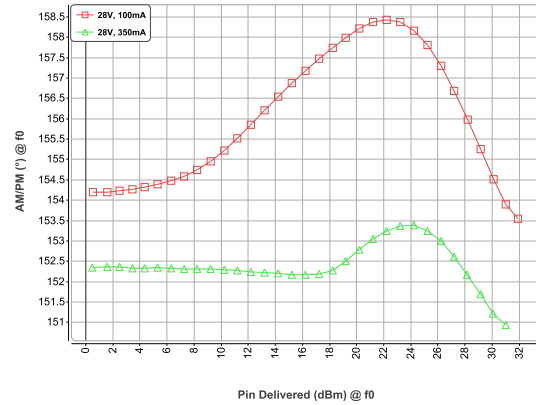
6.2.3.1 Measurement



(a) AM/PM measurement under 200 μ s pulse



(b) Pulsed AM/PM measurement 0 mA



(c) CW AM/PM measurement

Figure 6.10: AM/PM Measurements

We measured AM-to-PM distortion under different bias points to observe their effect on linearity, Figure 6.10a. Maximum AM-to-PM distortion was calculated as $0.7^\circ/\text{dB}$. Also, for $P_{6\text{dB}}$, phase of the reference bias(100 mA) is the same for small signal operation and maximum power. In addition, same measurement is also done for CW operation, Figure 6.10c.

In order to present the effect of different classes, the same measurement is also done under low current bias points, Figure 6.10b. Maximum AM-to-PM distortion of $1^\circ/\text{dB}$ is measured. The total phase difference between small signal and large signal operation is found as 10° .

6.2.4 Intermodulation Products

6.2.4.1 Setup

The setup consists of one Agilent N5183A Signal Generator, one Hittite HMC-T2000 signal generator, a Rigol DC supply and an Agilent E4440A spectrum analyzer. Figure 6.11 is a picture of the setup.

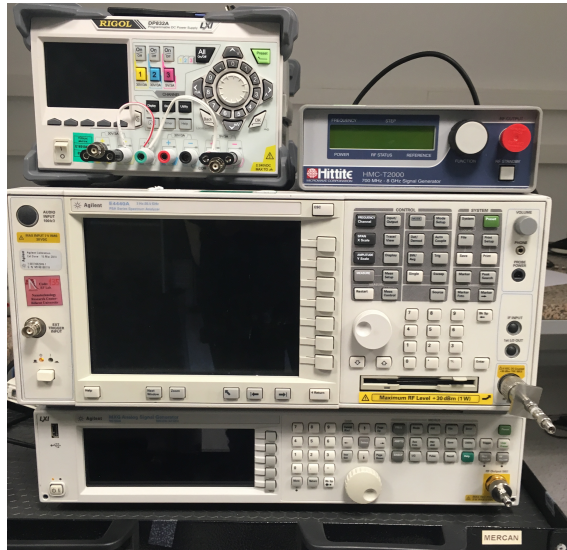
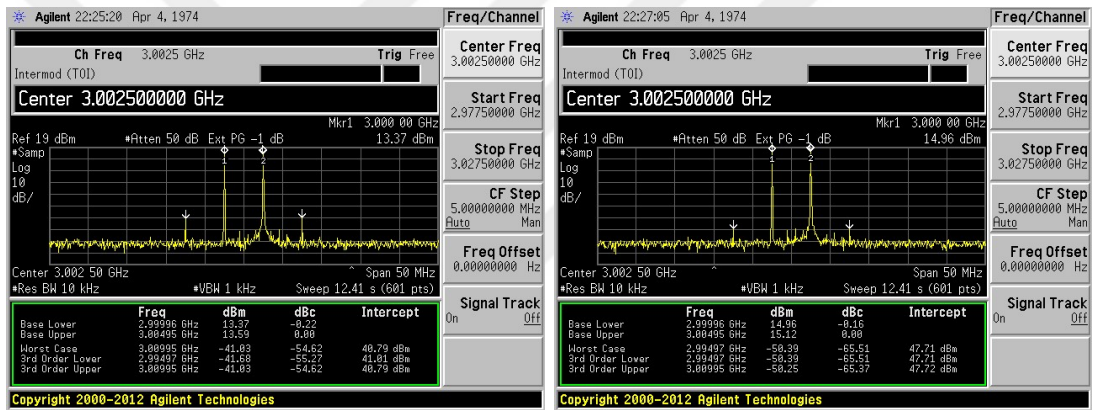


Figure 6.11: Picture of the IP3 measurement setup

6.2.4.2 IP3 Measurement

Measurement of the intermodulation products is required to observe the effects harmonic signals which cannot be filtered out. Especially for communication applications where different frequencies are utilized to get more bandwidth for data transmission. Two different bias points, 100 mA and 350 mA, are chosen for this measurement to demonstrate the effect of different classes. Third order intercept point is found as 40.8 dBm and 47.7 dBm respectively.



6.2.5 CGH40010f

6.2.5.1 Small Signal Measurement

At 2.3 GHz center frequency we have measured a small signal gain of 14.7 dB. Bandwidth, specified for input return loss greater than 10 dB is from 1.9 GHz to 2.6 GHz.

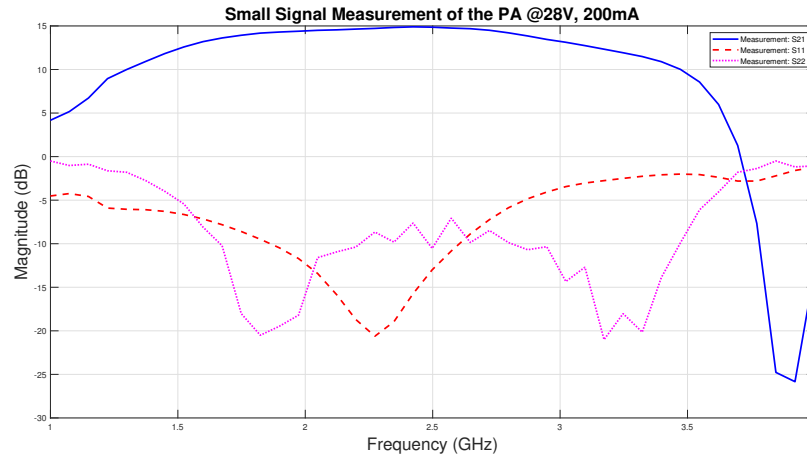


Figure 6.13: Small signal measurement of the PA built with CGH40010F

6.2.5.2 AM/AM and Efficiency Measurement at 2.25 GHz

We have measured the AM/AM compression character for two different bias points, 28 V 200 mA and 28 V 350 mA to observe different behaviour.

At 28 V 200 mA, Figure 6.14, we have reached 13.6 W output power and 10.43 dB gain at 4.27 dB compression. Amplifier started with soft compression in lower input power slowly moved to deep compression. Peak drain efficiency was 65 %.

At 28 V 350 mA, Figure 6.15, we have reached 14.3 W output power and 10.39 dB gain at 4.23 dB compression. It is noted that soft compression is no

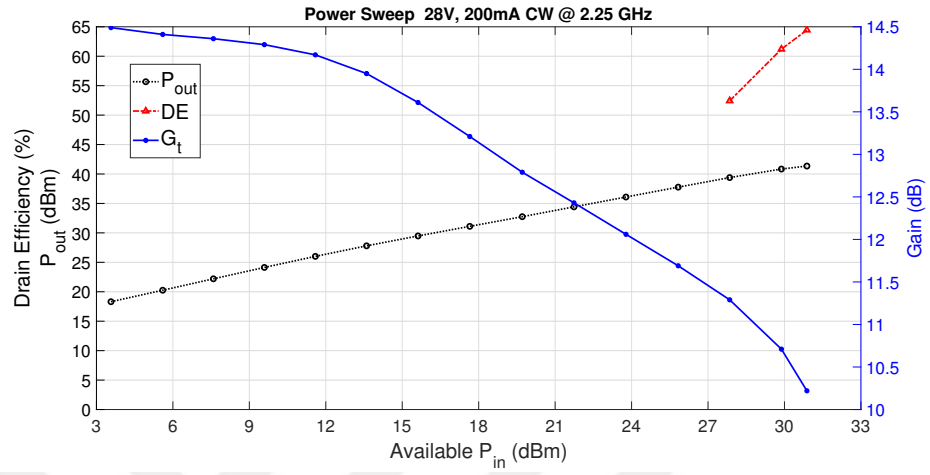


Figure 6.14: CW power sweep at 28 V 200 mA

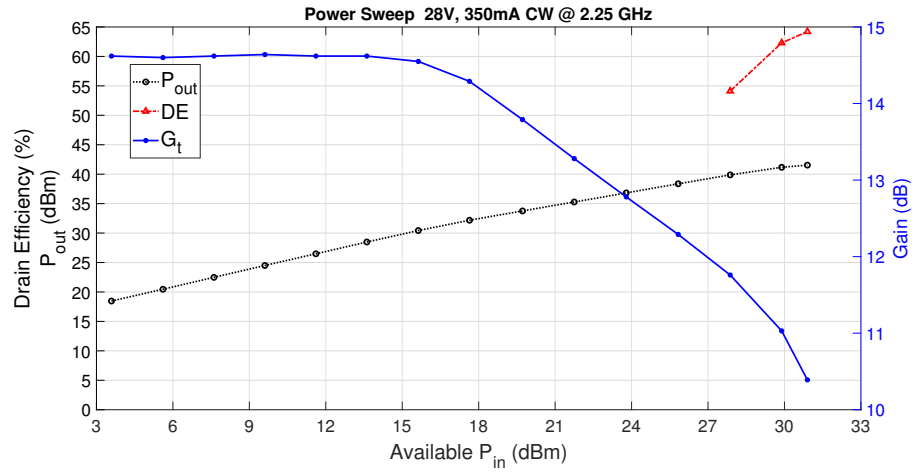


Figure 6.15: CW power sweep at 28 V 350 mA

longer present and the amplifier is linear for low input power. Peak drain efficiency was 64.8%.

Chapter 7

Conclusion

High power RF Microwave amplifiers are used in various applications such as the telecommunications, defense and aerospace industries. For most systems, relatively, they handle most of the available system power, therefore their efficiency and heat generation greatly affect the overall system design.

Wide bandgap materials such as GaN offer great improvement for solid state power amplifiers. Specifically, GaN as a semiconductor which offers high breakdown voltages, high power density, better form factor and thermal performance promise significant development in this area. In our work, we designed and manufactured a power amplifier based on GaN HEMT technology for wireless systems and communications. By using a GaN HEMT built in NANOTAM, we have built the amplifier. We used a $10 \times 250 \mu\text{m}$ internally unmatched discrete die. We compared the peripheral performance of our amplifier with other research groups.

In Chapters 1, 2 and 3 we focused on giving a general background for GaN technology and power amplifier fundamentals. In chapter 4, we explained a progress of how a packaged GaN HEMT is characterized empirically. In Chapter 5, we provided how a matching and optimization is conducted through models using the fundamentals explained in prior chapters.

Detailed measurements and the behaviour of the PA was given in Chapter 6. We provided the peak power over frequency, efficiency, AM/AM measurements both CW and pulse. AM/PM and third order intermodulation products on the center frequency were measured to provide a linearity analysis of the PA. Different bias points under CW and pulse operations were taken to measure their effects on all measurements. Thus, we also included their effects on the overall amplifier behaviour. In this work, we have empirically characterized a 2.5 mm GaN HEMT built in NANOTAM, successfully built a hybrid amplifier. Results for another hybrid amplifier built with a commercial transistor were also offered. We measured output powers over 13 Watts at the centre frequency 3 GHz. That totalled to a peak density of 5.4 W/mm. Small-signal gain greater than 14.5 dB has been measured. From our power amplifier built with CGH40010f, we have reached a 14.3 W output power and 10.39 dB gain.

Last but not least, GaN technology will be the main prospect for solid state high power microwave amplifier applications. As the power density and power per chip area of GaN devices are unrivalled, issues that were previously not considered such as high thermal dissipation will need to be addressed in the future. Nonetheless, GaN technology stands out to be the future. As many research and commercial parties are working on GaN MMIC technology, especially the industries which need mass production such as 5G phased array systems and system on chip solutions will benefit much thanks to this technology.

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