BROADBAND GAN LNA MMIC DEVELOPMENT WITH THE MICRO/NANO PROCESS DEVELOPMENT BY KINK-EFFECT IN S_{22} CONSIDERATION

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By

Sinan Osmanoğlu

January 2021

Broadband GaN LNA MMIC Development with the Micro/Nano Process Development by Kink-Effect in S_{22} Consideration
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We certify that we have read this dissertation and that in our opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

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ABSTRACT

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Ph.D. in Electrical and Electronics Engineering
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January 2021

Broadband *low noise amplifiers* (LNA) are one of the key components of the numerous applications such as communication, electronic warfare, and radar. The requirements for higher bandwidth, higher speed, higher survivability, higher reliability, etc. pushes the technological boundaries. The demand for high performance circuit components without a compromise stimulates the utilization of the high-end *gallium nitride* (GaN) technology to develop better *monolithic microwave integrated circuits* (MMIC) in a smaller footprint. To support the progress, the development of a proper GaN *high electron mobility transistor* (HEMT) technology and proper circuit models have become critical. To support the efforts and contribute to the progress, a 0.25 μm *microstrip* (MS) GaN HEMT technology is developed in Bilkent University Nanotechnology Research Center (NANOTAM). The technology development yields that the MS GaN HEMT technology is capable of supporting $\geq$4.4 W/mm *output power* (P_{OUT}), $\geq$50% *power added efficiency* (PAE), $\geq$15 dB gain, and $\sim$1 dB *noise figure* (*NF*) at 10 GHz. Moreover, the gate structure of the technology is studied by evaluating the *kink-effect* (KE) in the output reflection coefficient (S_{22}) of a HEMT to support the broadband operation. Besides the technology development, the *small-signal* (SS) and noise equivalent circuit models are studied, and the developed models present high convergence with the measurements. The accuracy of the models contributes to development of the cascode HEMT based LNAs even without fabricating the cascode HEMT. Furthermore, the developed models and the proper gate structure are used to develop the broadband *quad-flat no-leads* (QFN) packaged GaN LNA MMIC for the mobile radio communications, the military radar, and the commercial radar applications. The results of the circuit models and the GaN LNA MMIC also yield that the developed MS GaN HEMT technology is capable for developing different solutions up to 18 GHz.

Keywords: Broadband, GaN, HEMT, Kink-effect in S_{22}, LNA, Noise.

ÖZET

S_{22}'DE GÖZLENEN KİNK-ETKİSİ DİKKATE ALINARAK GENİŞBANTLI GAN LNA MMIC VE MİKRO/NANO PROSES GELİŞTİRİLMESİ

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Genişbantlı *düşük gürültülü yükselteçler* (LNA) iletişim, elektronik harp ve radar uygulamaları gibi çeşitli alanlarda anahtar devre elemanlarından biridir. Yüksek bant genişliği, yüksek hız, yüksek dayanıklılık ve yüksek güvenilirlik ihtiyaçları teknolojik sınırları zorlamaktadır. Performans kaybı olmaksızın talep edilen yüksek performanslı devre elemanlarına olan ihtiyaç yüksek teknoloji *galyum nitrür* (GaN) teknolojisyle geliştirilecek iyileştirilmiş performansa sahip, daha az yer kaplayan *yekpare mikrodalga entegre devre* (MMIC) olan talebi artırmaktadır. İlerlemeyi destekleyebilmek adına doğru GaN temelli *yüksek elektron hareketlilikli transistör* (HEMT) teknolojisinin ve uygun devre modellerinin geliştirilmesi kritik öneme sahiptir. Çalışmaları destekleyebilmek ve ilerlemeye katkı sağlayabilmek adına 0.25 μm kapı teknolojisine sahip *mikroşerit* (MS) GaN HEMT teknolojisi Bilkent Üniversitesi Nanoteknoloji Araştırma Merkezi (NANOTAM) bünyesinde geliştirilmiştir. Geliştirilen MS GaN HEMT teknolojisi çıkıtları teknolojinin 10 GHz test koşullarında $\geq$4.4 W/mm *çıkış gücüne* (P_{OUT}), $\geq$%50 *güç ekli verimliliğe* (PAE), $\geq$15 dB kazanca ve $\sim$1 dB *gürültü faktörüne* (NF) sahip olduğunu göstermektedir. Ayrıca, genişbantlı uygulamaları destekleyebilmek adına transistör kapı yapısı *çıkış yansıma katsayısı*nda (S_{22}) görülen *kink-etkisi* (KE) ile ilişkili olarak çalışılmıştır. Gerçekleştirilen çalışmaların yanısıra, ölçüm sonuçları ile yüksek doğruluğa sahip *küçük-işaret* (SS) ve gürültü eşdeğer devreleri geliştrilmiştir. Kaskod HEMT yapısı daha önce üretilmemesine rağmen geliştiren devre modellerinin yüksek doğruluğa sahip olması sayesinde kaskod HEMT yapısına sahip LNA geliştirme çalışmalarına katkı sağlamıştır. Ayrıca, geliştirilen devre modelleri ve KE etkisini en aza indirgeyen kapı yapısı kullanılarak mobil iletişim, savunma amaçlı ve ticari amaçlı radar uygulamalarında kullanılabilecek QFN paketli GaN LNA MMIC yapısı geliştirilmiştir. Elde edilen çıktıların yanısıra, ulaşılan sonuçlar geliştirilen MS GaN HEMT teknolojinin 18

GHz'e kadar geliştirilebilecek uygulamalar için çeşitli çözümler sunabileceğini göstermektedir.

Anahtar sözcükler: GaN, Genişbant, Gürültü, HEMT, LNA, S_{22}'de kink-etkisi.

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Chapter 1

Introduction

Modern communication, electronic warfare, and space technologies require more performance than ever. Therefore, the integrated circuit technologies have gained more interest to support applications with the amplifiers that have less noise, more power, more efficiency, more linearity, and more bandwidth in a small footprint. Furthermore, thermal requirement, reliability, and process yield have become very critical.

These challenges constantly push the technological boundaries and elevate the demand for better technological solutions. Thus, the *gallium nitride* (GaN) *high electron mobility transistor* (HEMT) technology has gained significant importance in the industry as a consequence of its superior material properties [1–3].

It is well known that the GaN HEMT technology has high power densities [4]. Moreover, the *noise figure* (*NF*) performance of the GaN HEMT technology is approaching to GaAs [5]. However, the GaN HEMT technology requires improvements to support the technological progress to develop better *monolithic microwave integrated circuit* (MMIC) solutions.

The GaN HEMT technology offers different MMIC solutions for different frequency ranges in the frequency spectrum shared in Fig. 1.1 [5]. Nevertheless, the *low noise amplifier* (LNA) MMICs have gained more attention in the last decade.

As depicted in Fig. 1.2, an LNA is a very critical component of a generic *radio frequency* (RF) transceiver system [6].

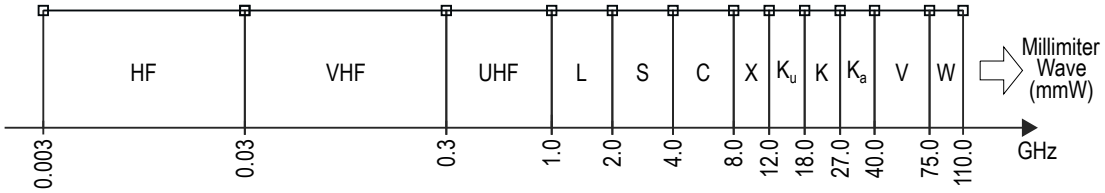


Figure 1.1: IEEE RF Spectrum in logarithmic scale.

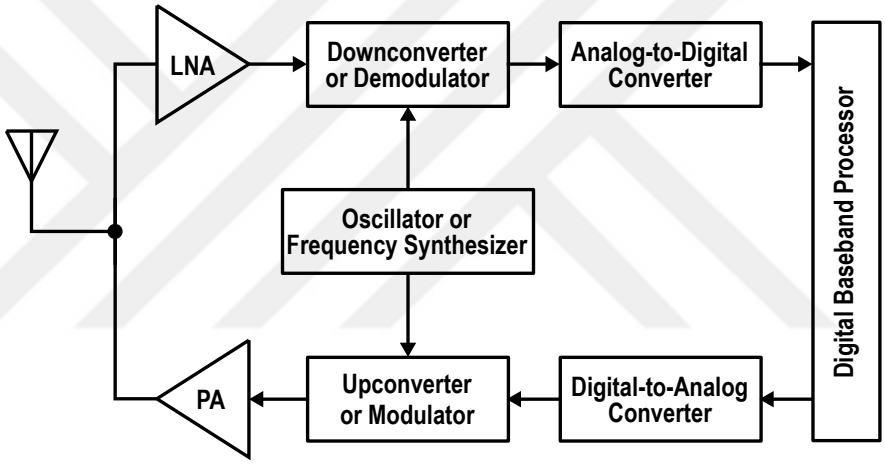


Figure 1.2: A generic RF transceiver block diagram.

In an RF transceiver system, the signal is captured by the antenna and sensed by the LNA and transferred to the demodulator or the downconverter on the receiver side. The LNA is a critical component on the receiver side, since the detectable weakest signal is determined by the *NF* performance of the LNA. An LNA is increasing the signal power with an expense of noise power as depicted in Fig. 1.3 [7]. Thus, the added noise (N_A) by the LNA determines the performance of the receiver.

The *noise factor* (F) and *NF* terms are often used to state the noise performance of an amplifier or a system. The F is the ratio of the input and the output *signal-to-noise ratios* (SNR):

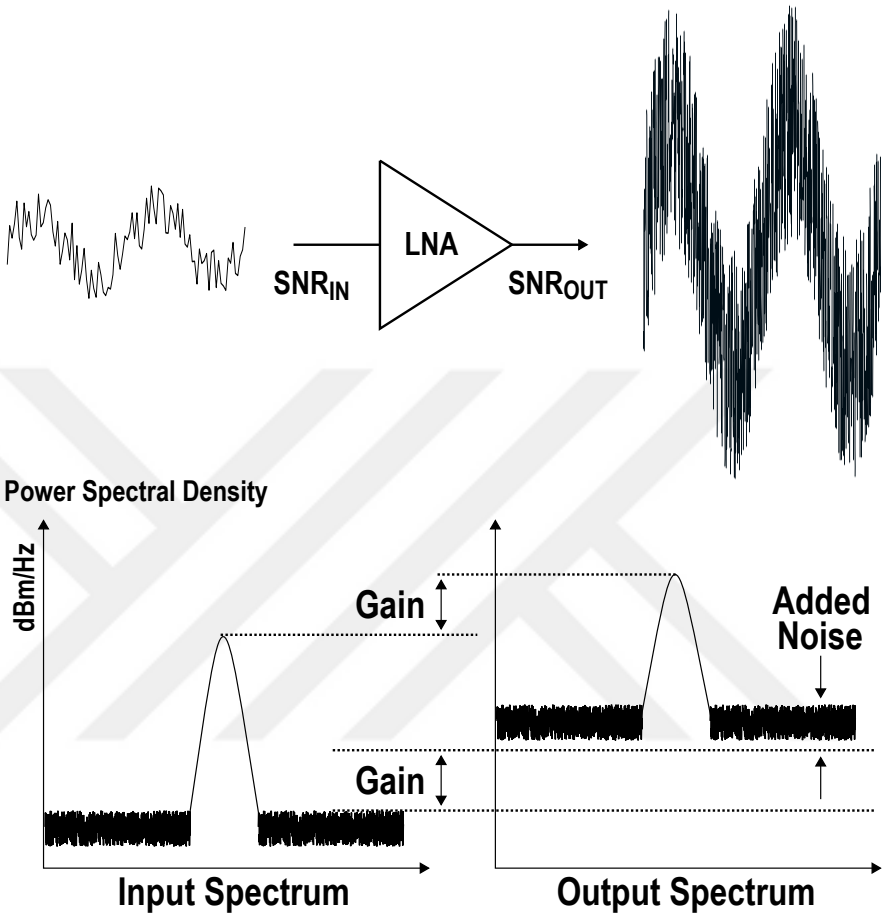


Figure 1.3: Representation of noise figure of an LNA with the corresponding power spectral density.

$$F = \frac{SNR_{IN}}{SNR_{OUT}} \tag{1.1}$$

while the NF is the F expressed in *decibels* (dB)

$$NF = 10log(F) \tag{1.2}$$

The F in a cascaded system can be expressed as:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \tag{1.3}$$

where F_n and G_n are the noise factor and the gain of the related stage, respectively.

The cascaded F equation clearly shows that the first stage is the most critical part of a system. If the first stage is a passive component, then the overall noise is increased by the amount of the noise of the component. Therefore, the GaN technology offers a better solution in comparison to *gallium arsenide* (GaAs) technology as depicted in Fig. 1.4. The GaN LNA technology do not require a limiter, increases the F, at the input of the LNA instead of a GaAs LNA [8].

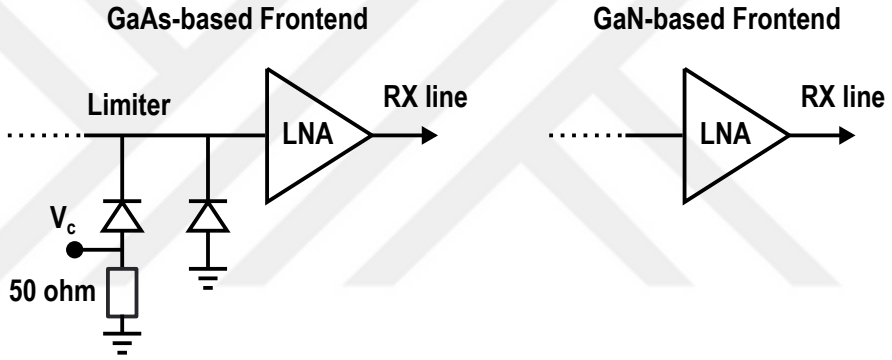


Figure 1.4: Representation of generic GaAs-based and GaN-based frontend.

1.1 The Motivation and the Organization of the Thesis

There were very limited GaN LNA solution for the frequency below 300 MHz, since the GaN HEMT technology is not mature yet. Thus, the motivation of the thesis is to develop a proper GaN LNA solution for portable and mobile radios operating at different frequency ranges, and L-band radar applications. To do that, a proper 0.25 μm *microstrip* (MS) GaN HEMT technology, proper *small-signal* (SS) and noise equivalent circuit models, and MMIC packaging is studied. Moreover, the *kink-effect* (KE) in the output reflection coefficient (S_{22}) is investigated in terms of the gate structure to improve the bandwidth of the amplifiers which can be designed with the developed technology. It has been shown that it is possible to design a broadband cascode LNA MMIC from the

developed model of the common-source HEMT. Moreover, it has also been shown that the gate structure has an important effect to develop a broadband process by reducing KE in S_{22}.

The rest of the thesis is organized as follows:

In Chapter 2, the development of 0.25 μm MS GaN HEMT is explained and the achieved performance is shared. Moreover, the device development and necessary parameters to control the quality of the process are explained.

In Chapter 3, the small-signal and the noise equivalent circuit model development process of a *common-source* (CS) HEMT are demonstrated. Both the extrinsic and the intrinsic parameter extraction considering the proper calibration techniques and the proper *NF* measurement system are explained.

In Chapter 4, the kink-effect in S_{22} that limits the broadband design is explained. The proper gate structure and the proper bias selection are discussed for a kink free HEMT development.

In Chapter 5, the development of a broadband GaN LNA MMIC starting from a concept cascode HEMT is discussed. The noise model development of a cascode HEMT is also explained. Moreover, the packaging and the application board design are demonstrated with the performance evaluation of the GaN LNA MMIC.

Chapter 6 summarizes the obtained findings in the previous chapters and outlines the future directions, and possible challenges.

Chapter 2

Device and Process Development

The micro/nano-fabrication process is developed according to the requirements of the targeted application areas. Since different applications require different devices during the design process, a proper micro/nano-fabrication process has to be developed to meet device requirements.

The micro/nano-fabrication process steps are needed to be defined to fabricate the defined devices. The number of the metal layers and the number of the insulator layers are the main parameters of a process. The resolution of the micro/nano-fabrication process steps plays an important role on the performance of the devices, since the performance of the devices are frequency dependent. Therefore, the photo-resist types must be suitable with the resolution requirements. Furthermore, the photo-masks have to be designed considering the resolution requirements and the types of the photo-resists.

To define a proper micro/nano-fabrication process flow, each process step has to be coherent with the previous and the next step. Thus, proper alignment has to be performed during the fabrication.

This chapter discusses the required active and passive devices and describes the process flow. Furthermore, the measurement results of the developed devices are shared to show the achived performance.

2.1 GaN RF Technology

Gallium-Nitride (GaN) high electron mobility transistor (HEMT) technology has superior properties, such as high power density, high efficiency, high saturation carrier velocity, high breakdown field, and high thermal conductivity [1, 9–11]. These properties make GaN technology highly preferable for the space applications, the defense industry applications, and the commercial products [2,3,12,13].

The comparison of the material technology is given in Table 2.1 [14–16]. Si, Sapphire, and SiC are the preferred substrates for GaN HEMT technology [1,17–22]. However, SiC is mainly used for the best power performance because of its high thermal conductivity [23–25]. Furthermore, diamond is also being used as a substrate for niche applications [25–28].

Table 2.1: The comparison of the RF semiconductor material properties

Semiconductor	E_g (eV)	n_i (cm^{-3})	ϵ_r	μn ($cm^2/V.s$)	E_c (MV/cm)	V_{sat} ($10^7 cm/s$)	λ (W/cm.k)	Direct (D) Indirect (I)
Si	1.1	1.5e10	11.8	1350	0.3	1.0	1.5	I
Ge	0.66	2.4e13	16.0	3900	0.1	0.5	0.6	I
GaAs	1.4	1.8e6	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	7.7e-1	11.1	350	1.3	1.4	0.8	I
InP	1.86	∼1e3	9.6	3000	1.0	2.5	-	D
GaN	3.39	1.9e-10	9.0	900	3.3	2.5	1.3	D
3C-SiC	2.2	6.9	9.6	900	1.2	2.0	4.5	I
4H-SiC	3.26	8.2e-9	10	720^a 650^c	2.0	2.0	4.5	I
6H-SiC	3.0	2.3e-6	9.7	370^a 50^c	2.4	2.0	4.5	I
Diamond	5.45	1.6e-27	5.5	1900	5.6	2.7	20	I
BN	6.0	1.5e-31	7.1	5	10	10^*	13	I
AlN	6.1	∼1e-31	8.7	1100	11.7	1.8	2.5	D

a: mobility along the a-axis, c: mobility along the c-axis, *: estimate

The high power and high efficiency performance GaN HEMT technology allows to develop Power Amplifiers (PA) with more than 80 W output power (P_{OUT}) utilizing 0.25 μm gate technology in X-Band [29–31]. On the other hand, it is also possible to develop PA with 30 W PA with 60% Power Added Efficiency (PAE) with 0.15 μm GaN HEMT technology [32].

2.1.1 GaN Technology RF Noise Performance

Noise performance of GaN technology approaches GaAs technology with the recent advancements in GaN technology and the reduction in gate size [33–35]. The properties of GaN technology make it feasible to develop LNAs with wide bandwidth, high survivability, high gain, and high linearity. Therefore, many low noise amplifiers (LNA) at different frequencies are developed using GaN HEMT technology in recent years [8, 36–44]. Moreover, multiple studies have shown that GaN based LNAs have more than 20 dB higher survivability than GaAs LNAs with a high breakdown field [8, 36, 37].

It is possible to achieve less than 1 dB Noise Figure (NF) with 0.25-μm GaN/SiC HEMTs at 10 GHz with the recent advancements in GaN HEMT technology [34]. These performance advancements make it possible to design GaN LNA MMICs with less than 2 dB in X-Band [45–47].

2.2 Active and Passive Device Design

2.2.1 Active Devices

Active devices are the devices which can utilize an active layer to inject power into the circuit. They have the ability of controlling electron flows in the active region by electrical signal. A circuit must contain at least one active device to be properly called as electronic.

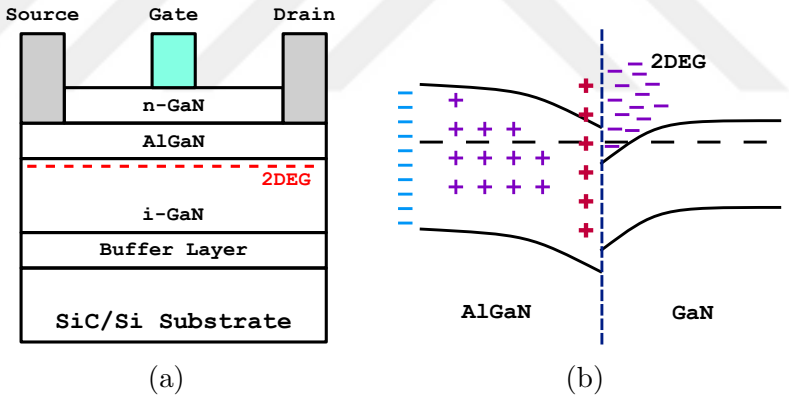
High Electron Mobility Transistor (HEMT) utilizes the superior properties of gallium nitride (GaN) technology with its special configuration.

HEMT: HEMT using GaN technology has very high efficiency as GaN material has wide band gap [48]. GaN technology have very high breakdown voltage levels which can support operation at high supply voltage levels. By these properties, GaN technology reaches higher power densities than the GaAs technology and

the other technologies.

The GaN HEMT as depicted in Fig. 2.1a utilizes high-density two-dimensional electron gas (2DEG). 2DEG is accumulated between GaN and AlGaN boundary layer through their natural polarization and piezoelectric effect [49,50]. The band diagram is depicted in Fig. 2.1b. It is possible to obtain low on-state resistance (R_{on}) thanks to the 2DEG. Moreover, the combination of low R_{on} and high gate-drain breakdown voltage (V_{br}), the GaN HEMT presents excellent RF power performance [50].

GaN HEMT is a depletion mode device by the nature. Thus, a GaN HEMT is normally on and negative gate-source voltage (V_{gs}) less than the pinch-off voltage (V_p) is required to turn-off the device.



(a) (b)

Figure 2.1: (a) Basic GaN HEMT configuration, (b) Energy band diagram of a GaN HEMT

By considering the structural properties of HEMT, mainly two types of HEMTs are designed and their photomasks are prepared for nanofabrication process. Design of those HEMTs based on microstrip (MS) and co-planar waveguide (CPW) technologies. The main difference in between two of them is MS HEMTs require backside via for ground connection, while the ground plane of CPW HEMTs are on the same plane with the actual devices as depicted in Fig. 2.2.

Both MS and CPW types of HEMTs are configured in different number of gate fingers to investigate on relation between gate size and total gate finger. MS type HEMTs have circular via-holes with specific diameter to guarantee that

inside of via-holes will be properly covered with metal. That also simplifies nano-fabrication process.

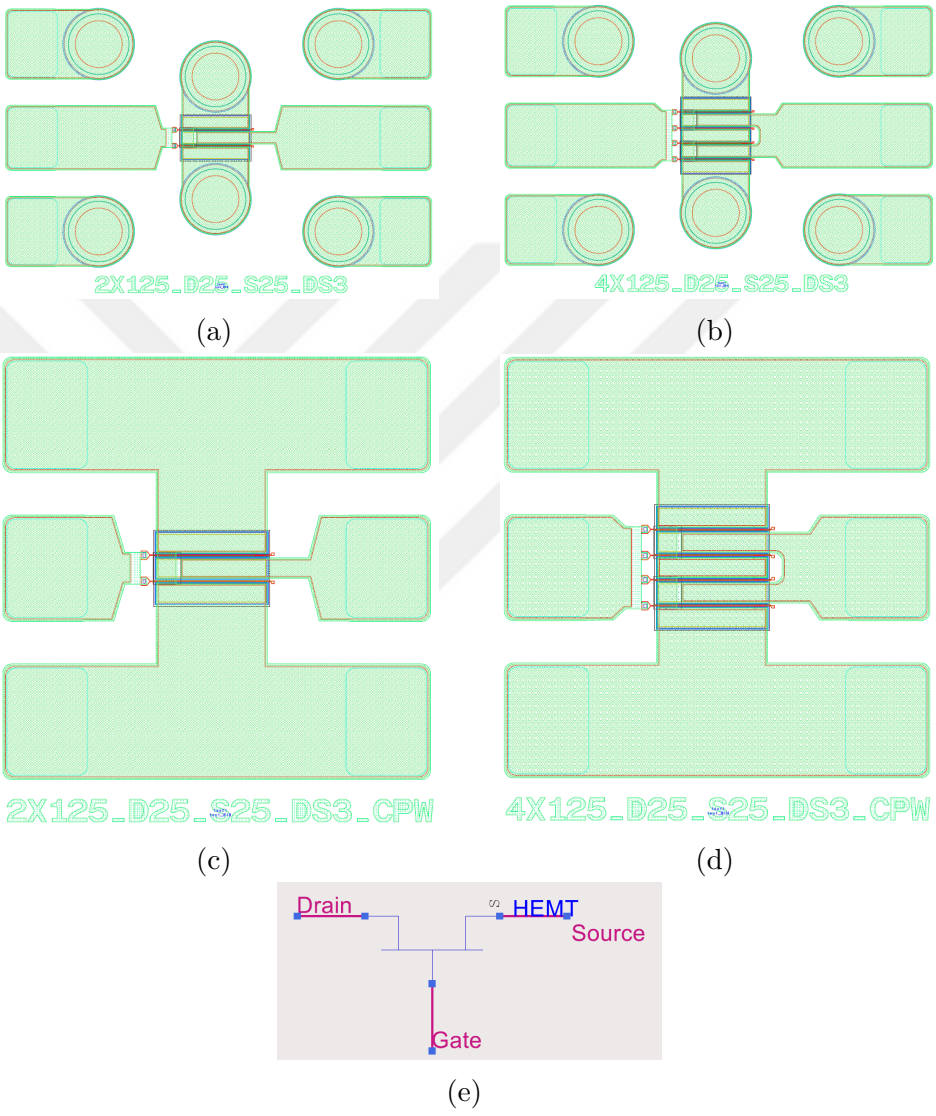


Figure 2.2: (a) 2×125 μm microstrip, (b) 4×125 μm microstrip, (c) 2×125 μm CPW, (d) 4×125 μm CPW GaN HEMT layouts, and (e) Circuit symbol

2.2.2 Passive Devices

On the contrary of an active device, passive devices do not have the ability to control electron flow by any kind of electrical signal. Therefore, resistors, capacitors, inductors, transmission lines and even diodes are called as passive devices in electronics.

Resistors:
A resistor is one of the simplest circuit elements in electronics. They have linear current and voltage relations. The slope of the IV curve of a resistor gives its resistance value.

The most common type of resistor in the integrated circuits is the *thin-film-resistor* (TFR). The sheet resistance (R_{sh}) of TFRs generally changes in between 10-50 $\Omega/\square$. To build a several kΩ resistor with TFRs requires too much space in any monolithic circuit. Therefore, the epi resistor (EPI-RES) which utilises the 2DEG in GaN technology, is used in the monolithic integrated circuits (MIC) to build several kΩ resistors. The epi layer has very high sheet resistance in comparison with TFR. Sheet resistance of EPI-RES is generally in between 250-500 $\Omega/\square$.

Both TFR and EPI-RES are very useful for different operations, so different sizes of TFRs and EPI-RESs are designed and their photomask is generated. The layouts of the TFRs and the EPI-ERSs are given in Fig. 2.3.

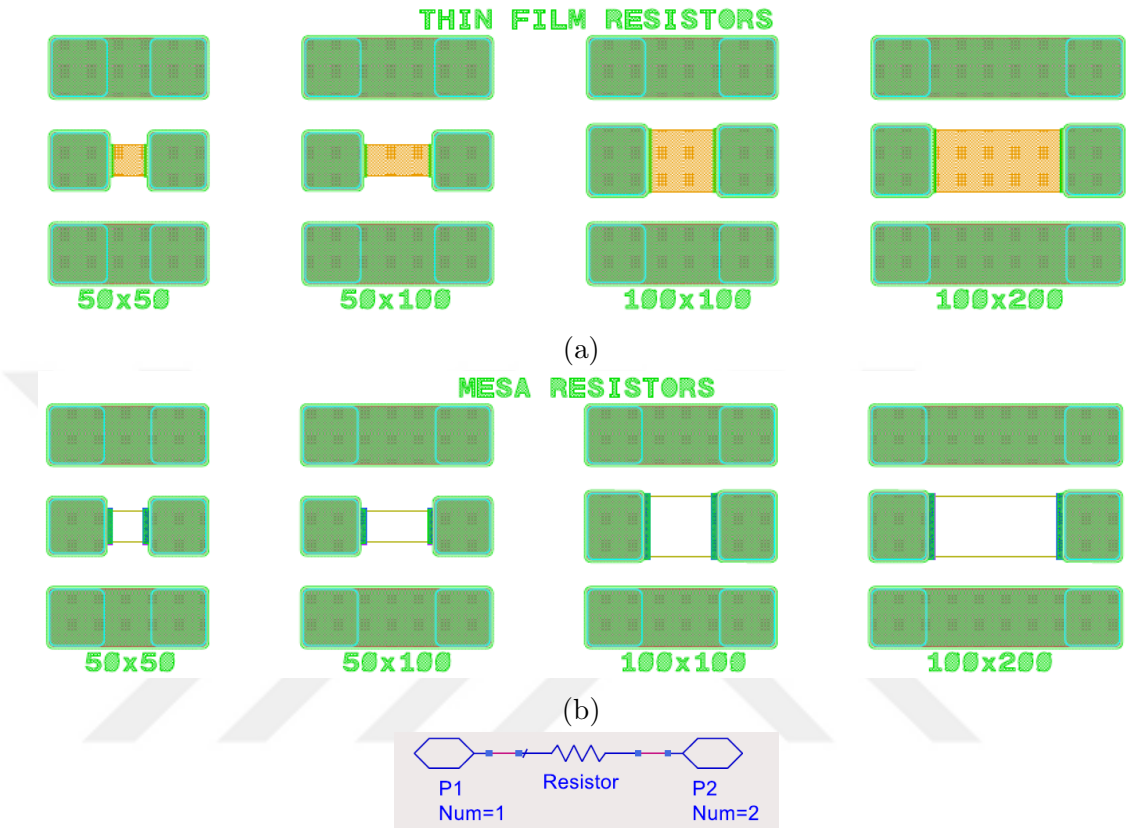


Figure 2.3: The layouts of (a) TFRs, (b) EPI-RESs in different sizes, and (c) the circuit symbol

Capacitors:

A capacitor is one of the two-terminal passive circuit elements. A simple capacitor has two conducting plates which are separated by a dielectric from each other and has the ability of storing electrical energy in an electric field.

Integrated circuits use *metal-insulator-metal* (MIM) combination by stacking them on top of each other to create an MIM capacitor. Therefore, integrated circuits require at least two metallization layers to form the capacitors. According to those specific requirements, MIM-CAPs designed in different sizes to characterize both capacitance density in pF/mm and dielectric properties like dielectric constant and loss tangent value. Different types of designed MIM-CAPs are depicted in Fig. 2.4.

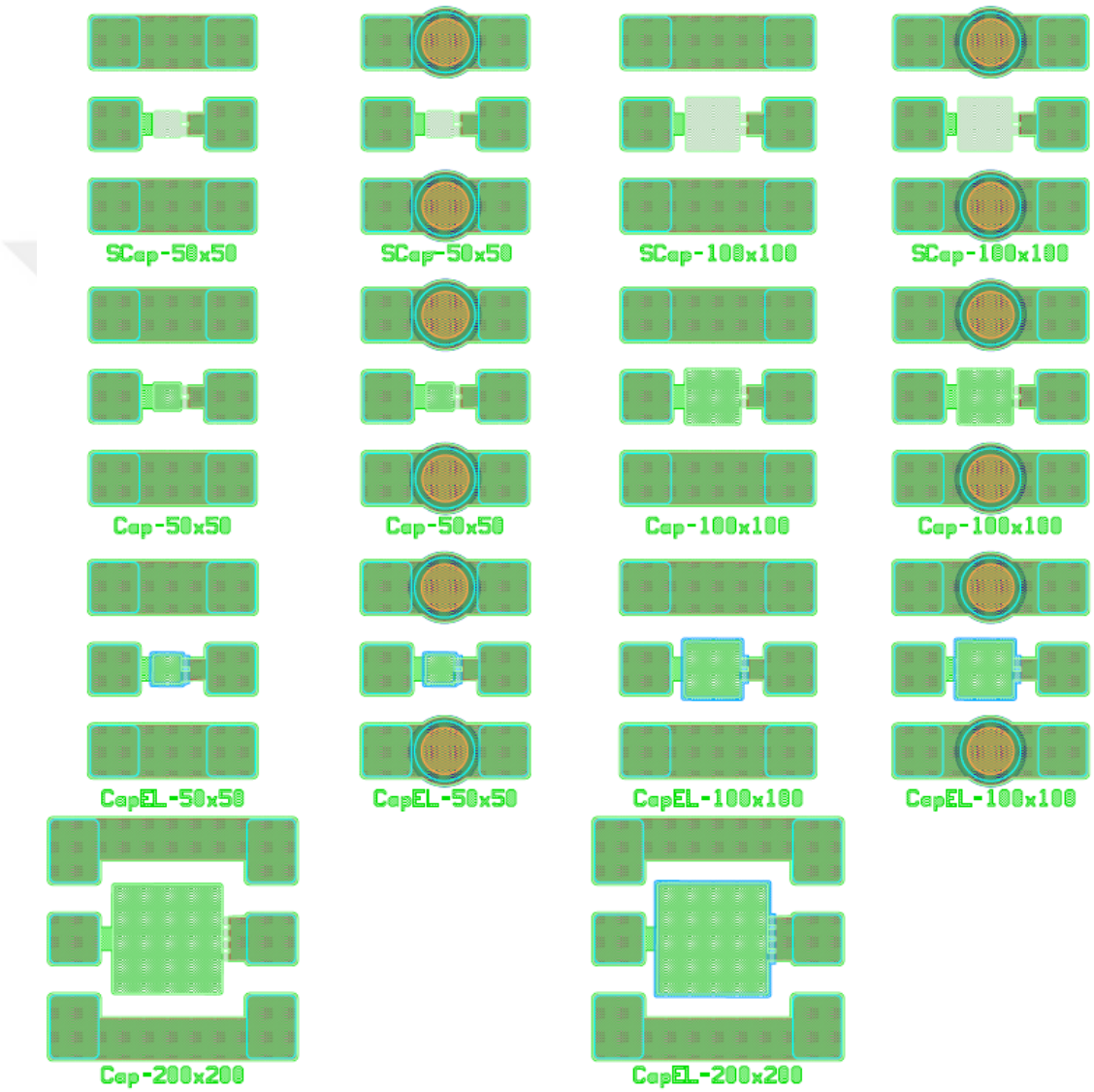


Figure 2.4: (a)The layouts of MIM-Capacitors in different sizes and (b) the circuit symbol

Inductors:

An inductor is another two-terminal passive device. Unlike a capacitor, an inductor stores magnetic energy.

Similar to capacitors, the inductors are also require two layers of metallization to support under/over passing at crossings. They can be designed in square, hexagonal, octagonal, spiral or arbitrary forms. Variety of inductors are designed at different turn numbers to investigate the coupling between turns. Only the inductors that have four turns are depicted in Fig. 2.5 to represent their configurations. The inductors are also in CPW and MS forms.

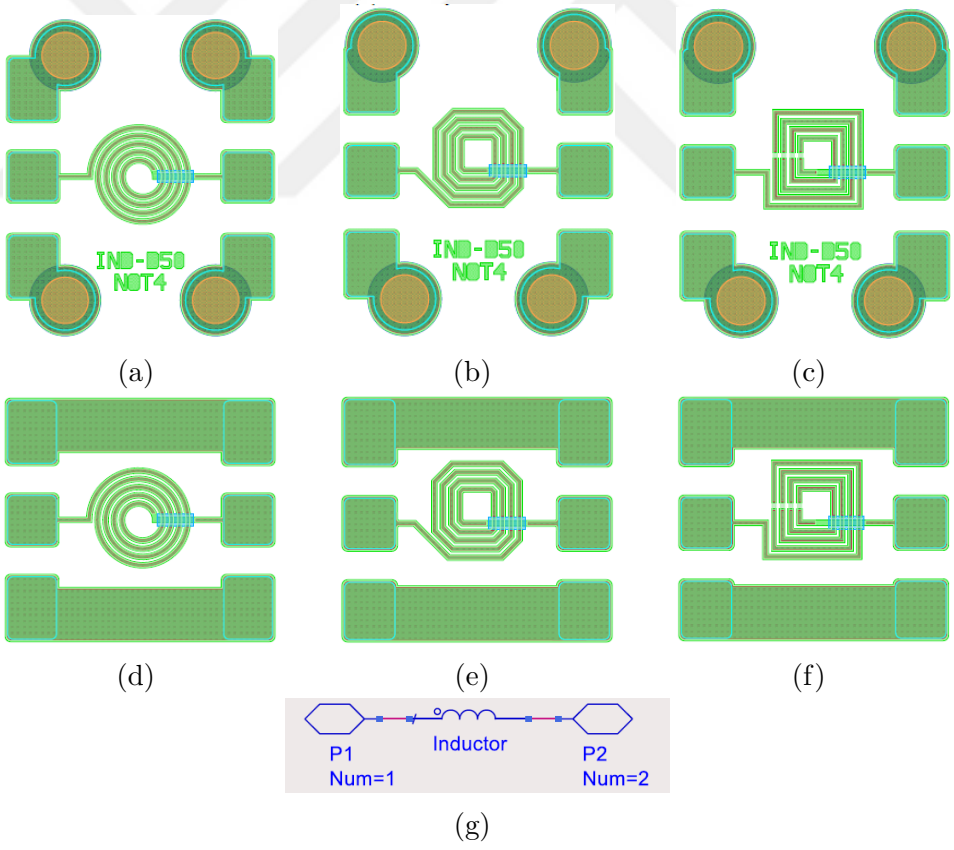


Figure 2.5: The layouts of (a) MS Spiral Ind., (b) MS Octagonal Ind., (c) MS Square Ind., (d) CPW Spiral Ind., (b) CPW Octagonal Ind., (c) CPW Square Ind., and (g) the circuit symbol

Transmission Lines:

Transmission lines (TLIN) are used for variety of purposes like designing stubs, connecting circuit elements, supplying power to devices etc. Considering the requirements for MIM-Caps and INDs, it is possible to design TLINs using both of the metallization layers together or separately. Since the first metallization layer is thinner according to the second metallization layer, it handles less power. Hence, the metallization layers and their widths have to be selected very carefully. Moreover, it is possible to stack both metallization to handle more power with a narrower TLIN.

Considering the technological requirements, different types of TLINs which can be formed utilizing MET1, MET2 or MET1+MET2 are designed. Their layouts are shown in Fig. 2.6.

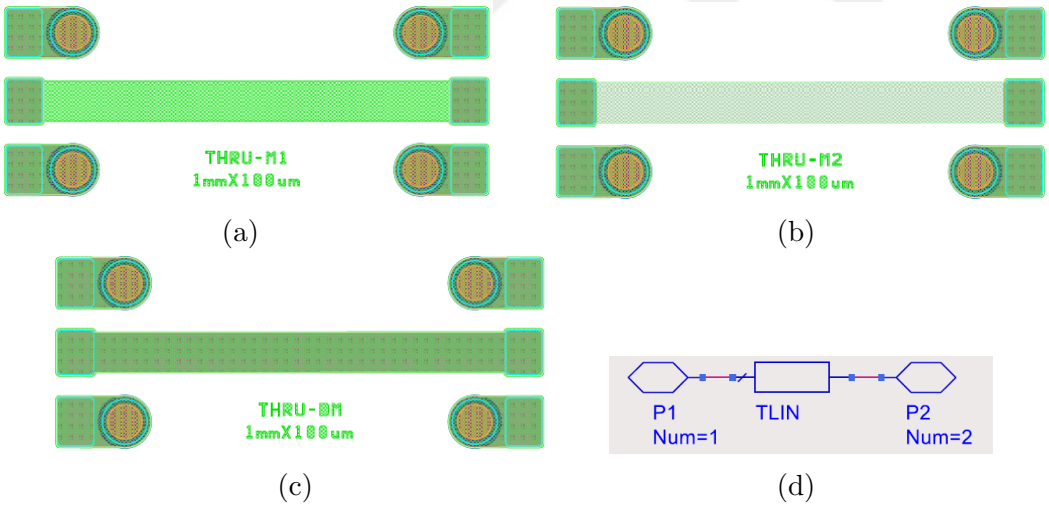


Figure 2.6: The layouts of different types of TLINs: (a) TLIN with MET1, (b) TLIN with MET2, (c) TLIN with MET1+MET2, and (d) the circuit symbol

2.3 Micro/Nano-fabrication Process Design

AlGaN/GaN integrated circuit technology requires certain circuit components to design an MMIC properly. The main circuit components required to design an MMIC are the MIM-CAPs, the inductors (IND), the TFRs, the TLINs, and the transistors. Therefore, the nano-fabrication process has to be developed considering the requirements for those circuit elements.

High Electron Mobility Transistor (HEMT) is the most suitable type of transistor for the AlGaN/GaN technology, since the 2DEG is formed inherently [5]. The electrons are confined in a very thin layer in between AlGaN/GaN barrier and they can move very fast in the channel. The epitaxial structure used to develop the LNA is given in Fig. 2.7.

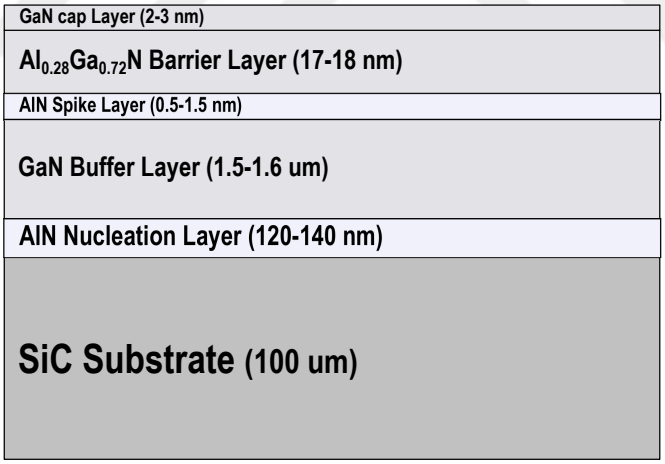


Figure 2.7: Cross-section of the epitaxial structure.

To form a suitable process, several dielectric layers are needed for different purposes. The first dielectric layer is used to passivate the surface of the wafer, the second dielectric layer is used to separate the gate of the HEMT from the source connected field-plate, and the third dielectric layer is used to develop the MIM capacitors. There is also a possibility for the fourth dielectric layer which can be used to seal the whole MMIC to protect it from environmental effects. *Silicon nitride* (SiN) is used as the dielectric material for all the dielectric layers.

Unlike the CPW technology, the MS process requires double-sided process. After completing the front-side micro/nano-fabrication process, there is also a back-side process to form the substrate vias to connect the ground plane by opening them from the back-side. To support the electrical connectivity, a metal has to be coated from the back-side by electroplating. Several critical circuit components that define the process flow are depicted from Fig.2.8 to Fig. 2.11.

The only active component required to design an MMIC in the process is the HEMT. On the other hand, there are several passive circuit components like TFR, EPI-RES, MIM-CAP, IND and TLIN. TFR and EPI-RES are both resistors but the sheet resistance of the EPI-RES is 10 times higher than the sheet resistance of the TFR.

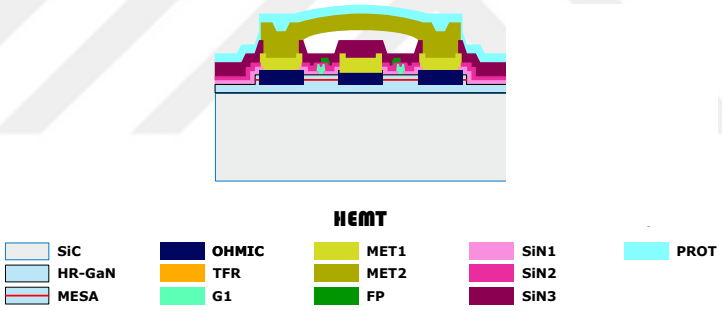


Figure 2.8: The cross-section of a HEMT

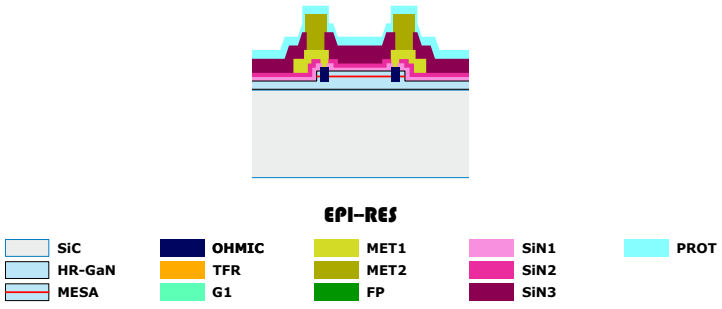


Figure 2.9: The cross-section of a EPI-RES

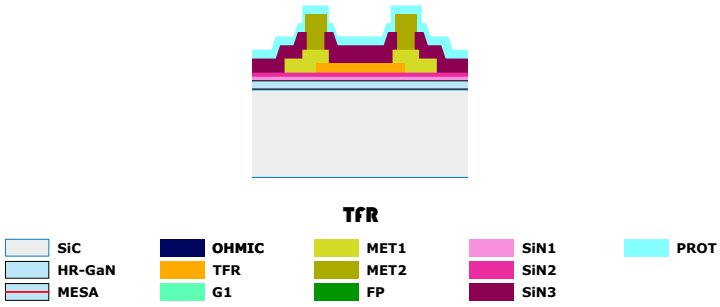


Figure 2.10: The cross-section of a TFR

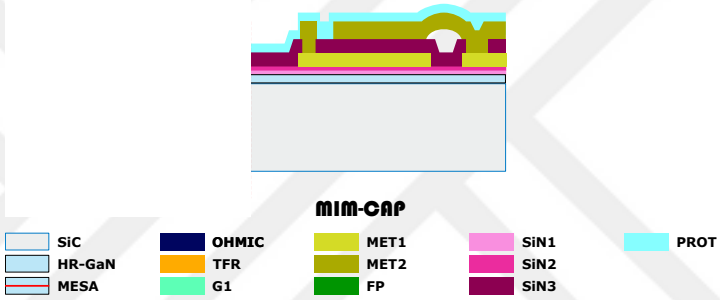


Figure 2.11: The cross-section of a MIM-Cap

2.3.1 Micro/Nano-fabrication Process Flow

The cross-sections of the devices are used to define the number of required layers and the photo-masks. The critical process steps are:

i. *OHMIC Metallization Step*: The stack of Ti/Ni/Al/Au metals are used to form the ohmic contacts of the transistors. After coating metals with e-beam evaporator, *rapid thermal annealing* (RTP) is applied to form the ohmic contacts.

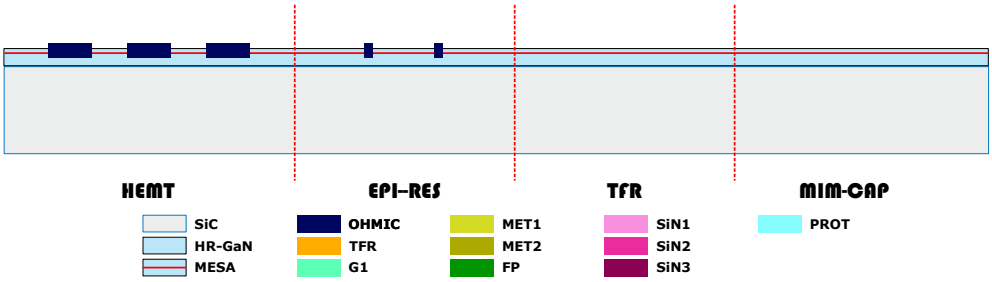


Figure 2.12: Step 1: OHMIC metallization

ii. *Mesa Etching Step*: The active areas of the transistors and the epi-resistor are isolated from the other circuit components by etching unnecessary active regions. The mesas are formed at this step by *inductivley coupled plasma reactive ion etching* (ICP-RIE) process..

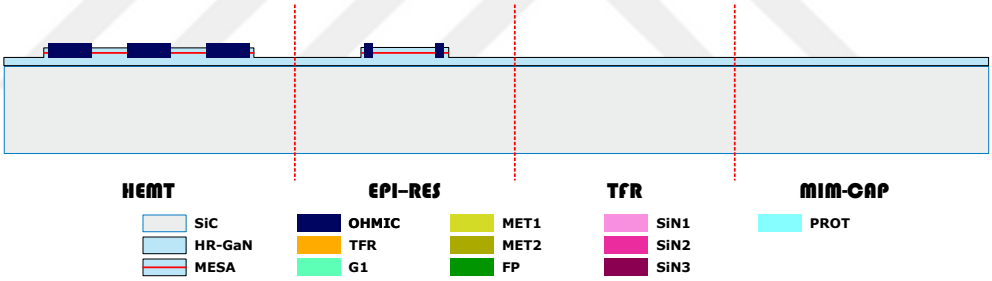


Figure 2.13: Step 2: Mesa etching

iii. *VIA0 Step*: VIA0 is an opening after coating the first layer of isolation dielectric. It is optional since applying a deeper etch at VIA1 step can also etch the first isolation dielectric layer.

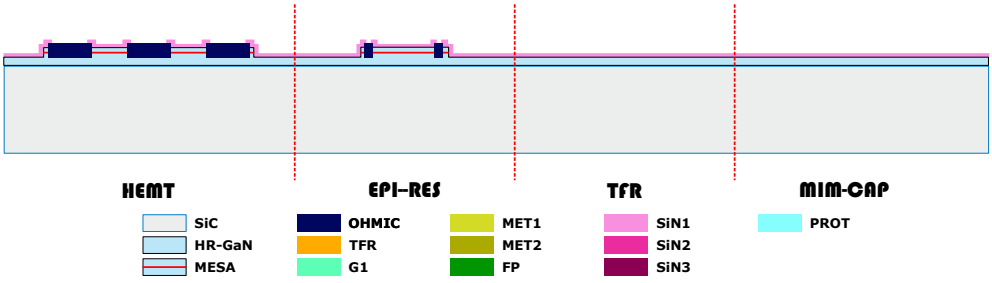


Figure 2.14: Step 3: 1^{st} VIA opening

iv. *Gate Foot Opening Step*: After coating the first isolation dielectric layer, a fine opening has to be developed to form the gate foot of the transistors. E-line lithography is used to develop the features, because of high resolution requirement. Therefore, there is no optical mask layer for this step.

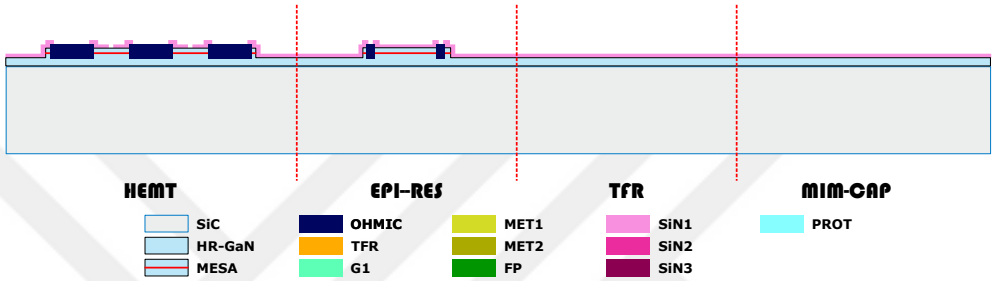


Figure 2.15: Step 4: Gate Foot opening

v. *Gate Foot Metallization Step*: After forming the opening of the gate foot, the gate metal is coated by e-beam evaporator to form the gate.

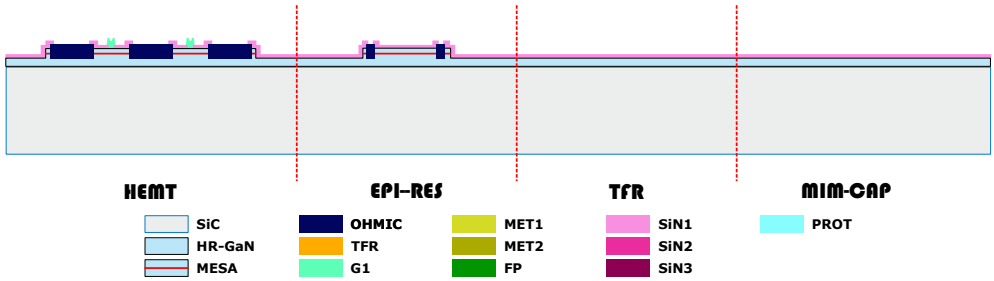


Figure 2.16: Step 5: Gate foot metallization

vi. *VIA1 Step*: After the gate metallization step, second layer of isolation dielectric is coated by *plasma enhanced chemical vapor deposition* (PECVD). To support the electrical connection between the ohmic contacts, the dielectric etching process is applied afterwards by ICP-RIE.

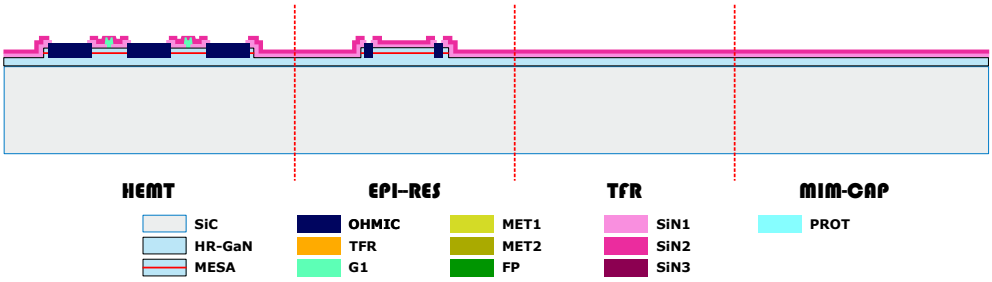


Figure 2.17: Step 6: 2^{nd} VIA opening

vii. *TFR Coating Step*: TaN is used to form the TFRs. It is coated by RF magnetron sputter.

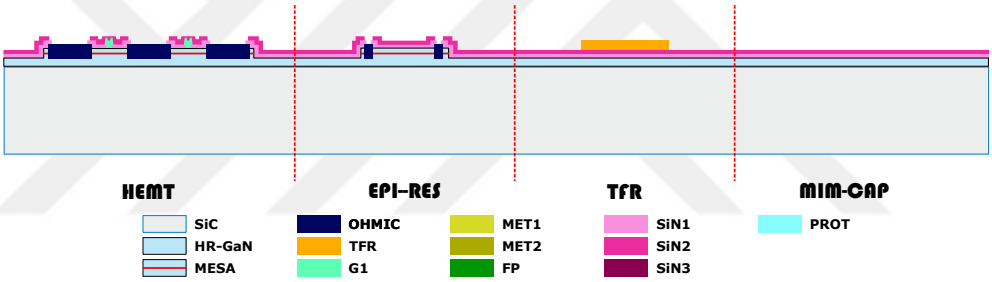


Figure 2.18: Step 7: TFR Coating

viii. *Field-Plate Metallization Step*: The surface is coated with a specific resist and e-line lithography is used to develop the field-plate. Then the field-plate formation is completed with the metal coating by the e-beam evaporator.

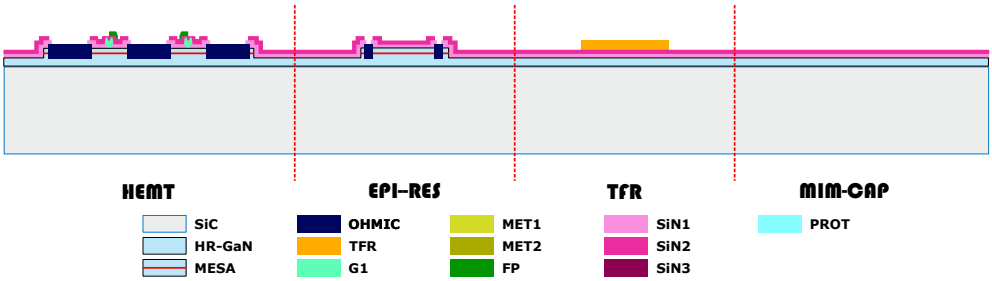


Figure 2.19: Step 8: Field-Plate metallization

ix. *MET1 Metallization Step*: To develop the first metal contact with the circuit components, $\sim$1 μm thick layer of gold is coated by the e-beam evaporator.

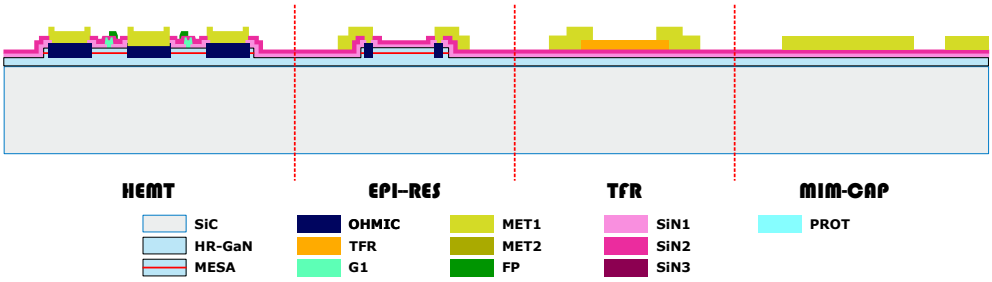


Figure 2.20: Step 9: 1^{st} metallization

x. *VIA2 Step*: To form the MIM-Cap, third layer of dielectric is coated by PECVD. Then a dielectric etching procedure is applied to etch away the dielectric layer from the contact areas of the circuit components.

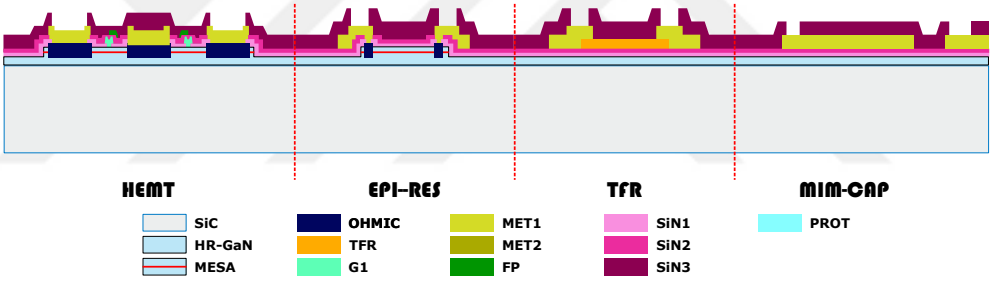


Figure 2.21: Step 10: 3^{rd} VIA opening

xi. *BRG Coating Step*: At certain points two different metal layers cross each other.. Therefore, one of the metals have to pass over the other. To develop the crossover, a specific type of resist is used to form the dome like structure.

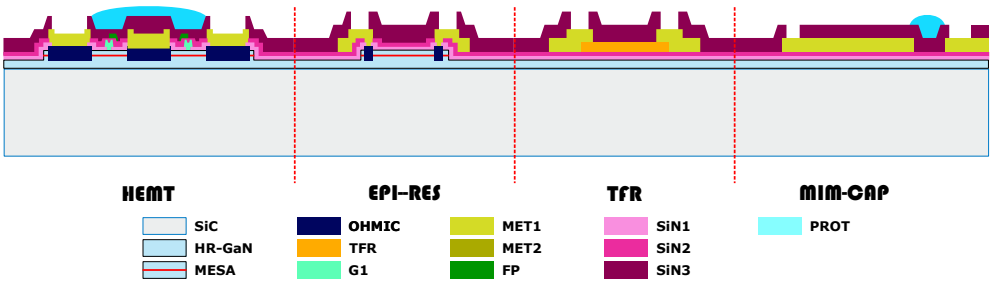


Figure 2.22: Step 11: Air-Bridge coating

xii. *MET2 Metallization Step*: To complete the circuit components and to make the actual contacts, at least 3 μm thick gold layer is coated by electroplating.

After that step, sacrificial air-bridge resist is removed to form the air-bridge. The formation of the air-bridge can be seen in Fig. 2.23 at HEMT and MIM-Cap sides.

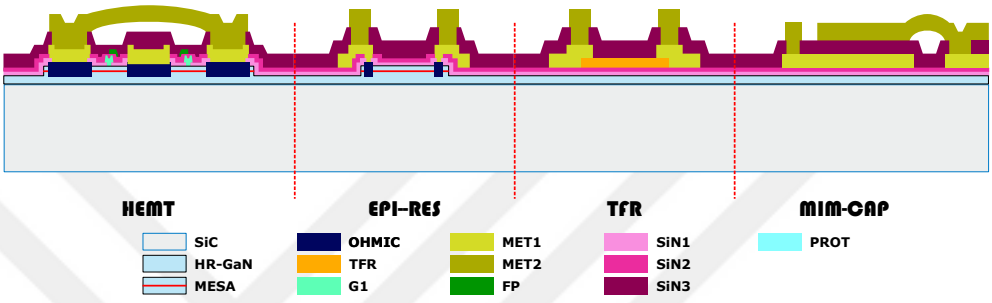


Figure 2.23: Step 12: 2^{nd} metallization

xiii. *PROT Step*: This step is also optional. The main purpose of this step is to cover the surface of the circuits with a thin dielectric layer. After coating this layer, to make the electrical contact, the dielectric layer is etched away at contact points. This step is the last step of the front-side process.

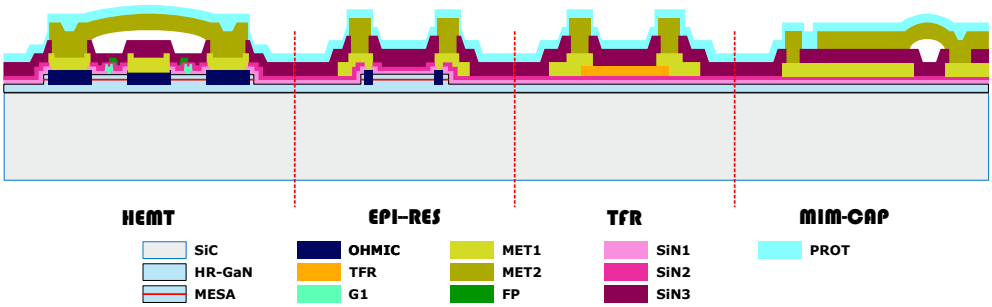


Figure 2.24: Step 13: Protection layer coating

xiv. *Back-side Step*: The substrate vias are opened by ICP-RIE and a thick gold layer is coated by electroplating to form the ground plane. The gold plating also covers the side walls of the substrate vias to establish the ground connection between the front-side and the back-side. After the metal coating, an optional step which is street etch can be applied to form the dicing paths.

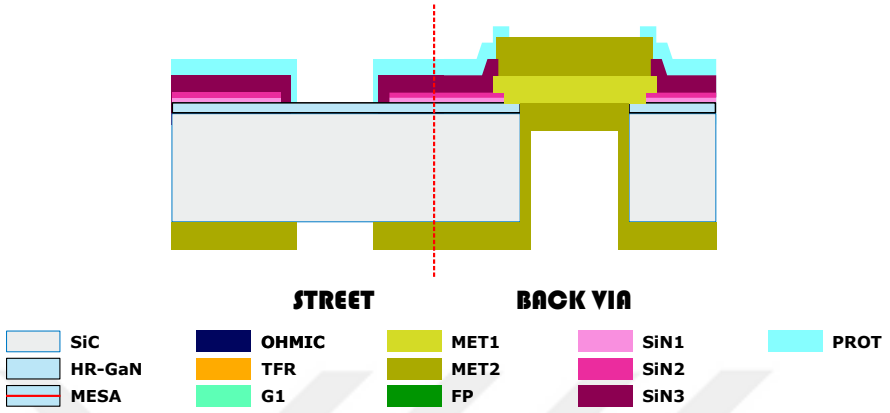


Figure 2.25: Step 14: Back-side processing

2.3.2 Photomask Design

There are two types of photo-lithography techniques, which are direct and reverse lithography. To accomplish a successful lithography, the right type of photoresist has to be used. In general, there are two kinds of photoresists which are called as positive tone resist and negative tone resist.

If the underling film is desired to be removed, then UV light is applied to the positive tone photoresist.The UV light exposure changes the chemical structure of the photoresist and the positive tone photoresist becomes soluble in the developer. Then, the developer solution is washed away to leave windows to the underlying layer. Thus, the photomask has to be designed in such a way that it contains the exact features which must remain on the wafer [51].

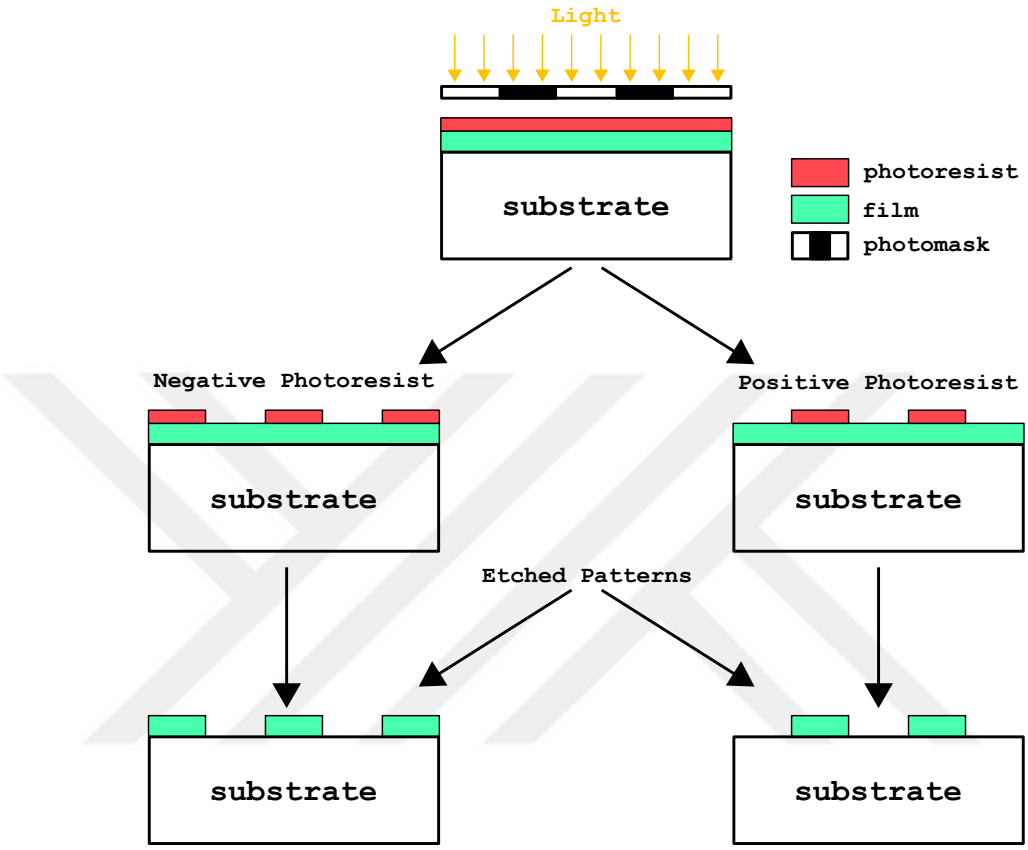


Figure 2.26: Photolithography process flow

On the other hand, if the underling film is not desired to be removed, then UV light is applied to the negative tone photoresist. The negative tone photoresist becomes polymerized with the UV light exposure and it becomes difficult to dissolve it in the developer. Thus, the exposed negative tone photoresist areas stay on the wafer and the unexposed areas are washed away by the developer solution. Therefore, the required photomask has to be designed in a way that it contains the inverse of the features which must remain on the wafer [51].

Different types of designed devices are located on a 9 mm $\times$ 9 mm square reticle as shown in Fig. 2.27. By using the reticle as a unit cell, 2" process development wafer layout is designed and given in Fig. 2.28.

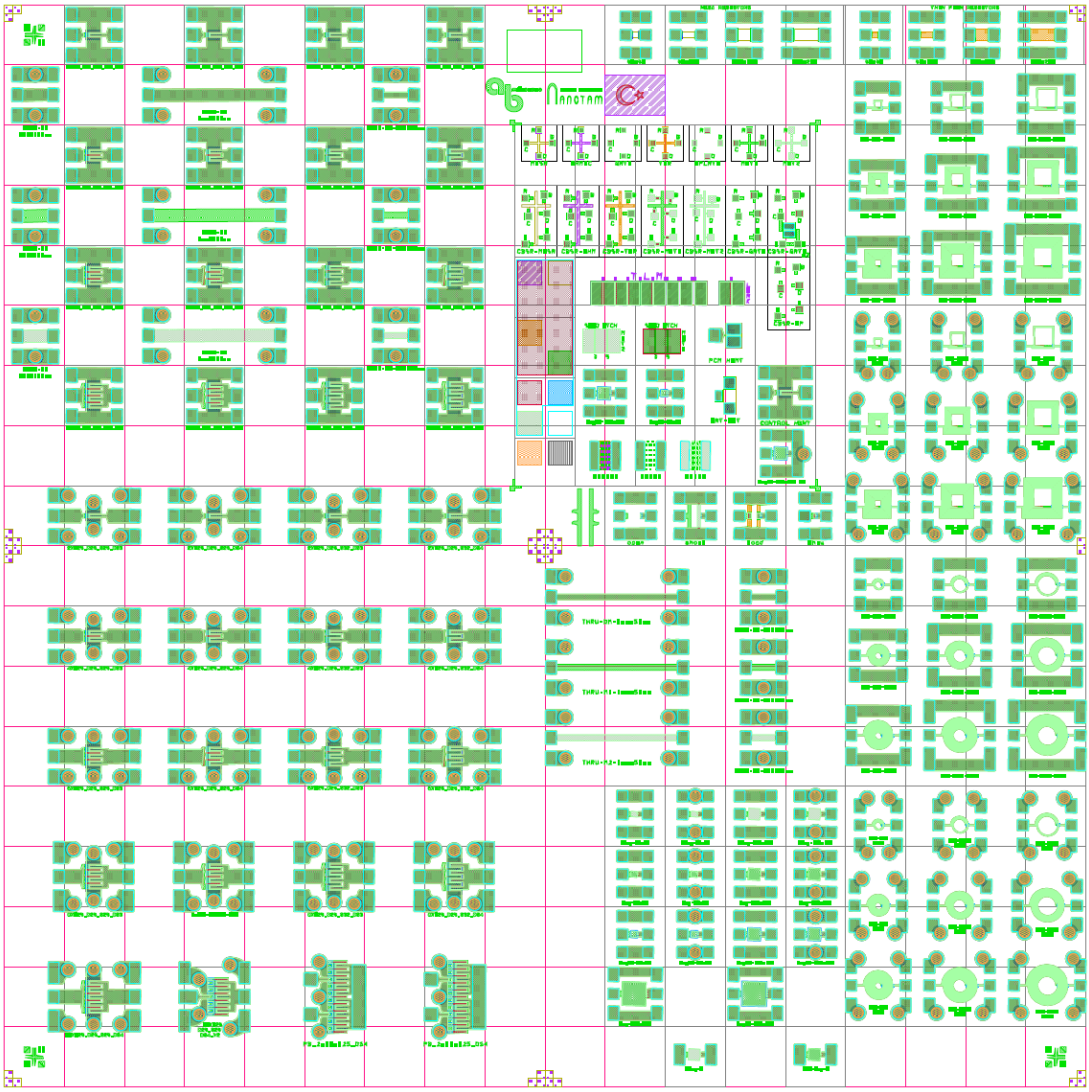


Figure 2.27: 9 mm × 9 mm square reticle

The 2” process development wafer layout composed of 9 different photomasks which are designed according to the specific requirements of the process flow. To make the process simplistic, the optional mask layers are eliminated at the first place. To start and optimize the process, 9 layers of photomasks are required which are OHMIC Layer, MESA Layer, VIA1 Layer, TFR Layer, MET1 Layer, VIA2 Layer, BRG Layer, MET2 Layer, and BVIA Layer. The photomask layers required to complete the micro/nano fabrication of a cascode HEMT properley are given in Appendix A.

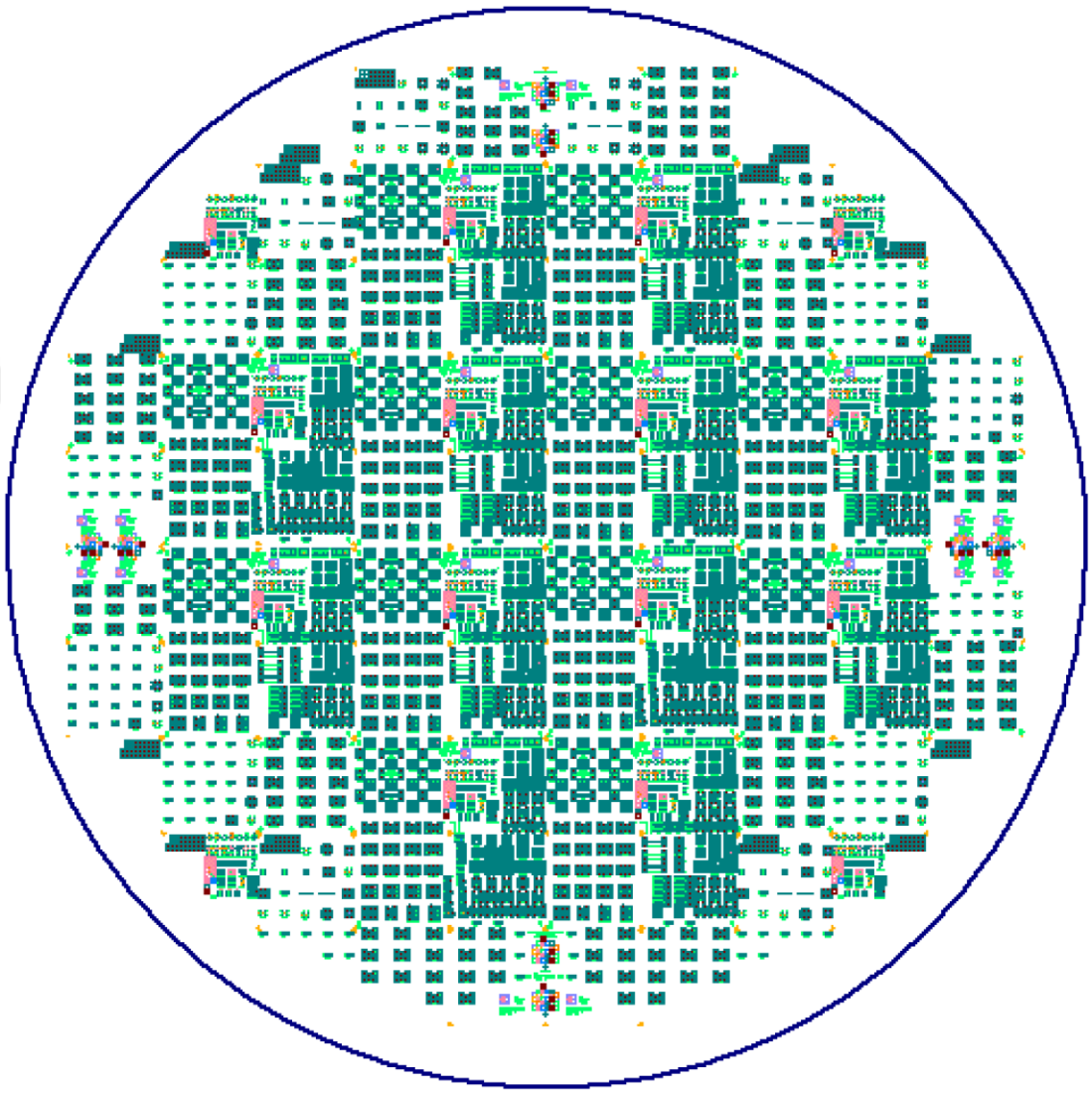


Figure 2.28: 2” process development wafer layout

2.4 Process Characterization

To develop a proper process, the process has to be characterized at each process step with the suitable electrical and the optical measurement patterns. To characterize the process, a cell called as Process Control Monitor (PCM) as in Fig. 2.29 is developed and implemented in the photomask at 16 different points.

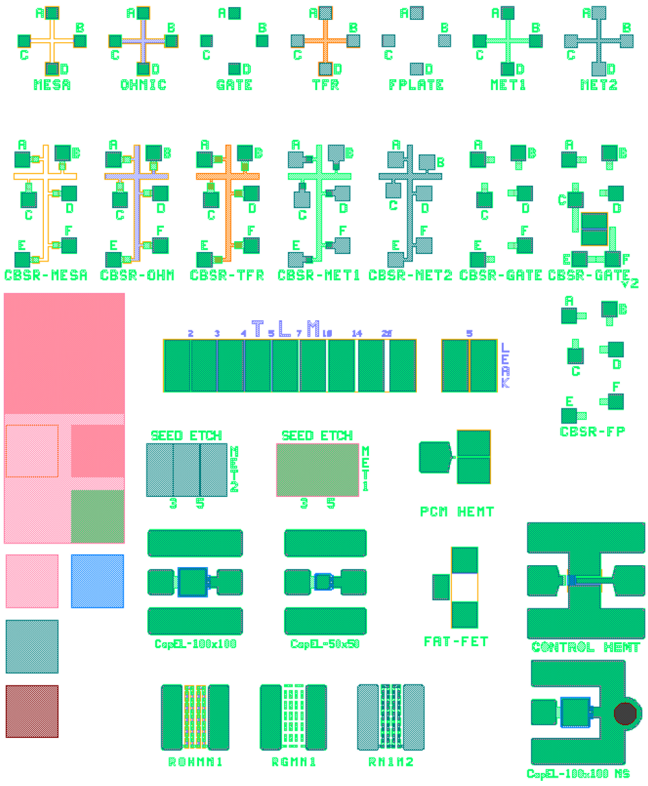


Figure 2.29: Process Control Monitor (PCM) cell

The PCM block consists of patterns to measure the contact resistance of the ohmic area, the sheet resistance of the epi-layer, the sheet resistance of the TFR, the sheet resistance of all metallization layers and the line widths of the metals and the DC/IV characteristics of the active devices. There are also several optical process development patterns to confirm that the etching, the metallization, etc. steps are done properly.

2.4.1 Cross Bridge Sheet Resistor (CBSR) Pattern

Monitoring the etching processes and conducting layers CBSR pattern in Fig. 2.30 is used. This pattern is the combination of the bridge structure used to determine the line width pattern and the van der Pauw structure to measure the sheet resistance [52].

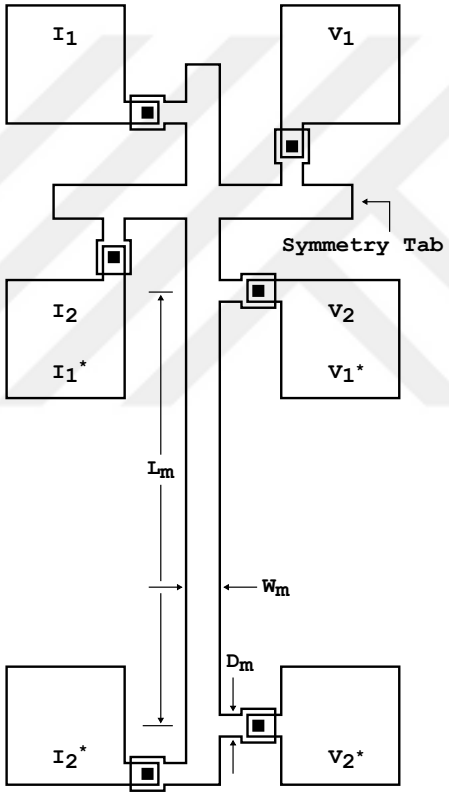


Figure 2.30: Cross-bridge sheet resistor test structure

The sheet resistance is determined from the van der Pauw structure by utilizing contact pads labelled as I_1, I_2, V_1, and V_2 as in Fig. 2.30 and is calculated by the following formula [52]:

$$R_S = \frac{\pi R}{ln(2)}(\Omega/\square) \tag{2.1}$$

2.4.2 TLM Pattern

Transmission Line Measurement (TLM) is performed to calculate the contact resistance of the ohmic layer. The most commonly used TLM pattern is depicted in Fig. 2.31a to measure the resistance between two consecutive ohmic contacts, a four-point-probe is used to minimize the effects of the probes [53]. The TLM method is depicted in Fig. 2.31b. The current is applied in between two sequential ohmic contacts and the voltage across is measured, then the resistance value is calculated.

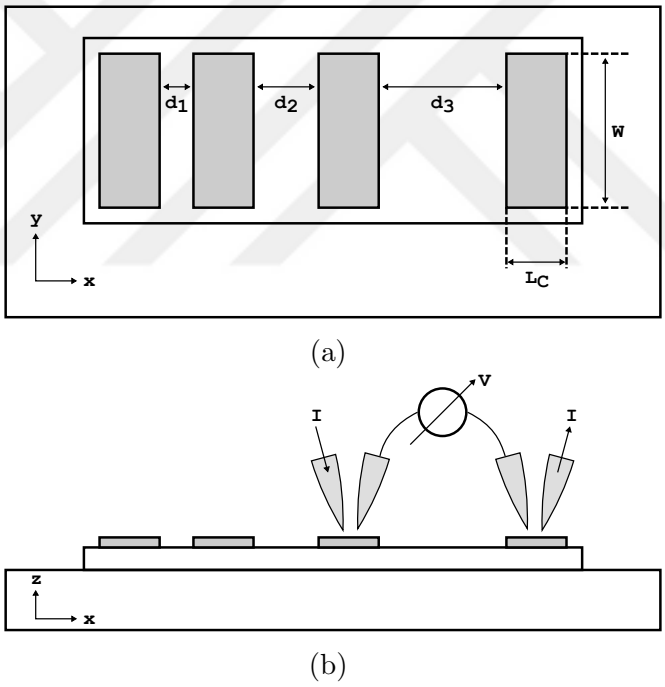


Figure 2.31: Illustration of (a) TLM pattern and (b) TLM method

After measuring all the sequential patterns one by one, calculated resistance values are plotted as in Fig. 2.32 and a curve fit is applied. The sheet resistance of the epi layer can be calculated from the slope of the fitting curve. Furthermore, contact resistance of the ohmic contacts can be calculated from the intercept of the fitting curve.

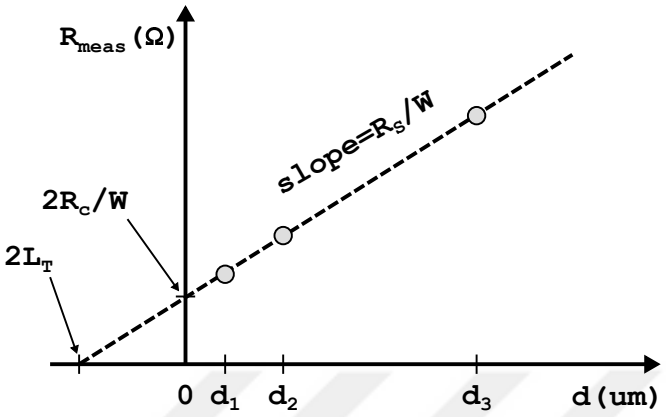
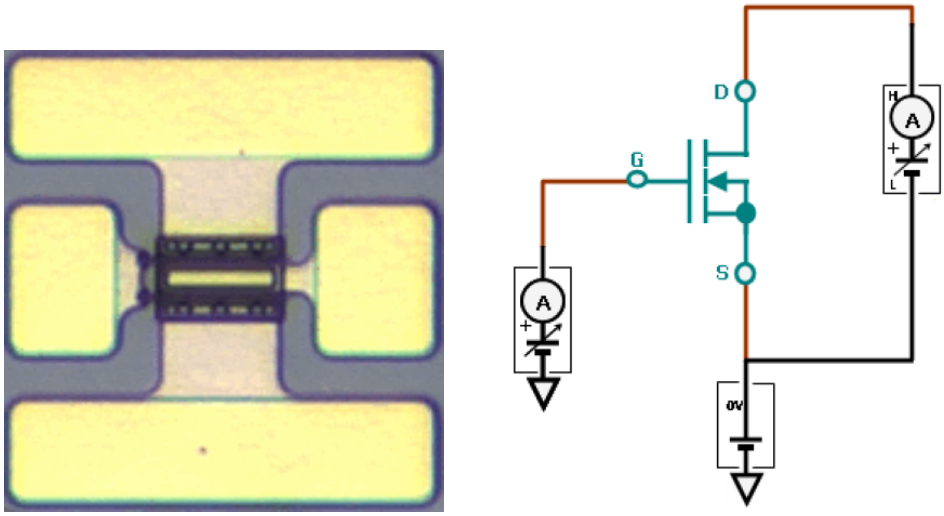


Figure 2.32: TLM Result

2.4.3 PCM HEMT

A PCM HEMT is a simple device that consists of two gate fingers as depicted in Fig. 2.33a. The IV curves, the current density (I_{DSS}), the on-resistance (R_{on}), the transconductance (g_m), the pinch-off voltage (V_P), the gate turn-on voltage ($V_{g,on}$) and the breakdown voltage (V_{br}) can be determined by measuring the performance of the PCM. The acquired data is very useful to analyze the quality of active devices from a specific fabrication.



(a) (b)

Figure 2.33: Illustration of (a) a fabricated 2×125 μm PCM HEMT and (b) the DC Measurement Setup

The IV curves are convenient to calculate I_{DSS} and R_{on} of a transistor. Moreover, V_P can be calculated but to determine V_P accurately, the voltage sweep steps have to be very narrow in an expense of the increased measurement time. Because of the increased measurement time, the thermal effects limit the actual performance of the transistor. Therefore, a separate pinch-off voltage measurement is required.

The gate-source voltage (V_{GS}) is set as the primary sweep and the drain voltage is set as the secondary sweep parameter and the drain-source current (I_{DS}) is measured to obtain the IV curves. The V_P measurement is performed by keeping V_{DS} constant and V_{GS} is swept from -8 V to +1 V. The derivative of the I_{DS} with respect to V_{GS} is used to calculate the g_m.

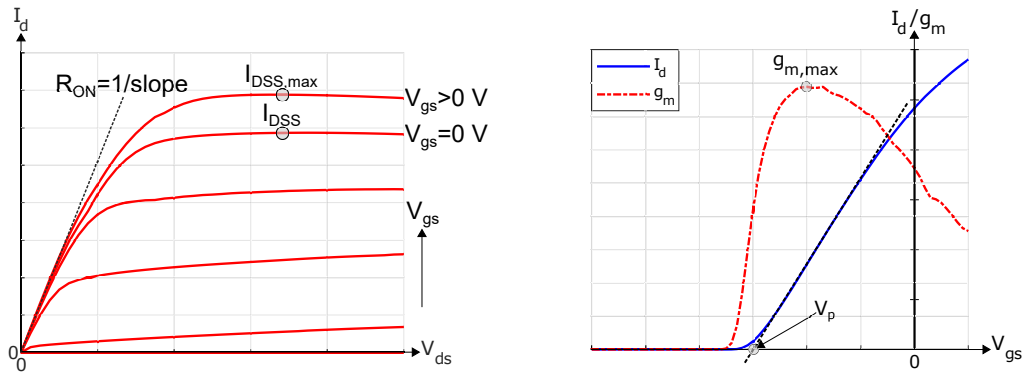
On the other hand, V_{br} is measured by keeping V_{GS} at a lower point than V_P and either the current or the voltage is swept at the drain side.

2.5 DC and RF Characterization

To characterize the devices in a proper way, the characterization equipments have to be selected according to the measurement requirements. In case of the transistors, most important characterization parts are the pulsed IV system and the pulsed S-Parameter system. On the other hand, the passive devices require simpler systems like S-Parameter measurement systems.

2.5.1 DC Figure of Merits

The DC figure of merits (FOM) are the maximum current density ($I_{DSS,max}$), the current density at $V_{gs} = 0V$ (I_{DSS}), the on-state resistance (R_{ON}), the maximum transconductance (g_m), and the pinch of voltage (V_p). Those parameters are calculated from the *DC-IV* and $I_d - V_{gs}$ measurements as presented on Fig. 2.34. The transconductance is calculated from the derivative of the drain current (I_d) with respect to the gate-source voltage (V_{gs}).



(a) (b)

Figure 2.34: (a) DC-IV and (b) $I_d - V_{gs}$ characteristics of a depletion mode FET.

2.5.2 RF Figure of Merits

RF FOMs can be divided into two groups considering the input signal conditions. Therefore, RF FOMs are described under the small-signal and the large-signal

conditions.

2.5.2.1 Small-Signal FOMs

The devices operate in linear region, the output signal level is proportional with the input signal level, under small-signal (SS) conditions [54]. So, the small-signal conditions could be different for different devices. There are important parameters to analyze the performance of a device, such as the maximum stable gain (MSG), the maximum available gain (MAG), the maximum frequency of oscillation (f_{max}), the cut-off or the transition frequency (f_T), and the stability factor K.

Stability:

The stability of network can be divided in two group: *conditional stability* and *unconditional stability*. A network is called as unconditionally stable if the input reflection coefficient (Γ_{IN}) and the output reflection coefficient (Γ_{OUT}) are always <1 for all passive source and load impedance states [54]. If this condition is only satisfied for limited range of passive load and source impedance, then the network refereed as conditionally stable [54]. Moreover, the input and the output stability circles can be plotted to determine the stability of the network [54].

To test the unconditional stability, a simpler test is defined and it is called as *Rollet's condition* [54]. If the conditions described in Eq. (2.2) and Eq. (2.3) satisfied simultaneously, then the network called as unconditionally stable.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.2}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.3}$$

It is also possible to extend the stability test with the condition given in Eq.

(2.4) [55]. $\mu-$test can be used to determine both the input and the output and larger values of $\mu-$test gives greater stability.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{2.4}$$

Transducer Power Gain:

The transducer power gain (G_T) is the ratio of the power delivered to the load (P_L) to the power available from the matched source (P_{AVS}) as given in Eq. (2.5). In Eq. (2.6), Γ_{IN} is the input reflection coefficient of the device under test (DUT) with a termination of arbitrary load (Γ_L) [56]. The S-parameters and the load and the source terminations of the DUT are necessary to calculate G_T.

$$G_T = \frac{Power\ delivered\ to\ the\ load}{Power\ available\ from\ matched\ source} = \frac{P_L}{P_{AVS}} \tag{2.5}$$

$$G_T = \frac{(1 - |\Gamma_S|^2)|S_{21}|^2(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L)| - S_{12}S_{21}\Gamma_S\Gamma_L} \tag{2.6}$$

To simplify the G_T expression, simply set $|S_{12}| = 0$ which is referred as the unilateral transducer gain (G_{TU}) [56–58]:

$$G_{TU} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{2.7}$$

Gain Expressions:

Even though there are different types of gain definitions in the literature, two gain definitions are commonly used to evaluate the performance of an active device. The *maximum stable gain* (MSG) and the *maximum available gain* (MAG) terms are used to state the SS gain of a transistor. MAG of the transistor can be written as in Eq. (2.8), if the transistor is unconditionally stable ($K > 1$) [54].

MAG term is also referred as the *maximum transducer power gain* ($G_{T_{max}}$) or *matched gain*.

$$MAG = G_{T_{max}} = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \tag{2.8}$$

If the transistor is conditionally stable ($K < 1$), MSG is a more useful term to use. MSG is defined as MAG with $K = 1$ [54]. MSG can be defined as follows:

$$MSG = G_{T_{max}} = \frac{|S_{21}|}{|S_{12}|} \tag{2.9}$$

MSG and MAG of a sample transistor is illustrated in Fig. 2.35 related with the K-point

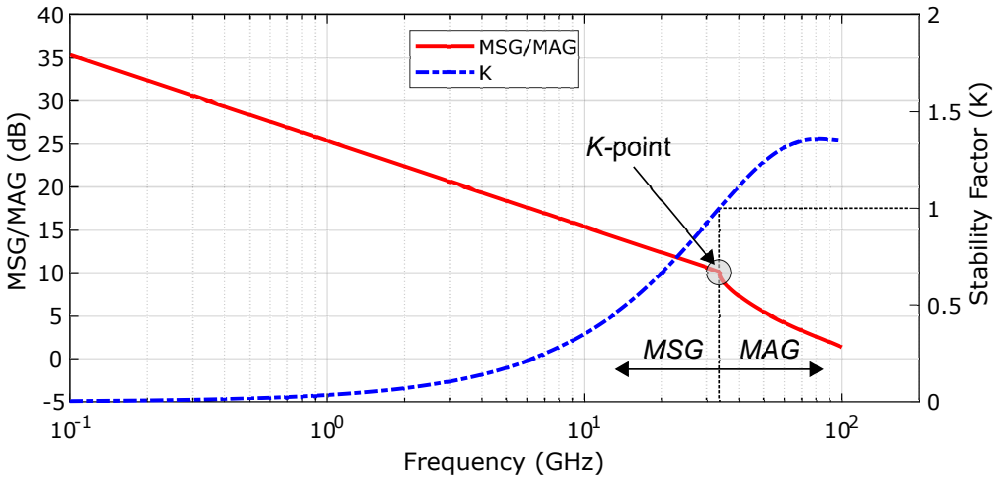


Figure 2.35: Representation of MSG/MAG and K-point of a FET

Maximum Frequency of Oscillation and Cut-off Frequency:

The cut-off frequency (f_T) is an important measure to asses the intrinsic performance of a transistor. The cut-off or transient frequency is defined as the short-circuit current gain cut-off frequency, where the short circuit current gain (β) is unity as described in Eq. (2.10) [59].

$$\beta = |h_{21}| = \left| \frac{i_{out}}{i_{in}} \right| \Bigg|_{v_{out}=0} = 1 \tag{2.10}$$

The short circuit current gain becomes unity at:

$$f_T \approx \frac{g_m}{2\pi C_{gs}} \tag{2.11}$$

On the other hand, the maximum frequency of oscillation (f_{max}) is defined by the frequency at which MAG becomes unity. f_{max} is defined by Eq. (2.12) and it represents the unity power gain frequency. From Eq. (2.12), it is clear that the paralytics play an important role to define f_{max} [59].

$$f_{max} \approx \frac{f_T}{2\sqrt{(R_s + R_g)g_{ds} + 2\pi f_T R_g C_{gd}}} \tag{2.12}$$

f_T and f_{max} can be determined by extrapolating $|h_{21}|$ and MSG/MAG data as presented in Fig. 2.36.

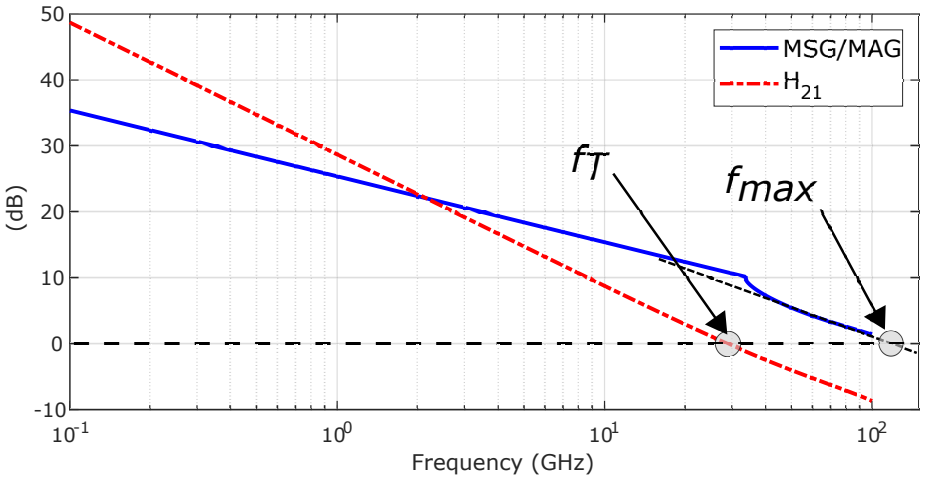


Figure 2.36: Representation f_T and f_{max} of a FET

2.5.2.2 Large-Signal FOMs

Large-Signal can be defined as the signal level that pushes the device to operate in a non-linear region. The gain of a FET under large-signal conditions has tendency to decrease as shown in Fig. 2.37. Thus, couple performance parameters are necessary to understand the large-signal FOMs.

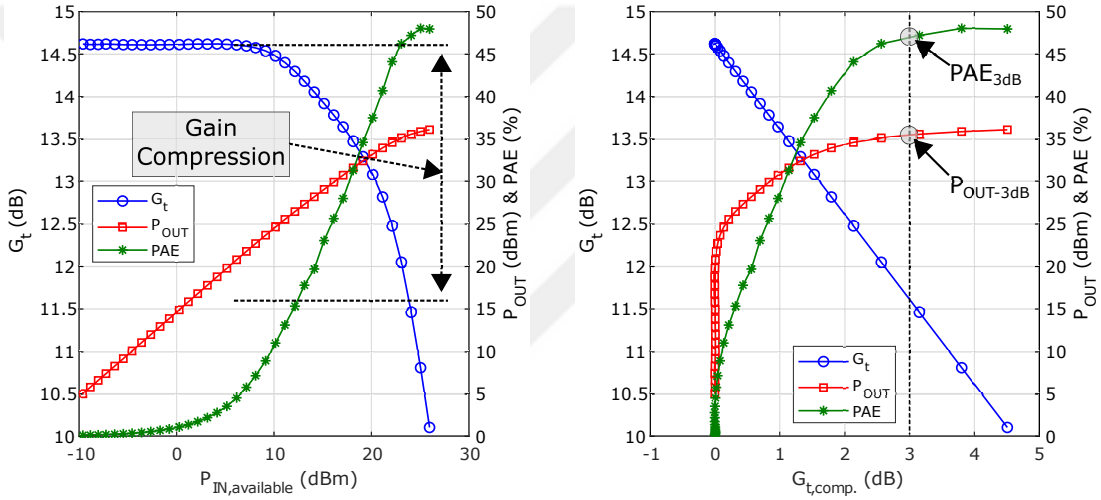


Figure 2.37: Representation of P_{OUT}, G_T, PAE, and the compression point of a FET

Gain Compression:

The gain compression (GC) can be defined as the reduction of G_T caused by the nonlinearity of the DUT as represented in Fig. 2.37. The output power is related with the input power with $P_{OUT} = G_T P_{IN}$ in the linear case. However, the gain of the DUT eventually starts to reduce after a certain input power level. The level of the gain drop from the linear gain determines the gain compression point. The new relation between the output and the input power becomes $P'_{OUT} = G'_T P_{IN}$. Thus, the GC can be expressed as $GC = G_T - G'_T$.

Output Power:

The output power (P_{OUT}) of a DUT depends of the input power (P_{IN}). As depicted in Fig. 2.37 after certain P_{IN} level, P_{OUT} level does not increase. Since the

P_{OUT} level is saturated, it is called as saturated output power ($P_{OUT,SAT}$). Other than power level, the output power named according to the gain compression level and described as $P_{OUT-XdB}$ where 'X' denotes the level of the gain compression. The level of P_{OUT} depends on the load termination of the DUT. Thus, P_{OUT} can be maximized by terminating the load in an optimum impedance [60].

Power Added Efficiency:

The power added efficiency (PAE) describes the amount of the DC power (P_{DC}) converted to the RF power considering P_{AVS} as given in Eq. (2.13). PAE can be expressed with Eq. (2.14) as described in [61, 62].

$$PAE = \frac{Power\ delivered\ to\ the\ load - Power\ available\ from\ matched\ source}{DC\ power} \tag{2.13}$$

$$PAE = 100\%\frac{P_L - P_{AVS}}{P_{DC}} \tag{2.14}$$

2.5.3 Measurement System Configuration

The active devices are characterized with the system presented in Fig. 2.38. The pulsed IV (PIV) and the pulsed S-Parameter measurements are performed sequentially. The pulse widths are adjusted to eliminate the thermal effects.

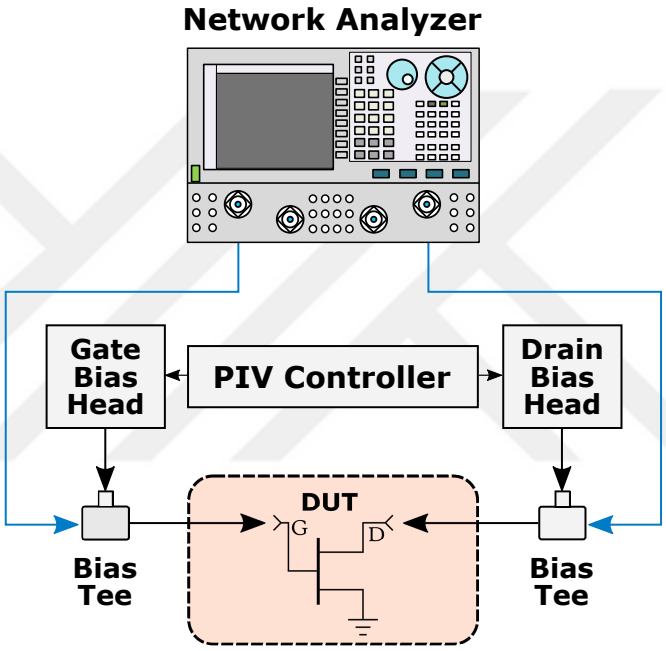


Figure 2.38: DC + RF Device Characterization Setup

RF Power related measurements are performed on the system depicted in Fig. 2.39. The collected data is used to verify and optimize the transistor model. This system is capable of measuring a_1, a_2, b_1, and b_2 waves and calculating the actual impedances of the transistors more accurately [63].

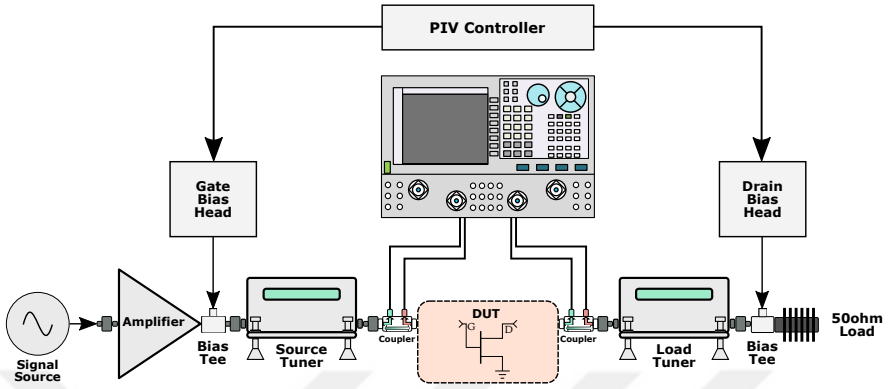


Figure 2.39: Load-Pull measurement Setup

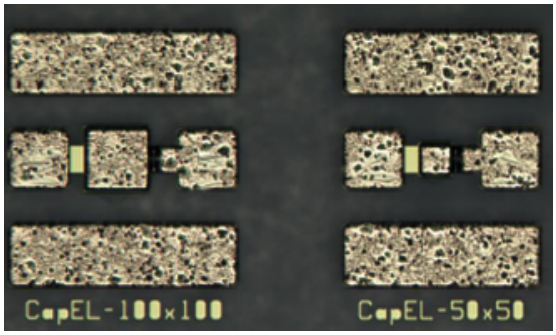
2.5.4 Measurement Results

After developing the process flow, multiple optimizations are applied to micro/nano-fabrication process to get the desired results. Therefore, each step is studied carefully. As a result, the microstrip GaN-on-SiC technology is developed and the following results represent the state of the acquired technology.

The image of the fabricated MIM-Caps are shown in Fig. 2.40a. Those MIM-Caps have two different periphery to validate the results. One of the MIM-Caps has $50 \times 50\ \mu m^2$ active area and the other one has $100 \times 100\ \mu m^2$ active area. The capacitance measurement results and the resonance frequency of each capacitor are provided in Fig. 2.40. The results show that the dielectric layer between two metals has high quality.

The image of the fabricated spiral inductor is given in Fig. 2.41a. The spiral inductor has four turns. The inductance measurement results and the resonance frequency of each inductor on the wafer are shown in Fig. 2.41b. The results show that the metal layer and the substrate qualities are high.

The image of the fabricated TFRs are given in Fig. 2.42a. Those TFRs have two different periphery to validate the results. One of the TFRs has $50 \times 100\ \mu m^2$ active area and the other one has $100 \times 100\ \mu m^2$ active area. The resistance measurement results of each TFR are shown in Fig. 2.42. Since the results show little variation over the wafer, the TFR layer has high quality.



(a)

CAP: 100x100

CAP: 50x50

PASSIVE W6
ABMN-MSPC01
CAPACITANCE

NA	2.97	2.93	2.91
0.71	0.73	0.73	0.73
2.91	2.91	2.93	2.91
0.718	0.715	0.716	0.734
2.92	2.92	2.94	2.97
0.73	0.712	0.733	0.72
NA	2.93	2.95	NA
NA	0.721	0.723	NA

PASSIVE W6
ABMN-MSPC01
RESONANCE FREQ.

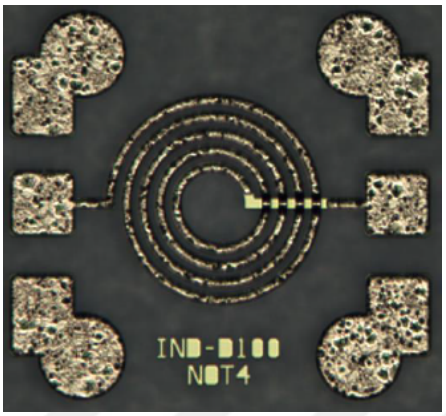
NA	7.85	8.95	9.45
16.75	17.35	21	20.7
9.2	9.1	8.75	9.65
20.35	20.85	20.15	20.85
9.1	9.05	9.15	8.45
20	19.7	19.25	19.8
NA	9	9.15	NA
19.8	19.8	19.6	NA

ABMN-MSPC01
PCM MAP

PCM1	PCM2	PCM3	PCM4
PCM8	PCM7	PCM6	PCM5
PCM9	PCM10	PCM11	PCM12
PCM16	PCM15	PCM14	PCM13

(b)

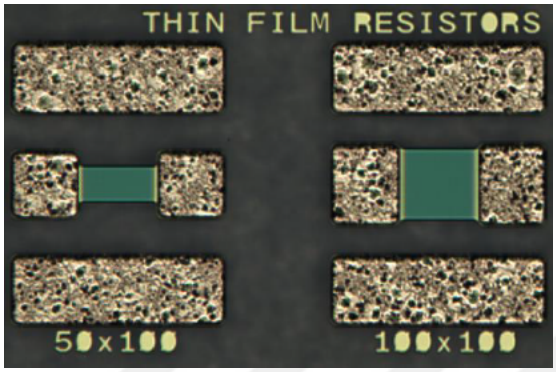
Figure 2.40: (a) Microphotograf of MIM-CAPs and (b) 100 $\mu m\times$ 100 μm & 50 $\mu m\times$ 50 μm MIM-CAP Measurement Results (Capacitance in pF & Resonance Frequency in GHz)



(a)

(b)

Figure 2.41: (a) Microphotograph of a Spiral Inductor and (b) Inductor Measurement Results (Inductance in nH & Resonance Frequency in GHz)



(a)

(b)

Figure 2.42: (a) Microphotograf of TFRs and (b) 50 $\mu m\times$ 100 μm (TFR50) & 100 $\mu m\times$ 100 μm (TFR100) Measurement Results (Resistance in Ω)

The image of one of the test HEMTs with 8×125 μm configuration is given in Fig. 2.43a. The DC-IV, g_m, and the forward-IV measurements are shown in Fig. 2.43b, Fig. 2.43c, and Fig. 2.43d, respectively. The measurement results yield that the developed HEMT has high current density, high g_m, and high turn-on voltage (V_{to}) to support high power and high bias applications.

To verify the performance of the fabricated HEMTs over the wafer, a 3" wafer is fabricated and the HEMTs on that wafer are measured. The distribution of those measurements are given in Fig. 2.44. These results confirm that the wafer has consistent quality.

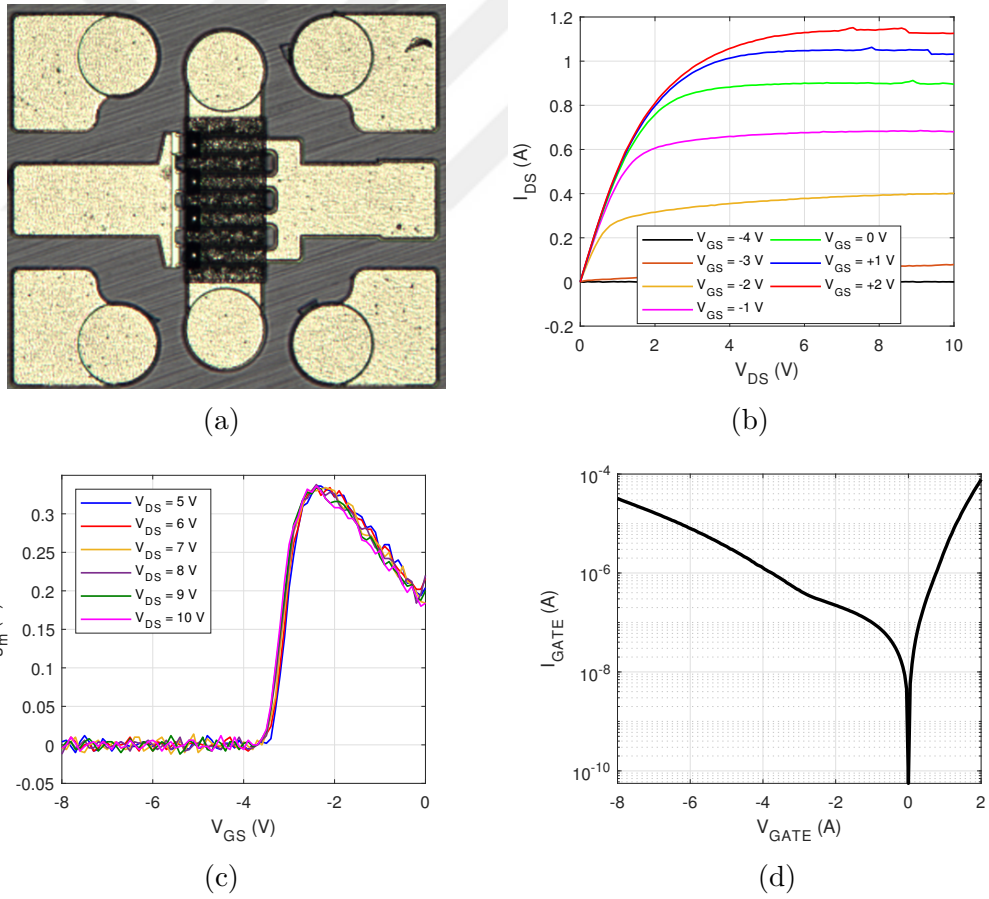


Figure 2.43: (a) Microphotograf of 8×125 μm HEMT and the (b) DC-IV, (c) DC-g$_m$, and (d) forward-IV data of the same HEMT

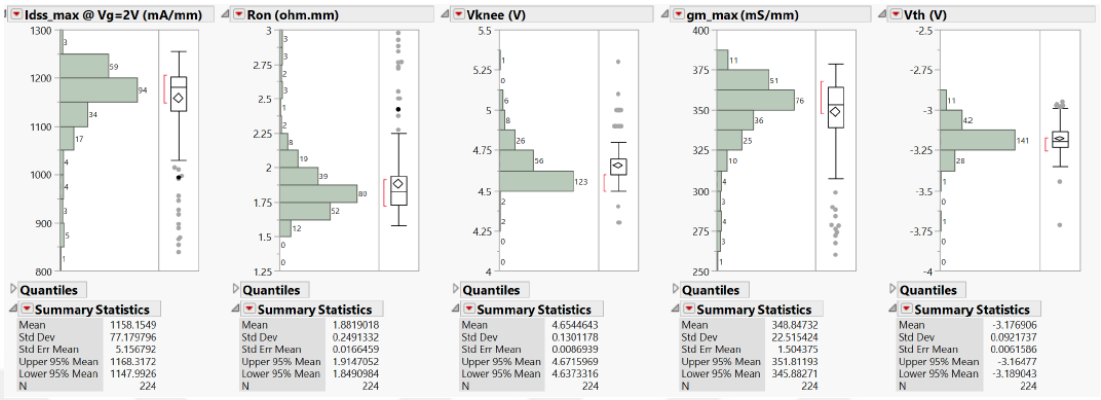


Figure 2.44: Statistical distribution of the DC measurement results of 224 8×125 μm HEMT on a wafer

To test the RF performance, S-parameters are measured and MSG/MAG, f_T, and f_{max} are calculated. The results are given in Fig. 2.44. The measured HEMT has high gain, and high f_T and f_{max}. To confirm the gain uniformity over the wafer, more than 100 HEMTs are measured over the wafer and the heat map is given in Fig. 2.46. Moreover, the power performance is measured at different load impedances and P_{OUT} and PAE results are obtained at 3dB and 4dB compression points. The results are shown in Fig. 2.47.

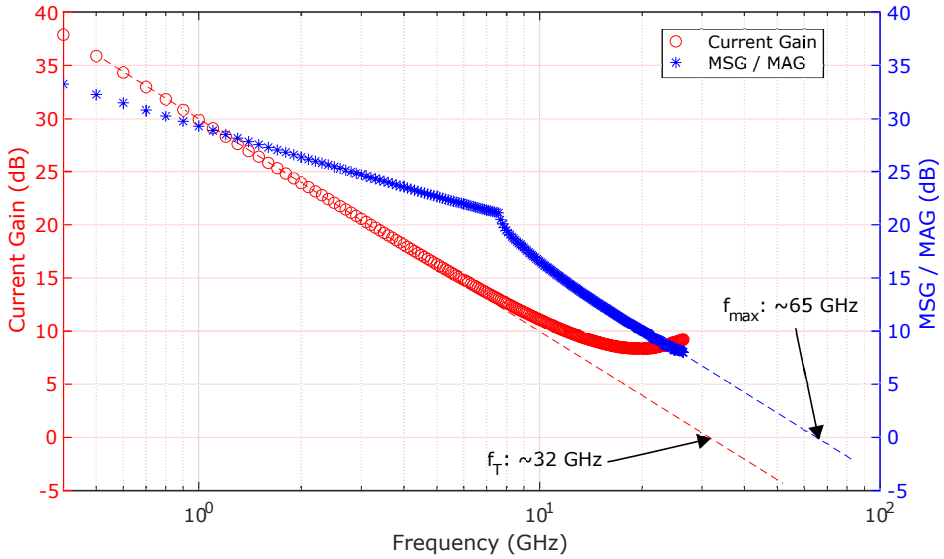


Figure 2.45: MSG/MAG and H_{21} on-wafer measurement result of a 8×125 μm HEMT. f_T and f_{max} results are shown on the figure.

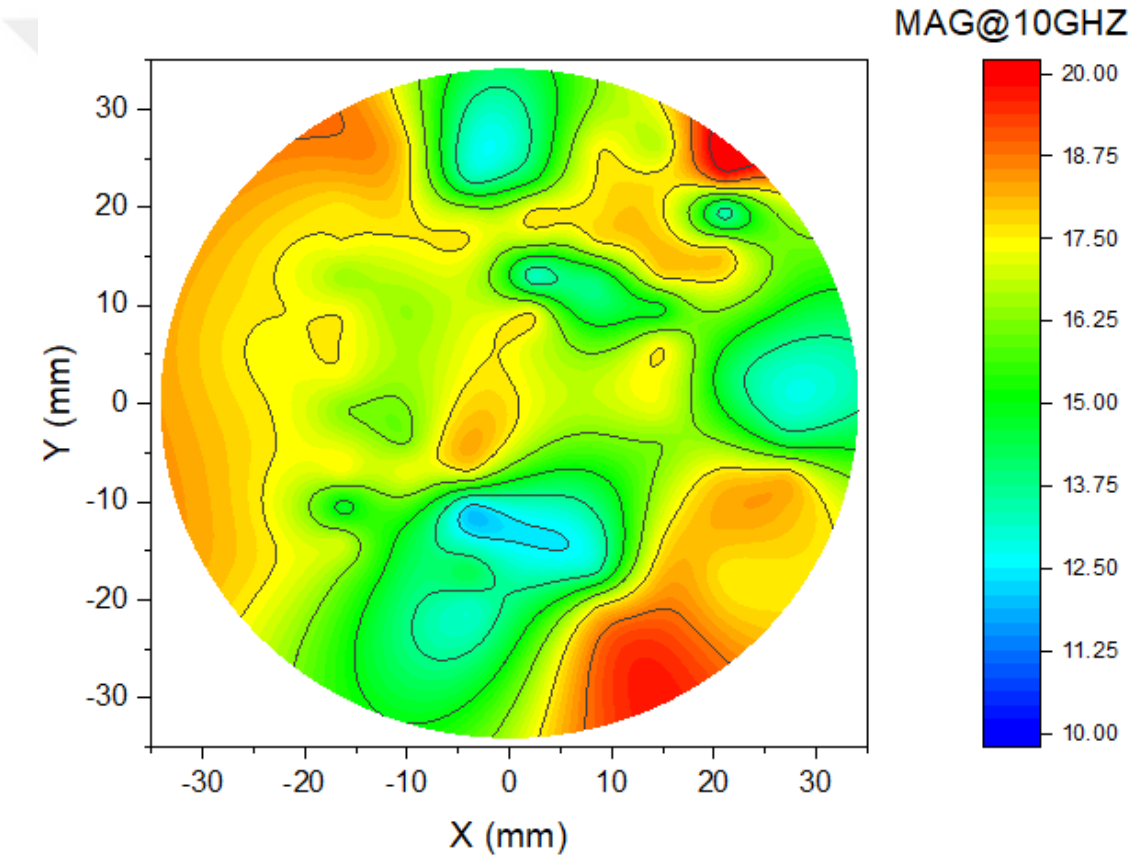
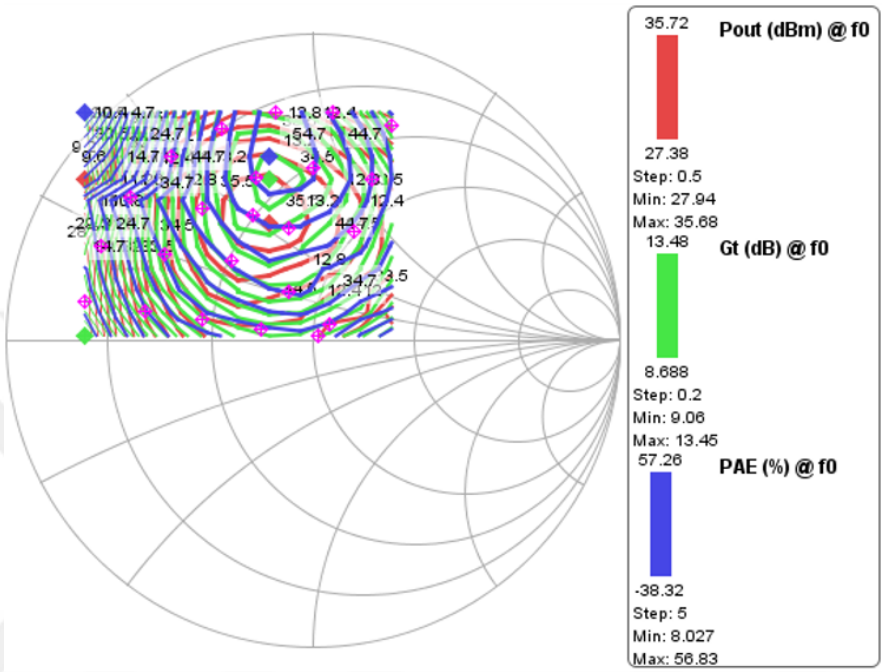
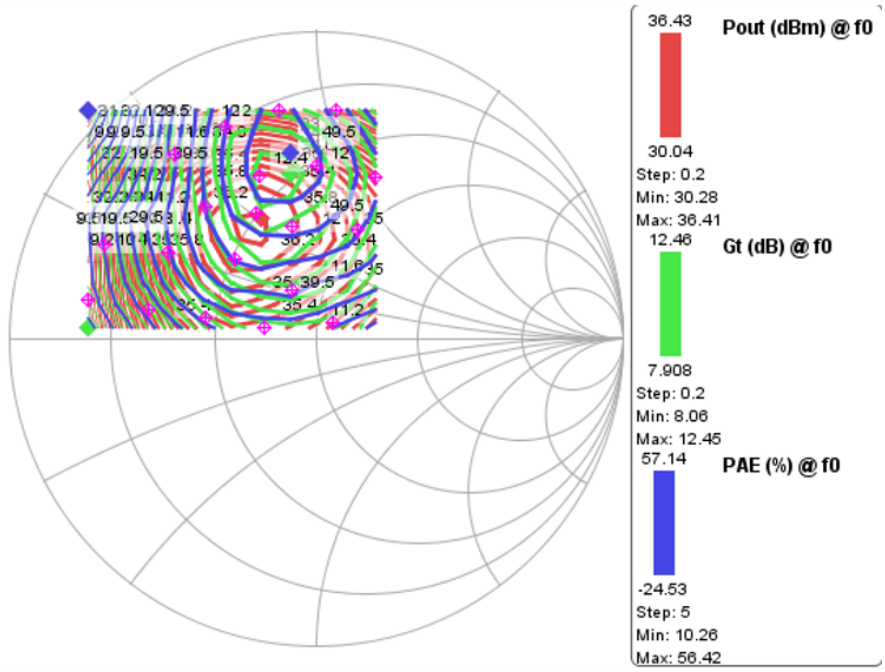


Figure 2.46: Heat map of measured MAG results of 100 8×125 μm HEMT on a wafer



(a)



(b)

Figure 2.47: 8×125 μm HEMT Load-Pull performance at (a) 3 dB compression point and (d) 3 dB compression point

2.5.4.1 Performance Summary

The performance results of the developed technology are provided in Table 2.2. The results clearly show that the developed technology is suitable for many applications up to 18 GHz.

Table 2.2: The performance summary of the technology development

Item	Parameter	Parameter Description	Value	Unit
1	$R_{sh,epi}$	The sheet resistance of the EPI layer	350	$\Omega/\square$
2	$R_{sh,TFR}$	The sheet resistance of the TFR layer	30	$\Omega/\square$
3	$C_{M1M2_{den}}$	The capacitance density of the MIM capacitors	290	pF/mm^2
4	$I_{DSS_{max}}$	The maximum current density measured at $V_{gs} = +2V$	1.2	A/mm
5	I_{DSS}	The maximum current density measured at $V_{gs} = 0V$	0.9	A/mm
6	$g_{m_{max}}$	The maximum transconductance measured at $V_{ds} = 10V$	350	mS/mm
7	R_{on}	The on-state resistance	1.8	$\Omega.mm$
8	V_{th}	The threshold voltage	3.1	V
9	f_T	The transient frequency	32	GHz
10	f_{max}	The maximum frequency of oscillation	65	GHz
11	MAG	The maximum available gain at 10 GHz	16.5	dB
12	$P_{OUT-3dB}$	The output power at 3 dB gain compression	3.7	W/mm
13	$P_{OUT-4dB}$	The output power at 4 dB gain compression	4.4	W/mm

Chapter 3

HEMT Modeling

A proper HEMT model which will satisfy MMIC designers has a good convergence between the measurements and the simulations. The convergence can be optimized using multiple formulation but the model has to be a physically reliable model. The model extraction procedure, which is defined by the model requirements, can be complex but regardless of the complexity of the model, an accurate and reliable measurement is desired.

The modeling of both active and passive devices has immense importance to develop a technology. The equivalent circuit models of the devices make the design procedure easier and shortens the time consuming design process. Moreover, the accuracy of the developed models become more critical. Hence, the modeling process, which covers defining a proper technology, device and photomask design with proper parameters, has to be studied carefully. Furthermore, configuring the equipments is critical for proper measurement and analyzing the characteristics of the components.

To develop a physically meaningful equivalent circuit model of die HEMT, a proper on-wafer calibration technique has to be preferred. There are different calibration techniques that have already been introduced in the literature. One of the most commonly used technique is the *short-open-load-thru* (SOLT) calibration

with 12-term error model. The SOLT method assumes that all the calibration standards and the impedances are precisely known. Thus, the accuracy of the SOLT calibration directly depends on the accuracy of the calibration standards, especially the thru standard [64]. Therefore, the accuracy of the SOLT method degrades at high frequencies [65].

There are also other calibration methods that require seven or eight term error model [66, 67]. The *thru-reflect-line* (TRL) method assumes that the *thru* is a lossless connection between the two ports of the DUT and it is assumed to be perfectly known [66]. There is also another calibration standard that is similar to the TRL standard called as *thru-match-reflect* (TMR) also known as TRM method [68]. The TRM method requires a match standard instead of the line standard in comparison with the TRL method. There is another method called as *line-reflect-match* (*LRM*) that is a derivative of TRM method. The LRM and its variant *line-reflect-reflect-match* (LRRM) are videly used for on-wafer calibrations besides the TRL standard [69]. The LRRM method does only require the real part of the match standard and does not require exactly known calibration standards instead of SOLT method [70]. It has been reported that the LRRM technique has significantly higher accuracy, lower error magnitudes, in comparison with the SOLT method according to measurement comparison at 40 GHz [71].

The reports show that the TRL and the LRRM methods are more appropriate for on-wafer characterizations. Furthermore these methods have better accuracy at high frequencies. Since, the LRRM method is not fully integrated with all types of measurement systems, the TRL method is more common for the on-wafer calibrations.

In Fig. 3.1, Small-Signal Model of a HEMT is given with intrinsic parameters in a block-box to represent the extrinsic parameters in a more obvious way. To extract a proper HEMT model, extraction of the extrinsic parameters plays a critical role. If there is an important error in extracted extrinsic parameters, it directly affects the precision of parameters of intrinsic HEMT which results with low level of convergence between simulation and measurements since the

parameters are not physically correct. Therefore, before beginning to extract intrinsic parameters, extrinsic parameters have to be studied with proper extraction methods with accurate measurements and required time has to be spent on the extraction of extrinsic parameters.

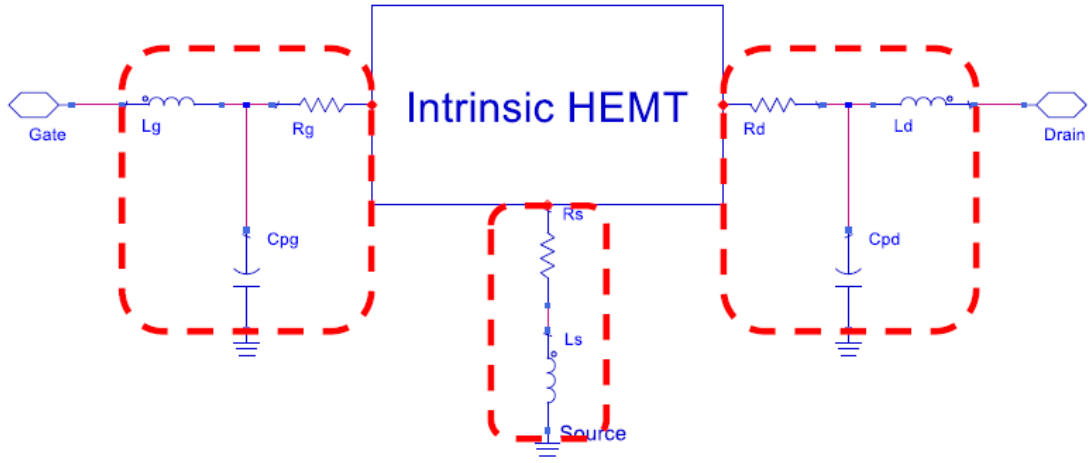


Figure 3.1: HEMT Small-Signal Model. Extrinsic Parameters are represented out of the Intrinsic HEMT box

In this chapter, required measurements will be introduced to extract extrinsic parameters of a HEMT. Then, the extraction of the values of the parasitic elements will be explained and how to separate them from the actual measurements to get intrinsic S-parameters will be discussed.

3.1 HEMT Small-Signal Modeling

There are two important parts for the small-signal model extraction: (*i*) the extrinsic parameter extraction and (*ii*) the intrinsic parameter extraction. Thus, to obtain the physically meaningful circuit parameters, the proper small-signal model extraction flow is provided in Fig. 3.2.

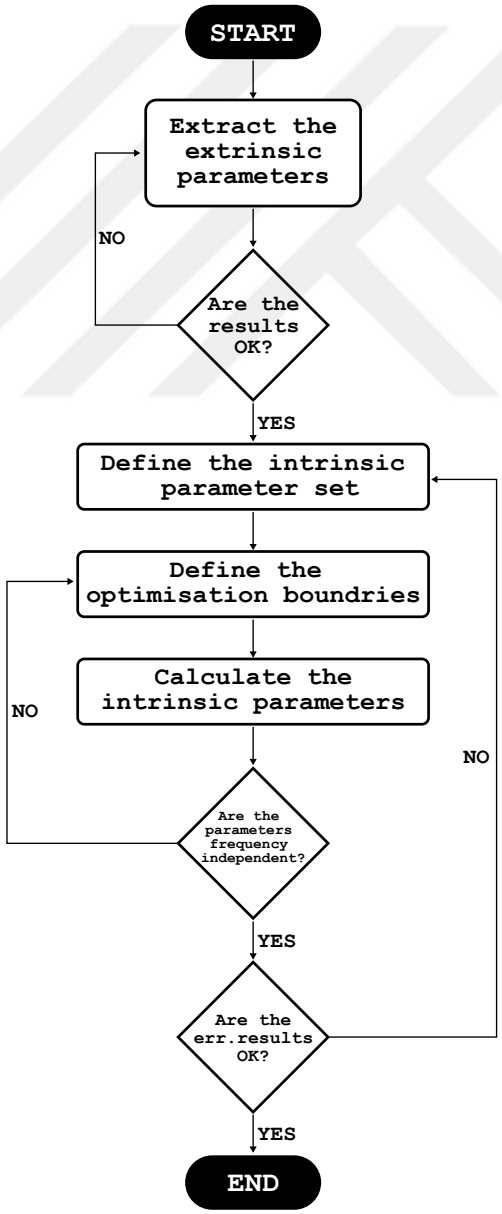


Figure 3.2: General Small-Signal modeling process flow

3.1.1 Extrinsic Parameter Extraction

There are couple of techniques to extract the extrinsic parameters of a HEMT [70]. Each method strictly relies on the measurement accuracy and required precautions have to be taken before starting measurements in order not to destroy the device and corrupt the measurements.

It is always good to have multiple devices for the modeling measurements but sometimes device count can be limited. Some of the measurement methods can be catastrophic for the device under test (DUT). Therefore, those methods are not explained here. There are two methods which are widely accepted to extract the extrinsic parameters which are the *cold-FET* method also known as the textitpinched-FET method and the *unbiased-FET* method. These methods are originally developed for GaAs HEMTs, and they are also suitable for AlGaN/GaN HEMTs.

The extrinsic parameters, R_g, R_d, R_s, L_g, L_d, L_s, C_{pg}, C_{pd}, are bias independent they are essential to obtain the physically meaningful intrinsic circuit parameters. Thus, the pinched-FET and the unbiased-FET methods are very useful and they can be used for extracting all the extrinsic parameters. In this research they are both used simultaneously for the extraction flow.

3.1.1.1 Pinched-FET Method

In [72] it has been suggested that making S-parameter measurements at zero drain bias voltage can be used for extracting the device parasitics. In Pinched-FET method, HEMT is biased at $V_{ds} = 0V$ and $V_{gs} \ll V_P$ and S-parameters are measured at that bias condition [73]. By doing this measurement at that conditions, equivalent circuit is simplified and it looks like as in Fig. 3.3.

Using the equivalent circuit topology given in Fig. 3.3 and the Pinched-FET S-parameter measurements, C_{pg}, C_{dp}, and C_b can be calculated by converting S-Parameters to Y-parameters with the following formulas [73].

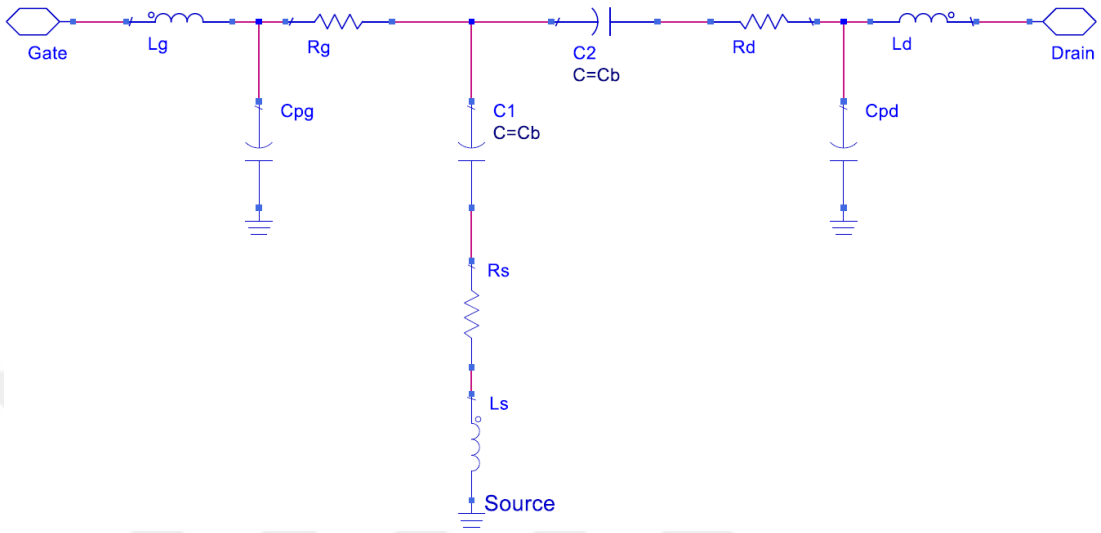


Figure 3.3: Pinched-FET Equivalent Circuit ($V_{ds} = 0V$, $V_{gs} \ll V_P$)

$$Im(Y_{11}) = \omega(C_{pg} + 2C_b) \tag{3.1}$$

$$Im(Y_{12}) = Im(Y_{21}) = -\omega C_b \tag{3.2}$$

$$Im(Y_{22}) = \omega(C_{pd} + C_b) \tag{3.3}$$

$$C_b = -\frac{Im(Y_{12})}{\omega} \tag{3.4}$$

$$C_{pg} = \frac{Im(Y_{11})}{\omega} - 2C_b \tag{3.5}$$

$$C_{pd} = \frac{Im(Y_{22})}{\omega} - 2C_b \tag{3.6}$$

C_b can be directly calculated from Eq. 3.4 which is directly derived from Eq. 3.2. Then C_{pg} and C_{pd} can be calculated from Eq. 3.5 and Eq. 3.6, respectively.

3.1.1.2 Unbiased-FET Method

Without forward-biasing the gate, it is also possible to extract the extrinsic parameters of a HEMT. The basic point of this method is that the HEMT is biased at $V_{gs} = V_{ds} = 0V$ [72]. As presented in [74], if a HEMT is biased with zero drain voltage, the region under the gate can be described with R-C transmission line. Under the unbiased condition, the equivalent circuit is a simple circuit as in Fig. 3.4 [75].

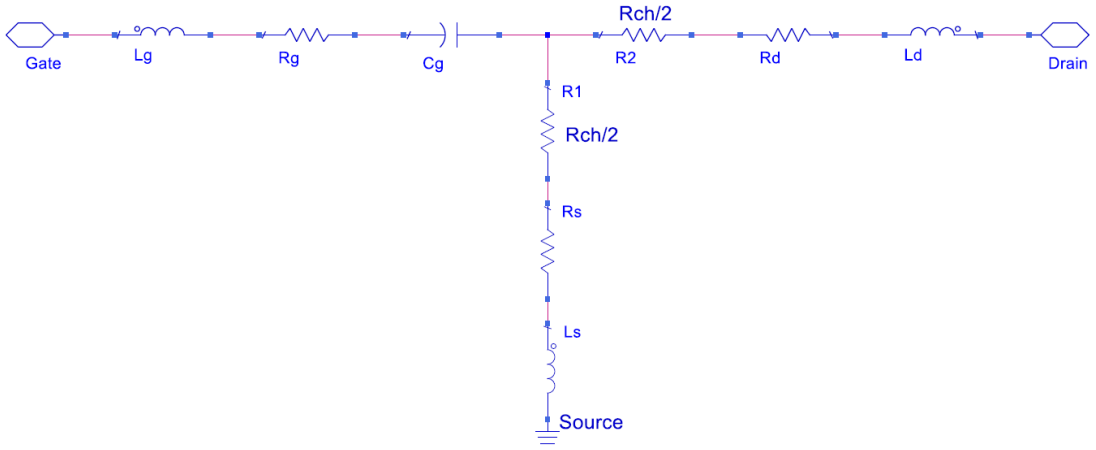


Figure 3.4: Unbiased-FET Equivalent Circuit Topology ($V_{gs} = V_{ds} = 0V$)

Using the equivalent circuit topology given in Fig. 3.4 and the Unbiased-FET S-parameter measurements, R_s, R_d, R_g, R_{ch}, L_s, L_d, and L_g can be calculated by converting S-Parameters to Z-parameters with the following formulas [75].

$$Z_{11} = R_s + 0.5R_{ch} + R_g + j(\omega(L_g + L_s) - \frac{1}{\omega C_g}) \tag{3.7}$$

$$Z_{12} = Z_{21} = R_s + 0.5R_{ch} + j\omega L_s \tag{3.8}$$

$$Z_{22} = R_s + R_{ch} + R_d + j\omega(L_d + L_s) \tag{3.9}$$

$$Re(Z_{11}) = R_s + 0.5R_{ch} + R_g \tag{3.10}$$

$$Re(Z_{12}) = R_s + 0.5R_{ch} \tag{3.11}$$

$$Re(Z_{22}) = R_s + R_{ch} + R_d \tag{3.12}$$

$$R_g = Re(Z_{11}) - Re(Z_{12}) \tag{3.13}$$

$$L_s = \frac{Im(Z_{12})}{\omega} \tag{3.14}$$

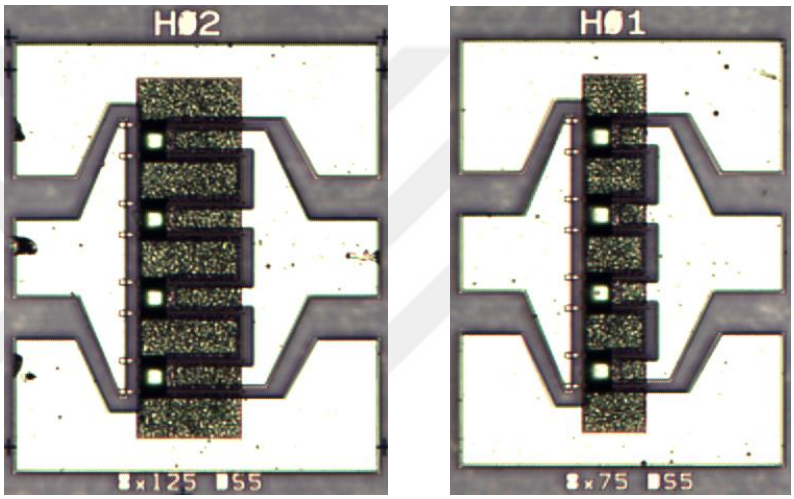
$$L_d = \frac{Im(Z_{22}) - Im(Z_{12})}{\omega} \tag{3.15}$$

After the extraction of all extrinsic parameters, extraction of intrinsic parameters starts. The intrinsic FET parameter extraction will give poor results if the values of extrinsic parameters are not ideal. During the extraction of parasitics, resistance values can result in negative values or no solution at all. Therefore, a final step of parameter optimization and fitting of measured and simulated s-parameters of Pinched-FET and Unbiased-FET have to be performed to get realistic results.

3.1.2 Verification of Extrinsic Parameters

After completing Pinched-FET and Unbiased-FET measurements and calculating initial values of the extrinsic parameters, the verification step starts. To guarantee that the values are realistic and give proper results to converge simulation and measurement, verification has to be performed. By using the equivalent circuit

topologies given in Fig. 3.3 and Fig. 3.4, Pinched-FET and Unbiased-FET models are simulated to find the optimum parasitic values by limiting the values of the parasitics in a meaningful range. Pinched-FET measurements and simulation results of the 8×125 μm (1 mm total gate periphery) AlGaN/GaN HEMT which is depicted in Fig. 3.5 are presented in Fig. 3.7. Unbiased-FET measurements and simulation results are presented in Fig. 3.8 of the same device.



(a) (b)

Figure 3.5: (a) 8×125 μm (b) 8×75 μm AlGaN/GaN HEMT

To increase the correlation between the simulations and the measurements, one more step of control mechanism is added to the procedure. At that step, errors are calculated with the following formulas given in [76]. Eq. 3.19 represents the scalar error in the frequency band.

$$\epsilon_{ij} = \frac{|Re(\delta S_{ij,n})| + |Im(\delta S_{ij,n})|}{W_{ij}}, i, j = 1, 2; n = 1, 2, \ldots, N \tag{3.16}$$

where,

$$W_{ij} = max|S_{ij}|, i, j = 1, 2; i \neq j \tag{3.17}$$

$$W_{ii} = 1 + |S_{ii}|, i = 1, 2 \tag{3.18}$$

$$\epsilon_s = \sum_{n=1}^{N} \|\epsilon(f_n)\|_1 \tag{3.19}$$

where,

$$\epsilon(f_n) = \begin{bmatrix} \epsilon_{11}(f_n) & \epsilon_{12}(f_n) \\ \epsilon_{21}(f_n) & \epsilon_{22}(f_n) \end{bmatrix} \tag{3.20}$$

Another test is also performed on the 8×75 μm AlGaN/GaN HEMT and the results are given in Fig. 3.10 for Pinched-FET measurements and simulation results and Unbiased-FET measurements and simulation results are presented in Fig. 3.11.

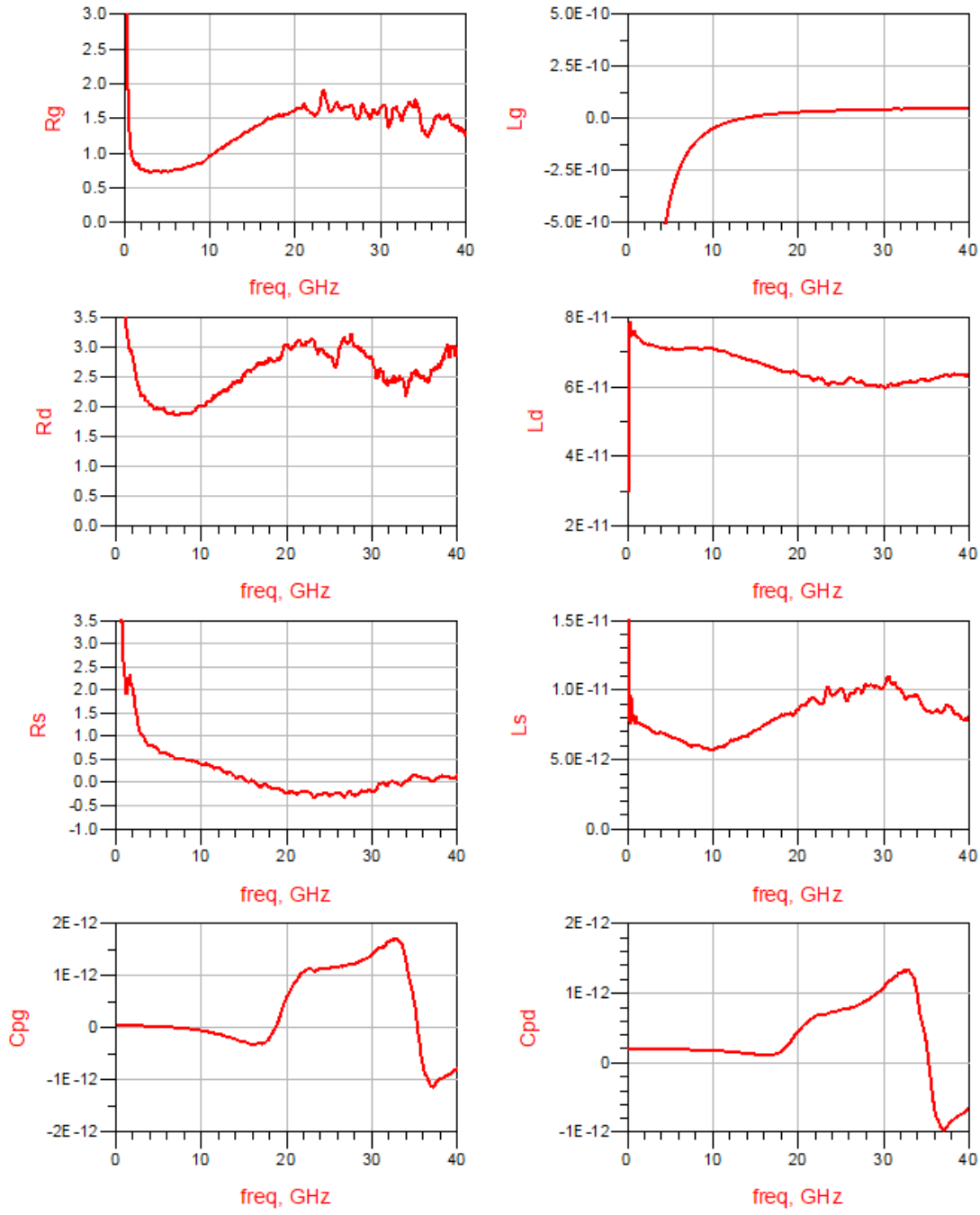
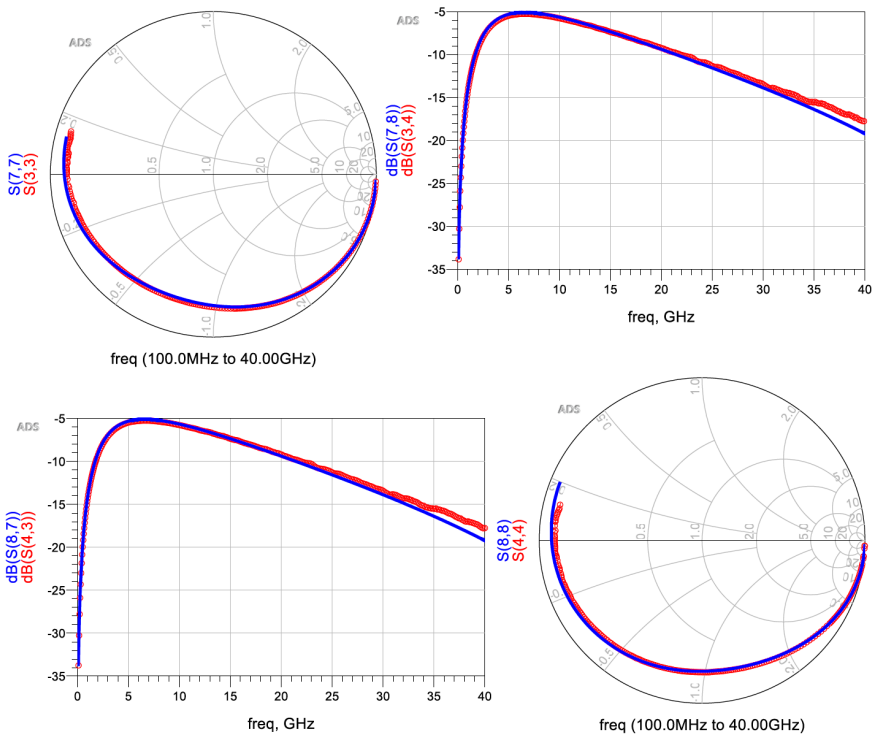
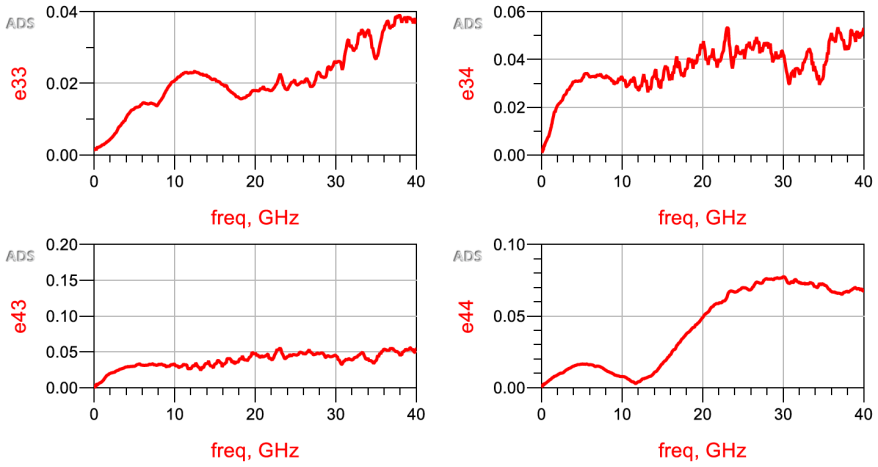


Figure 3.6: 8×125 μm extrinsic parameters vs. frequency



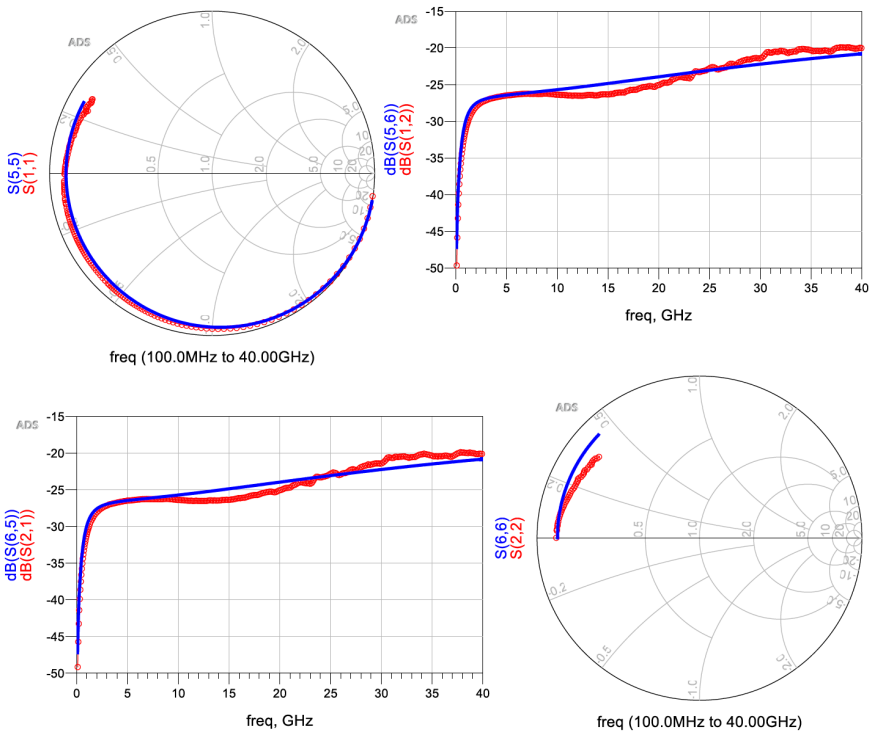
(a)

e33sc	e34sc	e43sc	e44sc
0.021	0.036	0.038	0.042



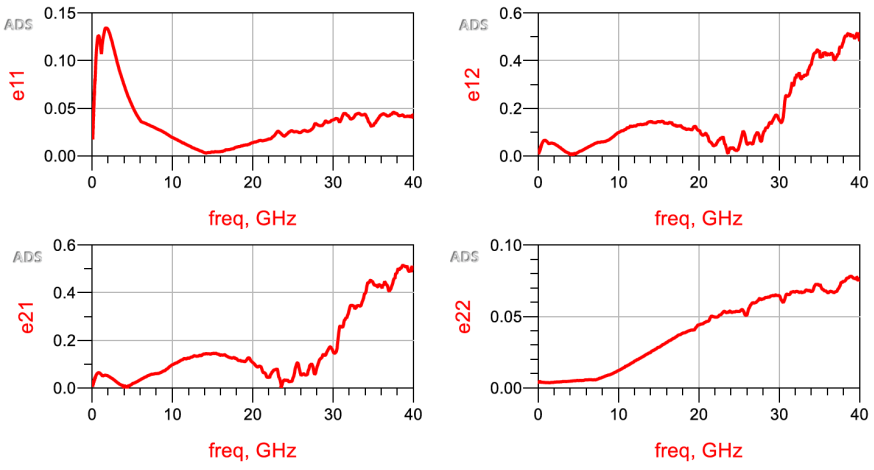
(b)

Figure 3.7: 8×125 μm HEMT (a) Pinched-FET measurement and simulation results (red: measurement, blues: simulation), (b) Errors between simulation and measurement (e33: error at S_{11}, e34: error at S_{12}, e43: error at S_{21}, e44: error at S_{22}, e33sc: scalar error at S_{11}, e34sc: scalar error at S_{12}, e43sc: scalar error at S_{21}, e44sc: scalar error at S_{22})



(a)

e11sc	e12sc	e21sc	e22sc
0.035	0.159	0.161	0.040



(b)

Figure 3.8: 8×125 μm HEMT (a) Unbiased-FET measurement and simulation results (red: measurement, blues: simulation), (b) Errors between simulation and measurement (e11: error at S_{11}, e12: error at S_{12}, e21: error at S_{21}, e22: error at S_{22}, e11sc: scalar error at S_{11}, e12sc: scalar error at S_{12}, e21sc: scalar error at S_{21}, e22sc: scalar error at S_{22})

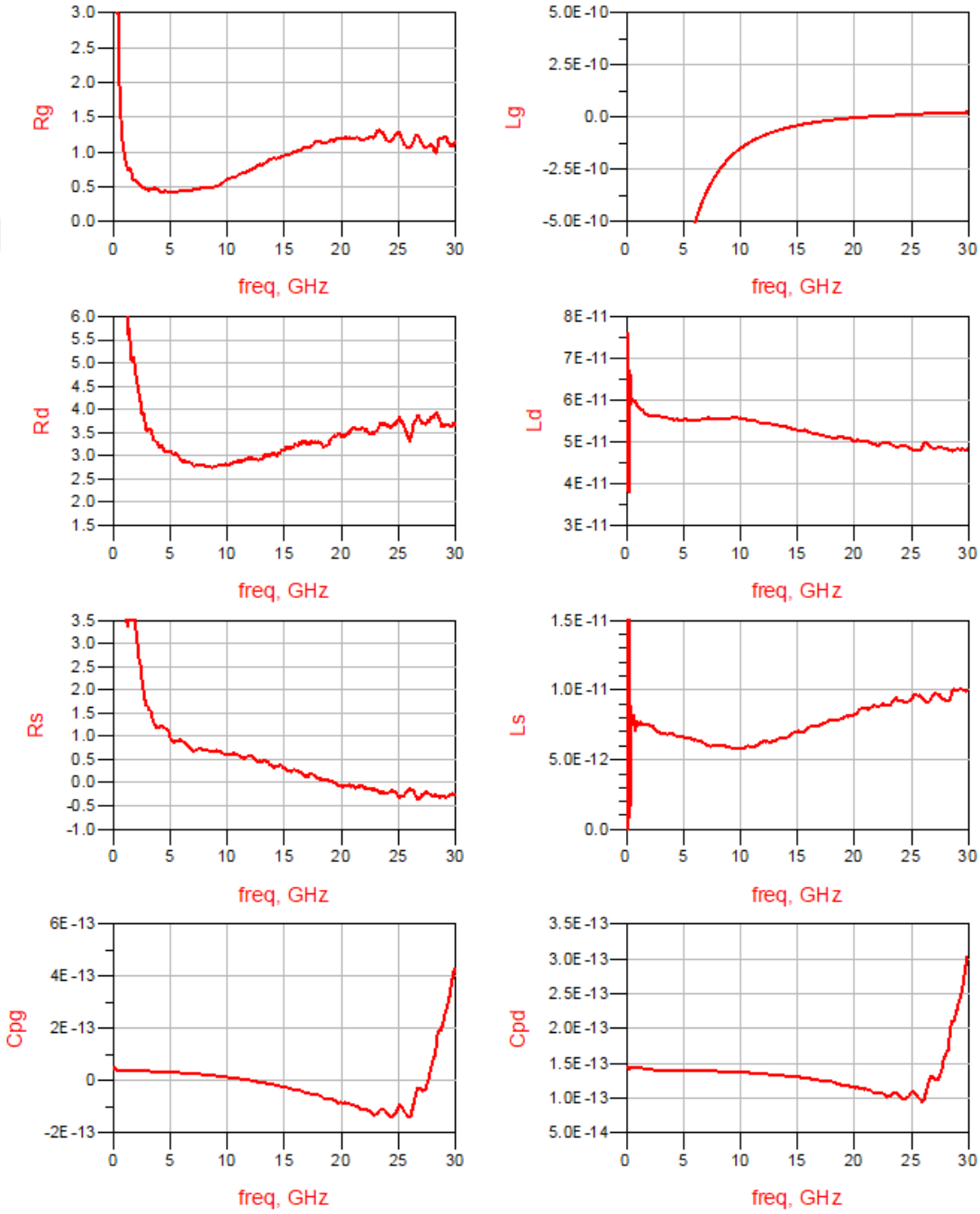
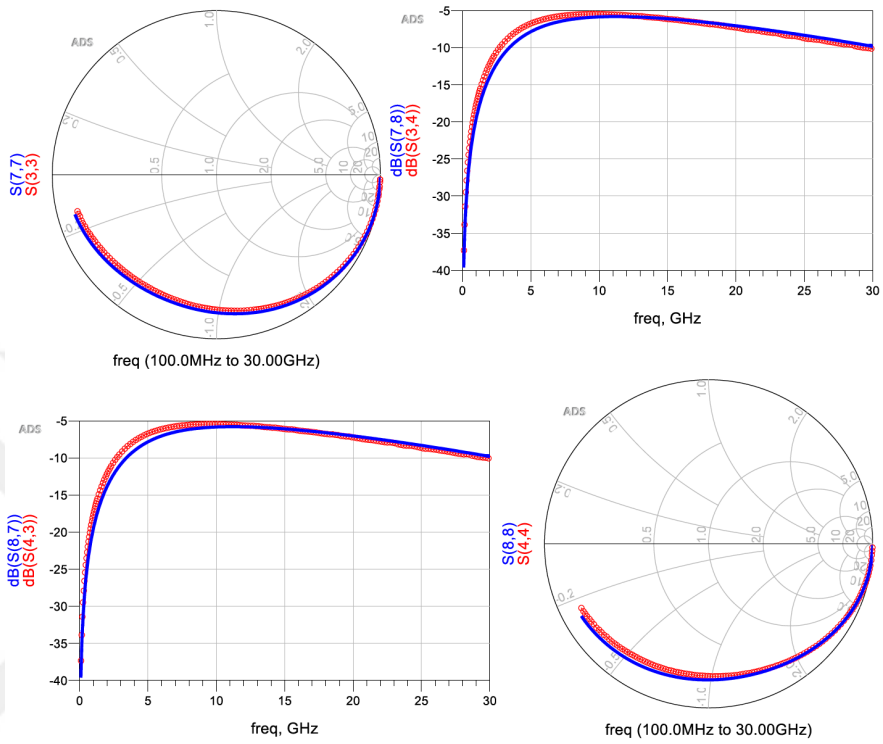
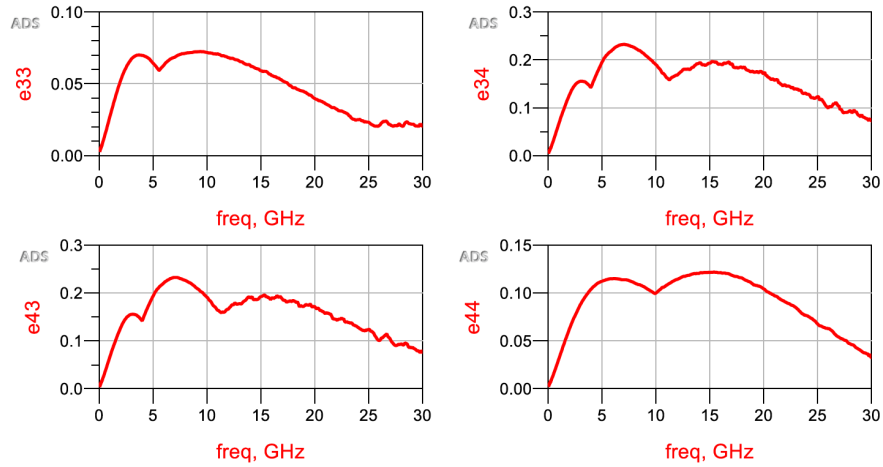


Figure 3.9: 8×75 μm extrinsic parameters vs. frequency



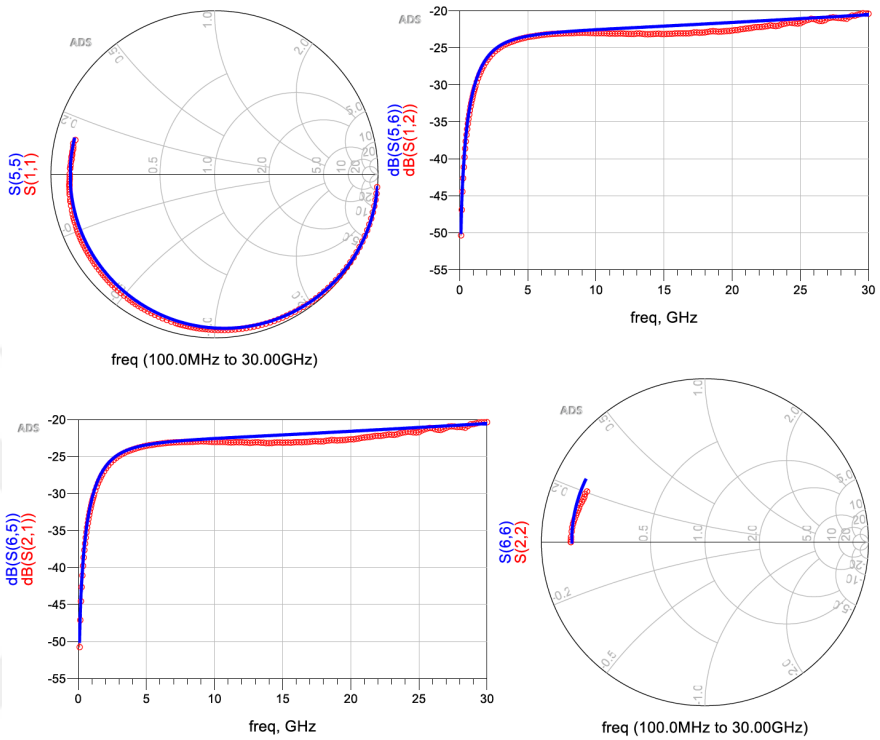
(a)

e33sc	e34sc	e43sc	e44sc
0.048	0.157	0.157	0.091



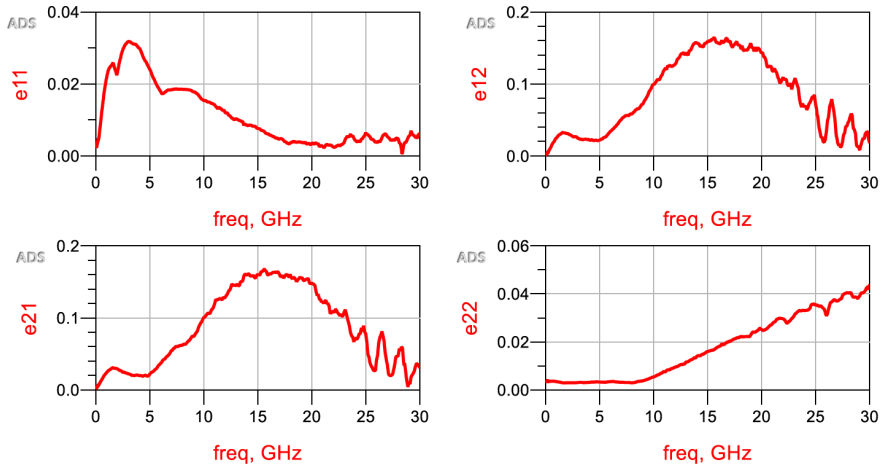
(b)

Figure 3.10: 8×75 μm HEMT (a) Pinched-FET measurement and simulation results (red: measurement, blues: simulation), (b) Errors between simulation and measurement (e33: error at S_{11}, e34: error at S_{12}, e43: error at S_{21}, e44: error at S_{22}, e33sc: scalar error at S_{11}, e34sc: scalar error at S_{12}, e43sc: scalar error at S_{21}, e44sc: scalar error at S_{22})



(a)

e11sc	e12sc	e21sc	e22sc
0.011	0.084	0.086	0.018



(b)

Figure 3.11: 8×75 μm HEMT (a) Unbiased-FET measurement and simulation results (red: measurement, blues: simulation), (b) Errors between simulation and measurement (e11: error at S_{11}, e12: error at S_{12}, e21: error at S_{21}, e22: error at S_{22}, e11sc: scalar error at S_{11}, e12sc: scalar error at S_{12}, e21sc: scalar error at S_{21}, e22sc: scalar error at S_{22})

Table 3.1: 8×125 μm HEMT extracted extrinsic parameters

L_g	L_d	L_s	C_b	C_{pg}	C_{pd}	C_{ds}	C_g	R_g	R_d	R_s	R_{ch}
(pH)	(pH)	(pH)	(pF)	(fF)	(fF)	(pF)	(Ω)	(Ω)	(Ω)	(Ω)	(Ω)
47.5	74	10	0.33	30	30	0.145	2.8	1.35	1.05	0.325	2

Table 3.2: 8×75 μm HEMT extracted extrinsic parameters

L_g	L_d	L_s	C_b	C_{pg}	C_{pd}	C_{ds}	C_g	R_g	R_d	R_s	R_{ch}
(pH)	(pH)	(pH)	(pF)	(fF)	(fF)	(pF)	(Ω)	(Ω)	(Ω)	(Ω)	(Ω)
45	55	10	0.17	60	60	0.046	1.31	1.05	1.2	0.3	3.65

Considering the results given in Fig. 3.6 and Fig. 3.9, the values of the extrinsic parameters are changing with respect to frequency. Moreover, L_g, C_{pg}, and C_{pd} may result with negative values. These values are unphysical and they reveal that the results are needed to be averaged over the measurement range. The average values can also result with negative values. Therefore, the results calculated with the equations from Eq. 3.1 to Eq. 3.15 can be only used as the initial values for the further optimisations.

The extrinsic parameters are the essential part of the intrinsic parameter extraction. If the extrinsic parameters are wrong and fixed for the process, then the intrinsic parameter extraction process will most likely end up with wrong results.

3.1.3 Intrinsic Parameter Extraction

As explained in the verification section, the methods defined in [72, 73, 75] may end up with unphysical extrinsic parameter results and require additional optimisations. Thus, an alternative approach is developed to extract the extrinsic parameters.

This method does not require pinched-FET and unbiased-FET measurements. At least three measurements at different bias points are required to extract both the extrinsic and the intrinsic parameters at a bias point. Each measurement is used to extract the parameters simultaneously.

The small-signal HEMT model is depicted in Fig. 3.12. It consists 8 extrinsic and 9 intrinsic parameters. The intrinsic parameters are:
C_{gs}: The gate-source capacitance
C_{ds}: The drain-source capacitance
C_{gd}: The gate-drain capacitance
R_i: The gate-source resistance
R_{ds}: The drain-source resistance
R_{gd}: The gate-drain resistance
R_{leak}: The leakage resistance
g_m: The transconductance
τ: The transient time delay

It is also possible to add a second current source to the model, which is controlled by V_{gd} to represent the possible output delay [77, 78]. The second current source is more useful at higher operation frequencies. Since the transistors used in this work operate up to 18 GHz, there is no need for the second current source.

The alternative approach uses the test bench presented in Fig. 3.13. The measurements at 12 V, 20, and 28 V drain bias (V_D) with 100 mA/mm drain current (I_D) are preferred to extract the extrinsic and the intrinsic parameters simultaneously. It is also possible to use the pinched-FET and the unbiased-FET results as the initial parameters for the extraction procedure. Moreover, if the

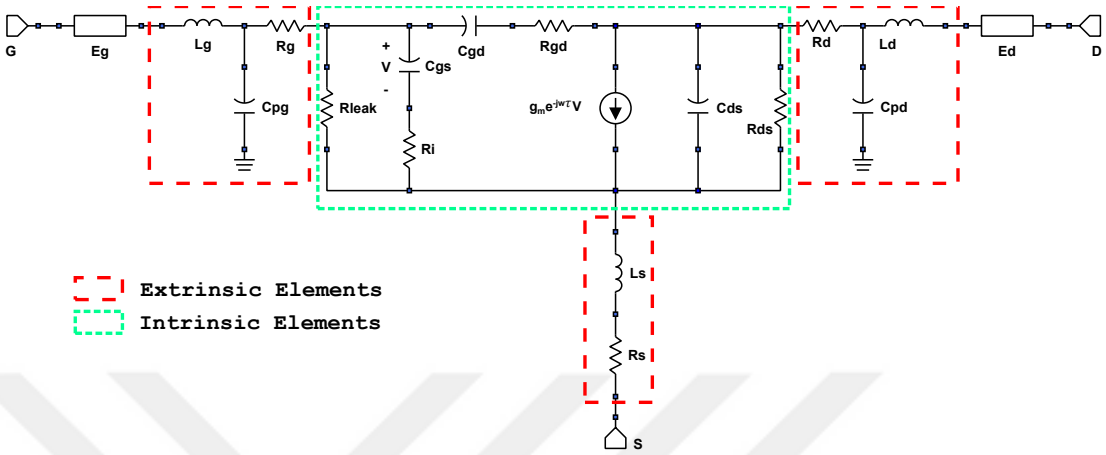


Figure 3.12: Complete Small-Signal HEMT Model. (E_g and E_d are the gate and the drain feed lines, respectively.)

process parameters, R_{sh}, R_c, and the drain-source spacing (L_{ds}) are available, they can be very useful to set the initial value for R_{ds}.

The extrinsic parameters are bias independent and they are kept the same for all bias points. The intrinsic parameters are automatically obtained by the optimisation. However, the optimisation parameters and the optimisation goals play an important role to get physically meaningful results for the intrinsic parameters. Since the Maximum Gain (G_{max}) and the Rollet's stability factor (K-factor) are the strong functions of S-parameters, they are also used as the optimisation parameters along with S_{11}, S_{12}, S_{21}, and S_{22}

The error is calculated as defined in Section 3.1.2. Errors are calculated separately for each parameter and both the individual errors and the total error are tried to be minimized.

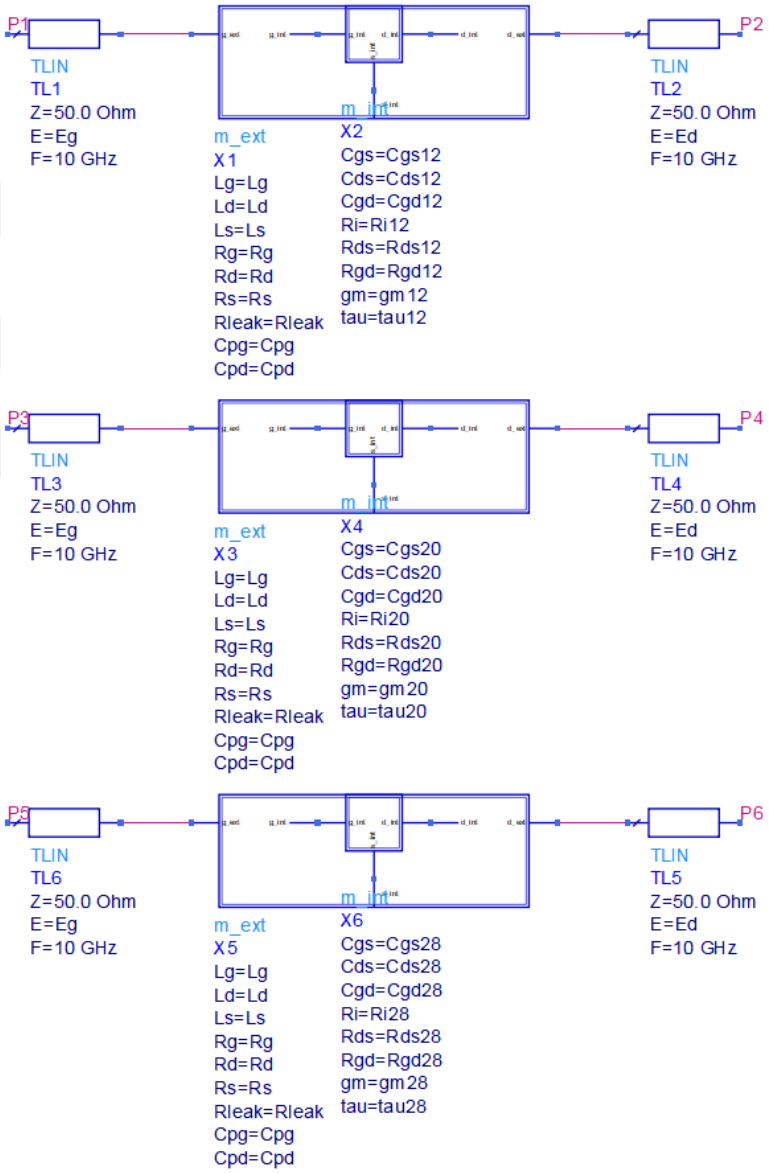
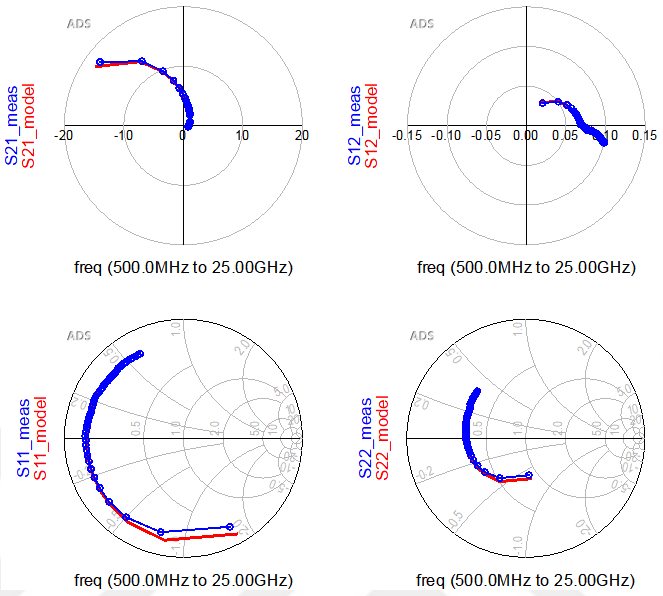
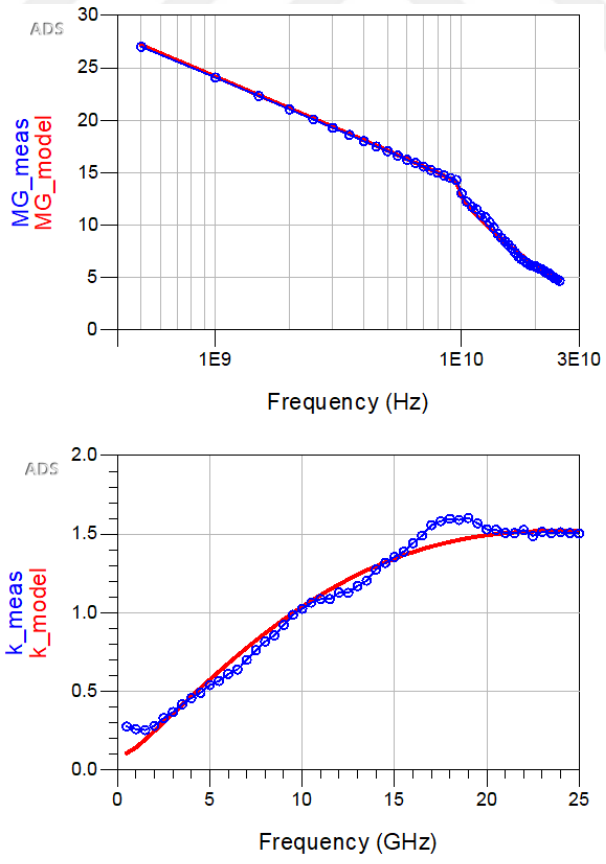


Figure 3.13: Test-bench to extract the extrinsic and the intrinsic parameters simultaneously.

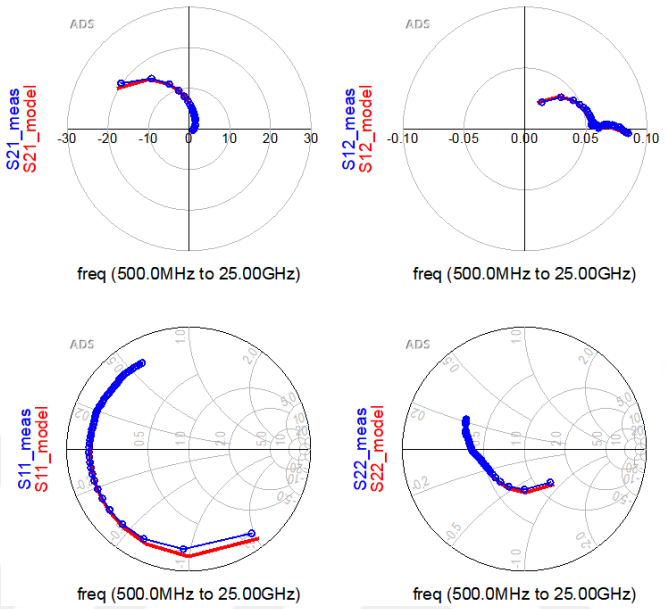


(a)

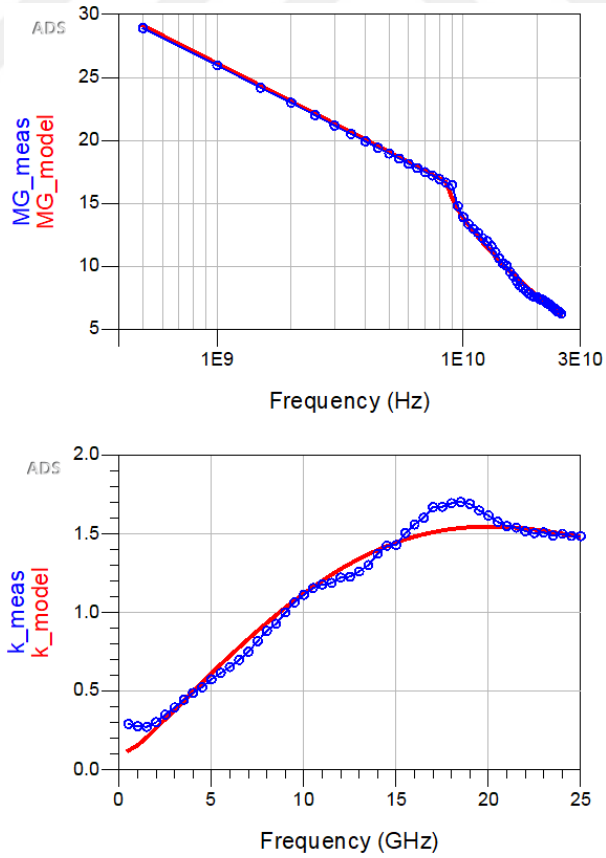


(b)

Figure 3.14: 10×125 μm HEMT (a) S-parameter and (b) MSG/MAG and K-factor model vs. measurement comparisons. ($V_D = 12V \& I_D = 100mA/mm$)

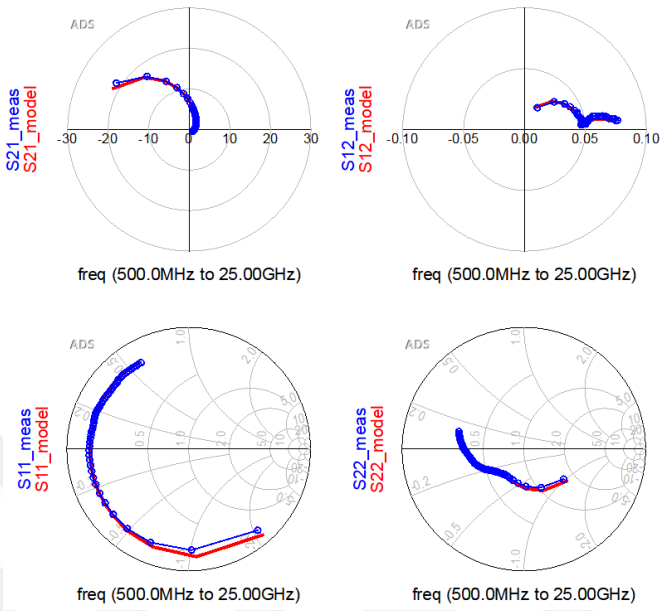


(a)

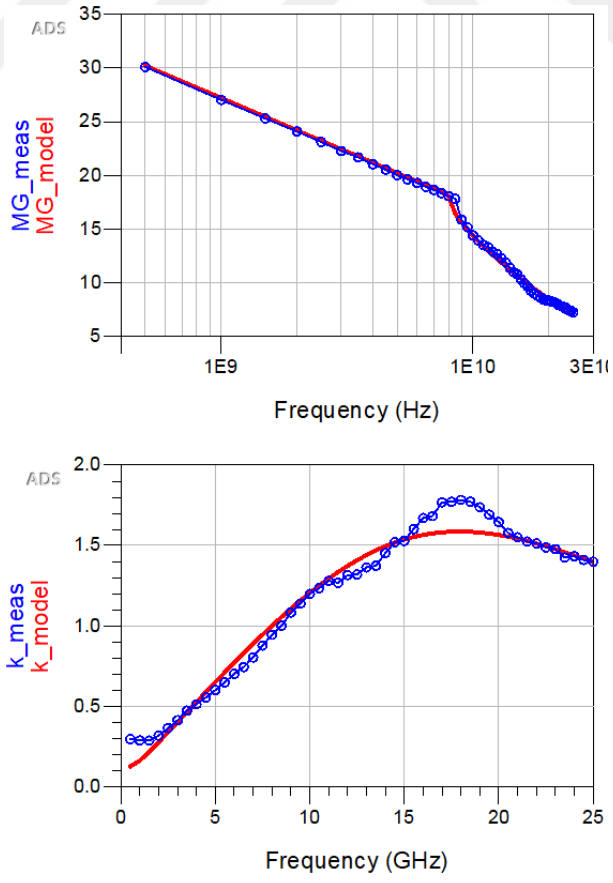


(b)

Figure 3.15: 10×125 μm HEMT (a) S-parameter and (b) MSG/MAG and K-factor model vs. measurement comparisons. ($V_D = 20V \& I_D = 100mA/mm$)



(a)



(b)

Figure 3.16: 10×125 μm HEMT (a) S-parameter and (b) MSG/MAG and K-factor model vs. measurement comparisons. ($V_D = 28V \& I_D = 100mA/mm$)

Table 3.3: Average error rates of 10×125 μm HEMT for $V_D = 12V$, $V_D = 20V$, and $V_D = 28V$ (Freq.: 0.5 GHz to 25.0 GHz)

Bias Point	err11	err12	err21	err22
$V_D = 12V$	0.9%	2.8%	0.4%	0.9%
$V_D = 20V$	1.0%	2.9%	0.5%	0.9%
$V_D = 28V$	0.9%	2.9%	0.5%	0.9%

Table 3.4: 10×125 μm HEMT extracted equivalent circuit parameters

Param.	Value	Param.	Value	Param.	Value	Param.	Value
$L_g(pH)$	13.6	$C_{gs,12}(pF)$	1.14	$C_{gs,20}(pF)$	1.29	$C_{gs,28}(pF)$	1.42
$L_d(pH)$	7.25	$C_{ds,12}(pF)$	0.13	$C_{ds,20}(pF)$	0.12	$C_{ds,28}(pF)$	0.12
$L_s(pH)$	25.03	$C_{gd,12}(pF)$	0.21	$C_{gd,20}(pF)$	0.13	$C_{gd,28}(pF)$	0.10
$R_g(\Omega)$	1.43	$R_{ds,12}(\Omega)$	84	$R_{ds,20}(\Omega)$	111.6	$R_{ds,28}(\Omega)$	140
$R_d(m\Omega)$	12	$R_{i,12}(\Omega)$	0.1	$R_{i,20}(\Omega)$	0.42	$R_{i,28}(\Omega)$	0.6
$R_s(m\Omega)$	4.13	$R_{gd,12}(\Omega)$	3.13	$R_{gd,20}(\Omega)$	3.44	$R_{gd,28}(\Omega)$	3.71
$C_{pg}(fF)$	138	$R_{leak,12}(k\Omega)$	2.3	$R_{leak,20}(k\Omega)$	2.3	$R_{leak,28}(k\Omega)$	2.3
$C_{pd}(fF)$	59	$g_{m,12}(mS)$	339	$g_{m,20}(mS)$	335	$g_{m,28}(mS)$	328
		$\tau_{12}(ps)$	2.08	$\tau_{20}(ps)$	1.91	$\tau_{28}(ps)$	2.0

3.2 HEMT Noise Modeling

The noise equivalent circuit model development is a crucial step to develop a proper LNA. To develop a proper noise model, the noise concept and the noise measurement have to be carefully studied.

3.2.1 Noise Concept

The random processes such as the flow of charges in a solid-state device, the thermal vibrations, etc. are the sources of the noise power [6, 54]. The source of the internally generated noise in a device is the random motion of the charge carriers in the device itself or the materials [54]. As a result of such random motions, different noise types occur.

i. *Thermal Noise*: The thermal noise is also known as *Nyquist* or *Johnson* noise caused by the thermally agitated charge carriers [6]

ii. *Shot Noise*: The source of the shot noise is the random fluctuations of the charge carriers inside a solid state device.

iii. *Phase Noise*: The phase noise also known as the *Flicker* noise is the random phase fluctuations in the signal itself. The phase noise is also called as $1/f$ noise, since the power of the phase noise is inversely proportional with the frequency. More information can be found in [79].

It is also possible to extend the types of noise with plasma noise and quantum noise but their sources are not directly related with the device itself.

3.2.1.1 Thermal Noise of a Resistor

Thermal noise is the main noise component in transistors. As given in Fig. 3.12, there are seven different resistors, R_g, R_d, R_s, R_i, R_{ds}, R_{gd}, and R_{leak} in the circuit model. Therefore, the concept of the thermal noise caused by the resistors become critical.

The noise model of a resistor can be represented with a series voltage source or a parallel current source as given in Fig. 3.17 [6]. The power spectral densities (PSD) of the voltage and the current sources are given in Eq. (3.21) and Eq. (3.22), respectively [6, 54].

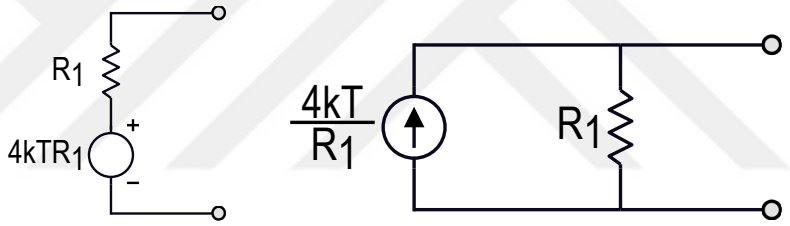


Figure 3.17: Resistor thermal noise model with (a) voltage source and (b) current source.

$$\overline{V_n^2} = 4kTR_1 \tag{3.21}$$

$$\overline{I_n^2} = V_n^2/R_1 = 4kT/R_1 \tag{3.22}$$

where

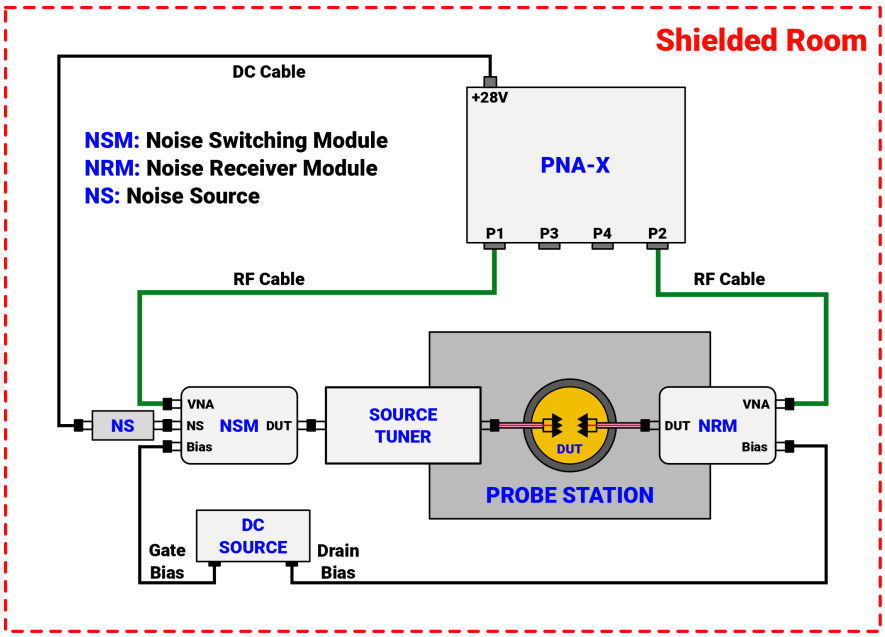
$k = 1.38 \times 10^{-23} J/K$ (Boltzmann's constant).
$T =$ the physical temperature of the resistor in kelvin (K).
$R =$ the resistance in Ω.

3.2.2 Noise Parameter Characterization Setup

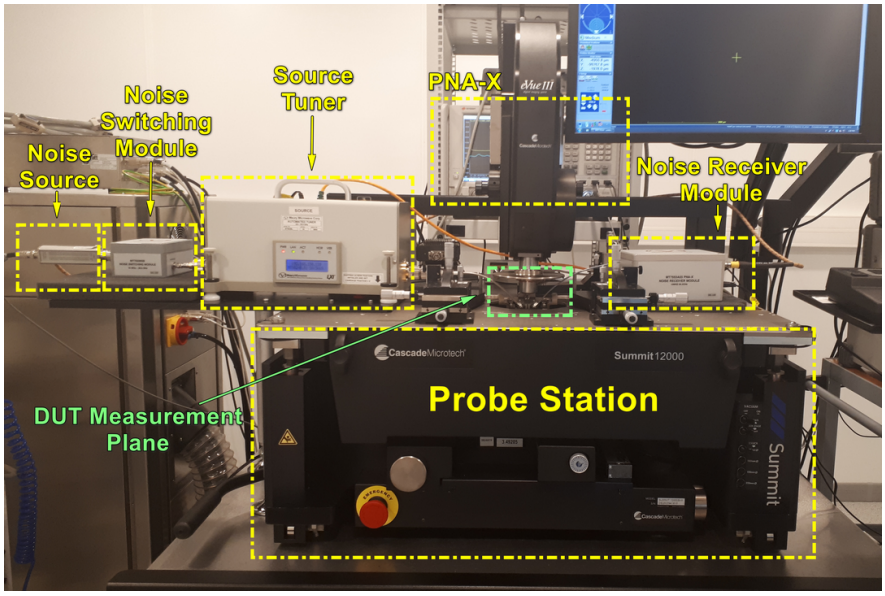
The photo of the characterization setup to measure the scattering (*S*-) parameters and the noise (*N*-) parameters is given in Fig. 3.18. The main system components of the measurement system are: the network analyzer (Keysight N5244A PNA-X), the source tuner (Maury MT982BL01), the noise source (Keysight 346C), the noise switching module (Maury MT553N26), the noise receiver module (Maury MT7553A03), the DC source (Keysight E3631A), and the probe station (Cascade Summit 1200K). The measurement system has common components with the system used in [80], but the main difference is that there is no external noise analyzer in this system. There is no need to use an external noise analyzer, since the network analyzer used in this work has an internal high quality low-noise receiver.

Although there are different representations of *N*-parameters, the common form is given in Eq. 3.23 where F_{min} is the minimum *NF*, Γ_{opt} is the optimum source reflection coefficient, R_n is the equivalent noise resistance, F is the *NF*, and Γ_S is the source reflection coefficient [80, 81].

$$F = F_{min} + 4\frac{R_n}{Z_0}\frac{|\Gamma_S - \Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2(1-|\Gamma_S|^2)} \tag{3.23}$$



(a)



(b)

Figure 3.18: (a) Block diagram and (b) the photo of the tuner based automated noise parameter measurement system.

To obtain accurate N-parameters, the calibration of the system has to be done properly. Conventionally, the Friis equation given in Eq. 3.24 is used to obtain the NF of the DUT, where F_{DUT} is the NF of the DUT, F_{total} is the total measured NF, F_{sys} is the NF of the measurement system, and G_{DUT} is the available gain of the DUT. This equation also reveals that if the DUT has low gain and the system has high NF, the measurements result with high errors. Thus, the system in Fig. 3.18 uses the noise power function provided in Eq. 3.25 [81]. The function parameters are: the measured total noise power (P), Boltzmann's constant (k), the measurement bandwith (B), the noise source temperature (T_{ns}), the reference temperature ($T_0 : 290K$), the NF of the DUT (F_{DUT}), the available gain of the DUT ($G_{a,DUT}$), the NF of the system (F_{sys}), and the transducer gain of the system ($G_{t,sys}$). Since F_{DUT} & $G_{a,DUT}$ are functions of the source impedances and F_{sys} & $G_{t,sys}$ are functions of the output impedances, they are calculated at each impedance state.

$$F_{DUT} = F_{total} - \frac{F_{sys} - 1}{G_{DUT}} \tag{3.24}$$

$$P = kB\{[T_{ns} + T_0(F_{DUT} - 1)]G_{a,DUT} + T_0(F_{sys} - 1)\}G_{t,sys} \tag{3.25}$$

The noise power method is suitable to use with both hot and cold, and "cold-only" measurements. Therefore, the reflection coefficients of the noise source is measured both for the hot and the cold states for improved accuracy during the calibration. On the other hand, the DUT NF results are calculated from cold-only formulation to obtain a fast result.

The S-parameters and the N-parameters of the DUT are obtained simultaneously by the Maury ATS software with respect to the procedure presented in Fig. 3.19. First, the S-parameters are measured at 50 Ω environment, then the system automatically switches to the N-parameter measurement. The N-parameters, which are NF_{min}, magnitude and phase of the Γ_{opt}, and the R_n are obtained at

22 different source impedances generated automatically by the source tuner for each frequency point. Since the N-parameter measurement system is limited by 1.0 GHz at the low frequency side, the measurements of the S-parameters and the N-parameters are performed from 1.0 GHz to 12.0 GHz.

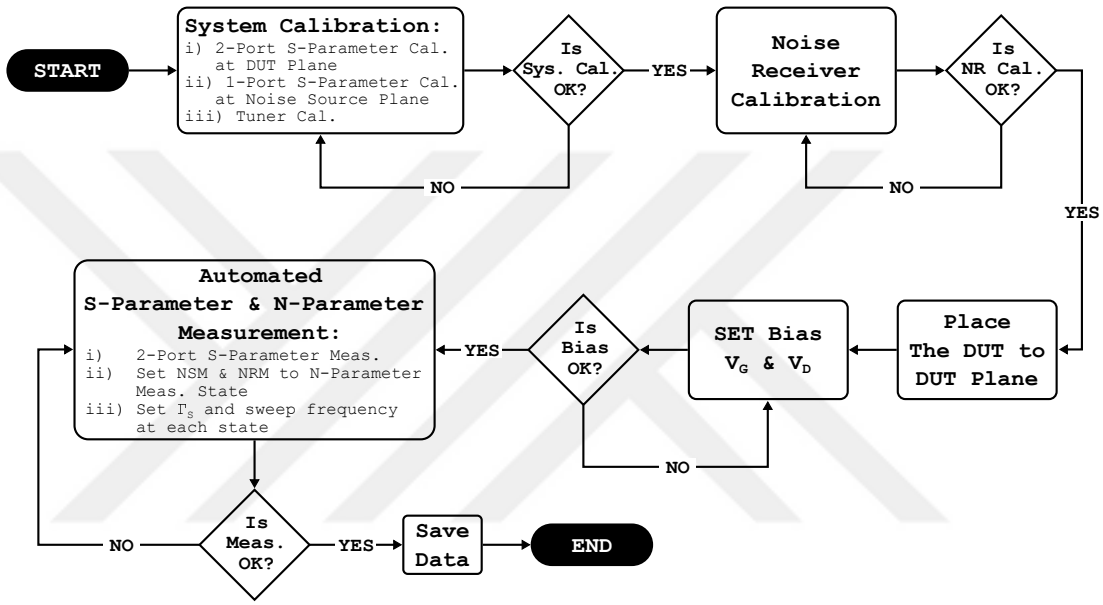


Figure 3.19: The tuner based automated noise parameter measurement flow.

3.2.3 Common Source HEMT Noise Modeling

Different modeling approaches have already been reported both for the *common-source* (CS) FET and the cascode FET. They are mainly based on EM simulations [82, 83] and assigning equivalent noise temperature to resistors of the small-signal equivalent circuit [80, 84]. The EM simulation based CS FET models have good accuracy but they require extensive simulations and careful calculations. On the other hand, noise temperature based CS FET models are easier to obtain and have high accuracy. Thus, the cascode HEMT equivalent circuit model based on the noise temperature approach is developed in this work to provide fast, accurate, and reliable outcome for designers.

The common-source (CS) HEMT shown in Fig. 3.20 is characterized with the tuner based automated N-parameter measurement system in Fig. 3.18, and no

additional measurement is used to extract the CS HEMT parameters.

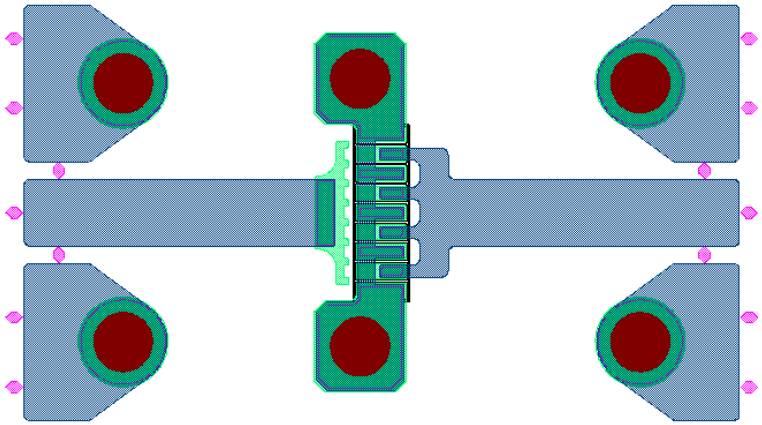


Figure 3.20: The layout of the CS HEMT

The S-parameter and the N-parameter extraction procedures are applied to the CS HEMT to extract the model parameters of the CS HEMT model given in Fig. 3.21. E_g and E_d in Fig. 3.21 represent the feed lines of the transistor at the gate and the drain sides, respectively. $T1$ and $T2$ are the noise temperatures of the resistors and R_{leak} represents the leakage path at the gate side. To extract the model parameters, S_{11}, S_{12}, S_{21}, S_{22}, NF, NF_{min}, R_n and Γ_{opt} are used as the optimization parameters. Since the stability (K-) factor and Maximum Available Gain (MAG) are strong functions of S-parameters, K-factor and MAG are constantly monitored to obtain the optimum model parameters. The comparison of the optimization parameters of the model and the measurement results of the CS HEMT are given in Fig. 3.23, Fig. 3.23, and MAG and K-factor results are presented in Fig. 3.24.

Ideally, Γ_{opt} of a CS HEMT starts from the open-circuit condition. On the other hand, Γ_{opt} of the CS HEMT in Fig. 3.23c starts from a real impedance since there exists a leakage path introduced with R_{leak}. To elaborate on the issue, the value of R_{leak} is swept and the results of Γ_{opt} is shared in Fig. 3.25. Fig. 3.25 shows that increasing leakage results with deviation of Γ_{opt} from the open-circuit condition at low frequency. This issue is the main reason of the high NF at low frequency presented in Fig. 3.23a.

To validate the accuracy of the model, the error rates of the optimization

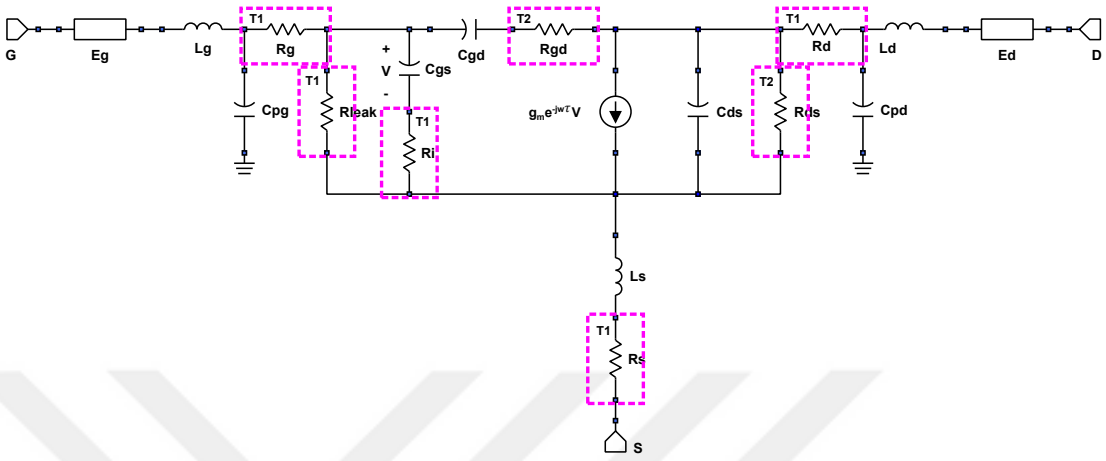


Figure 3.21: Equivalent circuit noise model of the CS HEMT

parameters are calculated with Eq. 3.26 where X_{sim} represents the simulated result and X_{meas} represents the measured result of the related parameter. The error rate results are provided in Fig. 3.26. The instant jumps in the error rates in Fig. 3.26 and the K-factor in Fig. 3.24 at ∼5.0 GHz are related with the phase change in the TRL calibration. Nevertheless, $\leq$ 0.7 % and $\leq$ 2.0 % mean error rates are achieved in S-parameters and noise parameters, respectively.

$$Err.(f) = \left| \frac{X_{sim}(f) - X_{meas}(f)}{X_{sim}(f) + X_{meas}(f)} \right| \tag{3.26}$$

The extracted CS HEMT model parameters are given in Table 3.5.

Table 3.5: The equivalent circuit parameters of the CS HEMT

Param.	Value	Param.	Value	Param.	Value	Param.	Value	Param.	Value
$L_g(pH)$	14.06	$L_d(pH)$	55.20	$L_s(pH)$	14.56	$C_{pg}(fF)$	234.3	$C_{pd}(fF)$	82.3
$R_g(\Omega)$	1.68	$R_d(\Omega)$	1.53	$R_s(\Omega)$	2.58	$R_{ds}(\Omega)$	71.03	$R_i(\Omega)$	0.70
$g_m(S)$	0.193	$\tau(ps)$	2.37	$R_{leak}(k\Omega)$	1.0	$C_{ds}(pF)$	0.03	$C_{gs}(pF)$	0.27
$C_{gd}(pF)$	0.20	$R_{gd}(\Omega)$	0.21	$T1(^{\circ}C)$	103	$T2(^{\circ}C)$	1333		

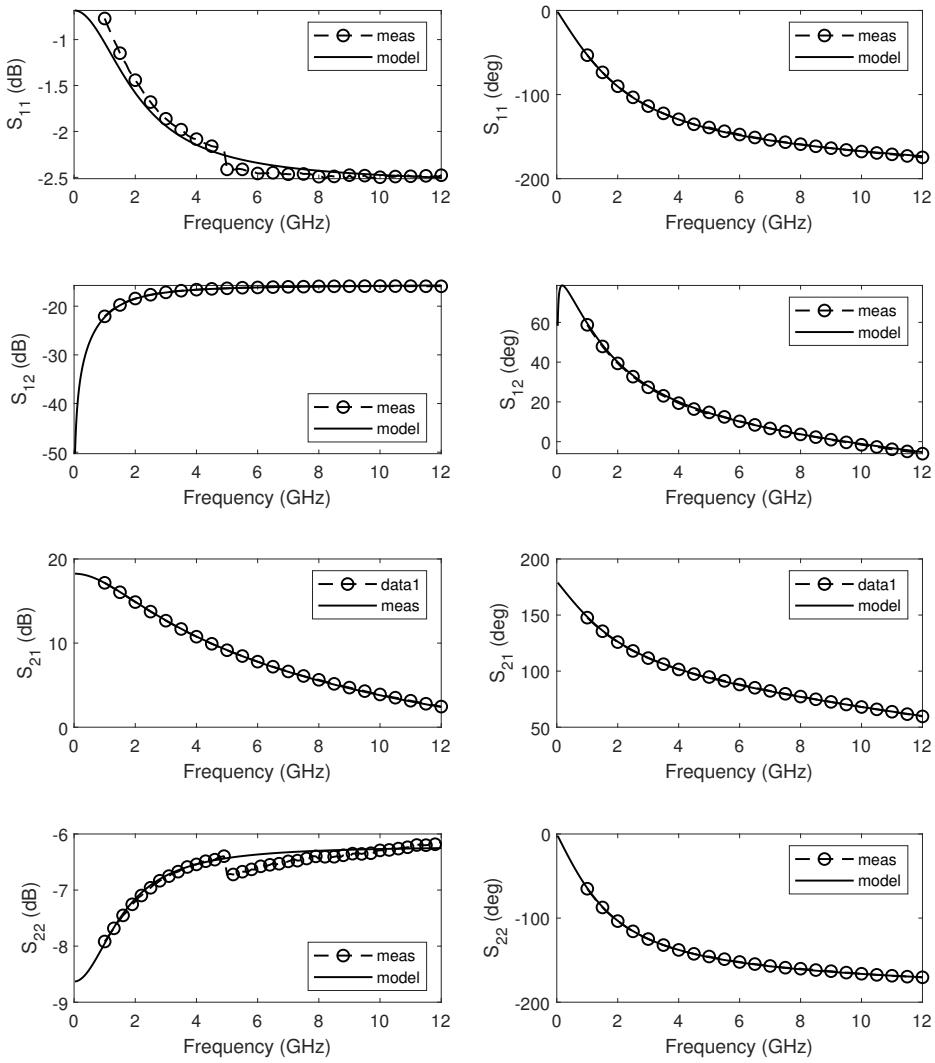
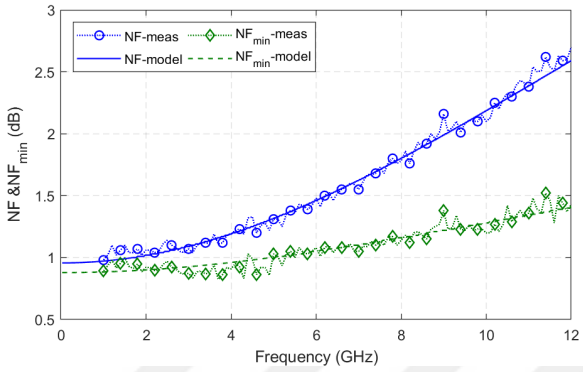
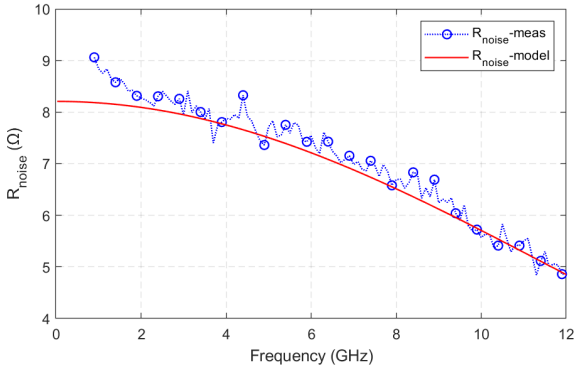


Figure 3.22: 8x75 μm CS HEMT Small-signal model vs. measurement results. Measurements from 1.0 GHz to 12.0 GHz, model simulations from 0.03 GHz to 12.0 GHz



(a)



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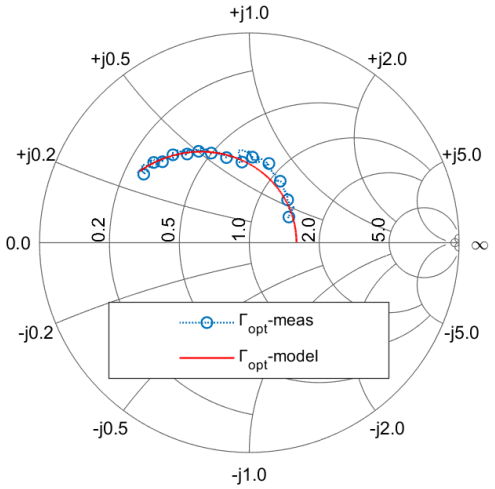


(c)

Figure 3.23: 8x75 μm CS HEMT model vs. measurement N-parameter results: (a) NF and NF_{min} results, (b) Noise Resistance results, and (c) Optimum noise reflection coefficient results

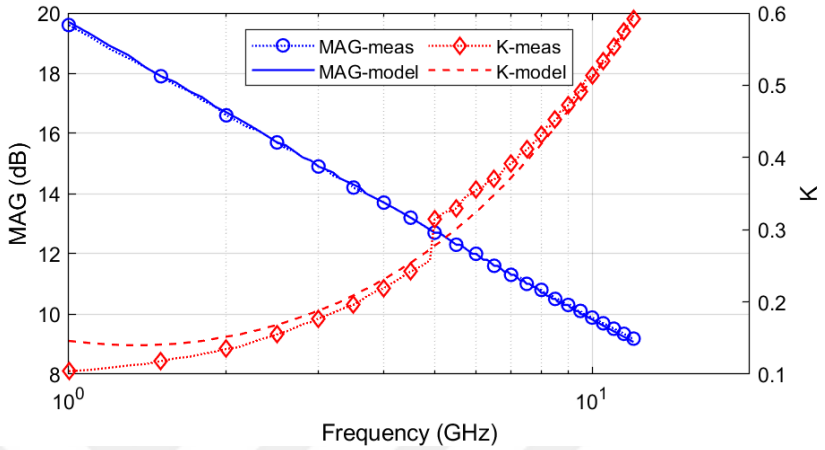


Figure 3.24: 8x75 μm CS HEMT model vs. measurement results of MAG and K-factor

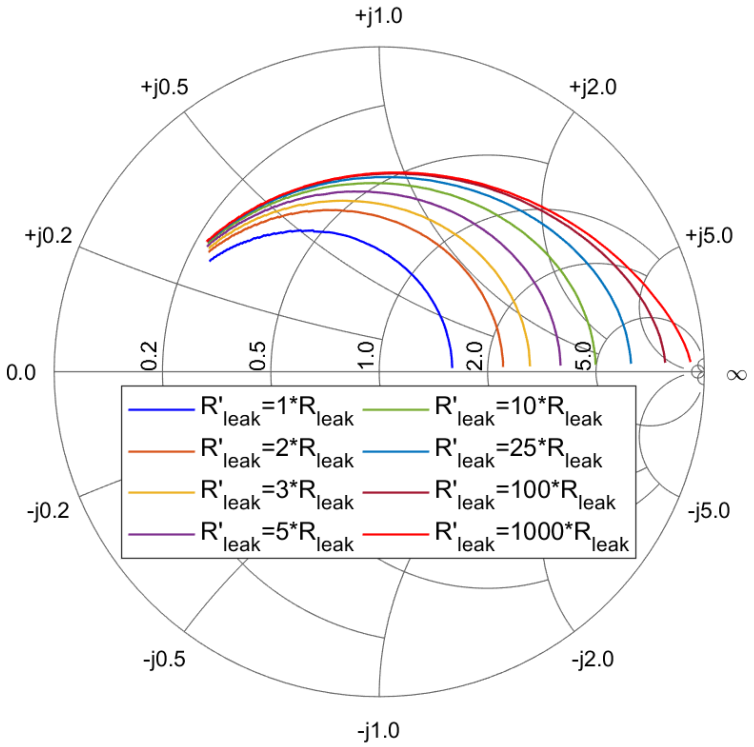


Figure 3.25: Simulated Γ_{opt} results with different R_{leak} for 8x75 μm CS HEMT (simulated from 0.1 GHz to 12.0 GHz)

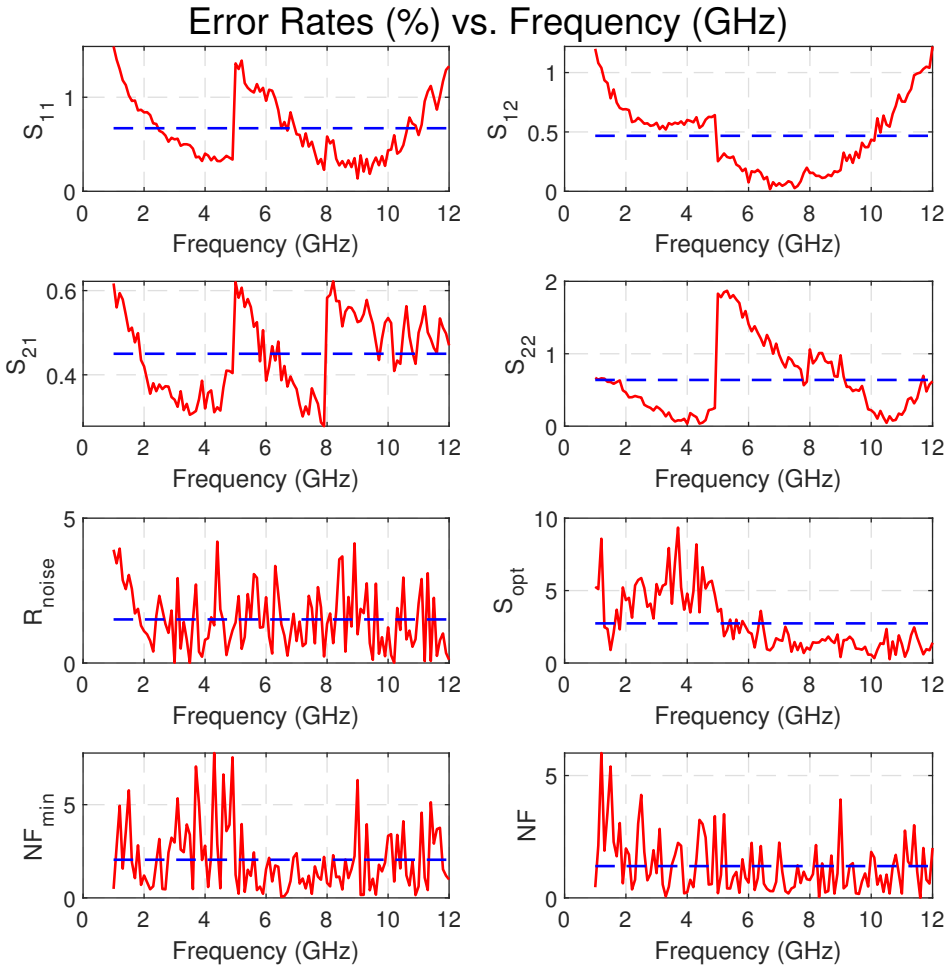


Figure 3.26: Error rates (%) of 8x75 μm CS HEMT (Solid Lines: Instant error, Dashed Lines: Mean error)

Chapter 4

Kink Effect in S_{22}

The GaN HEMT technology has gained significant importance in the industry as a result of its superior material properties [1–3]. Therefore, understanding the parameters like the kink effect (KE) in the output reflection coefficient (S_{22}), which can degrade the device performance, has become more important and multiple studies have been conducted to analyze the origin of the kink in S_{22} [2, 84–108].

4.1 Background of Kink Effect in S_{22}

The KE in S_{22} is defined as an abrupt dip in S_{22} behavior at a specific frequency as a result of the transition of the output impedance (Z_{out}) of the transistor from a low-frequency series RC circuit to a high-frequency parallel RC circuit [86]. The origin of the KE has been debated and, it has been studied by poles and zeros [89–91,93] and circuit models [84,85]. Moreover, the KE has been attributed to the feedback resistance [90], the substrate resistance [84, 85, 89, 91, 92, 96, 97], the low-frequency dispersion [108], the open dummy structure [94, 95] and the high values of transconductance (g_m) [86, 87, 98–100]. However, the KE in S_{22} depends on the intrinsic elements [88, 99]; and the extrinsic elements change its behaviour [2, 84].

The KE in S_{22} of GaN HEMTs has been attributed to the high values of g_m, but the other technologies such as GaAs and Si also suffer from the kink phenomenon [88, 90, 93, 95, 104–107]. Besides, the effect of the gate width (W_g), the bias condition and the temperature effect on the scattering (S-) parameters have been studied and the results are reported in [87, 88, 91, 101–103].

The AlGaN/GaN HEMT technology offers various L_g options such as 0.4-0.5 μm, 0.25 μm, and 0.15 μm for S-Band, X-Band, and Ka-Band applications, respectively. The L_g is not the only difference between those technologies. The device sizes, the drain-source spacing, the wafer properties, the bias conditions, etc. are the other possible differences. Therefore, direct comparison of those transistors would not be meaningful.

4.2 Test Set Development

In this study, to evaluate the effect of the gate periphery, represented in Fig. 4.1, on the KE in S_{22} of AlGaN/GaN HEMTs, 6 HEMTs with different L_g and L_{gH} values are fabricated. HEMTs with 0.2 μm, 0.25 μm, 0.30 μm, and 0.35 μm L_g with 0.9 μm L_{gH} are fabricated to investigate the effect of L_g on KE. The HEMTs with 0.7 μm and 0.9 μm L_{gH} with 0.25 μm L_g are fabricated to investigate the effect of L_{gH} on KE.

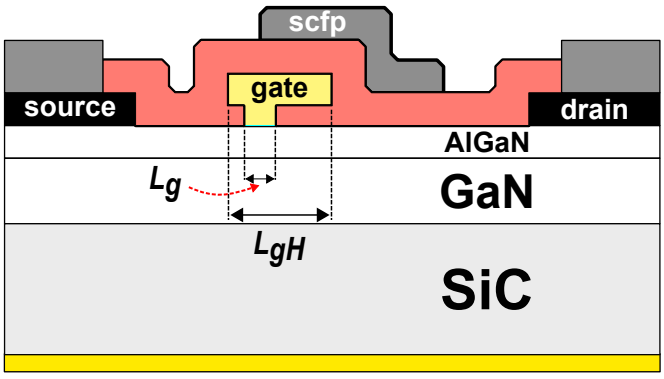
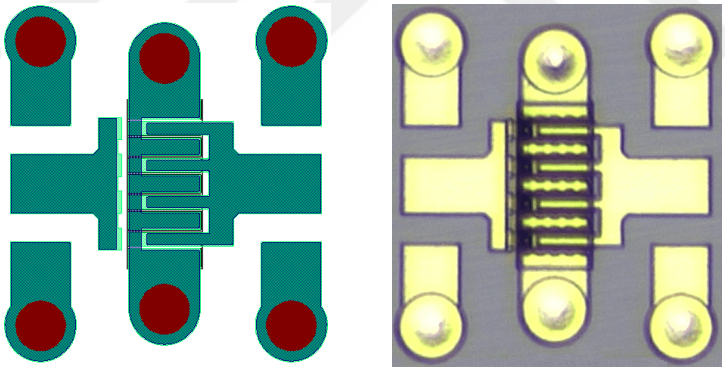


Figure 4.1: The cross-section of an AlGaN/GaN HEMT. L_g and L_{gH} are represented on thr figure.

4.3 Experimental Study and Results

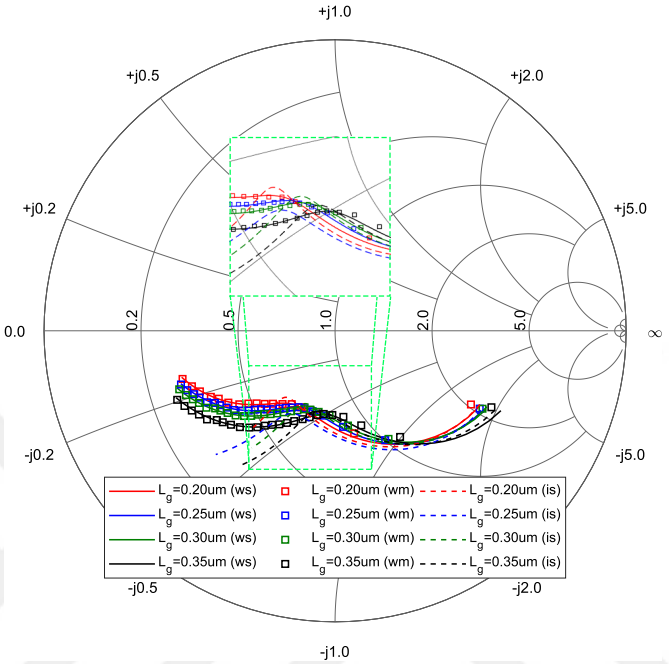
The devices used for the tests have 8×125 μm ($W_{g,tot}$ = 1.0 mm) configuration as depicted in Fig. 4.2 and are fabricated on the same wafer with the same process to eliminate the possible shifts that may affect the accuracy and the consistency of the analysis. The S-parameter measurements of the devices are performed with 28 V drain voltage (V_D) and 100 mA/mm drain current (I_D) at 25 °C chuck temperature from 0.5 GHz to 25.0 GHz.

The equivalent-circuit model, illustrated in Fig. 3.12, is used to develop the models of the HEMTs. The developed models are used for accurate analysis and the results of the models are compared with the measured S_{22} data and are presented in Fig 4.3.

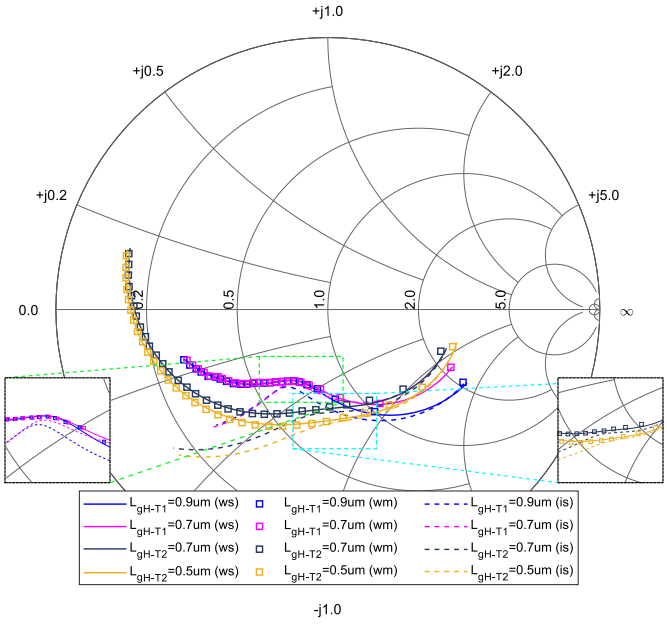


(a) (b)

Figure 4.2: (a) The layout and (b) the microphotograph of the 8×125 μm HEMT used for the tests.



(a)



(b)

Figure 4.3: Measured whole HEMT (symbols), simulated whole HEMT (solid lines) data, and simulated intrinsic HEMT (dashed lines) data of S_{22} from 0.5 GHz to 25.0 GHz (wm: measured whole HEMT, ws: simulated whole HEMT, is: simulated intrinsic HEMT, T1: technology-1, and T2: technology-2.) (a) Various Lg with 0.9 μm L_{gH}, (b) Various L_{gH} with 0.25 μm L_g.

The kink parameters: the kink frequency band (KFB), the kink frequency point (KFP), the kink size (KS), and the kink figure of merit (KFM) are calculated from the second derivative (D2) of Im(S_{22}) with respect to Re(S_{22}) as explained in [88]. Since the results of D2 from the measured data can be very noisy to evaluate the parameters properly, the simulation results of the models are used for the rest of the analysis. The complete equivalent circuit models, including both the intrinsic and the extrinsic elements, are used to extract the kink parameters.

The KFP is the frequency point where KE occurs in S_{22} and can be determined from the negative peak of D2. The KS is defined as the value of the negative peak in D2. The KFB is the frequency range between two zero crossing of D2. The KFM is the ratio of KS/KFB.

Fig. 4.4 and Fig. 4.5 show the Im(S_{22}) versus Re(S_{22}) and its corresponding first (D1) and second (D2) derivatives from 0.5 GHz to 25.0 GHz for the HEMTs with different L_g for the whole HEMT and the intrinsic HEMT, respectively. Fig. 4.6 illustrates the kink parameters for the HEMTs with different L_g.

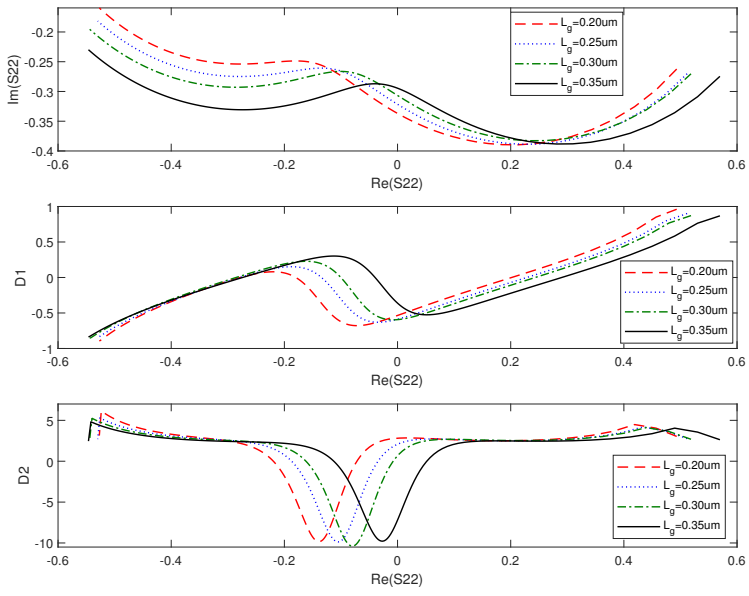


Figure 4.4: Im(S_{22}) versus Re(S_{22}), first, and second derivatives of Im(S_{22}) wrt. Re(S_{22}): The whole HEMTs with different L_g values (L_{gH} = 0.9 μm).

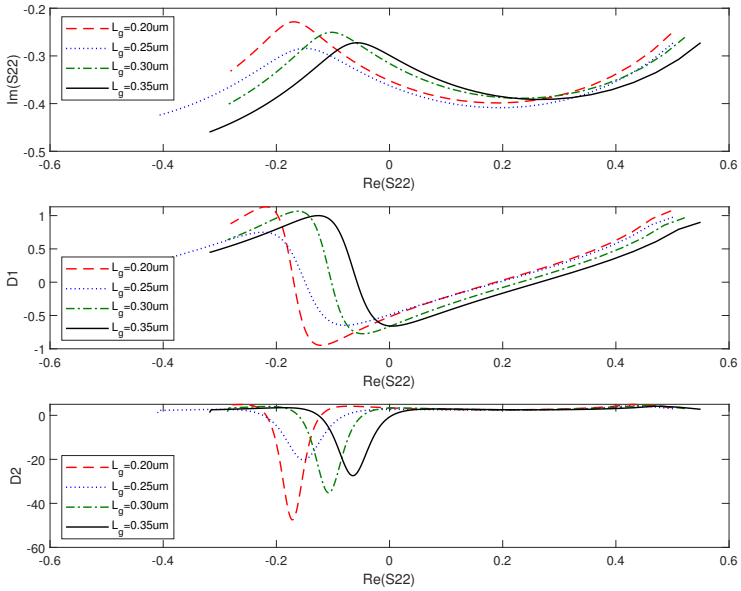
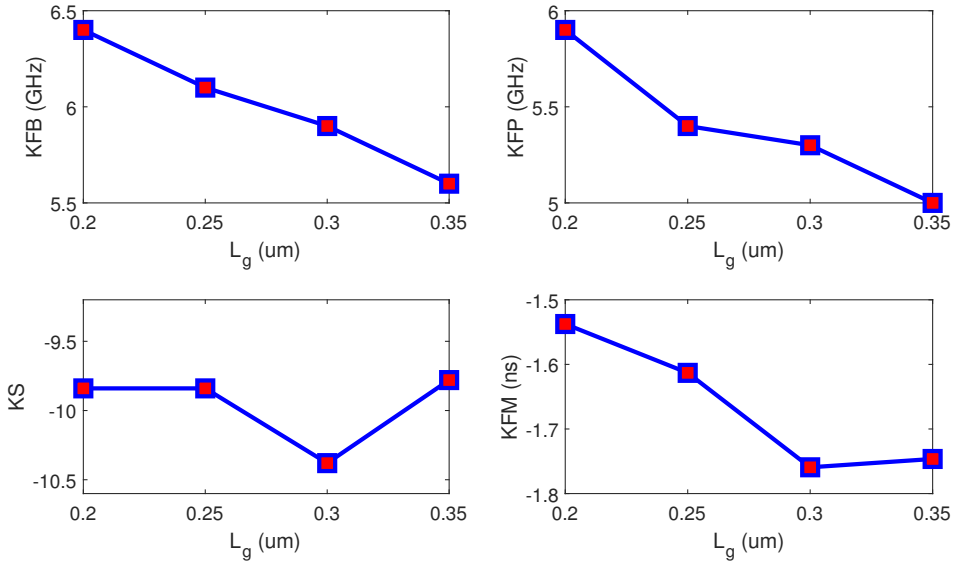
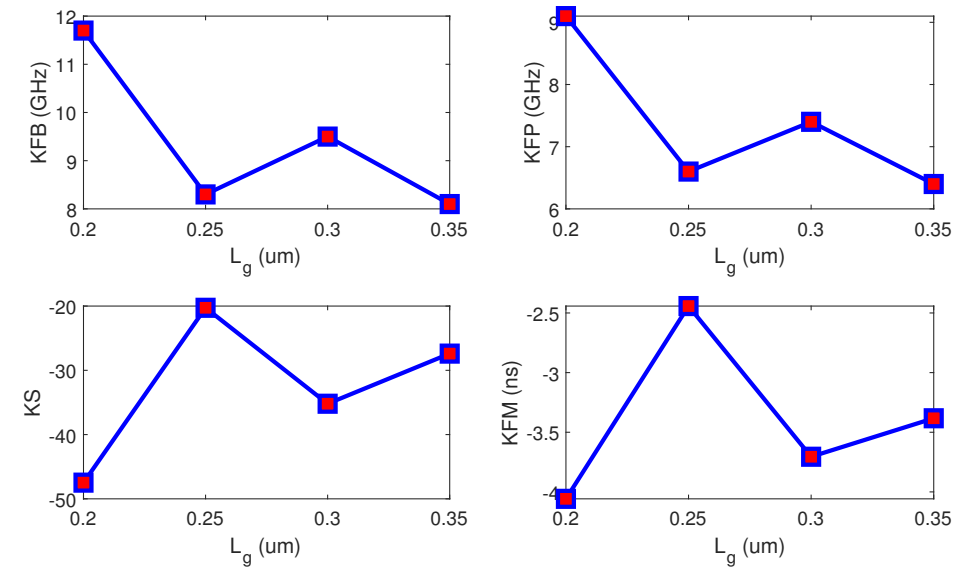


Figure 4.5: $\mathrm{Im}(S_{22})$ versus $\mathrm{Re}(S_{22})$, first, and second derivatives of $\mathrm{Im}(S_{22})$ wrt. $\mathrm{Re}(S_{22})$: The intrinsic HEMTs with different L_g values ($L_{gH} = 0.9$ μm)

The kink parameters in Fig. 4.6 for different L_g values are calculated from the D2s in Fig. 4.4 and Fig. 4.5. From Fig. 4.3a, Fig. 4.4, and Fig. 4.5 one can evaluate that KFP is moving to lower frequency points by the increase in L_g. Excluding the HEMT with 0.25 μm L_g, the increase in L_g results with the reduction in KPs of intrinsic HEMT, while there is no significant change in KS of whole HEMT. Thus, it is clear that the extrinsic parameters have major impact on KE [2, 84].



(a)



(b)

Figure 4.6: Kink parameters versus L_g ($L_{gH} = 0.9$ μm): (a) The whole HEMTs, (b) The intrinsic HEMTs.

SET1 HEMTs with 0.7 μm & 0.9 μm L_{gH} from T1 and SET2 HEMTs with 0.5 μm & 0.7 μm L_{gH} from T2 are analyzed separately; and the normalized KP results according to HEMTs with 0.7 μm L_{gH} from technology T1 and T2 are used to compare the changes in the KPs wrt. L_{gH}. Fig. 4.7 and Fig. 4.8 show the Im(S_{22}) versus Re(S_{22}), D1, and D2 from 0.5 GHz to 25.0 GHz for the intrinsic HEMTs with different L_{gH}. Fig. 4.9 illustrates the kink parameters for the intrinsic HEMTs with different L_{gH}. The actual KP values of SET1 and SET2 HEMTs, and g$_m$, C_{gd}, and C_{gs} values are shared in Table 4.1.

Table 4.1: Kink parameters, g_m @ $V_D = 28V$, C_{gd}, and C_{gs} of the intrinsic HEMTs with different L_{gH} ($L_g = 0.25$ μm)

L_{gH} (μm)	Tech.	g_m (mS)	C_{gd} (fF)	C_{gs} (pF)	KS	KFP (GHz)	KFB (GHz)	KFM (ns)
0.5	T2	153	54.7	0.78	-1.9	6.4	5.3	-0.36
0.7	T2	169	67.6	0.93	-3.43	5.8	5.6	-0.61
0.7	T1	219	96.8	1.08	-18.33	6.3	7.7	-2.38
0.9	T1	236	113.0	1.33	-20.27	6.6	8.3	-2.44

While KFP change is clear from the S_{22} data of varying L_g case, it is not clear for the varying L_{gH} case from Fig. 4.3b, Fig. 4.7, and Fig. 4.8. The kink parameters in Fig. 4.9 for different L_{gH} values are calculated from D2s in Fig. 4.7 and Fig. 4.8. The increase in L_{gH} results with increase in KFB, KS, and KFM, while there is no significant change in KFP.

The changes in L_g and L_{gH} directly affect the depletion region properties of the HEMTs. Therefore, the gate-to-drain capacitance (C_{gd}), the gate-to-source capacitance (C_{gs}), and g_m are directly affected by the gate structure. Although, C_{gs} is $\sim$10$\times$ larger than C_{gd}, the change in C_{gd} becomes critical with the change in the gate structure. Moreover, it is clear from Table 4.1 that KS can be negligible even with large gate widths unlike stated in [86, 88].

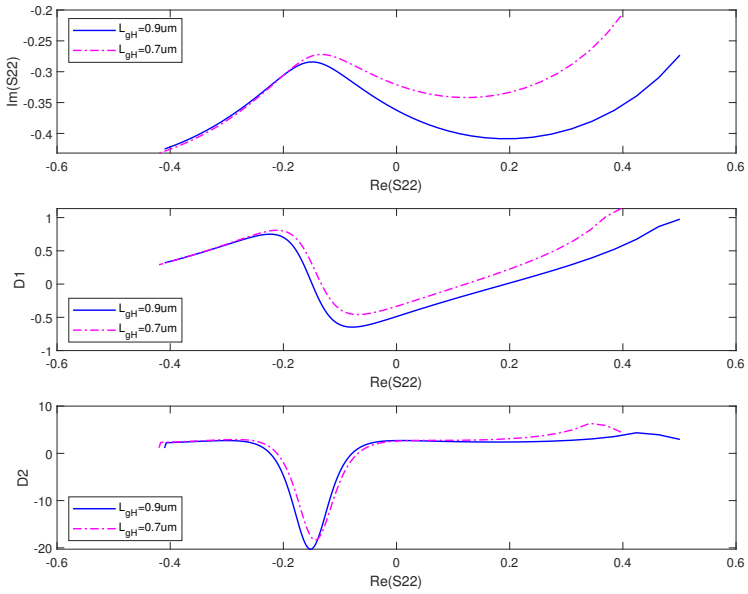


Figure 4.7: $\mathrm{Im}(S_{22})$ versus $\mathrm{Re}(S_{22})$, first, and second derivatives of $\mathrm{Im}(S_{22})$ wrt. $\mathrm{Re}(S_{22})$ for the intrinsic HEMTs with different L_{gH} values. ($L_g = 0.25$ μm): SET1 HEMTs.

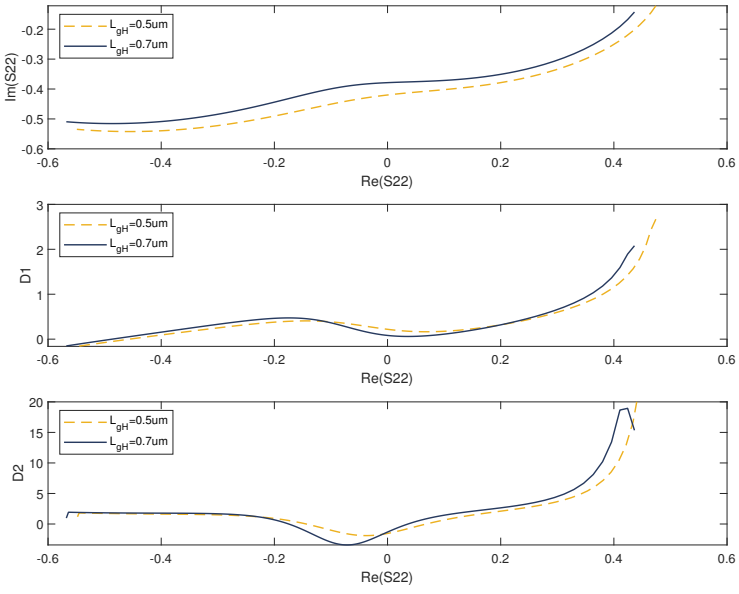


Figure 4.8: $\mathrm{Im}(S_{22})$ versus $\mathrm{Re}(S_{22})$, first, and second derivatives of $\mathrm{Im}(S_{22})$ wrt. $\mathrm{Re}(S_{22})$ for the intrinsic HEMTs with different L_{gH} values. ($L_g = 0.25$ μm): SET2 HEMTs.

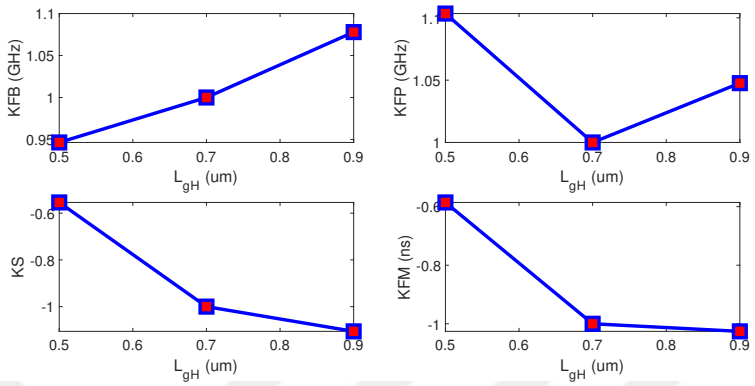


Figure 4.9: Kink parameters versus L_{gH}. ($L_g = 0.25$ μm)

Fig. 4.10 shows S_{22} results of the HEMT with $L_g = 0.25$ μm & $L_{gH} = 0.9$ μm. To investigate the effect of C_{gd}, C_{gs}, and g_m; C_{gd} & C_{gs} values are varied, and g_m is varied by excluding C_{gd} from the model. The results are compared with the whole HEMT and the intrinsic HEMT results, and the KP results are shared in Table 4.2. Since C_{gd} is related with the isolation of the HEMT, S_{12} results of those configurations are also given in Table 4.2.

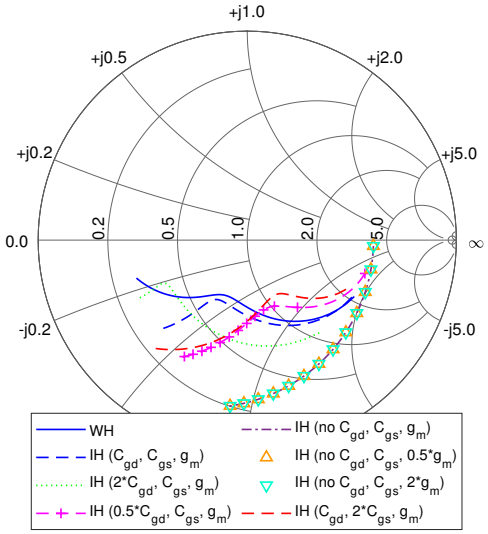


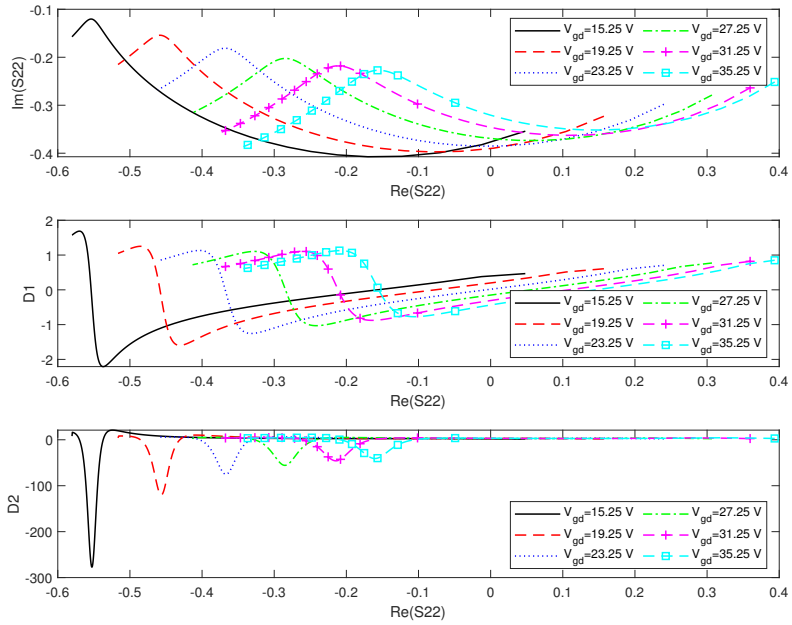
Figure 4.10: S_{22} comparison of the whole HEMT, and the intrinsic HEMT with different C_{gd}, C_{gs}, and g_m from 0.5 GHz to 25.0 GHz. ($L_g = 0.25$ μm & $L_{gH} = 0.9$ μm) (WH: Whole HEMT, IH: Intrinsic HEMT)

Table 4.2: Kink parameters of Whole HEMT (WH) and Intrinsic HEMTs (IH) ($L_g = 0.25\ \mu m$ & $L_{gH} = 0.9\ \mu m$)

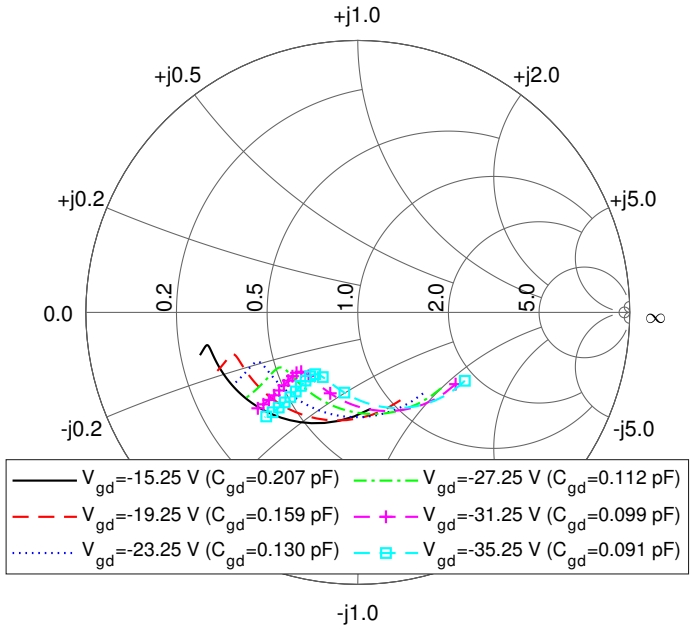
DUT	g_m	C_{gd}	C_{gs}	KS	KFP (GHz)	KFB (GHz)	KFM (ns)	$S_{12,max}$ (dB)
WH	g_m	C_{gd}	C_{gs}	-9.84	5.4	6.1	-1.61	-23.8
IH	g_m	C_{gd}	C_{gs}	-20.27	6.6	8.3	-2.44	-23.2
IH	g_m	$2{*}C_{gd}$	C_{gs}	-55.03	7.1	10.4	-5.29	-20.6
IH	g_m	$0.5{*}C_{gd}$	C_{gs}	-10.61	5.7	6.5	-1.63	-26.9
IH	g_m	C_{gd}	$2{*}C_{gs}$	-19.88	3.2	3.9	-5.09	-27.2
IH	g_m	no C_{gd}	C_{gs}	no KE				$-\infty$
IH	$0.5{*}g_m$	no C_{gd}	C_{gs}	no KE				$-\infty$
IH	$2{*}g_m$	no C_{gd}	C_{gs}	no KE				$-\infty$

The S_{12} comparison shows that the increase in C_{gd} results with lower isolation. Furthermore, the KPs are directly affected by the change in the isolation as a result of the change in C_{gd}. Although doubling C_{gs} has minor effect on KS, KFP is lowered, and KFB becomes narrow, which results with worse KFM. Excluding C_{gd} from the model eliminates the kink in S_{22} by increasing the isolation between the gate and the drain. Thus, it reveals that the limited isolation between the gate and the drain caused by the high values of C_{gd} leads to the kink in S_{22}. Since the feedback capacitance C_{gd} is a strong function of V_D, the KE can be also controlled with V_D.

A HEMT that has 10×125 μm ($W_{g,tot} = 1.25$ mm) configuration with 340 mS g_m is preferred to evaluate the effect of C_{gd} change that is caused by V_{DS} change. Thus, V_{GS} is kept constant at -3.25 V and V_{DS} is swept from 12 V to 32 V with 4 V steps. Moreover, $S-$parameter measurements are performed with 0.8 μs pulse width and 0.8% duty cycle to eliminate thermal effects. The S_{22} and KP results of the extracted intrinsic HEMT results are shared in Fig. 4.12. The results support the findings that the KE can be controlled by controlling the C_{gd}.



(a)



(b)

Figure 4.11: Intrinsic HEMT results of 10×125 μm ($W_{g,tot}$ = 1.25 mm): (a) Im(S_{22}) versus Re(S_{22}), first, and second derivatives of Im(S_{22}) wrt. Re(S_{22}) from 0.5 GHz to 25.0 GHz and (b) S_{22} results wrt. V_{gd} from 0.5 GHz to 25.0 GHz

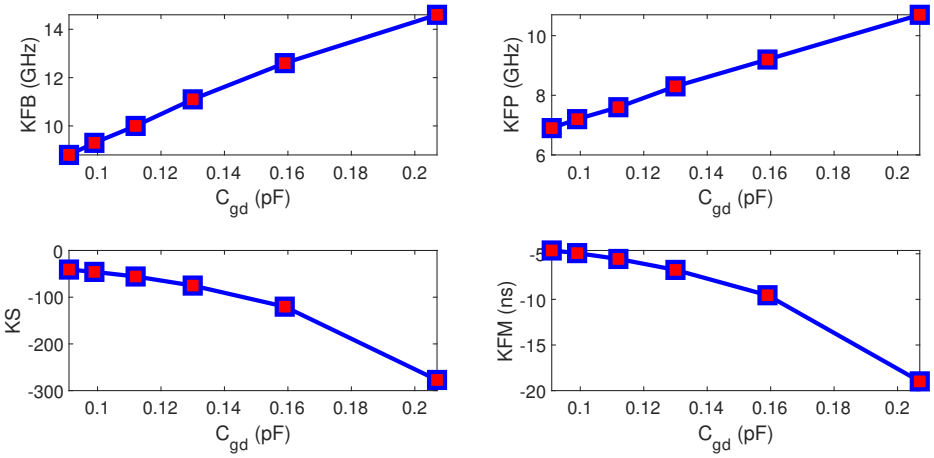


Figure 4.12: Intrinsic HEMT results of 10×125 μm ($W_{g,tot}$ = 1.25 mm): Kink parameters versus C_{gd}

The investigation of the effect of the gate structure on the kink in S_{22} with the transistors that have different L_g and L_{gH} configurations reveals important parameters to control KE. The kink effect can be controlled to develop a broadband amplifier with the selection of the proper gate structure and the proper bias point.

Chapter 5

Broadband LNA Design

This chapter represents an air cavity *quad-flat no-leads* (QFN) over-molded plastic packaged cascode broadband GaN LNA MMIC with resistive feedback, which is capable of more than 86:1 operation bandwidth. The LNA has a flat -3 dB gain bandwidth from 30 MHz to 2.6 GHz with low power consumption. 1.5 dB noise figure (NF) performance is achieved with a transistor that has a relatively higher minimum noise figure (NF_{min}) in comparison to [42].

The proposed LNA is developed mainly for portable and mobile radios operating at different frequency ranges, L-band and S-band radar applications. Moreover, the properties of this GaN LNA MMIC make it desirable for many other radio communications, electronic warfare, and commercial and military radar applications.

The gate structure is configured with L_g =0.25 μm and L_{gH} =0.7 μm to improve the S_{22} for broadband operations. Furthermore, to determine the bias conditions, the results given in Fig. 4.12 are taken into account besides the noise considerations.

The topology selection, the model of the cascode transistor, GaN LNA MMIC design, and measured performance of the QFN packaged LNA MMIC are discussed in the following sections.

5.1 Topology Selection

There are three commonly used LNA topologies as presented in Fig. 5.1. Those topologies are called as *common-source* (CS), *common-gate* (CG), and *cascode*. The performance comparison of those topologies are provided in Table 5.1 [61, 109].

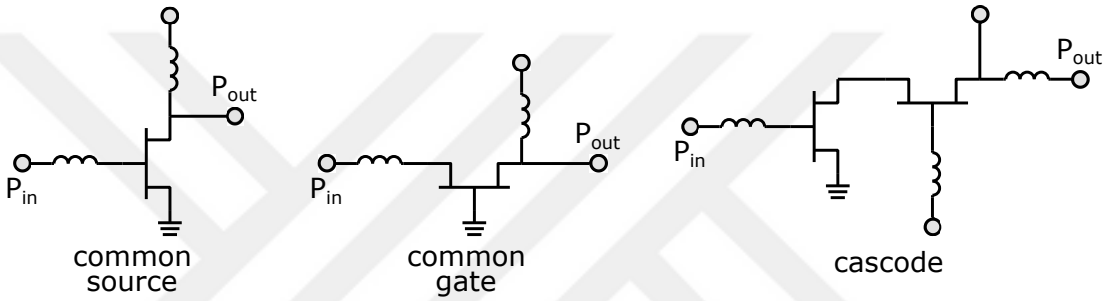


Figure 5.1: Representation of LNA topologies

Table 5.1: The performance comparison of the LNA topologies.

Parameter	CS	CG	Cascode
NF	Lowest	Rises rapidly with the increasing frequency	Slightly higher than the CS configuration
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially highest
Bandwidth	Narrow	Fairly broad	Broad
Stability	Requires compensation	High	Higher
Reverse Isolation	Low	High	High
Sensitivity*	High	Low	Low

*Sensitivity covers the temperature changes, the bias point variations, the process variations, and the tolerance of the components.

CS topology is the most promising topology for the lowest *NF*, while CG topology is a good solution for narrowband low noise applications, since the NF of the CG transistor increases rapidly with the frequency. On the other hand, the cascode transistor is the best candidate for the broadband applications that requires high linearity and low sensitivity. The cascode transistor has slightly higher *NF* according to CS transistor, but it has less sensitivity to process variations, temperature changes, and bias changes.

To minimize the efforts to get a good noise and input match simultaneously, an inductive feedback is introduced between the source and the ground of the

CS transistor as presented in Fig. 5.2a [110]. Implementation of the source degeneration inductance (L_S) also improves the linearity and the stability of the transistor with a gain expense [109].

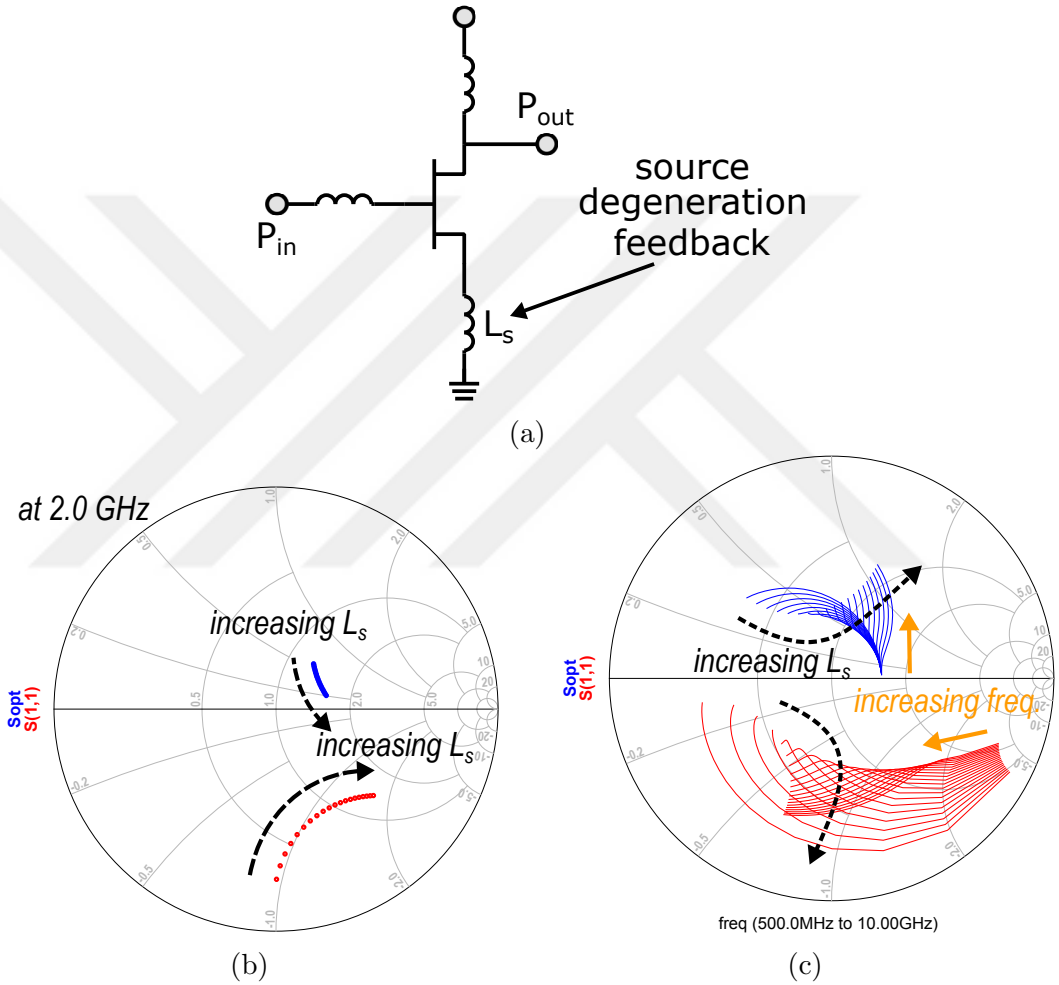
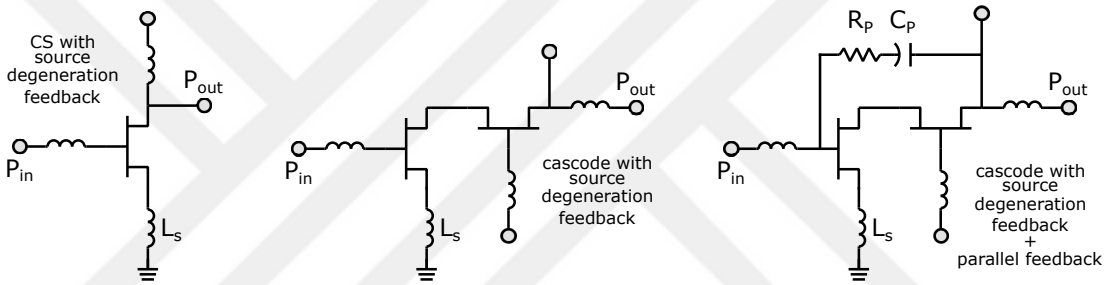


Figure 5.2: (a) CS transistor with inductive source degeneration feedback, the effect of the source degeneration feedback on CS configuration (b) at 2.0 GHz, and (c) from 0.5 GHz to 10.0 GHz

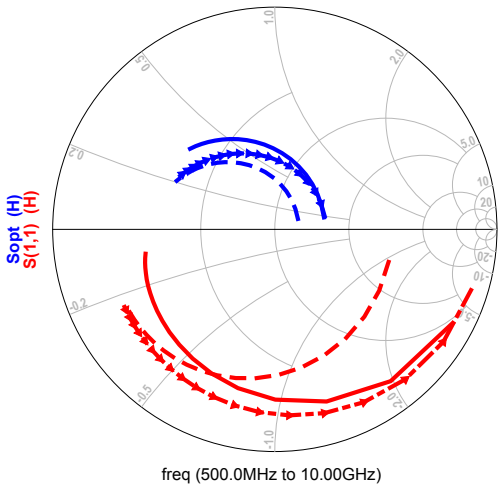
The cascaded combination of the CS transistor and the CG transistor results with the cascode configuration. The cascode transistor combines the features of the CS and CG transistors to reach better bandwidth with higher stability and linearity. To achieve the lowest possible *NF*, a LNA has to be designed with a single cascode transistor [111].

The cascode transistor can be configured with inductive source degeneration

at the CS transistor. The source degeneration technique reduces the gain. To compensate the gain reduction and to obtain a broadband matching a parallel feedback can be added from the drain of the CG transistor to the gate of the CS transistor. The effect of the CS transistor with source degeneration feedback, the cascode transistor with source degeneration feedback, and the cascode transistor with source degeneration feedback and parallel feedback on S_{opt} and S_{11} are presented in Fig. 5.3. It is clear from Fig. 5.3 that the cascode transistor with both feedback gives a simpler matching solution.



(a)



(b)

Figure 5.3: (a) The representation of the topologies with the feedbacks,(b) S_{11} and S_{opt} of CS HEMT with source degeneration (solid lines), Cascode HEMT with source degeneration (dashed lines), and Cascode HEMT with source degeneration + resistive feedback (dashed lines with arrows)

5.2 Cascode HEMT Development

The cascode HEMT, which is used to develop the GaN LNA MMIC, has not been fabricated previously and the model of the cascode HEMT is developed from the CS HEMT measurement provided in section 3.2. The cascode HEMT cell in Fig. 5.4d is configured by cascading a CS HEMT and a common-gate (CG) HEMT as in Fig. 5.4b. The peripheries and the bias conditions of the CS HEMT and the CG HEMT may be different. The concept cascode HEMT in Fig. 5.4d is based on the CS HEMT in Fig. 5.4c; therefore, both CS HEMT and CG HEMT have the same periphery and the same bias conditions.

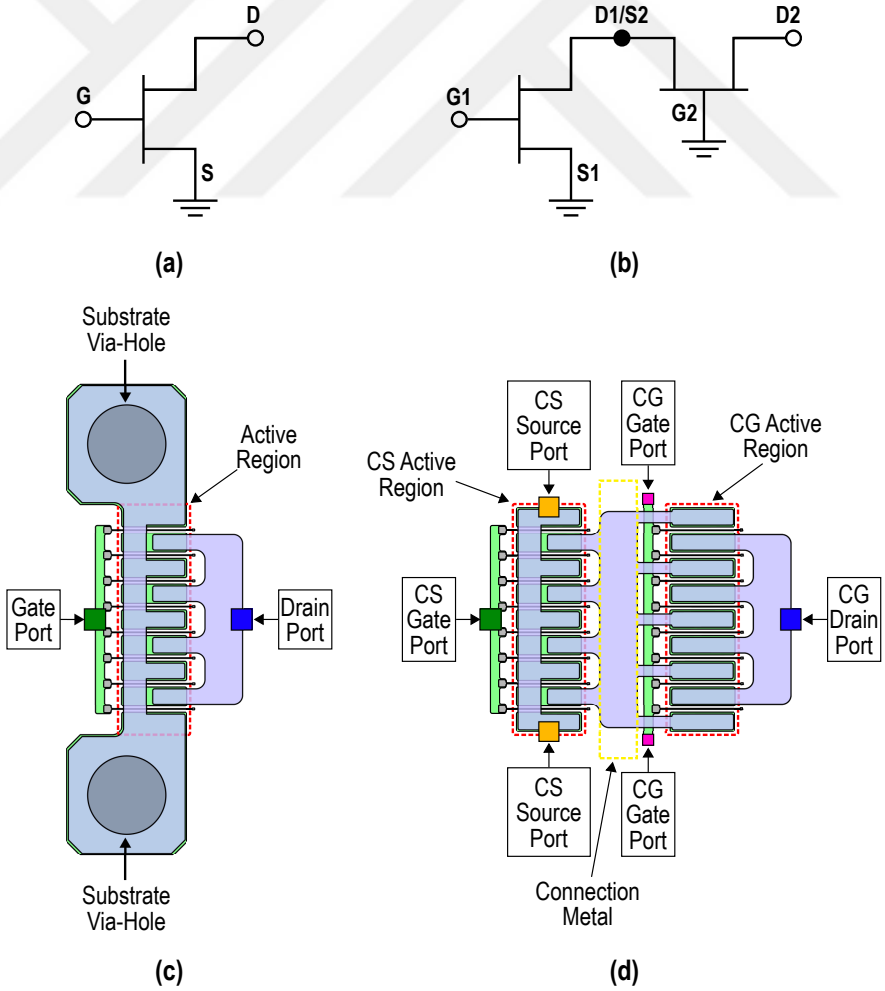


Figure 5.4: (a) CS configuration, (b) Cascode configuration, (c) layout of the CS cell, and (d) layout of the concept cascode cell.

The cascode HEMT equivalent circuit model, given in Fig. 5.5, is developed by the extracted optimum model parameters of the CS HEMT given in Table 3.5. Sub-indices 's' and 'g', in the model, represent the CS HEMT and the CG HEMT parameters, respectively. R_{cm}, L_{cm}, and C_{cm} are related with the connection metal between the CS HEMT and the CG HEMT. The connection metal can be modeled with Electromagnetic (EM) simulations for better accuracy, or simply $R_{cm} = R_S + R_D$, $L_{cm} \approx L_D$, and $C_{cm} = C_{pd}$ values can be used to get a fast output. The same circuit parameters are used for the CG HEMT as the CG HEMT is biased at the same bias conditions as the CS HEMT.

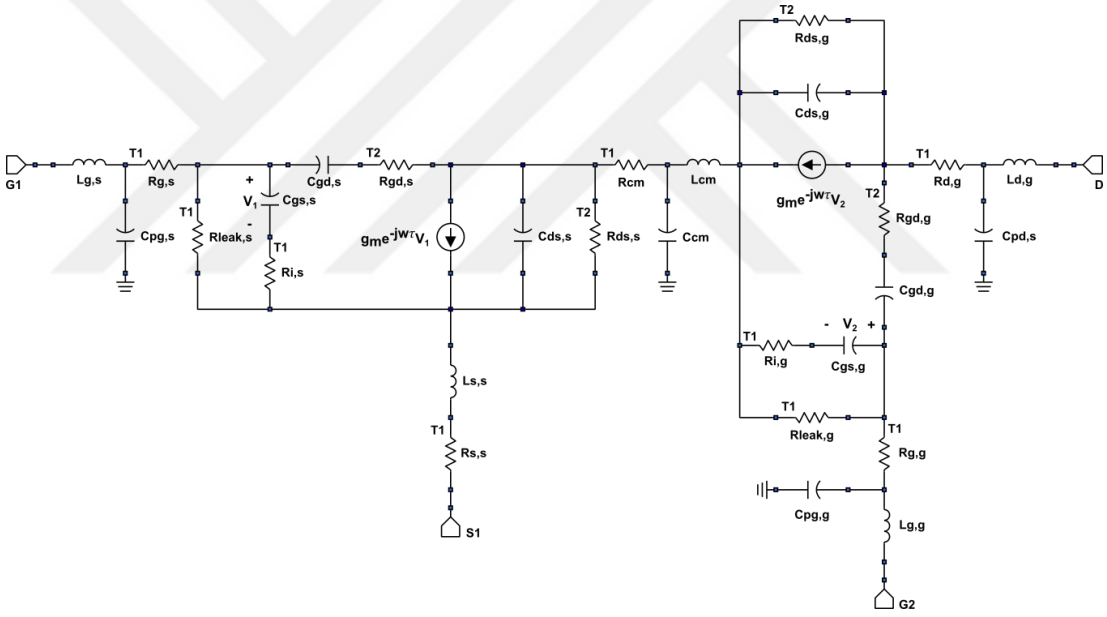
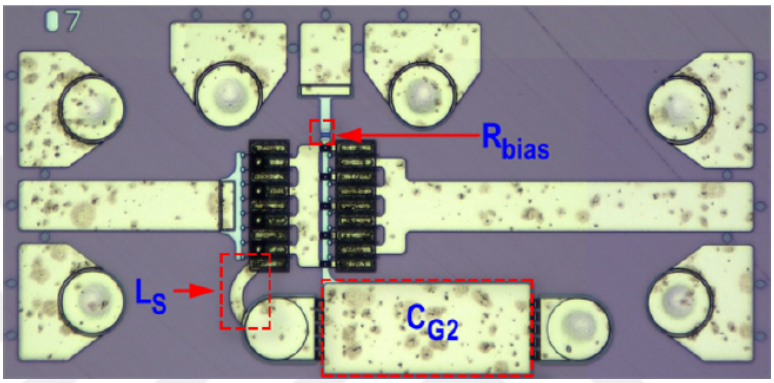


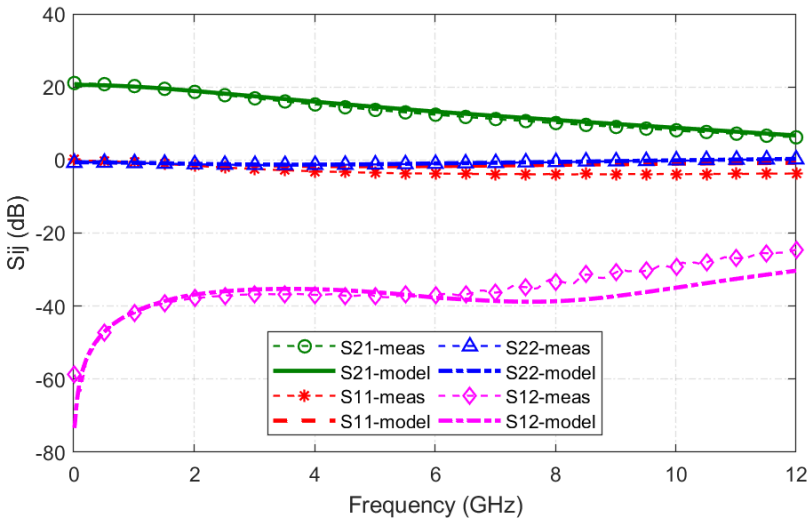
Figure 5.5: Equivalent circuit model of the cascode HEMT

To characterize the cascode HEMT properly, a biasing resistor (R_{bias}) and a capacitor (C_{G2}) are added to the gate of the CG HEMT. Moreover, a source degeneration inductor (L_S) is also added to the CS HEMT to replicate the cascode HEMT used in the MMIC design. Fig. 5.6a shows the fabricated cascode HEMT; and R_{bias}, C_{G2}, and L_S are also indicated on the figure.

The comparison of the model and the measurement results of the cascode HEMT are given in Fig. 5.6b. The results validate that the cascode HEMT model based on the CS HEMT model can be used to predict the cascode HEMT results with close correlation even without fabricating the cascode HEMT.



(a)



(b)

Figure 5.6: (a) Microphotograph of the cascode HEMT and (b) Small-signal results comparison of the model and the measurements

5.3 Broadband GaN LNA MMIC

The cascode configuration is useful to design a wideband LNA because it has high gain and high output resistance [112]. Therefore, cascode amplifier topology is used to obtain an LNA that has a wide operation bandwidth.

The design of the proposed LNA requires multiple steps as depicted in Fig. 5.7. Each design step requires different approaches and different simulation environments. The MMIC and the application board are designed in Keysight ADS design environment and 3D EM simulations are performed on the packaged LNA MMIC integrated application board.

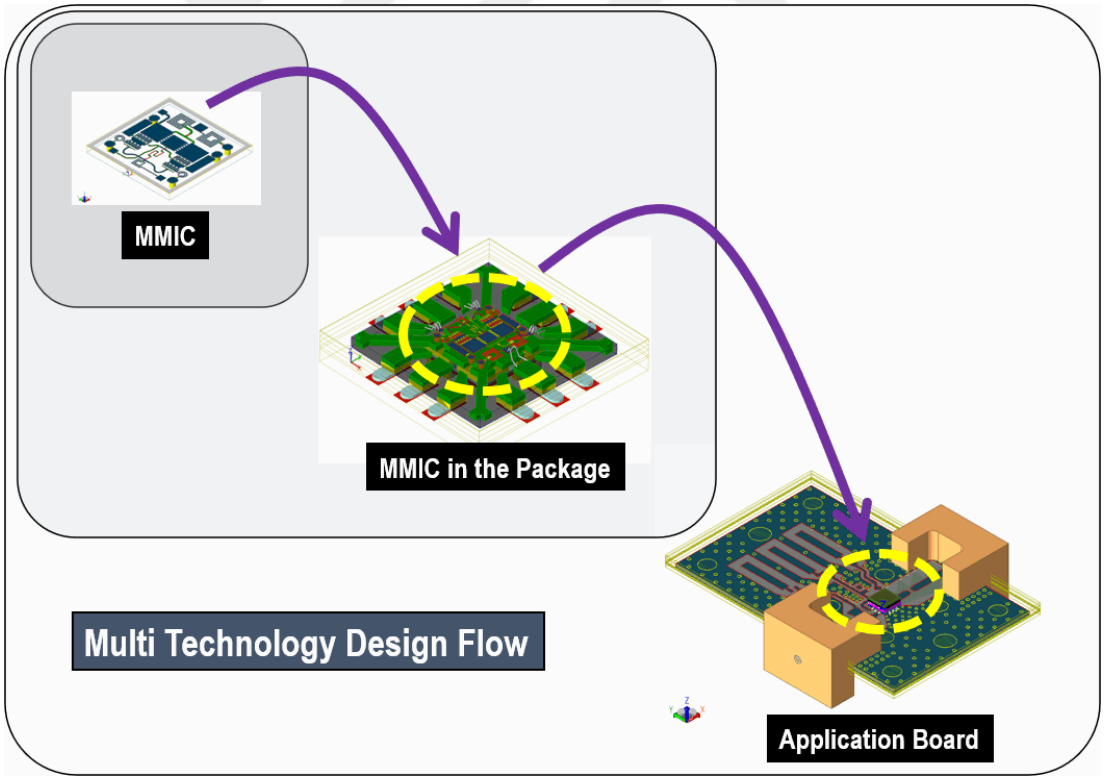


Figure 5.7: Multi technology design flow

To design the proposed MMIC LNA, a conceptual cascode HEMT, which was not fabricated before, is modeled, and the developed model is used. Negative feedback was preferred to get a broadband matching. Negative feedback has the tendency to reduce the gain and minimize the input impedance. To improve

the input and the output return losses and to get a flat gain response, a parallel feedback with ∼1.1 kΩ resistor and 15 pF capacitor is introduced from the output to the input as shown in Fig. 5.10. No additional optimization is performed to improve the 1-dB compression (P_{1dB}) point and the Output Third-Order Intercept Point ($OIP3$).

Since the LNA covers frequencies from 30 MHz to 2.6 GHz, a couple of additional components, which cannot be realized on-chip, are used on the application board. Fig. 5.10 shows the simplified schematic of the complete LNA with the application board. The gain of the LNA is kept below 13 dB by the addition of an internal attenuator that will reduce the linearity figure-of-merit ($LFOM$), output power, and the linearity of the LNA. The $LFOM$ is defined as $LFOM = OIP3/P_{DC}$.

To achieve a first-pass design success, full 3D EM simulations of the packaged LNA with the application board is performed and the final optimizations are performed. Fig. 5.12b shows the simulation results of the complete design based on the conceptual transistor model. The design achieved an average NF of ∼1.4 dB, ∼11.5 dB gain with 1.5 dB ripple, better than 10 dB input and output return losses, and better than 35 dB isolation with unconditional stability, where K-factor is >1 and source & load stability circles are always out of the smith-chart.

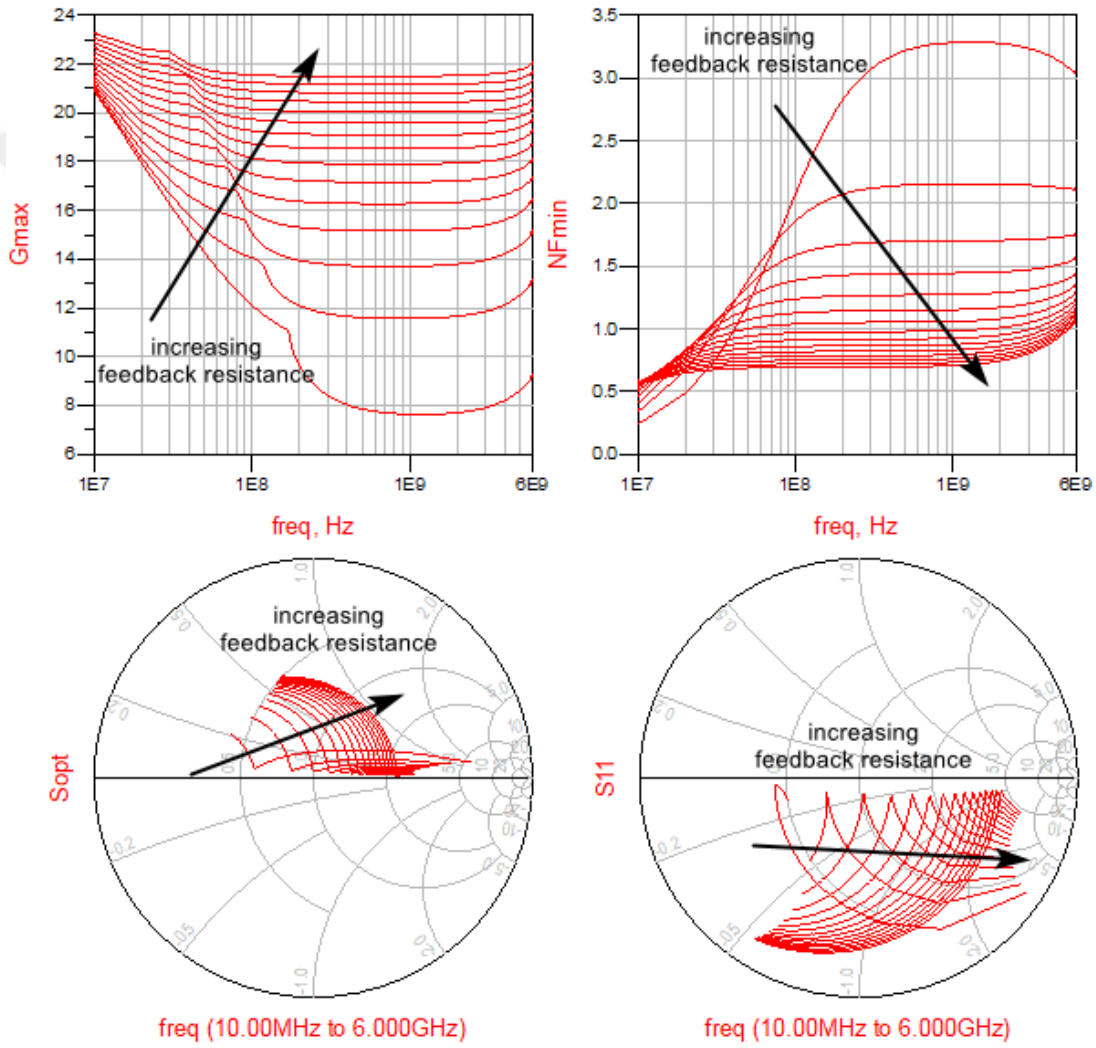


Figure 5.8: The performance change of the cascode HEMT with sweeping feedback resistance value from 100 Ω to 1500 Ω with 100 Ω steps ($C_{fb} = 15pF$). The simulations performed from 10.0 MHz to 6.0 GHz.

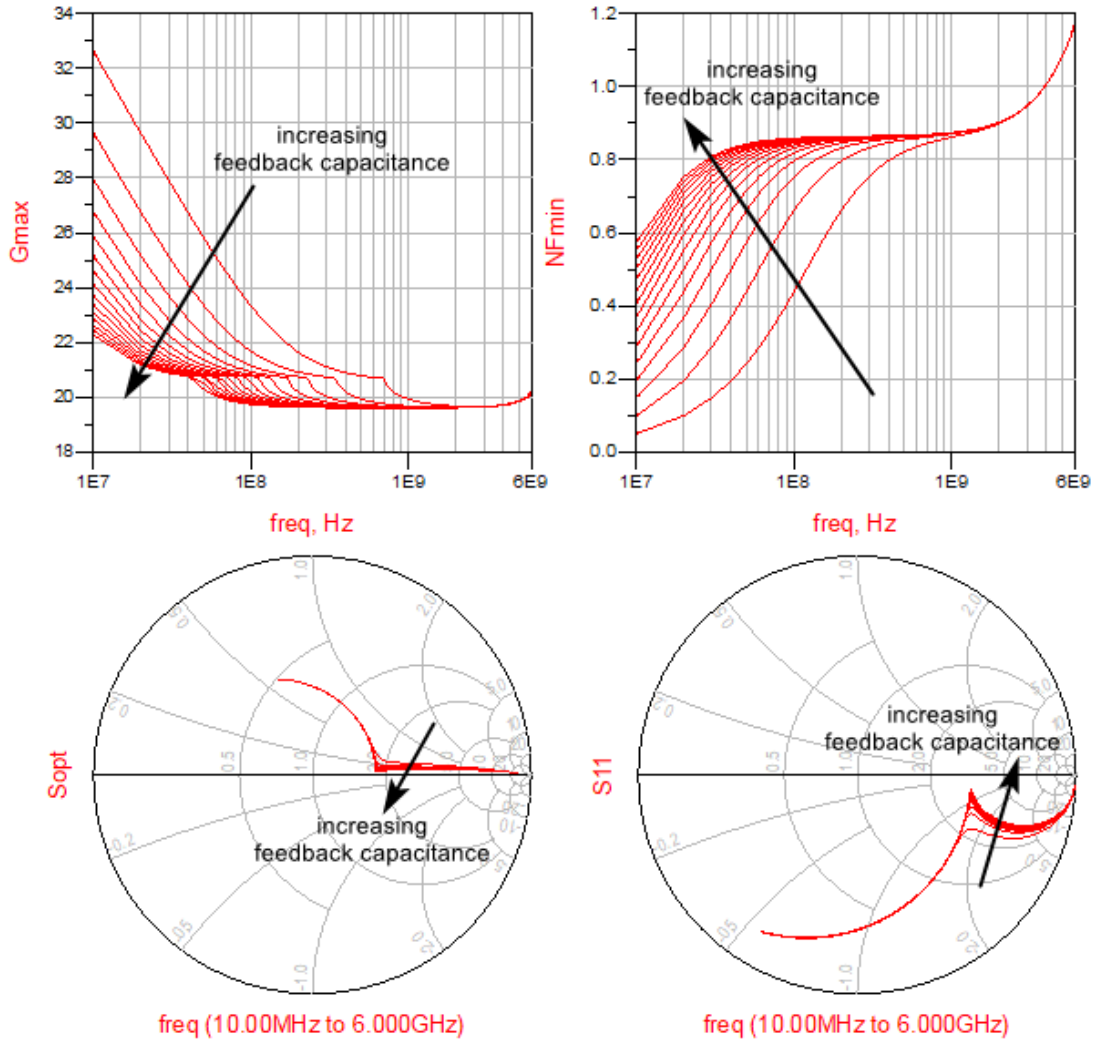


Figure 5.9: The performance change of the cascode HEMT with sweeping feedback capacitance value from 1 pF to 15 pF with 1 pF steps ($R_{fb} = 1000\Omega$). The simulations performed from 10.0 MHz to 6.0 GHz.

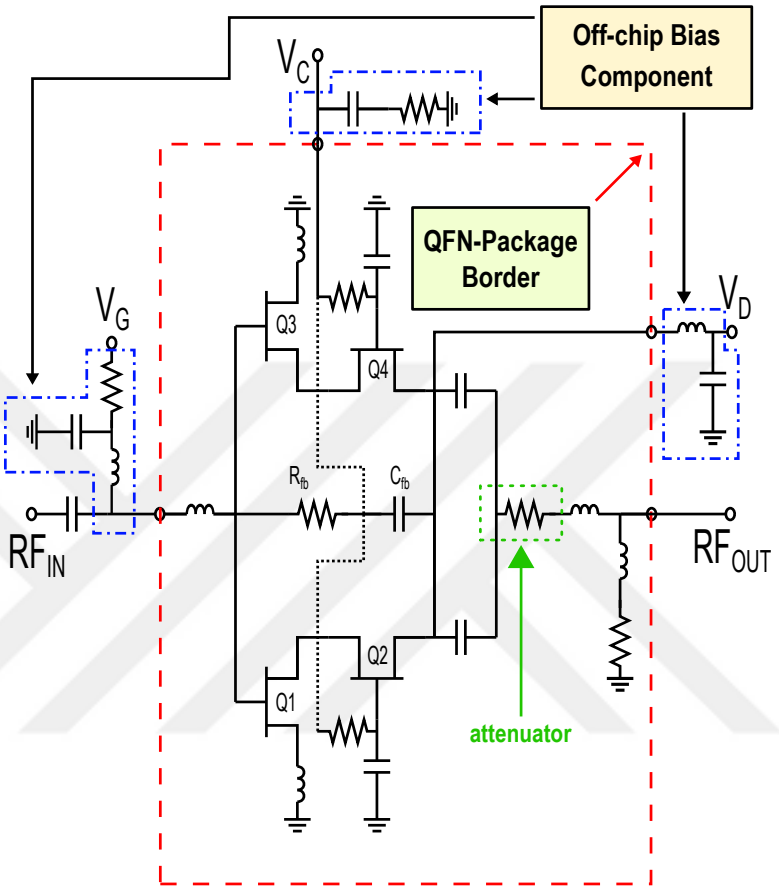
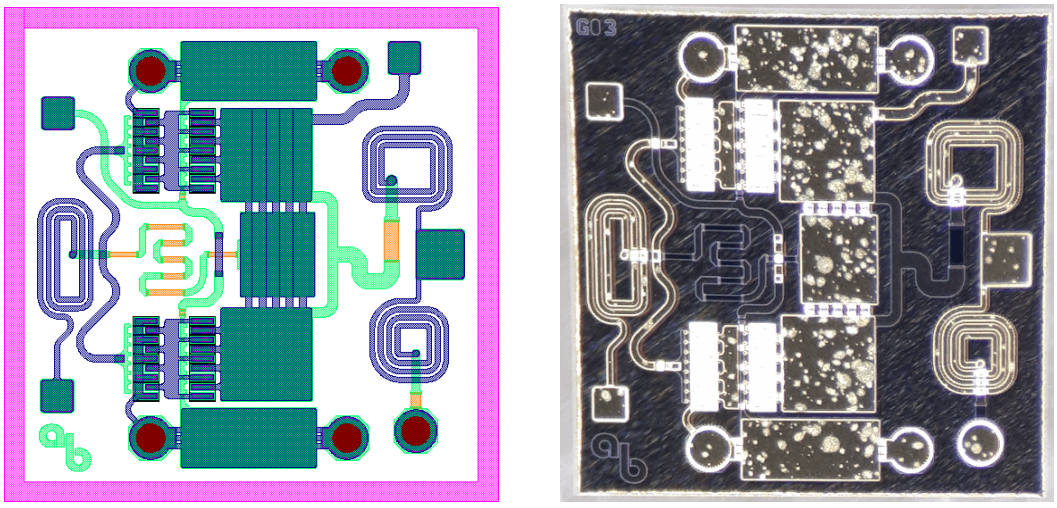


Figure 5.10: The schematic of the GaN LNA MMIC.



(a) (b)

Figure 5.11: (a) GaN LNA MMIC production ready layout and (b) the microphotograph of the fabricated GaN LNA MMIC.

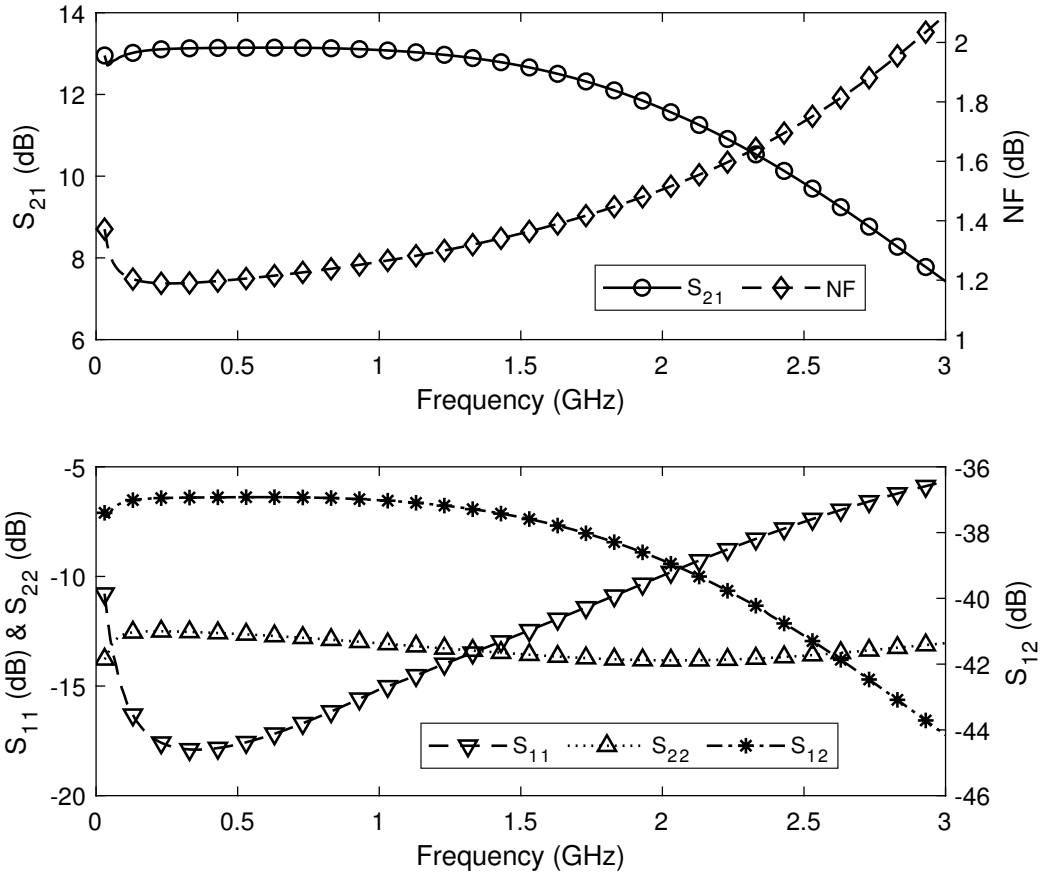


Figure 5.12: The simulation results of the GaN LNA MMIC with the QFN package and the application board.

5.3.1 GaN LNA MMIC Packaging and Application Board Design

The proposed LNA can operate from 30 MHz to 2.6 GHz. To support the ease of operation, a low-cost 12 lead 3×3 mm^2 air cavity QFN over-molded plastic package is preferred and modeled for the design flow as presented in Fig. 5.13. As Fig. 5.10 and Fig. 5.16a show, no additional components are used in the package besides the GaN LNA MMIC. The gold bond-wires with 25 μm diameter are used to connect the pins of the MMIC LNA to the package. The drawing of the bond-wires used for 3D EM simulations are shown in Fig. 5.14.

The packaged LNA is mounted on a PCB that has a thermal ground for the LNA, and a couple of circuit elements are mounted on the application board for biasing the LNA. The additional components are the off-chip biasing inductors, the capacitors, and the resistors can be seen on the schematic given in Fig. 5.10.

After developing the model of the QFN package and the model of the bond-wires, 3D EM simulations of the complete circuit performed on the 3D model of the complete circuit shown in Fig. 5.15. The simulation result given in Fig. 5.12 belongs to the 3D EM simulation of the complete circuit in Fig. 5.15 integrated with the developed noise model.

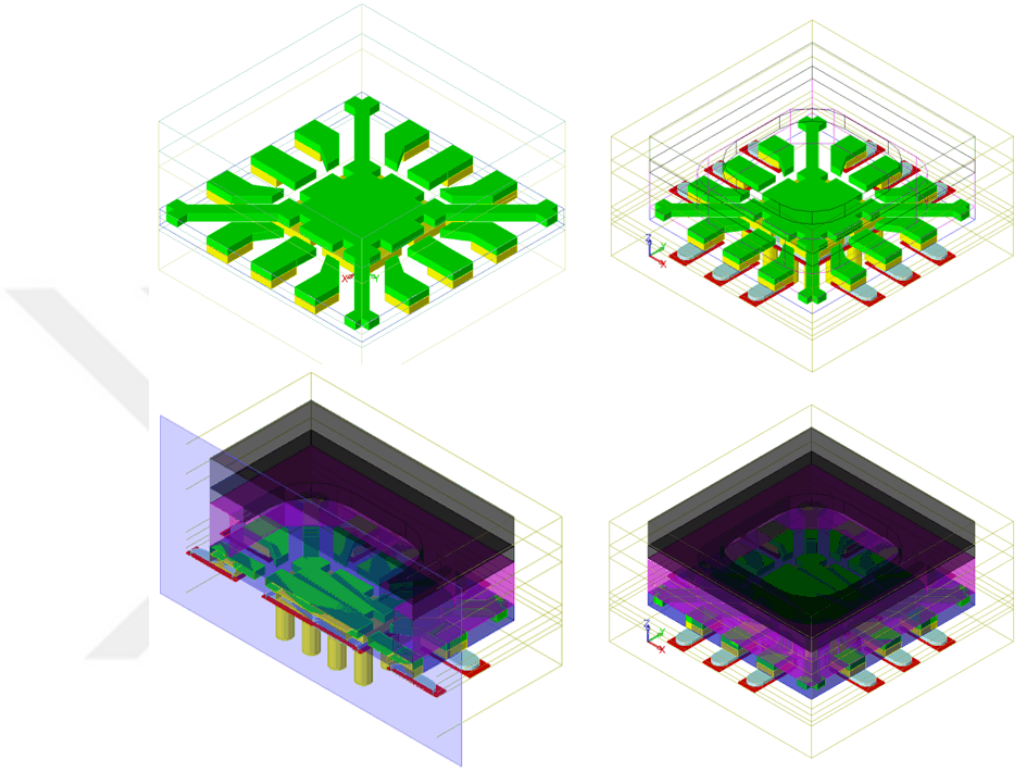


Figure 5.13: 3D drawing of the QFN package integrated in the simulation environment.

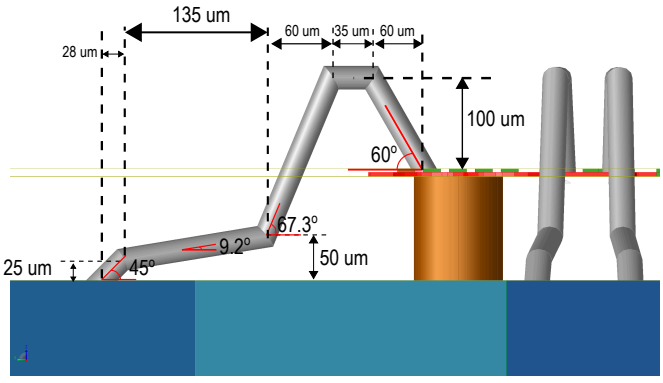


Figure 5.14: 3D drawing of the wire bonds used in the design

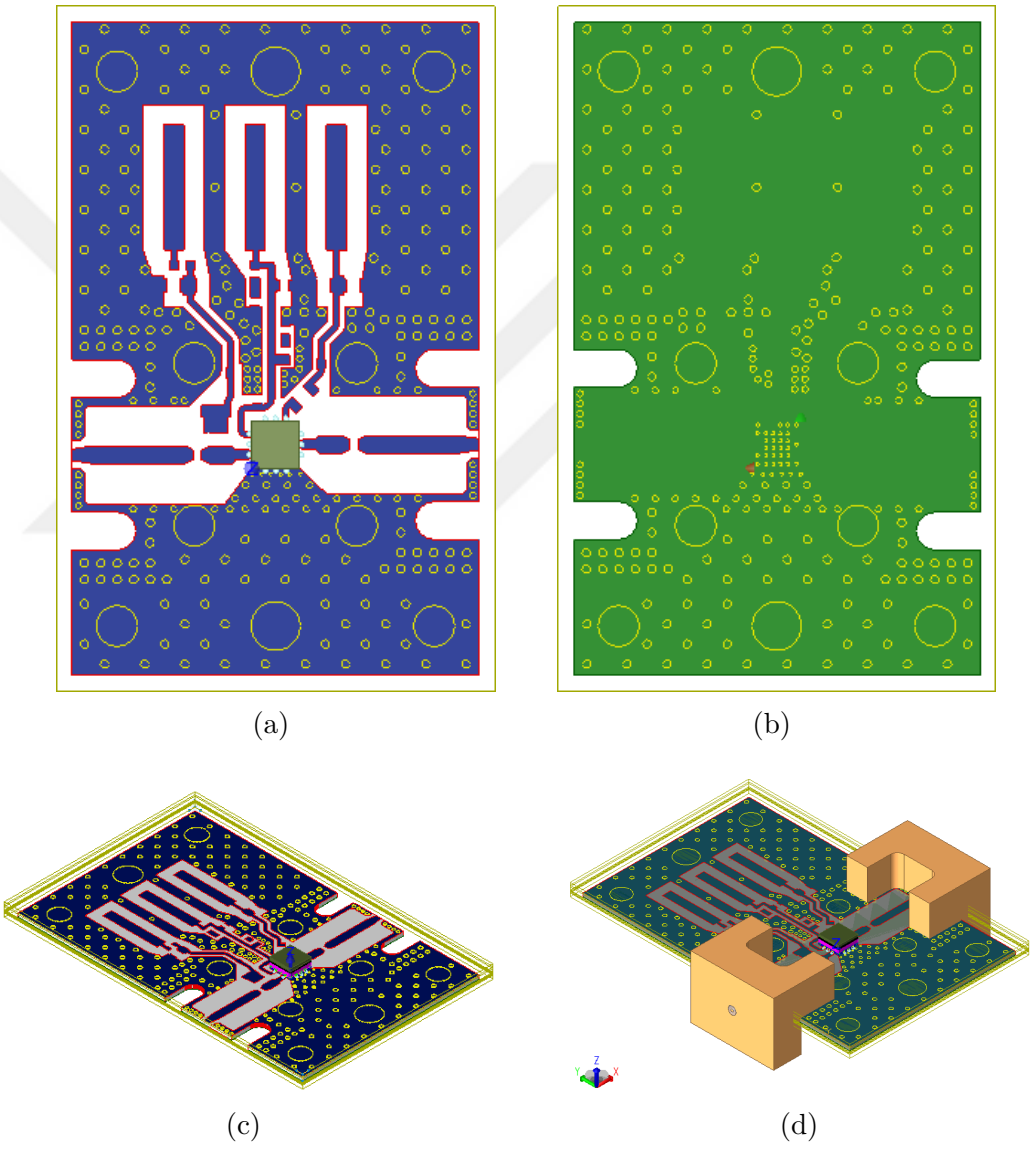
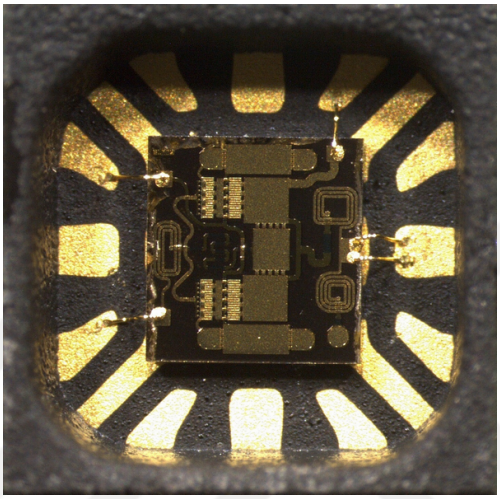
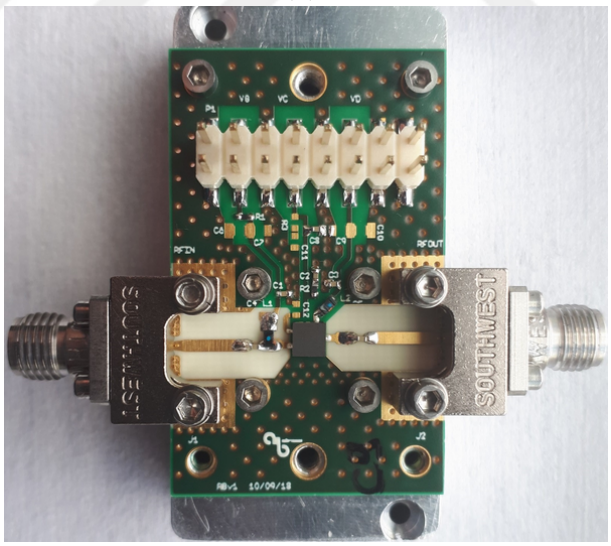


Figure 5.15: The application board used in the simulations: (a)the top view, (b) the bottom view, (c) the 3D view, and (d) the 3D view with the SMA connectors.

Fig. 5.16 presents the packaged LNA prepared for measurements under 50 Ω environment by mounting SMA connectors to the board. No additional cooling elements are employed other than the metal carrier of the application module.



(a)



(b)

Figure 5.16: Images of the GaN LNA MMIC and the application board (MMIC Die size: 1.35 × 1.35 mm^2): (a) LNA MMIC bonded into a 12-lead plastic QFN package, (b) Packaged LNA MMIC on an application board

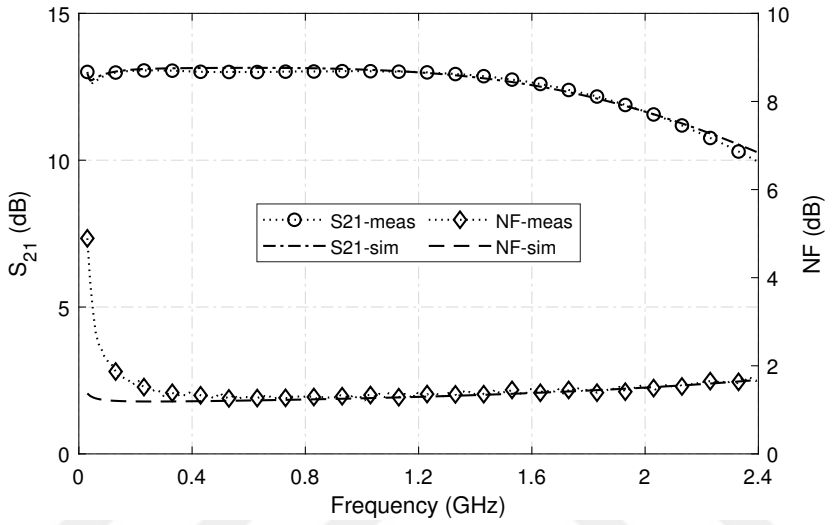
5.4 GaN LNA MMIC Characterisation Results

The operation range of the LNA requires some external components that can be mounted on the application board. Therefore, all the measurements of the module performed at the coaxial connector reference plane and no de-embedding is performed.

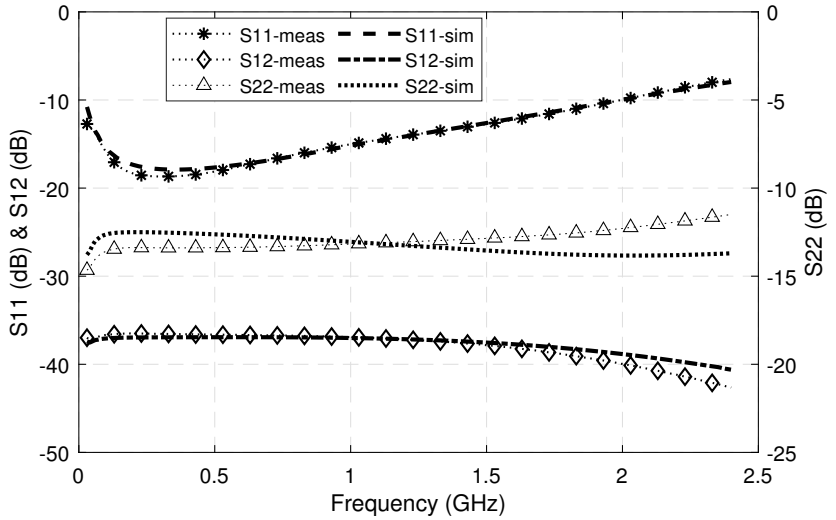
5.4.1 Small-Signal and Noise Figure Measurements

Small-signal and *NF* measurements are performed with a PNA-X at the same time, and the results are presented in Fig. 5.18a. Although there is a performance change in CS HEMT, the simulation and the measurement results are in good agreement. It was observed that the LNA has ∼1.4 dB *NF* with a minimum of 1.25 dB. Moreover, an average of 11.5 dB gain, better than 10 dB input and output matching, and better than 35 dB isolation with stable operation were realized from 30 MHz to 2.4 GHz. As shown in Fig. 5.18, by increasing the drain voltage (V_D) from 12 V to 24 V, the operation band extended to 2.6 GHz with ∼0.25 dB increase in *NF* without compromising from input and output return losses, and isolation.

Fig. 5.19a and Fig. 5.19b present gain and *NF* performance versus different power dissipation level, respectively. V_D and drain current (I_D) sweep were performed to investigate the performance change. As Fig. 5.19a shows, less than 3 dB *NF* is achieved in the worst case with a minimal gain change. Increasing the current beyond 100 mA results in a decrease in gain after 24 V V_D with a steep increase in *NF*.

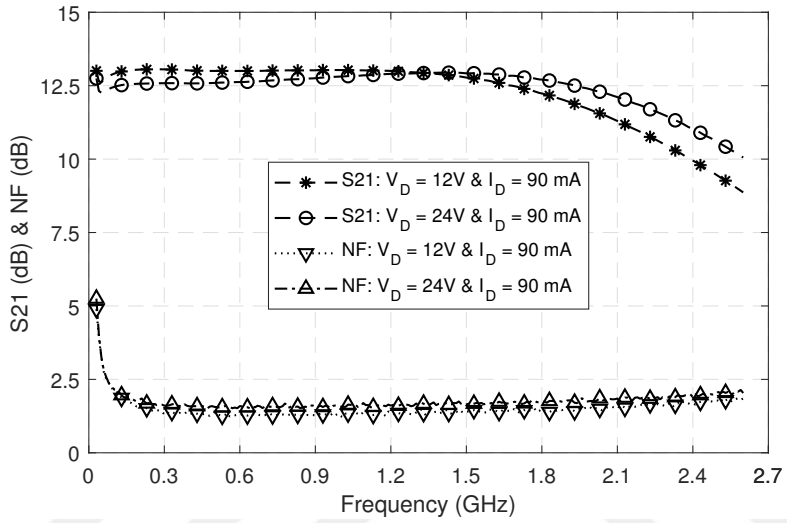


(a)

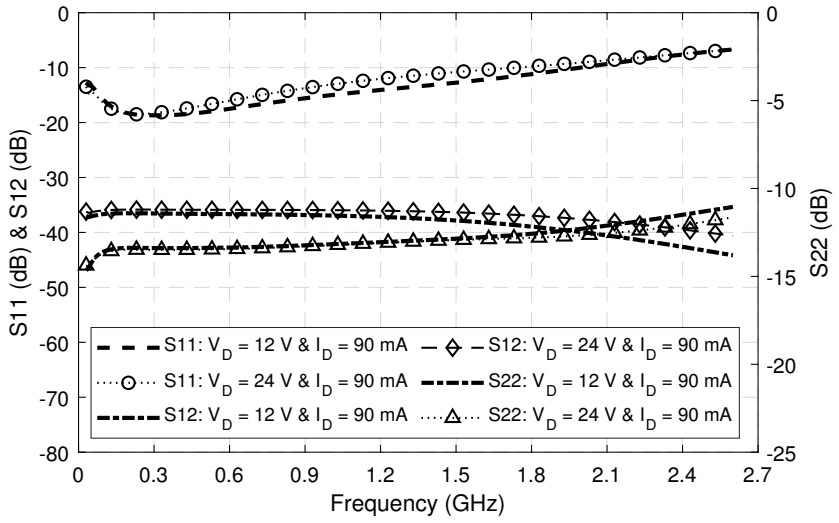


(b)

Figure 5.17: Mounted GaN LNA MMIC Small-Signal and *NF* measurement vs. simulation results (Bias Conditions: V_D=12 V & I_D=90 mA): (a) S_{21} and *NF*, (b) S_{11}, S_{22} and S_{12}

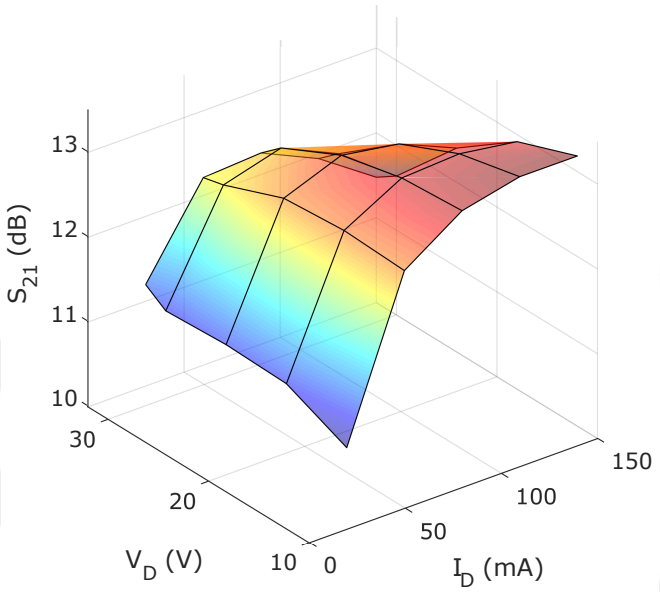


(a)

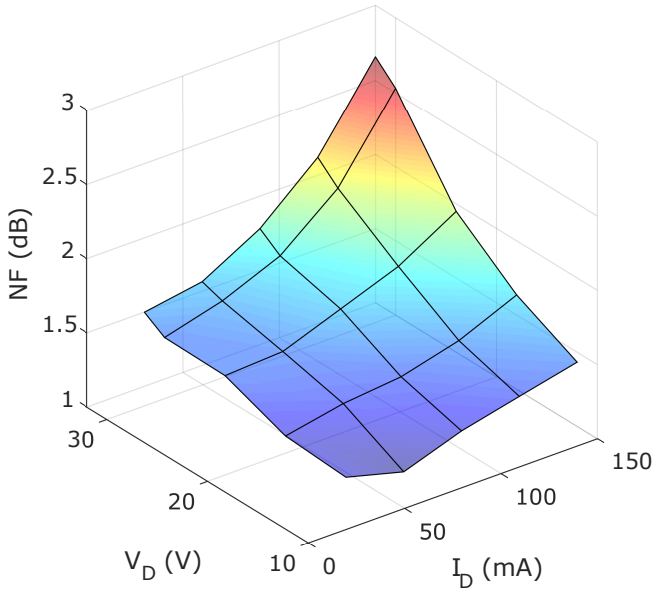


(b)

Figure 5.18: Mounted GaN LNA MMIC Small-Signal and *NF* measurement vs. V_D: (a) S_{21} and *NF*, (b) S_{11}, S_{22} and S_{12}



(a)



(b)

Figure 5.19: Mounted GaN LNA MMIC *NF* and Small-Signal Gain performance vs. power dissipation: (a) Small-Signal Gain at 1 GHz vs. Power Dissipation, (b) *NF* at 1 GHz vs. Power Dissipation.

5.4.2 Output Power and Input Survivability Measurements

As it is explained in the design section that an internal attenuator, which affects the P_{1dB} performance of the LNA, is introduced to the design. Since the total attenuation implemented in the design is ∼5 dB, it is expected to get 5 dB worse P_{1dB} level. Fig. 5.20 gives the P_{1dB} results at 1.0 GHz with the internal attenuator. Therefore, the LNA can support 21 dBm at 1-dB compression point with the internal attenuator. Moreover, the input survivability is tested up to 17 dBm input power and no performance degradation is observed.

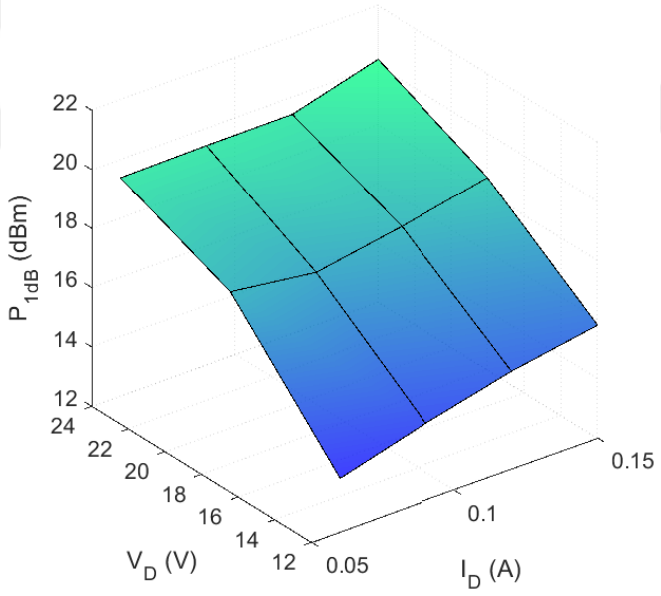


Figure 5.20: Mounted GaN LNA MMIC P_{1dB} vs P_{DC} measurement results at 1.0 GHz

5.4.3 Two-Tone Linearity Characterization

Two-tone linearity measurements have been performed with 1 MHz tone spacing with the application board under 50 Ω environment. *OIP3* measurements at 1.0 GHz for different power dissipation levels are given in Fig. 5.21. The *OIP3* performance of the LNA is lowered by the amount of the attenuation introduced by the internal attenuator [54]. Thus, the GaN LNA MMIC can support 27 dBm *OIP3* with the internal attenuator.

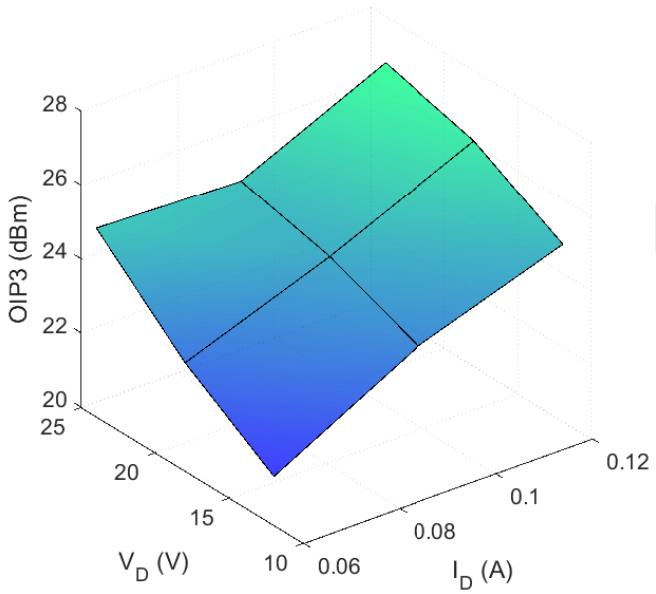


Figure 5.21: Mounted GaN LNA MMIC $OIP3$ vs P_{DC} measurement results at 1.0 GHz

Third-order intercept product (OIP3) is calculated with Eq. (5.1) and Eq. (5.2). Equation (5.1) can be expanded into Eq. (5.3b) by replacing ΔP with Eq. (5.2) in Eq. (5.1) where P_{OUT} is the output signal at the first-order and P_{OUT_3} is the output signal at the third-order. If there is an attenuator at the output of the LNA, Eq. (5.1) transforms into Eq. (5.4c) where P'_{OUT} is the output signal at the first-order before the attenuator, P'_{OUT_3} is the output signal at the third-order before the attenuator, and Attn. is the attenuation level. Therefore, additional attenuation at the output decreases the OIP3 by the amount of the attenuation.

$$OIP3 = P_{OUT} + \frac{\Delta P}{2} \tag{5.1}$$

$$\Delta P = P_{OUT} - P_{OUT\_3} \tag{5.2}$$

$$OIP3 = P_{OUT} + \frac{P_{OUT} - P_{OUT\_3}}{2} \tag{5.3a}$$

$$= \frac{3 \times P_{OUT} - P_{OUT\_3}}{2} \tag{5.3b}$$

$$OIP3 = \frac{3 \times (P'_{OUT} - Attn.) - (P'_{OUT\_3} - Attn.)}{2} \tag{5.4a}$$

$$= \frac{2P'_{OUT} - 2Attn. + (P'_{OUT} - P'_{OUT\_3})}{2} \tag{5.4b}$$

$$= P'_{OUT} + \frac{\Delta P}{2} - Attn. \tag{5.4c}$$

P_{1dB} and linearity measurements show the effect of the attenuation. Therefore, P_{1dB} and *OIP3* levels are decreased by the level of attenuation. Regarding this performance degradation, the performance of the QFN packaged LNA is compared with the state-of-the-art LNAs in Table 5.2.

Table 5.2: Performance Summary and Comparison

Reference	Frequency (GHz)	*NF* (dB)	Gain (dB)	IRL (dB)	ORL (dB)	OBW	P_{DC} (W)	P_{1dB} (dBm)	*OIP3* (dBm)	*LFOM* (OIP3/P_{DC})	Size (mm^2)	Type
[38]	1.0 - 21.0	3.3 - 4.6	11.5 ±1.5	≥ 10	≥ 10	21:1	0.9	17.5	28.5	0.79	1.2×1.2	MMIC
[40]	0.5 - 4.0	1.2 - 2.3	16.0 ±1.5	≥ 4	≥ 16	8:1	1.25	NA	NA	NA	2.7×1.8	MMIC
[41]	0.25 - 3.5	0.9 - 1.3	18.5 ±1.5	≥ 6	≥ 10	14:1	20.0	31.0	38.0	3.2	NA	MMIC
[42]	0.5 - 3.0	1.7 - 1.9	33.0 ±1.5	≥ 10	≥ 10	6:1	3.0	22.0	36.0	0.05	7.0×7.0	Plastic QFN
[113]	0.85 - 1.9	0.68 - 0.76 btw. 1.4 - 1.9 GHz	25.5 ±1.5	≥ 5	≥ 5	2.23:1	0.5	NA	31.0	2.52	4.0×4.0	THSSOP20
[114]	3.0 - 5.5	0.9 - 1.3	11.8 ±1.5	NA	NA	1.83:1	4.0	NA	NA	NA	NA	Simulation
[115]	2.3 - 4.0	2.9 - 4.0	15.7 ±1.5	≥ 7.5	≥ 7.5	1.74:1	0.23	NA	20	0.43	2.25	MMIC
[116]	2.4 - 4.0	2.9 - 4.0	12.5 ±1.5	NA	NA	1.67:1	2.92	NA	NA	NA	NA	Hybrid
This Work (V_D=12 V, I_D=90 mA)	0.03 - 2.4	1.25 - 1.6	11.5 ±1.5	≥ 10	≥ 10	80:1	0.72	14.6* 19.6†	23.4* 28.4†	0.31* 0.97†	3.0×3.0	Plastic QFN
This Work (V_D=24 V, I_D=90 mA)	0.03 - 2.6	1.5 - 2.0	11.5 ±1.5	≥ 10	≥ 10	86.6:1	1.44	19.4* 24.4†	24.9* 29.9†	0.22* 0.69†	3.0×3.0	Plastic QFN

NA: Not Available, IRL: Input Return Loss, ORL: Output Return Loss, OBW: Operation Bandwidth
*Result with the attenuator, †Result without the attenuator

Chapter 6

Conclusion

The aim of this work was to develop a 0.25 μm MS GaN HEMT technology, investigate the kink-effect to extend the operation bandwidth, and design & fabricate an LNA MMIC starting from VHF band. The micro/nano-process is developed in Bilkent University Nanotechnology Research Center (NANOTAM) and Aselsan Bilkent Mikro Nano (ABMN) facilities. All of the fabrications and the measurements are performed in these facilities.

To design the LNA MMIC, the proper equivalent circuit models for SS and noise analysis are developed and the developed CS HEMT model is used to concept cascode HEMT. The developed models show pretty good agreement with the measurements and the models are also used for the analysis of the gate structure on the KE.

The effect of the gate structure on the KE in S_{22} is investigated by developing the transistors with different L_g and L_{gH} configurations. The outputs of the kink study show that the kink parameters also depend on the gate structure besides the bias point, the gate width, and the thermal conditions. It was also shown that the change in C_{gd} affects the KS. Moreover, the isolation of the transistor is also affected as a result of the C_{gd} change. A proper bias point V_D and a proper feedback structure can be effective to suppress the kink in S_{22} associated with

C_{gd}. Therefore, to develop a proper kink-free technology, a proper gate structure has to be employed in the process development, and a proper feedback can be implemented in the design process to minimize the kink in S_{22}. Considering the transistor as a whole, KE exists as a combined effect of the parameters such as C_{gs}, C_{gd}, g_m, the operating temperature, and the bias conditions.

The design and the characterization of a single stage low cost cascode GaN LNA MMIC housed in a 12 lead 3×3 mm^2 air cavity QFN over-molded plastic package with an average *NF* of 1.4 dB is demonstrated. Moreover, the development of the concept cascode HEMT and its performance is presented. Less than 1.6 dB *NF* is achieved with 0.72 W DC power consumption and less than 2.0 dB *NF* is achieved with 1.44 W DC power consumption in a compact size, despite the reference CS transistor has higher NF_{min} in comparison with the state-of-the-art LNA technologies. Considering the operation bandwidth, proposed LNA is suitable for many VHF, UHF, L-Band, and S-Band radar, electronic warfare, and communication applications. Moreover, the modeling approach makes the development of high accuracy cascode HEMT model possible from a single CS HEMT measurement.

The KE study also revealed that it is also possible to develop a kink free process by controlling the process parameters. Thus, the study of the KE in S_{22} can be extended by investigating the epitaxial structure of the wafers, and the multiple process parameters. The concentration of the Al content in the epitaxy and the thickness of the epitaxial layers and growth parameters can be the research parameters for the epixay. Moreover, the isolation method, ohmic contact formation, the passivation method, and the passivation thickness can be the other research parameters for future works.

To improve the accuracy of the noise model at frequencies lower than 100 MHz, the investigation of phase noise is very critical. Therefore, the phase noise can be analyzed in GaN HEMT technology by investigating the trap formation in the substrate and the surface of the wafer. The epitaxial growth parameters will play an important role to suppress the phase noise. Moreover, it is also critical to use suitable process method in order not to create new traps.

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Appendix A

Process Photomasks

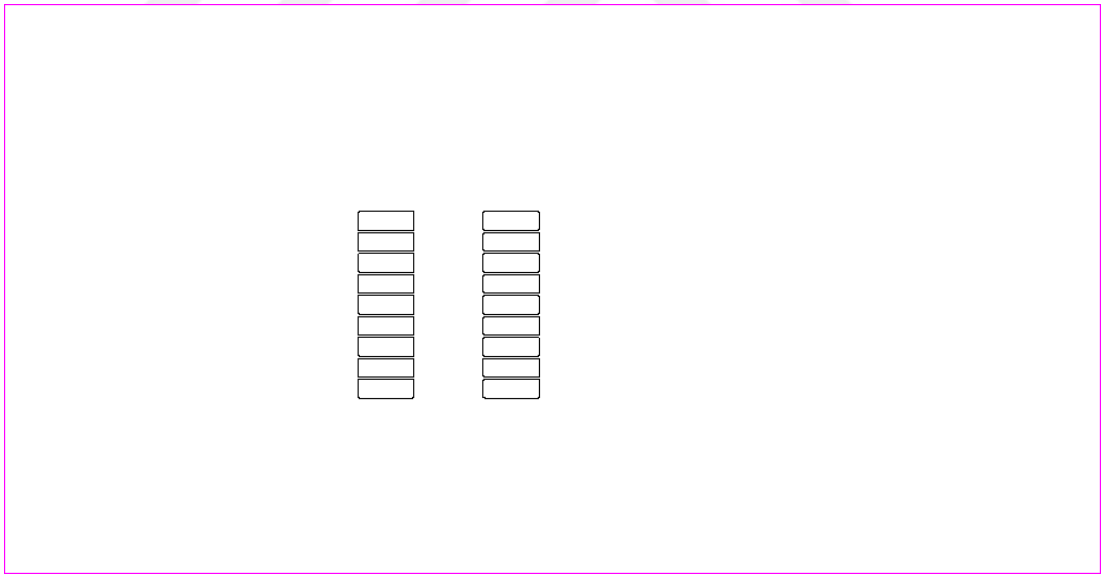

Figure A.1: Layer-1: OHMIC Layer photomask

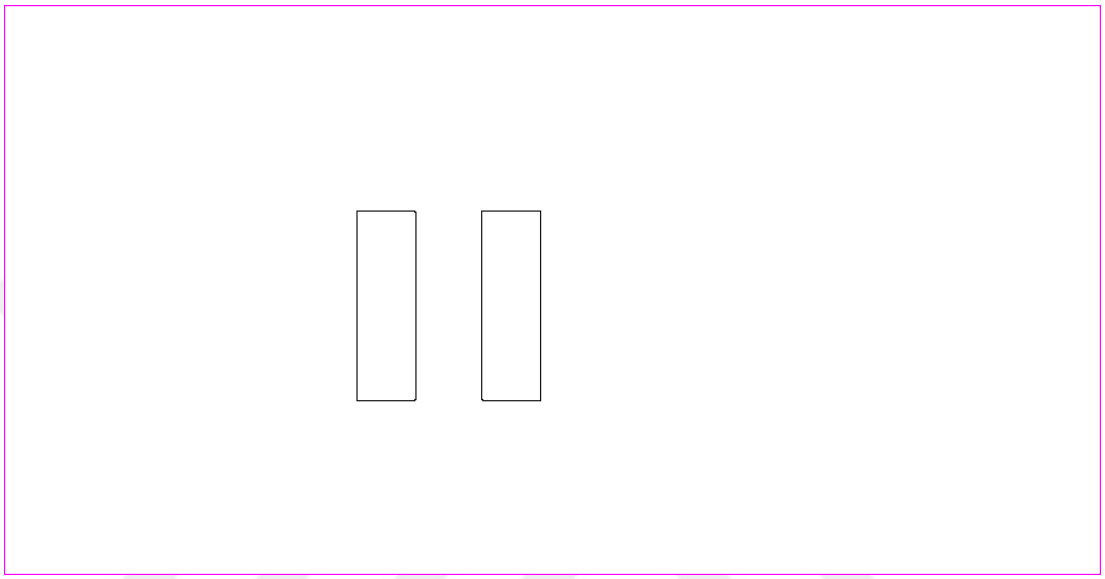

Figure A.2: Layer-2: MESA Layer photomask

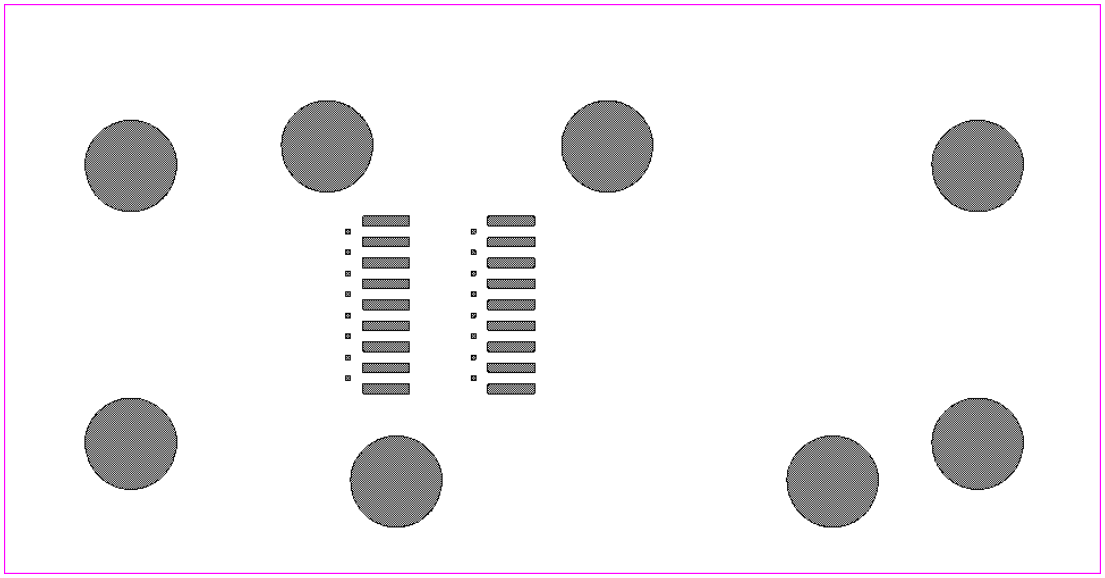

Figure A.3: Layer-3: VIA1 Layer photomask

Figure A.4: Layer-4: TFR Layer photomask

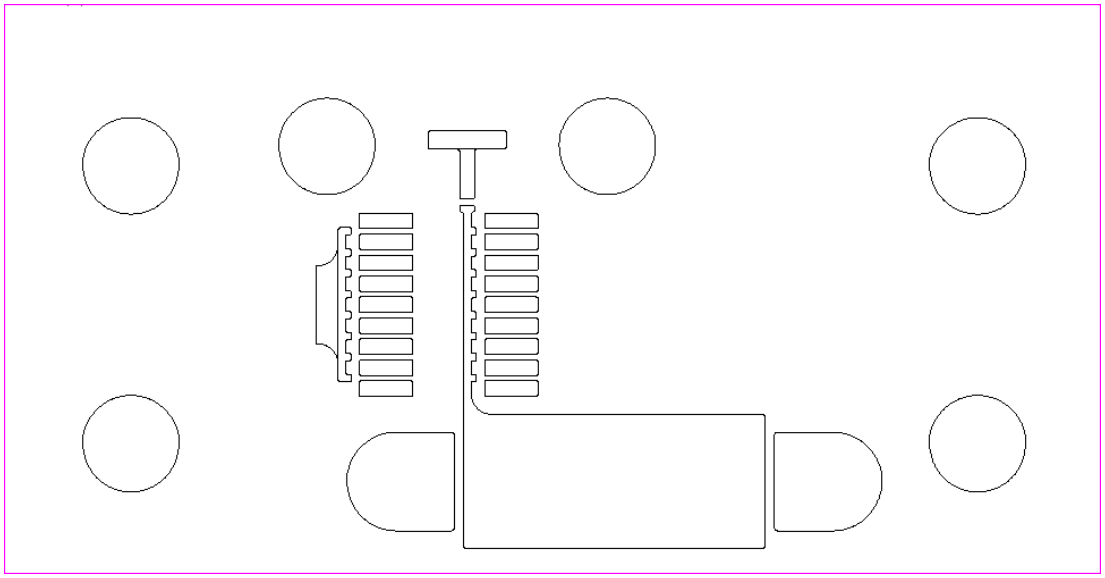

Figure A.5: Layer-5: MET1 Layer photomask

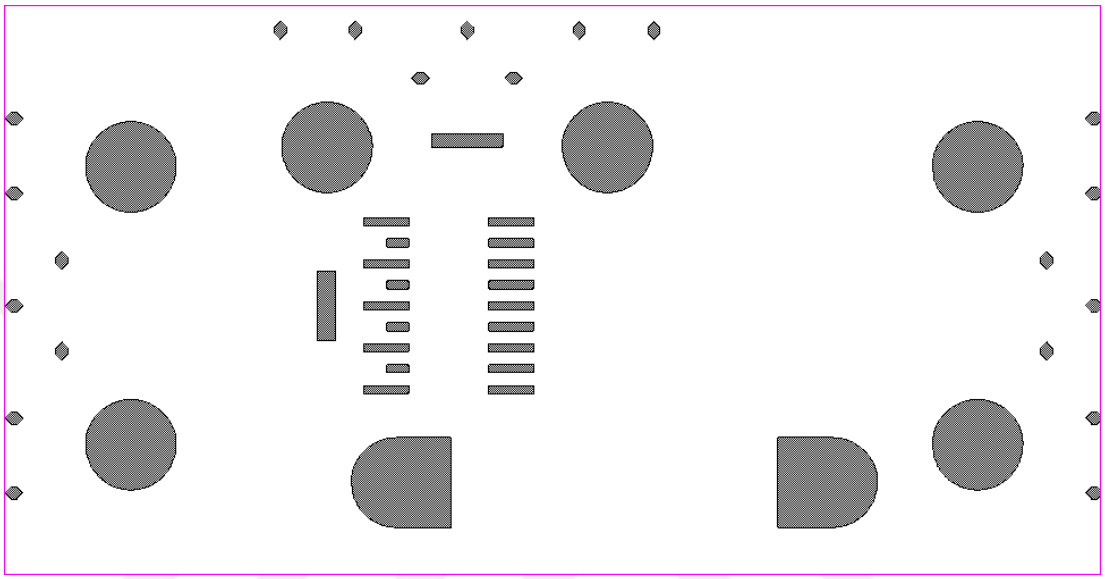

Figure A.6: Layer-6: VIA2 Layer photomask

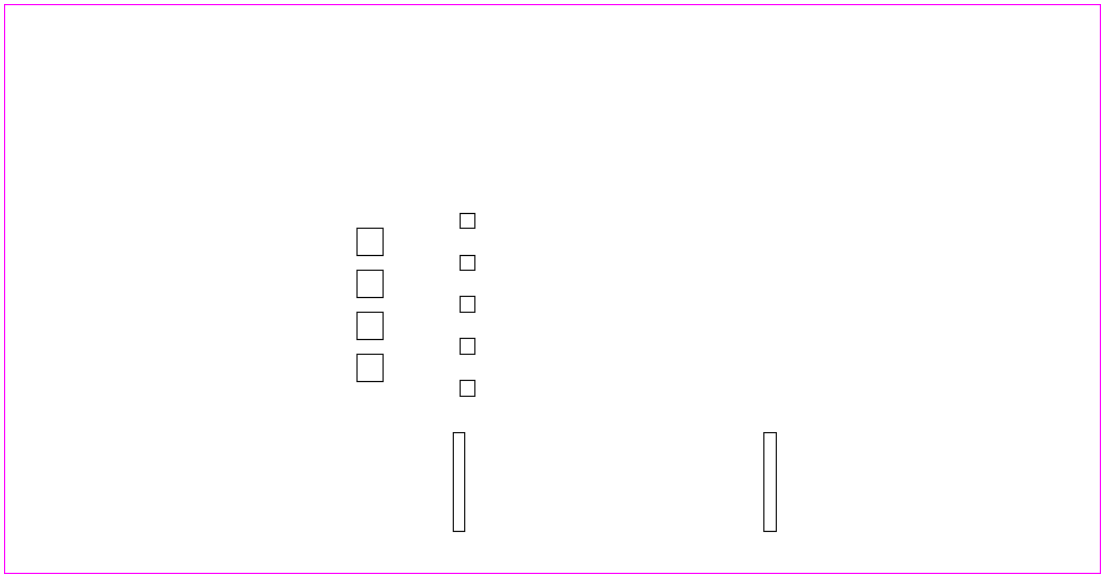

Figure A.7: Layer-7: BRG Layer photomask

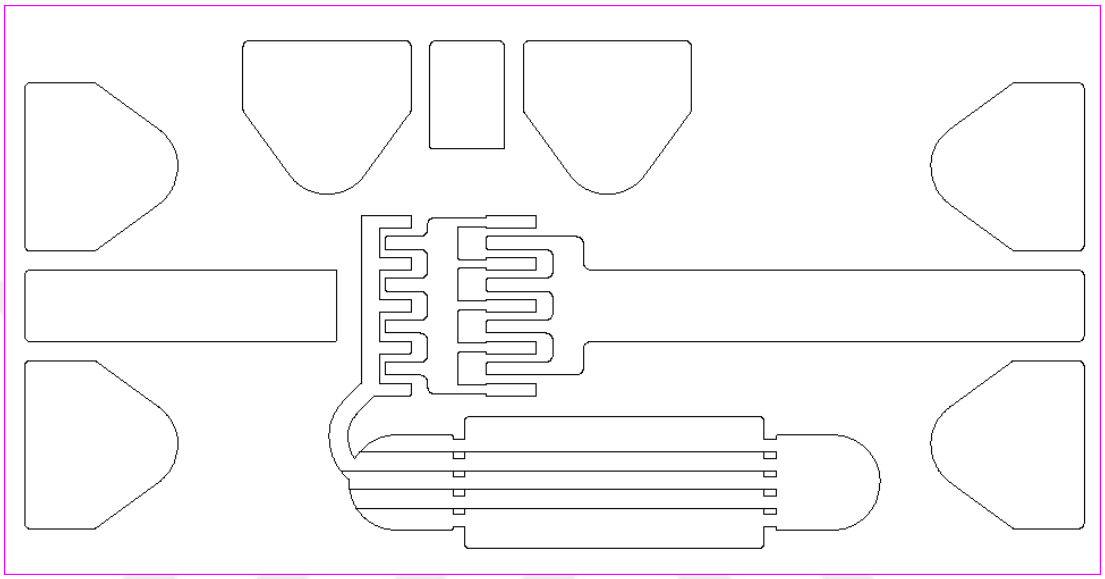

Figure A.8: Layer-8: MET2 Layer photomask

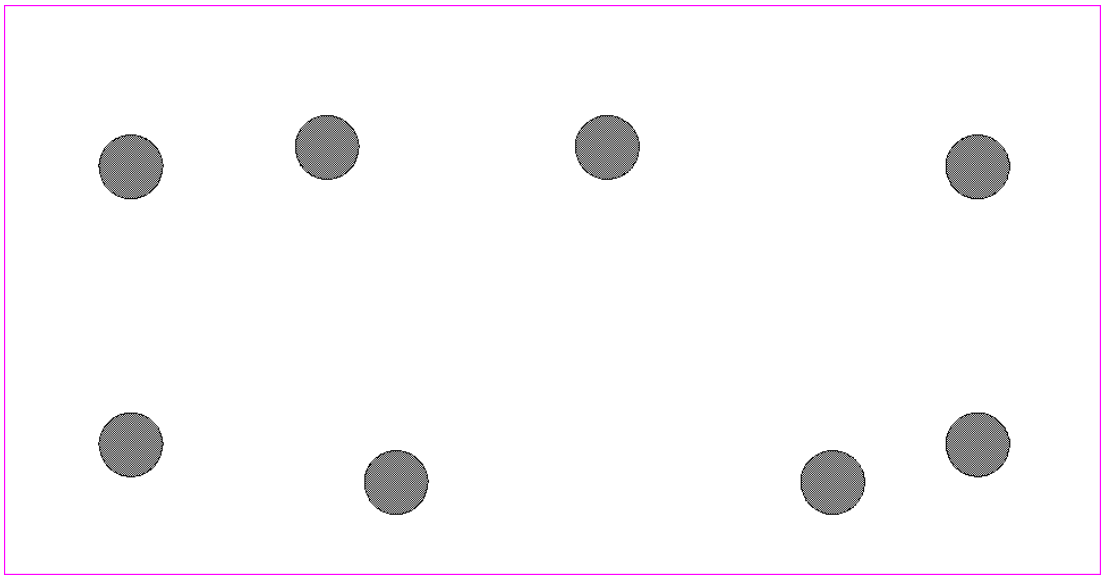

Figure A.9: Layer-9: BVIA Layer photomask