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BOLU ABANT İZZET BAYSAL ÜNİVERSİTESİ

INSTITUTE OF GRADUATE STUDIES

DEPARTMENT OF PHYSICS

INVESTIGATION OF STRUCTURAL AND ELECTRICAL CARACTERISATION OF Sc_2O_3 DIELECTRIC LAYER IN SiC BASE MOS TECHNOLOGY

MASTER OF SCIENCE

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THESIS SUPERVISOR
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BOLU, JANUARY 2025

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The thesis entitled **''INVESTIGATION OF STRUCTURAL AND ELECTRICAL CARACTERISATION OF Sc_2O_3 DIELECTRIC LAYER IN SiC BASE MOS TECHNOLOGY''** prepared and submitted by **NZIENGUI NZIENGUI DARIUS** in partial fulfillment of the requirements for the degree of **Master of Science** in Department of **PHYSICS** with unanimity vote is hereby approved. 12/31/2024

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ABSTRACT

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NZIENGUI NZIENGUI DARIUS
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INSTITUTE OF GRADUATE STUDIES
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BOLU, DECEMBER 2024
XIII + 58

This thesis presents a detailed study of the annealing temperature-dependent structural and electrical properties of scandium oxide (Sc_2O_3) grown, using an electron beam evaporation system, on a 4H-SiC substrate, with XRD, C-V and G/ω-V measurements conducted to analyze its characteristics. In order to enhance capacitor performance, SiO_2 was coated between Sc_2O_3 and 4H-SiC substrate. From XRD measurements, although the lattice parameters, strain and density dislocation increased, crystallite size decreased with increasing annealing temperature was obtained. Moreover, it was also observed that the optimum annealing temperature was found to be 800 $^{\circ}$C with optimal crystallization. From the electrical measurements, it was obtained that the higher annealing temperature enhances capacitance stability and lowers interface state density, resulting in flat band voltage adjustment. The measured capacitance and conductance's values due to the series resistance were corrected and it was obtained that the electrical properties was significantly affected by series resistance. The result indicated that both series resistance and interface states must be taken into account during the electrical characterization. Interface state density decreased while effective oxide state density increased with the increase in annealing temperature. The existing of thermally grown SiO_2 between the Sc_2O_3 thin film and SiC substrate enhanced the device of performance with rising annealing temperature.

KEYWORDS: 4H–SiC; Silicon Carbide, MOS Capacitor; Sc_2O_3, Dielectric, Annealing.

ÖZET

SiC TABANLI MOS TEKNOLOJİLERİNDE Sc_2O_3 DİELEKTRİK TABAKANIN YAPISAL VE ELEKTRİKSEL ÖZELLİKLERİNİN İNCELENMESİ
YÜKSEK LİSANS
NZİENGUİ NZİENGUİ DARİUS
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BOLU, ARALIK 2024
XIII + 58

Bu tez, XRD, C-V ve G/ω-V ölçümleri ile 4H-SiC altlığın üzerine elektron ışını buharlaştırma sistemi kullanılarak büyütülen skandiyum oksidin (Sc_2O_3) tavlama sıcaklığına bağlı yapısal ve elektriksel özelliklerine ilişkin ayrıntılı bir çalışma sunmak ve özelliklerini analiz etmektir. Kapasitörün performansını arttırmak için Sc_2O_3 ve 4H-SiC altlık arasına SiO_2 kaplandı. XRD ölçümlerinden kafes parametreleri, gerilme ve yoğunluk kaymanın artmasına rağmen tavlama sıcaklığının artmasıyla kristal boyutunun azaldığı gözlendi. Ayrıca optimum kristalizasyon ile optimum tavlama sıcaklığının 800 °C olduğu da gözlenmiştir. Elektriksel ölçümlerden, daha yüksek tavlama sıcaklığının kapasitans kararlılığını arttırdığı ve ara yüzey durum yoğunluğunu düşürdüğü, bunun sonucunda düz bant voltaj ayarının yapılması gerektiği sonucuna varıldı. Seri direnç nedeniyle ölçülen kapasitans ve iletkenlik değerleri düzeltilmiş ve elektriksel özellikleri seri dirençten önemli ölçüde etkilendiği gözlenmiştir. Sonuç, elektriksel karakterizasyon sırasında hem seri direnç hem de ara yüz durumlarının dikkate alınması gerektiğini gösterdi. Tavlama sıcaklığının artmasıyla ara yüzey durum yoğunluğu azalırken etkili oksit durum yoğunluğu arttı. Sc_2O_3 ince filmi ile SiC altlık arasında termal olarak büyütülmüş SiO_2'nin varlığı, artan tavlama sıcaklığıyla cihazın performansını arttırdı.

ANAHTAR KELİMELER: 4H–SiC, Silikon karbür, MOS kapasitör, Sc_2O_3, Dielektrik, Tavlama.

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LIST OF ABBREVIARIONS AND SYMBOLS

FWHM: Full width at half maximum

C-V: Capacitance-Voltage

Sc_2O_3: Scandium Oxide

D_{hkl} : The inter-planar spacing between crystallographic planes

Sm_2O_3 : Samarium Oxide

CMOS : Complementary Metal-Oxide-Semiconductor

G/ω-V: Conductance-Voltage

MOSFET: Isolated gate field effect transistor

Q_{SC}: Space charge density

N_s: Density of interface traps

CuKα: Copper K-α

θ: Bragg's angle

λ:Wavelengthof the incident X-ray

XRD: X-ray Diffraction

a: Lattice constant

V_{GB}: Voltage between the gate and base of semiconductor

ACKNOWLEDGEMENTS

I would like to express my deep gratitude to my supervisor Prof. Dr. Cabir TERZİOĞLU for his quality teaching since I arrived at the university, his patience, his professionalism, his advice, with him I acquired deep knowledge in Physics. I was much honored to learn from Prof. Dr. Cabir TERZİOĞLU, a source of inspiration and a role model.

I would like also to thank Assoc. Prof. Dr. Şenol KAYA for his supervision in the laboratory, his leadership, his rigor in his work, his advice and above all his availability. I thank him very much.

I wish to express my gratitude to all the teachers who supervised me during my Masters Prof. Dr. Nuray ER, Prof. Dr. Hakan YETİŞ, Prof. Dr. Mustafa AKDOĞAN, to all members of the Physics department and the center for Nuclear Radiation Detector Application and Research (NURDAM).

Finally, I especially thank my family members for their financial support, their prayers, their love and trust in me. Without them this project would never have been successful. To my late big sister Ornella, I thank her for everything she did for me.

This work was partially supported BAİBÜ Scientific Research Office with 2022.03.02.1535 and 2021.09.01.1521 projects. I also would like to thank to Presidency of the Republic of Turkey Presidency of Strategy and Budget (Contract Number: 2016K12-2834).

1. INTRODUCTION

1.1An Overwiew of Previous Studies

Lanthanide oxides have gained global attention due to their distinctive structural, optical, electrical and chemical properties. These oxides find extensive use in the production of photonic sensors, phosphors and solid-state optoelectronic, and are also integral to the next generation of photo-conversion-based solar cell devices. Specific applications include their role as electrode materials in high-performance supercapacitors (Majumder, 2017). Impact, antioxidants in the biomedical sector (Muthulakshmi, 2020), and catalysts for selective hydrogenation (Ning, 2020), and in the development of sensing devices like solar cells, thanks to their remarkable luminescent properties (Kumar, 2020). Additionally, they serve as buffer layers for generating acoustic resonators (Dargis, 2020), for gamma ray shielding (Mahmoud, K, 2020 and Rammah, Y. S. 2020), in photoluminescence-based gas sensors (Kisk, V, 2019), and as drug delivery agents (Abuid, N. J. 2020), among numerous other uses. Scandium oxide (Sc_2O_3) is emerging as a crucial material fort the next generation of silicon transistors and memory devices. With a band gap of 6 eV (Tippins, H. H. 1966), and a relative permittivity of 13 (Shannon, R. D. 1993), it is particularly studied for flash memory applications (Kitt, J. A. 2009). This material can provide electical isolation between the control gate and the charge storage layer in both floating gate memories (flotox) and charge trap memories. In flotox devices, the insulator is located between poly-Si gates (Mori, S. 1996), known as the inter-poly-Si dielectric. In charge trap memories, the insulator or blocking oxide is in contact with a silicon nitride trapping layer an a p-type metal (An, H. M. 2009). Furthermore, ternary compounds such as $GdScO_3$, $DyScO_3$ and LaScO3 are gaining interest in CMOS circuits due to their high permittivity and exceptional stability when in contact with silicon (Roeckerath, M. 2009).

Sc_2O_3 has been extensively studied for various applications (Klenow, 2005). While its permittivity is moderate, ranging from 13 to 14 (Shannon, R. D. 1993), Sc_2O_3 exhibits several advantageous properties, including a large band gap of approximately 6 eV (Afanas'ev, V. V. 2007) a conduction band offset of about

2 eV relative to the silicon, and predicted thermodynamic stability when in contact with silicon (Hubbard, K. J. Schlom, D. G. 1996). Sc_2O_3 has been investigated for different uses, such as a gate insulator for silicon-based MOSFETs (Klenov, 2005), a gate dielectric and surface passivation layer for GaN/AlGaN High Electron Mobility Transistors (Gila, B. P. 2003), and for providing electrical isolation betwen the control gate and charge storage layer in flash memory devices (Kittl, J. A. 2009). When depositing high-k materials in direct contact with silicon, an interfacial layer typically forms (Hakala, M. H. 2005). This unintentional interfacial layer can degrade the channel mobility of MOSFET transistors and increase leakage current. A common strategy to prevent this reaction is to grow a controlled, defect-free SiO_2 barrier. However, this barrier layer results in reduced permittivity. An alternative approach involves using silicon nitride (SiN_x) istead of SiO_2, which can enhance the capacitance equivalent thickness of the structures due to its higher permittivity. The initial thin films of Sc_2O_3 were produced by Heitmann (Heitmann, W. 1973) using reactive evaporation. Recently, various techniques, including dip coating (Grosso, D., Sermon, P. A. 2000), electron beam evaporation (Kuhaili, M. F. 2003), and metal-organic chemical vapor deposition, have been employed to deposit Sc_2O_3 films (Xu, Z., Daga, A., Chen, H. 2001), and their properties have been thoroughly analyzed.

In recent years, the application of high-k dielectric materials on SiC, either directly or with ultra-thin interfacial transition layers such as SiO_2, has significantly improved interface trap densities. However, much higher trap densities, 10^{11}–10^{12} cm^{-2}, are observed at the SiO_2/SiC interface compared to the SiO_2/Si interface, where trap densities range from 10^{9}–10^{10} cm^{-2} (Kil, T.-H., and Kumar, P). High-k dielectric materials can enhance performance by increasing the electric field on SiC relative to SiO_2 due to their higher permittivity (Liang, L. 2018 and Huang, L.H, 2022). Furthermore, these materials improve threshold voltage and reduce leakage current (Liang, L. 2018 and Huang, L.H, 2022). The reduction in trap densities is attributed to the use of ultra-thin SiO_2 layers as a transition layer. This minimizes structural defects by reducing the formation of potential CO_x compounds (Urresti, J 2019 and Liu, P 2021). The ultra-thin interfacial layer is deliberately grown at low temperatures to prevent undesired SiO_xC_y formation (Pande, P. Haasmann, D. et al., 2020). Thus, the ultra-thin SiO_2 layer grown at low temperatures serves as a

transition layer, improving interface quality and reducing trap sites, with high-k dielectric materials deposited on it.

In the research world, a considerable attention was carried out on the novel dielectric materials such as Sm_2O_3, Eu_2O_3, HfO_2 and TiO_2 for Metal-Oxide-Semiconductor (MOS) technology using in the field such as radiation sensors, components of computers, telephone and another electric device. Among these materials, Sc_2O_3 has a good linear performance, high sensitivity, thermodynamically stability, real time response and acceptable reliability (S. Steigerwald, J.1994). When MOS capacitor is made, any parameters can affect the structural and electrical characteristics of capacitor like silicate layers, series resistances and density of interface state. Impurity phase can cause malfunctions at the level of the capacitor performances (Kaya, S. Yılmaz, E,2015). S.M. Sze studied also the effects of post-temperatures on structural and electrical parameters of Sc_2O_3 thin films. Grains sizes decreased while lattice parameters and geometrical strain increased as annealing temperature increased were observed (Sze, S. M., 1981). Temperature dependent of capacitance-voltage (C-V) and conductance–voltage measurements were carried out at room temperature. It was observed that the changing of temperature increased capacitance and conductance values and causes the flat band voltage towards negatives values and it causes by positive charges trapped in the accumulation region (Hakala,M.H, 2006). H. Castánet al. investigated electrical characterization of high-pressure reactive sputtered ScO_x films on Si. They found that when oxide is directly in contact with Si, the interfacial layer formed is uncontrollable caused many defects in oxide-semiconductor interface, increased leakage current and reduced permittivity (Maxwell, J.C., 1873).

This study presents a comprehensive analysis of Al/Sc_2O_3/SiO_2/4H-SiC MOS capacitors, focusing on how annealing temperature influences structural and electrical properties on the films. Moreover, the effect of series resistance, effective charge density and interface state density on the electrical properties as a function of annealing temperature was focused. Despite quite a few reports of frequency, pressure, substrate temperature and interfacial layer dependent behavior of the Sc_2O_3 grown on Si substrate in the available literature, to the best of our knowledge, no reports have been published on the analyzing structural and electrical

characteristic of the Sc_2O_3 grown on SiC substrates annealed at different temperature.

1.2 Aim and Scope of the Study

The aim of this study is preparation of Al/Sc_2O_3/SiO_2/4H-SiC/Ag MOS capacitors to investigate the effect of annealing temperature on structural and electrical properties. SiO_2 is coated on SiC substrate via thermal oxidation method and Sc_2O_3 is grown on the SiO_2/SiC by electron beam evaporation system. To investigate the structural and electrical properties of the MOS capacitor, XRD, C-V and G-V measurements as a function of annealing temperature were performed. Moreover, the effect of series resistance, effective charge density and interface state density on the electrical properties as a function of annealing temperature was studied. Despite quite a few reports of frequency, pressure, substrate temperature and interfacial layer dependent behavior of the Sc_2O_3 grown on Si substrate in the available literature, to the best of our knowledge, no reports have been published on the analyzing structural and electrical characteristic of the Sc_2O_3 grown on SiC substrates annealed at different temperature. The annealing temperature has an important effect on crystal structure, capacitance and conductance. To eliminate the series resistance, the correction was performed on the C-V and G-V measurements. Annealing temperature affects the series resistance, interface state density and effective charge density values of the MOS capacitors. These effects were discussed and interpreted.

1.3 Dielectrics

1.3.1 Dielectric Parallel Plate Capacitors

In general, a capacitor is an electronic device having two conductors of similar or different electronic properties separated by a vacuum or an insulator. The structure of the capacitor is arranged such that the arrangement of the components forms a parallel structure. This device is called a dielectric capacitor when the insulating material (dielectric material) introduced in the middle of the two conductors (Serway,A., Jewett.W. 2008).

A dielectric material is a medium which does not have any free electrons capable of carrying electric current and capable of being polarized by an external electric field applied to this material between these terminals. Its conductivity (σ) is low and its electrical resistivity ($\rho = \frac{1}{\sigma}$) is generally between 10^{17} and $10^{19}\Omega.m$.

When the charges of opposite signs are inserted on the conductors, an electric field (E) appears at the level of the conductors and a potential difference between these two electric plates. The electric field is, in this case, proportional to the intensity of the charges in the capacitor. The difference in potential and the electric field decreases by a factor of $1/\varepsilon$ (ε is dielectric constant). The capacitance of a capacitor C_0 is the ability to store electric charges of opposite signs on these metal plates (conductors) and is defined as the ratio between its charge Q and the potential difference between its conductors V_{ab} given by the relation:

$$C_0 = \frac{Q}{V_{ab}} \tag{1.1}$$

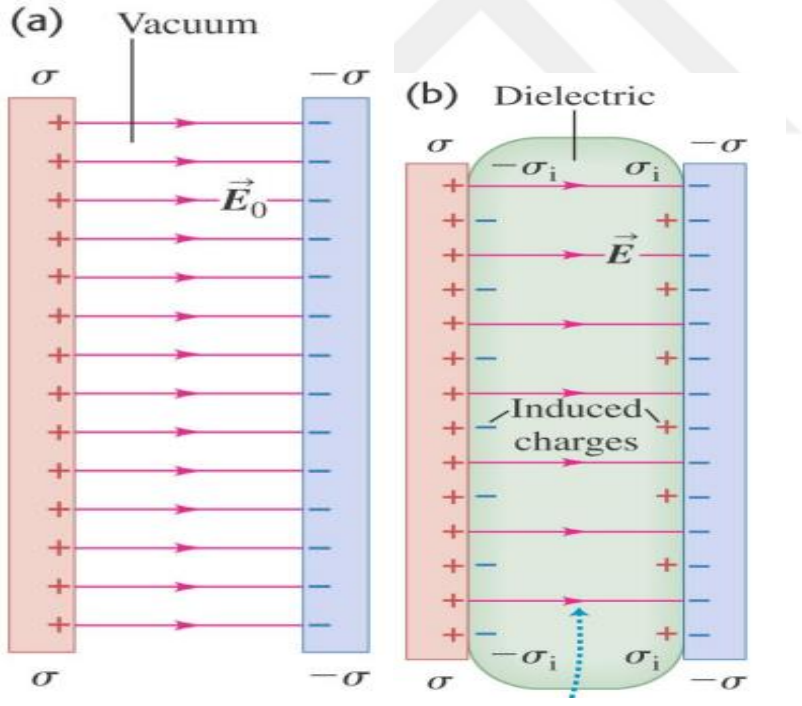


Figure 1.1. a) Capacitor without dielectric, b) Capacitor with dielectric

However, there is a small space between the conductors in the capacitor, if the conductors and the dielectric are placed so that the spacing between the three components are sufficiently negligible, the electric field will be uniformly

distributed on the opposite surfaces of the components called parallel-plate dielectric capacitor as illustrated in Figure 1.1.

There are several applications in the field of electronics such as integrated circuits, detectors, sensors, power distributions and conversion systems etc.... The presence of a dielectric in a capacitor is important because it allows both to have a sufficiently large electric field (dielectric breakdown) without breaking the dielectric, to maintain conductors with a small separation without contact and increases the capacitance of the capacitor.

1.3.2 Polarization Mechanisms

When a dielectric material is subjected to an external electric field, three phenomena actually occur including a modification of the dielectric revealed by the Kerr effect (Maxwell, J.C., 1873), in a considerable time, the observation of a real conductivity of the dielectric through its mass and its surface due to the impurities which cover it and finally the material presence of electrostatic dipoles capable of interacting with the electric field concerns. This interaction results in the creation of different types of polarization. Polarization changes occur gradually according to the degree of polarization depending on the temporal variation of the external electric field. The induced dipoles themselves produce fields whose result often tends to oppose the external electric field. By polarizability, it can be related to the amplitude of the dipole wave created. A macroscopic quantity can be used for the measurement: polarization which is the sum of all the dipoles of the dielectric material. At the microscopic level, measurement is still impossible. Consequently, there are different types of polarization: electronic polarization, atomic polarization, directional polarization and interfacial polarization. Each type of polarization presents characterizations in resonance frequency such as electronic and atomic polarization and relaxation characterizations in interfacial polarization.

1.3.2.1 Electronic Polarization

Electronic polarization is present in all the different types of dielectrics in existence. It is the result of the displacements of the external electronic orbitals of the nucleus of the atom of the corresponding dielectric. The deformation of the orbit is called elastic because the work supplied is stored in the electric field and is not

converted into heat by the Joule effect. It is independent of frequency and takes only approximately $10^{-15}s$. In the absence of an electric field, the barycenter of the charges in the atom are combined.

In the presence of the electric field, the electronic cloud deforms, creating a shift in the centers of gravity of the negative (electrons) and positive (protons) charges as shown in Figure 1.2. The atom now has a non-zero dipole moment, $\vec{P}$, is proportional to the electric field created at the atom and can be given by,

$$\vec{P} = \varepsilon_0 \chi \vec{E} \tag{1.2}$$

with ε_0 vacuum permittivity and χ electrical susceptibility of the dielectric. The electronic elastic polarization and the induced dipoles disappear when the electric field disappears.

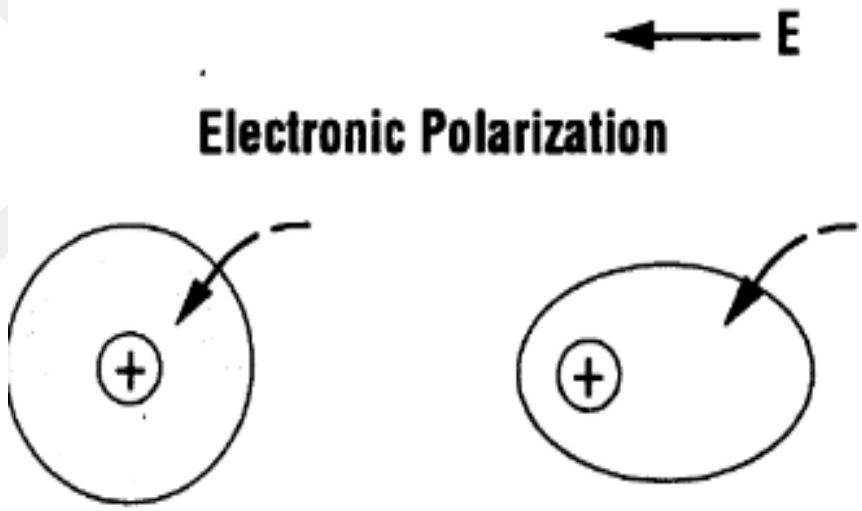


Figure 1.2. Electronic polarization

1.3.2.2. Atomic Polarization

Atomic polarization is characterized by the movement of atoms connected by ionic bonds in such a configuration as the electrons located in the valence shell circulate at the level of the orbitals shared with neighboring atoms. In this polarization, the networks of negative ions move as a whole relative to the network of positive ions in opposition to the electric field. This is the case for certain crystals. Given that the inertia of the ions is extremely heavy, the latter has a very

short settling time of the order of $10^{-14} \leq \tau \leq 10^{-12} s$, τ is the duration of atomic polarization.

It all depends on the intensity of the ionic bonding forces, i.e. the electrostatic attraction between neighboring atoms. Electrostatic attraction is the force that attracts electrons to the nucleus of the atom as demonstrated in Figure 1.3. The higher the electrostatic attraction, the less atomic polarization occurs. Note that ionic bonds are, in most solid, dielectrics. Its contribution is two to three times stronger than ionic polarization. Atomic polarization has similarities with electronic polarization such as the fact that it does not cause loss of energy producing induced dipoles which disappear when the external electric field is removed. It exists in the low frequency corresponding to infrared. Its frequencies are very far from those which usually occur in high voltage systems. In such a polarization according to Maxwell the relative permittivity ε_r is worth 2.

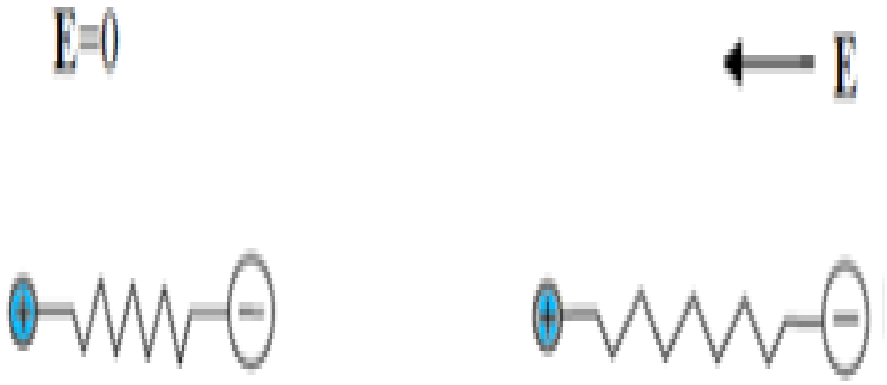


Figure 1.3. Atomic polarization

1.3.2.3 Directional Polarization

Directional polarization is governed by the orientation of dipolar molecules or atoms under the action of an electric field where they have a permanent dipole moment. Under the impulse of an electric field, a movement of charges occurs, producing a deformation of the structure of the dielectric. We subsequently observe a new so-called quasi-static arrangement of molecules in the dielectric followed by the creation of a dipole moment. There exist molecules having a dipole moment $\vec{P}_0$ in the absence of an electric field in thermal equilibrium. In the absence of an

electric field, these dipoles have a random arrangement and an indescribable orientation, the resulting dipole moment is zero. But in the presence of the electric field, the dipoles present in the molecules are subjected to a torque which orients them in the direction of the field as depicted in Figure 1.4. This results in a macroscopic dipole moment. The dipole moment disappears with the removal of the field because the thermal movement due to the temperature of the medium returns the molecules to their initial distribution. The change of direction takes place in a given time called relaxation time (τ_e), this is the time necessary to reach an equilibrium and appears at frequencies in the microwave range. It increases proportionally with the dipole moment and decreases with temperature (Hajji, R., Oueslati, A., 2015).

E= 0 E≠0

Figure 1.4. Directional polarization

1.3.2.4 Interfacial Polarization

Interfacial polarization occurs at the interface between two solids having different conductivity (σ) and permittivity (ε). It is characterized by dielectrics of different structures whose residual charges form an energy barrier which opposes the electric field inside the solid when they are in movement. This opposition slows down the movement of the charges in the dielectric and can be traps thus preventing any movement, a charge space is then produced so that the establishment of the polarization varies from $10^{-2}s$ to a few minutes. It can be observed in different

dielectrics made up of intrinsic free charge carriers (electrons or ions). At the interface level, there is a significant accumulation of charges.

1.3.3 High-k Dielectric Materials in MOS Structure

When an electric field is applied to a dielectric, the material polarizes aligning the charges with the direction of the electric field which allows the dielectric to store the electrical energy produced in the form of an electric field. The higher dielectric constant materials are used in the capacitor results in higher capacitance value and more stored electrical energy. In MOS structures, the dielectrics used are solid materials such as ceramics, polypropylene, glass and synthetic oxides. Oxides have high dielectric constants and are typically used in MOS and MOSFET devices because they can withstand intense electric fields. The dielectric constant is a very important property for dielectrics because the lower the dielectric loss, the stronger and more efficient the dielectric. If the electric field exceeds a certain threshold the dielectric becomes a perfect conductor and the electric current can flow freely, this is the phenomenon of dielectric breakdown, the damage can be permanent in the structure. The greater the dielectric constant, the more energy the capacitor will store within it.

1.3.4 Dielectric Properties

When an electric field is established in a dielectric, the dielectric becomes polarized by different mechanisms. The electric dipoles generated are in the direction of the periodic electric field of frequency ($\omega = 2\pi f$). The displacement vector thus generated in equation (1.3) oscillates with the external electric field thus describing a phase shift between the two. This is a complex situation, and the dielectric constant will be a complex number consisting of a real part noted ε' and an imaginary part noted ε''. The real part of the complex electrical permittivity is the energy stored in the dielectric and the imaginary part of the permittivity is the energy lost by the Joule effect. We have the following relationships:

$$\vec{D} = \varepsilon^* \vec{E} \tag{1.3}$$

and

$$\varepsilon^* = \varepsilon' + j\varepsilon''. \quad (1.4)$$

$$\varepsilon' = \frac{Cd}{\varepsilon_0 A} \text{ and } \varepsilon'' = \frac{Gd}{\omega A \varepsilon_0} \quad (1.5)$$

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} \quad (1.6)$$

A is the front contact area of the capacitor, C the measured capacitance, G the conductance, ω the angular frequency of the applied voltage, ε_0 the primitiveness of the vacuum and d the thickness of the desired dielectric films.

By introducing a dielectric between the conductors of the planar capacitor, the voltage (V) becomes smaller than the initial voltage also decreasing the electric field which also decreases. The capacitance of the capacitor having the dielectric has increased. It can be deduced from this that the capacity of the dielectric which stores energy does not depend on the voltage of the initial charge but rather on the nature of the dielectric introduced into the capacitor. The new capacity (C) is linked to the first by the relation:

$$C = \varepsilon^* C_0. \quad (1.7)$$

The fact that a dielectric in a planar capacitor is sensitive to an external electric field, we identify it with an electric circuit whose equivalent circuit is given by Figure 1.5. It will therefore be characterized by an admittance (Y) which is an important factor in the search for its properties given by

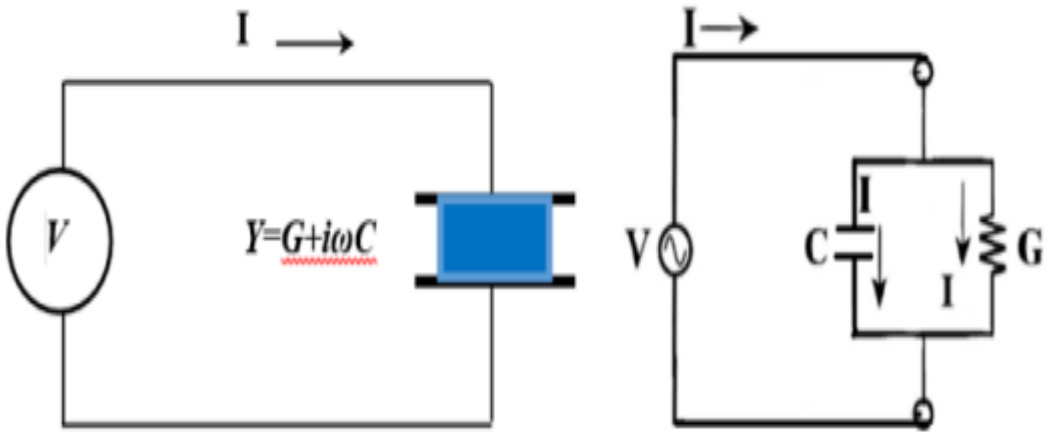


Figure 1.5. Equivalent circuit.

$$Y = G + j\omega C \quad (1.8)$$

$$Y = G + j\omega\varepsilon^* C_0 \quad (1.9)$$

$$Y = (G - \varepsilon'' C_0) + J\omega\varepsilon' C_0 \quad (1.10)$$

The conductivity of the dielectric is also characterized by its real part σ' considered as the electrical conductivity of the alternating current σ_{ac} and an imaginary part σ'' i.e. the equation:

$$\sigma^* = \sigma' + j\sigma'' \quad (1.11)$$

$$\text{with } \sigma_{ac} = \sigma' = \omega C \tan\delta \frac{d}{A} = \varepsilon'' \omega \varepsilon_0 \quad (1.12)$$

1.4. Basic Principles of Metal-Oxide-Semiconductor Structure

1.4.1 General Description of Semiconductors

Nowadays, almost all civil and military technologies contain semiconductors such as mobile phones, computers, satellites, missiles, etc. These so-called materials (semiconductors) have unique and very important characteristics which explains their usefulness in the field of electronics today. Possessing a conductivity which is between conductive materials and insulating materials, semiconductors can behave both as an insulator but also as a conductor by allowing electric current to pass under certain conditions. The manufacture of such materials requires chemical purification in order to eliminate all the impurities present in the material because these various impurities can cause irreversible damage, for example by preventing the transmission and control of electric current within the semiconductor.

Crystalline solid semiconductors are materials that can be found in column 4 of the periodic table of elements such as carbon (C), silicon (Si) and germanium (Ge) which crystallize in the diamond structure are the most important and most used semiconductors. Electrons of solid in nature are not strongly localized at the ionic core. The crystals which belong to the combination of columns 3 and 4 of the periodic table are partially ionic and partially covalent materials, these are the elements gallium (Ga), phosphorus (P), indium (ln) etc... as well as materials such as silicon carbide (SiC). The properties of these semiconductor materials are generally due to their thermal agitation, density of impurities, crystal lattice defects and stoichiometry. There are also amorphous and liquid semiconductors which have

disordered structures and do not have the rigid crystal structure of conventional semiconductors which are used to produce thin film structures MOS devices.

When a semiconductor is subjected to an electric field, electrons become mobile by moving through the semiconductor substrate, the higher the charge density, the better and faster the performance of the electrical device. The study of the movement of charge carriers within the semiconductor is important in order to determine the characteristics of the materials and to optimize them. Band theory gives us precise information on the arrangement of electrons in energy bands. The valence band has electrons bound to the nucleus and the conduction band has free electrons that can move around. Therefore, the distance separating the valence band and the conduction band determines whether a material is insulating, semiconducting or conducting. In insulators, the electrons in the valence band are separated from the conduction band by a large energy gap. In semiconductors, the gap between the valence band and the conduction band is small to the point where when the material is subjected to an external electric field, electrons can easily pass from the valence band to the conduction band producing pair's electron-hole responsible for electrical conductivity within semiconductors. In conductive materials, the valence band simply coincides with the conductor band so the electrons do not need energy for a transition between the valence and conduction bands as shown in Figure 1.6.

Fermi energy (E_F) can be defined as highest energy level that electron can occupy at the absolute zero temperature. It plays a very important role in the study of semiconductors because its location in relation to the conduction and valence bands informs us about the electrical characteristics by influencing the behavior of the charge carriers in the semiconductor. The Fermi level is close to the conduction band the electrons are more available for conduction and the holes become a minority, while it is close to the valence band the holes are more available for conduction the electrons become in this minority case. The Fermi-Dirac distribution describes how charge carriers populate energy levels as a function of temperature in the semiconductor with following formula:

$$n(k)=\frac{1}{e^{(\varepsilon(k)-\mu)/k_B T}+1} \tag{1.13}$$

At the absolute zero of temperature, $n(k)$ changes from one to zero discontinuously at the energy $\varepsilon(k) = \mu = E_F$ and all energy levels occupied by electrons, the energy levels above holes.

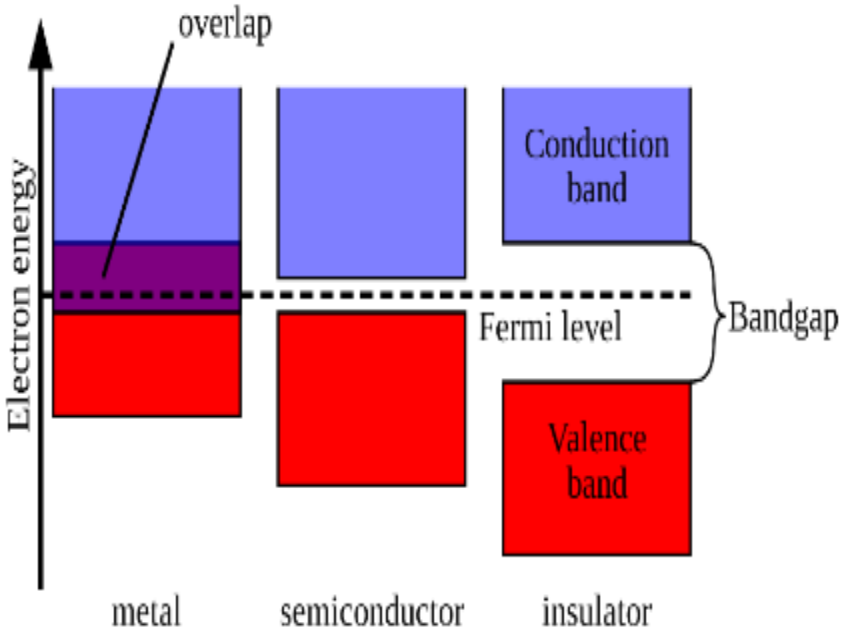


Figure 1.6. Energy band structure diagram.

1.4.2. Types of Semiconductors

In general, there are two types of semiconductors: n-type and p-type semiconductors have a higher electron density than holes because electrons are the majority charge carriers. It is a doped intrinsic semiconductor into which donor type impurities such as arsenic (As) are generally introduced (see Figure 1.7) because they make it possible to give an electron to the conduction band. During donor type doping, the atoms introduced into the semiconductor cause the appearance of an energy level located just below the conduction band which easily allows the electrons to reach the conduction band without the supply of a large quantity of energy compared to the intrinsic semiconductor.

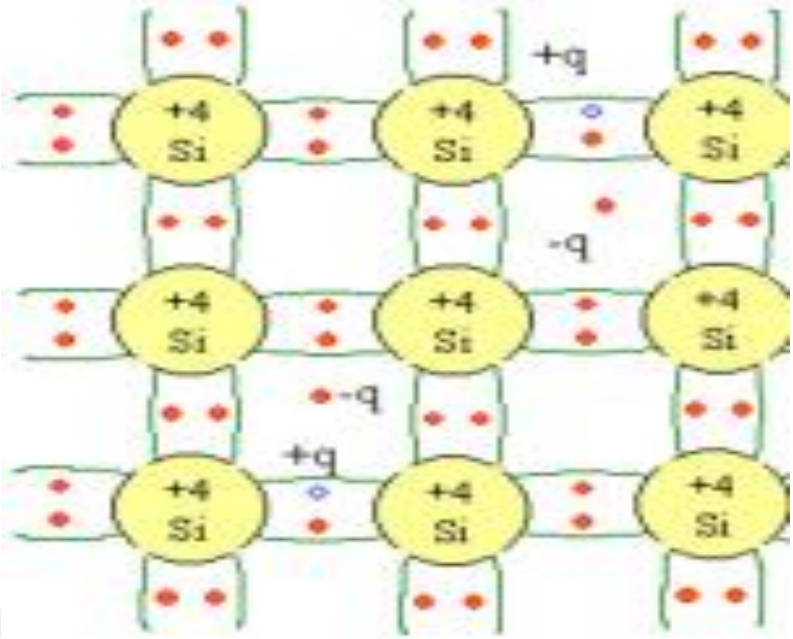


Figure 1.7. Intrinsic semiconductor

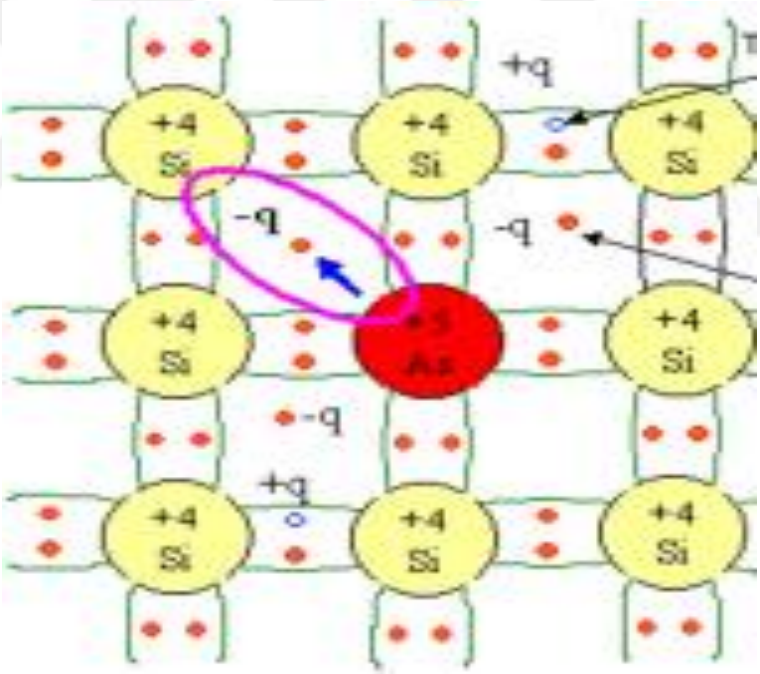


Figure 1.8. n-type semiconductor doped with arsenic.

p-type semiconductors have a lower electron density than holes because holes are the majority charge carriers. It is also an intrinsic dope semiconductor in which we generally introduce acceptor type impurities such as boron (B) (i.e. having an electron defect) as depicted in Figure1.9 and Figure1.10. Because they allow us to receive an electron from the conduction band in order to make connections within the semiconductor. During acceptor type doping, the atoms

introduced into the semiconductor cause the appearance of an energy level located above the valence band. The energy provided to the electrons to move in this energy level is low leading to the appearance of holes in the valence band (Sze S. and Lee M., Semiconductor Devices, 2007). In Figure 1.11, the Fermi energy creates with dopant n is between donor energy level and the conduction band. This energy appears closer to the conduction band than the valence band. The Fermi energy also creates with dopant p is between acceptor energy level and the valence band, then the Fermi level will be closer to the valence than conduction band.

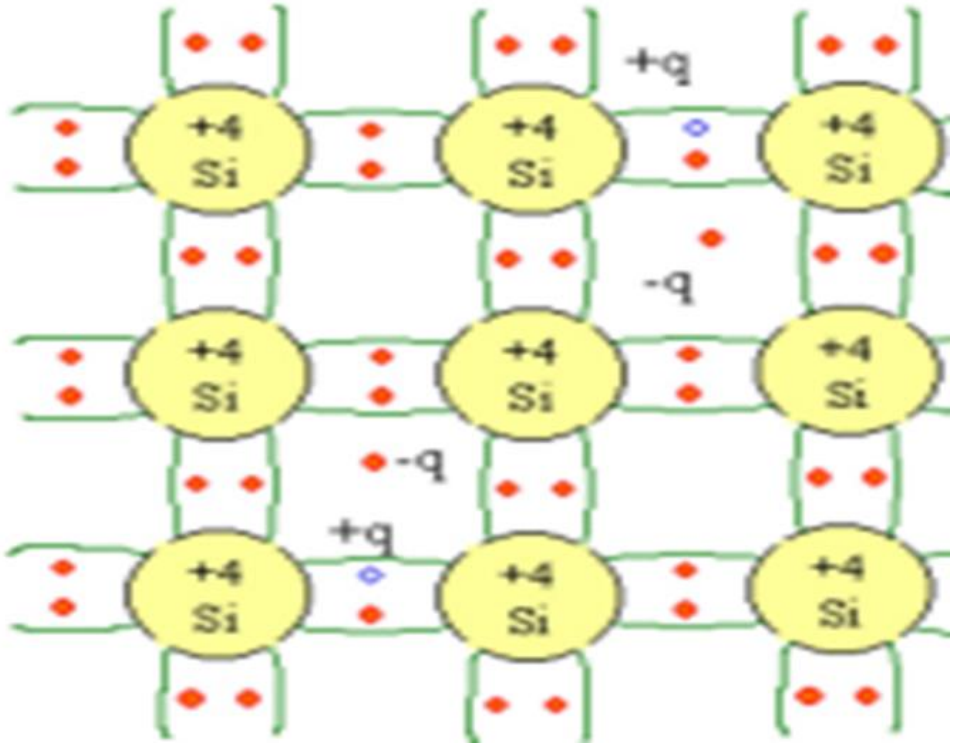


Figure 1.9. Intrinsic semiconductor

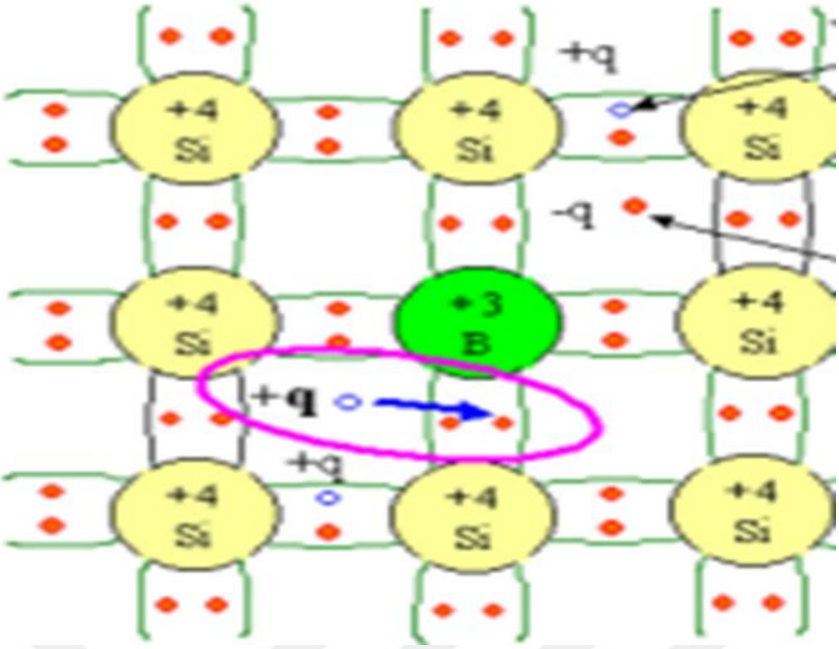
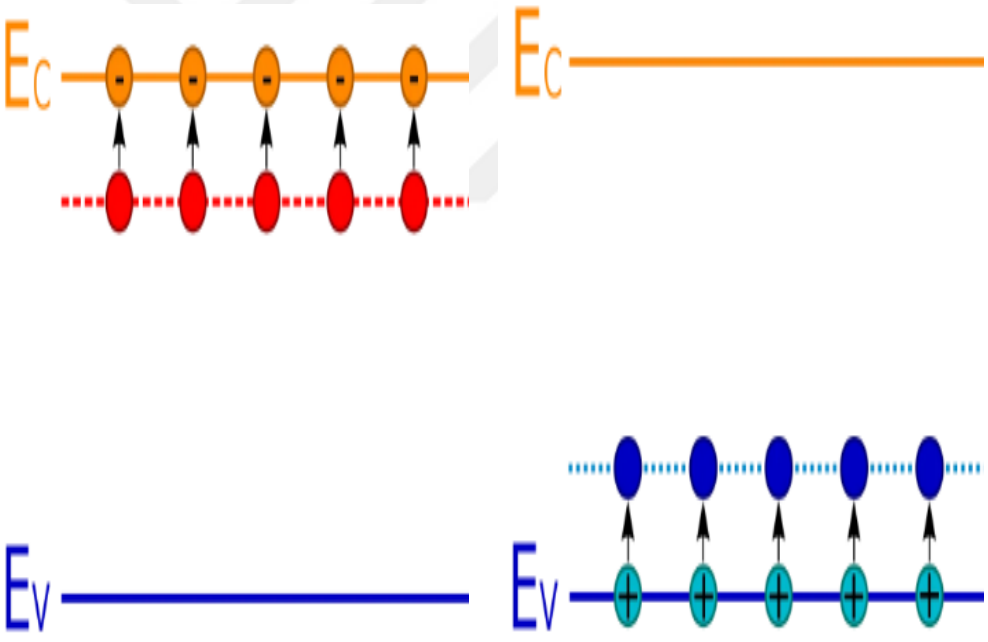


Figure 1.10. p-type semiconductor doped with boron.



(a) (b)

Figure 1.11. a) Fermi energy create with n-type doped and b) Fermi energy create with p-type doped

1.4.3 Importance of the Silicon Carbide in Semiconductor Technology

SiC is an important semiconductor material for medium, high power, high frequency and high temperature electronic applications such as energy conversion

systems and radiation sensors adapted to high temperatures. They present numerous polymorphic forms varying in their crystalline structures. Possessing a wide forbidden energy band, it is renowned for its resistance to radiation and provides a breakdown resistance approximately ten times higher than Si. Therefore, electronic components designed from SiC can have higher losses, for example, low MOSFET structures of SiC have a breakdown voltage of the order of kilovolt while Si is around 1000V. Shifting the threshold voltage SiC devices can be easily irradiated by thermal annealing time is affordable compared to that of Si.

The MOS electrical components obtained from the SiC are important because they allow the join in the world of electronics between the capacity of use of MOSFET and the high controllable powers of gate turn-off thermistor (GTO). The thickness of a SiC slice for a given voltage is almost 10 times lower than silicon because it has the capacity to withstand very high electric fields. As a result, the electrical characteristics, C-V and G-V in such devices are less impacted by impurities at the oxide-semiconductor interface. SiC cannot be melted at negligible temperatures above 2000 ºC to turn into gas.

1.4.4 Ideal Metal-Oxide-Semiconductor Structure

At the beginning of the 20th century, the physics of semiconductors developed in the field of civil and military electronic devices. The MOS capacitor, a very important device, is widely used in the study of semiconductor surfaces. The structure of a MOS capacitor is composed of three different layers, the first layer above is mainly a metallic conductor, the second layer, the one in the middle, is a dielectric called oxide such as samarium oxide (Sm_2O_3) and scandium oxide (Sc_2O_3). The bottom one, is a p-type or n-type monocrystalline semiconductor whose conductivity changes with temperature or doping. The semiconductor is generally used as substrate or wafers. The insulator is deposited on the substrate by different methods such as reactive RF sputtering in a specific environment and a metallic coating is carried out followed by ohmic contacts generally made with aluminum shown in Figure 1.12 (Sze S. and Lee M., Semiconductor Devices, 2007).

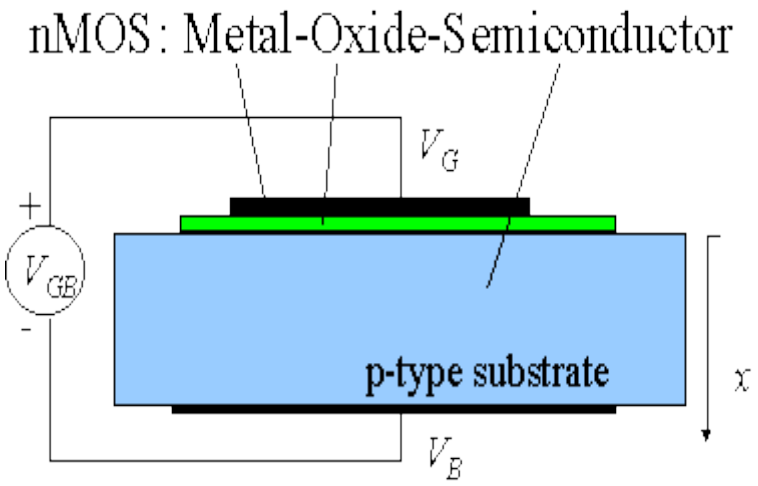


Figure 1.12. Representation of MOS capacitor.

Here, $V_{GB,}$ V_G and V_B are applied, gate and back voltages, respectively.

The MOS structure is represented by the energy band diagram under the conditions of accumulation, depletion and inversion as illustrated in Figure 1.13 where the movement of the charge carriers causes a curvature of the band curve of energies downward for voltages greater than zero and upwards for voltages less than zero. The voltage is positive when the metal is positively biased with respect to the semiconductor and the voltage is negative when the metal is negatively biased with respect to the semiconductor. A MOS capacitor characterized by the fact that at the interface of the metal and the oxide, there are no interface traps and other charges which could cause disturbances in the flow of electrical current, only the charges concerned are those of the semiconductor. Therefore, when the applied voltage is zero, the work function ϕ_{ms}, the difference between the metal work function ϕ_m and the semiconductor function ϕ_s, is zero. The energy band is therefore flat. We have the following relationships for n and p type semiconductors of ϕ_{ms};

$$\phi_{ms} = \phi_m - \phi_s = \phi_m - \left(\chi - \frac{E_g}{2q} - \psi_{Bn}\right) = 0 \quad \text{n-type} \tag{1.14}$$

$$\phi_{ms} = \phi_m - \phi_s = \phi_m - \left(\chi - \frac{E_g}{2q} - \psi_{Bp}\right) = 0 \quad \text{p type} \tag{1.15}$$

where ψ_{Bn} and ψ_{Bp} are Fermi potentiel, ϕ_m work function of metal, ϕ_s work function of semiconductor and E_g energy gap. χ is work function between Fermi and vacuum level.

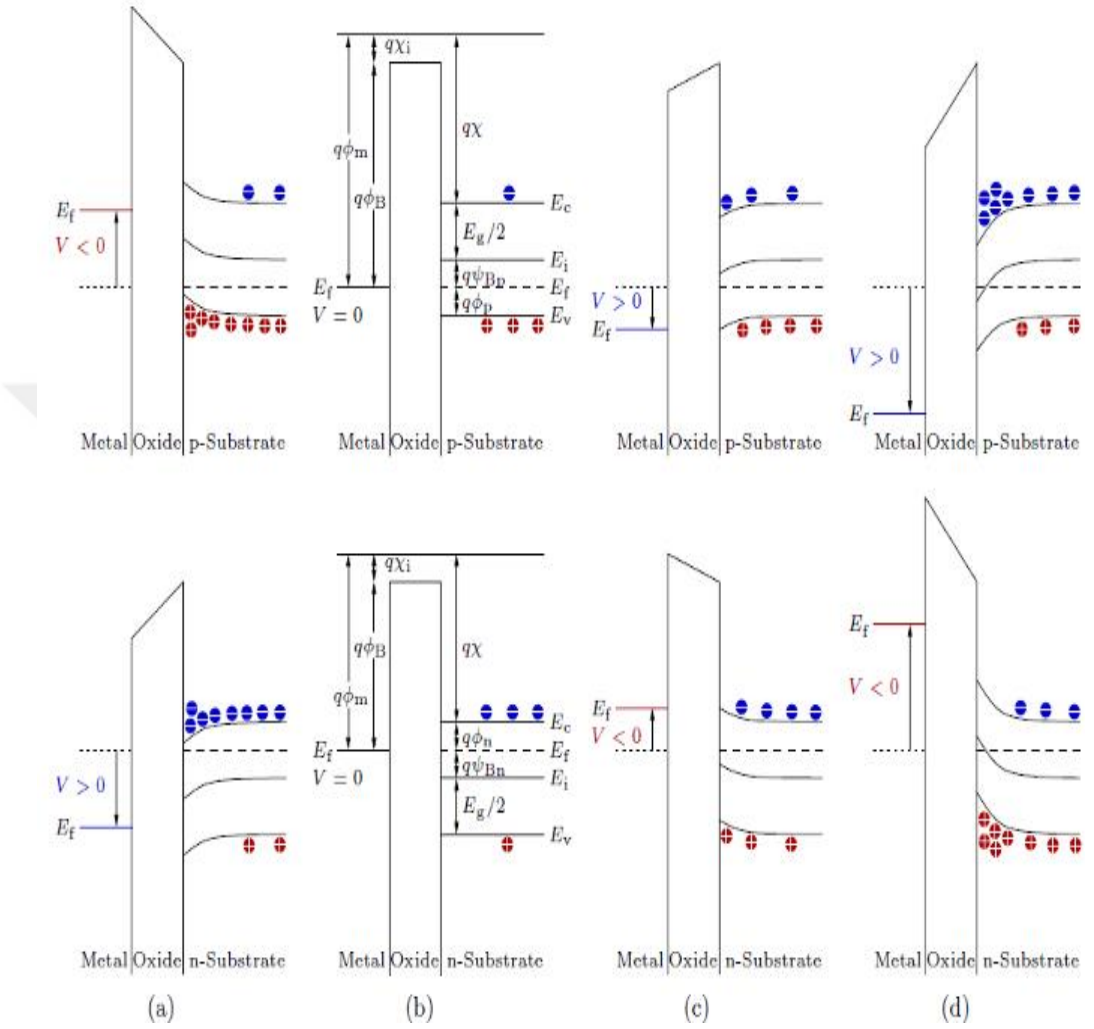


Figure 1.13. Energy band diagrams of MOS

1.4.4.1 Accumulation

When the negative voltage applied is less than the V_G to a MOS capacitor, electric fields are produced inside the oxide that attract positively charged holes from the p-type semiconductor up to the level of the semiconductor-oxide interface on the surface of the substrate. As a result, the capacitor begins to store more and more holes, increasing its density at the surface of the substrate. The electric fields always going in decreasing potentials the semiconductor is therefore positively charged and the metal above the dielectric is negatively charged. In this condition,

the majority concentration of carriers at the surface of the substrate is now higher than the concentration of holes in equilibrium in the substrate: this is the accumulation of carriers. In this region, the capacitance of the capacitor increases and it behaves like a conventional parallel plate capacitor. Its capacity becomes that of the oxide and is given by the following relation:

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_o}{d_{ox}} A \tag{1.16}$$

where ε_o is the vacuum permittivity, d_{ox} the width of the oxide and ε_{ox} the dielectric constant of the oxide. At the interface level, it was observed that the valence band energy and the Fermi energy level decrease. The capacity does not change when the device is in accumulation mode and does not depend on the gate voltage. The frequency being independent if it is low then the Fermi levels close to the surface of the semiconductor will approach at the level of the valence band shown in Figure 1.14.

For a p-type semiconductor, when the applied voltage is less than a flat band voltage, every hole is accumulated near the oxide-semiconductor and interface band as shown in Figure 1.15. This region gets even more positive charges and the potential is linear.

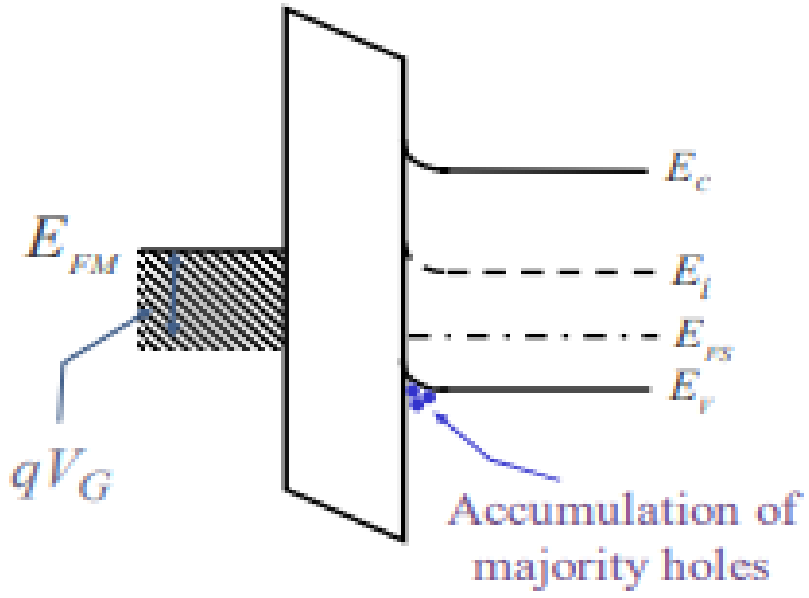


Figure 1.14. Energy band diagram for accumulation for p-type.

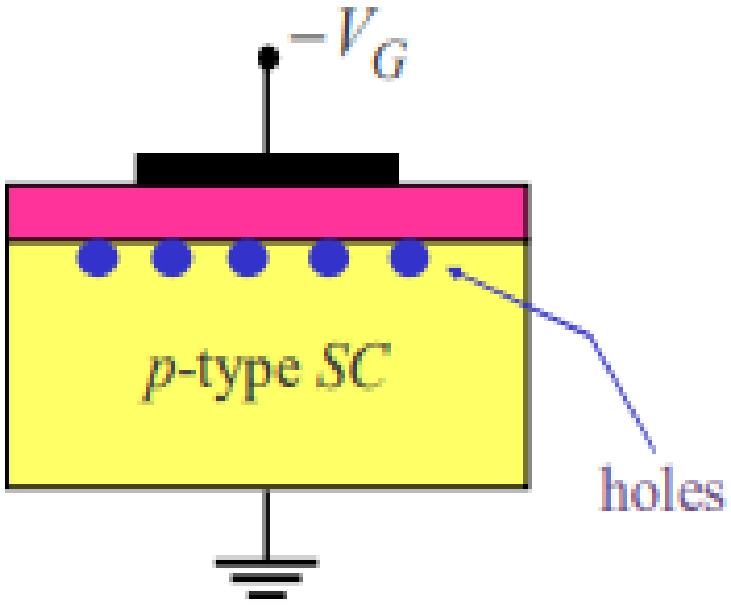


Figure 1.15. Representative of holes in substrate of p-type.

1.4.4.2 Depletion

When a small positive voltage is applied to the gate electrode, electric fields are produced between the metal terminal and the semiconductor terminal from top to bottom following the decreasing potentials, in fact, the metal terminal is positively, and the semiconductor terminal negatively charged. The presence of electric fields moves the majority carriers (holes) from the oxide-semiconductor interface towards the substrate, thus reducing the density of holes at the interface. Regions of space charges are created by containing negatively charged ionized acceptor ions. Its regions are called depletion regions. Note that the concentration increase in the band between the fermi and valence levels causing a downward band curvature between the oxide-semiconductor interfaces as presented in Figure 1.16. If we increase the gate voltage, the depletion region of the capacitor will increase in terms of its width, the capacitance linked to the depletion region, C_d, is added in series to the capacitance across the oxide, $C_{ox,}$ which will result in a decrease in the capacitance between the gate and the substrate. The space charge of the depletion layer acts as another capacitor giving an overall capacitance C by (Nicollian, E., 1986):

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d} \text{ with } \quad C_d = \frac{\varepsilon_o \varepsilon_s}{X_d} A \tag{1.17}$$

Thus

$$C = \left(\frac{1}{C_{ox}} + \frac{X_d}{\epsilon_o \varepsilon_s}\right)^{-1} \tag{1.18}$$

where ε_s is dielectric constant of semiconductor, A area and $X_d$the thickness of the depletion regions. In the depletion region, the surface potential is positive and the curvature of the band goes downwards, the value of $(E_i - E_F)$ having reduced the density of the holes becomes lower than that of the mass in the vicinity of the oxide-semiconductor interface producing a space charge region having stationary charges The space charge density is given by the following equation:

$$Q_{SC} = qN_A^{-1}X_d = Q_A \tag{1.19}$$

where Q_A acceptor of charge load in the unit surface is, $N_A^{-1}$is the ionized acceptor density. Combining equations (1.17 and 1.19)

$$X_d = \sqrt{\frac{2\epsilon_0 K_s \Psi_S}{qN_A}} \tag{1.20}$$

The relation between the applied gate voltage V_G and the total semiconductor potential Ψ_S is:

$$V_G = \Psi_S + \frac{\sqrt{2\varepsilon_0 \varepsilon_s q N_A \Psi_S}}{C_{ox}} \tag{1.21}$$

Only the majority carriers participate in the space free so the capacity depends on the frequency (Sze S. and Lee M., Semiconductor Devices, 2010).

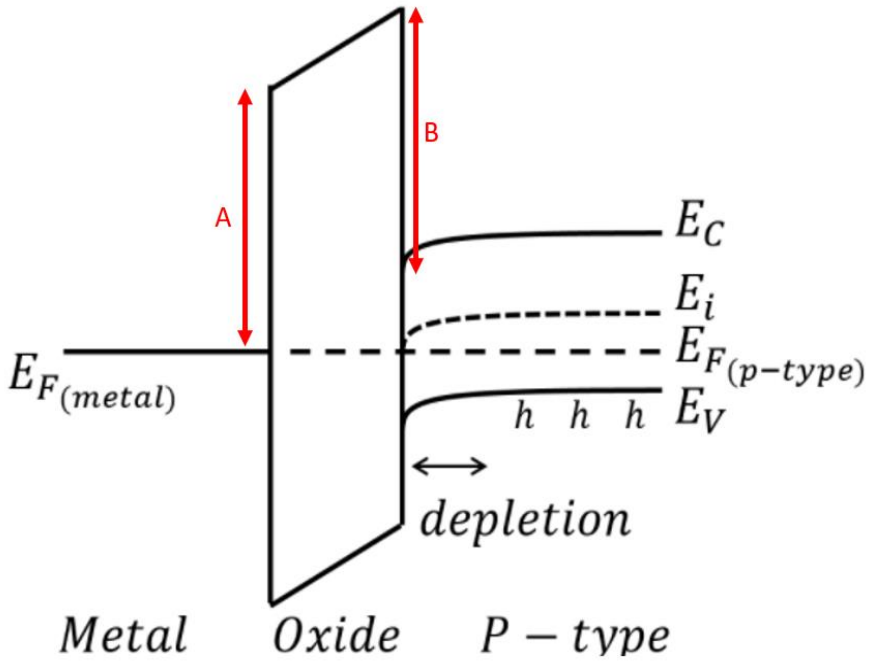


Figure 1.16. Representative of band diagram in depletion region.

Where E_C is conduction band energy, E_V valence band energy, E_F Fermi energy and E_i interface energy for p-type semiconductor.

1.4.4.3 Inversion

When a large V_G is applied to the metal plate and much higher than the threshold voltage, the interface energy level, E_i, falls below the E_F. The minority carriers (electrons) move from the substrate towards the surface of the semiconductor, and the accumulation and depletion regions enlarge as the electron density becomes greater than the density of the holes. An inversion region forms and the energy bands are bent further downwards as well as the Fermi energy which tilts near the conduction band as indicated in Figure1.17. In the case of p-type semiconductors the inversion layer is separated from the substrate by the depletion layer and its thickness is reduced to approximately 2 to 8 nm (Sze,S. M., 1982). The charge of the semiconductor can be written as:

$$Q_{sc} = Q_E + Q_A \tag{1.22}$$

where Q_E is the charge of the electrons in the unit surface in the inversion region and Q_A is the charge of the acceptor in the unit surface.

If the capacitance is measured when the inversion process has started, the electrons will not be able to follow the AC voltage and the variation in the voltage will not change the region of the depletion zone.

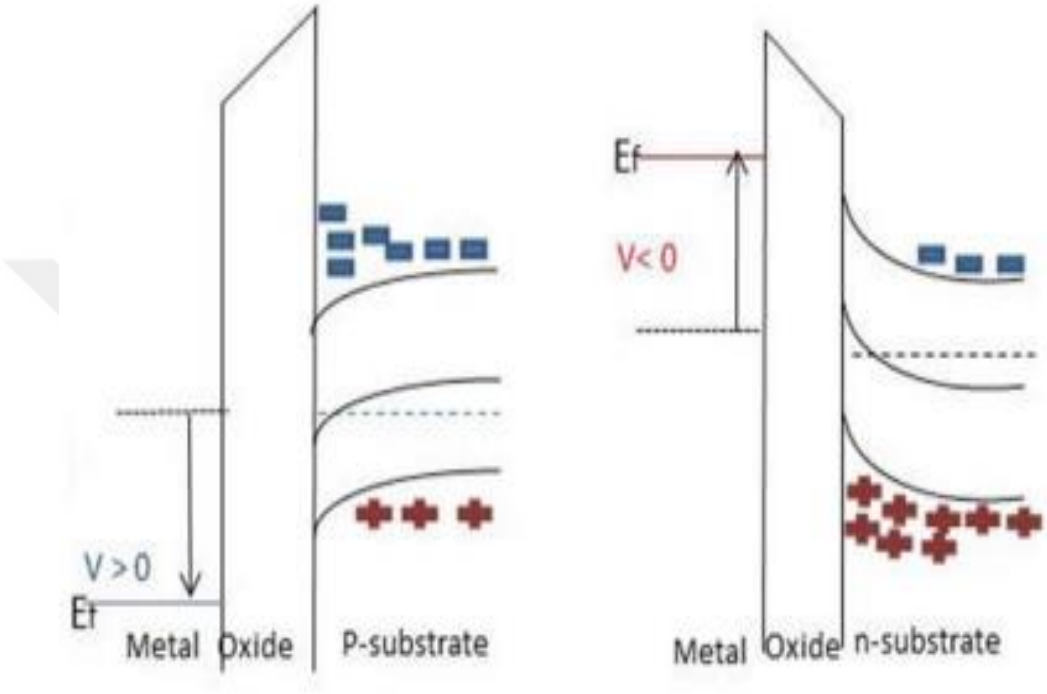


Figure 1.17. Representative of band diagram in inversion region.

1.5 Non-Ideal Metal-Oxide-Semiconductor Structure

Results reveal that the non-ideal MOS structure, no a mobile ionic and space charge at the oxide-interface, is different from the ideal MOS structure. Semiconductor and the oxide layer of the ideal MOS structure or in reality, there are mobile and space charges in the structure because according to elaborate studies in MOS structures, the flat band voltage and the threshold voltage are strongly affected by these charges producing a polarity at the interface. As a result, due to discharges of fixed, mobile, trapped by the oxide and trapped in the interface, the MOS structure gradually deviates from the ideal characteristic of MOS structures (Kaya, Ş.,2014).

1.5.1 Mobile Ionic Charges

Mobile ionic charges denoted Q_m are electrical carriers mainly located at the semiconductor-oxide and oxide-metal interfaces. Under the application of an electric field, these ionic charges move from the metal-oxide interface to the oxide-substrate interface producing an electric current as the charges move in the capacitor. The movement of these charges can lead to a deterioration of the electrical and structural characteristics producing impurities at the interfaces. The density of mobile ionic charges is determined by the equation:

$$Q_m = \triangle V_{FB} C_{ox} \tag{1.23}$$

where $\triangle V_{FB}$is flat band shift and C_{ox} oxide capacitance.

1.5.2 Fixed Oxide Charges

Fixed oxide charges are located in the dielectric and the oxide-semiconductor interface. These are charges that cannot move even under the effect of an electric field. Its charges being positive can have an influence on the electric current circulating in the oxide and the electrical and structural characteristics of the MOS device modifying the C-V towards more negative voltages than the ideal MOS structure and the ideal structure for the p-type capacitor.

1.5.3 Interface Trapped Charges

At the oxide-semiconductor interface, it is obtained that structural defects and metallic impurities cause radiation which produce interface traps interacting with the conduction band by trapping or releasing electrons and with the valence band by trapping or by freeing holes. The interface states behave like an acceptor by capturing electrons and also behave like an emitter by releasing electrons. They then become negatively and positively charged, respectively. The trap charges in the interface Q_{it} can shift the C-V curves towards negative and positive voltages depending on the type of trap charges varying with the frequency of the applied voltage.

1.5.4 Oxide Trapped Charges

The multitude of structural, metallic defects or ionization defects produce charge traps in the dielectric, thus blocking mobile charges and having an effect on the circulation of electric current in the oxide level. These oxide traps can be mobile traps in the oxide of symbol, Q_{ot}, and are also exchange charges between the oxide and the substrate at the interface and increase the charge density in the MOS structure. These charges can be positive or negative depending on the nature of the oxide but are most often positive charges influencing the C-V by moving them slightly due to the increase in positive charges in the oxide. The sum of all the oxide charges Q_{eff} is given by the following relation:

$$Q_{eff}=Q_f+Q_m+Q_{ot} \tag{1.24}$$

where Q_f, Q_m and Q_{ot} are fixed oxide charge, mobile ionic charge and oxide trapped charge, respectively.

1.6 Investigation of Interface and Oxide State Density in MOS Devices

In MOS structures, the presence of insulating fillers, interfacial traps and any other waste at the oxide-substrate interfaces can negatively affect the various characteristics of the ideal MOS structure because the presence of a single defect whether it is any atom, the degradation of the oxide, a deformation of any type produce new energy levels located mainly in the forbidden energy band called surface states composed of two kinds of surface state called: States fast surface and slow surface conditions. The density of its new energy levels varies between $10^{10}$and $10^{20}cm^{-2}$. Slow surface states in principle have no effect on the MOS device because being relieved by the thermal effects of oxidation, they most often migrate to the dielectric level through the channel of moving charge carriers which are located at the metal - dielectric interface. Fast surface states, on the other hand, have an effect in the structure because by having an upward and downward movement of charge at the Fermi level, there is consequently an exchange of charge between the valence and the conduction band. They are located at the oxide-semiconductor interface. These surface conditions can create a curvature of the semiconductor band and for reasons of efficiency of the characteristics of the MOS structure they can be treated using efficient thermal methods. The density of these

surface states can be studied and determined using two methods including the capacitance and the conductance method. The distribution function for interface traps is given by the following relations: (Omar. M., 1994)

$$f_D(E_t) = \frac{1}{1+g(E)\exp(\frac{E_F-E_t}{kT})} \text{ for all donor interface traps} \quad (1.25)$$

and

$$f_A(E_t) = \frac{1}{1+g(E)\exp\left(\frac{E_t-E_F}{kT}\right)} \text{ for all acceptors interface traps} \quad (1.26)$$

with $g(E) = \frac{1}{2\pi^2}\left(\frac{2m^*}{h^2}\right)^{\frac{3}{2}}(E_t - E)^{1/2}$, g(E) is the density of state for electrons or holes in the energy band and E_t is the interface trap level energy at the top of valence band, E_F is the Fermi energy.

1.6.1 Capacitance Methods

In the MOS structure, the density of interface traps using two capacitance methods, namely low frequency capacitance (C_{LF}) and high frequency capacitance (C_{HF}) can be determined. The low frequency capacitance maintains thermal stability at the interface and this balance is determined by the difference in charges on the voltage difference. At low frequency, the minority carriers do not have the possibility of increasing their concentration. The low frequency capacitance is confused in this case with the capacitance of the oxide. High frequency capacitance is a measurement of high frequency signal gradually varying the corresponding the C-V. It corresponds to the variation of loads at the level of the inversion and depletion zones of the MOS structure. At high frequencies, interface states cannot follow the applied voltage. Note that the C-V characteristics will always move according to the majority carriers in the interface, negative if they are electrons and positive if they are holes. The distribution of interface traps (N_s) can be determined by combining the high and low frequency capacitance using the equivalent capacitance circuit (ECCM) method as demonstrated in Figure 1.18 (Kaya, Ş., 2015).

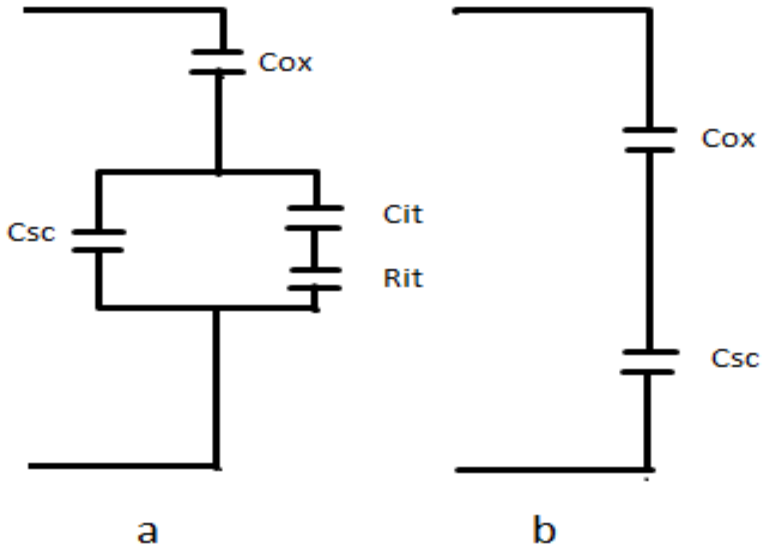


Figure 1.18: Equivalent capacitance circuit method: a) low frequency capacitance and b) high frequency capacitance.

At low frequency, the capacitance of the oxide C_{ox} and the capacitance of the interface states C_{it} are in parallel and the capacitance of the space charges C_{sc} according to the equation bellow (Kaya. Şenol and Lok. R, 2013)

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - C_{sc} \tag{1.27}$$

At high frequency, the capacitance is in series with the oxide capacitance C_{ox} and the space charge capacitance C_{sc}

$$C_{HF} = \frac{C_{ox}C_{sc}}{C_{ox}+C_{sc}} \tag{1.28}$$

The combination of interface traps by combining the two previous equations:

$$qAN_s = C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \tag{1.29}$$

1.6.2 Conductance Methods

Conductance is a technique used to study properly oxide-semiconductor interface. It measures directly the loss of energy during emission and capture of majority carrier in interface between interface trap level and conduction band for any applied voltages. This loss of energy is observed at low frequencies. The

conductance methods allow us to determine the density of the surface state and its distribution. At high frequency, there is a rapid change in the Fermi level until the energy loss becomes zero. At some point, a phase shift occurs between the interface state and the applied signal, consequently causing a transfer of electrons from higher energy states to lower states.

The relation between interface state and conductance is given by following formula:

$$\frac{G}{\omega} = \frac{AqD_{it}\ln(1+\omega^2\tau^2)}{2\omega\tau} \tag{1.30}$$

where D_{it} is interface state density, q electrical charge, τ time constant of interface state and ω angular frequency.

2. MATERIALS AND METHOD

2.1. Cleaning Process of Wafers

The manufacturing of very high-quality MOS devices requires rigorous cleaning of the SiC wafer in order to eliminate any kind of pollution and contaminations on the substrate because the presence of these can lead to the deterioration of the MOS device performance of the electrical properties of the SiC capacitor. Therefore, the international Radio Corporation of America (RCA) cleaning procedure was carried out to clean the SiC substrate in the ultrasonic bath inside at NURDAM as shown in Figure 2.1.

Firstly, the substrate was cleaned in a mixture of methyl alcohol and trichloroethylene (CH3OH +C2HCl3) in two phases for 3 minutes each and then washed with demineralized water (DIW) in an ultrasonic bath. Secondly, the substrate was cleaned in another mixture of hydrogen peroxide and sulfuric (H2O2+H2SO4) in three phases for 5 minutes in order to eliminate any residue of organic matter on the substrate and then cleaned with DIW to remove the chemical mixture of peroxide and sulfuric. Finally, a solution of nitrite acid, hydrofluoric acid and peroxide was used on the substrate and cleaned with DIW for 5 minutes.

At the end of cleaning, N_2 was used to dry the substrates so as not to leave any liquid substances on them.

Figure 2.1. RCA cleaning process at NURDAM.

2.2 Fabrication of Sc_2O_3 MOS Capacitor

In this study, thickness of 5nm of SiO_2 was grown on a cleaned substrate of n-type SiC by dry oxidation method to prevent any current leakage mechanism at 1000°C under oxygen atmosphere. This step is very important to start manufacturing devices. After SiO_2 grew, Sc_2O_3 was deposited on SiC (100) substrate using e-beam evaporation with a width of 130 nm under a pressure of 10^{-9} torr. e-beam evaporation is a good technique to make thin film with a good precision, versatility and high melting point and minimize damage on the substrate. e-beam is generated by electron channels by thermionic emission and accelerated by an electric field and directed at high speed onto the scandium oxide. This kinetic energy is transformed into thermal energy which systematically increases the temperature of the oxide until the materials evaporate and are deposited on the substrate as depicted in Figure 2.2. The thicknesses of thin films were measured by Spectroscopic ellipsometry.

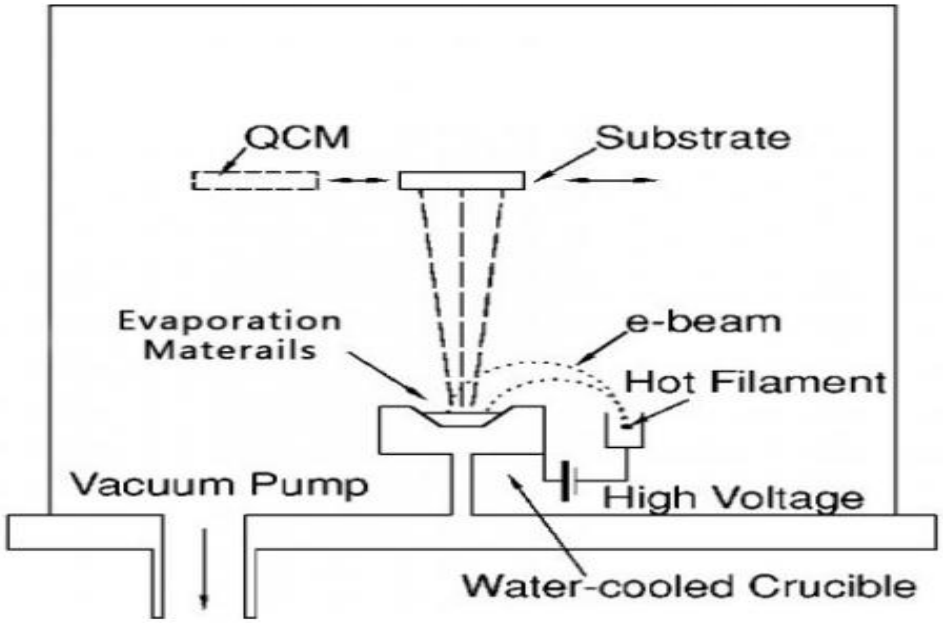


Figure 2.2.e-beam evaporation system

The evaporated thin films samples were divided into two groups. The first group were annealed at 400°C, 600°C, 800°C and 1000°C for one hour under N_2 ambient at atmospheric pressure and the second group were kept as-deposited as presented. The contacts of aluminum were evaporated by thermal evaporation techniques shown in Figure 2.4

Figure 2.3. Annealing process at NURDAM.

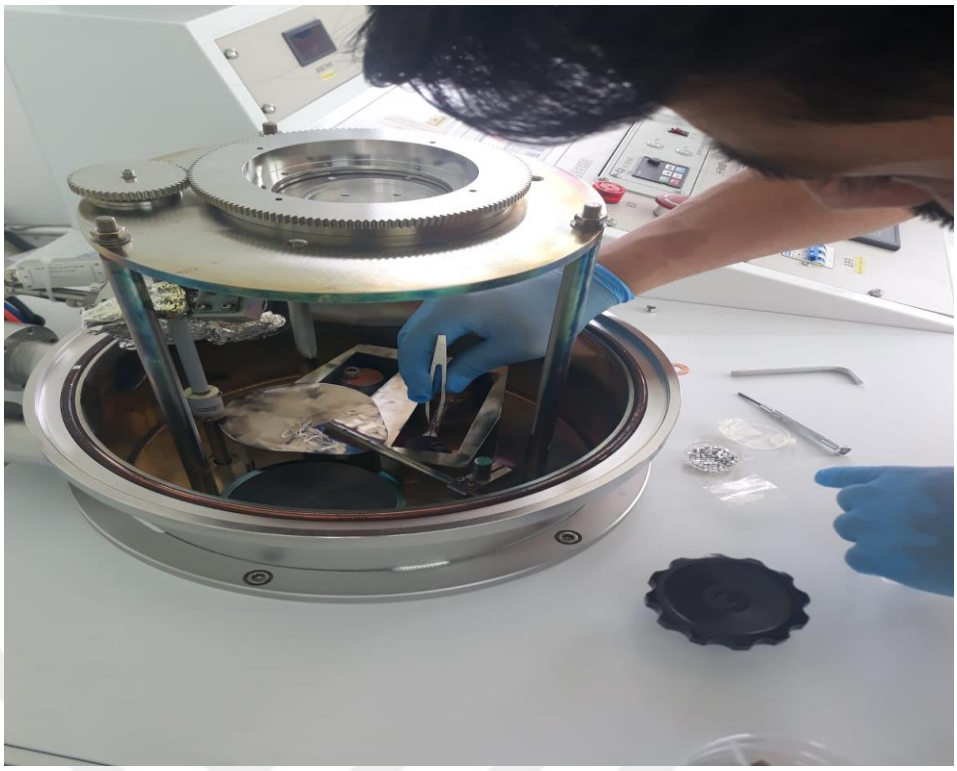


Figure 2.4. Thermal evaporation system at NURDAM.

2.3 Structural and Electrical Characterizations of Sc_2O_3 MOS Capacitor

2.3.1 XRD Measurements

X-ray Diffraction (XRD) is a main technique used to find or to examine the structure of crystalline structure of materials. The work of XRD is based on incident beam x-ray to diffract towards any directions on material. This technique provides precise measurements like orientation of single crystal, average distance between layers, sizes shapes, crystal structures and internal stresses. The measurements on Sc_2O_3thin film was carried out by a Rigaku Miniflex X-ray diffractometer system with CuKα, as shown in Figure 2.5, in the range 20°– 60° at a scan speed of 3°/min and a step increment of 0.02° at room temperature.

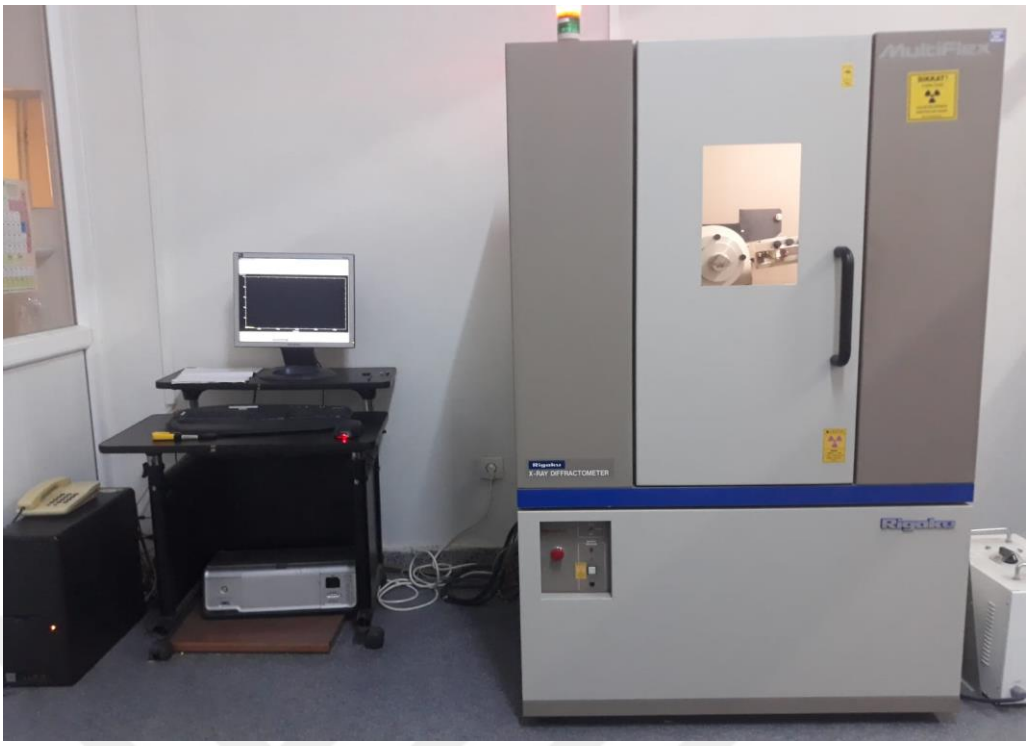


Figure 2.5. Rigaku Multiflex X-Ray Diffractometer in Physics laboratory.

2.3.2 C-V Measurements

Electrical properties of MOS capacitor are obtained by a shift of parameters like leakage current, capacitance and conductance in a mid-gap and flat-band regions. To analyze capacitance-voltage (C-V), we study the shift of semiconductor-oxide interface, density of oxide trapped charge and mobile ionic charge. Interface state density is result from flat band voltage changing and don't change at mid-gap. C-V and G/ω-V measurements were performed at 100 kHz for as-deposited and annealed samples at room temperature. The C-V and G/ω-V characteristics were measured by probe station Keithley 4200SCS located in NURDAM as presented in Figure 2.6.

2.3.3 G/ω-V Measurements

The conductance measurement can early see in a depletion region because the emission of minority's carrier is very low to be considered and doesn't contribute. However, in depletion region, interface trap shifted by capture and emission of majority carriers. So, G/ω-V measurements extract interface trap level density. In G/ω-V measurement silicon surface band bending is obtained as a function of gate from a measurement of charge on the MOS capacitor (Nicollian,

E. 1986) this band bending gives interface trap density probability, energy scale and delineate accumulation, depletion, weak inversion and strong inversion.

G/w-V measurements were performed at 100 kHz for as-deposited and annealed samples at room temperature. The G/w-V parameters were also examined by probe station Keithley 4200 SCS located in Nuclear Radiation Detector Center as presented in Figure 2.6 bellow.

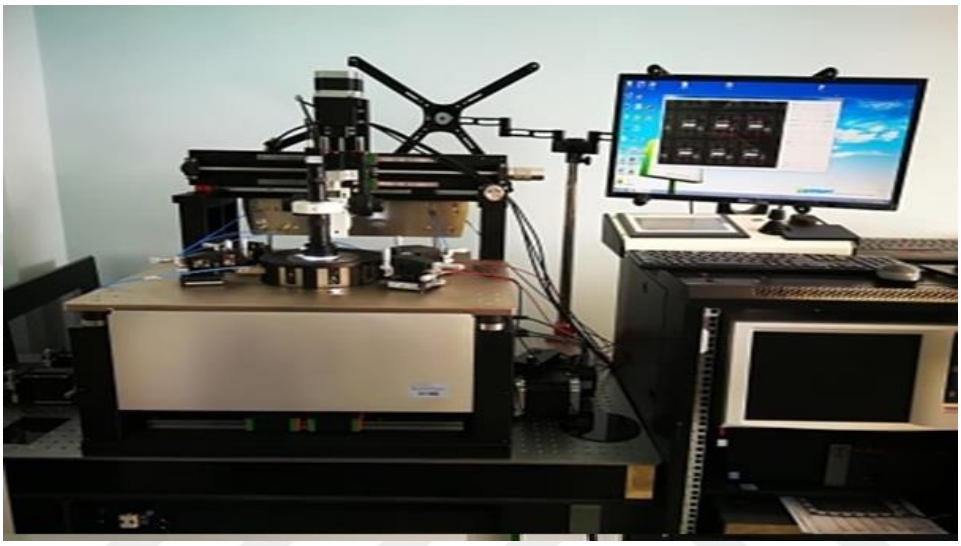


Figure 2.6. Probe station Keithley 4200 SCS at NURDAM.

3. RESULTS

3.1 Microstructural Analysis

In this work, in order to confirm the cubic crystal structure and to compute the lattice parameters, grain size, lattice strain and dislocation density of the thin films, XRD measurements were performed on the Sc_2O_3 films grown on (100) n-SiC substrates annealed at 400, 600, 800 and 1000 ˚C for a frequency of 100 kHz. The XRD patterns of the Sc_2O_3 films were illustrated in Figure3.1. Diffraction patterns of the films were indexed via International Centre for Diffraction Data (ICDD) database, demonstrating a strong correlation with 76-0179 ICDD card number which is the cubic phase of Sc_2O_3 with (222) preferred orientation. The peaks existing at 2θ = 22.223, 31.632, 36.686, 43.312, 52.855 and 62.918˚ corresponded to the (211), (222), (400), (322), (440) and (622) planes of the cubic structure of Sc_2O_3. No further peaks were appeared, an indication that this is the only crystallite phase. The agreement of the obtained pattern with the typical diffraction pattern of the cubic Sc_2O_3 suggests that no preferential direction in the polycrystalline growth was observed (P.C., Papillion, E., Andrés, E. S., Lucía, M.L., 2012).

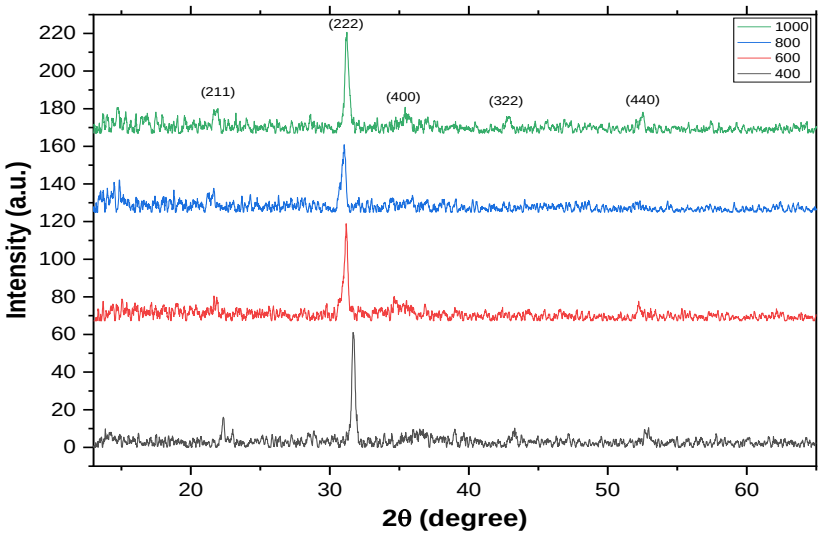


Figure 3.1. XRD patterns of Sc_2O_3/SiO_2 thin films annealed for 400, 600, 800 and 1000 °C at 100 kHz.

3.2 Analysis of Electrical Measurements

In order to improve or enhance the performance of MOS capacitors, their electrical properties need to be analyzed well. The aim of this study is to examine the effect of interface levels and series resistance (R_s) on the electrical characteristics of the Sc_2O_3 MOS capacitor depending on the annealing temperatures. Despite quite a few reports of pressure, frequency (Kahraman, A., Yılmaz, E.,2018), substrate temperature and interfacial layer (Castán,H., Dueñas,S., Gómez, A, 2011) dependent behavior of Sc_2O_3 grown on Si substrate in the available literature, to the best of our knowledge, no reports have been published on the analyzing structural and electrical characteristic of the Sc_2O_3 grown on SiC substrates annealed at different temperatures. In this sub-section, electrical properties were studied performing C-V and G-V measurements for different annealing temperatures at 100 kHz and the resulting graph was plotted in Figures3.2 and 3.3, respectively.

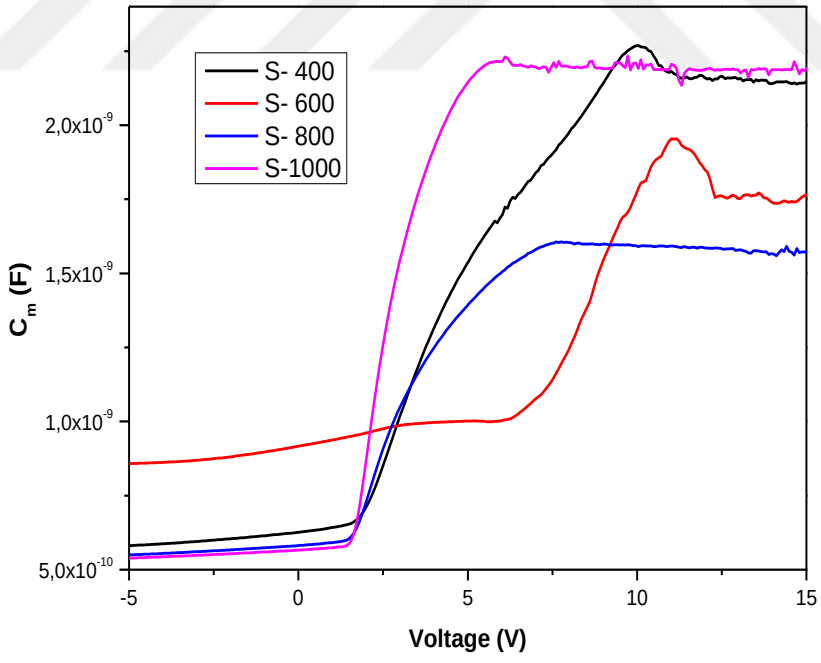


Figure 3.2. Capacitance as a function of voltage graph of MOS capacitors for different annealing temperatures.

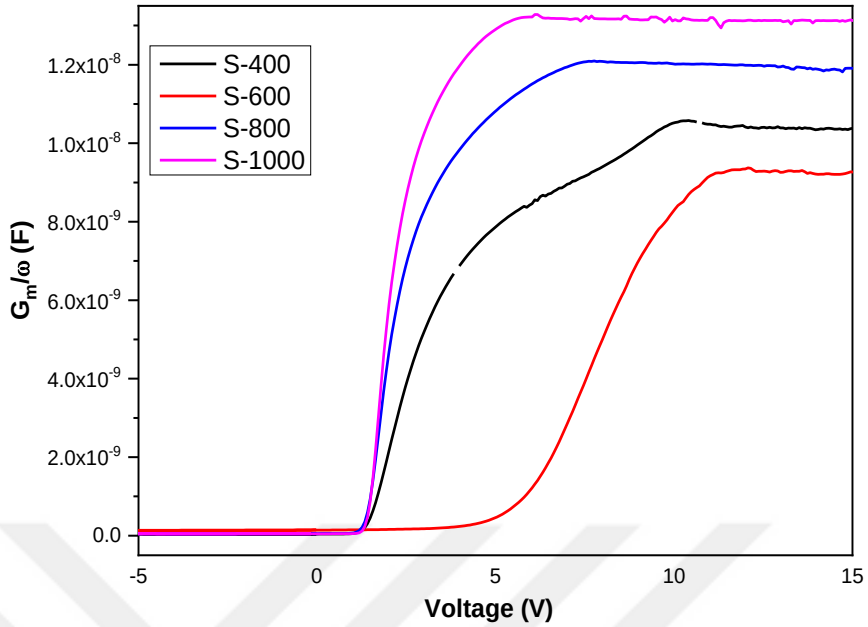


Figure 3.3. Conductance as a function of voltage graph of MOS capacitors for different annealing temperatures.

4. DISCUSSION

4.1 Microstructural Analysis

Lattice parameters of the films were calculated using the (222) peak and by the following equation for cubic structure

$$1/d^2_{(hkl)} = (h^2+k^2+l^2)/ a^2. \quad (4.1)$$

Here, $d_{(hkl)}$ and a are the distance between atomic layers and lattice parameter, $a=b=c$, respectively. The calculated values of lattice parameter a were tabulated in Table 4.1. As seen from the table, lattice parameters were found to be 9.769, 9.932, 9.962 and 9.921Å for annealed films at 400, 600, 800 and 1000°C, respectively. These results indicated that the values of lattice parameter increased with increasing the annealing temperatures, except for 1000 °C annealed film. This indication is due to the peak intensity shifting towards small angles as the annealing temperature increased, as expected. The indexed peaks were also consistent with literatures (Liu, G., Jin, Y., He, H., Fan, Z., 2010).

An accurate calculation of the grain size is difficult to accomplish, but the annealing-induced distribution of the (222) peaks facilitate calculation of the crystallite size (D) of the films using the Debye-Scherrer's formula (Cullity, B. D., 2019)

$$D = 0.9\lambda/\beta \cos\theta \quad (4.2)$$

where λ is the wavelength of the incident x-ray (1.5406 Å) and β, in radians, is the full width at half maximum (FWHM) of the (222) peak at 2θ. The values of FWHM were determined from the XRD pattern simulation. The crystallite size is assumed to be the size of a coherently diffracting domain and it is not necessarily the same as particle size. The extracted crystallite sizes were tabulated in Table 4.1. The values of crystallite size decreased while the lattice parameter increased as

increasing the annealing temperature was observed except annealed at 1000ºC. As seen from the table, the extracted crystallite sizes ranged from 309 to 249 Å.

The lattice strain (*S*) of the films was calculated using the following relation (Tiwari, S., Choudhary, R. J., Prakash, R., and Phase, D. M. 2007)

$$S = [((\lambda /D\cos\theta) - \beta)/\tan\theta] \quad (4.3)$$

Table 4.1. Some structural parameters for the films

Samples	**2θ (degree)**	**Crystallite size (Å)**	**Lattice strain X 10^{-3}**	**Lattice Parameter (Å)**
S-400	31.672	309.22	1.825	9.769
S-600	31.175	255.35	2.010	9.932
S-800	31.258	209.91	4.416	9.962
S-1000	31.219	249.63	3.334	9.921

The diffraction peak shape is related to crystallite size and the crystallite size is related to lattice strain. The lattice strain is a measure of the lattice distortion. The smaller the lattice strain, the greater is the crystallite size. The results were presented in Table 4.1. It was observed that the lattice parameter and strain increased while the crystallite size decreased with increasing the annealing temperature.

The dislocation density, δ, which represents the number of defects in the sample is defined as the length of dislocation lines per unit volume of the crystal and is calculated using the Equation (Saleem, M., Fang, L., 2012).

$$\delta = 1/D^2 \quad (4.4)$$

where D is the crystallite size as defined before. The calculated values with respect to annealing temperature ranged from $1.046x10^{-5}$ to $1.604x10^{-7}$ $(Å)^{-2}$. The smaller the dislocation density, the greater is the crystallite size was observed.

In order to discuss the influence of increasing annealing temperature on the microstructure properties, the observations that crystallite size decreases while lattice parameter and lattice strain increase have some implications:

1. Increasing the annealing temperature typically enhances recrystallization processes. At higher temperatures, atoms have more mobility, which allows for the rearrangement of dislocations and the formation of new strain-free grains. However, in some cases, the process may lead to the growth of smaller grains as they complete for available volume, resulting in a net decrease in crystallite size for certain condition. The increase in annealing temperature can facilitate dynamic recovery processes, while stored energy in the films (from dislocations) is released, leading to smaller and more stable grain formations (Barad,C., Kimmel,G., 2020).
2. Higher temperatures can cause thermal expansion, leading to an increase in the lattice parameter. As temperature rises, the atoms vibrate more vigorously, causing the average distance between them to increase. If the material contains impurities, these can also affect the lattice parameter (Liu,G., Jin,Y., He,H., Fan,Z, 2010).
3. As crystallite size decreases, the number of grain boundaries increases. Grain boundaries can be a source of strain due to differences in orientation between adjacent grains. If the films are experiencing stressor other forms of mechanical loading, this could contribute to increased lattice strain. Moreover, if the materials undergo any phase transformation at higher temperatures, such transformations can lead to changes in the lattice structure and associated strains (Kumar,S., Prakash,R., 2017)

In summary, the observation that crystallite size decreased while lattice parameter and strain increased with higher annealing temperatures indicated a complex interplay of thermally activated processes such as recrystallization, thermal expansion, and the behavior of defects with in the film. These changes can significantly affect the mechanical and physical properties of the films, potentially

leading to enhanced performance in certain applications, as will be discussed in investigation of electrical characteristics. At 1000ºC, there is a trend in crystallite size, lattice parameters and lattice strain as increasing annealing temperature except annealed at 1000ºC sample. This deviation is attributed to the Sc_2O_3 diffusion into SiO_2.

4.2 Analysis of Electrical Measurements

It was obtained that the annealing temperature affected the electrical properties of the films. Moreover, in all capacitance with respect to voltage curves, three well-known regions called accumulation, depletion, and inversion was observed. A shift to the positive voltages in the C–V characteristics was observed, which is indication of the presence of surface states. Dielectric constant of the gate oxide layer (Sc_2O_3) can be computed from the C-V measurements for 100 kHz using the following formula:

$$C_{ox} = (\varepsilon_0 \varepsilon A)/d \tag{4.5}$$

where ε_0 and ε are permittivity of free space and dielectric constant, respectively. *A*is the contact area of metal aluminum, *d* thickness of the gate oxide layer and C_{ox} oxide capacitance are 1.571×10^{-6} m^2, 120×10^{-9} m and 1.650×10^{-9} F for annealed film at 800 °C, respectively. From these data, the calculated dielectric constant was found to be 13.87 which is greater than the previously calculated value of 10.9 but less than 14 (Wang,X., Saadat,O.I., Xi,B., Lou,X., Molnar,R.J., Palacios,T., and Gordon,R.G., 2012) for Sc_2O_3 MOS capacitor.

On the other hand, a similar variation in the G/ω as a function of voltage measurements was observed as seen in Figure 3.3. However, as shown in the figure, the conductance peaks are not distinctly formed. Conductance reflects the losses caused by the exchange of majority carriers between the interface states and the majority carrier band of the semiconductor (Serway, A. 2008 and Hajji,R., 2015), typically showing a peak at the depletion edge. The non-ideal behavior observed may be attributed to factors such as oxide defects, interface states, and series resistance (] Hajji,R. 2015). Depending on series resistance and the surface states densities particularly time-dependent states, i.e., interface states, the electrical characteristics of MOS devices deviate from their expected ideal behaviors

(Bulbul,M. M. and Zeyrek,S. 2006 and Kaya, S., Lok,R., Aktag,A.,Seidel,J., and Yilmaz,E. 2014).

In order to eliminate series resistance (R_s) effect and remove the parasitic effects from the electrical measurements, correction was performed using the Nicollian method (Nicollian,E., and Aitken,R.,1986), and the R_s values can be calculated

$$R_s = \frac{G_m}{G_m{}^2+(\omega C_m)^2} \tag{4.6}$$

RR

where $\omega = 2\pi f$ is the angular frequency, C_m and G_m the measured capacitance and conductance in the strong accumulation region, respectively. The annealing temperature dependent R_s values of the Sc_2O_3 films at a frequency of 100 kHz were extracted and tabulated in Table 4.2. The calculated R_s values as a function of temperature have no trend, that is, they vary randomly, which is an indication of reordering and restructuring effects is caused by the applied voltages at different annealing temperatures (Nicollian,E., and Aitken,R., 1986). The corrected capacitance and conductance values can be calculated following equations, respectively (Sze,S. M., 1982);

$$C_C = \frac{\left[(G_m)^2 + (\omega C_m)^2\right]C_m}{a^2 + (\omega C_m)^2} \tag{4.7}$$

and

$$G_C = \frac{\left[(G_m)^2 + (\omega C_m)^2\right]a}{a^2 + (\omega C_m)^2} \tag{4.8}$$

where $a = (G_m) - \left[(G_m)^2 + (\omega C_m)^2\right]R_s$ and the rest of the quantities in equations (4.7 and 4.8) were defined before. The C_c-V and G_c/ω –V curves were plotted in Figures 4.1 and 4.2, respectively. When compared C_c with C_m in the accumulation region, it was obtained that the value of C_c substantially increased due to series resistance correction, but S-800 sample showed the highest increase. The rise in the C_c value for the S-800 sample may be due to the formation of Sc-Si-O bonds, where carbon-related defects emerge during high-temperature annealing. At low

frequencies, interface states can follow the AC signal and contribute to capacitance. At high frequencies, however, interface states cannot follow the AC signal, and their contribution to capacitance becomes negligible **(**Nicollian E.H., Brews J.R., 1982 and Kar S., Dahlke W. E.,1972).

In this study, the capacitance was measured at a low frequency (100 kHz), which is why the contribution to capacitance is quite significant. Here, it was seen that the R_s is also effective for both capacitance and conductance characteristics of Sic based MOS devices. It should be particularly taken in account for the capacitance and conductance curves.

As G_c/ω compared with G_m/ω in the accumulation region, the corrected conductivity value also rose considerably and the expected peaks were observed at the depletion edge, which is expected in MOS devices after applying series resistance corrections. The existence of the peaks in the corresponding depletion region verifies the interaction between interface states and majority carriers (Kaya, S. 2014 and Tugluoglu, N, 2017) It was observed that the maximum values of peaks in G_c/ω -V curves were in the sample annealed at 800°C.

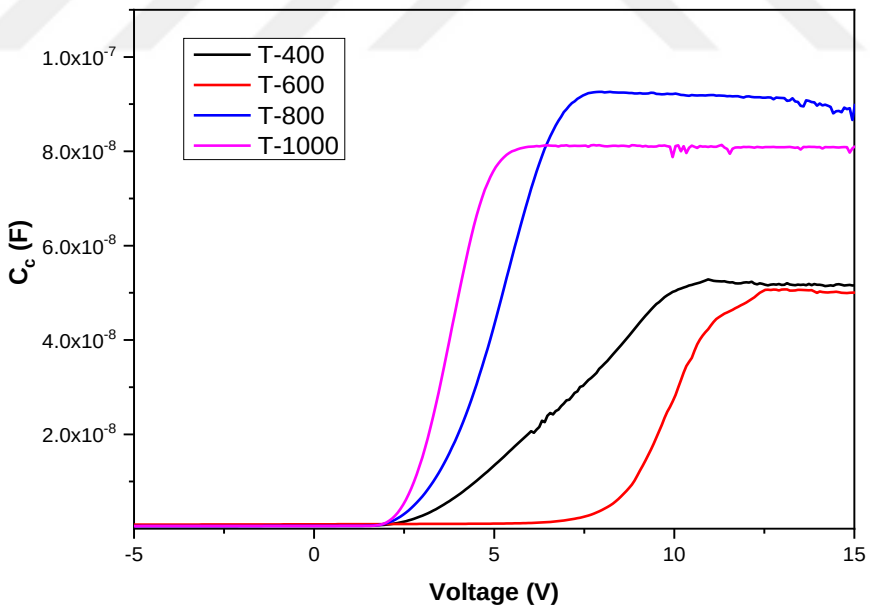


Figure 4.1. Characteristics of corrected capacitance as a function of voltage graph for different annealing temperatures of the films.

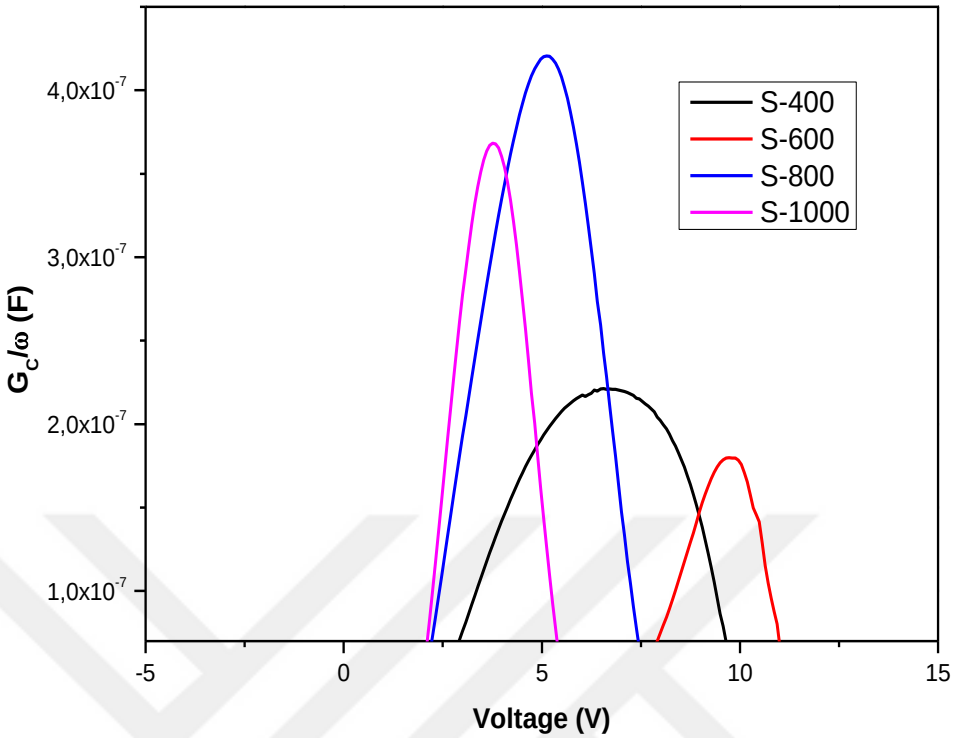


Figure 4.2. Characteristics of corrected conductance as a function of voltage graph for different annealing temperatures of the films

The flat band voltage (V_{fb}) values can be obtained from the curves where the curve starts linear behavior shown in Figure 4.1. We observed a difference in V_{fb} for different annealed samples, which is due to the presence of oxide state density (N_{eff}) in the thin films (Quah, H.J., and Cheong, K.Y. 2012).Using equations (5.8 and 5.9) (Kaya,S., Yilmaz,E., Aktag,A., and Seidel,J,2015), the effective oxide state densities (N_{eff}) and effective charge (Q_{eff}) can be calculated by utilizing the C_c-V curves, respectively;

$$V_{fb} = \Phi_{ms} - \frac{Q_{eff}}{C_{ox}} \quad (4.9)$$

$$Q_{eff} = qAN_{eff} \quad (4.10)$$

where Φ_{ms} work function difference between SiC and Al, C_{ox} in the oxide capacitance, q is the electrical charge and A is the contact area of capacitor. The calculated N_{eff} values as a function of annealing temperature were listed in Table 4.2. It was observed that the value decreased with rising the annealing temperature

up to 800 °C. Up to 800°C, the annealing process resulted in an improvement in oxide defects within the Sc_2O_3 film, likely due to the healing of oxygen vacancies and reorganization of the film structure. However, when the annealing temperature reached 1000°C, an increase in oxide traps was observed. This could be attributed to the onset of thermal degradation of the oxide material, leading to increased stress and defects at the oxide-substrate interface. Additionally, higher annealing temperatures may cause annoying reactions or diffusion of carbon or silicon impurities from SiC wafer, which could introduce more trap sites and degrade the electrical properties of the films.

Table 4.2. Some electric characteristics of $Sc_2O_3/SiO_2/SiC$ MOS capacitor

Sample	**R_s (Ω)**	**C_c x10^{-08} (F)**	**G_c/ω X10^{-7} (F)**	**D_{it}x10^{11} $(eV.cm^2)^{-1}$**	**V_{fb} (V)**	**N_{eff} x10^{14} $(1/cm^2)$**
S-400	144.0	2.45	2.23	3.56	9.88	2.045
S-600	164.0	2.30	1.79	3.26	11.4	1.975
S-800	129.0	4.87	4.28	1.68	6.93	2.455
S-1000	117.5	4.28	3.74	1.91	5.26	1.588

Interface states in a MOS capacitor are energy levels at the semiconductor-oxide interface caused by defects, which may trap charge carriers and impact the device's electrical performance. Thus, the density of interface states (D_{it}) can be calculated using equation (4.11) employing the Hill-Coleman method (Hill, W. A.; Coleman, C. C. 1980)

$$D_{it} = \frac{2}{Aq}\frac{G_{c,\max}/\omega}{\left(G_{c,\max}/\omega C_{ox}\right)^2 + (1 - C_c/C_{ox})^2} \tag{4.11}$$

where, $G_{c,max}/\omega$ is peak values of corrected G_c/ω–V curve, C_c is corrected capacitance of the MOS capacitor corresponding to $G_{c,max}/\omega$. The calculated D_{it} values were listed in Table 4.2. Initially, as annealing temperature increased, the

interface state density decreased, suggesting that the heat treatment effectively repairs crystal defects, reduces surface traps, and improves the oxide-semiconductor interface by enabling bond rearrangement or the removal of contaminants. It has also been reported that, at high temperatures—typically between 1000 and 1200 °C—a large number of carbon bonds break, releasing carbon monoxide from the surface and creating new crystal defects, while the remaining carbon on the surface becomes increasingly unstable due to this dissociation. Therefore, the increase in both N_{eff} and D_{it} values may also be attributed to carbon-related defect sites in the film structure, particularly at annealing temperatures reaching 1000 ° (Kaya, Ş., 2015). The calculate D_{it} value for annealed at 800 °C sample is in good agreement with the literature (Castán,H., 2011).

The annealing temperature plays a crucial role in the structural and electrical properties of MOS capacitors. In particular, it significantly influences the capacitance and conductance values, which are important parameters for device performance. Annealing treatments are commonly used to improve the interface quality between the oxide layer and the semiconductor substrate, which can, in turn, modify the electrical properties of the MOS structure. At higher temperatures, annealing can reduce the density of interface states, reduce defects in the oxide layer, and enhance the overall quality of the metal-oxide interface, leading to changes in capacitance and conductance behavior.

Capacitance measurements in MOS capacitors are sensitive to the interface states, oxide quality, and charge distribution within the semiconductor. As the annealing temperature increased, the capacitances of the device typically exhibited improved stability. Lower annealing temperature (400-600°C) can lead to an increase in the density of interface states. This reduction in interface states is often attributed to the healing of dangling bonds or the reduction of charge traps at the oxide-semiconductor interface, excessive annealing temperatures above a critical threshold can cause the formation of new defects, resulting in a degradation of capacitance performance and an increase in interface state density.

The G-V measurements of MOS capacitors can reveal important information about the quality of the interface and the degree of oxide or interface defects. At

higher annealing temperatures, the reduction in defect density generally leads to a decrease in the series resistance and an improvement in the conductance response. In particular, at optimal temperatures can significantly enhance the AC conductivity by improving the carrier exchange between the interface states and the majority carriers in the semiconductor. As a result, the conductance exhibits less frequency dependence, and the peak observed at the depletion edge becomes sharper and more defined as observed in the present study. Therefore, optimizing the annealing temperature is crucial for achieving the best possible performance in MOS capacitors, balancing the benefits of defect reduction with the potential risks of thermal degradation.

5. CONCLUSION

In this study, the structural and electrical characteristics of a dual gate dielectric stack comprising Sc_2O_3 and SiO_2 on 4H-SiC as a function of annealing temperature were investigated. Sc_2O_3 film was deposited via electron beam deposition system and the growth of SiO_2 via the dry oxidation method. The aim of this study is to investigate, at which annealing temperature, the Al/(Sc_2O_3/SiO_2/4H-SiC)/Ag MOS capacitors shows a good performance and the effect of using SiO_2 interfacial layer on its structural and electrical properties. Moreover, it seeks to explore the impact of series resistance and interface state density on C-V and G-V measurements of capacitors with respect to function of annealing temperature. The annealing temperature significantly influences the structural and electrical properties of MOS capacitors. The lattice parameter values increased with rising annealing temperatures, except for the 1000°C annealed film, where a slight decrease was observed. This trend is attributed to the shifting of peak intensity towards smaller angles as the annealing temperature increased. Crystallite sizes ranged from 309 Å to 249 Å, while lattice strains increased with temperature. The R_s values showed no clear trend, indicating reordering and restructuring effects due to the applied voltages. In the accumulation region, the values of C_c and G_c exhibited a substantial increase, with the S-800 sample showing the most significant change. The G_c-V curves displayed expected peaks at the depletion edge, typical of MOS devices due to the series resistance corrections. Additionally, the values of N_{eff} and D_{it} decreased with increasing annealing temperature up to 800°C, indicating that the heat treatment process effectively reduces surface traps, improves the oxide-semiconductor interface, and helps repair crystal defects. These results highlight the importance of annealing in optimizing the performance of MOS capacitors.

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