RELIABILITY MEASUREMENTS AND ANALYSIS OF GALLIUM NITRIDE ON SILICON CARBIDE HIGH ELECTRON MOBILITY TRANSISTORS (GaN-on-SiC HEMTs)

A DISSERTATION SUBMITTED TO

THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR

THE DEGREE OF

DOCTOR OF PHILOSOPHY

IN

ELECTRICAL AND ELECTRONICS ENGINEERING

By

Mahmut Can SOYDAN

December 2025

RELIABILITY MEASUREMENTS AND ANALYSIS OF GALLIUM NITRIDE ON SILICON CARBIDE HIGH ELECTRON MOBILITY TRANSISTORS (GaN-on-SiC HEMTs)

By Mahmut Can SOYDAN

December 2025

We certify that we have read this dissertation and that in our opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

Ekmel Özbay(Advisor)

Abdullah Atalar

Vakur Behçet Ertürk

Sefer Bora Lişesivdin

Ali Bozbey

Approved for the Graduate School of Engineering and Science:

Orhan Arıkan
Director of the Graduate School

ABSTRACT

RELIABILITY MEASUREMENTS AND ANALYSIS OF GALLIUM NITRIDE ON SILICON CARBIDE HIGH ELECTRON MOBILITY TRANSISTORS (GaN-on-SiC HEMTs)

Mahmut Can SOYDAN
Ph.D. in Electrical and Electronics Engineering
Advisor: Ekmel Özbay
December 2025

Gallium nitride (GaN) high electron mobility transistors (HEMTs) on semi-insulating SiC (GaN-on-SiC HEMT) have become the leading technology for high-power and high-frequency applications, yet their reliability is still under development. In particular, off-state operation under deep reverse bias is dominated by field-driven failure mechanisms such as impact ionization, hot-electron trapping, and gate and buffer leakage, which manifest as increased leakage currents, current collapse, and time-dependent breakdown. This thesis focuses on understanding and improving the off-state robustness of GaN-on-SiC HEMTs by systematically engineering the device layout, fabrication processes, and epitaxial design, using long-term off-state stress and leakage behavior as the primary evaluation criteria.

After introducing GaN material properties, device structure, and relevant failure mechanisms, the thesis first establishes a baseline by characterizing the RF-HTOL (RF-biased High Temperature Operating Life) behavior of the initial technology. Catastrophic failures under realistic RF stress motivated a series of geometric optimizations. By rearranging the lateral layout, in particular increasing the gate–drain spacing and rearranging the field-plate and drain pad connections, the breakdown voltage was significantly increased while maintaining essentially the same RF output power and efficiency. Next, fabrication-related reliability bottlenecks were addressed. Post-metal annealing and improved gate-foot etch resolved severe Q-point instability by restoring a true Schottky gate and eliminating residual SiN under the gate. An in-situ O_2/Ar ion pre-gate treatment and a high-temperature PECVD first nitride layer were then introduced, reducing gate and drain leakage by more than an order of magnitude and virtually eliminating catastrophic HTRB failures up to 200 °C. These improvements were validated by

DC-HTOL, HTRB, RF-HTOL, and step-HTRB tests.

Finally, the thesis investigates three epitaxial engineering routes targeting electric field redistribution and buffer-related trapping. A detailed root-cause analysis of gate degradation under HTRB test, combining TEM, elemental analysis, and electrical data, show that an ultra-thin oxide layer beneath the gate enhance the impact ionization at the drain-side gate edge. A dedicated buffer-engineering as thinning the c-GaN and increasing carbon concentration via growth condition control redistributes the vertical field, and reduces the active impact-ionization volume. That results in a reduction of final gate and drain leakage after long-term HTRB. Building on this, two epitaxial concepts are also developed. An AlGaN/GaN/AlGaN back-barrier design achieves roughly 30% higher breakdown voltage and more than a two-fold increase in time-to-failure under HTRB, with preserved RF performance and strongly reduced dynamic dispersion. A novel Fe-free ultra-thin buffer architecture with only 200 nm total GaN thickness further improves breakdown voltage by approximately 78%, increases RF output power and transconductance, and yields an order-of-magnitude reduction in off-state leakage, with zero failures observed in HTRB over the investigated stress window. TCAD simulations and TEM analysis consistently show that these epitaxial concepts relax the peak electric field at the gate edge. Overall, the thesis demonstrates that off-state reliability of GaN-on-SiC HEMTs can be substantially improved without sacrificing RF performance by coordinated optimization of layout, process, and epitaxy, guided by field distribution and leakage-based reliability metrics.

Keywords: GaN HEMT, Reliability, Failure Mechanism, HTRB, Off-state, Breakdown, Buffer engineering.

ÖZET

SİLİSYUM KARBÜR ÜZERİNDE GALYUM NİTRAT YÜKSEK ELEKTRON HAREKETLİLİĞİNE SAHİP TRANSİSTÖRLERİN (GaN-on-SiC HEMT) GÜVENİLİRLİK ÖLÇÜMLERİ VE ANALİZİ

Mahmut Can SOYDAN
Elektrik ve Elektronik Mühendisliği, Doktora
Tez Danışmanı: Ekmel Özbay
Aralık 2025

Yarı-yalıtkan SiC üzerine büyütülen galyum nitrür (GaN) yüksek elektron hareketliliğine sahip transistörler (GaN-on-SiC HEMT), yüksek güç ve yüksek frekans uygulamaları için lider teknoloji konumuna gelmiştir; ancak güvenilirlikleri halen gelişim aşamasındadır. Özellikle derin ters kutuplama altındaki kapalı (off-state) durumda, darbe iyonlaşması, sıcak elektron tutulması ve kapı/tampon kaçakları gibi alan kaynaklı arıza mekanizmaları baskındır ve bunlar artmış kaçak akımları, akım çökmesi ve zamana bağlı (time-dependent) yüksek gerilim kırılması olarak kendini gösterir. Bu tezde, GaN-on-SiC HEMT'lerin kapalı durum dayanıklılığı, uzun süreli off-state stres ve kaçak davranışı temel değerlendirme kriterleri olacak şekilde aygıt dizaynı (layout), mikrofabrikasyon süreçleri ve epitaksiyel tasarımı üzerinden sistematik olarak mühendislik yapılarak iyileştirilmektedir.

GaN malzeme özellikleri, cihaz yapısı ve ilgili arıza mekanizmaları tanıtıldıktan sonra, önce başlangıç teknolojisinin RF-HTOL (RF-uygulamalı Yüksek Sıcaklık Çalışma Ömrü) davranışı karakterize edilerek bir referans düzey oluşturulmuştur. Gerçekçi RF stres koşulları altında gözlenen katastrofik arızalar, bir dizi geometrik optimizasyonu tetiklemiştir. Yanal yerleşimin yeniden düzenlenmesiyle, özellikle kapı–akaç aralığının arttırılması ve alan levhası (field-plate) ile akaç pedinin yeniden tasarlanması sayesinde, kırılma gerilimi anlamlı düzeyde artmış, RF çıkış gücü ve verimlilik ise neredeyse değişmeden korunmuştur. Ardından, fabrikasyona bağlı güvenilirlik dar boğazları ele alınmıştır. Kapı metali sonrası tavlama (post-metal annealing) ve iyileştirilmiş kapı ayağı aşındırma (gate-foot etch) adımları, kapı altında kalan artık SiN tabakasını giderip gerçek bir Schottky kapı temasını yeniden oluşturarak ciddi Q-noktası kararsızlığını ortadan kaldırmıştır. Devamında, *in-situ* O_2/Ar iyonu kapı metal kaplaması öncesi

yüzey temizlik işlemi ve yüksek sıcaklıklı PECVD birinci nitrid katmanı prosese eklenmiş, böylece kapı ve akaç kaçakları bir mertebeden fazla azaltılmış ve 200 °C'ye kadar HTRB testlerinde katastrofik arızalar neredeyse tamamen ortadan kaldırılmıştır. Bu iyileştirmeler DC-HTOL, HTRB, RF-HTOL ve kademeli HTRB (step-HTRB) testleri ile doğrulanmıştır.

Son aşamada, elektrik alan yeniden dağılımı ve buffer kaynaklı tuzaklanmayı hedefleyen üç epitaksiyel mühendislik yaklaşımı incelenmiştir. TEM, element analizi ve elektriksel verilerin birleştirildiği ayrıntılı bir kök neden analizi, kapı altındaki uç derecede ince oksit tabakasının, akaç tarafı kapı kenarında darbe iyonlaşmasını belirgin şekilde arttırdığını göstermiştir. Bunu azaltmak için geliştirilen bir tampon katmanı mühendisliği adımında, c-GaN kalınlığının inceltilmesi ve karbon konsantrasyonunun büyütme koşulları ile arttırılması sayesinde dikey alan profili yeniden dağıtılmış, etkin darbe iyonlaşma hacmi azaltılmış ve uzun süreli HTRB sonrası nihai kapı/akaç kaçakları anlamlı düzeyde düşmüştür. Buna ek olarak iki epitaksiyel tasarım daha geliştirilmiştir. AlGaN/GaN/AlGaN arka bariyerli tasarım, HTRB koşulları altında yaklaşık %30 daha yüksek kırılma gerilimi ve iki kattan fazla artmış zamana bağlı arıza süresi sağlarken, RF performansını korumuş ve dinamik yayılmayı (dispersion) belirgin şekilde azaltmıştır. Toplam GaN kalınlığı yalnızca 200 nm olan yeni, Fe-içermeyen ultra-ince buffer mimarisi ise kırılma gerilimini yaklaşık %78 oranında arttırmış, RF çıkış gücü ve transkonduktansı iyileştirmiş ve incelenen stres penceresinde HTRB testlerinde hiç arıza gözlenmeden, kapalı durum kaçağını bir mertebe azaltmıştır. TCAD simülasyonları ve TEM analizi, bu epitaksiyel tasarımların kapı kenarındaki tepe elektrik alanını rahatlattığını tutarlı bir şekilde göstermektedir. Genel olarak, alan dağılımı ve kaçak-temelli güvenilirlik metrikleri ile yönlendirilen yerleşim, proses ve epitaksinin birlikte optimize edilmesiyle, GaN-on-SiC HEMT'lerin off-state güvenilirliğinin RF performansından ödün vermeden belirgin şekilde iyileştirilebileceği ortaya konmuştur.

Anahtar sözcükler: GaN HEMT, Güvenilirlik, Bozulma Mekanizmaları, HTRB, Kapalı durum, Kırılım, Tampon tabaka mühendisliği.

Acknowledgement

I would first like to express my deepest gratitude to my supervisor, Prof. Ekmel Özbay. Throughout this work, he has consistently looked out for what would be in my best interest as a researcher, not only in the short term but also for my long-term scientific growth. His guidance, support, and patience have been essential at every stage of this thesis. I am especially thankful for the outstanding laboratory infrastructure and working conditions he has provided, and for the opportunity to work in a productive, high-quality research environment. Being able to collaborate with such hardworking and knowledgeable people in his group has been a privilege, and it is a direct consequence of his leadership.

I would also like to thank Prof. Vakur Ertürk and Prof. Bora Lişesivdin for serving on my thesis monitoring committee and for the constructive comments and suggestions they offered during the progress of my work, and kindness they showed. I am equally grateful to Prof. Abdullah Atalar and Prof. Ali Bozbey for kindly agreeing to serve on my thesis jury and for the time and effort they dedicated to evaluating this work. Their questions, critiques, and perspectives have contributed both to the quality of this thesis and to my own understanding of the field.

My sincere thanks go to all my colleagues and friends in the research group. I have been fortunate to work in a team that is not only technically strong but also disciplined, supportive, and genuinely collaborative. The group has had a major impact on how I learned, how I think about problems, and how I approach research. Every fabrication run we completed, every measurement session we survived, and every long discussion we had while trying to interpret results has contributed to this thesis. I would like to thank Bayram Bütün, Erdem Aras, Emirhan Urfalı, Burak Güneş, Abdülkadir Gürbüz, Gizem Tendürüs, Ümit Binici, İmran Nawaz, Salahuddin Zafar, Arda Eren, Buse Seçkin, Metehan Bacak, Utku Ağtaş, Gamze Ulusoy Ghobadi and all of the fabrication team, to whom are still with us or not, for their help, ideas, and day-to-day support in the lab and office.

I owe very special thanks to Amir Ghobadi and Amir Ali Joya. They have contributed far beyond normal collaboration, both in the scientific and practical sense. They have been deeply involved in designing experiments, analyzing and

interpreting results, and critically reviewing the way I presented and framed this work. Their help during my research, during the long analysis sessions, and especially in the preparation of this thesis has been invaluable. I can say without exaggeration that their input has had a major influence on the final shape and quality of this work.

I am profoundly grateful to my family. To my mother Hacer, my father İsmail and my sister Hande, I owe far more than I can express here. Their support has always been steady and unconditional, even when the path I chose was demanding and uncertain. I have always felt that I could rely on them, and reaching this point is, in many ways, the result of their sacrifices and faith in me. Just knowing that they are there, even from a distance, has been a source of strength throughout this journey. I would also like to thank my wife's family. My father-in-law Süleyman, my mother-in-law İlknur, my brother-in-law Enes, and my sister-in-law Vildan have all added joy and balance to my life outside the lab. They have supported me in many visible and invisible ways. I am genuinely thankful for their kindness, and the way they have welcomed me into their family.

Finally, my deepest gratitude is to my dear wife, Mürşide. She is the most precious part of my life, and this thesis simply would not exist in its current form without her. She has stood by me through every stage of this process: the long days in the lab and the late nights at the computer. She has been patient when I was tired and absent-minded, understanding when research came first, and encouraging when results were unclear or disappointing. She has constantly pushed me to become a better version of myself, not only as a researcher but as a person. Her trust in me, even at times when I doubted myself, has been a decisive factor in getting this work done. Thanks to her support, I have not only completed this thesis but have also grown into a stronger and more confident scientist and human being. Our future is as bright as science.

Contents

1 Introduction **1**
1.1 Advantages and Market Share of GaN Devices 2
1.2 Reliability Bottleneck of GaN HEMTs 4
1.3 Research Scope and Main Scientific Contributions 6
1.3.1 Improving reliability by layout design 7
1.3.2 Improving reliability by fabrication-process optimization . 7
1.3.3 Reducing HTRB degradation through epitaxial design . . . 8
1.4 Thesis Structure 9

2 GaN-on-SiC HEMTs Technology Overview: Properties, Design and Process **12**
2.1 GaN material properties 12
2.2 GaN-on-SiC HEMT structure 14
2.2.1 Roles and design parameters of Epitaxial layers 16
2.2.2 Roles and design parameters of micro/nano fabrication layers 21
2.3 GaN-on-SiC HEMT process flow 24
2.3.1 Epitaxial growth 24
2.3.2 Micro/nano fabrication 26

3 Failure Mechanisms, Reliability Tests and Measurement Methods **28**
3.1 Failure Mechanisms of GaN HEMTs 28
3.1.1 Electric-field Distribution and Peak Points 28
3.1.2 Impact Ionization 29
3.1.3 Hot Electron Trapping 31

3.1.4 Leakage Current Mechanisms 32
3.2 Reliability Tests and Long-term Test Systems 33
3.2.1 DC-HTOL 34
3.2.2 HTRB 35
3.2.3 RF-HTOL 36
3.3 Measurement Systems 36
3.3.1 DC Measurement 36
3.3.2 RF Small-signal (S-parameter) Measurement 38
3.3.3 RF Large-signal (Load-pull) Measurement 39
3.3.4 Pulsed I–V Measurement 40

4 Layout Engineering 42
4.1 RF-HTOL Test Performance of the Devices Before Improvements 42
4.2 Breakdown Voltage Improvement via Lateral Geometries 46

5 Fabrication Process Flow Optimizations 55
5.1 Post-metal Annealing (PMA) Process to Solve Q-Point Instability 55
5.1.1 HTOL Test of Devices without PMA 56
5.1.2 TEM Analysis of Devices without PMA 57
5.1.3 HTOL Test of Devices with PMA 60
5.1.4 TEM Analysis of Devices with PMA 60
5.2 Improving Reliability by Nitride Layers and Gate-Treatment Methods 62
5.2.1 Reliability Improvement by Pre-Gate Treatment Technique 65
5.2.2 Reliability Improvement by Nitride Deposition Techniques 69
5.2.3 Optimization of O_2/Ar Ion Treatment Durations 76
5.3 RF-HTOL Test Performance after Process Improvements 79

6 The origin of gate degradation under HTRB operation: Buffer engineering to suppress impact ionization in GaN HEMT 82
6.1 Preface 82
6.2 Introduction 83
6.3 Device Design and Fabrication 85
6.4 Gate Degradation 86

6.5 Causes of Gate Degradation 89
6.6 Buffer Engineering to Prevent Impact Ionization 91
6.7 DC/RF Performance 96
6.8 Conclusion 100

7 Breakdown Voltage and Off-state Reliability Improvement using $Al_xGa_{1-x}N$ Back-barrier Layer 101
7.1 Introduction 102
7.2 Experimental details 105
7.3 Measured results and discussion 106
7.3.1 DC characteristics 107
7.3.2 Breakdown characteristics 108
7.3.3 Time-to-failure and time-dependent breakdown 109
7.3.4 Electric-field distribution and reliability 112
7.3.5 RF performance 113
7.3.6 Transient analysis 114
7.4 Conclusion 117

8 Buffer-free, Ultra-thin Barrier GaN-on-SiC HEMTs with a Highly Doped GaN Layer for Next Generation Power Devices 118
8.1 Introduction 119
8.2 Epitaxial Growth and Device Fabrication 120
8.3 HEMT Results 123
8.3.1 DC Characteristics and Breakdown 123
8.3.2 RF Characteristics 127
8.4 Conclusion 128

9 Conclusion and Future Work 129
9.1 Summary of the Thesis 129
9.2 Future Work 132

List of Figures

1.1 Cross-section view of a GaN-on-SiC HEMT showing the epitaxial stack and device layers. 2
1.2 Illustration of thermally, mechanically, and electrically triggered failure mechanisms in GaN HEMTs. 5

2.1 SEM images of fabricated GaN HEMTs. a) Top-view image of HEMT. b) Cross-sectional side view image of HEMT. 14
2.2 2DEG formation at AlGaN/GaN interface. a) Cut-line for the band diagram. b) Band diagram of metal–AlGaN–GaN stack and 2DEG formation. 15
2.3 Epitaxial stack of a standard GaN-on-SiC HEMT and epitaxial design parameters 16
2.4 Schematic of GaN HEMT cross-section with design parameters. . 21
2.5 Main process steps of GaN-on-SiC HEMTs. 25

3.1 E-field profiles at deep off-state in GaN HEMT. (a) E-field distribution in 2D map. (b) E-field inside AlGaN layer through the cut-line at inset picture. 29
3.2 Impact ionization mechanism in GaN HEMTs. 30
3.3 Hot electron effects in GaN HEMTs: trapping at AlGaN interfaces with SiN and GaN, and in the buffer dopants, and new defect generation. 32
3.4 Common leakage current mechanisms in GaN HEMTs. 33
3.5 Accel-RF company DC-96 and RF-16 AARTS test systems. 34
3.6 On-wafer DC measurement setup used for measuring HEMT and capacitor. 37

3.7 The schematic of small-signal RF measurement setup. 39
3.8 The schematic of RF load-pull measurement setup. 40
3.9 Pulsing diagrams for (a) I_D–V_{DS} and (b) I_D–V_{GS} characterizations using pulsed I–V method. 41

4.1 Optical image of the two-stage amplifier module showing the HEMTs and input/interstage/output matching networks. 43
4.2 RF output power of the amplifier modules under RF-HTOL stress as a function of elapsed stress time. 44
4.3 Gate leakage current of the amplifier modules under RF-HTOL stress as a function of elapsed stress time. 44
4.4 SEM image of a failed amplifier module showing a burnt HEMT and melted wire bonds. 45
4.5 SEM images of the burnt area: (a) exploded via holes; (b) field-plate anchors on the source pads within the damaged region. . . . 46
4.6 SEM images of baseline HEMTs that failed during breakdown voltage sweeps under off-state bias. 47
4.7 Schematic representation of gate and field-plate geometrical variations (V1–V7) for DS5 HEMTs. Each grid corresponds to 100 nm in the horizontal direction. 48
4.8 Breakdown-voltage histograms for gate/field-plate layout variants V1–V6 (DS5 devices). 49
4.9 Breakdown-voltage histograms comparing V1 and V7 gate/field-plate layouts (DS5 devices). 49
4.10 Layout comparison of DS5 and DS6 HEMTs in the first iteration, showing increased drain-to-source distance and modified drain-pad connections. 50
4.11 Field-plate and gate-metal to drain-pad design: SEM images of (a)-(b) previous layout (DS5) and (c)-(d) new layout (DS6). . . . 51
4.12 SEM images and measured breakdown voltages of DS5 and DS6 HEMTs, highlighting the improvement obtained by increasing L_{DS}. 52
4.13 Layout comparison of DS5 and DS6 HEMTs in the first iteration, showing increased drain-to-source distance and modified drain-pad connections. 53

5.1 (a) Drain current and (b) regulated gate-quiescent voltage of HEMTs during HTOL without PMA. 56
5.2 TEM cross-section of the HEMT showing the epitaxial stack, gate and field plate. 58
5.3 TEM images of the gate region of the initial device: (a) epitaxial layers, gate metals and Schottky contact; (b) magnified view of the gate/AlGaN interface. 58
5.4 Elemental analysis of the gate/AlGaN interface of the initial device: (a) location of the line scan on the TEM image, (b) elemental profile from epitaxy into gate metal showing a Si peak at the interface. 59
5.5 HTOL results of devices fabricated with improved gate-foot etch and PMA: (a) drain current, (b) regulated gate-quiescent voltage. 61
5.6 TEM images of the improved device with PMA: (a) overall cross-section, (b) high-magnification view of the gate/AlGaN interface. 61
5.7 Elemental analysis of the gate/AlGaN interface in the annealed device: (a) line-scan location, (b) elemental profile showing absence of Si at the interface. 62
5.8 Schematic cross-section of the three-layer SiN stack around the gate region. 63
5.9 Simulated electric-field distribution in a GaN HEMT under deep off-state bias. 64
5.10 DC characteristics of devices with NH_4OH and O_2/Ar pre-gate treatments: (a) output I–V, (b) transfer characteristics, (c) forward gate I–V, (d) off-state leakage. 66
5.11 Breakdown measurements of HEMTs with NH_4OH and O_2/Ar pre-gate treatments. 67
5.12 HTRB results of HEMTs with NH_4OH pre-gate treatment: drain leakage (left axis) and base temperature (right axis). 68
5.13 HTRB results of HEMTs with O_2/Ar pre-gate treatment: drain leakage (left axis) and base temperature (right axis). 68

5.14 (a) Layout and cross-section of the MIM capacitor used for nitride characterization; (b) I–V characteristics of capacitors with ICPCVD and PECVD SiN. 70
5.15 Drain leakage versus drain voltage for GaN HEMTs with ICPCVD and PECVD second SiN layers. 72
5.16 Breakdown characteristics of capacitors with PECVD SiN deposited at 275 °C and 350 °C. 73
5.17 FTIR measurements of SiN films deposited at 275 °C and 350 °C. 73
5.18 HTRB results of HEMTs with standard-temperature PECVD SiN as the first layer. 74
5.19 HTRB results of HEMTs with high-temperature PECVD SiN as the first nitride layer. 75
5.20 Breakdown measurements for HEMTs with different O_2/Ar treatment durations: (a) drain leakage vs. drain voltage, (b) breakdown-voltage histograms. 76
5.21 HTRB results for lot-A devices (10 min O_2 + 15 min Ar) at (a) 150 °C and (b) 200 °C. 77
5.22 HTRB results at 200 °C for (a) lot-B devices (5 min O_2 + 10 min Ar) and (b) lot-C devices (5 min O_2 + 15 min Ar). 77
5.23 Step-HTRB result for a lot-A HEMT (10 min O_2 + 15 min Ar): drain leakage (left axis) and base temperature (right axis). 78
5.24 Step-HTRB result for a lot-B HEMT (5 min O_2 + 10 min Ar): drain leakage (left axis) and base temperature (right axis). 78
5.25 Step-HTRB result for a lot-C HEMT (5 min O_2 + 15 min Ar): drain leakage (left axis) and base temperature (right axis). 79
5.26 RF-HTOL results at 110 °C for modules with improved HEMTs: (a) RF output power, (b) gate leakage current. 79
5.27 RF-HTOL results for modules with improved HEMTs at base temperatures of 130–150 °C: (a) RF output power, (b) gate leakage current. 80

6.1 (a)Schematic of the investigated HEMT, (b) SEM image of fabricated HEMT, (c) Zoomed SEM image of 10 finger 2.65 mm long fabricated HEMT with gate fingers, drain and source. 85

6.2 (a) Gate current from HTRB tests at (V_g,V_d)=(-8 V,125 V), (b) operation of fabricated GaN HEMT under UV radiation to suspect impact ionization as the reason of gate degradation, (c) operation of a known commercial GaN HEMT (Cree) under UV radiation . 87

6.3 (a) TEM image of gate-AlGaN contact to show a dielectric present between the gate metal, (b) EDX scan of gate-AlGaN contact shows an oxygen peak at the interface, and (c) a proposed mechanism that shows energy band profile of gate-oxide-AlGaN contact under HTRB conditions exhibiting hole accumulation in oxide layer causing oxide barrier thinning to maintain charge neutrality inside the oxide layer. 88

6.4 (a) HTRB tests, with varying V_d, on reference HEMTs to show onset drain voltage for gate degradation at $T = 150°C$ and V_g=-8 V (b) a lateral cutline of the reference device from electric field simulation at varying V_d from 30 V to 100 V to predict the electric field at the onset drain voltage of gate degradation 91

6.5 (a) Epitaxial differences between reference and proposed modified device to mitigate gate degradation and (b) SIMS data to show the difference in the carbon impurity profile between the reference and modified device 92

6.6 Maximum gate leakage value vs number of HEMTs in both reference and modified samples under HTRB conditions 93

6.7 Simulation results under HTRB at (V_g,V_d)=(-8 V,100 V) for (a) impact generation profile (b) field vectors in reference and modified HEMTs that lead to (c) hole accumulation under the gate on the source side 94

6.8 Comparison of (a) I_{dss}, (b) V_{th}, (c) g_m, and (d) $I_{d,off}$ between reference and modified HEMTs 96

6.9 Breakdown voltage histograms for reference and modified HEMTs showing V_{br} improvement 97

6.10 Large signal performance (P_{out}, G_T, and PAE) comparison of (a) reference and (b) modified HEMTs 98

6.11 Pulsed I_d-V_d test results to show current collapse due to bulk trapping in reference and modified HEMTs at two different stress levels 99

7.1 Epitaxial schematic of (a) the reference AlGaN/GaN HEMT and (b) the AlGaN/GaN/AlGaN back-barrier HEMT. 104
7.2 (a) Schematic cross-section and (b) FIB–SEM image of the fabricated back-barrier HEMT. 106
7.3 Simulated energy-band diagrams of HEMTs with and without an AlGaN back barrier at zero bias. 107
7.4 DC characteristics of the reference and back-barrier HEMTs: (a) output I_d–V_d curves at $V_g = 1\,\mathrm{V}$, (b) transfer characteristics at $V_d = 10\,\mathrm{V}$, and (c) transconductance g_m. 108
7.5 Off-state breakdown characteristics of HEMTs with and without back barrier: (a) linear scale and (b) logarithmic scale. 109
7.6 HTRB test at $(V_{gs}, V_{ds}) = (-8\,\mathrm{V}, 75\,\mathrm{V})$ and 150°C for HEMTs with and without back barrier. 110
7.7 HTRB results for back-barrier HEMTs: (a) drain current versus time at different V_{ds} and (b) extracted TTF with exponential fit versus V_{ds}. 111
7.8 Long-term HTRB results for (a) standard and (b) back-barrier HEMTs with $L_{ds} = 3.5\mu m$. 111
7.9 Simulated electric-field distribution in the top AlGaN barrier for HEMTs with and without back barrier at deep off-state. 112
7.10 TCAD simulations of impact-ionization-induced hole concentration for HEMTs with and without back barrier at high off-state bias. 113
7.11 Large-signal RF characteristics of HEMTs with and without back barrier: gain, output power P_{out}, and PAE versus input power. . . 114
7.12 Drain-current transient measurements for HEMTs with and without back barrier under off-state stress pulses. 115
7.13 Simulated energy-band diagram of the reference AlGaN/GaN HEMT from c-GaN to u-GaN, indicating Fe and C trap levels. . . 116

7.14 Simulated energy-band diagram of the AlGaN/GaN/AlGaN back-barrier HEMT, showing stronger channel confinement due to carbon-rich AlGaN. 116

8.1 (a) Epitaxial schematic of the standard (left) and UTB (right) HEMTs. (b) Simulated conduction band diagram along a vertical cut-line through the two epitaxies. 120

8.2 TEM images of UTB HEMTs. (a) Overall cross-section showing epitaxial, metal, and dielectric layers. (b) Gate region with ultra-thin GaN channel and Schottky contact. (c) SiC/AlN interface and (d) AlN/GaN interface, demonstrating high crystalline quality. 122

8.3 DC characteristics of Std and UTB HEMTs ($L_G = 0.25\ \mu$m, $W_G = 125\ \mu$m). (a) Output characteristics I_D–V_D for V_G from -4 V to 1 V. (b) Transfer characteristics I_D–V_G at $V_D = 10$ V. (c) Transconductance g_m versus V_G. (d) Off-state breakdown characteristics. 124

8.4 Off-state breakdown comparison for Std and UTB HEMTs ($L_G = 0.25\ \mu$m, $W_G = 125\ \mu$m, eight fingers, $L_{ds} = 3.3\ \mu$m). (a) Measured I_D–V_D curves at $V_G = -8$ V. (b) Breakdown voltage histograms for 14 devices of each type. 125

8.5 Long-term HTRB results for (a) standard and (b) UTB HEMTs with $L_{ds} = 3.5\mu m$. 125

8.6 TCAD-simulated electric field distribution under deep off-state bias for (left) Std epitaxy and (right) UTB epitaxy. The UTB design reduces field peaks at the gate and field-plate edges and spreads the field into the drain access region. 126

8.7 Large-signal RF performance of Std and UTB HEMTs: comparison of G_T, P_{out}, and PAE versus input power. 127

List of Tables

2.1 Comparison of material properties of Transistor compounds . . . 13

4.1 RF performance comparison of DS5 and DS6 HEMTs with V1 and V2 gate/field-plate layouts. 53

4.2 RF performance comparison of three types of HEMTs with different gate widths, gate-foot lengths and drain-to-source distances. . 54

7.1 Reported AlGaN/GaN HEMTs with AlGaN back barriers and their breakdown improvement as a function of channel thickness t_C, drain–source spacing L_{ds}, AlGaN back-barrier thickness t_{BB}, and Al content x. 103

7.2 Maximum available gain and cutoff frequencies for HEMTs with and without an AlGaN back barrier. 114

Chapter 1

Introduction

Gallium nitride (GaN) is a wide–bandgap III–V semiconductor with a bandgap of about 3.4 eV, high critical electric field (∼3 MV/cm), high electron saturation velocity, and good thermal conductivity. These intrinsic properties enable transistors to operate at higher voltages, higher frequencies, and higher junction temperatures than conventional Si or GaAs technologies while maintaining high efficiency [1].

In high-electron-mobility transistors (HEMTs), a two-dimensional electron gas (2DEG) is formed at the AlGaN/GaN interface due to strong polarization fields. The resulting 2DEG exhibits very high sheet charge density and mobility, which also brings low on-resistance and high-power density. A simplified cross-section of the baseline GaN-on-SiC HEMT used in this work is shown in Figure 1.1. The structure consists of a semi-insulating SiC substrate, AlN nucleation layer for compensating lattice mismatch, a thick GaN buffer, an AlGaN barrier supporting the 2DEG channel, an AlN sheet layer at AlGaN/GaN interface, a thin GaN cap layer in the epitaxy, and ohmic source/drain contacts, a Schottky gate, stacked SiN passivation layers, and a source-connected field plate. This combination of epitaxial and layout features is representative of state-of-the-art RF GaN-on-SiC technologies[2].

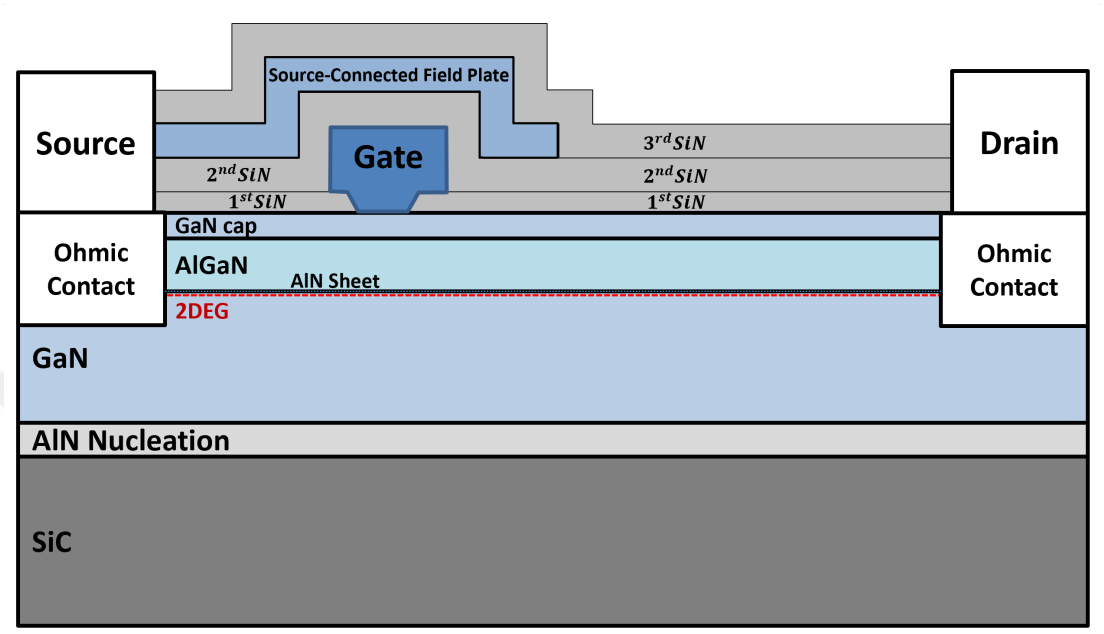


Figure 1.1: Cross-section view of a GaN-on-SiC HEMT showing the epitaxial stack and device layers.

1.1 Advantages and Market Share of GaN Devices

From a performance perspective, GaN HEMTs deliver substantially higher breakdown voltage, power density, and efficiency than incumbent Si LDMOS and GaAs PHEMT technologies over a wide frequency and power range [3, 4]. Comparative RF power-amplifier studies consistently show that GaN devices provide several-fold higher power density than LDMOS or GaAs while maintaining comparable or superior efficiency and linearity [5]. In RF, GaN-on-SiC HEMTs are optimized for high power density and high frequency. HEMTs and MMIC power amplifiers with 10–20 W/mm power density or drain efficiencies around 60–70% have been reported for S- [3, 6, 7], C-[8, 9, 10, 11], and X-band radar[4, 12, 13], ISM-band RF energy systems [14], and base-station PAs [15]. At the same time, GaN-on-Si and lower-voltage GaN-on-SiC devices are promising candidates for power electronics from tens of kilohertz up to several megahertz, enabling compact, high-efficiency converters for consumer fast chargers, data-center power supplies, photovoltaic

inverters, and on-board chargers in electric vehicles [16, 17, 18, 19, 20]. Therefore, GaN HEMTs cover applications from low-frequency, low-to-medium-power conversion up to high-frequency, very-high-power RF transmission, with GaN-on-SiC occupying the high-performance corner where maximum RF power density and robustness at elevated voltages and temperatures are required [3, 21].

These advantages have driven rapid adoption of GaN-on-SiC HEMTs in a wide range of applications: base-station power amplifiers for 4G/5G, active electronically steered array (AESA) radars, satellite and spaceborne transmitters, electronic warfare systems, cable TV infrastructure, and, increasingly, in high-frequency power conversion[22]. In parallel, lateral GaN-on-Si and vertical GaN power devices have penetrated fast chargers, data-center power supplies, automotive on-board chargers, and other high-density power conversion markets, accelerating the overall GaN ecosystem[2].

Market analyses consistently project strong growth for both RF and power GaN. Recent reports forecast the RF GaN device market to grow with a compound annual growth rate (CAGR) of 20% over the next decade, reaching multi-billion-dollar revenues by 2030, driven mainly by telecom infrastructure, defense, and satellite applications[2]. In this landscape, GaN-on-SiC HEMTs occupy the high-performance, high-reliability corner of the RF market, where high power density and robust operation at elevated voltages and temperatures justify the higher substrate cost.

As a result, GaN-on-SiC HEMTs are strategically important because they combine intrinsic material advantages over Si and GaAs, device-level performance that enables higher power density and efficiency, and rapidly growing adoption in critical RF and power-electronics markets.

1.2 Reliability Bottleneck of GaN HEMTs

Despite their excellent static performance, GaN-based HEMTs exhibit a variety of degradation and failure mechanisms when subjected to prolonged thermal, electrical, and mechanical stress. Reliability has therefore become one of the main bottlenecks for the full exploitation of GaN-on-SiC in demanding RF and power applications[23].

Figure 1.2 summarizes main failure mechanisms and relates them to specific regions of the device. At the metallization level, high current density and temperature can cause metal electromigration in the source pads and interconnects, ultimately leading to increased series resistance or open circuits [24, 25]. Around the gate, gate edge degradation is associated with relaxation under high field and temperature, resulting in enhanced gate leakage and ultimate breakdown[26, 27]. Mechanical stress, originating from thermal cycling, lattice mismatch, and intrinsic film stress (e.g. in SiN passivation), contributes to crack formation, delamination, and evolution of dislocation networks, which in turn opens additional leakage paths and modifies the local electric-field distribution[28].

Electrically driven mechanisms are particularly critical for GaN-on-SiC HEMTs because they operate close to the material's high breakdown field. Under high drain bias, large lateral and vertical electric fields near the gate edges and field-plate terminations lead to hot-electron injection, impact ionization, and trap creation both in the AlGaN/GaN interface region and in the buffer[29, 30, 31, 32, 33, 34]. In the passivation stack, hot-electron trapping in SiN and charge build-up at SiN/AlGaN or SiN/GaN interfaces modify the surface potential, contributing to dynamic on-resistance and V_{th} drift[23, 29].

Within the AlGaN barrier and the AlGaN/GaN heterointerface, hot-electron trapping in pre-existing or stress-induced defects reduces the 2DEG density and mobility, leading to drain current degradation and dispersion between DC and RF characteristics[29, 31]. Deeper into the GaN buffer, hot-electron trapping

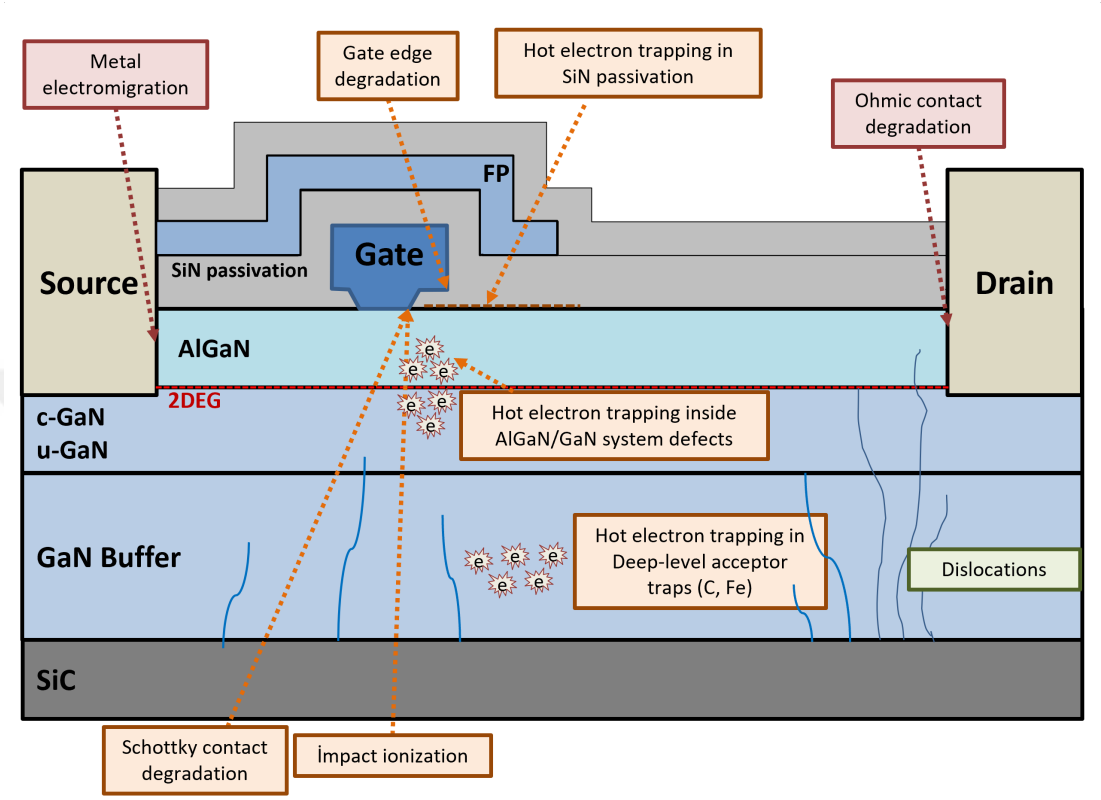


Figure 1.2: Illustration of thermally, mechanically, and electrically triggered failure mechanisms in GaN HEMTs.

in deep acceptor states, which is often associated with intentional C or Fe doping, accumulates negative charge, modifies the vertical electric-field profile, and can induce additional leakage paths or buffer-related current collapse[35, 36, 37]. Dislocations present in the buffer may contribute to vertical leakage for defect generation under stress.

At high reverse bias on the gate and drain, Schottky contact degradation (e.g. at the gate edge) and impact ionization in the high-field region near the drain-side gate edge become key precursors to catastrophic breakdown [26, 34]. Time-dependent breakdown studies under high-temperature reverse bias (HTRB) have shown that localized electric-field peaks at terminations or gate edges can trigger sequential breakdown mechanisms, starting with leakage-path formation and culminating in hard failure[38].

Among all these mechanisms, field-driven degradation is often the most critical in high-voltage GaN-on-SiC technologies. The combination of high lateral fields near the gate edge and vertical fields through the buffer means that many dominant failure modes—gate leakage acceleration, trap creation, impact ionization, and buffer breakdown— are governed primarily by electric field, with temperature acting as a secondary accelerator. This has led the community to focus heavily on test conditions that maximize electric-field stress.

For off-state reliability, the standard approach is the high-temperature reverse-bias (HTRB) test, in which the device is biased in deep pinch-off with a high drain-to-source voltage and elevated ambient or chuck temperature. HTRB selectively stresses the high-field regions without significant self-heating from conduction current, and is therefore particularly sensitive to field-driven mechanisms such as impact ionization, buffer leak paths, and gate edge breakdown. Typical evaluation metrics include time-to-failure distributions, changes in drain and gate leakage currents after stress. For on-state reliability, high-temperature operating life (HTOL) and, more specifically for RF applications, RF-HTOL tests are used to emulate realistic RF drive conditions and assess degradation and catastrophic failure rate under simultaneous high field, high current, and self-heating. Because field-driven mechanisms dominate many observed GaN HEMT failures, this thesis centers its reliability analysis on off-state HTRB testing and RF-HTOL experiments. The main evaluation criteria are measured breakdown voltage and leakage currents of devices before reliability testing, long-term HTRB failure rate, and leakage-current degradation during testing.

1.3 Research Scope and Main Scientific Contributions

This thesis addresses the reliability bottleneck of GaN-on-SiC HEMTs by proposing solutions from three complementary directions: layout engineering,

fabrication-process optimization, and epitaxial/buffer design. All three are evaluated primarily under deep off-state breakdown sweeps and HTRB stress, with RF-HTOL used to confirm improvements in realistic RF operation.

1.3.1 Improving reliability by layout design

The first research axis focuses on optimizing layout parameters to reduce local electric-field peaks while maintaining RF performance. In lateral GaN-on-SiC HEMTs with field plates, the peak field typically occurs near the drain-side gate edge or at field-plate terminations; excessive field concentration there directly correlates with early breakdown and high HTRB failure rates[38, 39, 4]. In this work, key geometrical parameters such as the source-to-gate and gate-to-drain spacings, the relative positions of high and low potential layers, and the length of source-connected field plates are systematically varied. Appropriate geometrical parameters are chosen for the intended operating voltage to mitigate field crowding. The goal is to identify layout configurations that redistribute the electric field more uniformly along the surface and in the buffer, thereby enhancing breakdown voltage and off-state robustness without sacrificing gain, output power, or bandwidth.

1.3.2 Improving reliability by fabrication-process optimization

The second research axis targets solving reliability limitations associated with the fabrication processes, especially in the gate and passivation regions. First, a post-metal annealing process is introduced after gate metallization to address threshold-voltage instability. By carefully selecting the annealing temperature and improving the gate foot etch processes, interfacial defects and residual process damage at the Schottky contact are reduced, leading to more stable V_{th} under bias stress and improved gate-leakage characteristics. Second, the gate pre-treatment method prior to gate metal deposition is revisited. Conventional wet treatments

can leave behind uncontrolled residues or modify surface stoichiometry, impacting gate leakage and device-to-device variability. An alternative in situ treatment is evaluated with the objective of lowering off-state gate leakage and improving Schottky barrier uniformity. Third, the thesis investigates first and second nitride passivation layers, comparing different SiN deposition techniques (ICPCVD vs PECVD) and recipes, including deposition temperature. Film quality, intrinsic stress, hydrogen content, and interface state density are known to strongly influence both surface trapping and long-term reliability of GaN HEMTs. Here, multiple SiN stacks are fabricated and bench marked in terms of leakage current, breakdown voltage, and HTRB failure statistics. Finally, RF-HTOL tests are carried out on devices before and after the combination of layout and process optimizations. These RF-HTOL experiments serve as an independent verification that the improvements observed under HTRB (gate leakage stability, breakdown enhancement, reduced failure rates) improves the reliability of the devices under realistic RF operation.

1.3.3 Reducing HTRB degradation through epitaxial design

The third research axis is epitaxial and buffer engineering. Here, the objective is to reduce the rate of leakage-current increase and the failure rate under HTRB by redesigning only epitaxial growth process without any change in layout and micro/nano fabrication processes. It is achieved by modifying the vertical electric-field distribution in the epitaxial stack and lateral field distribution in the gate edges.

In the first epitaxial variant, the channel GaN thickness is reduced and Carbon concentration in u-GaN is increased with growth conditions. A thinner channel increases the confinement of the 2DEG, leading to a reduction in hot-carrier-induced degradation while preserving RF performance when properly optimized.

In the second variant, an AlGaN back-barrier layer is introduced beneath the

channel. This back barrier enhances vertical confinement of the 2DEG and increases the effective breakdown voltage by decreasing the electric field peaks at the gate edge and in the buffer. Reliability improvement of the HEMTs is proved by time-to-failure measurements at various drain voltages.

The third epitaxial concept is a novel Fe-free ultra-thin barrier design, in which the total buffer thickness is drastically reduced and deep Fe acceptors are removed. The ultra-thin barrier reduces the maximum vertical electric field in the high-field region by roughly a factor of two and enables a more homogeneous potential distribution between the channel and the semi-insulating substrate. In the devices studied here, this architecture leads to 78% improvement in breakdown voltage compared to the standard design, along with a reduction of drain leakage and an improvement in HTRB robustness.

Across all three epitaxial designs, the common theme is the deliberate relaxation and redistribution of the maximum electric field at the gate edge and in the buffer, with the aim of suppressing impact ionization, trap generation, and field-assisted leakage paths that dominate off-state failures.

Overall, this thesis provides a comprehensive reliability analysis framework and a set of practical design and process guidelines for improving the off-state reliability of GaN-on-SiC HEMTs, addressing the dominant field-driven mechanisms identified in Section 1.2. It uses HTRB as the primary stress condition and correlates leakage degradation, breakdown behavior, and failure statistics with specific design and process changes, supported by RF-HTOL tests.

1.4 Thesis Structure

The remainder of this thesis is organized as follows.

Chapter 2 gives an overview of GaN material properties and GaN-on-SiC HEMT device operation. It discusses the epitaxial stack, device structure, and

key design parameters of both micro-/nano-fabrication and epitaxial layers, and describes the GaN-on-SiC HEMT process flow, including epitaxy and device fabrication.

Chapter 3 reviews the main failure mechanisms reported in GaN devices and the underlying leakage-current mechanisms. Particular attention is paid to field-driven degradation paths relevant to off-state and RF stress. This chapter also describes the reliability test systems and methods, and DC/RF measurement methods used in this work. It details the implementation of HTRB and RF-HTOL tests, as well as the characterization setups for DC, small-signal, and large-signal measurements, including pulsed I–V techniques employed to study current collapse.

Chapter 4 shows RF-HTOL results for the baseline technology before the improvements in layout and fabrication methods. Then, breakdown voltage improvement achieved through layout modifications is presented. It introduces a new HEMT design that increases breakdown while preserving RF performance by optimizing critical geometrical parameters.

Chapter 5 reports post-metal annealing process to mitigate Q-point instability. The fabrication-process improvements are described: the new gate pre-treatment method and its duration dependence, the comparison between ICPCVD and PECVD SiN passivation layers and PECVD nitrides deposited at different temperatures, and their impact on leakage current, breakdown voltage, and HTRB failure rate. Then, RF-HTOL performance of the final devices after layout and process developments is presented.

Chapter 6 analyzes the origin of gate degradation under HTRB stress. It identifies the main physical mechanism as impact ionization at the drain-side gate edge, and proposes a buffer-engineering strategy to suppress this effect. Long-term HTRB results are used to demonstrate the resulting leakage-current improvement.

Chapter 7 introduces an epitaxial design incorporating an AlGaN back-barrier

layer. The chapter shows how this design improves breakdown voltage and off-state lifetime by modulating the electric-field distribution at the gate edge. TCAD simulations are used to interpret the observed behavior, and DC, RF, and pulsed I–V measurements are used for experimental validation.

Chapter 8 proposes a novel Fe-free ultra-thin epitaxial design. Its DC, RF, and reliability performances are compared against standard designs. The new architecture achieves approximately 78% improvement in breakdown voltage, 11% increase in output power, 5% increase in saturated drain current, and 15% increase in transconductance, together with an order-of-magnitude reduction in drain leakage and zero failures in HTRB tests over the investigated stress window.

Chapter 9 summarizes the main findings, and highlights the contributions of the thesis. It concludes with a discussion of remaining challenges and outlines several directions for future work in GaN-on-SiC HEMT reliability and device design.

During the preparation of this thesis, I used the large language model ChatGPT (OpenAI, model GPT-5.1 Thinking) as a writing assistant for improving language, restructuring paragraphs, and generating alternative formulations of my own text. The scientific content, results, and conclusions are entirely my own, and all AI-assisted text has been critically checked, edited, or rewritten by me.

Chapter 2

GaN-on-SiC HEMTs Technology Overview: Properties, Design and Process

This chapter summarizes the technological background of the devices studied in this thesis. First, the key material properties of GaN are compared with competing semiconductors to justify the choice of GaN-on-SiC for high-power, high-frequency applications. Then the device structure is introduced, from the epitaxial stack to the micro/nano-fabrication layers, with emphasis on the design parameters that control electric field distribution, leakage, and RF performance. Finally, the epitaxial growth sequence and the main fabrication steps of the GaN-on-SiC HEMTs used in this work are described.

2.1 GaN material properties

Wide-bandgap (WBG) semiconductors such as GaN and SiC enable much higher breakdown fields and operating temperatures than Si or GaAs. Mishra et al. compiled a widely used comparison of material figures of merit for RF power

Table 2.1: Comparison of material properties of Transistor compounds

	Si	GaAs	4H-SiC	GaN	Diamond
E_g (eV)	1.1	1.42	3.26	3.39	5.45
n_i (cm^{-3})	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	1.9×10^{-10}	1.6×10^{-27}
ε_r	11.8	13.1	10	9.0	5.5
μ_n (cm^2/Vs)	1350	8500	700	1200 (Bulk) 2000 (2DEG)	1900
v_{sat} (10^7 cm/s)	1.0	1.0	2.0	2.5	2.7
E_{br} (MV/cm)	0.3	0.4	3.0	3.3	5.6
Θ (W/cm K)	1.5	0.43	3.3–4.5	1.3	20
$Johnson's FOM$	1	2.7	20	27.5	50

devices, including bandgap, critical electric field, thermal conductivity, electron mobility, and saturation velocity for Si, GaAs, 4H-SiC, GaN, and diamond [40]. In that table, GaN combines a large bandgap of about 3.4 eV, a high critical electric field on the order of 3 MV/cm, and a high electron saturation velocity ($\sim 2.5 \times 10^7$ cm/s), leading to a Johnson's figure of merit that significantly exceed those of Si and GaAs and are competitive with 4H-SiC and diamond.

Compared with 4H-SiC, GaN offers higher electron mobility and saturation velocity, which are critical for high-frequency operation, while maintaining a breakdown field only modestly lower than SiC. Diamond surpasses GaN in thermal conductivity and breakdown field, but the lack of mature epitaxy and device technology makes GaN the practical choice for current high-power RF and power-conversion markets.

These material advantages enable GaN transistors to operate at higher drain voltages, higher frequencies, and higher junction temperatures than Si or GaAs devices, while achieving higher efficiency and power density. This is the fundamental reason why GaN, and specifically GaN-on-SiC HEMTs, have become the dominant choice for high-power microwave amplifiers and are increasingly adopted in demanding power-electronics applications.

2.2 GaN-on-SiC HEMT structure

The GaN-on-SiC HEMTs studied in this thesis are lateral AlGaN/GaN devices grown on semi-insulating SiC substrates. A simplified cross-section schematic is shown in Fig. 1.1. Top-view and cross-sectional SEM images of HEMTs are given in Fig. 2.1. Starting from the epitaxial design, the structure consists of a semi-insulating SiC wafer, an AlN nucleation layer, a thick carbon- and iron-doped GaN buffer, unintentionally doped GaN (u-GaN), a thinner channel GaN region, a thin AlN spacer, an AlGaN barrier that hosts the 2DEG at the AlGaN/GaN interface, and an optional GaN cap layer. On top of the epitaxy, Ti/Al/Ni/Au ohmic contacts are formed for source and drain, a Schottky gate is defined in Ni/Au, and the surface is covered by stacked SiN passivation layers that also support source-connected field plates and interconnect metallization.

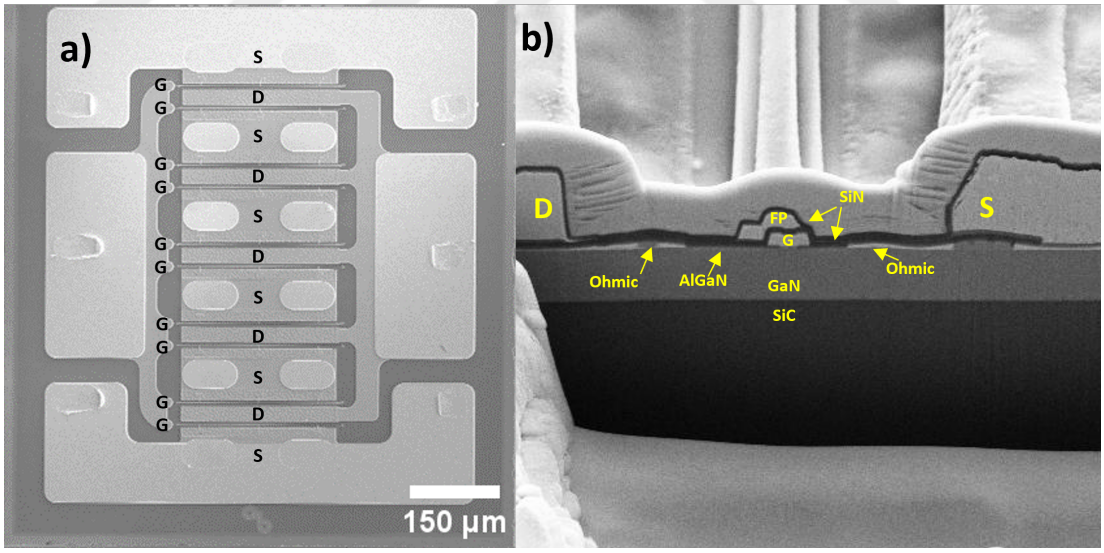


Figure 2.1: SEM images of fabricated GaN HEMTs. a) Top-view image of HEMT. b) Cross-sectional side view image of HEMT.

The 2DEG forms due to strong spontaneous and piezoelectric polarization discontinuities between the AlGaN barrier and the underlying GaN channel. 2DEG formation is shown in Figure 2.2. Figure 2.2(b), the band diagram through the cut-line shown in Figure 2.2(a), shows that band at the interface stays below Fermi level and creates 2DEG. The sheet charge density and mobility of the 2DEG are controlled by the barrier composition and thickness, the presence of

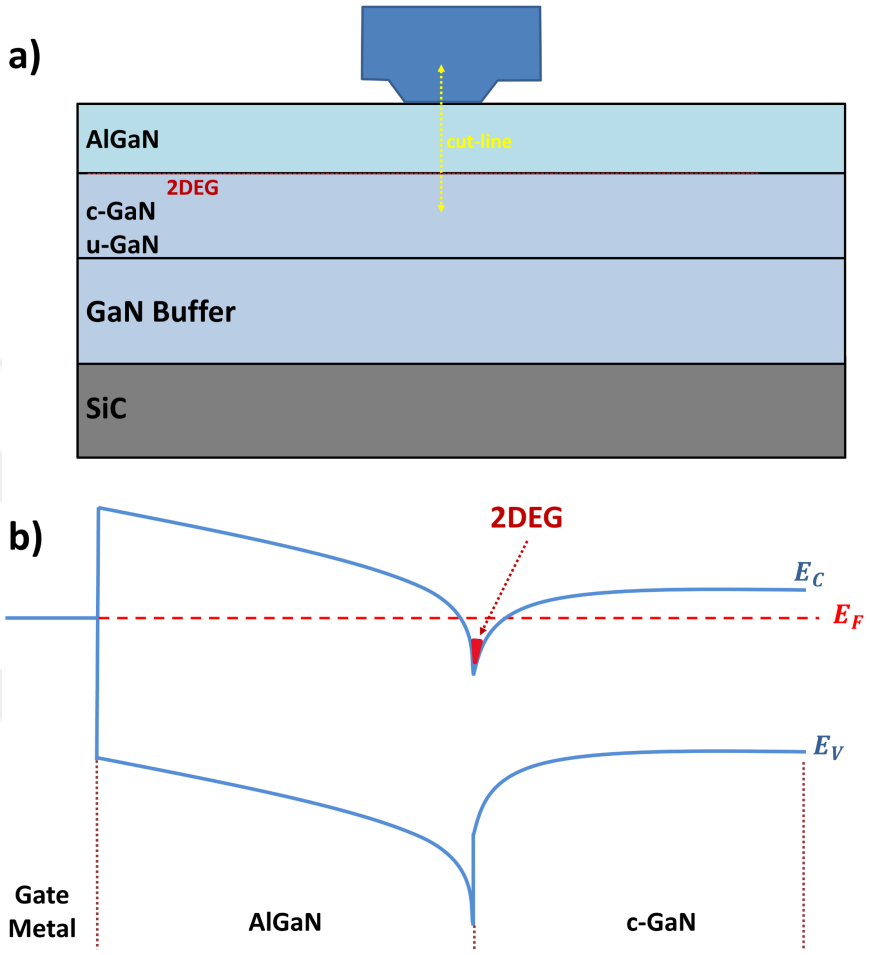


Figure 2.2: 2DEG formation at AlGaN/GaN interface. a) Cut-line for the band diagram. b) Band diagram of metal–AlGaN–GaN stack and 2DEG formation.

spacer and cap layers, and the quality of the buffer. At the same time, breakdown voltage and leakage are strongly influenced by the vertical and lateral electric-field distribution, which depends on the buffer design, barrier profile, and the geometry of the gate, field plates, and passivation layers.

The remainder of this section discusses the design parameters of the epitaxial layers and the micro/nano-fabrication stack, with emphasis on their impact on device performance and reliability.

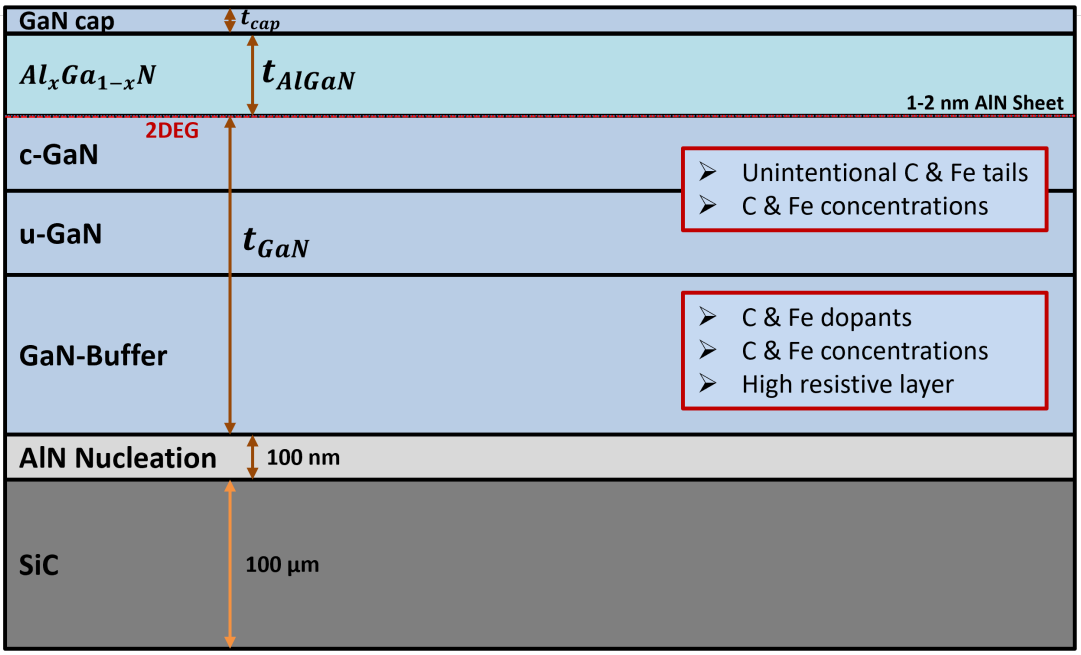


Figure 2.3: Epitaxial stack of a standard GaN-on-SiC HEMT and epitaxial design parameters

2.2.1 Roles and design parameters of Epitaxial layers

Figure 2.3 illustrates the epitaxial stack and the main epitaxial design parameters considered in this work: doping concentrations in the GaN buffer (C, Fe), u-GaN and c-GaN layer thicknesses (t_{GaN}), AlGaN barrier thickness (t_{AlGaN}) and Al mole fraction x, AlN spacer thickness, and GaN cap thickness (t_{cap}).

SiC substrate: Semi-insulating 4H-SiC provides high thermal conductivity (∼3–4.5 W/cm·K) and good lattice match to GaN, enabling low thermal resistance and relatively low threading dislocation density compared with GaN-on-Si.

AlN nucleation layer: A thin AlN nucleation layer accommodates lattice and thermal-expansion mismatch between GaN and SiC, suppressing cracking and reducing dislocation density in the overgrown GaN buffer.

C/Fe-doped GaN buffer: The thick GaN buffer is intentionally compensated with deep acceptors such as carbon and/or iron to achieve highly resistive

buffer, which suppresses parasitic conduction, and supports high breakdown voltage.

Unintentionally doped GaN (u-GaN) and channel GaN: These layers separate the heavily doped buffer from the 2DEG, limiting the diffusion of C/Fe trapping centers towards the channel and determining the vertical position of the 2DEG. Their thickness and strain affect both the 2DEG and the vertical field distribution.

AlN spacer: A very thin AlN interlayer between GaN and AlGaN increases confinement and can enhance 2DEG density and mobility by separating the channel from interface roughness and alloy disorder, provided the spacer is not too thick.

AlGaN barrier: The AlGaN layer provides the polarization charges that induce the 2DEG. Its thickness and Al content directly set the sheet charge density, threshold voltage, and maximum drain current, and also influence breakdown through the surface and interface fields.

GaN cap: A thin GaN cap protects the AlGaN surface from oxidation, also can be used to adjust surface charges, threshold voltage, gate leakage mechanisms and RF performance.

The following paragraphs discuss how each key epitaxial parameter affects device performance and reliability.

2.2.1.1 Carbon and iron concentrations in the buffer

Carbon and iron are widely used to compensate the GaN buffer and obtain semi-insulating behavior. Increasing the concentration of C or Fe in the buffer generally raises resistivity, suppresses buffer leakage, and improves breakdown by increasing the potential barrier under the channel. However, these deep acceptors also introduce traps that contribute to current collapse and dynamic R_{on} degradation, especially when the compensation is excessive.

Carbon and iron have different trap spectra and diffusion behavior. Fe creates deep acceptor levels (typically ∼0.5–0.6 eV below the conduction band) that are very effective in compensating residual donors, but Fe can diffuse along dislocations and towards the channel if growth conditions are not carefully controlled. Carbon, often introduced via intentional C doping or via growth conditions, tends to generate a distribution of deep traps that are strongly involved in buffer-related current collapse.

Gao et al. systematically compared HEMTs with different carbon concentrations and showed that higher C levels reduce off-state leakage and increase breakdown, but also enhance trapping and degrade dynamic performance under pulsed bias and OFF-state stress [41]. Similar trends are reported for Fe-doped buffers: heavy Fe doping greatly increases buffer resistivity and breakdown voltage, but Fe diffusion towards the channel can degrade mobility and increase gate leakage [42].

Comparative studies of C-only, Fe-only and C/Fe co-doped buffers show that, at similar total compensation, Fe-dominated buffers usually exhibit higher breakdown voltage and lower vertical leakage, while C-dominated buffers show stronger trapping and dynamic R_{on} degradation [43]. When C concentration is significantly larger than Fe, the buffer tends to be more resistive but also more trap-rich, leading to pronounced current collapse and long recovery times under high-field OFF-state stress, which is detrimental for HTRB reliability.

Conversely, Fe-rich buffers, especially when Fe is introduced deeper from the channel, can reduce current collapse and improve static and pulsed I–V characteristics, but may exhibit higher gate leakage due to field crowding and Fe-related traps near the surface if Fe tails extend too close to the 2DEG.

2.2.1.2 Thickness and doping of u-GaN and channel GaN

The thickness of the unintentionally doped GaN layer between the compensated buffer and the channel is a key handle on Fe/C "tails" and on the vertical electric-field distribution. Studies on AlGaN/GaN HEMTs with different u-GaN thicknesses show that thicker u-GaN effectively keeps the channel away from Fe tails, leading to higher breakdown voltage at the cost of slightly increased vertical capacitance [44].

Channel GaN thickness affects 2DEG confinement and impact-ionization volume. Too thin a channel can reduce mobility due to enhanced interface roughness scattering and strain relaxation, whereas too thick a channel increases the vertical extent of the high-field region, enhancing impact ionization and buffer-related degradation under OFF-state stress [44, 45]. Several recent works on thin-GaN and tensile-GaN buffers confirm that careful thinning can improve breakdown and reduce current collapse if the buffer design is appropriate [46, 47, 4]. These trade-offs are directly exploited in the thinner-channel and ultra-thin-buffer epitaxial designs discussed in later chapters.

2.2.1.3 AlGaN barrier thickness

The AlGaN barrier thickness t_{AlGaN} strongly influences 2DEG density, threshold voltage, and transconductance. Increasing t_{AlGaN} increases polarization charge and thus the 2DEG sheet density, enhancing maximum drain current but shifting the threshold voltage more negative and increasing gate-to-channel separation [48].

From a reliability perspective, thicker barriers also modify the surface electric field and can either improve or degrade breakdown depending on the field-plate configuration and passivation [4]. Recent designs using graded AlGaN barriers show that tailoring the barrier profile can significantly enhance breakdown without sacrificing 2DEG confinement [49].

2.2.1.4 Al mole fraction in AlGaN

The Al content x in $Al_xGa_{(1-x)}N$ sets the magnitude of polarization charges and thus the 2DEG density. Increasing x increases the polarization discontinuity and 2DEG sheet charge, leading to higher current capability and lower on-resistance but also more negative V_{th} and higher electric-field concentration at the barrier surface and gate edge [50, 51]. For RF power HEMTs, moderate Al contents (20–30%) are commonly used as a compromise between high 2DEG density, manageable gate leakage, and acceptable breakdown voltage [52].

2.2.1.5 AlN spacer thickness

A thin AlN spacer between GaN and AlGaN reduces alloy scattering and can increase mobility and drain current if optimized. Numerical and experimental studies report an optimum AlN thickness around 0.5–1.5 nm, where 2DEG density and mobility are maximized [53, 54]. Thicker spacers begin to increase series resistance and contact resistance and reduce mobility and drain current due to enhanced scattering. In this work, AlN spacer thickness is kept in the typical 1–2 nm range to balance these effects.

2.2.1.6 GaN cap thickness

The GaN cap thickness is another important design parameter. A few-nanometer GaN cap protects the AlGaN from oxidation, improves surface morphology, and can enhance sheet charge and mobility. Nie et al. fabricates transistors with various cap layer thicknesses from uncapped to 5 nm thick [55]. Thicker cap decreases saturation current; however, effectively improves the off-state characteristics, which are gate and drain leakage currents and breakdown voltage. The optimal cap layer is found as 3 nm in this work.

Another work reports that the presence and thickness of the GaN cap alter tunneling paths and trap-assisted leakage at the gate edge, affecting both gate

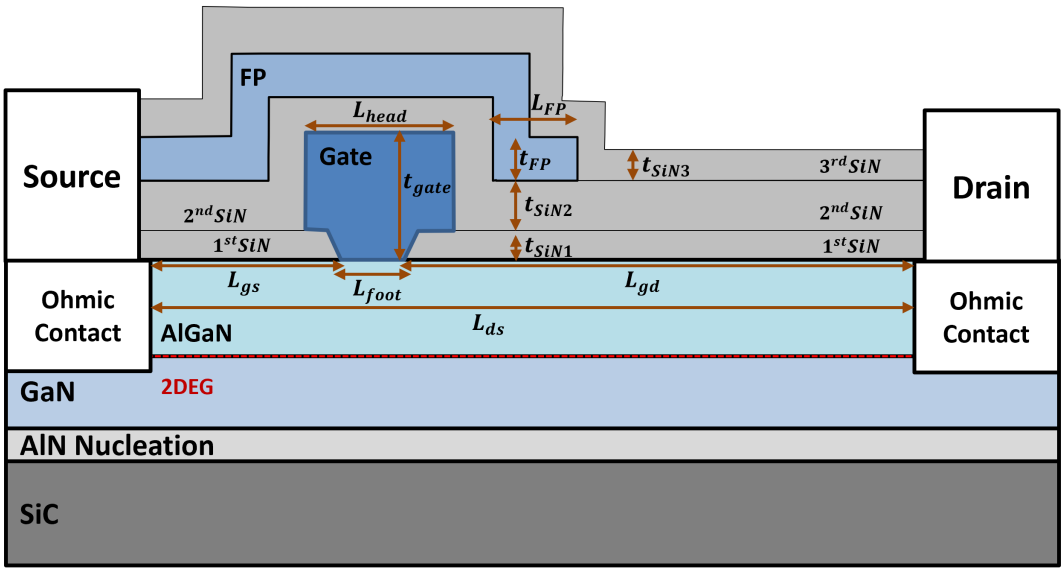


Figure 2.4: Schematic of GaN HEMT cross-section with design parameters.

breakdown and threshold-voltage stability under stress [56].

2.2.2 Roles and design parameters of micro/nano fabrication layers

Figure 2.4 shows a schematic cross-section of the fabricated HEMTs with the main process defined layers and geometrical parameters, which are stacked SiN passivation layers (SiN-1, SiN-2, SiN-3), the T-shaped gate (gate foot and gate head), source-connected field plate, interconnect metallization levels (MET-1, MET-2) in drain and source pads.

The following paragraphs outline the roles of these layers, main geometrical design parameters and their impact on performance.

2.2.2.1 Thicknesses of first, second, and third SiN layers

The total SiN thickness above the AlGaN surface and between the gate, field plate, and drain largely determines the electric-field distribution and the magnitude of surface trapping. Reported works show that increasing SiN thickness initially reduces surface fields and suppresses current collapse, but excessively thick SiN can move the peak field to the drain edge and induce cracking or high stress [57].

Bilayer or multi-layer SiN stacks with different stress and composition can mitigate these trade-offs [58]. For example, dual-layer SiN stressor passivation has been shown to dramatically reduce current collapse and improve RF performance by engineering the interface charge and stress profile. In this thesis, SiN-1 primarily isolates the AlGaN surface and sets the field-plate distance, SiN-2 supports the field plate, and SiN-3 provides additional passivation and mechanical protection; their thicknesses are adjusted to balance breakdown, trapping, and mechanical integrity.

2.2.2.2 Gate-to-source distance L_{gs}

Reducing the gate-to-source spacing decreases source access resistance, increases transconductance, and can improve f_{T}, but at the cost of higher gate-to-source capacitance [57, 59].

2.2.2.3 Gate-to-drain distance L_{gd} and drain-to-source distance L_{ds}

The gate-to-drain spacing L_{gd} is one of the primary parameters for breakdown voltage and off-state reliability. Larger L_{gd} spreads the lateral electric field and raises breakdown voltage, but increases on-resistance, chip area, and output capacitance. Two-dimensional simulations and measurements show that breakdown voltage approximately scales with L_{gd} up to a technology-specific limit set by

buffer and surface breakdown, after which further scaling yields diminishing returns [57, 60].

The total drain-to-source spacing L_{ds} similarly affects the trade-off between breakdown and on-resistance. It has to be determined by device specifications.

2.2.2.4 Gate foot length and gate head length

The gate foot defines the effective channel length and thus directly impacts f_T, f_{max}, transconductance, and short-channel effects. Aggressive scaling of the gate foot into the sub-200-nm regime significantly increases f_T and f_{max} but intensifies short channel effects [61]. Therefore, it requires careful field-plate and buffer design to maintain breakdown.

The gate head length in a T-gate controls gate resistance and the overlap of the "head" over the field plate or access regions. Extending the gate head reduces gate resistance and can improve f_{max} and large-signal performance, but increases gate-to-drain capacitance and may lower breakdown due to enhanced field coupling [59].

2.2.2.5 Gate metal thickness

Gate metal thickness primarily affects gate resistance, self-heating in the gate, and the vertical electric-field distribution at the gate edge. A thicker gate reduces sheet resistance and improves f_{max}, especially in multi-finger devices, but also increases process complexity and step height [59]. Increasing gate height can also increase breakdown voltage at the expense of larger parasitic capacitances [61].

2.2.2.6 Field plate length and thickness

Field plates are one of the most powerful design tools for controlling the peak electric field in GaN HEMTs. The length of the field plate over the drain access region and the thickness of the underlying dielectric determine where the electric-field peaks occur and how strongly they are reduced. Analytical and numerical studies show that there is an optimum combination of field-plate length and insulator thickness that maximizes breakdown voltage while minimizing additional capacitance [62, 57].

2.3 GaN-on-SiC HEMT process flow

Figures 2.5 summarizes the process flow and the resulting device cross-section. The process is divided into epitaxial growth and micro/nano-fabrication. First crystal GaN epitaxy is growth on SiC substrate, then contacts, metallic and dielectric layers are fabricated.

2.3.1 Epitaxial growth

The epitaxial structures are grown by metal-organic chemical vapor deposition (MOCVD), which is the dominant industrial technique for GaN HEMT epitaxy. Trimethylgallium (TMGa) and trimethylaluminium (TMAl) are used as group-III precursors for GaN and AlGaN, respectively, with ammonia (NH_3) as the nitrogen source. Hydrogen and/or nitrogen act as carrier gases.

Epitaxial layers are shown in Figure 2.3. Growth starts with high-temperature AlN nucleation on the semi-insulating 4H-SiC substrate, typically at temperatures above 1100 °C and high V/III ratios, to form a high-quality crystal and to manage strain. A relatively thick GaN buffer is then grown at lower temperature to reduce dislocations and provide a platform for subsequent layers.

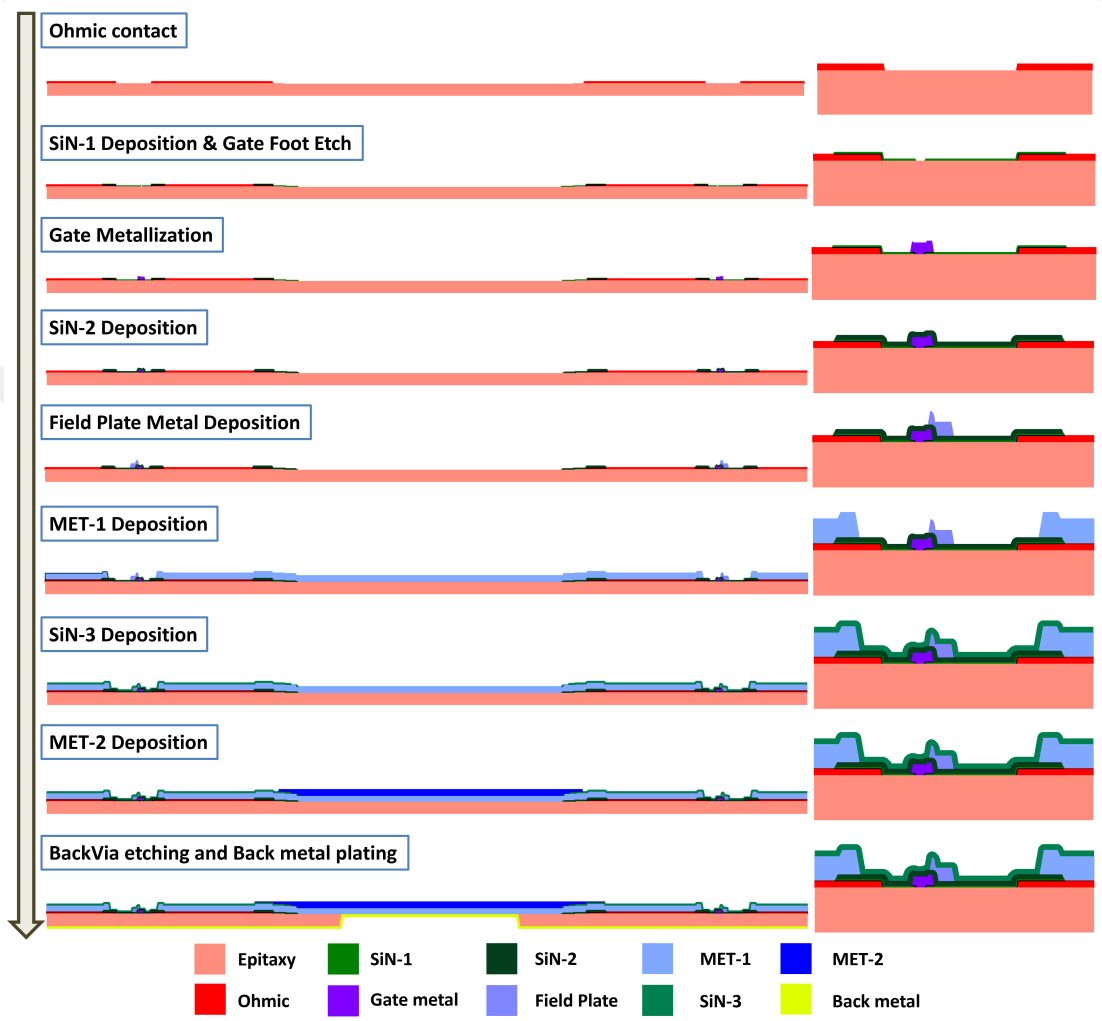


Figure 2.5: Main process steps of GaN-on-SiC HEMTs.

Carbon doping is introduced either intentionally via carbon-containing precursors or by adjusting growth temperature and V/III ratio. Fe doping is achieved using cyclopentadienyl-iron (Cp_2Fe) or similar precursors.

Above the compensated buffer, u-GaN and channel GaN layers are grown with carefully controlled thickness to achieve the desired separation between the doped buffer and the 2DEG. A very thin AlN spacer is deposited next, followed by the AlGaN barrier with target Al content and thickness chosen for the required 2DEG density and threshold voltage. Finally, a thin GaN cap is grown at reduced temperature to avoid decomposition and to stabilize the surface.

Throughout the epitaxial process, in-situ monitoring (e.g. reflectometry) and ex-situ characterization (XRD, PL, Hall measurements) are used to calibrate layer thicknesses, compositions, and electrical properties. The epitaxial design variants explored in later chapters (thinner channel, AlGaN back barrier, ultra-thin buffer) all follow this general growth sequence, with modified thicknesses, temperatures and doping profiles.

2.3.2 Micro/nano fabrication

The device fabrication follows a conventional AlGaN/GaN HEMT process with Au-based metallization, summarized in Figure 2.5. The main steps are:

Ohmic contact formation: Ti/Al/Ni/Au ohmic metal stacks are deposited by e-beam evaporation or sputtering, and annealed at ∼875 °C in N_2 to form low-resistance contacts to the 2DEG.

First SiN deposition (SiN-1) and gate foot etch: A first SiN layer is deposited by CVD (PECVD, ICPCVD or LPCVD) to passivate the surface. The gate foot opening is then defined by electron beam lithography, and etched through SiN-1 using fluorine-based plasma chemistry such as CF_4/O_2, stopping on the AlGaN barrier.

Gate metallization: The Schottky gate metal (Ni/Au) is deposited by PVD and patterned, forming the gate foot and gate head (T-gate). Gate recess or additional treatments can be included if required by the design. The gate defines the channel length and strongly influences breakdown and V_{th}.

Second SiN deposition (SiN-2): A second SiN layer is deposited to encapsulate the gate and form the dielectric under the source-connected field plate. Its thickness sets the gate-to-field-plate spacing and thus the degree of field modulation.

Field plate metal deposition: Ti/Au field-plate metal is deposited and

patterned to extend from the source over the gate edge and partially over the drain access region, as shown in Figure 2.4. This step is crucial for controlling peak electric fields and improving breakdown.

First interconnect metallization (MET-1): A thicker metal level (e.g. Ti/Au) is deposited to connect the device pads and route signals.

Third SiN deposition (SiN-3): A top SiN layer is deposited to protect the interconnects and to further passivate the surface. Openings for pads and vias are etched subsequently.

Second interconnect metallization (MET-2): An additional thick metal layer may be added for low-loss RF routing, power combining structures, or pad reinforcement, as indicated.

Back via etching and back metal plating: Finally, vias are etched from the backside through the SiC substrate typically using plasma etching, to reach the source ohmic contacts. Ni/Au back metal is then formed by electroplating to create a low-impedance ground. Back vias connect all source pads and make them common.

This process flow yields the multi-layer structure illustrated in Figures 2.3–2.5. The subsequent chapters build on this technological baseline, systematically modifying epitaxial, layout, and process parameters to improve breakdown voltage and off-state reliability under HTRB and RF-HTOL stress.

Chapter 3

Failure Mechanisms, Reliability Tests and Measurement Methods

This chapter first focuses on field-driven failure mechanisms that are critical for GaN-on-SiC HEMTs under high electric field. Then the Accel-RF AARTS reliability systems and the DC-HTOL, HTRB and RF-HTOL test methods used in this work are introduced. Finally, the DC, RF small-signal, RF large-signal and pulsed I–V measurement setups are described briefly.

3.1 Failure Mechanisms of GaN HEMTs

3.1.1 Electric-field Distribution and Peak Points

Figure 3.1(a) shows a TCAD electric-field simulation of the reference GaN-on-SiC HEMT under deep OFF-state bias (i.e., $V_{GS} = -8$ V, $V_{DS} = 100$ V). In the 2D map, the lateral field peaks occur at the drain-side edge of gate foot and gate head, and at edge of the field plate. The accompanying lateral field profile in the AlGaN barrier (Figure 3.1(b)) confirms that, if one looks only inside the AlGaN, the maximum field appears first under the gate foot (i.e., peak a), then under the

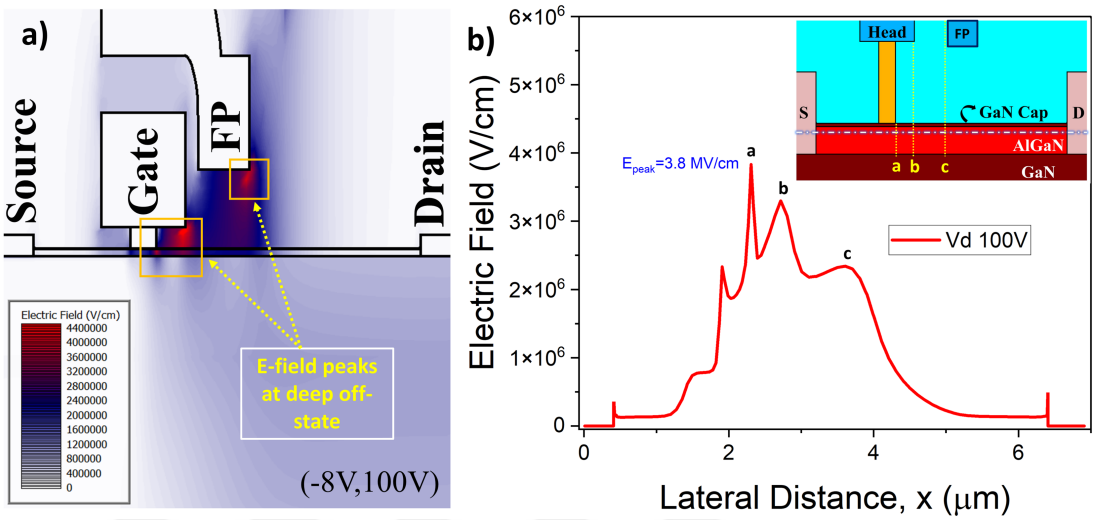


Figure 3.1: E-field profiles at deep off-state in GaN HEMT. (a) E-field distribution in 2D map. (b) E-field inside AlGaN layer through the cut-line at inset picture.

gate head (i.e., peak b), and then under the field plate edge (i.e., peak c). These regions are therefore the most vulnerable to field-driven failure mechanisms such as impact ionization, hot-electron-induced damage, time-dependent breakdown and accelerated gate leakage. Similar field distributions and failure hot-spots have been reported in a number of TCAD and experimental studies on RF GaN HEMTs.

In addition, high vertical field exists across the AlGaN barrier under the gate and under the field plate, and across the GaN buffer underneath the gate-drain region. This vertical field controls gate leakage, tunneling and buffer leakage paths, and drives trapping/detrapping dynamics that give rise to current collapse and dynamic on-resistance.

3.1.2 Impact Ionization

A band-diagram sketch of the impact-ionization mechanism is shown in Figure 3.2. Under large drain bias in OFF-state, the lateral electric field peaks at the drain-side gate edge. Electrons travelling in the 2DEG are accelerated in this region and can gain kinetic energy comparable to or larger than the GaN

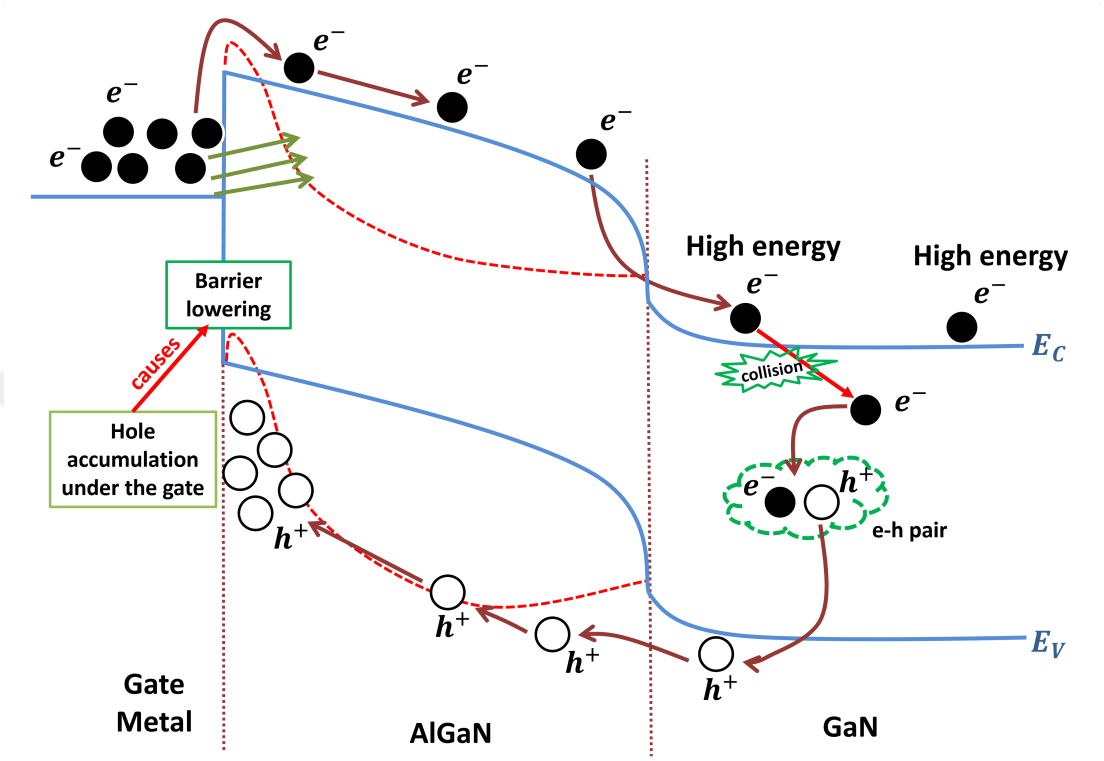


Figure 3.2: Impact ionization mechanism in GaN HEMTs.

band gap. When these hot electrons collide with the lattice, they can generate electron–hole pairs by impact ionization.

There are three key features in impact ionization mechanism. The collision takes place in GaN, just below the AlGaN/GaN interface, which corresponds to the maximum lateral field region. The created holes move in the valence band of AlGaN and GaN, and drift back towards the gate (against the electron flow) and accumulate in the AlGaN barrier under the Schottky gate. These local positive charges partially cancel the negative gate bias, and effectively lower the Schottky barrier (red dashed line in the band diagram). This results in more electron tunneling in the barrier, more collision and hole accumulation, which creates positive feedback.

Impact ionization contributes to time-dependent drain-source breakdown and catastrophic failure under HTRB conditions, permanent increase of gate leakage and soft breakdown at the drain-side gate edge, and threshold-voltage shift

through modification of the barrier potential profile significantly.

Solutions reported in the literature basically focus on improving breakdown voltage by field relaxation at the peak positions. Field-plate optimization and longer gate-to-drain spacing are used to spread the field and reduce the peak at the gate edge [63, 64]. Back-barrier or graded buffer designs that confine the field deeper in the buffer and reduce the electron energy near the channel are also proposed [49, 65]. Chapter 6 of this thesis also presents work to mitigate impact ionization observed during HTRB test.

3.1.3 Hot Electron Trapping

Figure 3.3 illustrates hot-electron trapping paths during operation. Electrons flowing in the 2DEG under large electric field gain high kinetic energy and can be scattered into AlGaN/GaN interface traps near the drain-side gate edge, SiN/AlGaN interface traps under the passivation, and deep-level acceptors in the GaN buffer (C, Fe and related complexes). These electrons can be captured by the traps or even can generate new traps if they have sufficiently high energy. Both TCAD-based and experimental studies reveal that hot electron trapping causes dynamic on-resistance increase, drain current collapse, transconductance drop, threshold-voltage shifts, and long-term degradation of leakage currents and breakdown [33, 66, 67, 68, 69, 70].

Common techniques to prevent hot electron mechanisms are based on improving SiN/AlGaN interface quality to reduce trap density [71], optimizing buffer doping and thickness to reduce deep acceptor concentration and to minimize trapping volume [72, 73] and to reduce the electric field [74, 75] for less hot electron generations in the HEMT.

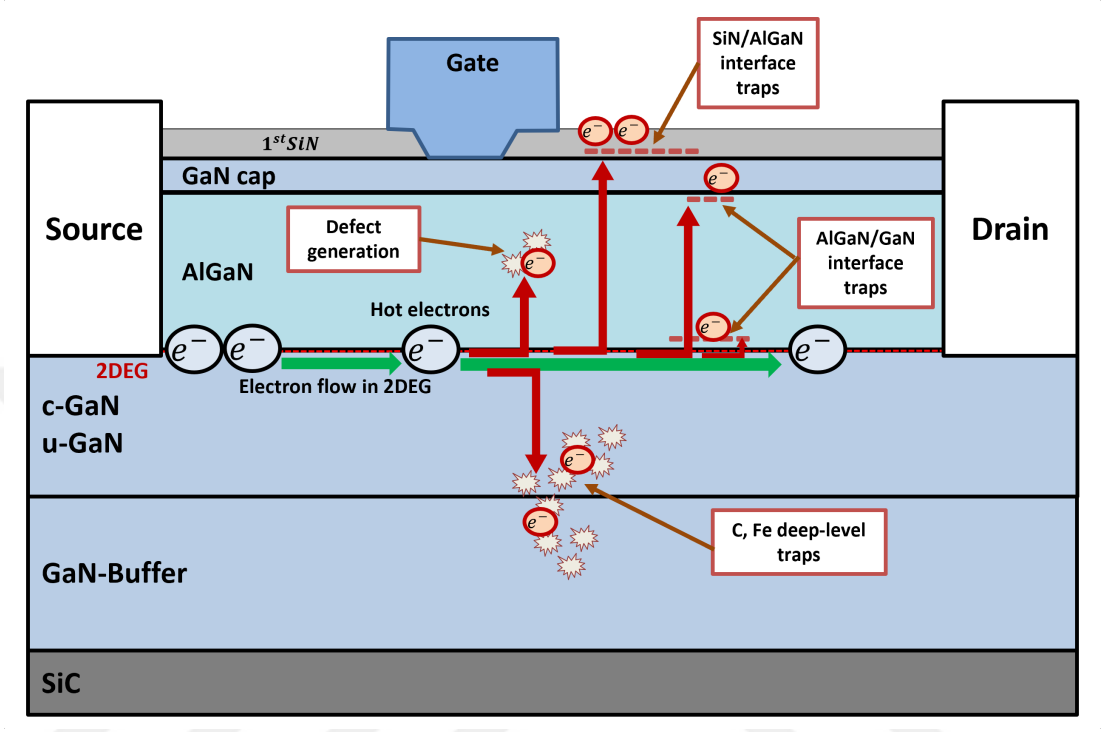


Figure 3.3: Hot electron effects in GaN HEMTs: trapping at AlGaN interfaces with SiN and GaN, and in the buffer dopants, and new defect generation.

3.1.4 Leakage Current Mechanisms

There are multiple ways of leakage paths in GaN HEMTs. Gate electrons can pass over the AlGaN barrier from gate into the 2DEG when the gate is forward-biased or electrons have sufficient thermal energy, which is called thermionic emission. Electrons can tunnel via one or multiple trap levels in the AlGaN under reverse bias, which is called trap-assisted tunneling (TAT)[76, 77].

Electrons can move laterally along the passivated surface via hopping between surface states, which is called surface leakage. Or, if the SiN is defective, current can flow through it, especially at high field regions. And, source electrons can travel laterally and vertically through deep acceptor traps in the buffer and transition layers. Figure 3.4 schematically summarizes these main leakage paths. All of these mechanisms are strongly field-dependent and are accelerated at the high field regions shown in Figure 3.1.

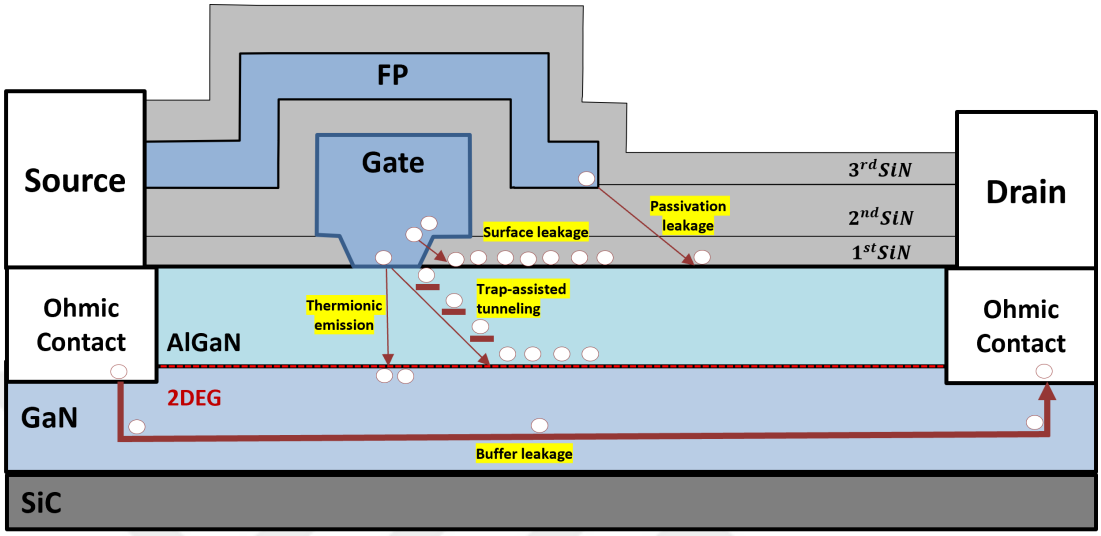


Figure 3.4: Common leakage current mechanisms in GaN HEMTs.

3.2 Reliability Tests and Long-term Test Systems

Figure 3.5 shows the Accel-RF DC-96 and RF-16 Automated Accelerated Reliability Test Station (AARTS) systems used in this work. These are commercial platforms designed for long-term reliability testing of RF and power compound-semiconductor devices with controlled DC, RF and thermal stress.

Each system consists of multiple individually controlled stress channels with programmable bias and temperature, an embedded semiconductor parameter analyzer (SPA) (i.e., Keithley 2612 source meter) used for interim DC characterization (I–V, leakage, transfer curves) during stress, and control software for automated stress/measure cycles and lifetime statistics extraction. The DC-96 AARTS is used primarily for DC-HTOL and HTRB tests, while the RF-16 AARTS provides RF, DC and thermal control capability simultaneously to mimic realistic operating conditions on packaged devices.

In this thesis we use three main long-term tests: DC-HTOL (High-Temperature Operating Life), HTRB (High-Temperature Reverse Bias), and RF-HTOL (RF-biased High-Temperature Operating Life). The general concepts of

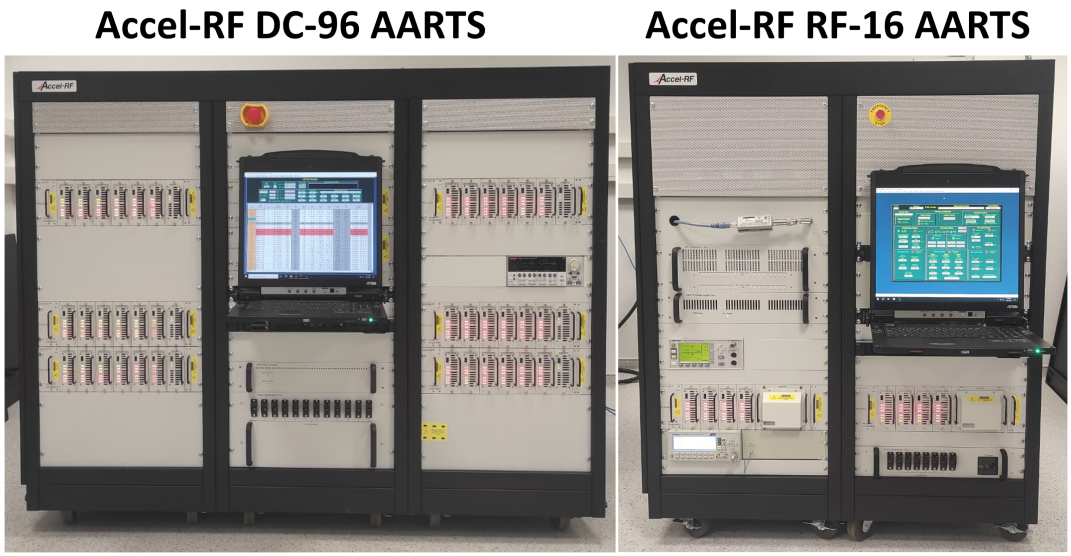


Figure 3.5: Accel-RF company DC-96 and RF-16 AARTS test systems.

these tests are briefly introduced below.

3.2.1 DC-HTOL

In DC-HTOL the device is biased close to a realistic Q-point in semi-ON state, typically at high drain voltage and significant drain current so that the channel temperature is elevated well above ambient. This test accelerates thermally and electrically activated failure mechanisms.

Two bias strategies are commonly used: constant current (or power) and constant voltage HTOL. In constant current test, the drain current is kept constant, and the gate voltage is regulated over time to maintain the target current as the device degrades. This keeps the channel temperature nearly constant, which is important because temperature is the dominant acceleration factor in GaN HEMTs. In constant voltage test, gate and drain voltages are fixed. As the device degrades, the drain current and junction temperature can decrease. This is simpler to implement but less controlled from an Arrhenius-acceleration-factor point of view. In this work, the constant-current approach is preferred to maintain a well-defined channel temperature and obtain reliable activation energies

for degradation processes.

DC-HTOL provides information on parametric drifts in on-resistance, transconductance, threshold voltage, and gate and drain leakages under on-state or semi-on bias. It is one of the standard qualification tests defined in many reliability standards, and it is widely used for GaN power and RF devices.

3.2.2 HTRB

In HTRB, the devices are held in deep OFF-state stress at elevated temperature and at a drain voltage typically in the range 2.5–3$\times V_{\mathrm{DD}}$, often close to breakdown voltage. For RF GaN PAs, this approximately corresponds to the maximum drain swing at the peak of RF cycle, and beyond. Therefore, HTRB directly probes the worst-case electric-field conditions relevant for real operation.

The main stress conditions are:

- V_{GS} is well below threshold voltage (e.g. -8 V),
- V_{DS} is at high reverse bias (around $3 \times V_{\mathrm{DD}}$),
- chuck temperature is typically 150 °C.

HTRB is the most relevant test for field-driven failure mechanisms discussed in Section 3.1. It creates a continuous high electric field inside HEMT, and triggers the above mechanisms. During HTRB, gate and drain leakage increase, time-dependent breakdown, hot-electron and impact-ionization induced degradations, and current collapse are observed. HTRB results (failure rate and leakage evolution) are used as primary metrics to compare different layouts, fabrication processes and epitaxial designs to assess off-state reliability.

3.2.3 RF-HTOL

RF-HTOL (RF-biased High-Temperature Operating Life) is a standard reliability test in which devices are operated under large-signal RF excitation and elevated temperature. Under such conditions, the devices experience repeated stress in the on-state, semi-on state and off-state within each RF cycle, making RF-HTOL the closest laboratory approximation to real operating conditions for power amplifiers. Devices are biased at nominal supply voltage and quiescent current. An RF input signal is applied so that the device operates in a specific compression (e.g. 3 dB gain compression) or output power and efficiency. The junction temperature under RF reaches values well above ambient (e.g., 200–250 °C).

In RF-HTOL test, gain and output-power degradation due to dynamic R_{on} and trapping, and catastrophic failures under realistic RF stress are monitored.

3.3 Measurement Systems

In this section, DC and RF measurement systems used for characterizing the devices are introduced.

3.3.1 DC Measurement

DC characteristics of devices are measured using a Keysight B1505A Power Device Analyzer / Curve Tracer. The B1505A includes high-voltage and high-current source/monitor units (SMUs) capable of up to 200 V/1 A and 40 V/20 A depending on options. It has fast pulsed measurement capability down to ~ 10 μs pulse width, $\mu\Omega$-level on-resistance resolution and sub-pA current resolution, and capacitance measurement units for C–V measurements.

The schematic of the common setup we used is given in Figure 3.6. SMU1 and SMU2 are typically connected to gate and drain, respectively. The common

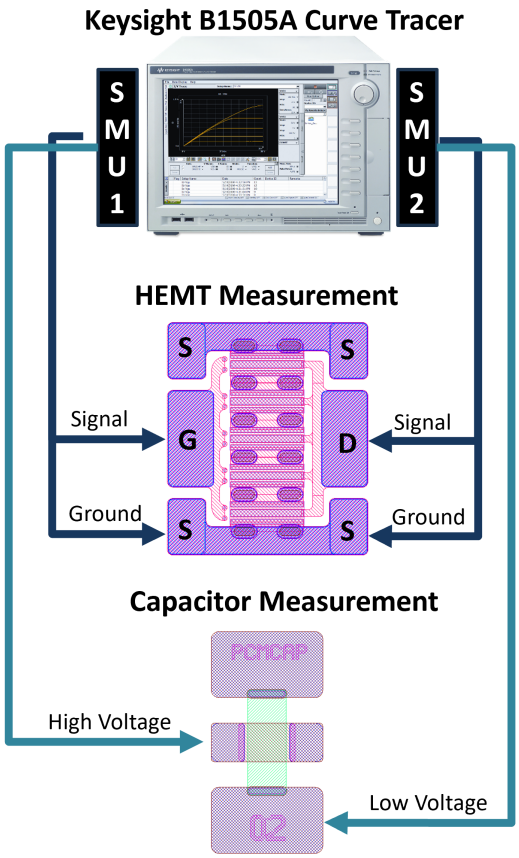


Figure 3.6: On-wafer DC measurement setup used for measuring HEMT and capacitor.

source pads are grounded through the chuck and/or a dedicated probe. For capacitor test structures, the SMUs are used as high and low voltage sources.

On-wafer measurements use GGB Industries GSG-150 and GSG-250 RF probes for the RF pads, and needle probes where needed for additional contacts. Standard DC characterizations include:

- output I–V (I_{D}–V_{DS} at fixed V_{GS}),
- transfer I–V (I_{D}–V_{GS} at fixed V_{DS}),
- Schottky contact characterization at zero V_{DS},
- gate and drain leakage versus voltage under off-state.

The packaged devices can also be measured with B1505A using an evaluation board. Also, they are periodically measured during long-term stress using the SPA integrated in the Accel-RF systems.

3.3.2 RF Small-signal (S-parameter) Measurement

Small-signal RF characterization is carried out with a Keysight PNA-X vector network analyzer configured as a 2-port system, as shown in Figure 3.7. The key components are:

- the PNA-X providing the RF sources and receivers at ports P1 (input) and P2 (output),
- bias tees on gate and drain lines to superimpose RF signals on the DC bias,
- DC power supplies to bias gate and drain,
- GSG probes for on-wafer measurement.

The standard procedure is:

- Full 2-port SOLT calibration on a GGB CS-5 calibration substrate (open, short, load, thru standards) is performed up to the target frequency range.
- Power supplies are used to bias the device at the desired Q-point (combinations of V_{DS} and V_{GS}, to provide required drain current).
- Measurement of S-parameters using PNA over the required frequency band.

From these data, small-signal gain, stability factors, and extracted parameters such as f_{T}, f_{max}, and small-signal models are obtained.

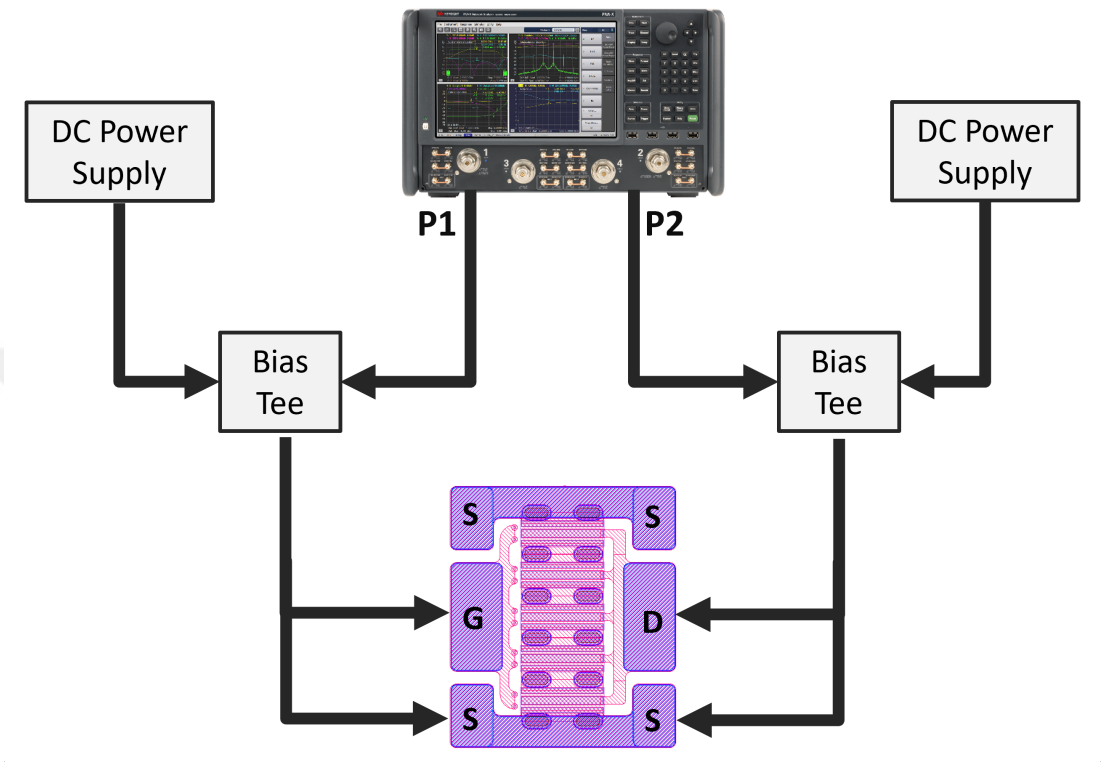


Figure 3.7: The schematic of small-signal RF measurement setup.

3.3.3 RF Large-signal (Load-pull) Measurement

Large-signal RF measurements (fundamental load-pull) are performed using the setup sketched in Figure 3.8. The main building blocks are:

- a PNA-X or signal generator/analyzer acting as RF source and receiver (4 ports),
- tunable passive or active tuners at the input and output to present controlled source and load impedances to the device,
- an RF driver amplifier to reach the desired input power levels,
- directional couplers for incident/reflected power monitoring,
- high-power attenuators and terminations where needed,
- bias tees and DC power supplies for gate and drain biases.

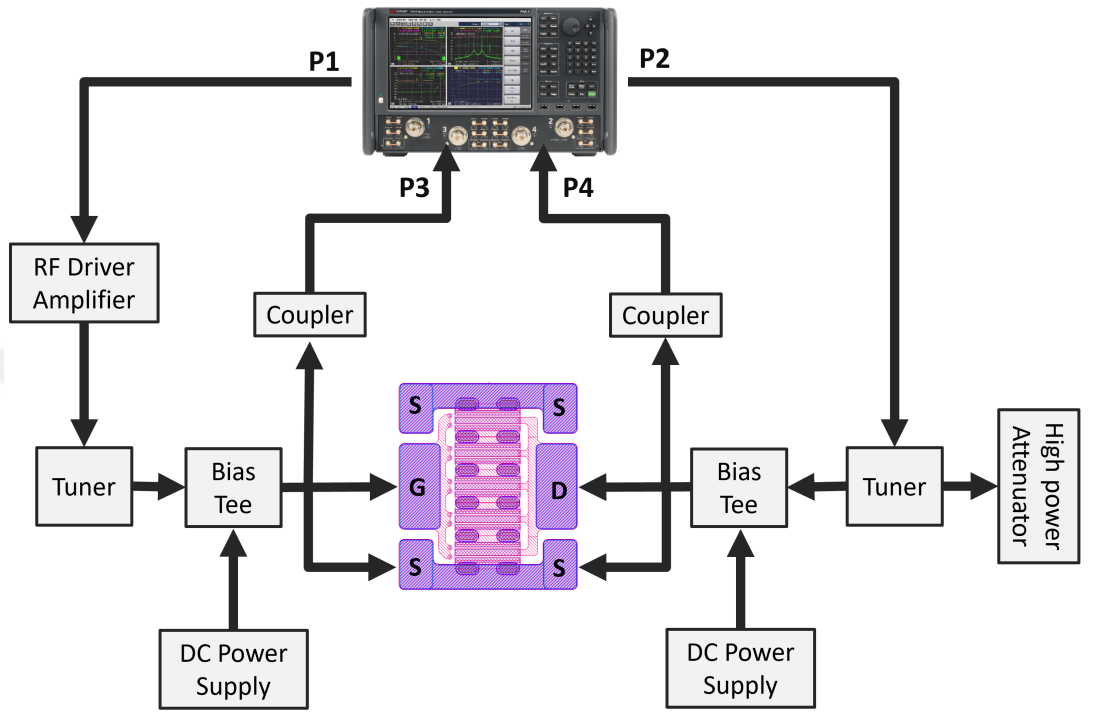


Figure 3.8: The schematic of RF load-pull measurement setup.

The device is biased at the target Q-point (e.g. Class AB) and then excited with an RF power sweep. For each load impedance condition, the output power, gain and efficiency versus input power are recorded. This setup is used for performing on-wafer characterizations.

3.3.4 Pulsed I–V Measurement

Pulsed I–V measurements are essential to separate intrinsic device behavior from trapping-induced current collapse. The pulsed bias sequences used here are illustrated in Figure 3.9:

- In the I_{D}–V_{DS} pulsed mode (Figure 3.9(a)), the device is stressed at a chosen OFF-state bias $(V_{g,\mathrm{stress}}, V_{d,\mathrm{stress}})$ (e.g., −6 V, 56 V) and then quickly pulsed to a measurement point $(V_{g,\mathrm{meas}}, V_{d,\mathrm{meas}})$ with short pulse width and low

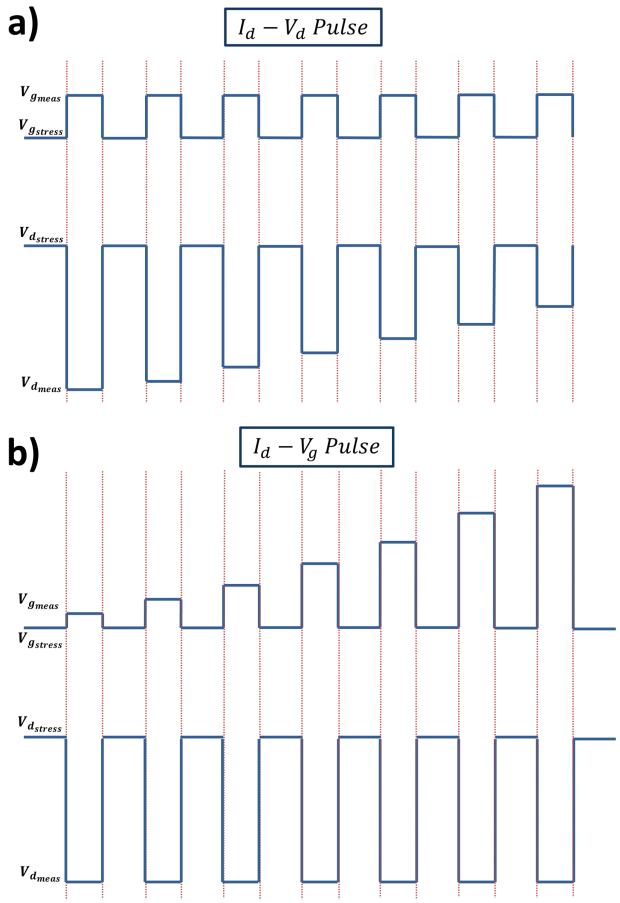


Figure 3.9: Pulsing diagrams for (a) I_D–V_{DS} and (b) I_D–V_{GS} characterizations using pulsed I–V method.

duty cycle. This is repeated for all measurement points in I–V curves for varying gate voltages.

- In the I_D–V_{GS} pulsed mode (Figure 3.9(b)), the drain voltage is kept at the off-state stress value while the gate is pulsed between stress and measurement values.

By varying the quiescent (stress) point and the delay between stress and measurement, one can map how trapped charges at the surface, in the barrier or in the buffer affect the dynamic drain current. The sequences are implemented either using the B1505A's pulsed measurement units or using dedicated pulsers.

Chapter 4

Layout Engineering

This chapter first presents the RF-HTOL test results of packaged amplifier modules based on the initial generation of fabricated GaN-on-SiC HEMTs, prior to any layout or process optimizations. These results highlight the reliability limitations of the baseline technology under realistic RF operating conditions. Subsequently, the chapter describes a series of geometrical optimizations aimed at improving breakdown voltage by modifying the lateral layout of the HEMT. The impact of these changes on RF performance is analyzed, and a final optimized design is proposed.

4.1 RF-HTOL Test Performance of the Devices Before Improvements

Long-term RF-HTOL testing of the fabricated HEMTs requires appropriate matching networks, since the RF-HTOL system operates with a nominal 50 Ω source and load impedance. For this purpose, a two-stage amplifier module was designed, incorporating three matching circuits. The first-stage transistor acts as a driver HEMT, whereas the second-stage transistor provides the main output power and is denoted as the power HEMT. An optical microscope image of

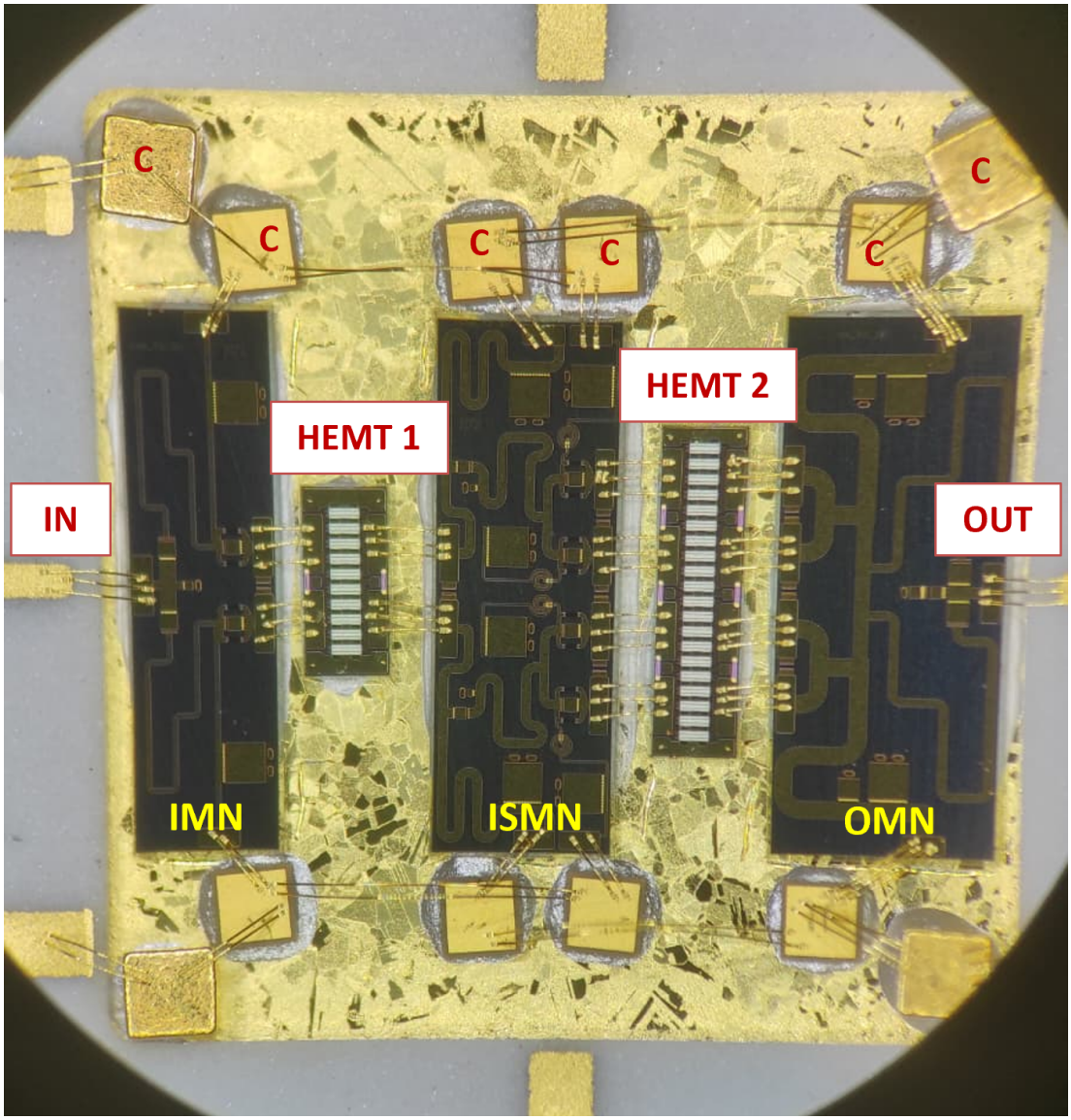


Figure 4.1: Optical image of the two-stage amplifier module showing the HEMTs and input/interstage/output matching networks.

the packaged amplifier is shown in Figure 4.1. The input, interstage and output matching networks are visible together with the two HEMTs. The circuit is assembled in a ceramic air-cavity package with a Cu-Mo-Cu flange, and includes off-chip components such as capacitors. Connections between the transistors, matching networks and off-chip components are implemented using wire bonds. The shortest possible wire bonds are employed in order to minimize additional series inductance.

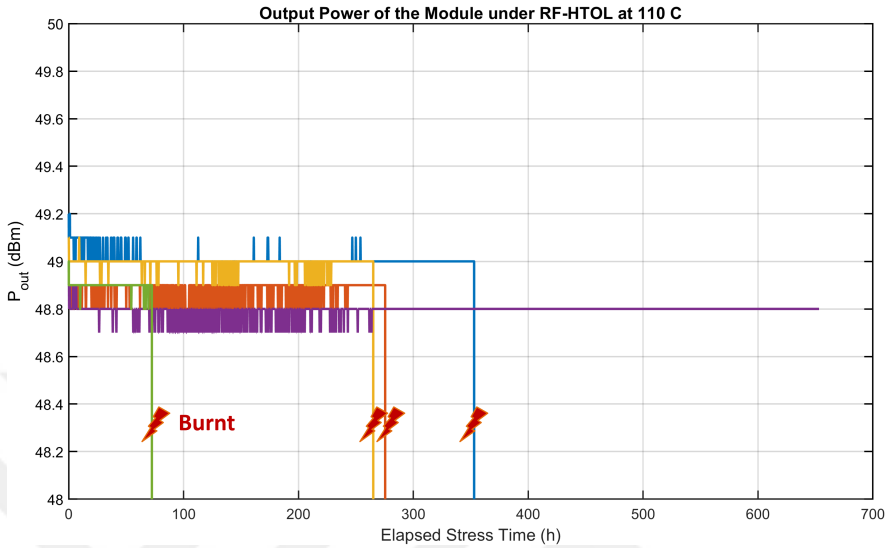


Figure 4.2: RF output power of the amplifier modules under RF-HTOL stress as a function of elapsed stress time.

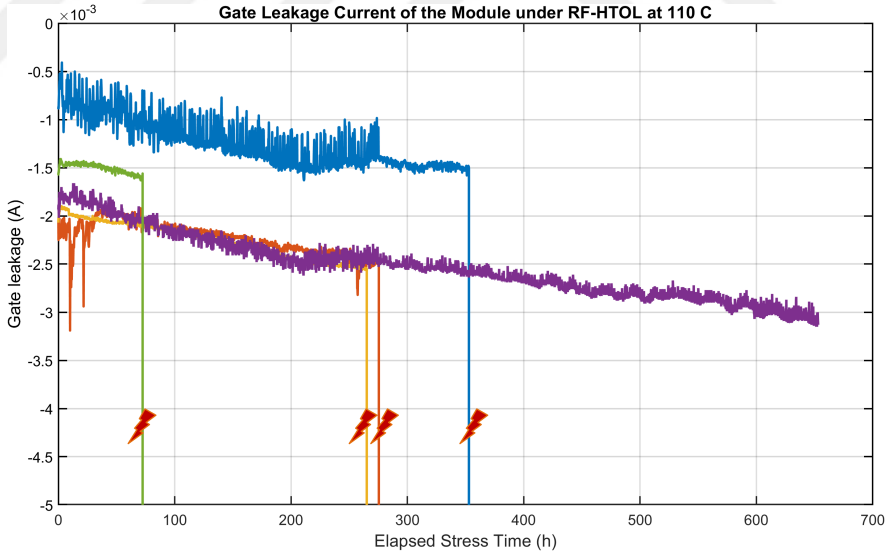


Figure 4.3: Gate leakage current of the amplifier modules under RF-HTOL stress as a function of elapsed stress time.

The amplifier modules are stressed in an Accel-RF RF-16 AARTS system under pulsed-RF operating conditions. The test conditions are: baseplate temperature of 110 °C, drain supply voltage of 45 V, RF input signal with 15% duty cycle, quiescent drain current of 250 mA, RF output power of 49 dBm (corresponding to 30 dBm RF input power) at 3 GHz. During the test, V_{DS} and the RF input are pulsed, whereas the gate bias is kept continuous. Under large RF

excitation, the instantaneous drain current reaches peak values of approximately 3.3 A.

A total of five modules were subjected to RF-HTOL stress under these conditions, and four of them eventually suffered catastrophic failure. The evolution of RF output power and gate leakage current versus stress time is plotted in Figure 4.2 and Figure 4.3, respectively. Over the test duration, the RF output power and drain current remain essentially constant up to failure. The gate leakage current exhibits a slow increase but remains well below 100 μA/mm. Consequently, the catastrophic burnout events occur without any obvious prior degradation in RF performance or leakage.

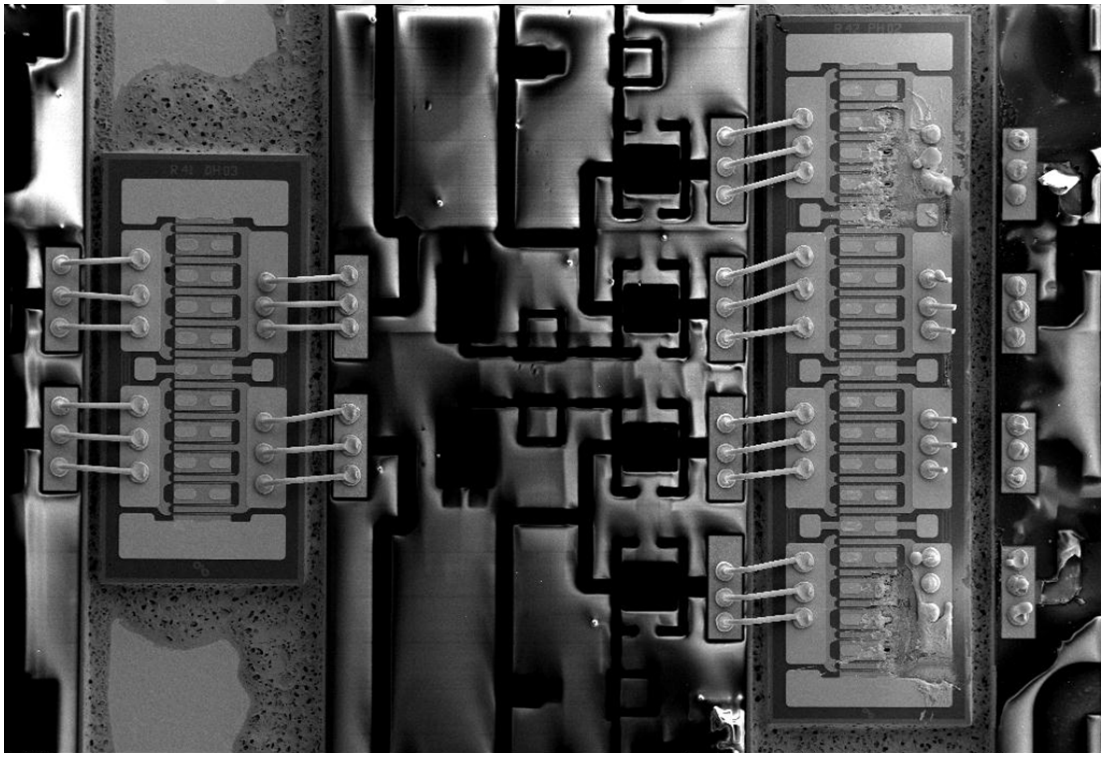


Figure 4.4: SEM image of a failed amplifier module showing a burnt HEMT and melted wire bonds.

A scanning electron microscopy (SEM) image of one of the failed modules is presented in Figure 4.4. One of the HEMTs is visibly burnt, and several wire bonds are melted, indicating exposure to very high current or extended local overheating following burnout. Figure 4.5 shows a closer view of the damaged

regions. In Figure 4.5(a), numerous exploded via holes can be seen, which is consistent with very high current flow through vertical interconnects. If any two layers of the HEMT become short-circuited, the resulting large current can cause instantaneous local explosions. Figure 4.5(b) shows the gate metallization in the burnt region. The exploded regions coincide with the field-plate anchors on the source pads, suggesting a possible gate-to-source short circuit. At the same time, the exploded vias point to a high drain-to-source current path, indicating that a drain-to-source short could also have occurred. It is therefore not possible to unambiguously identify a unique root cause from the post-test images alone. Nevertheless, the observations clearly show that one or more passivation layers or the gate control over the channel failed under high-field stress, eventually leading to short circuits and catastrophic burnout. The baseline device thus requires improvement in terms of robustness under high electric field.

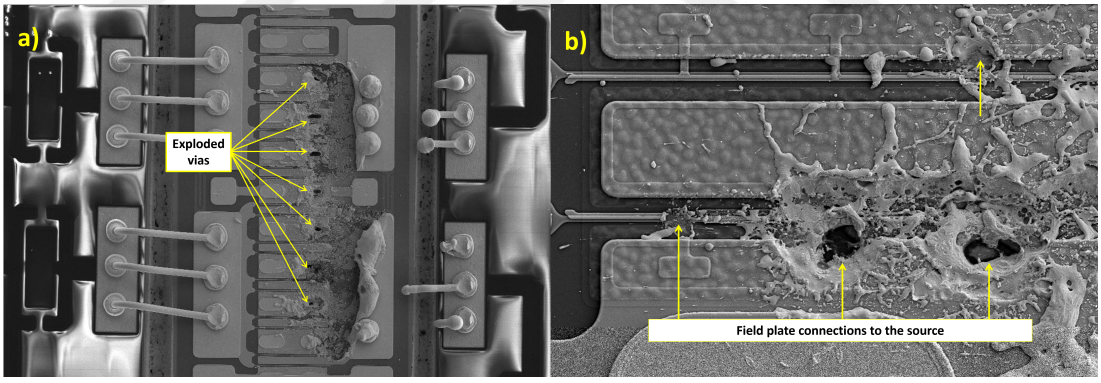


Figure 4.5: SEM images of the burnt area: (a) exploded via holes; (b) field-plate anchors on the source pads within the damaged region.

4.2 Breakdown Voltage Improvement via Lateral Geometries

For safe operation, the breakdown voltage of a power RF device should typically exceed at least three times the nominal operating drain voltage. Depending on the application, even higher margins may be required. The technology considered here is designed for operation at $V_{\mathrm{DD}} = 50$ V; therefore, a breakdown voltage

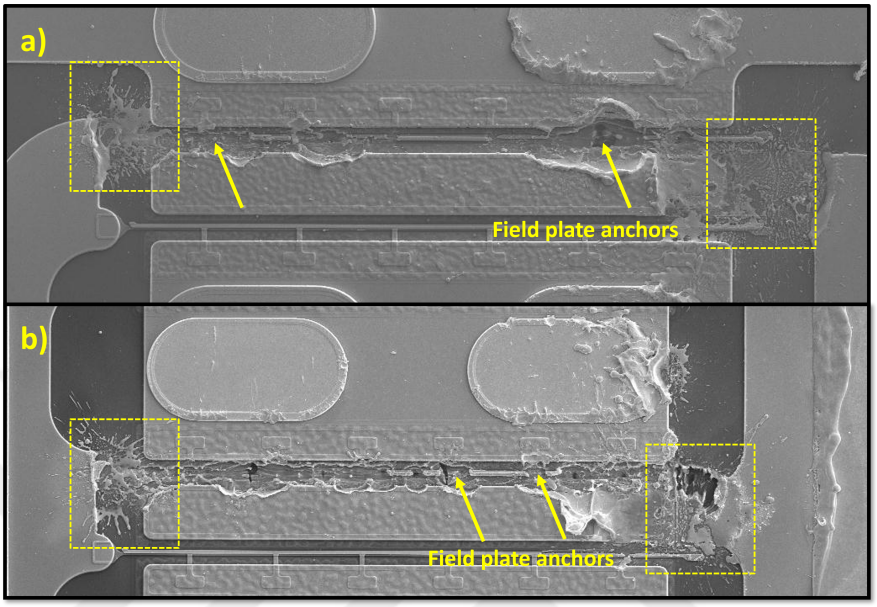


Figure 4.6: SEM images of baseline HEMTs that failed during breakdown voltage sweeps under off-state bias.

above 150 V is desirable to ensure reliable operation in the intended environment.

The initial generation of HEMTs (baseline layout) features the following lateral dimensions: gate foot length of 500 nm, gate width of 250 μm, horizontal distance from the field-plate edge to the gate-head edge of 900 nm, gate-foot-edge-to-source distance of 1.5 μm, and drain-to-source distance (L_{DS}) of 5 μm. The catastrophic breakdown voltages of these devices, measured under off-state drain-voltage sweeps, fall in the range 130–150 V. SEM images of several devices that failed during V_{DS} sweeps under off-state bias are shown in Figure 4.6. Strong explosions at the field-plate anchors and at the gate and drain interconnects are evident. Failure of the interconnects at the gate and drain entry points is most likely due to very high currents following breakdown of the gate region and consequent loss of channel control. These observations indicate that the electric-field peaks in the device exceed the critical field at voltages lower than the desired breakdown specification. Therefore, the internal field distribution must be modified and relaxed through layout optimization.

As a first step, the effect of gate and field-plate geometries on breakdown

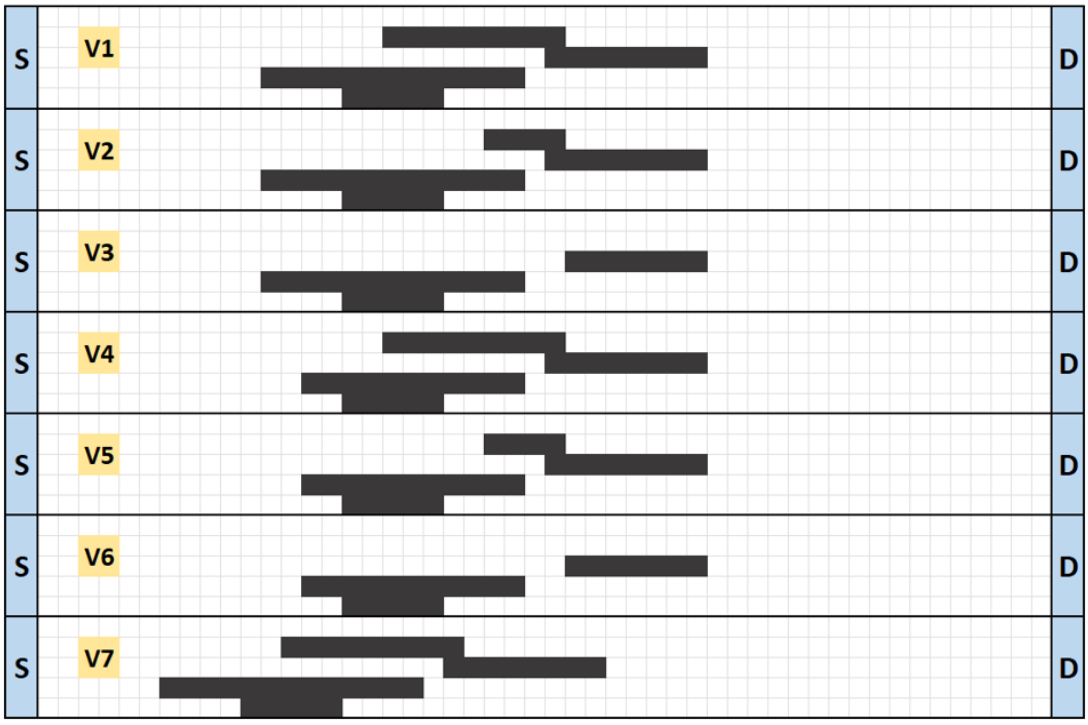


Figure 4.7: Schematic representation of gate and field-plate geometrical variations (V1–V7) for DS5 HEMTs. Each grid corresponds to 100 nm in the horizontal direction.

voltage was investigated using seven layout variants, all with $L_{\mathrm{DS}} = 5\ \mu$m (DS5 devices). These variants, denoted V1–V7, are illustrated schematically in Figure 4.7. Version V1 corresponds to the original baseline HEMT structure. Each grid cell in the schematic represents 100 nm in the horizontal direction. For V1 to V6, the gate-foot-edge-to-source distance, and thus the gate-to-drain distance, is kept constant at 1.5 μm. The differences between these variants lie in the gate-head length on the source side and the overlap lengths of the gate metal and field-plate metal. In V7, the gate is shifted closer to the source by 500 nm, reducing the gate-to-source distance to 1 μm and, consequently, increasing the gate-to-drain distance from 3 μm to 3.5 μm, while maintaining gate and field-plate geometries identical to V1.

Breakdown measurements were performed using the Keysight B1505A, with a fast drain-voltage sweep from 0 V to 150 V at a fixed gate bias of $V_{\mathrm{GS}} = -8$ V. Histograms of the measured breakdown voltages for V1–V6 are shown in

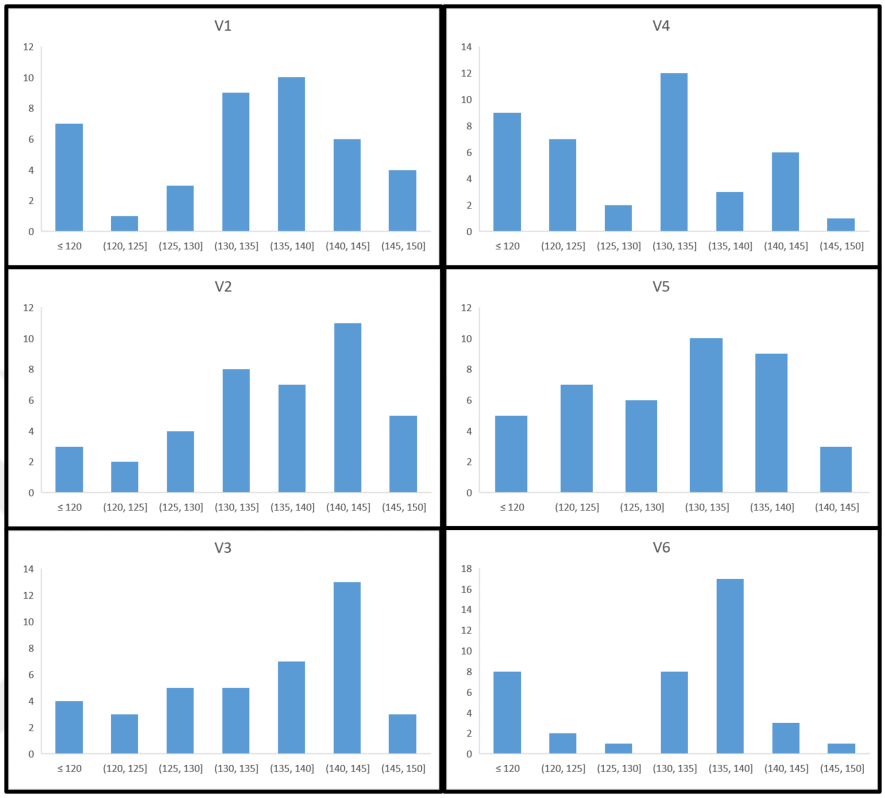


Figure 4.8: Breakdown-voltage histograms for gate/field-plate layout variants V1–V6 (DS5 devices).

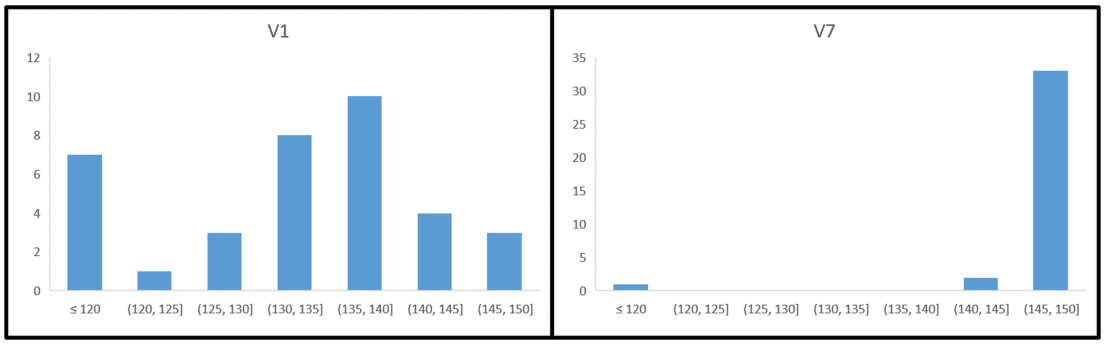


Figure 4.9: Breakdown-voltage histograms comparing V1 and V7 gate/field-plate layouts (DS5 devices).

Figure 4.8. These variants do not exhibit a clear advantage over one another in terms of breakdown. In contrast, the breakdown-voltage distribution for the V7 design, presented in Figure 4.9, shows a pronounced improvement. It is important to note that devices that do not break below 150 V are recorded at 150 V in these experiments; their actual breakdown voltage may be higher. These results

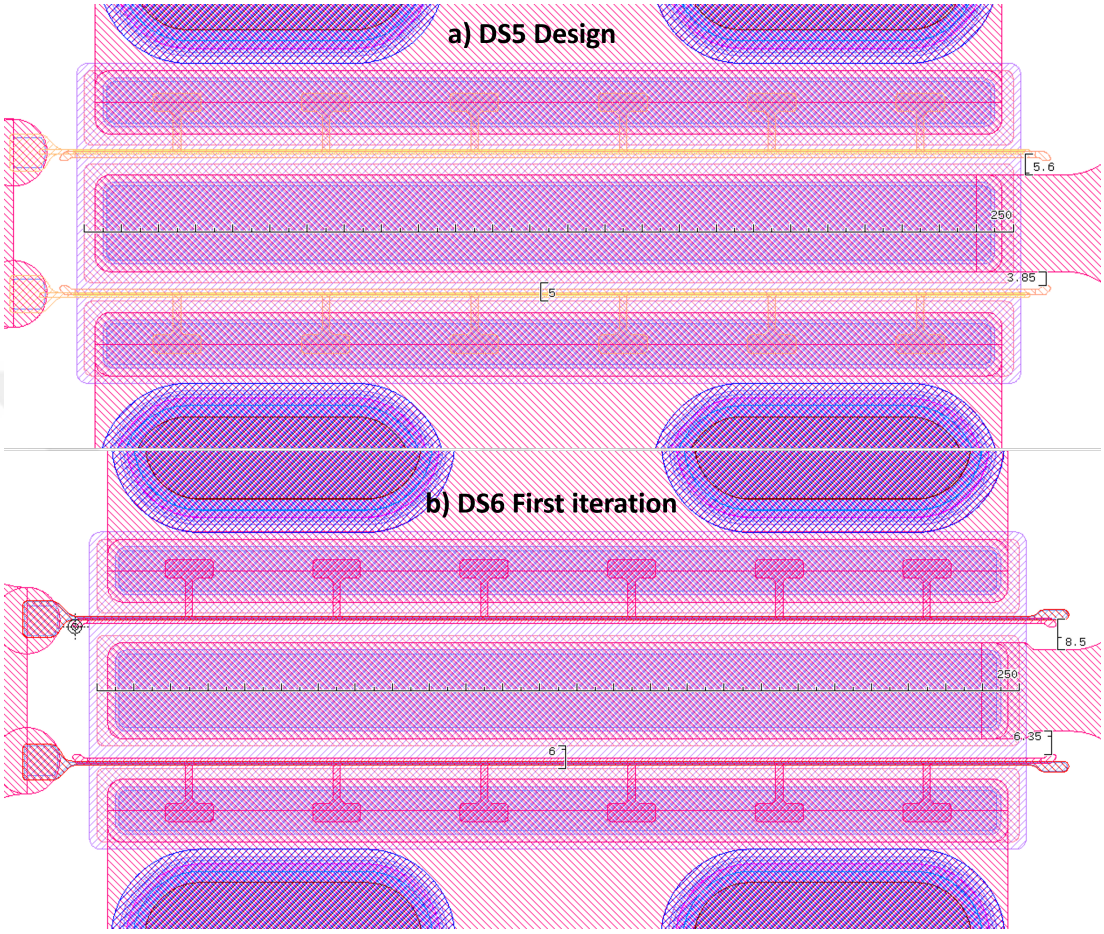


Figure 4.10: Layout comparison of DS5 and DS6 HEMTs in the first iteration, showing increased drain-to-source distance and modified drain-pad connections.

indicate that the gate-to-drain distance is the most critical parameter among the considered geometrical variations in defining breakdown voltage.

To further increase the gate-to-drain distance and thereby improve breakdown voltage, the drain-to-source spacing L_{DS} was increased from 5 μm to 6 μm, while keeping the other geometrical parameters unchanged. In addition, the drain pad connection of the drain ohmic region was redesigned for both DS5 and DS6 devices. These changes are highlighted on the mask layout in Figure 4.10. The distance from field plate to drain pad is increased from 3.85 μm to 6.35 μm, and the distance from gate metal to drain pad is increased from 5.6 μm to 8.5 μm. Figure 4.11 shows SEM images comparing the previous and new layouts of the field-plate and gate-to-drain-pad regions. During breakdown sweeps, the field

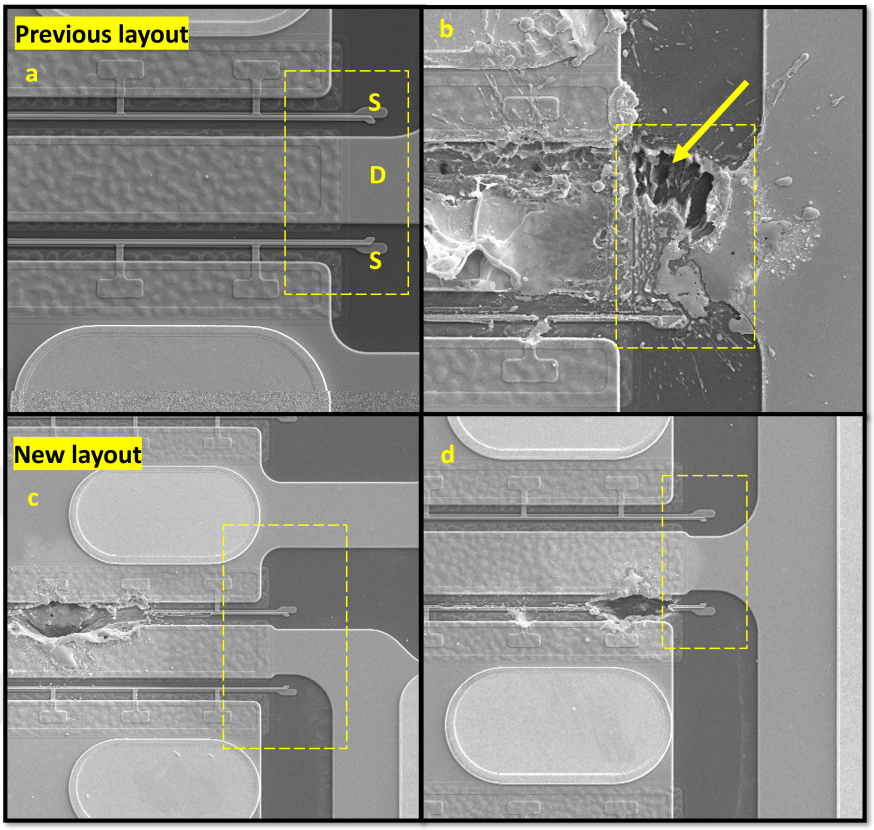


Figure 4.11: Field-plate and gate-metal to drain-pad design: SEM images of (a)-(b) previous layout (DS5) and (c)-(d) new layout (DS6).

plate is connected to source, the gate is negatively biased, and the drain pad is at high positive potential. Visual inspection of broken devices in the original layout (Figure 4.11(a)–(b)) motivated this redesign.

Representative SEM images of measured HEMTs with their corresponding breakdown voltages are shown in Figure 4.12. Increasing L_{DS} from 5 μm to 6 μm improves the breakdown voltage by approximately 35%. Furthermore, the images indicate that explosions in the previously critical regions are less frequently observed in the new layout. Thus, the targeted breakdown voltage improvement is achieved through the lateral geometry modifications.

After modifying the layout, RF performance must also be reassessed. Fundamental load-pull measurements were performed on multiple devices, and average values were extracted. Table 4.1 summarizes the RF performance of DS5 and

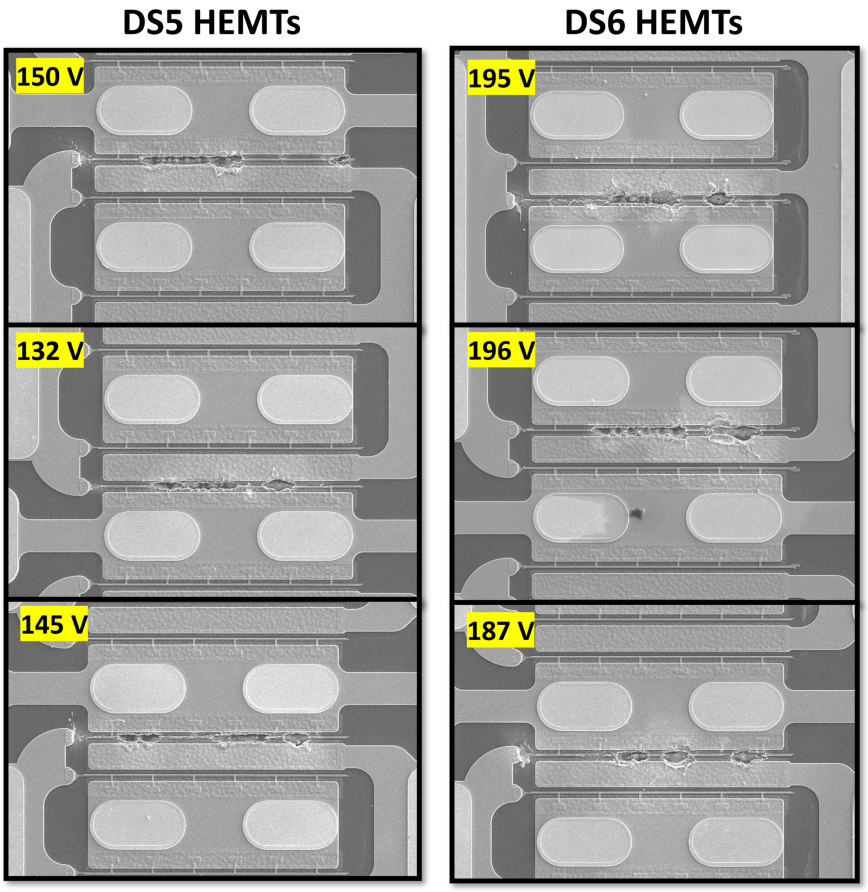


Figure 4.12: SEM images and measured breakdown voltages of DS5 and DS6 HEMTs, highlighting the improvement obtained by increasing L_{DS}.

DS6 HEMTs for V1 and V2 gate/field-plate layouts. The results indicate that increasing L_{DS} leads to slightly larger gain compression and higher input power at saturation, while the saturated output power ($P_{\mathrm{out,Sat}}$) and power-added efficiency at saturation ($\mathrm{PAE_{Sat}}$) decrease by approximately 0.25 dB and 2.5%, respectively. In other words, breakdown voltage is improved at the expense of a modest RF performance penalty.

To compensate for the decrease in RF performance, gate geometries were further optimized. The gate width was increased from 250 μm to 265 μm in order to boost output power and PAE, while the gate-foot length was reduced from 500 nm to 400 nm to improve small-signal gain. Average load-pull results for

Table 4.1: RF performance comparison of DS5 and DS6 HEMTs with V1 and V2 gate/field-plate layouts.

Name	$P_{\text{out,Sat}}$ (dBm)	PAE_{Sat} (%)	Comp_{Sat} (dB)	$P_{\text{in,Sat}}$ (dBm)	V_{GQ} (V)
V1-DS5	43.41	69.89	4.30	27.91	-3.23
V1-DS6	43.17	67.04	4.60	27.96	-3.23
V2-DS5	43.36	68.55	4.44	27.30	-3.20
V2-DS6	43.19	66.64	4.65	27.39	-3.22

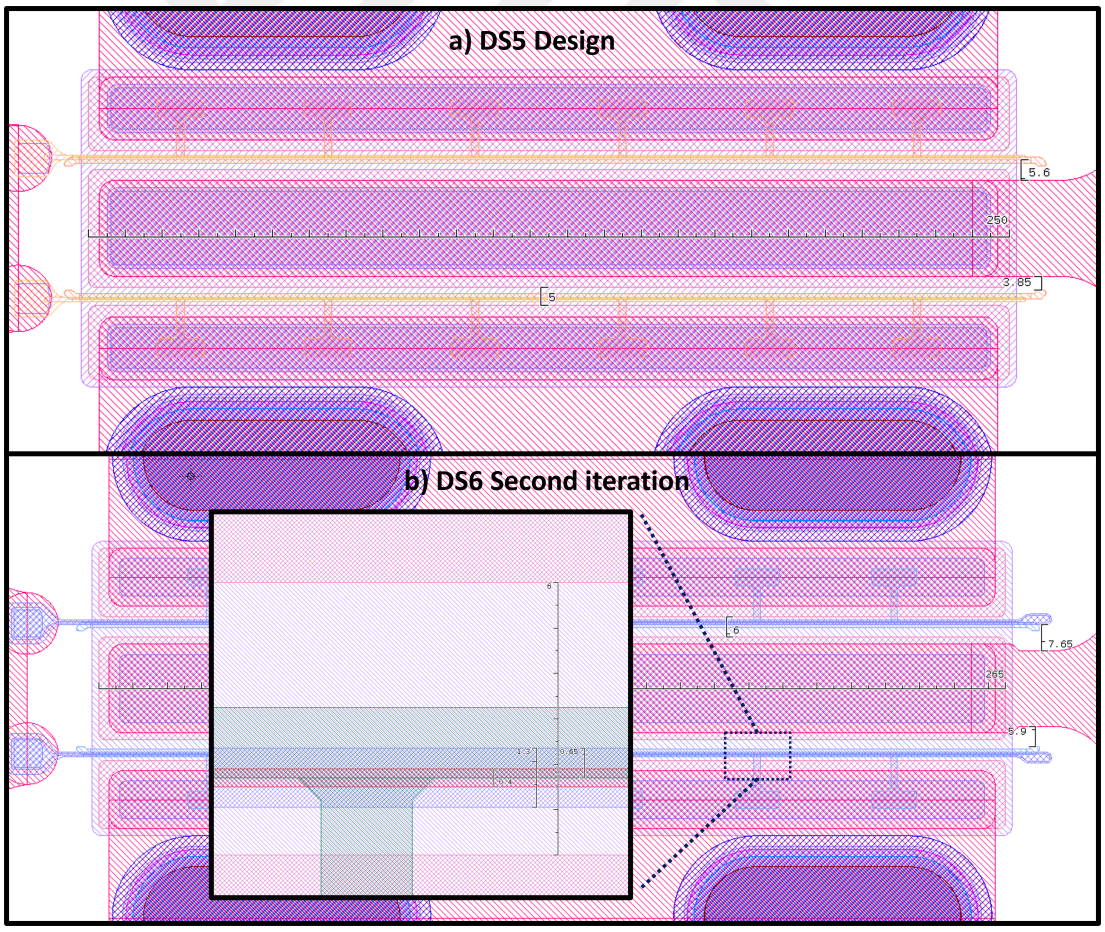


Figure 4.13: Layout comparison of DS5 and DS6 HEMTs in the first iteration, showing increased drain-to-source distance and modified drain-pad connections.

multiple HEMTs of three different types are listed in Table 4.2. Type 3 corresponds to the original design (DS5, 250 μm gate width, 500 nm gate-foot length), Type 2 has the same L_{DS} but a wider 265 μm gate and 500 nm gate foot, whereas Type 1 combines $L_{\mathrm{DS}} = 6$ μm with 265 μm gate width and 400 nm gate foot.

Comparing Type 2 and Type 3, one observes that increasing the gate width improves $P_{\mathrm{out,Sat}}$ and PAE, but slightly reduces the small-signal gain (G_{t}). Comparing Type 1 and Type 2 shows that the combination of increased L_{DS} and reduced gate-foot length leads to a small reduction in $P_{\mathrm{out,Sat}}$ and a more noticeable decrease in PAE, while significantly increasing small-signal gain. In summary, Type 3 and Type 1 represent the previous and final optimized designs, respectively. Overall, the new design exhibits increased gain and comparable output power with a moderate reduction in PAE; the absolute performance values, however, remain similar.

The main difference between the two designs is the threshold voltage. V_{GQ} in Table 4.2 represents the gate bias at which a drain current of 16 mA/mm is obtained. The new design exhibits a negative shift of approximately 150 mV in V_{GQ} due to the shorter gate length, which also indicates the onset of stronger short-channel effects that must be taken into account when interpreting the device performance. In final case, the first version of HEMT and the second iteration of design process is shown in Figure 4.13.

Table 4.2: RF performance comparison of three types of HEMTs with different gate widths, gate-foot lengths and drain-to-source distances.

Type	Device	G_t (dB)	$P_{\mathrm{out,Sat}}$ (dBm)	$\mathrm{PAE_{Sat}}$ (%)	$\mathrm{Comp_{Sat}}$ (dB)	$P_{\mathrm{in,Sat}}$ (dBm)	V_{GQ} (V)
Type 1	DS6-265µm-400nm	20.08	43.41	65.26	5.87	29.20	-3.22
Type 2	DS5-265µm-500nm	19.04	43.56	67.13	4.82	29.34	-3.06
Type 3	DS5-250µm-500nm	19.48	43.36	65.76	4.73	28.61	-3.06

Chapter 5

Fabrication Process Flow Optimizations

This chapter addresses reliability problems that were identified in the baseline GaN-on-SiC HEMT technology and describes the process improvements that were implemented to solve them. The proposed solutions are evaluated using long-term reliability tests (DC-HTOL, HTRB and RF-HTOL), leakage and breakdown measurements, and TEM analysis. The focus is on eliminating Q-point instability, reducing gate leakage current and lowering the HTRB failure rate.

5.1 Post-metal Annealing (PMA) Process to Solve Q-Point Instability

Q-point instability is defined as a drift of the drain current during on-state operation at fixed gate and drain voltages. In practice, the I_{D}–V_{GS} characteristic of the HEMT evolves with time, so that the drain current at a given bias no longer corresponds to its initial value. When Q-point instability is present, the threshold voltage shifts [78] , the transconductance peak moves[79], the drain current at fixed V_{GS} changes, and consequently output power and efficiency drift under

RF drive. Integrating such an unstable HEMT into an RF module represents an unacceptable risk; the phenomenon must be eliminated at technology level.

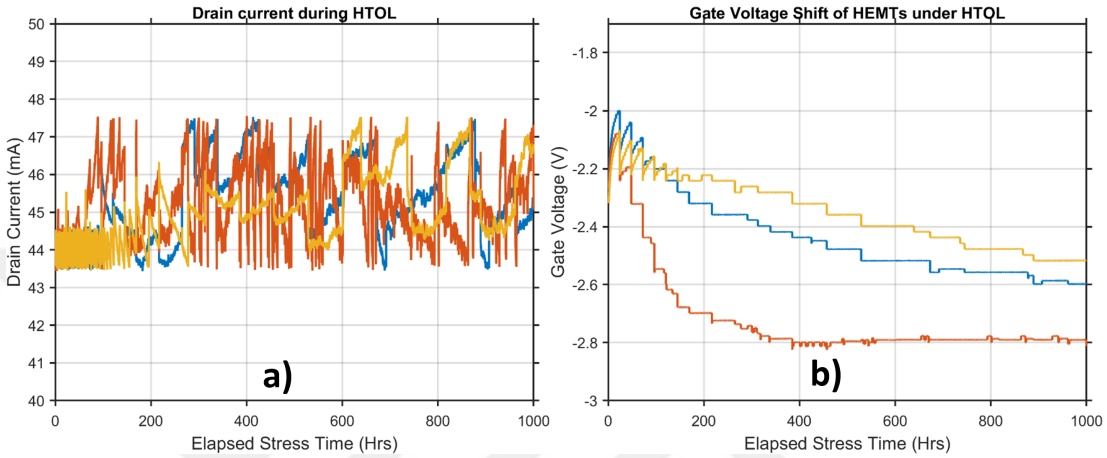


Figure 5.1: (a) Drain current and (b) regulated gate-quiescent voltage of HEMTs during HTOL without PMA.

5.1.1 HTOL Test of Devices without PMA

Q-point instability can be clearly observed under DC-HTOL stress. In HTOL, the device is biased close to its nominal operating point, and a constant drain current is enforced to obtain a fixed power dissipation. The reliability system adjusts the gate voltage whenever the measured drain current deviates from the target value. Therefore, the evolution of the regulated gate bias directly reveals the presence and severity of threshold-voltage drift.

An HTOL experiment was carried out on three packaged GaN HEMTs using an Accel-RF DC-96 AARTS system. The test conditions were $V_{\mathrm{DS}} = 45$ V, $I_{\mathrm{D}} = 45.5$ mA (corresponding to approximately 4 W/mm channel power dissipation) and a base temperature of 115 °C. The system was programmed so that the gate voltage was automatically corrected whenever the drain current error exceeded ±2 mA.

Figure 5.1(a) shows the recorded drain current of the three devices during 1000 h of HTOL. As expected, the current is maintained within the ±2 mA

tolerance by frequent corrections. Figure 5.1(b) presents the corresponding gate bias. In the early phase of the test, the gate voltage repeatedly shifts towards more positive values, indicating positive threshold-voltage drift. After several hundred hours, the drift reverses direction and the gate voltage moves back towards more negative values. The total excursion exceeds 600 mV, which is a very large and clearly unacceptable shift for practical applications.

Several mechanisms have been reported to cause Q-point instability in GaN HEMTs. Both epitaxial defects and micro/nano-fabrication steps can contribute, but the most frequently cited root cause is trapping at surface or interface states near the gate edge. Traps at the AlGaN surface or at the dielectric/AlGaN interface capture electrons, modify the local surface potential and produce hysteresis and drift in V_{th}. They typically exhibit long emission times. Surface damage during gate-foot etching, plasma damage during dielectric deposition, surface contamination or native-oxide formation can all increase the density of such traps and distort the Schottky contact. The resulting shallow interface states are directly implicated in Q-point instability. Reported solutions thus focus on improving these fabrication steps, including optimized surface passivation [80, 81], pre-gate surface cleaning[82], gate-metal stack engineering[83], buffer engineering[84] and post-gate-metal annealing (PMA)[82, 85].

5.1.2 TEM Analysis of Devices without PMA

To identify the dominant mechanism in our technology, detailed TEM analysis was performed on devices exhibiting Q-point instability. TEM imaging allows high-resolution inspection of the lateral and vertical device cross-section, including the Schottky gate contact, the epitaxial interfaces and dislocation structure, as well as local elemental analysis.

A low-magnification TEM image is shown in Figure 5.2, where the epitaxial layers, gate metals and field plate are visible. A higher-magnification image of the gate region is presented in Figure 5.3(a). Dislocations in the epitaxy, the polycrystalline structure of the gate metal and the gate/AlGaN interface can be

clearly identified. A more focused inspection of the Schottky contact is required.

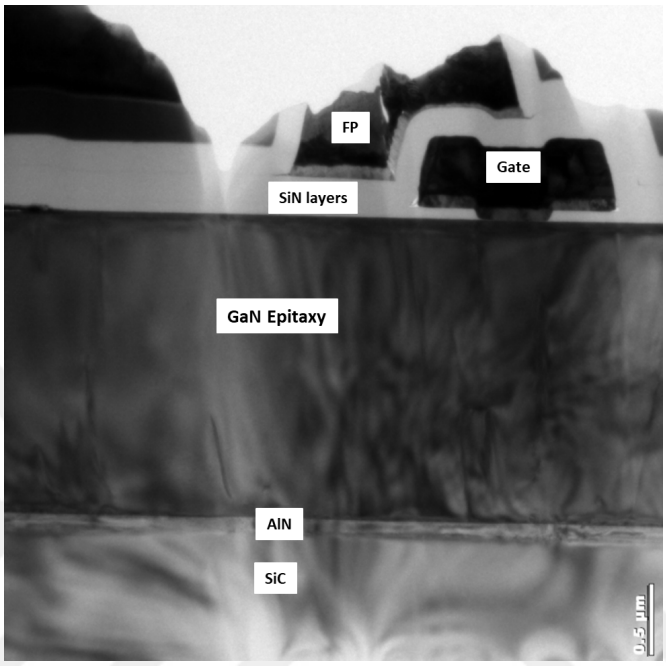


Figure 5.2: TEM cross-section of the HEMT showing the epitaxial stack, gate and field plate.

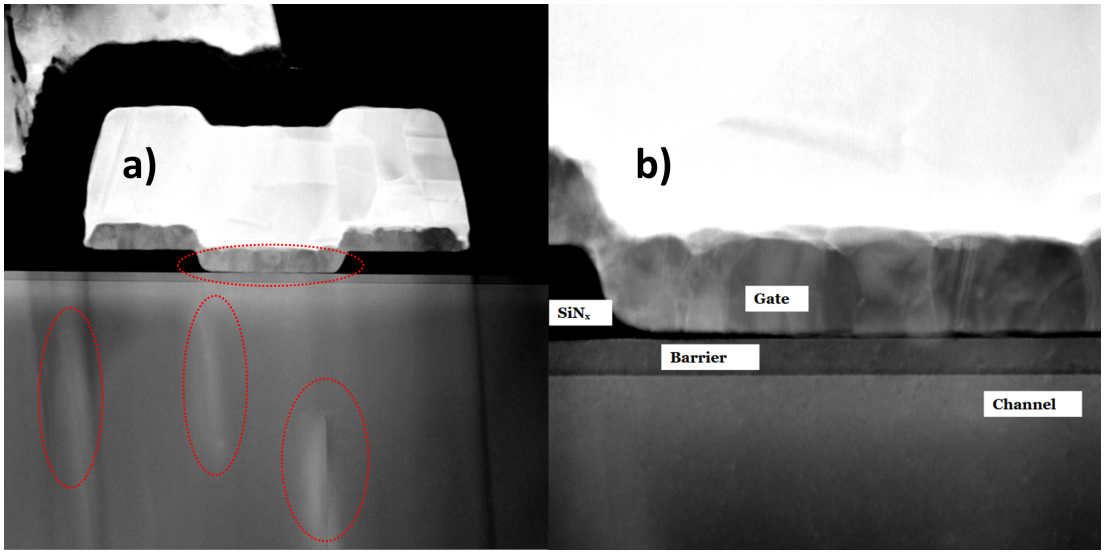


Figure 5.3: TEM images of the gate region of the initial device: (a) epitaxial layers, gate metals and Schottky contact; (b) magnified view of the gate/AlGaN interface.

The magnified image of the gate/AlGaN interface in Figure 5.3(b), where contrast has been adjusted to emphasize the interface, reveals that the Schottky

contact is not formed as intended. A dark layer is visible between the Ni gate metal and the AlGaN barrier. This layer is consistent with a thin nitride film, indicating that a residual SiN layer remains under the gate foot. In other words, instead of a metal–semiconductor (MS) gate, the device effectively has a metal–insulator–semiconductor (MIS) gate structure.

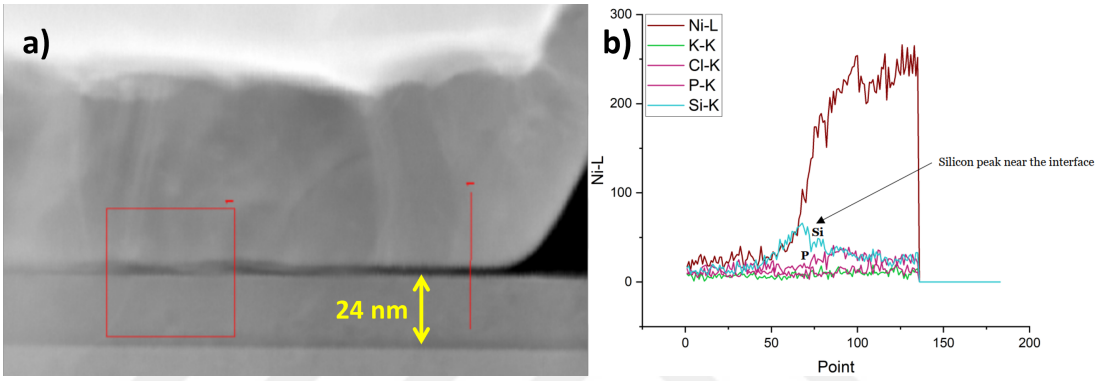


Figure 5.4: Elemental analysis of the gate/AlGaN interface of the initial device: (a) location of the line scan on the TEM image, (b) elemental profile from epitaxy into gate metal showing a Si peak at the interface.

To confirm the nature of this layer, a line-scan elemental analysis was performed through the interface. The scanned region is indicated in Figure 5.4(a). The corresponding elemental profile in Figure 5.4(b) shows a pronounced Si signal at the interface, confirming the presence of SiN under the gate foot. From comparison with the AlGaN thickness, the SiN thickness is estimated to be a few nanometers. This residual dielectric reduces gate control over the channel and introduces additional reliability issues. The SiN/AlGaN interface is known to host numerous charge traps, which are easily charged and discharged under bias, leading to Q-point instability, power drop and strong gate-lag effects. Even in the absence of SiN, a high density of shallow traps at the gate/AlGaN interface would be problematic; here, the presence of an unintended MIS structure aggravates the situation. The gate metal/AlGaN interface must therefore be improved to recover a well-behaved MS contact and reduce interface trap density.

This finding suggests two modifications to the process flow. First, the gate-foot etch must be improved so that the first nitride layer is fully removed in the gate opening. Either the etch duration must be increased, or the etch chemistry must

be changed. Second, a post-gate-metal annealing step (PMA) can be introduced to improve the Schottky contact. PMA does not remove the residual SiN, but it can anneal out interface defects, increase the effective Schottky barrier height and improve stability.

5.1.3 HTOL Test of Devices with PMA

Both modifications were implemented. The plasma etch time of the first nitride in the gate-foot region was increased to ensure complete removal of SiN before gate metallization, and a PMA step at 400 °C for 10 min was added after gate deposition.

New devices processed with these changes were evaluated with HTOL stress and re-examined by TEM. Figure 5.5(a) shows the drain current of several devices from the same lot during HTOL in the DC-96 system. The devices were initially stressed at $I_{\mathrm{D}} = 200$ mA (about 2 W/mm) at 110 °C base temperature, and after 300 h the current was increased to 400 mA. The higher currents compared with Section 5.1.1 are due to the larger gate periphery of the tested devices. As before, the system constrains the drain current within a small range to maintain constant power dissipation.

Figure 5.5(b) presents the corresponding gate bias. The total gate-voltage drift is less than 50 mV for both the 200 mA and 400 mA operating phases, a dramatic improvement over the 600 mV drift observed previously. This demonstrates that Q-point instability has been effectively eliminated by the revised fabrication flow.

5.1.4 TEM Analysis of Devices with PMA

TEM analysis was repeated on devices from the improved lot. A low-magnification cross-section is shown in Figure 5.6(a). Dislocations in the GaN epitaxy are visible but their density is consistent with typical GaN-on-SiC material and is not considered critical. Platinum in the image originates from the

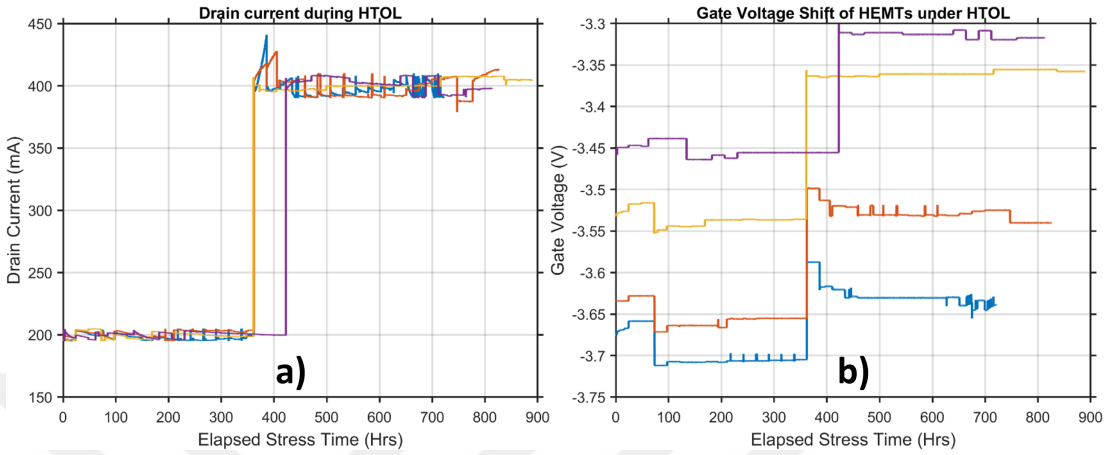


Figure 5.5: HTOL results of devices fabricated with improved gate-foot etch and PMA: (a) drain current, (b) regulated gate-quiescent voltage.

TEM sample preparation and is not part of the device. A high-magnification view of the gate/AlGaN interface is presented in Figure 5.6(b). In contrast to Figure 5.3(b), no residual SiN layer is visible beneath the gate foot, confirming that the foot-etch process now fully clears the first nitride in the gate opening.

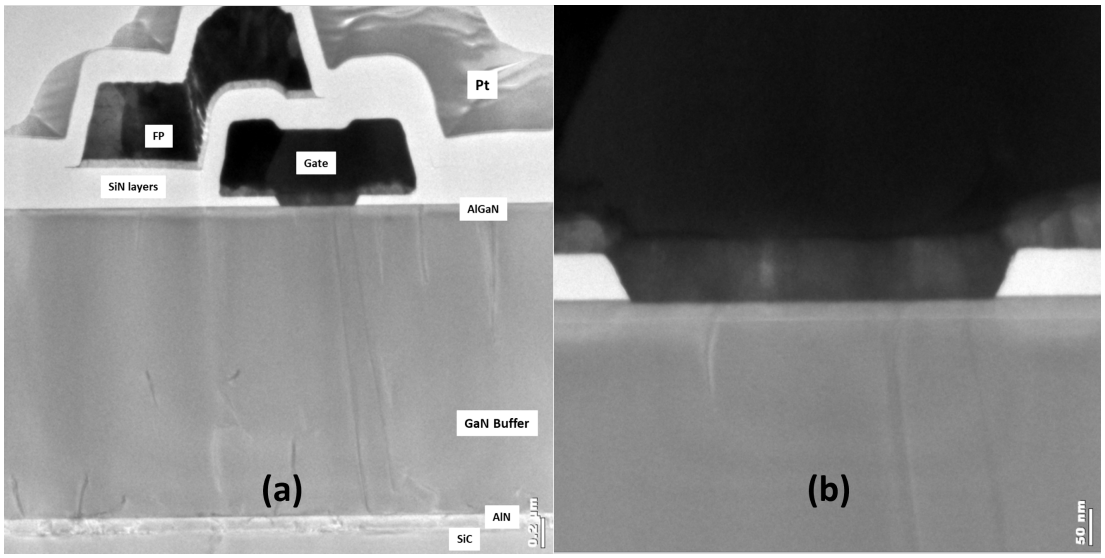


Figure 5.6: TEM images of the improved device with PMA: (a) overall cross-section, (b) high-magnification view of the gate/AlGaN interface.

Elemental line-scan analysis was again performed across the gate/AlGaN interface. The scanned line and resulting elemental profile are shown in Figures 5.7(a)

and 5.7(b), respectively. No Si peak is observed at the interface; only signals corresponding to Ga/Al (AlGaN) and Ni/Au (gate metal) are present. A small rise in Si at the end of the line is attributed to measurement artefacts, as that region corresponds to the gate metal, where Si is not expected. These results confirm that the combination of extended gate-foot etch and PMA successfully removes the residual SiN under the gate, restores a proper MS junction and resolves the Q-point instability.

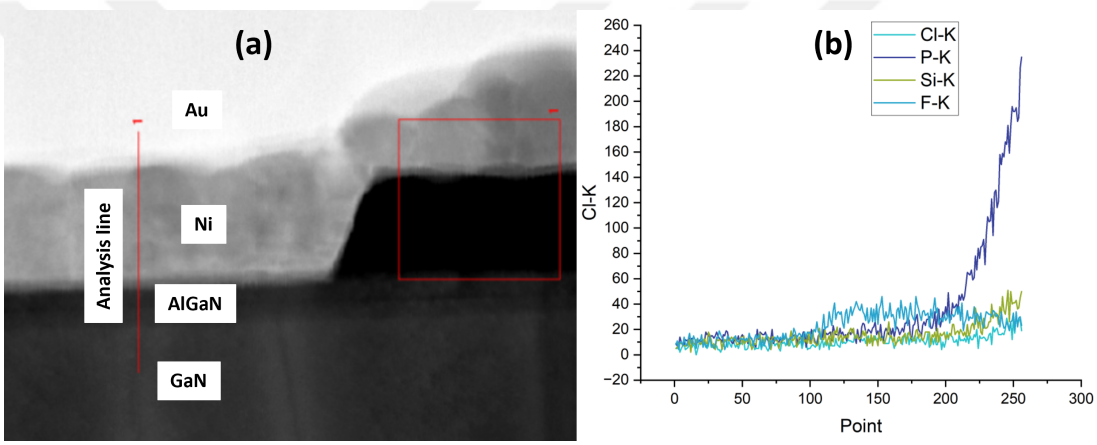


Figure 5.7: Elemental analysis of the gate/AlGaN interface in the annealed device: (a) line-scan location, (b) elemental profile showing absence of Si at the interface.

5.2 Improving Reliability by Nitride Layers and Gate-Treatment Methods

Silicon nitride (SiN) is widely regarded as the most suitable dielectric for GaN HEMTs. It can be deposited with processes that are thermally and chemically compatible with GaN technology, offers selective etch chemistries, adheres well to AlGaN/GaN surfaces, is stable under RF operation, acts as an effective diffusion barrier, and allows tuning of stress and strain. In typical T-gate GaN HEMTs with field plates, three SiN layers are used. A representative cross-section is illustrated in Figure 5.8. The first nitride layer (SiN-1) passivates the AlGaN surface, suppresses surface traps, defines the gate-foot etch stop and contributes to

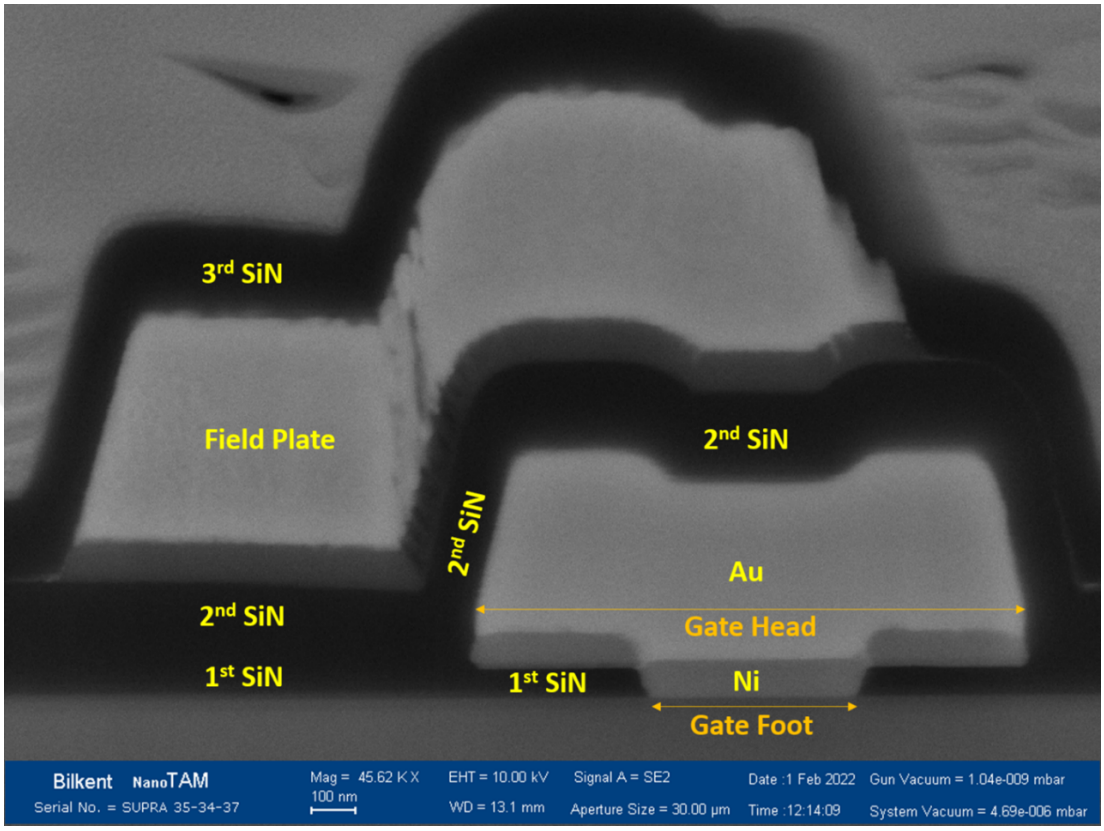


Figure 5.8: Schematic cross-section of the three-layer SiN stack around the gate region.

stress engineering. The second nitride (SiN-2) electrically separates the gate from the source-connected field plate. The third nitride (SiN-3) covers the field plate and interconnects, providing additional passivation and mechanical protection. Because the relative permittivity of SiN ($\varepsilon_r \approx 7$) is lower than that of many alternative dielectrics, the added capacitance between gate and source due to the field plate is minimized, while field-plate benefits on breakdown are retained.

Under large-signal RF operation the device swings between on-state and off-state during each RF cycle. High current and self-heating related mechanisms dominate in the on and semi-on portions of the cycle, whereas high electric field is the main driver of failure mechanisms in off-state. TCAD simulations, summarized in Figure 5.9, show that the maximum electric field under deep off-state stress occurs first at the drain-side gate-foot edge inside the AlGaN, then at the drain-side gate-head edge inside the SiN stack, and finally at the field-plate edge.

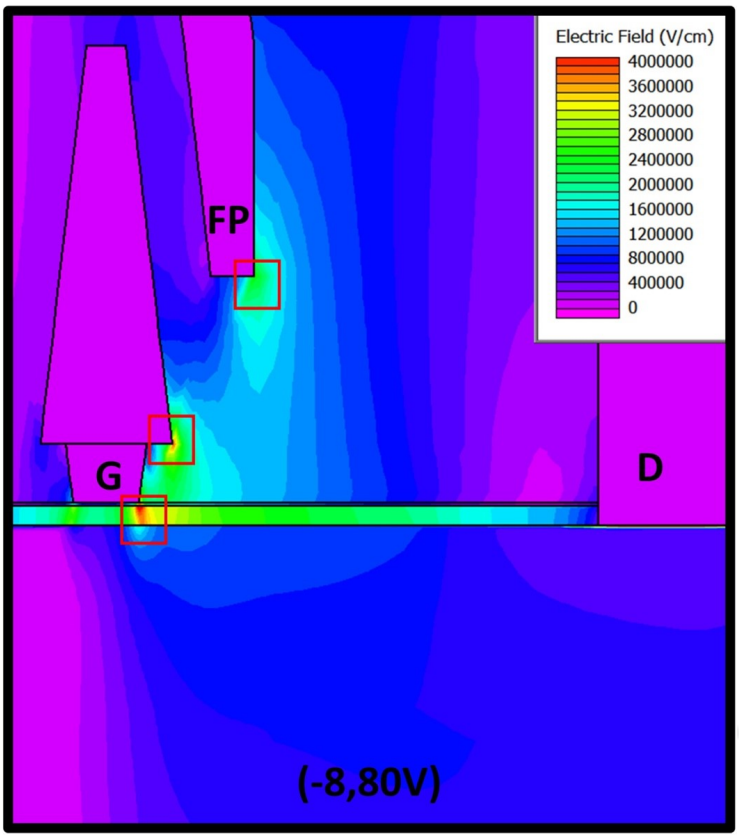


Figure 5.9: Simulated electric-field distribution in a GaN HEMT under deep off-state bias.

High-field stress in these regions can induce buffer and surface trapping, gate damage, permanent leakage increase, current collapse and ultimately catastrophic failure if the critical field is exceeded. Improving reliability therefore requires either reducing the peak field at these locations through field-management design or improving the quality and robustness of the layers at these high-field regions. The following sections analyze different nitride layers and gate-treatment schemes using MIM capacitors and GaN HEMTs.

5.2.1 Reliability Improvement by Pre-Gate Treatment Technique

The Schottky gate metal/AlGaN interface is one of the most critical regions in a GaN HEMT. Any degradation of this interface—due to contamination, residual dielectric, plasma damage, metal diffusion or trap formation—immediately impacts device behaviour. A degraded Schottky interface exhibits reduced barrier height and elevated trap density, leading to higher gate and gate-induced drain leakage, weaker gate control and enhanced electric field at the gate edge. Shallow traps at this interface capture and emit charge under bias, causing threshold-voltage drift, Q-point instability, shifts in g_m peak and pronounced hysteresis in transfer characteristics. Under high off-state field, the damaged region becomes a preferred hot-electron injection site, accelerating trap creation, boosting dynamic R_{on}, worsening current collapse and ultimately forming permanent leakage paths or catastrophic gate-edge breakdown. In short, an uncontrolled Schottky interface turns the gate edge into a dominant failure hot-spot.

In the original process, an aqueous NH_4OH treatment was used prior to Schottky gate metallization to remove native oxides, organic residues, adsorbed moisture and weakly bound contaminants from the AlGaN surface. This wet clean leaves the surface chemically cleaner and helps to reduce interface-state density, thereby improving barrier height, lowering leakage and stabilizing V_{th}. NH_4OH effectively removes Ga–O and Al–O species and provides good reproducibility of the Schottky barrier. However, the process is not perfectly selective: overexposure can roughen the AlGaN surface and residual amine species may remain if the rinse is insufficient.

Plasma-based surface treatments at the Schottky interface are generally avoided because they can damage the surface: O_2 plasma tends to increase oxide thickness and fixed charge, whereas Ar plasma can induce physical sputter damage, nitrogen vacancies and additional trap sites. Both effects typically degrade barrier uniformity and increase leakage. However, in this work an *in-situ* ion-based treatment was developed as an alternative to NH_4OH, using carefully

controlled O_2 and Ar ion bombardment. O_2 ions remove organic residues originating from lithography and general contamination, while Ar ions strip the native oxide without relying on wet chemistry. With optimized conditions, this combined O_2/Ar treatment significantly reduces reverse gate leakage—by more than one order of magnitude—without introducing detrimental plasma damage.

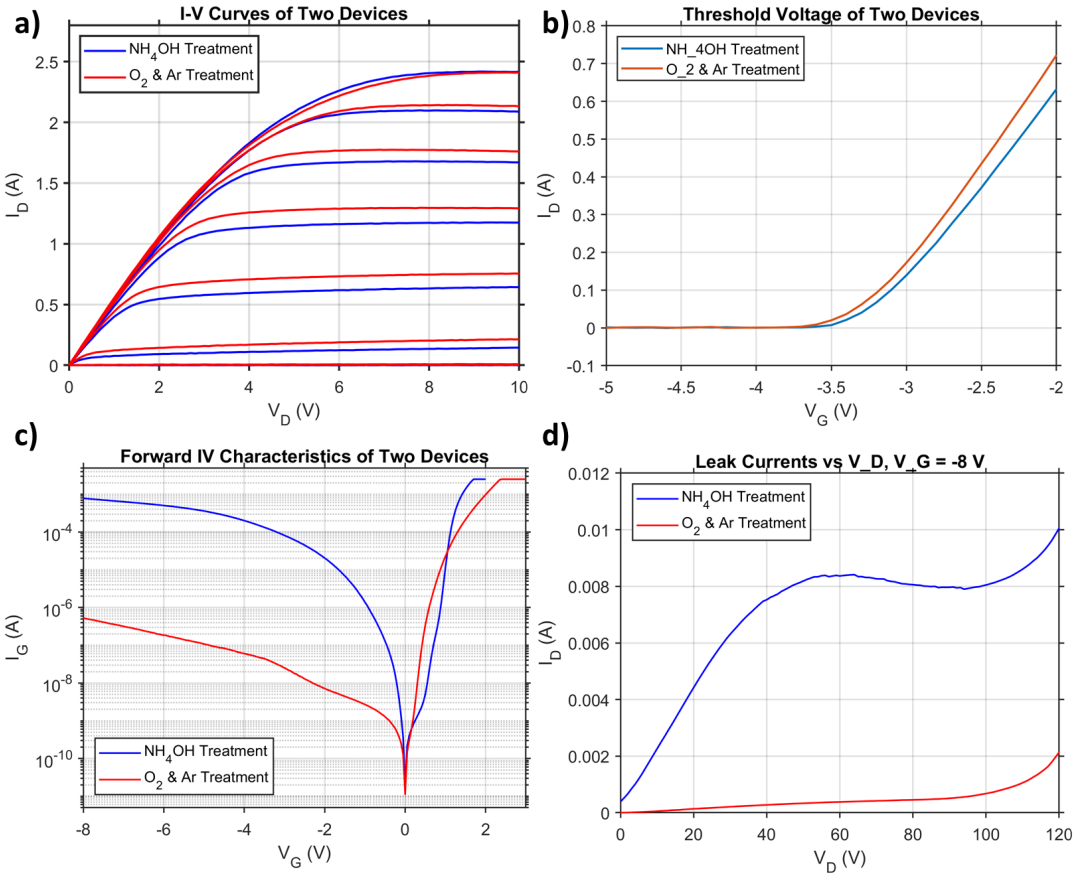


Figure 5.10: DC characteristics of devices with NH_4OH and O_2/Ar pre-gate treatments: (a) output I–V, (b) transfer characteristics, (c) forward gate I–V, (d) off-state leakage.

DC characteristics of representative devices processed with NH_4OH cleaning and with the O_2/Ar ion treatment are compared in Figure 5.10. In the plasma-treated devices, O_2 and Ar ions are applied for 10 min and 15 min, respectively. Figures 5.10(a) and 5.10(b) show the output and transfer characteristics. The plasma-treated device exhibits a slightly more negative V_{th}, while the saturation current remains essentially unchanged. The major differences appear in the

Schottky-diode characteristics and leakage. Figure 5.10(c) shows that the forward gate I–V curve is shifted to higher turn-on voltage and the reverse leakage at −8 V is reduced by more than two orders of magnitude. Figure 5.10(d) demonstrates that drain leakage under off-state bias is also reduced. These results indicate that the O_2/Ar ion treatment produces a superior Schottky interface with significantly lower leakage.

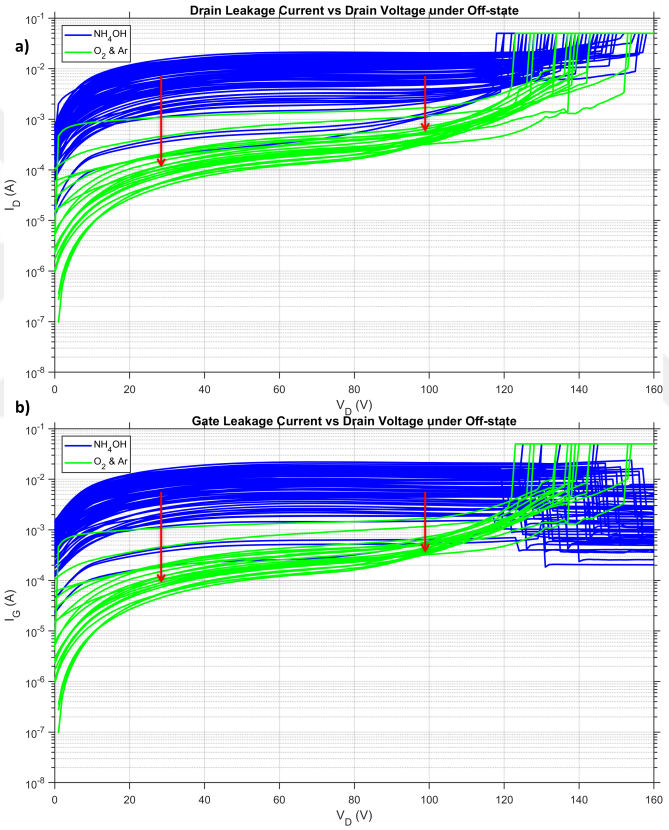


Figure 5.11: Breakdown measurements of HEMTs with NH_4OH and O_2/Ar pre-gate treatments.

Figure 5.11 compares breakdown measurements of HEMTs processed with different pre-gate treatments, including devices from multiple wafers. Figure 5.11(a) shows the drain leakage during a V_{DS} sweep from 0 to 160 V with $V_{GS} = -8$ V. The sharp increase in leakage marks breakdown. Figures 5.11(a) and 5.11(b) show that breakdown voltages are comparable for both treatments, but the devices with O_2/Ar ion cleaning exhibit gate and drain leakage currents roughly two orders of magnitude lower than those with NH_4OH.

Ultimately, reliability must be assessed using stress tests rather than only static characteristics. For this purpose, HTRB tests were carried out on devices with both pre-gate treatments. The off-state stress conditions were $V_{GS} = -8$ V, $V_{DS} = 100$ V, with base temperature stepped between 85 °C, 120 °C, 150 °C and, for some devices, 200 °C.

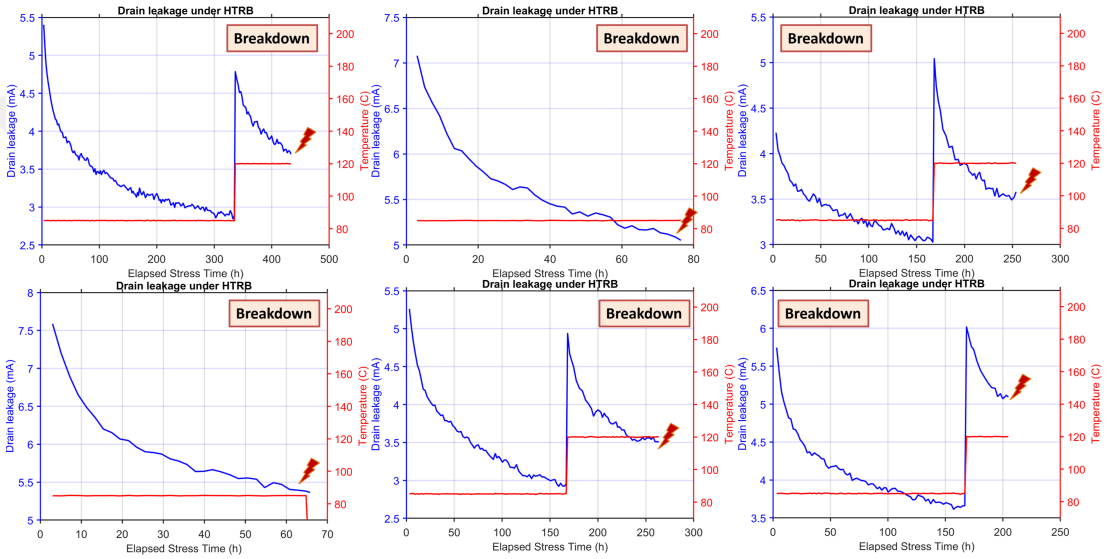


Figure 5.12: HTRB results of HEMTs with NH_4OH pre-gate treatment: drain leakage (left axis) and base temperature (right axis).

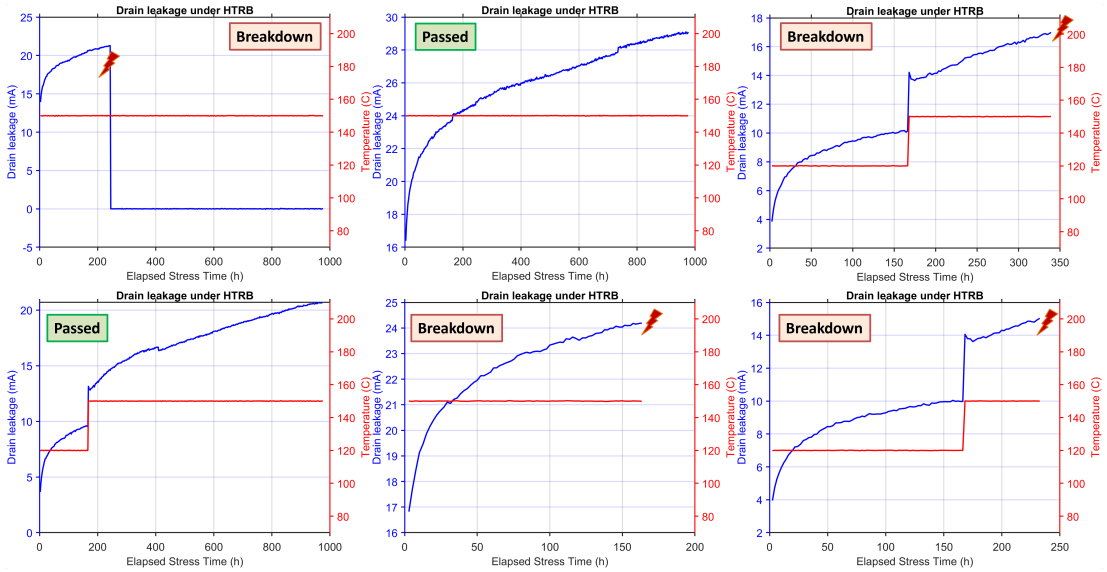


Figure 5.13: HTRB results of HEMTs with O_2/Ar pre-gate treatment: drain leakage (left axis) and base temperature (right axis).

Figure 5.12 shows HTRB results for devices cleaned with NH_4OH. The blue curves represent drain leakage, the red curves the base temperature. Six HEMTs were tested; two failed catastrophically within the first week at 85 °C, and the remaining four failed within one week at 120 °C. These results indicate poor off-state reliability for the NH_4OH-processed devices.

HTRB data for devices with O_2/Ar treatment are shown in Figure 5.13. Here, some HEMTs were stressed at 85 °C and 120 °C without any breakdown, so additional devices were tested directly at 150 °C. Out of six HEMTs, four failed catastrophically at 150 °C, while two devices successfully completed 1000 h at this temperature. Although the overall failure rate is still non-negligible, the O_2/Ar treatment clearly improves catastrophic breakdown behaviour, and the leakage currents during stress are about two orders of magnitude lower. On this basis, the O_2/Ar pre-gate treatment was adopted for subsequent fabrication runs.

5.2.2 Reliability Improvement by Nitride Deposition Techniques

As described earlier, the three SiN layers in the T-gate technology serve different purposes. Among them, the first nitride is by far the most critical, as it directly forms the SiN/AlGaN interface and thus controls trap density, leakage and high-field behaviour around the gate. Surface donor traps, hot-electron injection and interface degradation under stress all occur at this interface. If the first SiN layer is defective—due to high intrinsic stress, voids, plasma damage or poor stoichiometry—the device experiences severe reliability issues such as current collapse, surface trapping, gate lag, drain lag, V_{th} drift and premature breakdown, regardless of the quality of the upper nitride layers. The second and third SiN layers mainly play geometrical and field-shaping roles; they modulate the electric-field distribution but do not fundamentally set the trap physics. Consequently, the deposition method, stress state and damage level of the first nitride layer are of paramount importance.

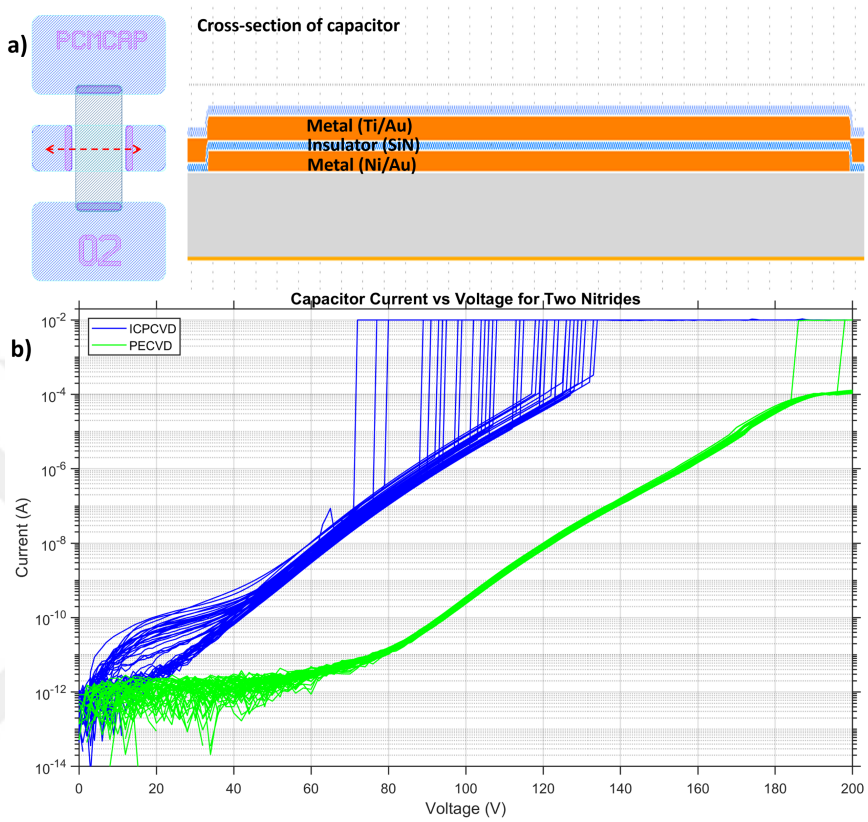


Figure 5.14: (a) Layout and cross-section of the MIM capacitor used for nitride characterization; (b) I–V characteristics of capacitors with ICPCVD and PECVD SiN.

To investigate these effects, different nitride deposition techniques and recipes were characterized using both MIM capacitors and GaN HEMTs. Two deposition systems were compared: ICPCVD and PECVD. In addition, two PECVD recipes with different deposition temperatures were evaluated.

5.2.2.1 Comparison of ICPCVD and PECVD Systems

In principle, inductively coupled plasma CVD (ICPCVD) produces a higher-density, more highly ionized plasma with lower ion bombardment energy at the substrate, whereas conventional PECVD operates with lower plasma density but higher ion energy. As a result, ICPCVD SiN is generally expected to be denser and to contain fewer traps than PECVD SiN. However, the actual film quality can

deviate from this expectation due to system-specific conditions, so experimental characterization is required.

MIM capacitors were designed as a simple test vehicle to evaluate the dielectric quality. Each capacitor consists of two Au plates separated by a 215 nm SiN layer, with an active area of 60 μm $\times$ 60 μm. The layout and cross-section are illustrated in Figure 5.14(a). Capacitance–voltage measurements yielded an effective permittivity of approximately 6.9. Leakage current and breakdown behaviour were characterized on more than 30 capacitors across a 3-inch wafer. Representative I–V curves are plotted in Figure 5.14(b). At low voltages both ICPCVD and PECVD nitrides exhibit similar leakage. As the field increases, however, the leakage of the ICPCVD nitride rises rapidly and catastrophic breakdown occurs between 70 V and 130 V. The PECVD nitride displays a more gradual increase in leakage and only two capacitors break down below 200 V. These results indicate that, in our equipment, the ICPCVD nitride is of significantly lower quality than the PECVD film.

The same ICPCVD and PECVD recipes were then used for the second nitride layer in GaN HEMTs, while all other process steps remained identical. Drain I–V measurements with $V_{\mathrm{GS}} = -8$ V and a V_{DS} sweep from 0 to 200 V are shown in Figure 5.15. Both sets of devices exhibit very similar leakage and breakdown voltages, consistent with the second nitride playing a less critical role for reliability.

HTRB tests were performed on HEMTs from the different lots using the DC-72 system. For devices with ICPCVD second nitride, the HTRB statistics are essentially those already discussed for the O_2/Ar pre-gate treatment (Figure 5.13). For devices with PECVD second nitride, 33 HEMTs were tested at base temperatures ranging from 85 °C up to 200 °C. Temperature was increased stepwise as long as devices remained functional. In total, 27 HEMTs failed catastrophically (4 at 120 °C, 14 at 150 °C, 9 at 200 °C), and 6 devices did not break down before the test was manually stopped. Overall, no clear superiority of one deposition system over the other is observed when the nitride is used as the second layer. This confirms that the quality of the second nitride is not the limiting factor for reliability

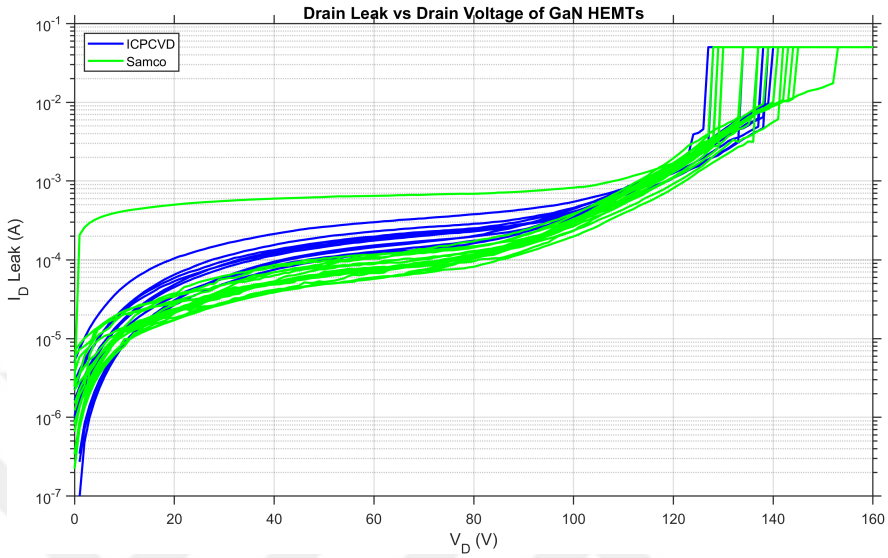


Figure 5.15: Drain leakage versus drain voltage for GaN HEMTs with ICPCVD and PECVD second SiN layers.

in this technology. Based on the capacitor data, PECVD nitride—showing lower leakage and higher breakdown—was selected for subsequent processes.

5.2.2.2 Comparison of PECVD SiN Recipes with Different Deposition Temperatures

The baseline PECVD SiN deposition recipe operated at 275 °C, a typical temperature for PECVD. Increasing deposition temperature is known to reduce hydrogen incorporation, increase film density, lower leakage and shift the film stress towards a more compressive character[86, 87, 88]. At the same time, higher temperature increases the risk of AlGaN surface oxidation and stronger plasma damage. To explore this trade-off, the first-nitride deposition temperature was increased from 275 °C to 350 °C, with other parameters adjusted to maintain stable deposition.

Figure 5.16 compares the breakdown characteristics of MIM capacitors with 270 nm thick nitrides deposited at the two temperatures. Up to about 100 V, the leakage currents are similar. At higher voltages, the high-temperature nitride exhibits four orders of magnitude lower leakage and a higher breakdown voltage around 310 V, whereas the standard-temperature nitride breaks down near 280 V.

This confirms that higher deposition temperature yields a denser, less leaky film.

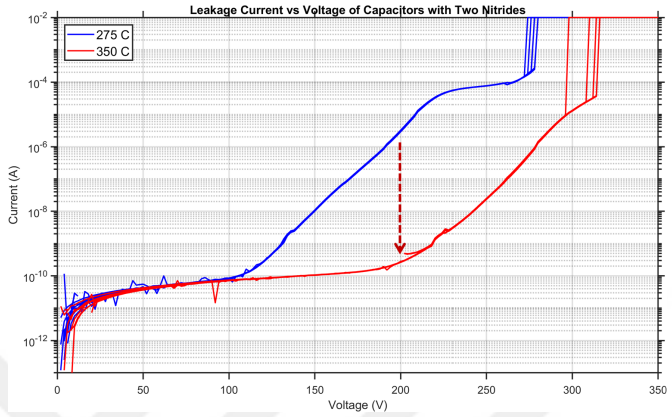


Figure 5.16: Breakdown characteristics of capacitors with PECVD SiN deposited at 275 °C and 350 °C.

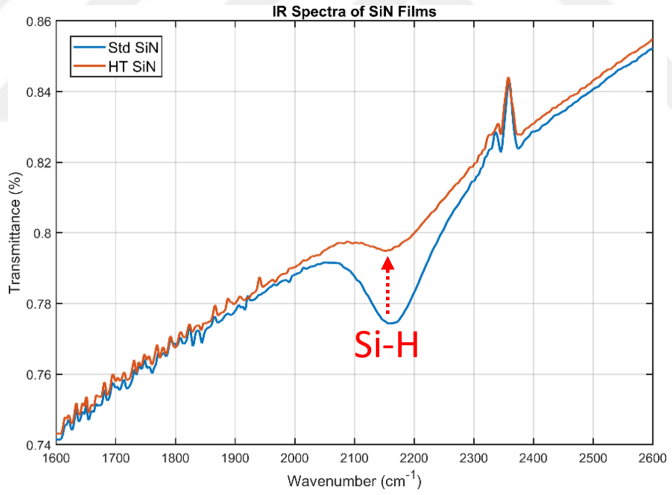


Figure 5.17: FTIR measurements of SiN films deposited at 275 °C and 350 °C.

Secondly, the hydrogen content of the deposited nitride films is evaluated using Fourier-transform infrared (FTIR) spectroscopy. SiN films are deposited on double-side-polished Si substrates, which are transparent in the infrared regime, and the transmittance of the samples is measured in the mid-infrared (MIR) range. As shown in Figure 5.17, the transmittance around 2160 cm^{-1}, corresponding to the Si–H stretching absorption, is higher for the films deposited at high temperature. This implies a lower density of Si–H bonds in the high-temperature SiN compared to the standard film, confirming reduced hydrogen incorporation at higher deposition temperature. Although no direct stress measurements are

available, this reduced hydrogen content, together with the agreement of the other film properties with theoretical expectations, strongly suggests that the film stress shifts towards a more compressive character for the high-temperature SiN.

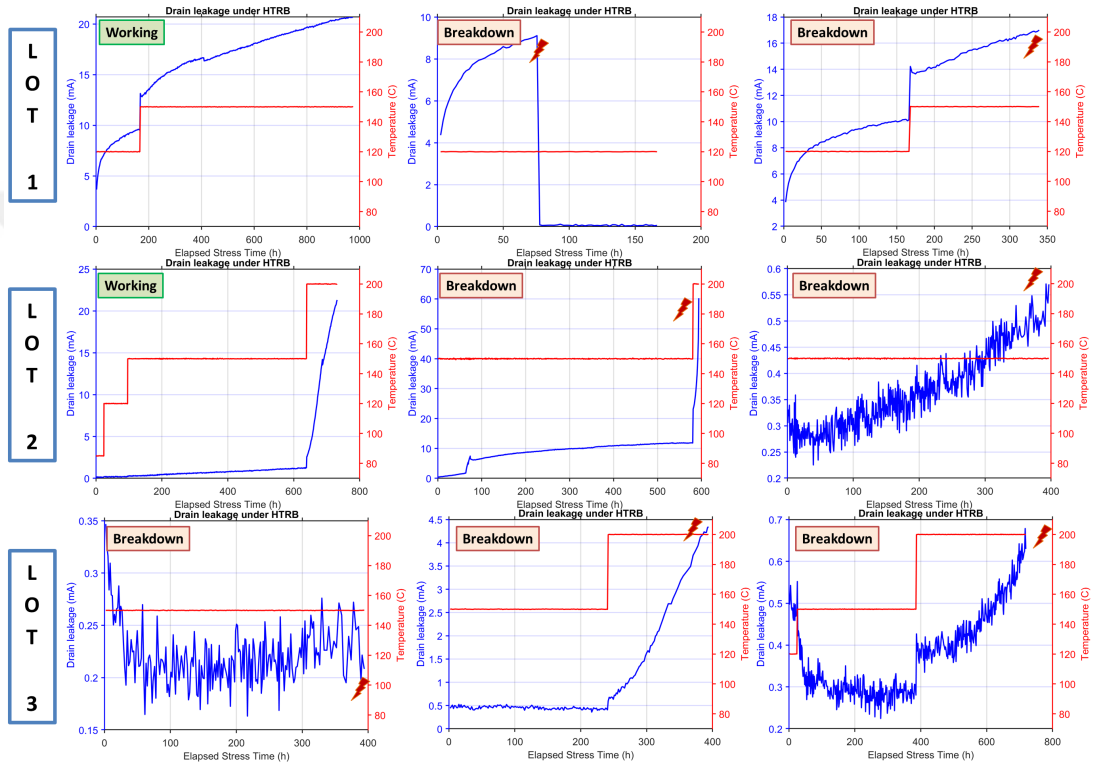


Figure 5.18: HTRB results of HEMTs with standard-temperature PECVD SiN as the first layer.

The high-temperature nitride was then used as the first SiN layer in HEMT fabrication, while the standard-temperature nitride was retained for the second layer. A control lot used the standard-temperature nitride for both layers. In all lots, O_2/Ar pre-gate treatment was applied as described previously.

HEMTs with 10.6 mm gate periphery were subjected to HTRB stress at $V_{GS} = -8$ V, $V_{DS} = 100$ V and base temperatures of 85 °C, 120 °C, 150 °C and 200 °C. Some devices were ramped through the temperature steps, while others were tested directly at higher temperatures. Figure 5.18 shows representative drain-leakage traces for devices with the standard-temperature first nitride. A total of 30 HEMTs were tested; only 3 survived until the test was stopped, while the remainder exhibited rapid leakage degradation and catastrophic breakdown.

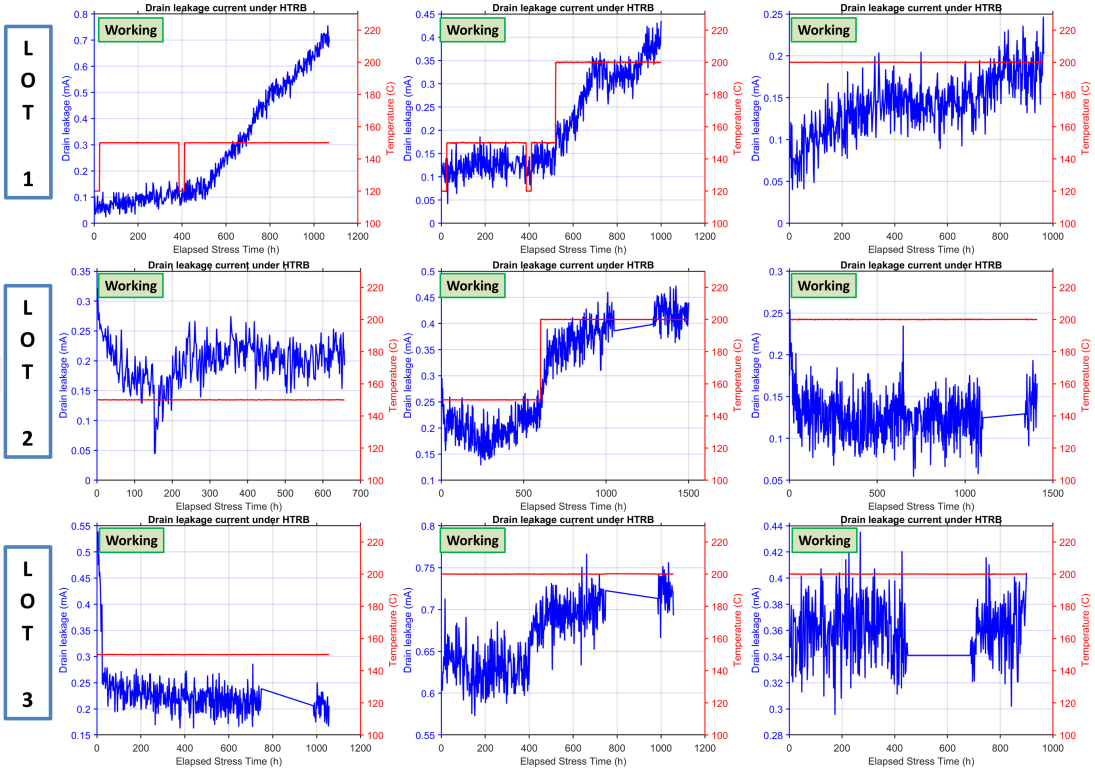


Figure 5.19: HTRB results of HEMTs with high-temperature PECVD SiN as the first nitride layer.

In contrast, Figure 5.19 shows HTRB results for devices with high-temperature first nitride. 14 HEMTs were stressed at 150 °C and 32 HEMTs at 200 °C; none of them experienced catastrophic breakdown. Some devices show modest increases in leakage under stress, but even at 200 °C the drain leakage remains below 100 μA/mm, which is well within acceptable limits. These results demonstrate that the high-temperature PECVD nitride at the first layer dramatically improves off-state reliability. The combination of higher breakdown voltage, lower leakage and a more favourable stress state in this film is believed to play a central role in this improvement.

5.2.3 Optimization of O_2/Ar Ion Treatment Durations

The effect of O_2/Ar treatment duration was further optimized using breakdown measurements and reliability tests. As shown earlier, the DC transfer and output characteristics (I_D–V_{DS}, I_D–V_{GS}) are weakly influenced by treatment conditions, whereas gate and drain leakage are more sensitive. Three treatment recipes were evaluated for three conditions:

- Lot A: 10 min O_2 + 15 min Ar,
- Lot B: 5 min O_2 + 10 min Ar,
- Lot C: 5 min O_2 + 15 min Ar.

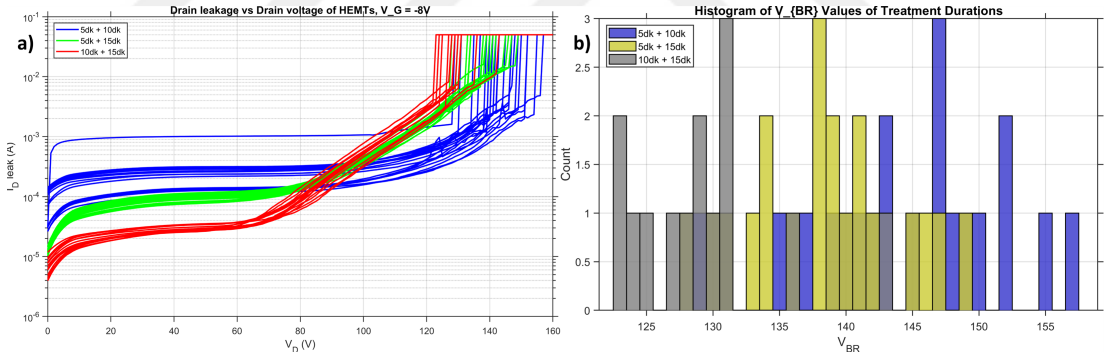


Figure 5.20: Breakdown measurements for HEMTs with different O_2/Ar treatment durations: (a) drain leakage vs. drain voltage, (b) breakdown-voltage histograms.

Drain leakage and breakdown voltage were first measured on HEMTs from each lot. Figure 5.20(a) shows representative leakage curves, and Figure 5.20(b) summarizes the breakdown statistics. Longer treatment durations reduce leakage but also tend to lower breakdown voltage. Lot A exhibits the lowest leakage but the lowest average breakdown voltage, whereas lot C presents somewhat higher leakage but the highest breakdown voltage. Reliability test results are therefore required to choose the optimum condition.

HTRB tests were performed on 10.6-mm-periphery HEMTs from all three lots. For lot A, Figures 5.21(a) and 5.21(b) show results at base temperatures of 150 °C

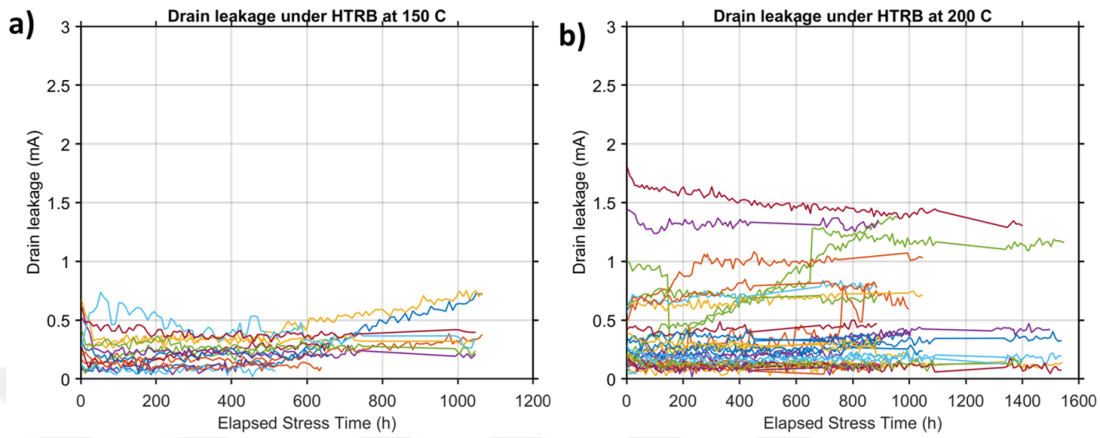


Figure 5.21: HTRB results for lot-A devices (10 min O_2 + 15 min Ar) at (a) 150 °C and (b) 200 °C.

and 200 °C, respectively, with $V_{GS} = -8$ V in all cases. Fourteen devices were stressed at 150 °C and thirty-one at 200 °C; none of them failed catastrophically. Leakage currents increase with temperature as expected but remain stable during stress.

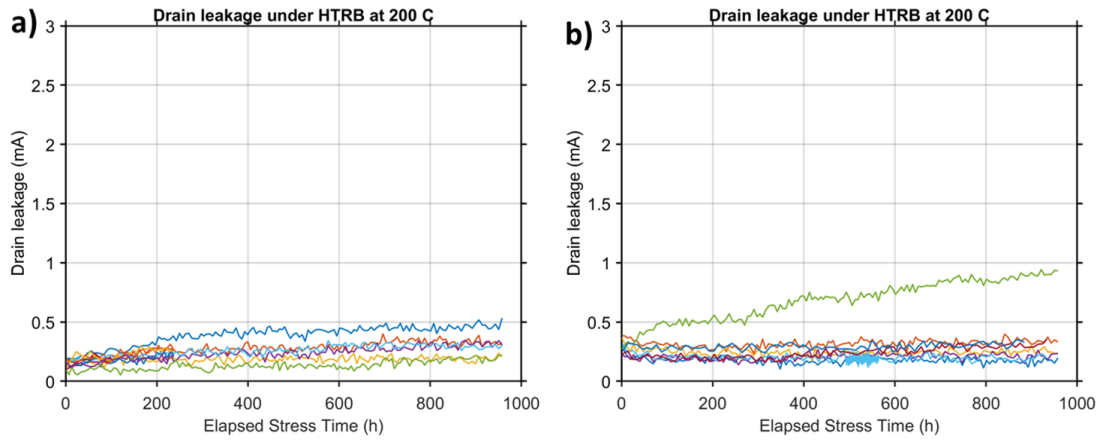


Figure 5.22: HTRB results at 200 °C for (a) lot-B devices (5 min O_2 + 10 min Ar) and (b) lot-C devices (5 min O_2 + 15 min Ar).

For lots B and C, only 200 °C HTRB was performed. Results in Figure 5.22 show that no catastrophic failures occur and leakage remains stable, similar to lot A. No clear reliability advantage is observed among the three recipes. Therefore, the lot-A condition, which provides the lowest leakage at operating voltages, was selected as the standard process despite its slightly lower breakdown voltage

in static tests.

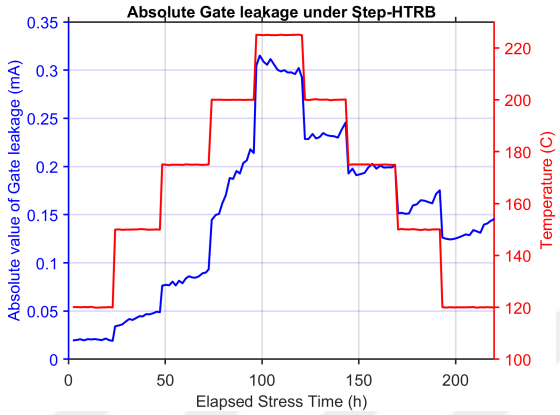


Figure 5.23: Step-HTRB result for a lot-A HEMT (10 min O_2 + 15 min Ar): drain leakage (left axis) and base temperature (right axis).

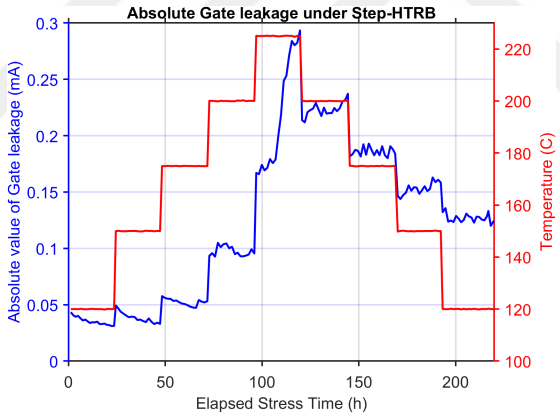


Figure 5.24: Step-HTRB result for a lot-B HEMT (5 min O_2 + 10 min Ar): drain leakage (left axis) and base temperature (right axis).

In addition to standard HTRB, a non-standard "step-HTRB" test was devised to further probe robustness under extreme conditions. Step-stress tests are commonly used at nominal operating voltage and high power to determine suitable acceleration temperatures before ALT. Here, the concept is adapted to off-state stress: devices are biased in HTRB mode while the base temperature is stepped. The sequence used was 120 °C, 150 °C, 175 °C, 200 °C, 225 °C, and then back down to 200 °C, 175 °C, 150 °C, 120 °C. Each temperature was held for 24 h, and the stress was re-applied after thermal stabilization.

Step-HTRB results for representative devices from lots A, B and C are shown in Figures 5.23, 5.24 and 5.25, respectively. In each figure, the blue curve denotes

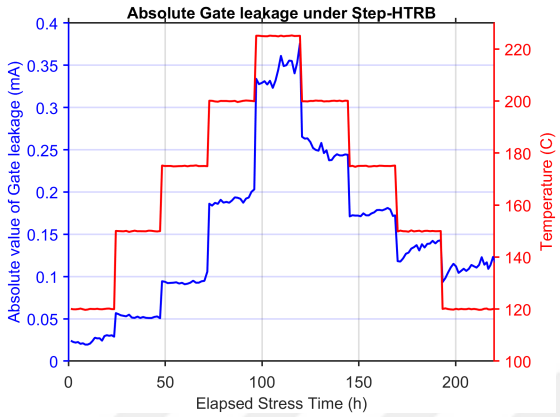


Figure 5.25: Step-HTRB result for a lot-C HEMT (5 min O_2 + 15 min Ar): drain leakage (left axis) and base temperature (right axis).

drain leakage and the red curve denotes base temperature. Leakage increases stepwise with temperature and fluctuates during stress, but in all cases the final leakage after returning to 120 °C remains at reasonably low levels. In total, 40 devices from lot A, 7 from lot B and 9 from lot C were tested; none experienced catastrophic breakdown. These results confirm that the combined improvements in layout, surface treatment and nitride deposition yield a robust GaN HEMT technology with strong off-state reliability margins.

5.3 RF-HTOL Test Performance after Process Improvements

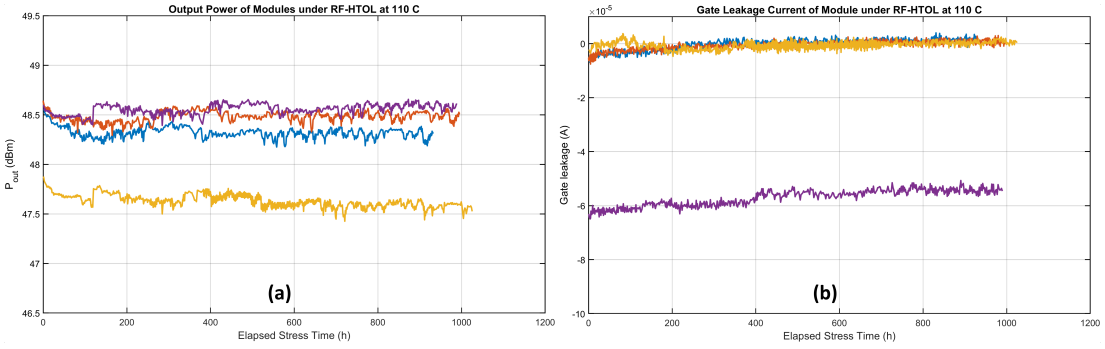


Figure 5.26: RF-HTOL results at 110 °C for modules with improved HEMTs: (a) RF output power, (b) gate leakage current.

Finally, RF-HTOL tests were repeated on the same two-stage amplifier modules described in Chapter 4, now fabricated with the improved, reliable HEMTs. The amplifier topology, matching networks and ceramic air-cavity package remained unchanged, in order to directly compare the results with the earlier, non-optimized technology.

The modules were stressed in an Accel-RF RF-16 AARTS system under the same RF-HTOL conditions as before: base temperature 110 °C, drain voltage 45 V, drain quiescent current 250 mA, 15% duty-cycle RF input at 3 GHz and approximately 49 dBm RF output power. Drain voltage and RF drive were pulsed, while the gate bias remained continuous.

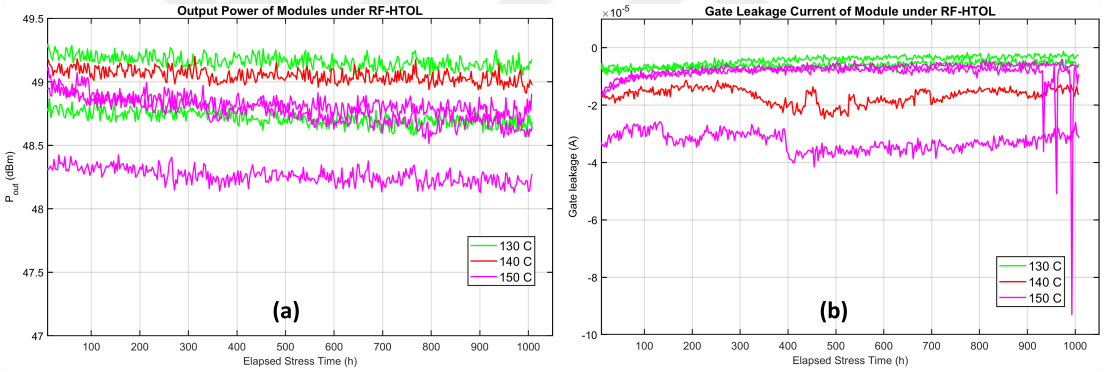


Figure 5.27: RF-HTOL results for modules with improved HEMTs at base temperatures of 130–150 °C: (a) RF output power, (b) gate leakage current.

Four modules were tested at 110 °C, and none of them suffered catastrophic burnout before the test was manually stopped. Figure 5.26(a) shows the evolution of RF output power versus stress time, and Figure 5.26(b) shows the corresponding gate leakage currents. Output power for all modules decreases by only about 0.3 dB, mostly within the first hours, after which it stabilizes. Gate leakage behaviour is markedly different from that of the initial technology: leakage currents remain below 100 μA and tend to decrease slightly with stress time.

To further challenge the improved technology, additional RF-HTOL tests were run at higher base temperatures of 130 °C, 140 °C and 150 °C, while keeping all other conditions identical. Two modules were stressed at 130 °C, one at 140 °C

and three at 150 °C. All devices completed 1000 h of RF-HTOL without catastrophic failure or significant degradation. Figure 5.27 summarizes the results: RF output power decreases by less than 0.5 dB over the entire stress period, and gate leakage currents remain below about 50 μA. Although leakage increases slightly with temperature, it does not show any progressive degradation under stress.

These RF-HTOL results, together with the extensive DC-HTOL and HTRB data presented earlier in this chapter, demonstrate that the combined process optimizations—PMA and gate-foot etch improvement, O_2/Ar pre-gate treatment, and high-temperature PECVD first nitride—lead to a substantial enhancement of both off-state and RF operating reliability in the GaN-on-SiC HEMT technology.

Chapter 6

The origin of gate degradation under HTRB operation: Buffer engineering to suppress impact ionization in GaN HEMT

6.1 Preface

This chapter of the thesis is based on the publication "The origin of gate degradation under HTRB operation: Buffer engineering to suppress impact ionization in GaN HEMT", M.C. Soydan, A.A. Joya, A. Ghobadi, E. Ozbay, IEEE Access. 2025. Adapted (or "Reproduced in part") under a creative commons license from IEEE.

This chapter investigates the origin of gate degradation in AlGaN/GaN HEMTs under high-temperature reverse bias (HTRB) conditions and proposes a buffer engineering strategy to mitigate this degradation. Transmission electron microscopy (TEM) analysis, HTRB test and TCAD simulations are carried out, and impact ionization mechanism is revealed as the dominant mechanism

on gate leakage increase. To address this issue, impact ionization is suppressed via thinning the channel GaN and adapting the growth conditions. Additionally, the impact of C-GaN thinning on breakdown characteristics and RF performance is discussed. Overall, the findings provide insights into the root cause of gate degradation and offer a buffer engineering strategy to minimize gate degradation under deep off-state stress.

6.2 Introduction

A critical parameter for assessing the reliability of GaN HEMTs under high-power and high-frequency conditions is the high-temperature reverse-biased (HTRB) reliability. Under HTRB stress, several key electrical parameters of GaN HEMTs, including the threshold voltage, saturated drain current, subthreshold slope, and others, undergo degradation. Among these parameters, the gate leakage current is of particular concern, as it provides the most direct and early indication of device aging [89]. In fact, many of the other degraded parameters under HTRB conditions can be directly attributed to the deterioration of the gate [90][91]. Therefore, controlling the gate leakage current is a critical priority for enhancing the reliability of these devices under off-state high-drain bias stress.

Whereas the origin of this degradation and the main contributing parameters are not thoroughly studied, gate leakage enhancement, under HTRB operation, primarily arises from the combination of intense local electric fields near the gate region [92] and the presence of dielectric/interface traps [93]. A variety of strategies have been explored to reduce the density of interface traps and improve off-state gate leakage such as O_2-Ar interface treatment [94]. Additionally, efforts have been made to optimize the electric field near the gate to reduce off-state leakage, using approaches such as unintentionally doped GaN (UID-GaN) growth beneath the gate in P-GaN HEMTs[95], dual-metal-gate (DMG) structures [95], meandering gate edges [96], and gate and source-terminated field plates [97]. Whereas these methods have shown varying degrees of effectiveness, they often introduce limitations, including increased structural complexity, and

are not always sufficient for metal-insulator-semiconductor (MIS) or metal-oxide-semiconductor (MOS) gate contacts, where traps are inevitable. In contrast, epitaxial buffer engineering could offer a more robust approach to control the electric field near the gate and to suppress impact ionization, a primary contributor to gate degradation under HTRB operation [98]. Despite its potential, there is limited literature focusing specifically on the use of epitaxial buffer engineering to reduce gate leakage under HTRB stress.

In this study, transmission electron microscopy (TEM) was employed to examine the gate–AlGaN interface, revealing the presence of a thin dielectric layer. TEM Energy-dispersive X-ray (EDX) analysis confirmed the presence of an oxygen peak adjacent to the gold and nickel peaks, indicating that the gate forms a MOS contact with the AlGaN barrier. This oxide layer was identified as the primary source of gate degradation. A leakage mechanism is developed in this work, linking impact ionization to off-state gate leakage, primarily driven by Fowler–Nordheim (FN) tunneling through the oxide barrier. To mitigate gate degradation under HTRB stress conditions, we propose a buffer engineering strategy aimed at improving the electric field distribution and minimizing impact ionization beneath the gate and field plate regions. Post HTRB (conducted over 1000 hours) leakage data demonstrates an approximately 90% improvement in average gate leakage compared to the baseline devices. This significant improvement is attributed to a more favorable electric field distribution and suppressed impact ionization rates consistent with prediction from Silvaco TCAD simulations, which were calibrated to align with the device characteristics in [99], ensuring consistency with previously reported results from our research center. Whereas achieving significant improvement in HTRB performance, no major degradation is seen in the DC and RF performance of the buffer-engineered devices. Overall, this work provides a fundamental analysis on the origin of gate degradation phenomenon with a novel approach that connects impact ionization to gate degradation and, in response to the reported works of [95, 96, 97] which increase complexity of the HEMT fabrication, presents a simplistic solution of buffer engineering to prevent gate degradation.

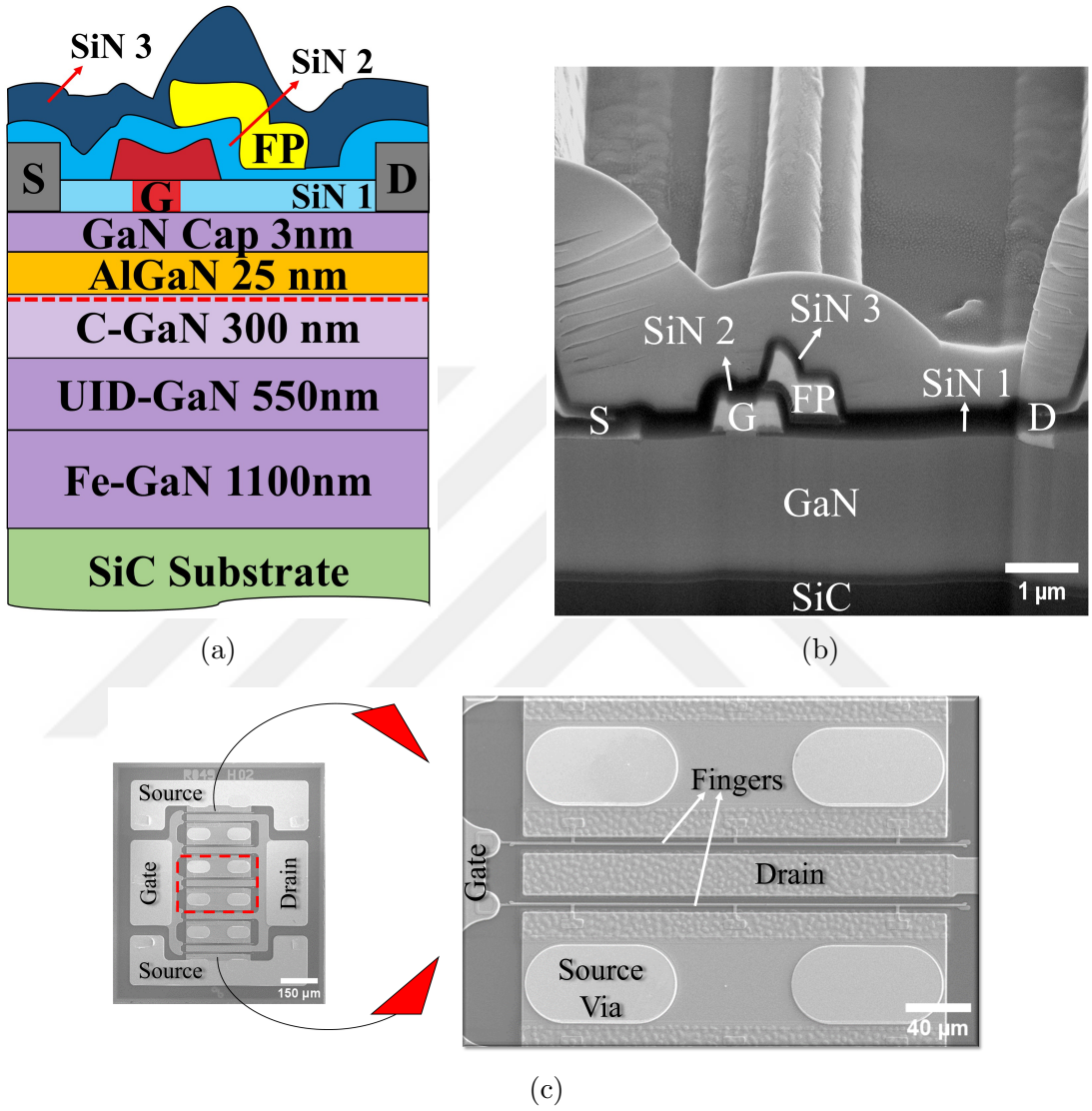


Figure 6.1: (a)Schematic of the investigated HEMT, (b) SEM image of fabricated HEMT, (c) Zoomed SEM image of 10 finger 2.65 mm long fabricated HEMT with gate fingers, drain and source.

6.3 Device Design and Fabrication

A cross-sectional schematic of the AlGaN/GaN HEMT is shown in Fig. 6.1(a). The epitaxial layers were grown on a 3-inch SiC substrate using metal organic chemical vapor deposition (MOCVD), starting with a 120 nm AlN nucleation layer to alleviate lattice mismatch. This was followed by a 1100 nm semi-insulating GaN buffer and 550 nm of UID GaN layer. Further, 350 nm of Channel

GaN was deposited with a 25 nm $Al_{0.25}Ga_{0.75}N$ barrier layer and a 3 nm GaN cap layer on top to complete the epitaxial growth.

Device fabrication started with the formation of ohmic contacts by depositing Ti/Al/Ni/Au (15/90/50/50 nm), followed by rapid thermal annealing at 875 °C for 30 s in a nitrogen ambient, providing a contact resistance of approximately 0.4 Ω·mm by using transfer length method (TLM). Mesa isolation was performed via reactive ion etching (RIE). A three-layer plasma enhanced chemical vapor deposition (PECVD) SiN was used to obtain T-shape gate, passivate the surface, encapsulate the gate, and form the field plate. Before the gate metallization, a surface treatment process using O_2 and Ar ions is applied. Schottky gates were patterned by electron beam lithography and formed by depositing Ni/Au (100/400 nm). The gate length (L_G) and width (W_G) were 0.4 μm and 265 μm, respectively. Final interconnect metallization was performed to complete the device fabrication. The SEM image of cross-section of the fabricated HEMT is shown in Fig. 6.1(b). This process is then turned to a 10 finger 2.65 mm HEMT device as shown in Fig. 6.1(c) with gate, drain, and source pads. It is further zoomed in to look at the gate fingers, source vias and drain contacts.

6.4 Gate Degradation

The reliability of GaN HEMTs is strongly dependent on the stability and performance of the gate region. In particular, under off-state stress conditions, the gate is highly susceptible to leakage, which ultimately compromises the overall device reliability. To systematically investigate this phenomenon, AlGaN/GaN HEMTs were fabricated and subjected to HTRB conditions to monitor gate behavior over an extended period of 1000 hours. The applied stress conditions were set at $V_g = -8$ V, $V_d = 125$ V, and $T = 150$°C, thereby subjecting the gate region to intense electrical and thermal stress. As illustrated in Fig. 6.2(a), the gate leakage current exhibits a clear degradation trend with time, with near an order of magnitude leakage current enhancement. A total of ten devices from the

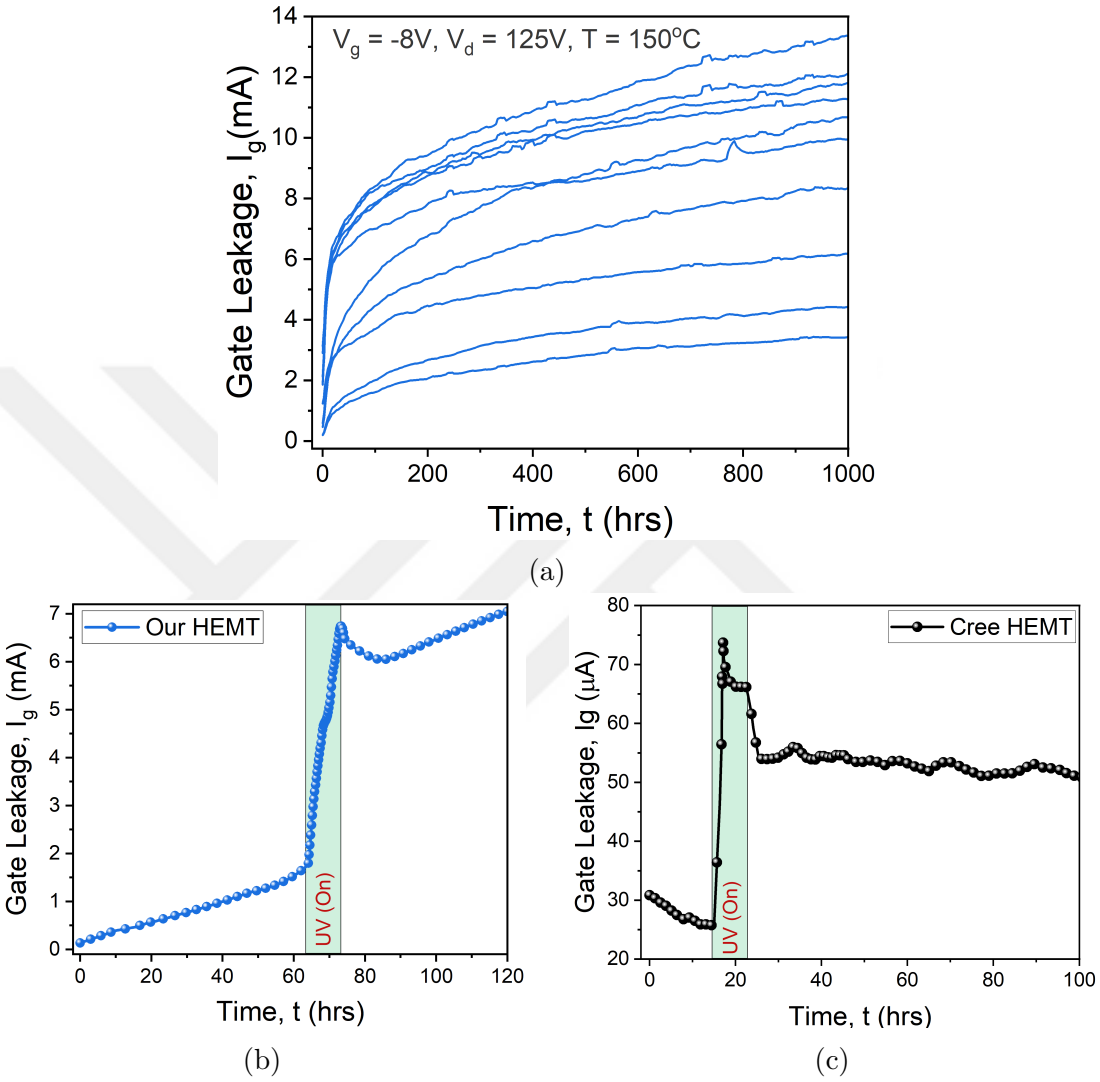


Figure 6.2: (a) Gate current from HTRB tests at (V_g,V_d)=(-8 V,125 V), (b) operation of fabricated GaN HEMT under UV radiation to suspect impact ionization as the reason of gate degradation, (c) operation of a known commercial GaN HEMT (Cree) under UV radiation

same wafer sample were analyzed, and their leakage characteristics were continuously monitored. The results reveal that the gate current increases progressively during stress application. Initially, a rapid increase is observed within the first 200 hours, after which the leakage current continues to rise but at a more gradual and stable rate.

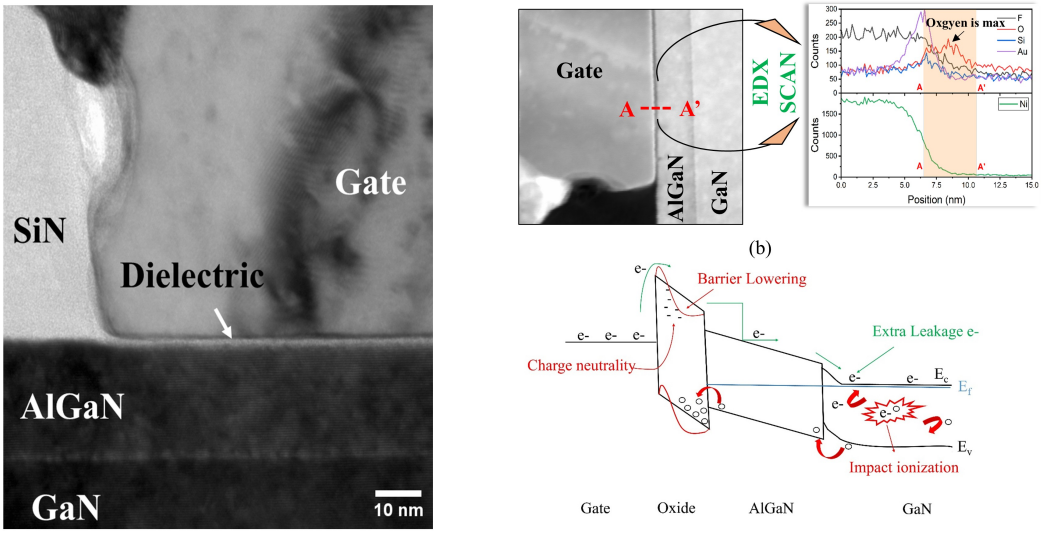


Figure 6.3: (a) TEM image of gate-AlGaN contact to show a dielectric present between the gate metal, (b) EDX scan of gate-AlGaN contact shows an oxygen peak at the interface, and (c) a proposed mechanism that shows energy band profile of gate-oxide-AlGaN contact under HTRB conditions exhibiting hole accumulation in oxide layer causing oxide barrier thinning to maintain charge neutrality inside the oxide layer.

This progressive increase in leakage current is a strong indication of gate degradation under prolonged HTRB stress. The elevated electric field around the gate region (specifically in the drain-side of the gate edge) facilitates electron transport across the AlGaN barrier, thereby initiating gate leakage. An important physical mechanism that further amplifies this effect is the generation of hot electron-hole pairs through impact ionization. To simulate this phenomenon, UV light exposure is used to generate a large density of electron-hole pairs, under high electric fields of HTRB operation. As seen in Fig. 6.2(b), upon the UV lamp turn-on, a sudden surge in gate leakage is observed. The leakage current does not recover as we turn off the lamp, demonstrating irreversible degradation effects in the gate region. This experimental observation serves as clear evidence that the excess of holes within the buffer (as electrons are already there with high densities) plays a central role in accelerating gate degradation in the investigated AlGaN/GaN HEMTs.

For comparison, the same measurement condition was applied to a commercially available CREE GaN HEMT (CGHV40050F) under identical UV exposure conditions because this HEMT has similar operating voltage, DC/RF characteristics, and gate periphery compared to our device. The gate leakage versus time characteristics for the CREE device are presented in Fig. 6.2(c). The overall qualitative behavior of the leakage current, particularly the UV-induced acceleration, shows strong similarities to that of our fabricated devices. Nevertheless, quantitative differences emerge in the post-illumination recovery behavior, as the commercial device exhibits a distinct leakage trend after the UV source is removed. This comparative study highlights that whereas the fundamental degradation mechanism driven by impact ionization is universal across GaN HEMTs, the magnitude and recovery dynamics of leakage strongly depend on device structure and fabrication process.

6.5 Causes of Gate Degradation

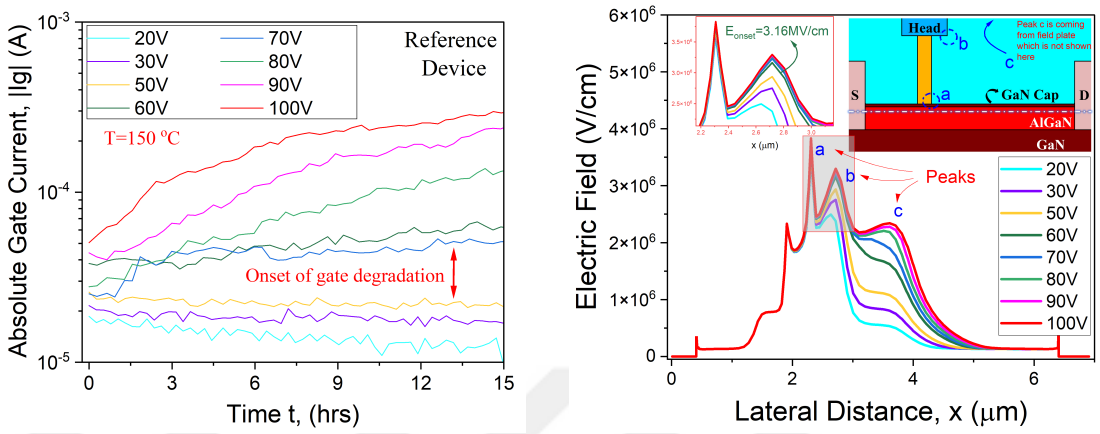
Under off-state conditions with high drain bias, electrons are accelerated to high kinetic energies, enabling them to collide with bound electrons in the GaN lattice and generate electron–hole pairs [100]. These newly created carriers, in turn, can repeat the process, thereby sustaining a chain reaction that contributes to an increase in drain-to-source leakage current. However, the specific mechanism responsible for the observed increase in gate leakage current under these stress conditions remains less clearly understood and requires further exploration.

The observed degradation of gate leakage current under HTRB stress is commonly found in metal–insulator–semiconductor field-effect transistors (MISFETs). Also, in GaN HEMT, the nitride/AlGaN interface under the gate has already been reported as a dominant contributor to reverse-bias gate leakage conduction [98]. To determine the underlying source of gate degradation in our AlGaN/GaN HEMTs subjected to HTRB stress, TEM analysis was employed to examine the gate–AlGaN interface. This investigation revealed the presence of a thin dielectric interlayer situated between the gate metal and the AlGaN barrier.

A TEM image highlighting this observation is provided in Fig. 6.3(a). To further characterize the nature of this interlayer, some of the devices were subjected to energy-dispersive X-ray spectroscopy (EDX) analysis. The obtained EDX results contain traces of Au, Si, F, O, and Ni and are presented in Fig. 6.3(b). A pronounced oxygen peak was detected in proximity to the characteristic gold and nickel peaks of the gate stack. Importantly, no silicon related peaks were identified at the oxygen peak position in gate–AlGaN interface. Considering the fact that the top epitaxial surface is GaN cap, most likely, the O_2 ions are positioned on Nitrogen vacancy points to form Ga_XO_Y compounds on the surface, during pre-gate metallization treatment process.

The presence of this oxide layer provides a plausible explanation for the observed gate leakage enhancement under HTRB operation. A simplified energy band schematic depicting the proposed leakage mechanism is presented in Fig. 6.3(c). Under HTRB stress, impact ionization events, occurring within the GaN channel, generate excess holes that sweep and accumulate near the source-side gate edge, under a static electric field. Driven by the applied reverse gate bias in the HTRB test, these holes migrate towards the AlGaN barrier. Due to its non-crystalline defective structure, the interfacial gallium oxide acts as a reservoir for both electron and hole trapping. Once the impact-generated holes traverse the AlGaN barrier, they face a high energetic barrier with a high density of trap states, due to the Ga_2O_3 layer. Therefore, holes are captured within the oxide layer, resulting in a net positive charge buildup. In response, electrons from the gate metal are injected into the oxide to maintain local charge neutrality. These injected carriers also become trapped, altering the effective barrier height of the oxide and facilitating subsequent electron tunneling. Consequently, additional electrons from the gate metal can tunnel through the oxide layer and consequently, the gate leakage enhances. These injected electrons accelerate under a high HTRB field and re-trigger impact ionization-induced gate degradation through a positive feedback mechanism.

Considering the fact that this ultra-thin oxide layer is inherent to GaN HEMT gate formation, any pre-gate metallization treatment cannot fully remove it, as shown in the commercial HEMT device. Therefore, in the light of the proposed



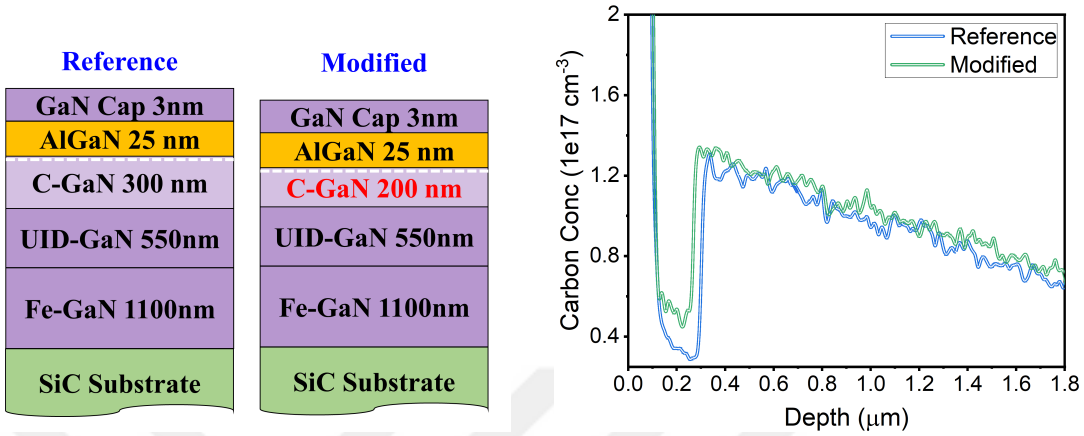
(a) (b)

Figure 6.4: (a) HTRB tests, with varying V_d, on reference HEMTs to show onset drain voltage for gate degradation at $T = 150°C$ and V_g=-8 V (b) a lateral cutline of the reference device from electric field simulation at varying V_d from 30 V to 100 V to predict the electric field at the onset drain voltage of gate degradation

degradation mechanism, the best way to control and mitigate this gate degradation is to reduce the impact ionization rate within the GaN layer, through epitaxial buffer engineering. Buffer engineering can also relax the field spot at the gate edge and further decelerate gate degradation.

6.6 Buffer Engineering to Prevent Impact Ionization

The onset of gate degradation in GaN HEMTs is primarily triggered by the generation of electron–hole pairs through the process of impact ionization. This takes place at a V_d of 50 V to 60 V in our devices (reference). Fig. 6.4(a) shows the HTRB absolute gate leakage of reference HEMTs at varying V_d values for 15 hours. The $|I_g|$ remains constant or decreases for V_d below 50 V. At V_d=60 V, a sudden degradation in $|I_g|$ is seen. It aggravates faster at higher drain voltages due to a higher impact generation rate. To predict the onset electric field, E_{onset}, at which gate degradation begins, an electric field simulation is conducted using a calibrated Silvaco TCAD software. At varying V_d from 20 V to 100 V, the electric



(a) (b)

Figure 6.5: (a) Epitaxial differences between reference and proposed modified device to mitigate gate degradation and (b) SIMS data to show the difference in the carbon impurity profile between the reference and modified device

field along a lateral cutline through the AlGaN barrier in the reference device is shown in Fig. 6.4(b). Three electric field peaks "a", "b", and "c", are seen and referred to as due to the gate foot edge, the gate head edge, and the field plate edge, respectively. Since the onset voltage from Fig. 6.4(a) is seen to be around 60 V, the electric field at this voltage is found to be 3.16 MV/cm. Thus, if the holes accumulated under the gate face a field greater than E_{onset}, the device will start to suffer from gate degradation. But if the impact ionization rate can be effectively suppressed, the subsequent gate degradation can be minimized.

To address this challenge, this study introduces the use of a modified c-GaN buffer in HEMTs as a strategy to mitigate excessive impact ionization and reduce gate degradation. A comparison between a reference epitaxy and the proposed modified C-GaN epitaxy is presented in Fig. 6.5(a). In the modified C-GaN design, the layer thickness is reduced by 100 nm. Also, the growth conditions have been adopted to introduce higher Carbon levels, compared to the reference sample, as seen in the SIMS data shown in Fig. 6.5(b). To enhance Carbon incorporation the growth pressure of the MOCVD chamber is reduced from 200 mbar to 150 mbar and surface temperature is declined from 1100 $°C$ to 1075 $°C$. The influence of these modifications on gate leakage current is highly significant, as demonstrated in Fig. 6.6. This figure shows the maximum gate leakage current

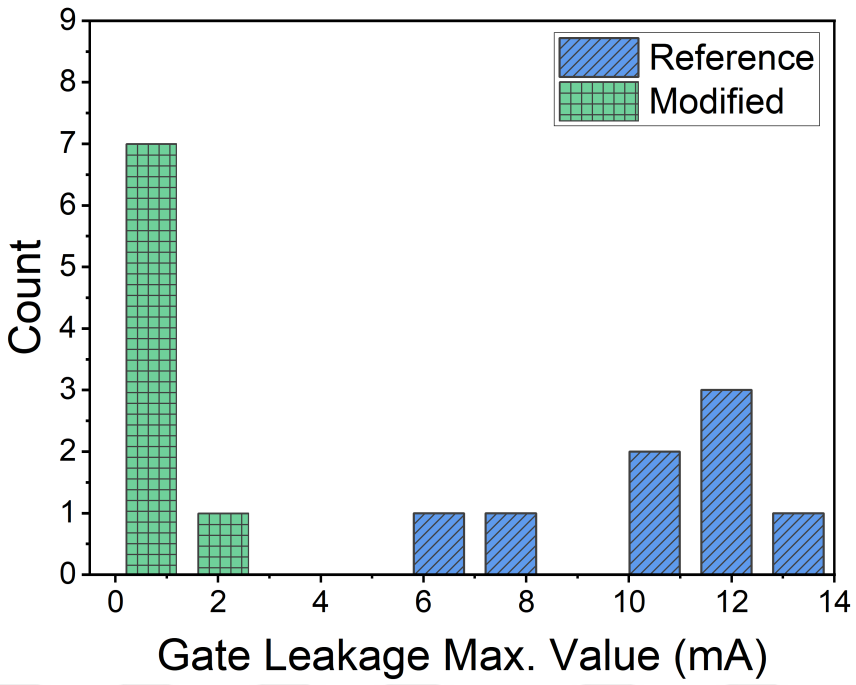
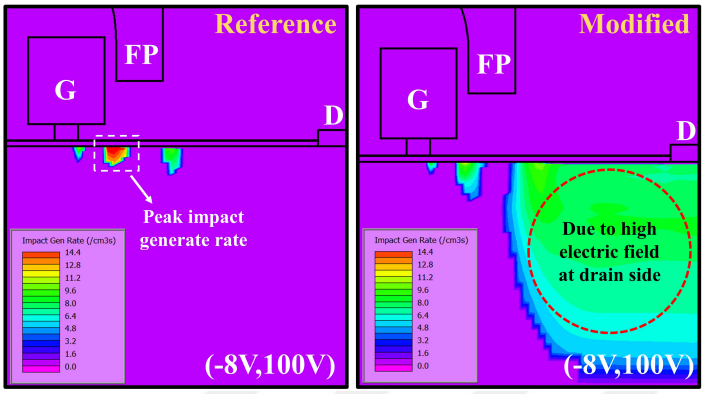


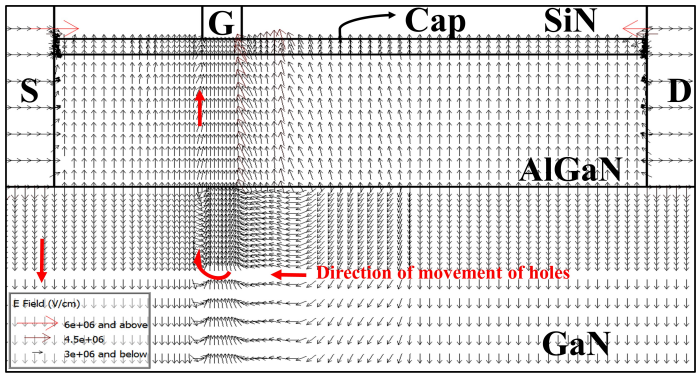
Figure 6.6: Maximum gate leakage value vs number of HEMTs in both reference and modified samples under HTRB conditions

values recorded after 1000 hours of HTRB stress for both device types. The modified C-GaN HEMTs consistently exhibit maximum gate leakage currents below 1 mA after 1000 hours for the majority of tested devices. By contrast, the reference HEMTs display much larger leakage values, scattered in the range of 6 mA to 13 mA, with an average around 10.5 mA. This corresponds to nearly a 90% reduction in gate leakage current under HTRB operation for the engineered epitaxial configuration.

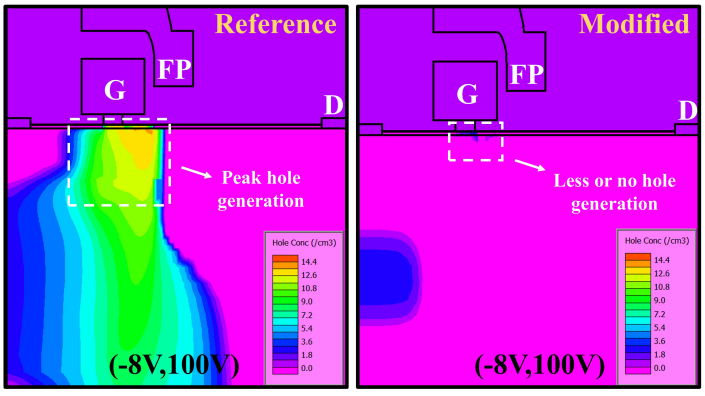
The underlying mechanism behind this improvement can be explained by considering the role of each layer within the epitaxy. UID-GaN typically contains a higher density of acceptor-type traps. In the modified design, the UID-GaN region is positioned closer to the gate, allowing these acceptor traps to participate more effectively in field modulation. Moreover, due to the altered growth conditions, the carbon levels are even higher in modified design and lead to higher electron trapping. Under HTRB stress, the acceptor traps in the UID-GaN layer become ionized, form stationary negatively charged points within the bulk, and act as a termination point of access region electric field. This leads to an increased



(a)



(b)



(c)

Figure 6.7: Simulation results under HTRB at (V_g,V_d)=(-8 V,100 V) for (a) impact generation profile (b) field vectors in reference and modified HEMTs that lead to (c) hole accumulation under the gate on the source side

vertical component of the electric field while decreasing the lateral field. This, in turn, causes an overall reduction of the electric field profile near the gate region, primarily through Coulombic repulsion [101].

Fig. 6.7(a) illustrates Silvaco TCAD simulation results comparing the impact generation rates in reference and modified C-GaN HEMTs under bias conditions of (V_g, V_d)=(−8 V, 100 V). The results clearly show that the intense impact generation peaks located under the gate foot and head edges in the thick buffer design are significantly reduced in the thin C-GaN structure. Since thinner channel epitaxy brings UID GaN closer to the 2-DEG, the ionized carbon traps under HTRB conditions, redistribute the electric field in such a way that the vertical field component is increased, leading to reduced field at the gate edge but increases at the drain side. That is why, on the drain side, there is high impact generation in thin C-GaN epitaxy. Due to this reduction in local electric field strength, channel electrons are subjected to less acceleration, which directly mitigates the rate of impact ionization in the critical regions beneath the gate edge. Another way to characterize this process is to track the hole distributions within the bulk, since impact ionization generates e-h pairs, and the internal electric field drifts them toward the contacts. The electric field vector profile is shown in Fig. 6.7(b). The electric field vector profile for both reference and modified HEMTs is seen to be identical in simulations. Only the vector magnitudes slightly differ due to electric field improvement in modified HEMTs. Therefore, the electric field vector profile for one of the devices is shown. The field vectors go away from the drain but bend and accumulate under the gate, specifically on the source side. Therefore, the impact generated holes also accumulate under the gate (trajectory of holes shown with red arrows). Due to the suppressed impact ionization rates in modified HEMTs, the hole density is significantly lower compared to the reference HEMT design, as seen in Fig. 6.7(c). As already explained, due to the gate bias, these holes are lined up under the gate region, cross the AlGaN barrier, and accumulate at the interfacial oxide layer. Some of these holes get trapped inside oxide and cause oxide barrier thinning leading to FN tunneling and gate degradation under HTRB conditions as explained in section IV.

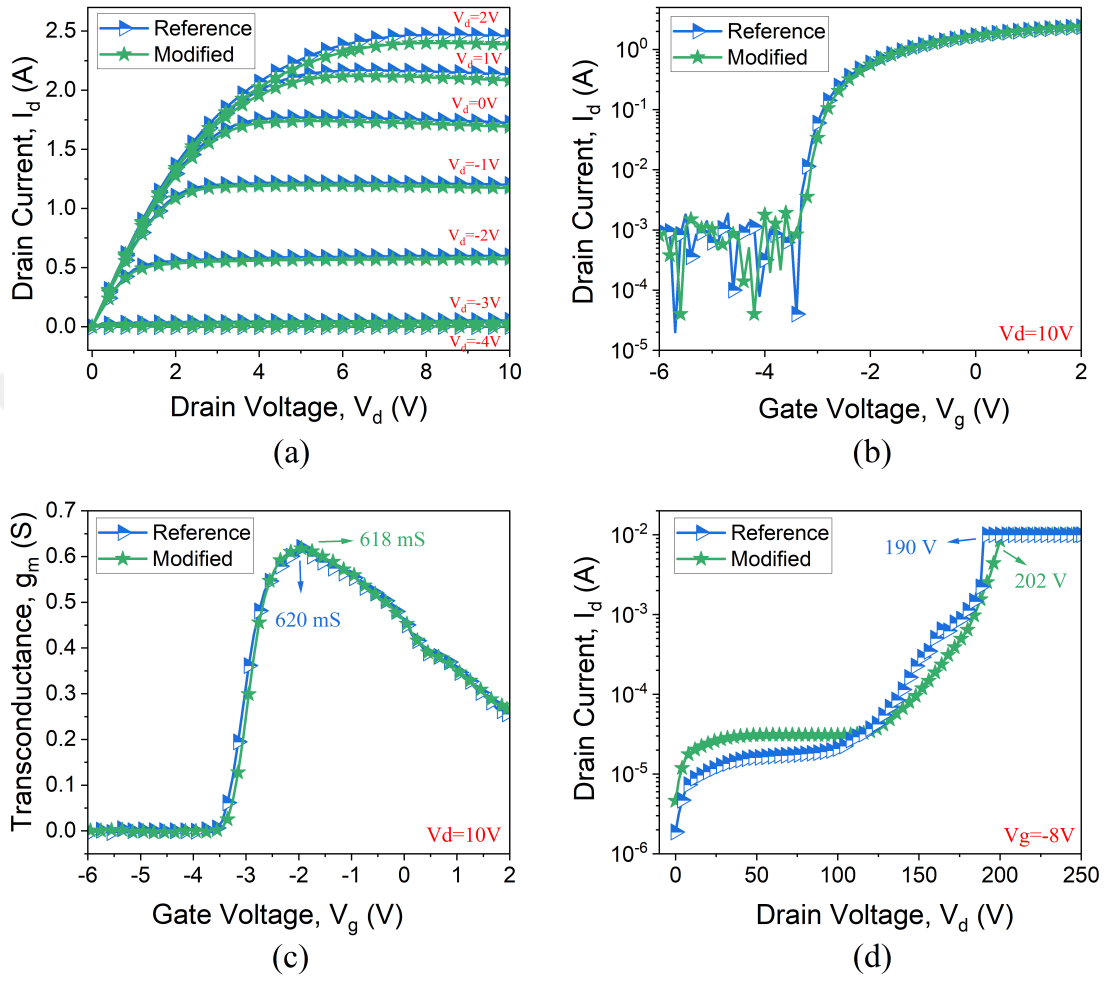


Figure 6.8: Comparison of (a) I_{dss}, (b) V_{th}, (c) g_m, and (d) $I_{d,off}$ between reference and modified HEMTs

6.7 DC/RF Performance

The DC characterization of the reference and modified HEMTs is also performed to predict a possible trade-off between improved gate degradation and DC performance. The I_{dss}, V_{th}, g_m, and $I_{d,off}$ (off-state drain leakage) are shown in Fig. 6.8. Fig 6.8(a) shows an I_{dss} degradation of 3% in the modified HEMTs due to higher carbon concentration in C-GaN and, consequently, lower v_{sat} to offer resistive flow to channel electrons. But the Fig. 6.8(b-c) shows no change in V_{th} and g_m for both modified HEMTs and reference HEMTs. Fig. 6.8(d) presents off-state $I_d - V_d$ plot at V_g=-8V. As a consequence of the SIMS profile shown in Fig. 6.5(b),

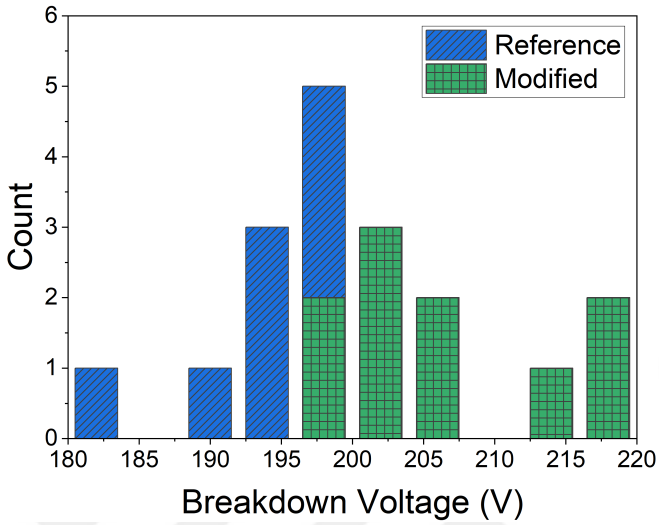
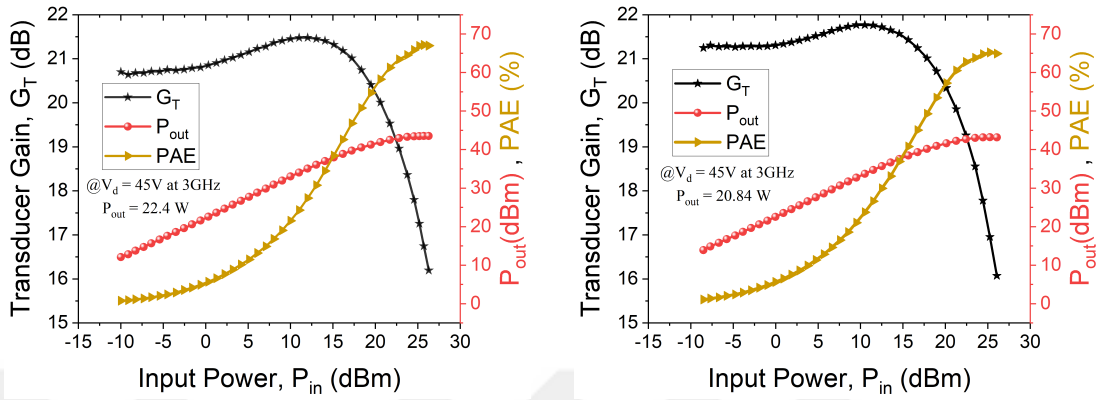


Figure 6.9: Breakdown voltage histograms for reference and modified HEMTs showing V_{br} improvement

the modified HEMTs suffer from less drain leakage at high V_d as compared to reference HEMTs and, therefore, evidence higher confinement of electrons in the C-GaN. There is a higher drain leakage at small V_d in modified HEMTs in the start but that off-set comes from random causes since the drain leakage curve for modified HEMTs stays below the one for reference HEMT at large V_d and, therefore, the device shows higher breakdown voltage. Overall, no significant trade-off is observed in the DC performance of the modified devices; rather, an improvement in the off-state drain leakage is seen in the modified HEMTs, attributed to the high carbon profile in the C-GaN.

The influence of the thin C-GaN buffer on device breakdown characteristics is also investigated. The breakdown voltages (V_{br}) of ten HEMTs from each of the thick and thin C-GaN epitaxy samples were measured at a gate bias of $V_g = -8$ V. The results, shown in Fig. 6.9, indicate that the modified HEMTs exhibit slightly higher breakdown voltages compared to thick C-GaN HEMTs. This improvement is directly linked to the reduction in electric field concentration, resulting in an average enhancement of approximately 6% in V_{br}. Whereas further thinning of the C-GaN buffer could potentially yield even greater breakdown voltage improvements, it is important to recognize the trade-off between RF performance that may arise in such designs, as will be discussed in the next



(a) (b)

Figure 6.10: Large signal performance (P_{out}, G_T, and PAE) comparison of (a) reference and (b) modified HEMTs

section[101].

The large-signal measurements are carried out to investigate the trade-offs between device reliability and RF output power performance. As expected, thinning of the C-GaN layer introduces certain limitations, since it places acceptor type trap states closer to the two-dimensional electron gas (2-DEG) channel and simultaneously increases the channel resistance [102]. Consequently, a reduction in output power (P_{out}) is anticipated in thin C-GaN HEMTs, primarily due to the combined effects of lower drain saturation current (I_{dss}) and a less favorable dynamic response. The experimental results for transducer gain (G_T), output power (P_{out}), and power-added efficiency (PAE) are summarized in Fig. 6.10(a & b). All measurements were conducted at an RF frequency of 3 GHz with a quiescent drain bias of 45 V. The results indicate that the gain exhibits a slight improvement, increasing from 20.8 dB in the thick C-GaN HEMTs to 21.3 dB in the thin C-GaN HEMTs. In contrast, P_{out} shows a degradation of approximately 7.5%, decreasing from 8.45 W/mm in the thick C-GaN devices to 7.8 W/mm in the thin C-GaN devices. For a more complete picture of the RF performance, the PAE is also presented in the same graph. A minor reduction is observed, with PAE decreasing from 67% in the thick C-GaN HEMTs to 65% in the thin C-GaN HEMTs.

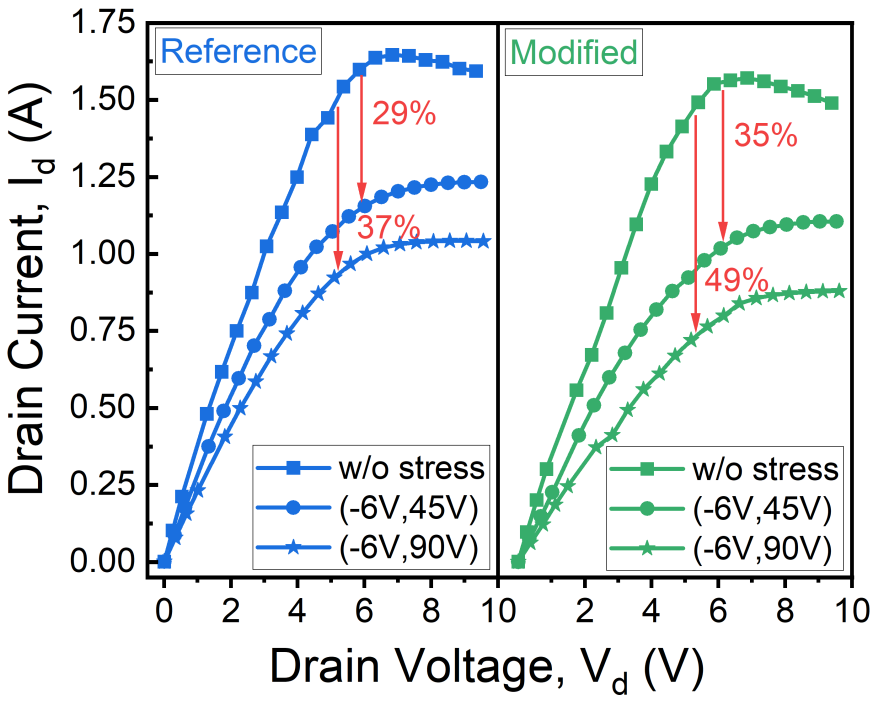


Figure 6.11: Pulsed I_d-V_d test results to show current collapse due to bulk trapping in reference and modified HEMTs at two different stress levels

The reduction in P_{out} observed in thin C-GaN HEMTs can be attributed to two primary factors; the increased channel resistance and the enhanced bulk trapping that occurs under deep off-state RF swings. To further analyze and confirm the trapping behavior, pulsed I_d–V_d measurements were performed on both the thick and thin C-GaN devices. The results are presented in Fig. 6.11. During these measurements, two different drain stress biases were applied while the gate bias was fixed at -6 V. Specifically, the devices were stressed at V_{dq} and at $2V_{dq}$, and the resulting collapsed I_d–V_d curves were compared against the unstressed case (w/o stress), corresponding to a gate bias of $V_g = 0$ V. For the thick C-GaN HEMTs, the measurements reveal a current collapse of 29% and 37% under stress conditions of (V_g, V_d)=(-6 V, 45 V) and (-6 V, 90 V), respectively. By contrast, the thin C-GaN HEMTs exhibit a more pronounced collapse, with reductions of 35% and 49% observed under the same bias conditions. This higher degree of current collapse in the thin C-GaN HEMTs arises from higher Carbon concentration in the vicinity of 2DEG channel. These Carbon impurities act as acceptor trap centers that leads to current collapse during transistor operation. Because

these traps are located closer to the channel, they are more readily activated and can capture carriers during off-state RF swings, causing DC-RF dispersion and slightly reducing the RF output power. In the meantime, these carbon centers significantly improve reliability of the HEMT device. In the proposed design, the buffer engineering is done in a way that a fair trade-off between RF performance and HTRB reliability is accomplished.

6.8 Conclusion

This study analyzes excessively increased gate leakage current in AlGaN/GaN HEMTs under HTRB test conditions, investigates the root causes of the gate degradation and proposes a buffer engineering method to improve the reliability of the device. TEM imaging and EDX mapping are performed to make structural analysis of the gate region. It is found that impact ionization and thin oxide layer below the gate metal are the driving forces of the fast degradation. A new epitaxial design with thinner C-GaN layer is proposed to alleviate impact ionization by decreasing electric field peaks at gate head and foot regions. SIMS analysis is used to show the carbon concentration modification in buffer with the new design. After 1000 hours of HTRB test, 90% lower average gate leakage currents are recorded with the modified HEMTs. Also, breakdown, RF parameters and current collapse characteristics are measured and compared to show the trade-offs.

Chapter 7

Breakdown Voltage and Off-state Reliability Improvement using $Al_xGa_{1-x}N$ Back-barrier Layer

This chapter investigates how an AlGaN back barrier can improve the breakdown voltage and time-to-failure (TTF) of AlGaN/GaN high electron mobility transistors (HEMTs). In addition to conventional AlGaN/GaN HEMTs, we designed and fabricated AlGaN/GaN/$Al_xGa_{1-x}N$ back-barrier HEMTs by inserting a thin AlGaN layer (i.e., 100 nm) underneath the channel GaN (c-GaN) region. Time-dependent breakdown measurements under high-temperature reverse-bias stress, DC, RF, transient measurements and TCAD simulations are carried out to analyze the differences and explain the findings. Results show that breakdown voltage, off-state lifetime and transient characteristics of the device are significantly improved in trade-off DC and RF parameters slightly.

7.1 Introduction

Fe-doped GaN buffers are widely used to obtain semi-insulating GaN and to increase off-state breakdown voltage in microwave and power HEMTs [103, 104]. Iron acceptor states compensate residual donors in the buffer, suppressing vertical leakage and therefore improving breakdown. However, the continuous push towards higher supply voltages and higher power density requires further enhancement of breakdown capability. Alongside field-plate engineering [105] and hybrid-Schottky drains [106], the introduction of a back barrier has emerged as an effective method to boost breakdown voltage in AlGaN/GaN HEMTs [107].

An AlGaN layer placed beneath the channel acts as an electrostatic barrier that confines the two-dimensional electron gas (2DEG) and suppresses sub-threshold drain–source leakage [108, 109, 110]. Comparative band-diagram analyses show that in a conventional AlGaN/GaN HEMT the Fermi level can approach the conduction band in the GaN buffer, whereas in an AlGaN/GaN/AlGaN back-barrier HEMT the Fermi level lies much closer to the valence band within the AlGaN back-barrier region. This lifts the conduction band in the buffer and produces a higher potential barrier for the 2DEG, improving electron confinement and breakdown behavior.

In earlier work we demonstrated high-quality semi-insulating GaN layers on SiC [116, 117]. Devices from that technology achieved breakdown voltages of about 80 V, although reliability was not the focus of those publications. In this chapter we extend that platform by integrating a thin $Al_xGa_{1-x}N$ back barrier below the channel. The resulting AlGaN/GaN/AlGaN HEMTs outperform conventional AlGaN/GaN HEMTs in both breakdown voltage and time-dependent reliability.

Table 7.1 summarizes representative literature on back-barrier HEMTs. The table lists whether the study is experimental or simulation based, the channel thickness t_C, back-barrier thickness t_{BB}, Al mole fraction x, drain–source distance L_{ds}, and breakdown voltages with and without a back barrier. Many

Ref.	**Work Type**	t_C **(nm)**	(t_{BB} **(nm),** x**%)**	L_{ds} **(nm)**	V_{br} **(no BB) (V)**	V_{br} **(BB) (V)**	**TTF Improvement (%)**
[107]	Fab	400	(100, graded (max 7%))	5500	141	> 200	Not reported
[111]	Fab	100	(1000, 4%)	4000	78	> 100	Not reported
[112]	Sim	3	(800, –)	3750	298	342	Not reported
[113]	Sim	20	(1000, 4%)	1100	45	75	Not reported
[114]	Sim	22	(8, 12%)	–	139	154	Not reported
[115]	Fab	50	(250, 5–90%)	3000	53	95	Not reported
This work	**Fab**	**190**	**(100, 7%)**	**3000**	**80**	**105**	> 100

Table 7.1: Reported AlGaN/GaN HEMTs with AlGaN back barriers and their breakdown improvement as a function of channel thickness t_C, drain–source spacing L_{ds}, AlGaN back-barrier thickness t_{BB}, and Al content x.

previously reported devices adopt relatively thick back barriers with high Al content. While this strongly increases breakdown, it can degrade thermal performance [109], increase dynamic R_{on} [118], and introduce additional defects due to the double heterostructure. Other studies rely on very thin channels to boost breakdown [112, 115]; however, ultra-thin channels suffer from reduced mobility and higher R_{on}, limiting I_{dss} [119], and in a back-barrier configuration the 2DEG density may also drop due to the opposing polarization field [115].

In contrast, our approach uses a relatively thin (100 nm) $Al_{0.07}Ga_{0.93}N$ back barrier combined with a moderately thick 190 nm GaN channel and a compact 3 μm drain–source spacing. With this design we obtain roughly 32 % higher breakdown voltage and more than 100 % improvement in TTF compared with the reference AlGaN/GaN HEMT. Thus, the device keeps a conventional channel thickness while still benefiting from back-barrier confinement.

Time-dependent breakdown was investigated by high-temperature reverse-bias (HTRB) I–V/t testing at 150°C. The back-barrier devices withstand off-state

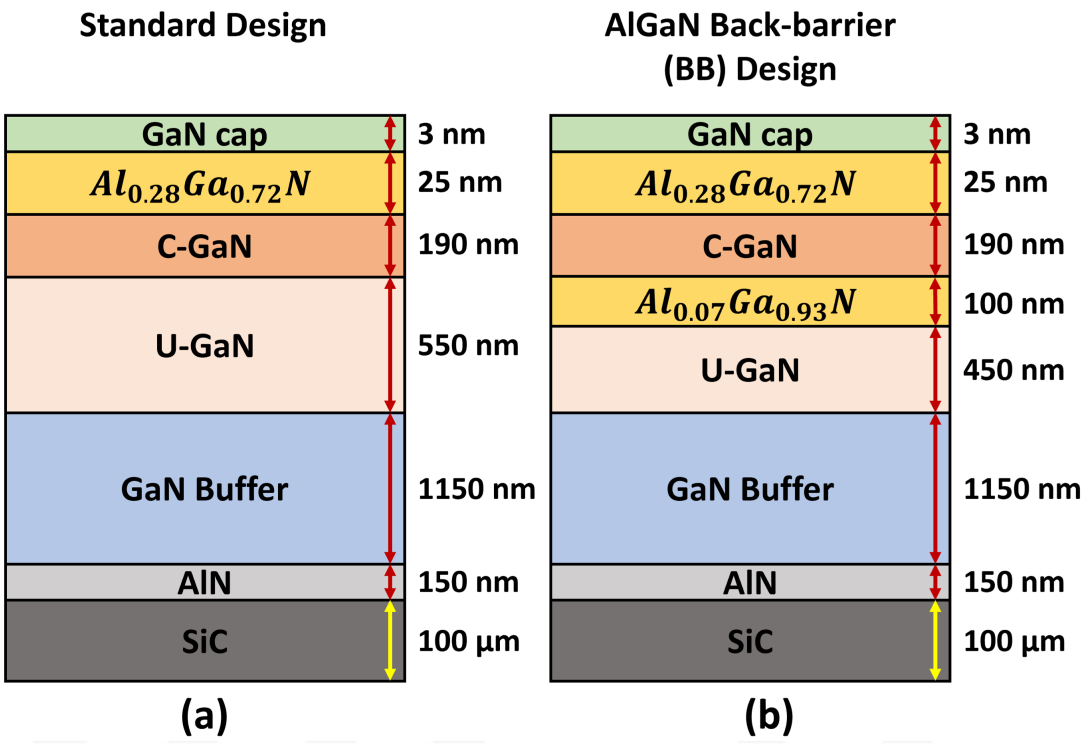


Figure 7.1: Epitaxial schematic of (a) the reference AlGaN/GaN HEMT and (b) the AlGaN/GaN/AlGaN back-barrier HEMT.

stress significantly longer than the reference devices, and the measured TTF follows an exponential dependence on drain–source voltage. Dynamic behavior was further examined using drain-current transient (DCT) measurements, which show strongly reduced current collapse for the back-barrier HEMTs. RF gain, output power and power-added efficiency remain essentially unchanged, confirming that reliability improvements are not obtained at the expense of RF performance.

The trends in breakdown, TTF, dispersion and leakage are also supported by Silvaco ATLAS TCAD simulations. Simulated electric-field distributions confirm that in both structures breakdown is initiated when the peak field in the top AlGaN barrier reaches its critical value, but the back-barrier device experiences a lower peak field at the gate edge and field-plate edge as well as reduced off-state gate and drain leakage.

Overall, the results in this chapter demonstrate that inserting a thin, lightly

Al-doped back barrier provides a compact and effective route to improve breakdown and reliability of GaN HEMTs, while keeping RF performance essentially unchanged.

7.2 Experimental details

All HEMTs were grown on c-plane SiC substrates by metal–organic chemical vapor deposition (MOCVD). The epitaxial stacks of the reference and back-barrier devices are sketched in Figure 7.1. A 120 nm AlN nucleation layer was first deposited on SiC, followed by an 1150 nm Fe-doped GaN buffer to obtain a semi-insulating template. On top of this, unintentionally doped GaN (u-GaN) was grown. For the standard structure, the u-GaN thickness is 550 nm. For the back-barrier structure, the upper 100 nm of this u-GaN was replaced with an $Al_{0.07}Ga_{0.93}N$ layer. Above this, a 190 nm channel GaN layer was grown, followed by a 25 nm $Al_{0.28}Ga_{0.72}N$ barrier and a 3 nm GaN cap. The thin cap helps reduce off-state gate and drain leakage currents [55, 120]. Finally, a three-layer SiN stack was deposited for surface passivation and to define the T-gate and field plate.

Ohmic contacts were formed from a Ti/Al/Ni/Au (15/90/50/50 nm) metal stack, annealed at 875°C for 30 s in N_2. Transfer-length-method (TLM) patterns yielded contact resistances of about 0.5 $\Omega \cdot$ mm for both epitaxies. Device isolation was achieved by reactive-ion-etched mesas. Schottky gates used a Ni/Au (100/400 nm) stack.

Figure 7.2 shows a schematic and a FIB–SEM cross section of the back-barrier device. Apart from the additional back-barrier layer, the geometries of the two HEMT types are identical. The gate length L_g, gate width W_g, gate–source spacing L_{gs}, gate–drain spacing L_{gd} and drain-source spacing L_{ds} are 0.25 μm, 125 μm, 1 μm, 1.75 μm and 3 μm, respectively. A 0.2 μm source-connected field plate extends over the drain access region.

The GaN buffer is Fe-doped to make it semi-insulating. The Fe concentration

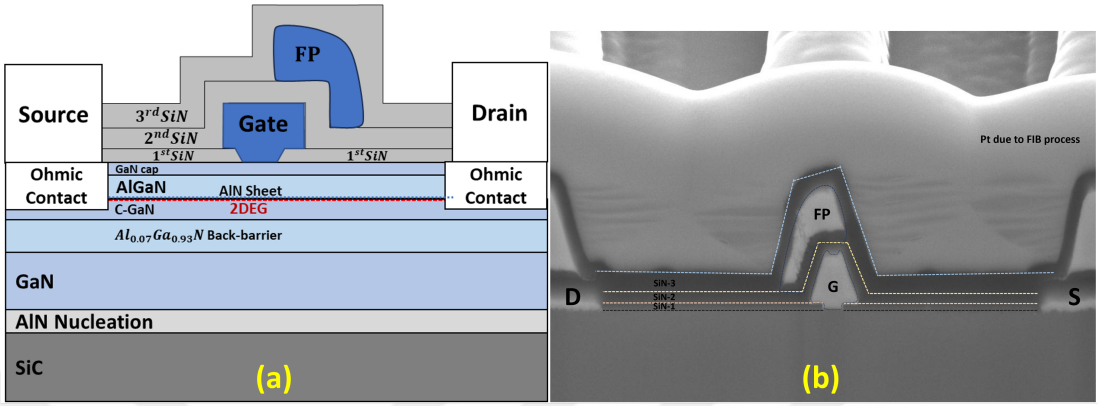


Figure 7.2: (a) Schematic cross-section and (b) FIB–SEM image of the fabricated back-barrier HEMT.

falls from about $1 \times 10^{18}\,\mathrm{cm}^{-3}$ in the deeper buffer to $\sim 1 \times 10^{16}\,\mathrm{cm}^{-3}$ near the channel. Carbon is present at a level of $\sim 1 \times 10^{16}\,\mathrm{cm}^{-3}$ throughout the buffer and channel. For the back-barrier devices the same profile is used, except in the AlGaN back-barrier region where SIMS measurements show a carbon concentration of about $1 \times 10^{18}\,\mathrm{cm}^{-3}$. This produces a pronounced carbon peak in the overall trap distribution.

7.3 Measured results and discussion

Hall measurements at 300 K give a 2DEG sheet density of $1.2 \times 10^{13}\,\mathrm{cm}^{-2}$. The low-field mobility is $2032\,\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ for the reference HEMT and $1956\,\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ for the back-barrier device, consistent with stronger confinement and slightly enhanced scattering in the latter.

The difference in confinement is illustrated by the simulated band diagrams in Figure 7.3, which overlay the conduction bands of the two structures at zero bias. In the back-barrier device the conduction band in the buffer is raised, limiting electron spillover from the channel. The Fermi level in the back-barrier region is pinned closer to the valence band due to the high concentration of carbon acceptors.

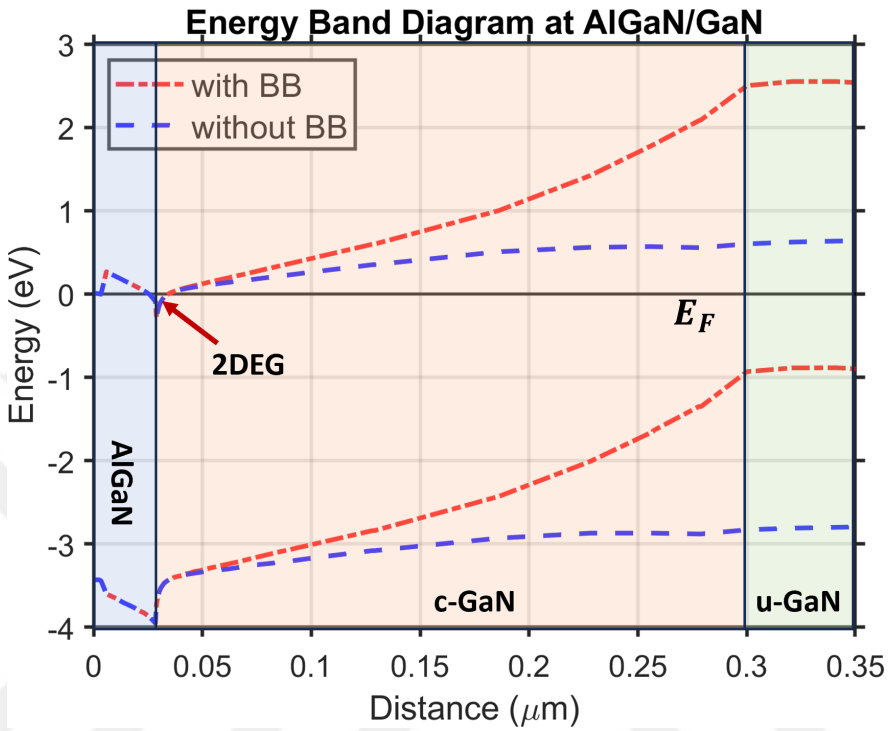


Figure 7.3: Simulated energy-band diagrams of HEMTs with and without an AlGaN back barrier at zero bias.

7.3.1 DC characteristics

The DC characteristics are summarized in Figure 7.4. Figure 7.4(a) shows the I_d–V_d curves at $V_g = 1\,\mathrm{V}$. The maximum drain current decreases from 1.116 A/mm for the reference device to 1.025 A/mm for the back-barrier device (about 8 % reduction). This is mainly attributed to a lower effective saturation velocity and slightly reduced mobility due to stronger confinement.

Figure 7.4(b) presents the transfer characteristics at $V_d = 10\,\mathrm{V}$. The threshold voltage shifts from $-3.52\,\mathrm{V}$ to $-3.42\,\mathrm{V}$ when the back barrier is added. The more positive threshold is consistent with the higher potential barrier between channel and buffer. The corresponding transconductance curves are shown in Figure 7.4(c). The peak g_m is 323 mS for the reference HEMT and 307 mS for the back-barrier device, again reflecting the modest reduction in carrier velocity and the slightly higher on-resistance.

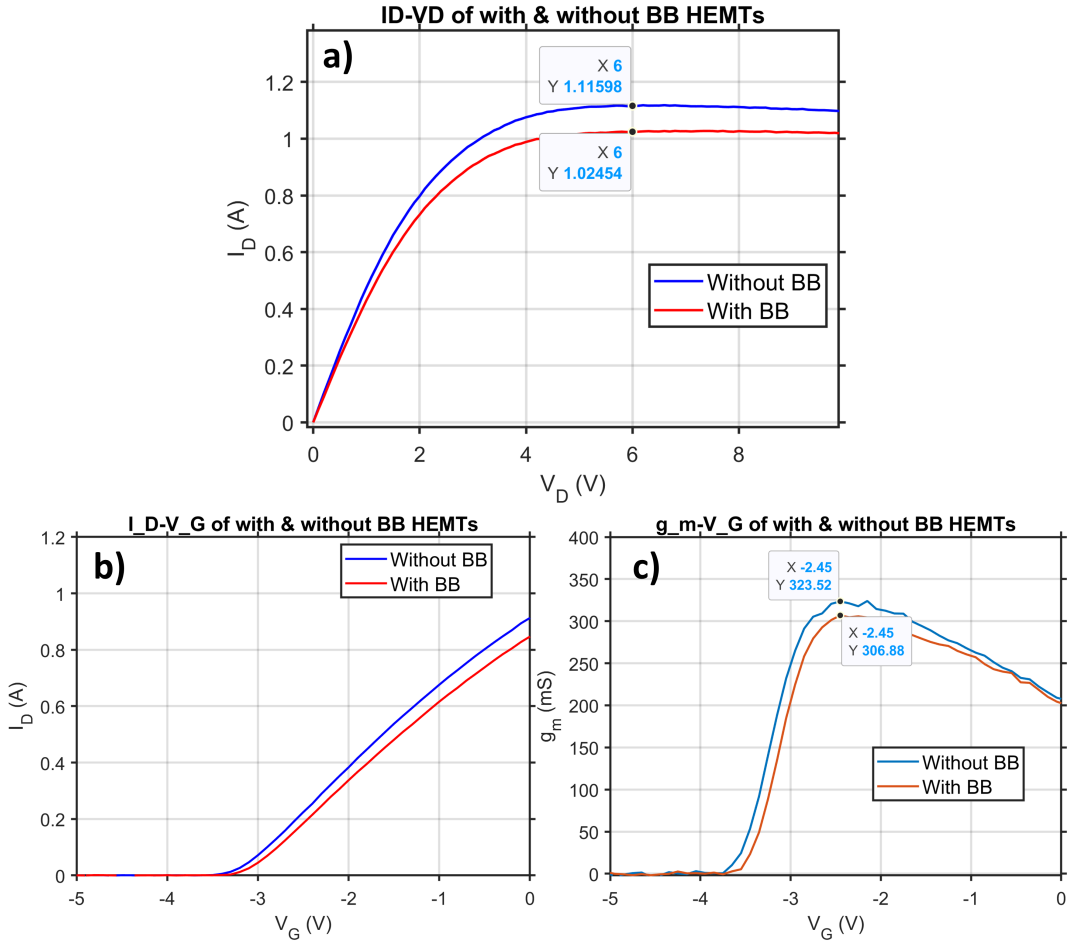


Figure 7.4: DC characteristics of the reference and back-barrier HEMTs: (a) output I_d–V_d curves at $V_g = 1\,\mathrm{V}$, (b) transfer characteristics at $V_d = 10\,\mathrm{V}$, and (c) transconductance g_m.

7.3.2 Breakdown characteristics

Figure 7.5 compares the off-state breakdown behavior of the two devices, with $V_g = -8\,\mathrm{V}$ and V_d swept up to breakdown. The breakdown voltage increases from about 80 V for the conventional HEMT to about 105 V for the back-barrier HEMT, corresponding to a 32 % improvement. At low V_d the drain leakage is similar in both devices, but at higher voltages the back-barrier device shows roughly an order of magnitude lower leakage. The semi-log plot in Figure 7.5(b) uses 1 mA/mm as the breakdown criterion.

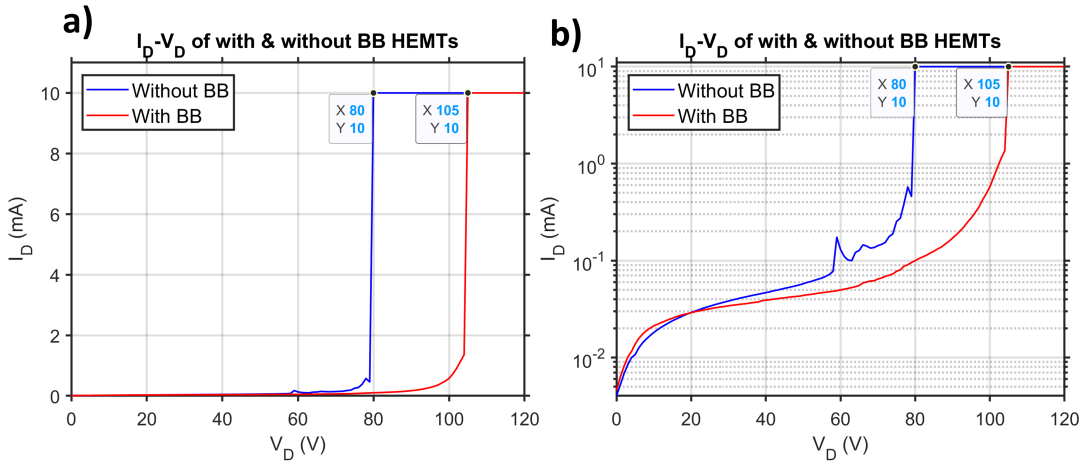


Figure 7.5: Off-state breakdown characteristics of HEMTs with and without back barrier: (a) linear scale and (b) logarithmic scale.

The reduction of leakage and increase in breakdown are consistent with the modified electric-field distribution introduced by the back barrier and with the higher carbon concentration in that region, which raises the effective barrier between channel and buffer. Many earlier reports on back-barrier HEMTs [112, 121] discuss breakdown improvements but do not explicitly link them to the trap distribution; our measurements and simulations indicate that carbon-rich AlGaN is a key contributor.

7.3.3 Time-to-failure and time-dependent breakdown

Because of their higher breakdown voltage, back-barrier HEMTs are expected to survive longer under constant off-state high-field stress [122]. To quantify this, we performed HTRB I–V/t tests at 150°C.

First, both device types were stressed at $(V_{gs}, V_{ds}) = (-8\,\mathrm{V}, 75\,\mathrm{V})$, slightly below the breakdown of the reference HEMT. The resulting drain-current transients are shown in Figure 7.6. The reference device fails after roughly 20 h, whereas the back-barrier device survives for about 42.6 h, i.e., more than twice as long. The gate-current evolution plotted in the same figure highlights the different

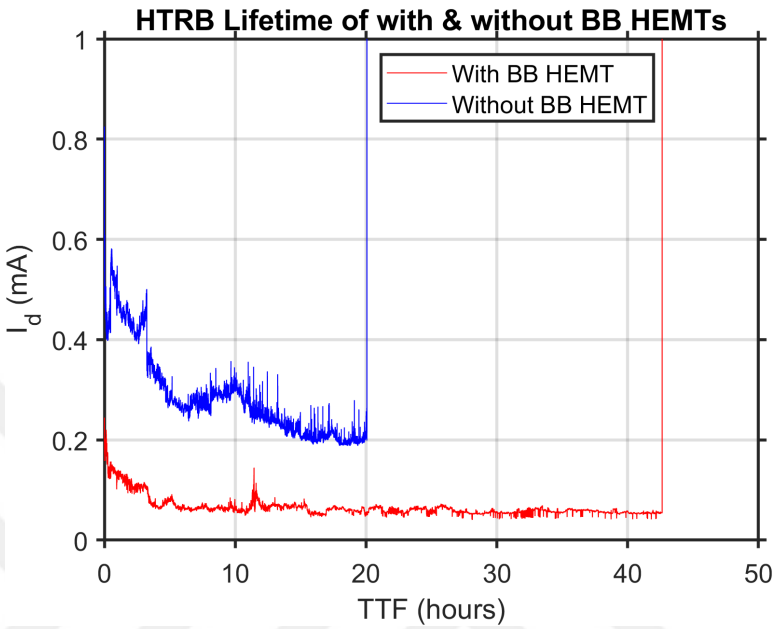


Figure 7.6: HTRB test at $(V_{gs}, V_{ds}) = (-8\,\mathrm{V}, 75\,\mathrm{V})$ and 150°C for HEMTs with and without back barrier.

breakdown dynamics.

To extract the voltage dependence of TTF for the back-barrier HEMTs, we repeated the test at $V_{ds} = 75$, 85 and 95 V with $V_{gs} = -8\,\mathrm{V}$ and $T = 150°\mathrm{C}$. Figure 7.7(a) summarizes the corresponding drain-current versus time traces. At 95 V the device fails in less than an hour, at 85 V it survives for about 10 h, and at 75 V the TTF exceeds 40 h.

Figure 7.7(b) shows the TTF as a function of V_{ds} together with an exponential fit, which is used to extrapolate TTF to lower voltages. For example, the fit predicts a lifetime of approximately 5.3×10^5 h (about 60 years) at $V_{ds} = 28\,\mathrm{V}$. This simple relation gives a convenient estimate of the safe operating region for off-state stress.

Long-term HTRB tests of standard and back-barrier HEMTs with $L_{\mathrm{ds}} = 3.5\ \mu\mathrm{m}$ are carried out using the Accel-RF DC AARTS system. The devices are stressed at $(V_{\mathrm{gs}}, V_{\mathrm{ds}}) = (-8\ \mathrm{V}, 84\ \mathrm{V})$ with a base temperature of $T = 150°\mathrm{C}$. The gate leakage currents of the tested devices at 150°C are shown in Figure 7.8.

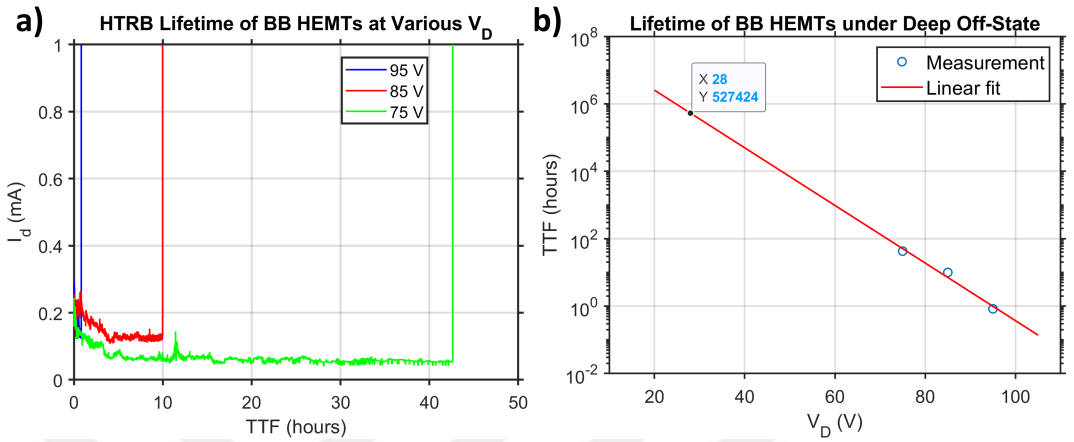


Figure 7.7: HTRB results for back-barrier HEMTs: (a) drain current versus time at different V_{ds} and (b) extracted TTF with exponential fit versus V_{ds}.

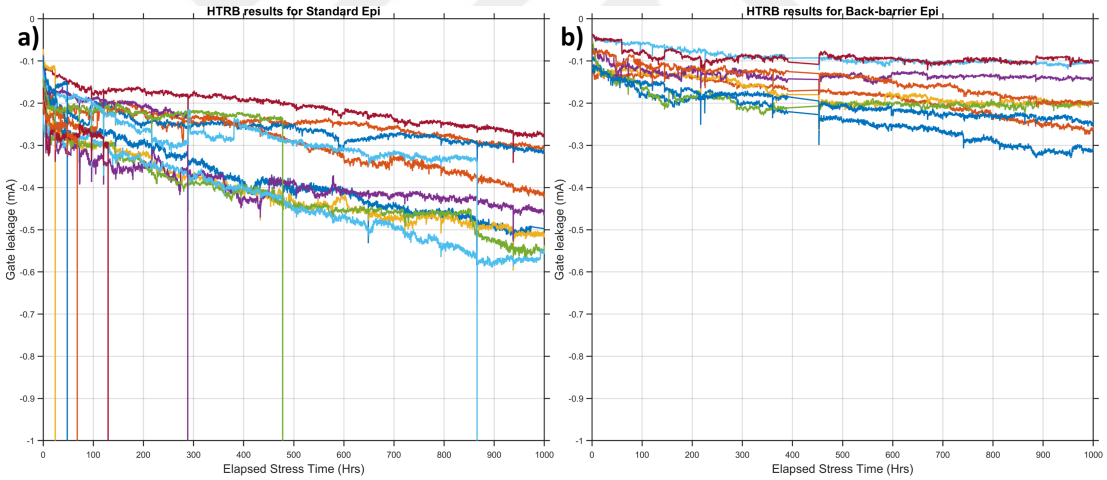


Figure 7.8: Long-term HTRB results for (a) standard and (b) back-barrier HEMTs with $L_{ds} = 3.5\mu m$.

The sharp drops in Figure 7.8(a) correspond to catastrophic breakdown events. In total, 7 out of 16 HEMTs with the standard epitaxial design fail during HTRB, whereas all back-barrier HEMTs successfully complete the test. It is also noted that the back-barrier HEMTs exhibit consistently lower gate leakage currents. These results confirm the improved breakdown behavior and extended TTF of the back-barrier devices under long-term HTRB stress.

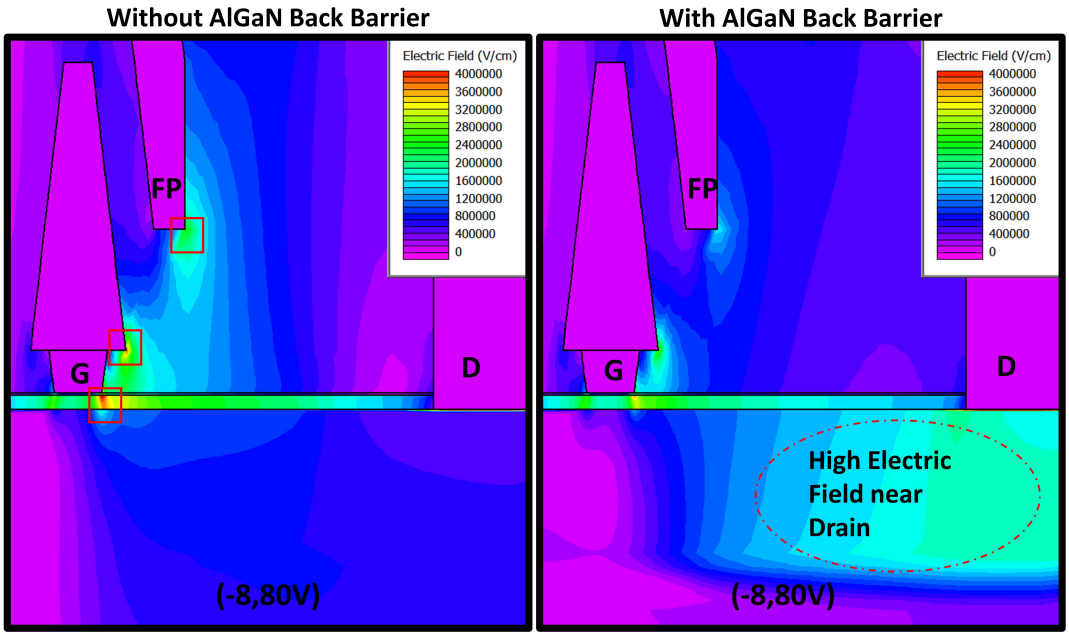


Figure 7.9: Simulated electric-field distribution in the top AlGaN barrier for HEMTs with and without back barrier at deep off-state.

7.3.4 Electric-field distribution and reliability

To clarify the physical origin of the improved breakdown and TTF, 2-D TCAD simulations were performed. Figure 7.9 compares the simulated electric-field maps in the top AlGaN barrier for both devices at $(V_{gs}, V_{ds}) = (-8\,\mathrm{V}, 80\,\mathrm{V})$. In both structures the dominant peaks are located at the drain-side gate foot edge, at the gate-head edge, and at the field-plate edge. However, the peak field in the reference HEMT reaches about 3.7 MV/cm, roughly 0.8 MV/cm higher than in the back-barrier HEMT. The field in the back-barrier device is also more spread towards the drain, leading to a more uniform distribution.

The reduced peak field delays avalanche breakdown driven by impact ionization. Simulated impact-generation and hole-concentration profiles at $(V_{gs}, V_{ds}) = (-8\,\mathrm{V}, 80\,\mathrm{V})$ are shown in Figure 7.10. In the reference device, impact generation is strongly localized near the drain-side gate edge, leading to an intense punch-through path. In the back-barrier device the generation rate is lower and more distributed in the drain access region. The lower peak field and reduced

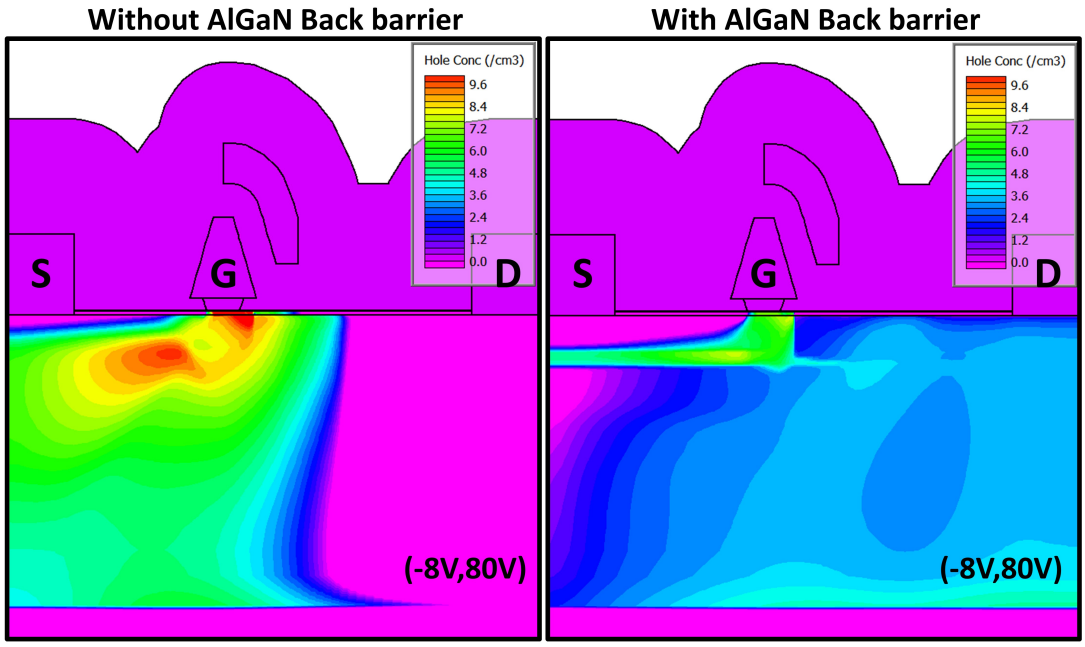


Figure 7.10: TCAD simulations of impact-ionization-induced hole concentration for HEMTs with and without back barrier at high off-state bias.

punch-through explain the higher breakdown voltage and longer TTF observed experimentally.

7.3.5 RF performance

Large-signal RF measurements show that the back-barrier has only a minor effect on RF performance. Figure 7.11 plots gain, output power and PAE versus input power at 10 GHz. The maximum input power is about 26.3 dBm. At this point the reference HEMT exhibits 10.7 dB gain, 37.8 dBm output power and 59.7 % PAE, whereas the back-barrier HEMT shows 10.6 dB, 37.5 dBm and 57.4 %, respectively. The slight reduction in PAE is consistent with the modest drop in I_{dss}, but the differences are small.

Small-signal parameters are summarized in Table 7.2. The maximum available gain (MAG) at 10 GHz is slightly higher for the back-barrier device. The

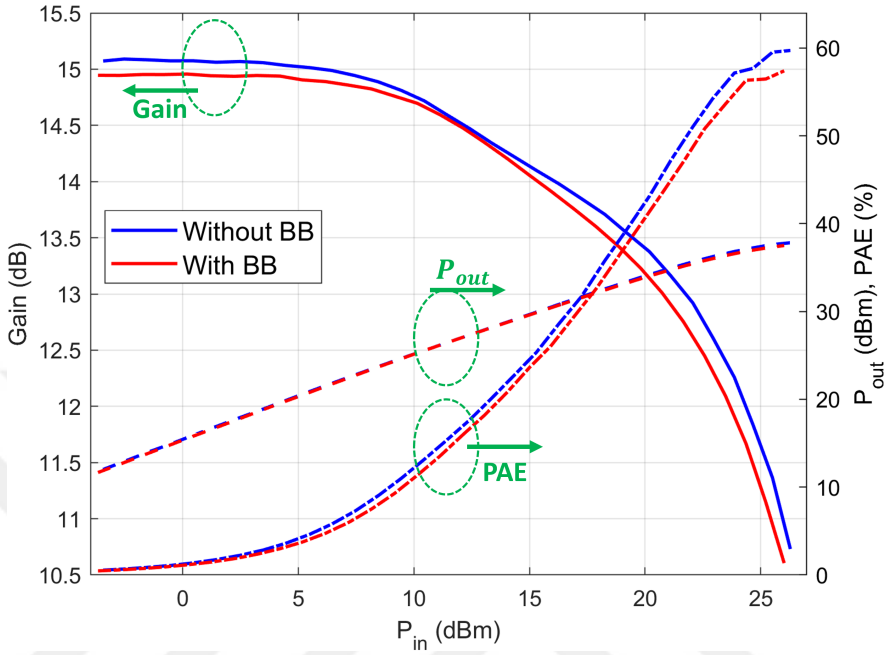


Figure 7.11: Large-signal RF characteristics of HEMTs with and without back barrier: gain, output power P_{out}, and PAE versus input power.

current-gain cutoff frequency f_t remains essentially unchanged, while the power-gain cutoff frequency $f_{\max}$ increases modestly from 68.0 to 71.1 GHz. This small improvement is attributed to reduced short-channel effects and better electrostatic control.

HEMT	**MAG (dB) at 10 GHz**	f_t **(GHz)**	$f_{\max}$ **(GHz)**
Without BB	16.49	39.51	68.03
With BB	16.95	38.42	71.11

Table 7.2: Maximum available gain and cutoff frequencies for HEMTs with and without an AlGaN back barrier.

7.3.6 Transient analysis

The influence of the back barrier on trapping and current collapse was studied using drain-current transient (DCT) measurements. After biasing the device at a quiescent point, a high-field stress pulse is applied to fill traps, and the subsequent

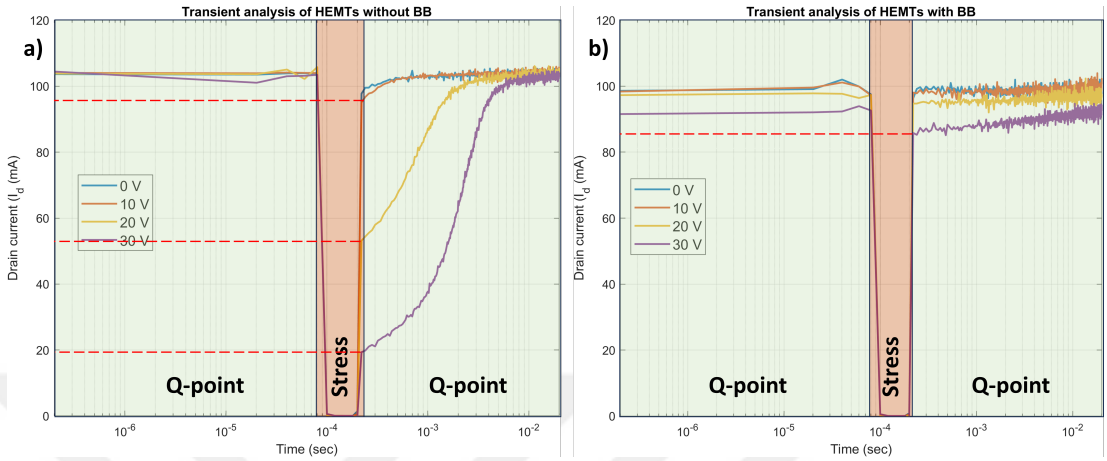


Figure 7.12: Drain-current transient measurements for HEMTs with and without back barrier under off-state stress pulses.

current recovery is monitored once the quiescent bias is restored.

To probe buffer traps, the quiescent bias was set to $(V_{gq}, V_{dq}) = (-3.42\,\mathrm{V}, 10\,\mathrm{V})$ for the reference device and adjusted to $-3.08\,\mathrm{V}$ for the back-barrier device so that both conduct 100 mA at quiescent conditions. Stress pulses with $(V_{gp}, V_{dp}) = (-6\,\mathrm{V}, 0\,\mathrm{V})$ to $(-6\,\mathrm{V}, 30\,\mathrm{V})$ in 10 V steps were then applied. The measured transients are shown in Figure 7.12.

For the reference HEMT the current collapse strongly increases with stress voltage and exceeds 81 % at $V_{dp} = 30\,\mathrm{V}$, accompanied by a clear threshold shift. In contrast, the back-barrier HEMT exhibits less than 5 % collapse under the same stress with similar recovery times and no noticeable threshold shift. This indicates that the back-barrier structure strongly suppresses buffer-related trapping.

TCAD simulations were used to interpret this improvement. Figure 7.13 shows the simulated energy-band diagram of the reference device from c-GaN into u-GaN at a representative quiescent bias. The energy levels of Fe and C trap centers are indicated. In this case carbon traps are largely pre-ionized, and trapping is dominated by Fe centers. For the back-barrier HEMT (Figure 7.14), the high carbon concentration in the AlGaN layer pins the Fermi level closer to the carbon trap level, effectively confining the channel and limiting the number of electrons that can reach Fe traps in the GaN buffer. As a result, the amount of charge that

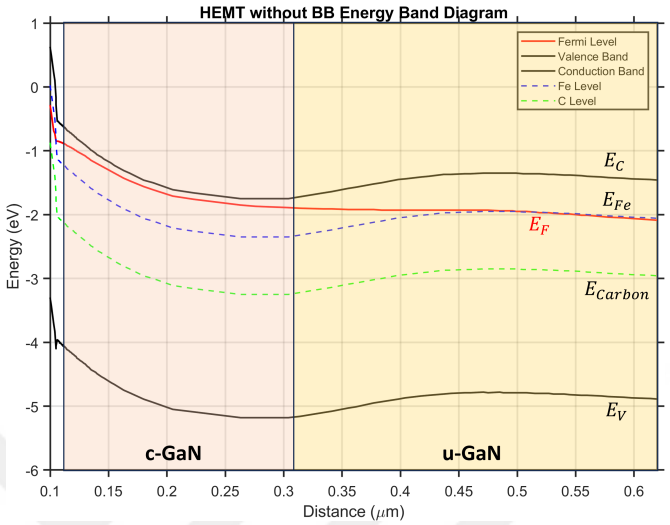


Figure 7.13: Simulated energy-band diagram of the reference AlGaN/GaN HEMT from c-GaN to u-GaN, indicating Fe and C trap levels.

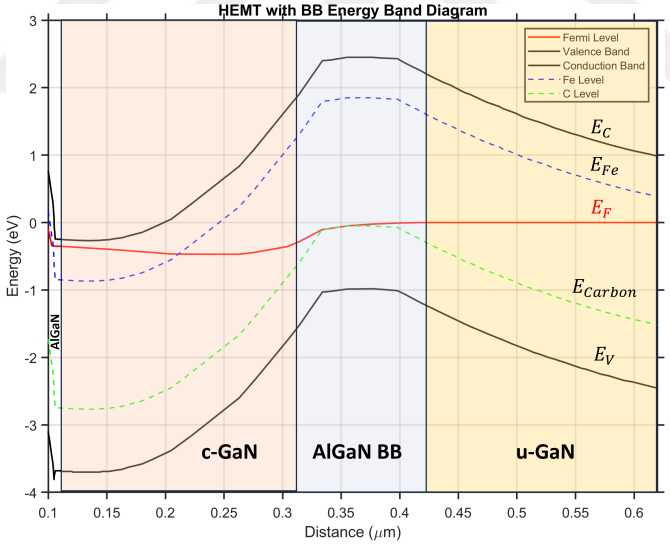


Figure 7.14: Simulated energy-band diagram of the AlGaN/GaN/AlGaN back-barrier HEMT, showing stronger channel confinement due to carbon-rich AlGaN.

can be stored in deep traps is reduced, leading to much smaller current dispersion.

7.4 Conclusion

The impact of inserting a thin AlGaN back barrier in an AlGaN/GaN HEMT has been systematically examined through experiment and simulation. A 100 nm $Al_{0.07}Ga_{0.93}N$ layer beneath a 190 nm GaN channel increases the off-state breakdown voltage from 80 V to 105 V and more than doubles the time-to-failure under high-temperature reverse-bias stress. These gains are traced to a reduction and redistribution of the peak electric field at the gate and field-plate edges, which delays avalanche breakdown and punch-through.

The back-barrier devices show only a modest decrease in I_{dss} and g_m, while large-signal and small-signal RF figures of merit remain essentially unchanged. Drain-current transient measurements reveal a dramatic reduction of current collapse from about 81 % to below 5 %, consistent with simulations that highlight the role of carbon-rich AlGaN in confining the channel and mitigating buffer trapping.

Taken together, these results demonstrate that a carefully engineered AlGaN/GaN/AlGaN back-barrier architecture can deliver higher breakdown voltage, longer off-state lifetime and improved dynamic behavior without compromising RF performance. This makes such devices strong candidates for future high-power, high-voltage GaN RF amplifiers operating under harsh environmental and electrical conditions.

Chapter 8

Buffer-free, Ultra-thin Barrier GaN-on-SiC HEMTs with a Highly Doped GaN Layer for Next Generation Power Devices

This chapter investigates a novel buffer-free ultra-thin buffer (UTB) AlGaN/GaN HEMT technology that replaces the conventional Fe-doped GaN buffer with a 0.2 μm-thick Fe-free GaN stack including a highly doped GaN (hd-GaN) layer. The proposed devices are evaluated against standard (Std) AlGaN/GaN HEMTs in terms of DC characteristics, leakage and breakdown behavior, RF performance, and off-state reliability. The experimental results are supported and interpreted using 2-D TCAD simulations.

8.1 Introduction

State-of-the-art GaN-on-SiC power HEMTs typically employ thick Fe-doped GaN buffers to obtain semi-insulating behavior and high off-state breakdown voltage. This approach is effective for suppressing vertical leakage, but deep Fe- and C-related centers in the buffer are now recognized as major sources of trapping, current collapse, and dynamic R_{on} degradation, particularly under high-temperature reverse-bias (HTRB) stress [123]. Several reliability studies on Fe-doped AlGaN/GaN HEMTs under HTRB conditions have reported pronounced degradation in leakage and transconductance, even in the absence of catastrophic failure [124]. In parallel, carbon-related studies show that higher C concentration in the buffer improves off-state leakage but strongly enhances buffer trapping and current collapse [125].

These limitations have motivated a shift towards alternative buffer concepts, such as C-doped Fe-free buffers, thin or "buffer-free" heterostructures, and engineered back-barriers that move the high-field region away from trap-rich layers and provide better electrostatic control [126, 127]. Following this direction, the present work explores an ultra-thin, Fe-free GaN buffer concept with a total GaN thickness of only 200 nm, which is much smaller than in our standard technology. We compare these UTB HEMTs with reference Std HEMTs using DC and RF characterization, off-state breakdown measurements, systematic HTRB stress, 2-D electric-field simulations, and TEM cross-sections. The results show a strong increase in breakdown voltage and a marked improvement in HTRB robustness while preserving competitive DC and RF performance. Overall, the data indicate that aggressive buffer thinning combined with an Fe-free design can simultaneously boost breakdown and reliability, provided that the vertical field profile is carefully engineered and verified by simulation and microscopy.

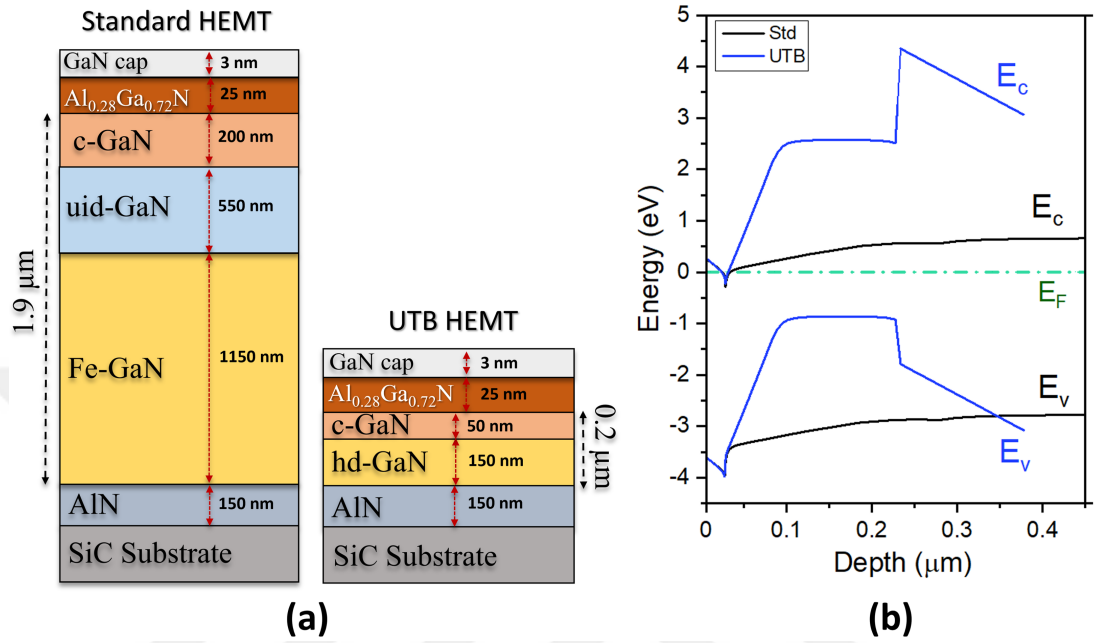


Figure 8.1: (a) Epitaxial schematic of the standard (left) and UTB (right) HEMTs. (b) Simulated conduction band diagram along a vertical cut-line through the two epitaxies.

8.2 Epitaxial Growth and Device Fabrication

The cross-sectional schematics of the AlGaN/GaN epitaxial stacks are shown in Figure 8.1(a). For the standard (Std) structure [Figure 8.1(a), left], the heterostructure was grown on a 3-inch semi-insulating SiC substrate by metal–organic chemical vapor deposition (MOCVD). Growth begins with a 120 nm AlN nucleation layer to accommodate the lattice and thermal mismatch between GaN and SiC. A 1150 nm Fe-doped semi-insulating GaN buffer is then deposited to suppress vertical leakage and provide isolation. Above this buffer, a 550 nm unintentionally doped (uid) GaN spacer is inserted to mitigate Fe memory effects. The electron channel is formed by a 200 nm GaN channel layer (c-GaN), followed by a 25 nm $Al_{0.25}Ga_{0.75}N$ barrier (28% Al) and a 3 nm GaN cap, completing the Std epitaxial stack.

In the UTB AlGaN/GaN design [Figure 8.1(a), right], the thick Fe-doped buffer is removed and replaced by a thin, Fe-free structure. The epitaxy is again

grown on a semi-insulating SiC substrate by MOCVD, but the buffer concept is altered. A three-step transphormic AlN nucleation layer is first grown directly on SiC to relax strain and ensure high crystalline quality in the overlying layers. On top of this, a 150 nm highly doped GaN (hd-GaN) layer is introduced to act as a thin buffer and to confine the vertical field, thereby helping to control short-channel effects and electron spillover. No uid-GaN spacer is used in this Fe-free design. Above hd-GaN, the channel GaN (c-GaN) thickness is reduced to 50 nm, and the same $Al_{0.25}Ga_{0.75}N$ barrier and 3 nm GaN cap as in the Std epitaxy are grown. Keeping the upper layers identical in both structures allows a direct comparison of buffer concepts.

Hall measurements on the Std epitaxy yield a 2DEG sheet density of $1.2 \times 10^{13}\,\mathrm{cm}^{-2}$ with a low-field mobility of about 1900 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. For the UTB HEMTs, the 2DEG density is approximately 25% higher, while the mobility remains close to 1900 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. As a result, the sheet resistance decreases from about 270 $\Omega/\square$ (Std) to a 25% lower value in UTB. The higher 2DEG density in the UTB structure is attributed to the stronger compressive stress in the AlGaN barrier induced by the thinner c-GaN, which increases the polarization charge. The Silvaco ATLAS TCAD simulations used in this work reproduce these trends and help visualize the band structure. Figure 8.1(b) compares the simulated conduction and valence bands and Fermi levels for Std and UTB epitaxies along a vertical cut-line. In the UTB structure, the hd-GaN layer pins the Fermi level close to the carbon acceptor level, the thinner c-GaN and the AlN nucleation layer together act as an effective back-barrier, and the 2DEG is more tightly confined near the AlGaN/GaN interface. These features suppress electron spillover into the substrate and reduce off-state drain-to-source leakage, providing an Fe-free alternative to traditional thick-buffer designs.

The same microfabrication flow is used for both Std and UTB epitaxies. Ohmic contacts are formed by depositing a Ti/Al/Ni/Au (15/90/50/50 nm) metal stack, followed by rapid thermal annealing at 875 °C for 30 s in nitrogen, yielding a contact resistance of approximately 0.4 $\Omega \cdot$ mm as extracted by the transfer length method (TLM). Mesa isolation is defined by reactive ion etching (RIE). A three-layer SiN stack deposited by PECVD is used to passivate the surface, realize a

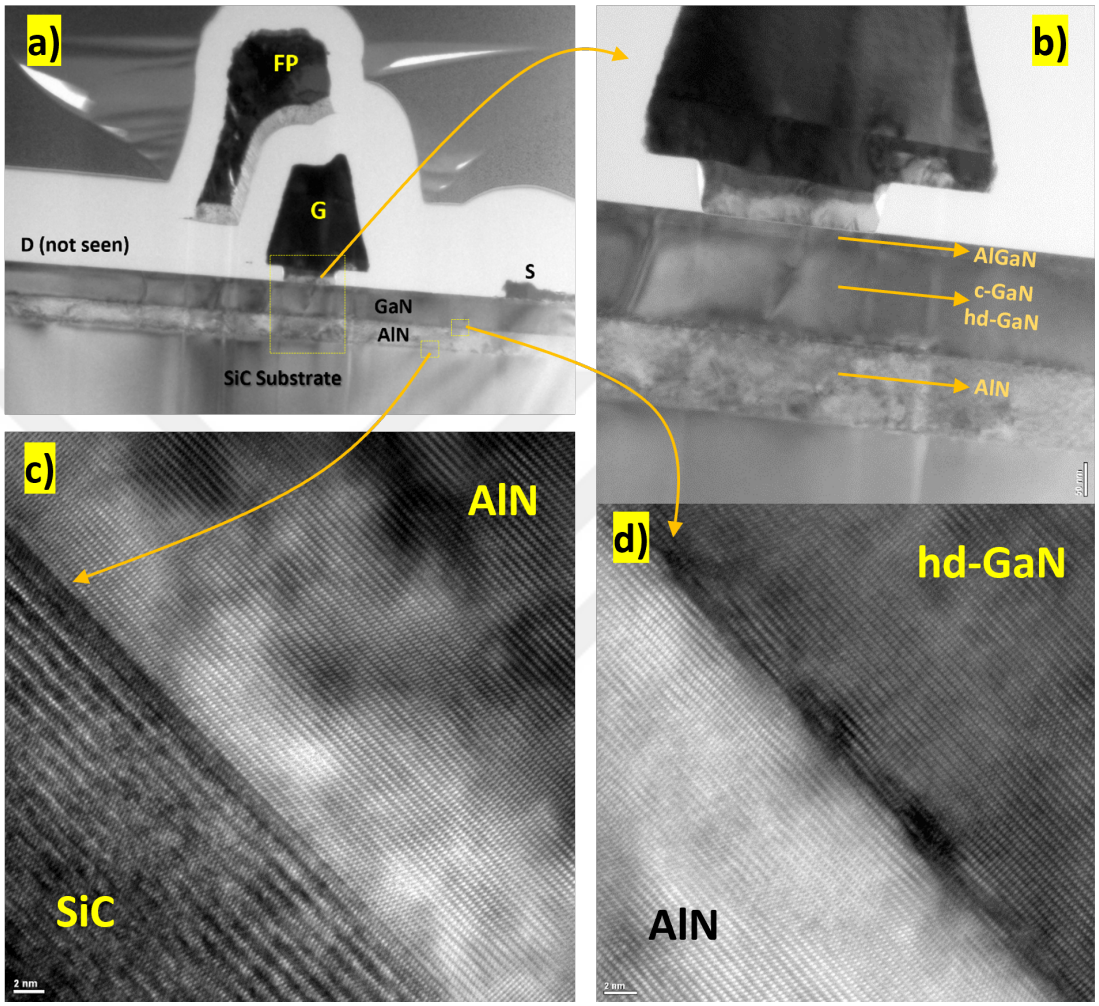


Figure 8.2: TEM images of UTB HEMTs. (a) Overall cross-section showing epitaxial, metal, and dielectric layers. (b) Gate region with ultra-thin GaN channel and Schottky contact. (c) SiC/AlN interface and (d) AlN/GaN interface, demonstrating high crystalline quality.

T-shaped gate, encapsulate the gate metal, and form the source-connected field plate. Schottky gates are patterned by electron-beam lithography and implemented with Ni/Au (50/600 nm). The gate length L_G is 0.25 μm, and the gate width per finger W_G is 125 μm; multi-finger peripheries are used in larger test structures as discussed later. Final interconnect metallization completes the devices.

Representative TEM images of the UTB HEMT are shown in Figure 8.2. The low-magnification cross-section in Figure 8.2(a) reveals the full stack, including

the epitaxial layers, source ohmic contact, gate and field-plate metals, and SiN layers. Figure 8.2(b) shows a magnified view of the gate region, clearly resolving the ultra-thin GaN channel and the Schottky gate contact. Figures 8.2(c) and 8.2(d) focus on the SiC/AlN and AlN/GaN interfaces, respectively; no dislocations were observed in the imaged regions. The thin-layer stack reduces strain and appears to promote good interface quality in the UTB epitaxy.

8.3 HEMT Results

8.3.1 DC Characteristics and Breakdown

The measured DC characteristics of Std and UTB HEMTs are summarized in Figure 8.3. Figure 8.3(a) shows the output I_{D}–V_{D} curves for V_{G} swept from -4 V to 1 V. At $V_{\mathrm{G}} = 1$ V, the UTB HEMTs exhibit about 5% higher saturated drain current $I_{\mathrm{D,ss}}$ than the Std devices, which is consistent with the higher 2DEG density extracted from Hall measurements. The transfer characteristics in Figure 8.3(b) (measured at $V_{\mathrm{D}} = 10$ V) show that this benefit comes with a modest penalty in subthreshold behavior: the Std HEMTs have a slope of roughly 174 mV/dec, whereas the UTB devices show a slope of about 217 mV/dec, reflecting the absence of Fe compensation and the different vertical field profile.

Figure 8.3(c) compares the transconductance g_m versus V_{G}. The peak g_m in the UTB HEMTs is approximately 15% higher than in the Std devices, again in line with the increased 2DEG density and reduced sheet resistance. Off-state breakdown measurements are presented in Figure 8.3(d). In these tests, the gate is biased at -8 V and the drain voltage is swept up to device failure. The UTB devices clearly show a shift of the breakdown range from about 80–90 V (Std) to approximately 150–190 V, indicating a major improvement in breakdown margin.

To obtain statistically meaningful breakdown data, a larger set of multi-finger devices was evaluated. These HEMTs have $L_G = 0.25$ μm, $W_G = 125$ μm per finger, eight gate fingers, a source-connected field plate, and a drain–source

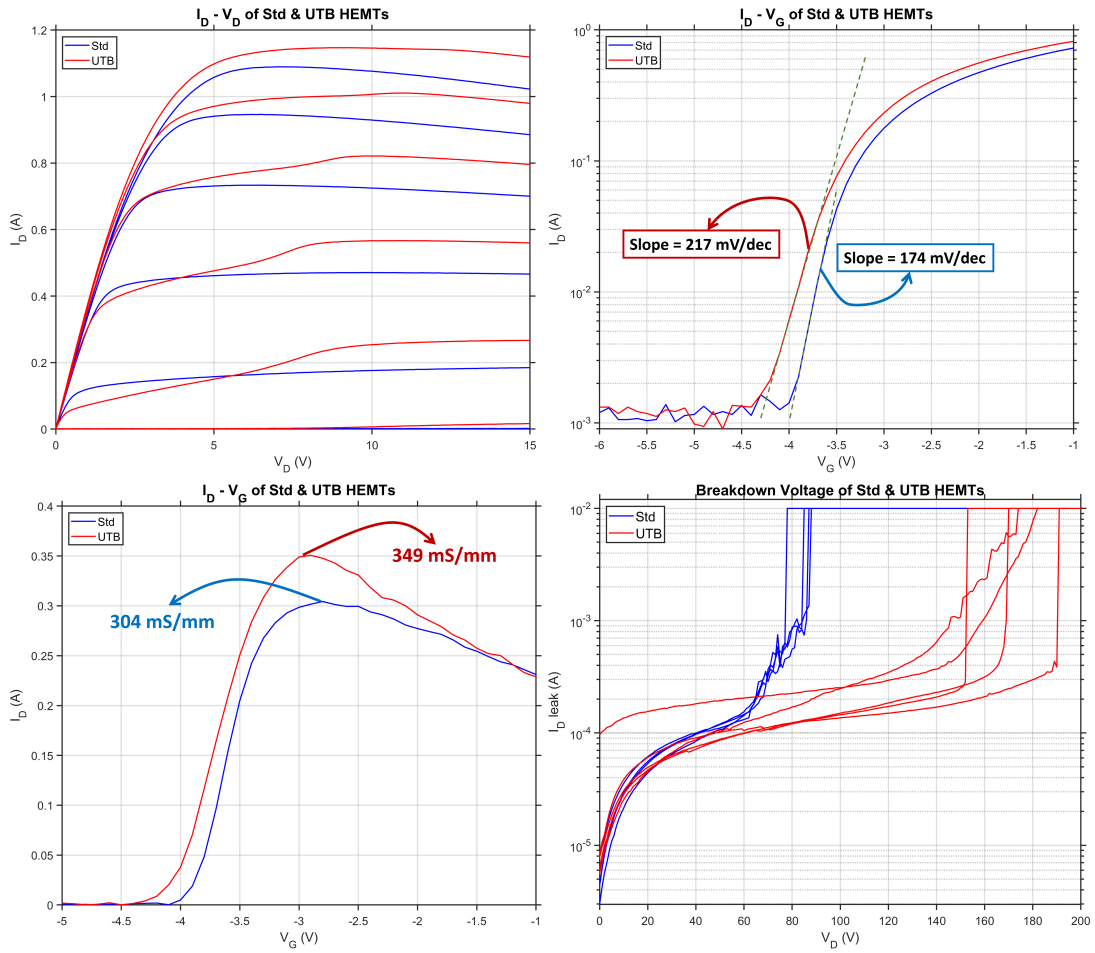


Figure 8.3: DC characteristics of Std and UTB HEMTs ($L_G = 0.25$ μm, $W_G = 125$ μm). (a) Output characteristics I_D–V_D for V_G from -4 V to 1 V. (b) Transfer characteristics I_D–V_G at $V_D = 10$ V. (c) Transconductance g_m versus V_G. (d) Off-state breakdown characteristics.

spacing $L_{ds} = 3.3$ μm. Figure 8.4(a) shows the off-state I_D–V_D curves for Std and UTB HEMTs under $V_G = -8$ V, with the drain swept to 200 V. The UTB devices not only break at significantly higher voltages but also exhibit roughly one order of magnitude lower leakage current in the high-voltage range compared with the Std devices. The corresponding breakdown histograms for 14 devices of each type are shown in Figure 8.4(b). The Std HEMTs exhibit an average breakdown around 105 V, whereas the UTB HEMTs show an average breakdown around 187 V, corresponding to an improvement of approximately 78%.

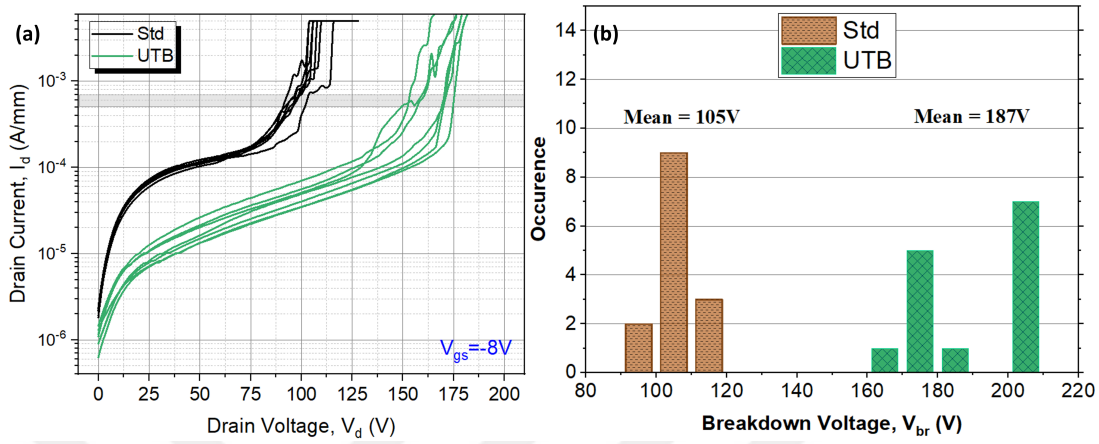


Figure 8.4: Off-state breakdown comparison for Std and UTB HEMTs (L_G = 0.25 μm, W_G = 125 μm, eight fingers, L_{ds} = 3.3 μm). (a) Measured I_{D}–V_{D} curves at $V_{\mathrm{G}} = -8$ V. (b) Breakdown voltage histograms for 14 devices of each type.

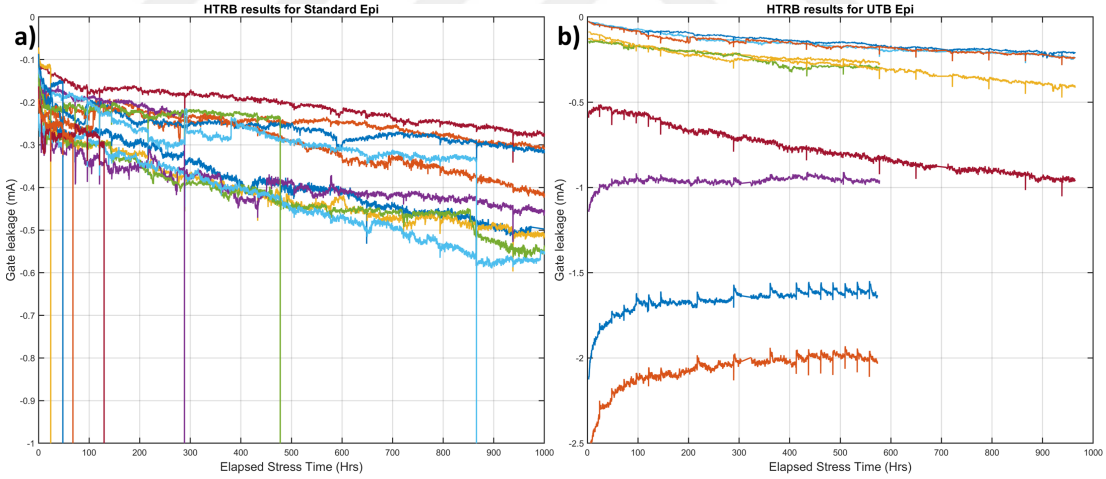


Figure 8.5: Long-term HTRB results for (a) standard and (b) UTB HEMTs with $L_{ds} = 3.5\mu m$.

Long-term HTRB tests of standard and UTB HEMTs with $L_{\mathrm{ds}} = 3.5$ μm are performed using the Accel-RF DC AARTS system. The devices operate under off-state stress at $(V_{\mathrm{gs}}, V_{\mathrm{ds}}) = (-8\text{ V}, 84\text{ V})$ and a base temperature of $T = 150°\mathrm{C}$. The evolution of gate leakage current at 150°C is plotted in Figure 8.5, where the abrupt drops in Figure 8.5(a) indicate catastrophic breakdown events. Under these conditions, 7 out of 16 HEMTs with the standard epitaxial design fail during HTRB, while all UTB HEMTs remain functional throughout the test. These results demonstrate that the UTB architecture not only enhances the breakdown

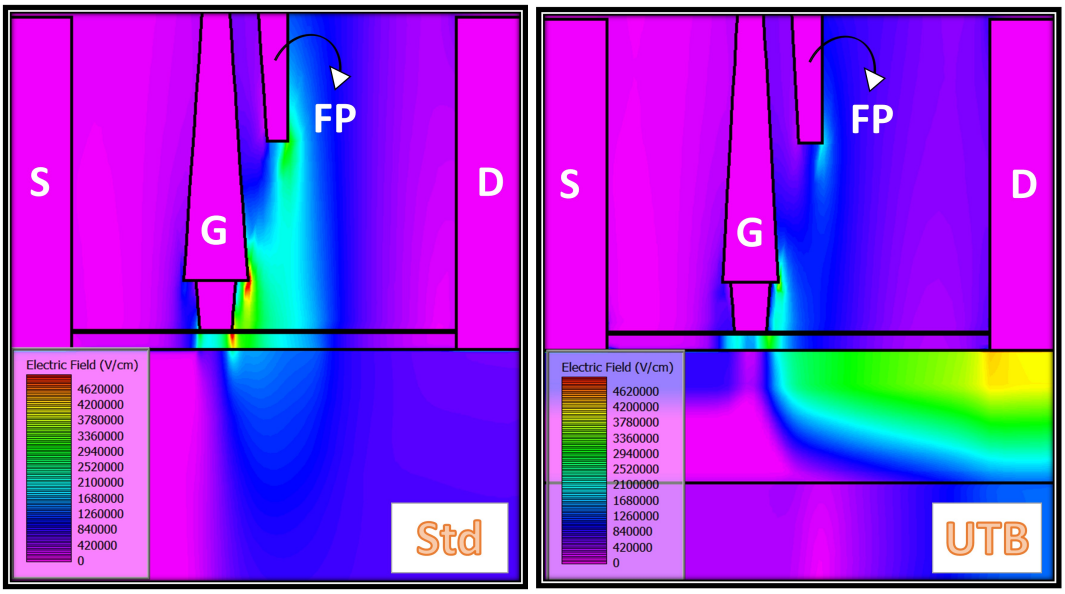


Figure 8.6: TCAD-simulated electric field distribution under deep off-state bias for (left) Std epitaxy and (right) UTB epitaxy. The UTB design reduces field peaks at the gate and field-plate edges and spreads the field into the drain access region.

voltage but also significantly improves long-term HTRB reliability.

This improvement is linked to the redistribution and relaxation of the electric field around the gate region. In the UTB devices, the hd-GaN layer beneath the 50 nm c-GaN contains a high concentration of carbon acceptor states, which act as a "virtual" buried field plate and modify the vertical field. As a result, the y-component of the electric field E_y in the GaN around the gate, field plate, and drain access region becomes more uniform. The peak field at the gate foot and gate head edges is reduced, while the field under the drain is slightly increased relative to Std HEMTs. These effects were confirmed by TCAD simulations.

Figure 8.6 compares the simulated electric field maps for Std and UTB HEMTs under deep off-state bias. In the Std case, strong field peaks appear at the drain-side gate foot edge, at the gate-head edge, and at the field-plate edges. When the peak field in these regions exceeds the critical field of the AlGaN/barrier stack, catastrophic breakdown occurs. In the UTB design, the field is more distributed along the access region and concentrated deeper under the drain, while the peaks

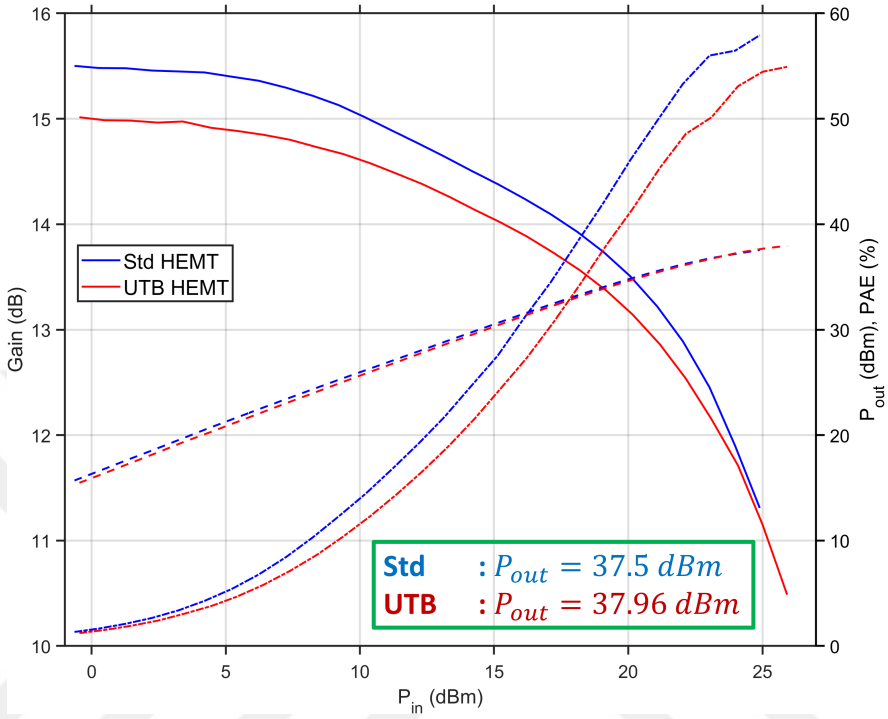


Figure 8.7: Large-signal RF performance of Std and UTB HEMTs: comparison of G_T, P_{out}, and PAE versus input power.

around the gate region are substantially reduced. Because the same critical field level is reached only at much higher drain voltages, the UTB devices achieve significantly higher breakdown voltage.

8.3.2 RF Characteristics

The impact of the buffer-free UTB epitaxy on RF performance was evaluated using large-signal load-pull measurements. Figure 8.7 summarizes the comparison between Std and UTB HEMTs in terms of transducer gain G_T, output power P_{out}, and power-added efficiency (PAE). The UTB devices deliver a peak output power density of 6.25 W/mm, which is about 11% higher than the 5.62 W/mm obtained from the Std HEMTs. The maximum G_T is slightly higher for Std devices (15.5 dB) than for UTB (15.0 dB), reflecting a small penalty in gain. PAE at saturation decreases from 57.9% (Std) to 54.9% (UTB). Thus, the primary RF benefit of the UTB design is higher P_{out} at very similar gain and only a modest

reduction in PAE. This can be traced back to the higher $I_{\mathrm{D,ss}}$ enabled by the Fe-free, higher-density 2DEG.

8.4 Conclusion

This work has presented a 0.2 μm-thick buffer-free ultra-thin buffer (UTB) AlGaN/GaN HEMT technology that replaces the conventional thick Fe-doped GaN buffer with an Fe-free stack comprising an AlN nucleation layer, a 150 nm hd-GaN layer, and a 50 nm c-GaN channel. By eliminating the Fe-doped buffer while maintaining a stable AlN-on-SiC nucleation scheme, the epitaxial process is simplified and the total GaN thickness is drastically reduced, without sacrificing crystalline quality.

In DC operation, the UTB devices show about 5% higher saturated drain current $I_{\mathrm{D,ss}}$ and roughly 15% higher peak transconductance g_m than the Std devices, with only a moderate degradation in subthreshold slope. In RF operation, the UTB HEMTs provide approximately 0.45 dB higher saturated P_{out}, at the expense of about 0.5 dB reduction in G_T and a small decrease in PAE. The most striking advantage appears in the off-state behavior: the average breakdown voltage increases by about 78%, and the off-state drain leakage is reduced by nearly one order of magnitude. TCAD simulations link these improvements to the altered electric field distribution in the UTB design, in which the hd-GaN layer and thin channel act together with the AlN nucleation to relax field peaks at the gate and field-plate edges and to shift part of the field into the drain-side region.

Overall, the UTB devices deliver significantly enhanced breakdown and leakage behavior, with competitive DC and RF performance, while avoiding the complexity and reliability risks associated with thick Fe-doped buffers. This buffer-free ultra-thin approach thus represents a promising direction for next-generation high-voltage, high-reliability GaN-on-SiC HEMTs.

Chapter 9

Conclusion and Future Work

9.1 Summary of the Thesis

The main objective of this thesis was to improve the reliability of GaN-on-SiC HEMTs under the most critical operating condition for high-voltage RF power amplifiers: deep off-state, high electric field, and elevated temperature. In this regime, field-driven failure mechanisms dominate, and degradation is often first observed as increased gate and drain leakage, current collapse, and time-dependent breakdown. For this reason, off-state durability, which is quantified primarily by breakdown voltage, HTRB failure rate, and leakage-current evolution, was adopted as the central figure of merit throughout the work.

Chapter 2 provided the technological background. It summarized the advantages of GaN as a wide-bandgap material, reviewed the AlGaN/GaN-on-SiC HEMT structure from substrate to metallization, and discussed the key epitaxial and micro-/nano-fabrication design parameters that determine electric-field distribution, leakage, and RF performance. The GaN-on-SiC process flow used in this work, including MOCVD epitaxy and multi-layer SiN T-gate fabrication, was described as the baseline platform.

Chapter 3 reviewed relevant failure and leakage mechanisms, with emphasis on impact ionization at the drain-side gate edge, hot-electron trapping at AlGaN/SiN and AlGaN/GaN interfaces and in the buffer, current collapse, and the various gate and drain leakage paths. It also introduced the long-term reliability tests (DC-HTOL, HTRB, RF-HTOL) and the DC and RF measurement setups used in the subsequent chapters, including pulsed I–V techniques for separating intrinsic behavior from trapping effects.

Chapters 4 and 5 focused on layout and process optimization of the baseline technology. RF-HTOL tests on packaged two-stage amplifiers built from the initial HEMTs showed early catastrophic failures under realistic RF stress, despite only modest degradation in output power and gate leakage. Breakdown measurements and post-failure SEM analysis indicated that the electric field peak regions are the weak points, causing premature breakdown below the targeted voltage range. By increasing the gate–drain spacing, adjusting the high voltage to low voltage distances, and preserving gate width and RF-relevant geometries, the breakdown voltage was increased by several tens of percent while the penalty in output power and efficiency remained small.

The same chapters also addressed process-related reliability issues. DC-HTOL tests on the first-generation devices revealed strong Q-point instability, with gate bias shifts up to several hundred millivolts during constant-current stress. TEM and STEM/EDS analysis showed a thin residual SiN layer under the gate, turning the intended Schottky contact into a thin MIS structure with a trap-rich interface. By extending the gate-foot etch and introducing a post-metal anneal (PMA), the SiN residue was removed, the Schottky interface was recovered, and the gate-voltage drift during HTOL was reduced to less than 50 mV. A new in-situ O_2/Ar ion pre-gate treatment further reduced gate and drain leakage by more than an order of magnitude and improved HTRB robustness. In parallel, the first SiN layer was redesigned using a higher-temperature PECVD process, resulting in denser, lower-leakage passivation and a dramatic reduction of catastrophic HTRB failures up to 200 °C. Extended HTRB and step-HTRB tests confirmed that the combination of improved gate treatment and optimized SiN passivation produced a stable and repeatable technology.

Chapter 6 presented a buffer-engineering method to mitigate impact ionization under deep off-state stress. Long-term HTRB measurements and analysis of gate-current degradation pointed out impact ionization at the drain-side gate edge as the dominant trigger. A buffer-engineering strategy based on thinning the channel GaN and reshaping the vertical field profile was proposed and validated. Devices with modified buffer design showed reduced impact-ionization volume, lower gate-edge stress, and improved HTRB leakage behavior, confirming that careful vertical field management in the buffer is as important as lateral field control in the access regions.

Chapter 7 introduced an AlGaN/GaN/AlGaN back-barrier epitaxial design to further control the field and electron confinement. The thin AlGaN back-barrier shifted the Fermi level and raised the conduction band in the buffer, improving confinement of the 2DEG and suppressing buffer leakage. Experimentally, the back-barrier devices exhibited about 30% higher breakdown voltage and more than a two-fold increase in time-to-failure under off-state HTRB stress compared to the standard Fe-doped buffers, while maintaining comparable DC and RF performance. Dynamic dispersion and current collapse were also significantly reduced. TCAD simulations showed lower peak electric field at the drain-side gate edge and field-plate edge, and a more favorable distribution of impact-ionization rate, explaining the improved reliability.

Chapter 8 proposed a more radical epitaxial concept: a Fe-free, ultra-thin buffer (UTB) design with a total GaN thickness of only 200 nm and a highly doped GaN layer acting as an electrostatic back barrier. This architecture eliminated the conventional thick Fe-doped buffer and exploited an AlN nucleation layer, a thin high-doped GaN region, and a thin channel to confine the 2DEG and redistribute the electric field. Compared to the standard epitaxy, the UTB devices showed approximately 78% higher average breakdown voltage, an order-of-magnitude lower off-state drain leakage, and zero failures in HTRB tests within the examined stress window. At the same time, they delivered higher output power and transconductance with only modest changes in gain and efficiency. TCAD and TEM analyses confirmed the high crystalline quality of the ultra-thin stack and demonstrated that the highly doped GaN effectively acted as a

field-shaping layer, relaxing the gate-edge field while shifting the maximum field deeper towards the drain.

9.2 Future Work

While the thesis demonstrates significant progress in off-state robustness of GaN-on-SiC HEMTs, several open problems and promising directions remain:

Deeper characterization of trap kinetics: The work relied mainly on HTRB, RF-HTOL, and pulsed I–V measurements to infer the role of traps. Future studies could combine these with temperature-dependent transient measurements and advanced spectroscopy to quantitatively extract trap energies, capture cross sections, and spatial distributions in both buffer and surface regions.

Extended characterization of ultra-thin buffer (UTB) epitaxy: The Fe-free UTB technology should be characterized more broadly: across different gate lengths, peripheries and frequency bands (RF and power), and under additional stress methods such as extended RF-HTOL, dynamic RF stress, and thermal cycling. Its compatibility with different HEMT platforms (gate lengths, field-plate schemes, substrates) should be tested to see whether the UTB concept can be transferred as a general reliability solution.

Extension to higher-voltage and higher-frequency nodes: The proposed epitaxial and process concepts should be evaluated for higher operating voltages and for millimeter-wave devices with shorter gate lengths, where field crowding and hot-electron effects are even more severe.

Advanced gate stack and gate-region engineering: The results clearly show that gate processing is a dominant lever for off-state reliability. Future work should develop controlled ways to remove or precisely tune the ultra-thin oxide/nitride under the gate, and systematically explore alternative gate metal

stacks, sidewall angles, and coverage that reduce local field crowding and hot-electron injection at the gate edge.

Refined modeling and variability-aware reliability metrics: Coupled electro-thermal TCAD and compact models should be built to link breakdown, HTRB lifetime, and dynamic trapping to V_{DS}, temperature, and duty cycle, including device-to-device variability. These models can then be used by circuit and module designers to predict lifetime at PA and converter level, and to co-optimize device design with real application stress profiles.

In conclusion, this thesis establishes a systematical analysis and testing for improving off-state reliability in GaN-on-SiC HEMTs. It is demonstrates that substantial improvements in breakdown performance, leakage stability, and lifetime are achievable through layout, process, and epitaxial engineering. The methods and design principles developed here provide a foundation for the next generation of robust GaN power and RF devices operating under increasingly demanding conditions.

Bibliography

[1] M. Di Paolo Emilio, *Gallium Nitride*, pp. 35–47. Cham: Springer Nature Switzerland, 2024.

[2] N. Islam, M. F. P. Mohamed, M. F. A. J. Khan, S. Falina, H. Kawarada, and M. Syamsul, "Reliability, applications and challenges of GaN HEMT technology for modern power devices: A review," *Crystals*, vol. 12, no. 11, p. 1581, 2022.

[3] H. Lu, M. Zhang, L. Yang, B. Hou, R. P. Martinez, M. Mi, J. Du, L. Deng, M. Wu, S. Chowdhury, *et al.*, "A review of GaN RF devices and power amplifiers for 5G communication applications," *Fundamental Research*, vol. 5, no. 1, pp. 315–331, 2025.

[4] Z. Tian, X. Ji, D. Yang, and P. Liu, "Research progress in breakdown enhancement for GaN-based high-electron-mobility transistors," *Electronics*, vol. 12, no. 21, p. 4435, 2023.

[5] R. Gracia Sáez and N. Medrano Marqués, "LDMOS versus GaN RF power amplifier comparison based on the computing complexity needed to linearize the output," *Electronics*, vol. 8, no. 11, p. 1260, 2019.

[6] N. Miyazawa, M. Nishihara, K. Usami, M. Aojima, and T. Yamamoto, "S-band 600W and X-band 200W high-power GaN HEMTs for radar transmitters," *SEI Technical Review*, vol. 84, p. 146, 2017.

[7] S. C. Bera, *Microwave GaN Transistors*, pp. 23–31. Singapore: Springer Nature Singapore, 2022.

[8] T. Yamasaki, Y. Kittaka, H. Minamide, K. Yamauchi, S. Miwa, S. Goto, M. Nakayama, M. Kohno, and N. Yoshida, "A 68% efficiency, C-band 100W GaN power amplifier for space applications," in *2010 IEEE MTT-S International Microwave Symposium*, pp. 1384–1387, IEEE, 2010.

[9] J.-C. Jeong, D.-P. Jang, B.-G. Han, and I.-B. Yom, "A compact C-band 50 W AlGaN/GaN high-power MMIC amplifier for radar applications," *ETRI Journal*, vol. 36, no. 3, pp. 498–501, 2014.

[10] S. Krause, P. Brückner, and R. Quay, "100-V GaN HEMT technology with record-high efficiency at C-band frequencies," in *International Conference on Compound Semiconductor Manufacturing Technology 2022*, 2022.

[11] G. Formicone, "A 15 W/mm GaN technology for C-band pulsed radars with 45% PAE," in *Proc. CS-MANTECH*, pp. 29–32, 2018.

[12] A. Yamada, Y. Minoura, N. Kurahashi, Y. Kamada, T. Ohki, M. Sato, and N. Nakamura, "31 W/mm at 8 GHz in InAlGaN/GaN HEMT with thermal CVD SiNx passivation," *IEEE Electron Device Letters*, vol. 45, no. 3, pp. 324–327, 2024.

[13] M. Peng, Y. Zheng, W. Luo, and X. Liu, "14.2 W/mm internally-matched AlGaN/GaN HEMT for X-band applications," *Solid-state electronics*, vol. 64, no. 1, pp. 63–66, 2011.

[14] M. Góralczyk and W. Wojtasiak, "ISM 2.45 GHz band high-efficient 15 W GaN HEMT power amplifier: design validation," *International Journal of Microwave and Wireless Technologies*, vol. 11, no. 7, pp. 546–553, 2019.

[15] J. Kim, "A review of Ku-band GaN HEMT power amplifiers development," *Micromachines*, vol. 15, no. 11, p. 1381, 2024.

[16] J. Weimer, D. Koch, M. Nitzsche, J. Haarer, J. Roth-Stielow, and I. Kallfass, "Miniaturization and thermal design of a 170 W AC/DC battery charger utilizing GaN power devices," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 13–25, 2021.

[17] O. Bay, M. T. Tran, M. El Baghdadi, S. Chakraborty, and O. Hegazy, "A comprehensive review of GaN-based bi-directional on-board charger topologies and modulation methods," *Energies*, vol. 16, no. 8, p. 3433, 2023.

[18] R. Ponnambalam and I. Vairavasundaram, "GaN-based DC-DC converters for EV fast charging: A review of wide bandgap devices technology," *Results in Engineering*, p. 107548, 2025.

[19] L. Garcia-Rodriguez, V. Jones, J. Balda, E. Lindstrom, A. Oliva, and J. Gonzalez-Llorente, "Design of a GaN-based microinverter for photovoltaic systems," in *2014 IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1–6, IEEE, 2014.

[20] O. Karimzada and G. De Donato, "Design and verification of a GaN-based, single stage, grid-connected three-phase PV inverter," *IEEE Transactions on Power Electronics*, 2024.

[21] A. Talukder, M. R. Ifty, and A. Al Fahad, "Comprehensive review of GaN HEMTs: Architectures, recent developments, reliability concerns, challenges, and multifaceted applications," *e-Prime-Advances in Electrical Engineering, Electronics and Energy*, p. 101059, 2025.

[22] M. Susmita, L. Catherine, E. Surya, and K. Hao-Chung, "A comprehensive study on GaN power devices: Reliability, performance, and application perspectives," *Electronics*, vol. 14, no. 22, p. 4430, 2025.

[23] D. Cheney, E. Douglas, L. Liu, C. Lo, Y. Xi, B. Gila, F. Ren, D. Horton, M. Law, D. J. Smith, *et al.*, "Reliability studies of AlGaN/GaN high electron mobility transistors," *Semiconductor Science and Technology*, vol. 28, no. 7, p. 074019, 2013.

[24] M. Kuball, M. Ťapajna, R. J. Simms, M. Faqir, and U. K. Mishra, "AlGaN/GaN HEMT device reliability and degradation evolution: Importance of diffusion processes," *Microelectronics Reliability*, vol. 51, no. 2, pp. 195–200, 2011.

[25] J. W. Pomeroy, M. J. Uren, B. Lambert, and M. Kuball, "Operating channel temperature in GaN HEMTs: DC versus RF accelerated life testing," *Microelectronics Reliability*, vol. 55, no. 12, pp. 2505–2510, 2015.

[26] E. Zanoni, M. Meneghini, A. Chini, D. Marcon, and G. Meneghesso, "AlGaN/GaN-based HEMTs failure physics and reliability: Mechanisms affecting gate edge and Schottky junction," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3119–3131, 2013.

[27] S. Park, C. Floresca, U. Chowdhury, J. L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri, and M. J. Kim, "Physical degradation of GaN HEMT devices under high drain bias reliability testing," *Microelectronics Reliability*, vol. 49, no. 5, pp. 478–483, 2009.

[28] D. Marcon, G. Meneghesso, T.-L. Wu, S. Stoffels, M. Meneghini, E. Zanoni, and S. Decoutere, "Reliability analysis of permanent degradations on AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3132–3141, 2013.

[29] G. Meneghesso, M. Meneghini, A. Stocco, D. Bisi, C. de Santi, I. Rossetto, A. Zanandrea, F. Rampazzo, and E. Zanoni, "Degradation of AlGaN/GaN HEMT devices: Role of reverse-bias and hot electron stress," *Microelectronic engineering*, vol. 109, pp. 257–261, 2013.

[30] D. Marcon, J. Viaene, P. Favia, H. Bender, X. Kang, S. Lenci, S. Stoffels, and S. Decoutere, "Reliability of AlGaN/GaN HEMTs: Permanent leakage current increase and output current drop," in *Proceedings of the 20th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, pp. 249–254, IEEE, 2013.

[31] A. D. Latorre-Rey, F. F. Sabatti, J. D. Albrecht, and M. Saraniti, "Hot electron generation under large-signal radio frequency operation of GaN high-electron-mobility transistors," *Applied Physics Letters*, vol. 111, no. 1, 2017.

[32] A. Tajalli, M. Meneghini, I. Rossetto, P. Moens, A. Banerjee, E. Zanoni, and G. Meneghesso, "Field and hot electron-induced degradation in GaN-based power MIS-HEMTs," *Microelectronics Reliability*, vol. 76, pp. 282–286, 2017.

[33] A. Minetto, B. Deutschmann, N. Modolo, A. Nardo, M. Meneghini, E. Zanoni, L. Sayadi, G. Prechtl, S. Sicre, and O. Häberlen, "Hot-electron effects in AlGaN/GaN HEMTs under semi-on DC stress," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4602–4605, 2020.

[34] H. Onodera, T. Kabemura, and K. Horio, "Analysis of impact ionization effects on current collapse of AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 69, no. 11, pp. 6028–6034, 2022.

[35] R. Tsurumaki, N. Noda, and K. Horio, "Similarities of lag phenomena and current collapse in field-plate AlGaN/GaN HEMTs with different types of buffer layers," *Microelectronics Reliability*, vol. 73, pp. 36–41, 2017.

[36] Y. Jia, Y. Xu, K. Lu, Z. Wen, A.-D. Huang, and Y.-X. Guo, "Characterization of buffer-related current collapse by buffer potential simulation in AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 65, no. 8, pp. 3169–3175, 2018.

[37] Y. Saito, R. Tsurumaki, N. Noda, and K. Horio, "Analysis of reduction in lag phenomena and current collapse in field-plate AlGaN/GaN HEMTs with high acceptor density in a buffer layer," *IEEE Transactions on Device and Materials Reliability*, vol. 18, no. 1, pp. 46–53, 2017.

[38] J. Hu, S. Stoffels, M. Zhao, A. N. Tallarico, I. Rossetto, M. Meneghini, X. Kang, B. Bakeroot, D. Marcon, B. Kaczer, *et al.*, "Time-dependent breakdown mechanisms and reliability improvement in edge terminated AlGaN/GaN Schottky diodes under HTRB tests," *IEEE Electron Device Letters*, vol. 38, no. 3, pp. 371–374, 2017.

[39] J. R. Kumar, H. V. Du John, B. K. J. IV, J. Ajayan, D. Nirmal, *et al.*, "A comprehensive review of AlGaN/GaN high electron mobility transistors:

Architectures and field plate techniques for high power/high frequency applications," *Microelectronics Journal*, vol. 140, p. 105951, 2023.

[40] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287–305, 2008.

[41] Z. Gao, M. Meneghini, F. Rampazzo, M. Rzin, C. De Santi, G. Meneghesso, and E. Zanoni, "Reliability comparison of AlGaN/GaN HEMTs with different carbon doping concentration," *Microelectronics Reliability*, vol. 100, p. 113489, 2019.

[42] Z. Gao, F. Rampazzo, M. Meneghini, C. De Santi, F. Chiocchetta, D. Marcon, G. Meneghesso, and E. Zanoni, "Degradation mechanism of 0.15 μm AlGaN/GaN HEMTs: Effects of hot electrons," *Microelectronics Reliability*, vol. 114, p. 113905, 2020.

[43] P.-H. Chang, C.-R. Huang, C.-H. Liu, K.-W. Lee, and H.-C. Chiu, "The effect of dual-layer carbon/iron-doped buffers in an AlGaN/GaN high-electron-mobility transistor," *Micromachines*, vol. 16, no. 9, p. 1034, 2025.

[44] Q. Yu, S. Wu, M. Zhang, L. Yang, X. Zou, H. Lu, C. Shi, W. Gao, M. Wu, B. Hou, *et al.*, "The effect of channel layer thickness on the performance of GaN HEMTs for RF applications," *Micromachines*, vol. 16, no. 1, p. 1, 2024.

[45] R. Elwaradi, J. Mehta, T. H. Ngo, M. Nemoz, C. Bougerol, F. Medjdoub, and Y. Cordier, "Effects of GaN channel downscaling in AlGaN–GaN high electron mobility transistor structures grown on AlN bulk substrate," *Journal of Applied Physics*, vol. 133, no. 14, 2023.

[46] K. Narang, V. K. Singh, A. Pandey, R. Khan, R. K. Bag, D. Rawal, M. Padmavati, R. Tyagi, and R. Singh, "Suitability of thin-GaN for AlGaN/GaN HEMT material and device," *Journal of Materials Science*, vol. 57, no. 10, pp. 5913–5923, 2022.

[47] K. Harrouche, S. Venkatachalam, L. Ben-Hammou, F. Grandpierron, E. Okada, and F. Medjdoub, "Low trapping effects and high electron confinement in short AlN/GaN-on-SiC HEMTs by means of a thin AlGaN back barrier," *Micromachines*, vol. 14, no. 2, p. 291, 2023.

[48] A. Anand, K. Sehra, Chanchal, Reeta, R. Narang, D. Rawal, M. Mishra, M. Saxena, and M. Gupta, "Impact of barrier layer thickness on DC and RF performance of AlGaN/GaN high electron mobility transistors," *Applied Physics A*, vol. 129, no. 8, p. 563, 2023.

[49] H. Hamza and A. Jarndal, "Improved graded barrier/buffer double-channel GaN HEMT for high-power RF applications," *Journal of Electronic Materials*, vol. 54, no. 10, pp. 9219–9233, 2025.

[50] F. Zeng, J. X. An, G. Zhou, W. Li, H. Wang, T. Duan, L. Jiang, and H. Yu, "A comprehensive review of recent progress on GaN high electron mobility transistors: Devices, fabrication and reliability," *Electronics*, vol. 7, no. 12, p. 377, 2018.

[51] M. K. Reddy and Y.-L. Song, "Impact and analysis of Al composition in barrier and buffer regions of $Al_xGa_{(1-x)}N$/GaN HEMT device using TCAD simulations," *Semiconductors*, vol. 59, no. 10, pp. 1112–1123, 2025.

[52] B. Mounika, J. Ajayan, S. Bhattacharya, and D. Nirmal, "Recent developments in materials, architectures and processing of AlGaN/GaN HEMTs for future RF and power electronic applications: A critical review," *Micro and Nanostructures*, vol. 168, p. 207317, 2022.

[53] N. M. Shrestha, Y. Y. Wang, Y. Li, and E. Chang, "Simulation study of AlN spacer layer thickness on AlGaN/GaN HEMT," *Himalayan Physics*, vol. 4, pp. 14–17, 2013.

[54] T.-S. Ko, D.-Y. Lin, C.-F. Lin, C.-W. Chang, J.-C. Zhang, and S.-J. Tu, "High-temperature carrier density and mobility enhancements in AlGaN/GaN HEMT using AlN spacer layer," *Journal of Crystal Growth*, vol. 464, pp. 175–179, 2017.

[55] Z. Nie, K. Wang, X. Liu, and H. Wang, "Effect of GaN cap thickness on the DC performance of AlGaN/GaN HEMTs," *Micromachines*, vol. 15, no. 5, p. 571, 2024.

[56] B. Lv, S. Ma, J. Lang, F. Yu, Z. Wang, and J. Mo, "GaN cap impacts on gate leakage mechanisms in AlGaN/GaN high-electron mobility transistors," *Applied Physics Letters*, vol. 126, no. 26, 2025.

[57] S. Pharkphoumy, V. Janardhanam, T.-H. Jang, J. Park, K.-H. Shim, and C.-J. Choi, "Optimized device geometry of normally-on field-plate AlGaN/GaN high electron mobility transistors for high breakdown performance using TCAD simulation," *Electronics*, vol. 10, no. 21, p. 2642, 2021.

[58] C. Deng, W.-C. Cheng, X. Chen, K. Wen, M. He, C. Tang, P. Wang, Q. Wang, and H. Yu, "Current collapse suppression in AlGaN/GaN HEMTs using dual-layer SiNx stressor passivation," *Applied Physics Letters*, vol. 122, no. 23, 2023.

[59] W. Dongfang, Y. Tingting, W. Ke, C. Xiaojuan, and L. Xinyu, "Gate-structure optimization for high frequency power AlGaN/GaN HEMTs," *Journal of Semiconductors*, vol. 31, no. 5, p. 054003, 2010.

[60] V. Palankovski, S. Vitanov, and R. Quay, "Field-plate optimization of AlGaN/GaN HEMTs," in *2006 IEEE Compound semiconductor integrated circuit symposium*, pp. 107–110, IEEE, 2006.

[61] Z.-X. Wang, L. Du, J.-W. Liu, Y. Wang, Y. Jiang, S.-W. Ji, S.-W. Dong, W.-W. Chen, X.-H. Tan, J.-L. Li, *et al.*, "Breakdown voltage enhancement in GaN channel and AlGaN channel HEMTs using large gate metal height," *Chinese Physics B*, vol. 29, no. 2, p. 027301, 2020.

[62] N. Shi, K. Wang, B. Zhou, J. Weng, and Z. Cheng, "Optimization AlGaN/GaN HEMT with field plate structures," *Micromachines*, vol. 13, no. 5, p. 702, 2022.

[63] B. Liao, Q. Zhou, J. Qin, and H. Wang, "Simulation of AlGaN/GaN HEMTs' breakdown voltage enhancement using gate field-plate, source field-plate and drain field plate," *Electronics*, vol. 8, no. 4, p. 406, 2019.

[64] A. A. Fletcher, D. Nirmal, J. Ajayan, and L. Arivazhagan, "Analysis of AlGaN/GaN HEMT using discrete field plate technique for high power and high frequency applications," *AEU-International Journal of Electronics and Communications*, vol. 99, pp. 325–330, 2019.

[65] R. Natarajan, P. Murugapandiyan, N. Vigneshwari, A. Mohanbabu, S. Ravi, *et al.*, "Investigation of different buffer layer impact on AlN/GaN/AlGaN HEMT using silicon carbide substrate for high-speed RF applications," *Micro and Nanostructures*, vol. 189, p. 207815, 2024.

[66] M. Meneghini, A. Stocco, R. Silvestri, G. Meneghesso, and E. Zanoni, "Degradation of AlGaN/GaN high electron mobility transistors related to hot electrons," *Applied Physics Letters*, vol. 100, no. 23, 2012.

[67] I. Hwang, J. Kim, S. Chong, H.-S. Choi, S.-K. Hwang, J. Oh, J. K. Shin, and U.-I. Chung, "Impact of channel hot electrons on current collapse in AlGaN/GaN HEMTs," *IEEE electron device letters*, vol. 34, no. 12, pp. 1494–1496, 2013.

[68] F. Yang, S. Dalcanale, M. Gajda, S. Karboyan, M. J. Uren, and M. Kuball, "The impact of hot electrons and self-heating during hard-switching in AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 67, no. 3, pp. 869–874, 2020.

[69] M. Meneghini, N. Ronchi, A. Stocco, G. Meneghesso, U. K. Mishra, Y. Pei, and E. Zanoni, "Investigation of trapping and hot-electron effects in GaN HEMTs by means of a combined electrooptical method," *IEEE transactions on electron devices*, vol. 58, no. 9, pp. 2996–3003, 2011.

[70] A. Sozza, C. Dua, E. Morvan, S. Delage, F. Rampazzo, A. Tazzoli, F. Danesin, G. Meneghesso, E. Zanoni, A. Curutchet, *et al.*, "Evidence of traps creation in GaN/AlGaN/GaN HEMTs after a 3000 hour on-state and off-state hot-electron stress," in *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.*, pp. 4–pp, IEEE, 2005.

[71] Y. Zhu, Y. Zhang, H. Qu, H. Gao, H. Du, H. Guo, and X. Zou, "Suppressed current collapse and improved threshold voltage stability of AlGaN/GaN HEMT via O_2 plasma treatment," *Microelectronics Journal*, vol. 148, p. 106191, 2024.

[72] M. J. Uren, J. Moreke, and M. Kuball, "Buffer design to minimize current collapse in GaN/AlGaN hfets," *IEEE Transactions on Electron Devices*, vol. 59, no. 12, pp. 3327–3333, 2012.

[73] K. Li, T. Matsuda, E. Yagyu, K. H. Teo, and S. Rakheja, "Trapping phenomena in GaN HEMTs with Fe-and C-doped buffer," in *2022 Device Research Conference (DRC)*, pp. 1–2, IEEE, 2022.

[74] H. Wu, X. Fu, Y. Wang, J. Guo, J. Shen, and S. Hu, "Breakdown voltage improvement of enhancement mode AlGaN/GaN HEMT by a novel step-etched GaN buffer structure," *Results in Physics*, vol. 29, p. 104768, 2021.

[75] M. Ma, Y. Cao, H. Lv, Z. Wang, X. Zhang, C. Chen, L. Wu, L. Lv, X. Zheng, W. Tian, *et al.*, "Effect of acceptor traps in GaN buffer layer on breakdown performance of AlGaN/GaN HEMTs," *Micromachines*, vol. 14, no. 1, p. 79, 2022.

[76] I. Jabbari, M. Baira, H. Maaref, and R. Mghaieth, "Evidence of Poole-frenkel and Fowler-Nordheim tunneling transport mechanisms in leakage current of (Pd/Au)/$Al_{0.22}Ga_{0.78}N$/GaN heterostructures," *Solid State Communications*, vol. 314, p. 113920, 2020.

[77] K. Li, E. Yagyu, H. Saito, K. H. Teo, and S. Rakheja, "Compact modeling of gate leakage phenomenon in GaN HEMTs," in *2020 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, pp. 225–228, IEEE, 2020.

[78] S. S. Mahajan, A. Tomer, A. Malik, R. Laishram, V. R. Agarwal, and A. Naik, "Electrical characteristics of post-gate-annealed AlGaN/GaN HEMTs on sapphire substrate," in *2014 IEEE 2nd International Conference on Emerging Electronics (ICEE)*, pp. 1–3, IEEE, 2014.

[79] C. Chen, Q. Wang, W. Li, Q. Wang, C. Feng, L. Jiang, H. Xiao, and X. Wang, "Effect of the post-gate annealing on the gate reliability of AlGaN/GaN HEMTs," *Journal of Semiconductors*, vol. 42, no. 9, p. 092802, 2021.

[80] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Transactions on electron devices*, vol. 48, no. 3, pp. 560–566, 2002.

[81] M. J. Tadjer, A. D. Koehler, C. R. Eddy Jr, T. J. Anderson, K. D. Hobart, and F. J. Kub, "Optimization of AlGaN/GaN HEMT SiN passivation by mixed frequency PECVD," in *CS Mantech Conf. Digest*, p. 307, 2016.

[82] X. Lu, H. Jiang, C. Liu, X. Zou, and K. M. Lau, "Off-state leakage current reduction in AlGaN/GaN high electron mobility transistors by combining surface treatment and post-gate annealing," *Semiconductor Science and Technology*, vol. 31, no. 5, p. 055019, 2016.

[83] S. Chakraborty and T.-W. Kim, "Comprehensive schottky barrier height behavior and reliability instability with Ni/Au and Pt/Ti/Pt/Au on AlGaN/GaN high-electron-mobility transistors," *Micromachines*, vol. 13, no. 1, p. 84, 2022.

[84] N. Sharma, C. Periasamy, N. Chaturvedi, and N. Chaturvedi, "Trapping effects on leakage and current collapse in AlGaN/GaN HEMTs," *Journal of Electronic Materials*, vol. 49, no. 10, pp. 5687–5697, 2020.

[85] J. Kim, G. Lee, K. Cho, J. Y. Park, B.-G. Min, J. Jeong, H.-G. Ji, W. Chang, J.-M. Lee, and D.-M. Kang, "The impact of gate annealing on leakage current and radio frequency efficiency in AlGaN/GaN high-electron-mobility transistors," *Electronics*, vol. 13, no. 20, p. 4038, 2024.

[86] S. M. Sze, Y. Li, and K. K. Ng, *Physics of semiconductor devices*. John wiley & sons, 2021.

[87] M. Belyansky, N. Klymko, A. Madan, A. Mallikarjunan, Y. Li, A. Chakravarti, S. Deshpande, A. Domenicucci, S. Bedell, E. Adams, *et al.*,

"Stress generation in PECVD silicon nitride thin films for microelectronics applications," *MRS Online Proceedings Library (OPL)*, vol. 863, pp. B7–9, 2005.

[88] B. E. Jang and S. J. Hong, "Spectroscopic analysis of film stress mechanism in PECVD silicon nitride," *Transactions on Electrical and Electronic Materials*, vol. 19, no. 1, pp. 1–6, 2018.

[89] L. RuGuan, W. YuanSheng, Z. Chang, L. XueYang, L. Ping, and H. Yun, "Impact of high temperature reverse bias (htrb) stress on the degradation of AlGaN/GaN HEMTs," in *2014 IEEE International Conference on Electron Devices and Solid-State Circuits*, pp. 1–2, IEEE, 2014.

[90] P. Dai, S. Wang, and H. Lu, "Research on the reliability of threshold voltage based on GaN high-electron-mobility transistors," *Micromachines*, vol. 15, no. 3, p. 321, 2024.

[91] Z. Gao, M. Meneghini, K. Harrouche, R. Kabouche, F. Chiocchetta, E. Okada, F. Rampazzo, C. De Santi, F. Medjdoub, G. Meneghesso, *et al.*, "Short term reliability and robustness of ultra-thin barrier, 110 nm-gate AlN/GaN HEMTs," in *2020 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, pp. 1–6, IEEE, 2020.

[92] E. Miller, X. Dang, and E. Yu, "Gate leakage current mechanisms in AlGaN/GaN heterostructure field-effect transistors," *Journal of applied Physics*, vol. 88, no. 10, pp. 5951–5958, 2000.

[93] G. Meneghesso, M. Meneghini, D. Bisi, I. Rossetto, T.-L. Wu, M. Van Hove, D. Marcon, S. Stoffels, S. Decoutere, and E. Zanoni, "Trapping and reliability issues in GaN-based MIS HEMTs with partially recessed gate," *Microelectronics Reliability*, vol. 58, pp. 151–157, 2016.

[94] M. I. Nawaz, A. Gurbuz, G. Salkim, S. Zafar, B. C. Akoglu, A. Bek, and E. Ozbay, "Gate leakage reduction in AlGaN/GaN HEMTs using in situ ion treatment," *Engineering Research Express*, vol. 6, no. 3, p. 035366, 2024.

[95] G. Zhou, F. Zeng, R. Gao, Q. Wang, K. Cheng, G. Xia, and H. Yu, "Improved gate reliability of p-GaN gate HEMTs by gate doping engineering," *arXiv preprint arXiv:2106.01495*, 2021.

[96] S. Kumar, S. B. Dolmanan, S. Tripathy, R. Muralidharan, and D. N. Nath, "Meandering gate edges for breakdown voltage enhancement in AlGaN/GaN high electron mobility transistors," *physica status solidi (a)*, vol. 217, no. 5, p. 1900766, 2020.

[97] A. N. Khan, A. M. Bhat, K. Jena, T. R. Lenka, and G. Chatterjee, "Improved breakdown voltage mechanism in AlGaN/GaN HEMT for RF/microwave applications: design and physical insights of dual field plate," *Microelectronics Reliability*, vol. 147, p. 115036, 2023.

[98] Y. Chen, Q. Zhu, J. Zhu, M. Mi, M. Zhang, Y. Zhou, Z. Zhao, X. Ma, and Y. Hao, "Degradation induced by holes in si_3n_4/AlGaN/GaN MIS HEMTs under off-state stress with UV light," *Science China Information Sciences*, vol. 66, no. 2, p. 122401, 2023.

[99] B. Güneş, A. Ghobadi, O. Odabasi, B. Bütün, and E. Özbay, "Improved drain lag by reduced surface current in GaN HEMT via an ultrathin HfO_2 blanket layer," *Semiconductor Science and Technology*, vol. 38, no. 6, p. 065002, 2023.

[100] G. Meneghesso, M. Meneghini, and E. Zanoni, "Breakdown mechanisms in AlGaN/GaN HEMTs: an overview," *Japanese Journal of Applied Physics*, vol. 53, no. 10, p. 100211, 2014.

[101] X. Wang, S. Huang, Y. Zheng, K. Wei, X. Chen, H. Zhang, and X. Liu, "Effect of GaN channel layer thickness on DC and RF performance of GaN HEMTs with composite AlGaN/GaN buffer," *IEEE Transactions on electron devices*, vol. 61, no. 5, pp. 1341–1346, 2014.

[102] D. Bisi, A. Stocco, I. Rossetto, M. Meneghini, F. Rampazzo, A. Chini, F. Soci, A. Pantellini, C. Lanzieri, P. Gamarra, *et al.*, "Effects of buffer compensation strategies on the electrical performance and RF reliability

of AlGaN/GaN HEMTs," *Microelectronics Reliability*, vol. 55, no. 9-10, pp. 1662–1666, 2015.

[103] Y. C. Choi, M. Pophristic, H.-Y. Cha, B. Peres, M. G. Spencer, and L. F. Eastman, "The effect of an Fe-doped GaN buffer on off-state breakdown characteristics in AlGaN/GaN HEMTs on Si substrate," *IEEE transactions on Electron devices*, vol. 53, no. 12, pp. 2926–2931, 2006.

[104] L.-Y. Peng, Y.-H. Cheng, H.-C. Chiu, *et al.*, "Effects of the Fe-doped GaN buffer in AlGaN/GaN HEMTs on SiC substrate," in *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, pp. 645–648, IEEE, 2015.

[105] V. Suresh, S. Siddhartthan, and M. Varadharajaperumal, "Increasing the breakdown voltage in gate–field plate high electron mobility transistor using a surface field distribution layer and gate-drain edge passivation," *Micro and Nanostructures*, vol. 164, p. 107164, 2022.

[106] Y.-W. Lian, Y.-S. Lin, H.-C. Lu, Y.-C. Huang, and S. S. Hsu, "AlGaN/GaN HEMTs on silicon with hybrid Schottky–ohmic drain for high breakdown voltage and low leakage current," *IEEE electron device letters*, vol. 33, no. 7, pp. 973–975, 2012.

[107] L. Yang, B. Hou, F. Jia, M. Zhang, M. Wu, X. Niu, H. Lu, C. Shi, M. Mi, Q. Zhu, *et al.*, "The DC performance and RF characteristics of GaN-based HEMTs improvement using graded AlGaN back barrier and Fe/C co-doped buffer," *IEEE Transactions on Electron Devices*, vol. 69, no. 8, pp. 4170–4174, 2022.

[108] D. Nirmal, L. Arivazhagan, *et al.*, "Impact of AlGaN back barrier in AlGaN/GaN HEMT on GaN substrate," in *2020 5th International Conference on Devices, Circuits and Systems (ICDCS)*, pp. 290–293, IEEE, 2020.

[109] H. Wang, H. Chiu, W. Hsu, C. Liu, C. Chuang, J. Liu, and Y. Huang, "The impact of $Al_xGa_{1-x}N$ back barrier in AlGaN/GaN high electron mobility transistors (HEMTs) on si x-inch MCZ Si substrate," *Coatings*, vol. 10, no. 6, p. 570, 2020.

[110] E. Bahat-Treidel, O. Hilt, F. Brunner, J. Wurfl, and G. Trankle, "Punchthrough-voltage enhancement of AlGaN/GaN HEMTs using AlGaN double-heterojunction confinement," *IEEE Transactions on Electron Devices*, vol. 55, no. 12, pp. 3354–3359, 2008.

[111] Y. Chen, Y. Jiang, P. Xu, Z. Ma, X. Wang, T. He, M. Peng, W. Luo, X. Liu, L. Wang, *et al.*, "Improvement of breakdown characteristics of a GaN HEMT with AlGaN buffer layer," *Journal of electronic materials*, vol. 41, pp. 471–475, 2012.

[112] A. Augustine Fletcher, D. Nirmal, L. Arivazhagan, J. Ajayan, and A. Varghese, "Enhancement of Johnson figure of merit in III-V HEMT combined with discrete field plate and AlGaN blocking layer," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 30, no. 2, p. e22040, 2020.

[113] S. A. Franklin, S. Chander, D. Nirmal, *et al.*, "Enhancing reliability and RF performance: The impact of Fe doped back barrier optimization in GaN HEMTs," in *2024 7th International Conference on Devices, Circuits and Systems (ICDCS)*, pp. 258–261, IEEE, 2024.

[114] G. P. Rao, T. R. Lenka, and H. P. T. Nguyen, "Field-plated and back-barrier engineered wide-bandgap iii-nitride/β-Ga_2O_3 nano-HEMT for emerging RF/microwave micro/nanoelectronics applications," *Microelectronics Reliability*, vol. 155, p. 115365, 2024.

[115] H. Yu, S. B. Lisesivdin, B. Bolukbas, O. Kelekci, M. K. Ozturk, S. Ozcelik, D. Caliskan, M. Ozturk, H. Cakmak, P. Demirel, *et al.*, "Improvement of breakdown characteristics in AlGaN/GaN/$Al_xGa_{1-x}N$ HEMT based on a grading $Al_xGa_{1-x}N$ buffer layer," *physica status solidi (a)*, vol. 207, no. 11, pp. 2593–2596, 2010.

[116] O. Odabaşı, D. Yılmaz, E. Aras, K. E. Asan, S. Zafar, B. Ç. Akoğlu, B. Bütün, and E. Özbay, "AlGaN/GaN-based laterally gated high-electron-mobility transistors with optimized linearity," *IEEE Transactions on Electron Devices*, vol. 68, no. 3, pp. 1016–1023, 2021.

[117] Y. Durmus, D. Yilmaz, A. Toprak, A. B. Turhan, O. A. Sen, and E. Ozbay, "AlGaN/GaN HEMT with ft: 100GHz and fmax: 128GHz," in *2015 10th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 199–202, IEEE, 2015.

[118] W. Wang, L. Li, L. He, F. Yang, Z. Chen, Y. Zheng, L. He, Z. Wu, B. Zhang, and Y. Liu, "Influence of AlGaN back barrier layer thickness on the dynamic Ron characteristics of AlGaN/GaN HEMTs," in *2016 13th China International Forum on Solid State Lighting: International Forum on Wide Bandgap Semiconductors China (SSLChina: IFWS)*, pp. 77–80, IEEE, 2016.

[119] D. S. Lee, B. Lu, M. Azize, X. Gao, S. Guo, D. Kopp, P. Fay, and T. Palacios, "Impact of GaN channel scaling in InAlN/GaN HEMTs," in *2011 International Electron Devices Meeting*, pp. 19–2, IEEE, 2011.

[120] P. Waltereit, S. Müller, K. Bellmann, C. Buchheim, R. Goldhahn, K. Köhler, L. Kirste, M. Baeumler, M. Dammann, W. Bronner, *et al.*, "Impact of GaN cap thickness on optical, electrical, and device properties in AlGaN/GaN high electron mobility transistor structures," *Journal of Applied Physics*, vol. 106, no. 2, 2009.

[121] A. Hickman, R. Chaudhuri, S. J. Bader, K. Nomoto, K. Lee, H. G. Xing, and D. Jena, "High breakdown voltage in RF AlN/GaN/AlN quantum well HEMTs," *IEEE Electron Device Letters*, vol. 40, no. 8, pp. 1293–1296, 2019.

[122] I. Rossetto, F. Hurkx, J. Šonskỳ, J. A. Croon, G. Meneghesso, E. Zanoni, *et al.*, "Extensive investigation of time-dependent breakdown of GaN-HEMTs submitted to off-state stress," *IEEE Transactions on Electron Devices*, vol. 62, no. 8, pp. 2549–2554, 2015.

[123] M. Meneghini, C. De Santi, I. Abid, M. Buffolo, M. Cioni, R. A. Khadar, L. Nela, N. Zagni, A. Chini, F. Medjdoub, *et al.*, "GaN-based power devices: Physics, reliability, and perspectives," *Journal of Applied Physics*, vol. 130, no. 18, 2021.

[124] P. V. Raja, J.-C. Nallatamby, M. Bouslama, J. C. Jacquet, R. Sommet, C. Chang, and B. Lambert, "HTRB stress effects on 0.15 μm AlGaN/GaN HEMT performance," in *2022 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO)*, pp. 1–4, IEEE, 2022.

[125] P. Klein, S. Binari, K. Ikossi, A. Wickenden, D. Koleske, and R. Henry, "Current collapse and the role of carbon in AlGaN/GaN high electron mobility transistors grown by metalorganic vapor-phase epitaxy," *Applied Physics Letters*, vol. 79, no. 21, pp. 3527–3529, 2001.

[126] C. R. Huang, H. C. Chiu, C. H. Liu, H. C. Wang, C. W. Chiu, H. L. Kao, C. T. Chen, and K. J. Chang, "Electrical and thermal performance analysis of AlGaN/GaN HEMT without voltage-blocking buffer layer design," in *37th International Conference on Compound Semiconductor Manufacturing Technology, CS MANTECH 2023*, 2023.

[127] D.-Y. Chen, A. Malmros, M. Thorsell, H. Hjelmgren, O. Kordina, J.-T. Chen, and N. Rorsman, "Microwave performance of 'buffer-free' GaN-on-SiC high electron mobility transistors," *IEEE Electron Device Letters*, vol. 41, no. 6, pp. 828–831, 2020.